Compal Confidential

CSL50/CSL52 Schematics Document

Sky Lake-U(2+2)-DDR4 SODIMMx2

GPU AMD R17M-M1-30

R17M-M2-50

(DDR3L 4GB)

Date : 2018-01-08 REV : 1.0

SecurityClassification	Compal Secret Data		
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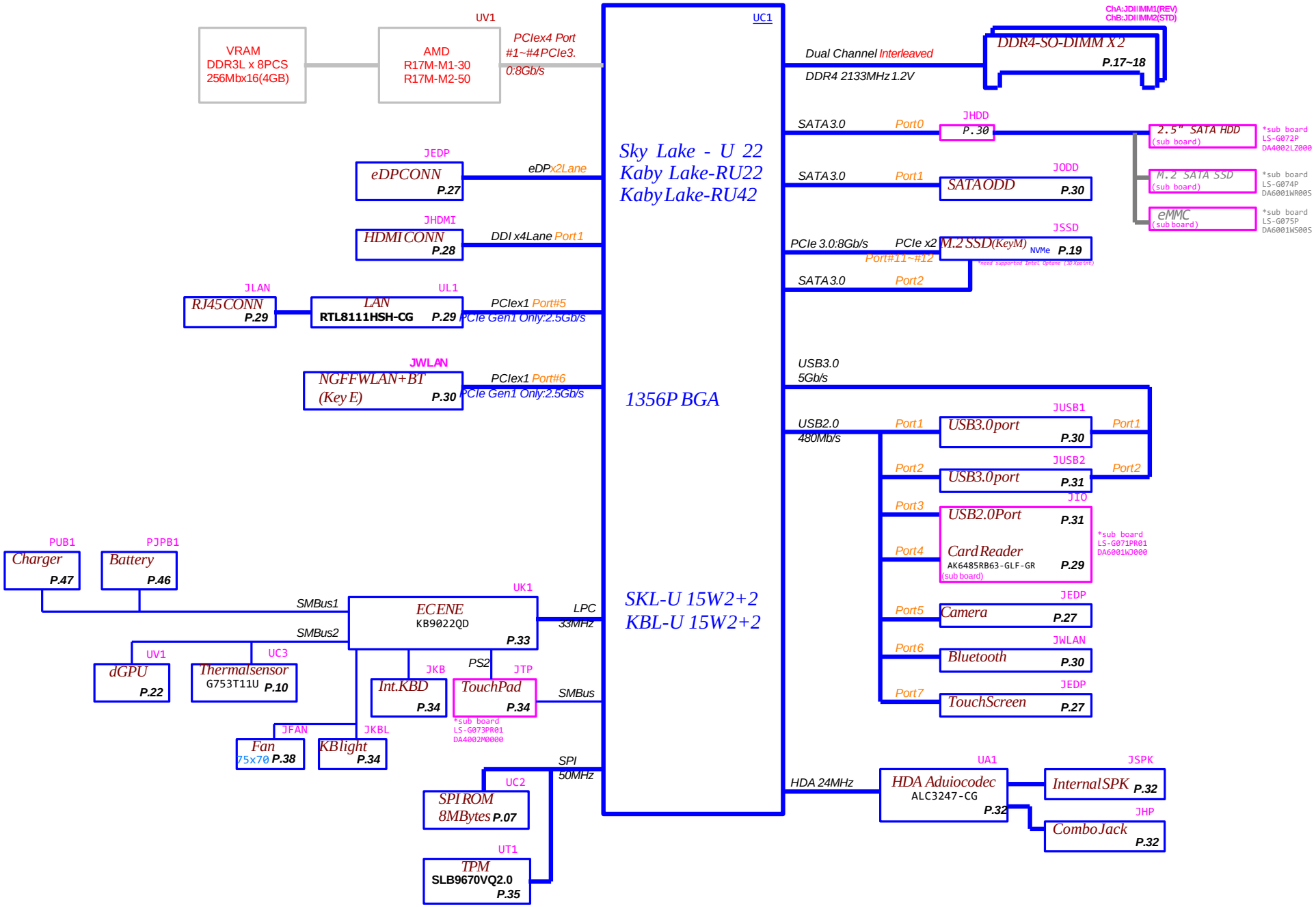
Compal Electronics, Inc.			
Title: Cover Page			
Size: Custom	Document Number: CSL50 / CSL52		Rev: v0.3
Date: Monday, January 08, 2018		Sheet 1 of 59	



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Block Diagrams

Document Number: CSL50 / CSL52

Rev: v0.3

Custom

Date: Monday, January 08, 2018

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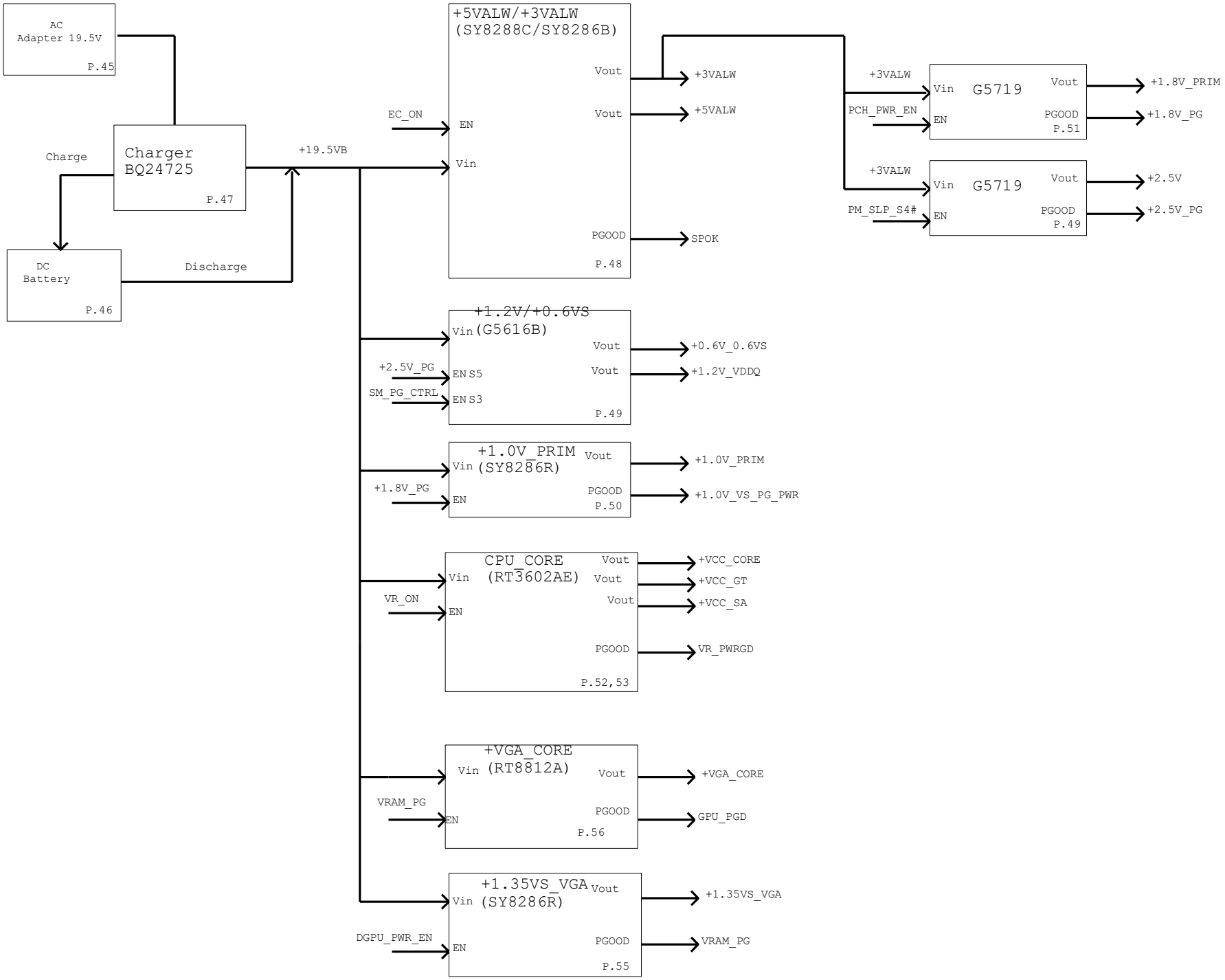

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *Power Block Diagram*

Size: Document Number: CSL50 / CSL52 Rev: 0.3

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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW _EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

BOM Structure Table (1/2)

Function	*Stuff*	*Un-Stuff*
DGPU SKU	PX@	
UMA SKU	UMA@	
TPM	TPM@	

SOC SMBUS Address Table

SOC_SMBUS NetName	Power Rail	Device	Address(7bit)	Address(8bit) Write	Address(8bit) Read
SMBCLK SMBDATA	+3V_PRIM	DIMM1	0x50	0xA0	0xA1
		DIMM2	0x52	0xA4	0xA5
		TouchPAD	0x2C	0x58	0x59

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address(7bit)
SMBUS Port1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port2	+3VS	dGPU	
		Thermal Sensor	0x90
		PCH	

Power State

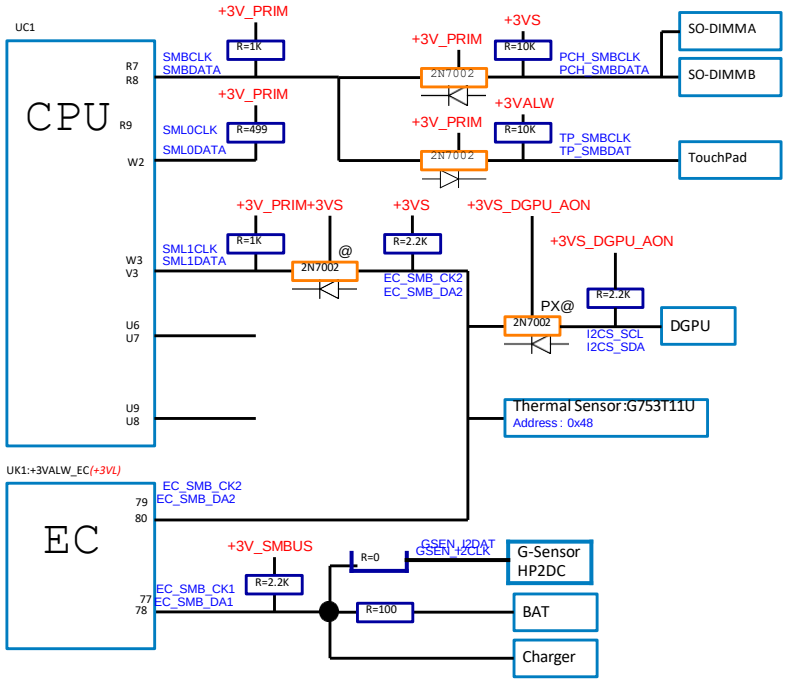
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (FullON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (SuspendtoRAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (SuspendtoDisk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SoftOFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

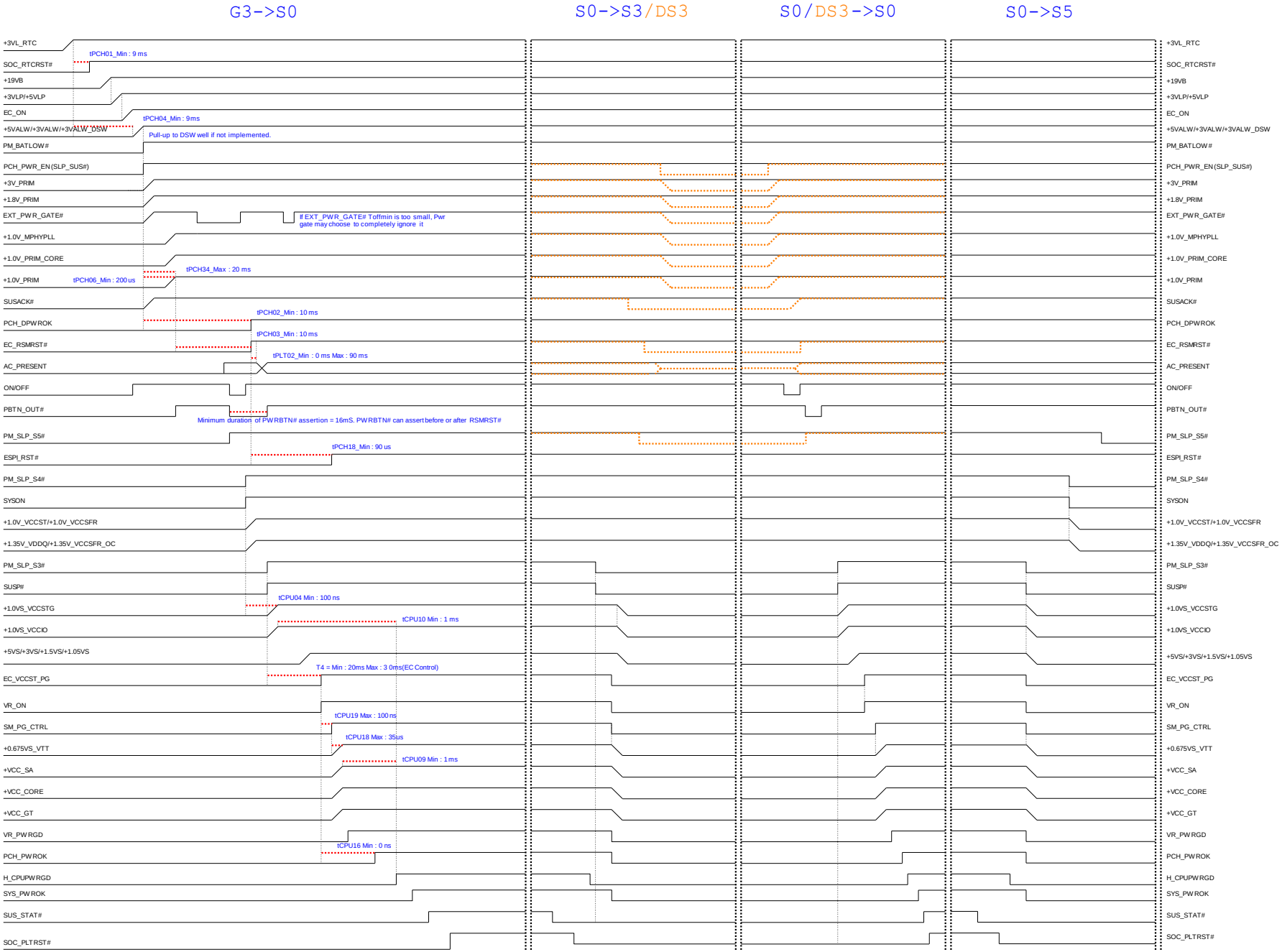
USB2.0port	DESTINATION
1	USB3.0 Type-C
2	USB2.0/USB3.0
3	USB2.0/USB3.0
4	BT
5	HD/IR_1/IR_2 Camera
6	IR_2 Camera
7	Card Reader
8	X
9	X
10	X

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0		DESTINATION	CLK
1				1	USB3.0 Type-C	X
2				2	USB3.0 Type-C	X
3				3	USB2.0/USB3.0	X
4				4	USB2.0/USB3.0	X
5	1			5	GPU(DISonly)	CLK0
6	2			6	GPU(DISonly)	
7	3				GPU(DISonly)	
8	4				GPU(DISonly)	
9	5				LAN	CLK1
10	6				WLAN	CLK2
11	7	0			HDD	X
12	8	1a			ODD	CLK3
13	9				X	X
14	10				X	X
15	11	1b*			NVMe x2 SATASSD	CLK4
16	12	2				X



[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]



SecurityClassification	Compal Secret Data		Compal Electronics, Inc.
IssuedDate		DecipheredDate	Title: HW Reserve
Size: Custom	Document Number: CSL50 / CSL52		Rev: v0.3
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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

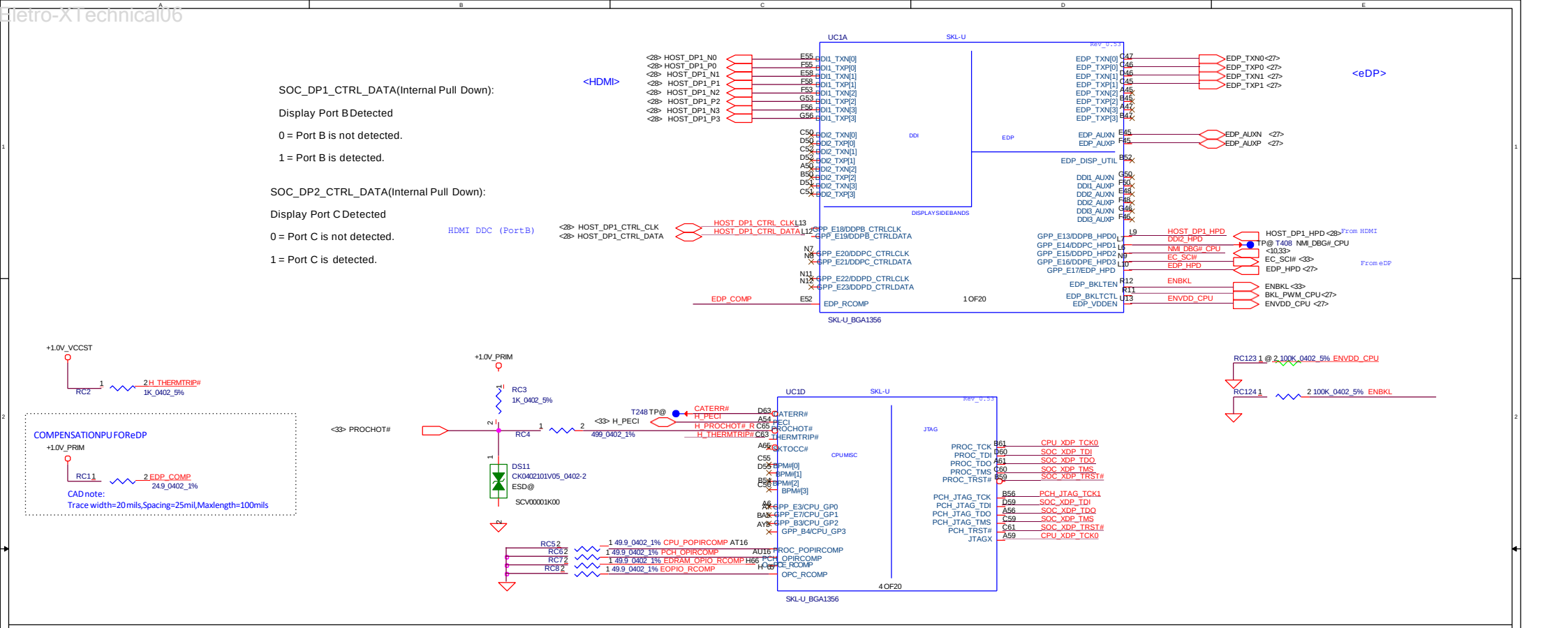
1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.



XDP CONN

Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Decipher Date	2019/12/15

Compal Electronics, Inc.	
Title	SKL-U(1/12)DDI,MSIC,XDP,EDP
Size: Custom	Document Number: CSL50 / CSL52
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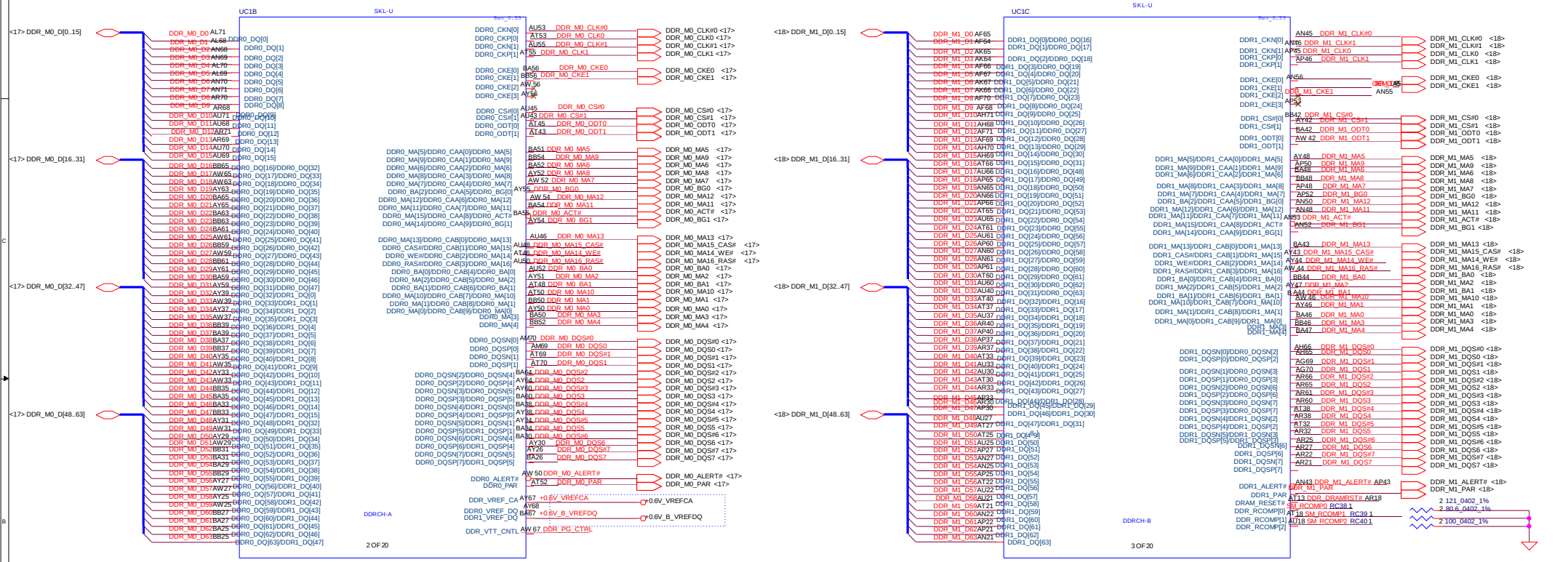
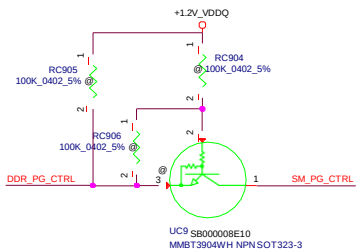
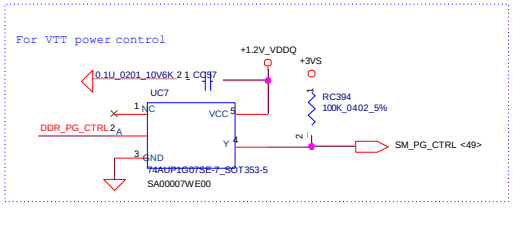
Interleaved Memory

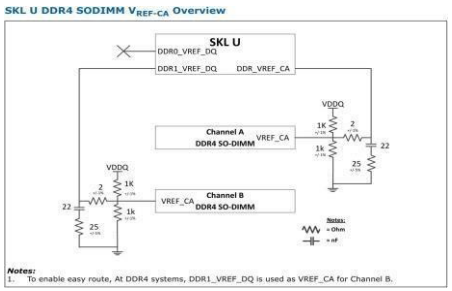
Interleaved Memory

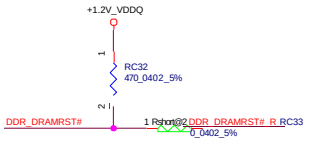
<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)











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Compal Electronics, Inc.	
Title	SKL-U(2/12)DDRIII
Size	Document Number: CSL50 / CSL52
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Eletro-XTechnical07

SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use 1
= eSPI is selected for EC --> For KB9032 Only.

UC1E
SKL-U
SPI-FLASH
SMBUS,SMLINK
SPI-TOUCH
LPC
CLINK
5 OF 20
SKL-U_BGA1356

<35> HOST_SPI_0_SO
<35> HOST_SPI_0_SI
HOST_SPI_0_CLK AV2 SPI0_CLK
HOST_SPI_0_SO AW3 SPI0_MISO
HOST_SPI_0_SI AV3 SPI0_MOSI
HOST_SPI_0_SIO2 AW2 SPI0_IO2
HOST_SPI_0_SIO3 AU4 SPI0_IO3
HOST_SPI_0_CS0# AU3 SPI0_CS0#
AU2 SPI0_CS1#
<35> HOST_SPI_0_CS2#
HOST_SPI_0_CS2# AU1 SPI0_CS2#

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C8 CL_CLK
C7 CL_DATA
G1 CL_RST#

GPP_C0/SMBCLK R7 SMBCLK
GPP_C1/SMBDATA R8 SMBDATA
GPP_C2/SMBALERT# R10 SMBALERT# TP@T239
GPP_C3/SML0CLK R9 SML0CLK
GPP_C4/SML0DATA W2 SML0DATA
GPP_C5/SML0ALERT# W1 SML0ALERT#
GPP_C6/SML1CLK W3 SML1CLK
GPP_C7/SML1DATA V3 SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23 1 2 SML1ALERT#
RC902 @ 0 0201 5% TP@T234

SMB (Link to XDP, DDR, TP)
SML1 (Link to EC,DGPU, LAN, Thermal Sensor)

SML0ALERT# RC218 1K_0402_1%
SML1ALERT# RC903 2 @ 1 150K_0402_1%
SML0ALERT# RC360 2 @ 1 10K_0402_5%
SMBALERT#
EC_KBRST#
RPC19 10K_0804_8P4R_5%
+3V_PRIM
+3VS

<33> EC_KBRST# EC_KBRST# AW13 GPP_A0/RCIN#
To TPM <33,35> SERIRQ SERIRQ AY11 GPP_A6/SERIRQ
LPC Mode

GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0 LPC_AD0 <33>
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1 LPC_AD1 <33>
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2 LPC_AD2 <33>
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3 LPC_AD3 <33>
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# LPC_FRAME# <33>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 SUS_STAT# TP@ T2402

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI0 RC387 1 2 22_0402_5% CLK_PCI_LPC <33>
GPP_A10/CLKOUT_LPC1 AV9
GPP_A8/CLKRUN# AW11 PM_CLKRUN# PM_CLKRUN# <33>
CC182 22P 50V J NPO 0402 EMI@
To EC

To SPI ROM/UC2 SourceFrom
RPH11
HOST_SPI_0_CS0#_R 1 8 EC_SPI_CS0#
HOST_SPI_0_CS0#_R 2 7 HOST_SPI_0_CS0#
HOST_SPI_0_SO_R 3 6 EC_SPI_SO
HOST_SPI_0_SO_R 4 5 HOST_SPI_0_SO
15_0804_8P4R_5%
EC_SPI_CS0# <33>
EC_SPI_SO <33>

RPH12
HOST_SPI_0_HOLD# 1 8 HOST_SPI_0_SIO3
HOST_SPI_0_SI_R 2 7 HOST_SPI_0_SI
HOST_SPI_0_SI_R 3 6 EC_SPI_SI
15_0804_8P4R_5%
EC_SPI_SI <33>

HOST_SPI_0_WP# 2 RC388 15_0402_5% 1 HOST_SPI_0_SIO2

SPI ROM (8MByte Only)
+3V_SPI
CC8 1 2 0.1U_0201_10V6K
UC2
HOST_SPI_0_CS0#_R 1 CS# VCC 8 HOST_SPI_0_HOLD#
HOST_SPI_0_SO_R 2 DO(IO1) HOLD#(IO3) 7 HOST_SPI_0_CLK_R
HOST_SPI_0_WP# 3 P#(IO2) CLK 6 HOST_SPI_0_SI_R
GND DI(IO0) 5
XM25QH64AHIG SOP 8P
SA00000B8300 SPI ROMPart: SA00000B8300, S IC FL 64M XM25QH64AHIG SOP 8P(XMC)
ACES_91960-0084L_8P-T 2nd: SA00000B9A40, S IC FL 64M W25Q64JVSSIQ SOIC 8P SPI ROM(Winbond)
3th: SA00000B5L00, S IC FL 64M MX25L6473FMQI-08G SOP 8P(MXIC)
Use socketfootprint

+3VS
RC216 10K_0402_5%
RC215 10K_0402_5%
QC1A
SMBCLK 6
L2N7002SDW1T1G 2NSC88-6
SB00001FF00
PCH_SMBCLK <17,18>
QC1B
SMBDATA
PCH_SMBDATA <17,18>

+3V_PRIM
SML0CLK RC49 1 2 499_0402_1%
SML0DATA RC50 1 2 499_0402_1%
RPC7
SML1CLK 1 8
SML1DATA 2 7
SMBCLK 3 6
SMBDATA 4 5
1K_0804_8P4R_5%

+3V_SPI
HOST_SPI_0_SIO2 RC3901 @ 2 1K_0402_1%
HOST_SPI_0_SIO3 RC3911 @ 2 1K_0402_1%
HOST_SPI_0_CS0#_R 1 @ 2 RC357 1K_0402_5%

+3VS
<DB> Un-pop QC2 for new 0x90 thermal sensor
SML1CLK
QC2A
L2N7002SDW1T1G 2NSC88-6
SB00001FF00
EC_SMB_CK2 <10,33>
SML1DATA
QC2B
EC_SMB_DA2 <10,33>

+3V_PRIM
+3VALW
RC81 10K_0402_5%
RC82 10K_0402_5%
SB00001FF00
SMBCLK 1
QC7A
L2N7002SDW1T1G 2NSC88-6
TP_SMBCLK <34>
SMBDATA
QC7B SB00001FF00
TP_SMBDATA <34>

HOST_SPI_0_SIO3 RC51 1 ES@ 2 1K_0402_1%
From WW36 MOW for SKL-U ES sample

+3VS_PGPPA
PM_CLKRUN# RC107 1 2 8.2K_0402_5%
SERIRQ RC122 1 2 8.2K_0402_5%

Follow 543016_SKL_U_Y_PDG_0_9

CLK Source CPU to SPI ROM/UC2 & EC
HOST_SPI_0_CLK 2 RC368 15_0402_5% 1 HOST_SPI_0_CLK_R
HOST_SPI_0_CLK_R <33,35>
CC9 10P_0402_50V8J @EMI@

ECN SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P MXIC
SA00006N100 S IC FL 64M MX25L6473EM2I-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64VSSIQ SOIC 8P SPI ROM
Micron SA00005L100 S IC FL 64M N25Q064A13ESEC0FSO8W8P

ENE Fixed Code Block Diagram
CPU
EC
SPI_ROM
M:Master
S : Slave
O : Output
I : Input

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Issued Date	2017/04/10	DecipheredDate	2019/12/15

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Title: SKL-U(3/12)SPI,ESPI,SMB,LPC
Size: Custom
Document Number: CSL50 / CSL52
Rev: v0.3
Date: Friday, January 05, 2018
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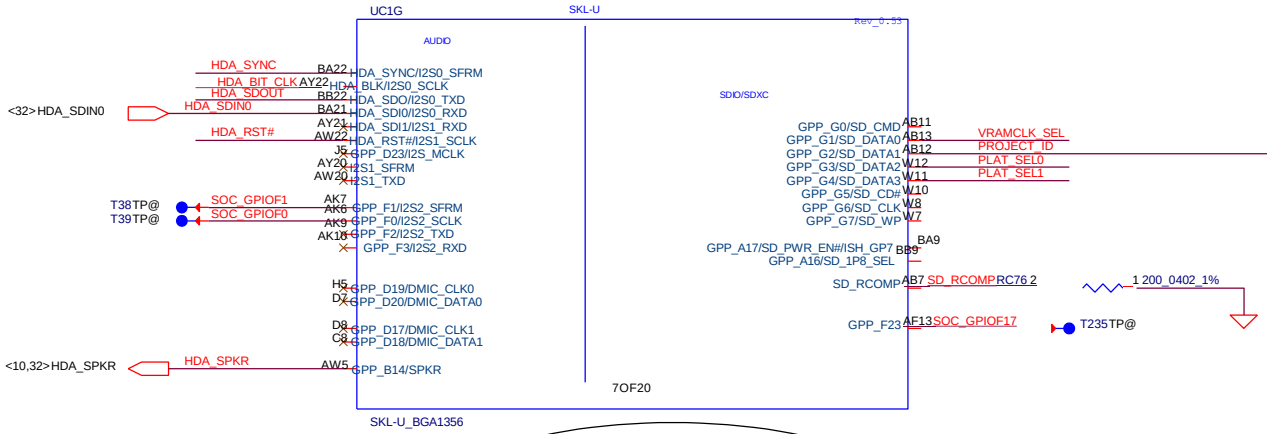
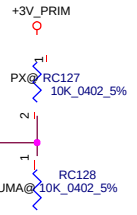
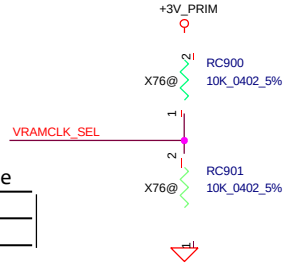




	UMA	DIS
PROJECT_ID	0	1

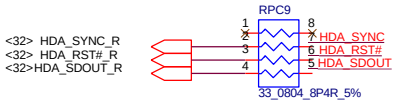
	2G VRAM	4G VRAM
VRAM Clock	0	1

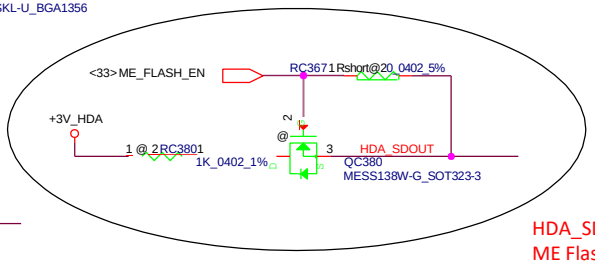


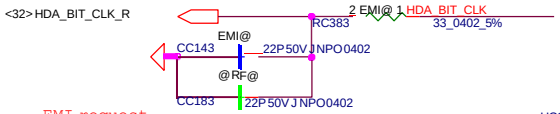
X76 BOM control RAM size

Net Name	4G	2G
VRAMCLK_SEL	1	0

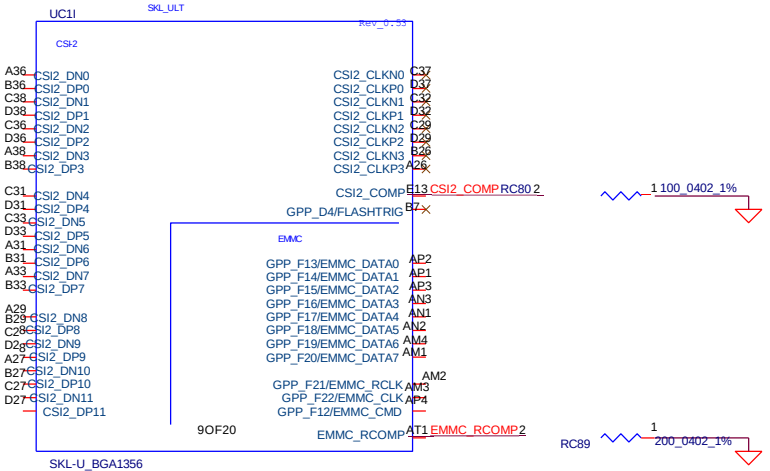
HDA for AUDIO

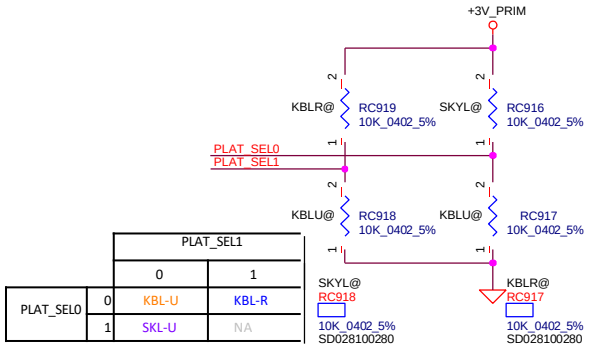






HDA_SDOUT:
ME Flash Descriptor Security Override
Low : Disabled(Default)
High : Enabled





PLAT_SEL0	PLAT_SEL1 = 0	PLAT_SEL1 = 1
0	KBL-U	KBL-R
1	SKL-U	NA

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Compal Electronics, Inc.			
Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2			
Size: Custom	Document Number: CSL50 / CSL52		Rev: v0.3
Date: Friday, January 05, 2018		Sheet 8 of 59	

RTCVCC

RC91 1 2 20K_0402_5% PCH_SRTCRST#
CC10 1 2 1U_0402_6.3V6K
CLRP1 1 2 SHORT PADS CLR_ME
RC93 1 2 20K_0402_5% PCH_RTCRST#
CC11 1 2 1U_0402_6.3V6K
CLRP2 1 2 SHORT PADS CLR_CMOS
RC941 2 1M_0402_5% SM_INTRUDER#

PCH_RTCRST# 2 0_0402_5% 1 R1088 CLR_CMOS# <33>
PCH_SRTCRST# 2 0_0402_5% 1 R1089
JCMOS1 1 2 0_0603_5% Clear CMOS close to RAM door

+3VS
RC165 1 2 CLKREQ_PCIE#4 10K_0402_5%
RC105 1 2 CLKREQ_PCIE#5 10K_0402_5%
From 545659_SKL_PCH_U_Y_EDS_R0_7
<Cocoa_1027>
check un use GPIO for termination guidance
RPC10 10K_0804_8P4R_5%
8 1 CLKREQ_PCIE#1
7 2 CLKREQ_PCIE#2
6 3 CLKREQ_PCIE#0
5 4 CLKREQ_PCIE#3

UC1J SKL_ULT
CLOCKSIGNALS
D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
CLKREQ_PEG#0
LAN <29> CLK_PCIE_N1 <29> CLK_PCIE_P1 <29> CLKREQ_PCIE#1
CLK_PCIE_N1 B42 CLKOUT_PCIE_N1
CLK_PCIE_P1 A42 CLKOUT_PCIE_P1
CLKREQ_PCIE#1 AT7 GPP_B6/SRCCLKREQ1#
W LAN <30> CLK_PCIE_N2 <30> CLK_PCIE_P2 <30> CLKREQ_PCIE#2
CLK_PCIE_N2 D41 CLKOUT_PCIE_N2
CLK_PCIE_P2 C41 CLKOUT_PCIE_P2
CLKREQ_PCIE#2 AT8 GPP_B7/SRCCLKREQ2#
CLKREQ_PCIE#3
PCIe SSD <31> CLK_PCIE_N4 <31> CLK_PCIE_P4 <31> CLKREQ_PCIE#4
CLK_PCIE_N4 B40 CLKOUT_PCIE_N4
CLK_PCIE_P4 A40 CLKOUT_PCIE_P4
CLKREQ_PCIE#4 AU8 GPP_B9/SRCCLKREQ4#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
E40 CLKOUT_PCIE_N5
E38 CLKOUT_PCIE_P5
CLKREQ_PCIE#5 AU7 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17 SUSCLK SUSCLK <30>
XTAL24_IN E37 PCH_KBLU24_IN
XTAL24_OUT E35 PCH_KBLU24_OUT
XCLK_BIASREF E42 XCLK_BIASREF RC96 1 2 2.7K_0402_1% +1.0V_CLK5_F24NS
RTCX1 AM18 PCH_RTCX1
RTCX2 AM20 PCH_RTCX2
SRTCRST# AN18 PCH_SRTCRST#
RTCRST# AM16 PCH_RTCRST#
10 OF 20
SKL-U_BGA1356

XCLK_BIASREF RC97 1 @ 2 60.4_0402_1%

<DB> Add RX1~4 for KBL U/R Colay
Change XTAL(YC1) to 2016Type

PCH_KBLU24_IN RX1 KBLU@ 1 33_0402_1% PCH_XTAL24U_IN
PCH_KBLU24_OUT RX2 KBLU@ 1 33_0402_1% PCH_XTAL24U_OUT
RC92 KBLU@ 1M_0402_5%
YC1 KBLU@ 24MHZ 18PF XRCGB24M000F2P51R0
NC NC
CC12 KBLU@ 8.2P_0402_50V
CC13 KBLU@ 27P_0402_50V
SJ10000J300

PCH_RTCX2
PCH_RTCX1
RC98 1 2 1M_0402_5%
YC2 32.768KHZ 9PF 10PPM 9H03200055
SJ10000Q800
CC15 6.8P_50V_C_NPO_0402 SE07168AC80
CC16 6.8P_50V_C_NPO_0402 SE07168AC80
<SI> CC15/CC16 SI change 3.9p=>6.8p

+3VALW_DSW
+3V_PRIM
RC925 1 2 PCH_PWROK 10K_0402_5%
RC926 1 2 LAN_WAKE# 10K_0402_5%
RC927 1 2 PCH_RSMRST# 10K_0402_5%
RC928 1 2 SYS_RESET# 10K_0402_5%

PCH PLTRST Buffer
RC99 1 2 0_0402_5%
+3VS @ CC145 1 2 0.1U_0201_10V6K
@ UC8 SN74AHC1G08DCKR_SC70-5
PLT_RST#_PCH
PLT_RST# PLT_RST# <29,30,31,33,35>

DS12 2 1 PCH_PWROK CK0402101V05_0402-2 ESD@ SCV00001K00

CLRP3 2 1 SYS_RESET# SHORT PADS
RC100 1 @ 2 SUSCLK 1K_0402_5%
RC101 2 1 PCH_DPWROK 100K_0402_5%

+3VALW_DSW
RC103 1 2 8.2K_0402_5% PM_BATLOW#
RC104 1 2 1K_0402_5% WAKE#
RC106 1 @ 2 10K_0402_5% AC_PRESENT_R

+3V_PRIM
RC1151@ 2 10K_0402_5% SOC_VRALERT#
+3VALW_DSW
RC111 2 @ 1 100K_0402_5% PBTN_OUT#

Only For Power Sequence Debug

UC1K SKL-U
SYSTEMPOWERMANAGEMENT
PLT_RST# PCH AN10 GPP_B13/PLTRST#
SYS_RESET# B5 SYS_RESET#
T296 TP@ PCH_RSMRST# AY17 RSMRST#
RC102 1 @ 2 1K_0402_5% H_CPUPWRGD A68 PROCPW RGD
EC_VCCST_PG B65 VCCST_PWRGD
<33> SYS_PWROK <33> PCH_PWROK
SYS_PWROK B6 SYS_PWROK
PCH_PWROK BA20 PCH_PWROK
PCH_DPWROK_R BB20 DSW_PWROK
2 Rshort@ 1 RC110 0_0402_5% <33> PCH_SUSWARN#
PCH_SUSWARN# AR13 GPP_A13/SUSWARN#/SUSPWRDNACK
<33> SUSACK# SUSACK#_R AP11 GPP_A15/SUSACK#
<30> WAKE# WAKE# BB15 GPP_A14/WAKE#
LAN_WAKE# AM15 GPD2/LAN_WAKE#
AW17 GPD11/LANPHYPC
AT15 GPD7/RSVD
T94 TP@
11 OF 20
SKL-U_BGA1356

GPP_B12/SLP_S0# AT11 PM_SLP_S0#
GPD4/SLP_S3# AP15 PM_SLP_S3#
GPD5/SLP_S4# BA16 PM_SLP_S4#
GPD10/SLP_S5# AY16 PM_SLP_S5#
PM_SLP_S3# <12,33,40>
PM_SLP_S4# <12,33,40,49>
PM_SLP_S5# <33>
SLP_SUS# AN15 PM_SLP_SUS#
PM_SLP_SUS# <33>
SLP_LAN# AW15
GPD9/SLP_WLAN# BB17
GPD6/SLP_A# AN16 PM_SLP_A#
GPD3/PWRBTN# BA15 PBTN_OUT#
PBTN_OUT#<33>
GPD1/ACPRESENT AV15 AC_PRESENT_R
GPD0/BATLOW# AU13 PM_BATLOW# RC108 0_0402_5% ACIN <33>
GPP_A11/PME# AU11 EC_PCIE_W AKE#_CPU
INTRUDER# AP16 SM_INTRUDER#
RC922 2 @ 1 0_0402_5% EC_PCIE_W AKE# <30,33>
GPP_B11/EXT_PWR_GATE# AM11 SOC_VRALERT#
GPP_B2/VRALERT# AM10 EXT_PWR_GATE#
TP@T298

TP@T254
TP@T255
TP@T256
TP@T257
TP@T258

DS13 ESD@ SCV00001K00 1 2 H_CPUPWRGD CK0402101V05_0402-2
DS14 @ESD@ SCV00001K00 1 2 SUSACK# CK0402101V05_0402-2
ESD@ C5229 1 2 SYS_PWROK 0.1U_0402_25V6

DC3 SCS00000Z00 RB751V-40 SOD-323
PCH_RSMRST# 1 2 PCH_PWROK
DC4 2 1 SCS00000Z00 RB751V-40 SOD-323 SPOK <48>
<33> PCH_DPWROK 2 RC112 Rshort@ 1 0_0402_5% PCH_DPWROK_R

From EC (open-drain)
+1.0V_VCCST
RC113 1K_0402_5%
<33,40> EC_VCCST_PG_R RC1161 2 60.4_0402_1% EC_VCCST_PG

Security Classification	Compal Secret Data		
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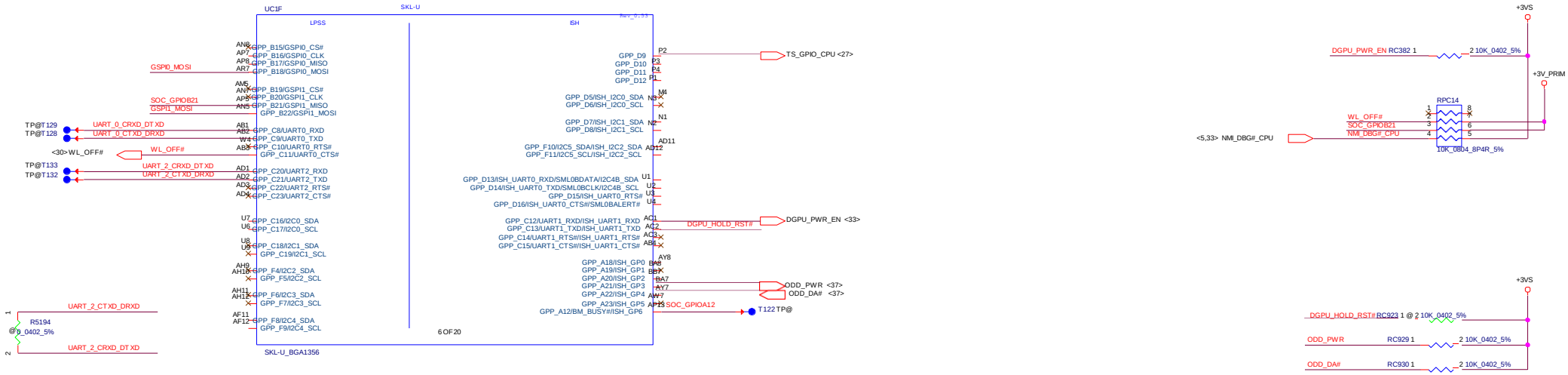
Compal Electronics, Inc.
Title: SKL-U(5/12)CLK,GPIO
Size: Custom
Document Number: CSL50 / CSL52
Rev: v0.3
Date: Friday, January 05, 2018
Sheet: 9 of 59



Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

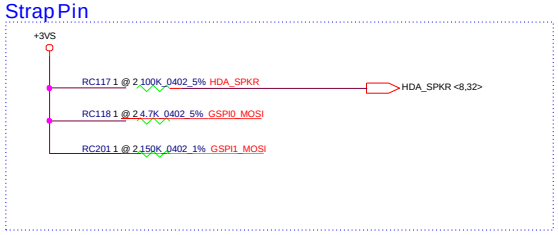
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

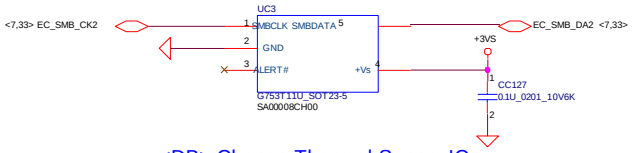
1 = LPC Mode

Strap Pin



CPU THERMAL SENSOR

Address : 0x48



<DB> Change Thermal Sensor IC

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Title	Compal Electronics,Inc.
	SKL-U(6/12)GPIO
Size: Custom	Document Number: CSL50 / CSL52
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Date: Friday, January 05, 2018	Sheet 10 of 59

UC1H

SKL-U

Rev_0.53

PCIE/USB3/SATA

SSIC / USB3

USB2

LAN

WLAN

HDD

ODD

M.2 SSD

USB2.0/USB3.0

USB2.0/USB3.0

USB2.0/USB3.0

USB2.0

CardReader

Camera

BT

TS

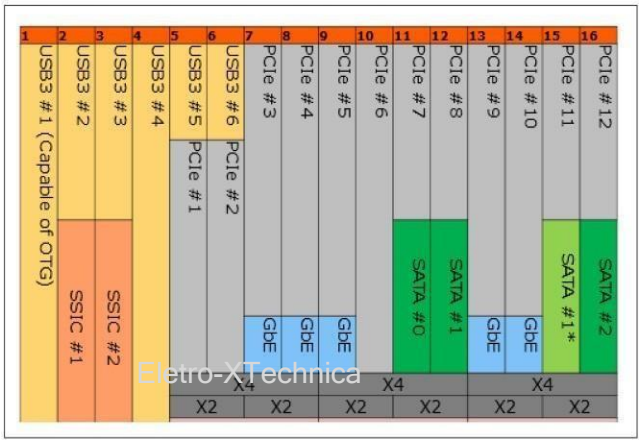
8OF20

SKL-U_BGA1356

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
						Cycle Router #2				Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3		RP5				RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5				RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6			RP9	RP10	RP11	RP12
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port2
USB_OC1#	USB2 Port 3
USB_OC2#	N/A
USB_OC3#	N/A
DEVSLP0	N/A
DEVSLP1	N/A
DEVSLP2	NGFF SSD KEY-M
SATA_GP0	N/A
SATA_GP1	ODD_PLUG#
SATA_GP2	PCIE/SATA

SecurityClassification	Compal Secret Data		
IssuedDate	2017/04/10	DecipheredDate	2019/12/15

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Title: SKL-U(7/12)PCIE,USB,SATA

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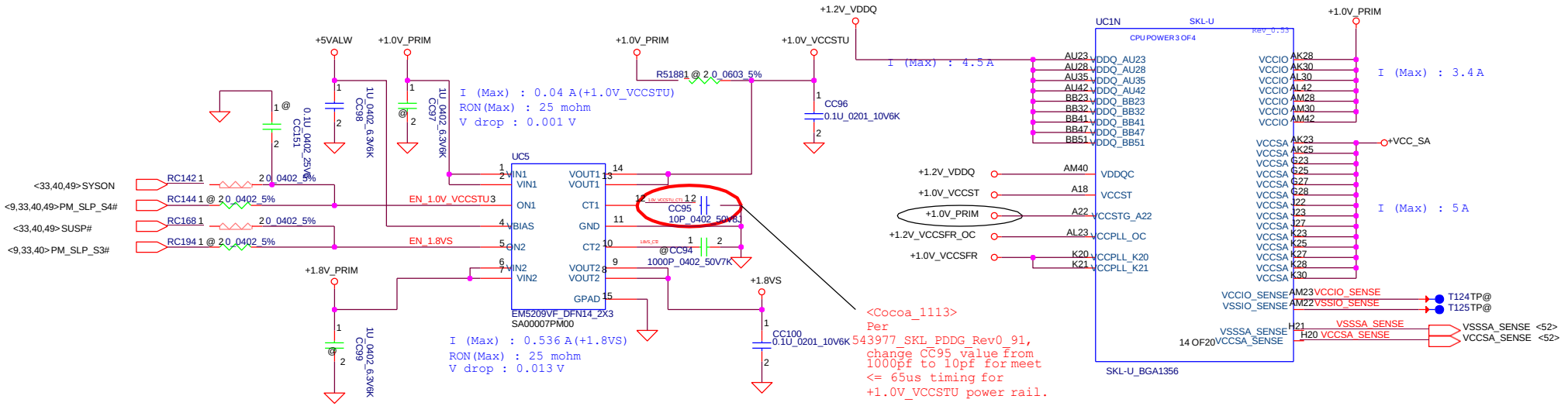
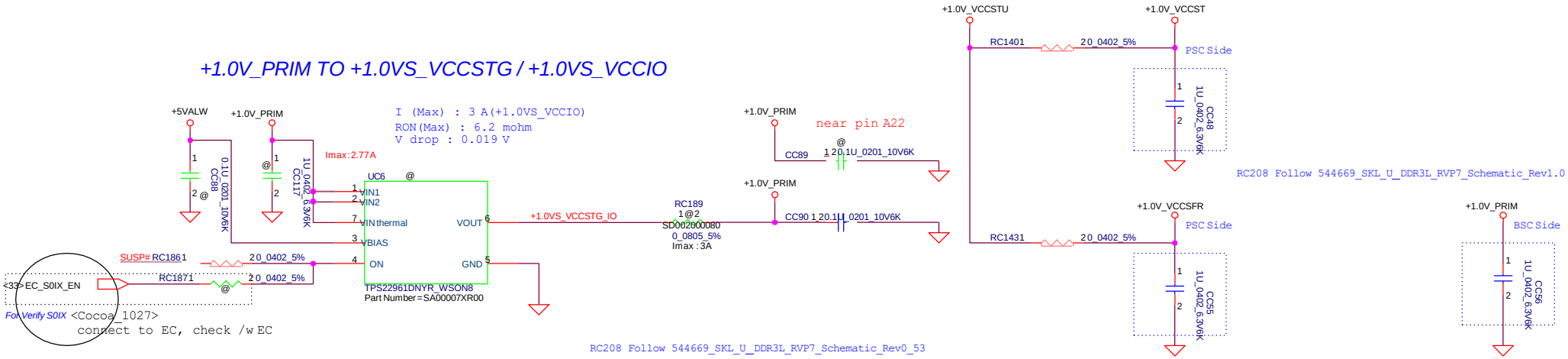
Date: Friday, January 05, 2018 | Sheet 11 of 59

+1.0V_PRIM TO +1.0V_VCCSTU

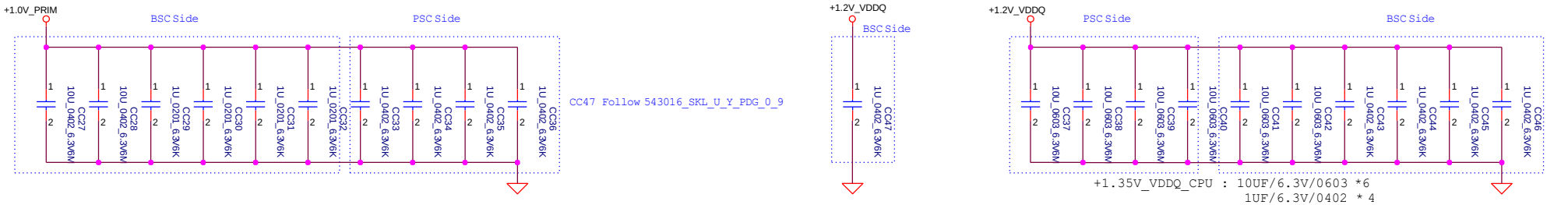


<Cocoa_1113>
Per 543977_SKL_PDDG_Rev0_91, change CC95 value from 1000pf to 10pf for meet <= 65us timing for +1.0V_VCCSTU power rail.

+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO



RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev0_53



+1.35V_VDDQ_CPU : 10UF/6.3V/0603 *6
1UF/6.3V/0402 * 4

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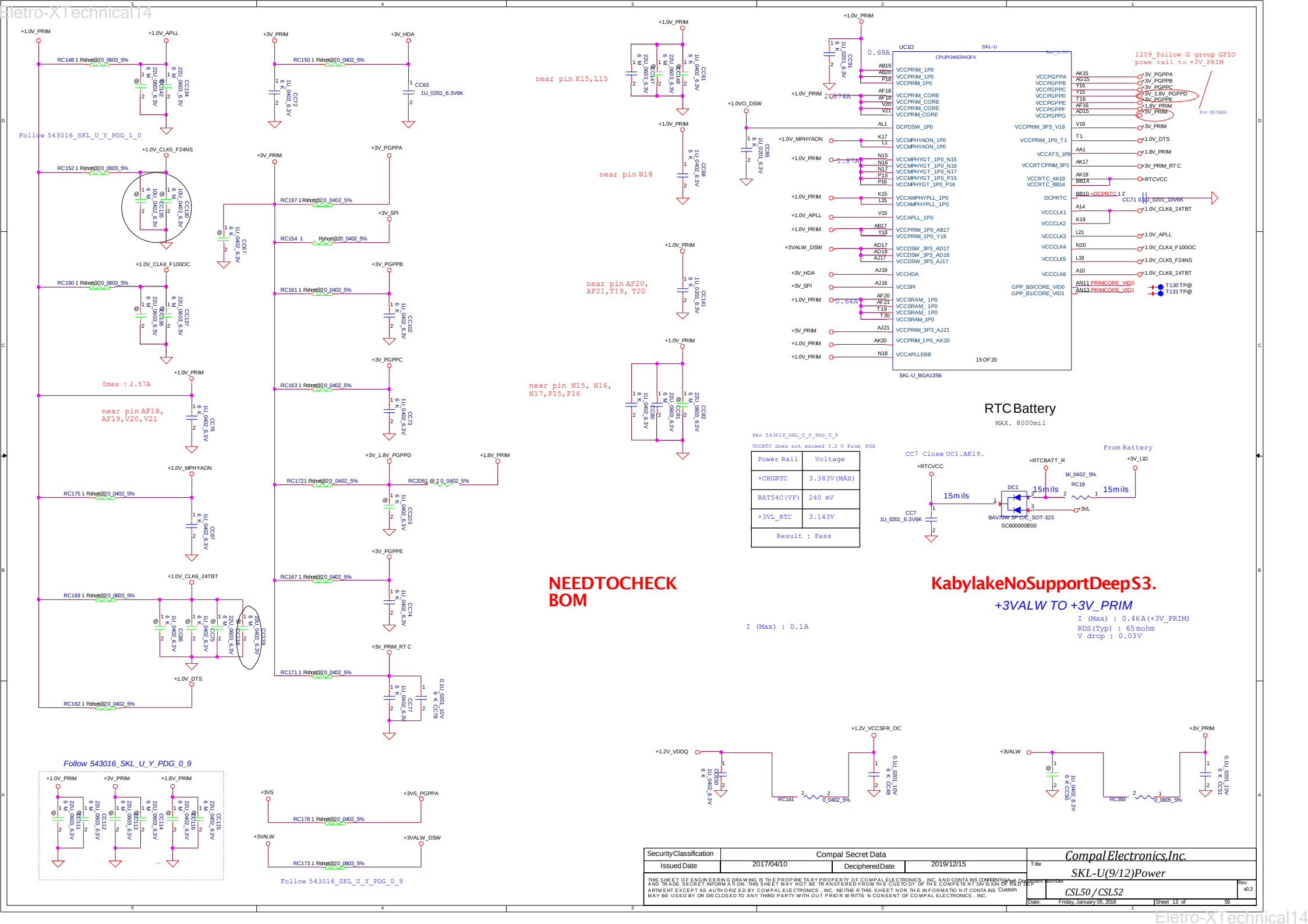
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.			
Title	SKL-U(8/12)Power		
Size: Custom	Document Number: CSL50 / CSL52		Rev: v0.3
Date: Friday, January05, 2018	Sheet 12 of 59		



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Title	Compal Electronics,Inc.
	SKL-U(9/12)Power
Document Number	CSL50 / CSL52
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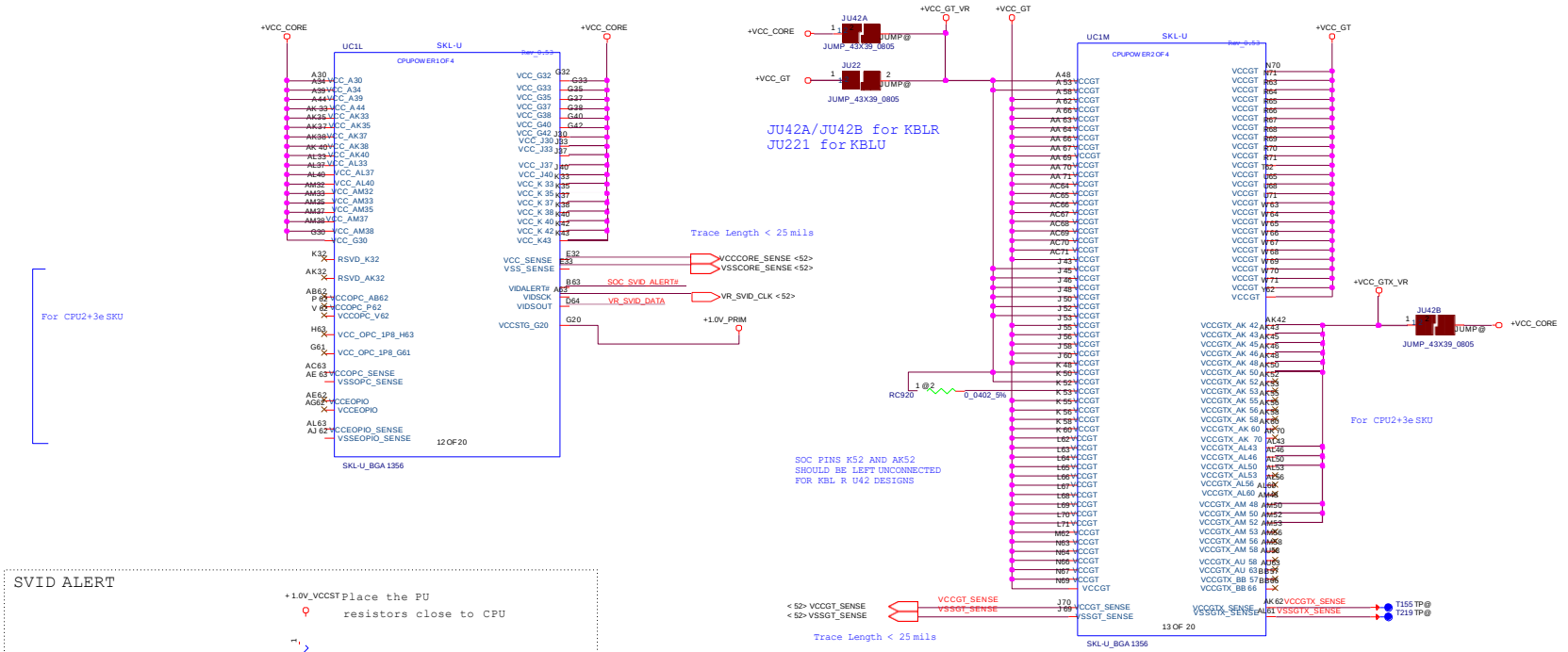
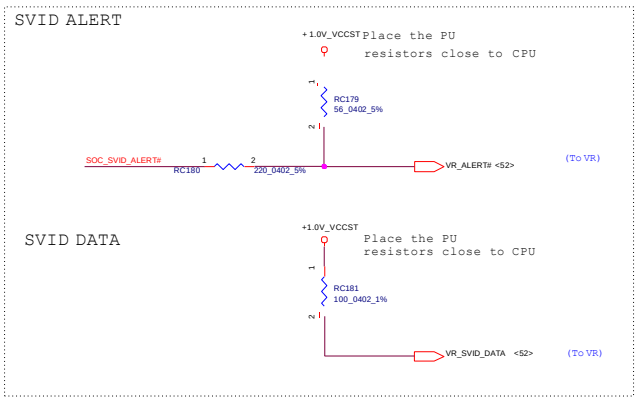
Date: Friday, January 05, 2018	Sheet 13 of 59





Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E35	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL43	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGT/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
A53	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected**. RVP use this signal for debug and testing purpose only.

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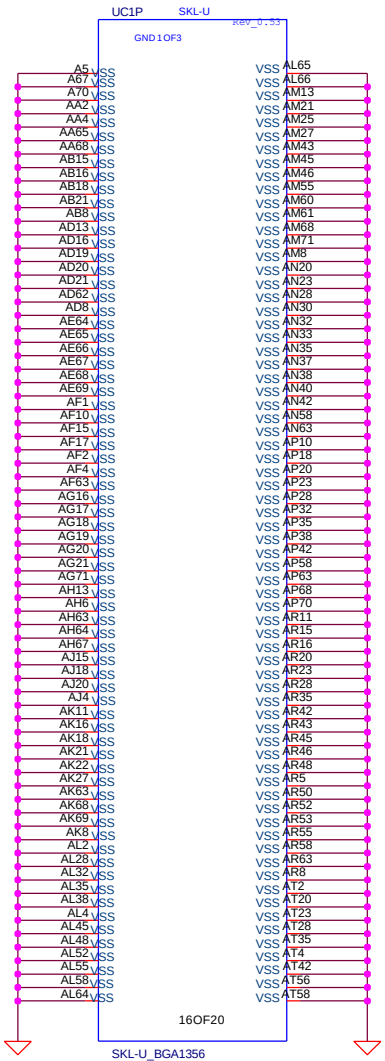
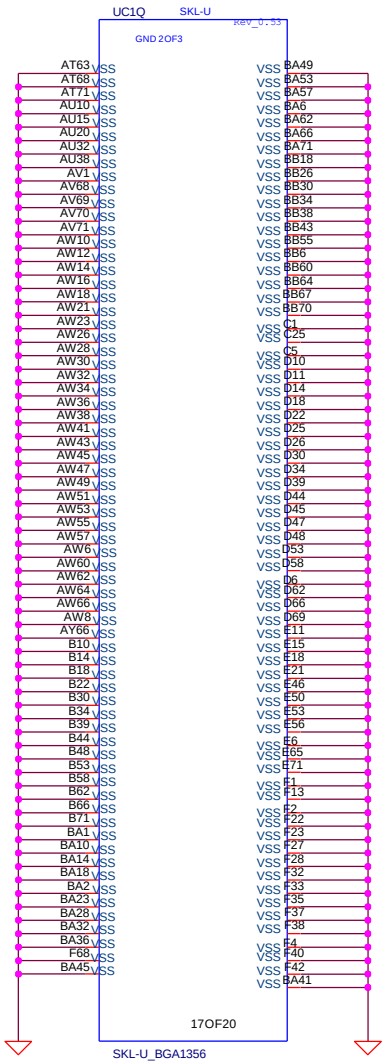
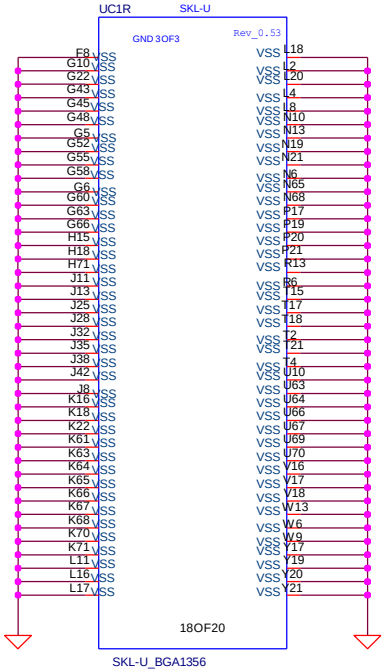
Title	SKL-U(10/12)Power,SVID		
Size: D Custom	Document Number CSL50 / CSL52		Rev 0.3
Date: Friday, January 05, 2018	Sheet 14 of 59		







Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.	
Title	SKL-U(11/12)GND
Size	Document Number: CSL50 / CSL52
Rev	v0.3
Date:	Friday, January 05, 2018
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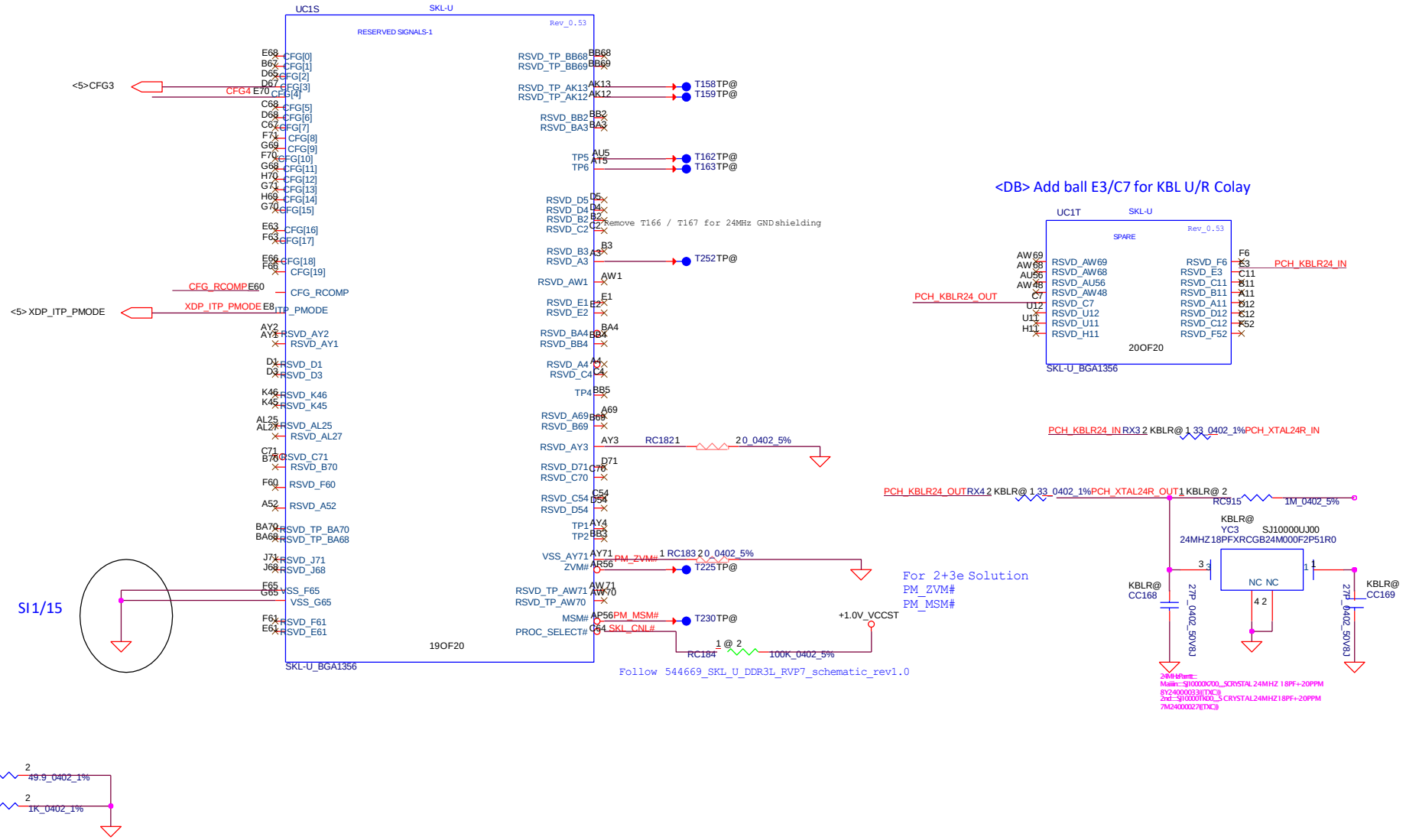

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size: Custom | Document Number: CSL50 / CSL52 | Rev: v0.3

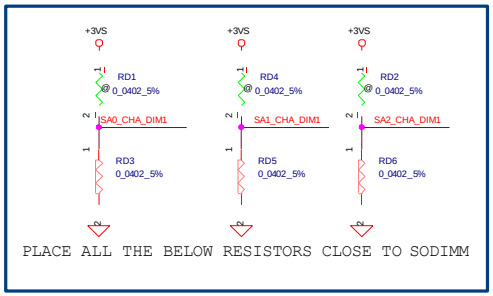
Date: Friday, January 05, 2018 | Sheet 16 of 59

CHANNEL-A

REVERSE TYPE

Interleaved Memory

TOP: JDIMM1 CONN Non-ECC DIMM



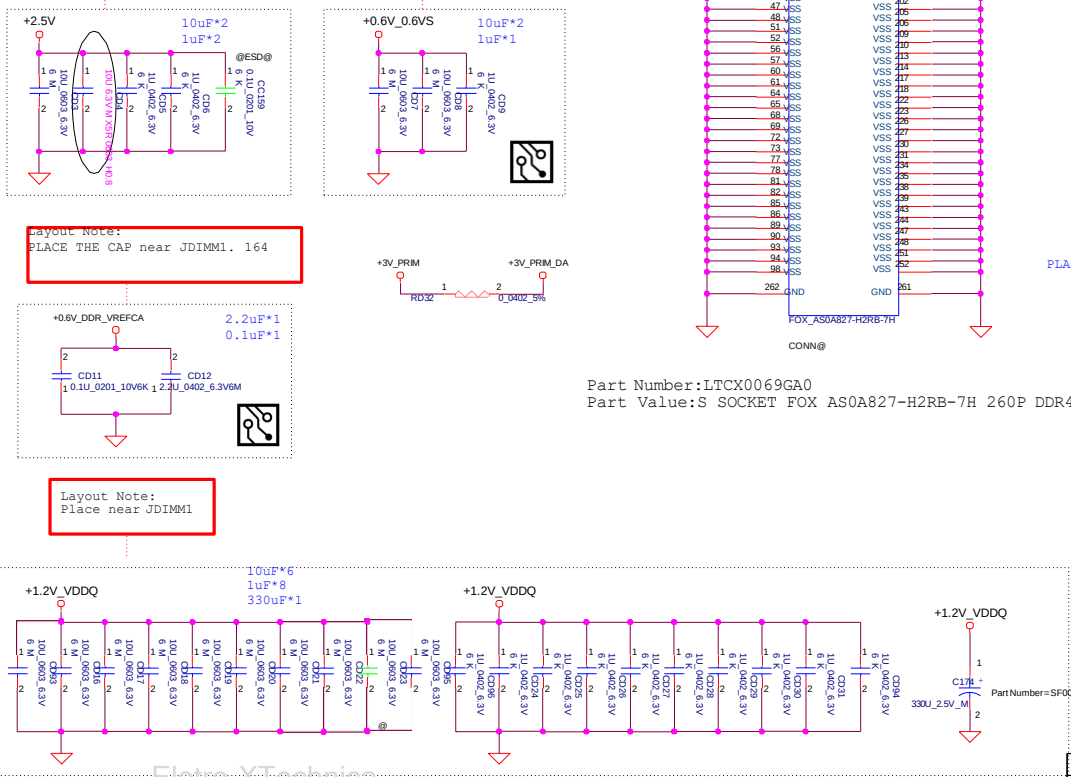
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
PLACE THE CAP near JDIMM1. 164

Layout Note:
Place near JDIMM1



Security Classification	Compal Secret Data		
Issued Date	2017/04/10	Deciphered Date	2019/12/15

Compal Electronics, Inc.	
Title	P18-DDRIV_CHA: DIMM0
Document Number	CSL50 / CSL52
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CHANNEL-B

STD (5.2 mm)

Interleaved Memory

DIMM TOP: JDIMM2 CONN Non-ECC

PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.258

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

Layout Note:
Place near JDIMM2

PLACE NEAR TO PIN

Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4

For ECC DIMM

PLACE NEAR TO SODIMM

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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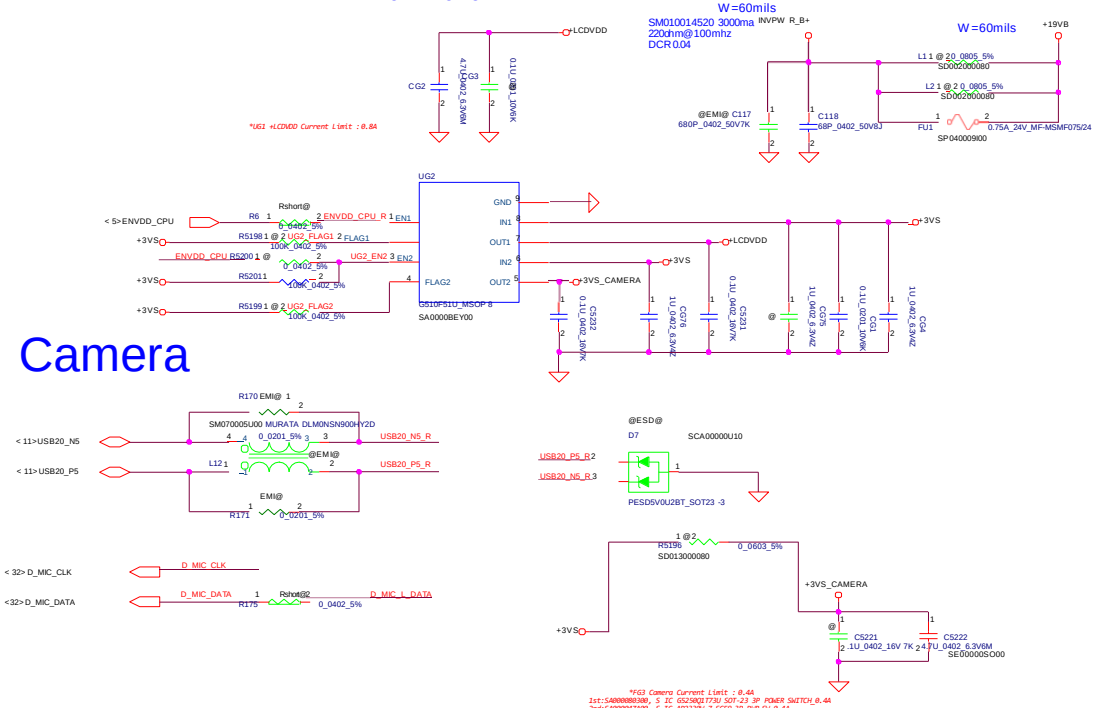
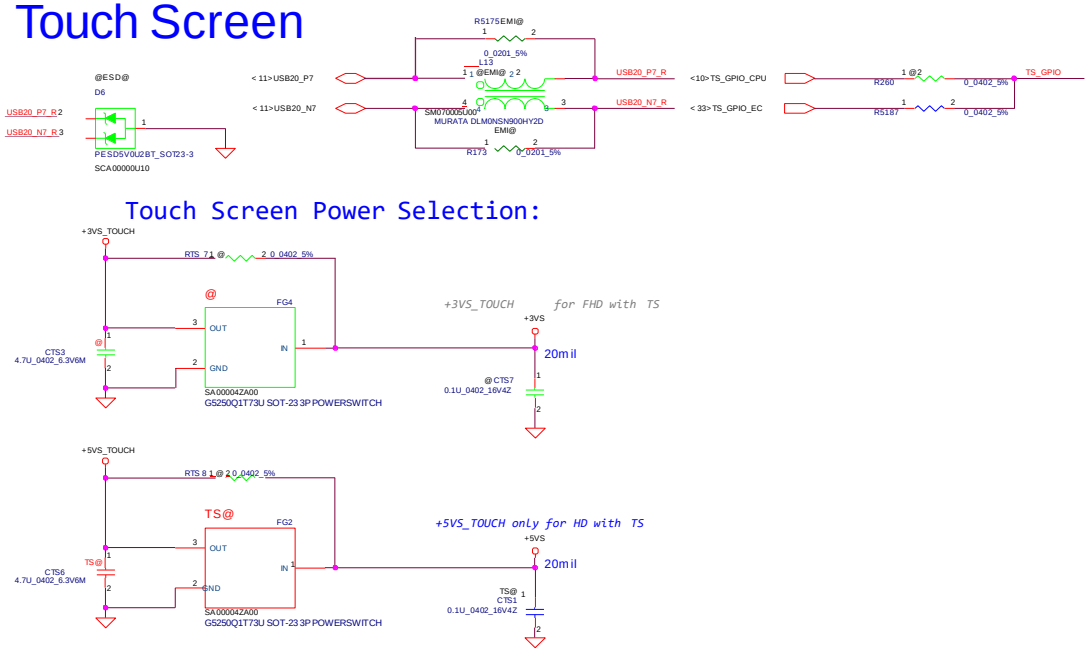
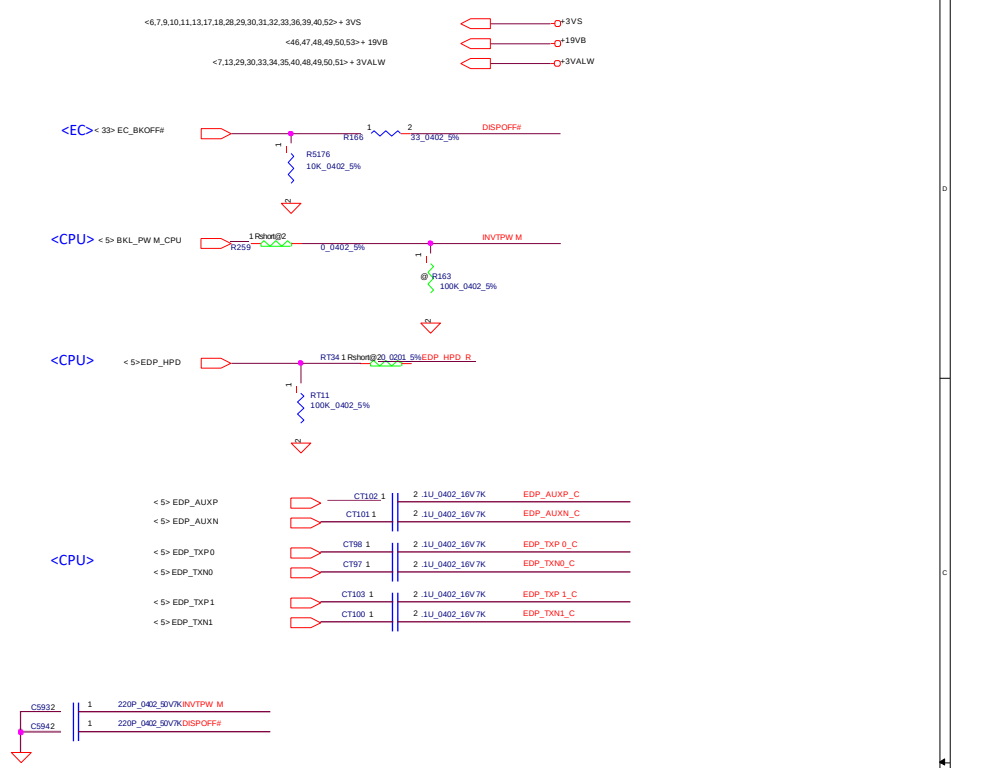
			Document Number: CSL50 / CSL52 Rev: v0.3
			Date: Friday, January 05, 2018 Sheet 18 of 59

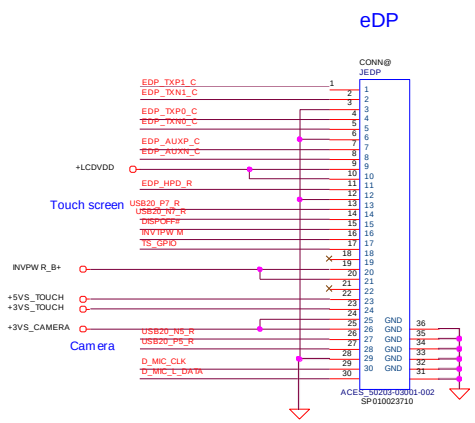
Camera



Touch Screen

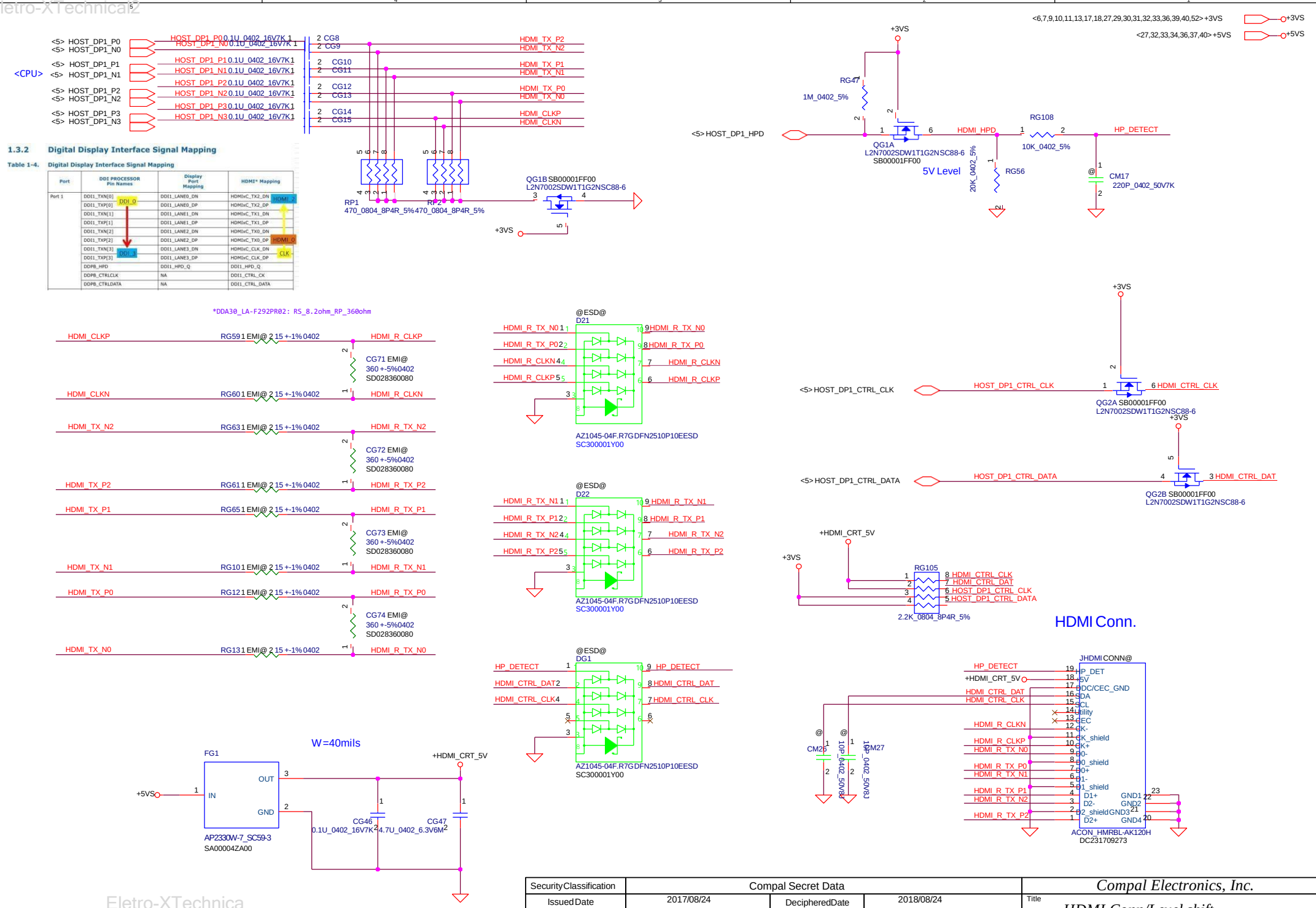






Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Title	eDP CONN/Camera/TS		
Size	Document Number		Rev
	CSL50 / CSL52		v0.3
Date: Friday, January 05, 2018		Sheet 27 of	59



Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: HDMI Conn/Level shift

Size: E | Document Number: CSL50 / CSL52 | Rev: v0.3

Date: Friday, January 05, 2018 | Sheet 28 of 59

+LAN_VDD_3V3 Rising time need>0.5mS and <100mS

CL8,CL23closeLL2.
CL26closeUL1Pin3.
CL12closeUL1Pin8.
CL13~CL15closeUL1Pin22.
CL11,CL27close UL1 Pin30.

RTL8107ESH-CG/RTL8111HSH-CG Co-Lay

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32

CL10& CL16 close to UL1: Pin 23

(SA0000ALR00)RTL8107ESH-CG10/100
(SA000084T00)RTL8111HSH-CGGiga

powe rail need to check

powe rail need to check

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Compal Electronics, Inc.

Title: LAN 8111

Document Number: CSL50 / CSL52

Rev: v0.3

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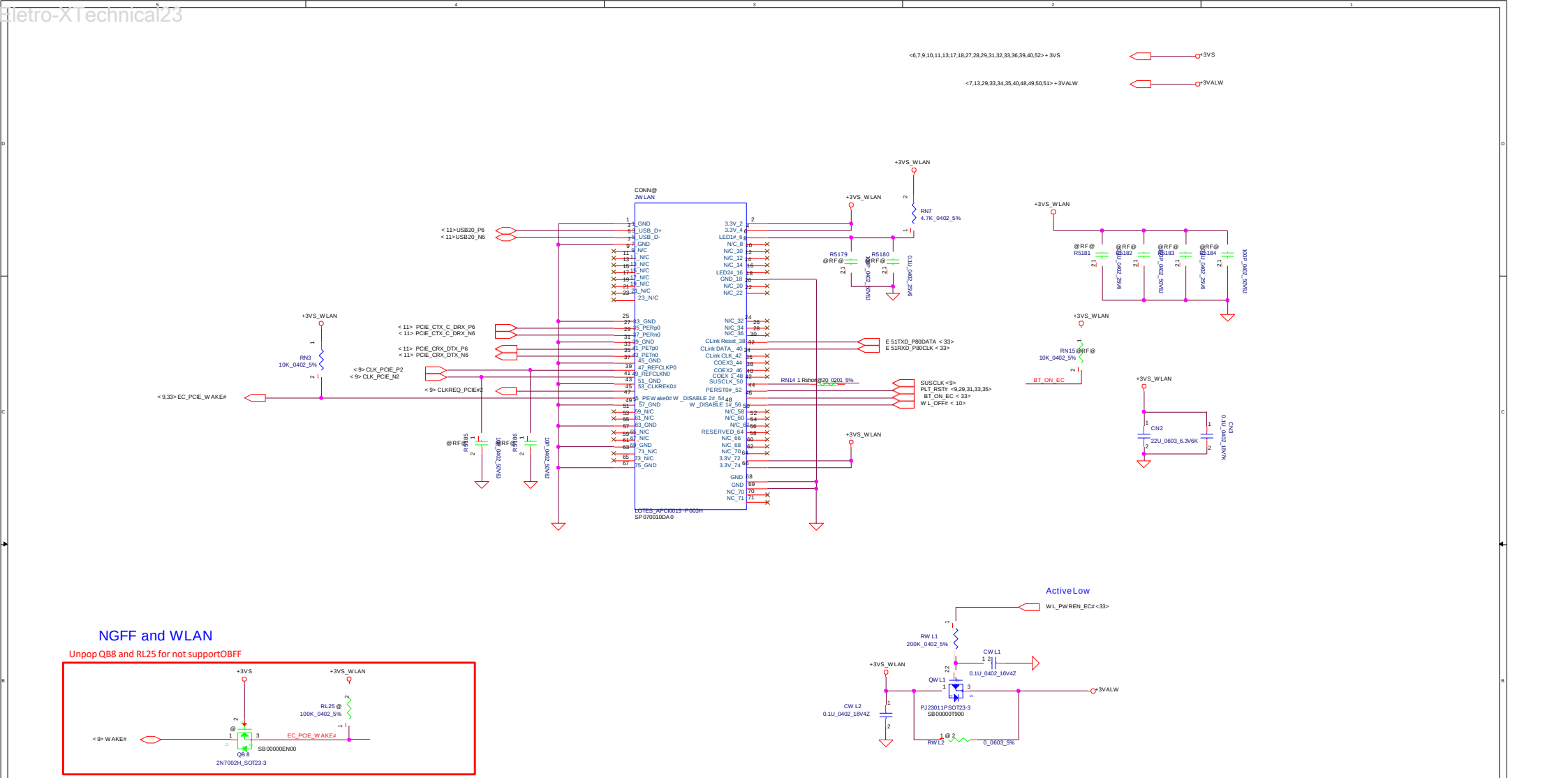

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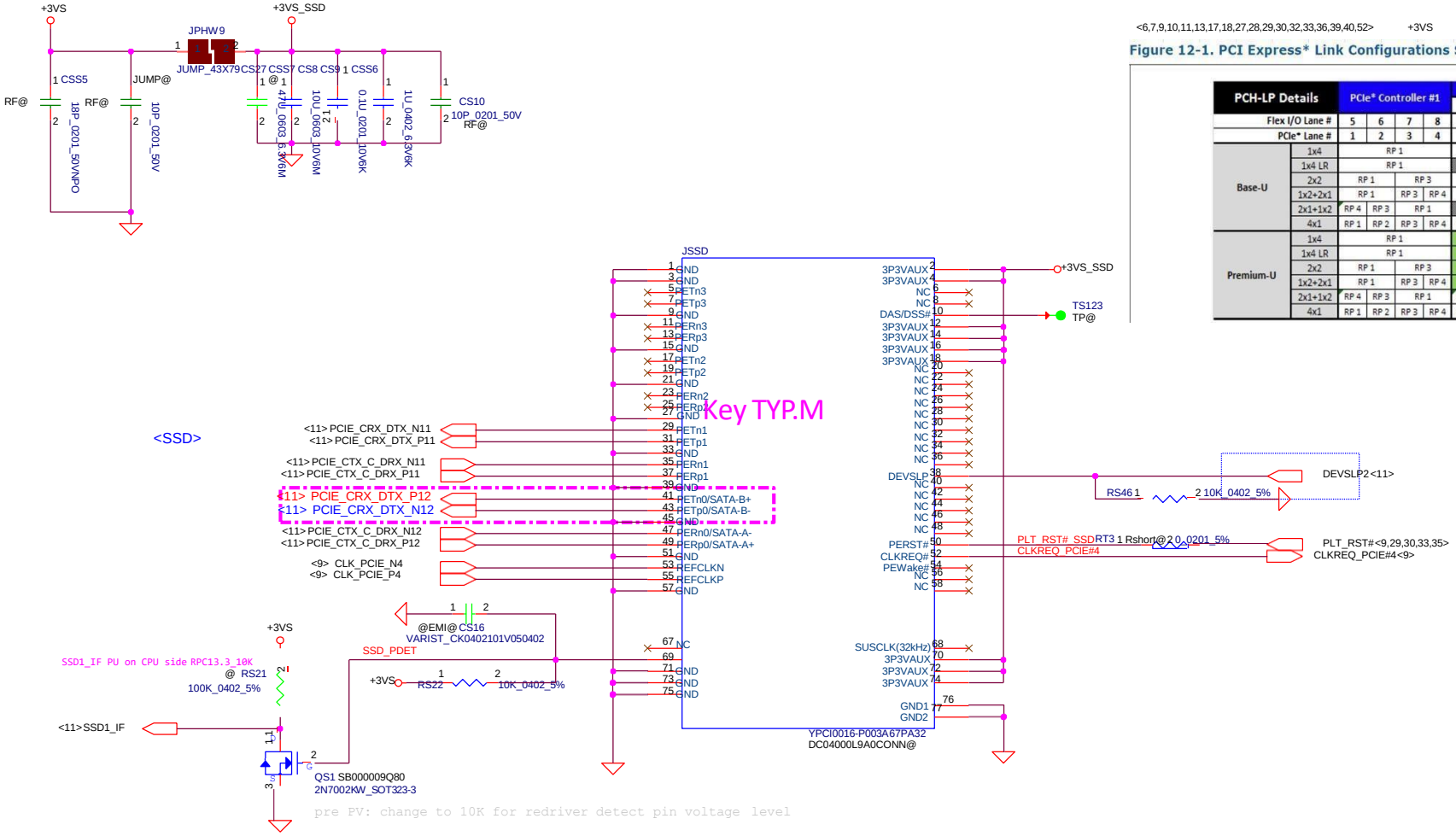

<6,7,9,10,11,13,17,18,27,28,29,30,32,33,36,39,40,52> +3VS +3VS

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2 Cycle Router #2				PCIe* Controller #3 Cycle Router #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1						RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	1x4 LR	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH	
41	PETn0	PCIe TX	42 N/C
43	PETp0	PCIe TX	44 N/C
45	GND	Return current path	46 N/C
47	PERn0	PCIe Rx	48 N/C
49	PERp0	PCIe Rx	50 PERST#
51	GND	Return current path	52 CLKREQ#

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

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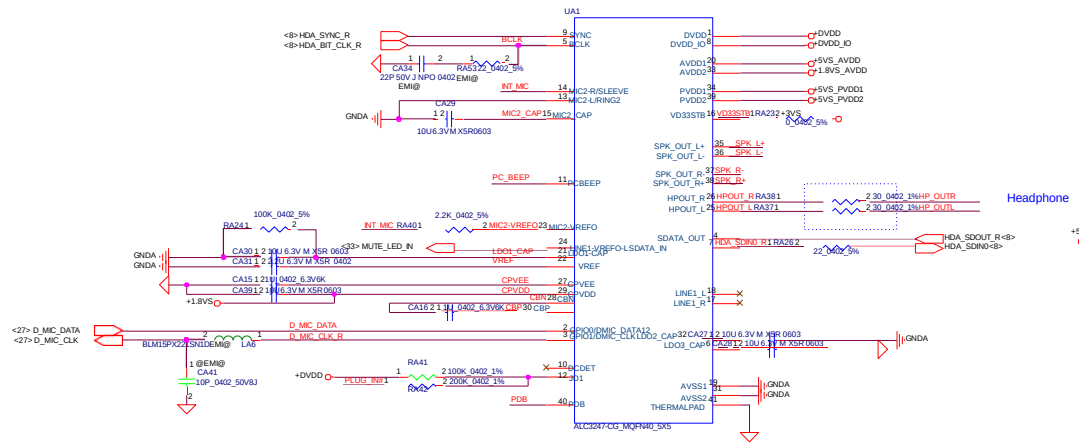
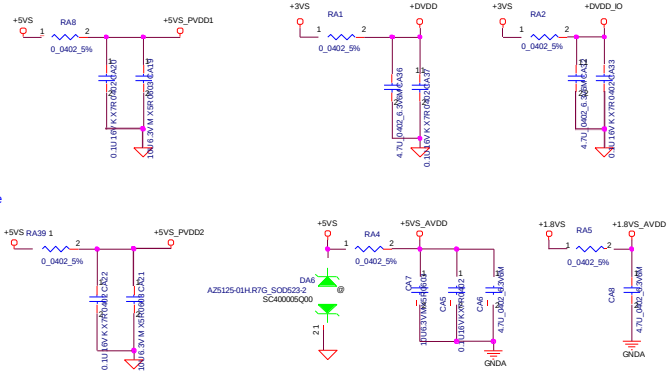
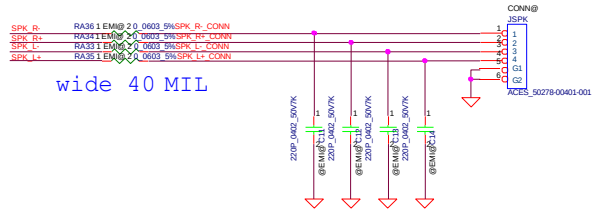
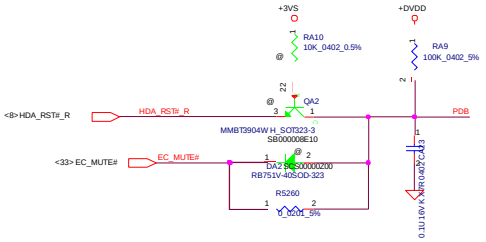




Internal SPK



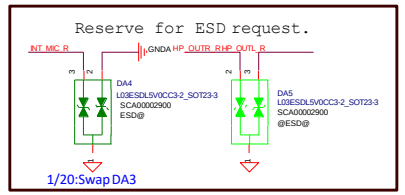


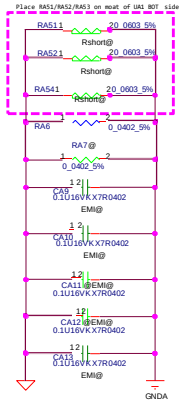
PC Beep

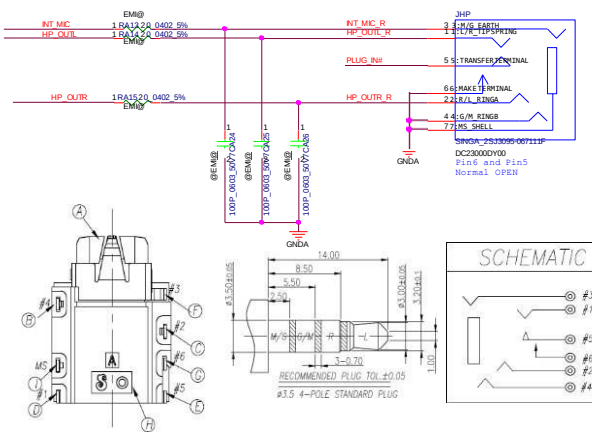
EC Beep<33> EC_BEEP#

SB Beep<8,10> HDA_SPKR

Close to Codec pin34







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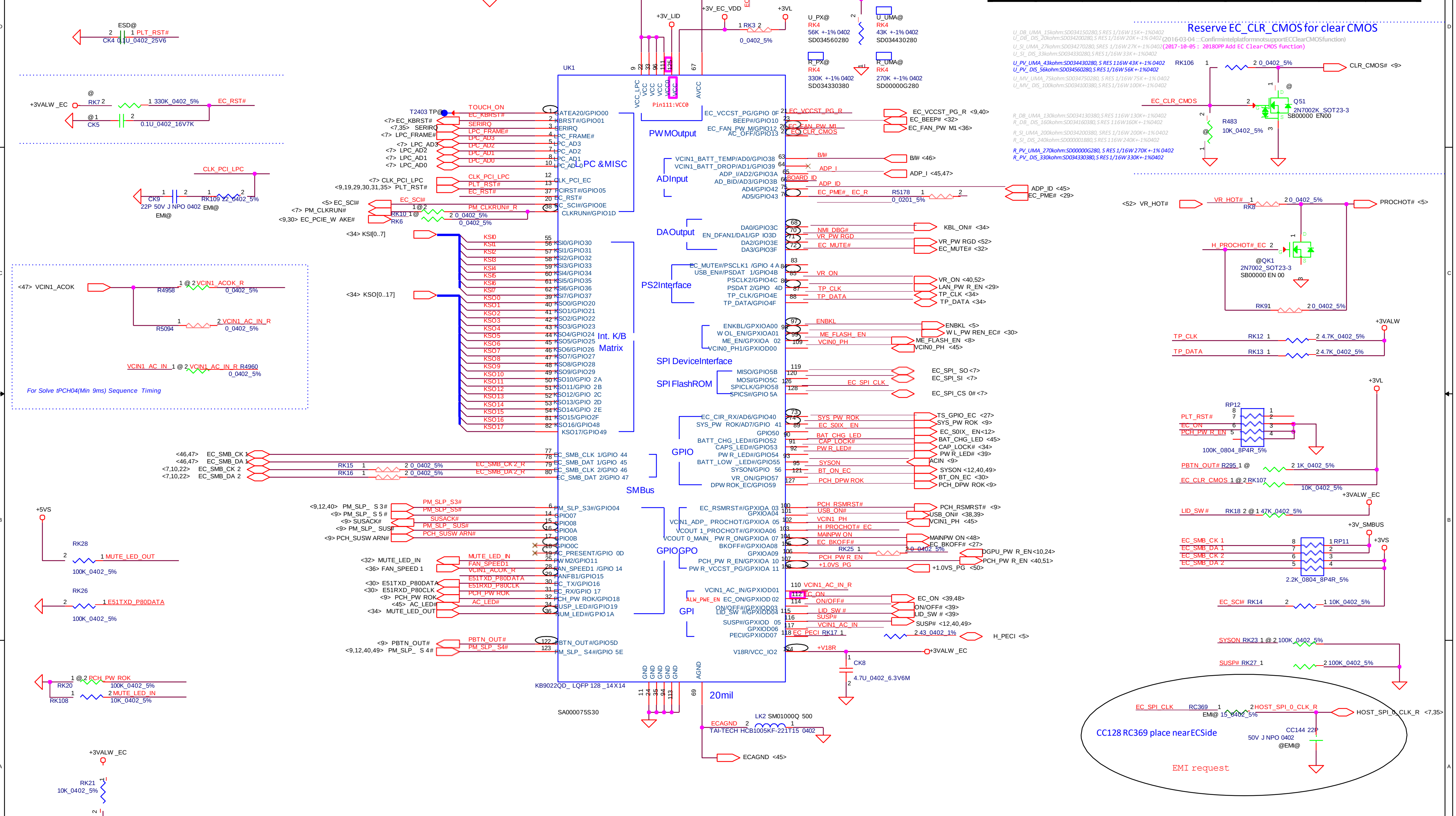
EC Board ID (UMA, DIS, phase) control table

RK4	KBL-U				KBL-R			
	DB	SI	PV	MV	DB	SI	PV	MV
UMA	15K	27K	43K	75K	130K	200K	270K	430K
DIS	20K (0x0?) (0x03)	33K (0x04) (0x05)	56K (0x06) (0x07)	100K (0x08) (0x09)	160K (0x0A) (0x0B)	240K (0x0C) (0x0D)	330K (0x0E) (0x0F)	560K (0x10) (0x11)



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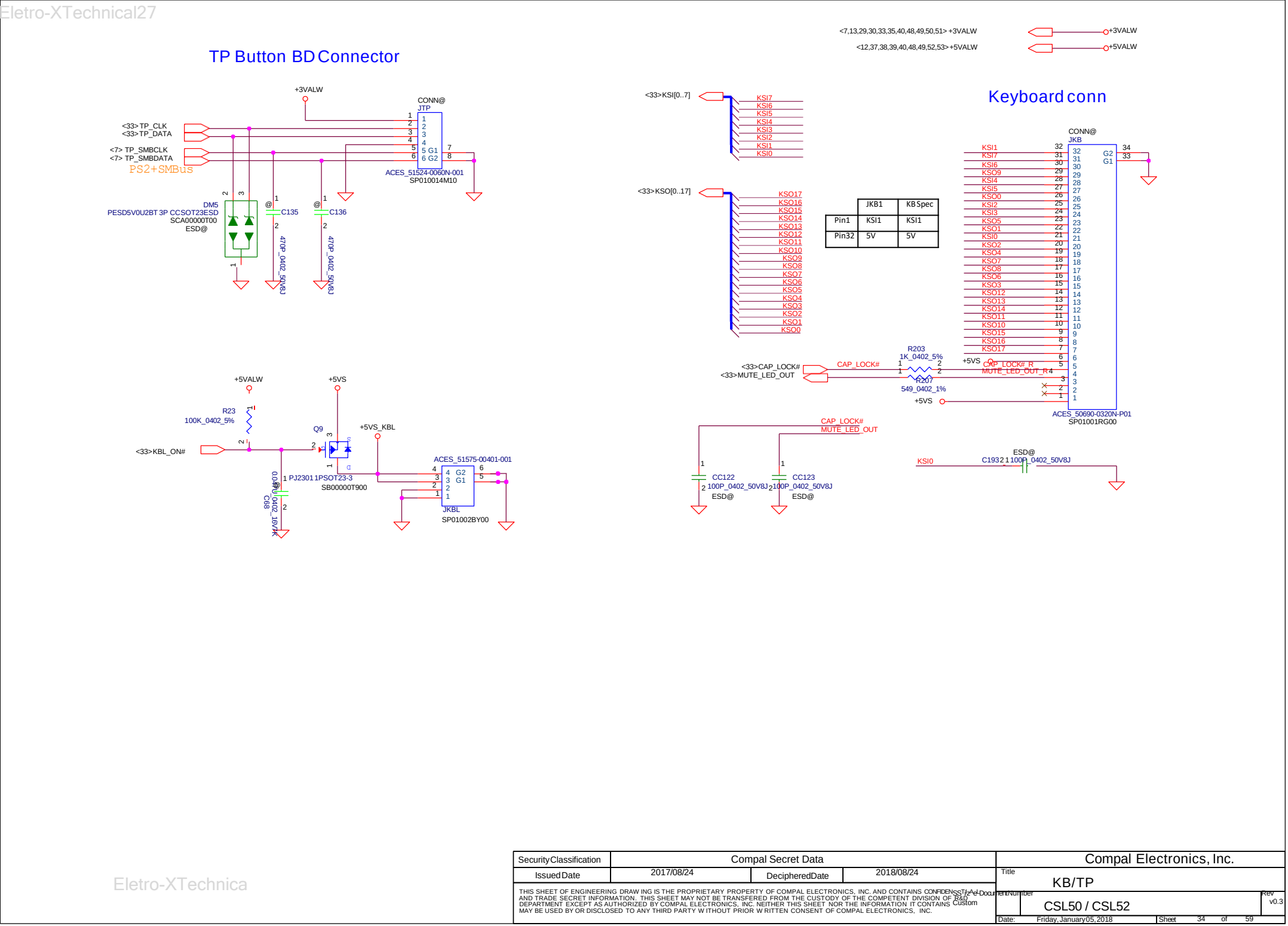

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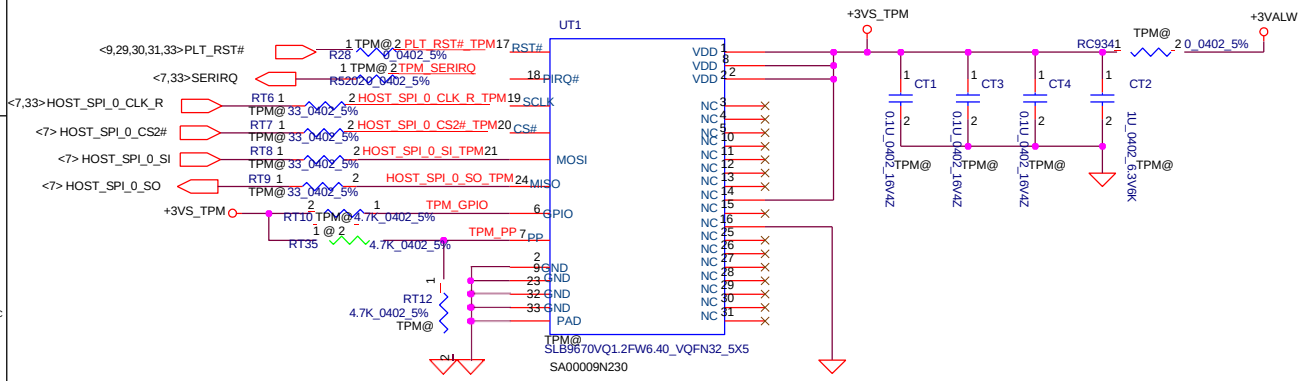
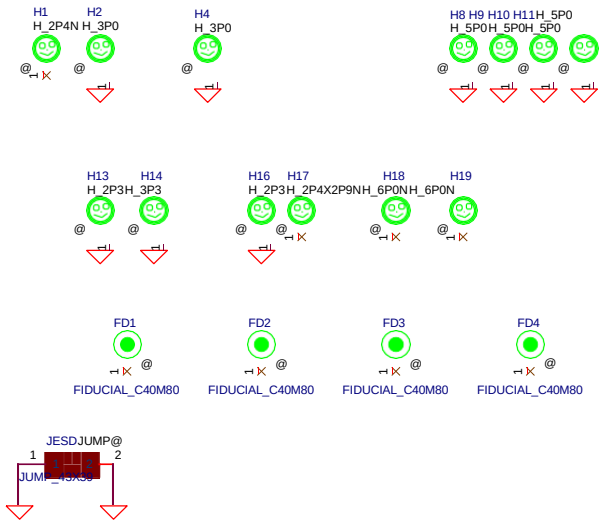
+3VALW +3VALW <7,13,29,30,33,34,40,48,49,50,51>

TPM2.0



Screw Hole

CPU



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Compal Electronics, Inc.

Title: TPM/Screw

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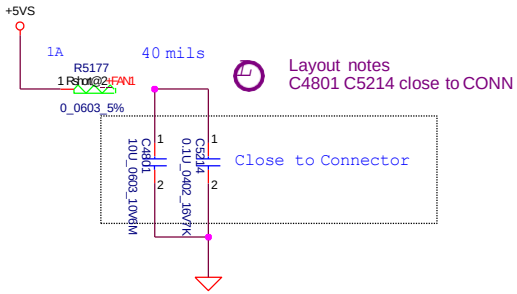

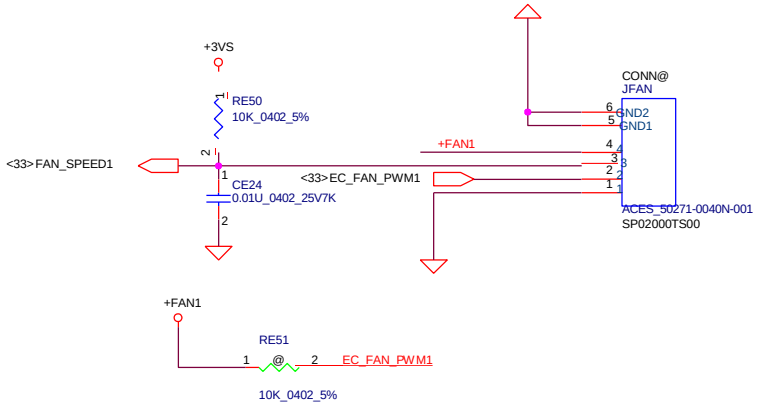

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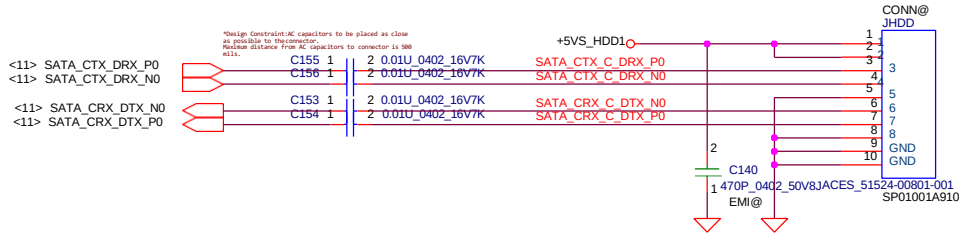
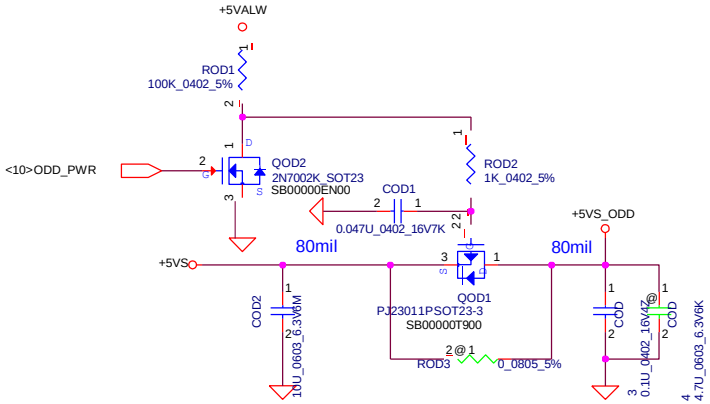
2.5" SATAHDD

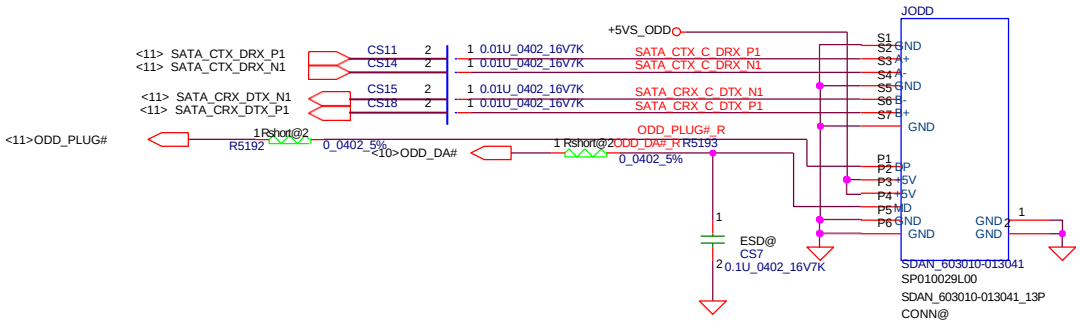
<27,28,32,33,34,36,40>+5VS
<12,34,38,39,40,48,49,52,53> +5VALW
<7,13,29,30,33,34,35,40,48,49,50,51> +3VALW

<PV> change shortpad



SATAODD





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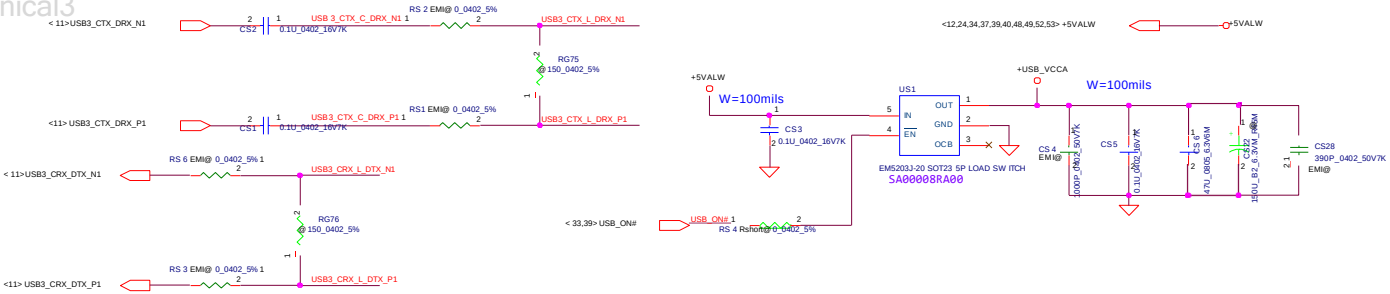
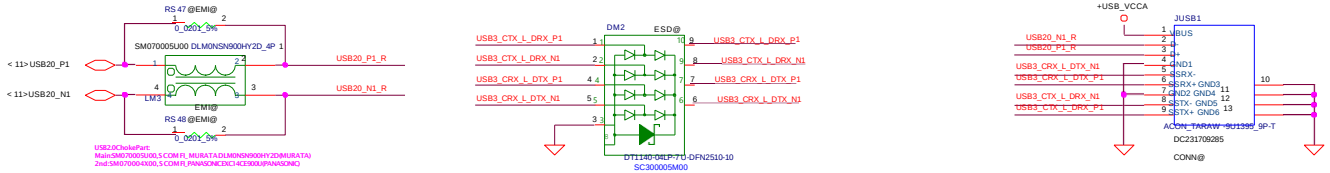
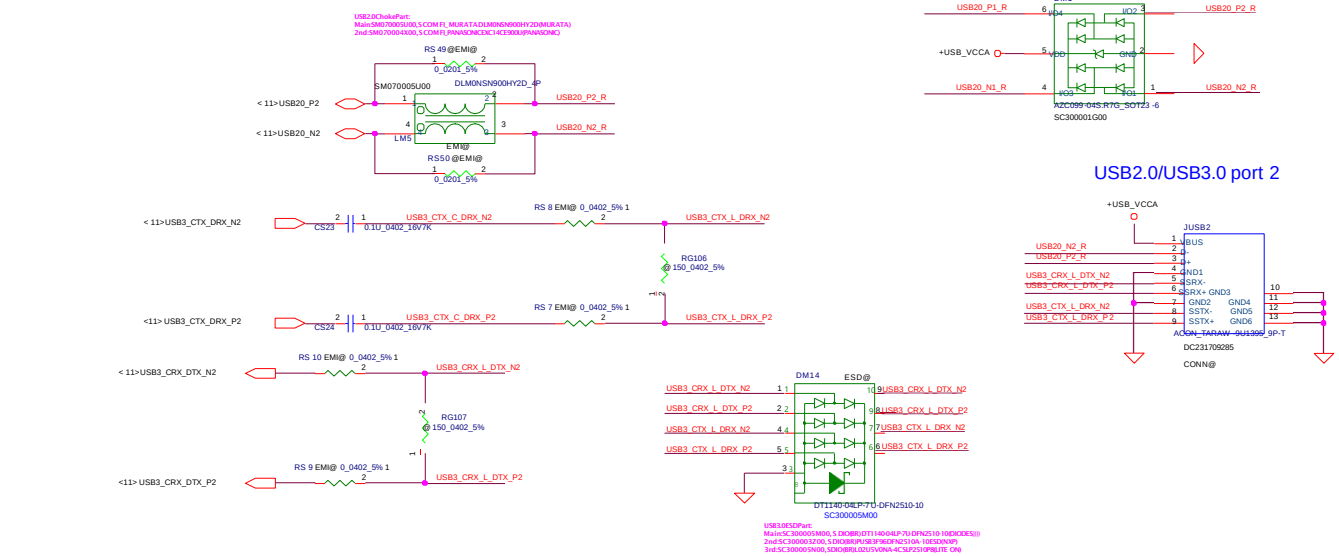


USB2.0/USB3.0 port 1



USB2.0/USB3.0 port 2



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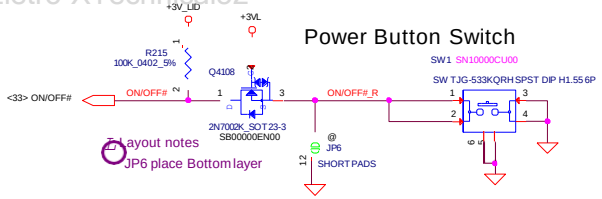
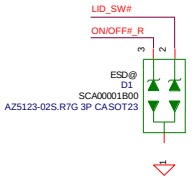
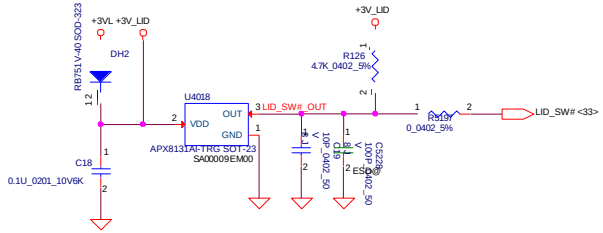
Power Button Switch

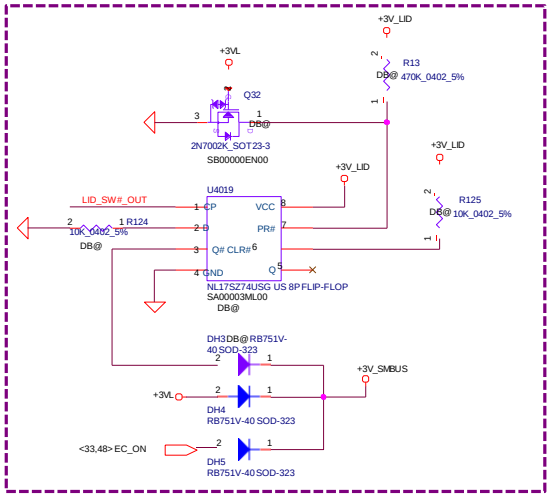


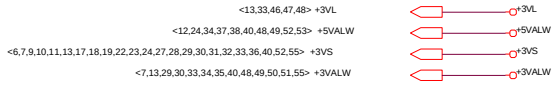
ESD Diode



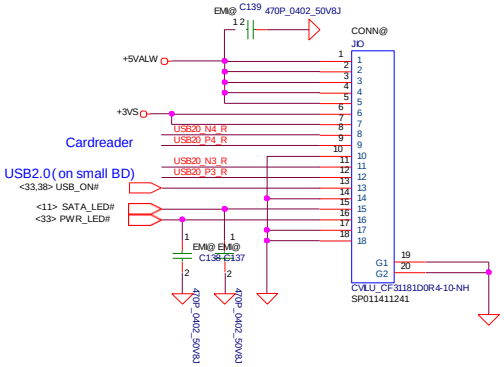
Lid Switch (Hall Effect Sensor)

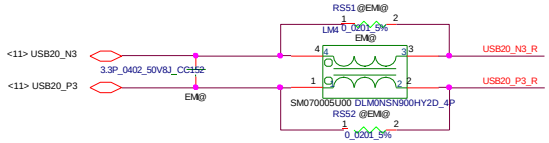


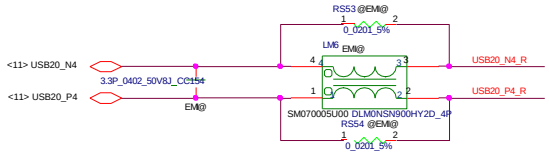




IO BD Connector (USB2.0,Card reader,HDD & PWR LED)







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			Document Number: CSL50 / CSL52
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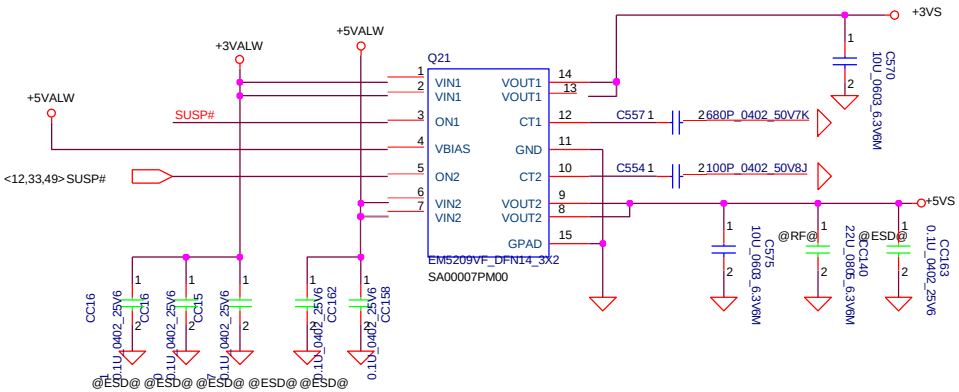
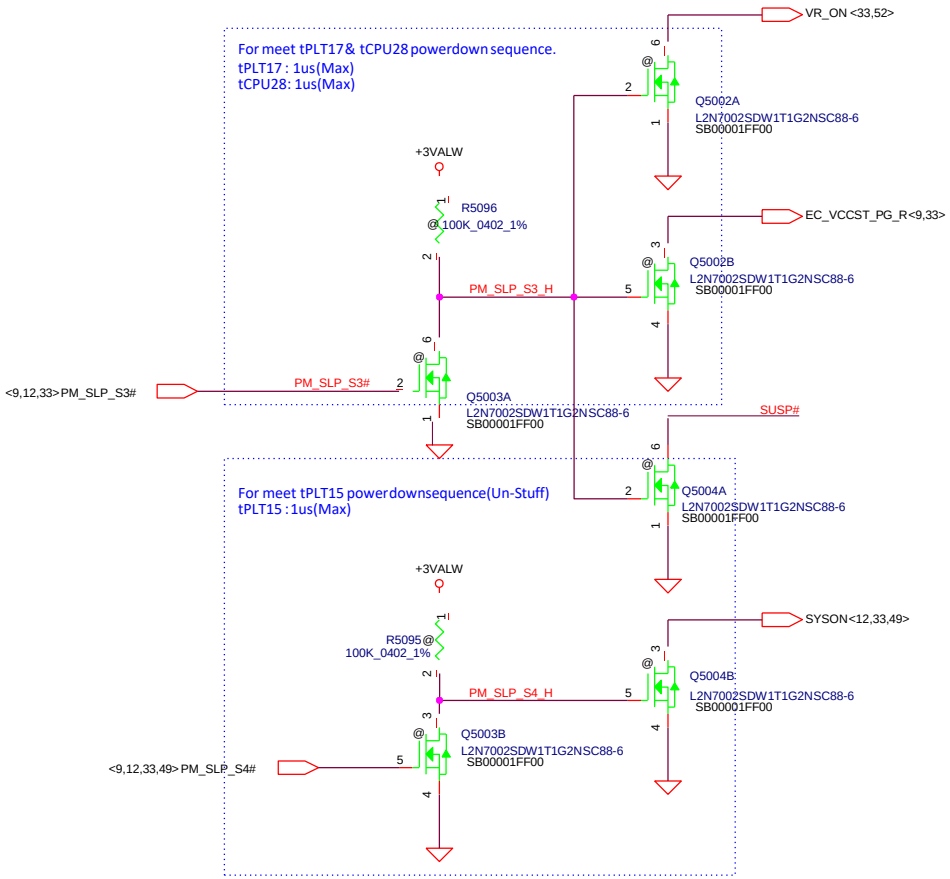
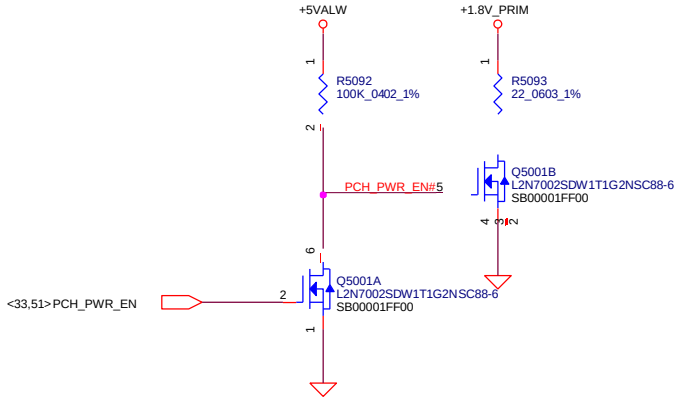
+3VS
+5VS

+3VS <6,7,9,10,11,13,17,18,27,28,29,30,31,32,33,36,39,52>
+5VS <27,28,32,33,34,36,37>





For +1.8V_PRIM Discharge



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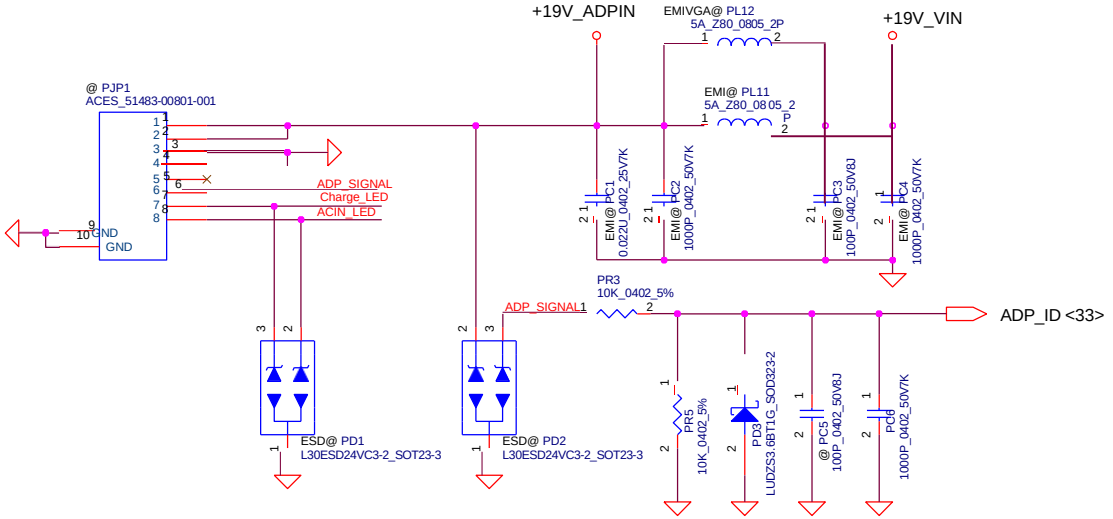

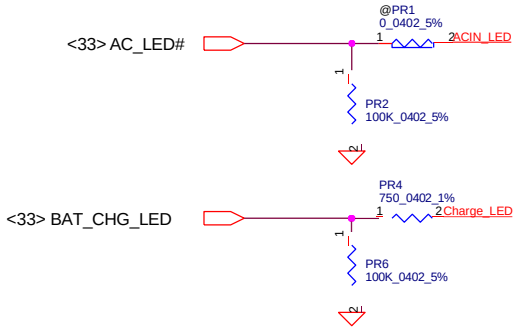

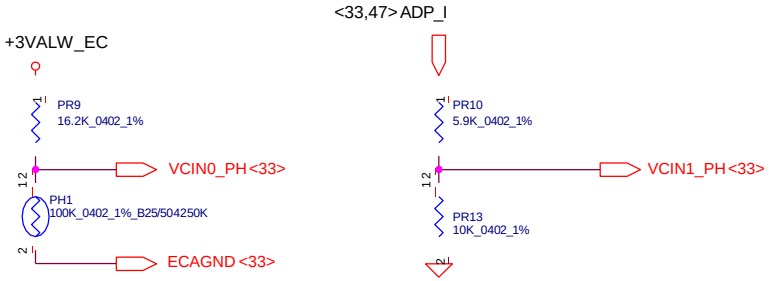

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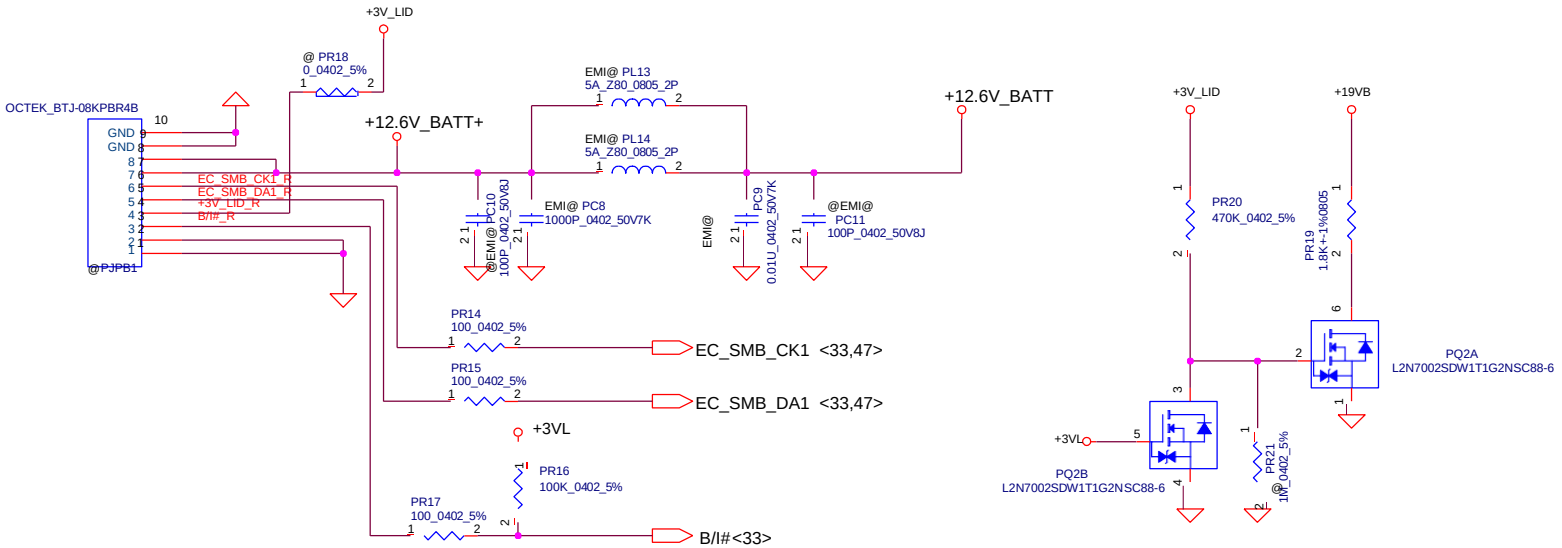

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Size	Document Number		Rev
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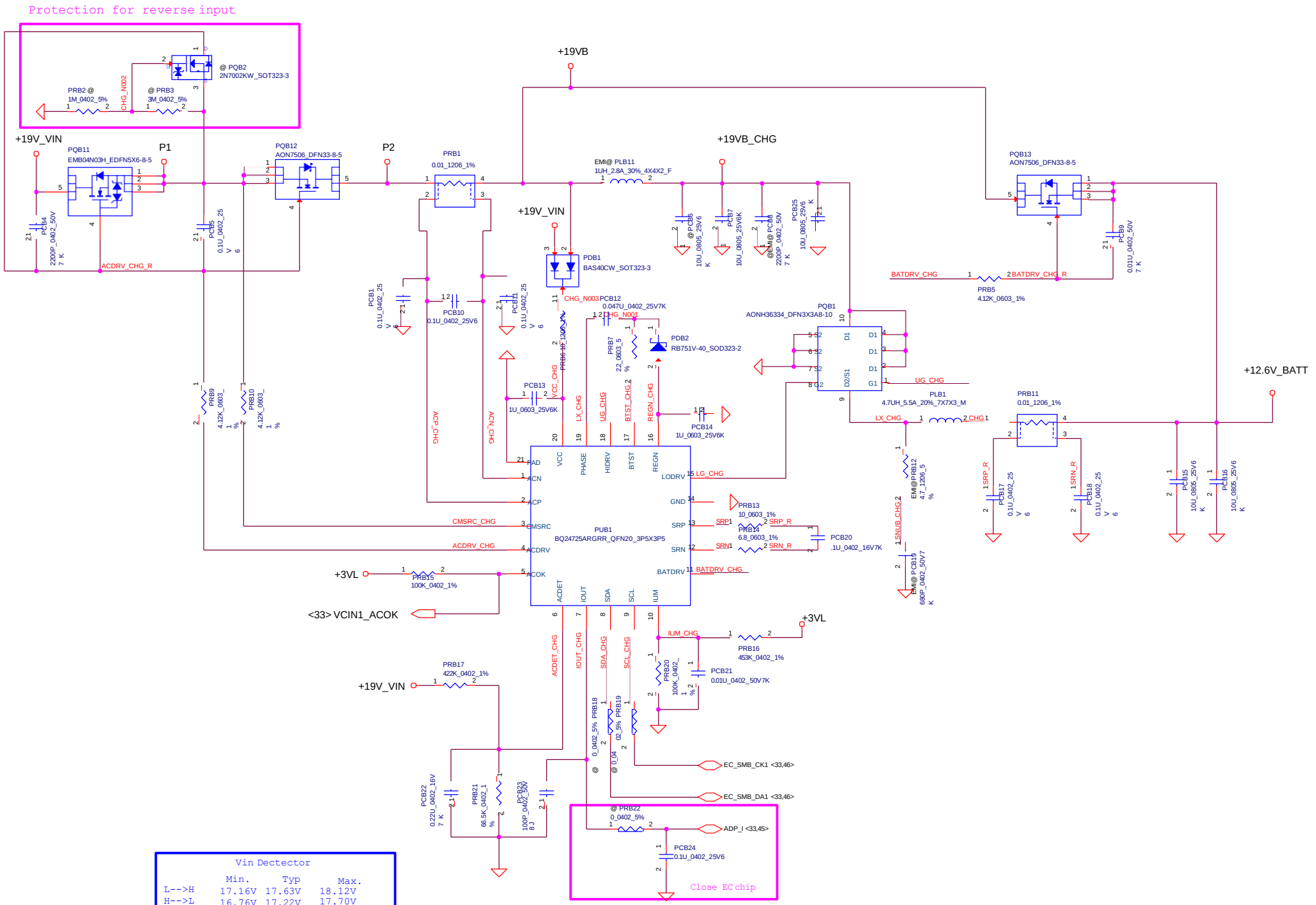

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Title: CHARGER

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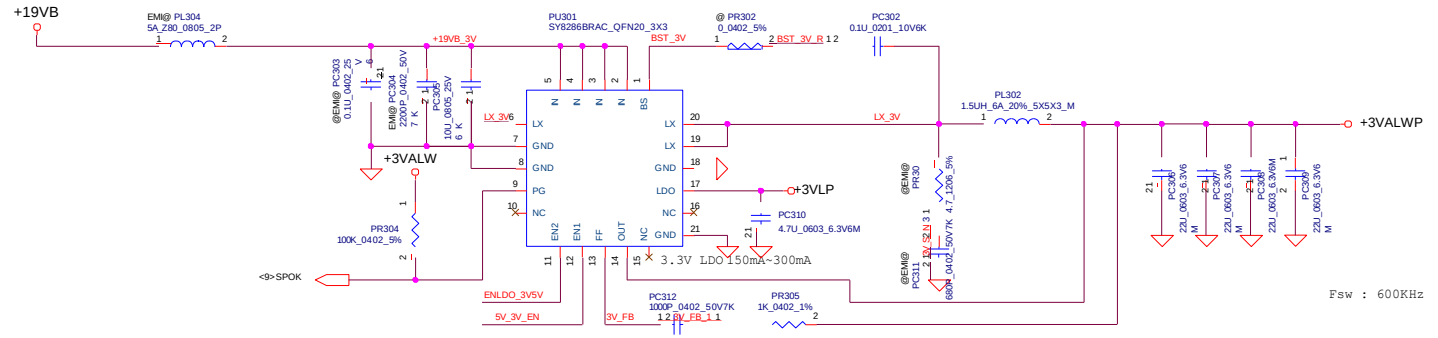
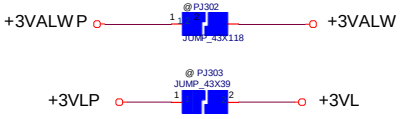
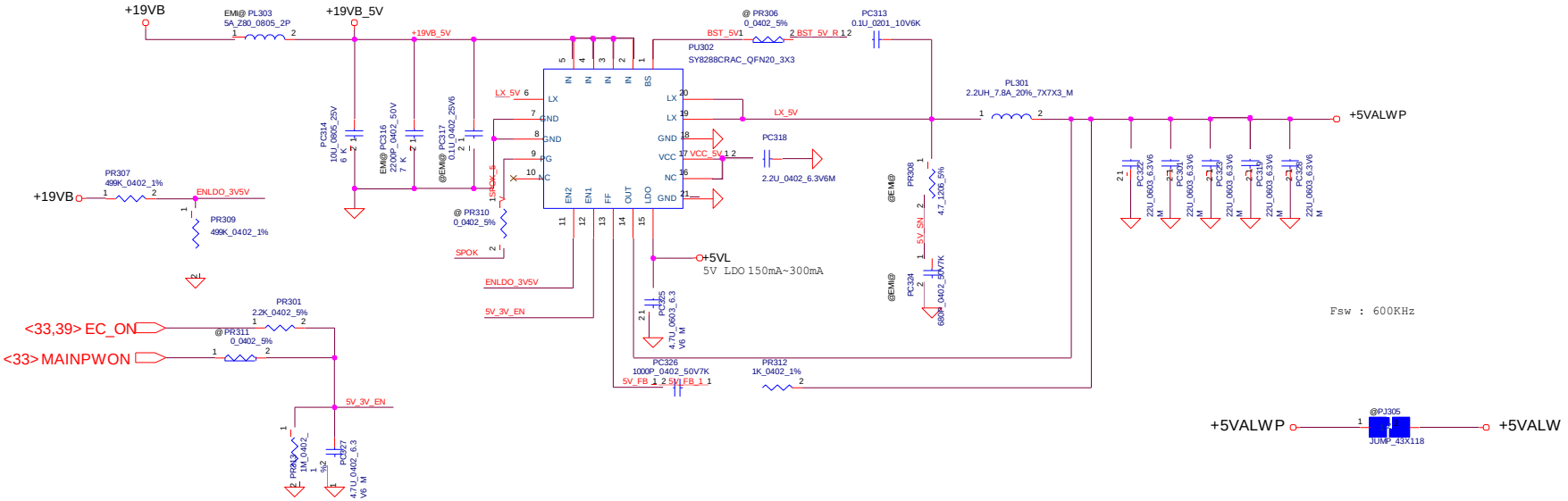




2 Cell battery : Cin=10uF*2pcs
3 Cell ~ 4 Cell battery :Cin=10uF*1pcs



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Size: Custom | Document Number: CSL50 / CSL52 v0.3 | Rev:

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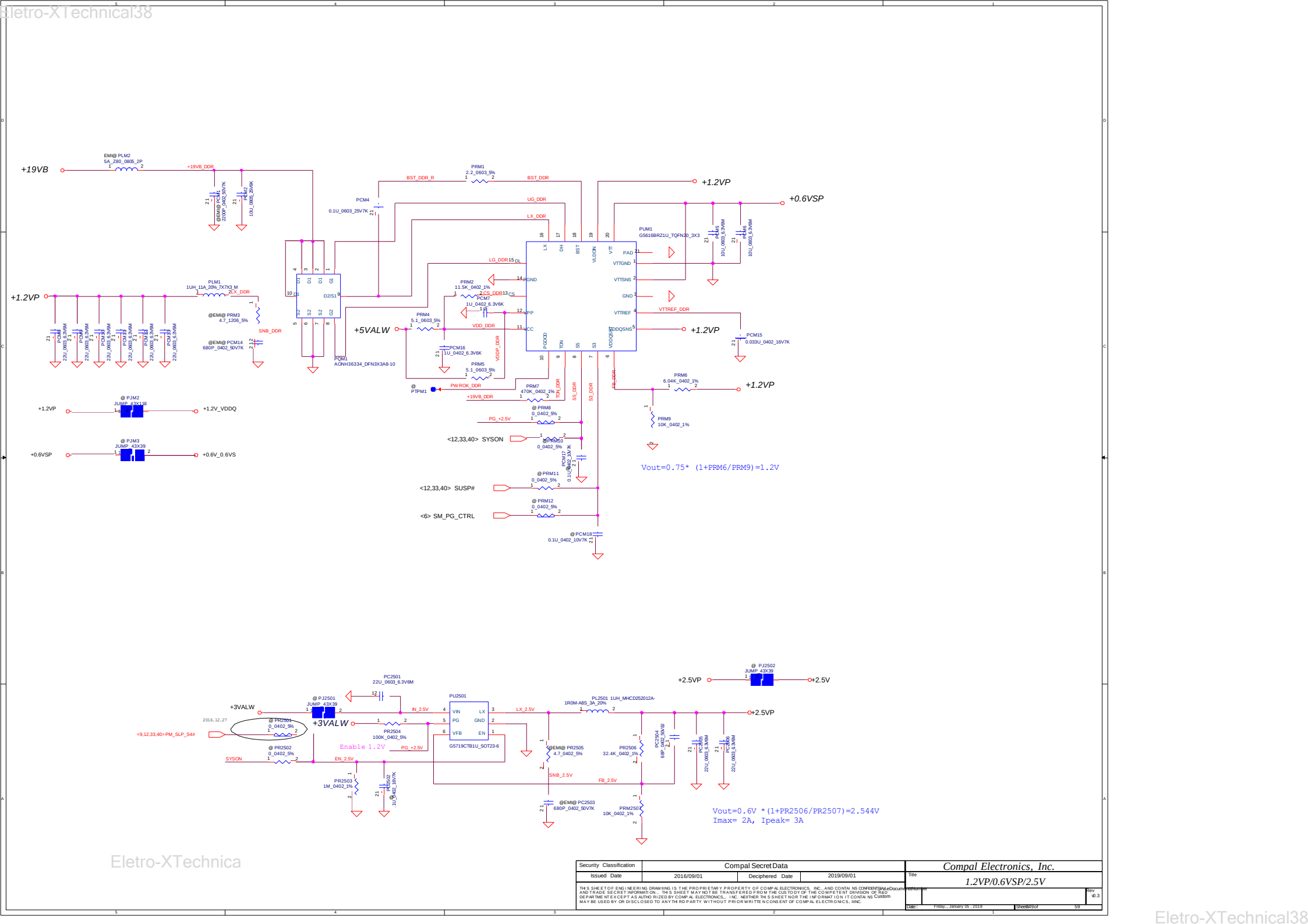

Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.	
Title	1.2VP/0.6VSP/2.5V
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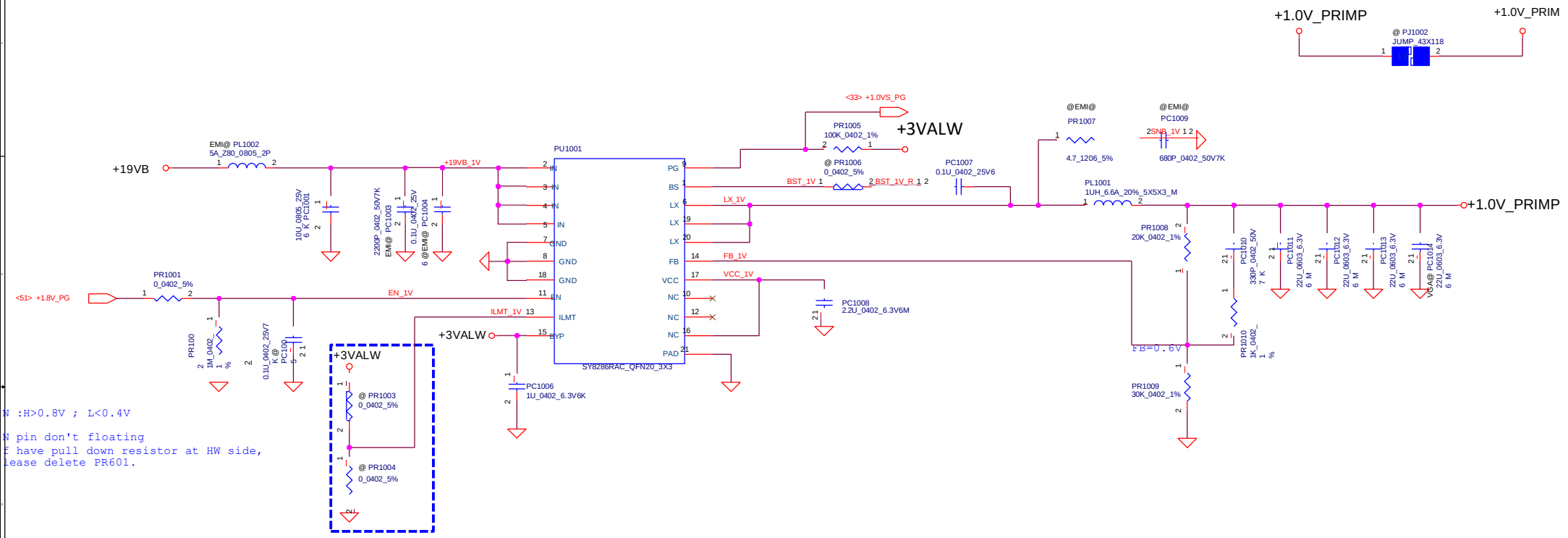
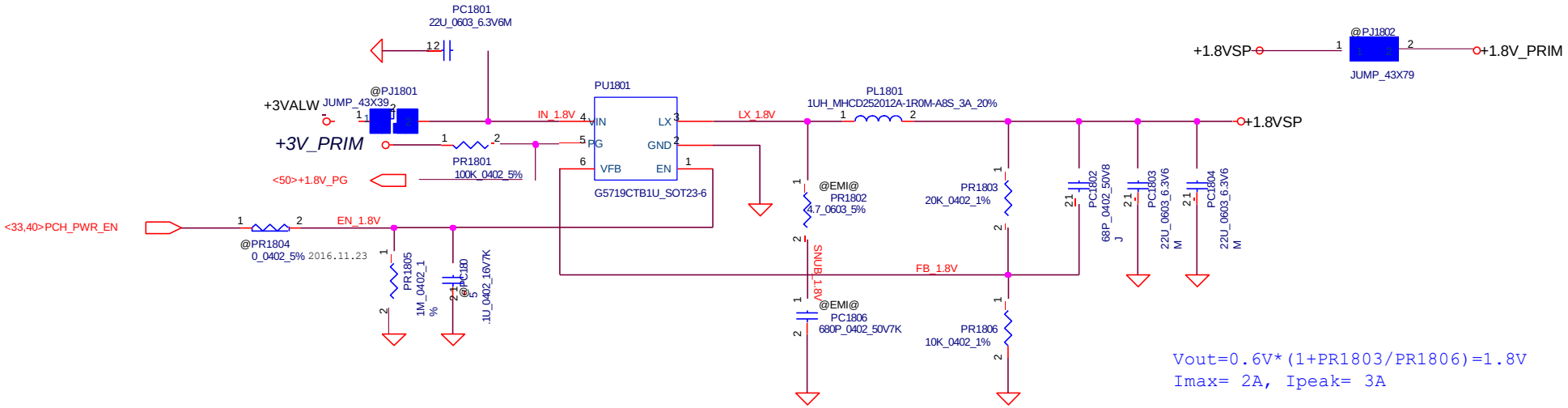


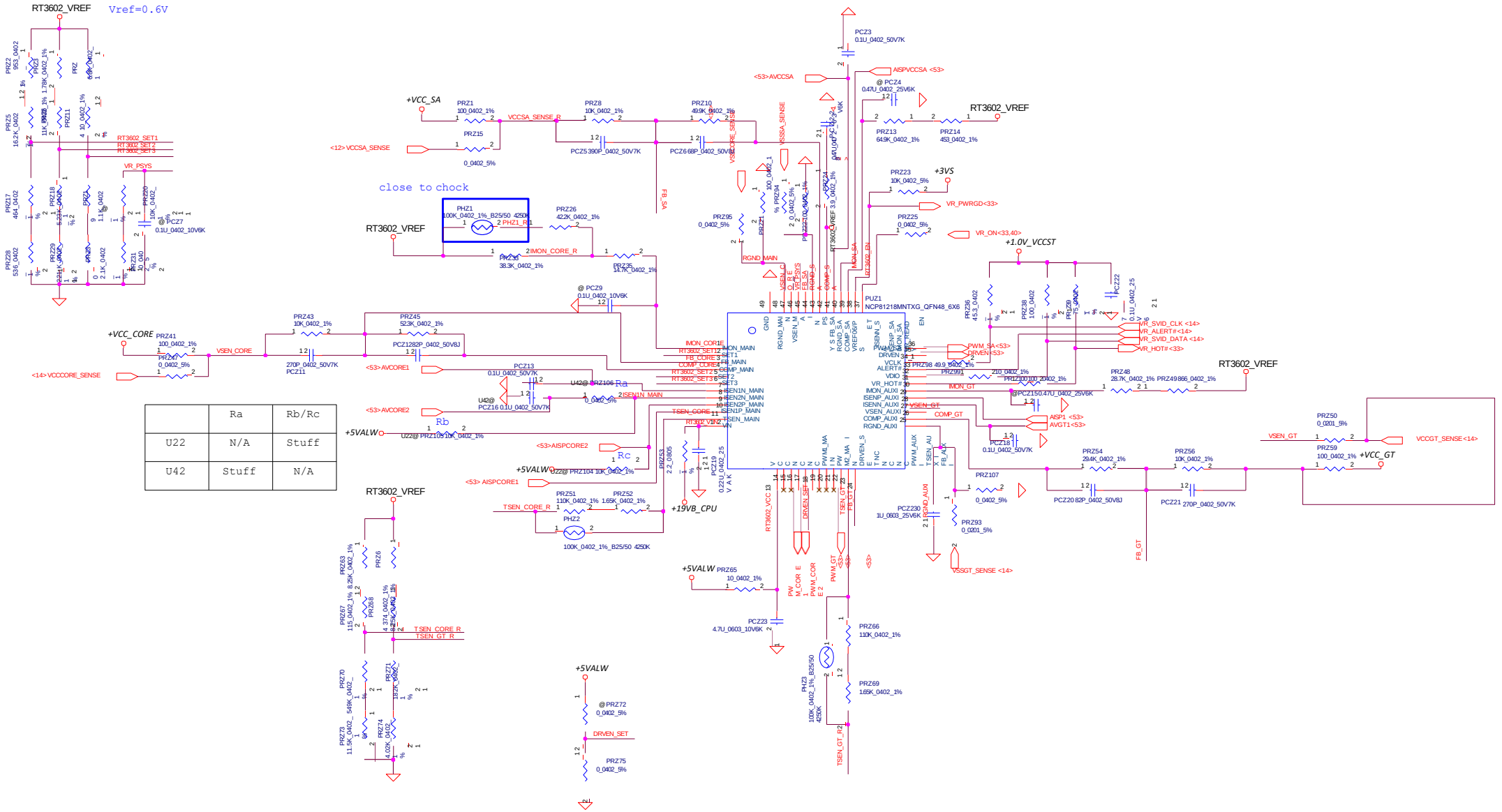
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Size: Custom	Document Number		Rev: v0.3
Date: Friday, January 05, 2018	Sheet 50 of 59		

Title: 1.0V_PRIM



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date 2019/09/01	Title: 1.8V_PRIM
			Size: B — Document Number: CSL50 / CSL52 — Rev: v0.3
			Date: — Sheet 51 of 59



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01
Title	CPU_CORE		
Document Number	CSL50 / CSL52		Rev 0.3
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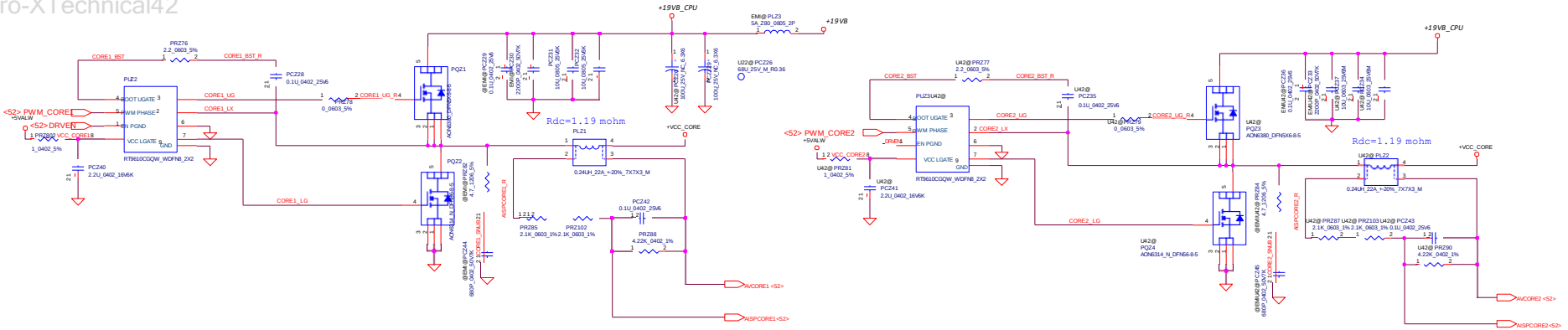
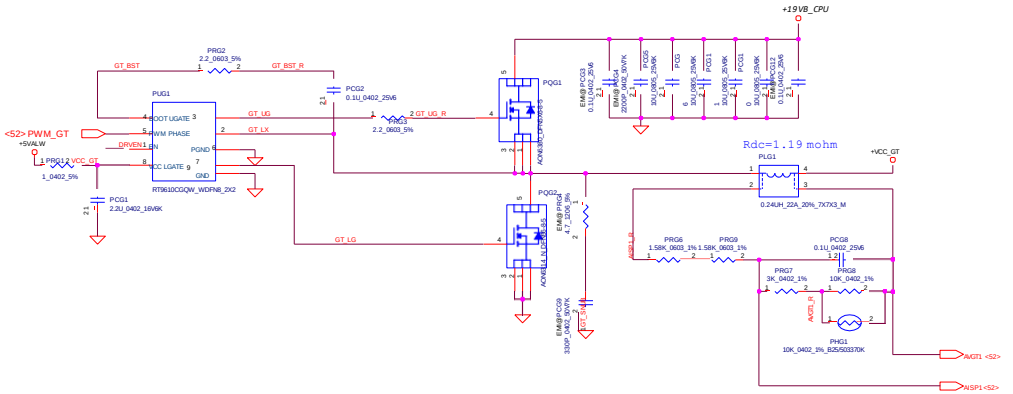




VCC_CORE
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=500kHz
Choke=0.24uH
DCR=1.19 mohm +/- 5%

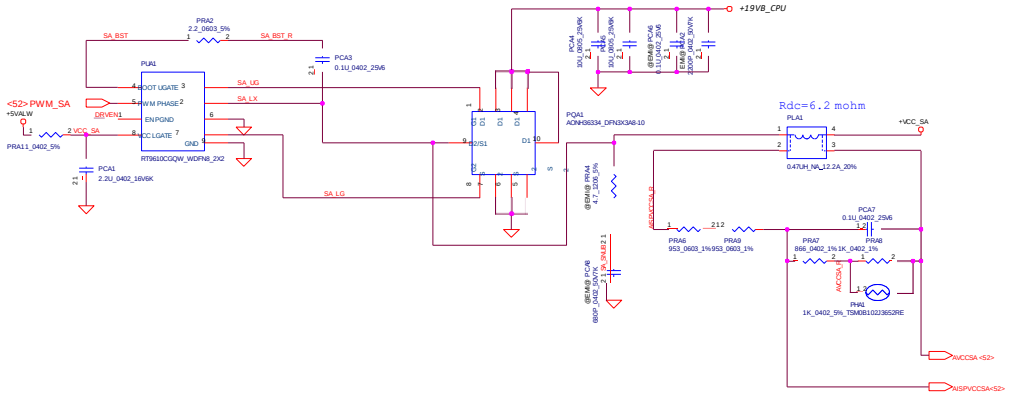
U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=4.5A
OCP=9.5A

U42
LL=10.3 mohm
TDC=
ICCMAX=5A
OCP=9.5A



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01	Title: CPU Power stage
			Document Number: CSL50 / CSL52	Rev: 0.3
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+VCC_CORE

2016.12.29

VCC_CORE :
U22
390uF*1
22uF*18
1uF*35

U42
390uF*2
22uF*22
1uF*35

+VCC_GT

VCC_GT :
U22 & U42
390uF*1
22uF*33
1uF*13

+VCC_SA

VCC_SA :
U22 & U42
22uF*9
1uF*7

2016.11.21

2016.11.10

BOM option
by JU22(for GT) and JU42A (for IA)

U42@

+VCC_GT_VR

+VCC_GTX_VR

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Title: *PROCESSORDECOUPLING*

Size: A3 | Document Number: CSL50 / CSL52 | Rev: v0.3

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