Compal Confidential

Broadwell M/B Schematics Document

Intel ULV Processor with DDR3L

Date : 2015/04/14

Version 1.0

Project : Puccini (15")
ABW50

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

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Title	Cover Page	
Size: Custom	Document Number: LA-C501P	Rev: 1.0
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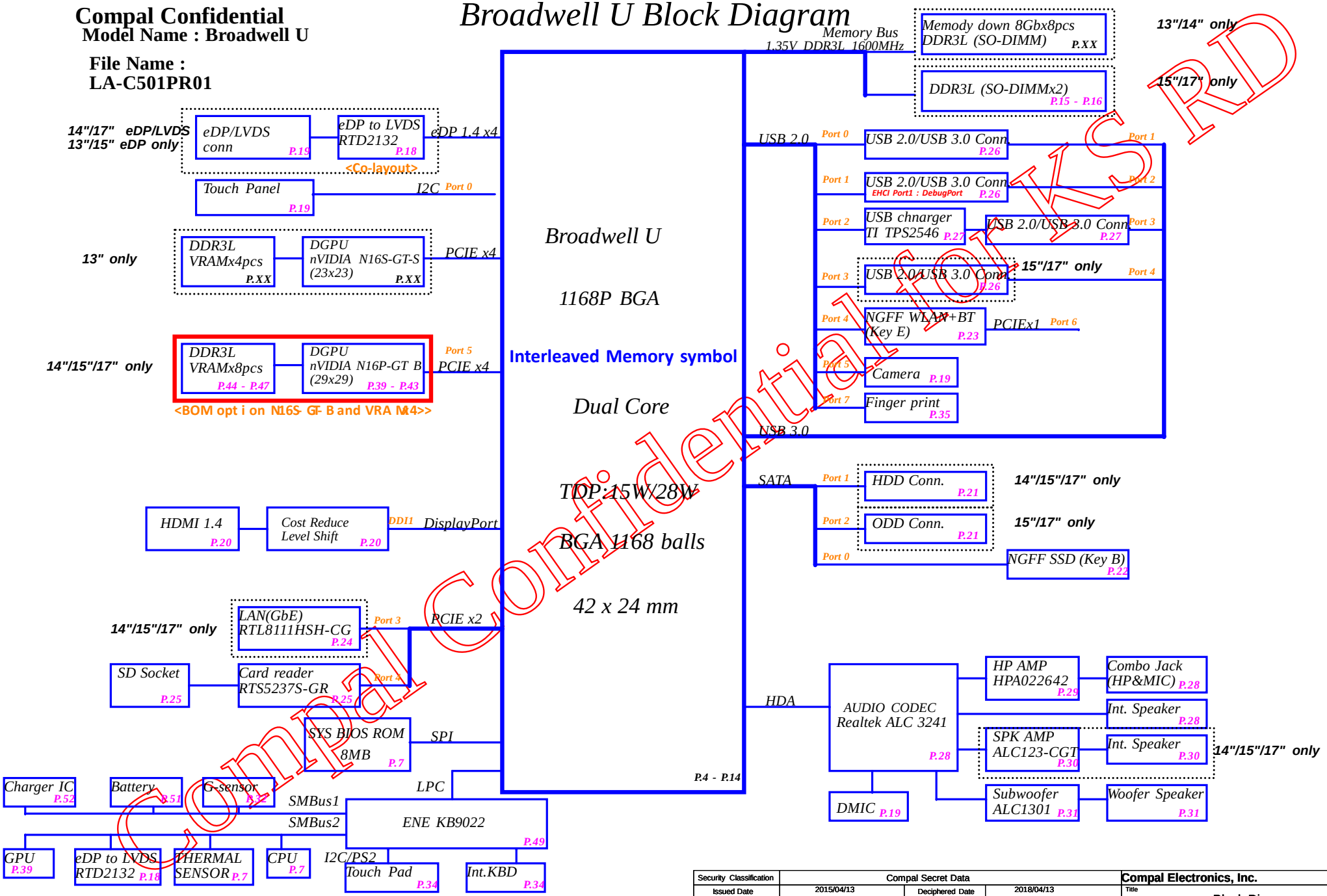
Compal Confidential
Model Name : Broadwell U

File Name :
LA-C501PR01

Broadwell U Block Diagram



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Title: Block Diagrams

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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
+19VB	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VL_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.35V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.675VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

@ is NO SMT part (empty)

short@ : short pad , don't pop.

@EMI@,@ESD@,@RF@ : Reserve , don't pop.

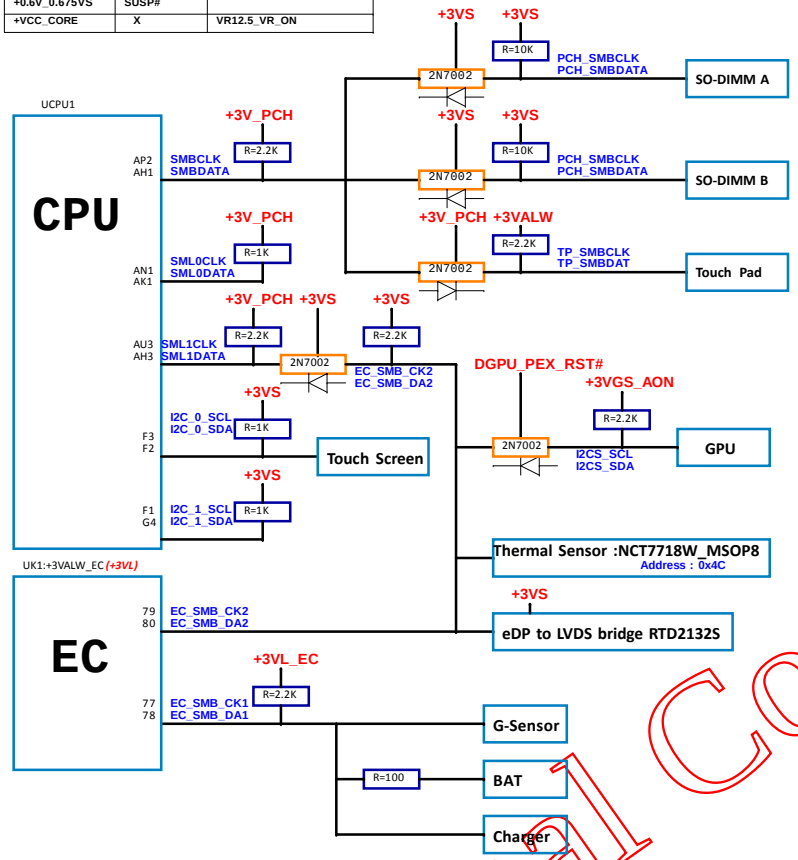
RF@ : RF team request, must add.

EMI@ : EMI team request, must add.

ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel.

DIS@ : GPU BOM conf i g



ZZZ

PCB

Part Number = DAZ1DO00100

PCB 1DO LA-C501P REV0 M/B 4

45@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

RO0000003HM

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SOC_SMBCLK SOC_SMBDATA	+3VS	DIMMA	0xA0	TBC	TBC
		DIMMB	0xA4	TBC	TBC
	+3V_PCH	Touch Pad	0X2C	TBC	TBC
SOC_SML0CLK SOC_SML0DATA	+3V_PCH	NA	NA	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3VS	EC	0x1A 0X19	TBC	TBC
		DGPU	0X96	TBC	TBC
		Thermal Sensor	0x4C	TBC	TBC
		LVDS	0X94~97 0X6A 0X6B	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port 1	+3VLP_EC	BAT	0x14 0X15	TBC	TBC
		CHGR	0x12	TBC	TBC
		G-Sensor	0x29	TBC	TBC
SMBUS Port 2					

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C 0	+3VS	Touch Panel	0x20	TBC	TBC
I2C 1	+3VS	NA	TBC	TBC	TBC

CPU Memory down vender control table

CPU_GPIO50 SDRAM_ID4	CPU_GPIO49 SDRAM_ID3	CPU_GPIO48 SDRAM_ID2	CPU_GPIO47 SDRAM_ID1	Vender	MD size	Vender descipti on	Note	Project
0	0	0	0	X	X	X	SODIMMx2 (A,B)	15"/17"
0	0	0	1	X	X	X	SODIMMx1(A) No MDx16bitx4pcs (B)	13"
0	0	1	0	Micron	256x16	MT41K512M16TNA-125:E	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	0	1	1	Samsung	256x16	4B8G1646Q-MYK0	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	1	0	0	Hynix	256x16	H5TC8G63AMR-PBA	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	1	0	1	Micron	512x8	MT41K512M8RG-107:N	MDx8bitx8pcs (A) SODIMMx1(B)	14"
0	1	1	0	Samsung	512x8	K4B4G0846Q-HYK0	MDx8bitx8pcs (A) SODIMMx1(B)	14"
0	1	1	1	Hynix	512x8	H5TC4G83BFR-PBA	MDx8bitx8pcs (A) SODIMMx1(B)	14"

<USB2.0 port>

USB2.0 port	DESTINATION UMA	DESTINATION Dis
0	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
1	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
2	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
3	USB 2.0/3.0(right side)	USB 2.0/3.0(right side)
4	WLAN/BT	WLAN/BT
5	Camera	Camera
6	X	X
7	FingerPrint	FingerPrint

<PCI-E,SATA,USB3.0>

Lane#	PCI-E		SATA	USB3.0	DESTINATION UMA	DESTINATION Dis
1				1	USB3.0	USB3.0
2				2	USB3.0	USB3.0
3	1			3	USB3.0	USB3.0
4	2			4	USB3.0	USB3.0
5	3				10/100/1000 LAN	10/100/1000 LAN
6	4				Card reader(PCI-E)	Card reader(PCI-E)
7	5					GPU(DIS only)
8						GPU(DIS only)
9						GPU(DIS only)
10						GPU(DIS only)
11	6	L0	3		WLAN	WLAN
12		L1	2		ODD	ODD
13		L2	1		HDD	HDD
14		L3	0		SSD	SSD

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Title: Notes List

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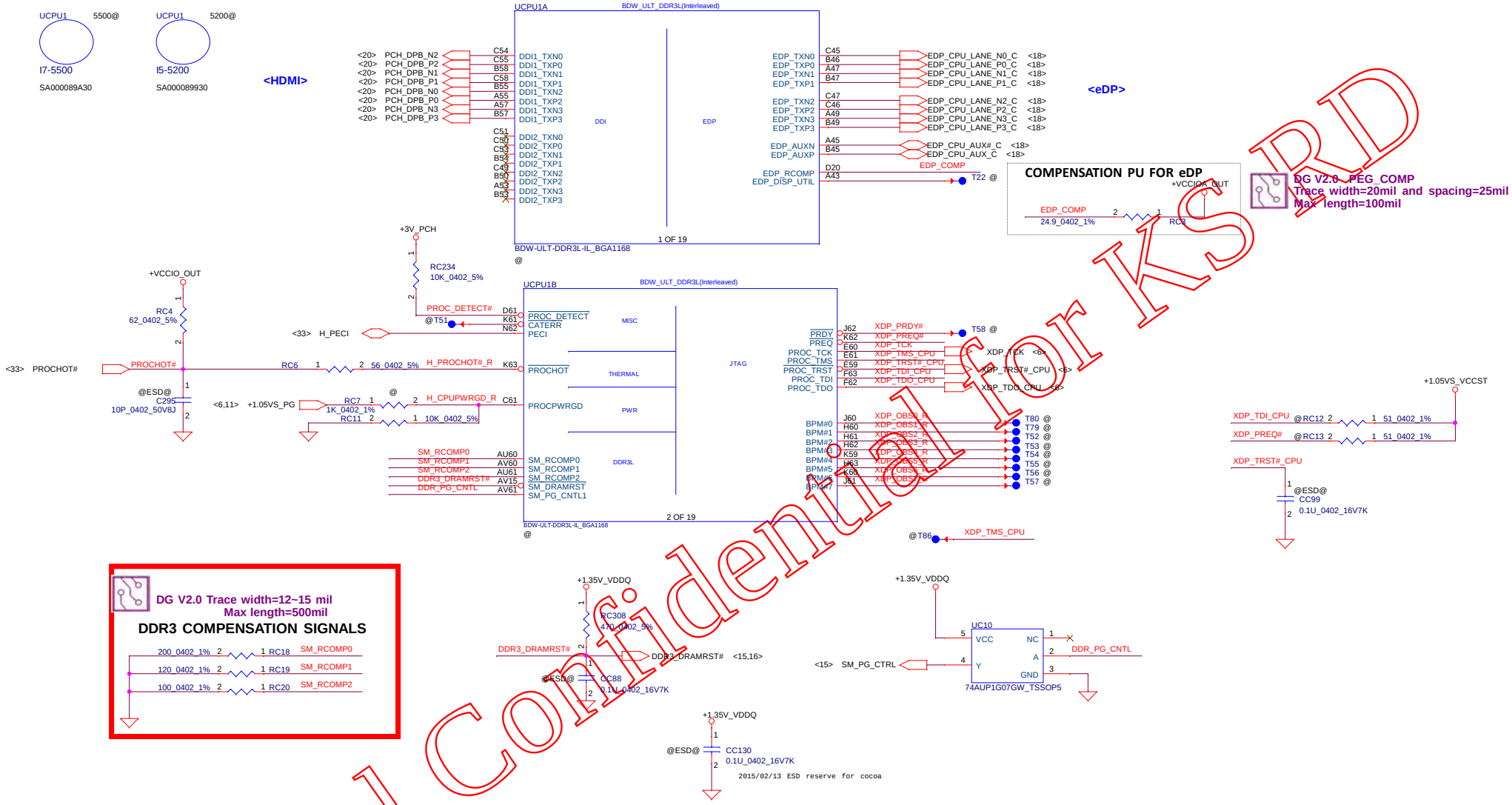

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Title: DDI,MSIC,XDP

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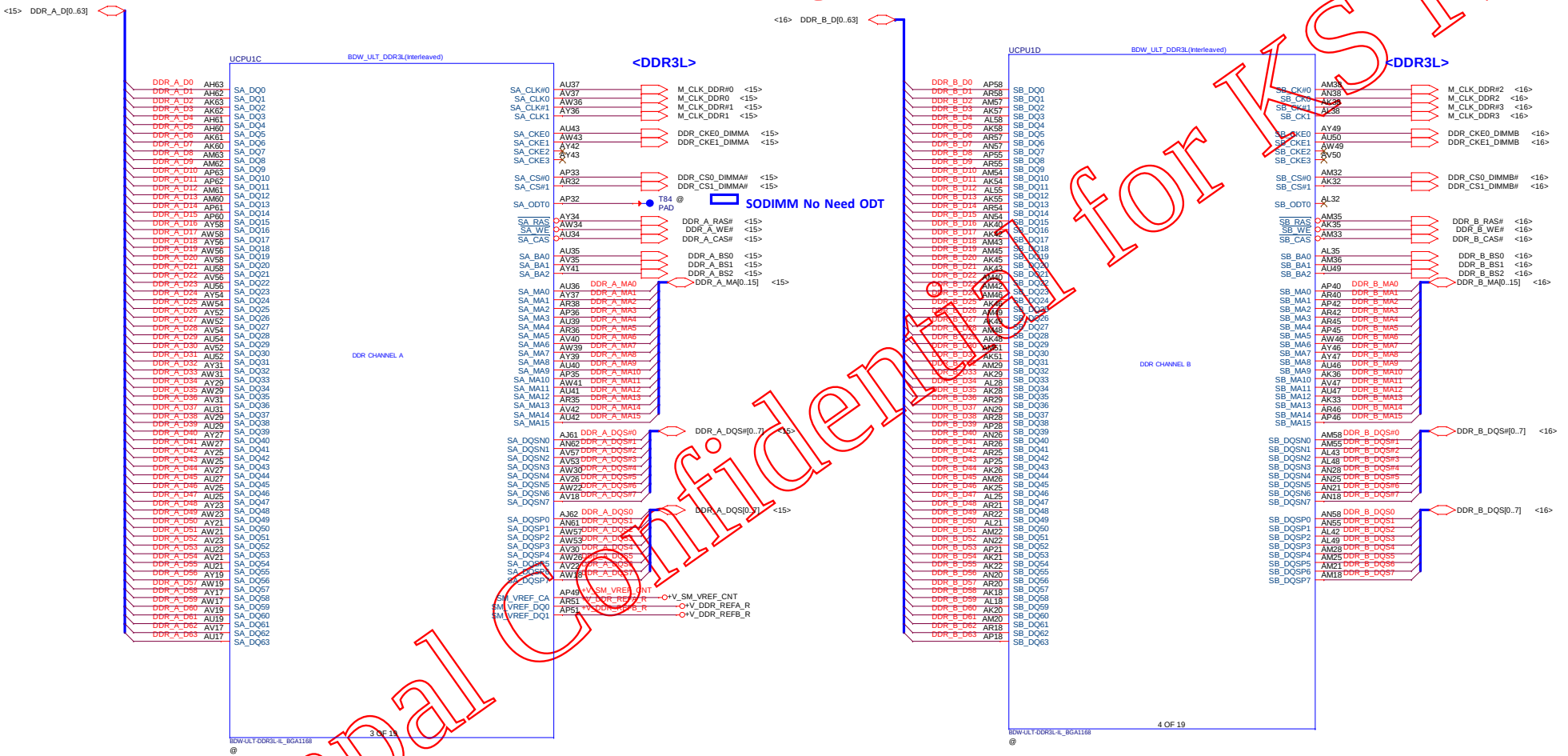
Interleaved Memory



Interleaved Memory

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Title	DDRIII		
Size	Document Number		Rev
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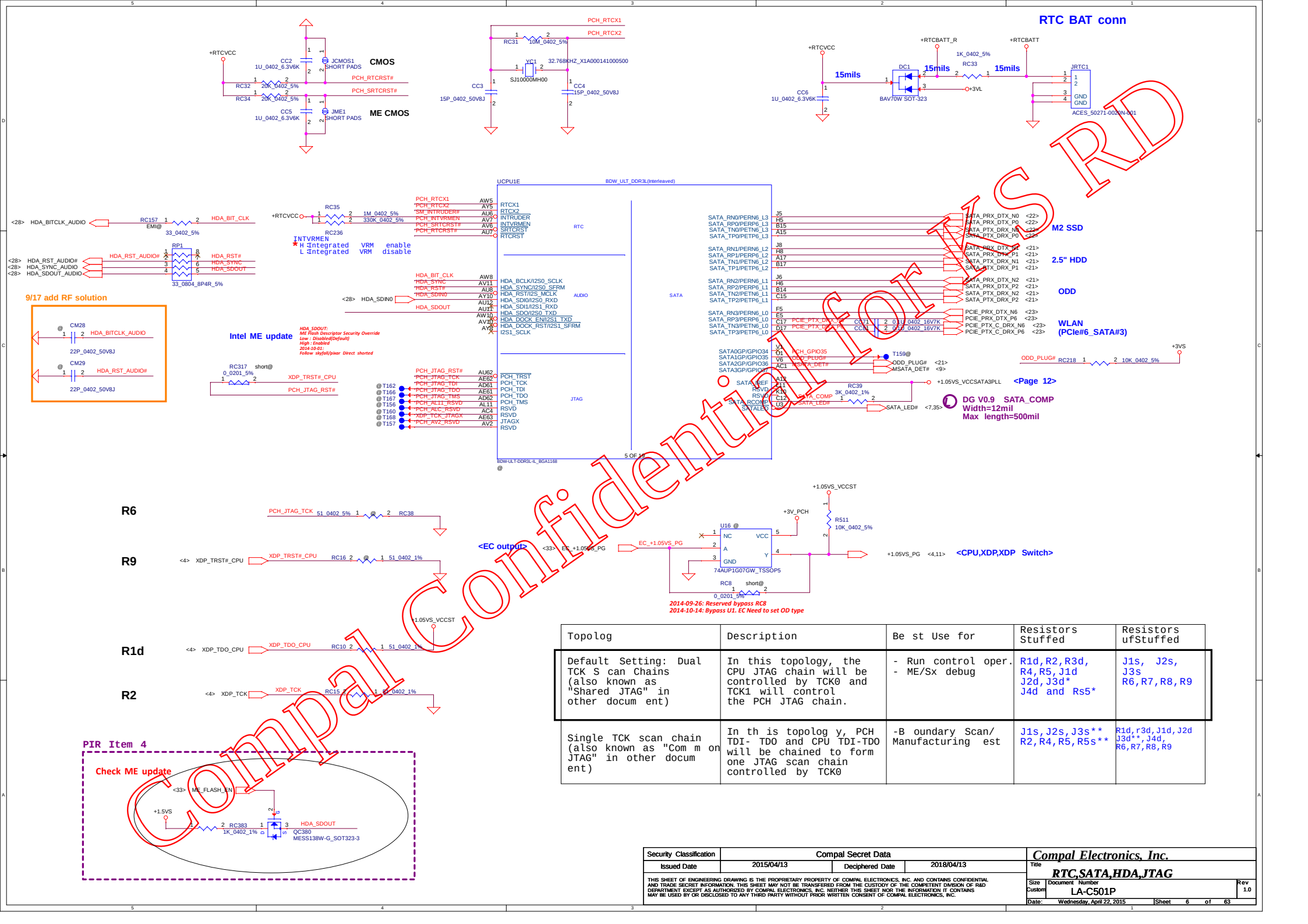

Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s, J2s, J3s** R2, R4, R5, R5s**	R1d, r3d, J1d, J2d J3d**, J4d, R6, R7, R8, R9

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Title: RTC,SATA,HDA,JTAG

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Intel #521772 : PCICLKRQ_Usage_Guidelines
Mapping
– Each PCIECLKRQn# needs to be routed to PCIE Port (n+1) – New to LPT-LP and what is not clear in EDS. Updated in LPT-LP EDS SU Rev1.5.1 (#508767).
– Each CLKOUT_PCIE[5:0] can be assigned to any PCIECLKRQn#

LAN(PCIe#3)

CardReader(PCIe#4)

GPU(PCIe#5)

WLAN(PCIe#6_SATA#3)

UCPU1F
BDW_ULT_DDR3L(Interleaved)
CLOCK
SIGNALS
6 OF 19
BDW-ULT-DDR3L-IL_BGA1168

UCPU1G
BDW_ULT_DDR3L(Interleaved)
LPC
SMBUS
SPI
C-LINK
7 OF 19
BDW-ULT-DDR3L-IL_BGA1168

<Page12>

<XDP CLK reserve TP>

<EC>

9/17 add RF solution

SPI ROM 8M

EON SA000046400 S IC FL 64M EN25Q64-104HIP SOP 8P
MXIC SA00006N100 S IC FL 64M MX25L6473EMI-10G SOP 8P
WINBOND SA000039A30 S IC FL 64M W25Q64FVSSIQ SOIC 8PI SPI ROM
Micron SA00005L100 S IC FL 64M N25Q064A13ESC40F SOP8 8P

CPU THERMAL SENSOR

Thermal sensor SMBus address --> 100-1_100xb : 0x4C
(x=0)Write Address(0x98h)
(x=1)Read Address(0x99h)

Thermal sensor SMBus address -->0111_100xb (0x78h)

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Title: CLK,SPI,SMB,LPC

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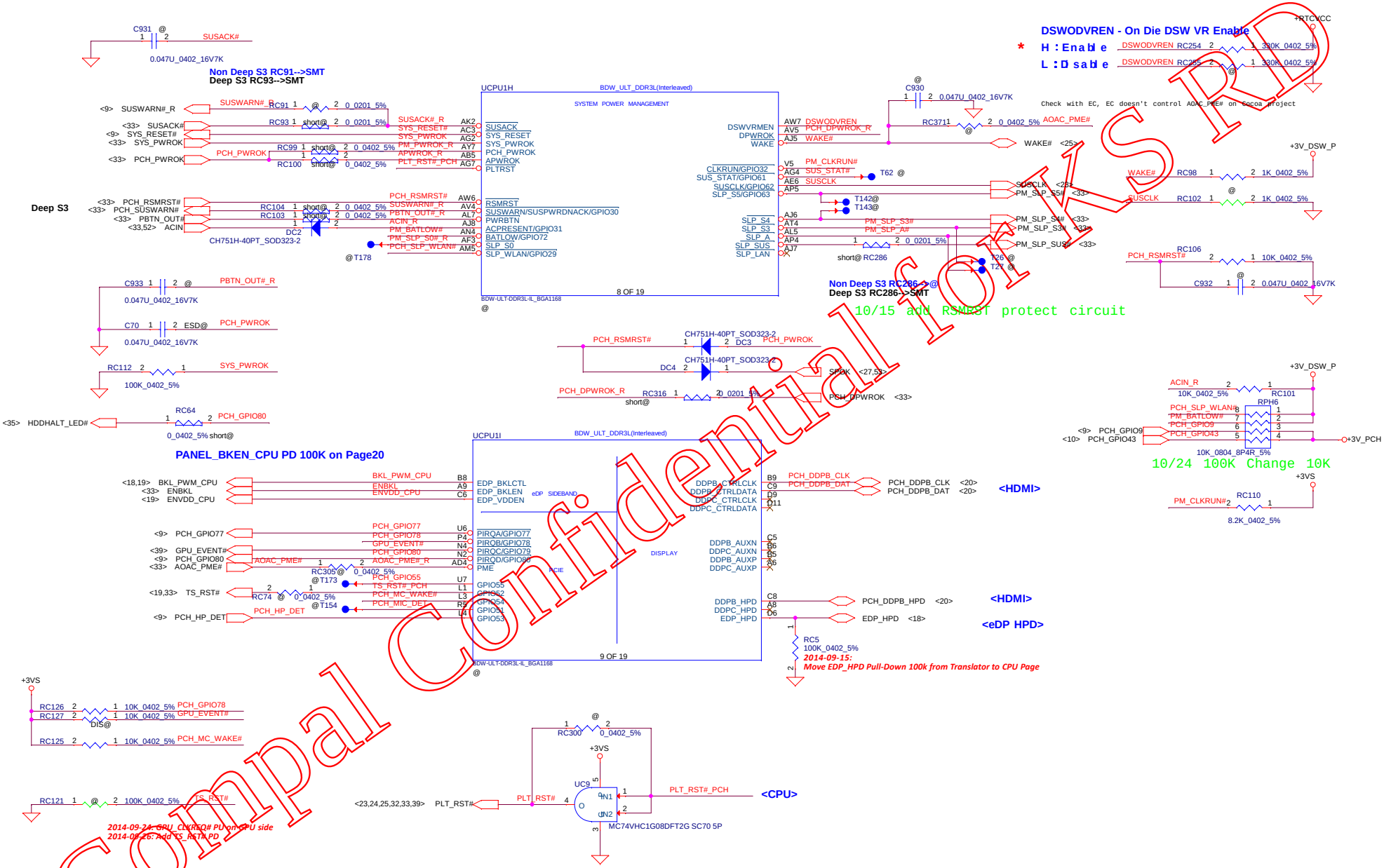

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Title: PM,GPIO,DDI		
Size: Custom	Document Number: LA-C501P	Rev: 1.0
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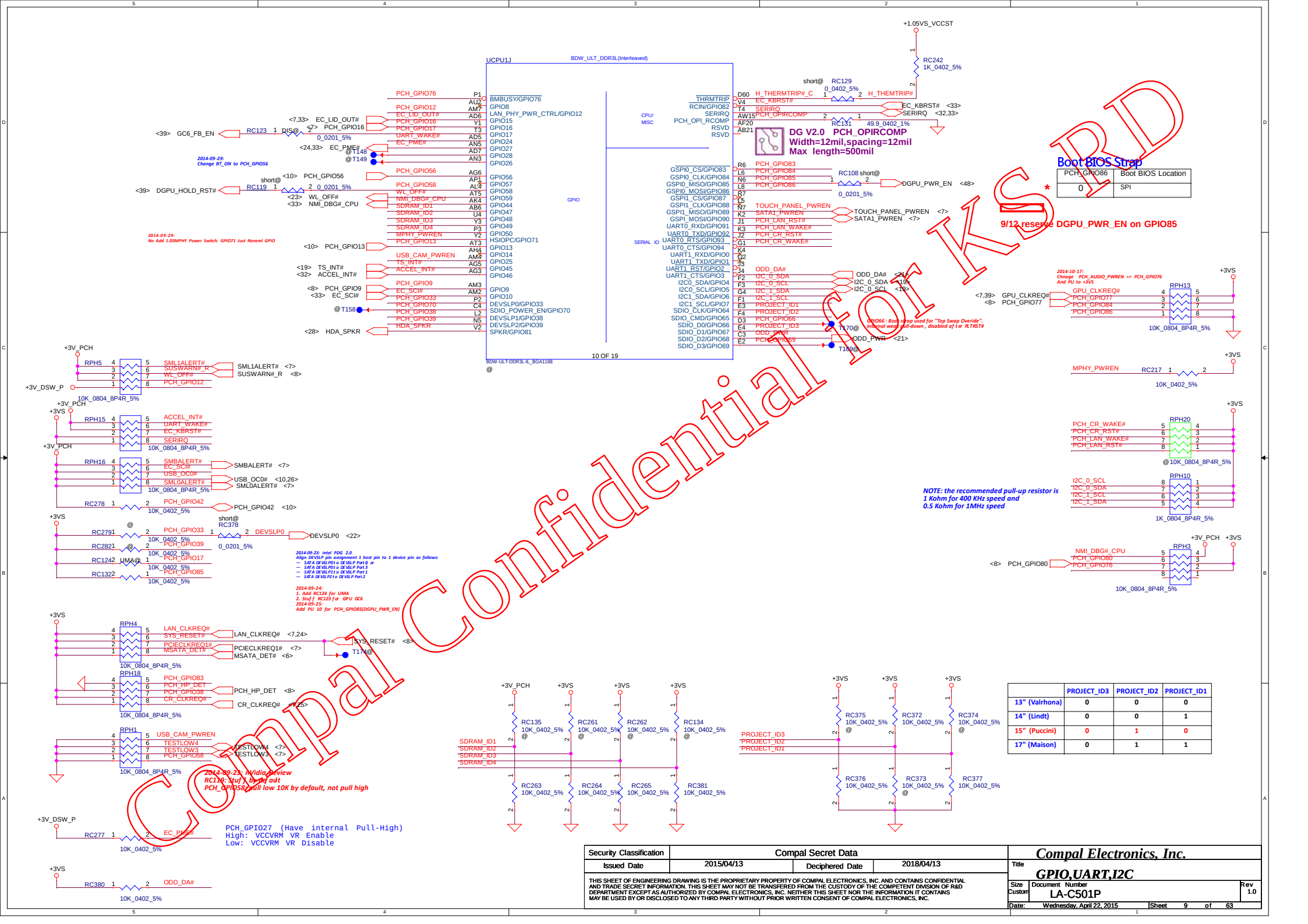

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Title: **GPIO,UART,I2C**

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change AC cap to 0.22uF review by Nvidia

UCPU1K

BDW_ULT_DDR3L(Interleaved)

PEG(PCIe#5)

LAN(PCIe#3)

CardReader(PCIe#4)

USB2.0/USB3.0

15"/17" only USB2.0/USB3.0

<Page12>

DG V2.0 PCIE_RCOMP
Width=12mil,spacing=12mil
Max length=500mil

USB2.0/USB3.0

USB2.0/USB3.0 EHCI Port1 : DebugPort

USB2.0/USB3.0(ChargingPort)

USB2.0/USB3.0 15"/17" only

W/LAN/BT

Camera

Touch screen

Finger print

USB2.0/USB3.0

USB2.0/USB3.0(ChargingPort)

DG V2.0 USBRBIAS
Trace width=50ohm and spacing=15mil
Max length=500mil

OC#: Signals must NOT float if they are not being used
intel BDW PDG v2.0
Overcurrent Pin Default Usage:
OC0# : Port0,1
OC1# : Port 2,3
OC2# : Port 4,5
OC3# : Port 6,7

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Title: PCIE,USB

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+VCC_CORE@10000mA

SVID ALERT

<PWR VR12.6> <56> VR_SVID_ALRT# — RC1551 43_0402_1% — H_CPU_SVIDALRT#

+1.05VS_VCCST — RC154 75_0402_5% — H_CPU_SVIDALRT#

DG V0.5 H_CPU_SVIDALRT#
RC154 close to CPU<300mil
Max length=1000~2000mil

SVID DATA

<PWR VR12.6> <56> VR_SVID_DAT — VR_SVID_DAT

+1.05VS_VCCST — RC156 130_0402_1% — VR_SVID_DAT

DG V0.5 VIDSOUT
RC156 close to CPU<500mil
Max length=1000~2000mil

VCC_SENSE

<PWR VR12.6>

PH on power page

<56> VCCSENSE — VCCSENSE

+VCCIO_OUT — +VCCIOA_OUT

<VR IV and CPU>
<EDP_COMP power rail>

<56> VR_SVID_CLK — VR_SVID_CLK

<56> VR_SVID_DAT — VR_SVID_DAT

<56> VGATE — VGATE — RC87 short@ — <56> VR12.5_VR_ON — 0_0402_5%

<4,6> +1.05VS_PG — VR12.6PG_MCP

CPU_PWR_DEBUG

2014-09-23:
1.Follow intel VR12.6 and skyfall H5W
2.Remove UC8(74AUP1G07GW Buf f er) and RC288(10K)
3.Need to make sure VGATE is Pull-High 1.5kohm to VR_ON

+1.05VS — RC294 @ 0_0402_5% — +VCCIO_OUT

UCPU1L — BDW_ULT_DDR3L(Interleaved)

+1.35V_VDDQ — 2500mA

+VCC_CORE — 600mA

+1.05VS_VCCST

HSW ULT POWER

12 OF 19

BDW-ULT-DDR3L-IL_BGA1168

+1.05VS_VCCST — RC166 150_0402_5% — CPU_PWR_DEBUG — 10K @RC167 0402_5%

+1.05VS — RC2231 short@ 0_0805_5% — +1.05VS_VCCST

CC20 2.2U_0402_6.3V6M
CC21 2.2U_0402_6.3V6M @
CC22 2.2U_0402_6.3V6M
CC23 2.2U_0402_6.3V6M
CC24 330U_2V_D2_LESR9ME_EFSX_H1.9 — SGA20331E10
CC26 10U_0603_6.3V6M
CC27 10U_0603_6.3V6M @
CC28 10U_0603_6.3V6M
CC29 10U_0603_6.3V6M @
CC30 10U_0603_6.3V6M
CC31 10U_0603_6.3V6M @

<PV> Reserve CC24

<Cocoa> Del reserve CC25 330u OSCON cap

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Title: Power

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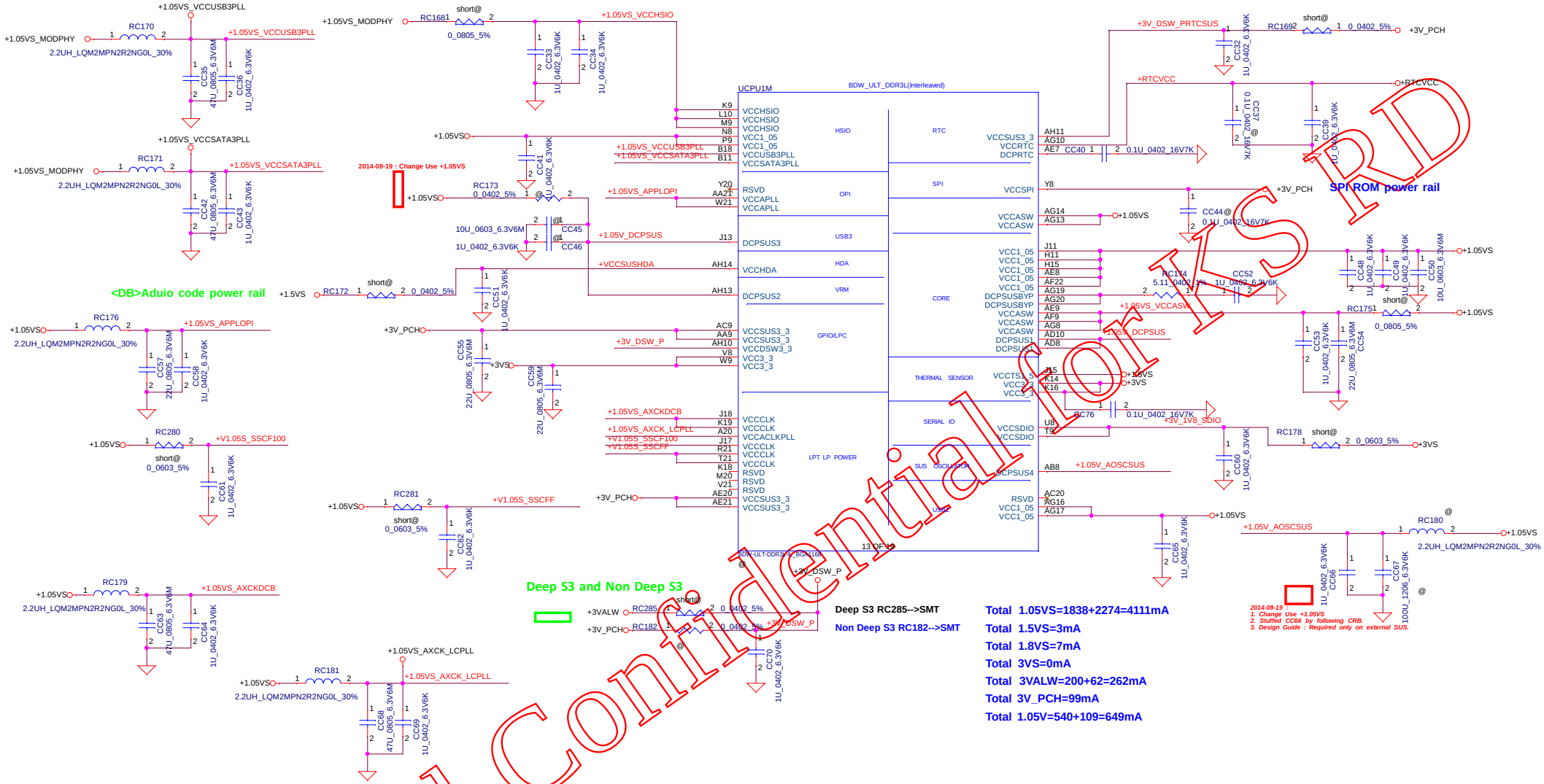

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Title: **Power**

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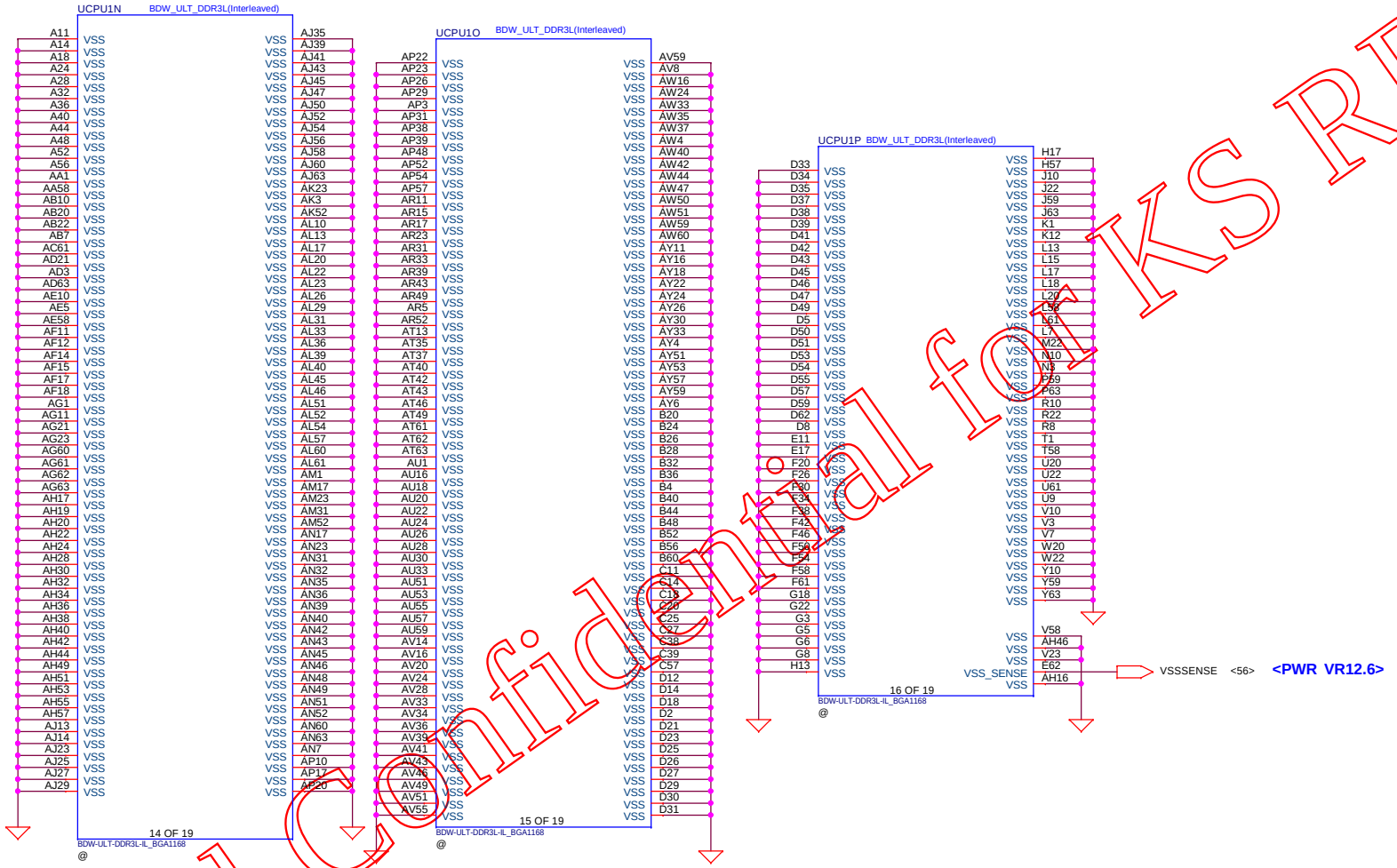

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Title	GND/VSSSEN	
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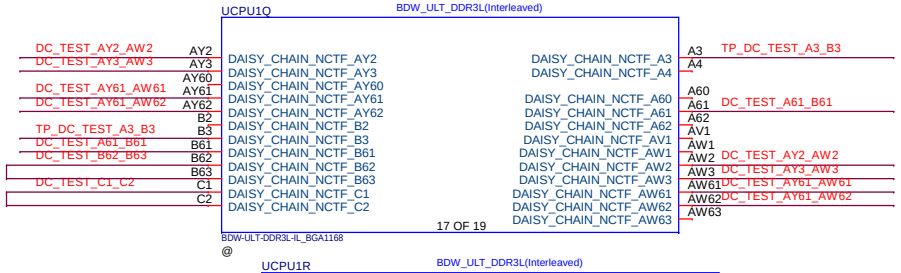
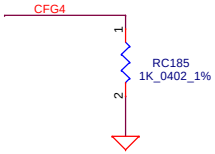
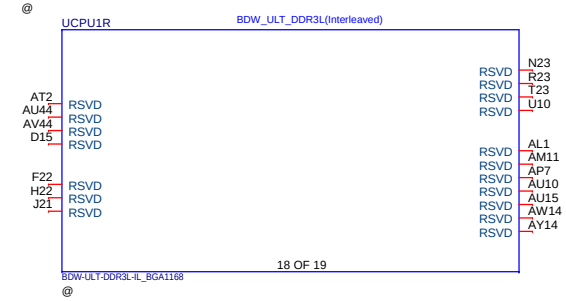
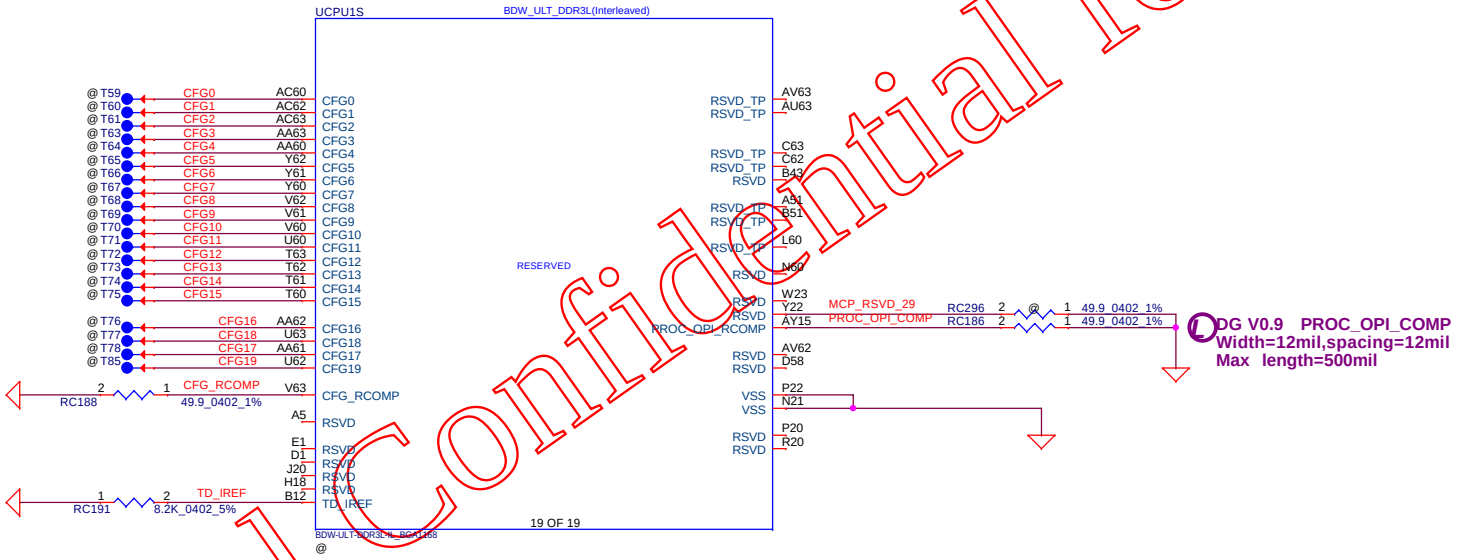




Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port





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Title: **RSVD/CFG**

Size	Document Number	Rev
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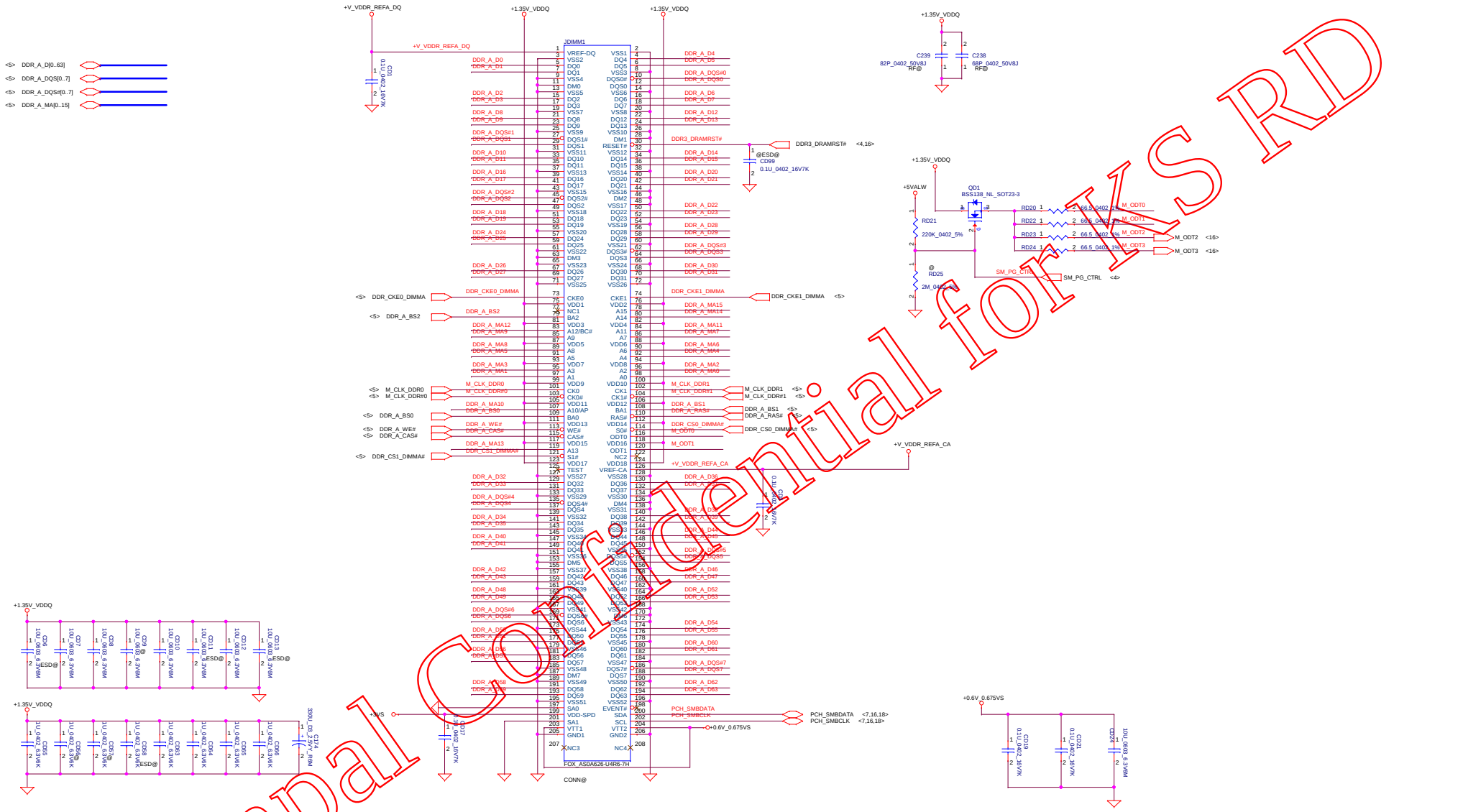

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Title: DDR3L DIMM0

Size	Document Number	Rev
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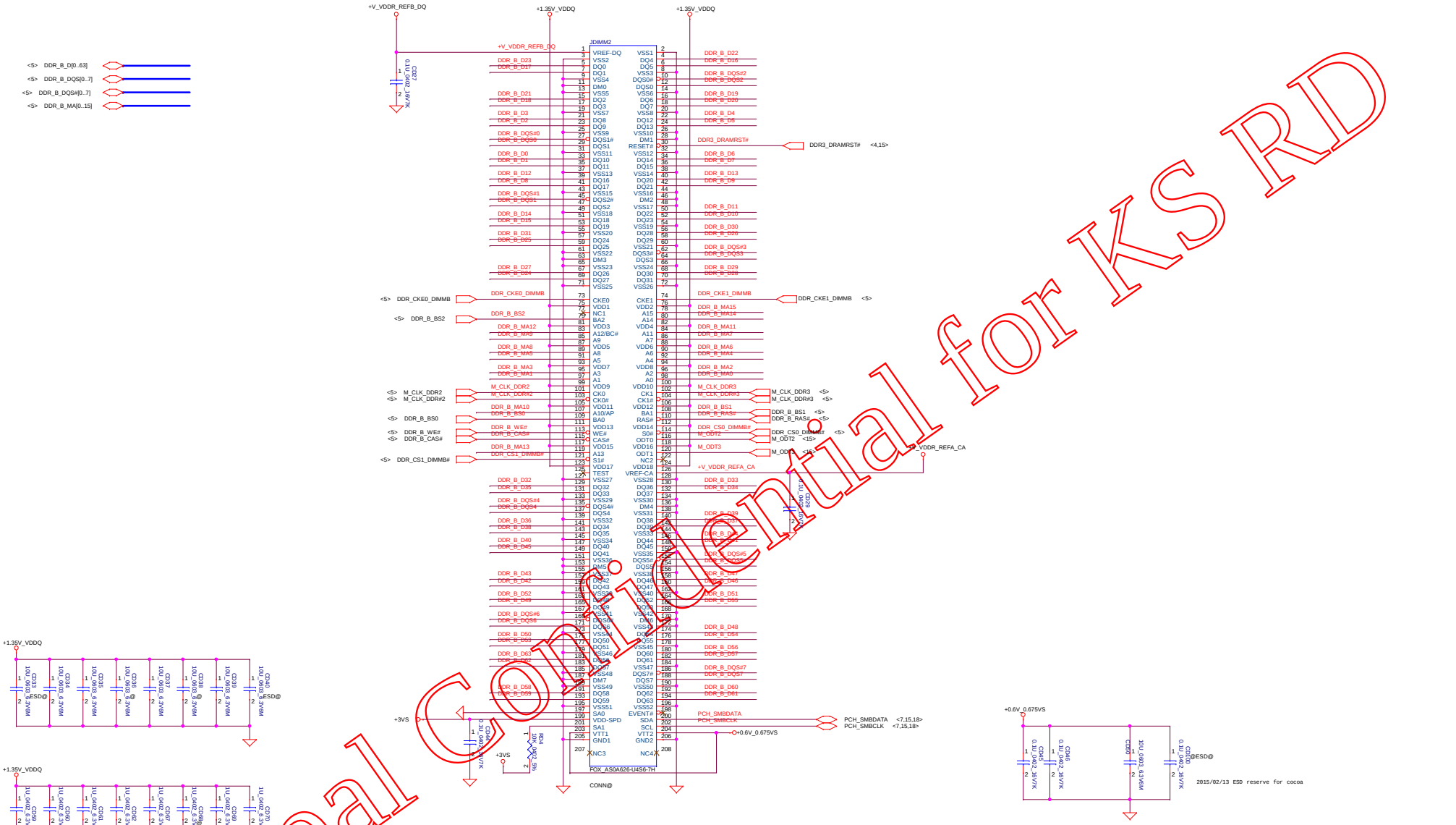

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Title: DDR3L DIMM1

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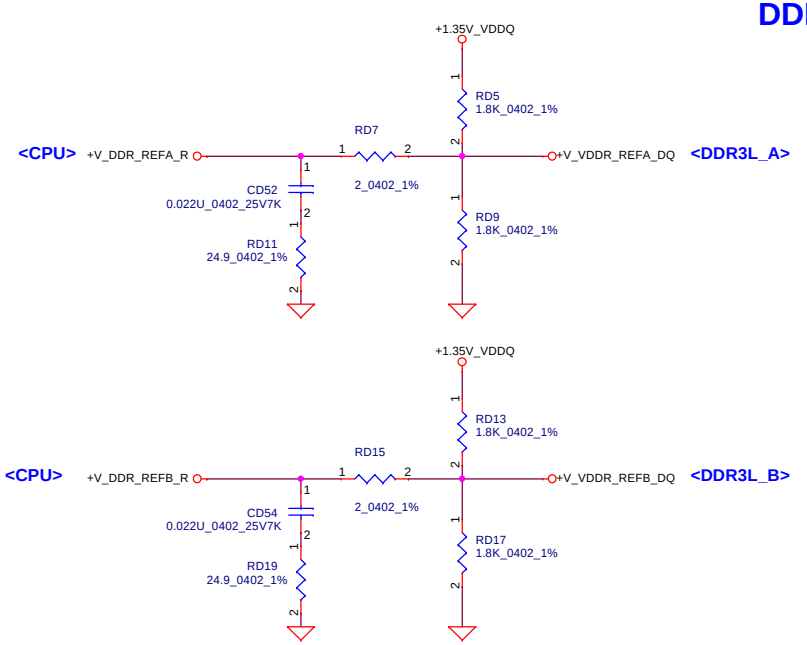
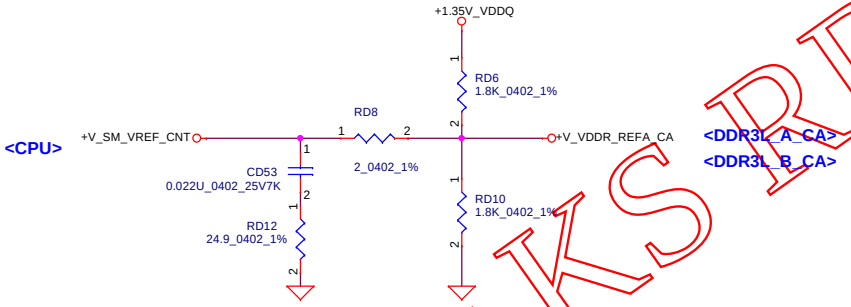
DDR3L VREF





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Title: **DDR3L VREF**

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Title: *LVDS Translator-RTD2132R*

Size | Document Number: **LA-C501P** | Rev: 1.0

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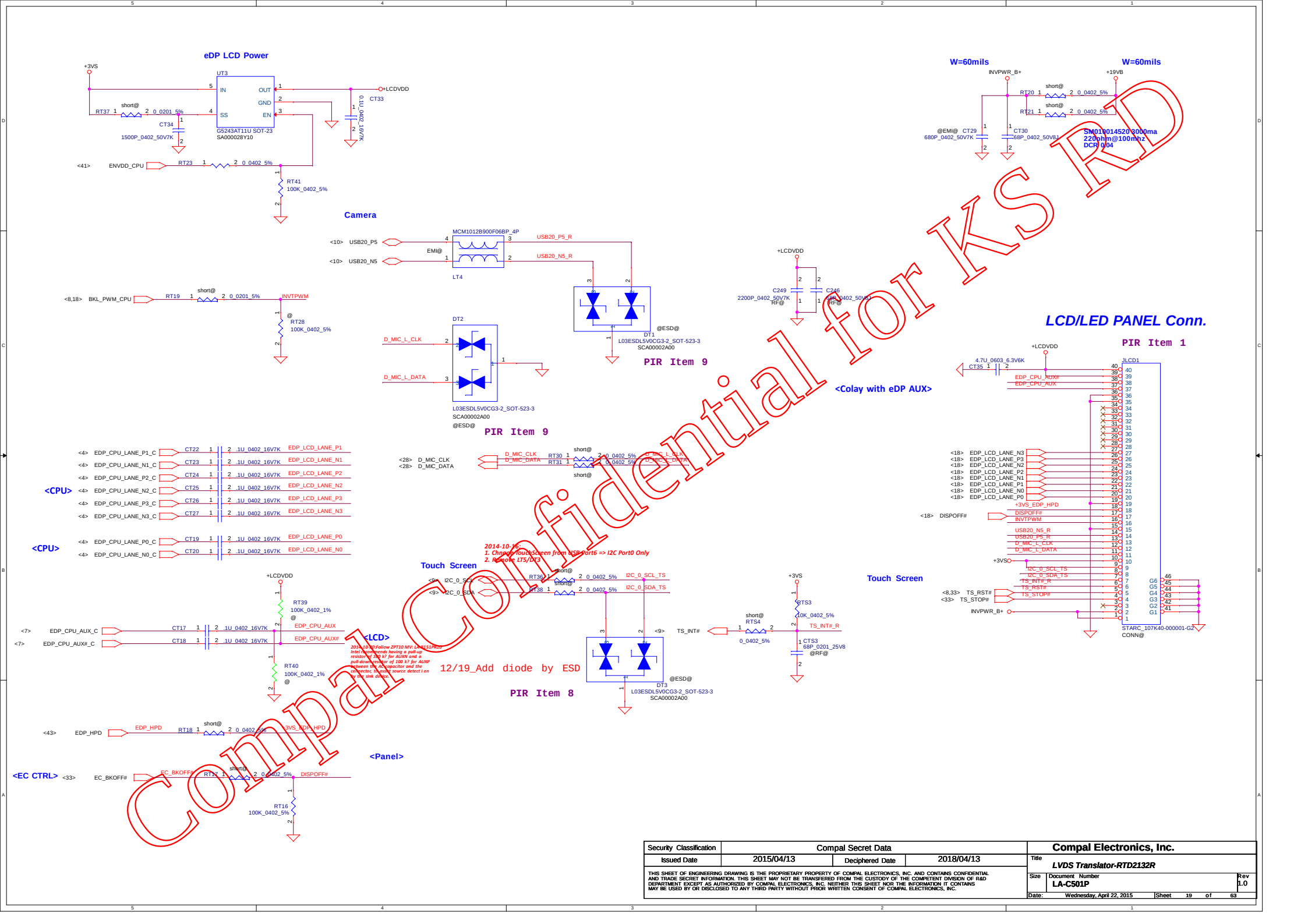

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: *LVDS Translator-RTD2132R*

Size	Document Number	Rev
	LA-C501P	1.0

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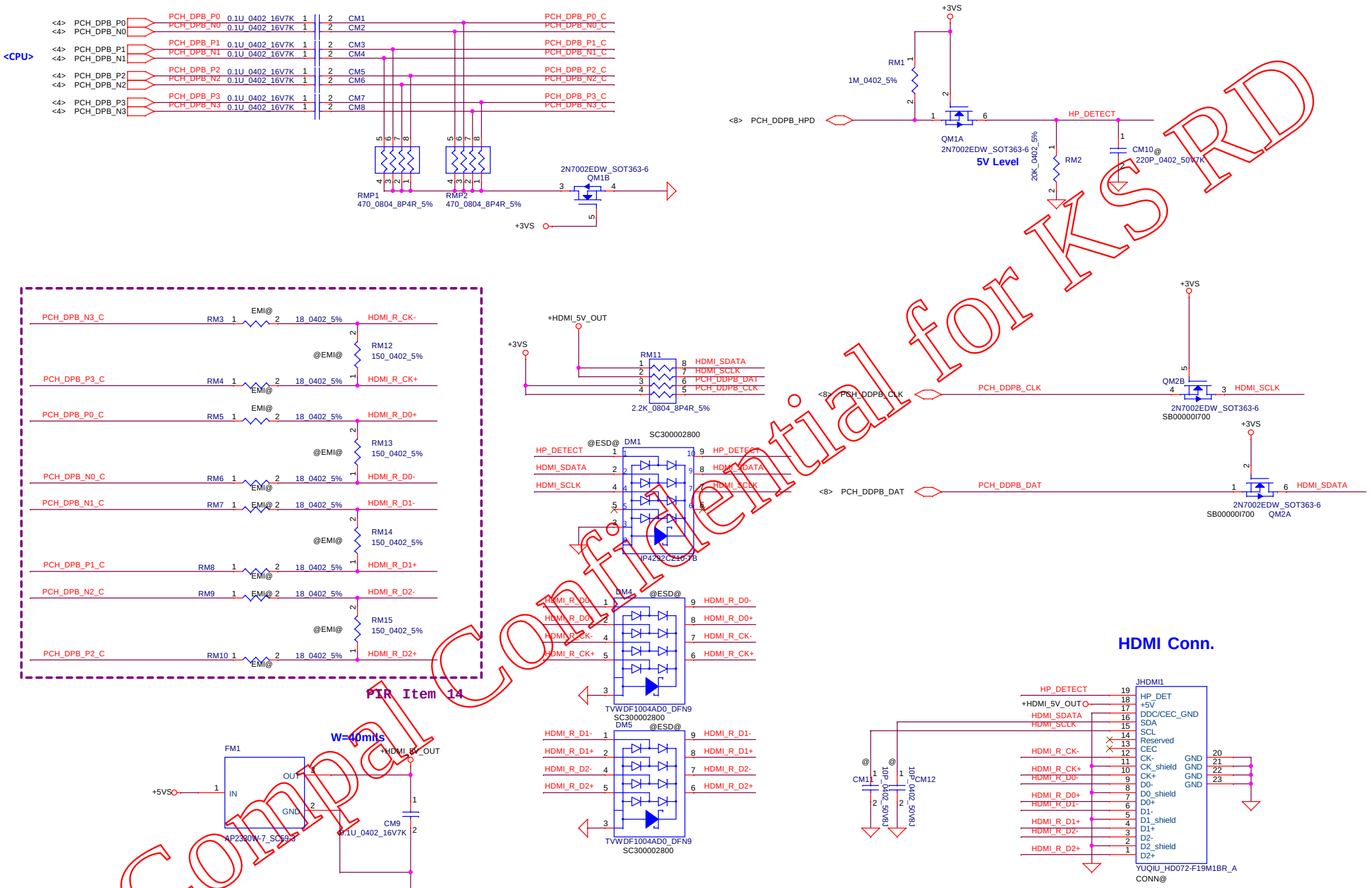


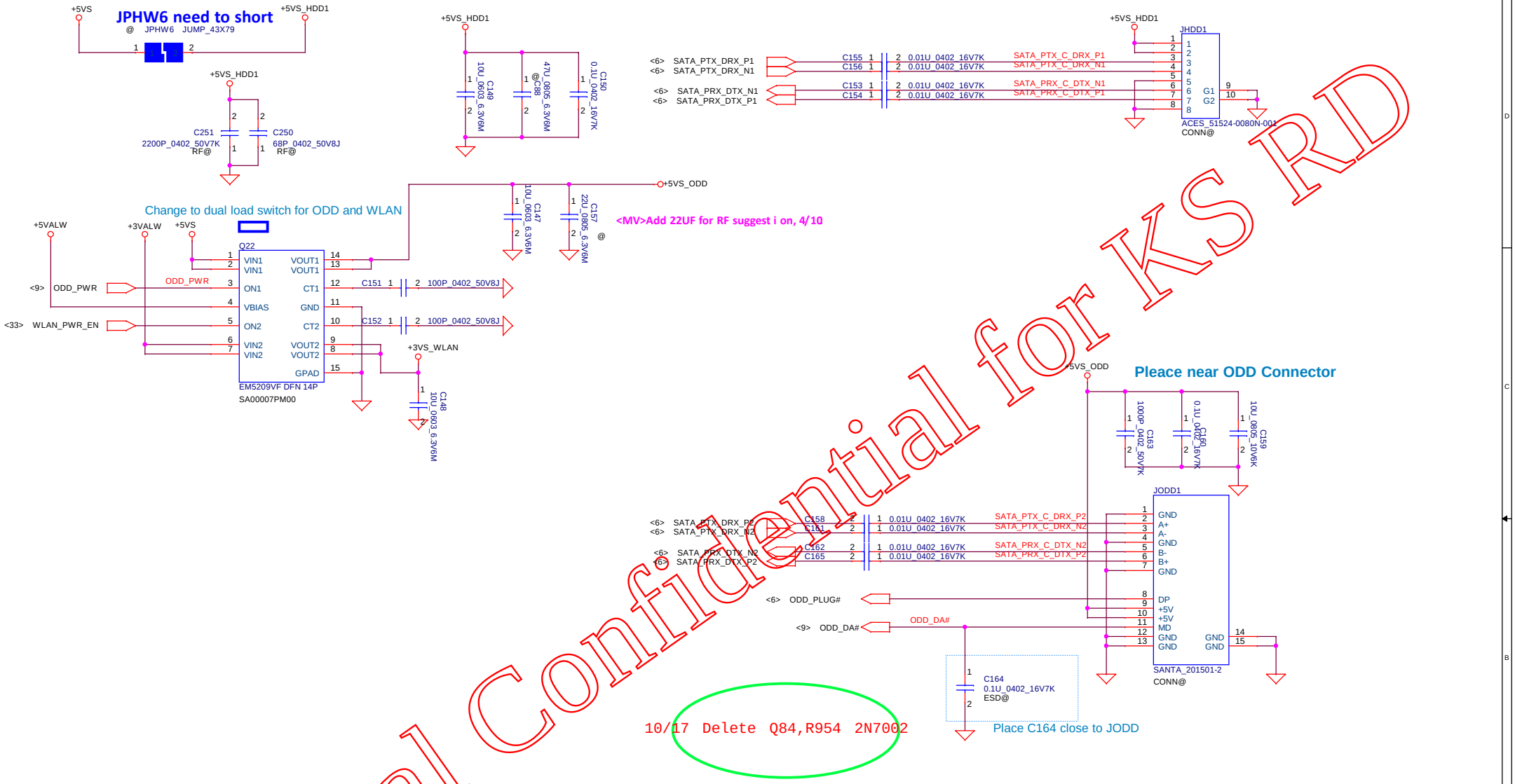
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **HDMI_Conn/Level shift**

Size	Document Number	Rev
	LA-C501P	1.0

Date: Wednesday, April 22, 2015 | Sheet 20 of 63



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

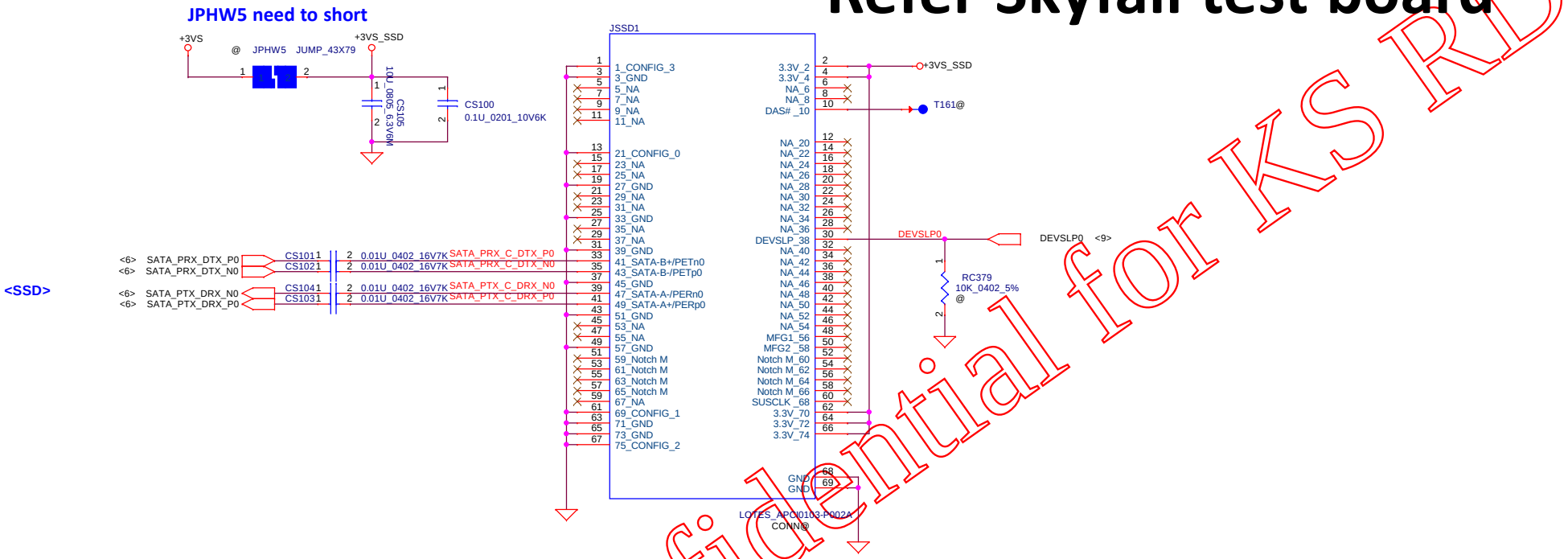
Compal Electronics, Inc.

Title: ODD/SATA Conn

Size: Custom | Document Number: LA-C501P | Rev: 1.0

Date: Wednesday, April 22, 2015 | Sheet 21 of 63

Refer Skyfall test board



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

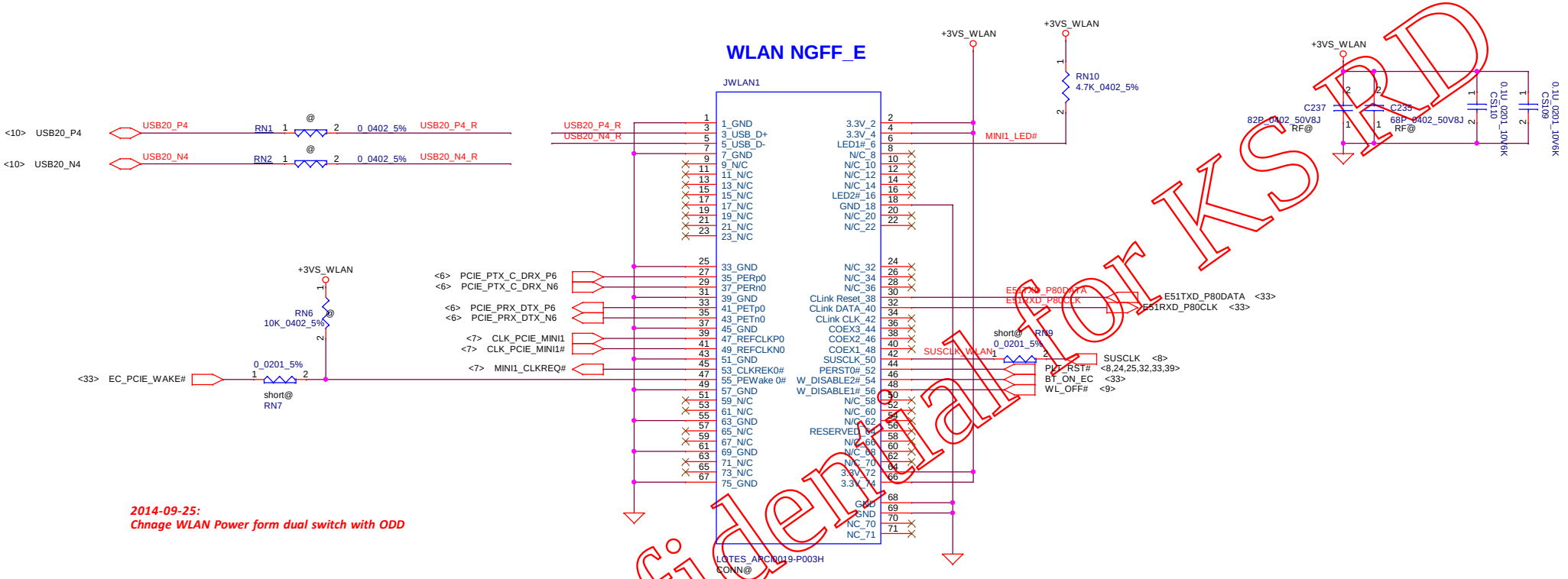
Compal Electronics, Inc.

Title: eDP to CRT

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 22 of 63

Refer Skyfall NGFF



2014-09-25:
Chnage WLAN Power form dual switch with ODD

WLAN
NGFF Key_E 67P P0.5 CH 0.32 H2.2 STD

Del +1.5VS_WLAN

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **WLAN**

Size	Document Number	Rev
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JHW1 need to short

+LAN_VDD_3V3 Rising t i me need>0.5mS and <100mS

RTL8111HSH-CG=> Switching Regulator Only

Place Note :
CL12&CL13 close UL1 Pin 3,8
CL14 & CL15 close UL1_Pin22
CL26 & CL27 close UL1_Pin30

LL2, CL8, CL23 for 8161
CL8 & CL123 close LL2

Place CL11~CL13 close UL1 Pin 3, 8 , 22

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

CL10& CL16 close to UL1: Pin 23

SP050005L00 Footprint

Amber

White

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **LAN 8111G**

Size	Document Number	Rev
	LA-C501P	1.0

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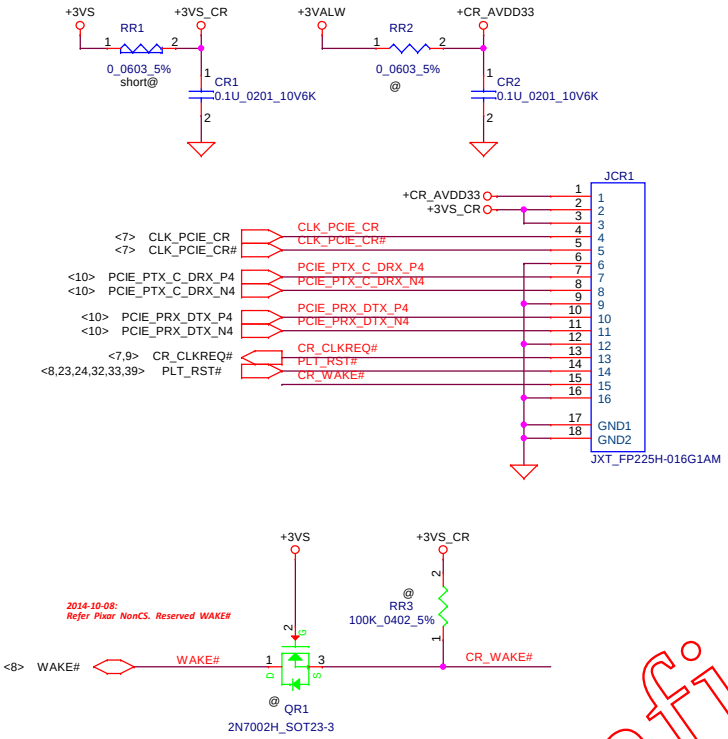
CardReader on Suboard



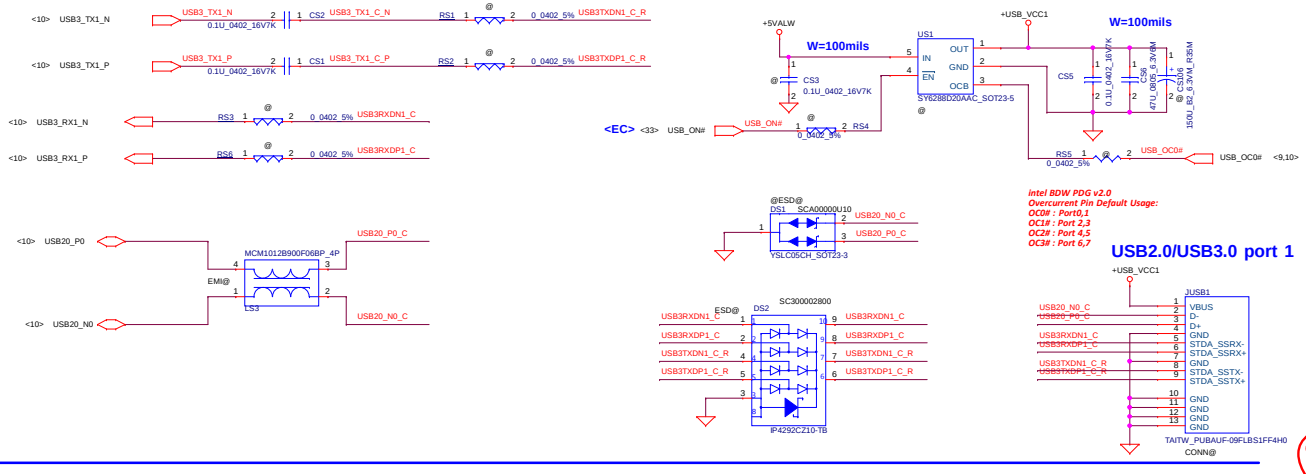
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

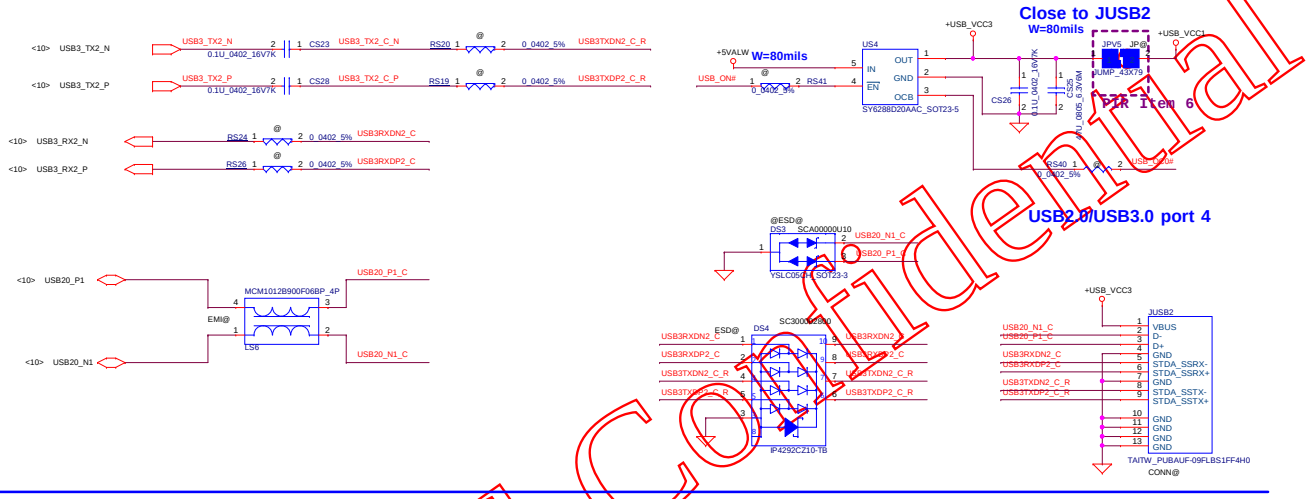
Title: **Card Reader_RTS5237S-CG**

Size	Document Number	Rev
	LA-C501P	1.0

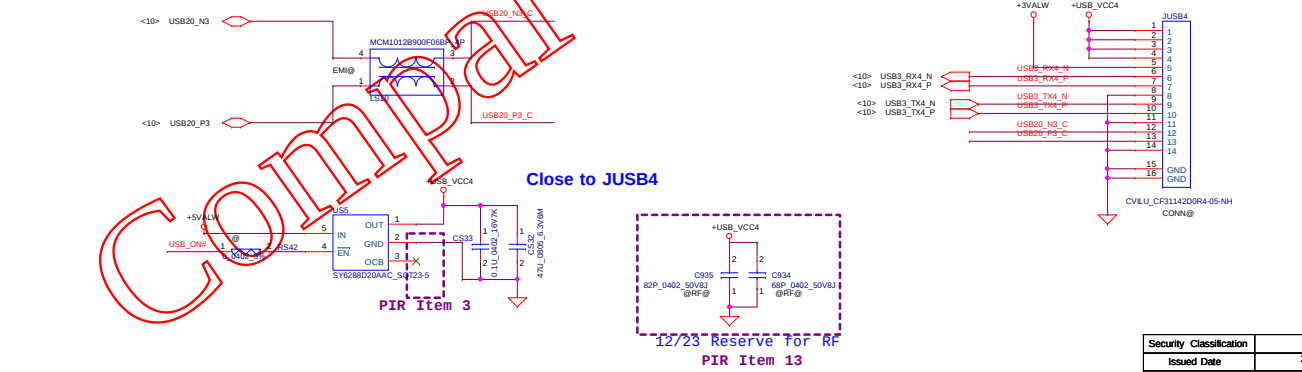
Date: Wednesday, April 22, 2015 | Sheet 25 of 63



EHCI Port1 : DebugPort



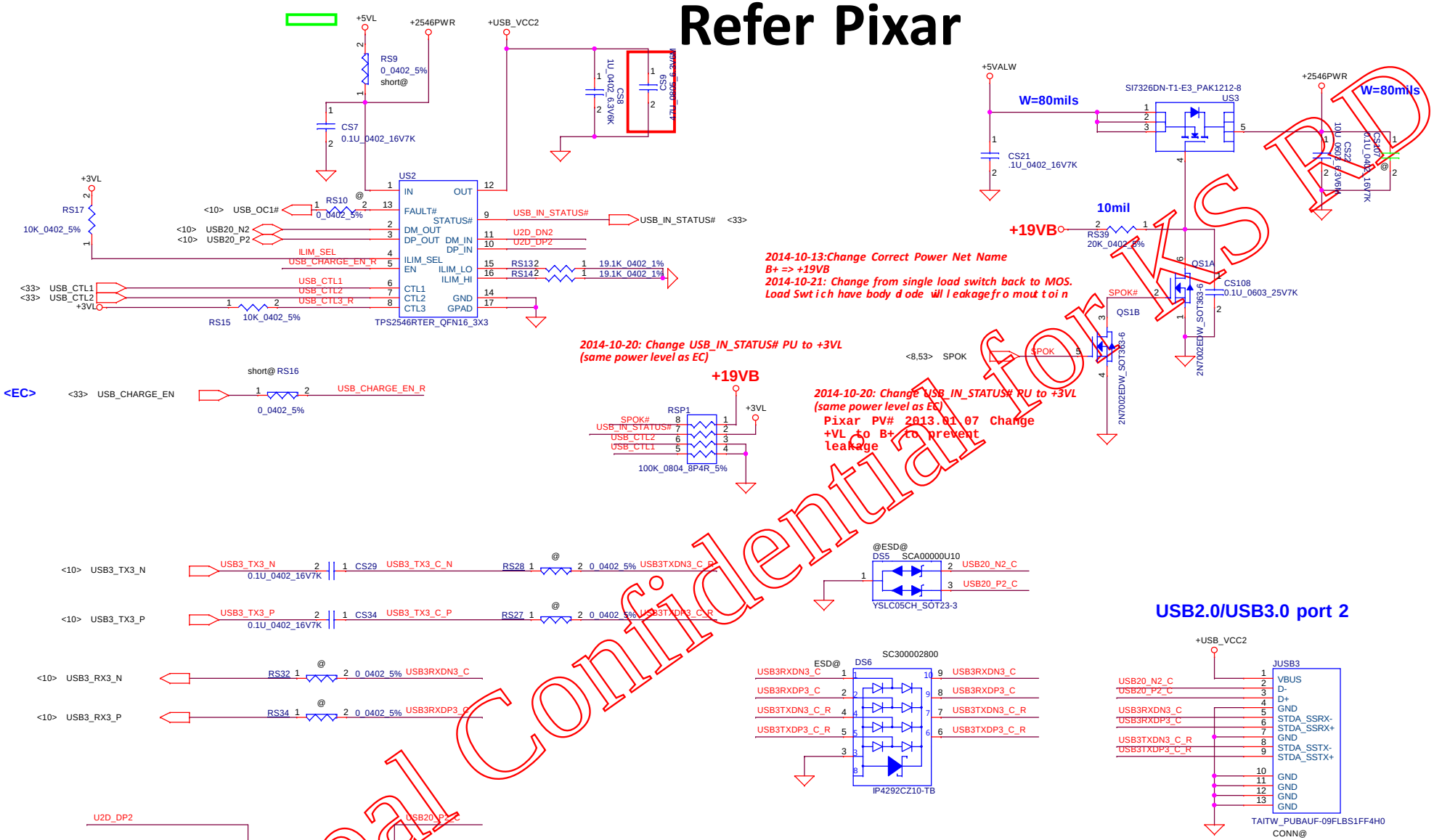
IO Suboard



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title	USB 3.0/2.0 conn		
Size	Document Number	LA-C501P	Rev 1.0
Date: Wednesday, April 22, 2015	Sheet 26 of 63		

Refer Pixar



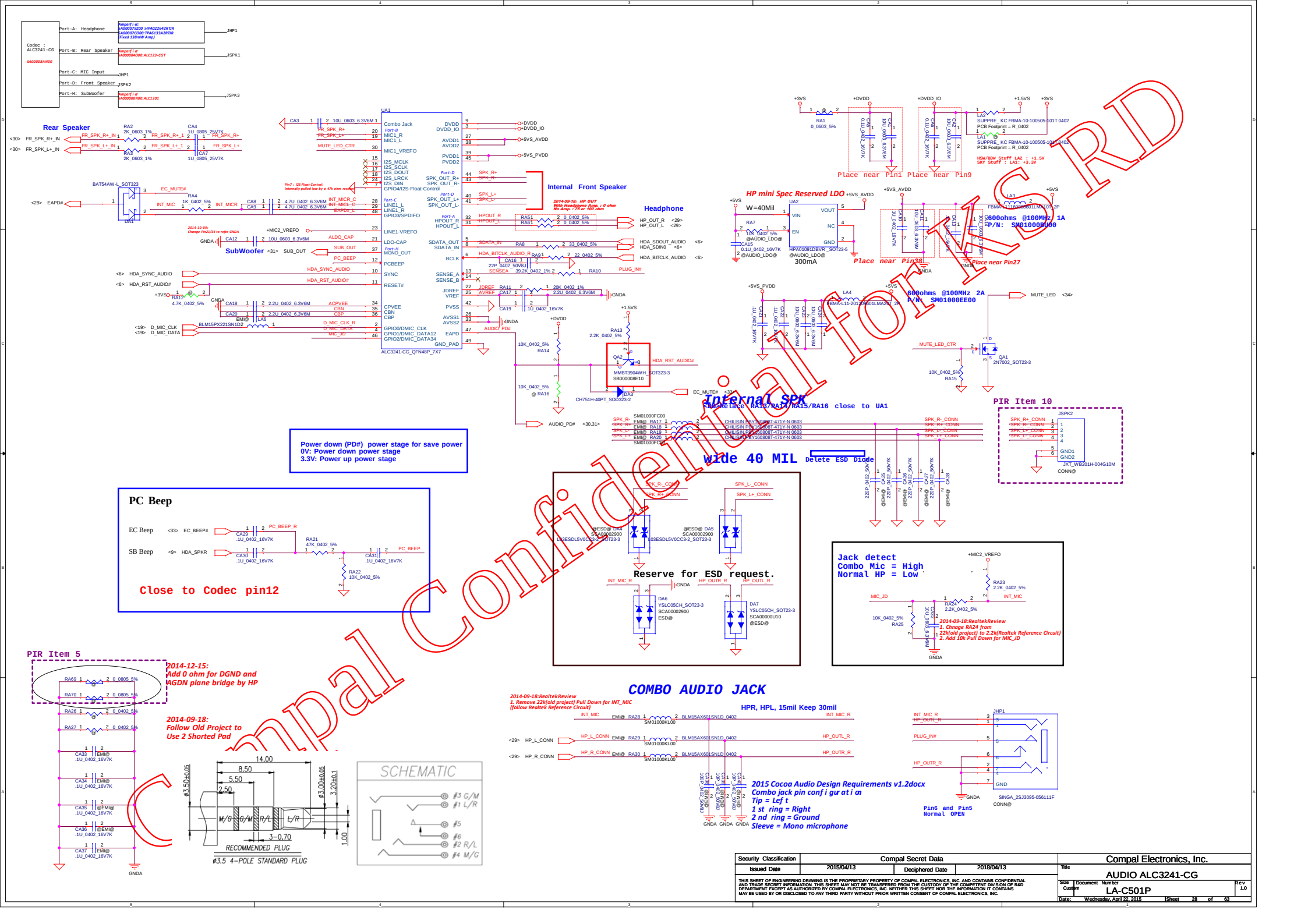
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: USB Charger

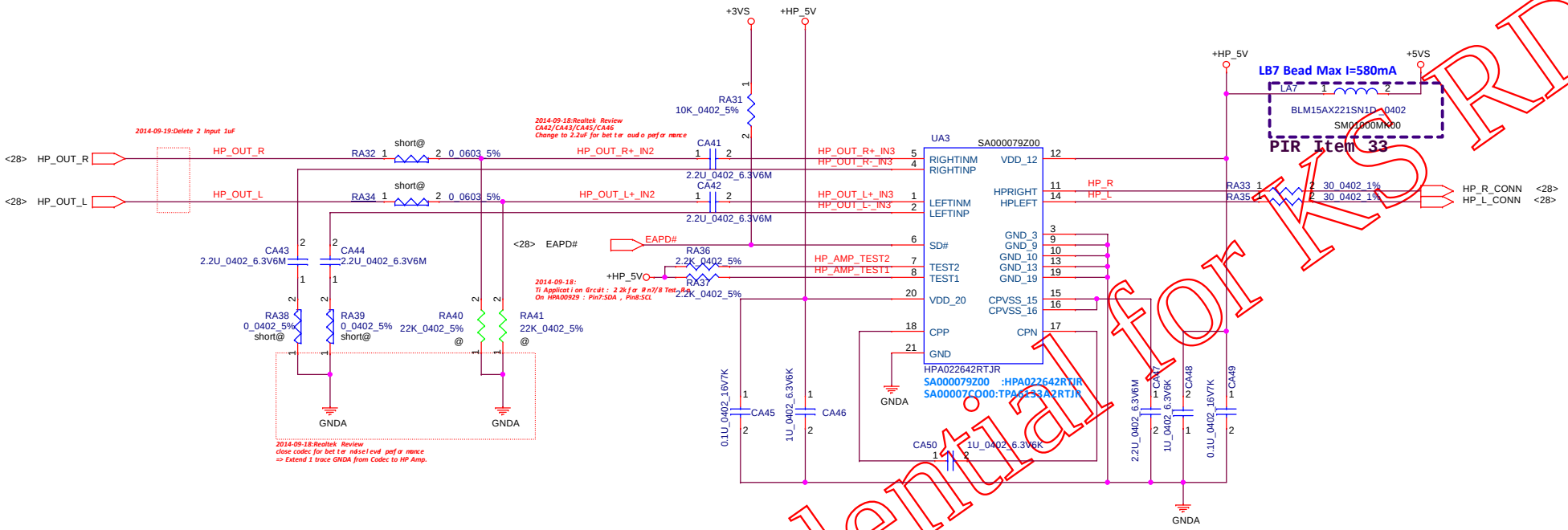
Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 27 of 63



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.	
Title	AUDIO ALC3241-CG
Size / Custom	Document Number: LA-C501P
Rev	1.0
Date:	Wednesday, April 22, 2015
Sheet	28 of 63



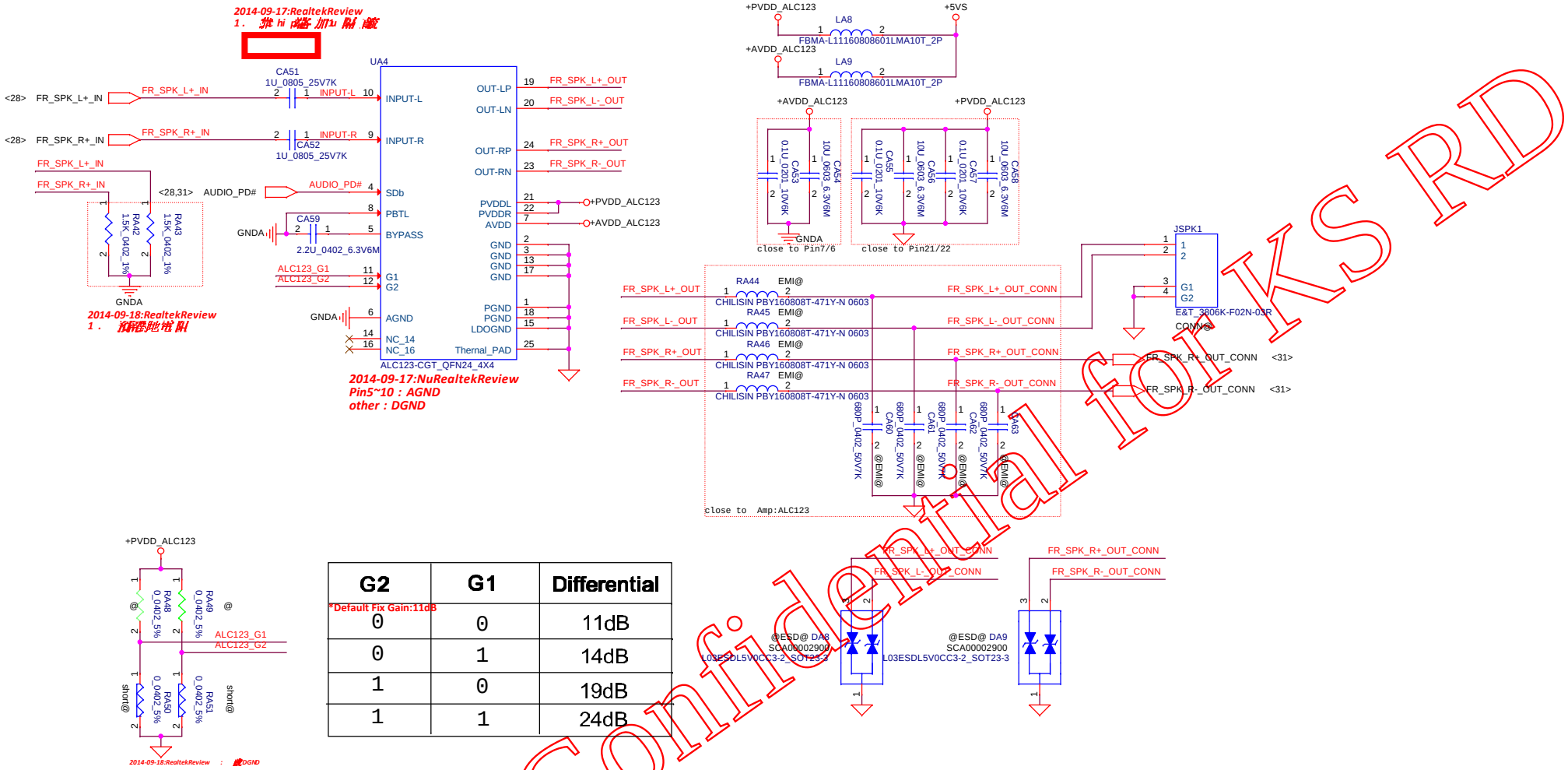
Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: Audio HP Amp

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 | Sheet 29 of 63



G2	G1	Differential
*Default Fix Gain:11dB		
0	0	11dB
0	1	14dB
1	0	19dB
1	1	24dB

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: Audio Front Speaker Amp:ALC123-CGT

Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 | Sheet 30 of 63

2014-09-15:Realtek Review

2014-10-13:Change Correct Power Net Name
B+ => +19VB +19VB : 9V~19.5V

2014-10-14:Realtek Review
Change all ALC1301 refer to DGND. Only Input Refer to AGND from Codec

2014-10-15:Realtek Review
1. Add RA65/RA66:10kohm for fine-tune output speaker 4 W8ohm
2. Change CA64 from 1uF to 4.7uF

2014-10-15:
Change CA69/70/81/83 from 1000pF to 10uF

2014-10-15:
Change 2x220uF to 6x22uF
Need Realtek Confir m

PIR Item 11

PIR Item 18

PIR Item 11

PIR Item 18

LB12 LB13 Bead Max I=2A

Close to Amp Output

Rear Speaker

ALC1301-CGT_QFN48_6X6

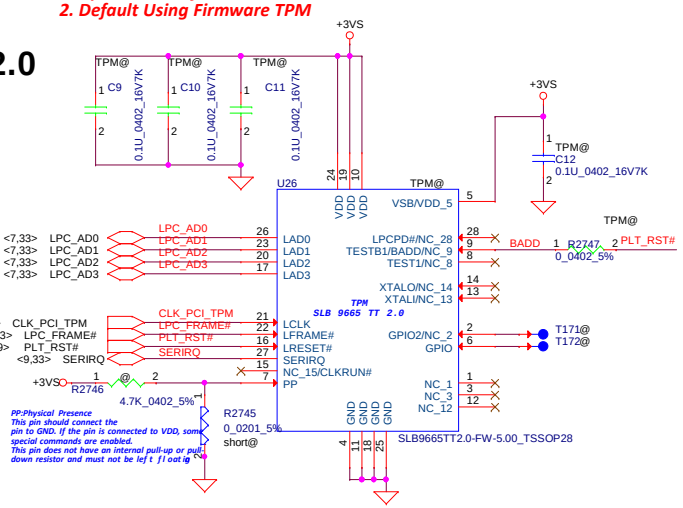
Gain	GAIN2	GAIN1	GAIN0	Min	Typ	Max	Unit
	1	1	1	31	32	33	dB
			0	25	26	27	
		0	1	19	20	21	
			0	17	18	19	
	0	1	1	11	12	13	
			0	9	10	11	
		0	1	5	6	7	
			0	-	0	-	

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title	Audio Subwoofer AMP : ALC1301-CGT		
Size: Custom	Document Number: LA-C501P		Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 31 of 63		

2014-10-14:
1. Upated Pin def i net o TP M2 0
2. Default Using Firmware TPM

TPM2.0

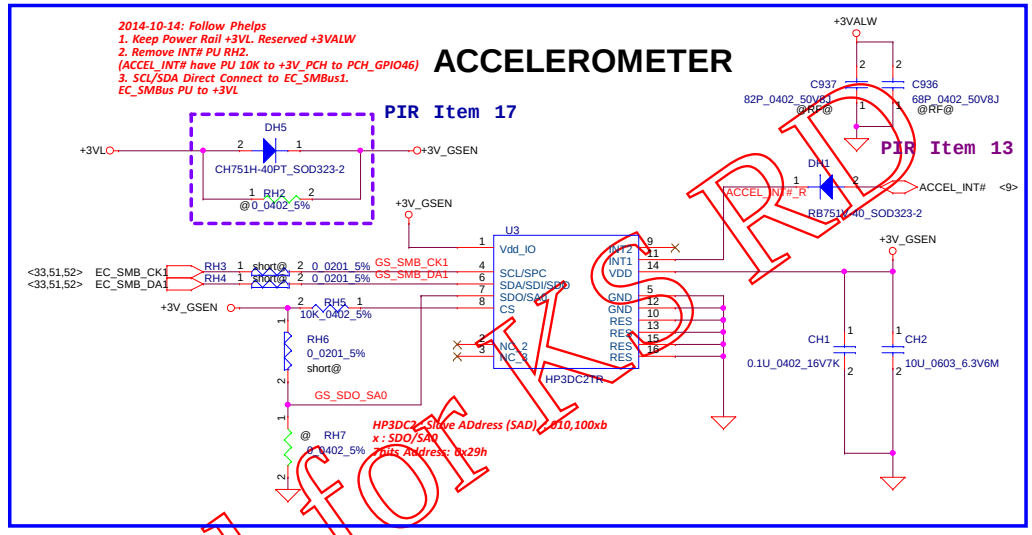


ACCELEROMETER

2014-10-14: Follow Phelps
1. Keep Power Rail +3VL. Reserved +3VALW
2. Remove INT# PU RH2.
(ACCEL_INT# have PU 10K to +3V_PCH to PCH_GPIO46)
3. SCL/SDA Direct Connect to EC_SMBus1.
EC_SMBus PU to +3VL

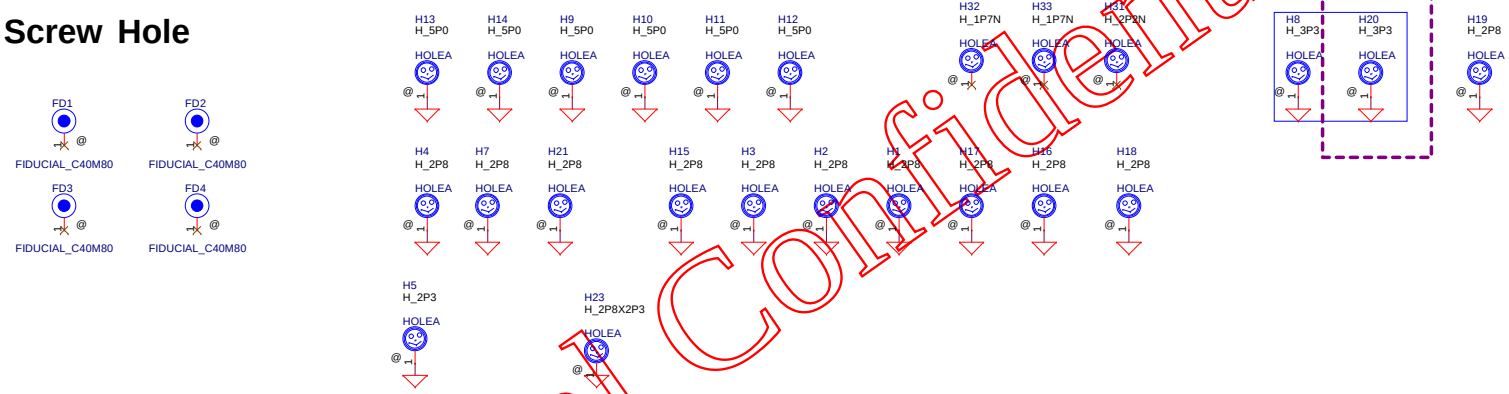
PIR Item 17

PIR Item 13



Screw Hole

PIR Item 2



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: LED/14"Screw hole

Size	Document Number	Rev
	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 32 of 63

PV# 2013.01.29 Add CK4 for ESD protect i on

ESD@ CK4 PLT_RST# 0.1U_0402_16V7K

PIR Item 12

10/21 +3VALW Change +3VALW_EC

PIR Item 11

Board ID control for 15

15"	DB	SI	PV	MV
UMA RK13	0 ohm	15K ohm	27K ohm	43K ohm
DIS RK13	12k ohm	20k ohm	33k ohm	56k ohm

Board ID control

DIS@ RK13 56K_0402_1% SD034560280

RK6 100K_0402_1% BOARD_ID RK13 43K_0402_1% UMA@ SD034430280

2014-10-13: Change to the same connect i on as LA A721 for EC Power

2014-10-16: 1. Use PCH_GPIO85((DGPU_PWR_EN)) to turn on "ALL" power for DGPU. Remove from EC_GPIO00. 2. Assign THERMAL_ALERT# from thermal sensor to EC_GPIO00

2014-09-25: Unpop RC for EC_RST# For KB9022, the ECRST# is internally pull-up to VCC via 40Kohm resistor, so you can remove external pull-up resistor and capacitor.

2014-09-30 : Need EC Check Pin106 : USB_CTL1 Pin108 : USB_CTL2

2014-09-25: Add RK62 For 1.8V power plane: VCC_IO2 and VCC_LPC pull up +1.8VALW or +1.8V(P). (ex: for Bay Trial M plat f or /B For 3.3V power plane: VCC_IO2 and VCC_LPC pull up +3.3VALW or +3.3V(P).

2015/02/12 ESD reserve for cocoa

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

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Compal Electronics, Inc.

Title: EC ENE-KB9012

Size: Custom | Document Number: LA-C501P | Rev: 1.0

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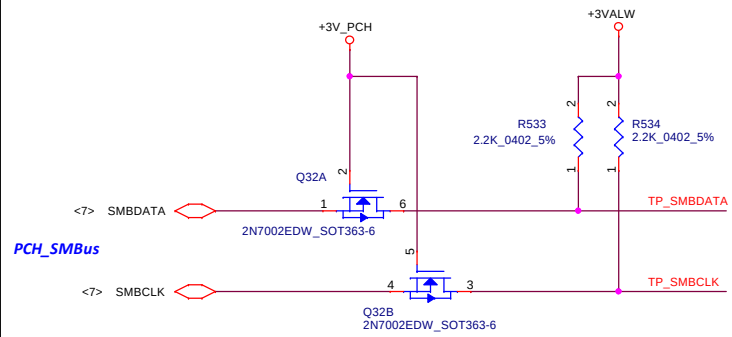
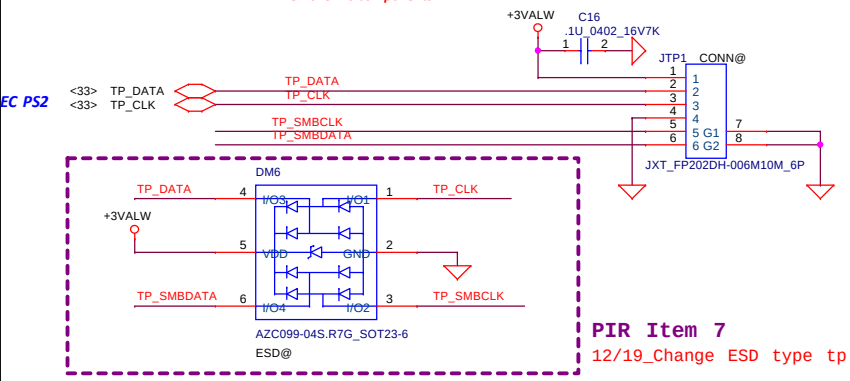
Touch pad conn

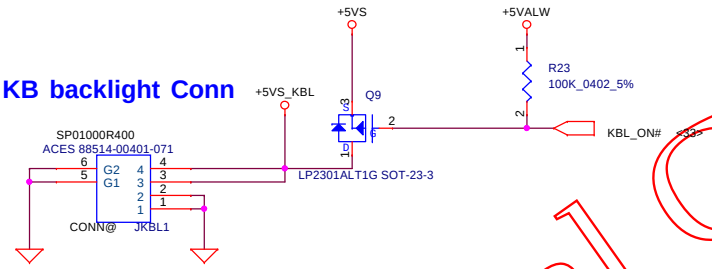


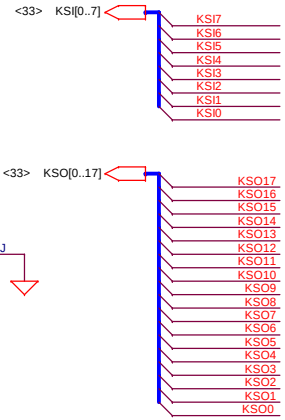
2014-10-14:
Confirm with Synaptics "Only" PS2+ SMBus" interface
Remove I2C components.



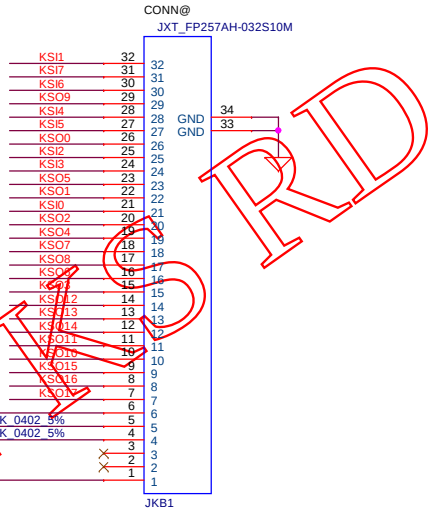
PIR Item 7
12/19_Change ESD type tp 6 pin

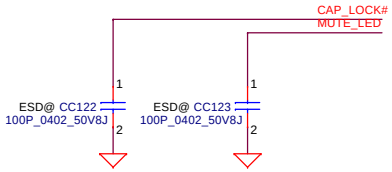
KB backlight Conn





Keyboard conn





Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: KB/TP

Size	Document Number	Rev
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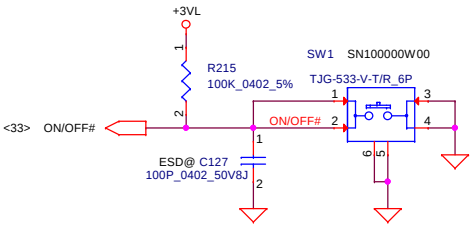
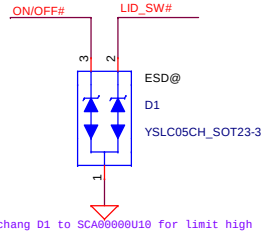
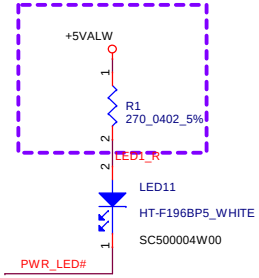
Powert Button Switch

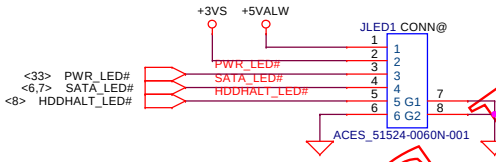


ESD Diode

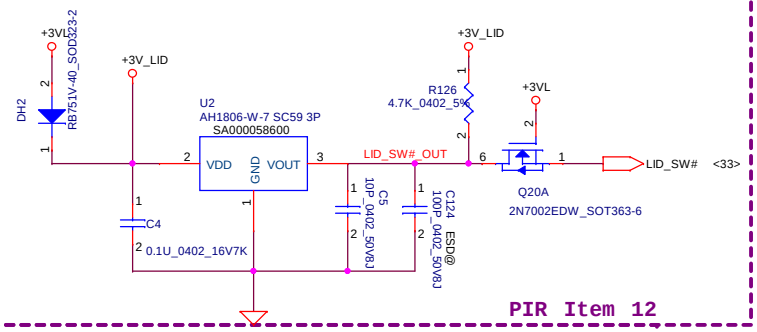




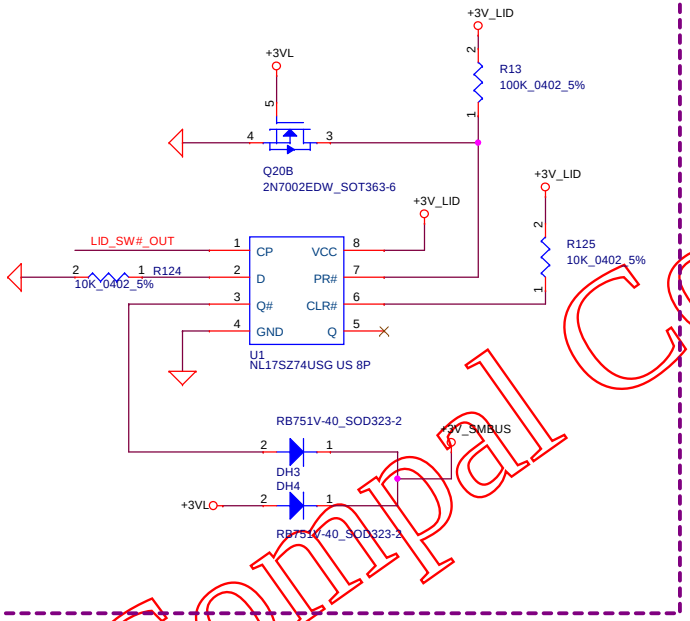
to LED Board



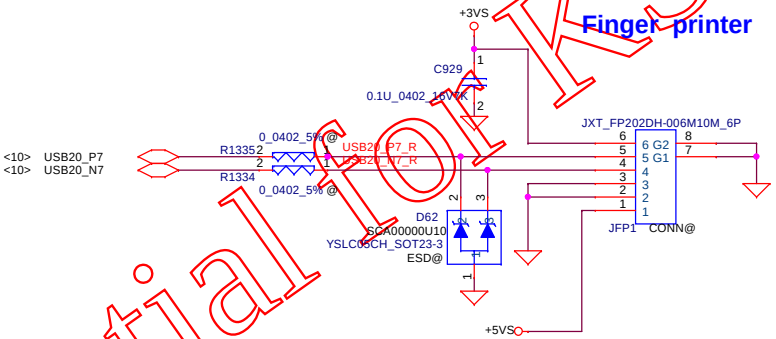
Lid Switch (Hall Effect Sensor)



PIR Item 12

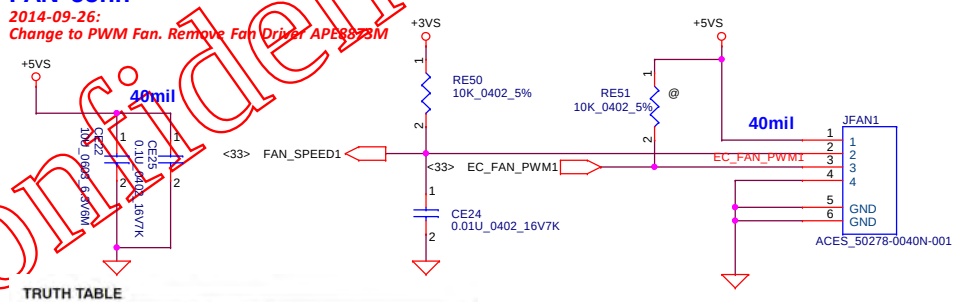


Finger printer



FAN conn

2014-09-26:
Change to PWM Fan. Remove Fan Driver APE8873M



TRUTH TABLE

Inputs				Outputs		
PR	CLR	CP	D	Q	Q̄	Operating Mode
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	l	L	H	
H	H	‡	X	NC	NC	Hold

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
↑ = Low-to-High Transition
‡ = Not a Low-to-High Transition

For I_{CC} reasons, DO NOT FLOAT Inputs

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title	PWRBTN/FAN		
Size Custom	Document Number LA-C501P		Rev 1.0
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Reserve for HW

Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **GCLK**

Size | Document Number: **LA-C501P** | Rev: 1.0

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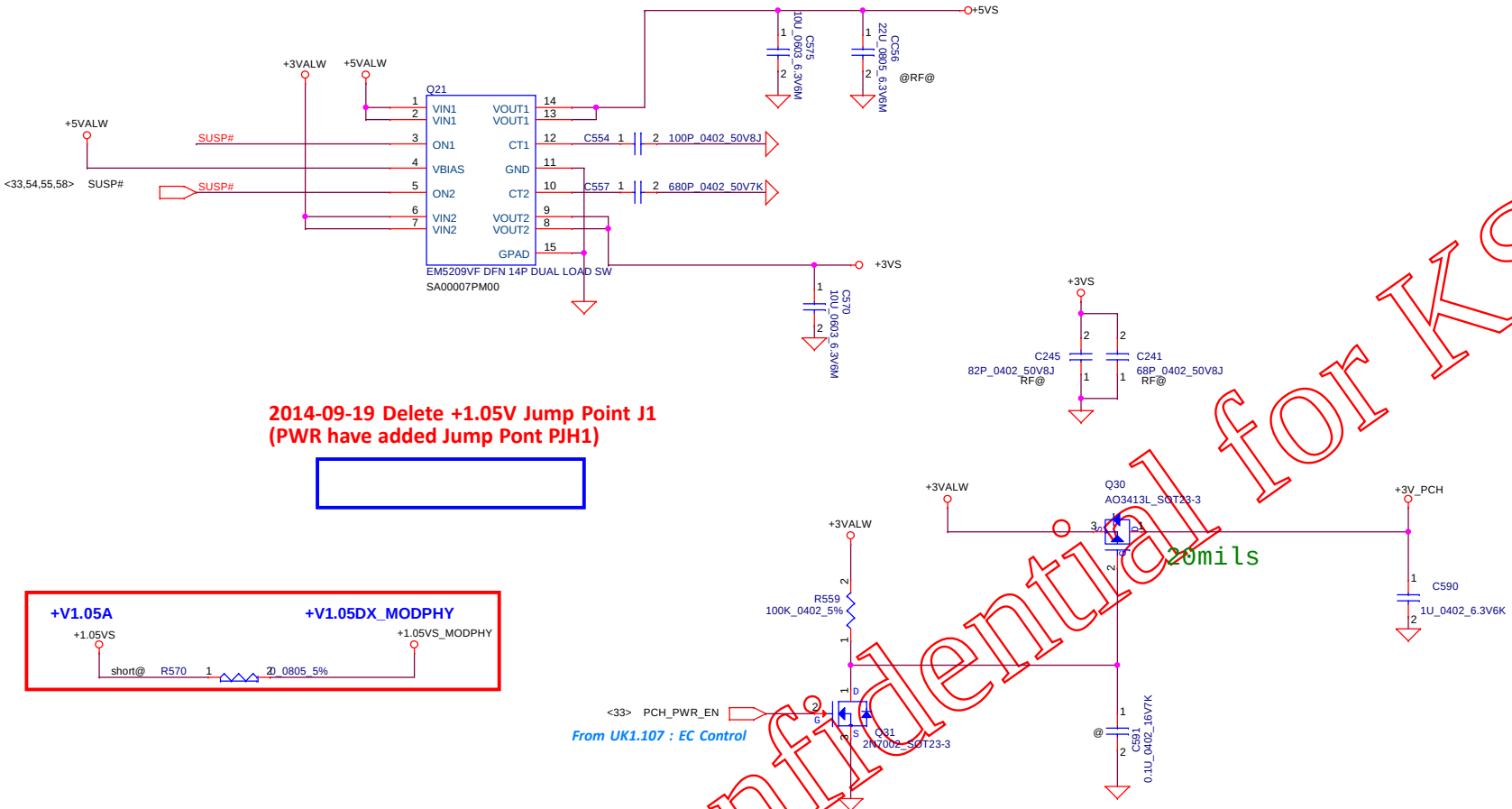


Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: DC Interface

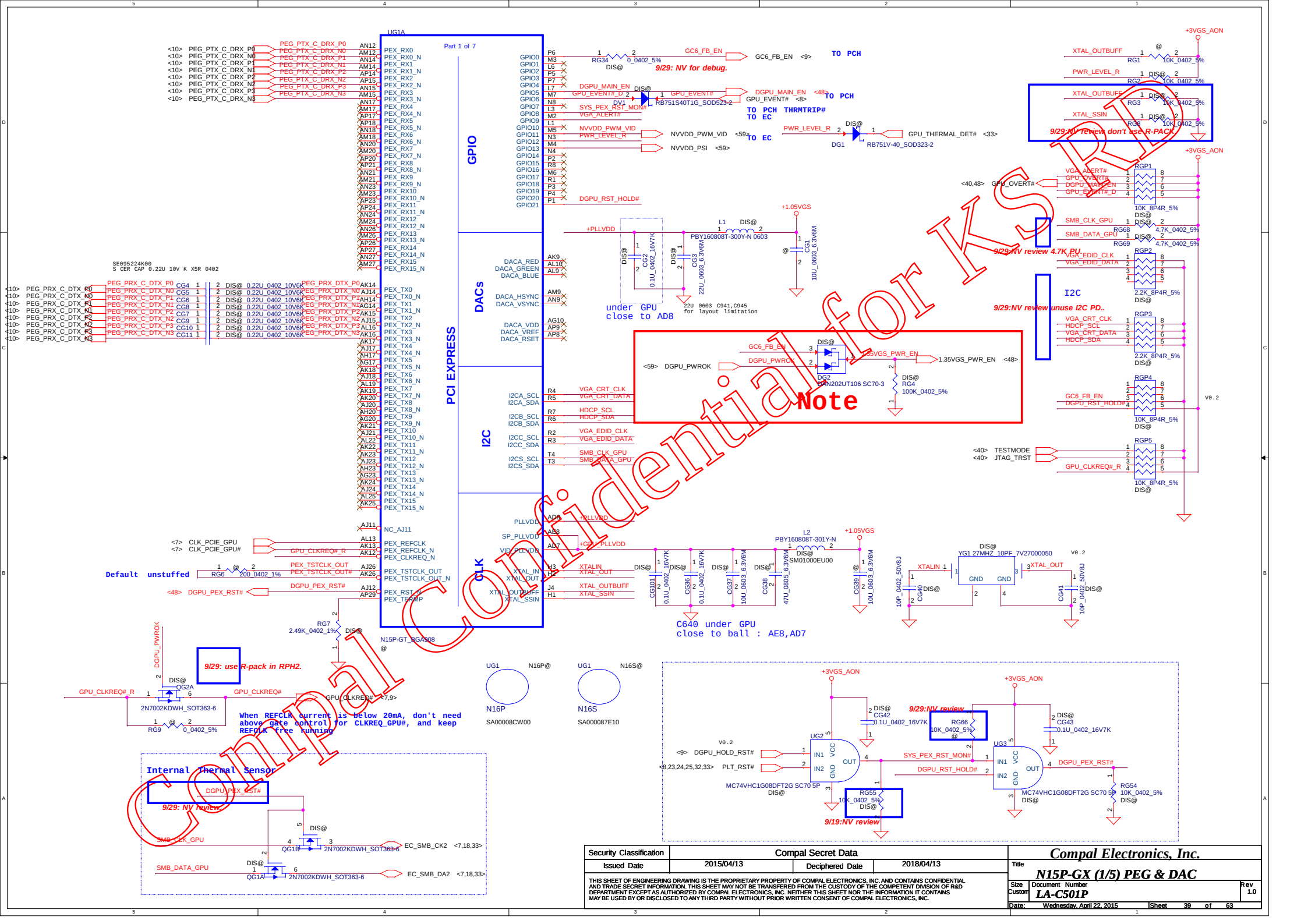
Size	Document Number	Rev
Custom	LA-C501P	1.0

Date: Wednesday, April 22, 2015 Sheet 37 of 63

Reserve for HW

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: WAKE and RST-1

Size: Custom	Document Number: LA-C501P	Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 38 of 63	



Security Classification	Compal Secret Data		
Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **N15P-GX (1/5) PEG & DAC**

Size	Document Number	Rev
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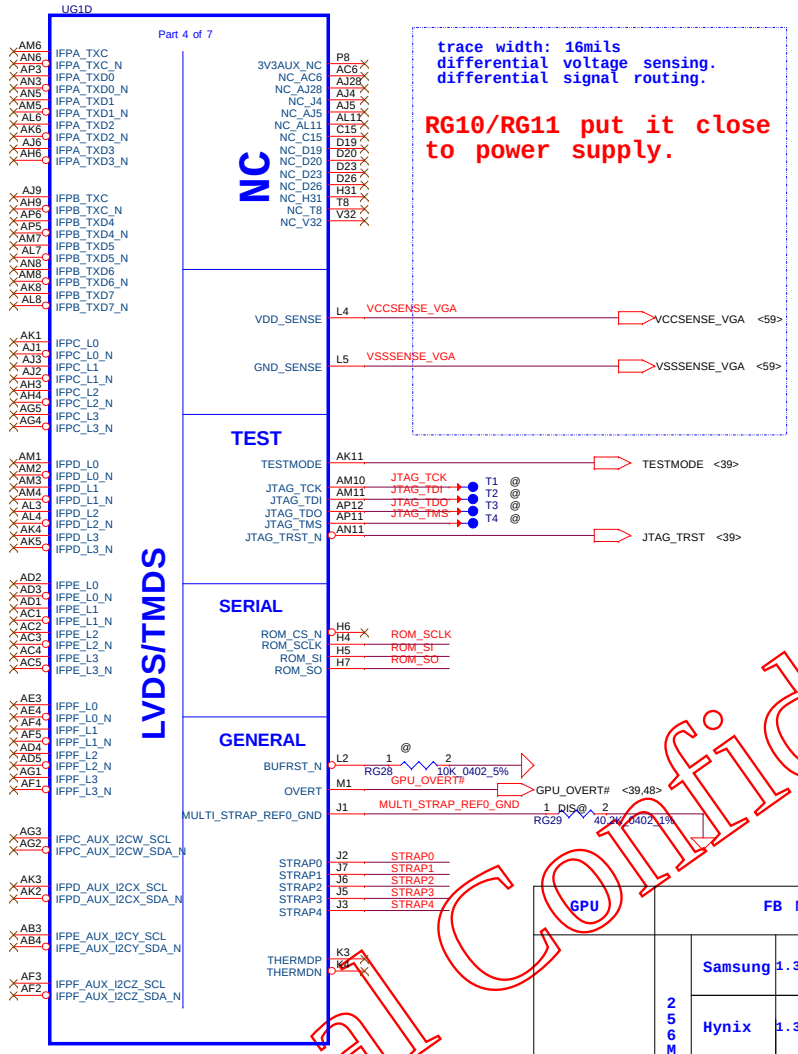
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS_MAIN	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	+3VGS_MAIN	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	+3VGS_MAIN	**DEVID_SEL**	**PCIE_CFG**	**SMB_ALT_ADDR**	VGA_DEVICE
STRAP0	Keep pull-up to 3V3_AON and pull-down to GND foot print and stuff 50K ohm pull-up				
STRAP1					
STRAP2	RESERVED				
STRAP3					
STRAP4					

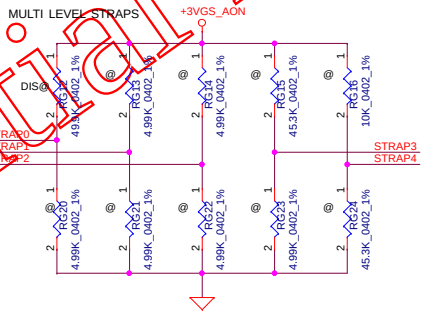
SKU	Device ID	bit5 to bit0
N16P-GT		

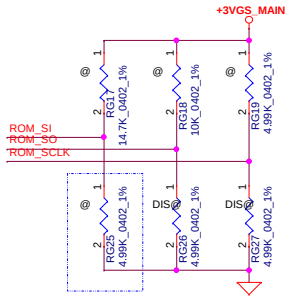
Resistor Values	Pull-up to +3VGS_MAIN	Pull-down to Gnd
5K	1000 =8	0000 =0
10K	1001 =9	0001 =1
15K	1010 =A	0010 =2
20K	1011 =B	0011 =3
25K	1100 =C	0100 =4
30K	1101 =D	0101 =5
35K	1110 =E	0110 =6
45K	1111 =F	0111 =7



trace width: 16mils
differential voltage sensing.
differential signal routing.

RG10/RG11 put it close to power supply.





GPU	FB Memory DDR3L(1.35V)				RAM_CFG[3:0] (ROM_SI)	
N16P-GT, N16S-GT	256M x16	Samsung	1.35V	900MHz	K4W4G1646E-BC1A	0x1(PD 10K)	
		Hynix	1.35V	900MHz	H5TC4G63CFR-N0C	0x2(PD 15K)	
		Hynix	1.35V	900MHz	H5TC4G63AFR-11C	0x3(PD 20K)	
		Micron	1.35V	900MHz	MT41J256M16HA-093G:E DateCode_Min:1332	0x4(PD 24.9K)	V
		Samsung	1.35V	900MHz	K4W4G1646D-BC1A	0x5(PD 30.1K)	

Table 6. N16P-GT DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank	Hynix	H5TC2G63FFR-11C	F-die	0x9	900	N/A	Production candidate
				Micron	MT41J128M16JT-093G:K	K-die	0xA	900	1322	Production candidate
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	N/A	Production candidate
		256Mx16	Single Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production candidate
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production candidate
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production candidate

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Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: N15P-GX (2/5) TMDS/LVDS

Size: Custom | Document Number: LA-C501P | Rev: 1.0

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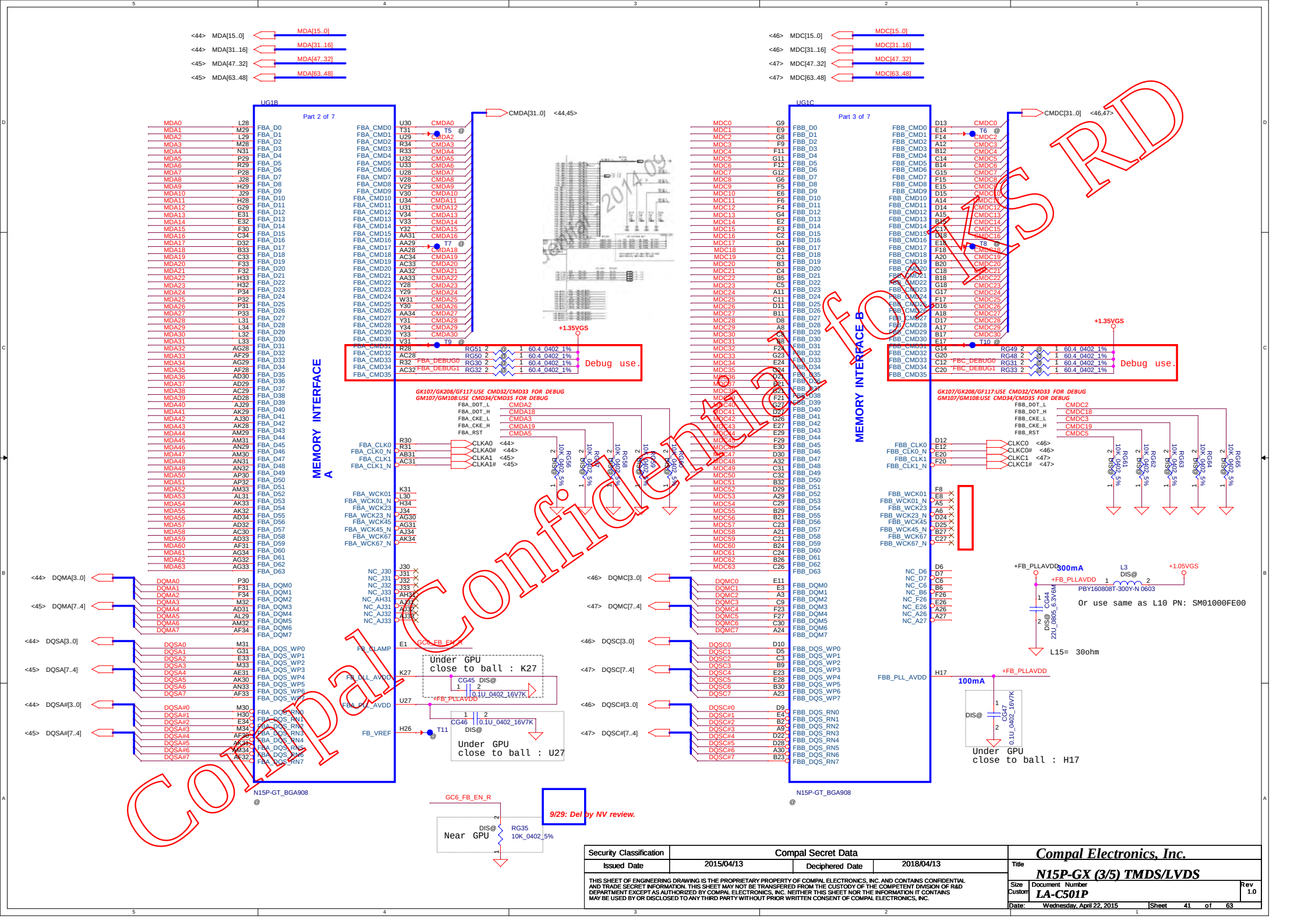

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Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **N15P-GX (3/5) TMDS/LVDS**

Size	Document Number	Rev
Custom	LA-C501P	1.0

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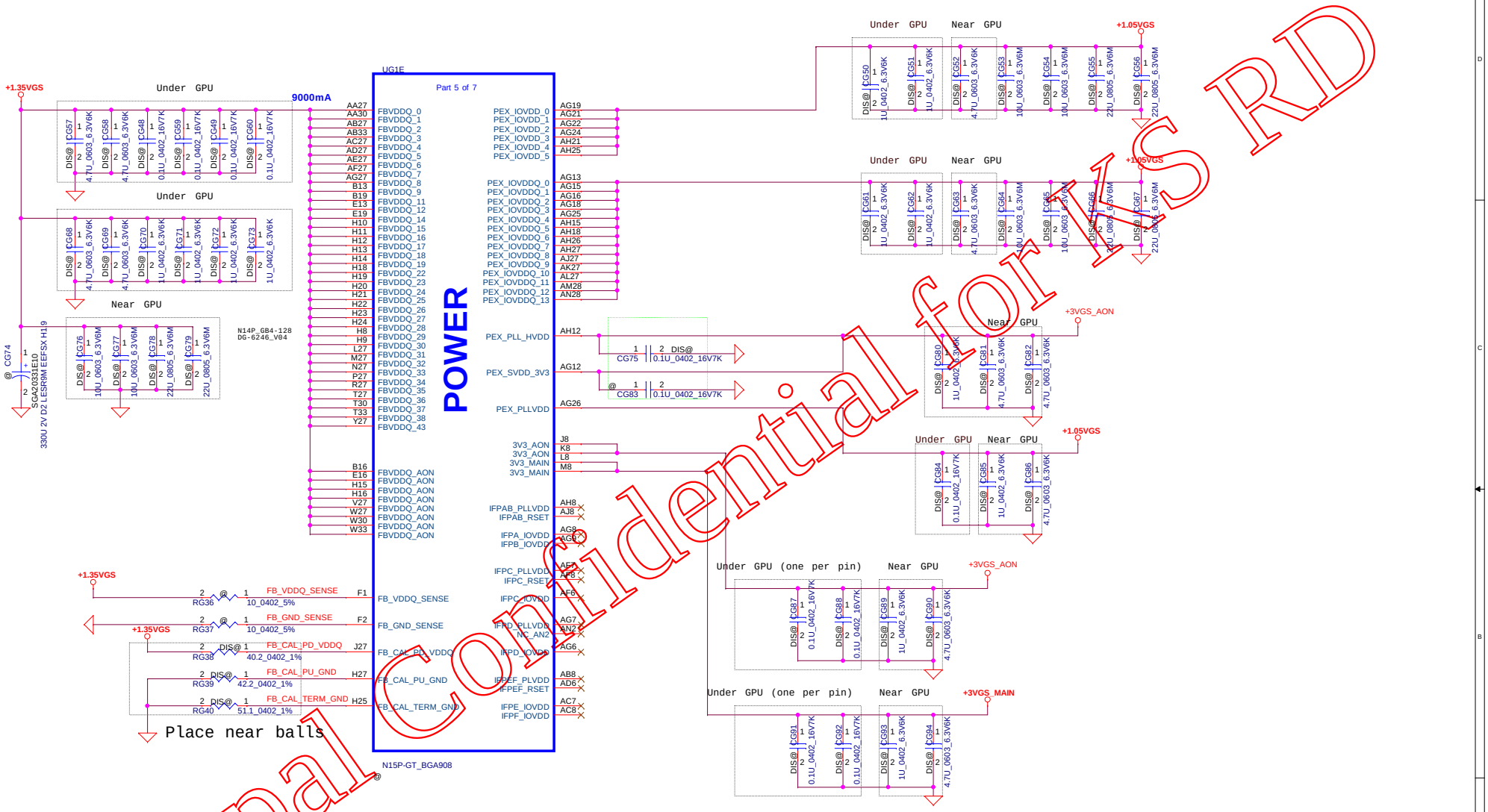

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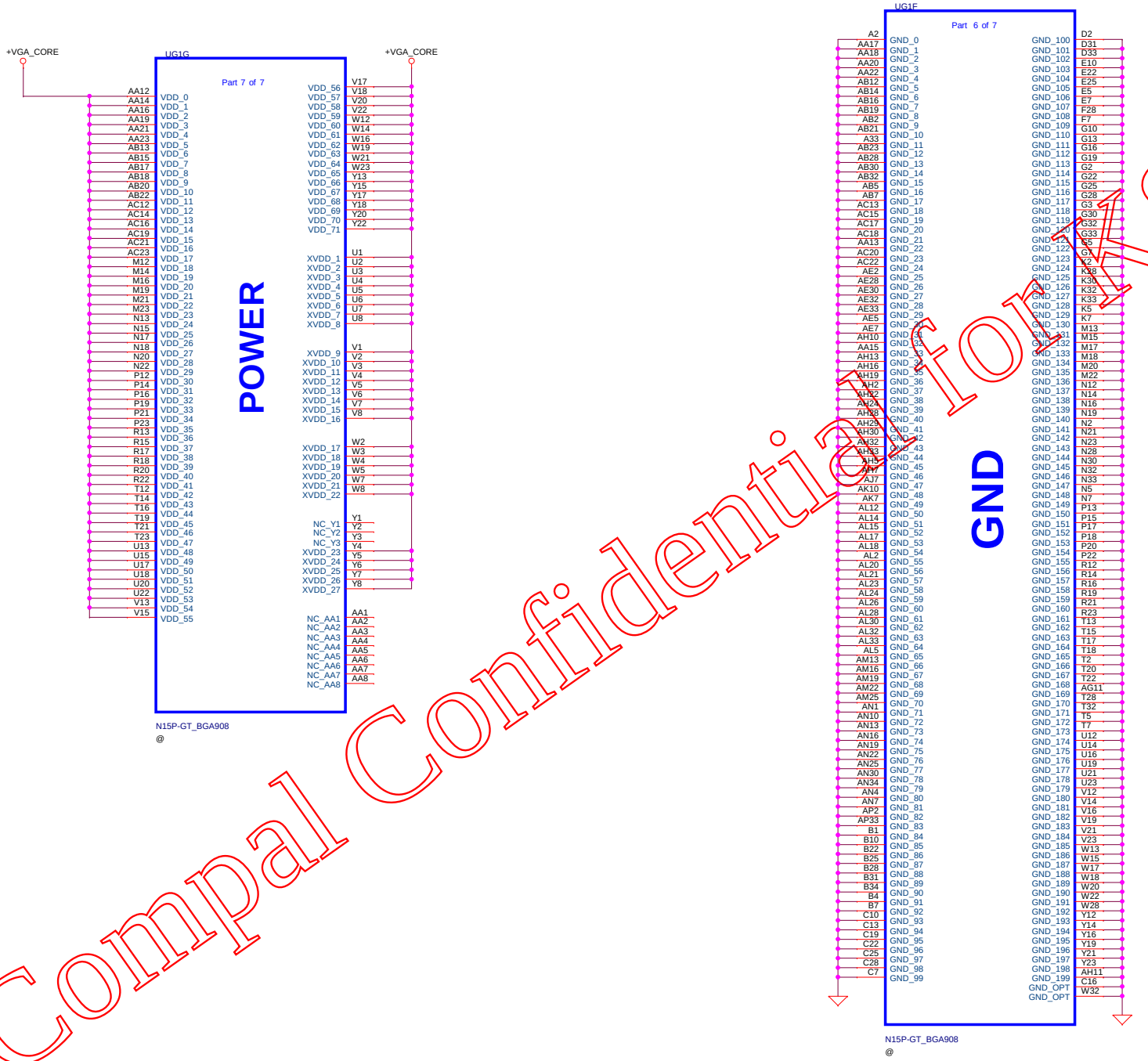
Compal Electronics, Inc.		
Title: N15P-GX (4/5) POWER		
Size: Custom	Document Number: LA-C501P	Rev: 1.0
Date: Wednesday, April 22, 2015	Sheet 42 of 63	



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Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.			
Title	N15P-GX (5/5) POWER/ GND		
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Memory Partition A - Lower 32 bits [31..0]

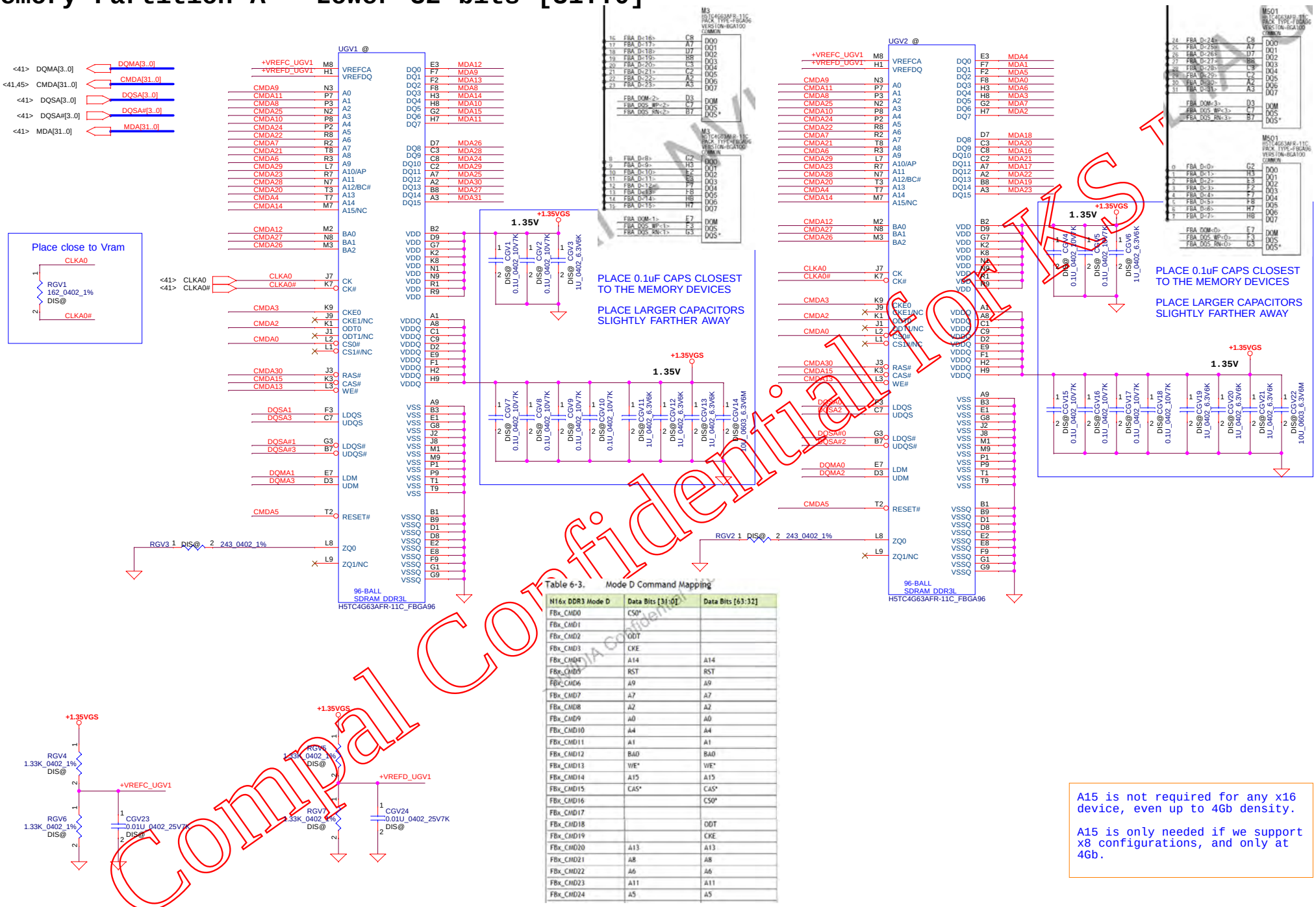

Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

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Issued Date	2015/04/13	Deciphered Date	2018/04/13

Compal Electronics, Inc.

Title: **VRAM_DDR3_A Lower**

Size	Document Number	Rev
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Memory Partition A - Upper 32 bits [63..32]

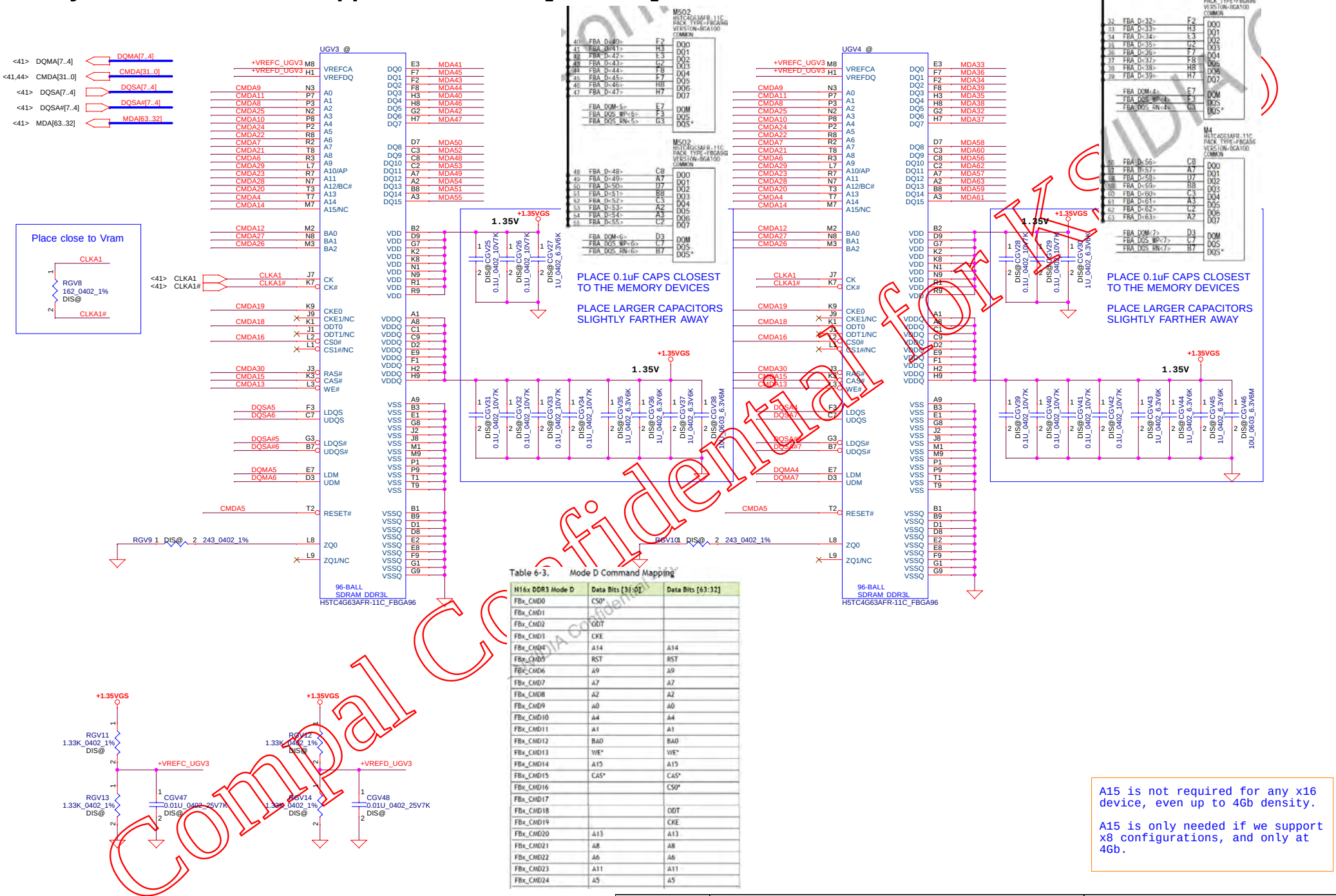

Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

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Compal Electronics, Inc.			
Title	VRAM_DDR3_A Upper		
Size	Document Number		Rev
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Memory Partition C - Lower 32 bits [31..0]

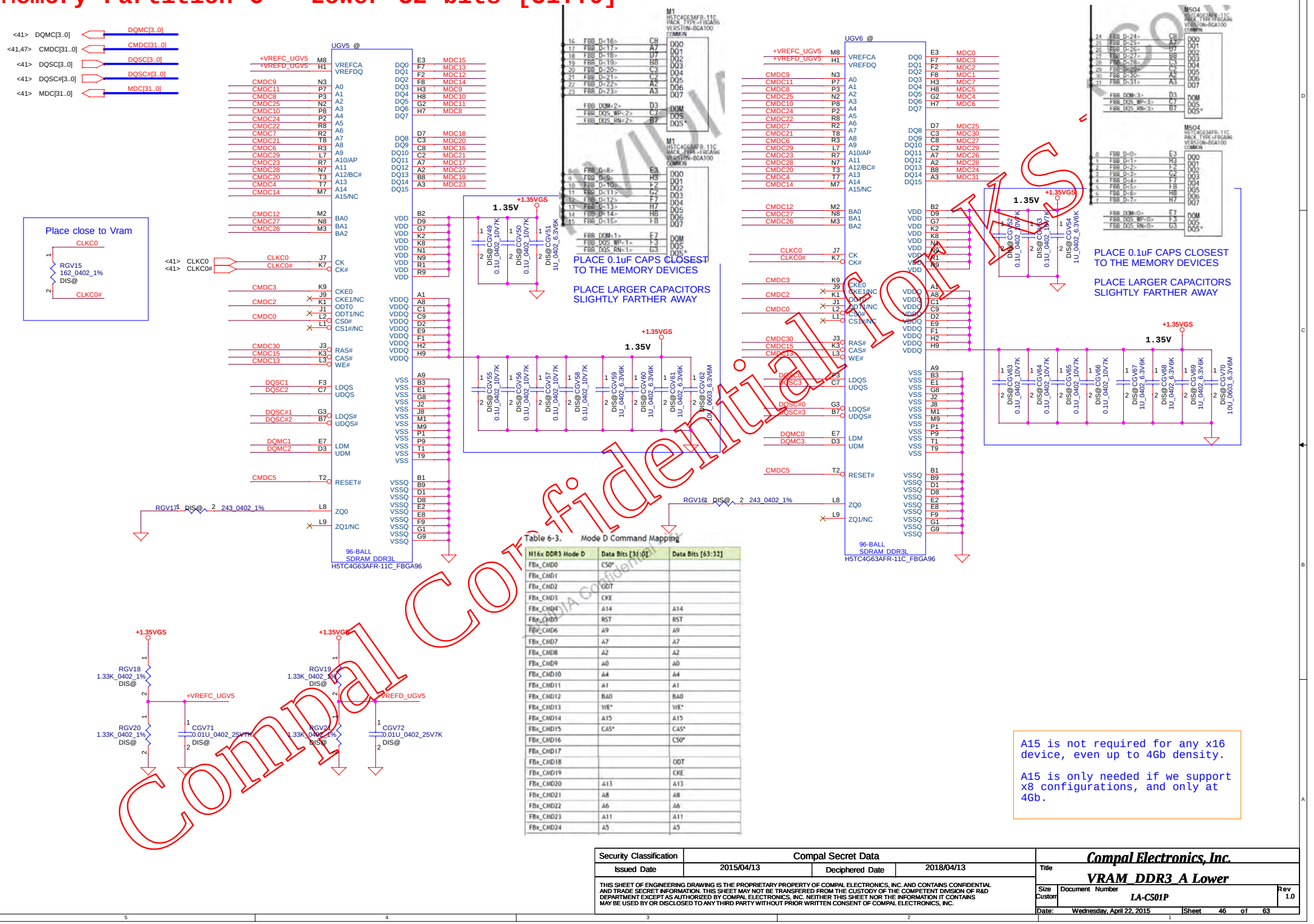

Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

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Size: Custom	Document Number: LA-C501P		Rev: 1.0
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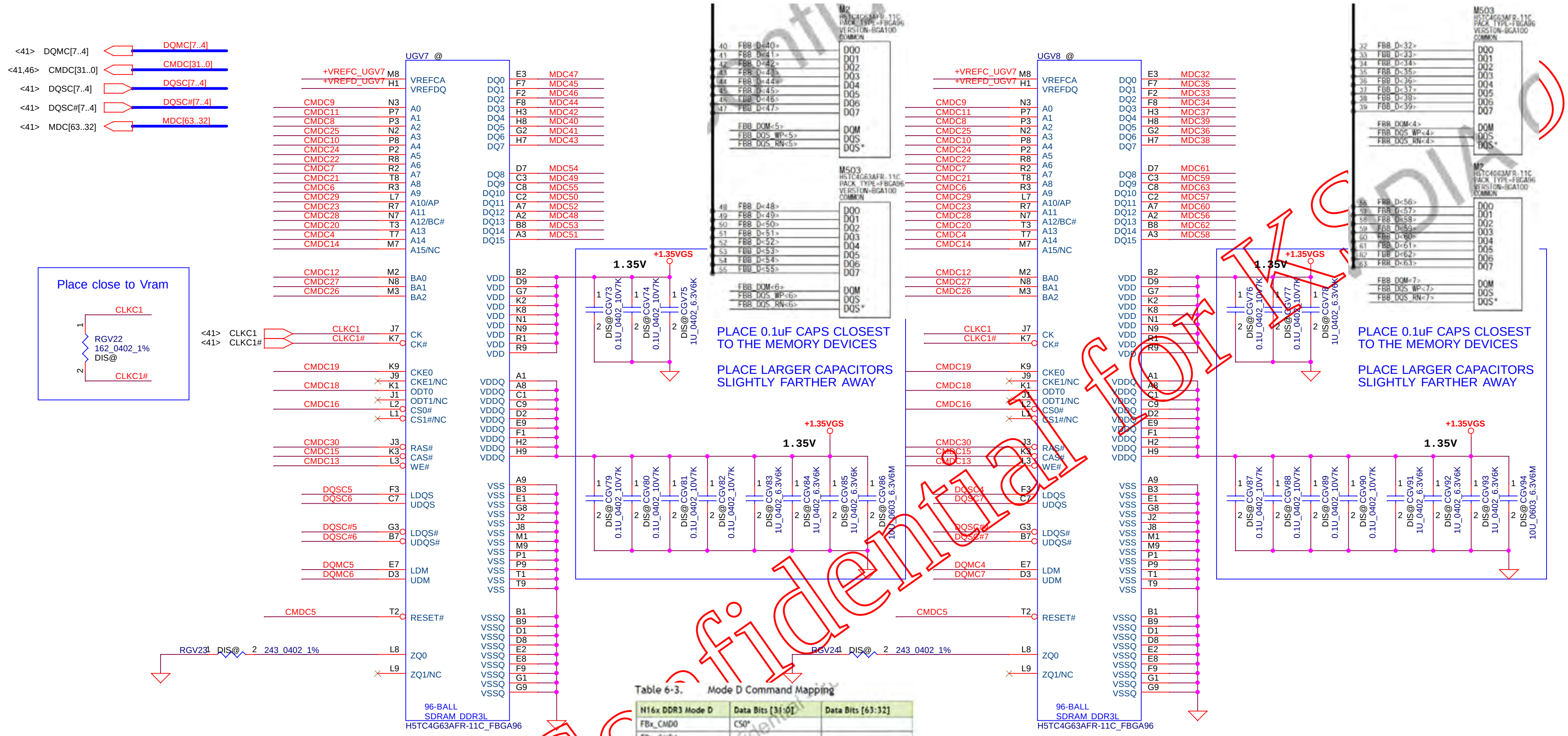
Memory Partition C - Upper 32 bits [63..32]



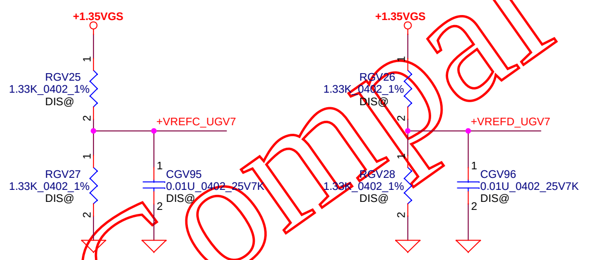


Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5

A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

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Compal Electronics, Inc.

Title: **VRAM_DDR3_A Upper**

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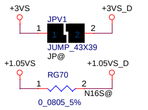
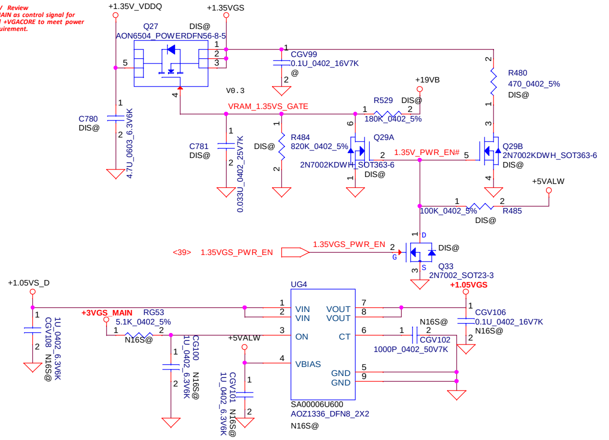
For Power consumption Measurement

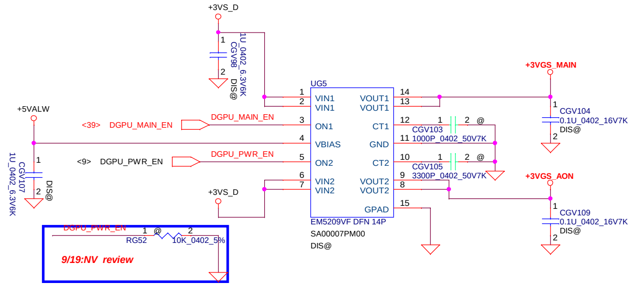


9/19:NV add delay.



PIR Item 15 *GPU VDDQ and VRAM Shared with DDR3*

+3VS_DGPU for GC6 reserved.



3.10.2 Power Sequencing Recommendations

Power sequencing guidelines are provided relative to the ramping up of the main 3.3V system rail, which is the 3.3V input to the GPU.

3.10.2.1 Power-Up Sequence

The following condition is recommended:

3.3V → NVVDD/PEX_VDD → FBVDD/Q

- All GPU power rails must ramp up after 3.3V.
- FBVDD/Q should ramp up after both NVVDD and PEX_VDD are in regulation.

All other 3.3V power rails can ramp up with 3.3V, and all other 1.05V power rails can ramp up with PEX_VDD. Figure 3-6 shows an example of proper GPU power up sequence.

IFPx_VDD powered at 3.3V can ramp up with other 3.3V power rails. IFPy_VDD powered at 1.05V can ramp up with other 1.05V power rails. Figure 3-7 shows an example of proper GPU power up sequence.

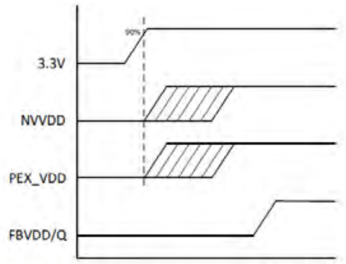


Figure 3-7. Example of Power-Up Sequencing Order

Note:
- 3.3V includes all rails powered at 3.3V; PEX_VDD includes all rails that are shared on 1.05V
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- Designs that support GC6 2.0 are required to meet all GC6 timing requirements. Refer to Section 18.3.2.3 for requirement details.
- PEX_VDD can ramp up before, after, or at the same time with NVVDD.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.

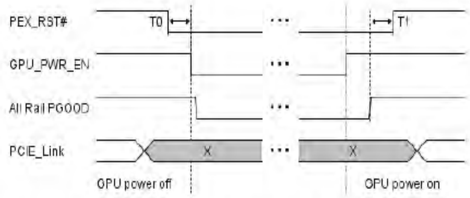


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

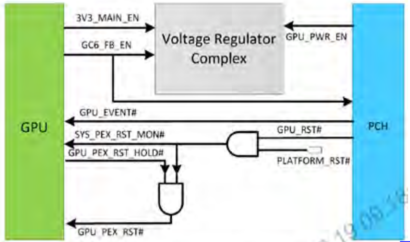
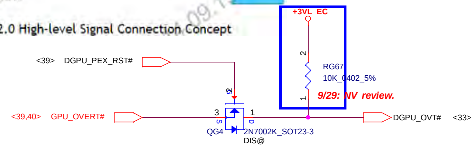


Figure 18-9. GC6 2.0 High-level Signal Connection Concept



GPU side *EC side*

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 entry and exit sequence and timing requirements.

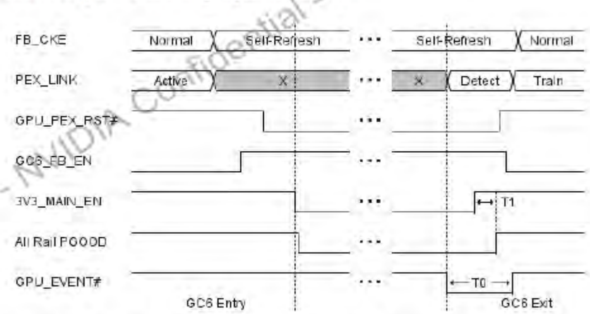


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

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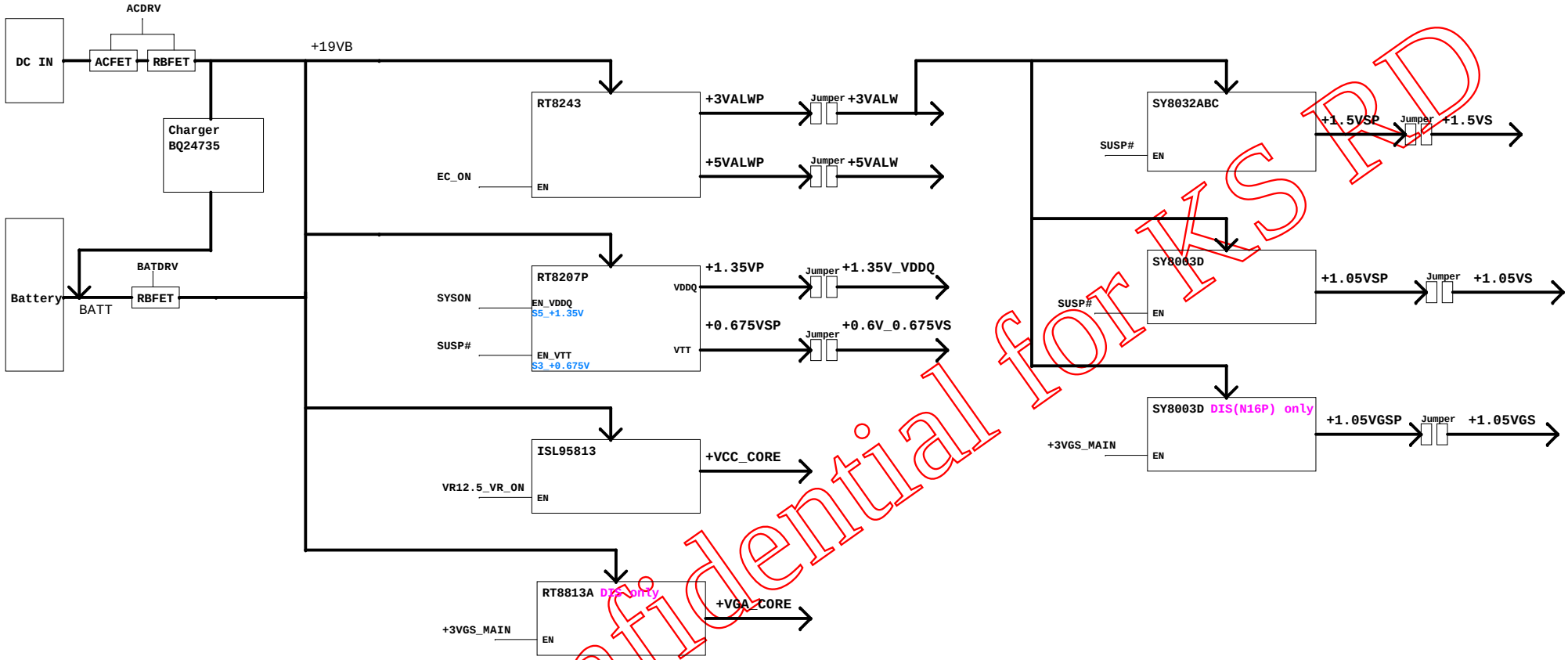
Issued Date	2015/04/13	Deciphered Date	2018/04/13	Title: N15P-GX DC-DC
				Size: Custom; Document Number: LA-C501P; Rev: 1.0
				Date: Wednesday, April 22, 2015; Sheet 48 of 63



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Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: *Power Block Diagram*

Size	Document Number	Rev
	LA-C501P	0.1

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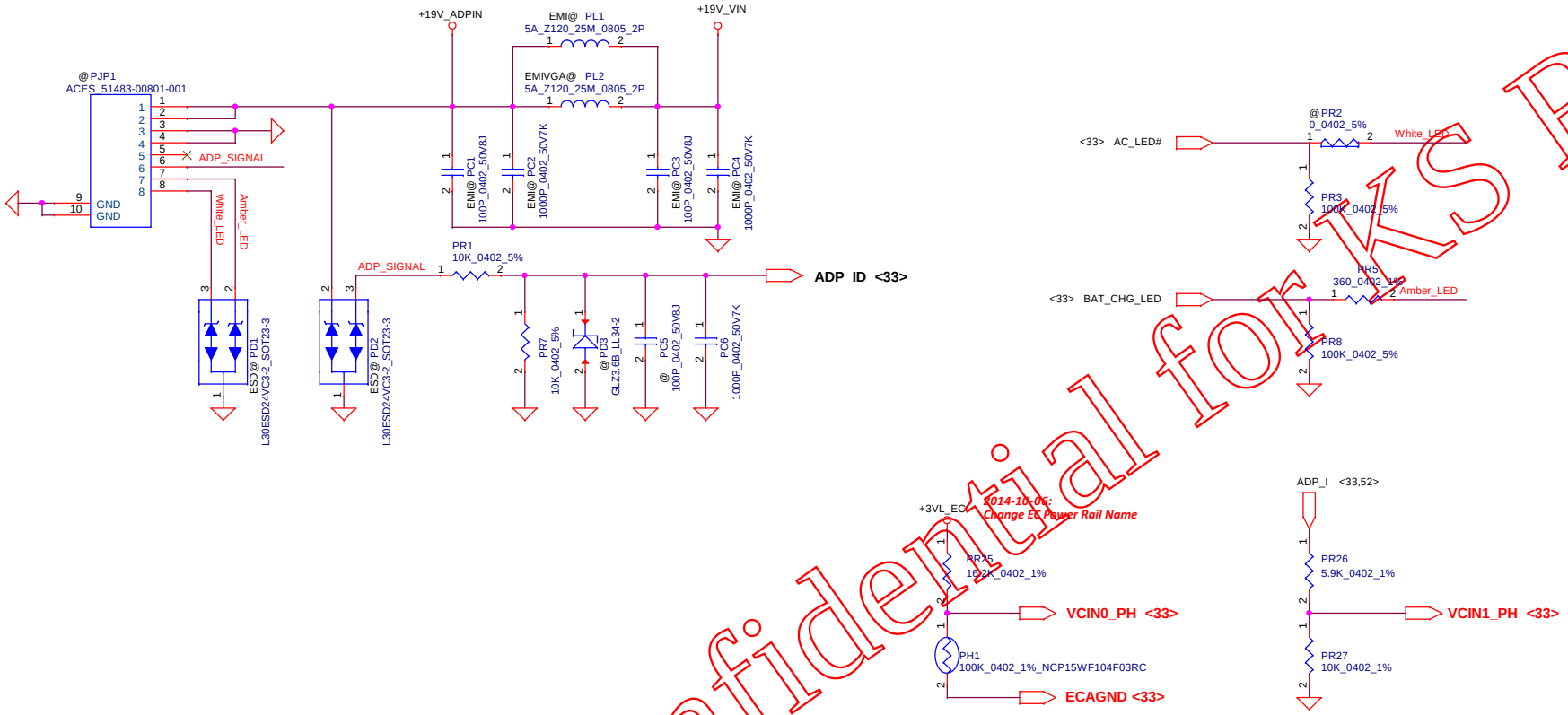


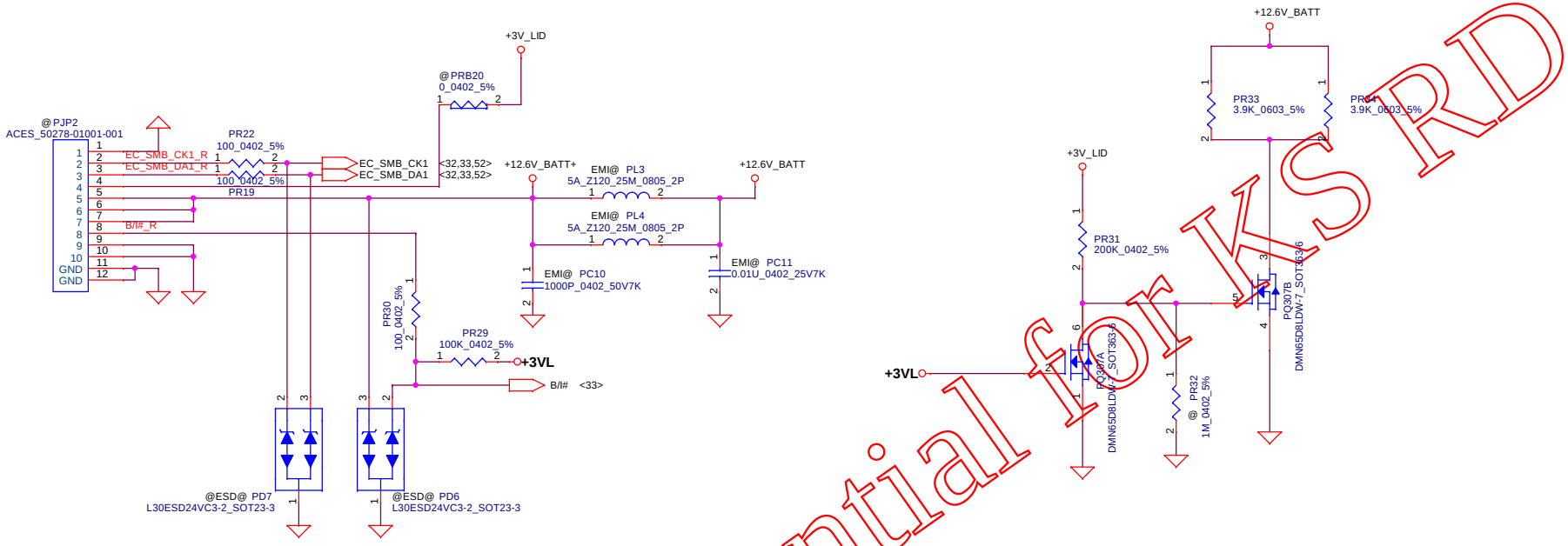
VCIN0_PH set ting
Trigger point = 1V (92C)
Recovery point = 2.02V (56C)

VCIN1_PH set ting
90W
Active: VCIN1_PH = 0.799V(123.86 W)
Resume : VCIN1_PH = 0.0.581V(90.07W)
65W
Active: VCIN1_PH = 0.599(92.86 W)
Resume : VCIN1_PH = 0.419(64.96W)
45W
Active: VCIN1_PH = 0.414(64.18 W)
Resume : VCIN1_PH = 0.289(44.8W)

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

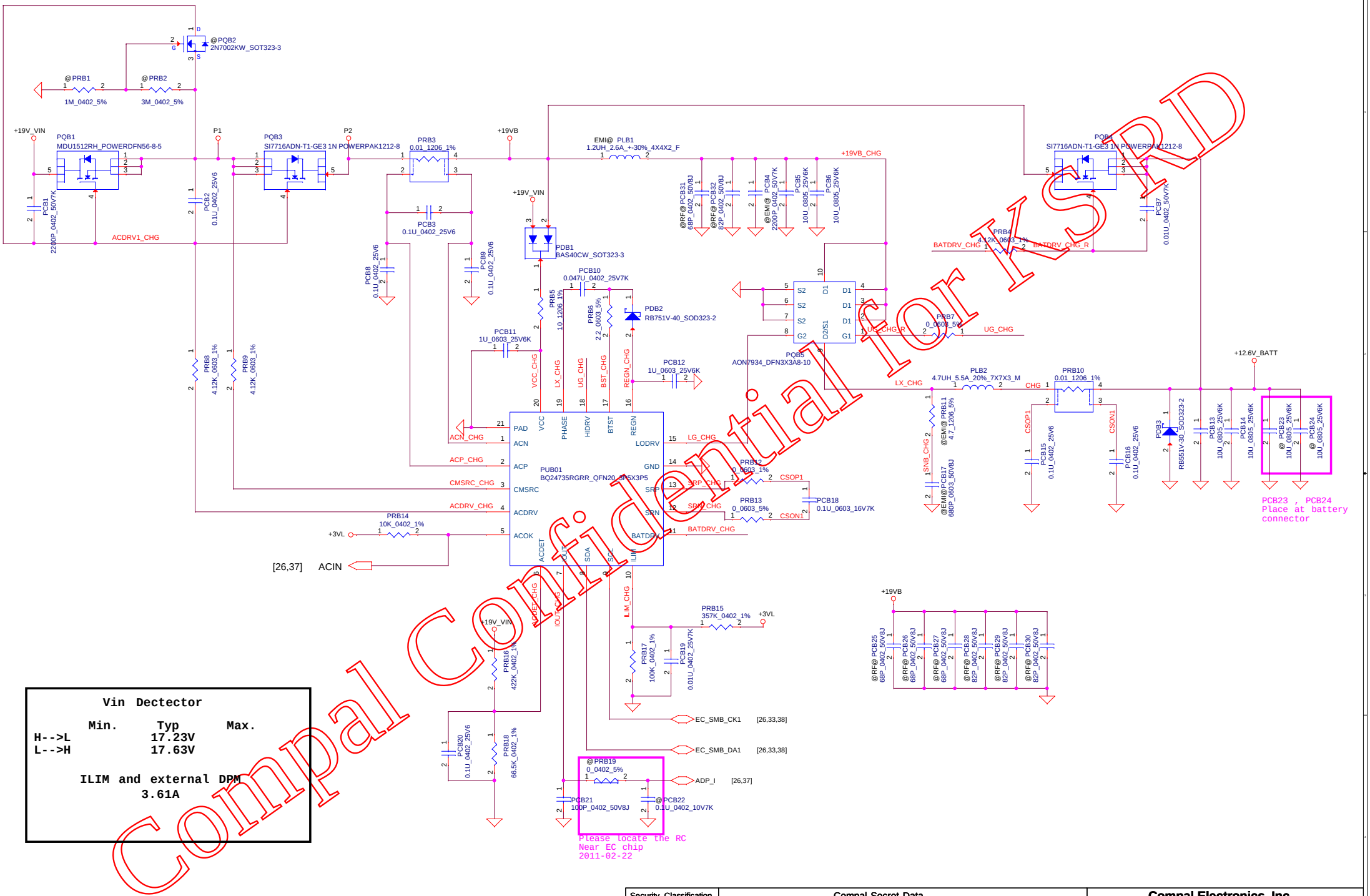
Title	*DC Conn*	
Size	Document Number: **LA-C501P**	Rev: 0.1
Date: Wednesday, April 22, 2015	Sheet 50 of 61	



Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title	***BATT Conn***	
Size	Document Number: **LA-C501P**	Rev: 0.1
Date: Wednesday, April 22, 2015	Sheet 51 of 61	



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
3.61A

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
Custom	LA-C501P	0.1

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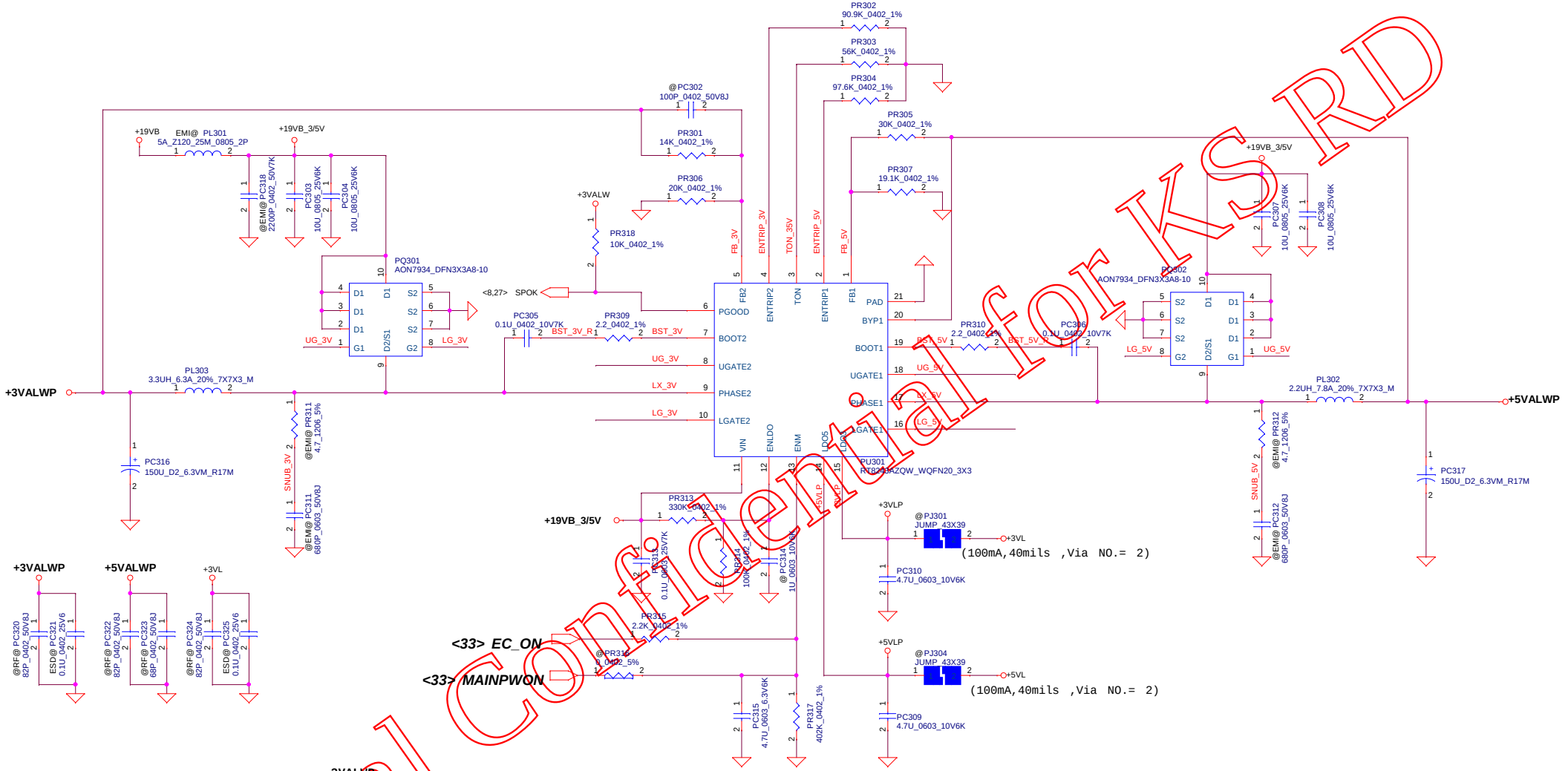

3VALWP
Fsw : 455kHz
ITDC : 5.6A
Ipeak : 7A
Iocp: 8.4A
OVP : 113%~120%

5VALWP
Fsw : 390kHz
ITDC : 6.4A
Ipeak : 8A
Iocp: 9.6A
OVP : 113%~120%

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size	Document Number	Rev
Custom	LA-C501P	0.1

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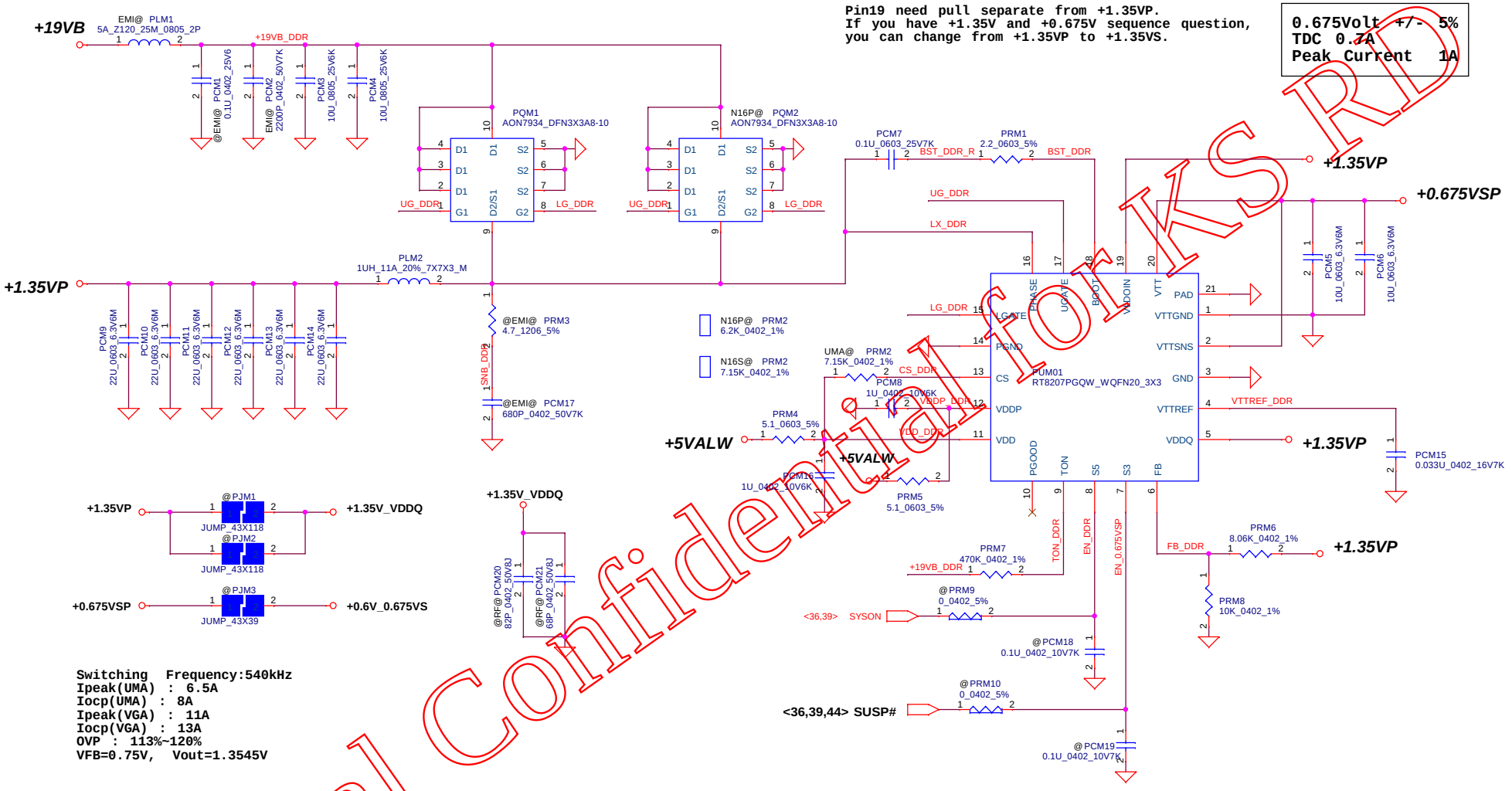

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Switching Frequency:540kHz
Ipeak(UMA) : 6.5A
Iocp(UMA) : 8A
Ipeak(VGA) : 11A
Iocp(VGA) : 13A
OVP : 113%~120%
VFB=0.75V, Vout=1.3545V

MOSFET: 3x3 DFN
H/S Rds(on): 12.4mohm(Typ), 15.8mohm(Max)
Idsm: 13A@Ta=25C, 7.8A@Ta=70C

L/S Rds(on): 9.4mohm(Typ), 11.6mohm(Max)
Idsm: 15A@Ta=25C, 9A@Ta=70C

Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: 1.35V/0.675VS

Size	Document Number	Rev
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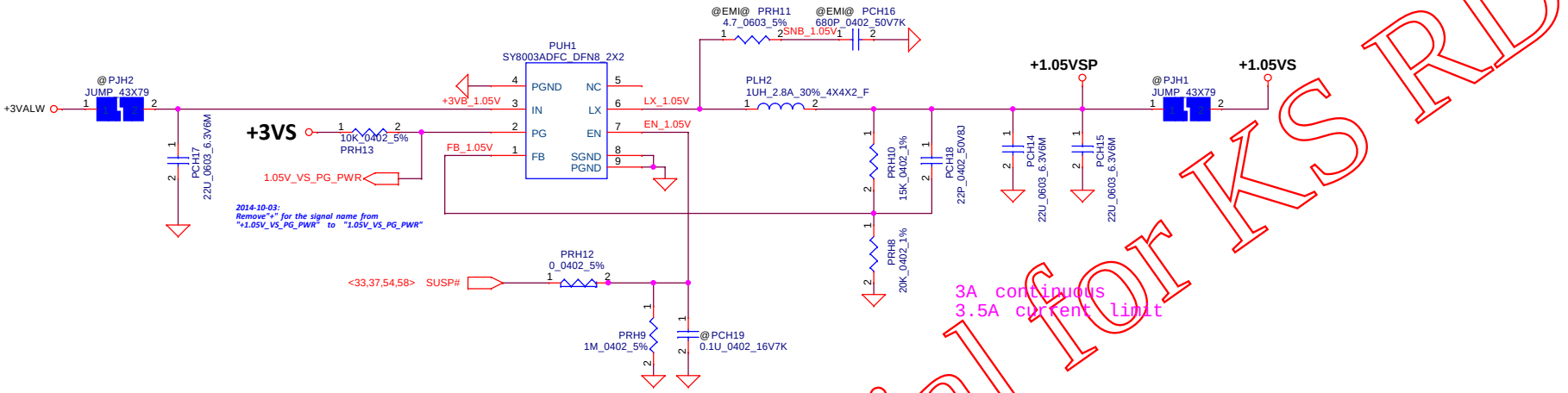

3A continuous
3.5A current limit

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

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Title	*1.05V*	
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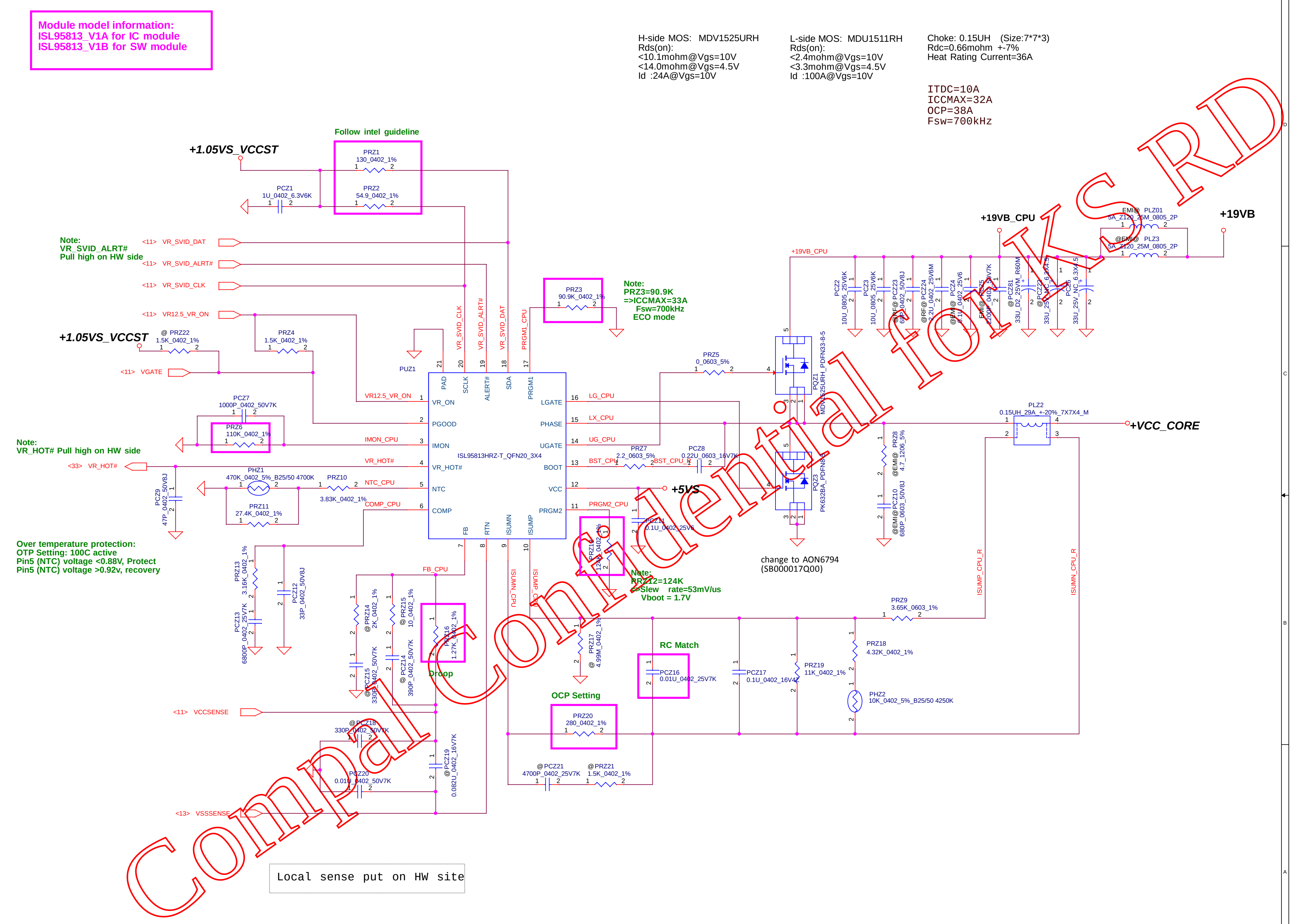

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **VCC_CORE**

Size | Document Number: **LA-C501P** for CN30 | Rev 0.1

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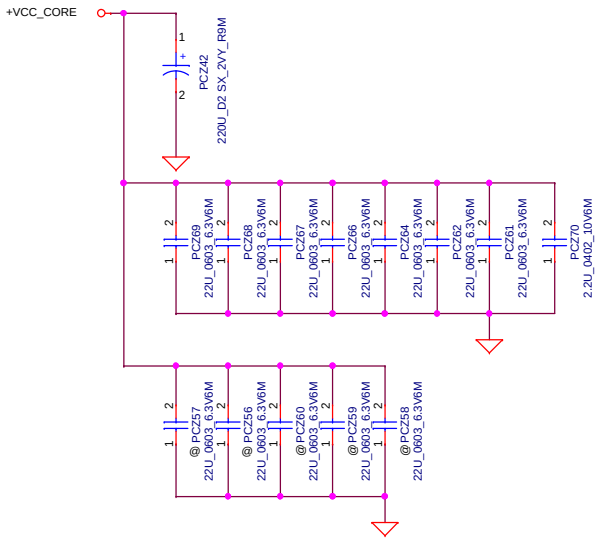

BDW-U 15W
220uF X 1
22uF X7
2.2uF X1

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
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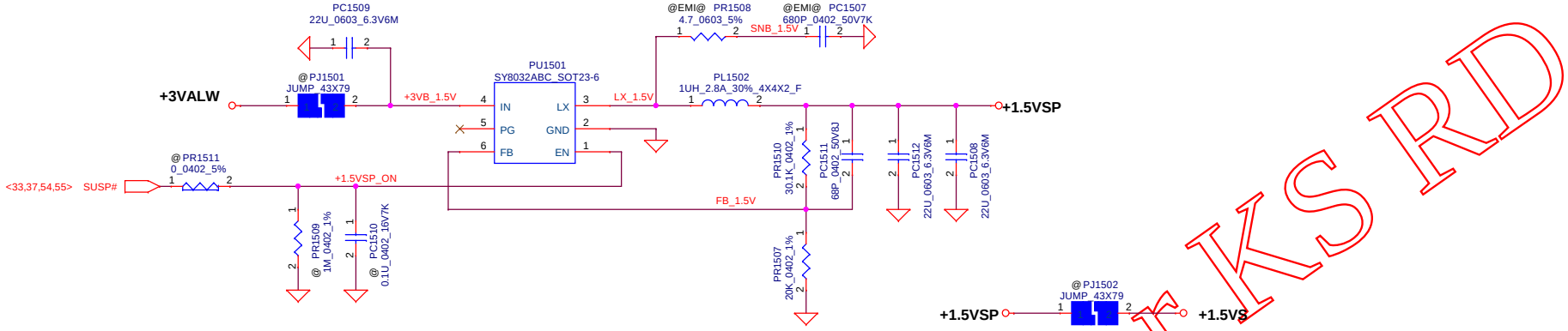

continuous 2.8A

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title	*1.5VS*	
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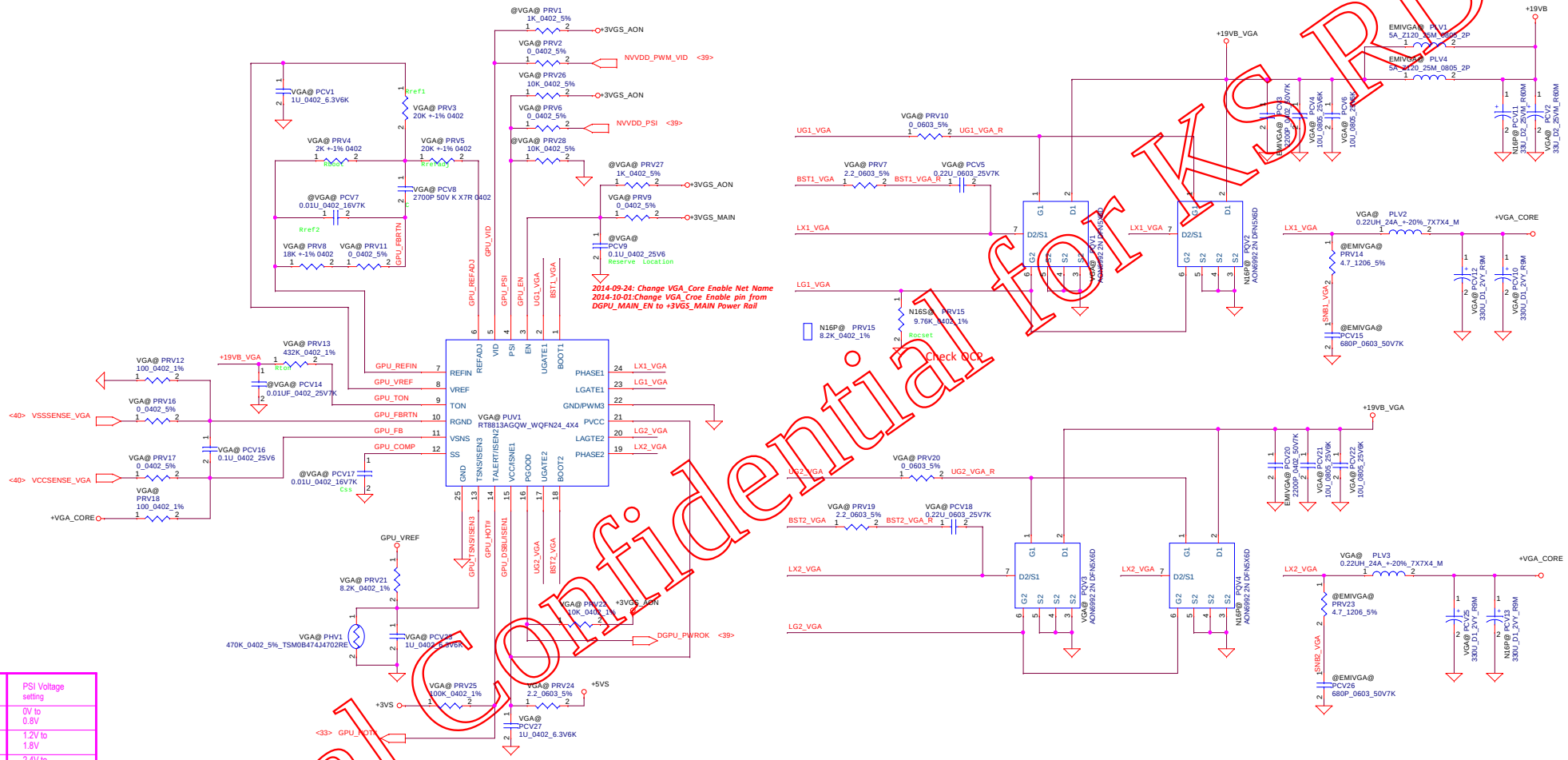
H-side MOS: AON6992
Rds(on):
4.3mohm@Vgs=10V
5.2mohm@Vgs=4.5V
Id :32A@Tc=100C

L-side MOS: AOS6992
Rds(on):
2mohm@Vgs=10V
2.2mohm@Vgs=4.5V
Id :66A@Tc=100C

Choke: 0.22UH (Size:7*7*3)
Rdc=0.98mohm +-5%
Heat Rating Current=28A



Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

1. VSNS Soft-Start time (Internal) is 0.7ms (PCV17 un-pop)
   Tss=(Css*Vrefin)/Iss+2.3ms
   =0.01U*0.9V/5uA+2.3ms=4.1ms (PCV17 pop)

2. Switching frequency setting:
   Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=353Khz

3. Thermal monitoring:
   (VGPU_VREF-VTSNS)/PRV21=VTSNS/Rth

	T_min	T_typical	T_max
PRV21=18.7K	99.16C	101.57C	103.94C
PRV21=13K	110.19C	112.75C	115.26C
PRV21=8.2K	125.15C	127.91C	130.62C

Switching Frequency : 353kHz
Ipeak(N16P-GT) : 70A
Iocp(N16P-GT) : 83A
Ipeak(N16-S-GT) : 50A
Iocp(N16S-GT): 61A

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **VGA_CORE**

Size	Document Number	Rev
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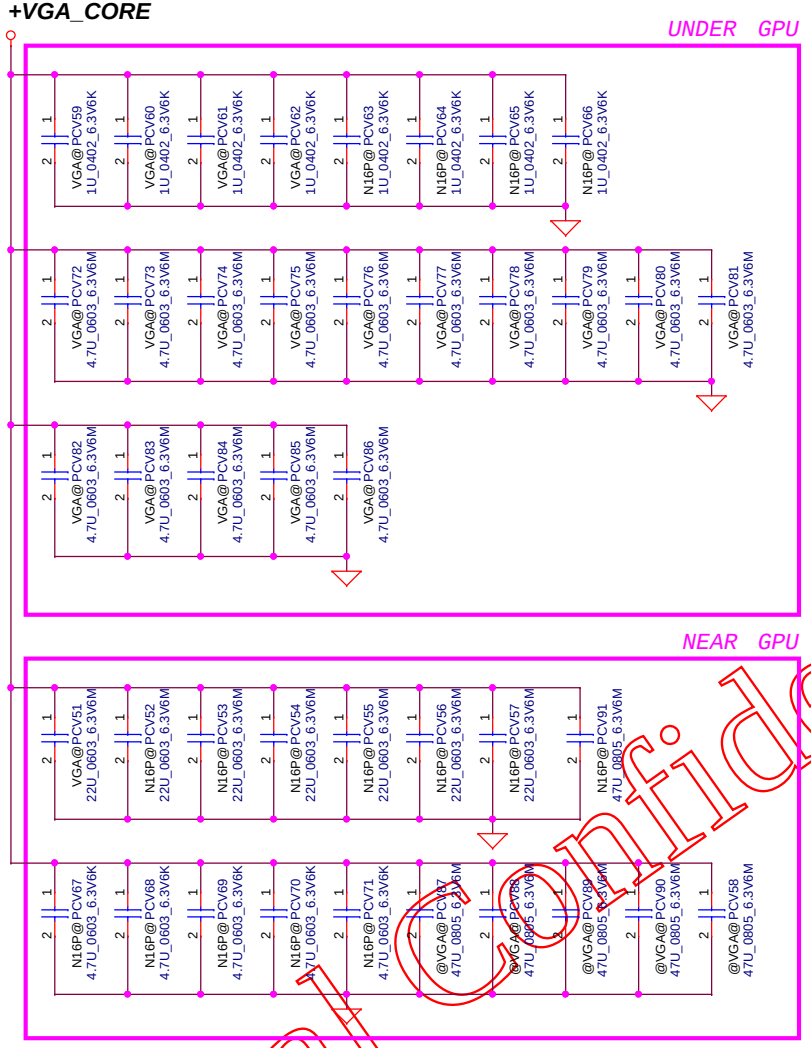
+VGA_CORE



N16S-GT
330U 2V LESR6M H1.9 (SGA00001Q80) X 3
47U 6.3V X5R 0805 (SE00000PL00) X 1
22U 6.3V X5R 0603 (SE00000M000) X 1
4.7U 6.3V X5R 0603 H0.8 (SE107475M80) X 15
1U 6.3V X5R 0402 (SE000000K80) X 4

N16P-GT
330U 2V LESR6M H1.9 (SGA00001Q80) X 4
22U 6.3V X5R 0603 (SE00000M000) X 7
4.7U 6.3V X5R 0603 H0.8 (SE107475M80) X 15
4.7U 6.3V X5R 0603 (SE107475K80) X 5
1U 6.3V X5R 0402 (SE000000K80) X 8

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: VGA CHIP DECOUPLING

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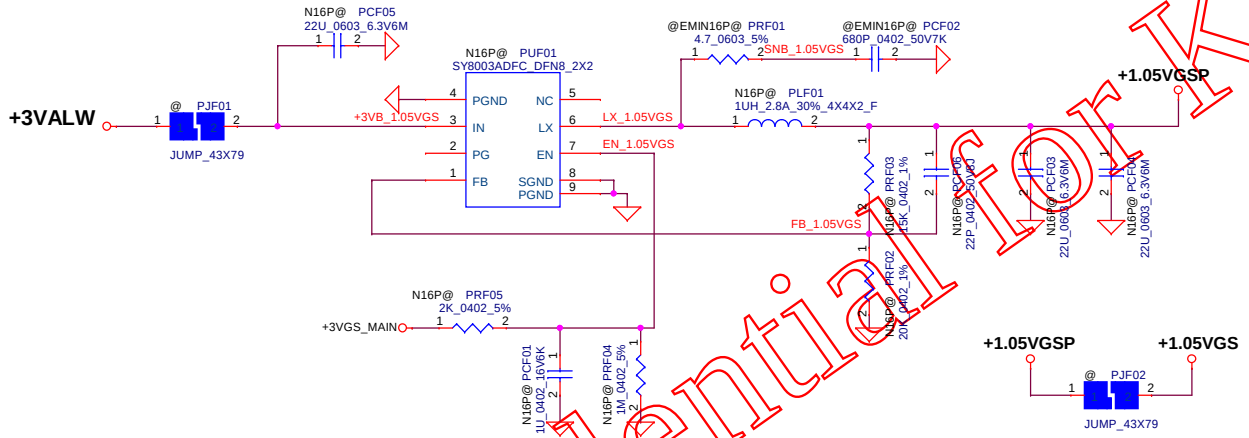
For Nvdia N16P-GT



3A continuous
3.5A current limit

Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **1.05VGS**

Size	Document Number	Rev
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							

Compal Electronics, Inc.

Title: PWR-PIR

Size: Custom | Document Number: <Doc> | Rev: 1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		ME request	0.2	P19	Change eDP Connector(JLCD1) for ME	12/15	
2		Screw Hole	0.2	P32	Change H20 from 3.0 mm to 3.3 mm	12/15	
3		Sub USB Power Switch	0.2	P26	Change Power Switch US5 circuit	12/15	
4		ME Flash Circuit	0.2	P6	Add ME FLASH Circuit	12/15	
5		Audio GND Bridge circuit	0.2	P28	Add two Resistor for HP request	12/15	
6		Add JUMP on JUSB1 and JUSB2 Power	0.2	P26	Add JUMP JPV5	12/19	
7		ESD request	0.2	P34	Change Touch PAD Diode for ESD request	12/19	
8		ESD request	0.2	P19	Reserve Touch Screen Diode for ESD	12/19	
9		ESD request	0.2	P19	Change Camera and D-MIC Diode for ESD request	12/19	
10		Audio team Request	0.2	P28	Change JSPK2 Pin define	12/22	
11		Vendor Request	0.2	P31 P33	Change Subwoofer circuit	12/22	
12		Customer Request	0.2	P35 P33	Add Shipping Mode Circuit	12/22	
13		RF Request	0.2	P26 P32	Reserve 68P and 82P on +3VALW and +USB_VCC4	12/23	
14		ESD request	0.2	P20	Change HDMI EMI Solution	12/23	
15		HW Modify	0.2	P48	Change N16X 1.35V and 1.05V solution	12/25	
16		HW Modify	0.3	P48	Change N16X 1.35V and 1.05V solution	01/23	
17		HW Modify	1.0	P32	Add DH5 for storage Mode	04/02	
18		Vendor Request	1.0	P31	Change Subwoofer circuit	04/02	
19		HW Modify	1.0		Change 0 ohm to short pad. RC8,RC108,RC119,RC378, RT19,RT37,RA32,RA34, RA38,RA39,RA50,RA51, RT17 RT18,RTS4	04/13	

Compal Electronics, Inc.

Title: HW PIR

Size: Custom | Document Number | Rev: 1.0

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