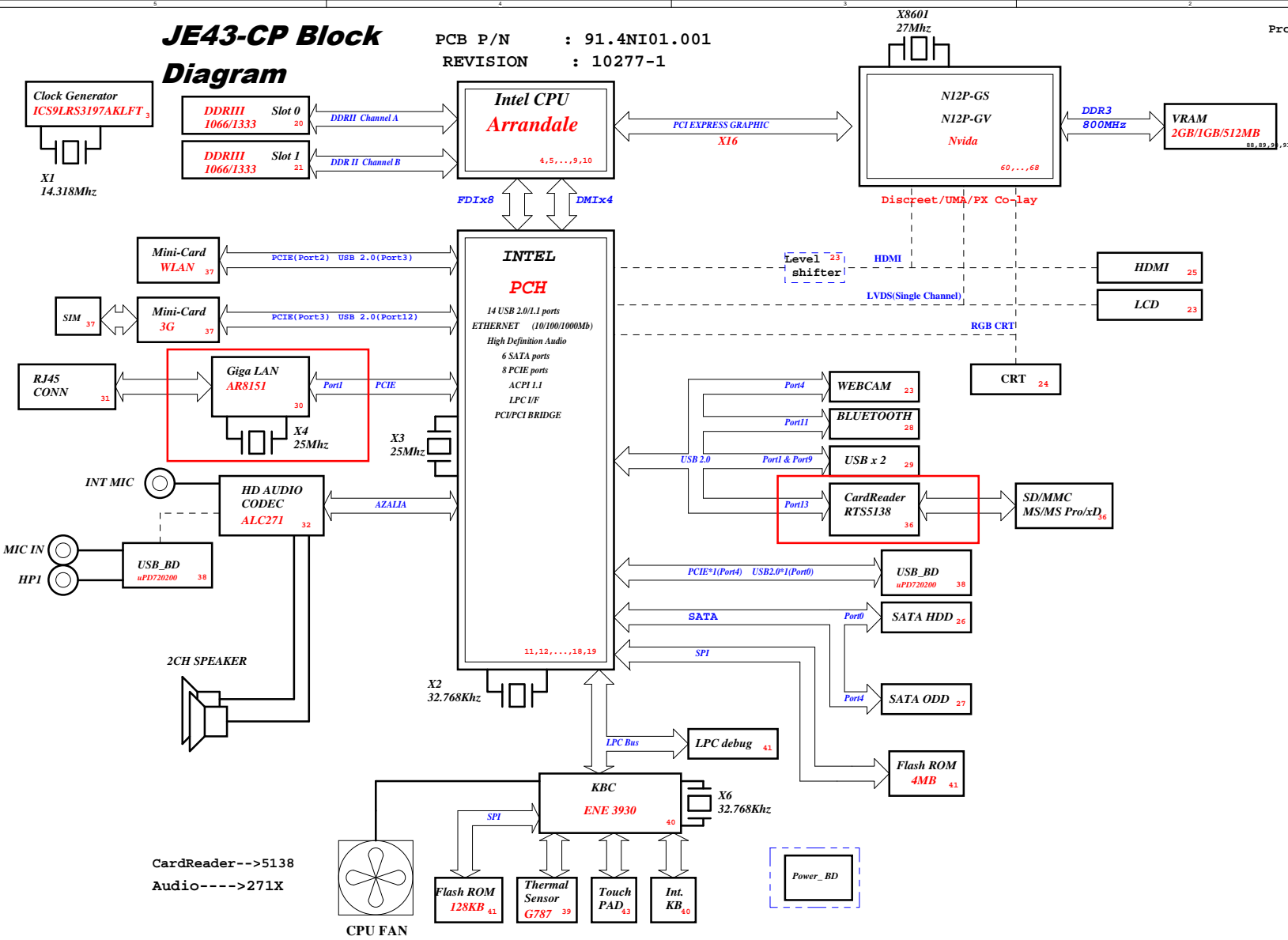


JE43-CP Block Diagram

PCB P/N : 91.4NI01.001
REVISION : 10277-1

Project code: 91.4NI01.001(JE43-CP)



CPU DC/DC ISL62881		54
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
SYSTEM DC/DC RT8209E		50
INPUTS	OUTPUTS	
DCBATOUT	1D05V_VFT	1D05V_S0
SYSTEM DC/DC		49
INPUTRT8220OUTPUTS		
DCBATOUT	SV_S5	3D3V_S5
SYSTEM DC/DC RT8209E		50
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3	ODP5V_S0
SYSTEM DC/DC ISL62881		54
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFXCORE_PWR	
VGA RT8208B		55
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	
TI CHARGER BQ24745		53
INPUTS	OUTPUTS	
DCBATOUT	BT+	
SYSTEM DC/DC RT9025		52
INPUTS	OUTPUTS	
3D3V_S0	1D8V_S0	
SYSTEM DC/DC RT9025		56
INPUTS	OUTPUTS	
3D3V_VGA_S0	1D8V_VGA_S0	
Switches		56
INPUTS	OUTPUTS	
1D5V_S3	1D5V_VGA_S0	
3D3V_S0	3D3V_VGA_S0	
1D05V_VFT	1V_VGA_S0	

PCB STACKUP

TOP _____
GND _____
S _____
S _____
GND _____
BOTTOM _____

Hynix 1G 800M N11PGV SKU

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

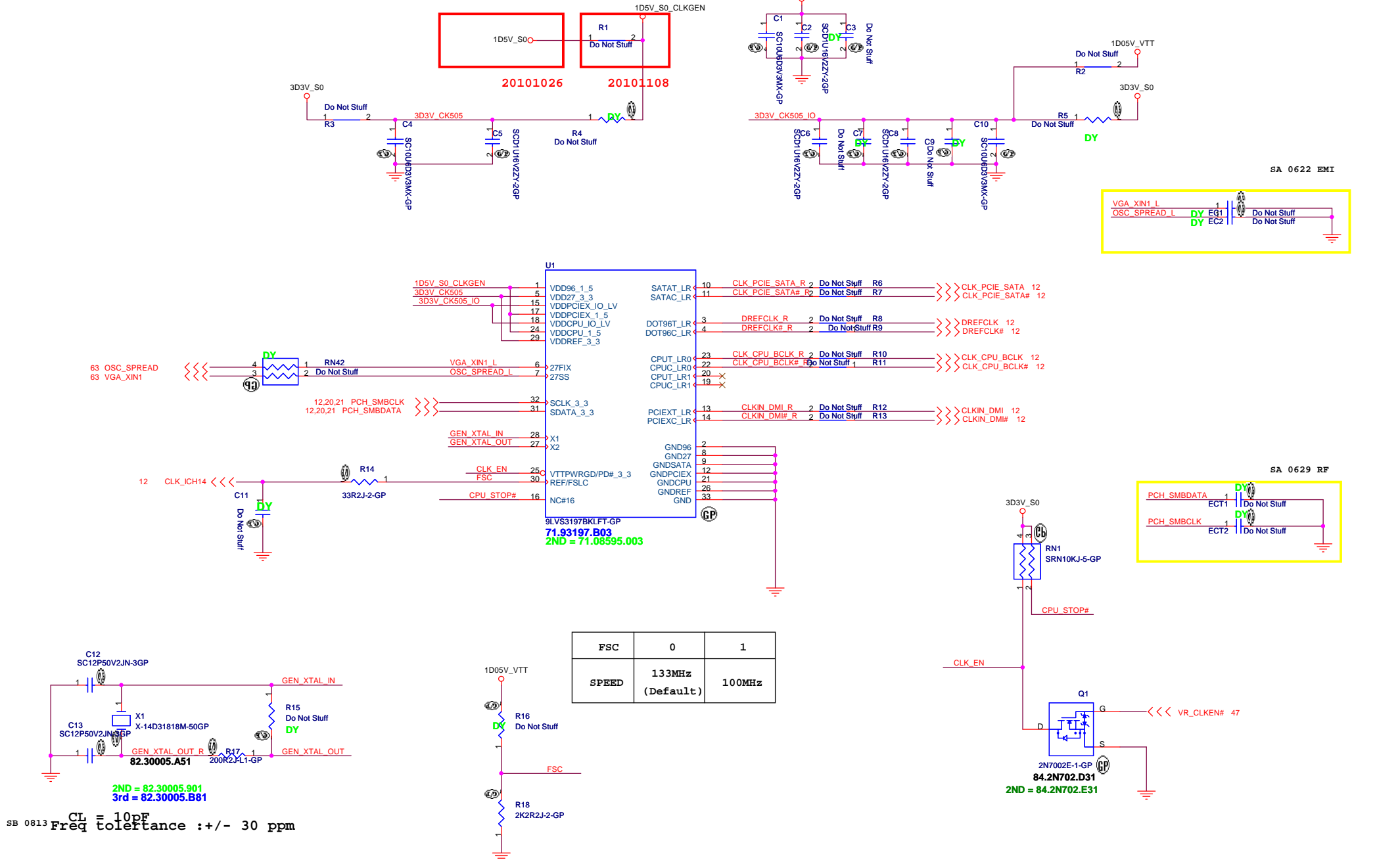
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Processor Strapping

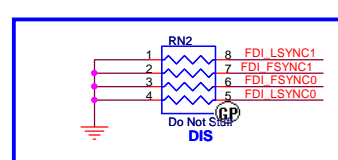
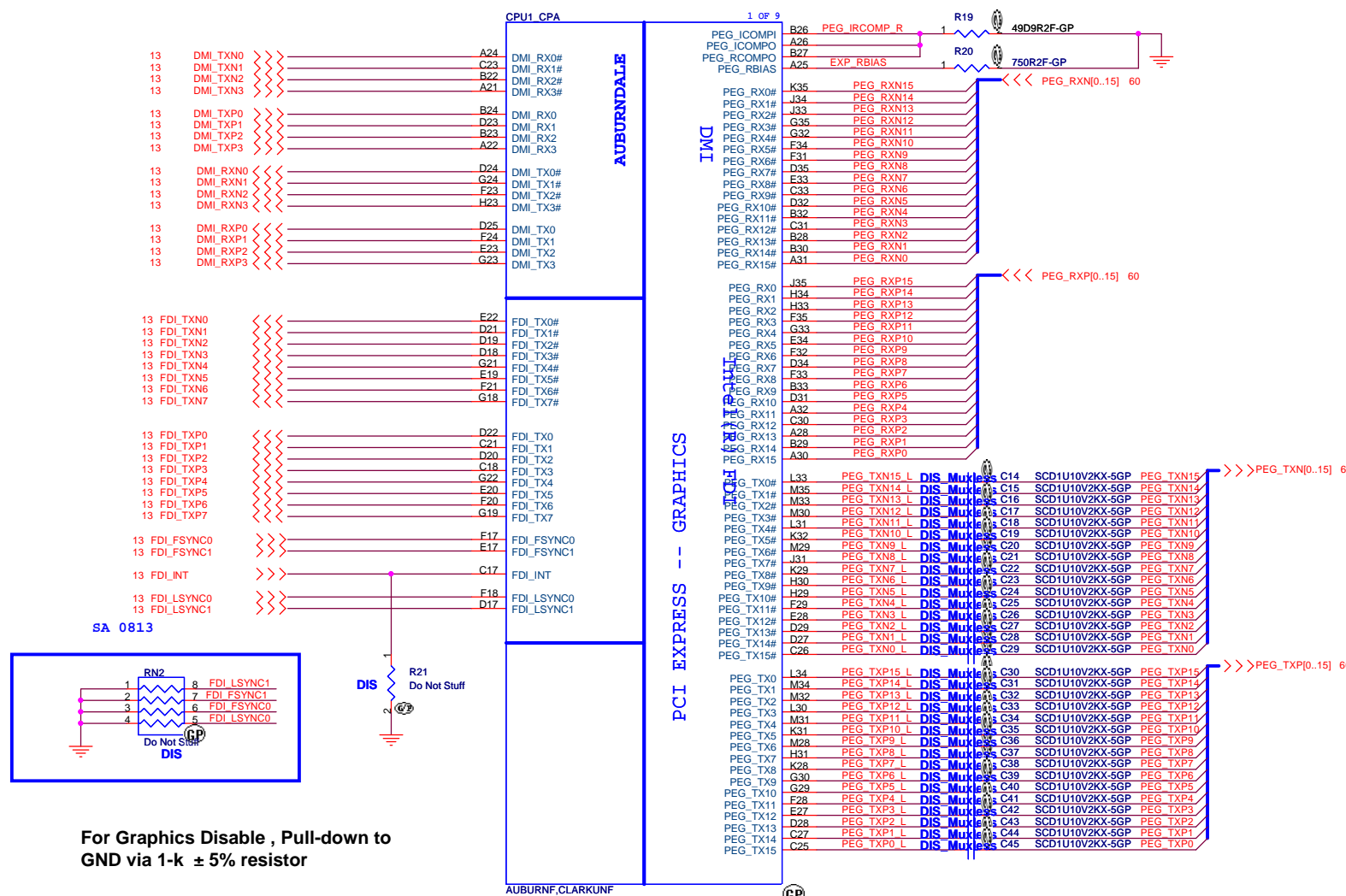
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

Hynix 1G 800M N11PGV SKU

<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div>		Title	
Size A3		Document Number	
Date: Wednesday, November 24, 2010		Sheet 2 of 69	
Table of Content		Rev	
JE43-CP		-1	



Hynix 1G 800M N11PGV SKU



For Graphics Disable , Pull-down to GND via 1-k ± 5% resistor

62.10055.321
3RD = 62.10055.341
4th = 62.10040.611
2ND = 62.10053.561

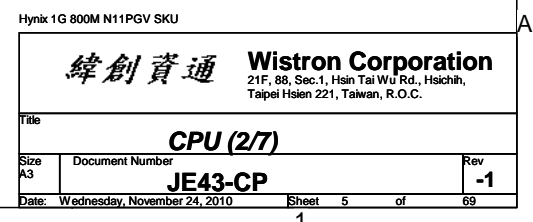
0113 -1

del 3rd 62.10055.341 and 4th 62.10055.321
3rd and 4th have been purged
CE will confirm SQM if it can add BOM
CE will release EC to add to BOM

lab stuff 2nd,3rd and 4 th in BOM
Eng add 1st source(62.10040.611)
Eng do not stuff 4 th in BOM
because 4 th have been purge ,so stuff 1st in BOM
but CE said, 4th need stuff in PD if not any concern

WMA4G-BOM-M-1PGV SKU

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU (1/7)	
Title Size A3 Date: Wednesday, November 24, 2010	Document Number JE43-CP Sheet 4 of 69
Rev -1	



AUBURNF,CLARKUNF
62.10055.321
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611

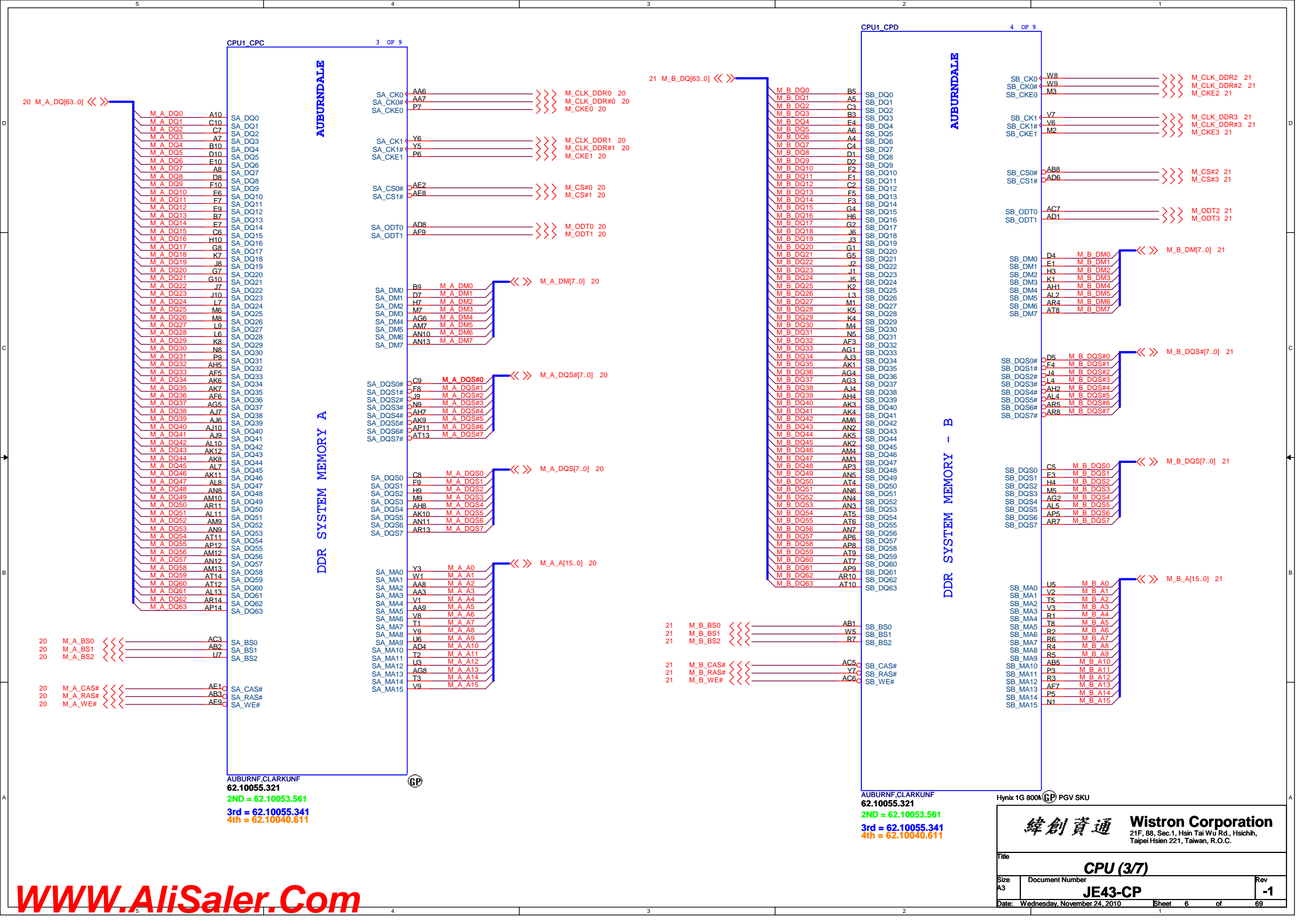


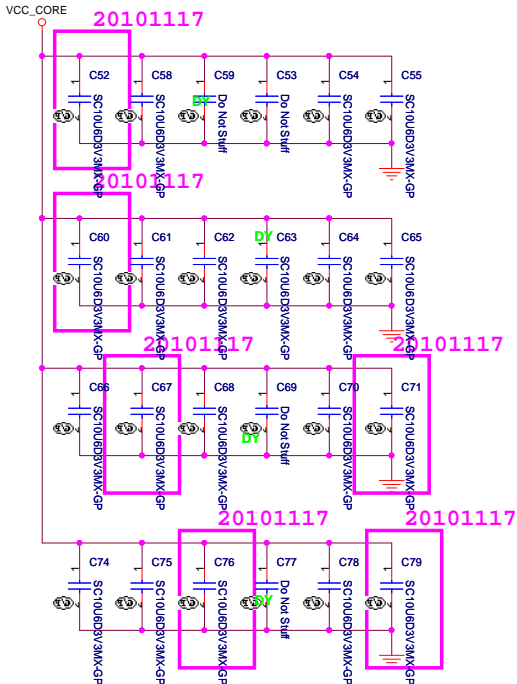
AUBURNF,CLARKUNF
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2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10040.611

Hynix 1G 800K GPV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU (3/7)
Size	Document Number	Rev	
A3	JE43-CP	-1	
Date:	Wednesday, November 24, 2010	Sheet	6 of 69





PROCESSOR CORE POWER

VCC_CORE
48A

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

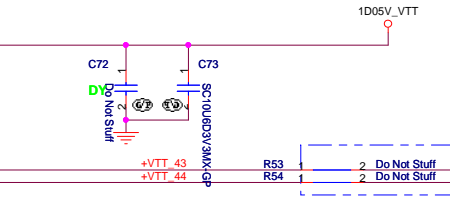
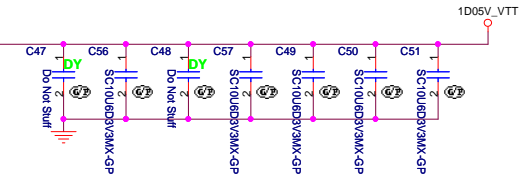
SENSE LINES

- VTT0 AH14
- VTT0 AH12
- VTT0 AH11
- VTT0 AH10
- VTT0 J14
- VTT0 J13
- VTT0 H14
- VTT0 H12
- VTT0 G14
- VTT0 G13
- VTT0 G12
- VTT0 F14
- VTT0 F13
- VTT0 F12
- VTT0 E11
- VTT0 E14
- VTT0 E12
- VTT0 D14
- VTT0 D12
- VTT0 D11
- VTT0 C14
- VTT0 C13
- VTT0 C12
- VTT0 C11
- VTT0 B14
- VTT0 B12
- VTT0 A14
- VTT0 A13
- VTT0 A12
- VTT0 A11

- VTT0 AF10
- VTT0 AE10
- VTT0 AC10
- VTT0 AB10
- VTT0 Y10
- VTT0 W10
- VTT0 U10
- VTT0 T10
- VTT0 J12
- VTT0 J11
- VTT0 J16
- VTT0 J15

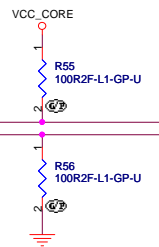
PSI# >AN33 >>> PSI# 47
AK35 H_VID0 >>> H_VID[6..0] 47
AK33 H_VID1 >>>
AK34 H_VID2 >>>
AL35 H_VID3 >>>
AL33 H_VID4 >>>
AM33 H_VID5 >>>
AM35 H_VID6 >>>
AM34 >>> PM_DPRSLPVR 47
G15 H_VTTVID1 1 TP7 Do Not Stuff
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

ISENSE >AN35 <<< IMVP_IMON 47
VCC_SENSE >AJ34 >>> VCC_SENSE 47
>AJ35 >>> VSS_SENSE 47
VTT_SENSE >B15 >>> VTT_SENSE 51
>A15 TP VSS_SENSE_VTT 1 TP8 Do Not Stuff

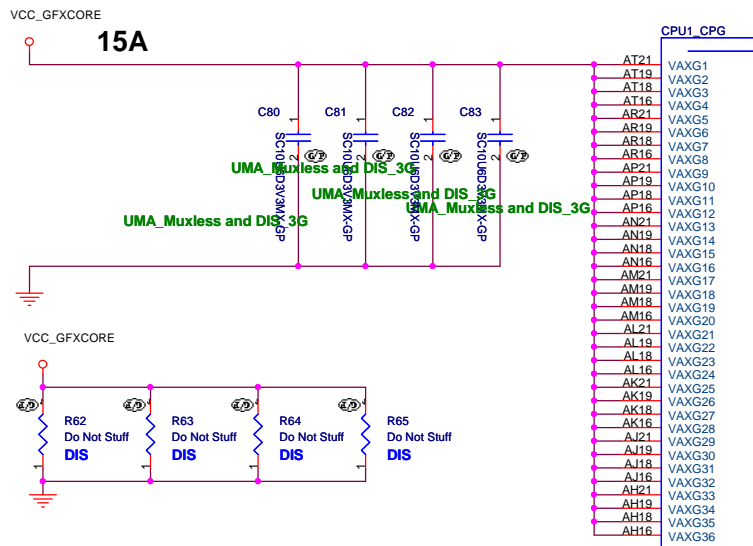


The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

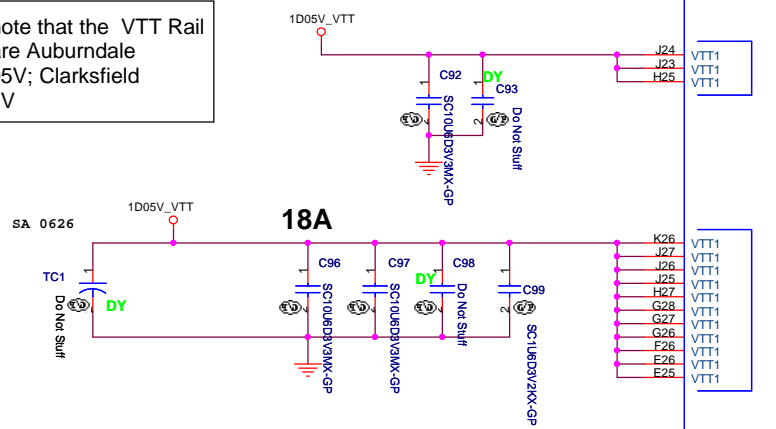
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



AUBURNF.CLARKUNF
62.10055.321
2ND = 62.10053.561 3rd = 62.10055.341 4th = 62.10040.611



Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

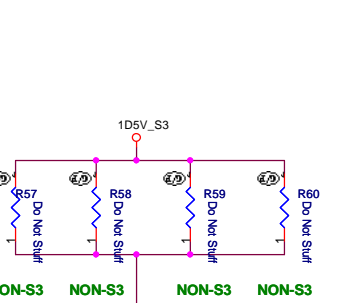
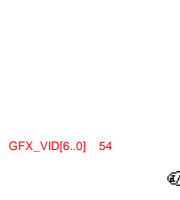
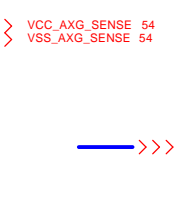
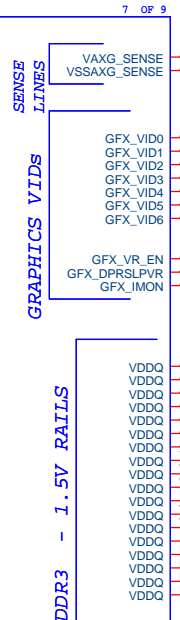


AUBURNDALE

GRAPHICS

POWER

PEG & DMI



VDDQ 3A for Auburndale
VDDQ 6A for Clarksfield

13.20 PM_SLP_S3_CTLD >>>

original reservation 10uF
0123 -1 RF

2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

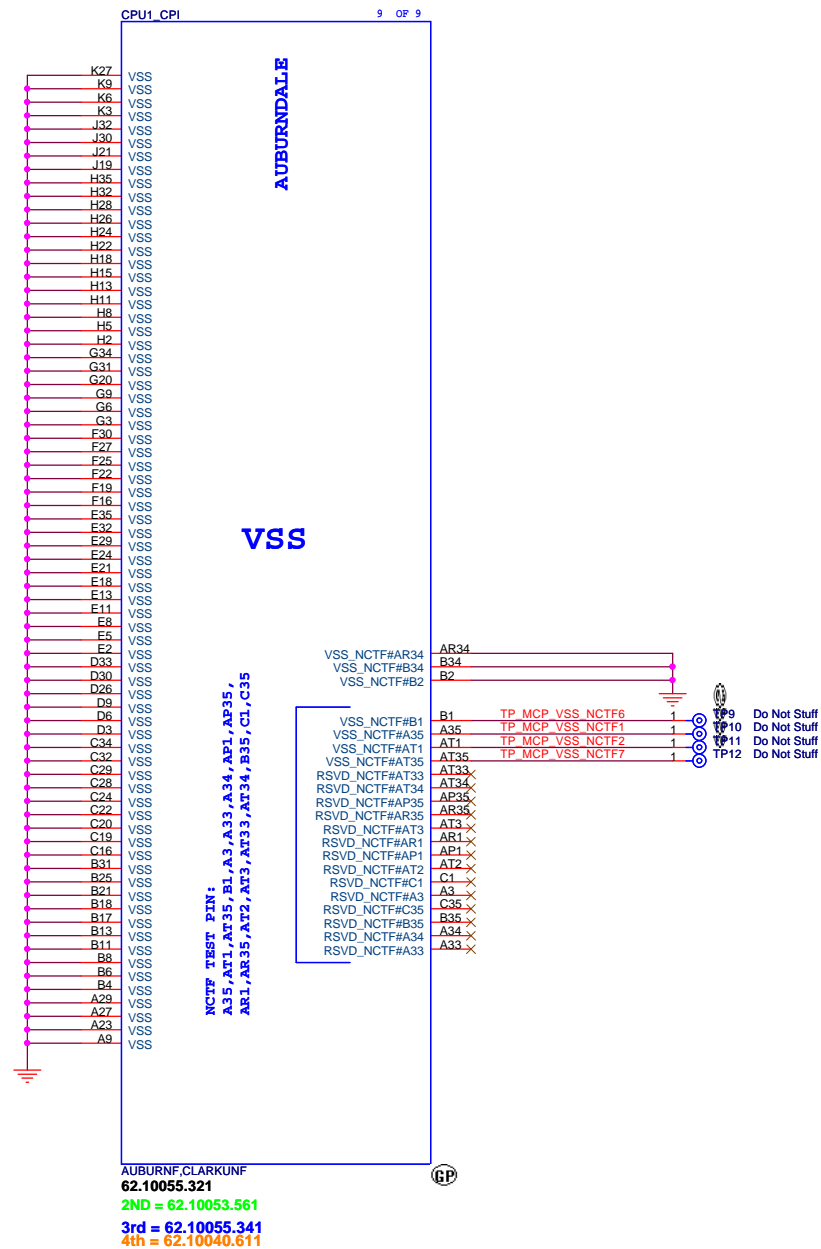
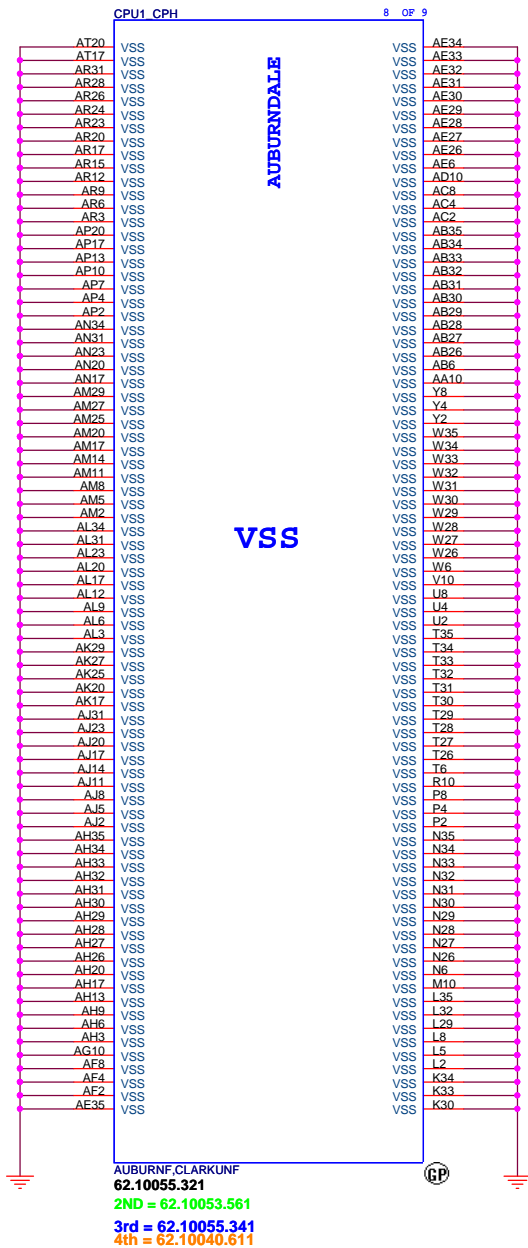
1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

1D05V_VTT

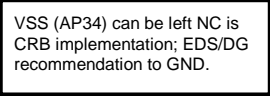


Hynix 1G 800M N11PGV SKU

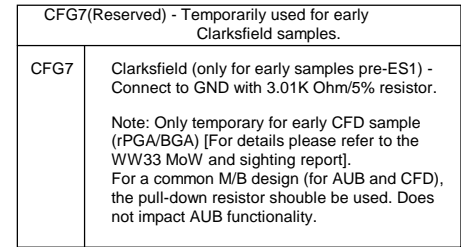
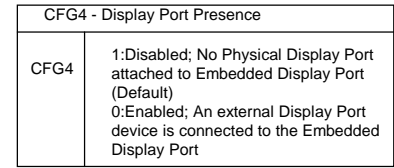
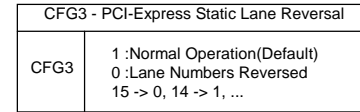
20 M_VREF_DQ_DIMM0 <<< 1 2 3 4 H_RSVD9_R
 21 M_VREF_DQ_DIMM1 <<< 2 3 4 H_RSVD10_R

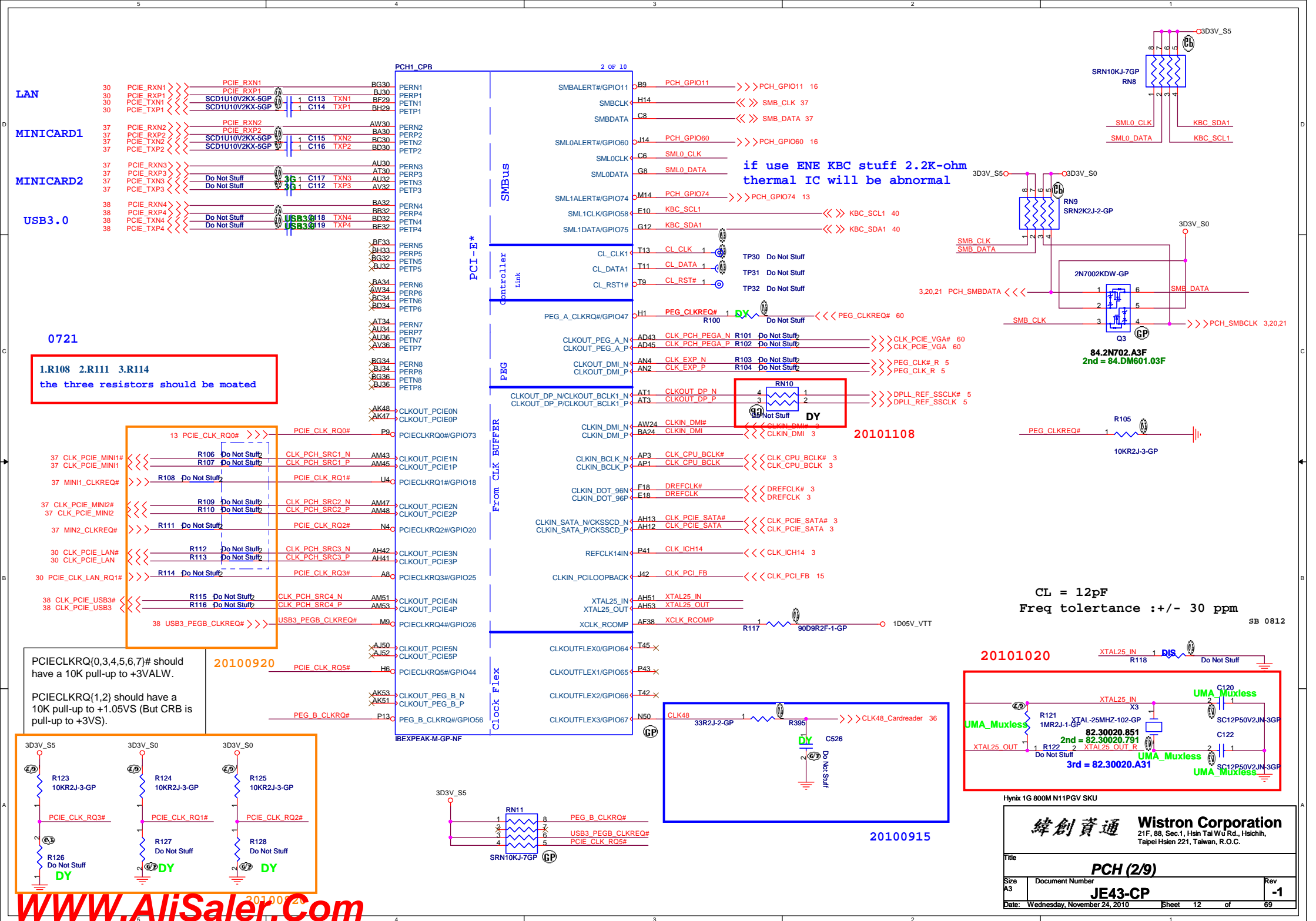
Do Not Store
 DY

20101108

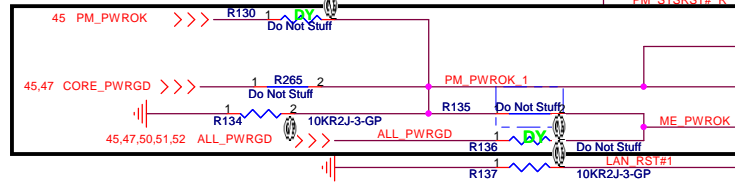


PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled





0804 SA
1.cause of thermal sensor
2.solution by JM31-CP

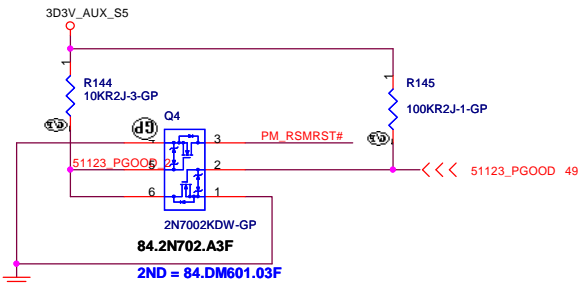


5 PM_DRAMPWROK <<< PM_DRAMPWROK

40 SUS_PWR_DN_ACK <<< 1 R139 2 Do Not Stuff SUS_PWR_DN_ACK

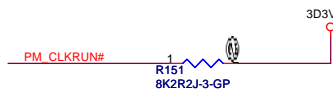
40,59 PM_PWRBTN# >>> 1 R141 2 Do Not Stuff PM_PWRBTN#_R

40 AC_PRESENT >>> 1 R143 2 Do Not Stuff AC_PRESENT_R

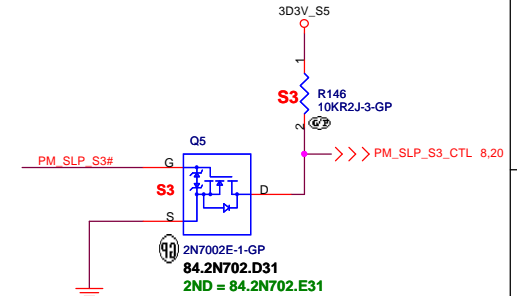
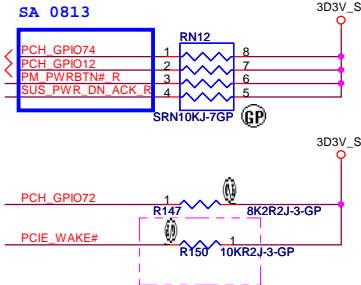


40 RSMRST#_KBC >>> 3
Do Not Stuff
2ND = 83.BAT54.D81
3rd = 83.00054.S81

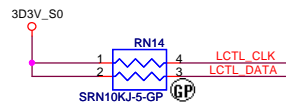
12 PCIE_CLK_RQ0# <<< AC_PRESENT_R
PCIE_CLK_RQ0#
PM_R#



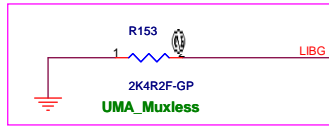
change pull up 1K to 10K for Intel suggestion



Hynix 1G 800M N11PGV SKU

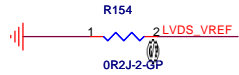


UMA_Muxless

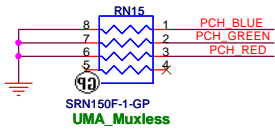


UMA_Muxless

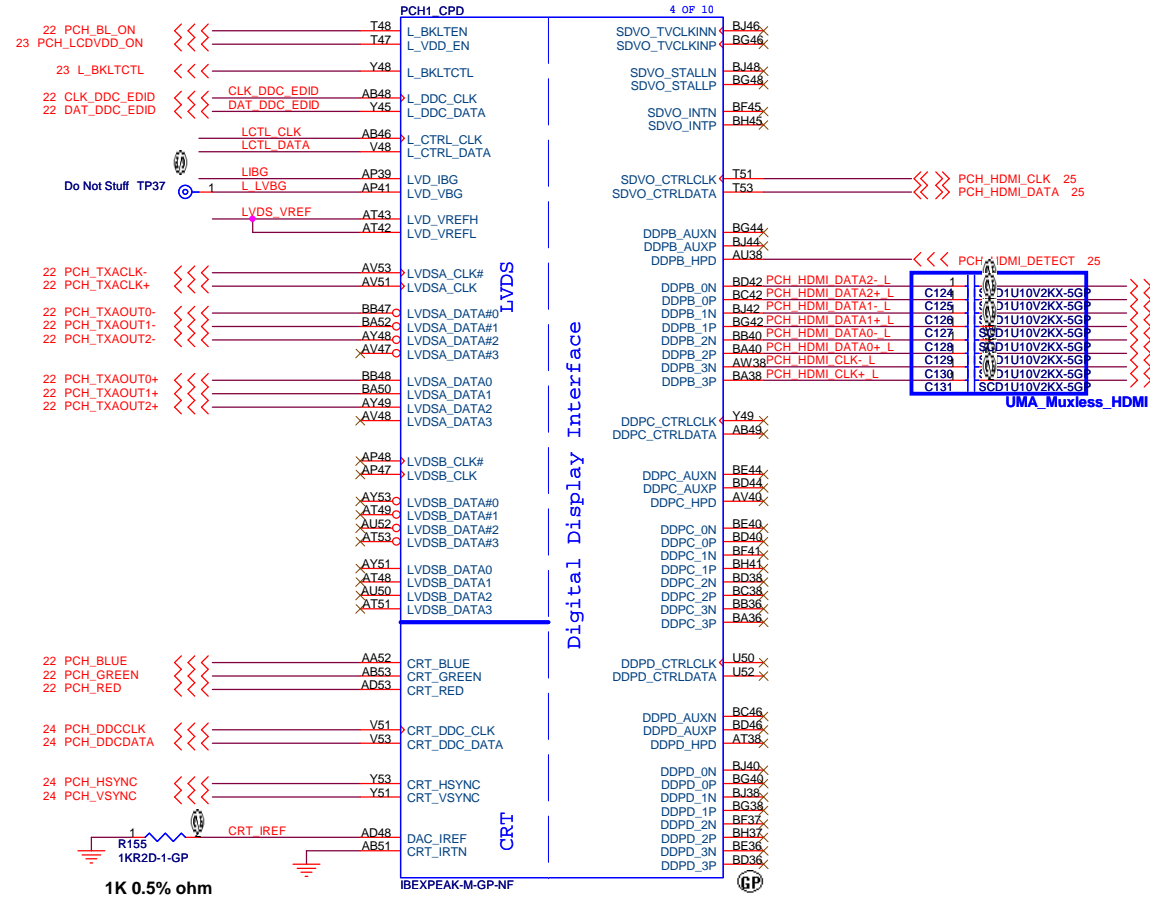
Muxless->64.23715.6DL,UMA-2.4K



UMA_Muxless



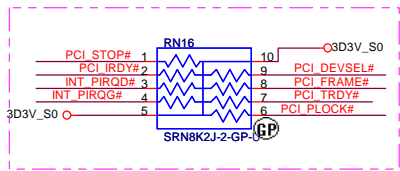
UMA_Muxless



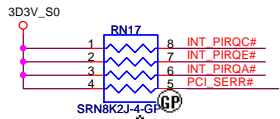
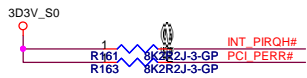
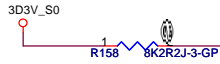
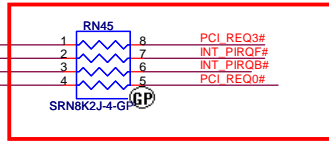
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (4/9)		
Size	Document Number	Rev
A3	JE43-CP	-1
Date:	Wednesday, November 24, 2010	Sheet 14 of 69



These pins are left as NC, because the function is disable.

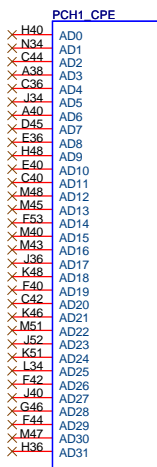
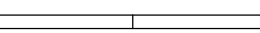
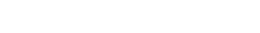
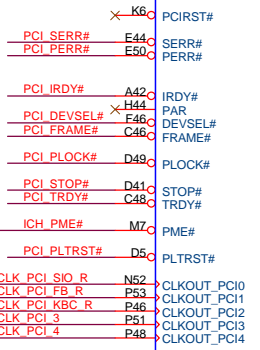
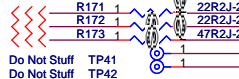


PCH strapping

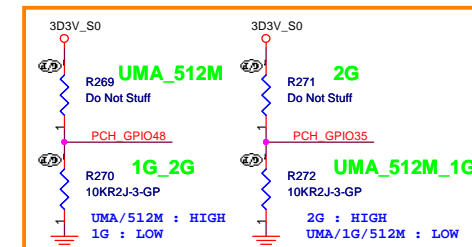
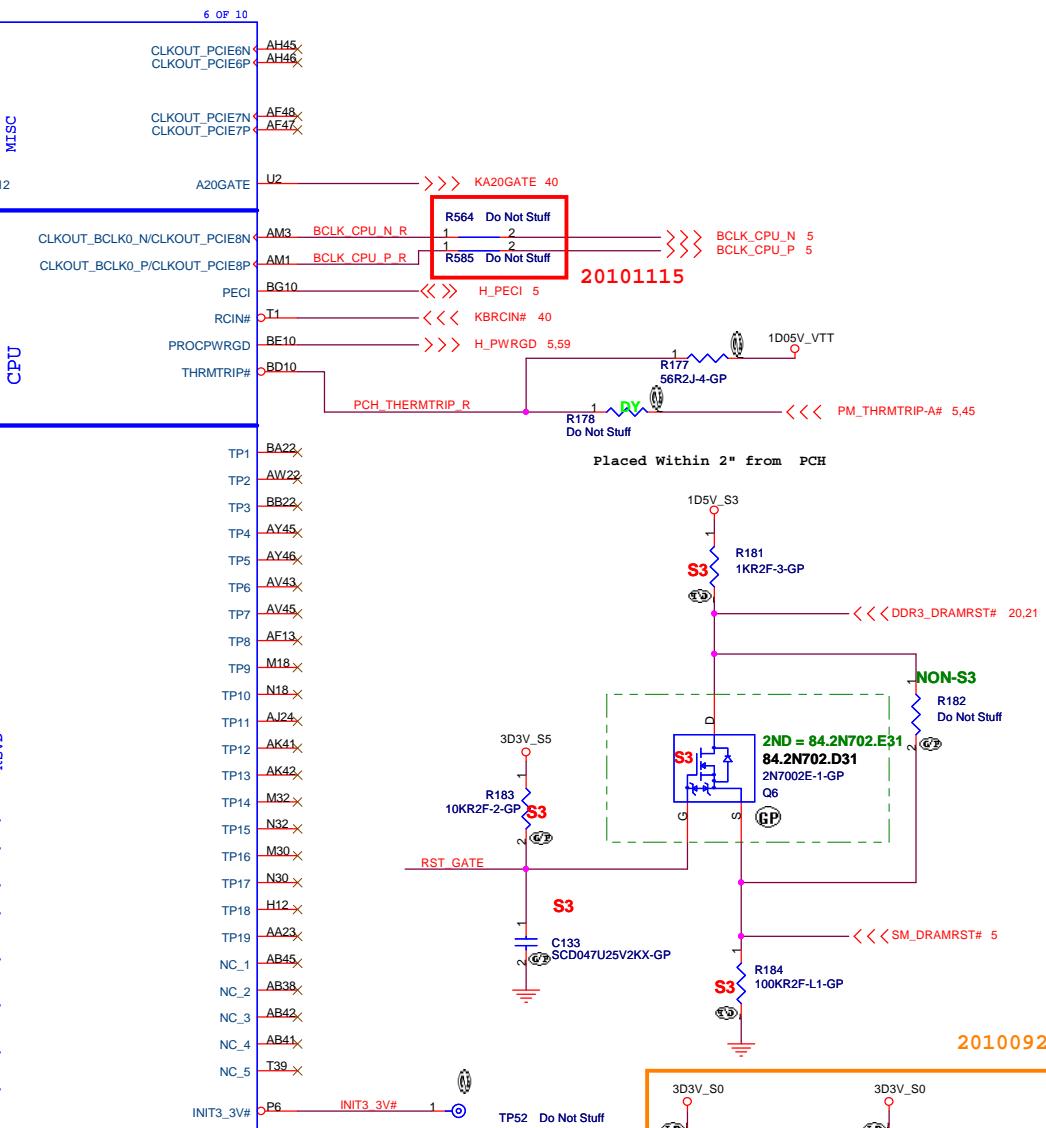
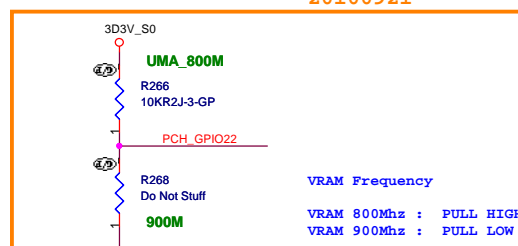
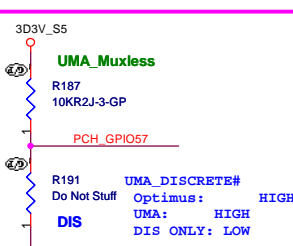
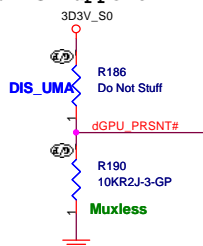
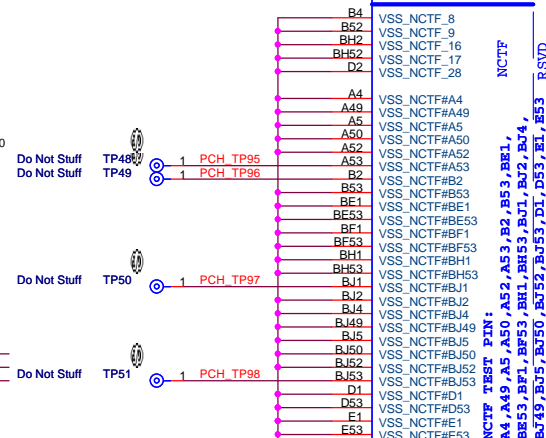
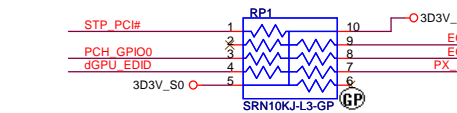
BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI(Default)

PCI_GNT#1	
1	Default (internal pull-up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

41 PCLK_FWH
12 CLK_PCI_FB
40 CLK_PCI_KBC

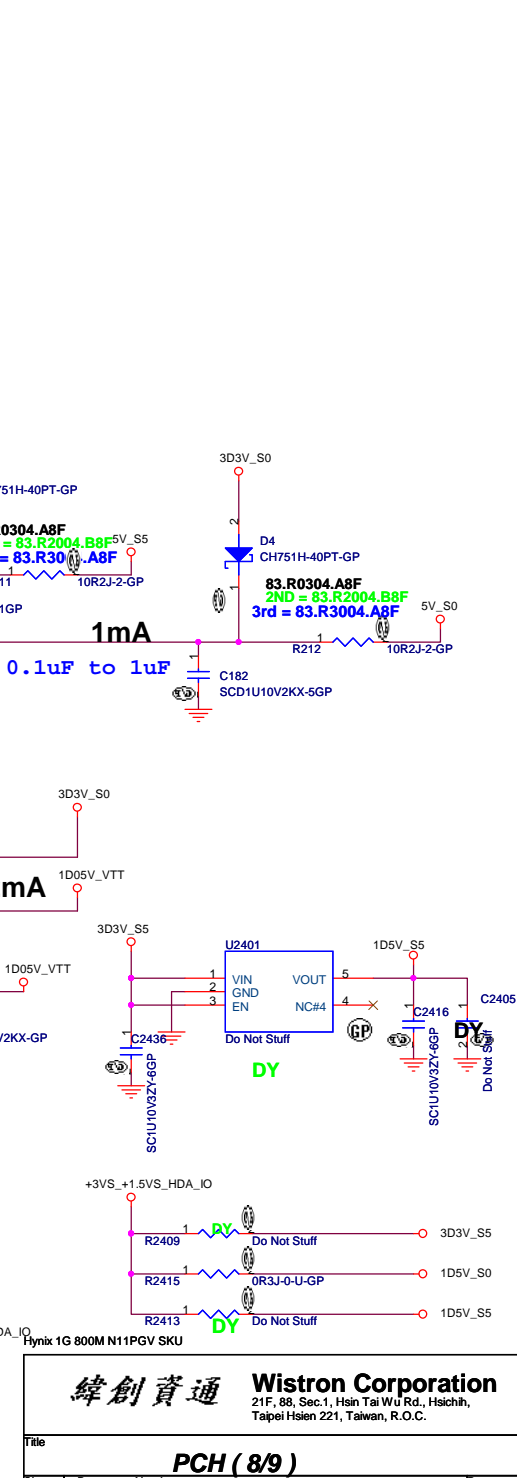
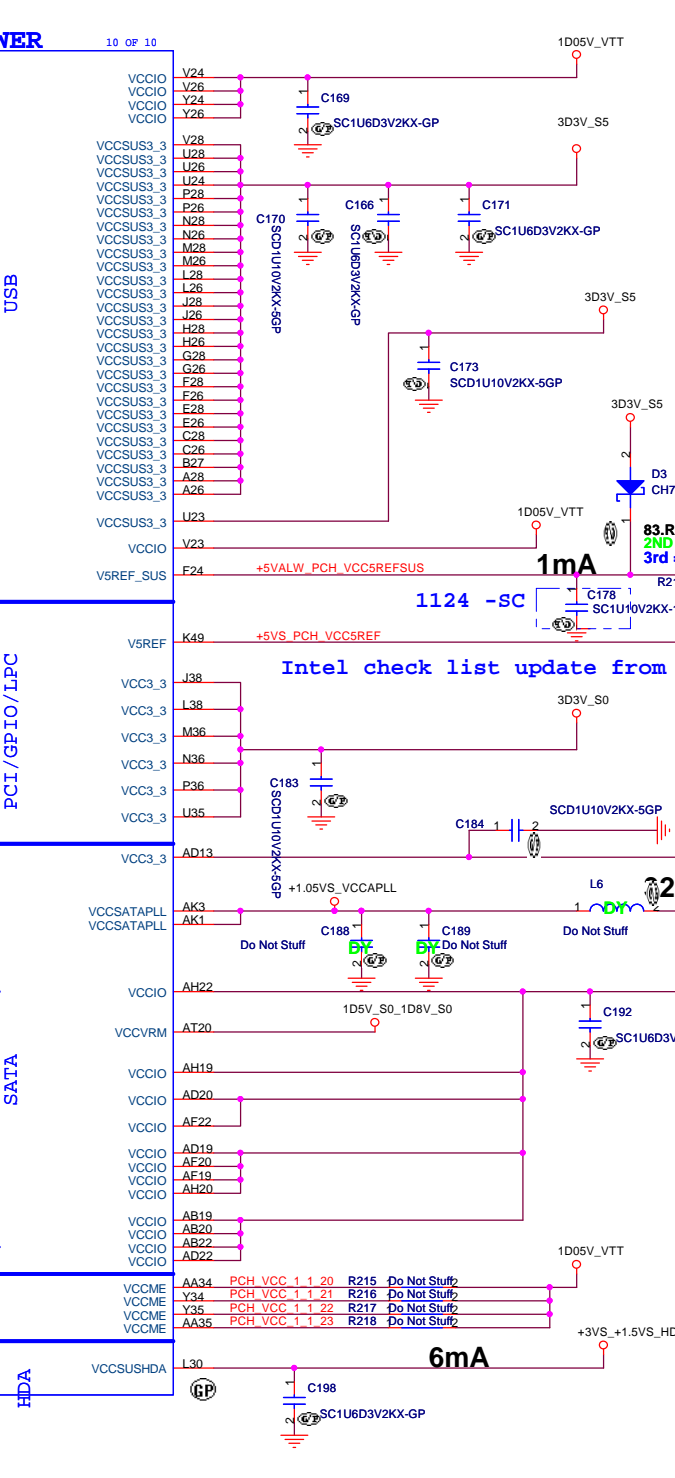
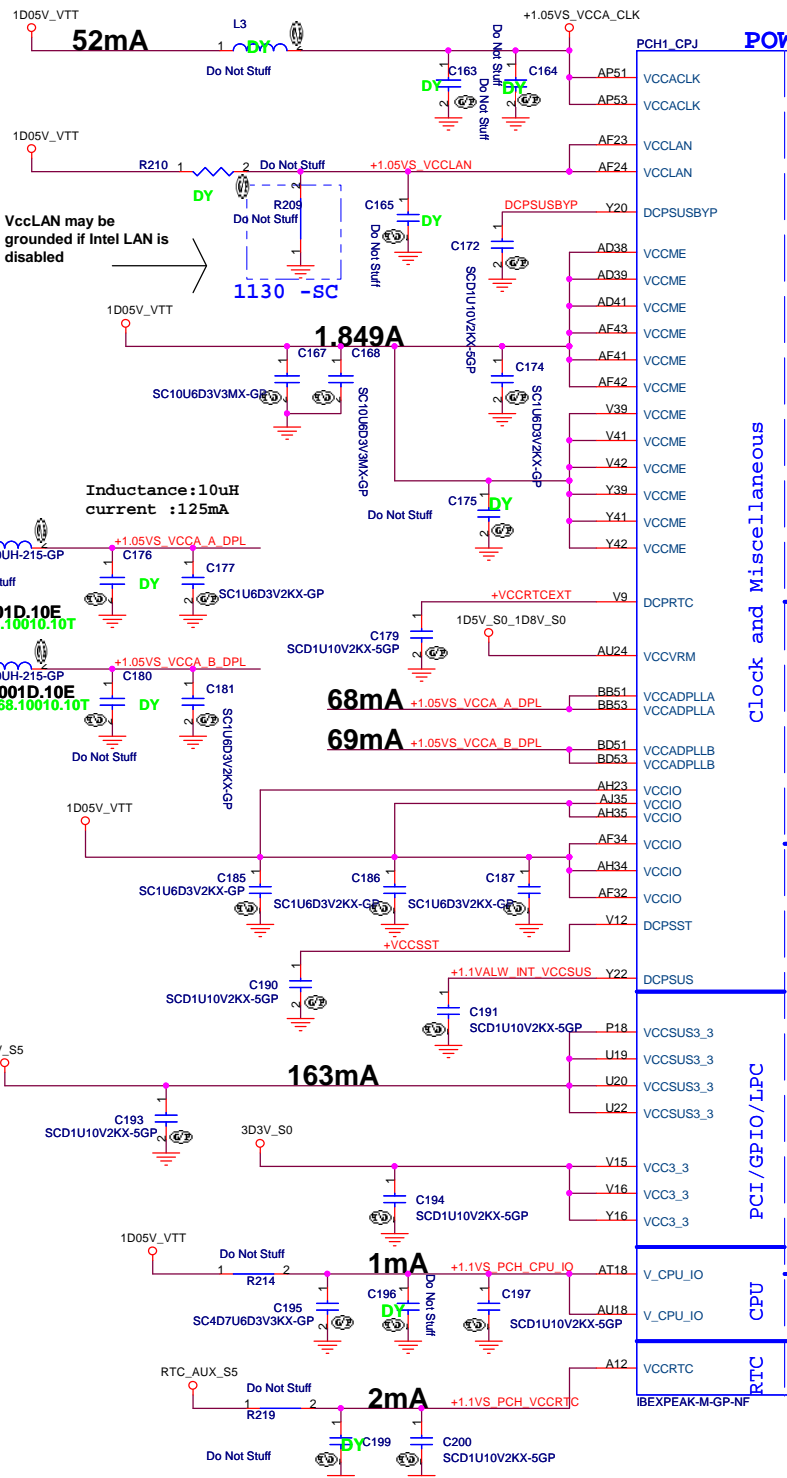


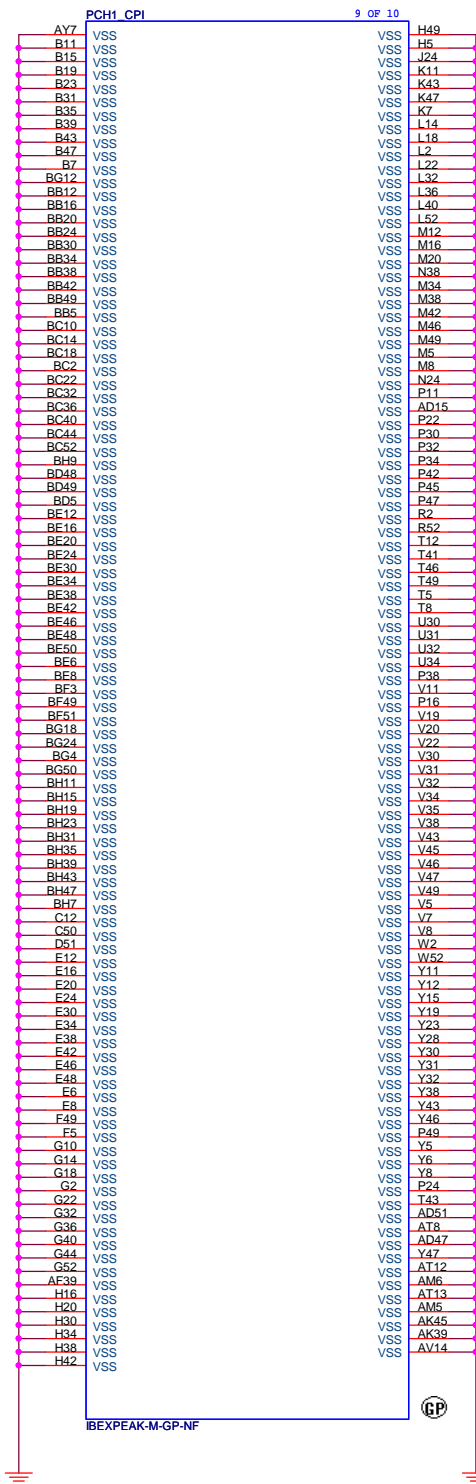
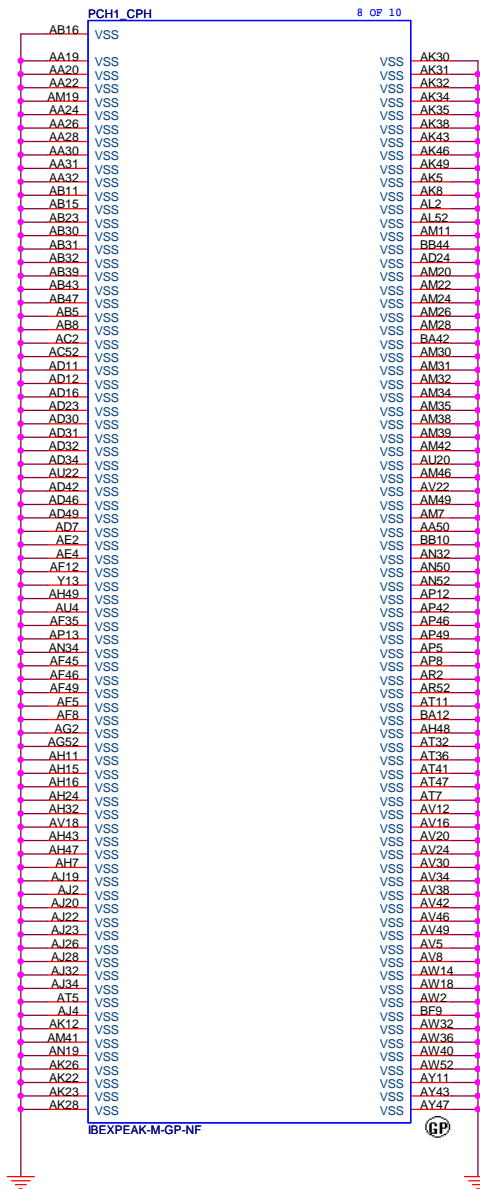
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



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Title			
PCH (6/9)			
Size A3	Document Number		Rev
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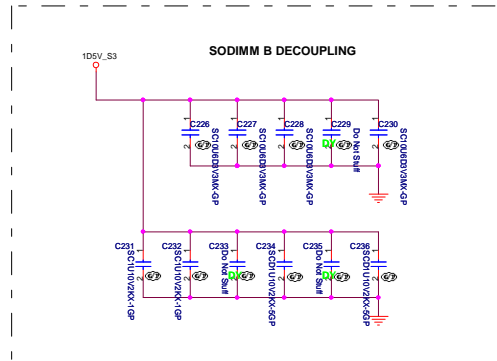




Hynix 1G 800M N11PGV SKU

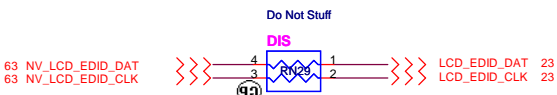
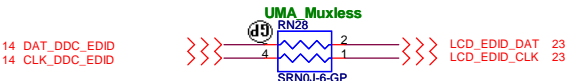
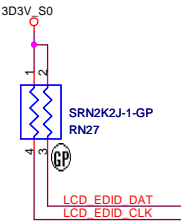
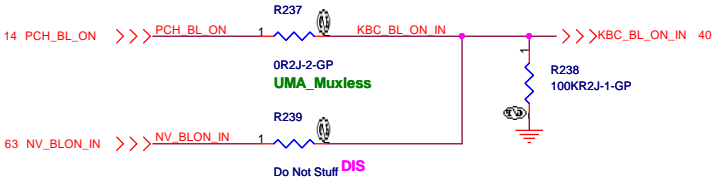
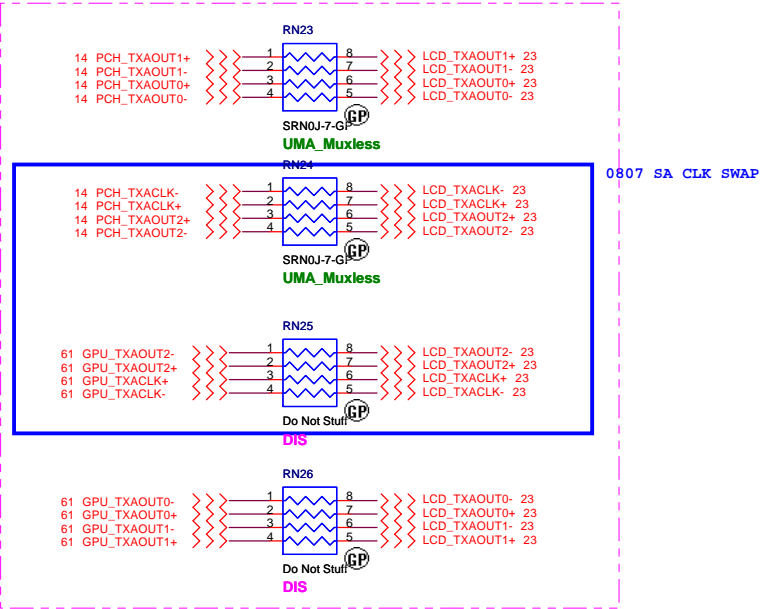
緯創資通 **Wistron Corporation**
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Title			
PCH (9/9)			
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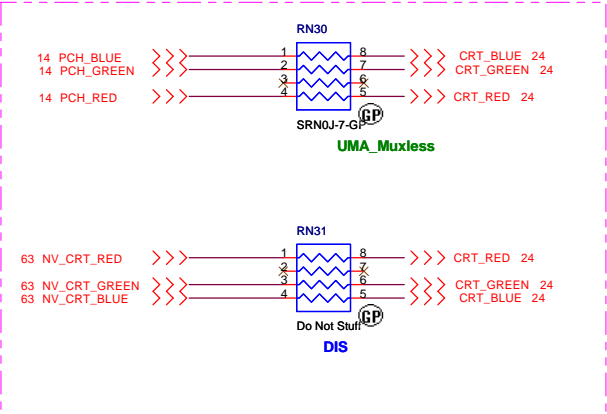


SO-DIMMB is placed farther from the Processor than SO-DIMMA

LCD



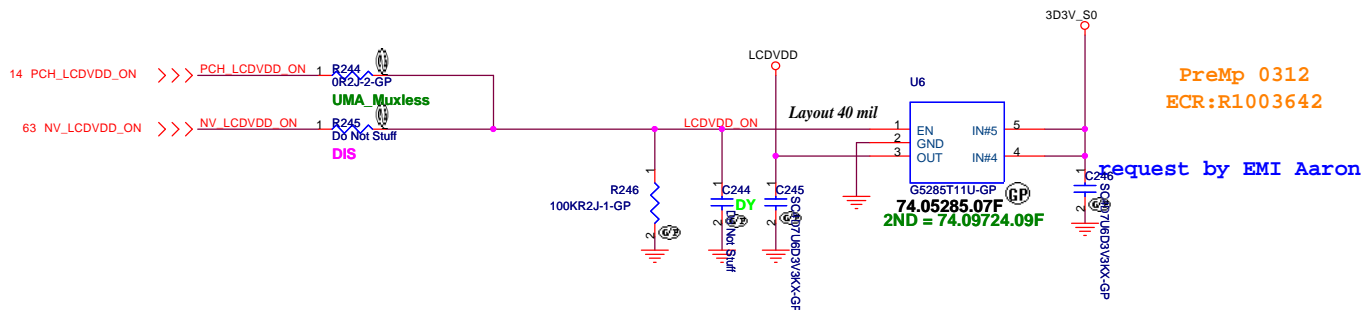
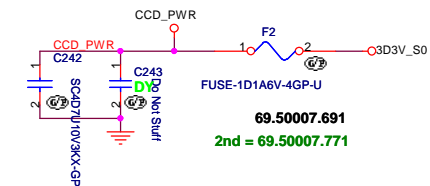
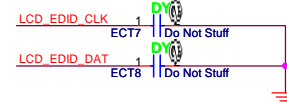
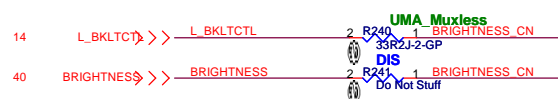
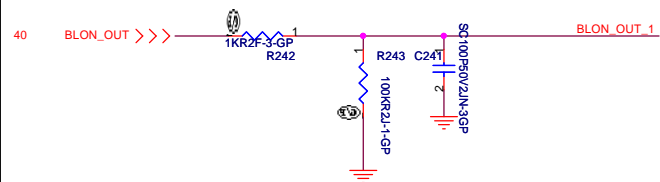
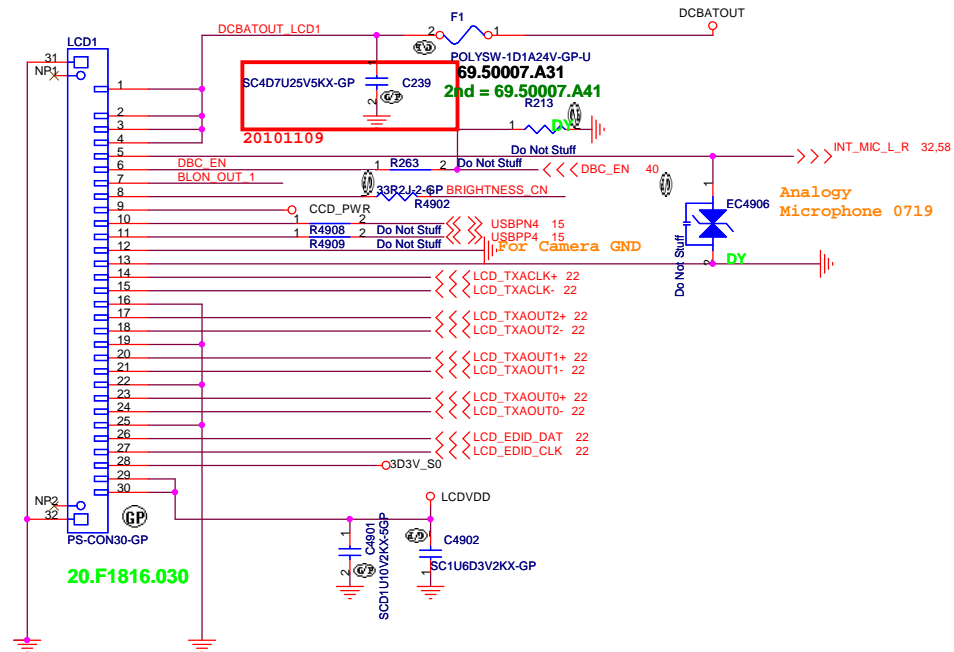
CRT



Hynix 1G 800M N11PGV SKU

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Title			
LCD CRT SWITCHABLE			
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LCD/CCD CONN



PreMp 0312
ECR:R1003642

request by EMI Aaron

Hynix 1G 800M N11PGV SKU

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD CONN

Size

Document Number

JE43-CP

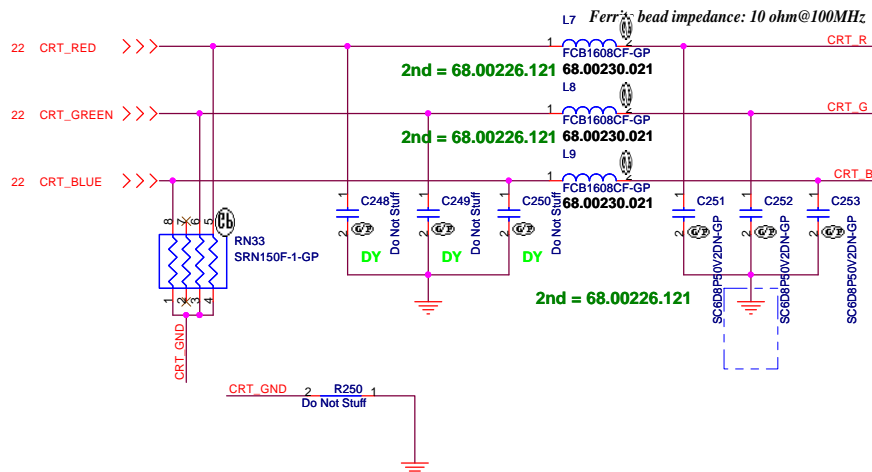
-1

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Sheet	23
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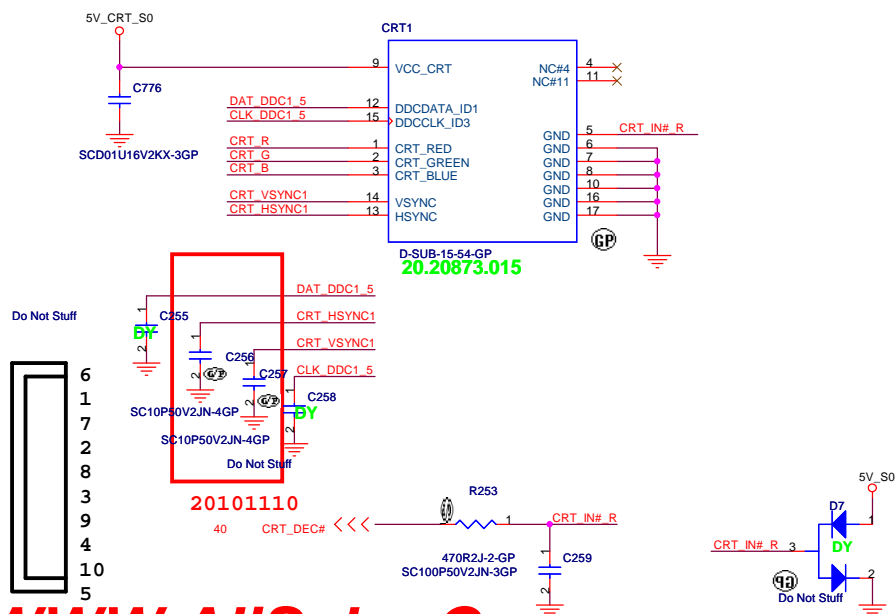
69

Layout Note:
Place these resistors
close to the CRT-out
connector

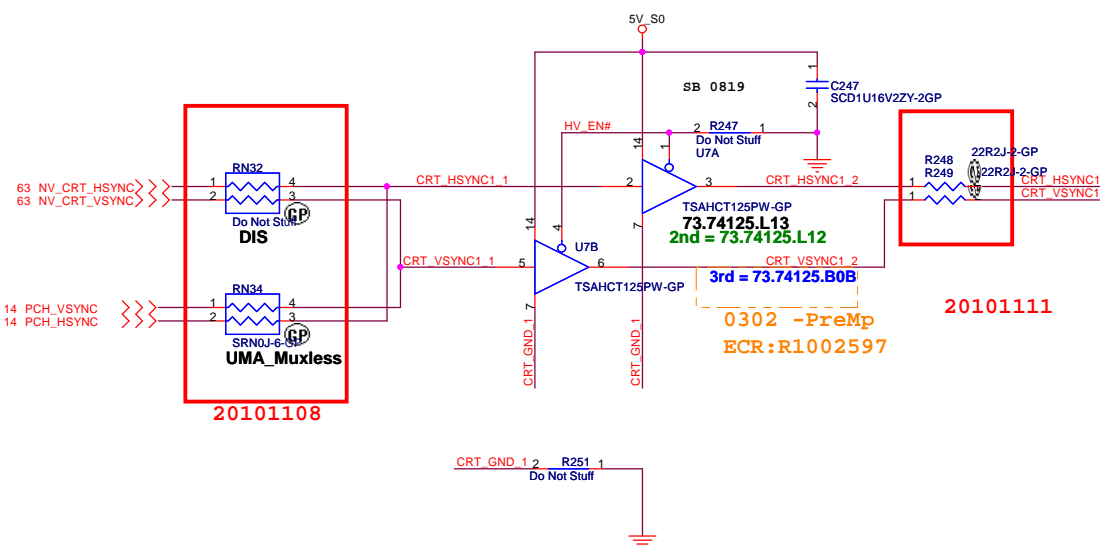


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

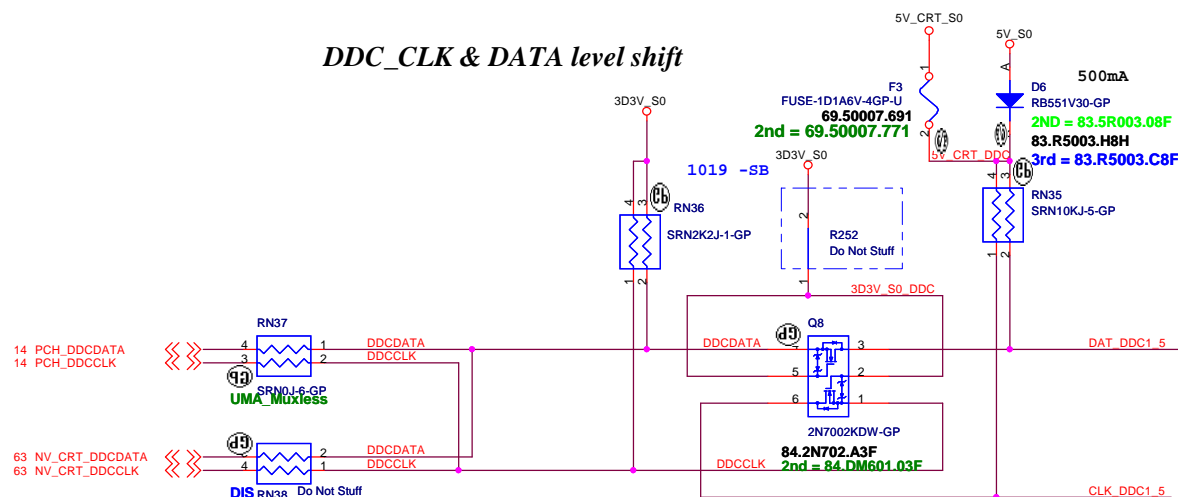
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC CLK & DATA level shift

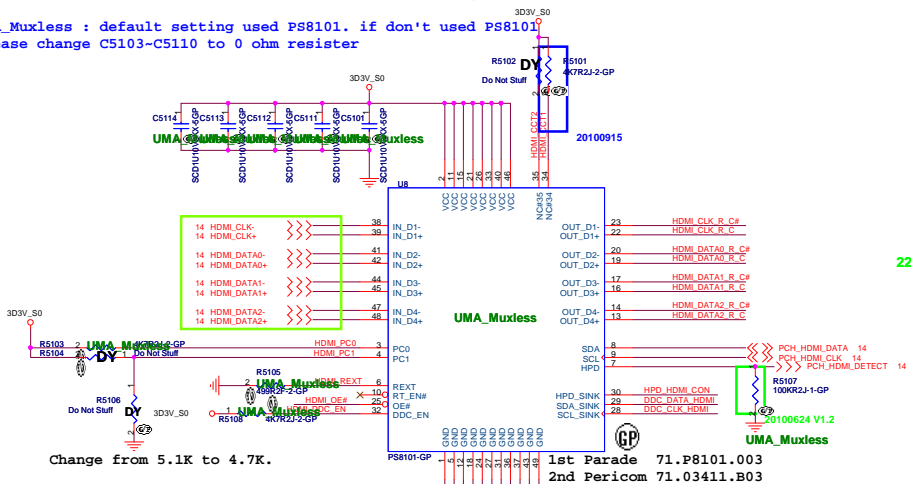


Hynix 1G 800M N11PGV SKU

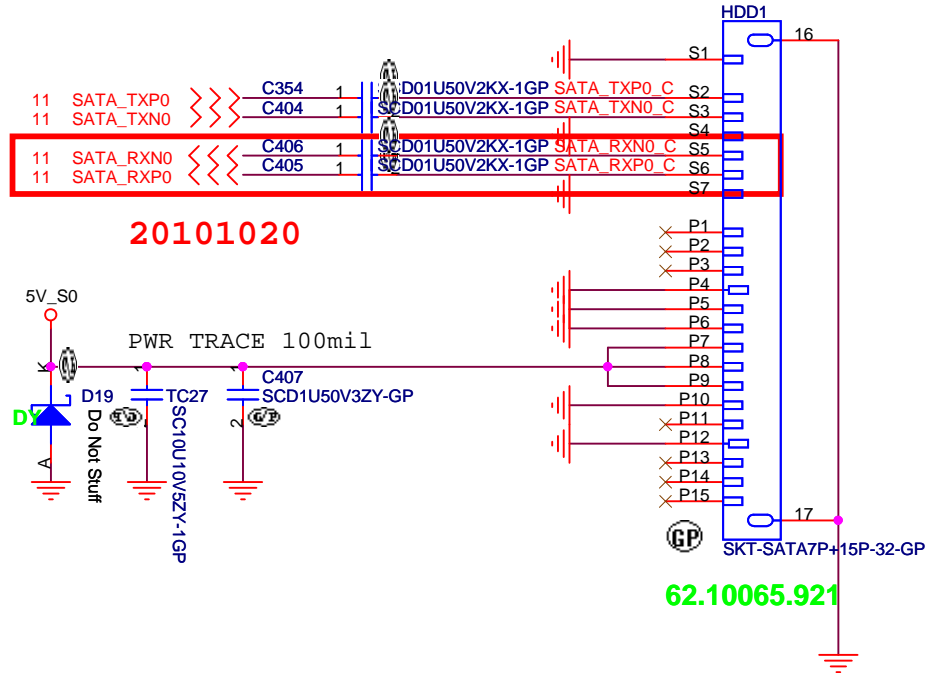
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
CRT CONN			
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UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103-C5110 to 0 ohm resistor



SATA Connector



Hynix 1G 800M N11PGV SKU

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Title

HDD CONN

Size	Document Number
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JE43-CP

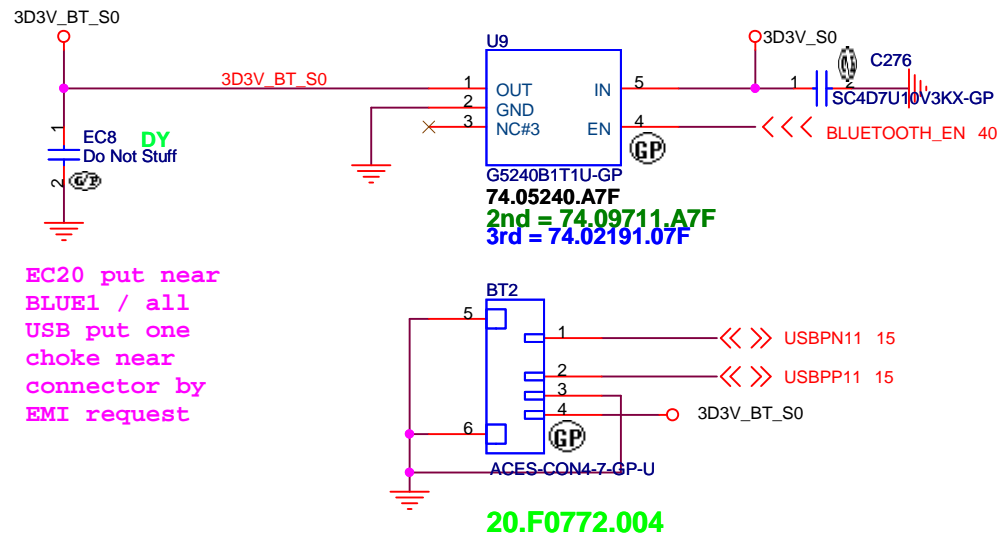
Rev	-1
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[illegible]

20101108

BLUETOOTH MODULE



Hynix 1G 800M N11PGV SKU

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Title

BLUETOOTH CONN

Size

Document Number

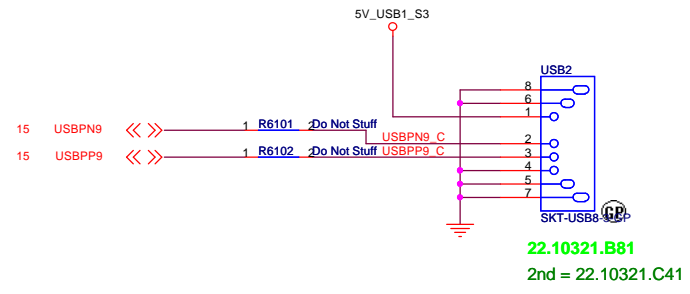
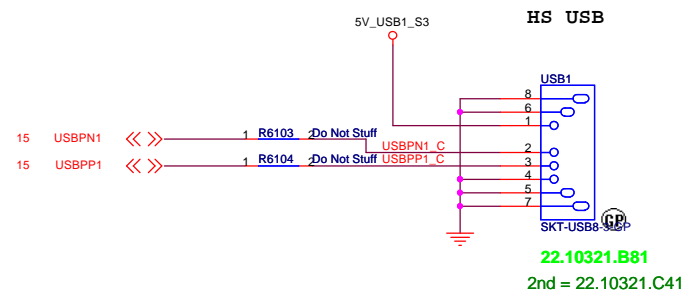
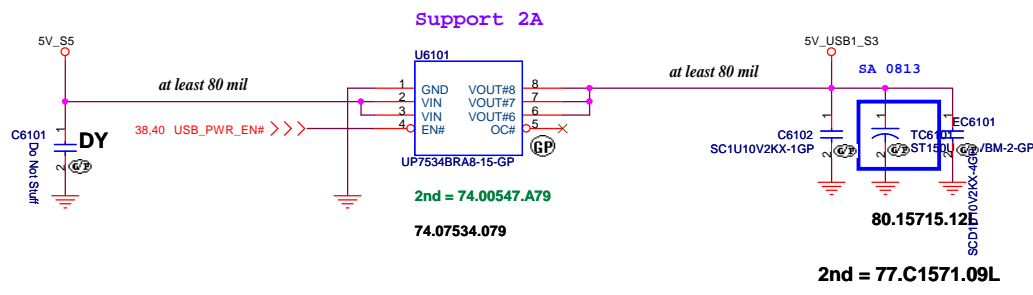
JE43-CP

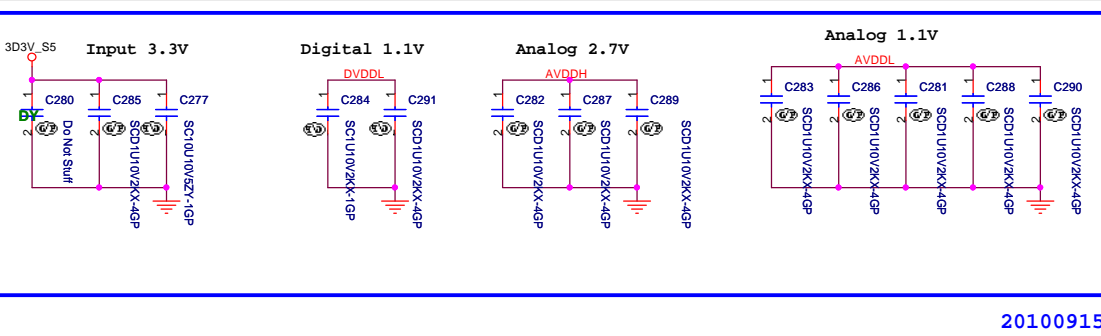
Rev

-1

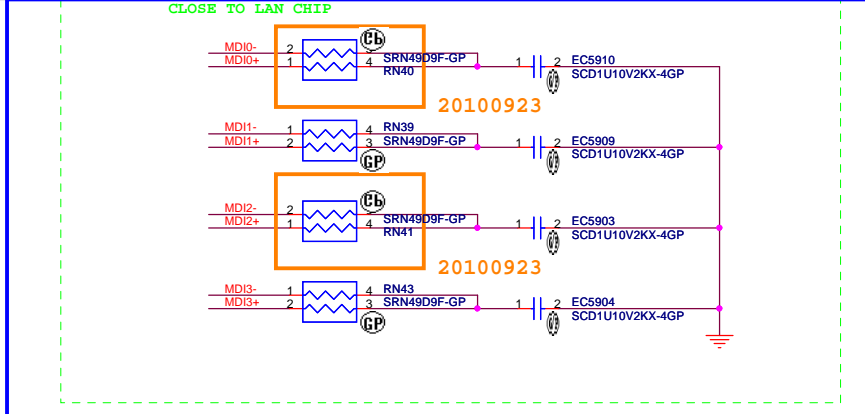
Date: Wednesday, November 24, 2010

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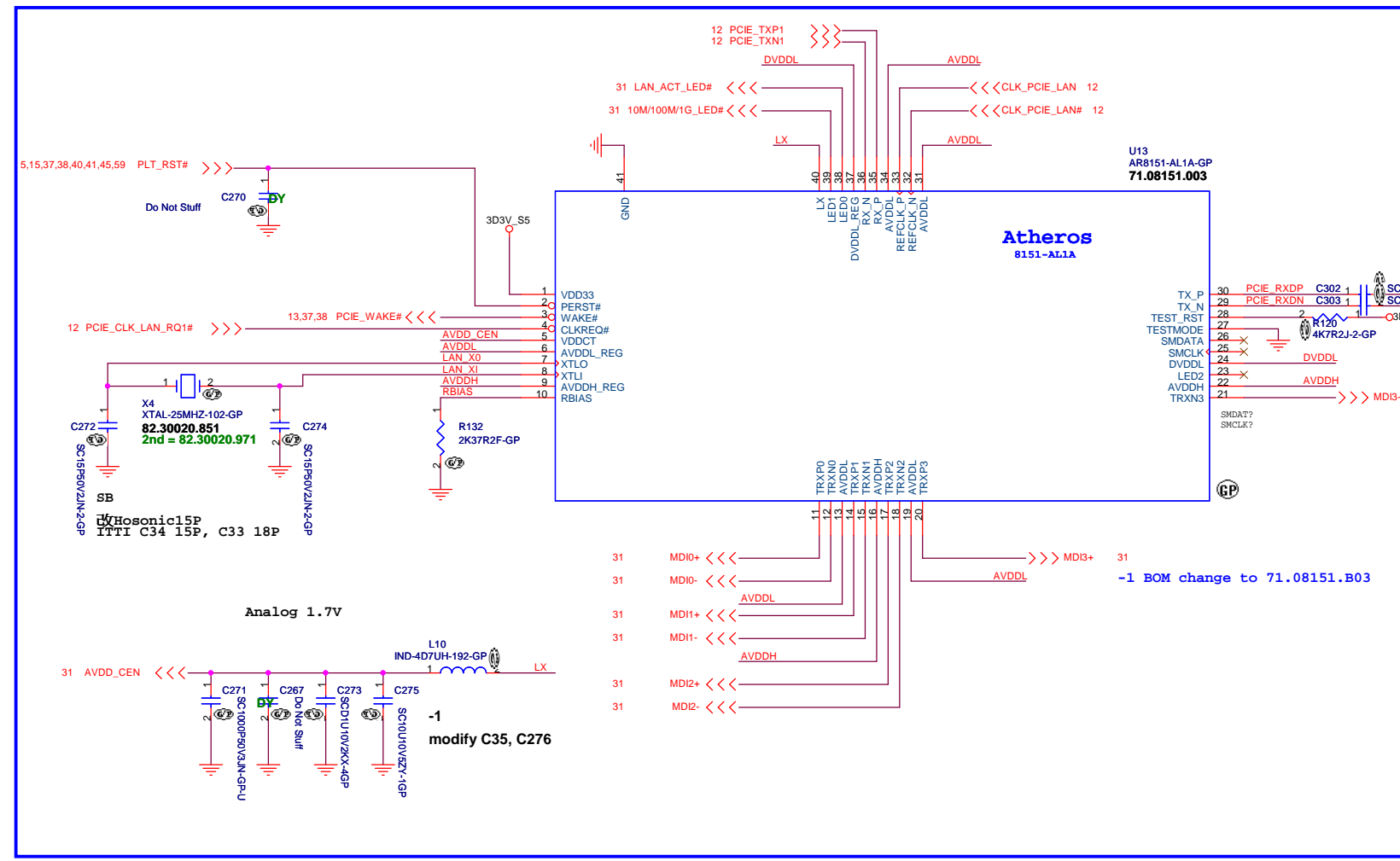




20100915



20100915



20100915

WWW.AliSaler.Com

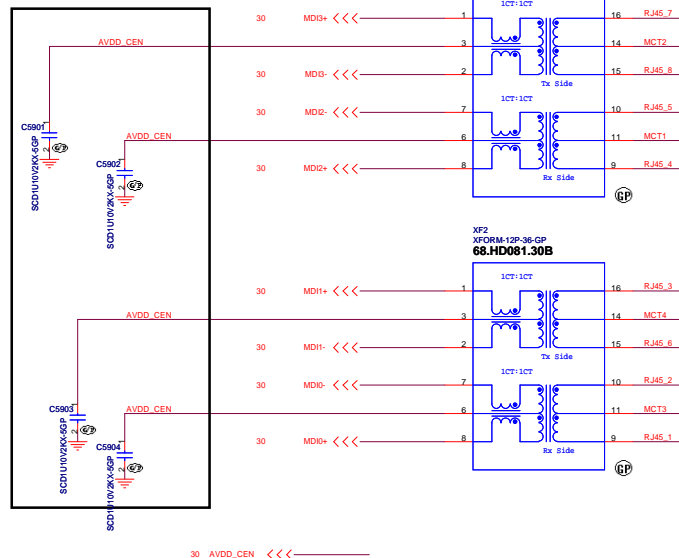
Hynix 1G 800M N11PGV SKU

Title		AR8151 chip	
Size	Document Number	Rev	
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Date:	Wednesday, November 24, 2010	Sheet	30 of 69

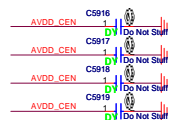
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

GIGA Lan Transformer

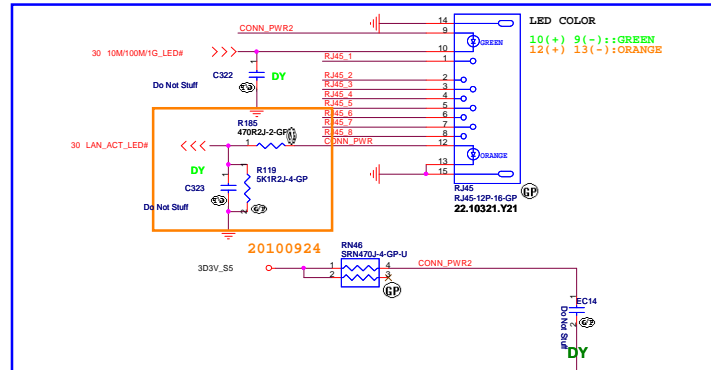
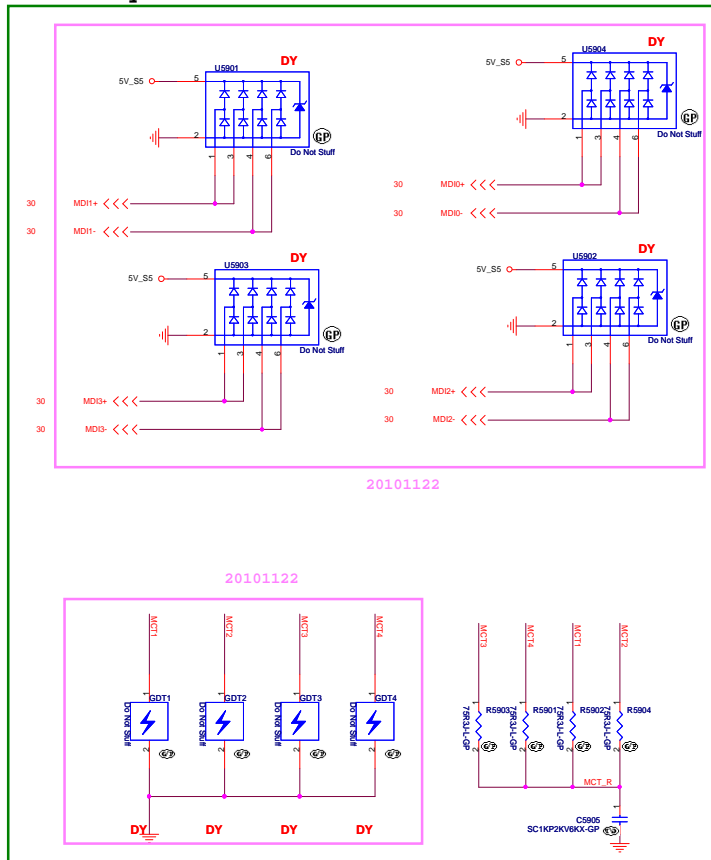
SSID = LOM



20100915



SB modify For EMI



20100915

Hynix 1G 800M N11PGV SKU

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LAN CONN		
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	A	B	C	D	E
4					
3					
2					
1					

Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			

Size	Document Number		Rev
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Hynix 1G 800M N11PGV SKU

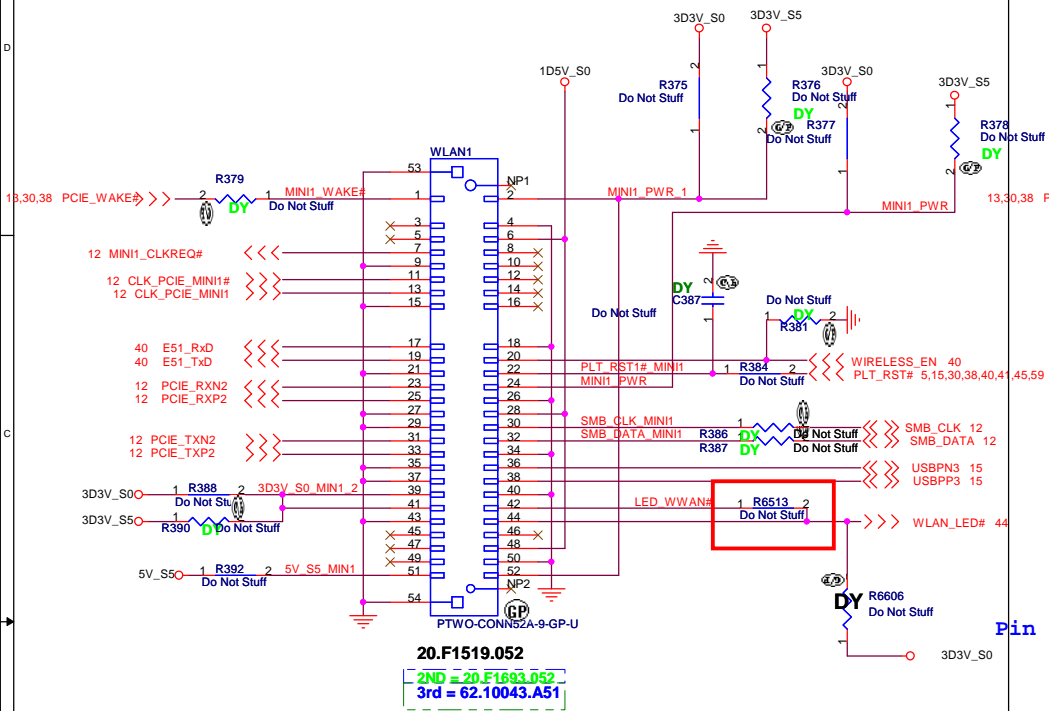
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title *****			
Size	Document Number		Rev
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5	4	3	2	1
D				
C				
B				
A				

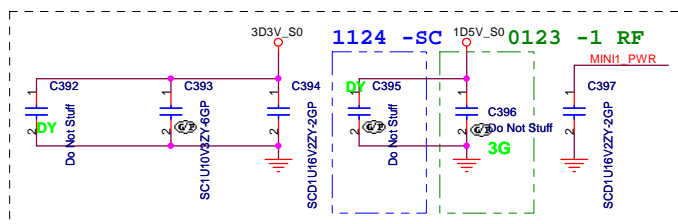
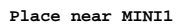
Hynix 1G 800M N11PGV SKU

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RTS5138 (CARD READER)			
Size	Document Number		Rev
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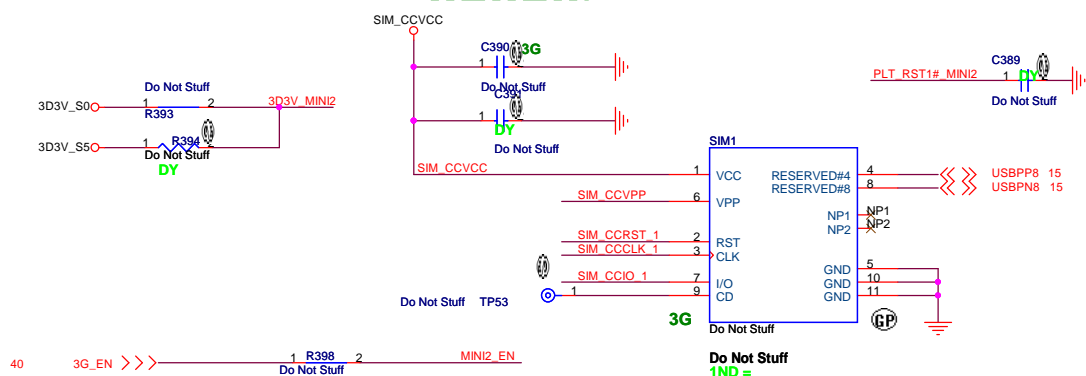
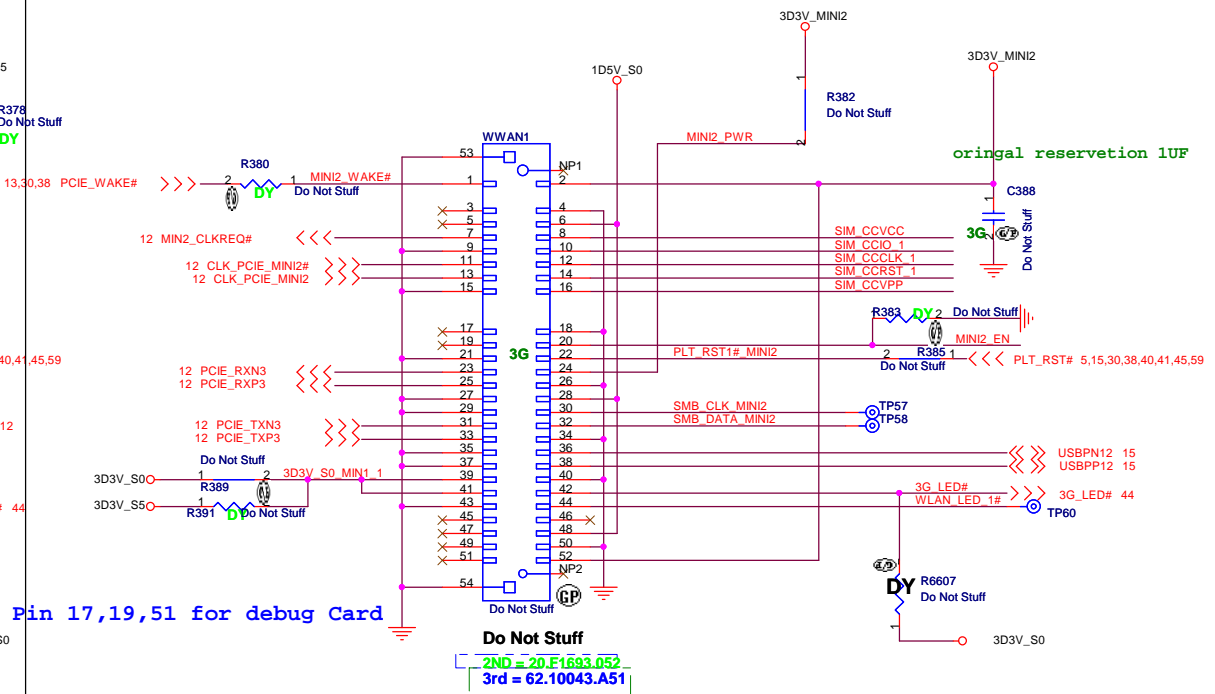
Mini Card Connector(WLAN)



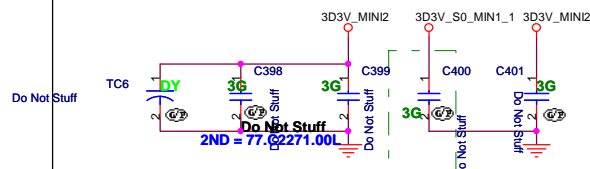
Pin 17,19,51 for debug Card



Mini Card Connector(Robson2 and 3G)



original reservation 10UF

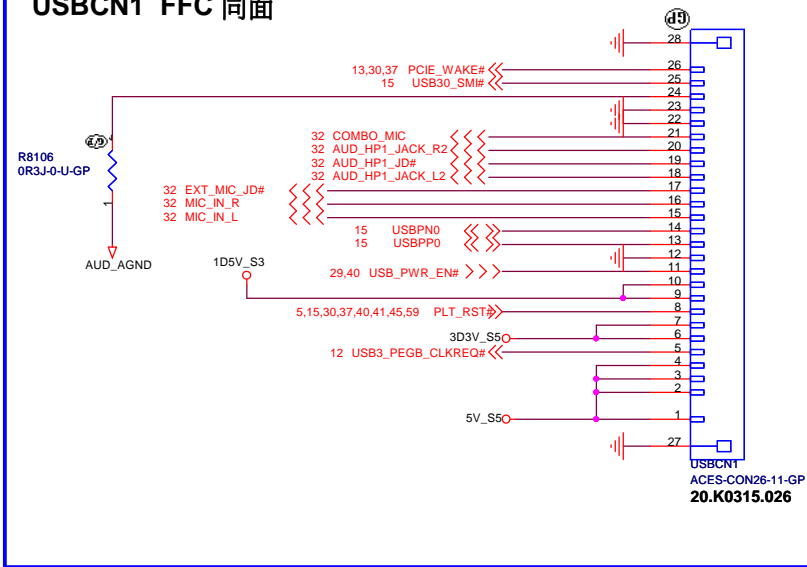


Hynix 1G 800M N11PGV SKU

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

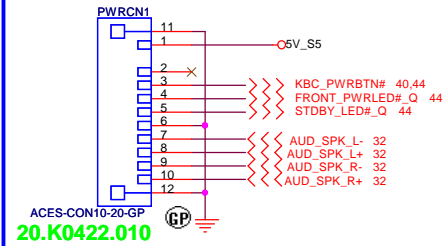
Title			
MINI CARD			
Size A3	Document Number		Rev
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USBCN1 FFC 同面

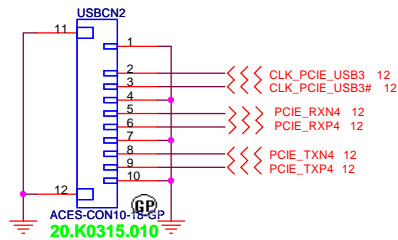


20100915

PWRCN1 FFC 異面



USBCN2 FFC 同面

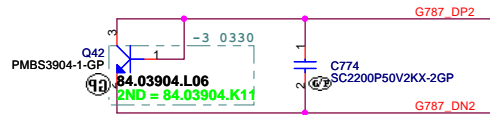


Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

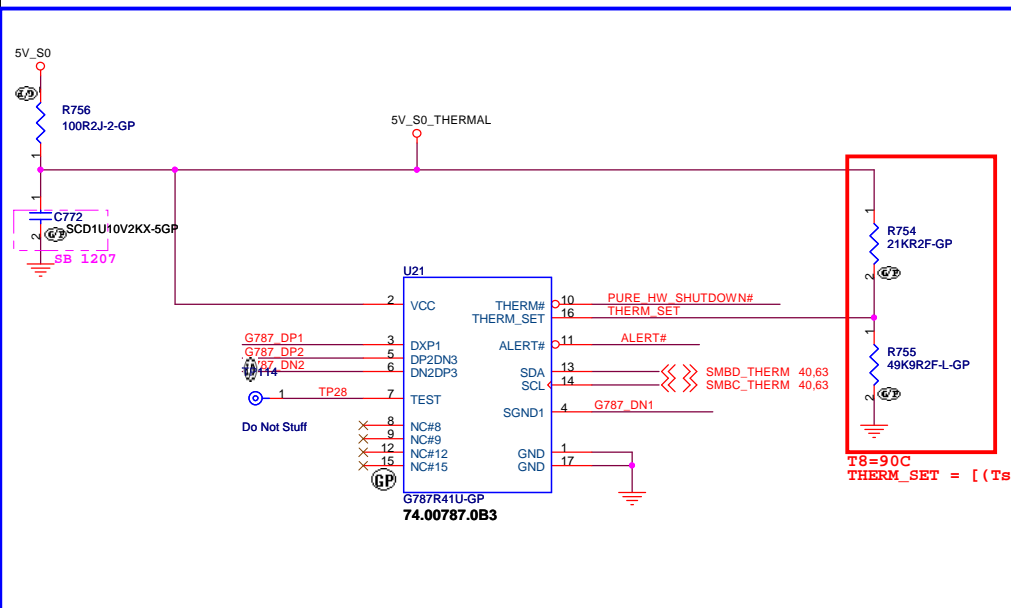
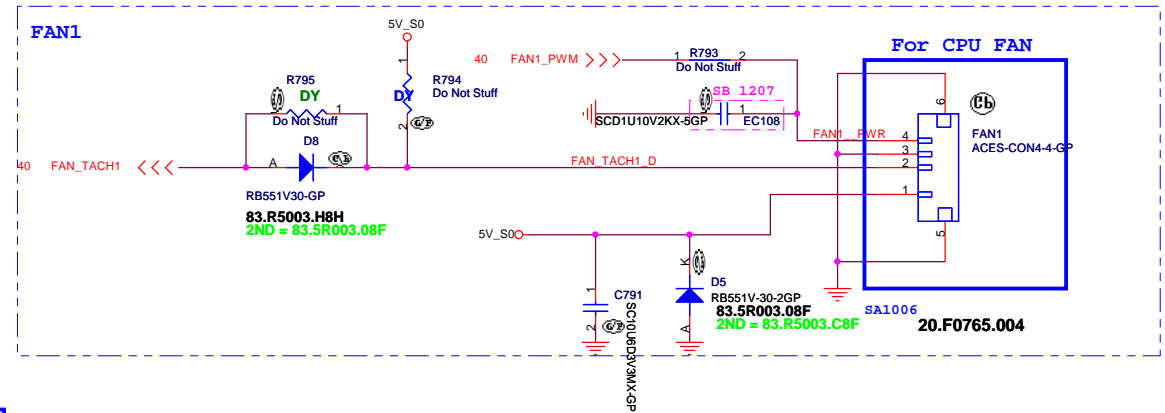
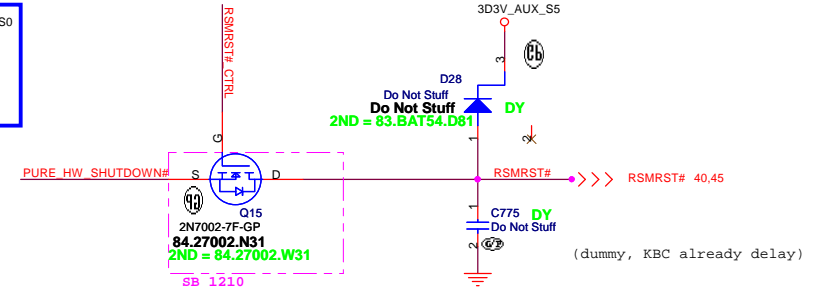
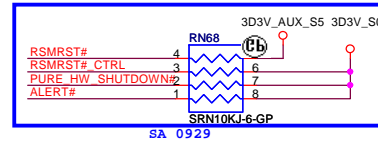
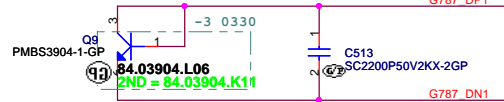
Title		
I/O Board		
Size A3	Document Number JE43-CP	Rev -1
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for T8 thermal diode



C82 & C561 CLOSE TO G787

for system thermal diode



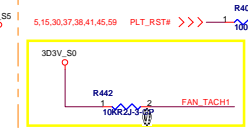
$$T8=90^{\circ}\text{C}$$

$$\text{THERM_SET} = [(T_{\text{set}}-72) \times 0.02+0.34] \times \text{VCC}$$

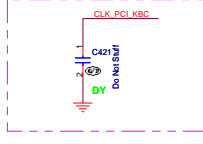
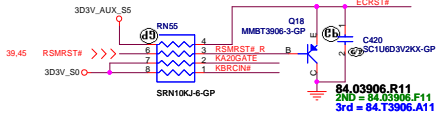
Hynix 1G 800M N11PGV SKU

Prevent BIOS data loss solution
1019 -SB

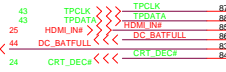
83.00054.TB1
2ND = 83.BAT54.D81
3rd = 83.00054.S81



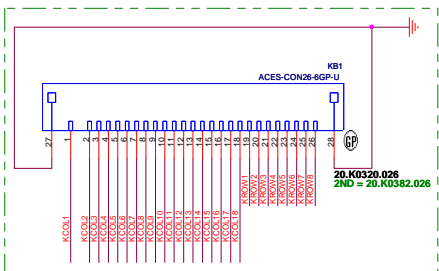
20101027



0806 SA STOP_CHG#拉至Pin83

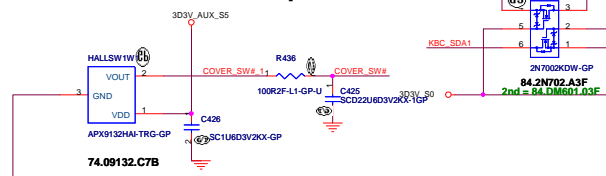


Internal Keyboard Connector



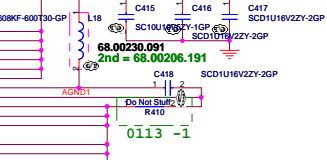
0105 -1

Cover Up Switch

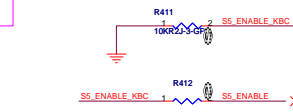


L16 -> 68.00082.011 is an obsoleted part
0930 -SA

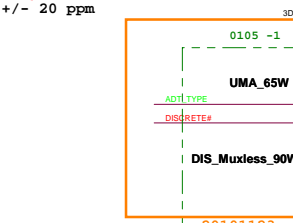
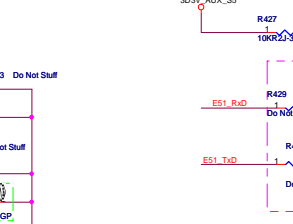
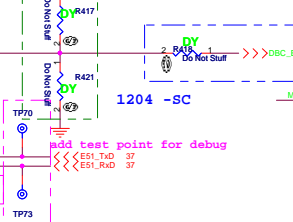
Impedance: 60-ohm
rated Current :3A



BATTERY
THERMAL



Model ID
14* PH 10K 3.3V_AUX_S5
17* PL 10K GND



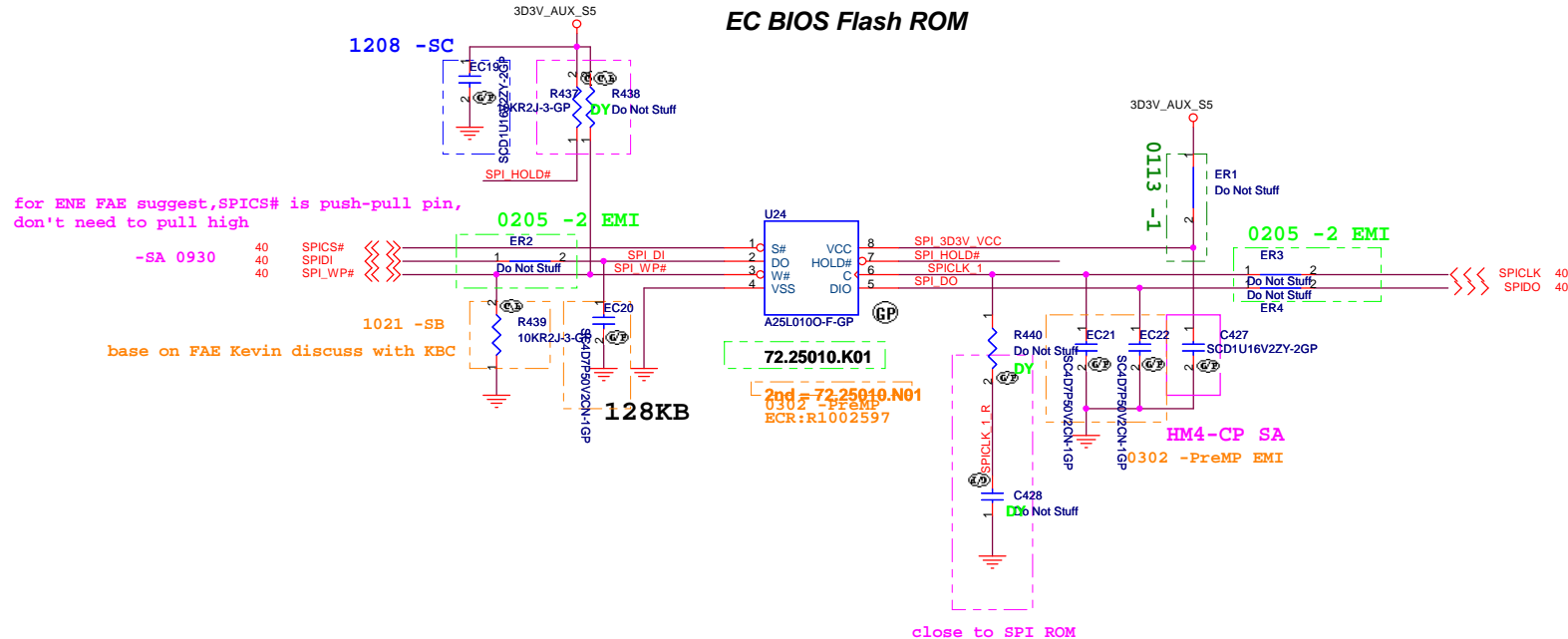
PCB Version AD (PinB)	Full-Low Resistor	Full-High Resistor (20V, 0.5)	Voltage
SA	100 K	10 K	3.0 V
SB	100 K	10 K	2.75 V
SC	100 K	10 K	2.5 V
SD	100 K	10 K	2.2 V
SE	100 K	10 K	1.9 V
SF	100 K	10 K	1.6 V
SG	100 K	10 K	1.3 V
SH	100 K	10 K	1.0 V
SI	100 K	10 K	0.7 V
SJ	100 K	10 K	0.4 V
SK	100 K	10 K	0.1 V

Value	PN
20K	64.20025.6DL
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

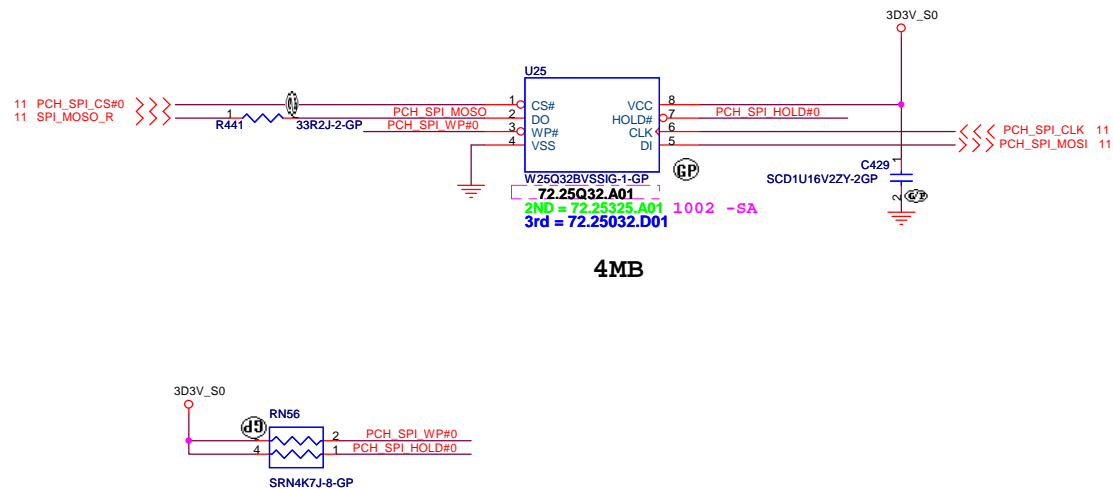
Hylix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan 305, R.O.C.

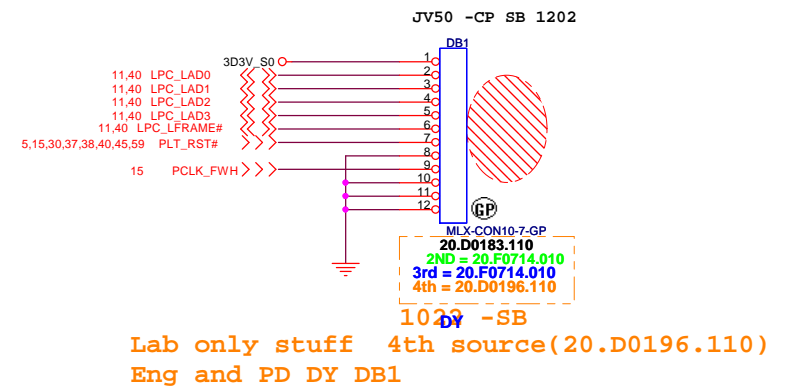
File: KBC KB3930
Size: Document Number: JE43-CP
Date: Wednesday, November 24, 2010 Sheet: 40 of 69



System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD



Hynix 1G 800M N11PGV SKU

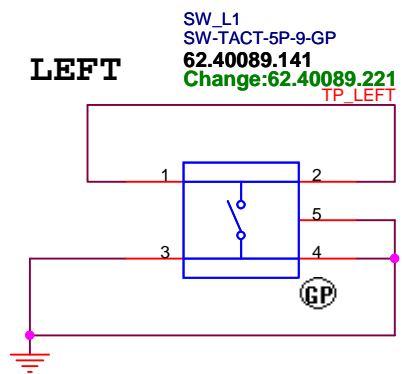
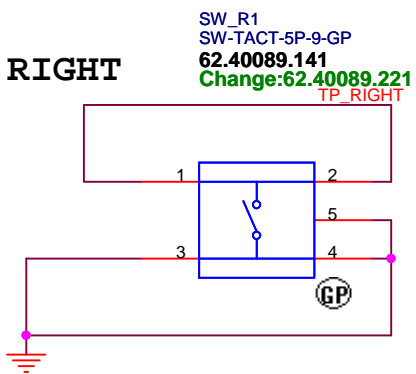
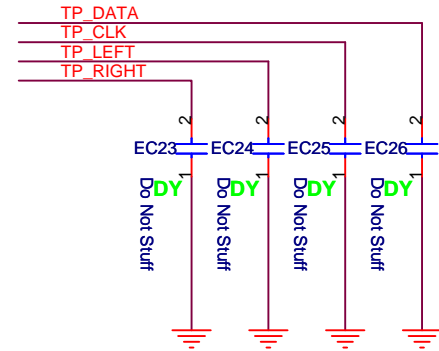
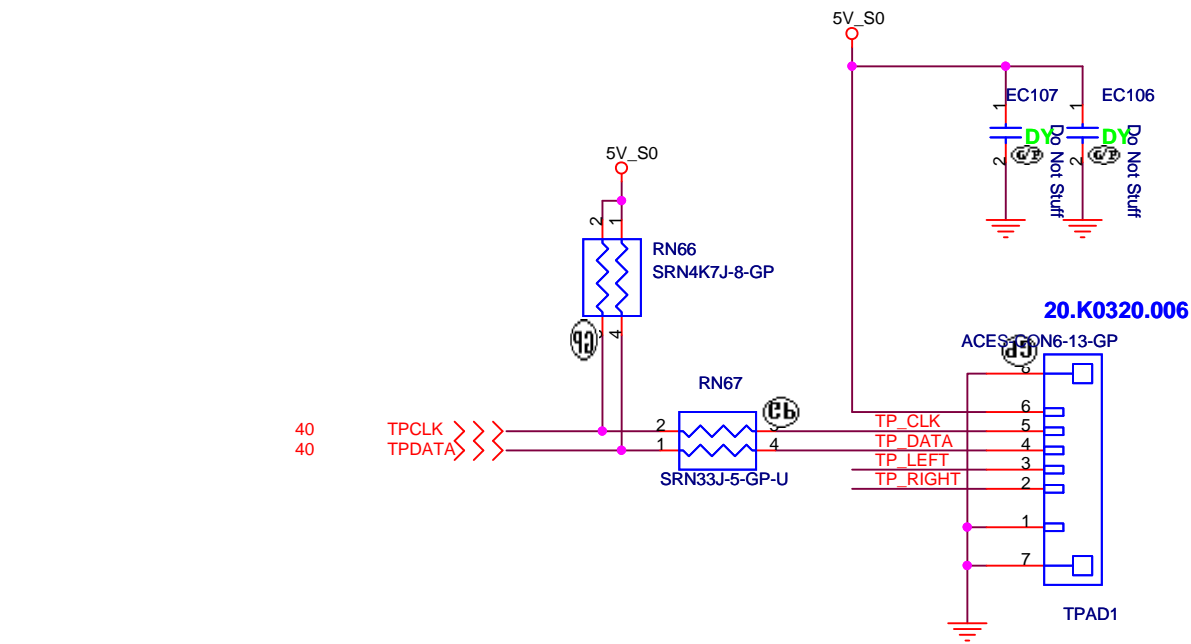
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		BIOS
Size	Document Number	JE43-CP
Date: Wednesday, November 24, 2010	Sheet 41 of 69	Rev -1

Hynix 1G 800M N11PGV SKU

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			

Size	Document Number		Rev
A3	JE43-CP		-1
Date: Wednesday, November 24, 2010		Sheet 42 of	69

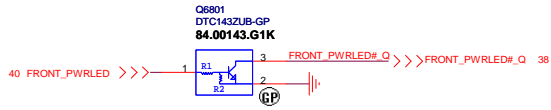


Hynix 1G 800M N11PGV SKU

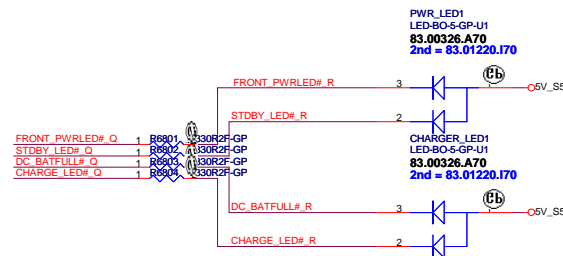
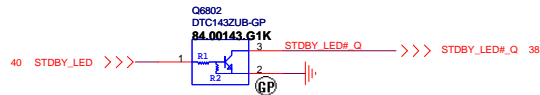
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Touch PAD FP CONN		
Size	Document Number	Rev
	JE43-CP	-1
Date: Wednesday, November 24, 2010		
2	Sheet 43 of 69	1

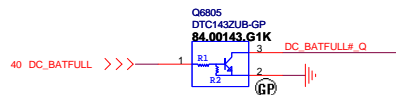
Power button LED



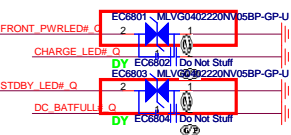
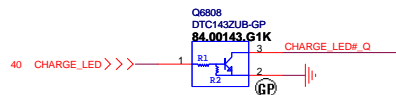
Power STDBY_LED



Battery LED2(DC_BATFULL)

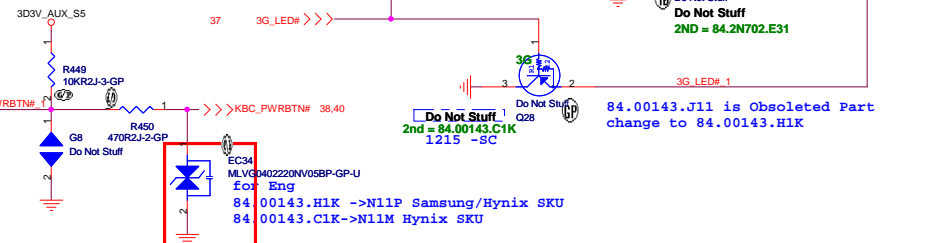
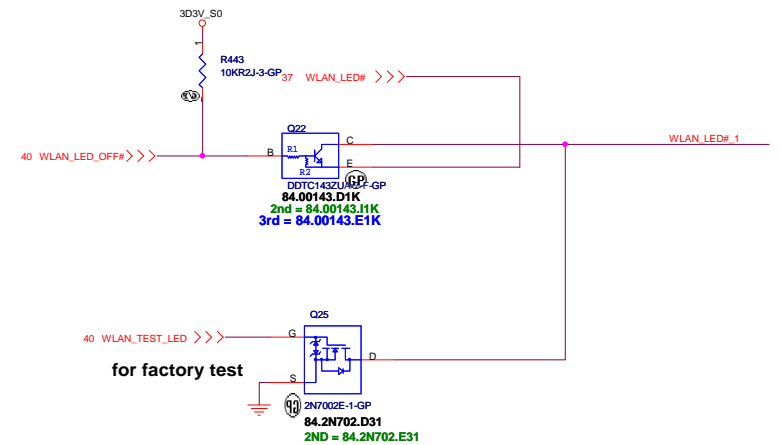


Battery LED1(CHARGE)

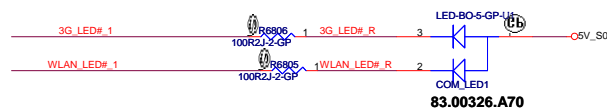


EC6801, EC6803, EC34 請幫忙上件 22p 5.5V 的 Varistor料號是 69.80024.011

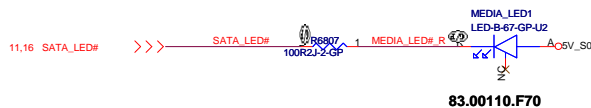
For 2010 Acer Project, WLAN and 3G LED control by KBC



Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net



SATA HDD LED



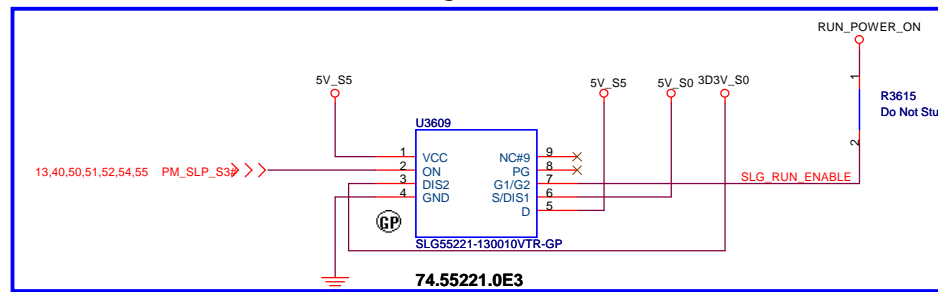
Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

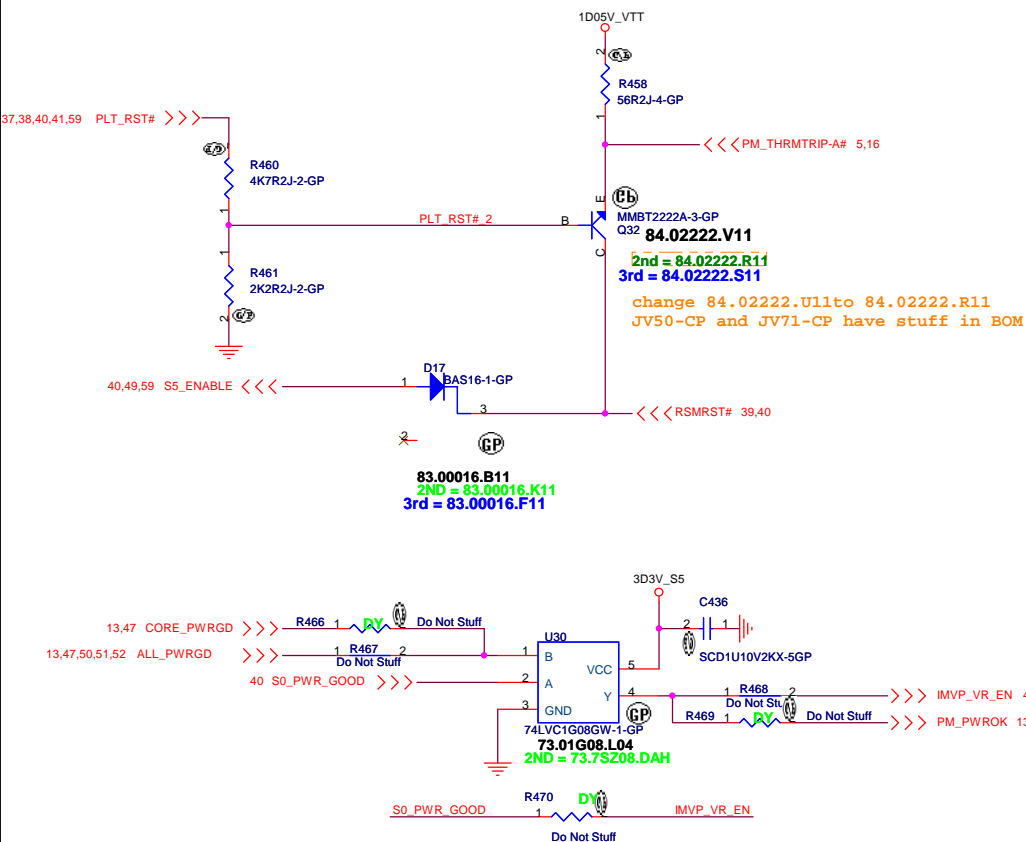
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichang, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
LED&POWERBD CONN	
Size	Document Number
JE43-CP	
Date: Wednesday, November 24, 2010	Sheet 44 of 68

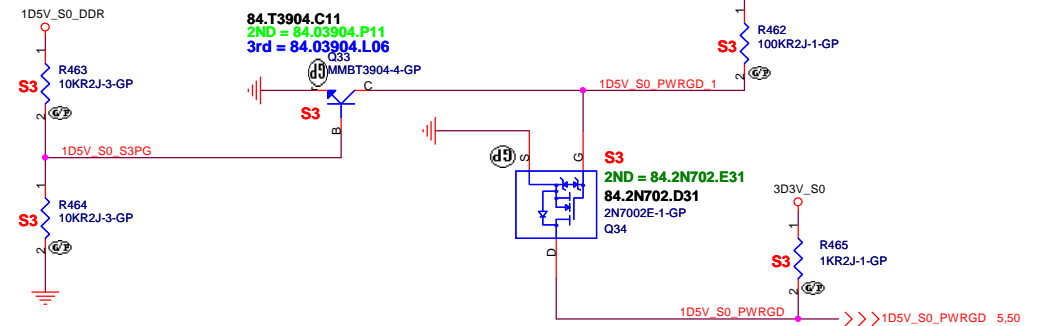
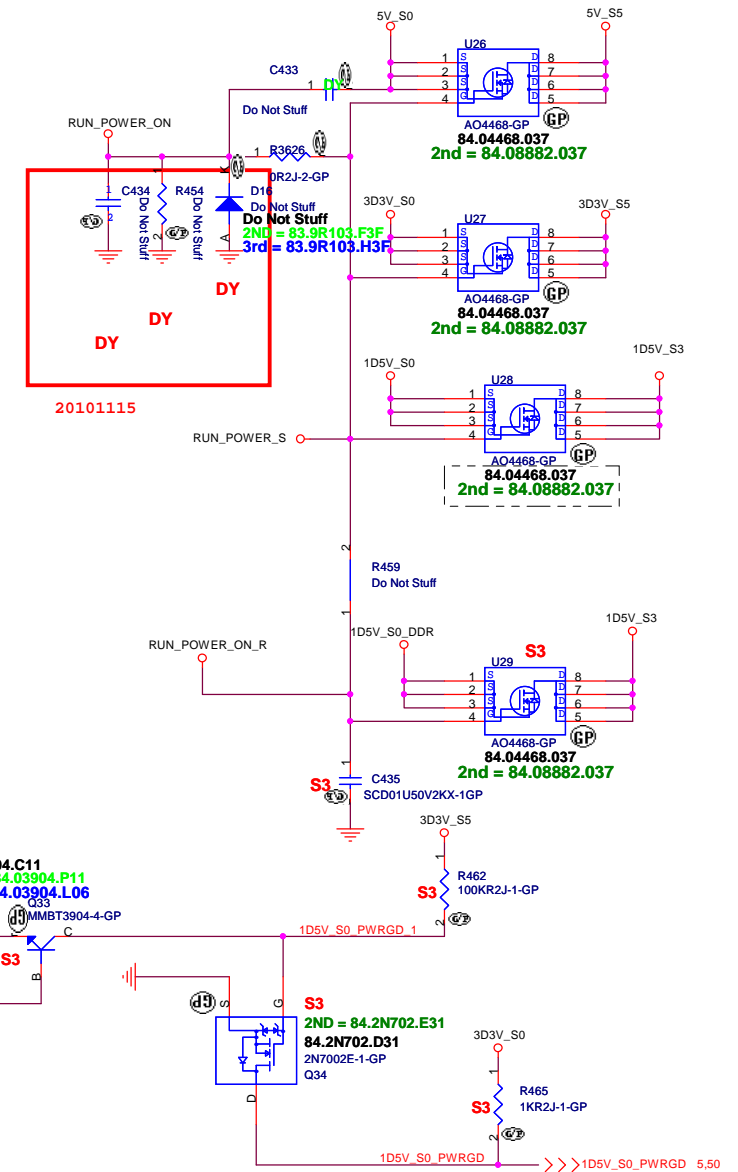


3D3V_AUX_S5

*Del Aux Power schematic,
it is not necessary for reservation*



Run Power



Hynix 1G 800M N11PGV SKU

PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

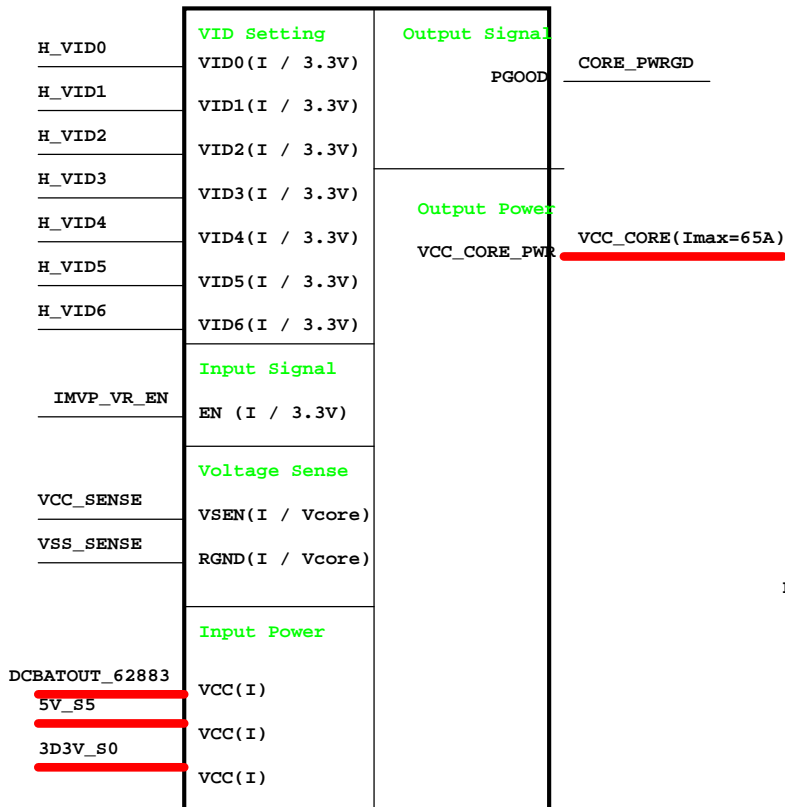
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V AUX S5**

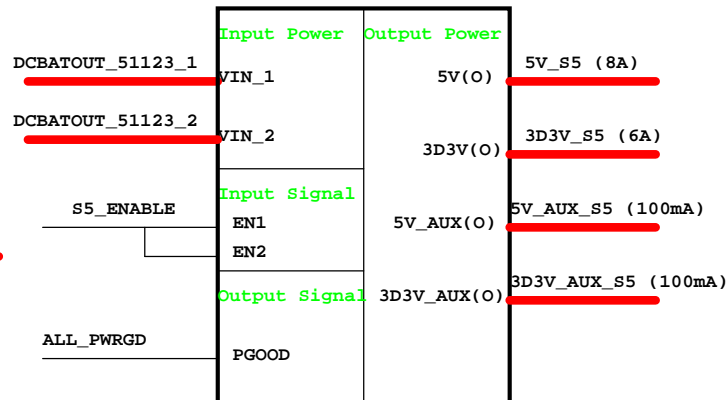
Size: Document Number **JE43-CP** Rev **-1**

Date: Wednesday, November 24, 2010 Sheet 45 of 69

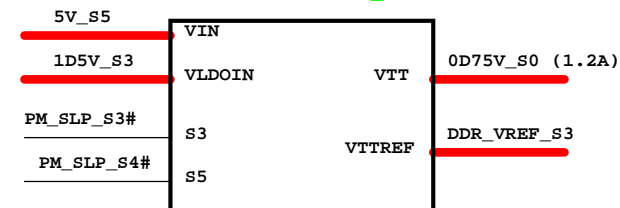
ISL62883 VCC_CORE



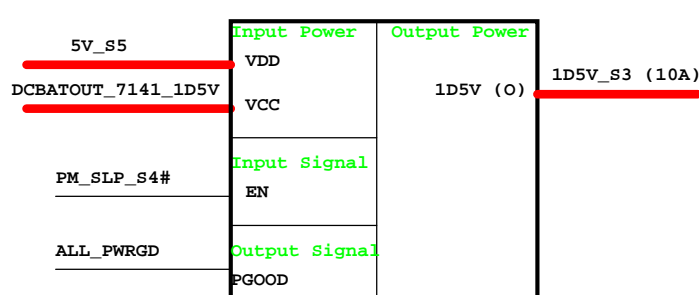
TPS51123 5V/3D3V



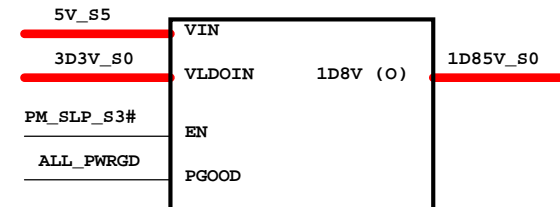
RT9026 0D75V_S0



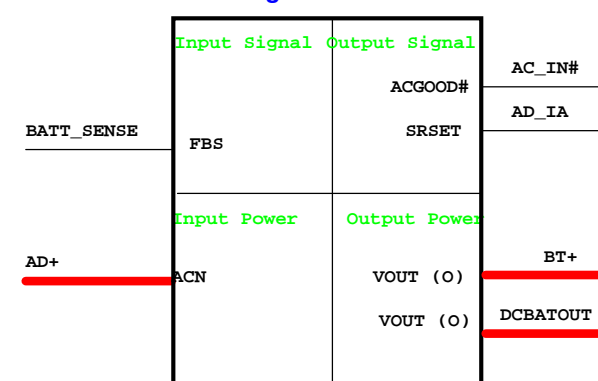
RT9025 1D5V



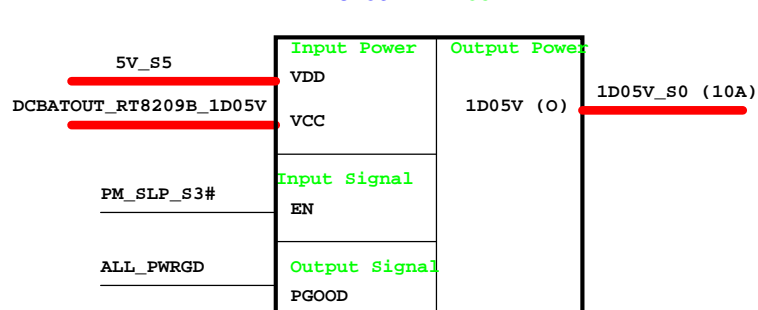
RT9025 1D8V



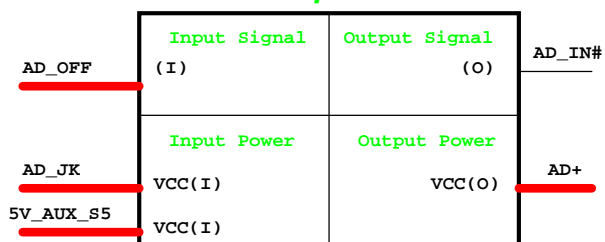
Charger BQ24745



RT8209B 1D05V



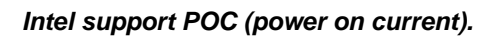
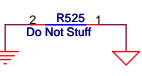
Adapter



Hynix 1G 800M N11PGV SKU

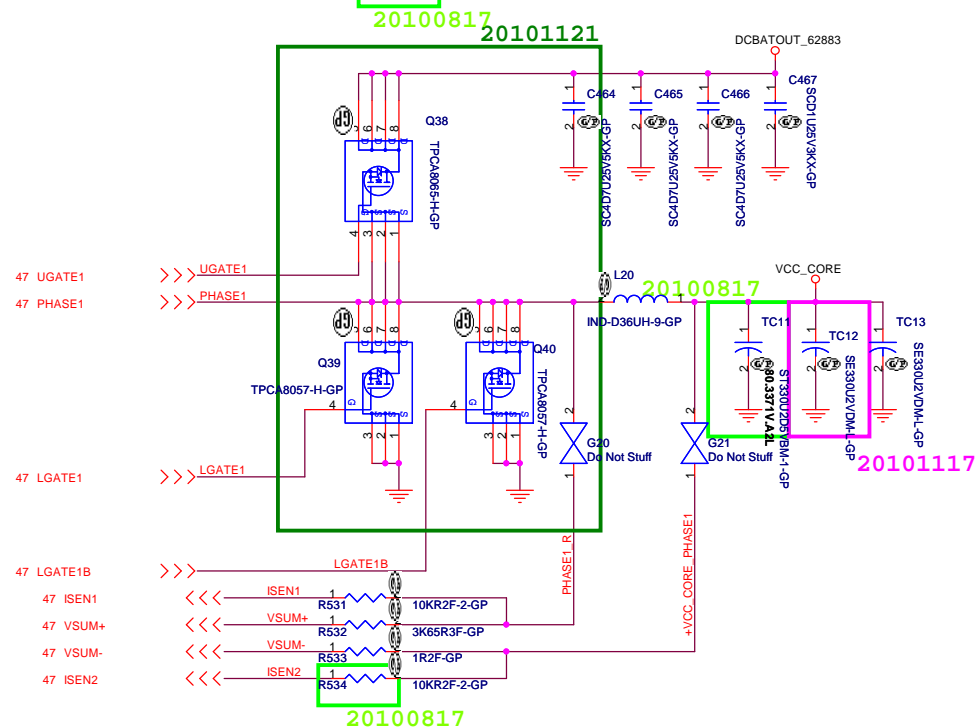
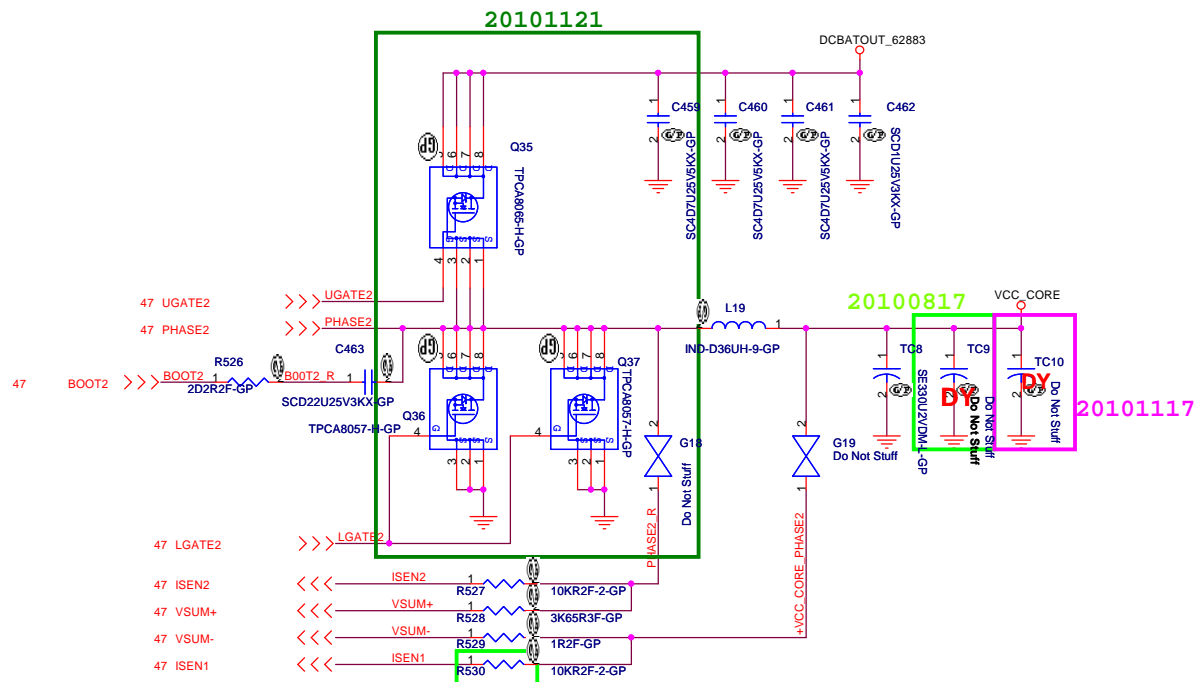
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**
Size: Document Number: **JE43-CP** Rev: **-1**
Date: Wednesday, November 24, 2010 Sheet: 46 of 69



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Title			
ISL62882 CPU CORE (1/2)			
Size	Document Number		Rev
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Date:	Wednesday, November 24, 2010	Sheet 47 of	69

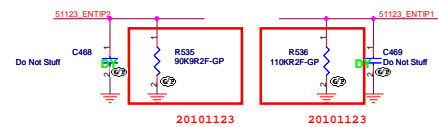
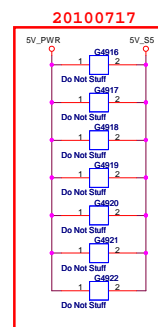
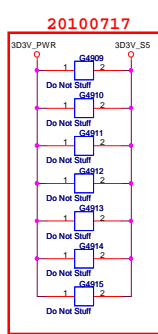
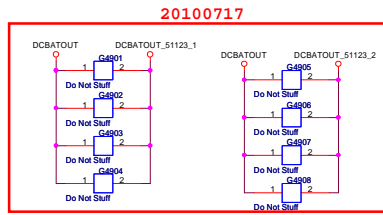


Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		ISL62882 CPU CORE (2 / 2)	
Size	Document Number	JE43-CP	
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Rev
-1

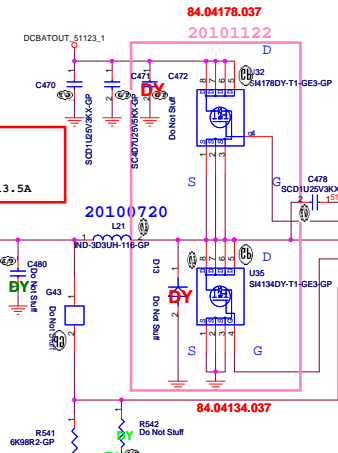


20100717
68.3R31A.10V
Mag, 6.86*6.74*3
IND-3D30H
DCR=28-30mohm
Irating=6A, Isat=13.5A

Iomax=5A
OCP>7.5A

20100717
68.3R31A.10V
Mag, 6.86*6.74*3
IND-3D30H
DCR=28-30mohm
Irating=6A, Isat=13.5A

Iomax=6A
OCP>9A



20100720

20100720

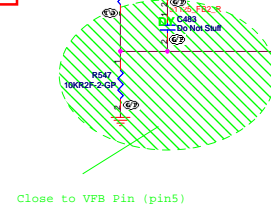
20101122

20101122

20100726

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79.22710.3EL
LIELON
SE220U, 6.3V
ESR:<14mohm, Iripple:3.16A

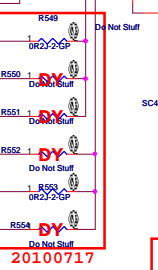
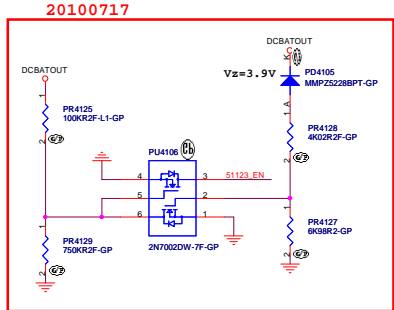
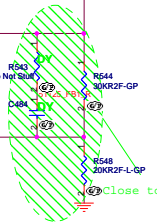
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79.22710.3EL
LIELON
SE220U, 6.3V
ESR:<14mohm, Iripple:3.16A



84.04134.037

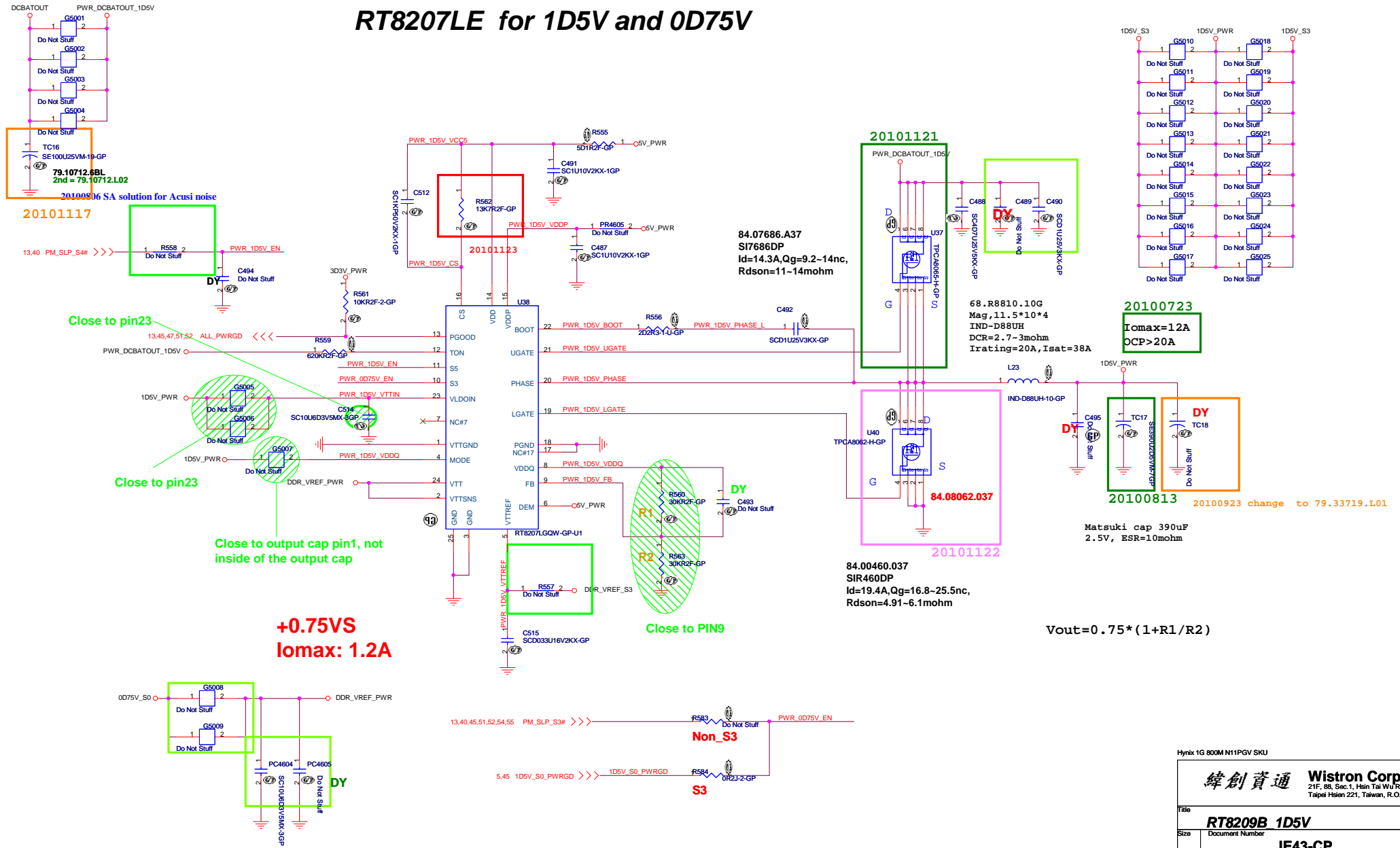
84.04134.037

84.04134.037



20100717
Vout=2*(1+R1/R2)

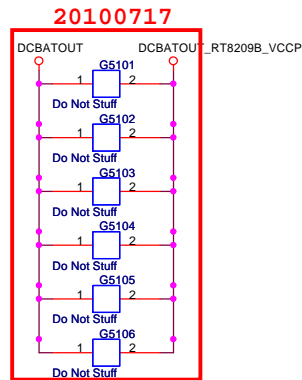
	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

RT8207LE for 1D5V and 0D75V

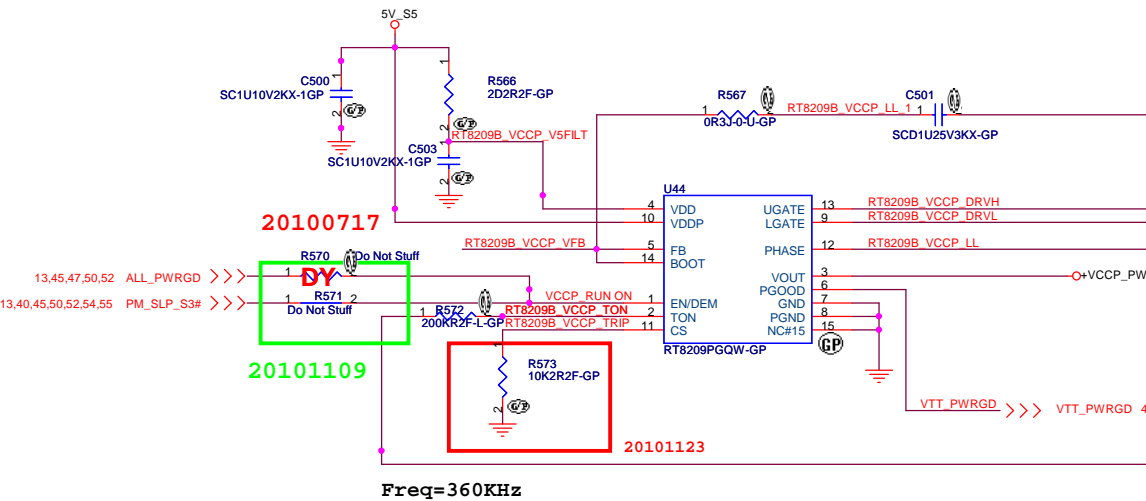
Hynix 1G 800M N11PGV SKU

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Taipei Hsien 221, Taiwan, R.O.C.

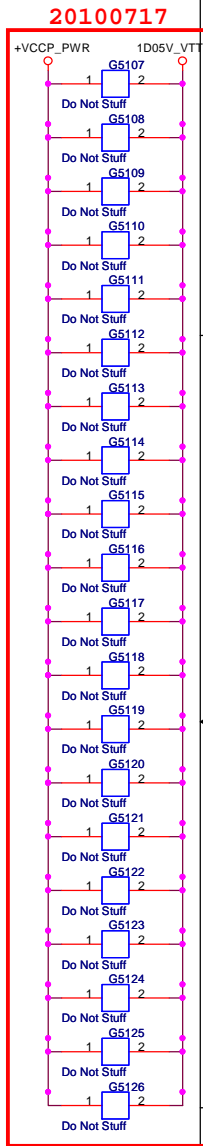
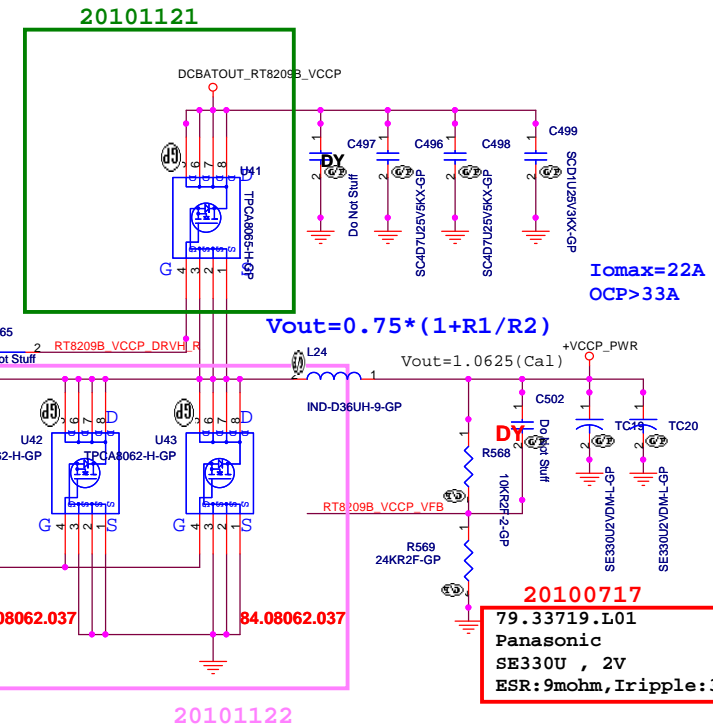
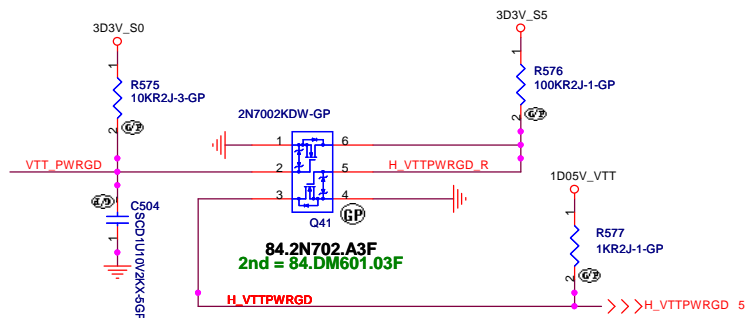
Title			
RT8209B 1D5V			
Size	Document Number		Rev
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Date:	Wednesday, November 24, 2010	Sheet 50 of	69



RT8209E for VCCP



because of 1.05V_S0 and 1.05V_VTT combin together
use PM_SLP_S3# Enable 1.05V power



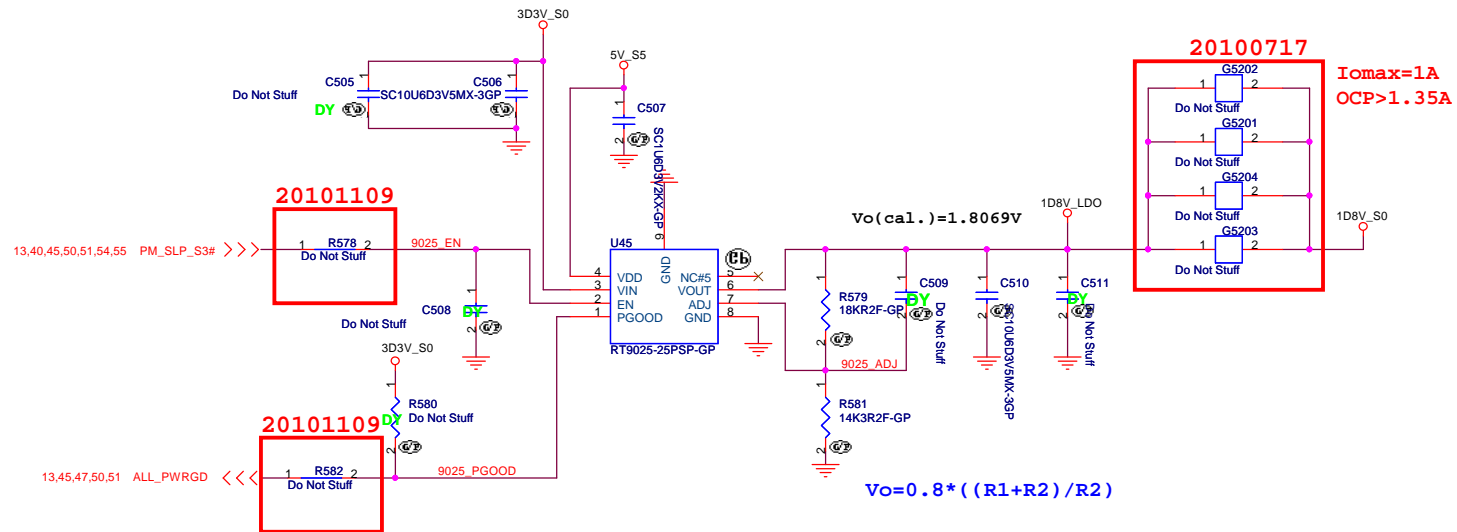
Hynix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File		
Size	Document Number	Rev
	RT8209B +VCCP	
	JE43-CP	-1
Date: Wednesday, November 24, 2010	Sheet 51 of 69	

RT9025 for 1D8V_S0

20090915

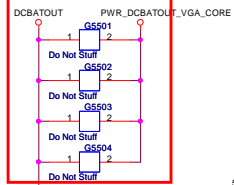


Hynix 1G 800M N11PGV SKU

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		RT9025 1D8V/RT9026 0D75	
Size	Document Number	JE43-CP	Rev -1
Date: Wednesday, November 24, 2010		Sheet 52	of 69

20100717



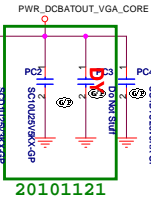
SSID = PWR.Plane.Regulator_GFX

N12P-GV and N11P-GV, PR6換成9.1K
(part number: 64.91015.6DL), MOSFET 請用TPCA8065-H

+TPCA8062-Hx2 上一下二

20100813

20101121

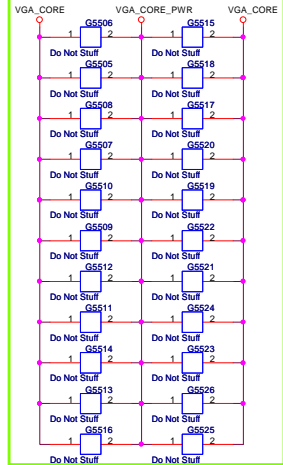


$$V_{out} = 0.75V * (R1 + R2) / R2$$

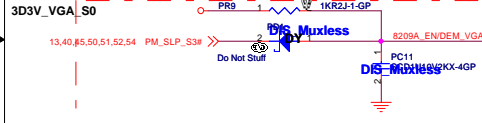
84.07686.A37
CYNTEC, 11.5*10*4
IND-D36UH
DCR=1.05mohm
Irating=30A, Isat=60A

Design Current = 21.94A
24.14A < OCP < 28.53A

20100813



RT8208B



N11P-GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8, P12	L	L	0.85V
P0 - HOT	L	H	0.90V
P0 - COLD	H	L	0.95V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V BEPSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mOhm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

N12P_GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8, P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.05V
	H	H	

N12P_GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8, P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.02V
	H	H	

N12P GS: PR11=10K, PR14=100K, PR13=49.9K, PR15=33.2K

N12P GV: PR11=10K, PR14=75K, PR13=49.9K, PR15=43K

N11P GV: PR11=10K, PR14=75K, PR13=150K, PR15=75K

33.2K=64.33225.6DL
43K=64.43025.6DL
75K=64.75025.6DL
100K=64.10035.6DL
150K=64.15035.6DL

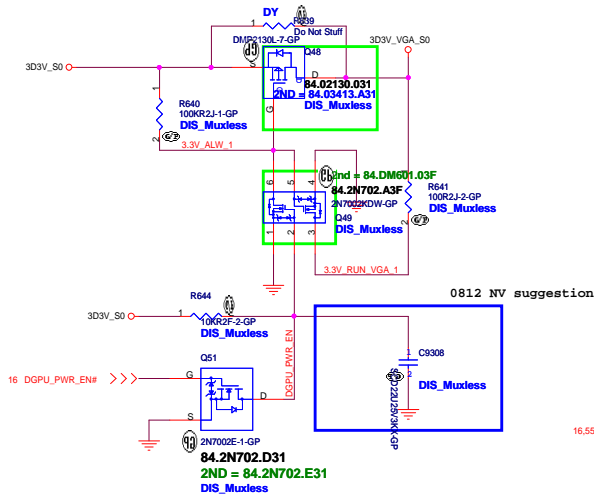
Hylix 1G 800M N11PGV SKU

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

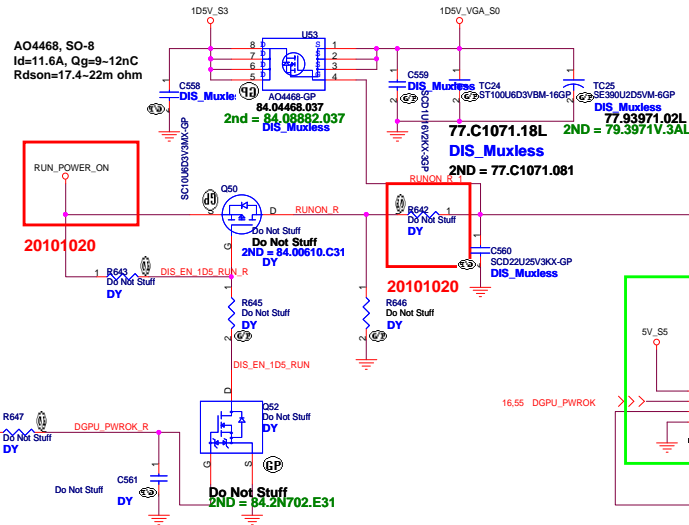
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Size	Document Number	Rev	-1
Custom	JE43-CP		
Date:	Wednesday, November 24, 2010	Sheet	55 of 69

+3VS to 3.3V_DELAY Transfer

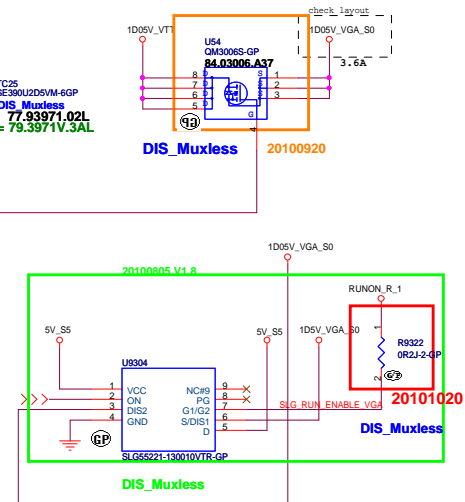
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

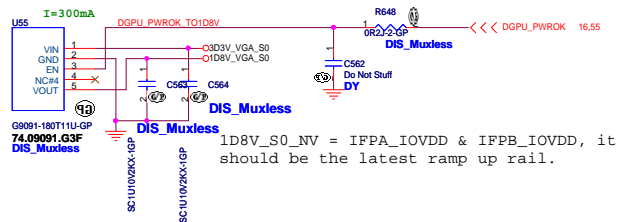


1.05V to 1.05V_VGA_S0 Transfer



RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer

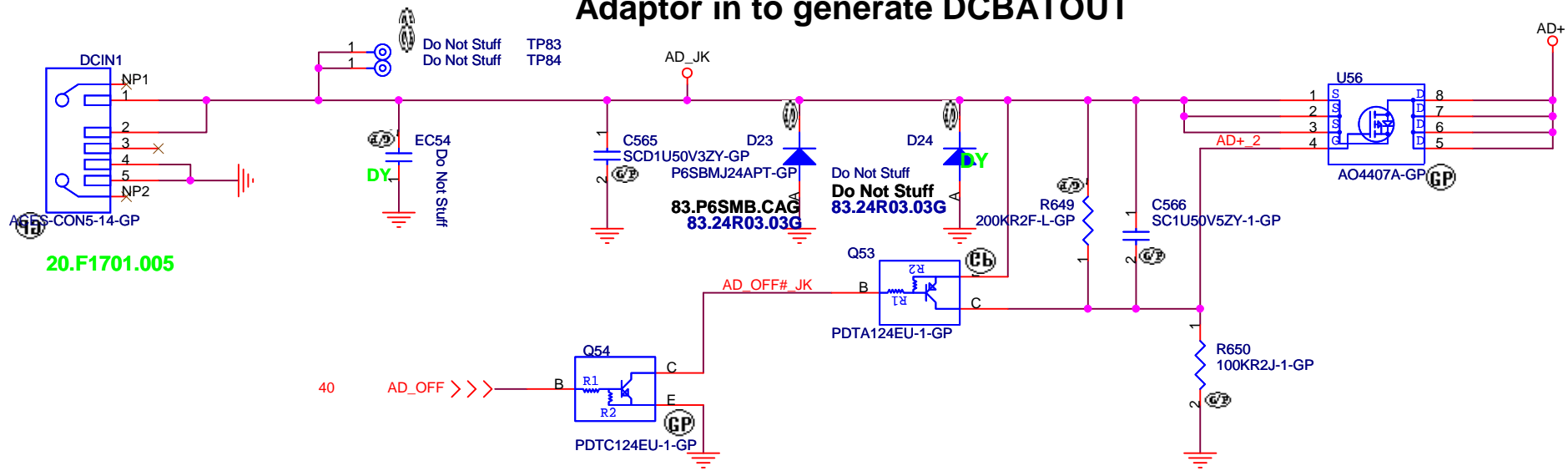


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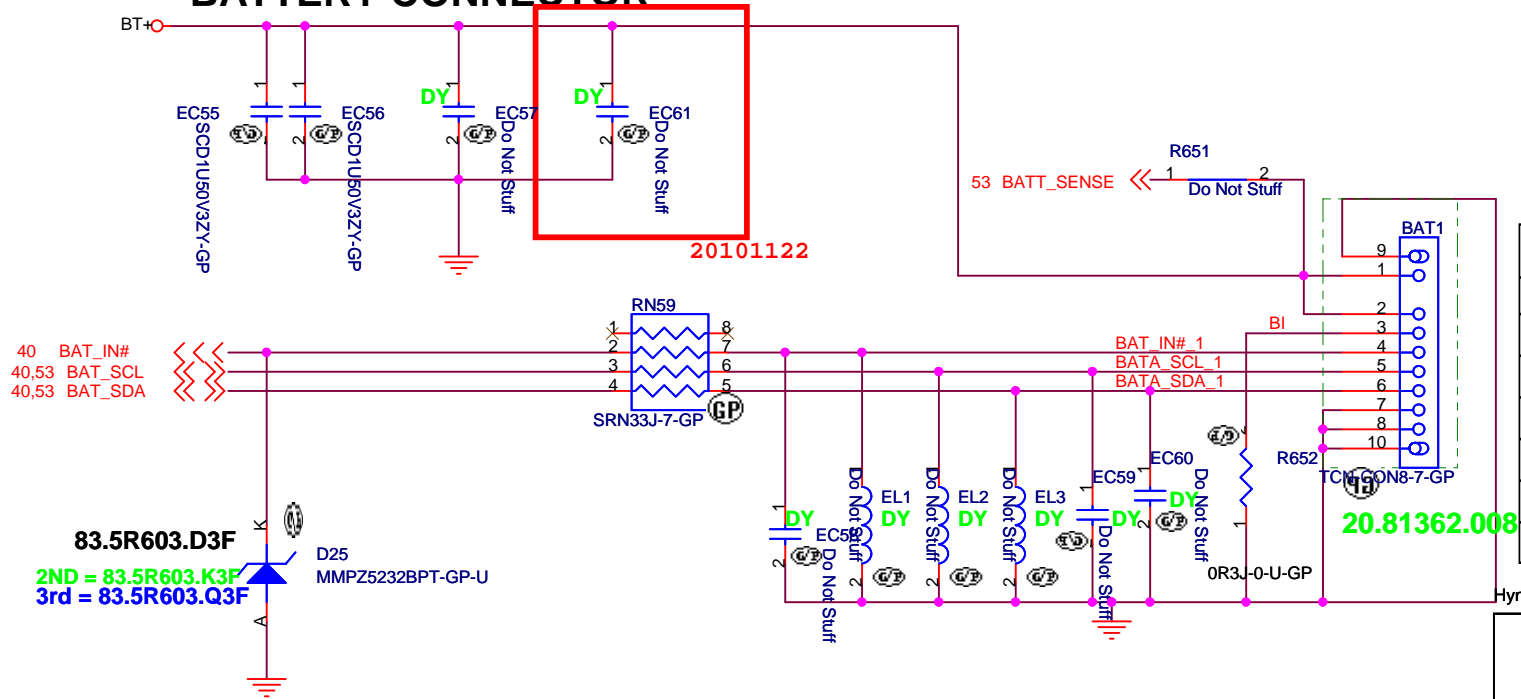
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DISCRETE VGA POWER			
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



- Pin Definition: +

1 ^o	GND ^o	Batt-, Battery Negative Terminal ^o
2 ^o	GND ^o	Batt-, Battery Negative Terminal ^o
3 ^o	SMD ^o	SMBus data interface I/O pin ^o
4 ^o	SMC ^o	SMBus clock interface I/O pin ^o
5 ^o	TH ^o	Connect to Resistor to GND (10kΩ to GND) ^o
6 ^o	BI ^o	System present pin, low active ^o
7 ^o	BATT+ ^o	Batt+, Battery Positive Terminal ^o
8 ^o	BATT+ ^o	Batt+, Battery Positive Terminal ^o

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AD/BATT CONN

Size	Document Number
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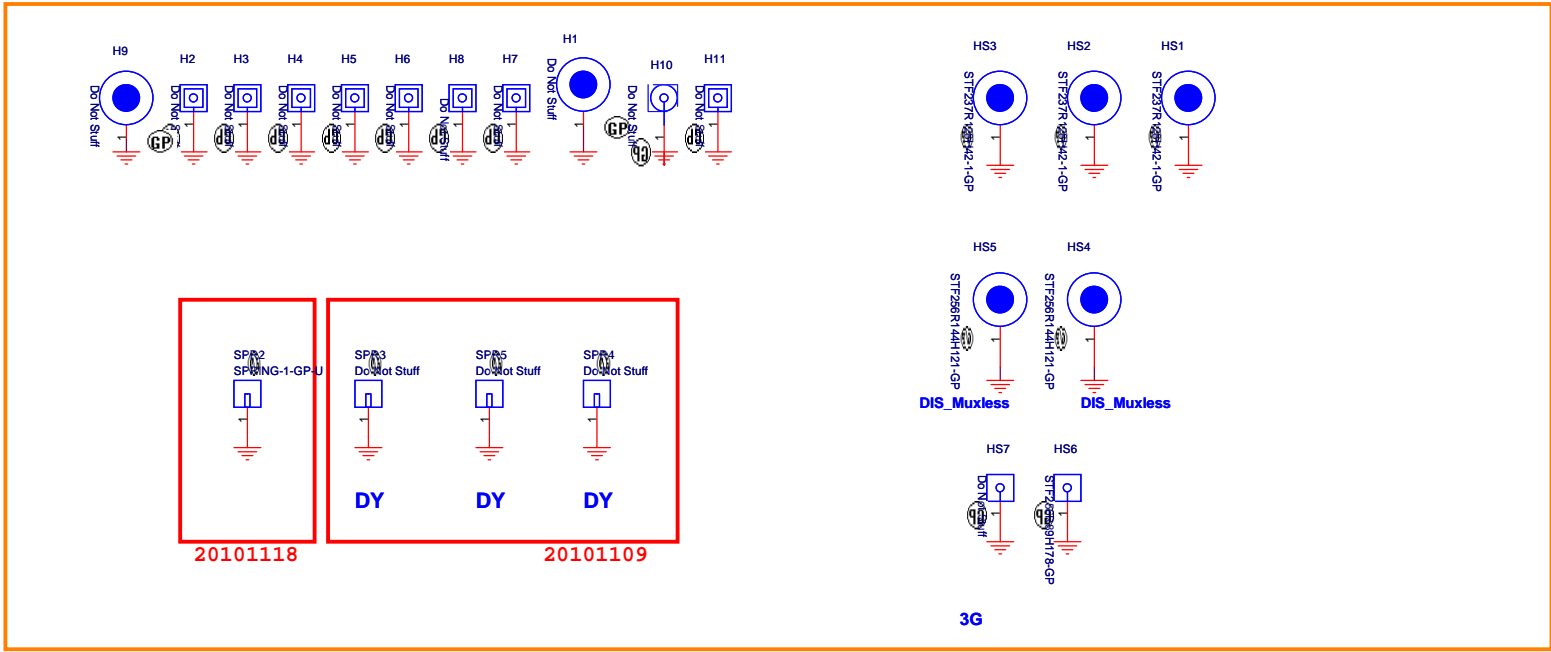
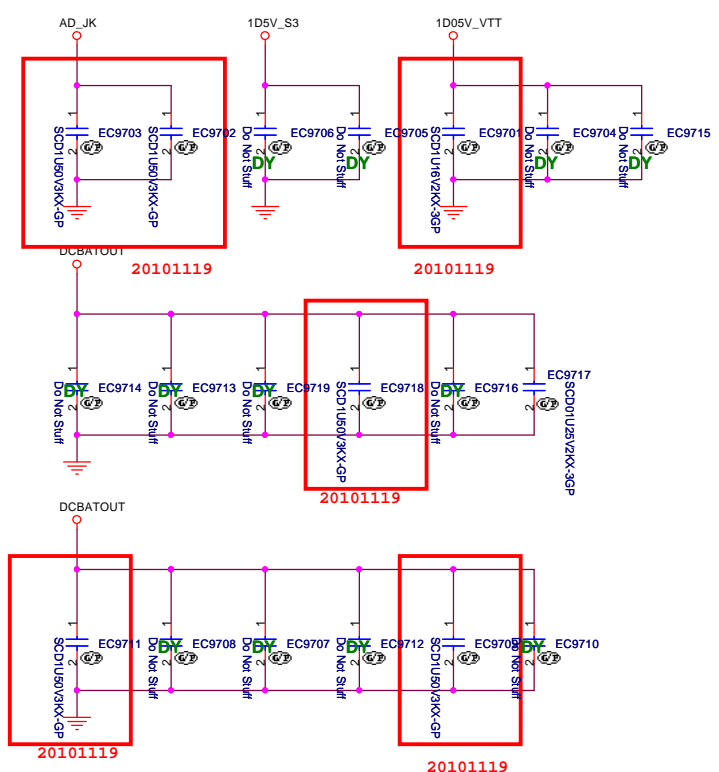
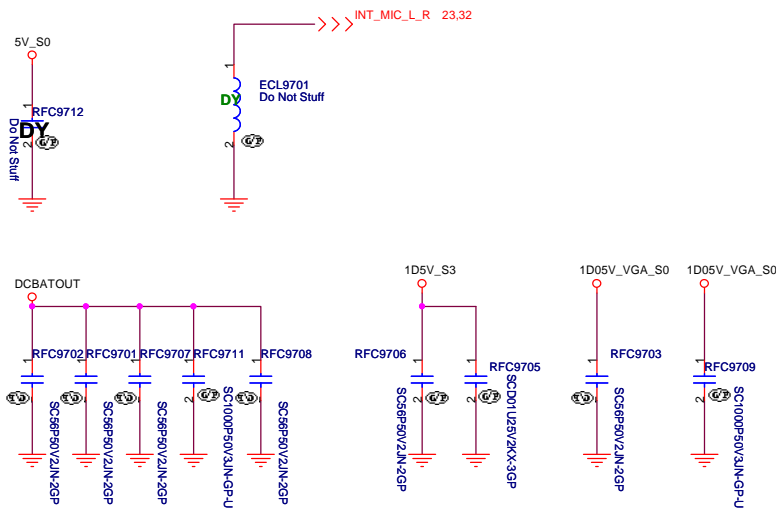
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Size: Document Number: **JE43-CP** Rev: -1

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Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

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AFTE TP

Size

Document Number

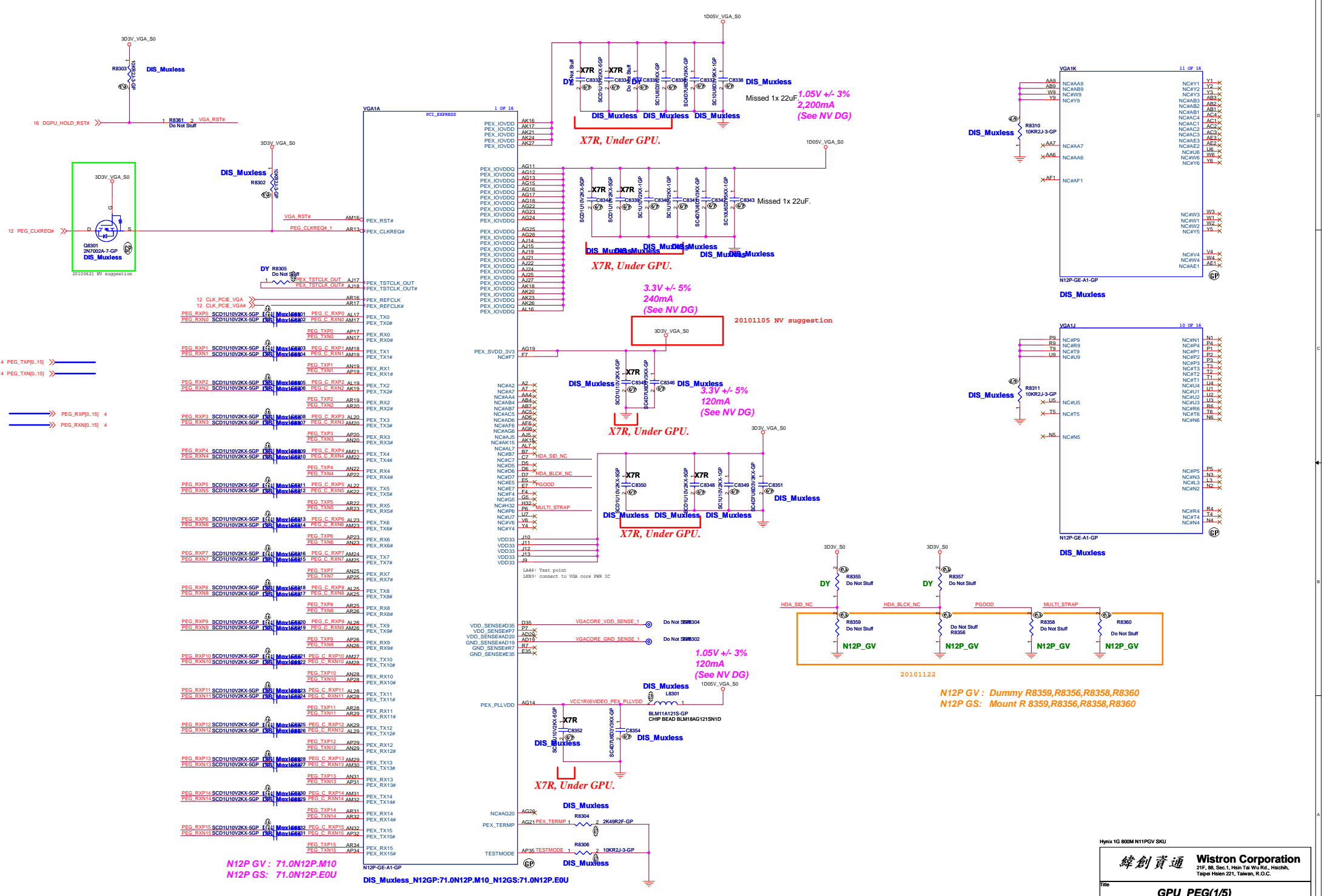
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Rev

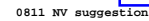
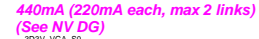
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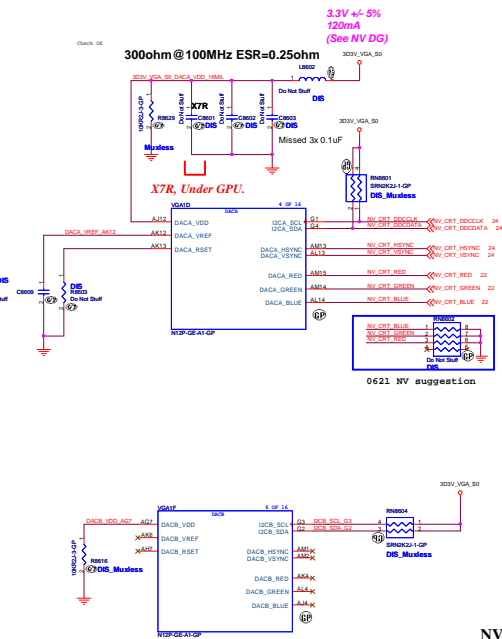
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VGA1G 7 OF 16



VGA Thermal sensor 787



Configuration	Vendor	Straps	Manufacturer Part Number	Speed Bin (MHz)
S4Mx16 DDR3	Hynix	0x2	H5TG1G63CFR-11C	800/800
	Samsung	0x3	K4W1G1646E-HC11	900
	Samsung	7BD	K4W1G1646E-BC11	900/900
	Hynix	0x0	H5TG1G63EFR-12C	800
	Samsung	0x1	K4W1G1646E-HC12	800

NVIDIA TABLE

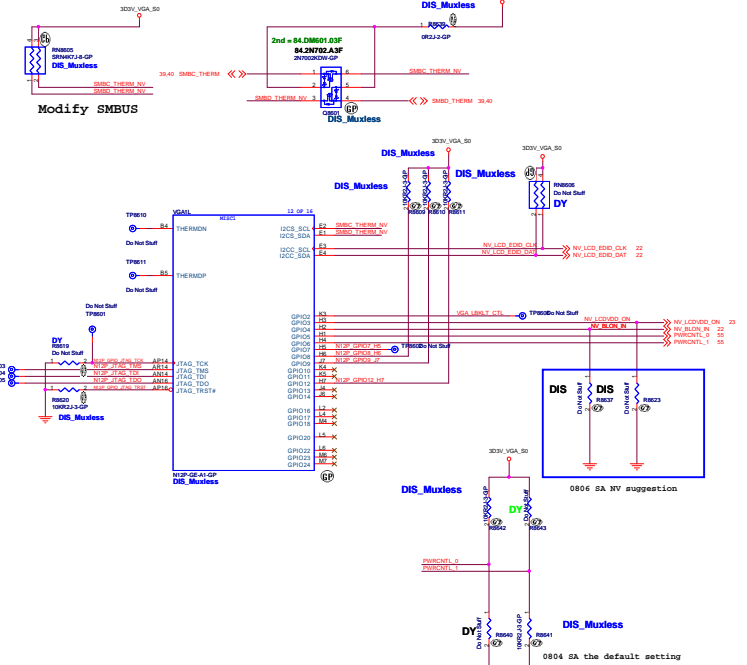
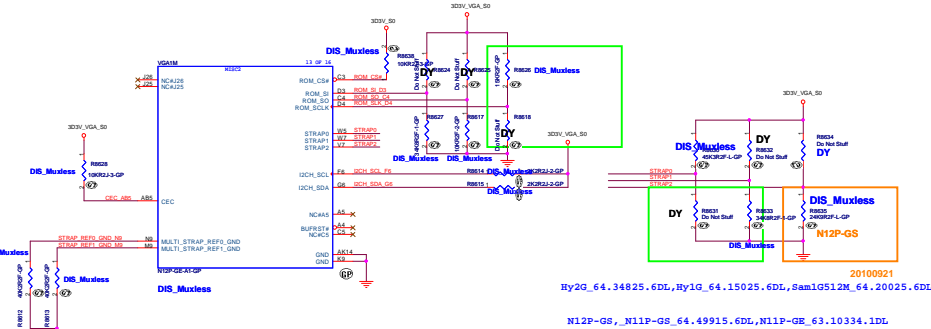
	Hynix 2G 0010 128*16*8	Hynix 1G 0010 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm	15Kohm	20Kohm	20Kohm	45Kohm
	64.34825.6DL	64.15025.6DL	64.20025.6DL	64.20025.6DL	64.45325.6DL

GPU_ROM_ST for 10bit for 20bit for 10bit for 20bit
Hynix VGRAM Hynix VGRAM Samsung VGRAM Samsung VGRAM
RAM_CPG[3]>0 RAM_CPG[3]>0 RAM_CPG[3]>1 RAM_CPG[3]>1
RAM_CPG[1]>1 RAM_CPG[1]>1 RAM_CPG[1]>1 RAM_CPG[1]>1
RAM_CPG[2]>0 RAM_CPG[2]>0 RAM_CPG[2]>0 RAM_CPG[2]>0
RAM_CPG[3]>0 RAM_CPG[3]>0 RAM_CPG[3]>0 RAM_CPG[3]>0

GPU_ROM_BO VBA_SERVISE=1 (low bit)
PRM_AJL_AJOL=0
PRM_SAR_STEER=0
SCLER_417=0 (High bit)

GPU_ROM_SCLER PRM_PIL_BN_TERN=0
SLOT_CLK_CFG=1
PRM_VENOM=0
PCE_DRIVE[4]=1

N11P Fermi QS 1



TABLE

NVIDIA	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x0DF7	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GV DEV ID: 0x0DF5 (0101)
STRAP2 PU R8634	25Kohm	45Kohm	10Kohm	5Kohm	30Kohm
	64.24925.6DL	64.45325.6DL	63.10334.1DL	64.49915.6DL	64.30025.6DL

STRAP0 USER[0]=1
USER[3]=4
USER[2]=1
USER[3]=1

N12P-GS
USE 1111 (45K)

N12P-GV

N11P-GE Pull Low

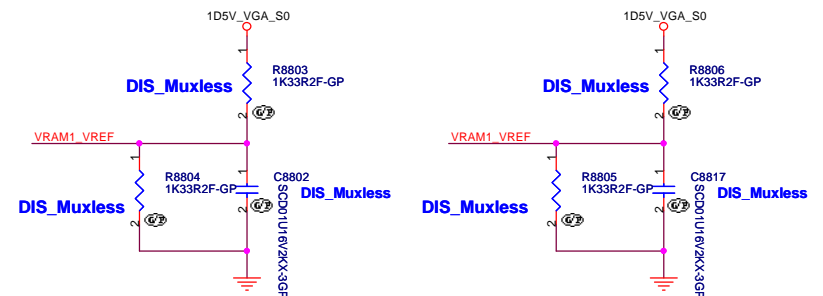
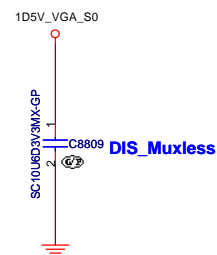
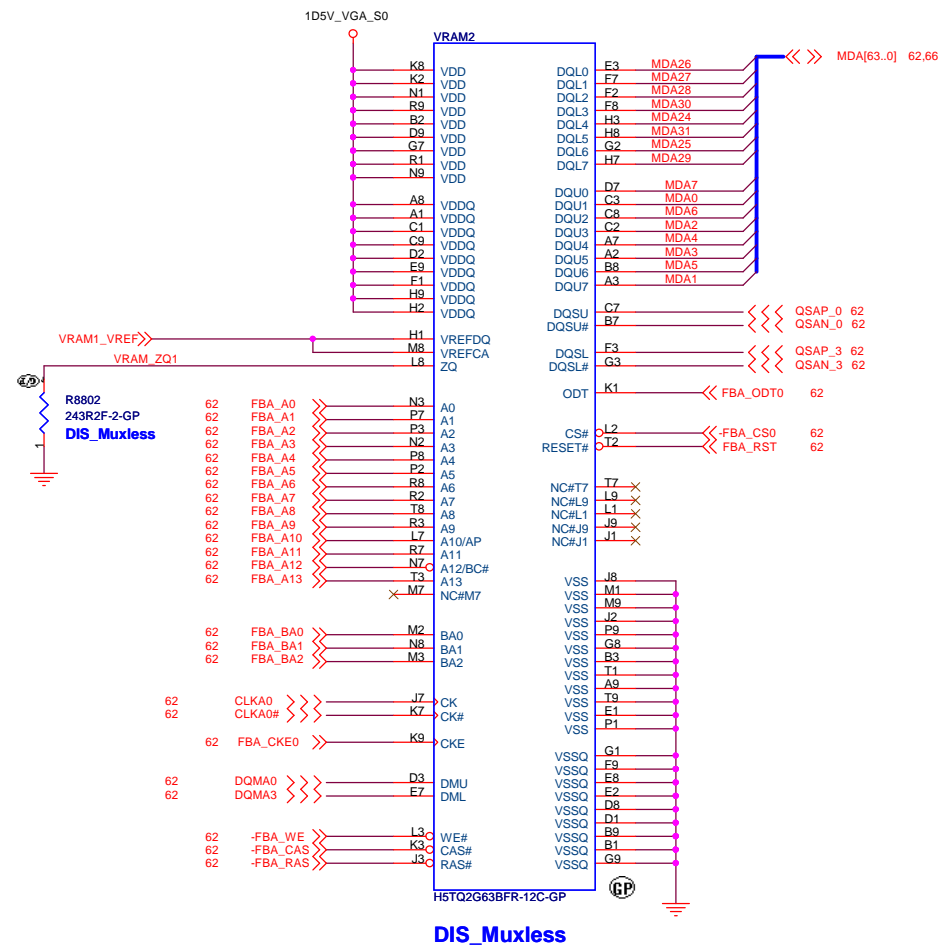
N11P-GS Pull Low

N12P-GV

STRAP1 3G10_PADCW[0]=0
3G10_PADCW[1]=1
3G10_PADCW[2]=1
3G10_PADCW[3]=1

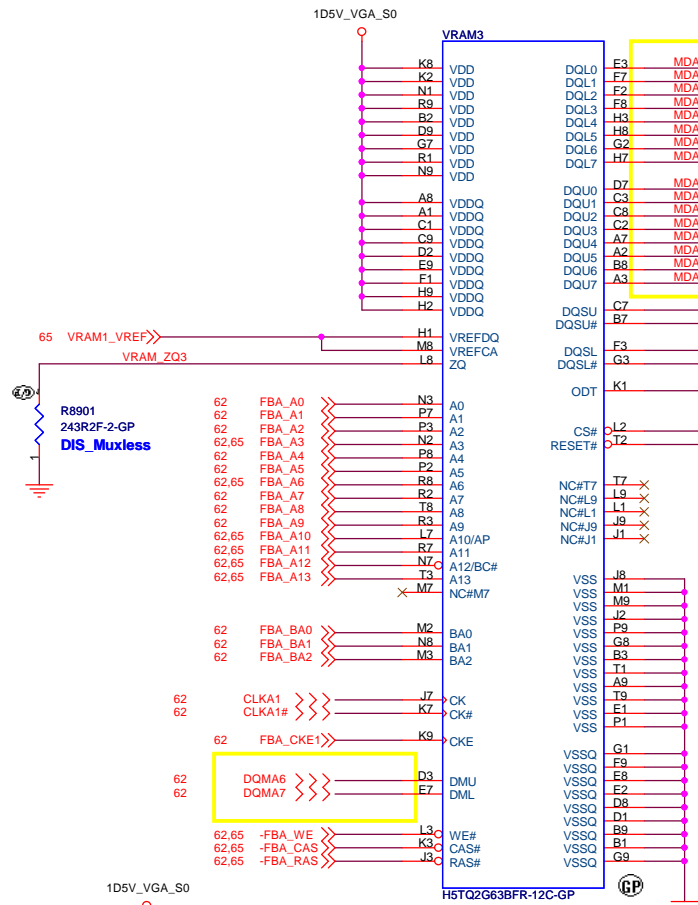
USE 0110 (35K)

STRAP2 PCI_DRIVE[0]=1 N12P-GS
PCI_DRIVE[1]=0 N12P-GV
PCI_DRIVE[2]=0 N11P-GS
PCI_DRIVE[3]=0 N11P-GE



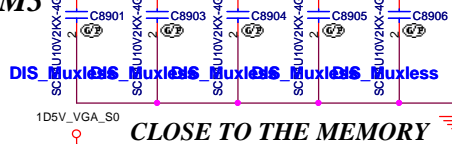
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Title			
GPU-VRAM1,2 (1/4)			
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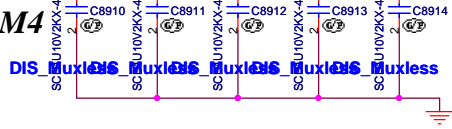
DIS_Muxless

FOR VRAM3



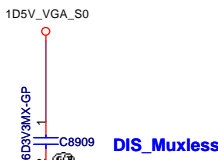
CLOSE TO THE MEMORY

FOR VRAM4

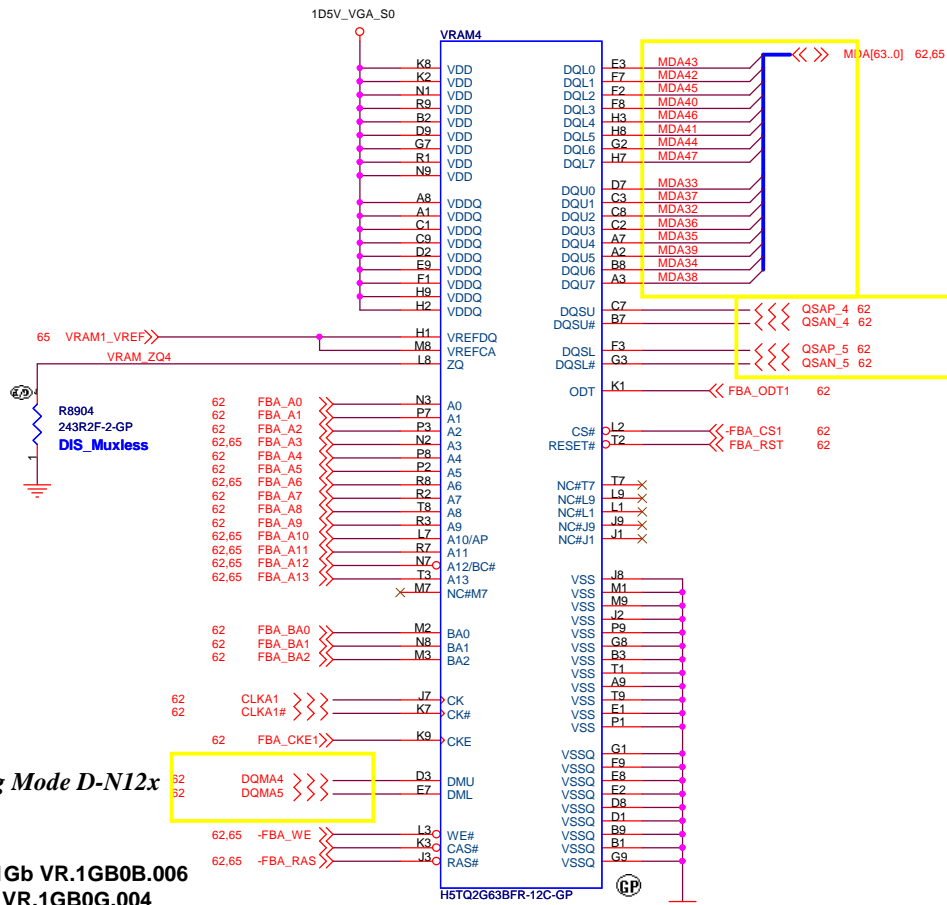


FB CMD mapping Mode D-N12x

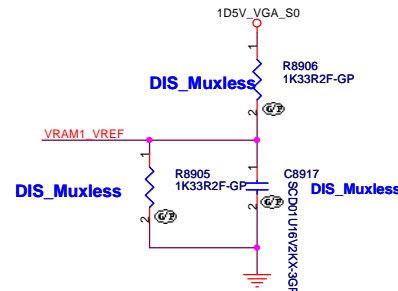
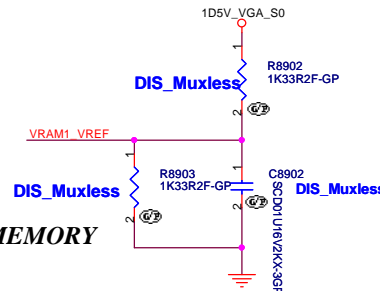
VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb VR.1GB0G.004
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY



DIS_Muxless

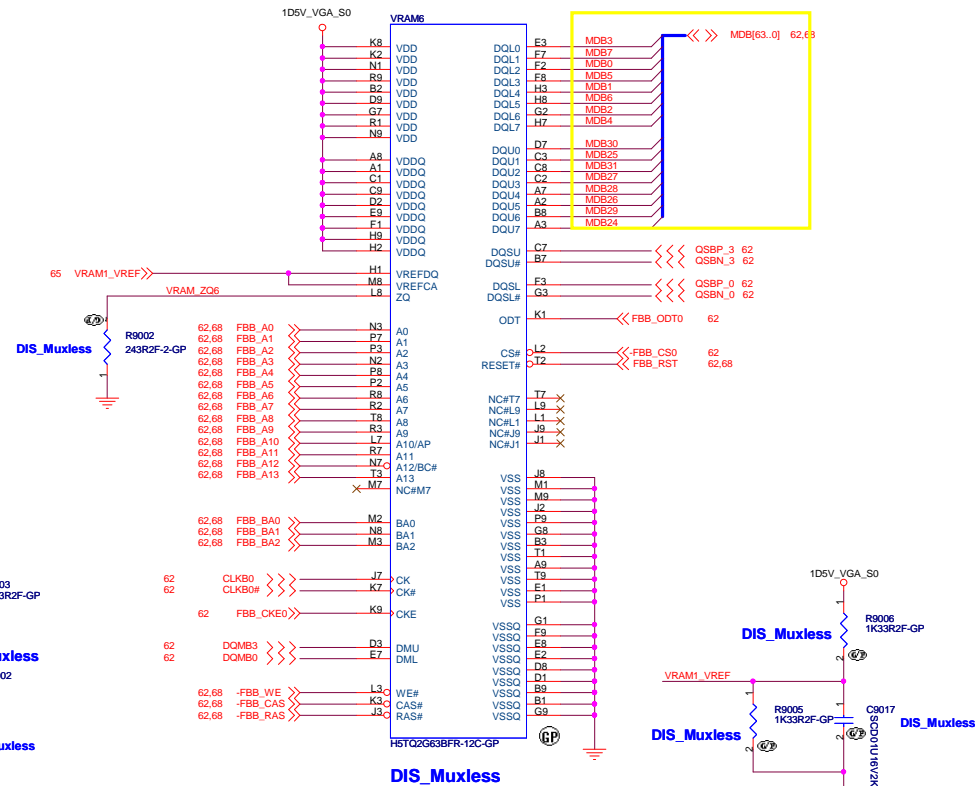


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GPU-VRAM3,4 (2/4)		
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FOR VRAM5

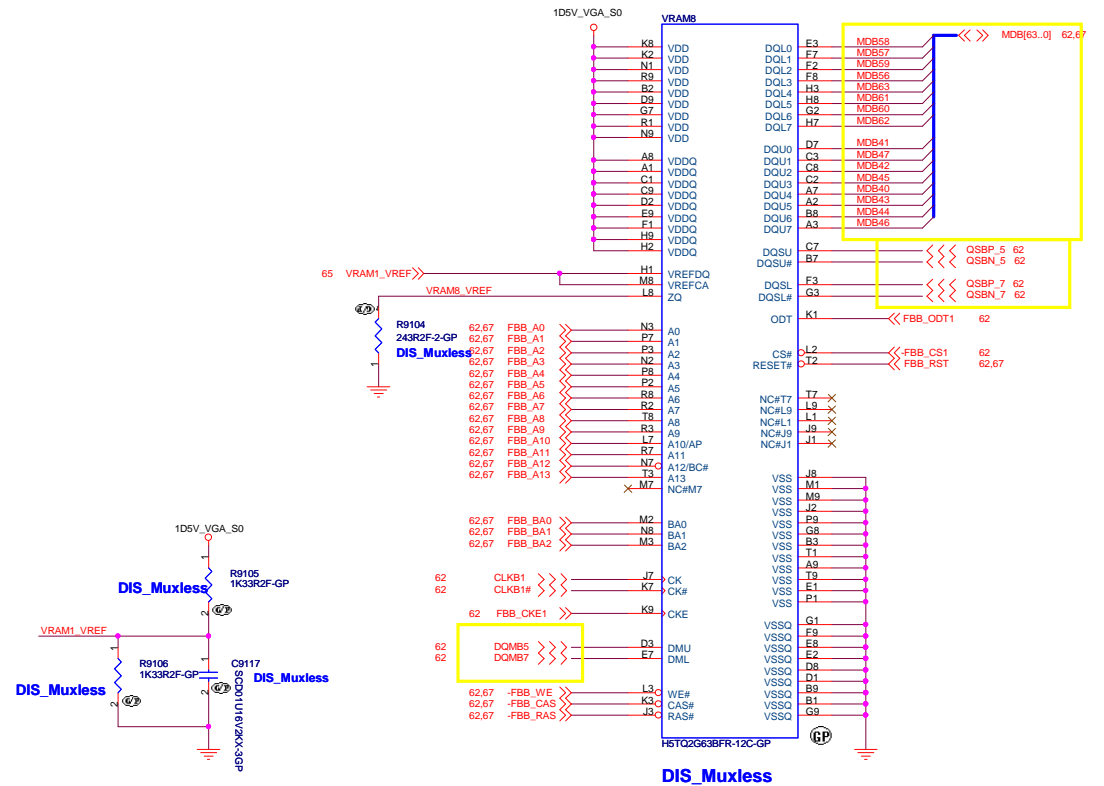
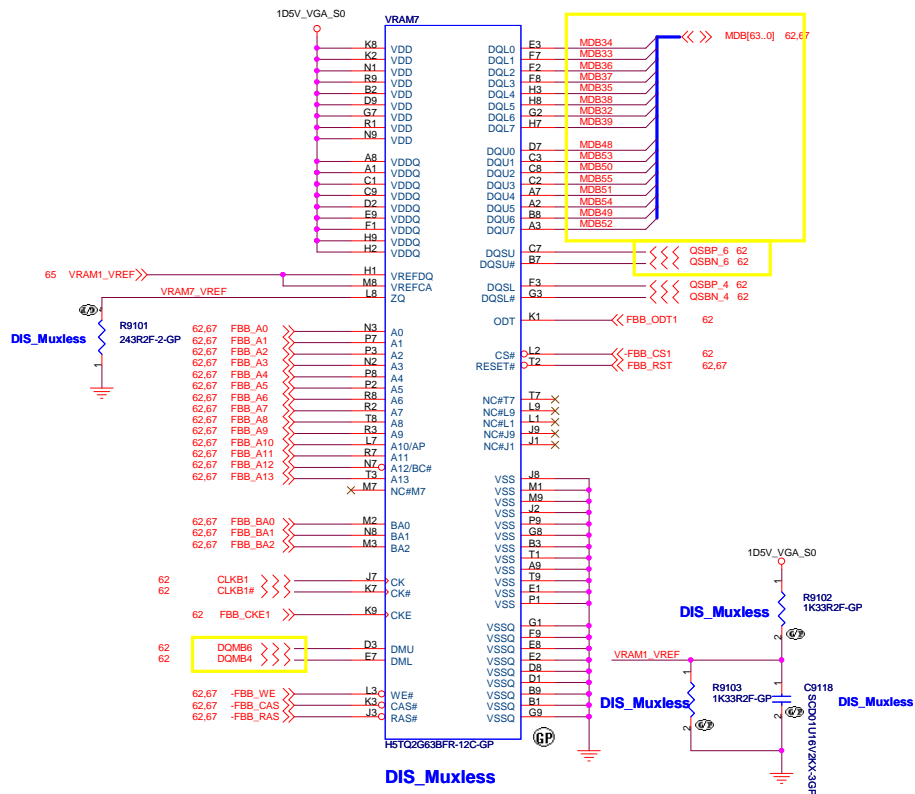
DIS_mux1016 DIS_mux1016 DIS_mux1016 DIS_mux1016 DIS_mux1016 DIS_mux1016

CLOSE TO THE MEMORY

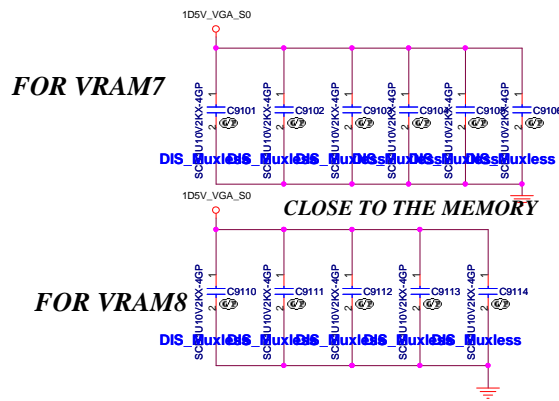
FOR VRAM6

DIS_mux1016 DIS_mux1016 DIS_mux1016 DIS_mux1016 DIS_mux1016 DIS_mux1016

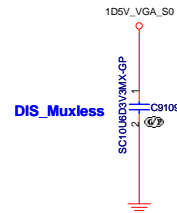
CLOSE TO THE MEMORY



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb VR.1GB0G.004
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY



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