WWW.AliSaler.Com

Berry Discrete/UMA Schematics Document

AMD Danube CPU S1g4

AMD GPU Madison-LP/M96-LP M2

RS880M + SB820M

2010-03-08

REV : A00

DY : Nopop Component

WWW.AliSaler.Com

<Core Design>

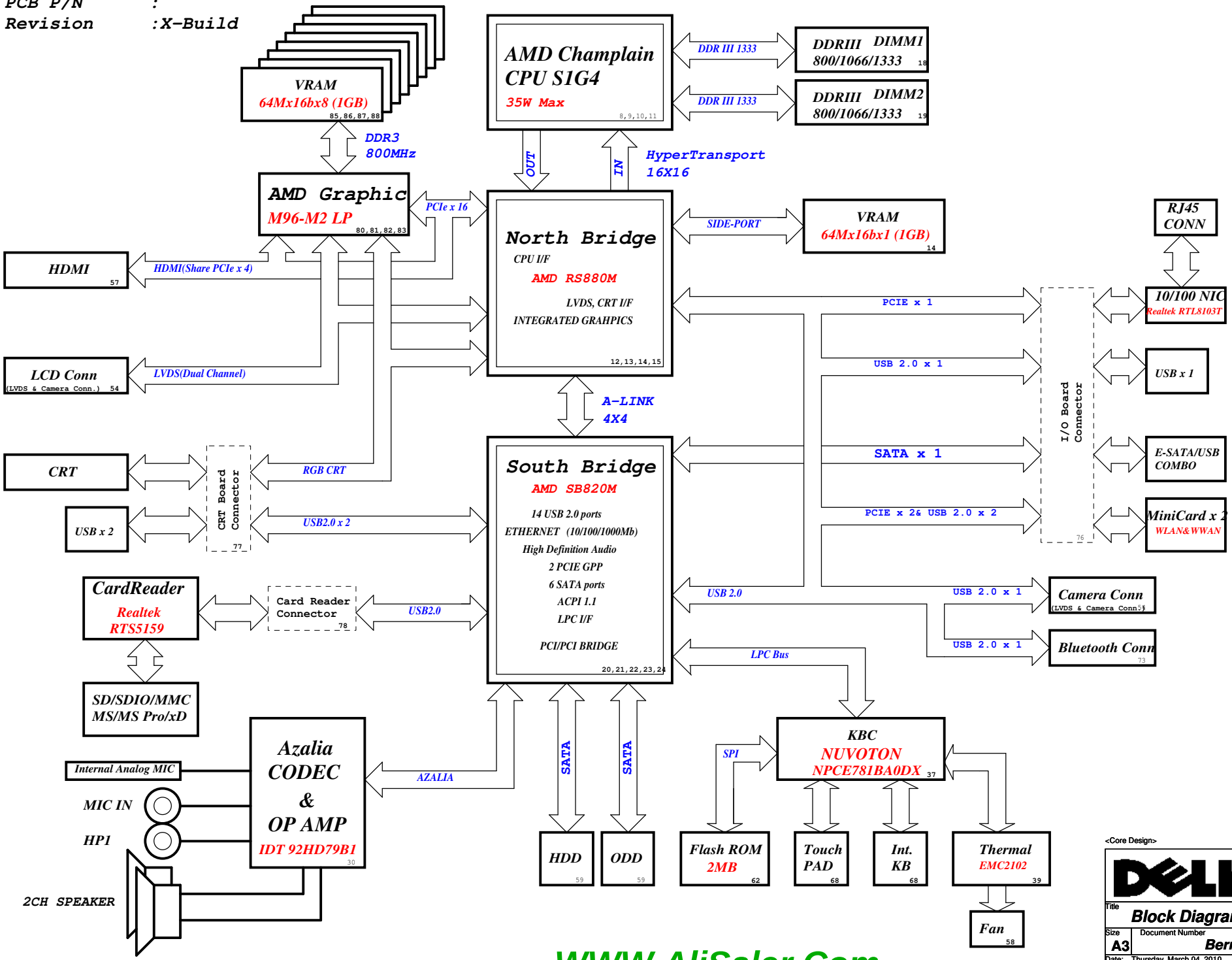
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size A4	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Monday, March 08, 2010	Sheet 1 of 95	

WWW.AliSaler.Com

Project code : 91.4LH01.001
PCB P/N :
Revision :X-Build

Berry DG15 Discrete/UMA Block Diagram



CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN_SS +VCHGR	+PWR_SRC

SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+3.3V_RTC_LDO +5V_ALW +3.3V_ALW

CPU VDDR RT9025 48	
INPUTS	OUTPUTS
+1.5V_SUS	+CPU_VDDR

CPU CORE ISL6265AHRTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB

AMD RS880M CORE RT8209 50	
INPUTS	OUTPUTS
+PWR_SRC	+NB_VDDC

AMD SB820M S5 POWER RT9025 48	
INPUTS	OUTPUTS
+3.3V_ALW	+1.1V_ALW

DDR III SUS&VTT RT8207 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS

DDR III SUS&VTT RT8207 49	
INPUTS	OUTPUTS
+PWR_SRC	+0.75V_DDR_VTT

AMD GPU CORE RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 2 of 95

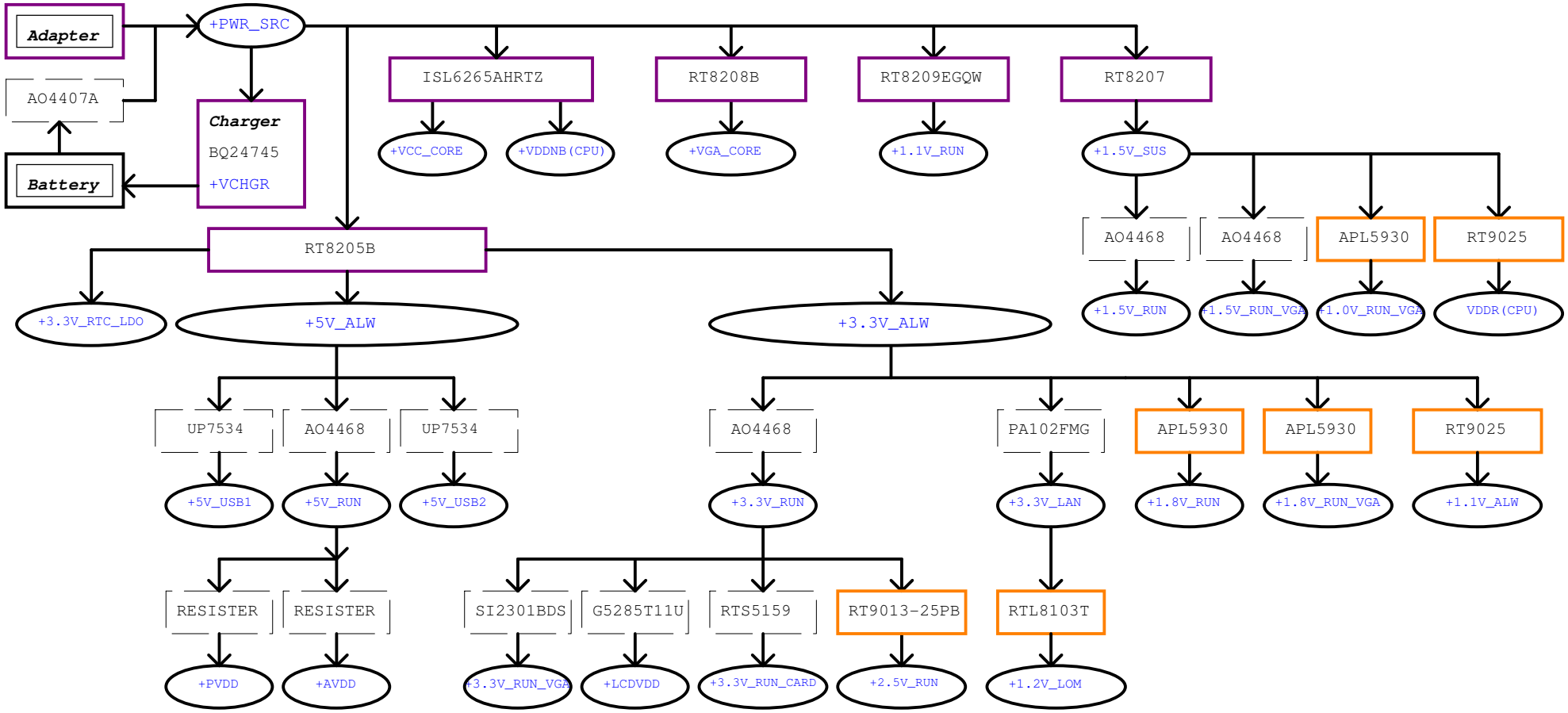
WWW.AliSaler.Com

WWW.AliSaler.Com

Power Block Diagram

Power Shape

Regulator | LDO | Switch



<Core Design>

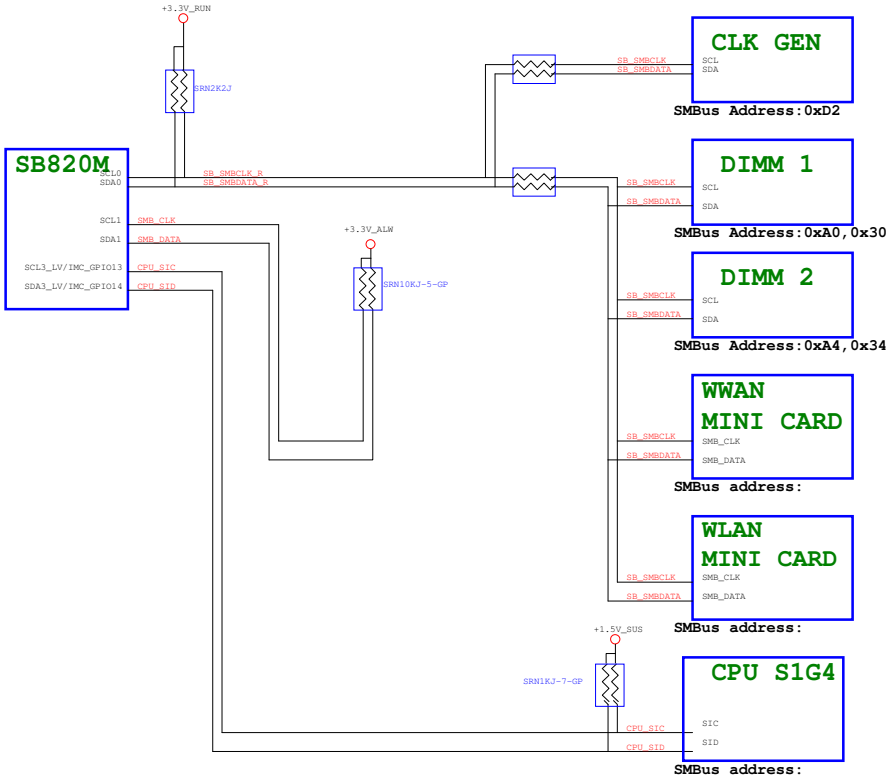
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power Block Diagram	
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 3 of 95	

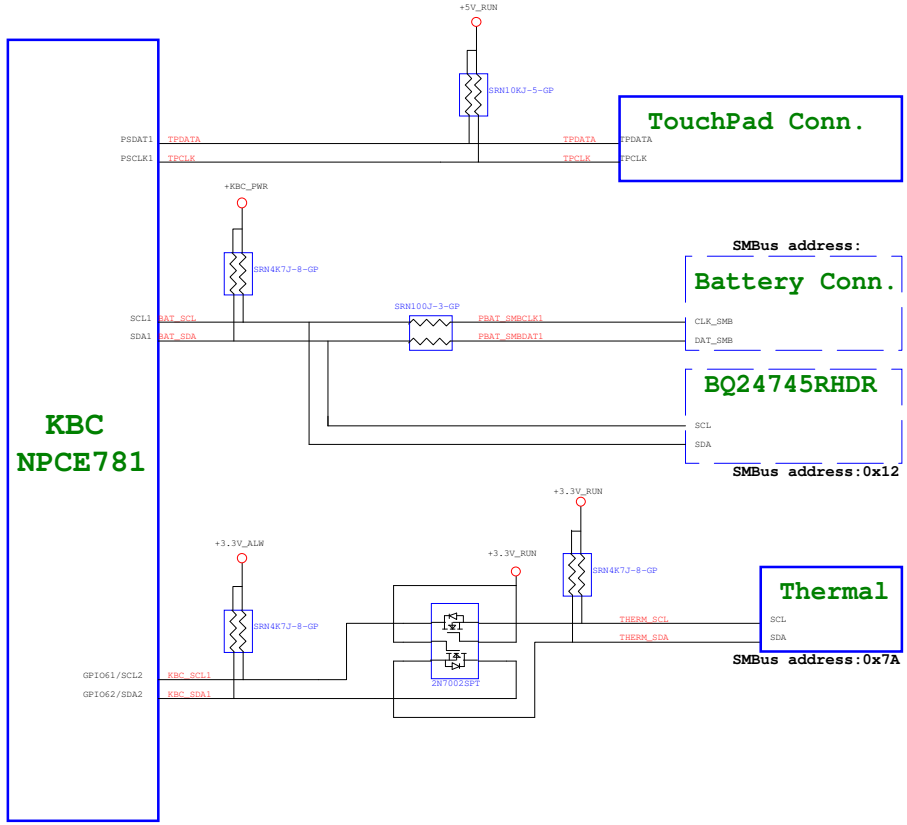
WWW.AliSaler.Com

WWW.AliSaler.Com

SB820M SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

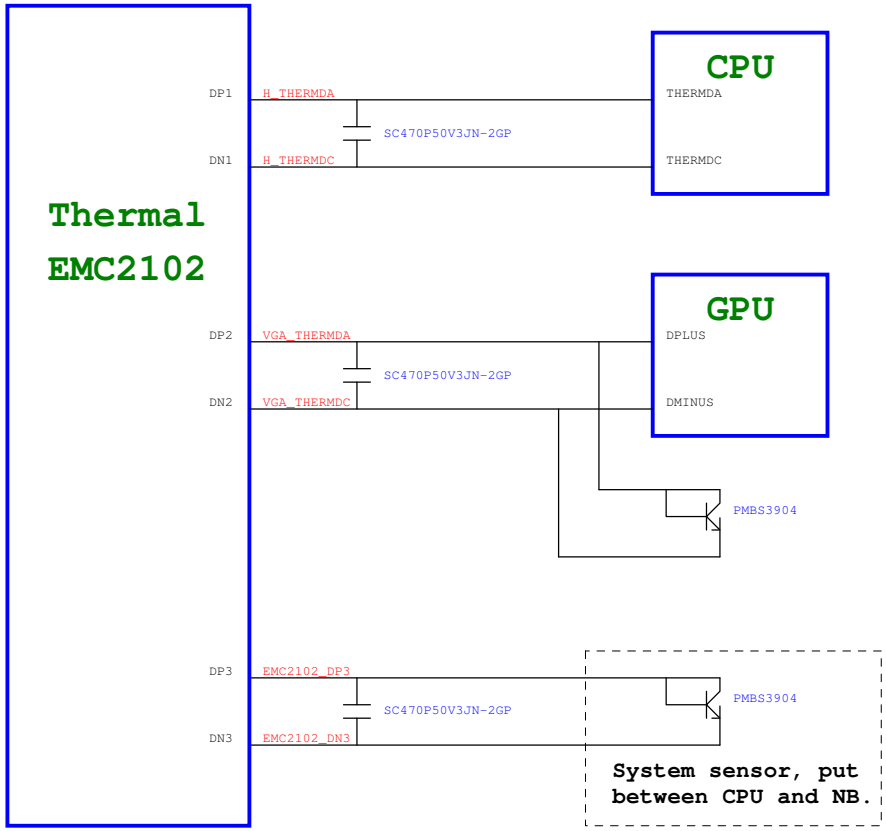
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM		
Size: A2	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 4 of 95	

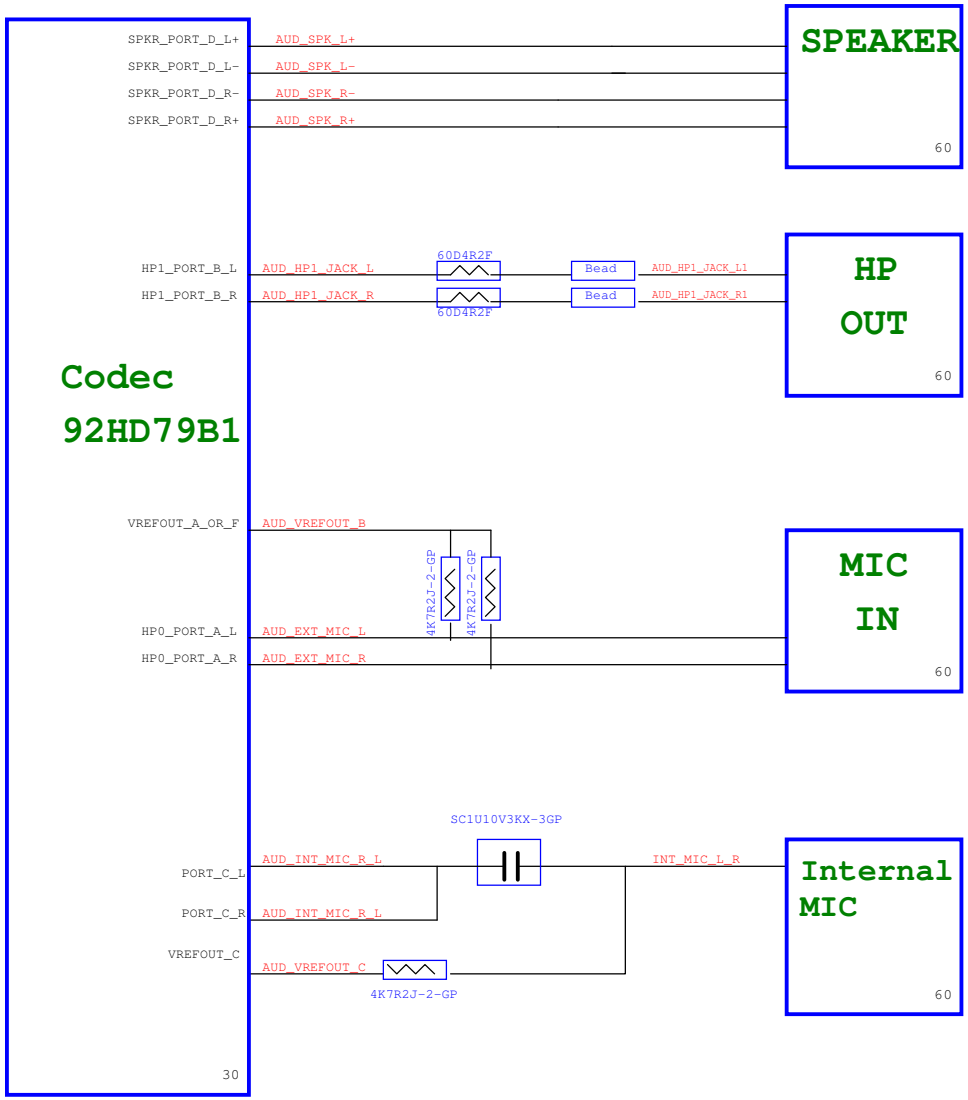
WWW.AliSaler.Com

WWW.AliSaler.Com

Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/AUDIO BLOCK DIAGRAM

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 5 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	**Embedded Controller (EC)** * 0 V - Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub 0V / 3.3V / LPC ROM * (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	**Defines clock generator** * 0V – External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. 3.3V– Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	**Set PCIe to Gen II mode** 0V– Force PCIe interface at Gen I mode * 3.3V– PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	**Watchdog function** * 0V– Disable the boot fail timer function 3.3V– Enable the boot fail timer function
PCICLK3	DefaultStrapMode	**Default Debug Straps** * 0V– Disable Debug Straps. 3.3V– Select external Debug Straps
PCICLK4	CPUClkSel	**CPU/NB HT Clock Selection** 0V– Reserved. * 3.3V– Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	**Slow down core clock for low power platform.** * 0V– Performance mode 3.3V– Low Power mode

RS880M Strapping

Capture from 46113_rs880m_ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available(UMA) 1: Not available(Discrete)
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB0 (I/O Board/ESATA)
1	USB1 (I/O Board)
2	USB2 (CRT Board)
3	USB3 (CRT Board)
4	WLAN USB
5	WWAN USB
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA (LVDS CONN)
12	RESERVED
13	RESERVED

PCIE Routing

	RS880M
LANE0	MiniCard WLAN
LANE1	LAN
LANE2	MiniCard WWAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

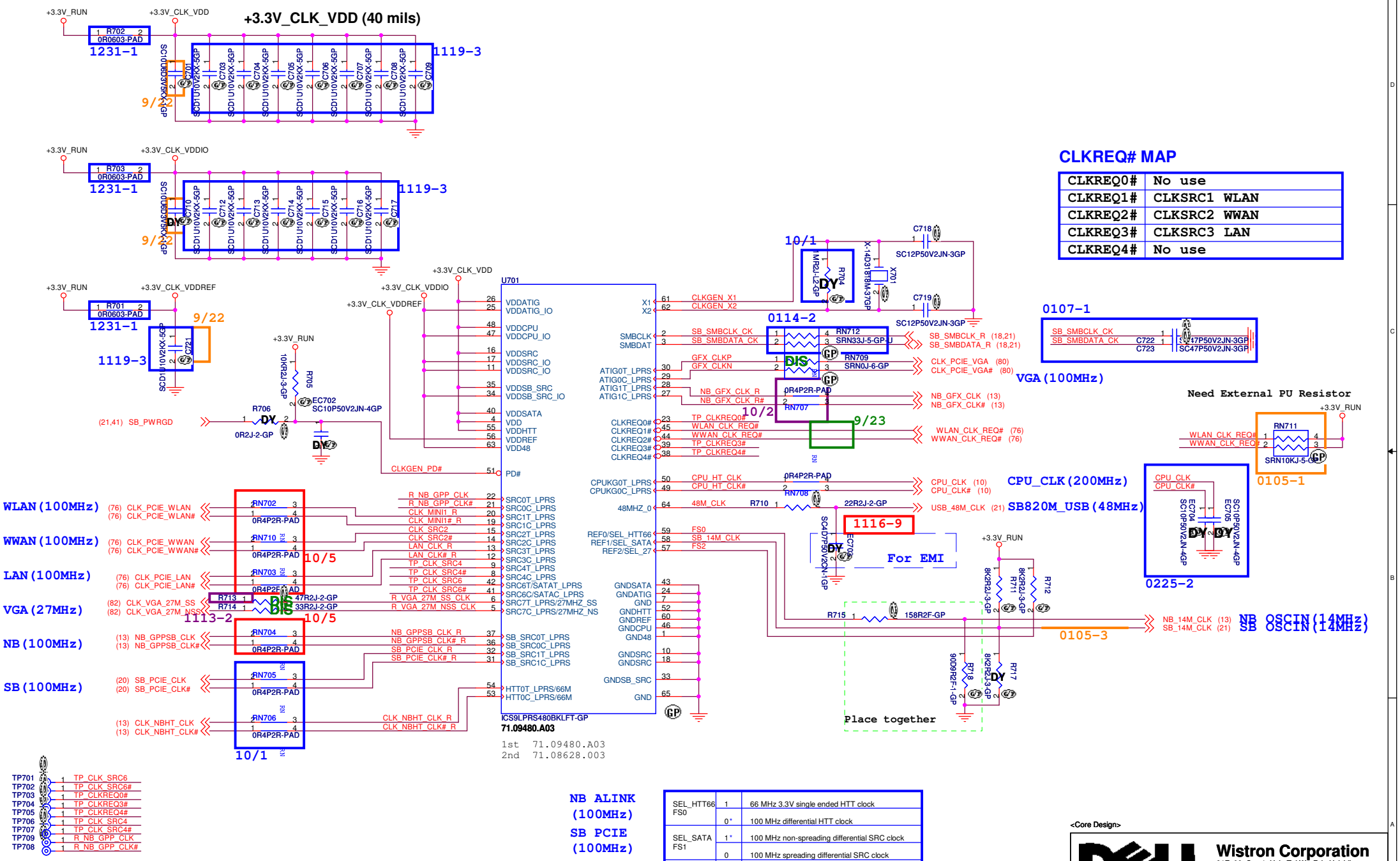
Title: Table of Content

Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 6 of 95

WWW.AliSaler.Com

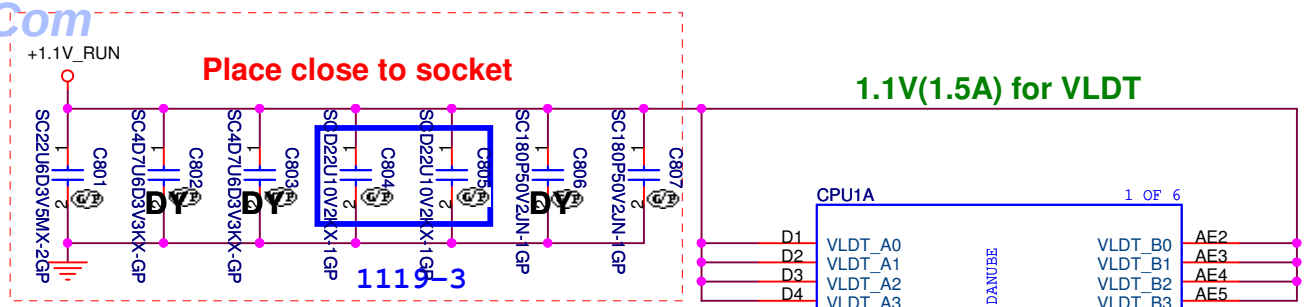
WWW.AliSaler.Com



WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = CPU



CPU1A 1 OF 6

DANUBE

D1	VLDT_A0		VLDT_B0	AE2	
D2	VLDT_A1		VLDT_B1	AE3	
D3	VLDT_A2		VLDT_B2	AE4	
D4	VLDT_A3		VLDT_B3	AE5	
E3	L0_CADIN_H0	(12) HT_NB_CPU_CAD_H0	L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0 (12)
E2	L0_CADIN_L0	(12) HT_NB_CPU_CAD_L0	L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0 (12)
E1	L0_CADIN_H1	(12) HT_NB_CPU_CAD_H1	L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1 (12)
F1	L0_CADIN_L1	(12) HT_NB_CPU_CAD_L1	L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1 (12)
G3	L0_CADIN_H2	(12) HT_NB_CPU_CAD_H2	L0_CADOUT_H2	AB1	HT_CPU_NB_CAD_H2 (12)
G2	L0_CADIN_L2	(12) HT_NB_CPU_CAD_L2	L0_CADOUT_L2	AA1	HT_CPU_NB_CAD_L2 (12)
G1	L0_CADIN_H3	(12) HT_NB_CPU_CAD_H3	L0_CADOUT_H3	AA2	HT_CPU_NB_CAD_H3 (12)
H1	L0_CADIN_L3	(12) HT_NB_CPU_CAD_L3	L0_CADOUT_L3	AA3	HT_CPU_NB_CAD_L3 (12)
J1	L0_CADIN_H4	(12) HT_NB_CPU_CAD_H4	L0_CADOUT_H4	W2	HT_CPU_NB_CAD_H4 (12)
K1	L0_CADIN_L4	(12) HT_NB_CPU_CAD_L4	L0_CADOUT_L4	W3	HT_CPU_NB_CAD_L4 (12)
L3	L0_CADIN_H5	(12) HT_NB_CPU_CAD_H5	L0_CADOUT_H5	V1	HT_CPU_NB_CAD_H5 (12)
L2	L0_CADIN_L5	(12) HT_NB_CPU_CAD_L5	L0_CADOUT_L5	U1	HT_CPU_NB_CAD_L5 (12)
L1	L0_CADIN_H6	(12) HT_NB_CPU_CAD_H6	L0_CADOUT_H6	U2	HT_CPU_NB_CAD_H6 (12)
M1	L0_CADIN_L6	(12) HT_NB_CPU_CAD_L6	L0_CADOUT_L6	U3	HT_CPU_NB_CAD_L6 (12)
N3	L0_CADIN_H7	(12) HT_NB_CPU_CAD_H7	L0_CADOUT_H7	T1	HT_CPU_NB_CAD_H7 (12)
N2	L0_CADIN_L7	(12) HT_NB_CPU_CAD_L7	L0_CADOUT_L7	R1	HT_CPU_NB_CAD_L7 (12)
E5	L0_CADIN_H8	(12) HT_NB_CPU_CAD_H8	L0_CADOUT_H8	AD4	HT_CPU_NB_CAD_H8 (12)
F5	L0_CADIN_L8	(12) HT_NB_CPU_CAD_L8	L0_CADOUT_L8	AD3	HT_CPU_NB_CAD_L8 (12)
F3	L0_CADIN_H9	(12) HT_NB_CPU_CAD_H9	L0_CADOUT_H9	AD5	HT_CPU_NB_CAD_H9 (12)
F4	L0_CADIN_L9	(12) HT_NB_CPU_CAD_L9	L0_CADOUT_L9	AC5	HT_CPU_NB_CAD_L9 (12)
G5	L0_CADIN_H10	(12) HT_NB_CPU_CAD_H10	L0_CADOUT_H10	AB4	HT_CPU_NB_CAD_H10 (12)
H5	L0_CADIN_L10	(12) HT_NB_CPU_CAD_L10	L0_CADOUT_L10	AB3	HT_CPU_NB_CAD_L10 (12)
H3	L0_CADIN_H11	(12) HT_NB_CPU_CAD_H11	L0_CADOUT_H11	AB5	HT_CPU_NB_CAD_H11 (12)
H4	L0_CADIN_L11	(12) HT_NB_CPU_CAD_L11	L0_CADOUT_L11	AA5	HT_CPU_NB_CAD_L11 (12)
K3	L0_CADIN_H12	(12) HT_NB_CPU_CAD_H12	L0_CADOUT_H12	Y5	HT_CPU_NB_CAD_H12 (12)
K4	L0_CADIN_L12	(12) HT_NB_CPU_CAD_L12	L0_CADOUT_L12	W5	HT_CPU_NB_CAD_L12 (12)
L5	L0_CADIN_H13	(12) HT_NB_CPU_CAD_H13	L0_CADOUT_H13	V4	HT_CPU_NB_CAD_H13 (12)
M5	L0_CADIN_L13	(12) HT_NB_CPU_CAD_L13	L0_CADOUT_L13	V3	HT_CPU_NB_CAD_L13 (12)
M3	L0_CADIN_H14	(12) HT_NB_CPU_CAD_H14	L0_CADOUT_H14	V5	HT_CPU_NB_CAD_H14 (12)
M4	L0_CADIN_L14	(12) HT_NB_CPU_CAD_L14	L0_CADOUT_L14	U5	HT_CPU_NB_CAD_L14 (12)
N5	L0_CADIN_H15	(12) HT_NB_CPU_CAD_H15	L0_CADOUT_H15	T4	HT_CPU_NB_CAD_H15 (12)
P5	L0_CADIN_L15	(12) HT_NB_CPU_CAD_L15	L0_CADOUT_L15	T3	HT_CPU_NB_CAD_L15 (12)
J3	L0_CLKIN_H0	(12) HT_NB_CPU_CLK_H0	L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0 (12)
J2	L0_CLKIN_L0	(12) HT_NB_CPU_CLK_L0	L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0 (12)
J5	L0_CLKIN_H1	(12) HT_NB_CPU_CLK_H1	L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1 (12)
K5	L0_CLKIN_L1	(12) HT_NB_CPU_CLK_L1	L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1 (12)
N1	L0_CTLIN_H0	(12) HT_NB_CPU_CTL_H0	L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0 (12)
P1	L0_CTLIN_L0	(12) HT_NB_CPU_CTL_L0	L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0 (12)
P3	L0_CTLIN_H1	(12) HT_NB_CPU_CTL_H1	L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1 (12)
P4	L0_CTLIN_L1	(12) HT_NB_CPU_CTL_L1	L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1 (12)

SKT-BGA638H176
1'nd 62.10055.111
2'nd 62.10055.171

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size: A4 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 8 of 95

WWW.AliSaler.Com

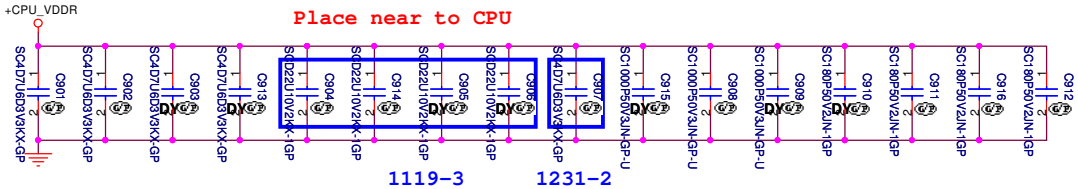
WWW.AliSaler.Com

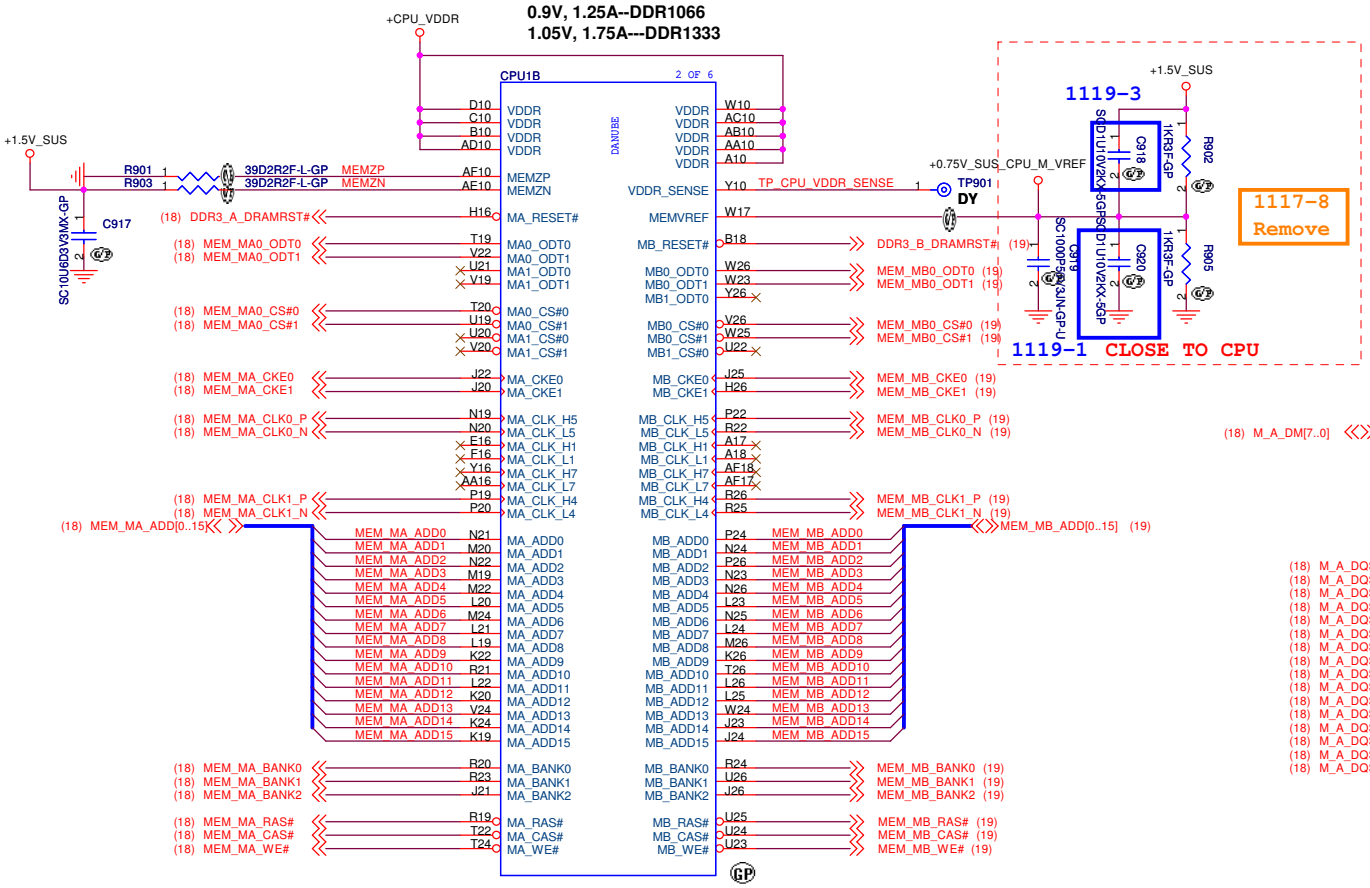
SSID = CPU

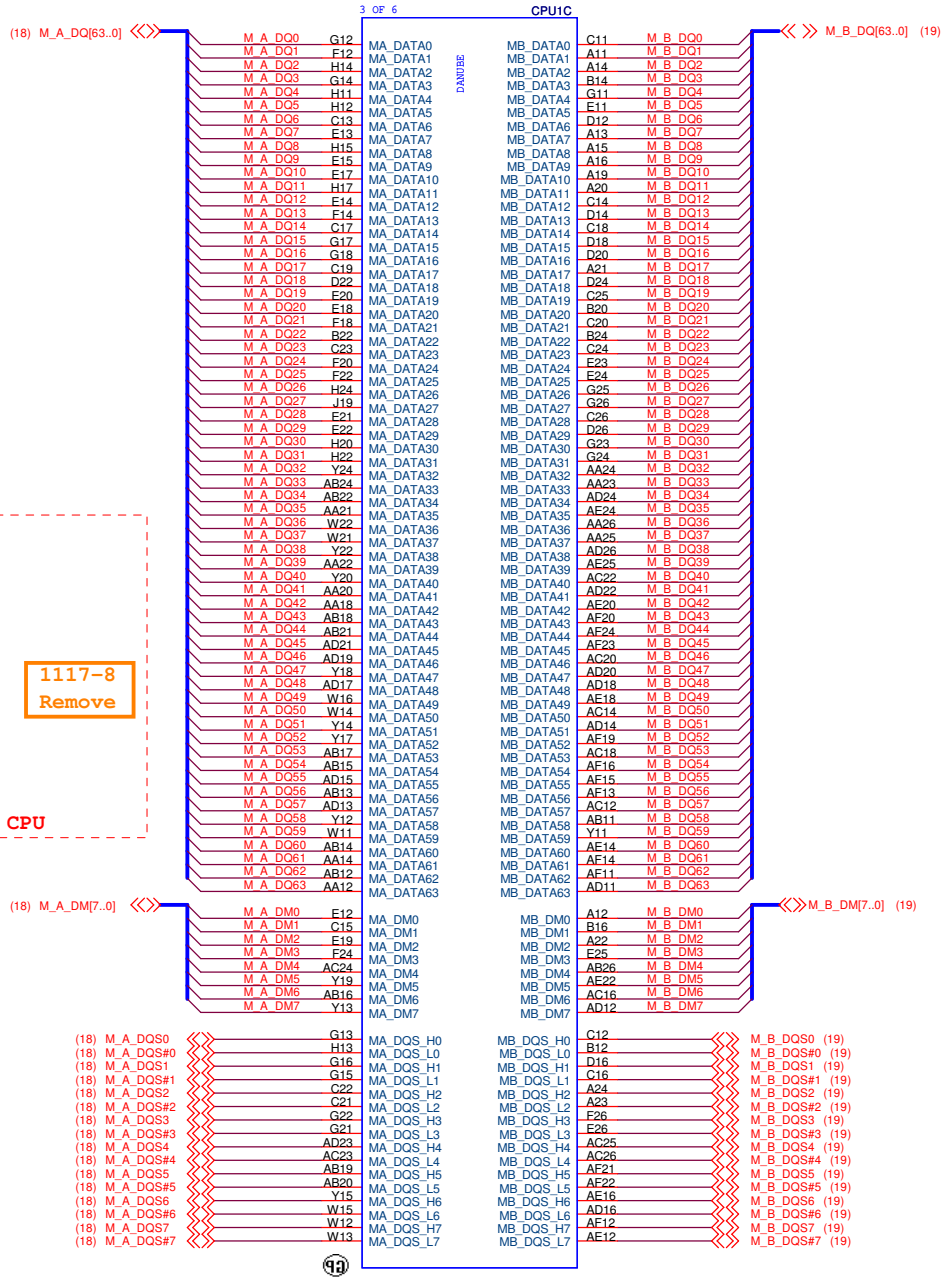
1231-2

Set empty: C905,C906,C903,C909,C913,C910,C915

4.7UF*4
0.22UF*4
1000PF*4
180PF*4







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 9 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = CPU

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

2.5V(250mA) for VDDA

+2.5V_RUN 1119-1 L1001 PBY160808T-330Y-N-GP 33R, 3A +2.5V_RUN_VDDA

SC180P50V2JN-1GP C1001 SC10U10V5ZY-1GP C1002 11/6 SCD22U10V2KX-1GP C1003 SC3300P50V3KX-1GP C1004

CPU1D 4 OF 6 DANUBE

VDDA F8 VDDA F9
CLKIN_H A9 CLKIN_L A8
RESET# B7 PWROK A7 LDTSTOP# F10 LDTREQ# C6
SIC AF4 SID AF5 ALERT# AF6
HT_REF0 R6 HT_REF1 P6
VDD0_FB_H F6 VDD0_FB_L E6
VDD1_FB_H Y6 VDD1_FB_L AB6
DBRDY G10 TMS AA9 TCK AC9 TRST# AD9 TDI AF9
TEST23 AD7
TEST18 H10 TEST19 G9
TEST25_H E9 TEST25_L E8
TEST21 AB8 TEST20 AF7 TEST24 AE7 TEST22 AE8 TEST12 AC8 TEST27 AF8
TEST9 C2 TEST6 AA6
RSVD#A3 A3 RSVD#A5 A5 RSVD#B3 B3 RSVD#B5 B5 RSVD#C1 C1

VSS M11 RSVD#W18 W18
SVC A6 SVD A4
THERMTRIP# AF6 PROCHOT# AC7 MEMHOT# AA8
THERMDC W7 THERMDA W8
VDDIO_FB_H W9 VDDIO_FB_L Y9
VDDNB_FB_H H6 VDDNB_FB_L G6
DBREQ# E10 TDO AF9
TEST28_H J7 TEST28_L H8
TEST17 D7 TEST16 E7 TEST15 F7 TEST14 C7
TEST7 C3 TEST10 K8
TEST8 C4
TEST29_H C9 TEST29_L C8
RSVD#H18 H18 RSVD#H19 H19 RSVD#AA7 AA7 RSVD#D5 D5 RSVD#C5 C5

1225-4 +1.5V_SUS RN1006 SRN1KJ-7-GP 9/25 9/14 1KR2J-1-GP R1006 300R2J-4-GP R1007

CPU_SVC (47) CPU_SVD (47)
CPU_THERMTRIP# CPU_PROCHOT# (20)
CPU_PROCHOT# CPU_MEMHOT# TP1002 S1G4 not support MEMHOT
H_THERMDC (39) H_THERMDA (39)
TP_CPU_VDDIO_SUS_FB_H TP_CPU_VDDIO_SUS_FB_L
CPU_VDDNB_RUN_FB_H (47) CPU_VDDNB_RUN_FB_L (47)
CPU_DBREQ# R1015 300R2J-4-GP +1.5V_SUS
CPU_TDO
TP_CPU_TEST28_H TP_CPU_TEST28_L
TP_CPU_TEST17 TP_CPU_TEST16 TP_CPU_TEST15 TP_CPU_TEST14
TP_CPU_TEST7 CPU_TEST10 R1021 300R3-GP +1.1V_RUN
TP_CPU_TEST8
CPU_TEST29H CPU_TEST29L R1024 80D6R2F-L-GP

+1.5V_RUN 10/5 RN1001 SRN300J-3-GP

CPU_CLK(200MHz) (7) CPU_CLK (7) CPU_CLK# C1005 C1006 SC3900P50V2KX-2GP SC3900P50V2KX-2GP R1008 169R2F-GP Cloce To CPU CPUCLK_IN CPUCLK_IN#

CPU_R_LDT_RST# HDT_RST_R# R1009 0R2J-2-GP For HDT DBG

CPU_R_LDT_PWRGD CPU_R_LDT_STOP# CPU_LDT_REQ# 0108-5 SCD10U10V2KX-3GP C1007 Close CPU

CPU_SIC CPU_SID CPU_ALERT#

+1.1V_RUN R1010 R1011 44D2R2F-GP CPU_HTREF0 CPU_HTREF1

(20) CPU_LDT_RST# (20,42) CPU_LDT_PWRGD (13,20) CPU_LDT_STOP# 1231-1 R1001 R1002 R1003 0R0402-PAD CPU_R_LDT_RST# CPU_R_LDT_PWRGD CPU_R_LDT_STOP# 11/6 SCD10U10V2KX-3GP C1008 1129-1 EC1001 SCD01U16V2KX-3GP 1231-2

9/11 S1g4 no support LDTREQ#

+1.5V_RUN R1012 DY 300R2J-4-GP CPU_LDT_REQ#

R1013 DY 300R2J-4-GP CPU_DBRDY
R1014 DY 300R2J-4-GP TP_CPU_TEST14
R1016 DY 300R2J-4-GP TP_CPU_TEST15
R1017 1KR2J-1-GP CPU_TEST23
R1025 1KR2J-1-GP CPU_TEST12
RN1002 SRN1KJ-7-GP CPU_TEST18 CPU_TEST19
RN1004 SRN1KJ-8-GP CPU_TEST20 CPU_TEST21 CPU_TEST24 CPU_TEST22 1231-1

+1.5V_SUS R1018 510R2F-L-GP R1019 510R2F-L-GP R1020 510R2F-L-GP DY R1022 510R2F-L-GP 1231-1

CPU_TEST23 CPU_TEST18 CPU_TEST19 CPU_TEST25_H CPU_TEST25_L CPU_TEST21 CPU_TEST20 CPU_TEST24 CPU_TEST22 CPU_TEST12 CPU_TEST27 CPU_TEST9 R1023 0R0402-PAD 1231-1

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

HDT Connectors

HDT1 DY CPU_DBREQ# CPU_DBRDY CPU_TCK CPU_TMS CPU_TDI CPU_TRST# CPU_TDO +1.5V_SUS CPU_R_LDT_RST# 1.5V R1038 DY 0R2J-2-GP HDT_RST# 3.3V SMC-CONN26A-FP

+1.5V_SUS R1026 1KR2J-1-GP CPU_TEST27 R1029 DY 300R2J-4-GP

TP1001 TP_CPU_VDDIO_SUS_FB_H TP1002 TP_CPU_VDDIO_SUS_FB_L TP1003 TP_CPU_TEST28_H TP1004 TP_CPU_TEST28_L TP1005 TP_CPU_TEST17 TP1006 TP_CPU_TEST16 TP1007 TP_CPU_TEST15 TP1008 TP_CPU_TEST14 TP1009 TP_CPU_TEST8 TP1010 TP_CPU_TEST7 TP1011

+1.5V_SUS 9/22 RN1005 SRN1KJ-7-GP 2K2R2J-2-GP R1032 11/6 1KR2J-1-GP R1033

(21) CPU_SIC CPU_SIC (21) CPU_SID CPU_SID (21,39) TALERT# CPU_ALERT# Q1001 PMBS3904-1-GP

11/11 +KBC_PWR +1.5V_RUN 8K2R2J-3-GP DY R1027 2K2R2J-2-GP R1028 (21,37,39,42,82) H_THERMTRIP# CPU_THERMTRIP# Q1002 PMBS3904-1-GP

1229-1 +3.3V_RUN +1.5V_RUN 8K2R2J-3-GP R1040 2K2R2J-2-GP R1039 (37) CPU_PROCHOT#_EC CPU_PROCHOT# Q1005 PMBS3904-1-GP

For old HDT tool (3.3V level) +3.3V_RUN +1.8V_RUN 10K2J-3-GP DY R1037 2K2R2J-2-GP DY R1036 HDT_RST# HDT_RST_R# Q1004 PMBS3904-1-GP

+3.3V_RUN +1.8V_RUN 10K2J-3-GP R1034 2K2R2J-2-GP R1035 Q1003 PMBS3904-1-GP (47) CPU_PWRGD_SVID_REG CPU_R_LDT_PWRGD R1041 DY 0R2J-2-GP 0112-2

WWW.AliSaler.Com

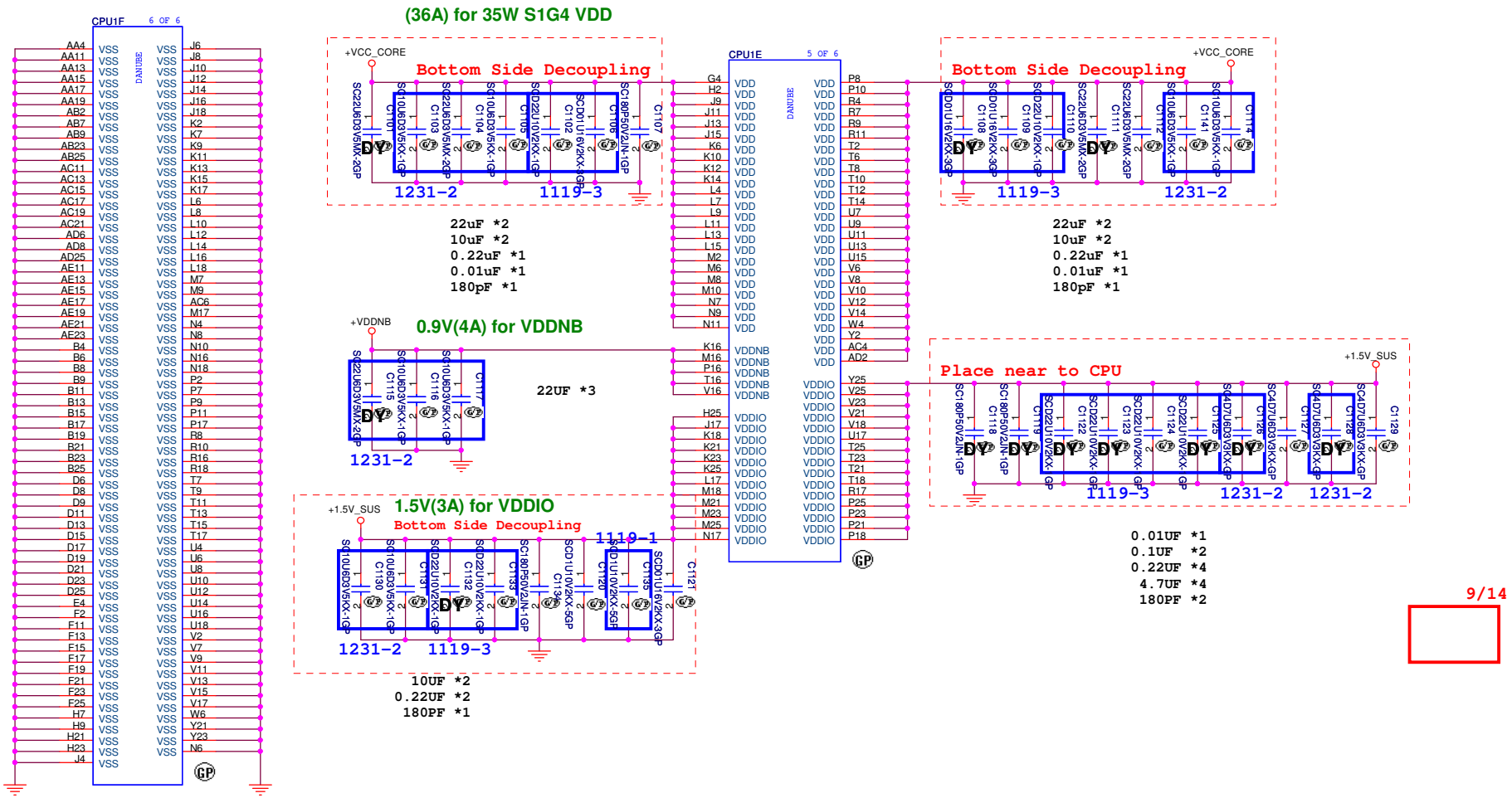
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00
Date: Thursday, March 04, 2010 | Sheet 10 of 95

WWW.AliSaler.Com

SSID = CPU



9/14

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 11 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = N.B

RS880M : 71.RS880.M05

U1A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

(8) HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0 (8)
(8) HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0 (8)
(8) HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1 (8)
(8) HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1 (8)
(8) HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2 (8)
(8) HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2 (8)
(8) HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3 (8)
(8) HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3 (8)
(8) HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4 (8)
(8) HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4 (8)
(8) HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5 (8)
(8) HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5 (8)
(8) HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6 (8)
(8) HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6 (8)
(8) HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7 (8)
(8) HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7 (8)
(8) HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8 (8)
(8) HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8 (8)
(8) HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9 (8)
(8) HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9 (8)
(8) HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10 (8)
(8) HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10 (8)
(8) HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11 (8)
(8) HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11 (8)
(8) HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12 (8)
(8) HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12 (8)
(8) HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13 (8)
(8) HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13 (8)
(8) HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14 (8)
(8) HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14 (8)
(8) HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15 (8)
(8) HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15 (8)
(8) HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0 (8)
(8) HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0 (8)
(8) HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1 (8)
(8) HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1 (8)
(8) HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0 (8)
(8) HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0 (8)
(8) HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1 (8)
(8) HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1 (8)
	C23	HT_RXCALP	HT_TXCALP	B24	
	A24	HT_RXCALN	HT_TXCALN	B25	

RS880M-1-GP

R1201 1 — 301R2F-GP — HT_RXCALP, HT_RXCALN

R1202 1 — 301R2F-GP — HT_TXCALP, HT_TXCALN

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

PCIE_NTX_GRX_P[12..15] — PCIE_NTX_GRX_P[12..15] (57)

PCIE_NTX_GRX_N[12..15] — PCIE_NTX_GRX_N[12..15] (57)

PCIE_NTX_GRX_P[0..11] — PCIE_NTX_GRX_P[0..11] (80)

PCIE_NTX_GRX_N[0..11] — PCIE_NTX_GRX_N[0..11] (80)

PCIE_NRX_GTX_P[0..15] — PCIE_NRX_GTX_P[0..15] (80)

PCIE_NRX_GTX_N[0..15] — PCIE_NRX_GTX_N[0..15] (80)

U1B

PART 2 OF 6

PCIE I/F GFX

LANE REVERSAL

9/15

PCIE_NRX_GTX_P15	D4	GFX_RX0P	GFX_TX0P	A5	PCIE_NTX_GRX_C_P15	C1231 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P15
PCIE_NRX_GTX_N15	C4	GFX_RX0N	GFX_TX0N	B5	PCIE_NTX_GRX_C_N15	C1232 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N15
PCIE_NRX_GTX_P14	A3	GFX_RX1P	GFX_TX1P	A4	PCIE_NTX_GRX_C_P14	C1229 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P14
PCIE_NRX_GTX_N14	B3	GFX_RX1N	GFX_TX1N	B4	PCIE_NTX_GRX_C_N14	C1230 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N14
PCIE_NRX_GTX_P13	C2	GFX_RX2P	GFX_TX2P	C3	PCIE_NTX_GRX_C_P13	C1227 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P13
PCIE_NRX_GTX_N13	C1	GFX_RX2N	GFX_TX2N	B2	PCIE_NTX_GRX_C_N13	C1228 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N13
PCIE_NRX_GTX_P12	E5	GFX_RX3P	GFX_TX3P	D1	PCIE_NTX_GRX_C_P12	C1225 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P12
PCIE_NRX_GTX_N12	F5	GFX_RX3N	GFX_TX3N	D2	PCIE_NTX_GRX_C_N12	C1226 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N12
PCIE_NRX_GTX_P11	G5	GFX_RX4P	GFX_TX4P	F2	PCIE_NTX_GRX_C_P11	C1223 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P11
PCIE_NRX_GTX_N11	G6	GFX_RX4N	GFX_TX4N	E1	PCIE_NTX_GRX_C_N11	C1224 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N11
PCIE_NRX_GTX_P10	H5	GFX_RX5P	GFX_TX5P	F4	PCIE_NTX_GRX_C_P10	C1221 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P10
PCIE_NRX_GTX_N10	H6	GFX_RX5N	GFX_TX5N	F3	PCIE_NTX_GRX_C_N10	C1222 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N10
PCIE_NRX_GTX_P9	J6	GFX_RX6P	GFX_TX6P	F1	PCIE_NTX_GRX_C_P9	C1219 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P9
PCIE_NRX_GTX_N9	J5	GFX_RX6N	GFX_TX6N	F2	PCIE_NTX_GRX_C_N9	C1220 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N9
PCIE_NRX_GTX_P8	J7	GFX_RX7P	GFX_TX7P	H4	PCIE_NTX_GRX_C_P8	C1217 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P8
PCIE_NRX_GTX_N8	J8	GFX_RX7N	GFX_TX7N	H3	PCIE_NTX_GRX_C_N8	C1218 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N8
PCIE_NRX_GTX_P7	L5	GFX_RX8P	GFX_TX8P	H1	PCIE_NTX_GRX_C_P7	C1215 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P7
PCIE_NRX_GTX_N7	L6	GFX_RX8N	GFX_TX8N	H2	PCIE_NTX_GRX_C_N7	C1216 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N7
PCIE_NRX_GTX_P6	M8	GFX_RX9P	GFX_TX9P	J2	PCIE_NTX_GRX_C_P6	C1213 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P6
PCIE_NRX_GTX_N6	L8	GFX_RX9N	GFX_TX9N	J1	PCIE_NTX_GRX_C_N6	C1214 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N6
PCIE_NRX_GTX_P5	P7	GFX_RX10P	GFX_TX10P	K4	PCIE_NTX_GRX_C_P5	C1211 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P5
PCIE_NRX_GTX_N5	M7	GFX_RX10N	GFX_TX10N	K3	PCIE_NTX_GRX_C_N5	C1212 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N5
PCIE_NRX_GTX_P4	P5	GFX_RX11P	GFX_TX11P	K1	PCIE_NTX_GRX_C_P4	C1209 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P4
PCIE_NRX_GTX_N4	M5	GFX_RX11N	GFX_TX11N	K2	PCIE_NTX_GRX_C_N4	C1210 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N4
PCIE_NRX_GTX_P3	R8	GFX_RX12P	GFX_TX12P	M4	PCIE_NTX_GRX_C_P3	C1207 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P3
PCIE_NRX_GTX_N3	P8	GFX_RX12N	GFX_TX12N	M3	PCIE_NTX_GRX_C_N3	C1208 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N3
PCIE_NRX_GTX_P2	R6	GFX_RX13P	GFX_TX13P	M1	PCIE_NTX_GRX_C_P2	C1205 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P2
PCIE_NRX_GTX_N2	R5	GFX_RX13N	GFX_TX13N	M2	PCIE_NTX_GRX_C_N2	C1206 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N2
PCIE_NRX_GTX_P1	P4	GFX_RX14P	GFX_TX14P	N2	PCIE_NTX_GRX_C_P1	C1203 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P1
PCIE_NRX_GTX_N1	P3	GFX_RX14N	GFX_TX14N	N1	PCIE_NTX_GRX_C_N1	C1204 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N1
PCIE_NRX_GTX_P0	T4	GFX_RX15P	GFX_TX15P	P1	PCIE_NTX_GRX_C_P0	C1201 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_P0
PCIE_NRX_GTX_N0	T3	GFX_RX15N	GFX_TX15N	P2	PCIE_NTX_GRX_C_N0	C1202 1	SCD1U10V2KX-5GP	PCIE_NTX_GRX_N0

1119-3

9/15

9/11

WLAN
LAN
WWAN

(76) PCIE_RXP0	AF3	GPP_RX0P	GPP_TX0P	AC1	PCIE_C_TXP0	C1264 1	SCD1U10V2KX-5GP	PCIE_TXP0 (76)
(76) PCIE_RXN0	AD4	GPP_RX0N	GPP_TX0N	AC2	PCIE_C_TXN0	C1261 1	SCD1U10V2KX-5GP	PCIE_TXN0 (76)
(76) PCIE_RXP1	AE2	GPP_RX1P	GPP_TX1P	AB4	PCIE_C_TXP1	C1266 1	SCD1U10V2KX-5GP	PCIE_TXP1 (76)
(76) PCIE_RXN1	AD3	GPP_RX1N	GPP_TX1N	AB3	PCIE_C_TXN1	C1262 1	SCD1U10V2KX-5GP	PCIE_TXN1 (76)
(76) PCIE_RXP2	AD1	GPP_RX2P	GPP_TX2P	AA2	PCIE_C_TXP2	C1265 1	SCD1U10V2KX-5GP	PCIE_TXP2 (76)
(76) PCIE_RXN2	AD2	GPP_RX2N	GPP_TX2N	AA1	PCIE_C_TXN2	C1263 1	SCD1U10V2KX-5GP	PCIE_TXN2 (76)
	V5	GPP_RX3P	GPP_TX3P	Y1				
	W6	GPP_RX3N	GPP_TX3N	Y2				
	U5	GPP_RX4P	GPP_TX4P	Y4				
	U6	GPP_RX4N	GPP_TX4N	Y3				
	U8	GPP_RX5P	GPP_TX5P	V1				
	U7	GPP_RX5N	GPP_TX5N	V2				

PCIE I/F GPP

9/11

A-LINK

(20) ALINK_NBRX_SBTX_P0	AA8	SB_RX0P	SB_TX0P	AD7	ALINK_NBTX_SBRX_C_P0	C1237 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_P0 (20)
(20) ALINK_NBRX_SBTX_N0	Y8	SB_RX0N	SB_TX0N	AE7	ALINK_NBTX_SBRX_C_N0	C1238 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_N0 (20)
(20) ALINK_NBRX_SBTX_P1	AA7	SB_RX1P	SB_TX1P	AE6	ALINK_NBTX_SBRX_C_P1	C1239 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_P1 (20)
(20) ALINK_NBRX_SBTX_N1	Y7	SB_RX1N	SB_TX1N	AD6	ALINK_NBTX_SBRX_C_N1	C1240 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_N1 (20)
(20) ALINK_NBRX_SBTX_P2	AA5	SB_RX2P	SB_TX2P	AB6	ALINK_NBTX_SBRX_C_P2	C1241 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_P2 (20)
(20) ALINK_NBRX_SBTX_N2	AA6	SB_RX2N	SB_TX2N	AC6	ALINK_NBTX_SBRX_C_N2	C1242 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_N2 (20)
(20) ALINK_NBRX_SBTX_P3	W5	SB_RX3P	SB_TX3P	AD5	ALINK_NBTX_SBRX_C_P3	C1243 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_P3 (20)
(20) ALINK_NBRX_SBTX_N3	Y5	SB_RX3N	SB_TX3N	AE5	ALINK_NBTX_SBRX_C_N3	C1244 1	SCD1U10V2KX-5GP	ALINK_NBTX_SBRX_N3 (20)

PCIE I/F SB

		PCE_CALRP	AC8	PCE_PCAL	R1203 1 — 1K2R2F-L-GP
		PCE_CALRN	AB8	PCE_NCAL	R1204 1 — 2KR2F-3-GP — +1.1V_RUN_VDDPCIE

RS880M-1-GP

Place < 100mils from pin AC8 and AB8

WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_HT LINK&PCIe(1/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 12 of 95

WWW.AliSaler.Com

SSID = N.B

RS880M : 71.RS880.M05

UMA DAC Signal:
GREEN/BLUE: Connected to GND through two separate 150- 1% resistors.

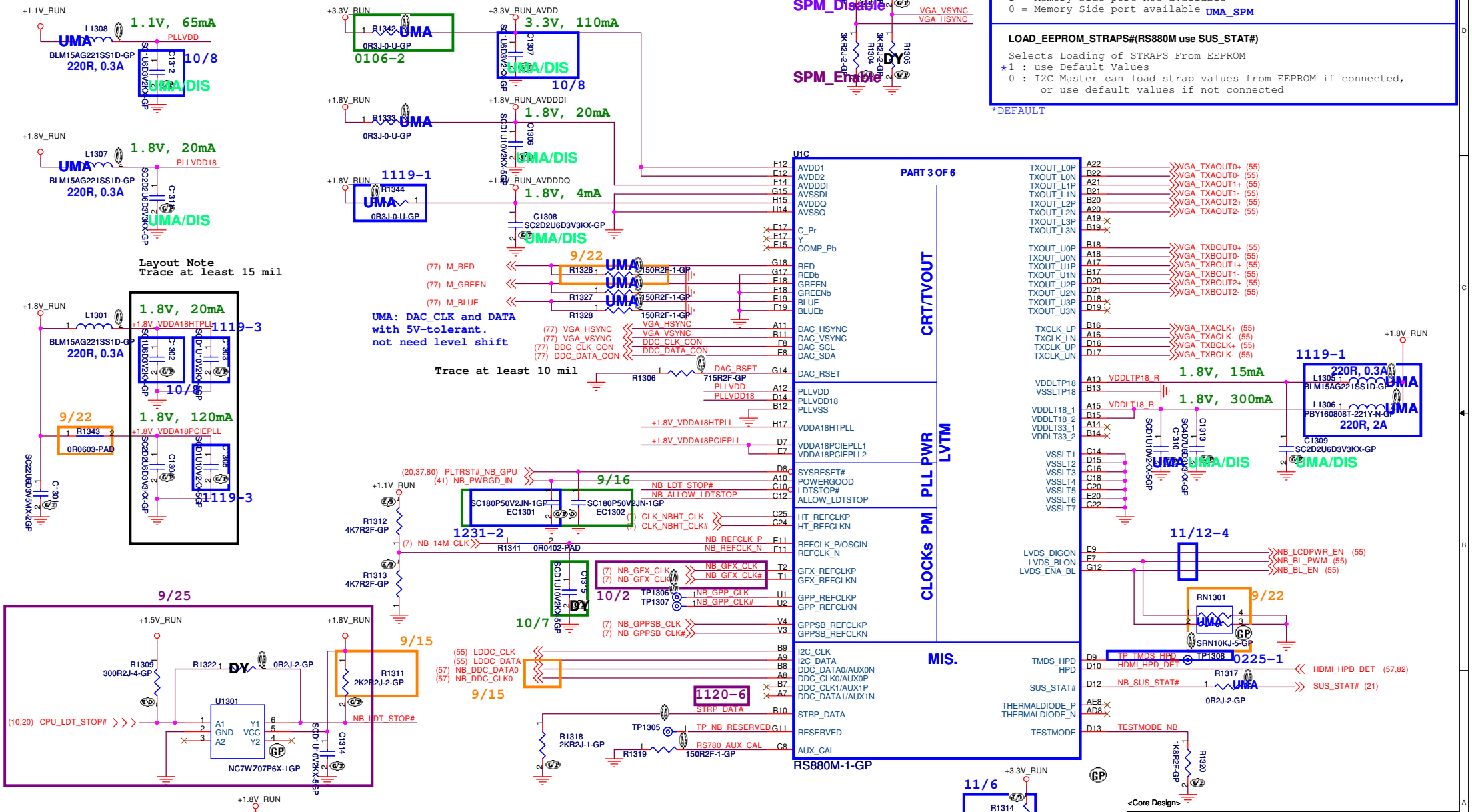
RED: Connected to GND through two separate 133- 1% resistors.(For match resistor on CRT/B 150- 1%)

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use DAC_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use DAC_HSYNC)
1 = Memory Side port Not available DIS
0 = Memory Side port available UMA_SPM

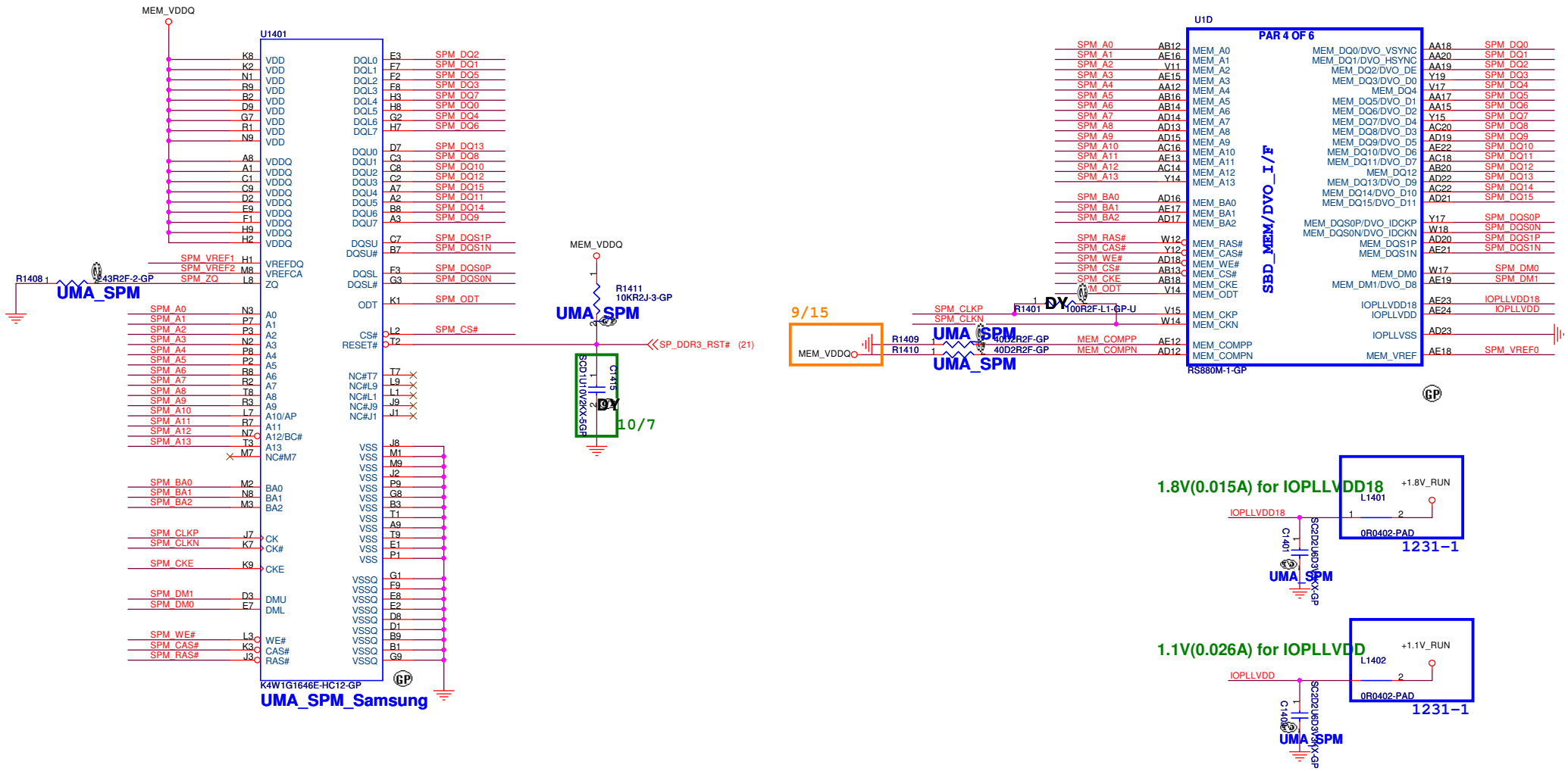
LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT


+1.1V_RUN
L1308
1.1V, 65mA
PLLVDD
UMA
BLM15AG221SS1D-GP
220R, 0.3A
10/8
UMA/DIS
+1.8V_RUN
L1307
1.8V, 20mA
PLLVDD18
+3.3V_RUN
R1342
0R3J-0-U-GP
0106-2
+3.3V_RUN_AVDD
3.3V, 110mA
+1.8V_RUN
R1333
+1.8V_RUN_AVDDDI
1.8V, 20mA
1119-1
R1344
+1.8V_RUN_AVDDDQ
1.8V, 4mA
C1308
SC2D2U6D3V3KX-GP
Layout Note
Trace at least 15 mil
L1301
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL
1119-3
9/22
R1343
0R0603-PAD
UMA: DAC_CLK and DATA with 5V-tolerant. not need level shift
Trace at least 10 mil
R1326
R1327
R1328
150R2F-1-GP
R1306
715R2F-GP
(77) M_RED
(77) M_GREEN
(77) M_BLUE
(77) VGA_HSYNC
(77) VGA_VSYNC
(77) DDC_CLK_CON
(77) DDC_DATA_CON
PART 3 OF 6
U1C
CRT/TVOUT
PLL PWR
CLOCKs PM
MIS.
LVTM
RS880M-1-GP
9/16
SC180P50V2JN-1GP
EC1301
EC1302
1231-2
R1341
0R0402-PAD
(7) NB_14M_CLK
R1312
4K7R2F-GP
R1313
4K7R2F-GP
10/2
10/7
9/25
+1.5V_RUN
R1309
300R2J-4-GP
R1322
0R2J-2-GP
R1311
2K2R2J-2-GP
9/15
U1301
NC7WZ07P6X-1GP
(10,20) CPU_LDT_STOP#
NB_LDT_STOP#
(55) LDDC_CLK
(55) LDDC_DATA
(57) NB_DDC_DATA0
(57) NB_DDC_CLK0
1120-6
STRP_DATA
TP1305
TP_NB_RESERVED
RS780_AUX_CAL
R1318
2KR2J-1-GP
R1319
150R2F-1-GP
R1315
1KR2J-1-GP
(20) ALLOW_LDTSTOP
NB_ALLOW_LDTSTOP
R1316
0R0402-PAD
ALLOW_LDTSTOP:
1 = LDTSTOP# can be asserted
0 = LDTSTOP# has to be de-asserted
+3.3V_RUN
SPM_Disable
SPM_Enable
R1302
R1303
R1304
R1305
3KR2J-2-GP
VGA_VSYNC
VGA_HSYNC
11/12-4
LVDS_DIGON
LVDS_BLON
LVDS_ENA_BL
NB_LCDPWR_EN (55)
NB_BL_PWM (55)
NB_BL_EN (55)
RN1301
SRN10KJ-5-GP
TP_TMDS_HPD
TP1308
0225-1
HDMI_HPD_DET (57,82)
R1317
0R2J-2-GP
NB_SUS_STAT#
SUS_STAT# (21)
TESTMODE_NB
R1320
1K8R2F-GP
11/6
R1314
4K7R2J-2-GP
R1321
3KR2J-2-GP
1119-1
220R, 0.3A
L1305
L1306
PBY160808T-221Y-N-GP
220R, 2A
1.8V, 15mA
1.8V, 300mA
C1309
SC2D2U6D3V3KX-GP
C1310
C1313
SC4D7U6D3V3KX-GP
SC2D2U6D3V5MX-2GP
C1307
C1306
C1305
C1304
C1314
C1315
C1316
C1317
C1318
C1319
C1320
C1321
C1322
C1323
C1324
C1325
C1326
C1327
C1328
C1329
C1330
C1331
C1332
C1333
C1334
C1335
C1336
C1337
C1338
C1339
C1340
C1341
C1342
C1343
C1344
C1345
C1346
C1347
C1348
C1349
C1350
C1351
C1352
C1353

WWW.AliSaler.Com

SSID = N.B



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

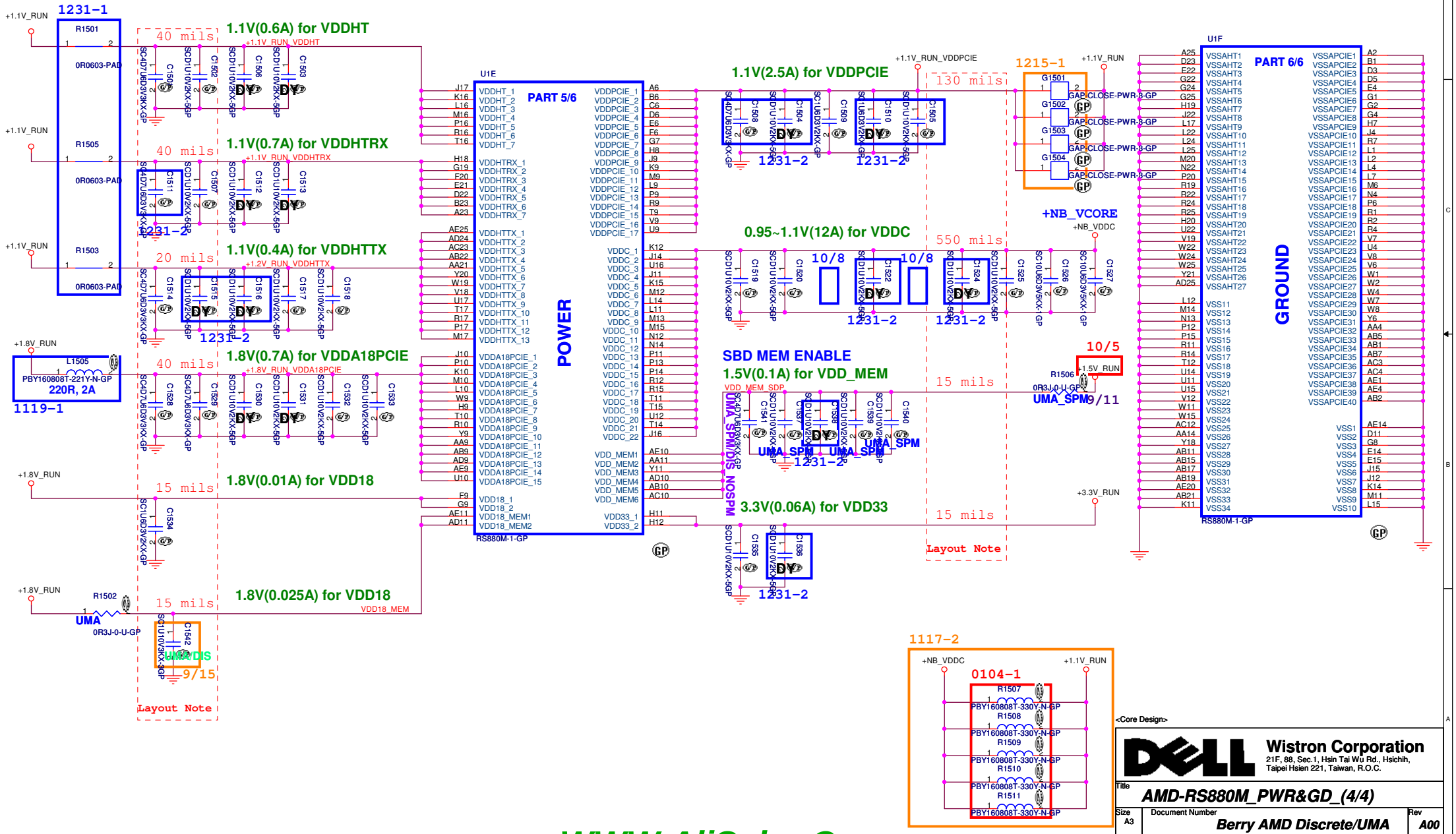
Title: AMD-RS880M_SidePort_(3/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 14 of 95

WWW.AliSaler.Com

SSID = N.B



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMD-RS880M_PWR&GD_(4/4)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 15 of 95

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 16 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

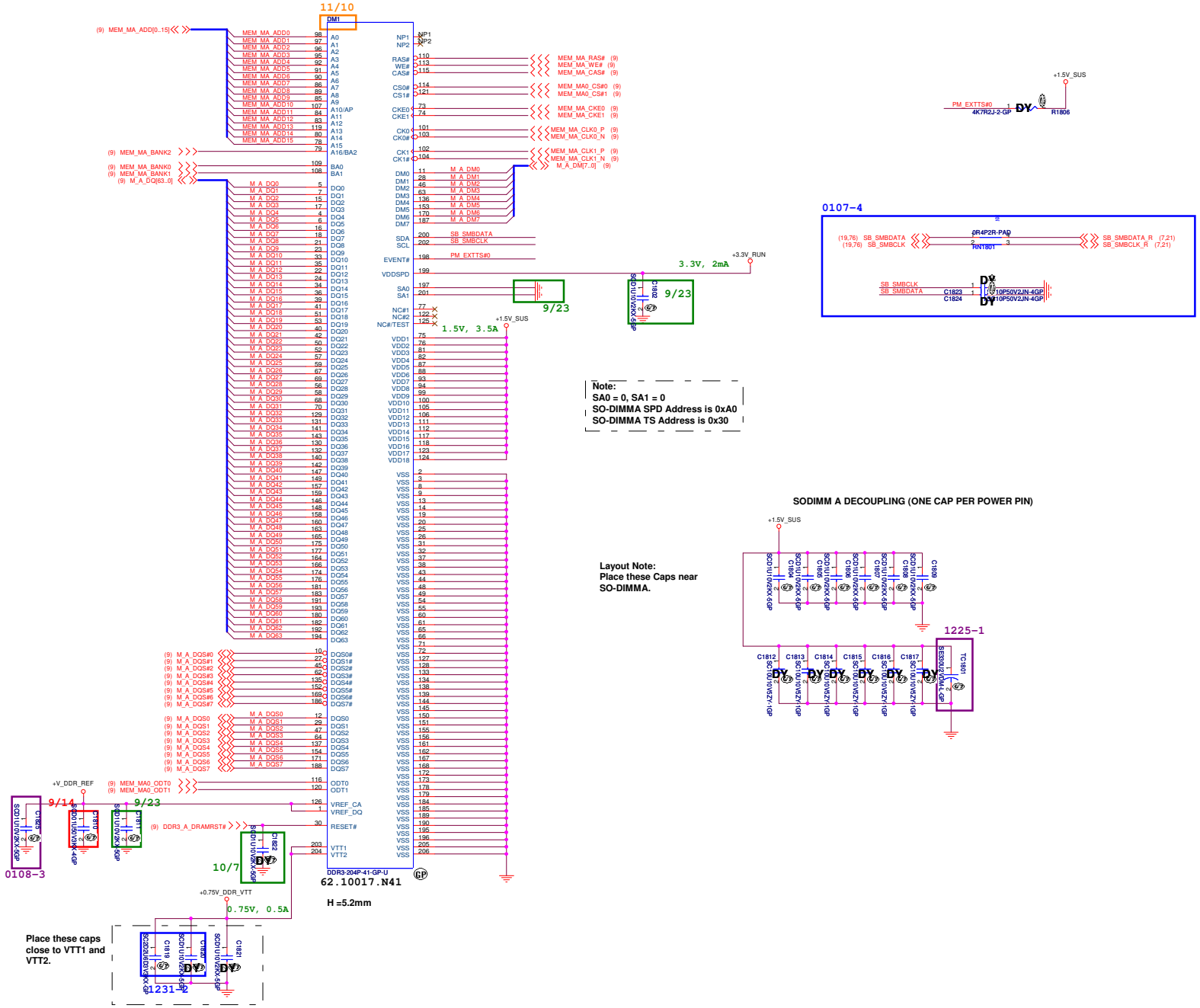
Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 17 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com



WWW.AliSaler.Com

<Core Design>

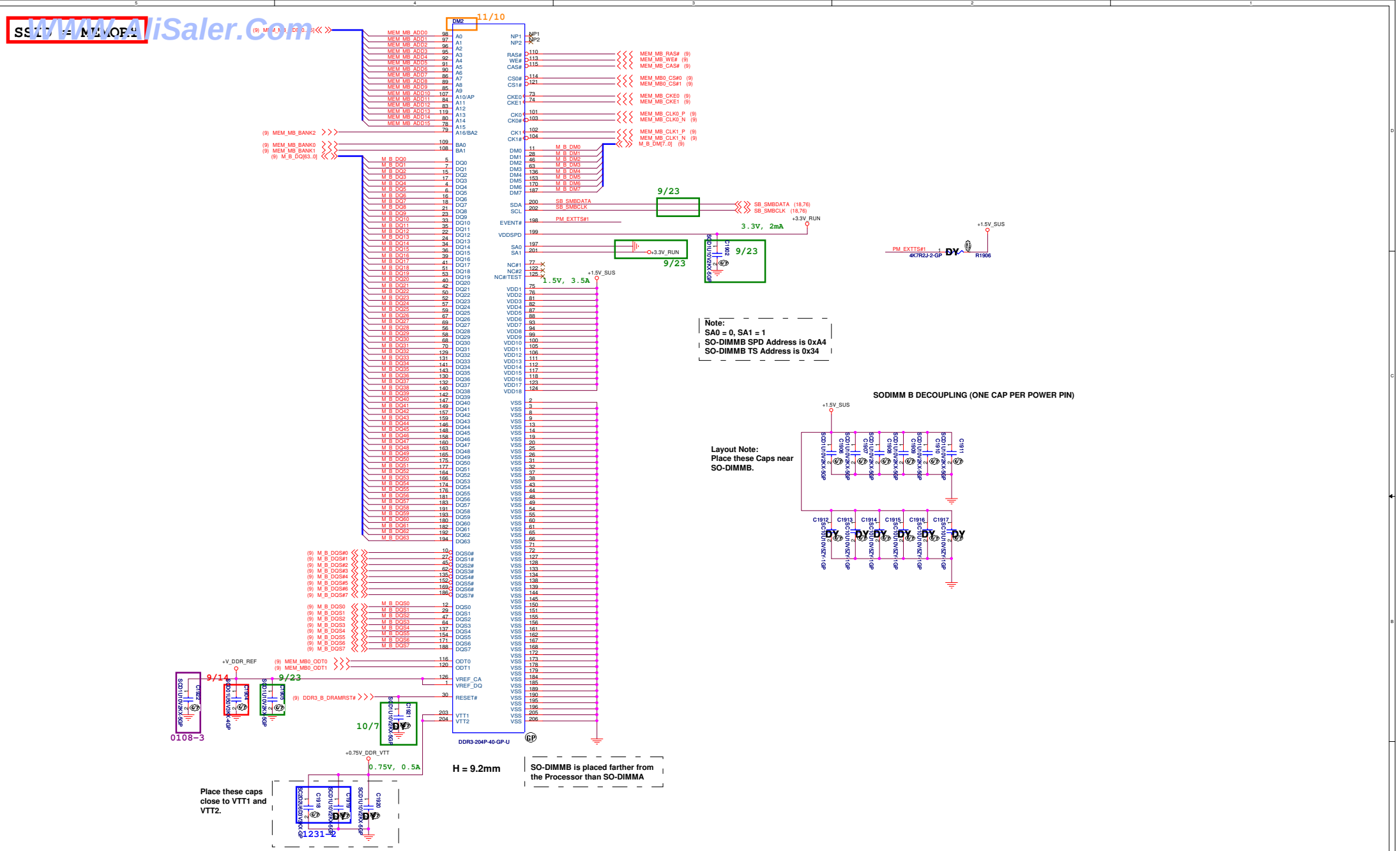
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 18 of 95

WWW.AliSaler.Com



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

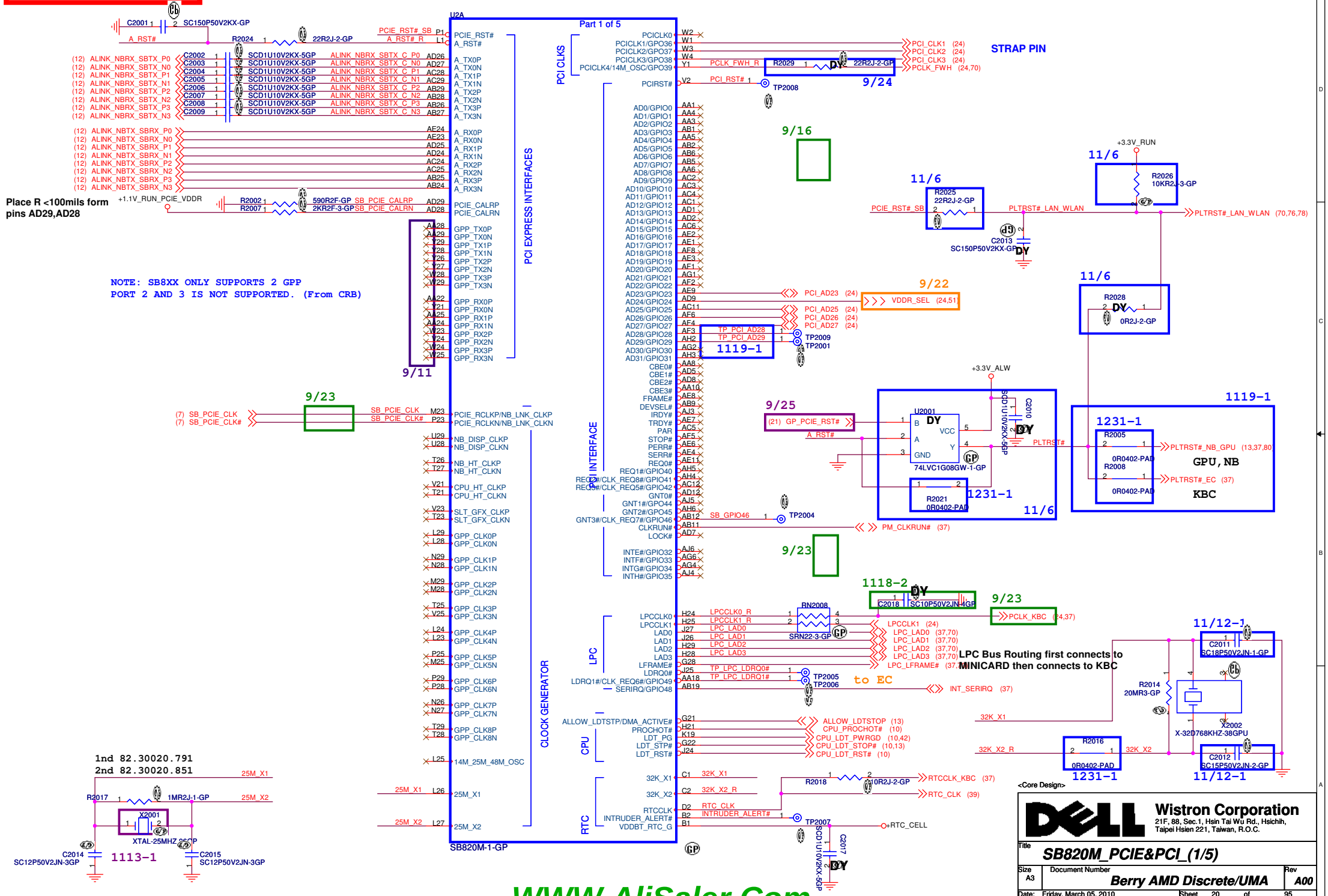
Title: DDR3-SODIMM2

Size | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 19 of 95

WWW.AliSaler.Com

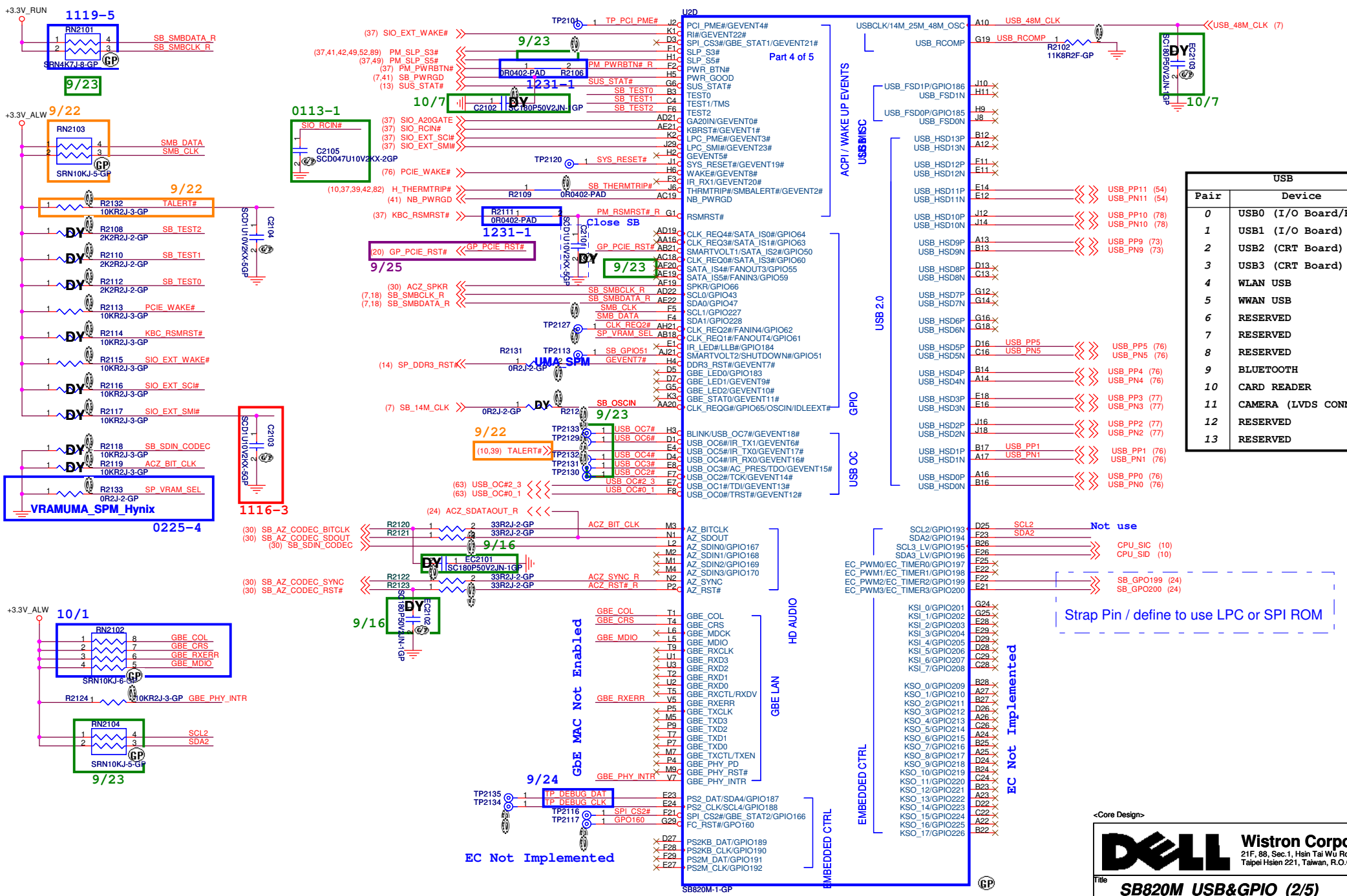
SB820M - S.B SB820M 71.SB820.M02



WWW.AliSaler.Com

WWW.AliSaler.Com

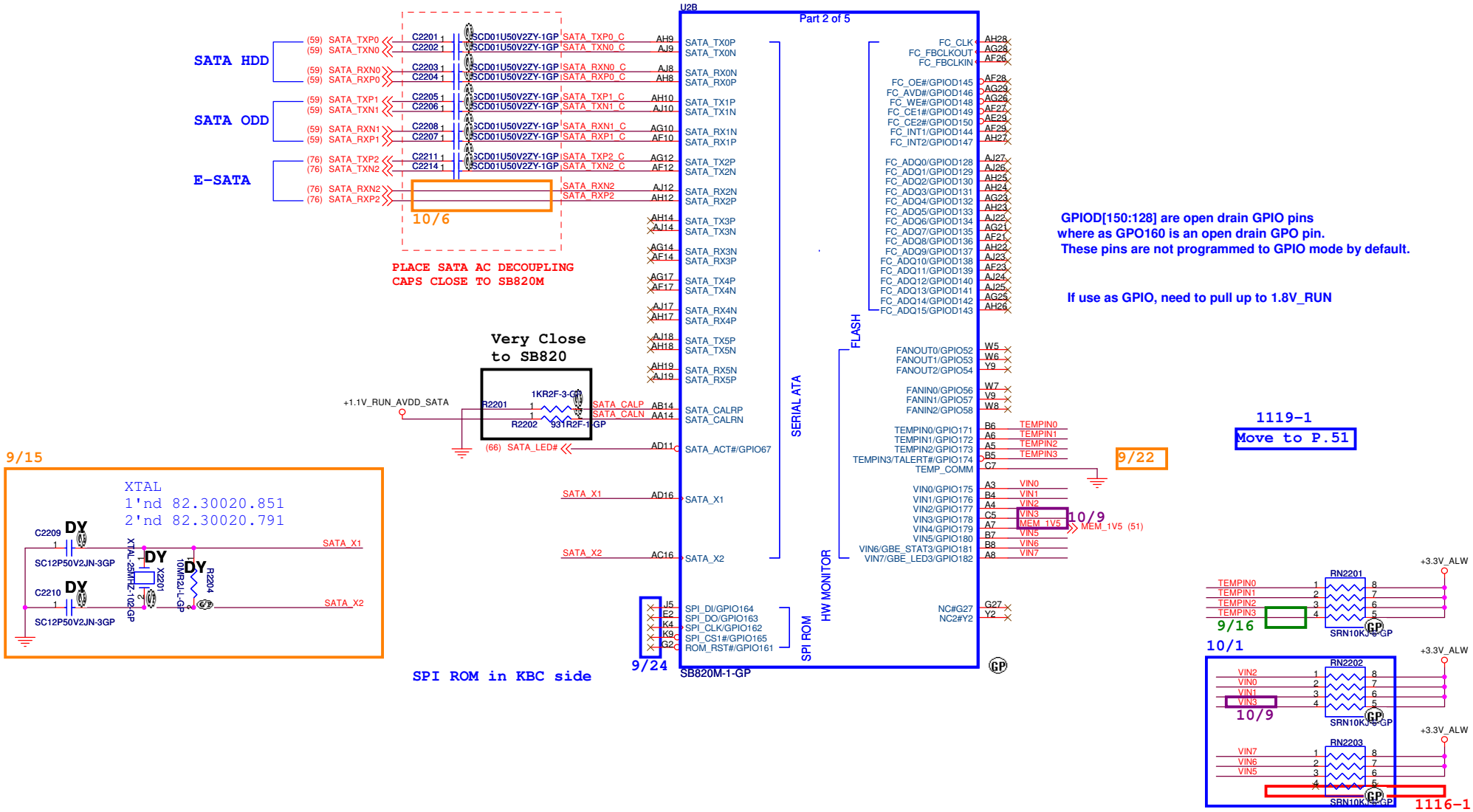
SSID = S.B



WWW.AliSaler.Com

WWW.AliSaler.Com

SS1D = S.B



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

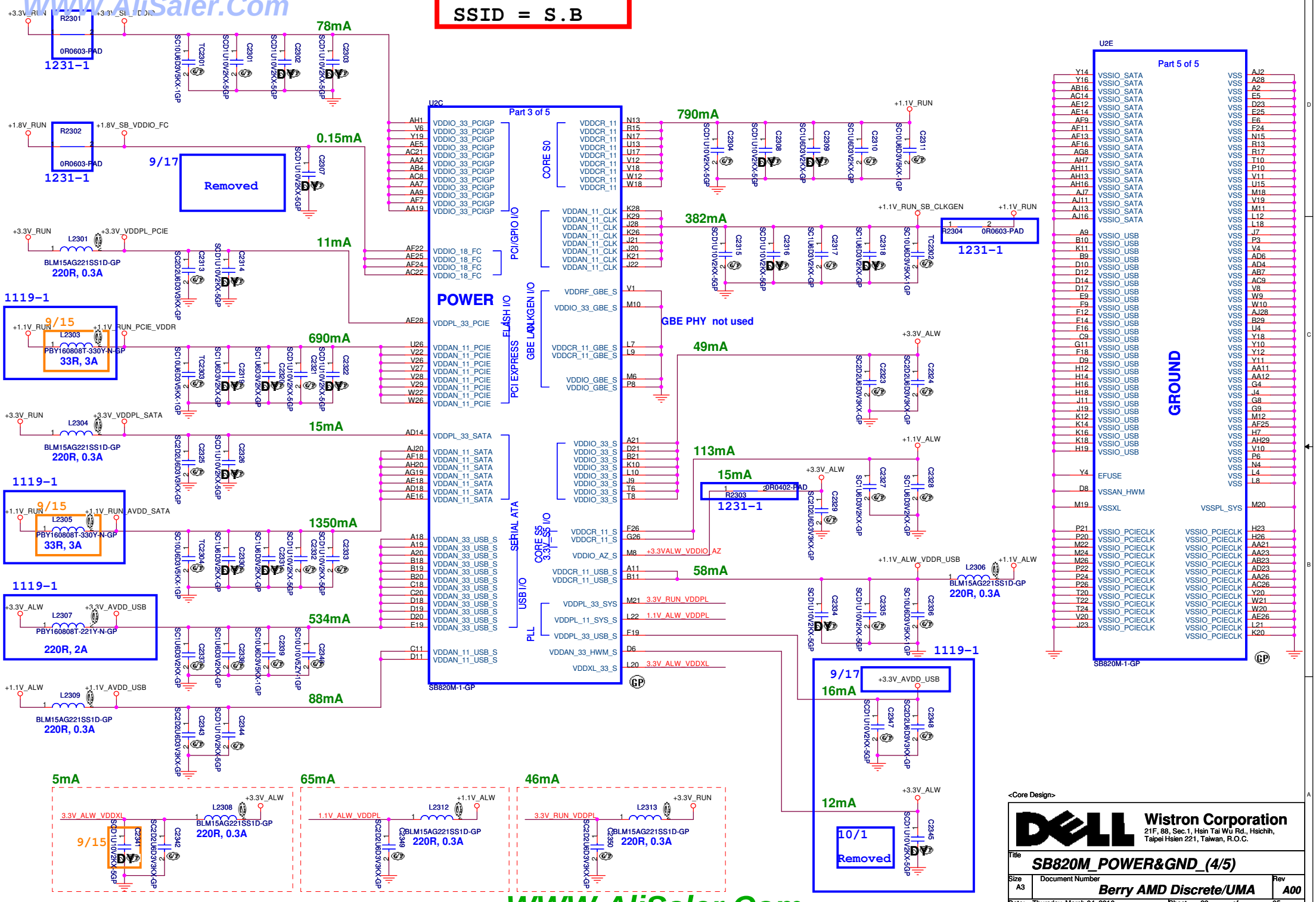
Title: SB820M_SATA-IDE_(3/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 22 of 95

WWW.AliSaler.Com

SSID = S.B



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_POWER&GND_(4/5)

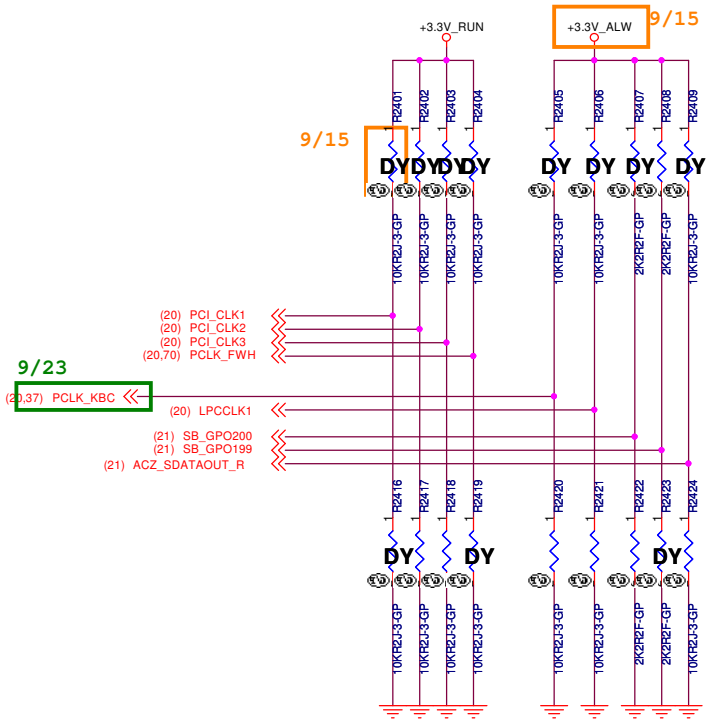
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 23 of 95

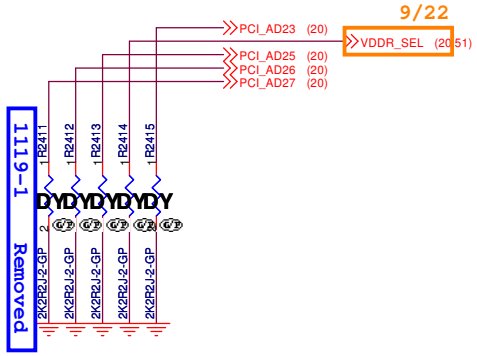
WWW.AliSaler.Com

SSID = S.B

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCLK_KBC (PCI_CLK3)	PCLK_FWH (PCI_CLK4)	LPCCLK0	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820M has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Friday, March 05, 2010 | Sheet 24 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Reserved***	
Size	Document Number: ***Berry AMD Discrete/UMA***	Rev: ***A00***
Date: Thursday, March 04, 2010	Sheet 25 of 95	

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 26 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 27 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 28 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

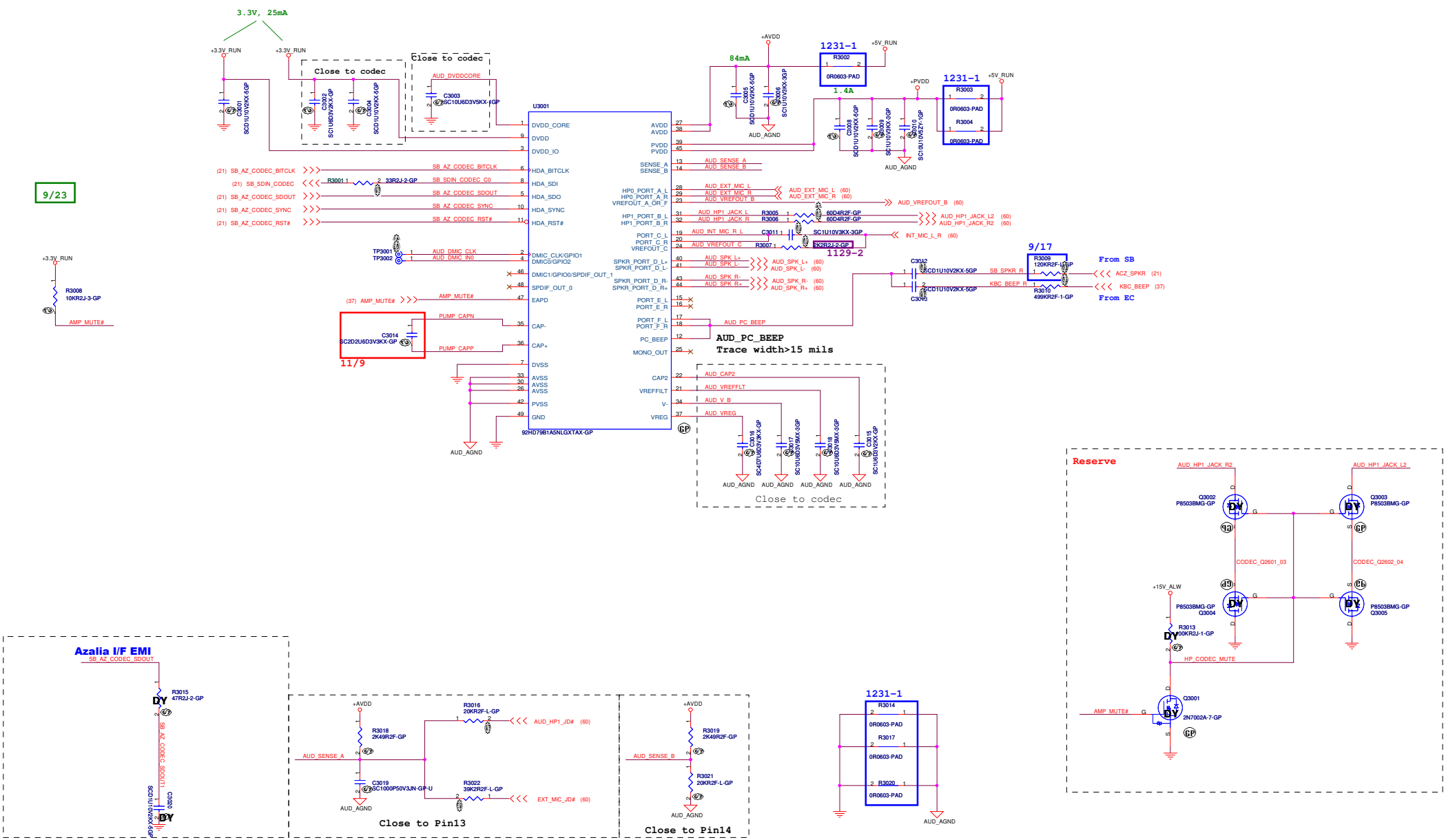
Date: Thursday, March 04, 2010 Sheet 29 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = AUDIO

9/23



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD79B1

Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 30 of 95

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 31 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 | Sheet 32 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 33 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 34 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 35 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 36 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = KBC

CAP close to VCC-GND pin pair

3.3V, 2mA

3.3V, 23mA

U3701A

NPCE781BA0DX-GP

A/D, D/A, LPC, SMB, SP, SPI, SER/IR, GPIO

Reserved

PD for Berry Keyboard Matrix
PU for DJ Keyboard Matrix

PU for Discrete
Internal PL for UMA

9/14

Remove reserved crystal.

MB VERSION			
ID	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

KBC CLK
EMI

U3701B

NPCE781BA0DX-GP

KBC

PS/2

FIU

Internal PU

WWW.AliSaler.Com

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Friday, March 05, 2010 | Sheet 37 of 95

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

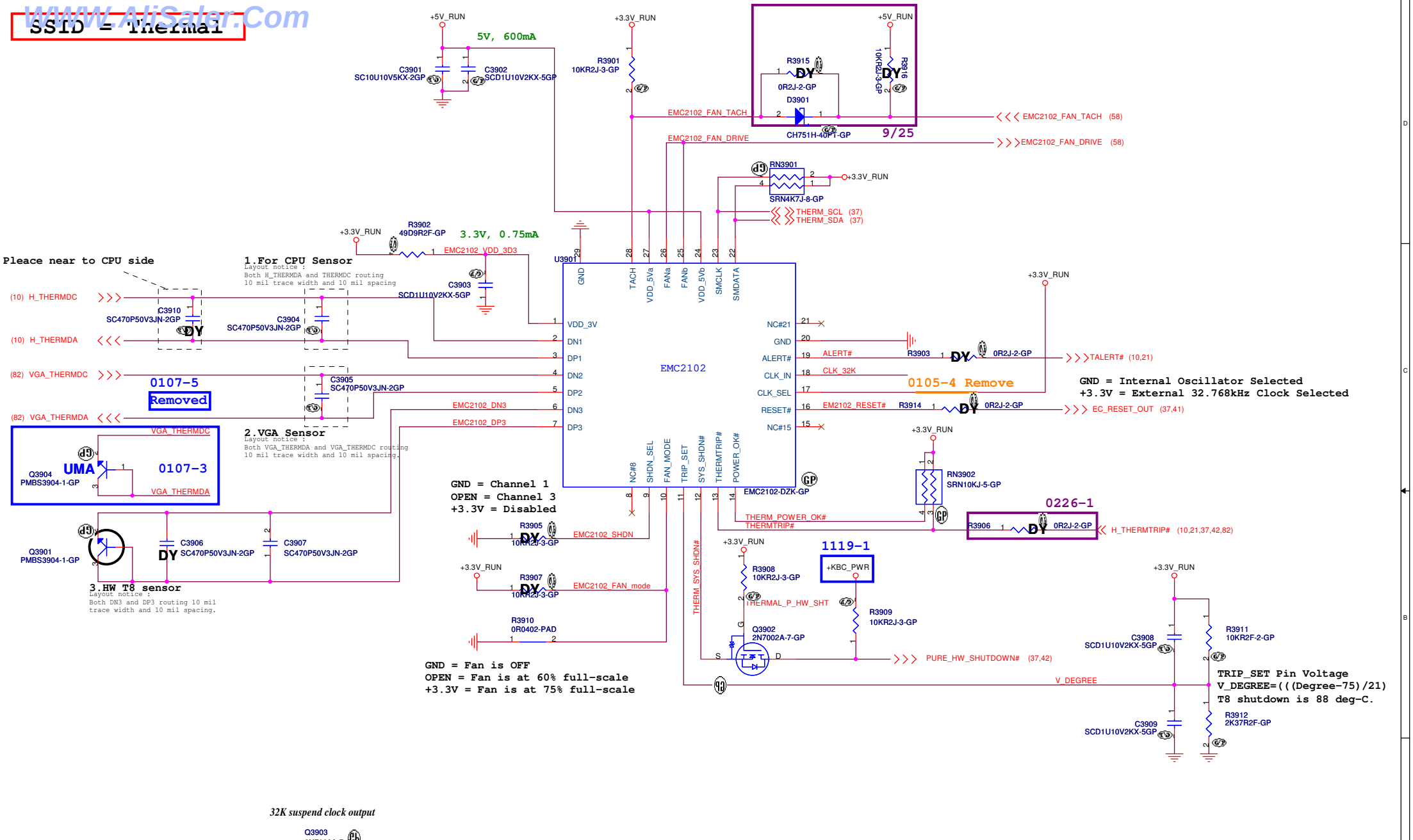
Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 | Sheet 38 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = Thermal



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 39 of 95

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

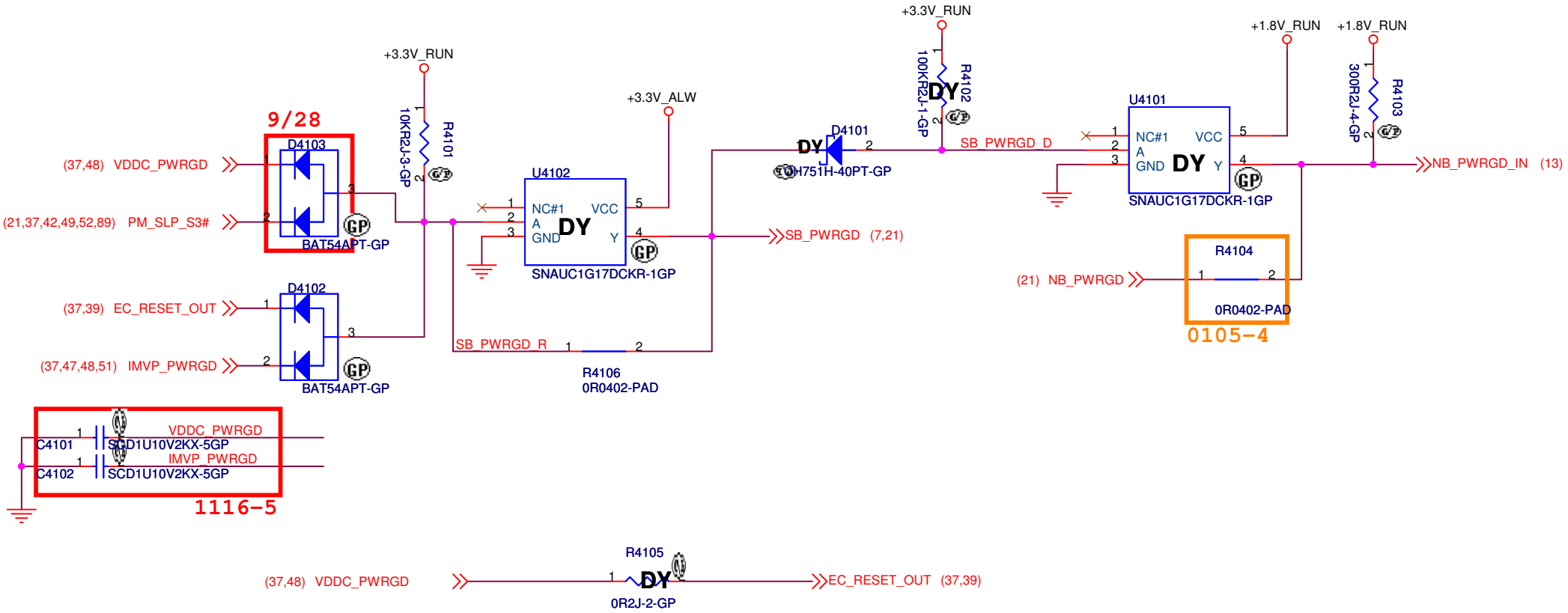
Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 40 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = Reset.Suspend



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power On Logic***

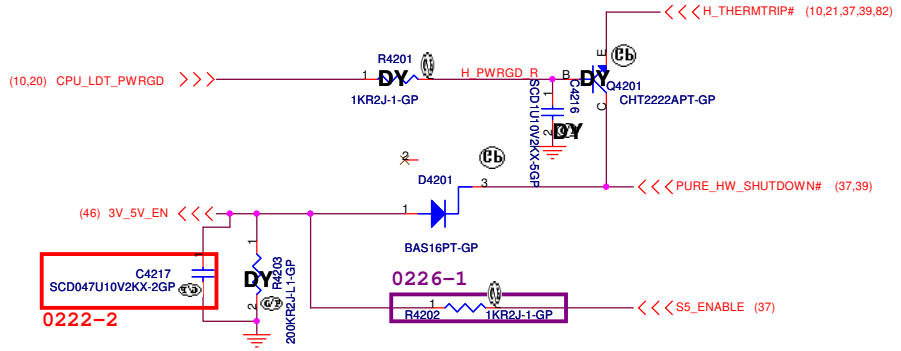
Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 41 of 95

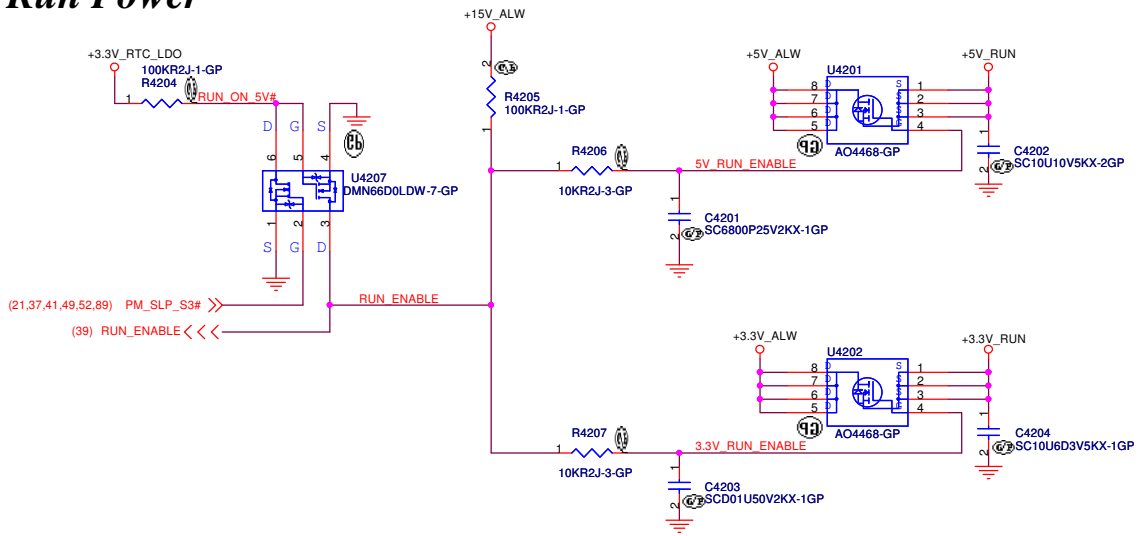
WWW.AliSaler.Com

WWW.AliSaler.Com

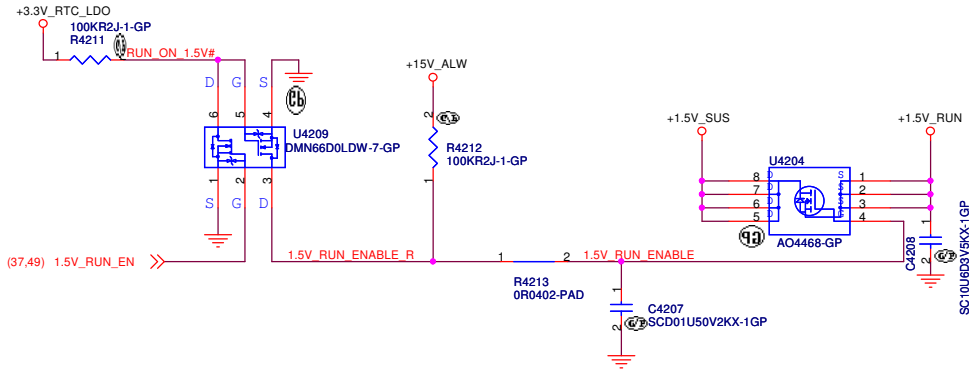
SSID = Reset.Suspend

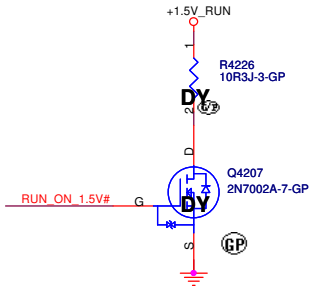


Run Power



1117-2
Remove





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 42 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

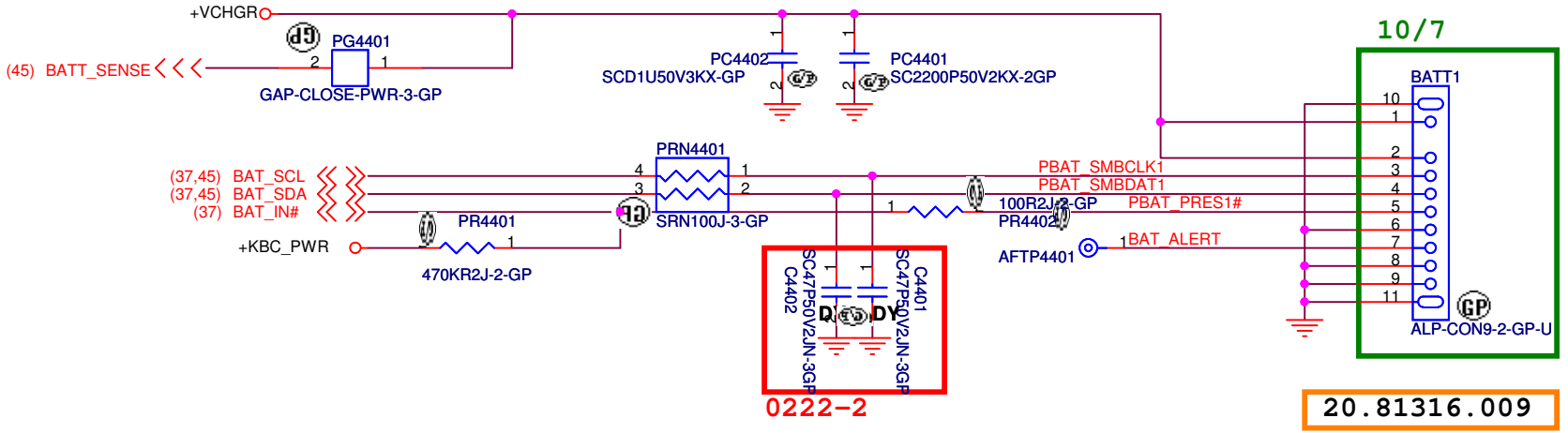
Date: Thursday, March 04, 2010 Sheet 43 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

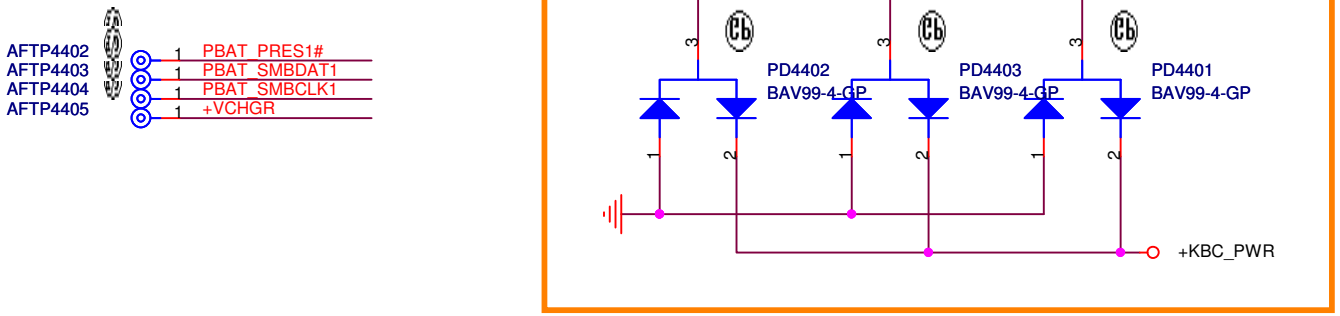
SSID = BATT CONN

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

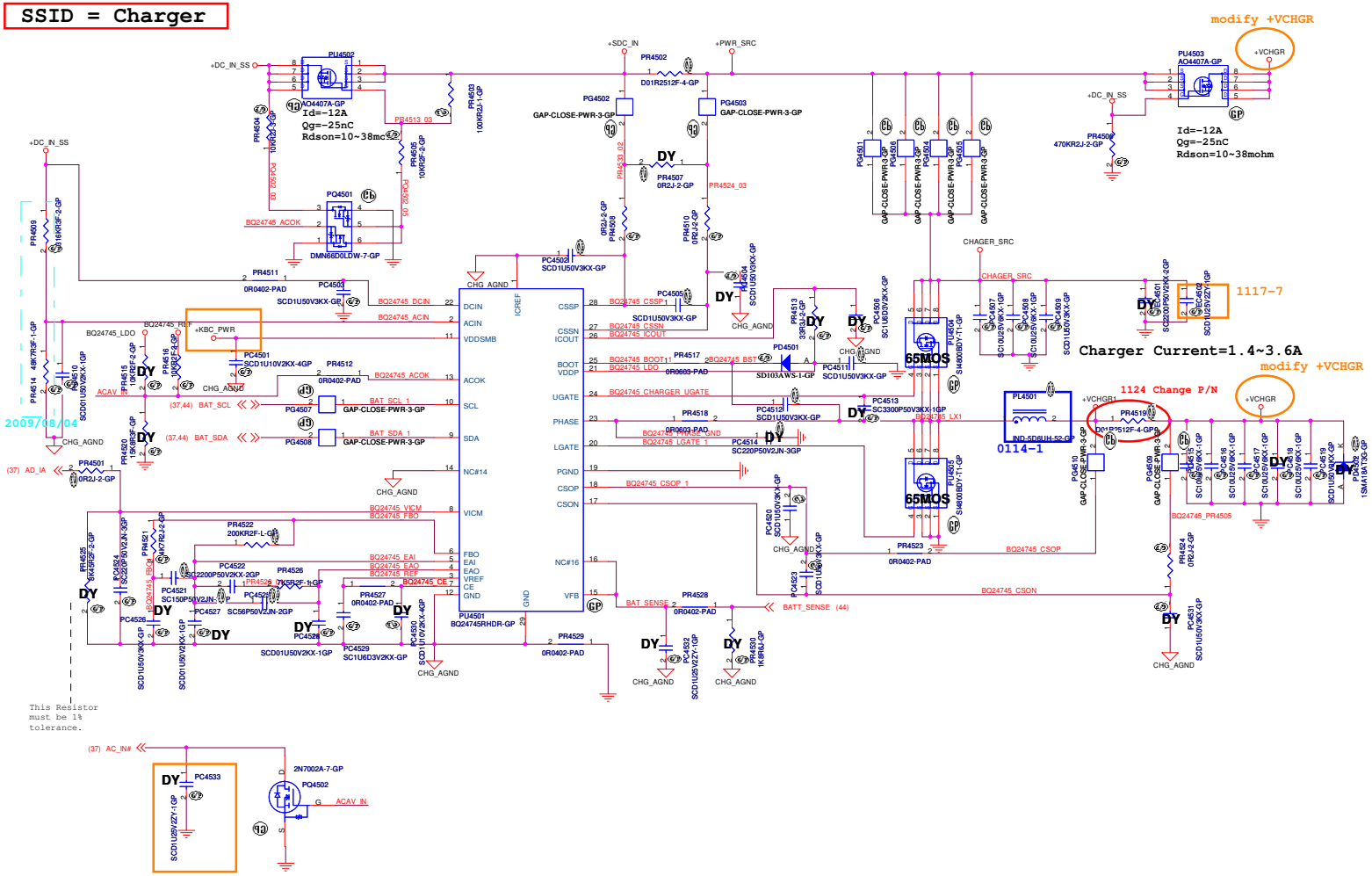
Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 44 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = Charger



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

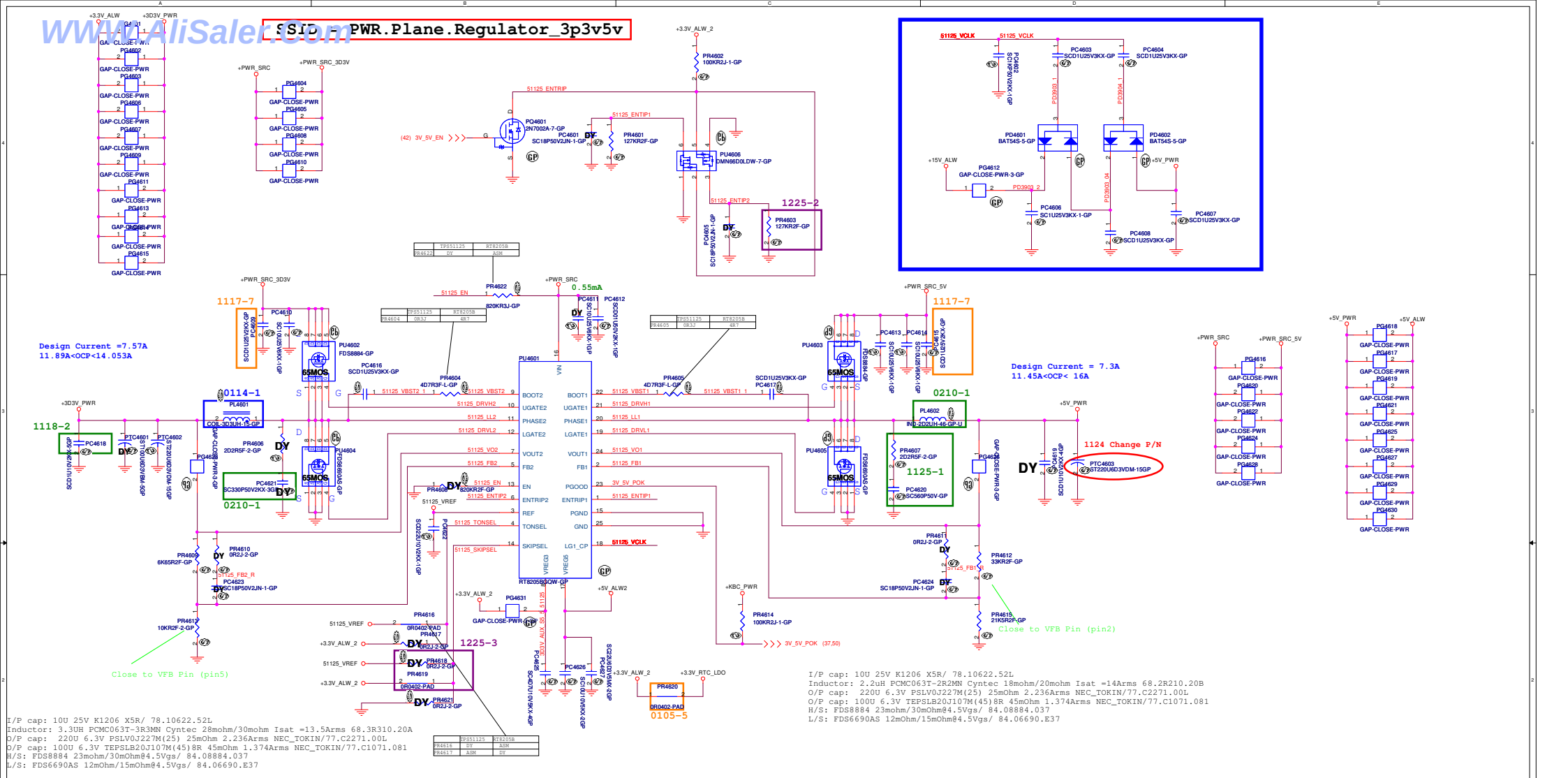
Title: CHARGER BQ24745

Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Monday, March 08, 2010 | Sheet 45 of 95

WWW.AliSaler.Com

SSID - PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.E37

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8208BGQW	74.08208.A73

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

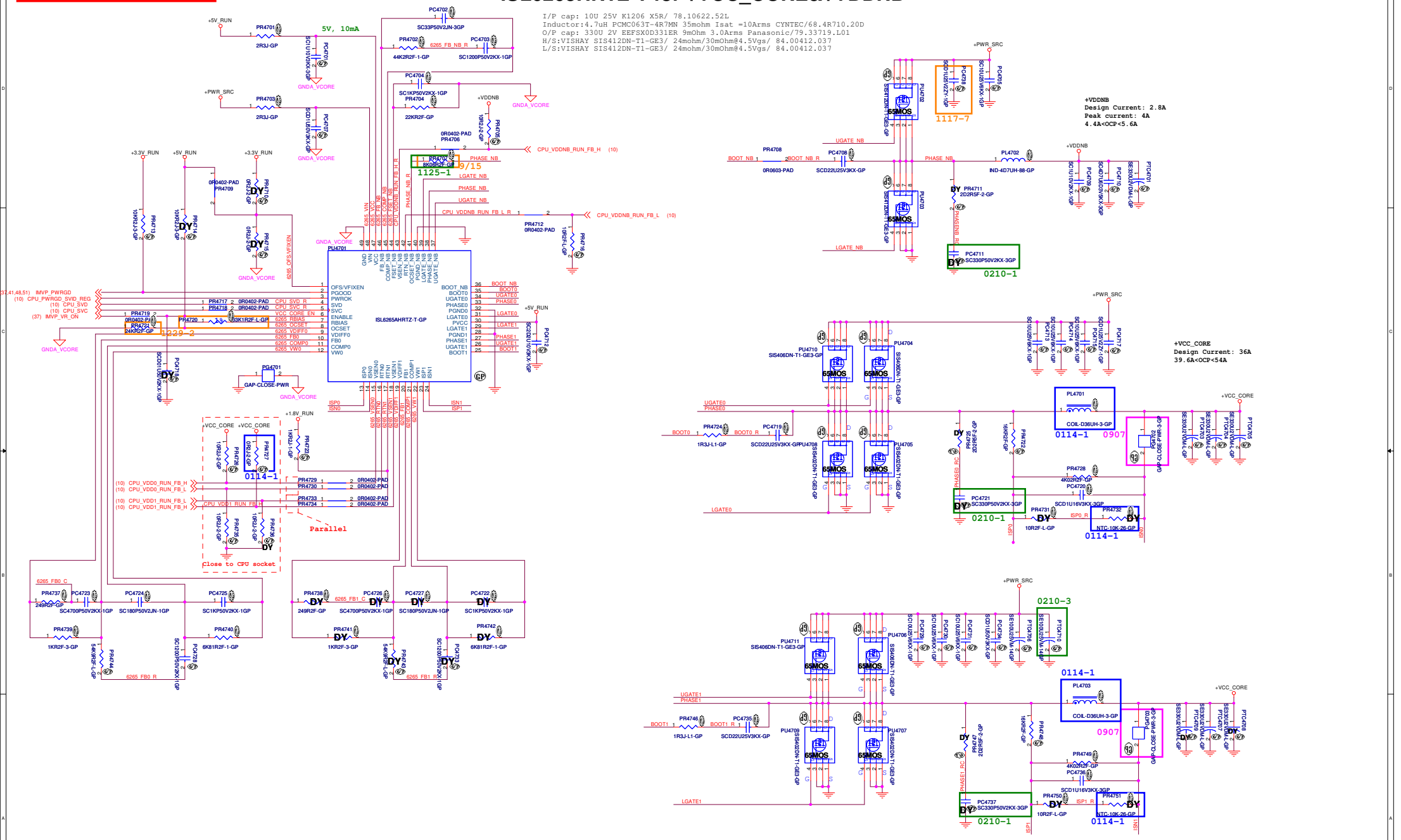
Size: A2 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 46 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

ISL6265HRTZ-T for +VCC_CORE&+VDDNB



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
A2	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 47 of 95

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_+1.1V_RUN

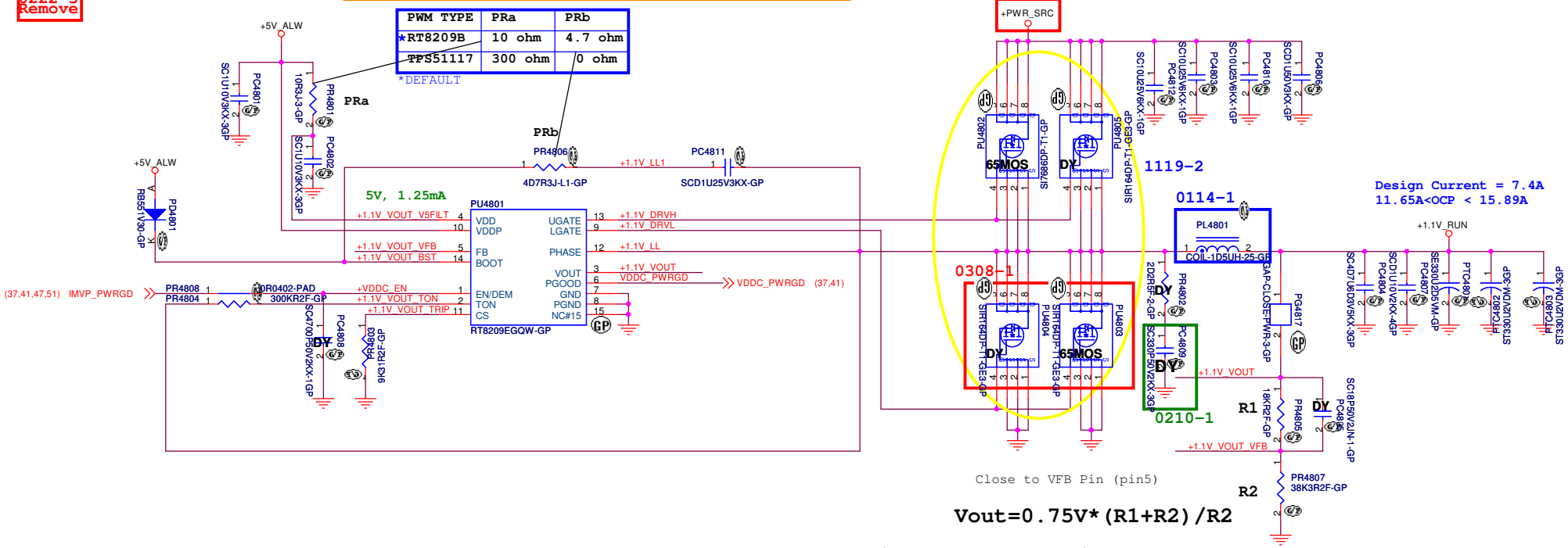
1117-2

RT8209EGQW for +1.1V_RUN

0222-3 Remove

PWM TYPE	PRa	PRb
*RT8209B	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT



$$Vout=0.75V*(R1+R2)/R2$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN 33Arms CYNTEC/ 68.1R510.10J
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E_+1.1V_RUN

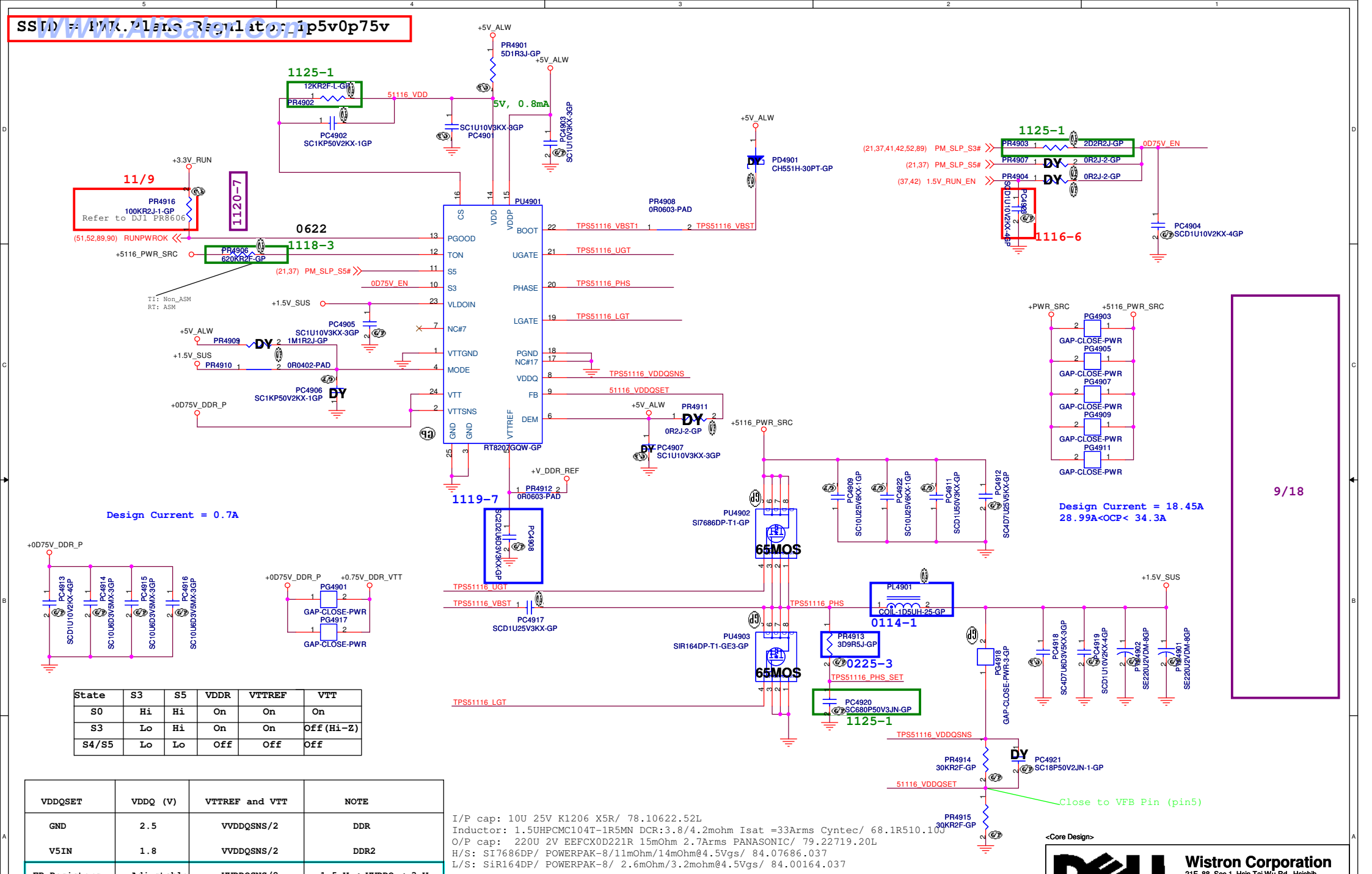
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Monday, March 08, 2010 | Sheet 48 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator.1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207_+1.5V_SUS

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 49 of 95

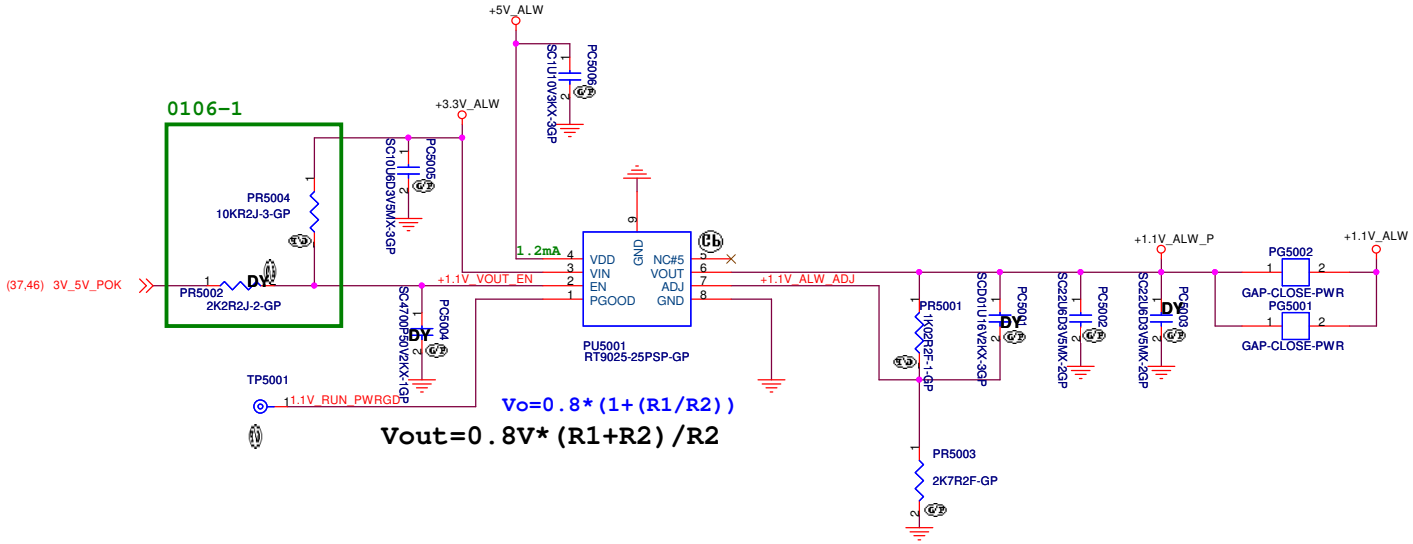
WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_+1.1V_ALW

1117-2

RT9025 for +1.1V_ALW



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_+1.1V_ALW

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

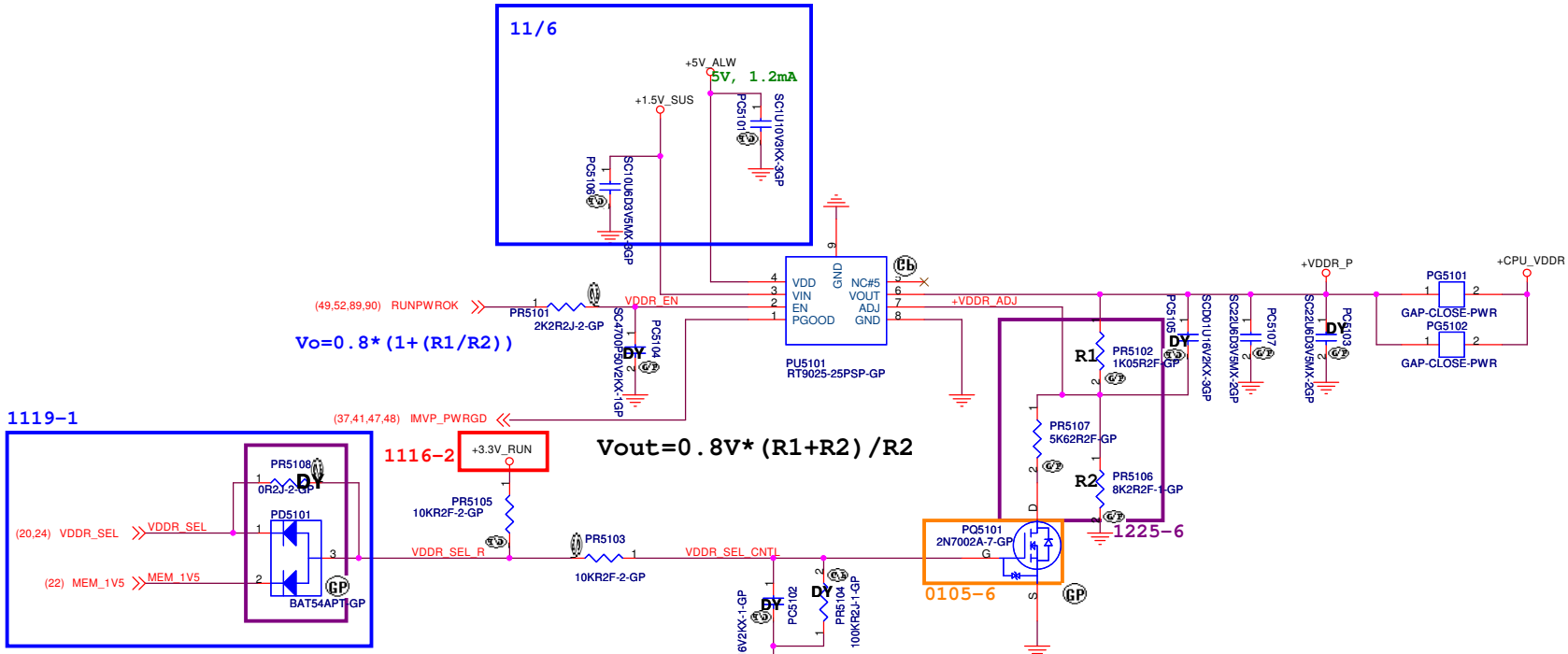
Date: Thursday, March 04, 2010 | Sheet 59 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



+1.5V_RUN +/- 5%
Design Current: 0.805A
Peak current 1.15A

VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

10/2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025 +VDDR

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

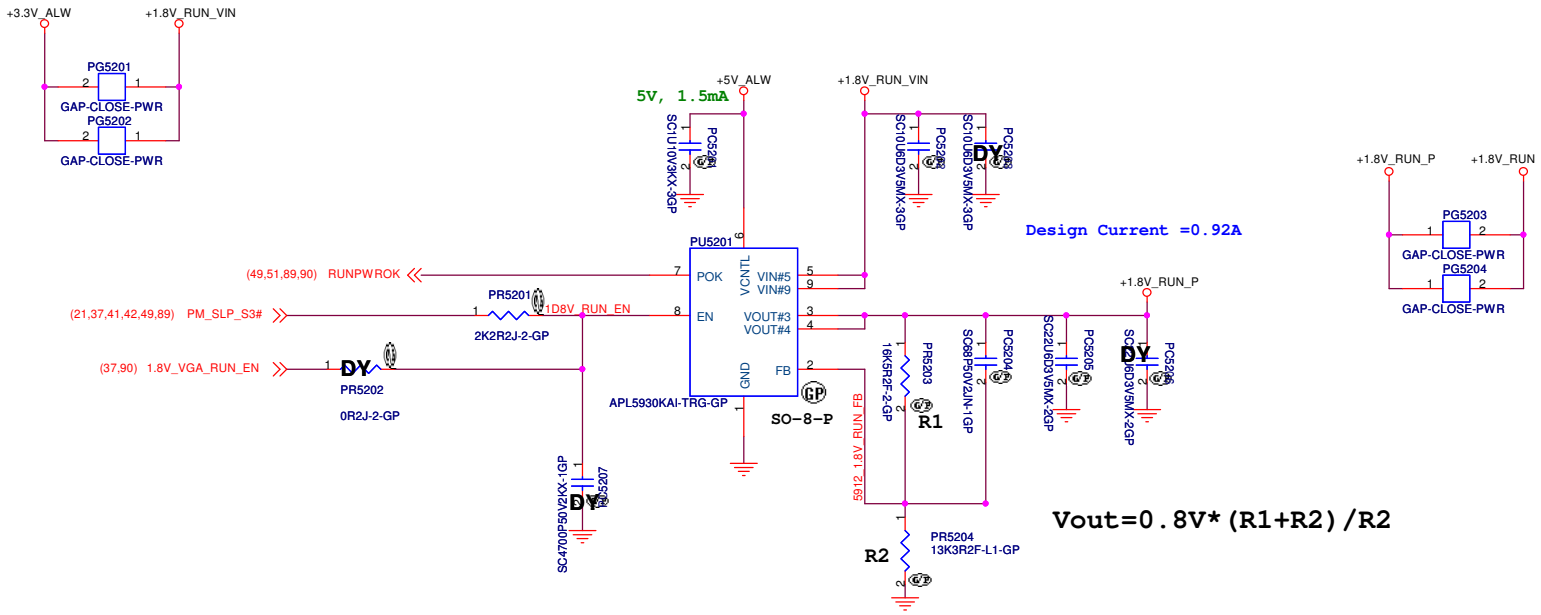
Date: Thursday, March 04, 2010 | Sheet 51 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930_+1.8V_RUN

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 52 of 95

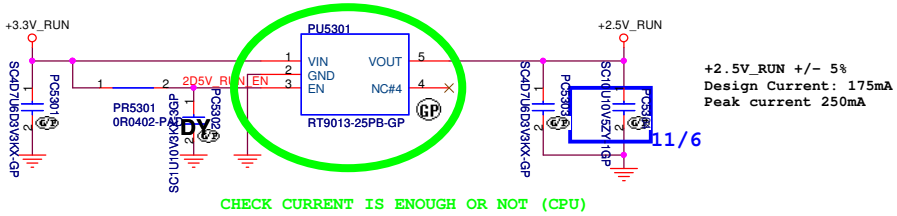
WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = PWR.Plane.Regulator_0P9v

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN



+2.5V_RUN +/- 5%
Design Current: 175mA
Peak current 250mA

CHECK CURRENT IS ENOUGH OR NOT (CPU)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +CPU_VDDR&+2.5V_RUN

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

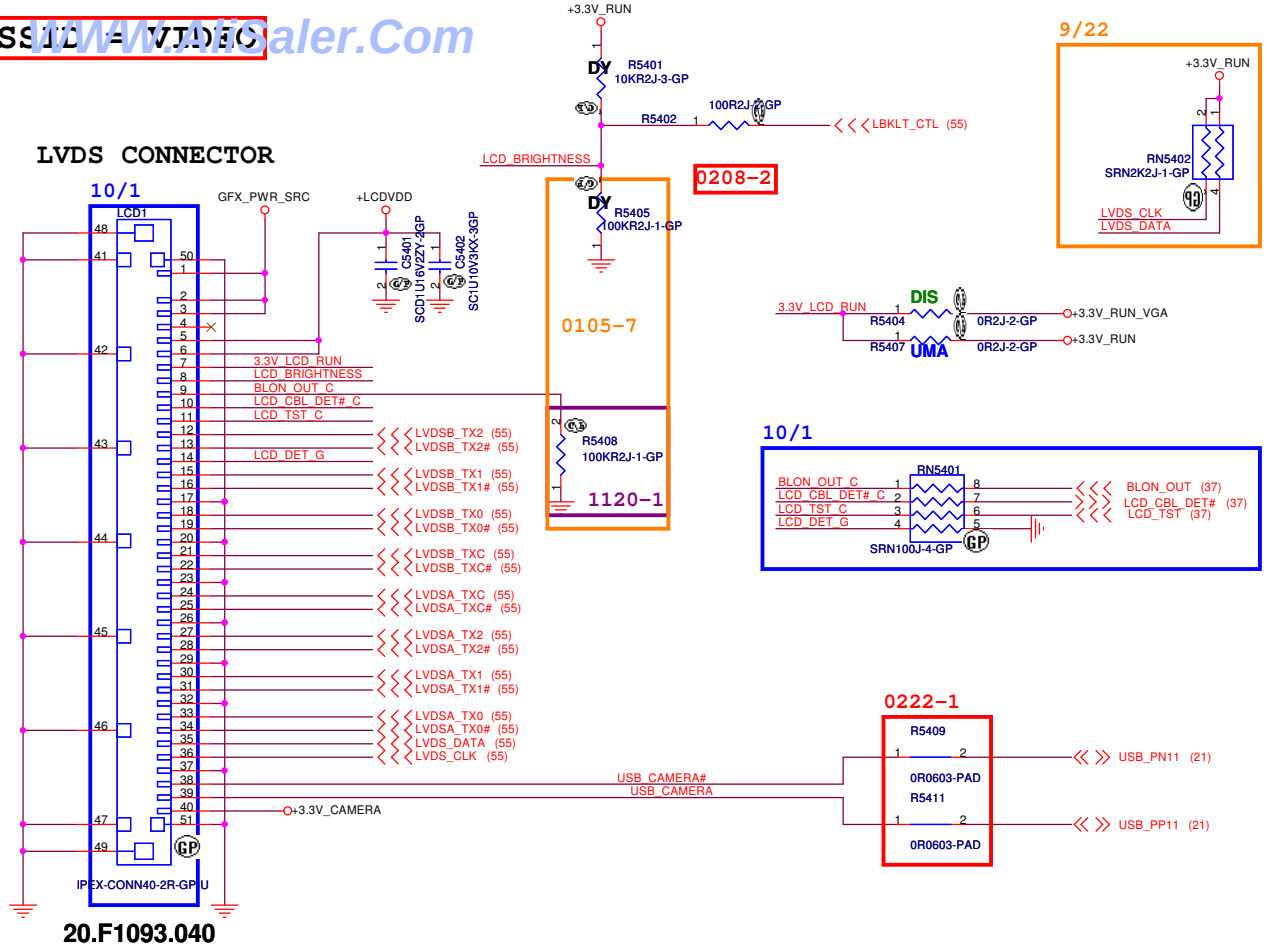
Date: Thursday, March 04, 2010 | Sheet 53 of 95

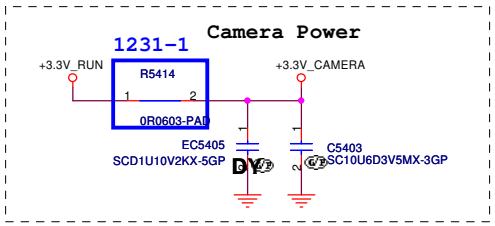
WWW.AliSaler.Com

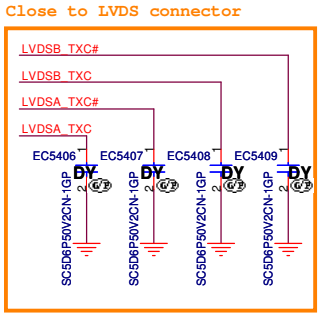
WWW.AliSaler.Com

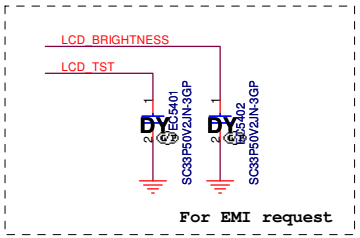
SSID = VIDEO

LVDS CONNECTOR



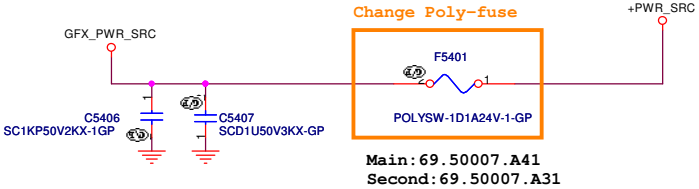






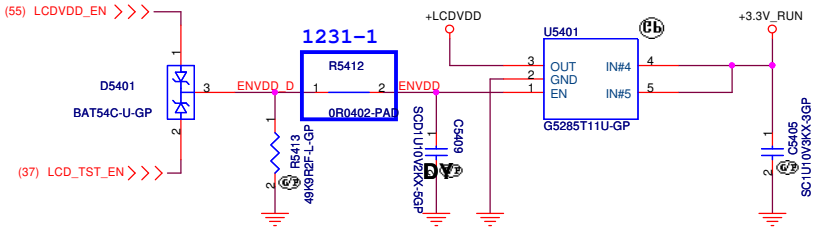
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

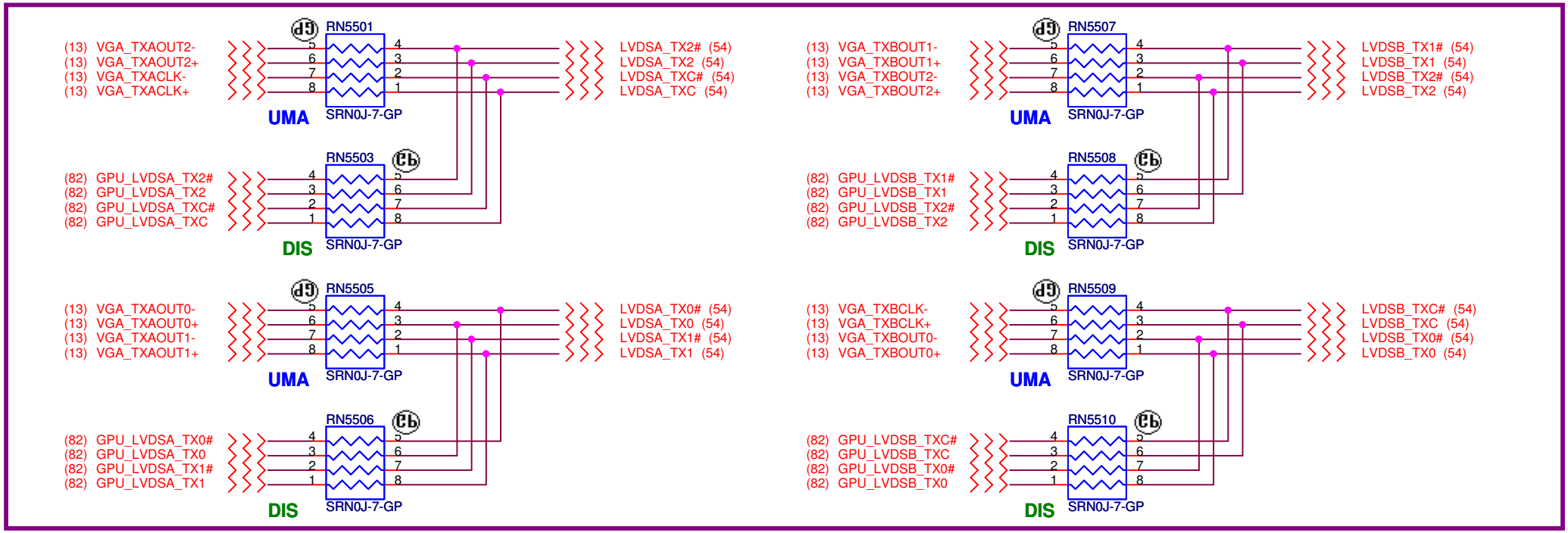
Date: Thursday, March 04, 2010 | Sheet 54 of 95

WWW.AliSaler.Com

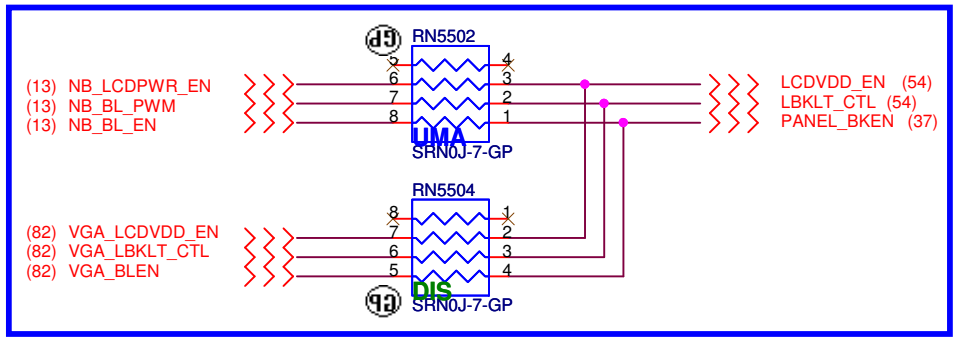
WWW.AliSaler.Com

SSID = VIDEO

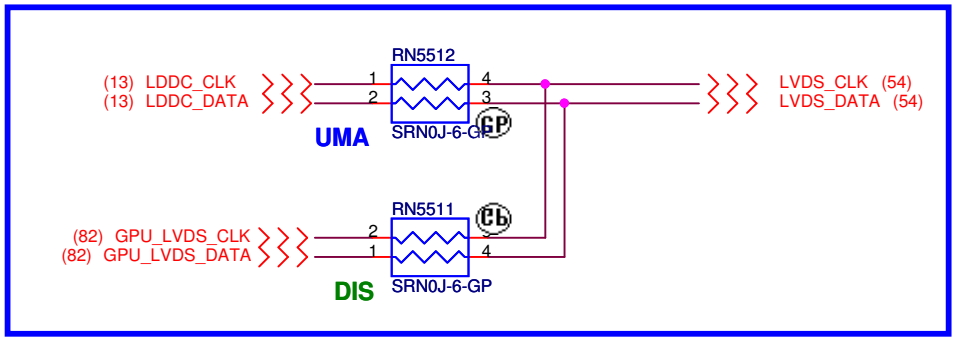
9/18



10/1



10/1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LVDS_Switch***

Size	Document Number	Rev
	Berry AMD Discrete/UMA	***A00***

Date: Thursday, March 04, 2010 Sheet 55 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 56 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

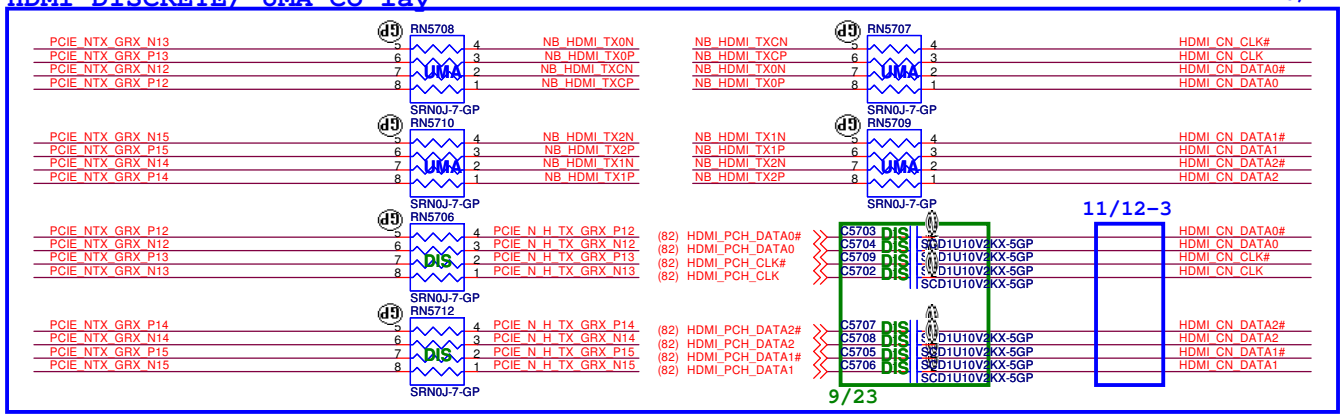
SSID = VIDEO

HDMI CONNECTOR

(12) PCIE_NTX_GRX_P[12..15]
(12) PCIE_NTX_GRX_N[12..15]
PCIE_N_H_TX_GRX_P[12..15] (80)
PCIE_N_H_TX_GRX_N[12..15] (80)

HDMI DISCRETE/ UMA Co-lay

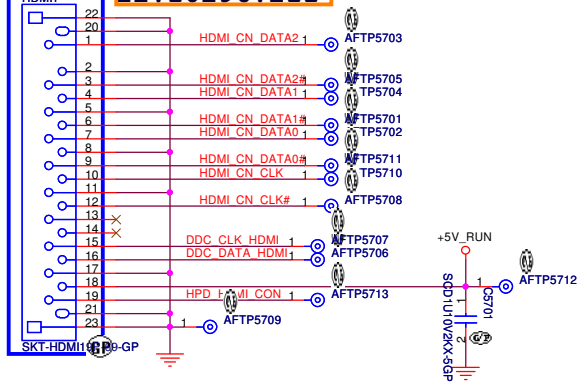
10/1



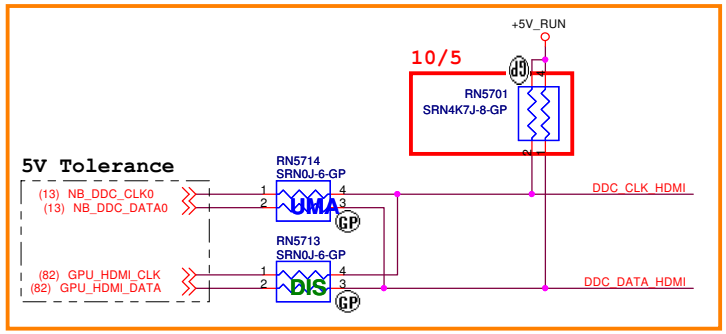
HDMI CONN

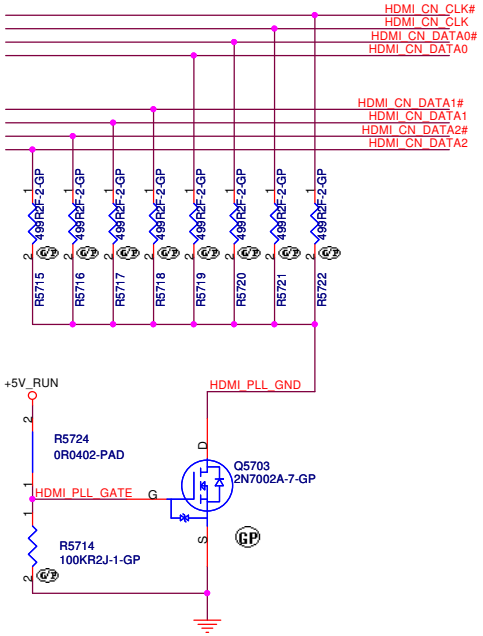
10/1

22.10296.211

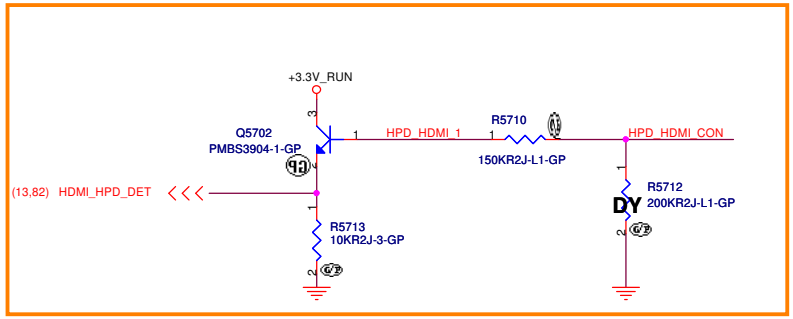


9/15





9/22



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 57 of 95

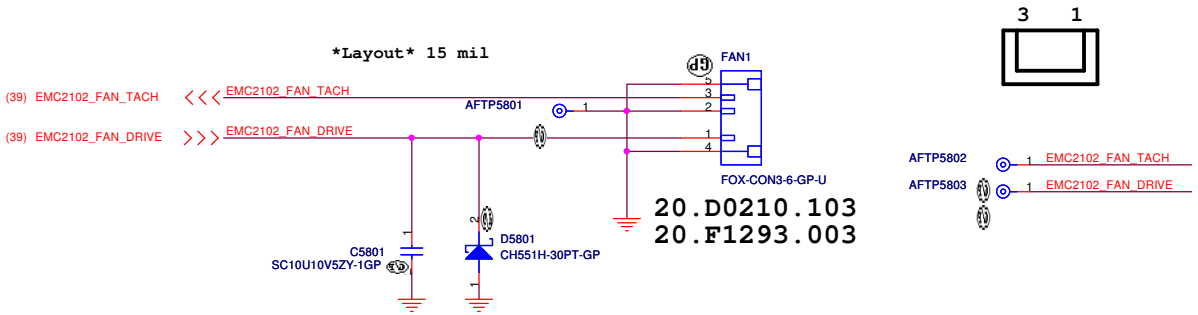
WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = User.Interface

SSID = Thermal

Fan Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

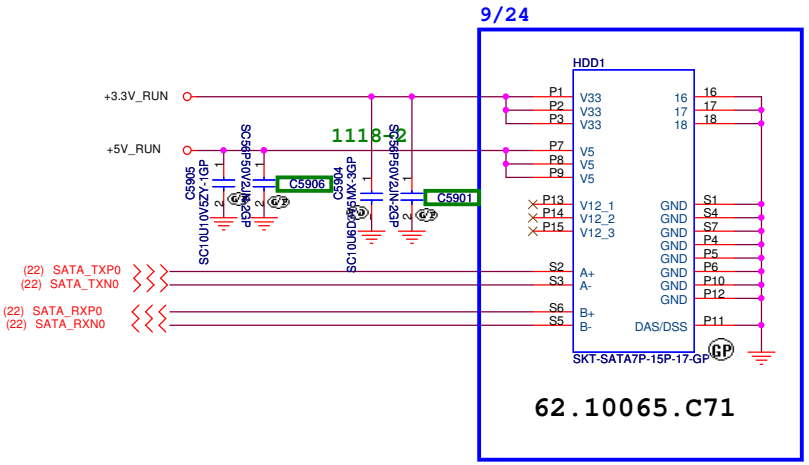
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

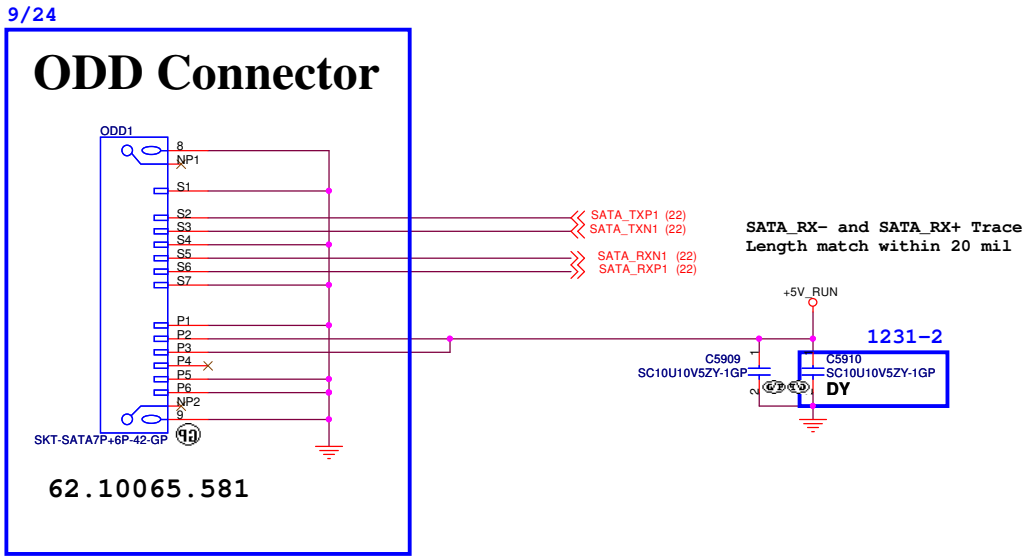
Date: Thursday, March 04, 2010 | Sheet 58 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SATA HDD Connector





WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

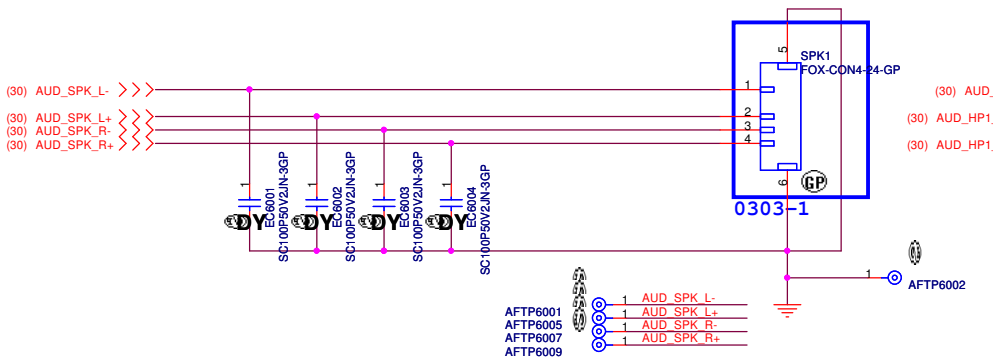
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 59 of 95

WWW.AliSaler.Com

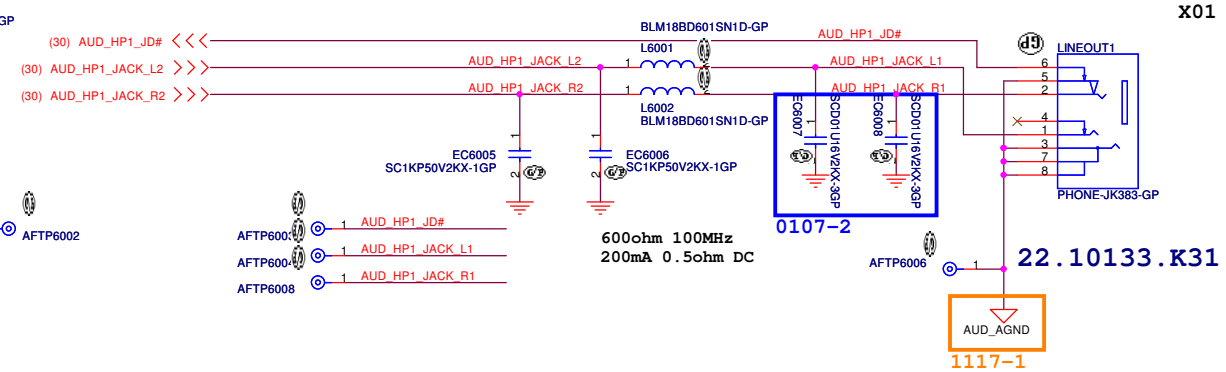
Speaker Connector

Main 20.F0693.004
SEC. 20.F0693.004

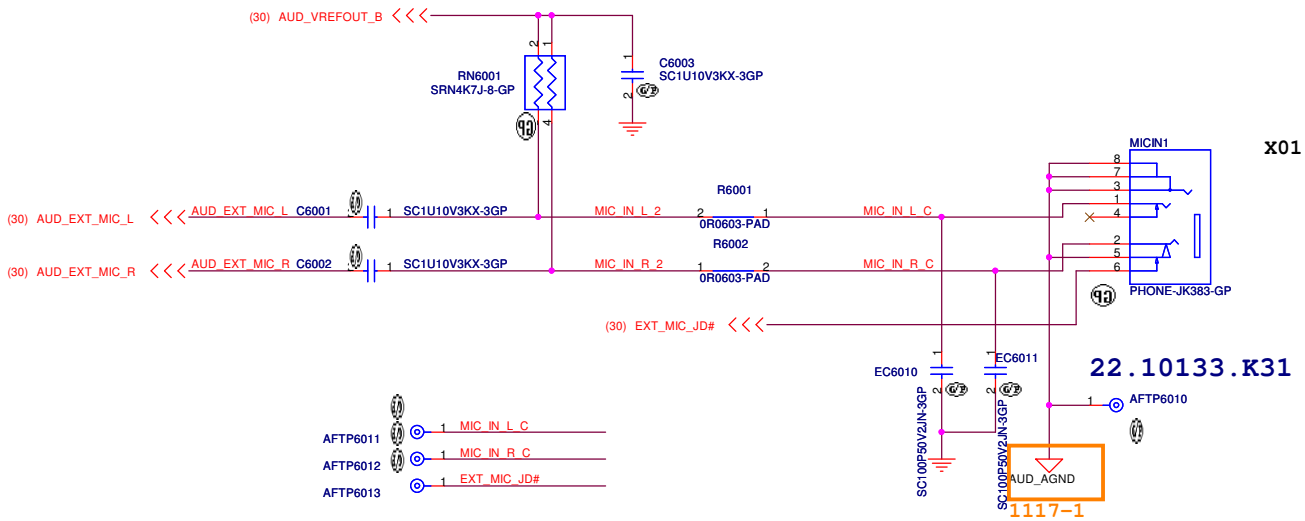


LINE1 OUT

X01 0713



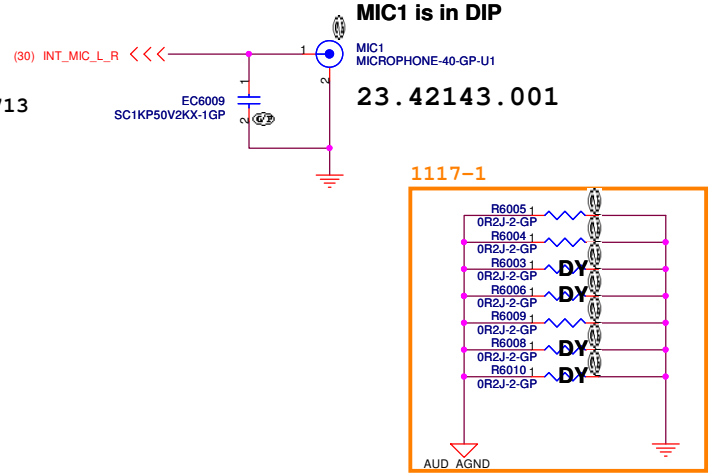
MIC IN



Internal Microphone

MIC1 is in DIP

X01 0713



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 60 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

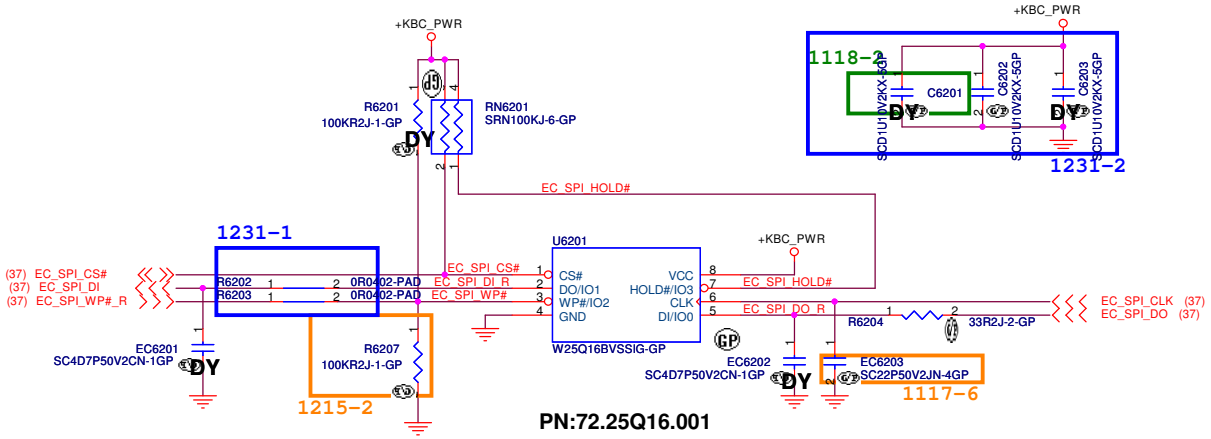
Date: Thursday, March 04, 2010 Sheet 61 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

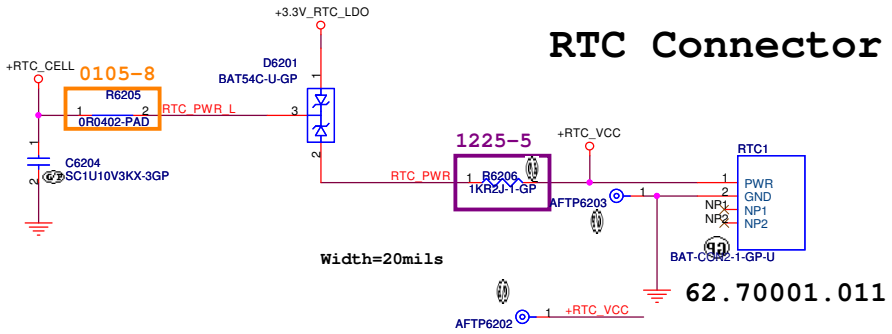
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

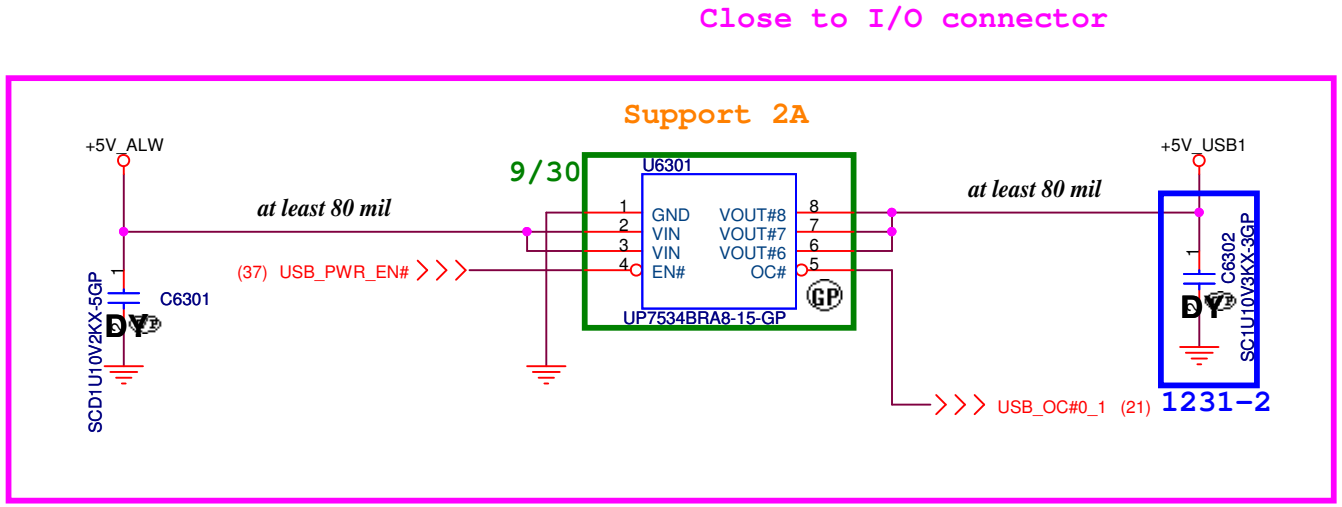
Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 62 of 95

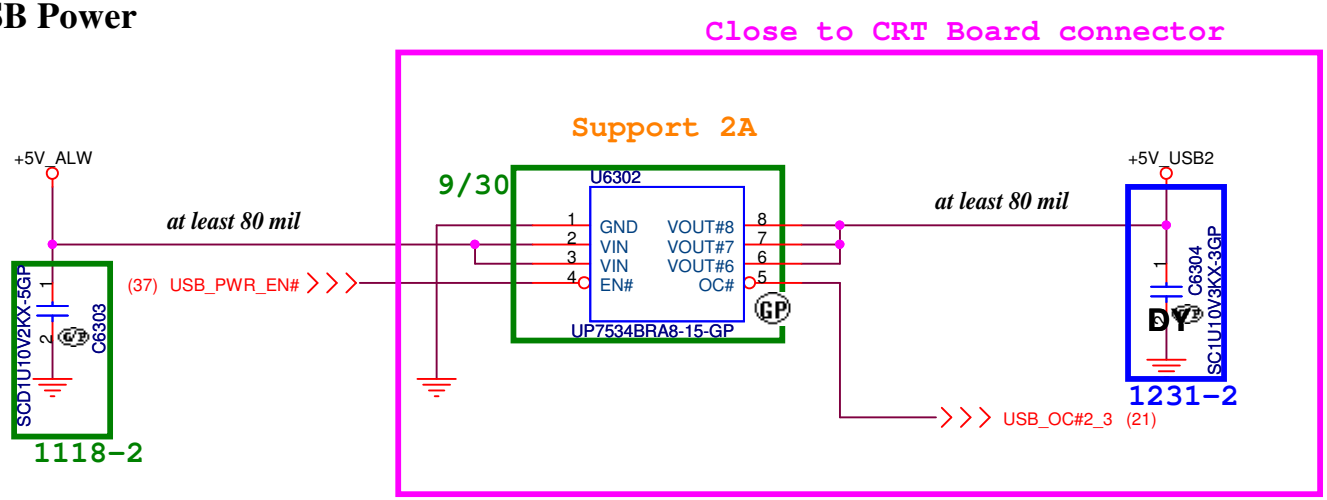
WWW.AliSaler.Com

SSID = USB

IO Board USB Power



CRT Board USB Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size	Document Number	Rev
	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 63 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 | Sheet 64 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

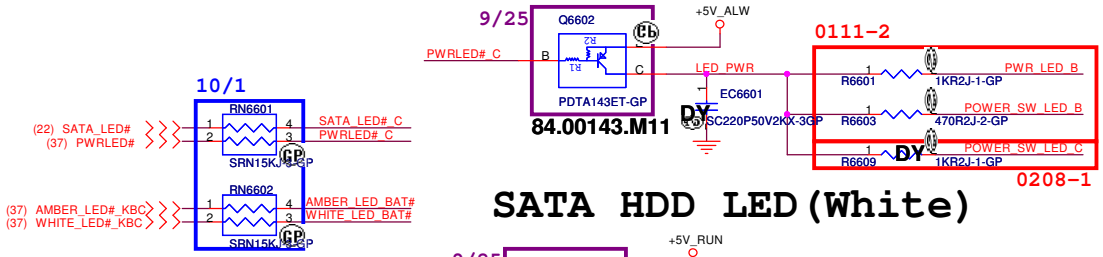
Date: Thursday, March 04, 2010 Sheet 65 of 95

WWW.AliSaler.Com

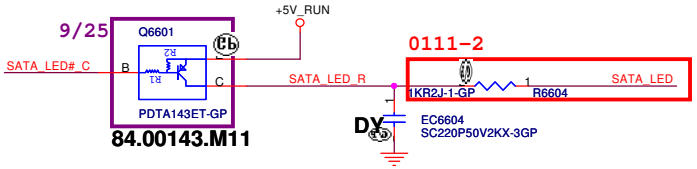
SSID - User Interface

WWW.AliSaler.Com

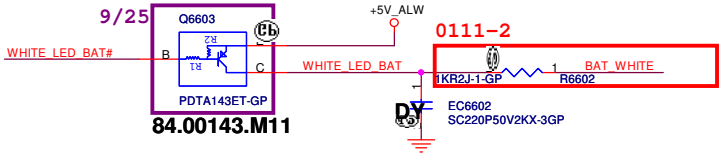
Power LED (White)

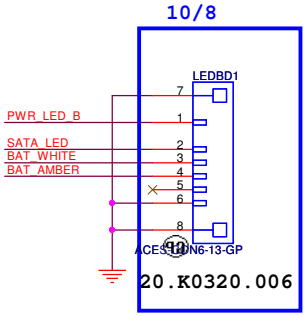


SATA HDD LED (White)

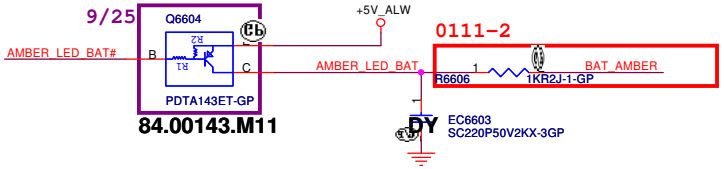


Battery LED1 (White)

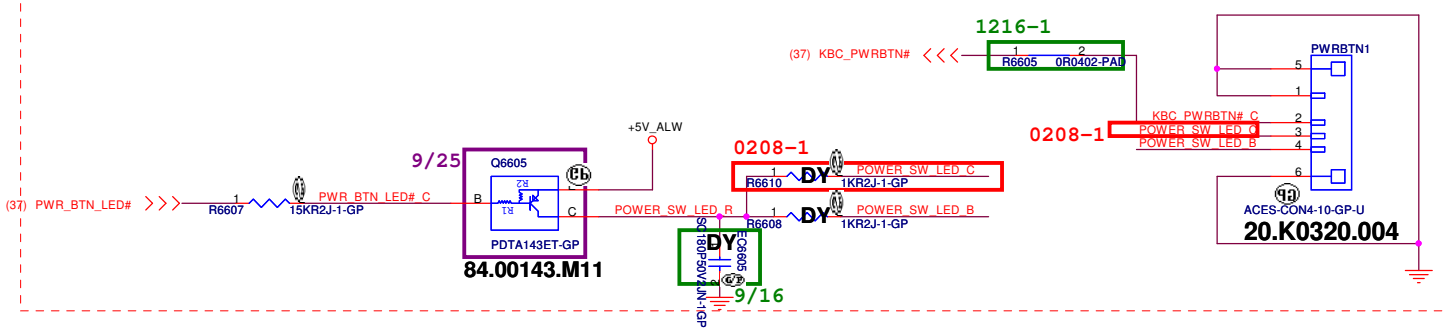




Battery LED2 (Amber)



Power button LED (White)



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 66 of 95

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

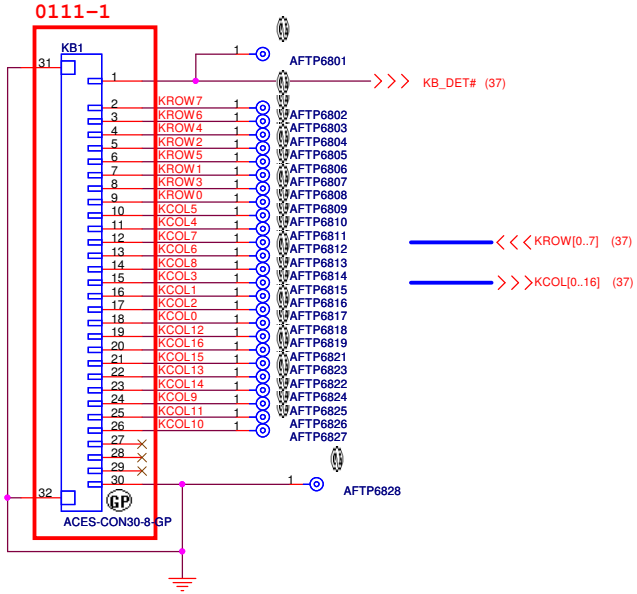
Date: Thursday, March 04, 2010 Sheet 67 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = KBC

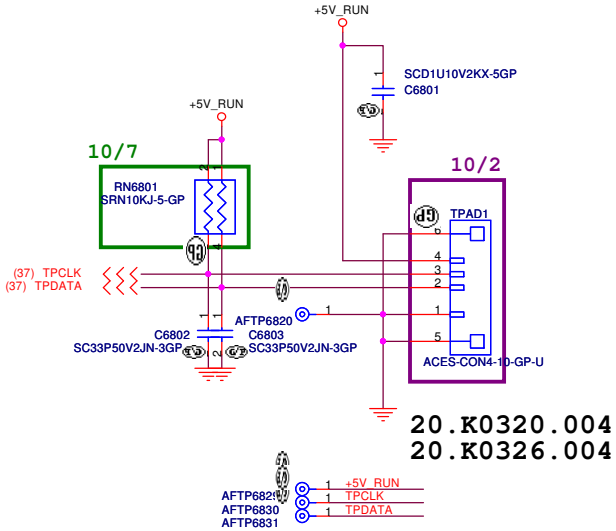
Internal KeyBoard Connector



20.K0524.030
20.K0461.030

SSID = Touch.Pad

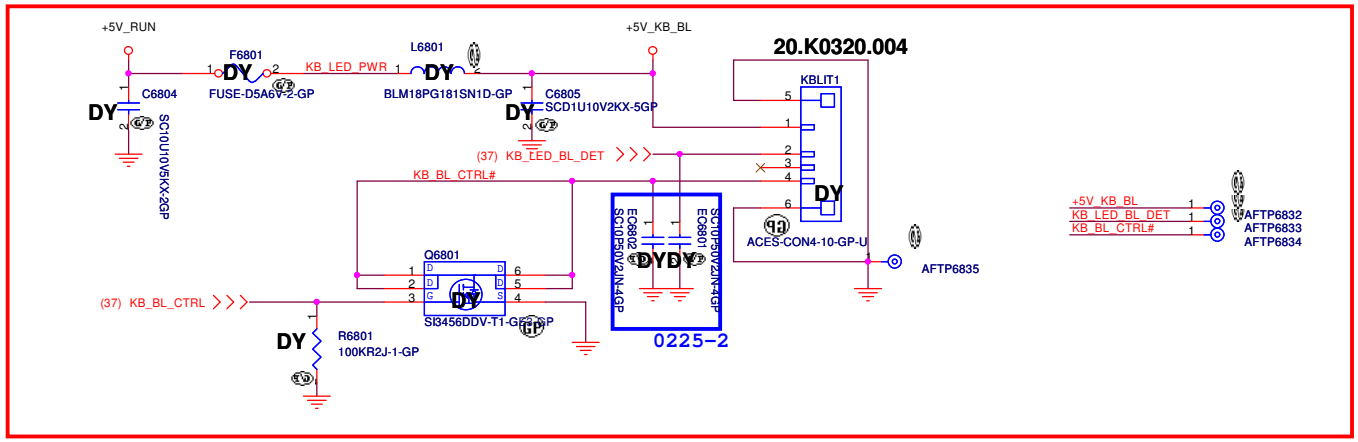
TouchPad Connector



20.K0320.004
20.K0326.004

KB Backlight Connector

0208-2



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

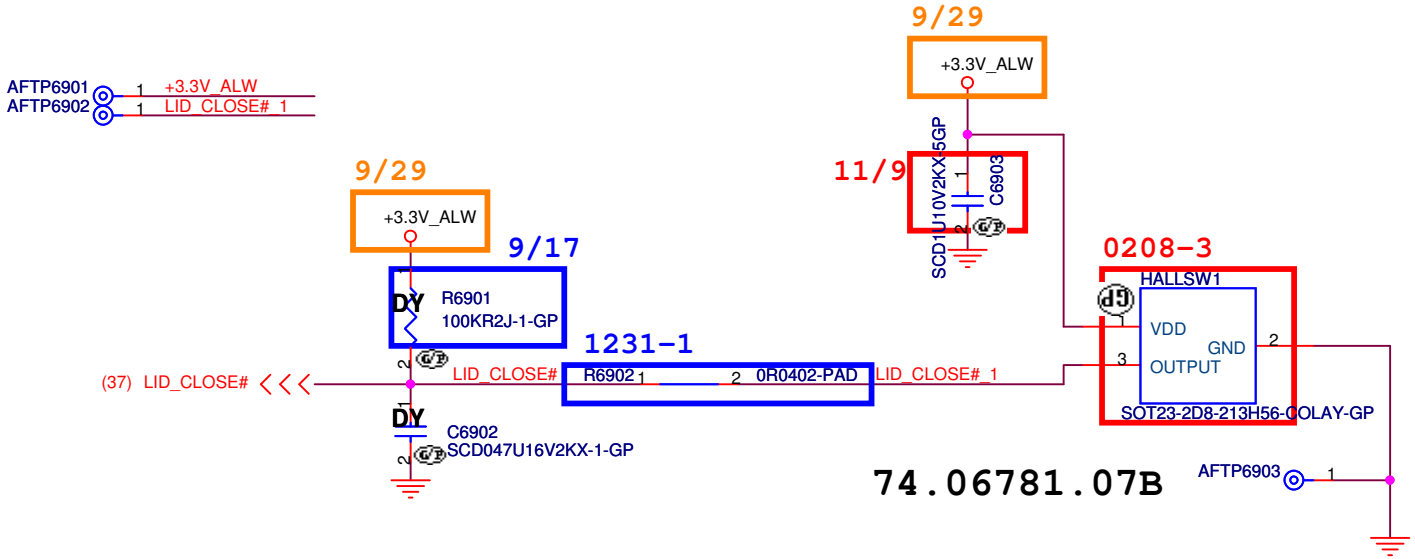
Title: Key Board/Touch Pad

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 68 of 95

WWW.AliSaler.Com

SSID = Hall.Sensor



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Effect Sensor***

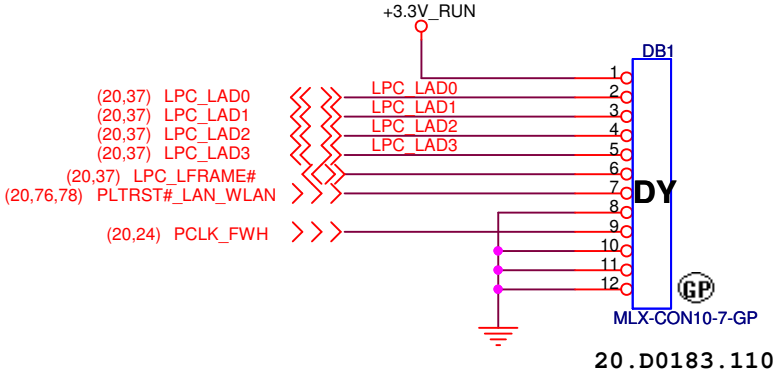
Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 69 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = Debug



20.D0183.110

WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

Date: Thursday, March 04, 2010 Sheet 70 of 95

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	**Berry AMD Discrete/UMA**	**A00**

Date: Thursday, March 04, 2010 Sheet 71 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RESERVED

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

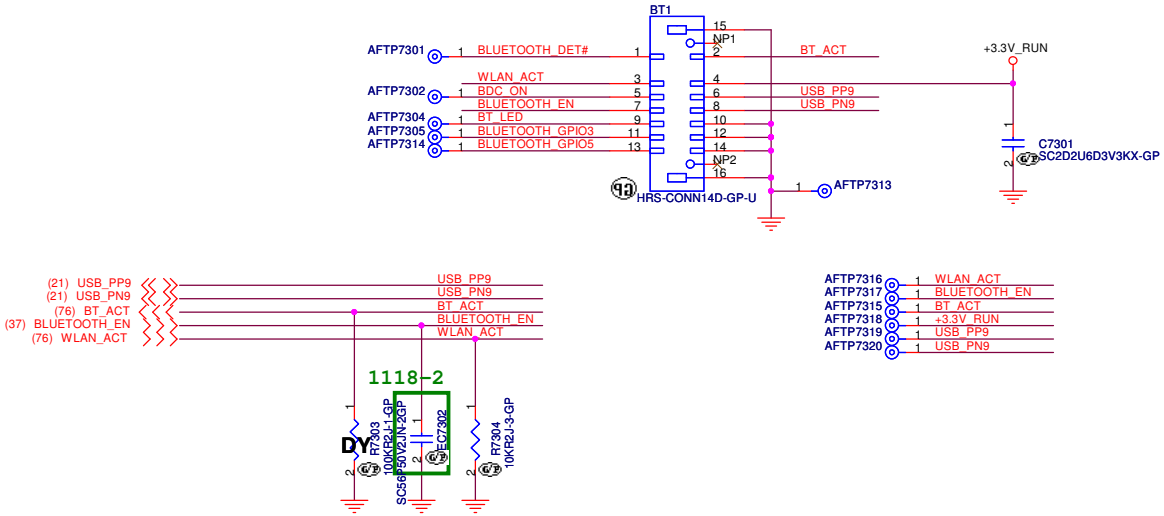
Date: Thursday, March 04, 2010 Sheet 72 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = User.Interface

Bluetooth Module conn.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
	Bluetooth	
Size A3	Document Number ***Berry***	Rev ***A00***
Date: Thursday, March 04, 2010	Sheet 73 of 95	

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 74 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Berry AMD Discrete/UMA***	***A00***

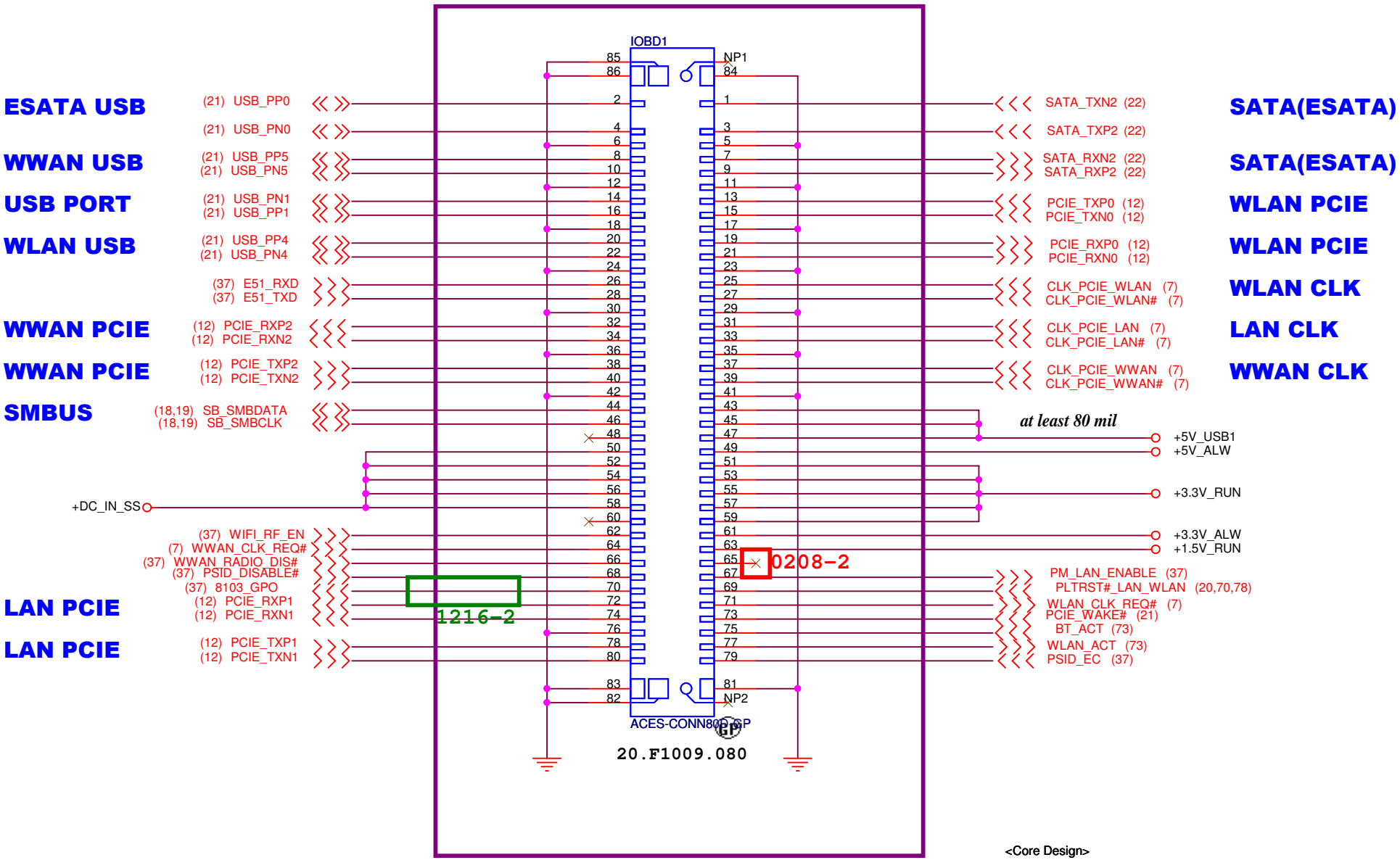
Date: Thursday, March 04, 2010 Sheet 75 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = Int.Conn

10/9



0107-6

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

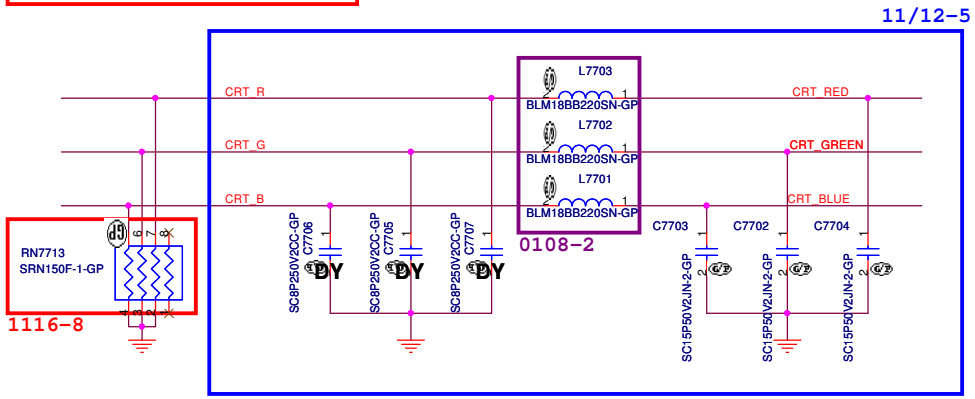
Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 76 of 95

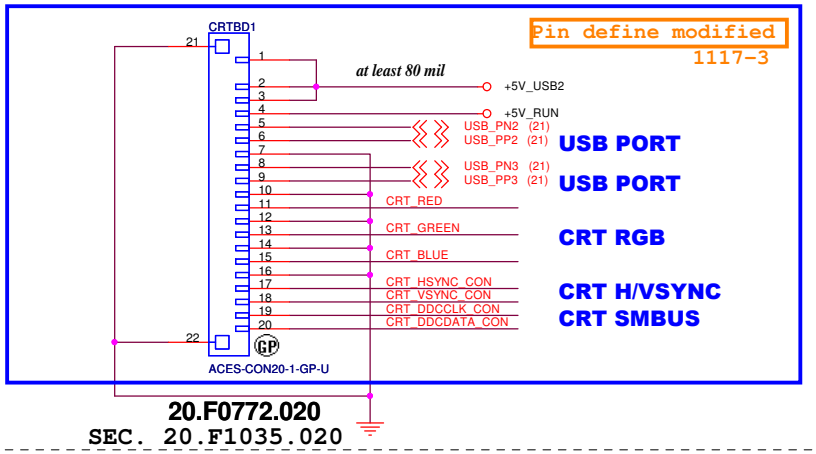
WWW.AliSaler.Com

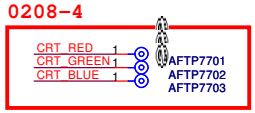
WWW.AliSaler.Com

SSID = Int.Conn



10/1 CRT Board Connector

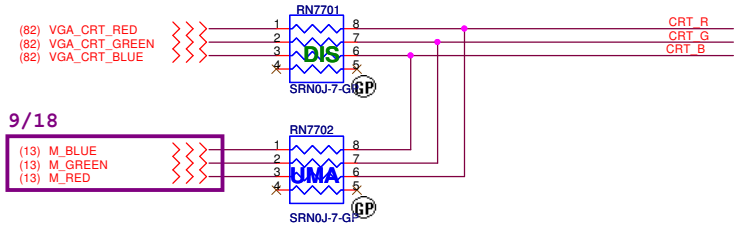




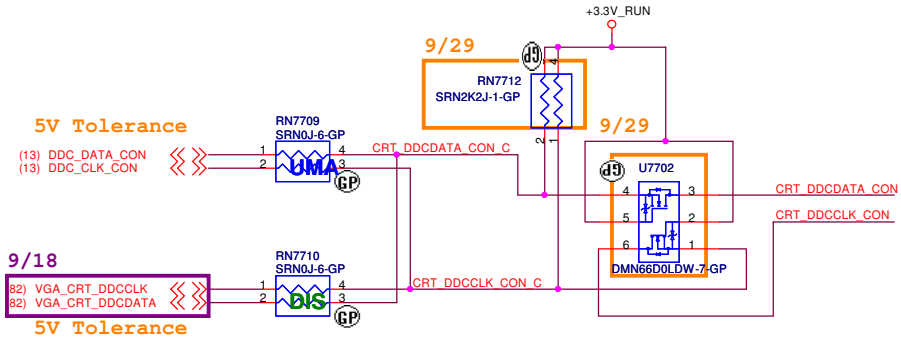
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board

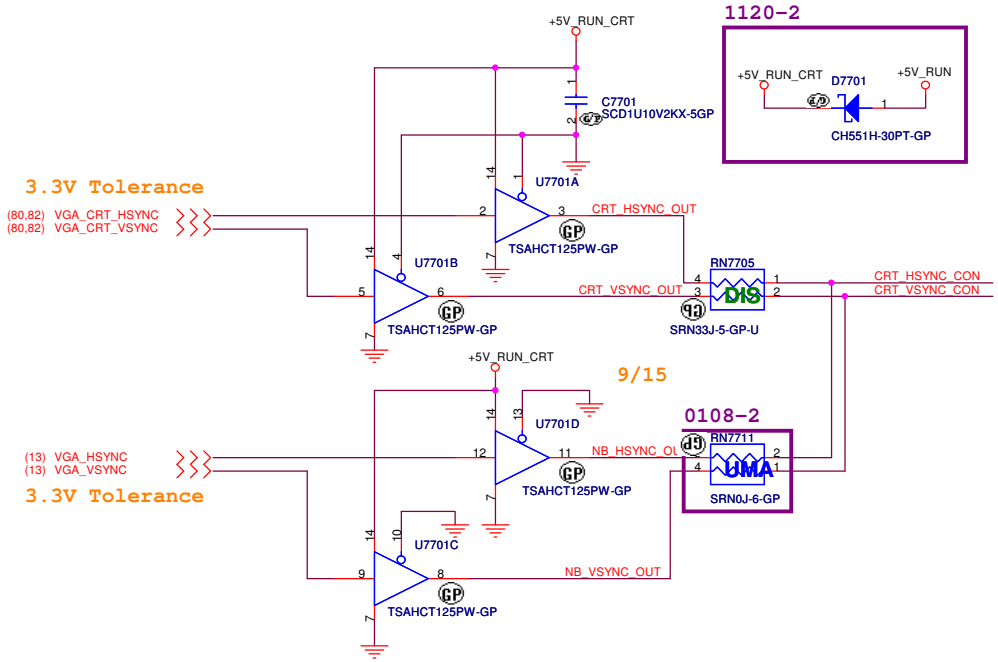


CRT DDCDATA & DDCCLK



CRT Hsync & Vsync level shift

Close to CRT Board CONN

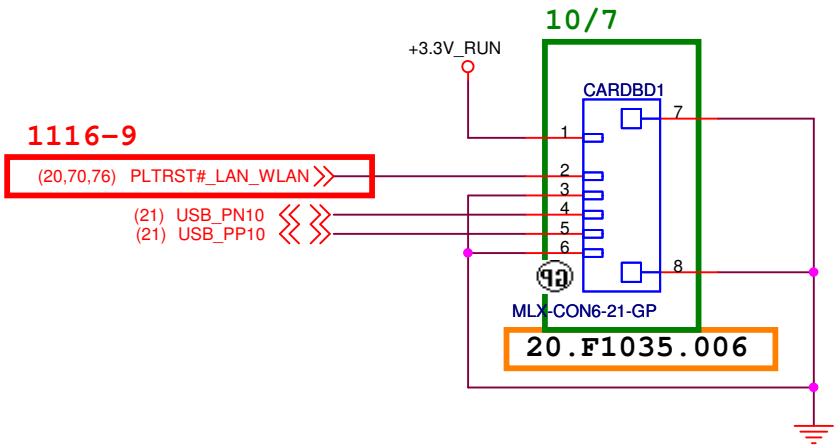


WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = SDIO

Card Reader connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	Berry AMD Discrete/UMA	A00

Date: Thursday, March 04, 2010 Sheet 78 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

H1 HTE95BE95R29-R-5-GP
H2 HTE95BE95R29-R-5-GP
H3 HTE95BE95R29-R-5-GP
H4 HTE95BE95R29-R-5-GP
H6 HTE95BE95R29-R-5-GP
H7 HTE95BE95R29-R-5-GP
H8 HTE95BE95R29-R-5-GP
H9 HTE95BE95R29-R-5-GP
H5 HOLE256R111-GP
H11 HOLE256R111-GP
H10 HOLE335R115-GP DY

CPU Thermal module hole
HTML1 HOLE197R166-GP DY
HTML2 HOLE197R166-GP DY
HTML3 HOLE197R166-GP DY

GPU Thermal module hole
HGPU1 STF237R117H83-1-GP

0210-2
stand off
HBT1 STF237R117H123-GP

EMI Reserve

+PWR_SRC
EC7901 SCD1U25V2KX-GP
EC7902 SCD1U25V2KX-GP
EC7904 DY SCD1U25V2KX-GP
EC7903 SCD1U25V2KX-GP
EC7905 DY SCD1U25V2KX-GP
EC7906 SCD1U25V2KX-GP

+VGA_CORE
1118-2
EC7907 SCD1U10V2KX-5GP
10/6
+3.3V_RUN
EC7910 DY SCD1U25V2KX-GP
+5V_ALW
EC7911 DY SCD1U25V2KX-GP
EC7912 DY SCD1U25V2KX-GP
10/5

SPR1 SPRING-58-GP DY

EMI Reserve 1117-4

+PWR_SRC
EC7924 DY SC10P50V2JN-4GP
+3.3V_RUN
EC7916 DY SC10P50V2JN-4GP
EC7920 DY SC10P50V2JN-4GP
EC7923 DY SC10P50V2JN-4GP
EC7917 DY SC10P50V2JN-4GP

+3.3V_RUN +5V_RUN
EC7922 DY SC10P50V2JN-4GP
EC7915 DY SC10P50V2JN-4GP

+5V_RUN +VCC_CORE
EC7919 DY SC10P50V2JN-4GP
EC7921 DY SC10P50V2JN-4GP

+5V_RUN +PWR_SRC
EC7914 DY SC10P50V2JN-4GP
EC7913 DY SC10P50V2JN-4GP

+5V_RUN +1.5V_RUN
EC7918 DY SC10P50V2JN-4GP

1118-2 RF Team Solution

+3.3V_ALW
C7909 SC56P50V2JN-2GP
C7906 DY SC56P50V2JN-2GP

+1.5V_RUN
C7905 SC56P50V2JN-2GP
C7904 DY SC56P50V2JN-2GP

+5V_RUN
C7902 SC56P50V2JN-2GP
C7917 DY SC56P50V2JN-2GP

+15V_ALW
C7907 DY SCD1U25V2KX-GP
C7915 DY SCD1U25V2KX-GP
C7911 DY SCD1U25V2KX-GP

+1.1V_RUN
C7910 SC56P50V2JN-2GP
C7908 SC56P50V2JN-2GP

+1.8V_RUN
C7919 SC56P50V2JN-2GP

+3.3V_RUN
C7920 SC56P50V2JN-2GP

0106-3 RF Team Solution

+PWR_SRC
C7922 DY SC56P50V2JN-2GP

+1.5V_SUS
C7921 DY SC56P50V2JN-2GP

0108-1 EMC reserved

+PWR_SRC
EC7927 DY SC56P50V2JN-2GP

+1.5V_SUS
EC7926 DY SC56P50V2JN-2GP
EC7925 DY SC56P50V2JN-2GP

0224-1

+PWR_SRC
EC7928 DY SC56P50V2JN-2GP
EC7931 DY SC56P50V2JN-2GP

0225-5

+DC_IN_SS
EC7929 DY SC56P50V2JN-2GP

+SDC_IN
EC7932 DY SC56P50V2JN-2GP

WWW.AliSaler.Com

<Core Design>

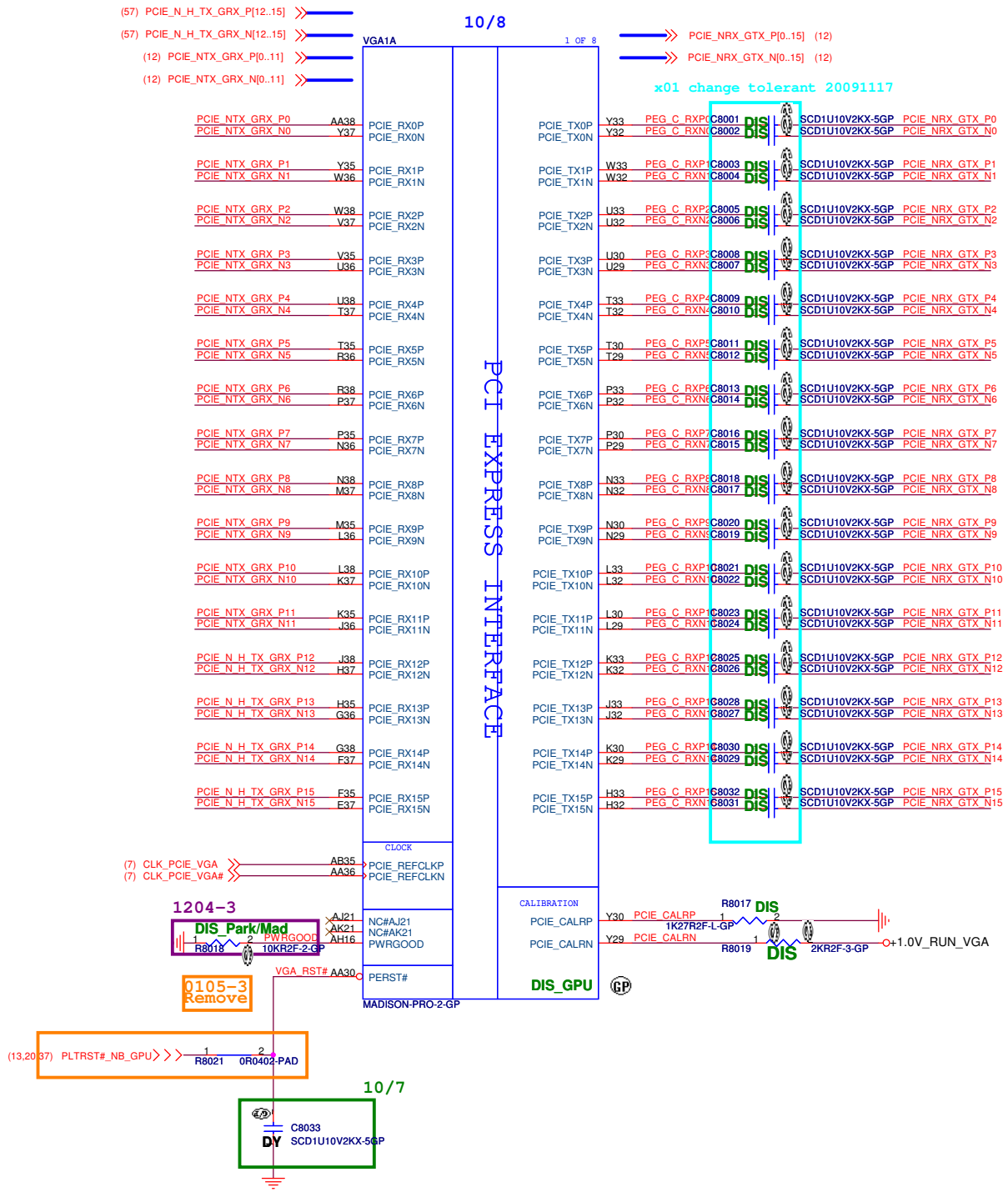
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Berry	A00

Date: Thursday, March 04, 2010 Sheet 79 of 95

WWW.AliSaler.Com



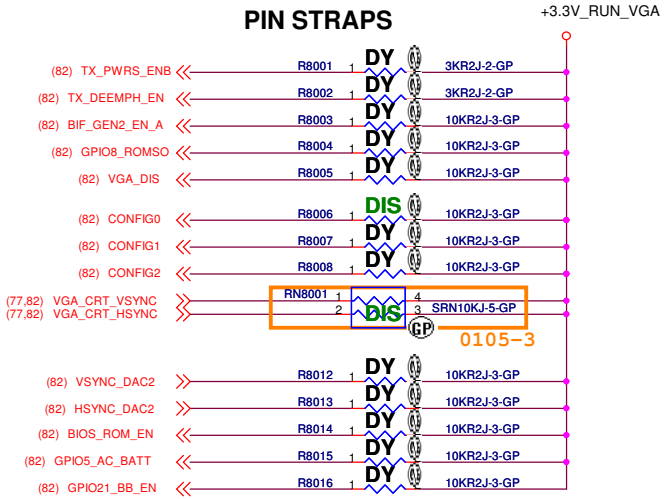
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

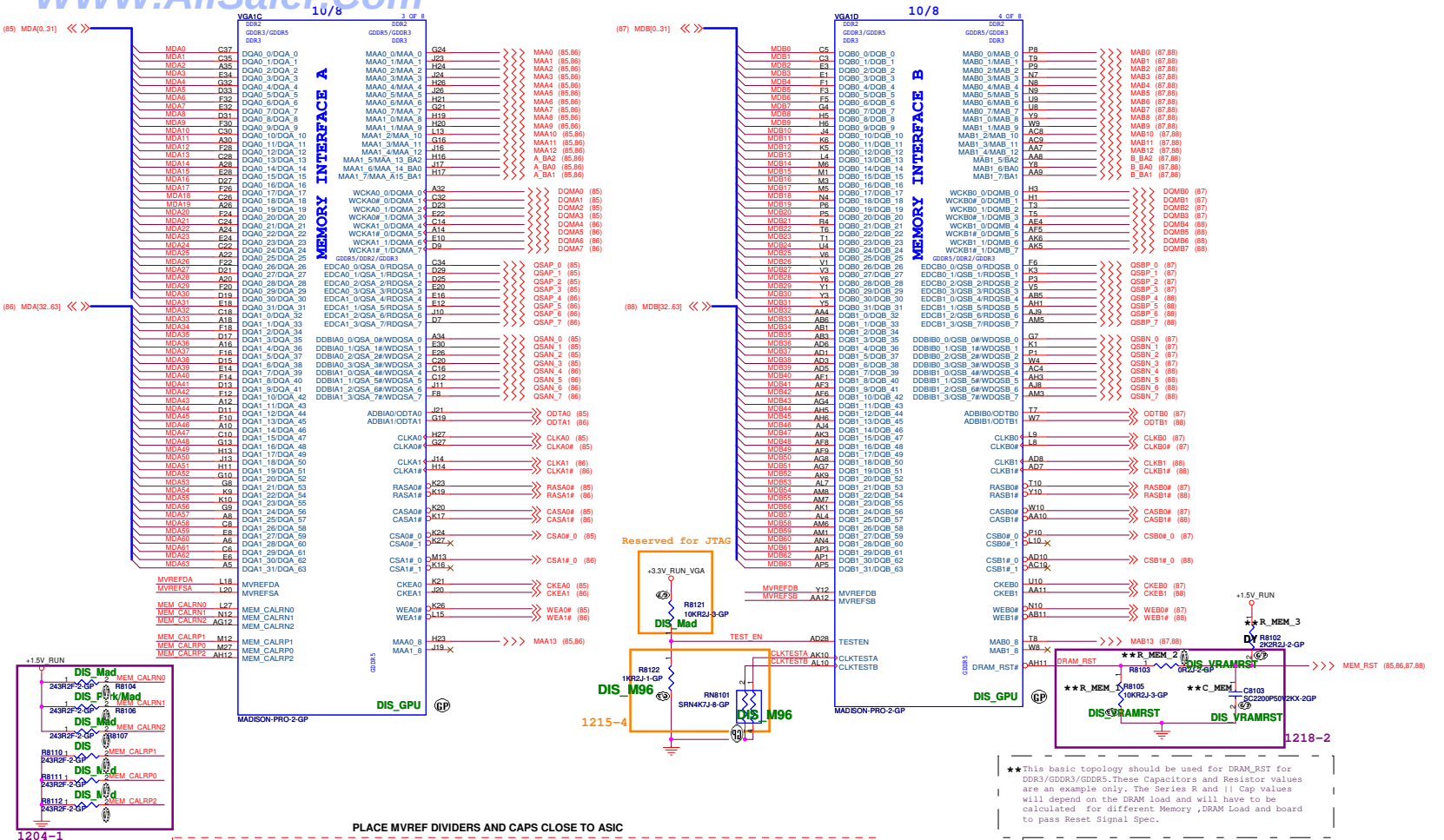
Title: GPU_PCIE/STRAPPING(1/5)

Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 80 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com



★★This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For Mannhatton	For M96-M2
R_MEM_1	68pF	10K
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	10K	2.2nF

X02-20091218

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

DDR3/GDDR3 Memory Stuff Option(M96/M92)

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size: A2 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 81 of 95

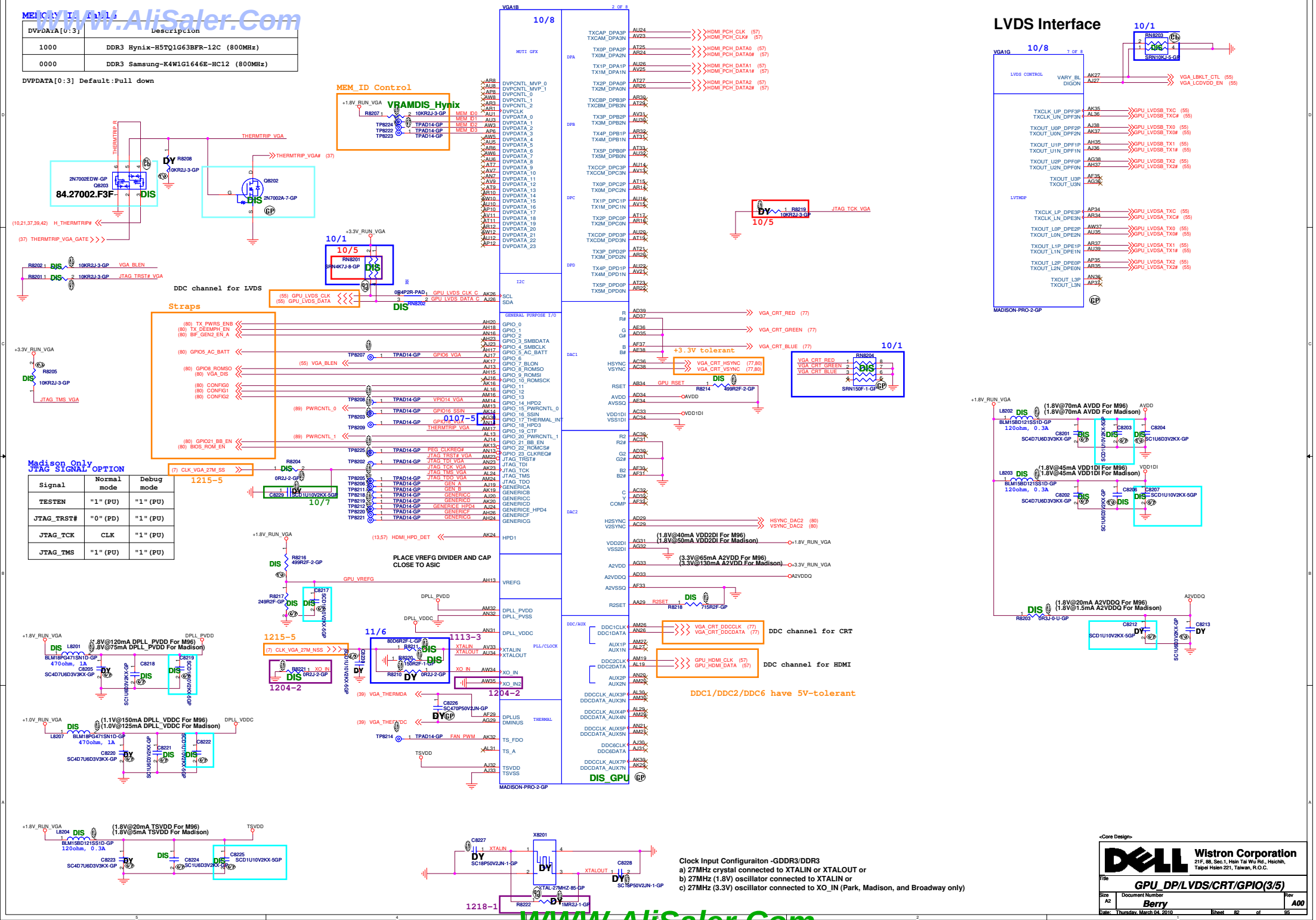
WWW.AliSaler.Com

WWW.AliSaler.Com

MEMORY Table

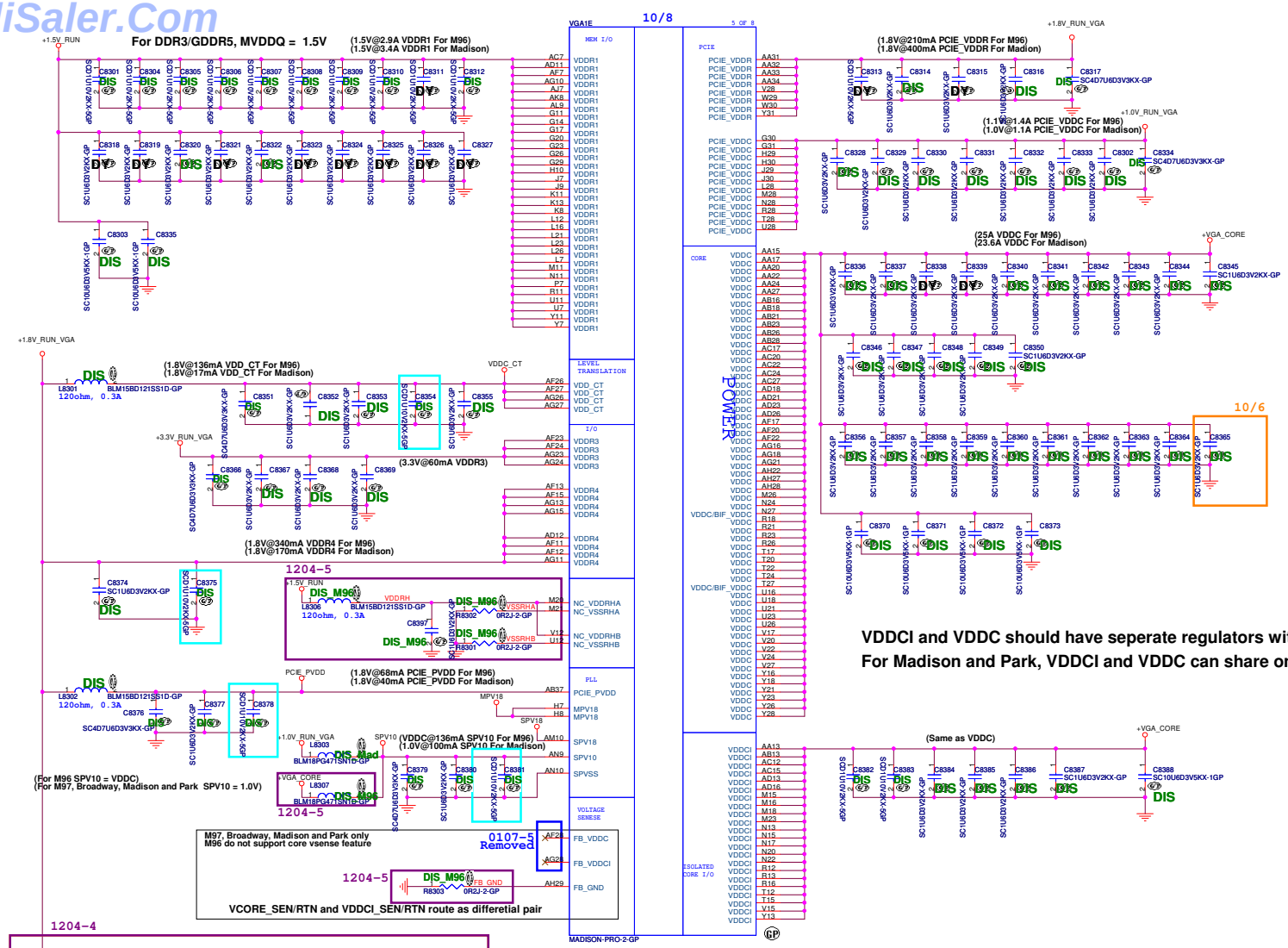
DVPDATA[0:3]	Description
1000	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
0000	DDR3 Samsung-K4W1G1646E-HC12 (800MHz)

DVPDATA[0:3] Default:Pull down



WWW.AliSaler.Com

WWW.AliSaler.Com



NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134

NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96

NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.

NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

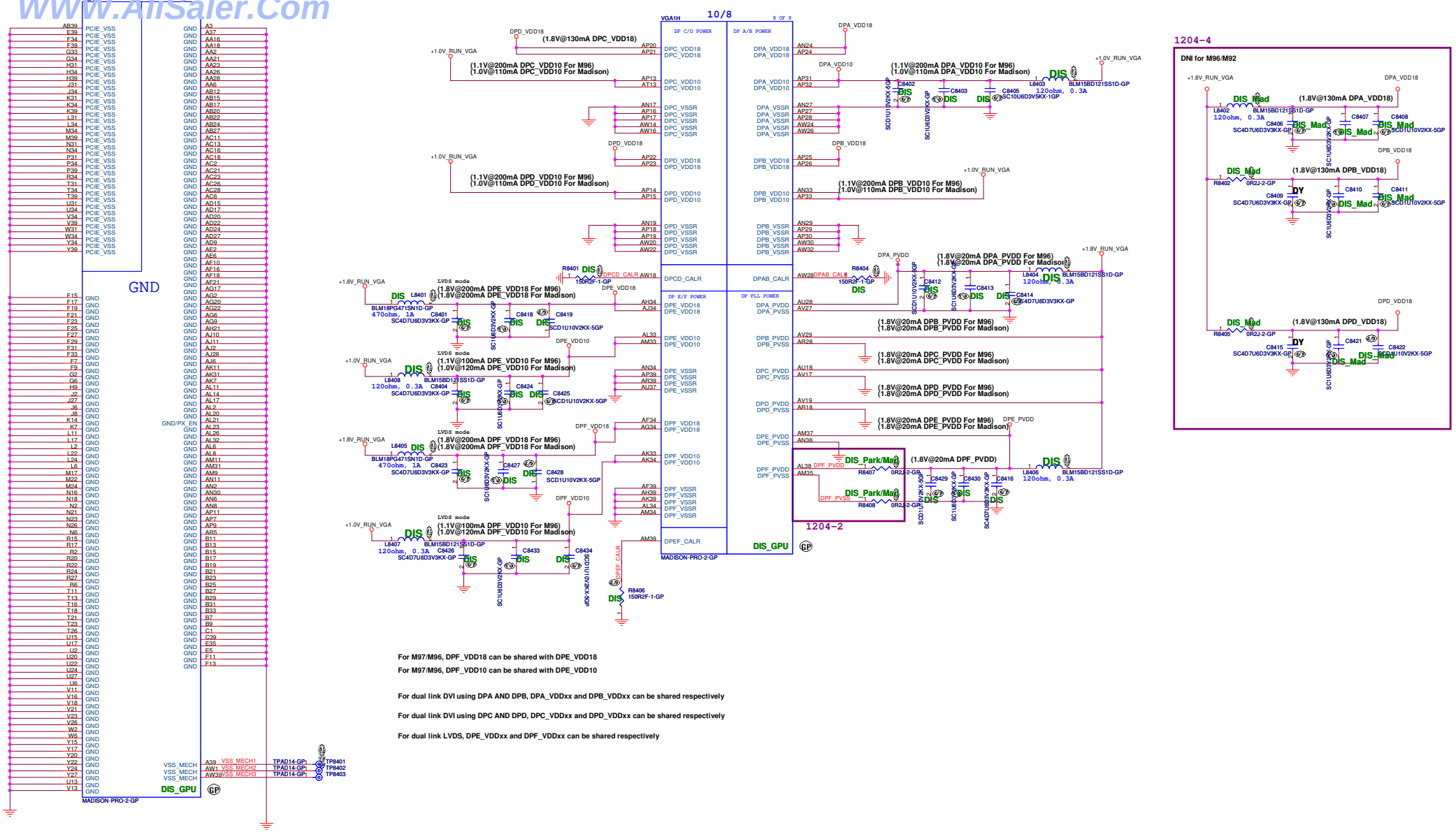
Title: GPU_POWER(4/5)

Size	Document Number	Rev
A2	Berry	A00

Date: Thursday, March 04, 2010 Sheet 83 of 85

WWW.AliSaler.Com

WWW.AliSaler.Com



For M97/M96, DPF_VDD18 can be shared with DPE_VDD18

For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively

For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively

For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

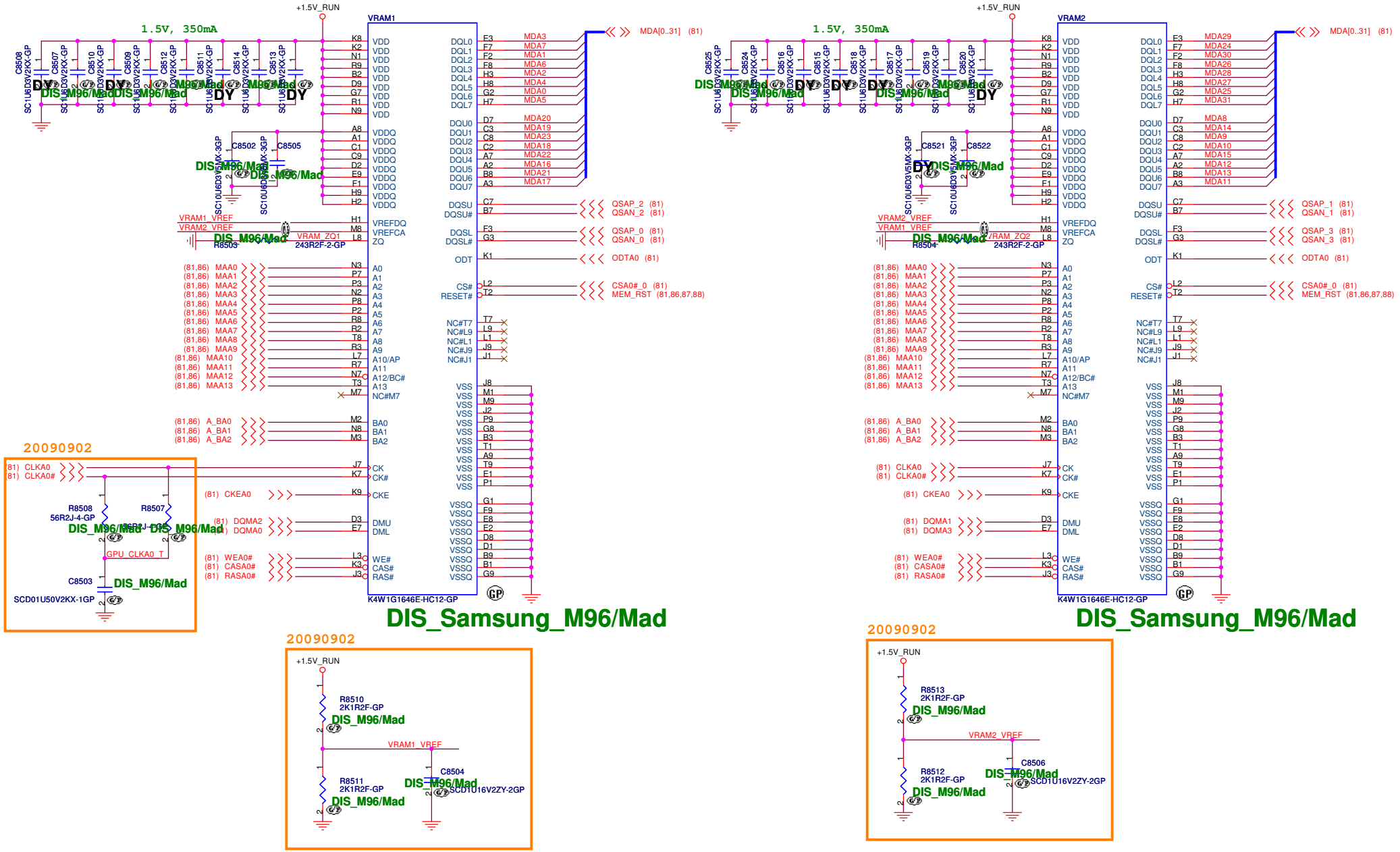
Title: GPU_DPPWR/GND(5/5)

Size: A2 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 84 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com



WWW.AliSaler.Com

<Core Design>

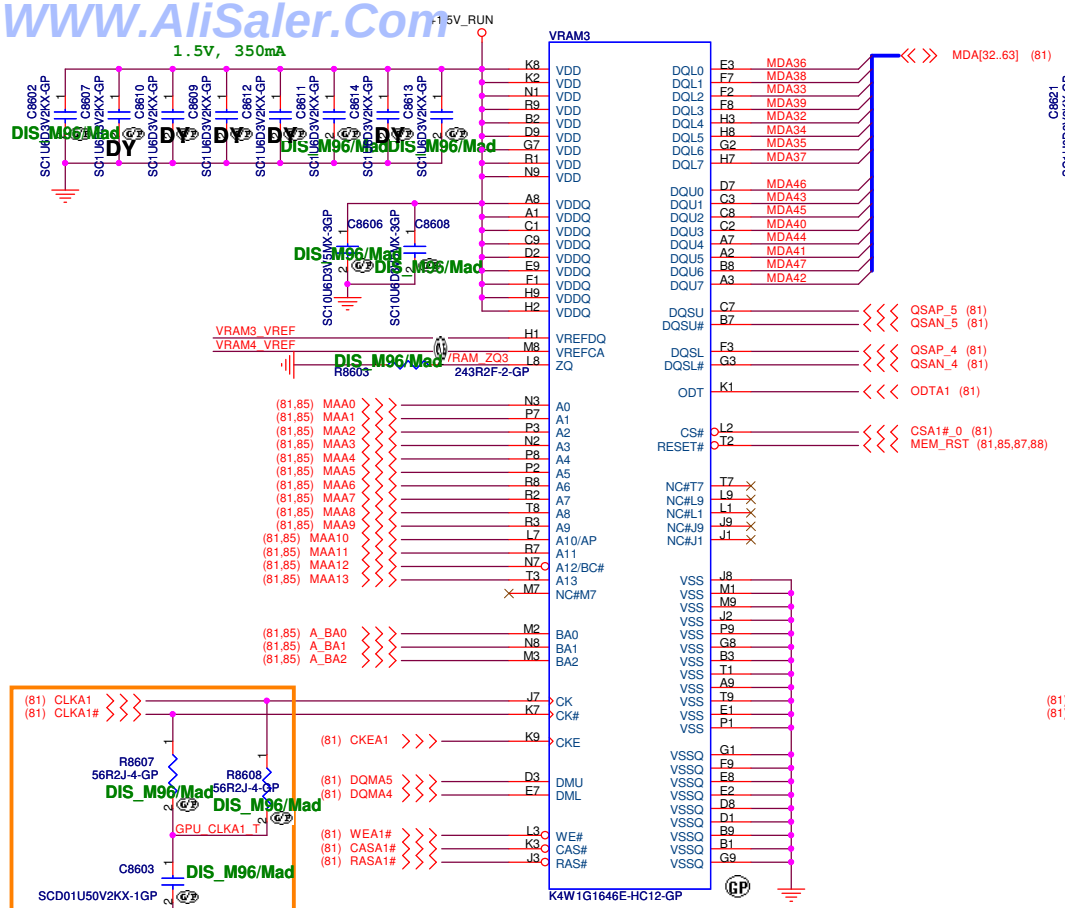
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

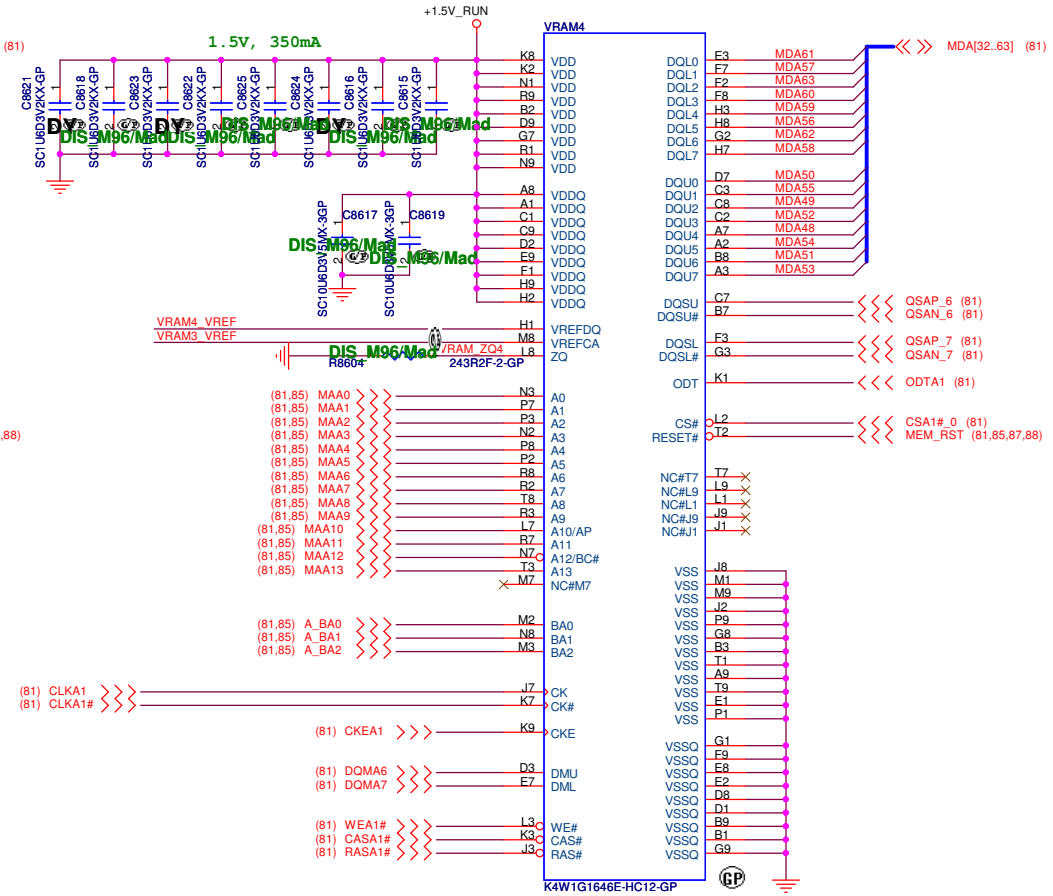
Size	Document Number	Rev
A3	Berry	A00

Date: Thursday, March 04, 2010 Sheet 85 of 95

WWW.AliSaler.Com

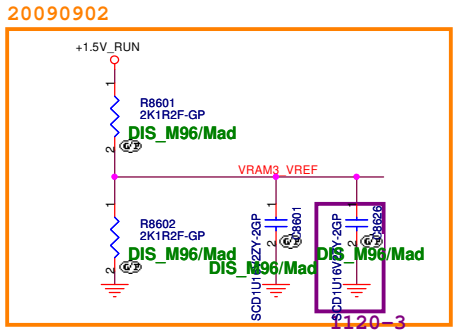


DIS_Samsung_M96/Mad

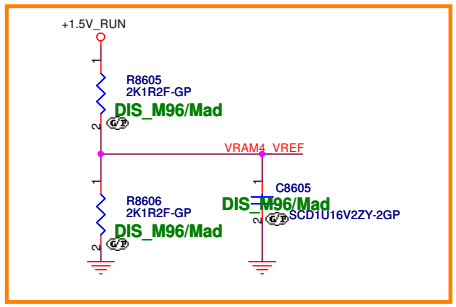


DIS_Samsung_M96/Mad

20090902



20090902



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

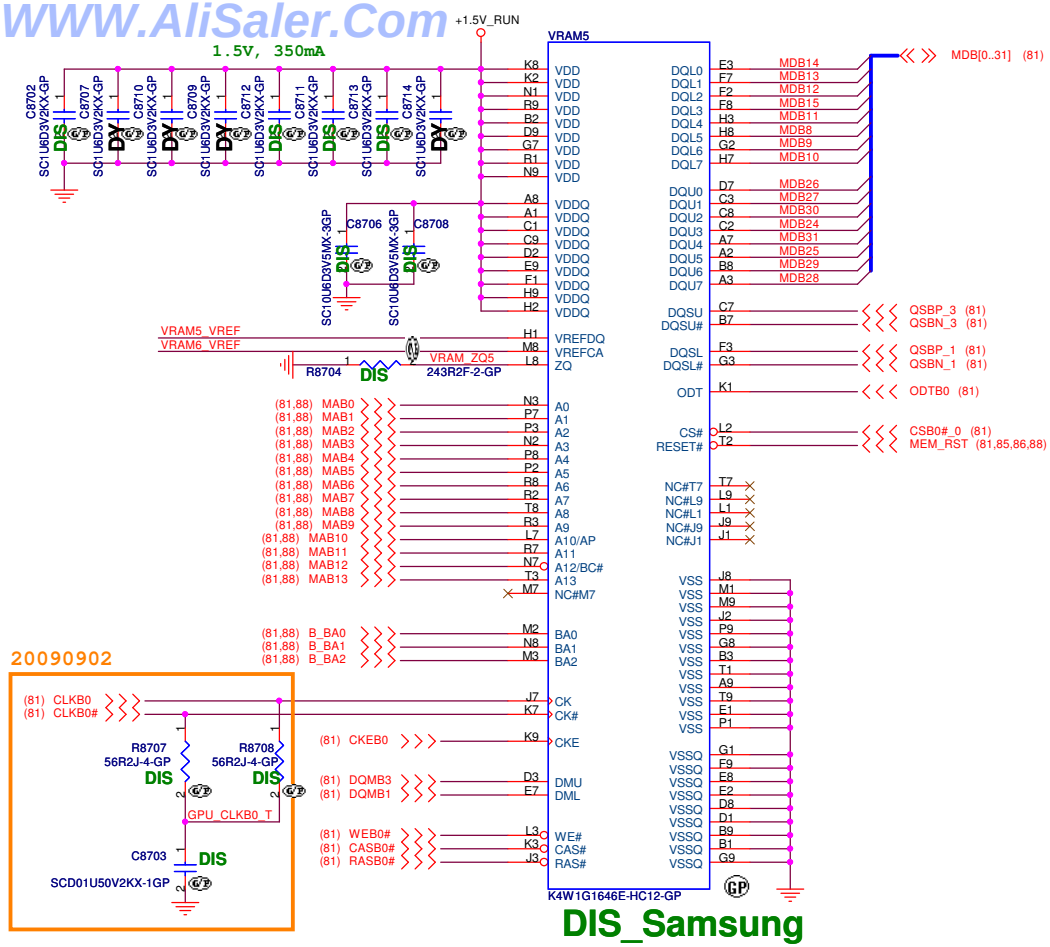
Title: GPU-VRAM3,4 (2/4)

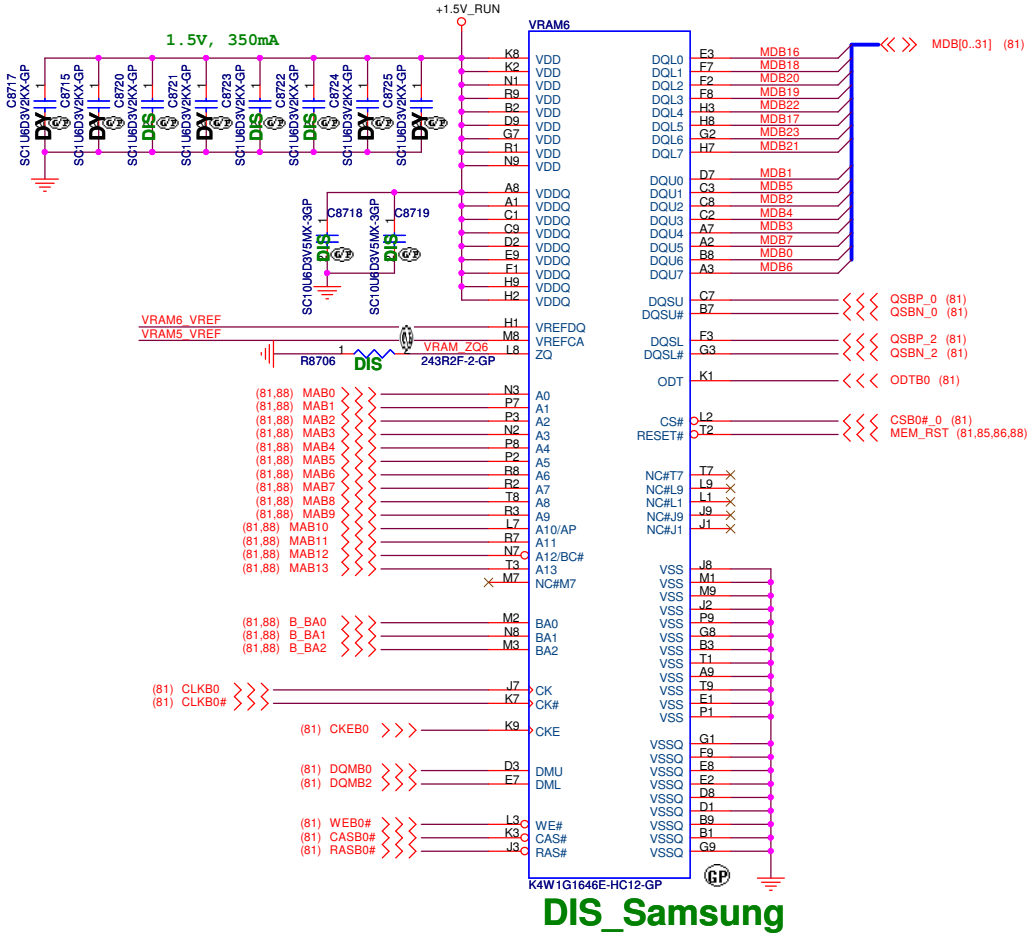
Size: A3 | Document Number: Berry | Rev: A00

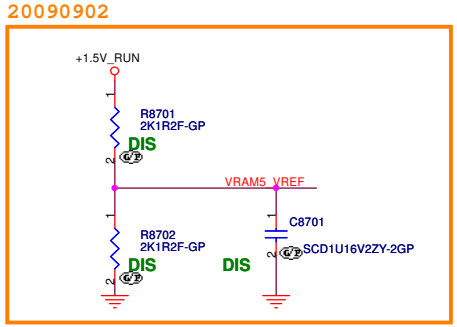
Date: Thursday, March 04, 2010 | Sheet 86 of 95

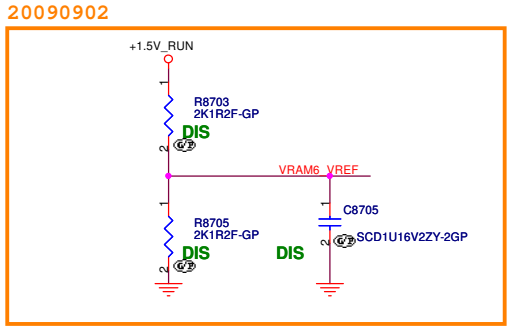
WWW.AliSaler.Com

WWW.AliSaler.Com









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

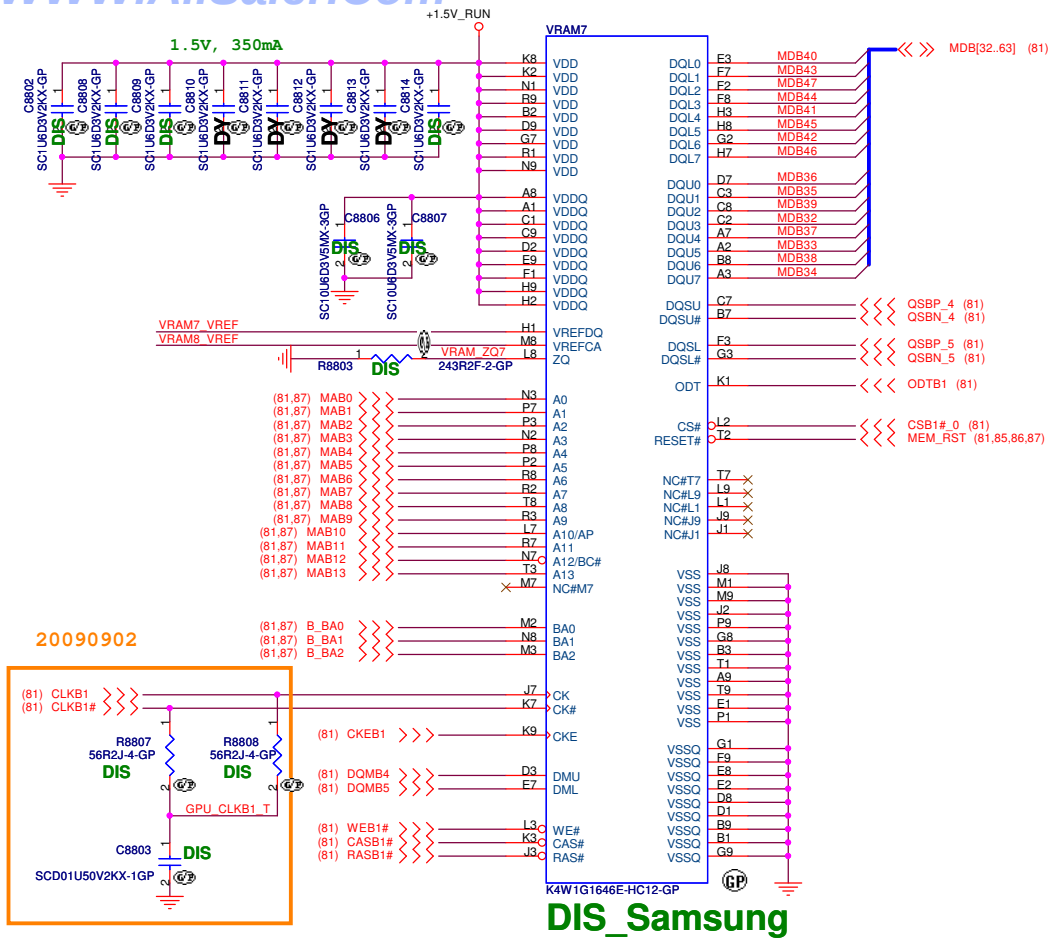
Title: GPU-VRAM5,6 (3/4)

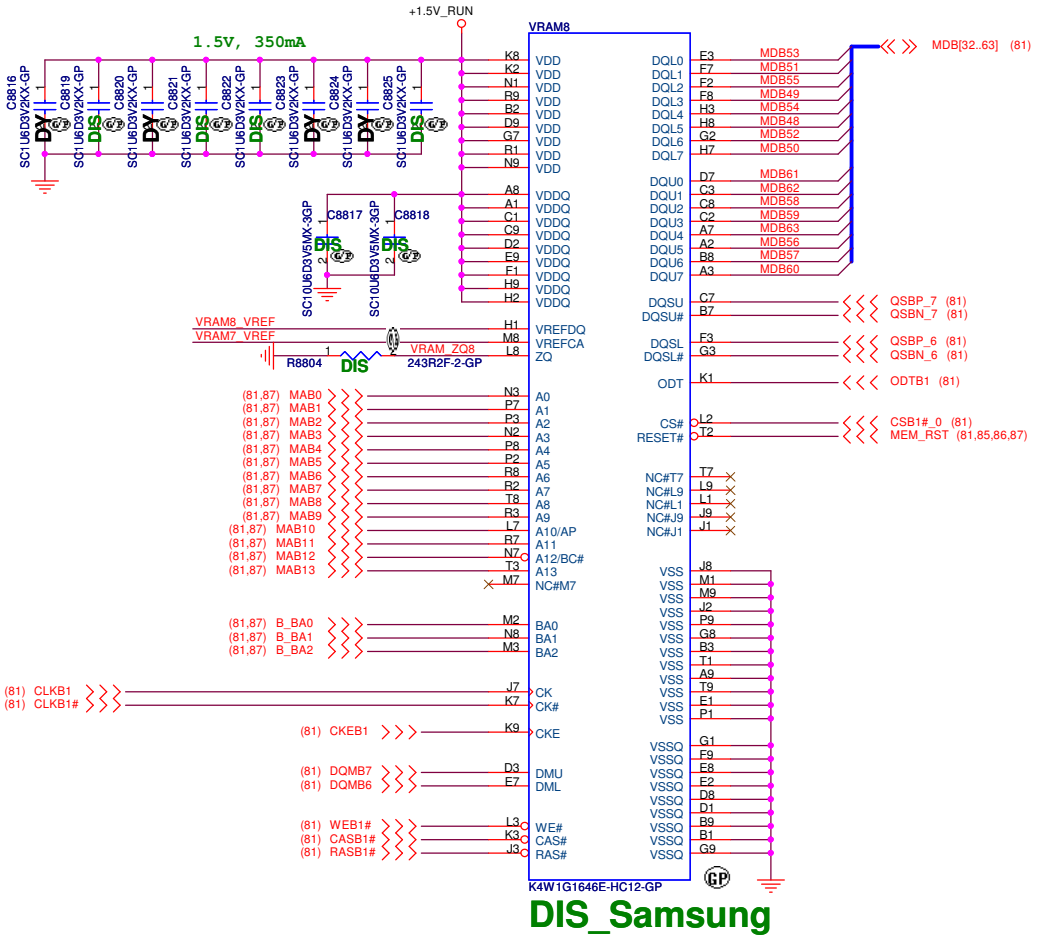
Size: A3 | Document Number: Berry | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 87 of 95

WWW.AliSaler.Com

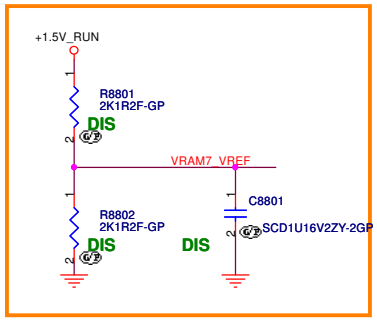
WWW.AliSaler.Com



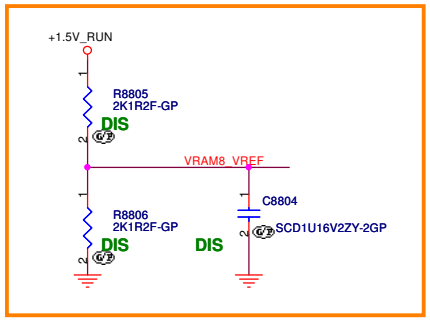


20090902

20090902



20090902



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Berry | Rev: A00

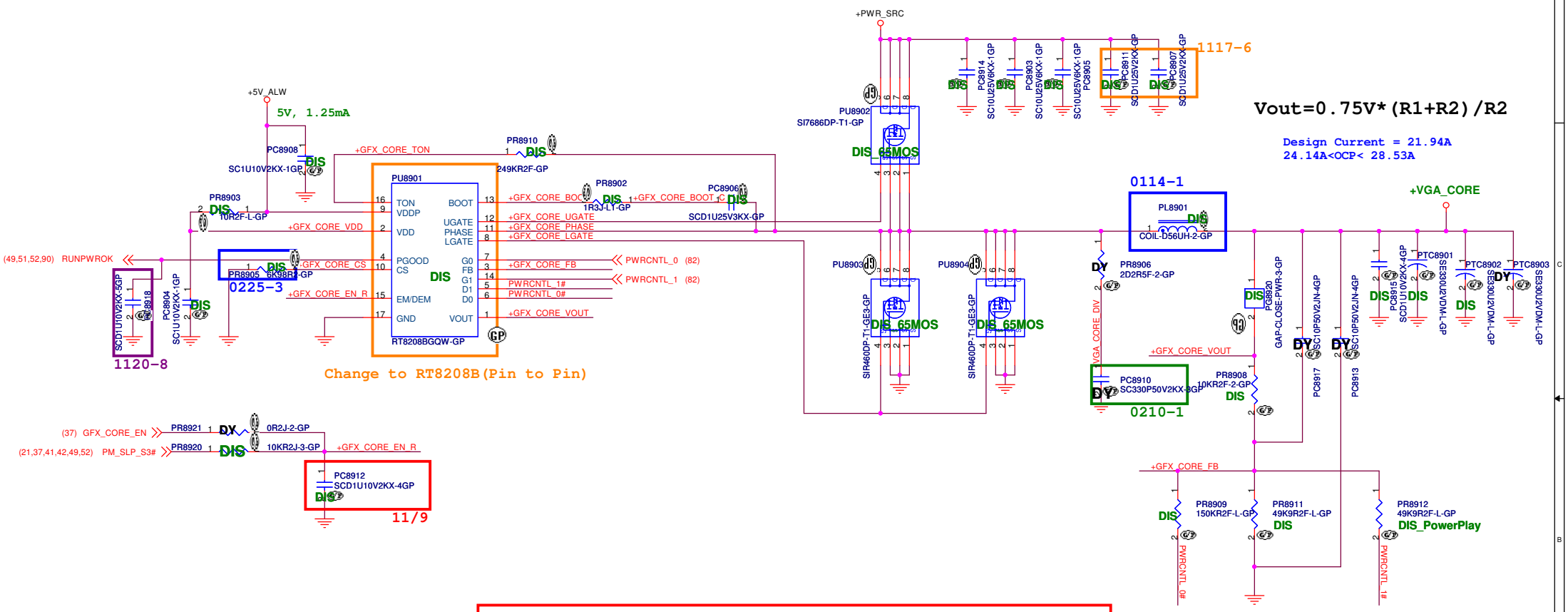
Date: Thursday, March 04, 2010 | Sheet 88 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

SSID = Video.PWR.Regulator

RT8208AGQW for +VCC_GFX_CORE



M96 Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

PR8912=49.9KR
64.49925.6DL

Park Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

PR8912=49.9KR
64.44225.6DL

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

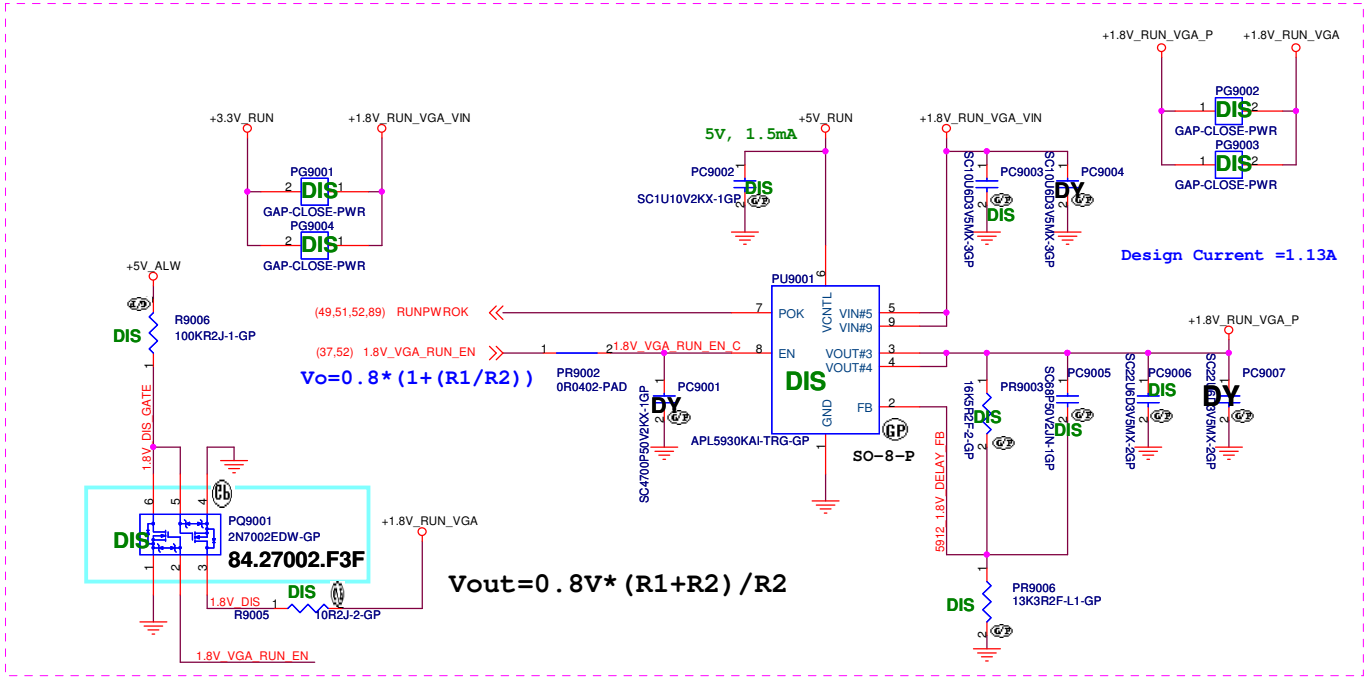
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VCC_GFXCORE
Size: A3
Document Number: Berry AMD Discrete/UMA
Rev: A00
Date: Thursday, March 04, 2010
Sheet 89 of 95

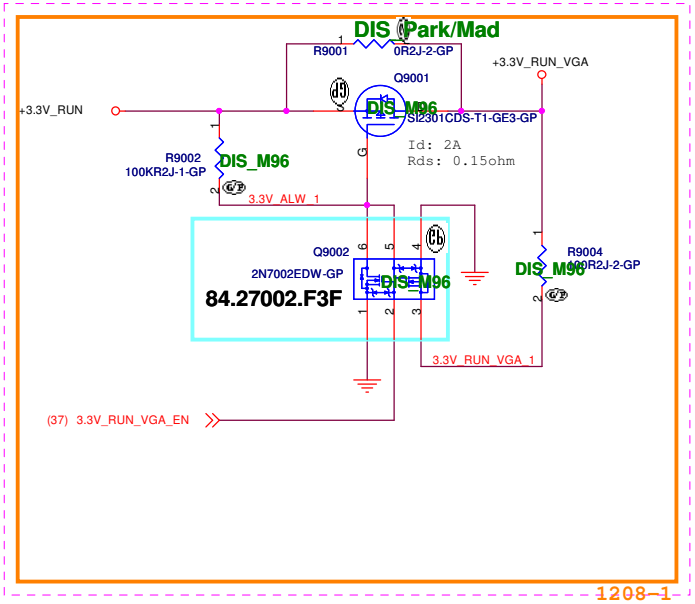
WWW.AliSaler.Com

WWW.AliSaler.Com

APL5930 for +1.8V_RUN_VGA

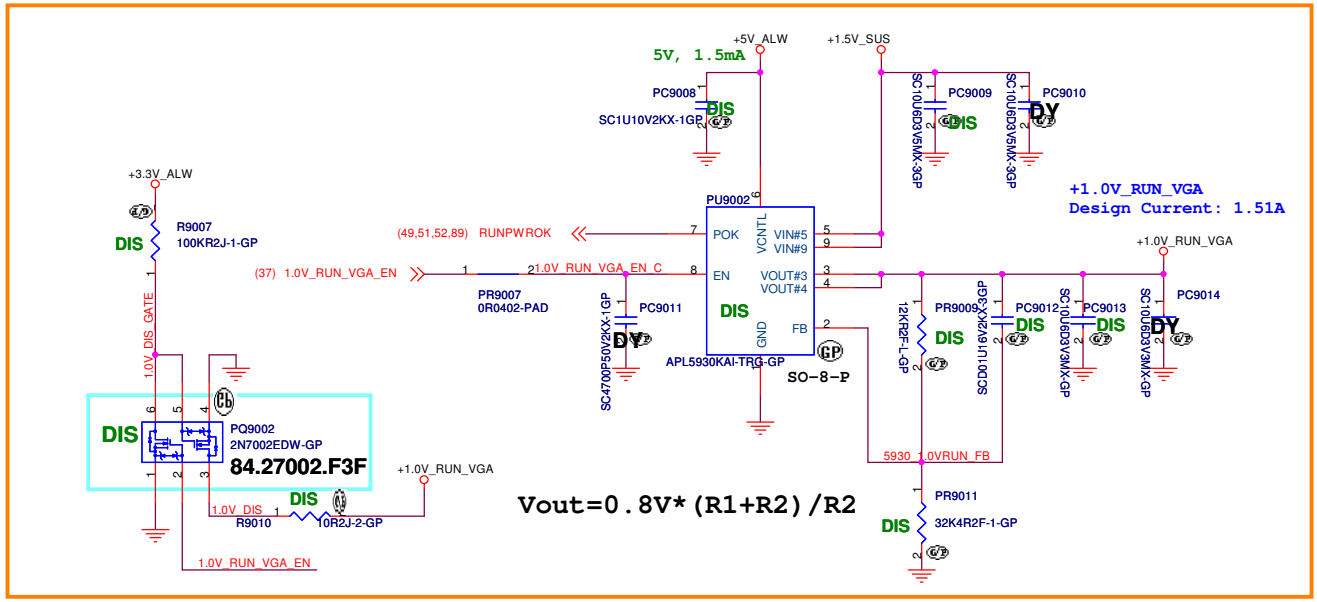


+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA

Will be Change to +1.0V_RUN_VGA



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

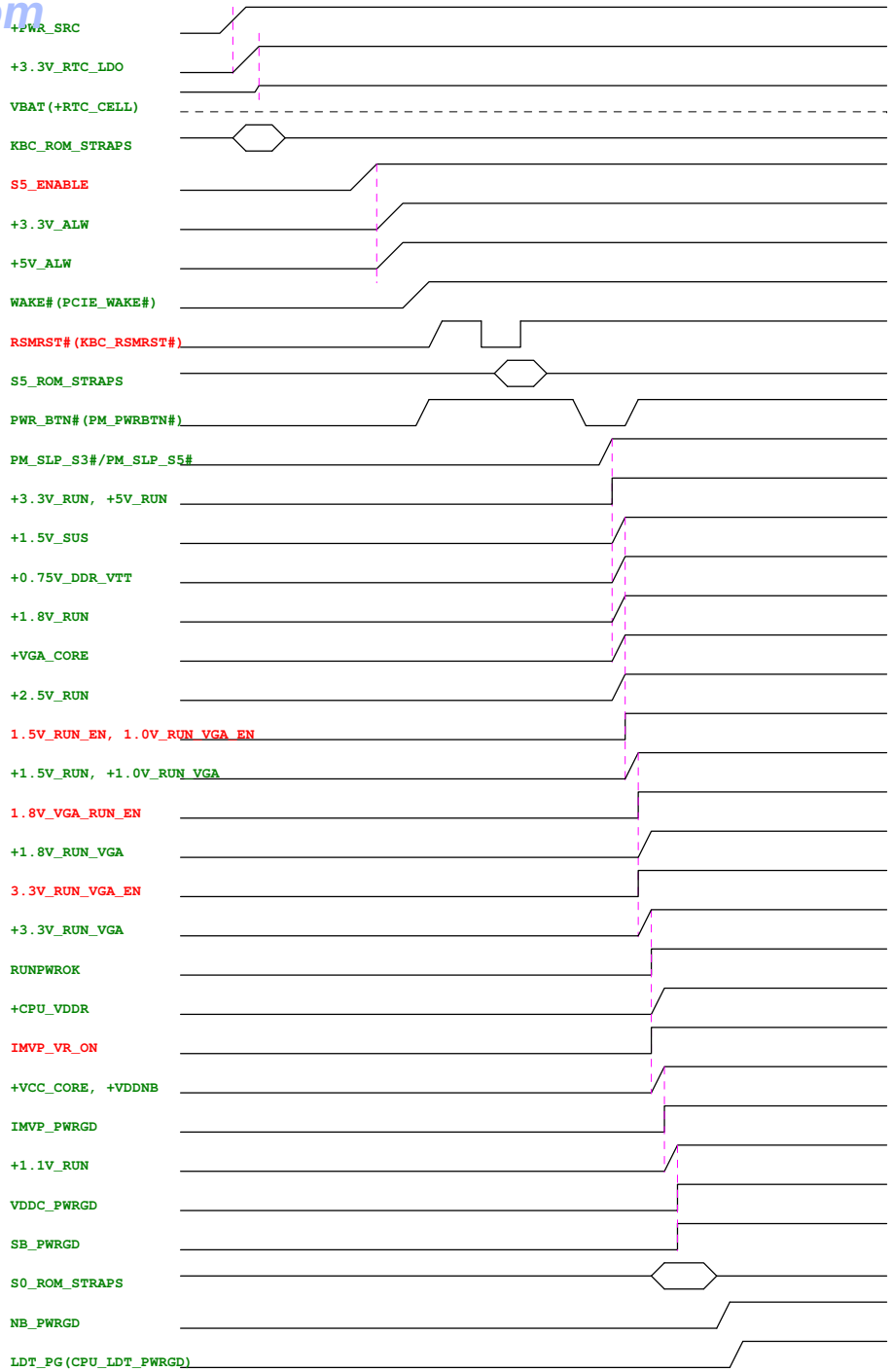
Title: DISCRETE VGA POWER

Size: A3 | Document Number: Berry | Rev: A00

Date: Tuesday, March 09, 2010 | Sheet 90 of 95

WWW.AliSaler.Com

POWER SEQUENCE



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER SEQUENCE	
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 91 of 95	

WWW.AliSaler.Com

WWW.AliSaler.Com

Change notes - Page 1

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X01	11/6	1	10	Add C1002 10uF, C1007, EC1001 0.1uF, C1008 10pF.	Insure signal quality.	EE
		2	13	Change R1314 to 4.7K.	Meet CRB.	EE
		3	51	Swap PU5101 pin3, pin4.	Correct input voltage level.	EE
		4	82	Add R8210 0R.	Reserve GPU clock input source.	EE
	11/9	1	30	Change C3014 to 2.2uF.	Reduce package size.	EE
		2	69	Change C6903 to 0.1uF.	Reduce package size.	EE
		3	49	Add PR4916 100KR.	To prevent leakage in S3 status.	EE
	11/10	1	18,19	Change DIMM socket Part Number.	Request by ME.	ME
		2	37	Add R3754 100KR.	To detect leakage current.	EE
	11/11	1	10	Modify R1028 pull-up to +1.5V_RUN.	Solve leakage in S3 status.	EE
	11/12	1	20	Change C2011 to 18pF, C2012 to 15pF.	Set accurate clock frequency.	EE
		2	37	Add C3717 10pF.	Stable singal level.	EE
		3	57	Delete RN5711, RN5705.	Redundant parts.	EE
		4	13	Delete R1331, R1332, R1308.	Redundant parts.	EE
		5	77	Add Pi-filter.	Cure EMI.	EMC
	11/13	1	20	Change X2001 P/N.	Request by Sourcer.	Sourcer
		2	7	Change R713 to 47R.	Fine tune damping.	EE
		3	82	Add R8211 80.6R, R8220 150R.	Set a voltage divider to 1.8V level swing.	EE
		4	21	Add R2133 1KR.	For UMA VRAM vendor selection.	EE
	11/16	1	22	Delete RN2203 pin 4, pin 5 connection.	Solve S5 leakage.	EE
		2	51	Change PR5105 pull-up to +3.3V_RUN.	Prevent leakage.	EE
		3	21	Add C2103, C2104 0.1uF.	For signal stability.	EE
		4	37	Add C3718 0.1uF.	For signal stability.	EE
		5	41	Add C4101, C4102 0.1uF.	For signal stability.	EE
		6	49	Add PC4923 0.1uF.	For signal stability.	EE
		7	66	Add C6601, C6602 0.1uF.	For signal stability.	EE
		8	77	Add RN7713 150R.	Move impedance matching resistor from CRT/B to M/B.	EMC
		9	78	Change CARDBD1 pin 2 link to PLTRST#_LAN_WAN.	Change card reader chip to RTS5159 to solve EMI.	EMC
	11/17	1	30	Add R3014, R3017, R3020 0R to link AGND and GND.	Issue for pop noise when system boot.	EE
		2	42,48,50	Merge 1.1V power solution on main board.	Save components.	EE, Power
		3	77	Modify CRTBD1 pin define.	Relief EMI.	EMC
		4	79	Add some decoupled capacitors.	Request by EMC.	EMC
		5	37	Change R3737 to 33R, stuff C3715 10pF.	Request by EMC.	EMC
		6	62,89	Sutff EC6203 22pF, PC8911, PC8907 0.1uF.	Request by EMC.	EMC
		7	45,46,47	Stuff EC4502 0.1uF, PC4605, PC4609, PC4738 0.1uF.	Request by EMC.	EMC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change notes

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 92 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

Change notes - Page 2

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X01	11/17	8	9	Delete R904.	Remove redundant layout trace.	EE
	11/18	1	81	Swap R8105, C8103 location.	Meet CRB.	EE
		2	79	Add some decoupled capacitor.	By RF team request.	RF
		3	49	Change PR4903 to 620KR.	Change to common part.	Power
	11/19	1	All	Synchronize with DJ schematic.	Schematic standardlize.	EE
		2	48	Change P/N for PU4802, PU4803, PU4804, PU4805.	Rquest by Power team	Power
		3	All	Review all capacitors tolerance.	Total review for deratig.	EE
		4	21	Add RN2105 0R.	Reserve to fine tune signal quality.	EE
		5	21	Change RN2101 to 4.7KR.	Fine tuned value for signal.	EA
		6	37	Add RN3705, R3755 0R.	To isolate layout trace to DB1 connector.	EA
		7	49	Change PC4908 to 2.2uF.	Changed by EA report.	EA
	11/20	1	54	Modify R5408 connection.	To synchronize with DJ.	EE
		2	57	Add D7701.	To prevent leakage from RGB monitor.	EE
		3	86	Add C8626 0.1uF.	By EA report.	EA
		4	37	Add R3756 10KR, C3720 0.1uF.	Synchronize with DJ.	EE
		5	37	Delete RN3705, R3755.	For more layout space.	EE
		6	13	Delete TP1303, TP1304.	For more layout space.	EE
		7	49	Delete PR4905.	For more layout space.	EE
		8	89	Add PC8918 0.1uF.	Stable signal quality.	EE
	11/24	1	46,49	Change PU4601, PU4901 Power components.	Request by Power team.	Power
	11/25	1	46,47,49,89	Change power components.	Request by Power team.	Power
	11/29	1	10	Change C1008 to 10pF.	Fine tuned signal slew rate to meet specification.	EE
		2	30	Change R3007 to 2.2KR.	By FAE suggestion.	EE
X02	12/04	1	81	Set BOM mark R8104, R8106, R8107, R8110, R8111, R8112.	Implement co-layout Madison and M96.	EE
		2	82,84	Add R8407, R8408 0R.	Implement co-layout Madison and M96.	EE
		3	80	Add R8016 10KR.	Implement co-layout Madison and M96.	EE
		4	83,84	Set BOM mark.	Implement co-layout Madison and M96.	EE
		5	83	Add L8306, L8307, C8397, R8301, R8302, R8303.	Implement co-layout Madison and M96.	EE
	12/05	1	37	Change R3756, C3720 connection.	Correct soft-start for EC power.	EE
	12/08	1	90	Set BOM mark.	Implement co-layout Madison and M96.	EE
	12/15	1	15	Delete RN1501, Add G1501~G1504.	Synchronize with DJ and supply sufficient power rail.	EE
		2	62	Add R6207 100KR.	Insure SPI Write-Protect pin signal level.	EE
		3	66	Change C6602 net name.	Correct signal name.	EE
		4	81	Add R8122 1KR, RN8101 4.7KR.	Meet M96 schematic check list.	EE
		5	82	Swap CLK_VGA_27M_NSS and CLK_VGA_27M_SS connection.	Solve external RGB display tremble issue.	EE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change notes

Size: A3 | Document Number: Berry AMD Discrete/UMA | Rev: A00

Date: Thursday, March 04, 2010 | Sheet 93 of 95

WWW.AliSaler.Com

WWW.AliSaler.Com

Change notes - Page 3

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	12/16	1	66	Change R6605 to 0R.	Assure power button level set to low.	EE
		2	37,76	Add net "8103_GPO".	Implement LAN DSM hardware function.	EE
	12/17	1	37	Add U3703.	To solve SPI WP signal malfunction on EC.	EE
	12/18	1	82	Add R8222 1MR.	Assure crystal resonant clock stable.	EE
		2	81	Set VRAM reset circuit.	Follow M96 reset circuit and reseve BOM option.	EE
	12/25	1	18	Change TC1801 to 330uF, 2V tolerance.	Implement common part for 1.5V power rail.	EE
		2	46	Change PR4603 to 127KR.	Set 5V current limitation.	Power
		3	46	Empty PR4618 and stuff PR4619.	Set Ultra-sonic mode to keep +15V_ALW voltage level.	Power
		4	10	Set RN1006 PU to +1.5V_SUS.	Follow AMD check list and cure +1.5V_RUN leakage.	EE
		5	62	Change R6206 to 1KR.	According to Safety request, verified OK.	Safety
		6	51	Change PR5102 1KR, PR5106 8.2KR, PR5107 5.62KR.	Set VDDR low voltage level to 0.9V.	EE
	12/29	1	10,37	Add Q1005, R1039, R1040.	Request by AMD to set CPU into HTC mode in DOS.	EE
		2	47	Change PR4720 93.1KR, PR4721 24KR.	Set power OCP value.	Power
	12/31	1	ALL	Change some resistors as short-pad or resistor array.	Save component counts.	EE
		2	ALL	Change some capacitors with smaller value or empty.	Save component counts.	EE
	01/04	1	15	Change R1507,R1508,R1509,R1510,R1511 to bead.	Filter power noise.	EMC
	01/05	1	7	Combine R707,R721 as RN711.	For more layout space.	EE
		2	81	Delete TP8101,TP8102.	Remove useless test point for more layout space.	EE
		3	7,80	Delete R716,R8020, combine R8009,R8010 as RN8001.	Redundant part.	EE
		4	37,39,41	R3747,R4104 short pad, delete R3722,R3904.	Redundant part.	EE
		5	46	Change PR4620 as short pad.	Redundant part.	EE
		6	51	Change PQ5101 with ESD protector.	Change to common part.	Power
		7	54	Empty R5405 and Stuff R5408.	Avoid LCD white panel.	EE
		8	62	Change R6205 to 0R.	Already have one 1KR ahead.	EE
	01/06	1	50	Add PR5004 10KR and empty PR5002.	Avoid +1.1V_ALW leakage in South Bridge.	EE
		2	13	Change R1342 to size 0603.	Synchronous schematic w/DJ.	EE
		3	79	Add R7921 and R7922.	Reserved RF team solution.	RF
	01/07	1	7	Add RN712,C722,C723	Reserve for SMBus signal quality tuning.	EE
		2	60	Change EC6007,EC6008 to 0.01uF.	According FAE Request.	IDT FAE
		3	39	Add Q3904.	According thermal team request.	Thermal
		4	21,18	Change location RN2105 to RN1801, add C1823,C1824.	For SMBus signal quality fine tune.	EE
		5	39,82,83	Remove C3912,TP8301,TP8302,TP8213.	Remove dummy part for more layout space.	EE
		6	76	Reserve C7601, C7602.	Fine tune USB signal quality.	EE
	01/08	1	79	Reserve EC7925,EC7926,EC7927.	Reserve by EMC team.	EMC
		2	77	Change RN7711 to 0R, L7701,L7702,L7703 to bead 22R.	According EMC measurement result.	EMC

0108

WWW.AliSaler.Com

WWW.AliSaler.Com

Change notes - Page 4

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	01/08	3	18,19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	According ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 0R.	Add 0R for level shift off.	EE
	01/13	1	21,37	Add C3725, C2105.	Reserve for singal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory requst.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
	02/25	1	13	Add TP1309.	As factory requset to add.	Factory
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE
		3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
		5	79	Remove EC7928.	Layout space limitation.	EE
	02/26	1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
	03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE
	03/08	1	48	Stuff PU4803 and empty PU4804.	Place the H/S and L/S MOS at the same surface.	Power

0308-1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change notes

Size: A3 | Document Number: Berry | Rev: A00

Date: Monday, March 08, 2010 | Sheet 95 of 95

WWW.AliSaler.Com