

# Compal Confidential

## DAT20 Schematics Document

### Banias uFCPGA Package with 855PM(Odem) + ICH4-M

2003-09-25

REV: 0.3

**Compal Electronics, Inc.**

Title

**Cover Sheet**

Size

Document Number

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**DAT20 LA-1971**

Rev

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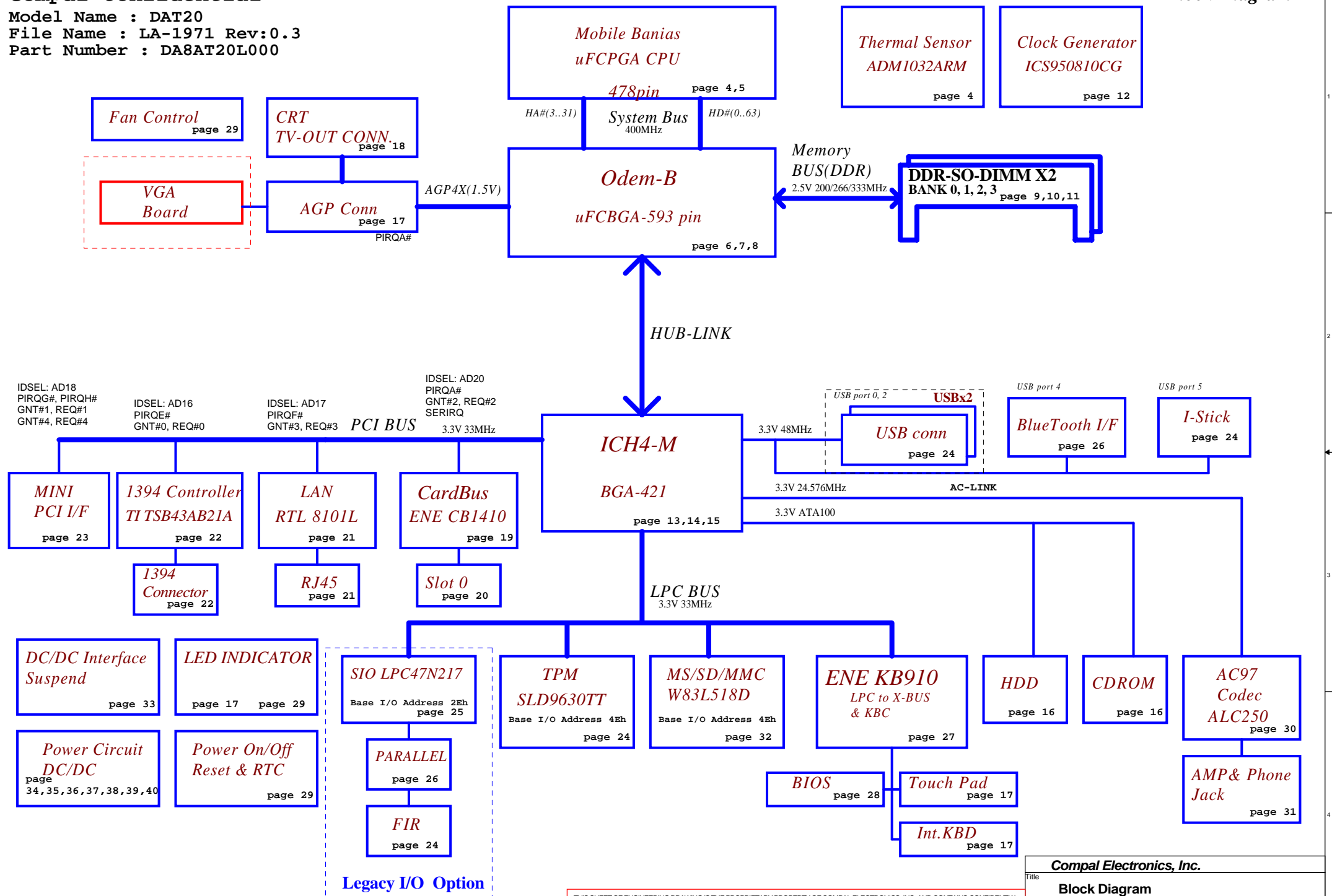
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Model Name : DAT20

File Name : LA-1971 Rev:0.3

Part Number : DA8AT20L000

## Block Diagram



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## Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for MCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18,AD22	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b		
(24C04)	1011 000Xb		

## EC SM Bus2 address

## ICH4-M SM Bus address

Device	Address
Clock Generator (ICS950810CG)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 001Xb

## Board ID Table for AD channel

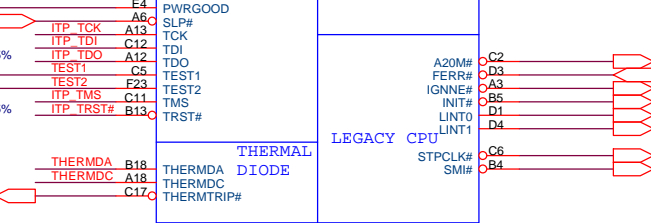
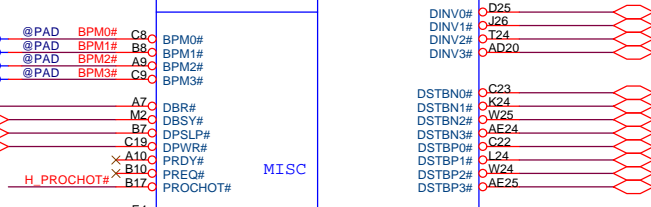
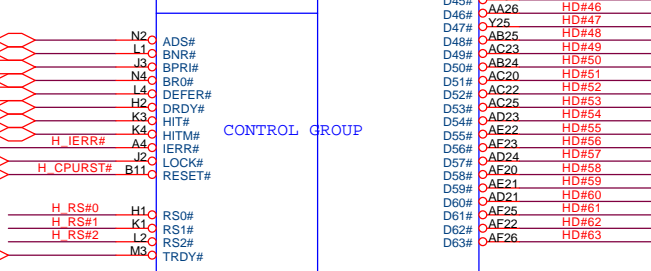
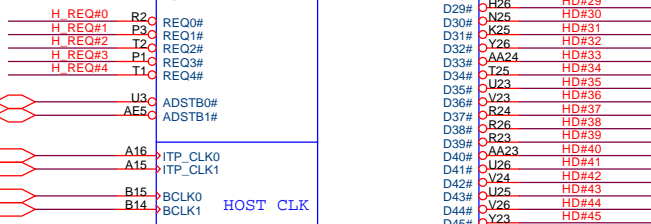
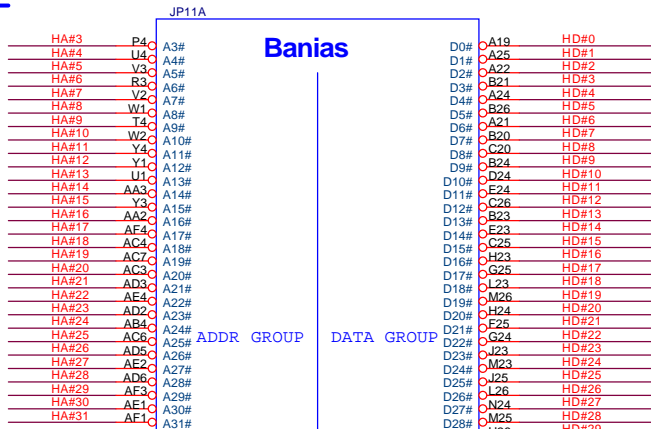
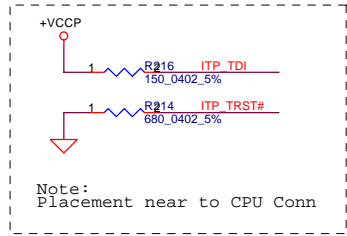
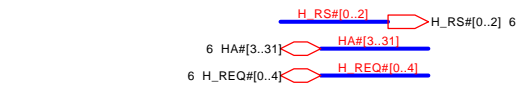
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
* 1	0.2
2	0.3
3	0.4
4	
5	
6	
7	

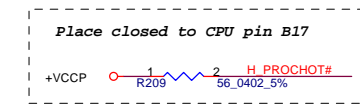
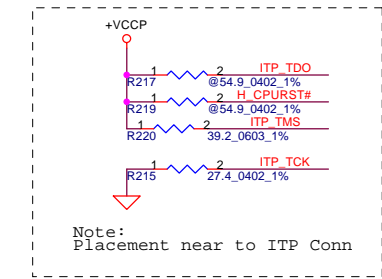
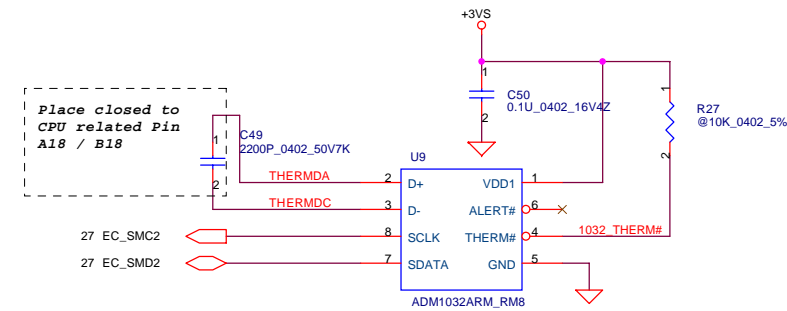
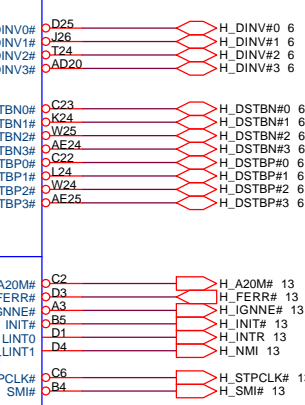
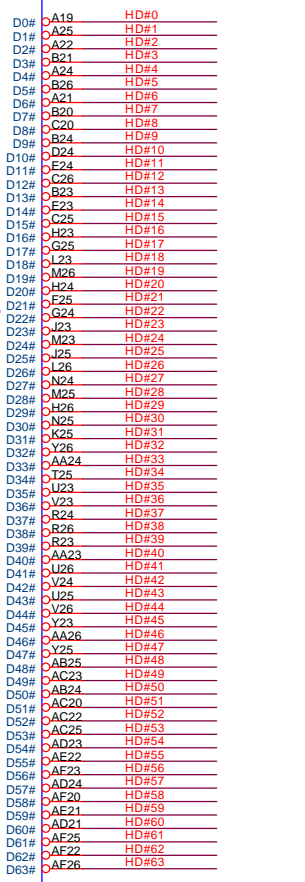
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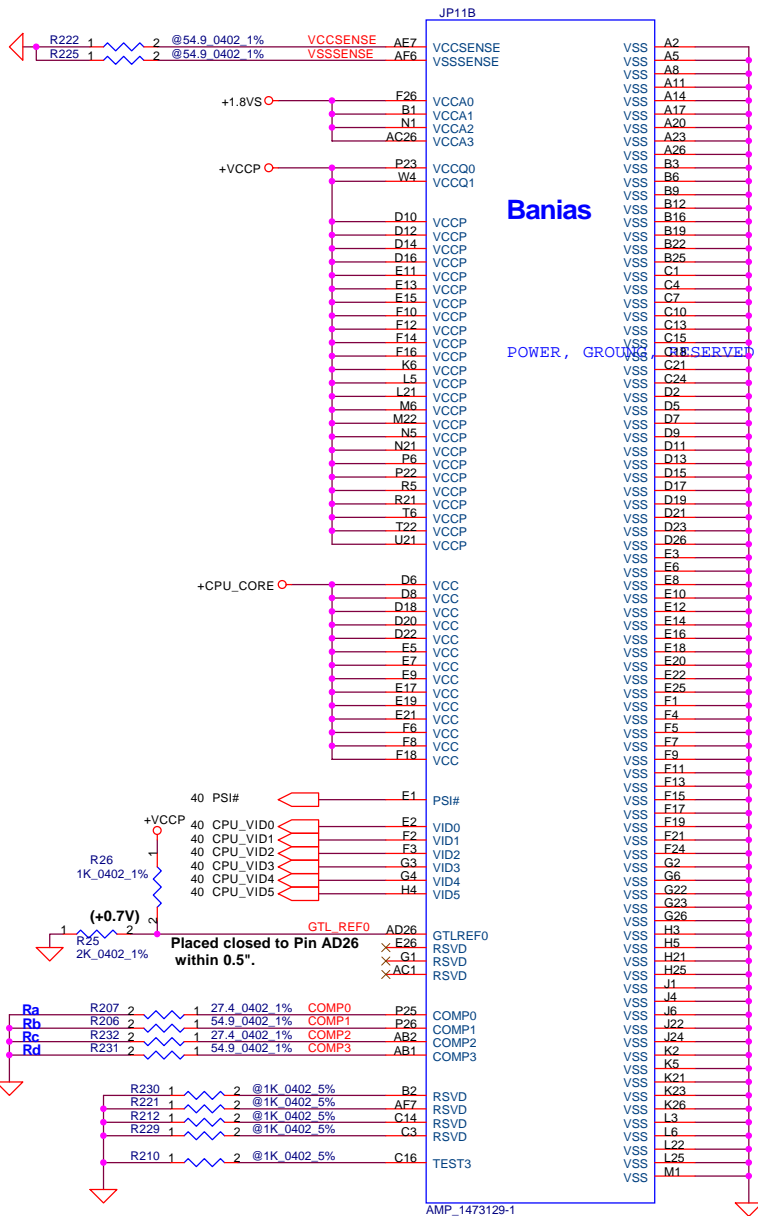


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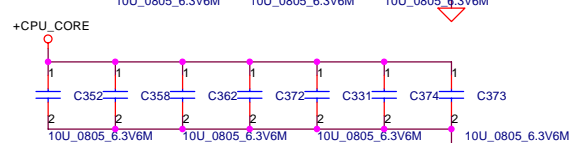
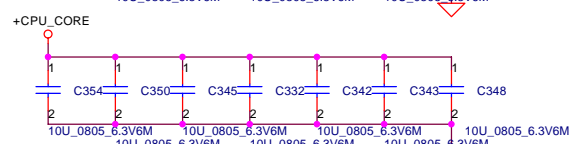
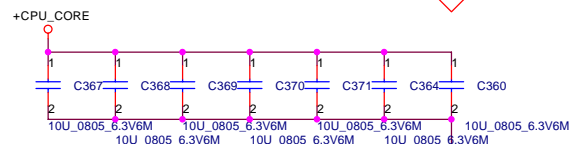
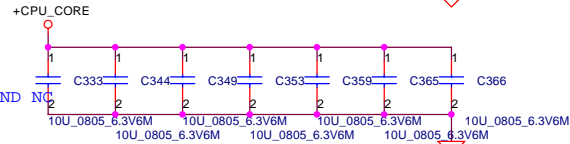
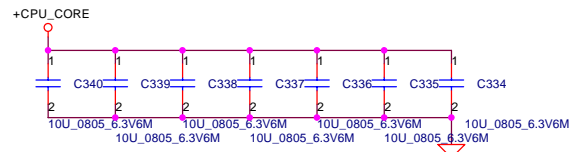
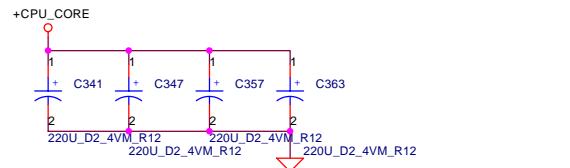


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Title Banias Processor in mFCPGA479 (1/2)			
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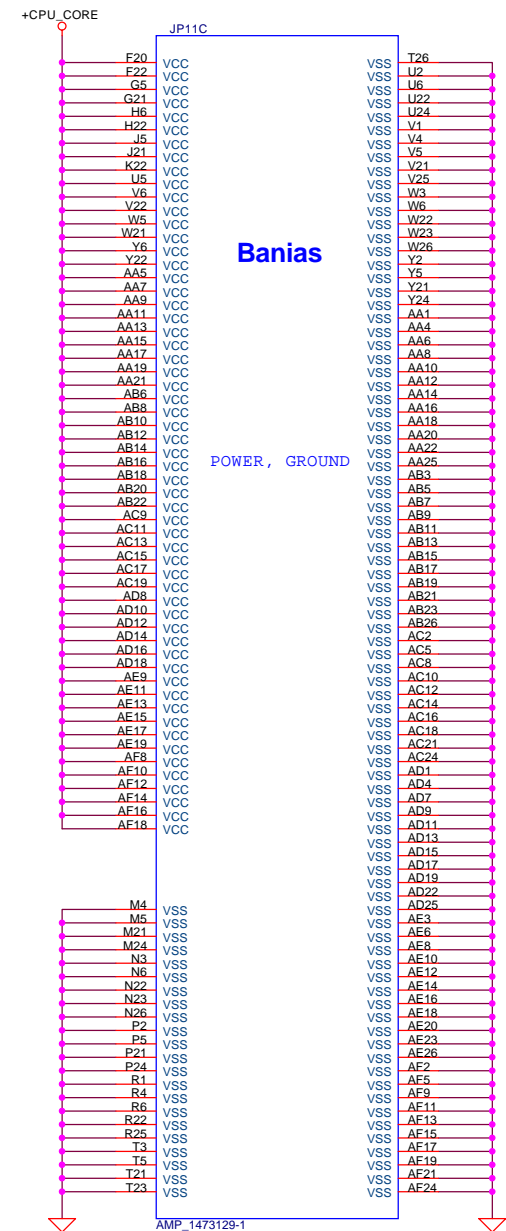
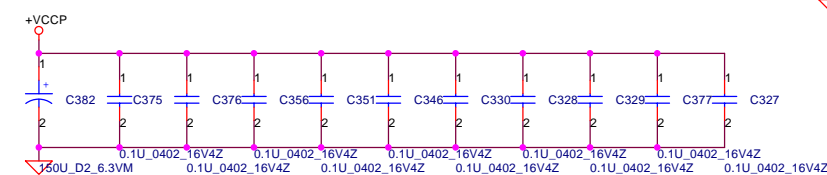
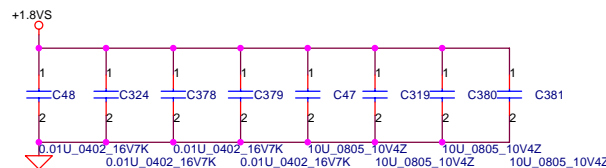
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Ra, Rb, Rc, Rd placed close to related pin within 0.5".  
COMP0/1/2/3 Trace should 25mil away from any other toggling signal.



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



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4 H\_RS#[0..2] H\_RS#[0..2]  
4 HA#[3..31] HA#[3..31]  
4 H\_REQ#[0..4] H\_REQ#[0..4]

HD#[0..63] HD#[0..63] 4

HUB\_PD#[0..10] HUB\_PD#[0..10] 13

U8A

Odem

HOST

HA#3 U6 HA#3  
HA#4 T5 HA#4  
HA#5 R2 HA#5  
HA#6 U3 HA#6  
HA#7 R3 HA#7  
HA#8 P7 HA#8  
HA#9 T3 HA#9  
HA#10 P4 HA#10  
HA#11 P3 HA#11  
HA#12 P5 HA#12  
HA#13 R6 HA#13  
HA#14 N2 HA#14  
HA#15 N2 HA#14  
HA#16 N3 HA#15  
HA#17 J3 HA#16  
HA#18 M3 HA#18  
HA#19 M4 HA#19  
HA#20 M5 HA#20  
HA#21 L5 HA#21  
HA#22 K3 HA#22  
HA#23 J2 HA#23  
HA#24 N6 HA#24  
HA#25 L6 HA#25  
HA#26 L2 HA#26  
HA#27 K9 HA#27  
HA#28 L3 HA#28  
HA#29 L7 HA#28  
HA#30 K4 HA#30  
HA#31 J5 HA#31

H\_REQ#0 U2 HREQ#0  
H\_REQ#1 T7 HREQ#1  
H\_REQ#2 R7 HREQ#2  
H\_REQ#3 U5 HREQ#3  
H\_REQ#4 T4 HREQ#4

4 H\_ADSTB#0 R5 HADSTB#0  
4 H\_ADSTB#1 N7 HADSTB#1

12 CLK\_MCH\_BCLK# K8 BCLK#  
12 CLK\_MCH\_BCLK# J8 BCLK

4 H\_ADS# U7 ADS#  
4 H\_TRDY# V4 HTRDY#  
4 H\_DRDY# W2 DRDY#  
4 H\_DEFER# Y4 DEFER#  
4 H\_HITM# Y5 HITM#  
4 H\_HIT# W3 HIT#  
4 H\_LOCK# V7 HLOCK#  
4 H\_BR0# V3 BR0#  
4 H\_BNR# V7 BNR#  
4 H\_BPRI# V5 BPRI#  
4 H\_DBSY# W7 DBSY#  
H\_RS#0 W5 RS#0  
H\_RS#1 W5 RS#1  
H\_RS#2 W6 RS#2

4 H\_CPURST# AE17 CPURST#

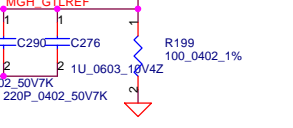
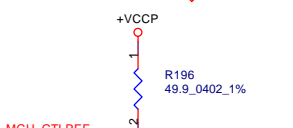
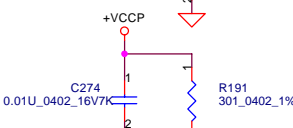
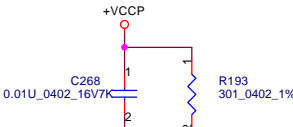
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4 H\_DSTBN#1 AF2 HDSTBN#1  
4 H\_DSTBN#2 AC15 HDSTBN#2  
4 H\_DSTBN#3 AC15 HDSTBN#3  
4 H\_DSTBP#0 AG6 HDSTBP#0  
4 H\_DSTBP#1 AE11 HDSTBP#1  
4 H\_DSTBP#2 AC16 HDSTBP#2  
4 H\_DSTBP#3 AD5C HDSTBP#3  
4 H\_DINV#0 AG5 DBI#0  
4 H\_DINV#1 AH9 DBI#1  
4 H\_DINV#2 AH9 DBI#2  
4 H\_DINV#3 AD15C DBI#3

HD#0 AA2 HD#0  
HD#1 AB5 HD#1  
HD#2 AA5 HD#2  
HD#3 AB3 HD#3  
HD#4 AB4 HD#4  
HD#5 AC5 HD#5  
HD#6 AA3 HD#6  
HD#7 AA6 HD#7  
HD#8 AE3 HD#8  
HD#9 AB7 HD#9  
HD#10 AE5 HD#10  
HD#11 AC3 HD#11  
HD#12 AC3 HD#12  
HD#13 AC3 HD#13  
HD#14 AF4 HD#14  
HD#15 AE2 HD#15  
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HD#17 AE7 HD#17  
HD#18 AE8 HD#18  
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HD#23 AD7 HD#23  
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HD#26 AG8 HD#26  
HD#27 AG8 HD#27  
HD#28 AG7 HD#28  
HD#29 AH3 HD#29  
HD#30 AF8 HD#30  
HD#31 AC11 HD#31  
HD#32 AC12 HD#32  
HD#33 AE9 HD#33  
HD#34 AC10 HD#34  
HD#35 AE10 HD#35  
HD#36 AC9 HD#36  
HD#37 AC9 HD#37  
HD#38 AC9 HD#38  
HD#39 AC12 HD#39  
HD#40 AE10 HD#40  
HD#41 AC11 HD#41  
HD#42 AC11 HD#42  
HD#43 AH11 HD#43  
HD#44 AG12 HD#44  
HD#45 AE13 HD#45  
HD#46 AF12 HD#46  
HD#47 AC13 HD#47  
HD#48 AH13 HD#48  
HD#49 AH13 HD#49  
HD#50 AC14 HD#50  
HD#51 AE14 HD#51  
HD#52 AG14 HD#52  
HD#53 AE14 HD#53  
HD#54 AG15 HD#54  
HD#55 AG16 HD#55  
HD#56 AG17 HD#56  
HD#57 AH15 HD#57  
HD#58 AC17 HD#58  
HD#59 AE16 HD#59  
HD#60 AE15 HD#60  
HD#61 AH17 HD#61  
HD#62 AD17 HD#62  
HD#63 AE16 HD#63

HVREF0 M7  
HVREF1 P8  
HVREF2 AA9  
HVREF3 AB12  
HVREF4 AB16

HSWNG1 AD13 H SWNG1  
HSWNG0 AA7 H SWNG0

HRCOMP1 AC13 H RCOMP1  
HRCOMP0 AC2 H RCOMP0



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AGP AD0 R27  
AGP AD1 R28  
AGP AD2 T25  
AGP AD3 R25  
AGP AD4 T26  
AGP AD5 T27  
AGP AD6 U27  
AGP AD7 U28  
AGP AD8 V26  
AGP AD9 V27  
AGP AD10 T23  
AGP AD11 U23  
AGP AD12 T24  
AGP AD13 U24  
AGP AD14 U25  
AGP AD15 V24  
AGP AD16 Y27  
AGP AD17 Y26  
AGP AD18 AA28  
AGP AD19 AB25  
AGP AD20 AB27  
AGP AD21 AB27  
AGP AD22 AB26  
AGP AD23 Y23  
AGP AD24 AB23  
AGP AD25 AA24  
AGP AD26 AA25  
AGP AD27 AB24  
AGP AD28 AC25  
AGP AD29 AC24  
AGP AD30 AC24  
AGP AD31 AC22

AGP C/BE#0 V25  
AGP C/BE#1 V23  
AGP C/BE#2 Y25  
AGP C/BE#3 AA23

AGP FRAME# Y24  
AGP DEVSEL# W28  
AGP IRDY# W27  
AGP TRDY# W24  
AGP STOP# W23  
AGP PAR W25  
AGP REQ# AG24  
AGP GNT# AH25

AGP ADSTB0 R24  
AGP ADSTB#0 R23  
AGP ADSTB1 AC27  
AGP ADSTB1# AC28

AGP SBA0 AH28  
AGP SBA1 AH27  
AGP SBA2 AG28  
AGP SBA3 AG27  
AGP SBA4 AE28  
AGP SBA5 AE27  
AGP SBA6 AE24  
AGP SBA7 AE25

AGP SBSTB AF27  
AGP SBSTB# AF26  
AGP RBF# AE22  
AGP WBF# AE23  
AGP PIPE# AE22

AGP ST0 AG25  
AGP ST1 AG24  
AGP ST2 AG26

CLK MCH 66M P22

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

CLK MCH 66M

U8B

Odem

HUB

AGP

GND

HI\_0 P25 HUB\_PD0  
HI\_1 P24 HUB\_PD1  
HI\_2 N27 HUB\_PD2  
HI\_3 P23 HUB\_PD3  
HI\_4 M26 HUB\_PD4  
HI\_5 M25 HUB\_PD5  
HI\_6 L28 HUB\_PD6  
HI\_7 L27 HUB\_PD7  
HI\_8 M27 HUB\_PD8  
HI\_9 M24 HUB\_PD9  
HI\_10 M24 HUB\_PD10

HI\_STB N25  
HI\_STB# N24  
HLRCOMP P27  
HI\_REF P26

HUB\_PSTRB 13  
HUB\_PSTRB# 13

HUB\_RCOMP 1  
HUB\_VREF

HUB\_VREF

HUB\_VREF

HUB\_VREF

HUB\_VREF

HUB\_VREF

HUB\_VREF

HUB\_VREF

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ST1	ST2	MCH	STRAP
X	1	DDR	
0	X	TEST MODE	
1	X	400 Mhz	PSB

Note:  
Ra & Rb placed at center of MCH and AGP

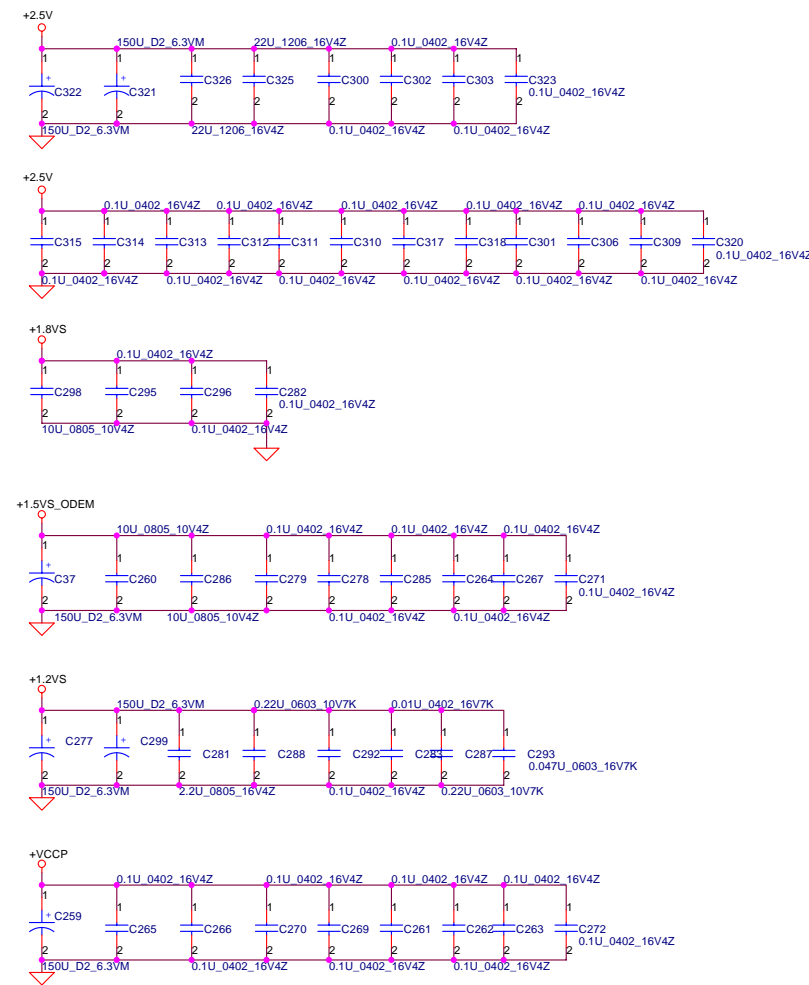
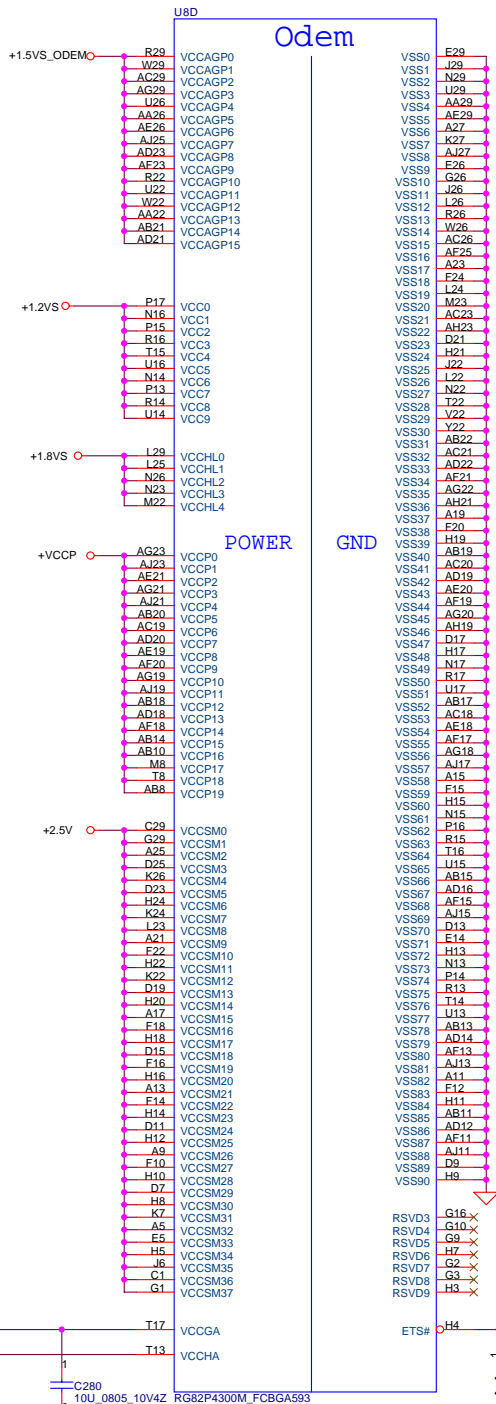
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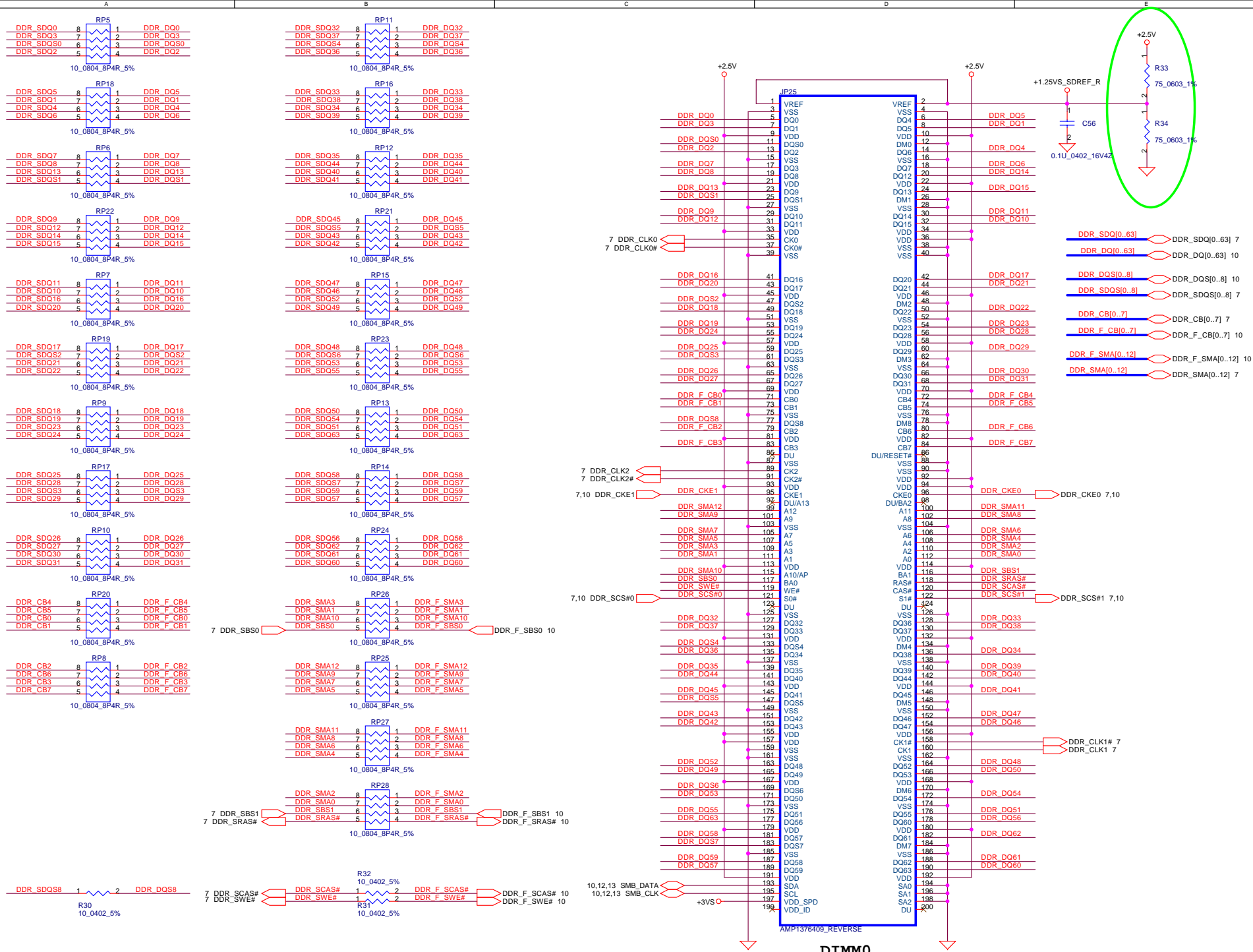
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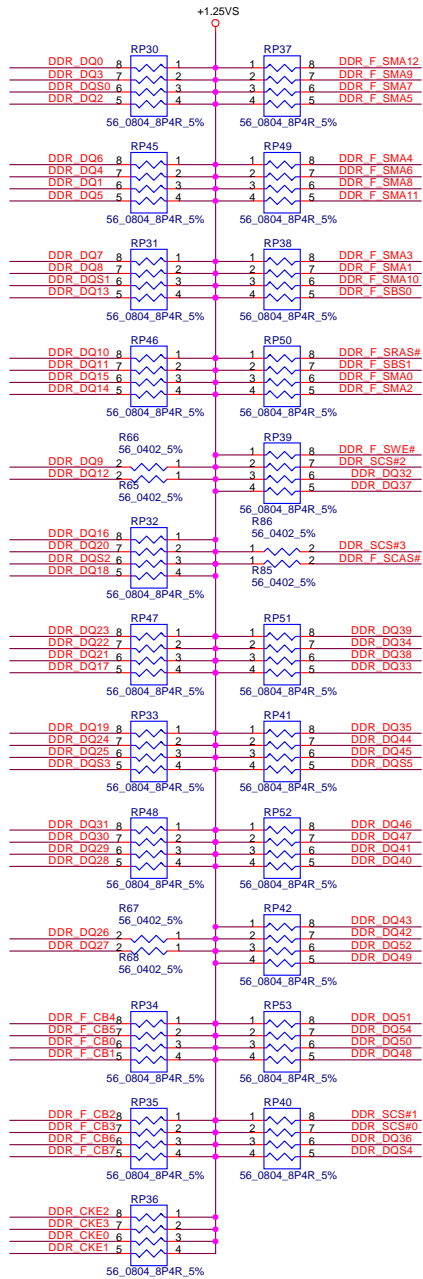




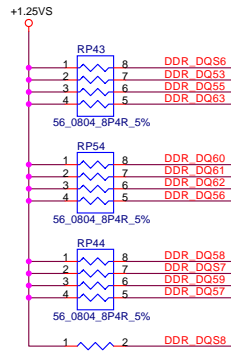


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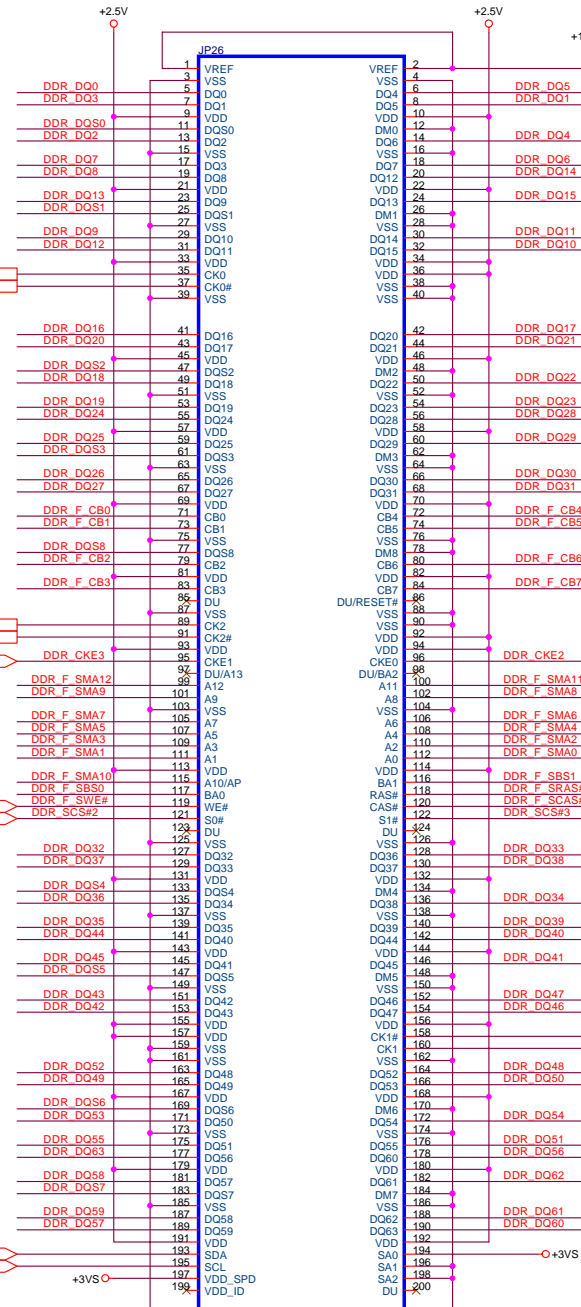
DDR\_F\_SBS0 → DDR\_F\_SBS0 9  
 DDR\_F\_SBS1 → DDR\_F\_SBS1 9  
 DDR\_SCS#0 → DDR\_SCS#0 7,9  
 DDR\_SCS#1 → DDR\_SCS#1 7,9  
 DDR\_CKE0 → DDR\_CKE0 7,9  
 DDR\_CKE1 → DDR\_CKE1 7,9



R64 56\_0402\_5%  
 R65 56\_0402\_5%  
 R66 56\_0402\_5%  
 R67 56\_0402\_5%  
 R68 56\_0402\_5%



DDR\_F\_SBS0 → DDR\_F\_SBS0 9  
 DDR\_F\_SBS1 → DDR\_F\_SBS1 9  
 DDR\_SCS#0 → DDR\_SCS#0 7,9  
 DDR\_SCS#1 → DDR\_SCS#1 7,9  
 DDR\_CKE0 → DDR\_CKE0 7,9  
 DDR\_CKE1 → DDR\_CKE1 7,9



DIMM1

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

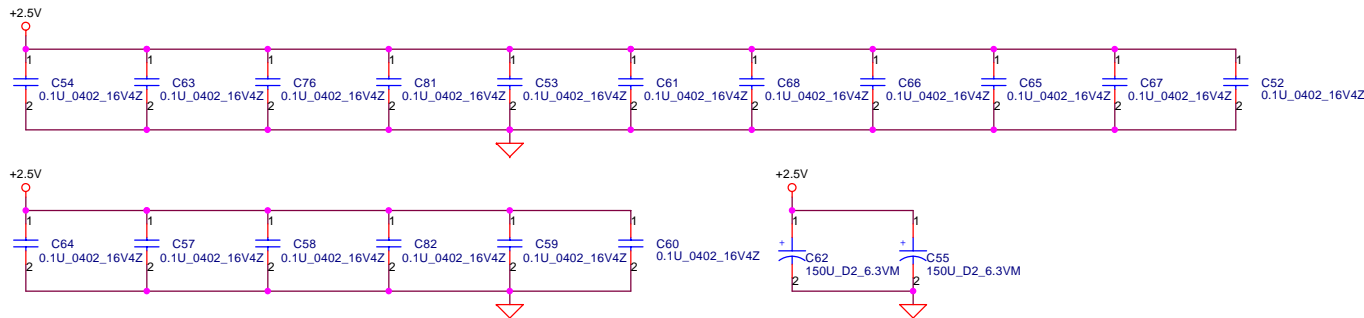
DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

DDR\_F\_SMA[0..12] → DDR\_F\_SMA[0..12] 9  
 DDR\_DQ[0..63] → DDR\_DQ[0..63] 9  
 DDR\_DQS[0..8] → DDR\_DQS[0..8] 9  
 DDR\_F\_CB[0..7] → DDR\_F\_CB[0..7] 9

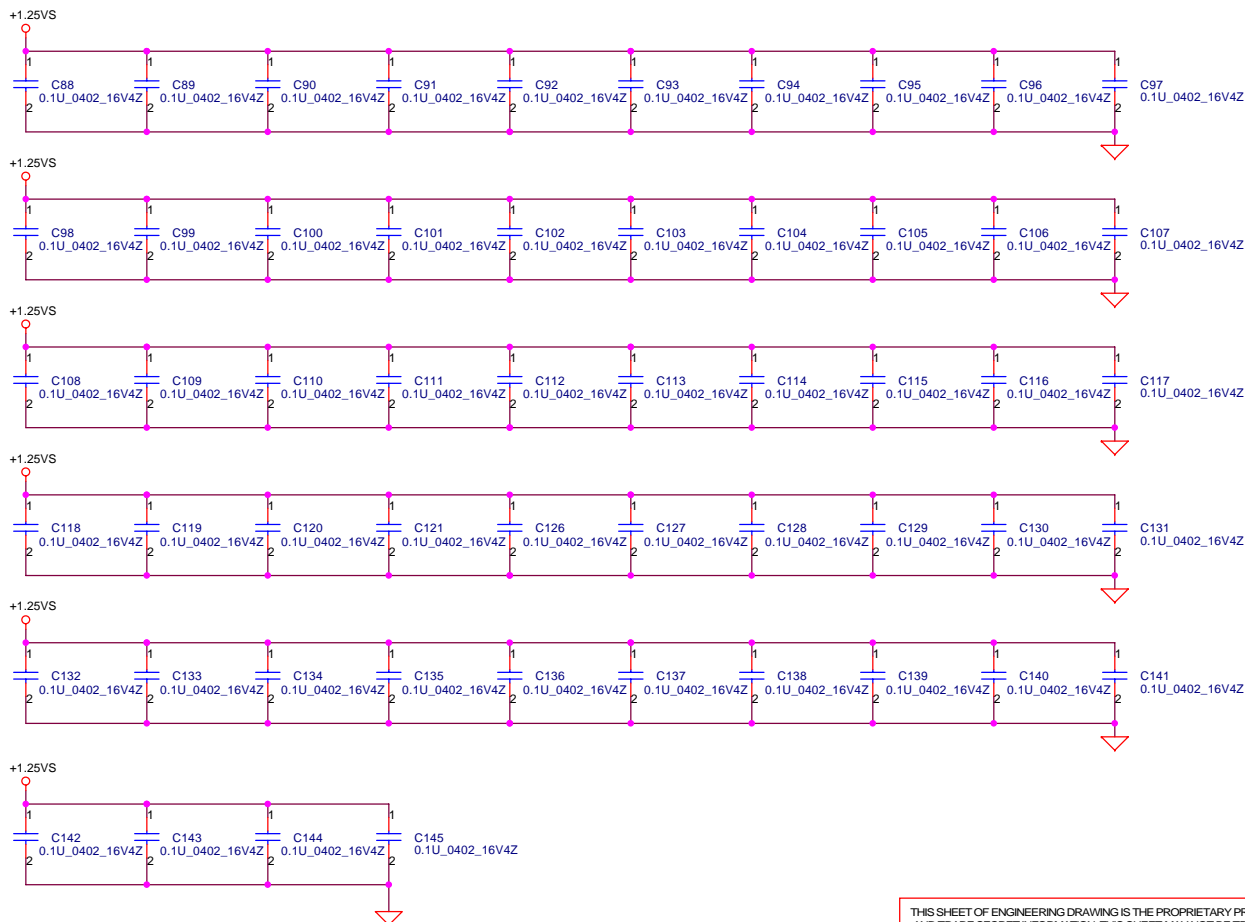
Compal Electronics, Inc.			
Title			
DDR-SODIMM SLOT1			
Size	Document Number	Rev	
Custom	DAT20 LA-1971	0.3	
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Layout note :  
Distribute as close as possible  
to DDR-SODIMM.



Layout note :  
Place one cap close to every 2 pull up resistors termination to  
+1.25V



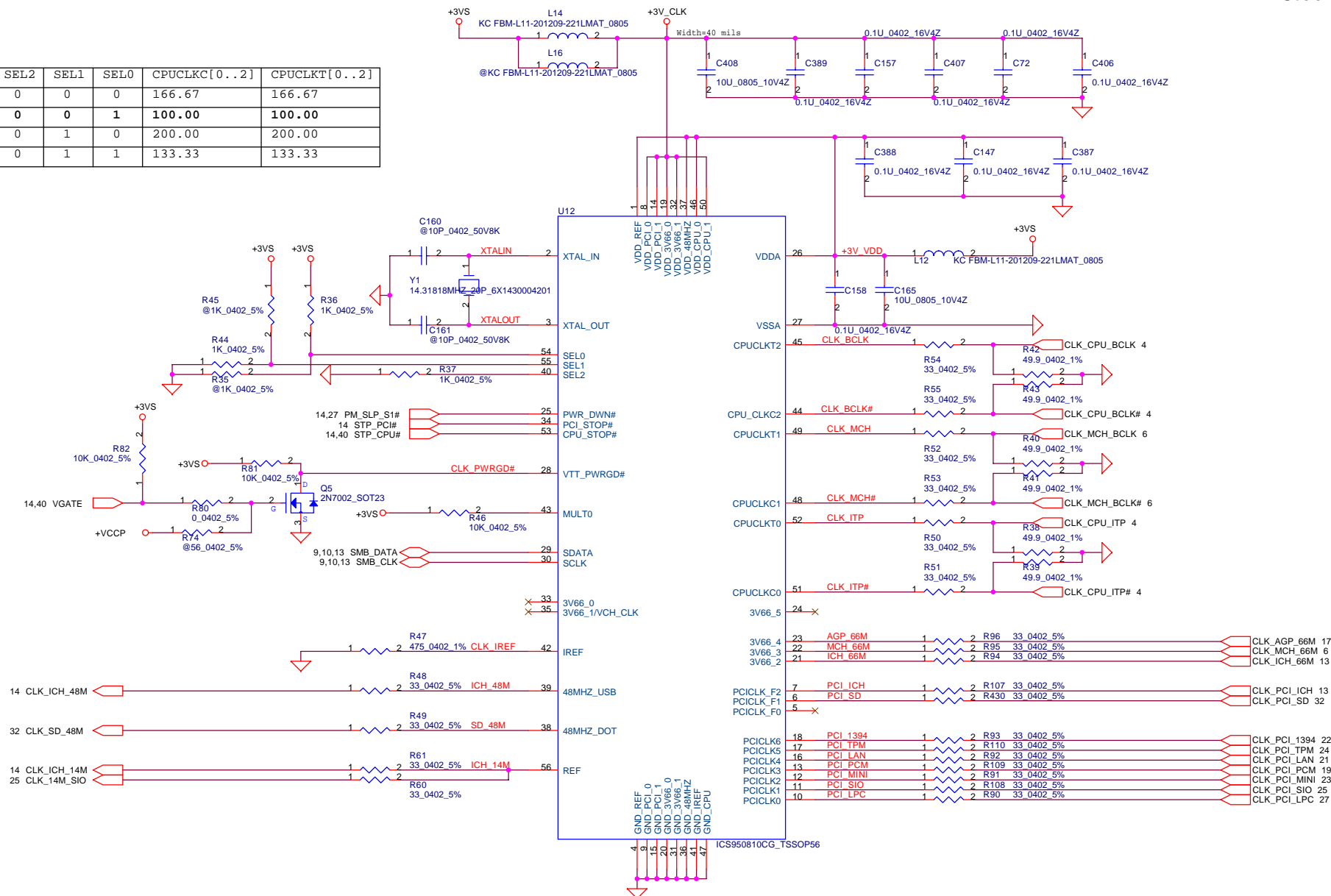
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Compal Electronics, Inc.

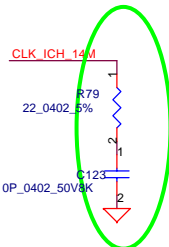
Title			DDR SODIMM Decoupling
Size	Document Number	Rev	
Custom	DAT20 LA-1971	0.3	
Date:	Friday, September 26, 2003	Sheet	11 of 42

### *Clock Generator*

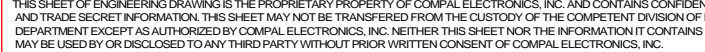
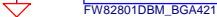
SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
<b>0</b>	<b>0</b>	<b>1</b>	<b>100.00</b>	<b>100.00</b>
0	1	0	200.00	200.00
0	1	1	133.33	133.33





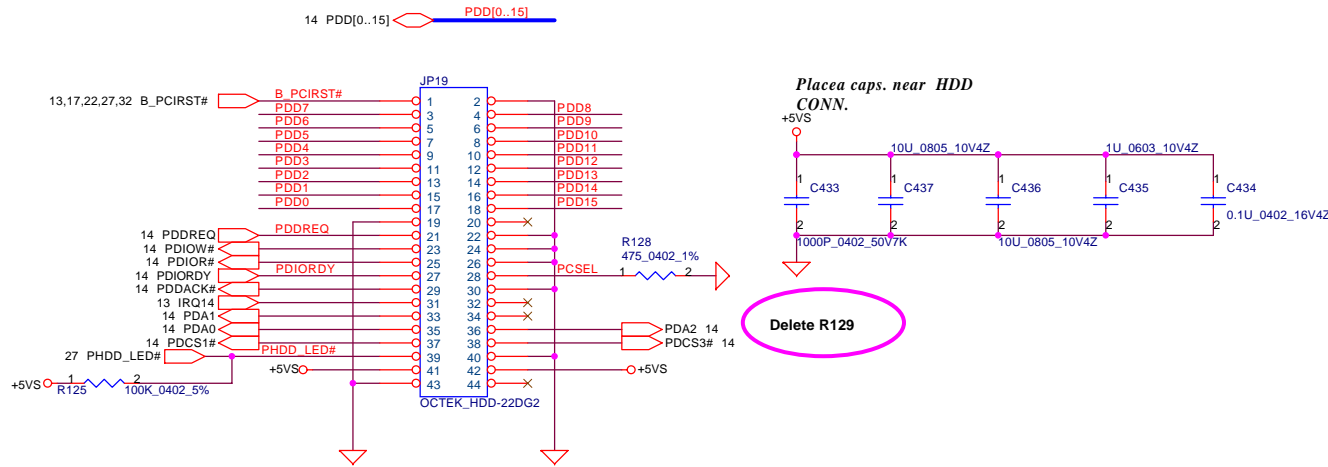


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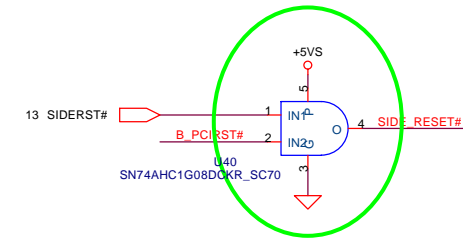
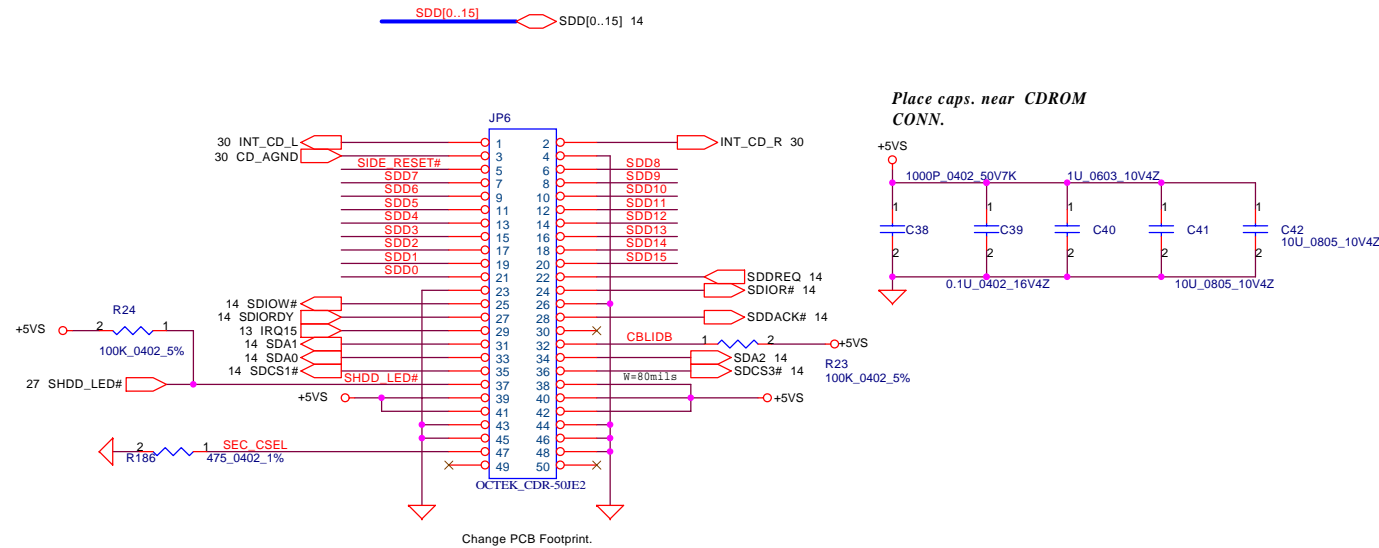




# HDD Connector



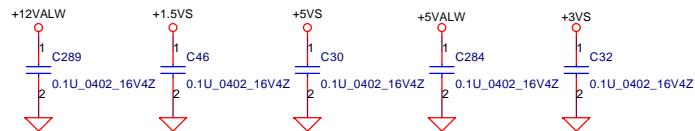
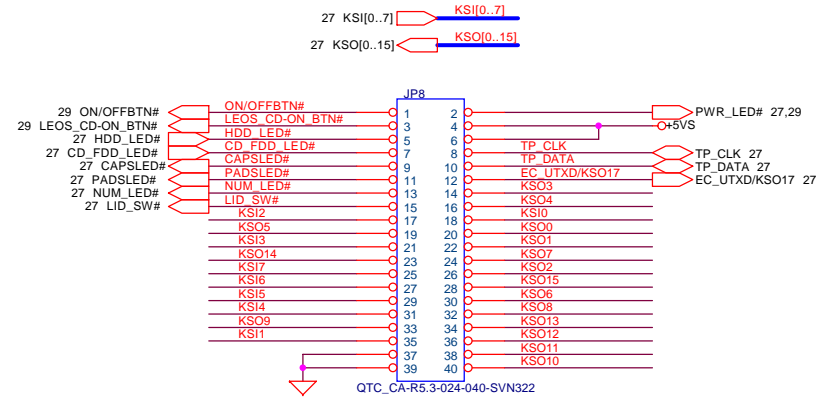
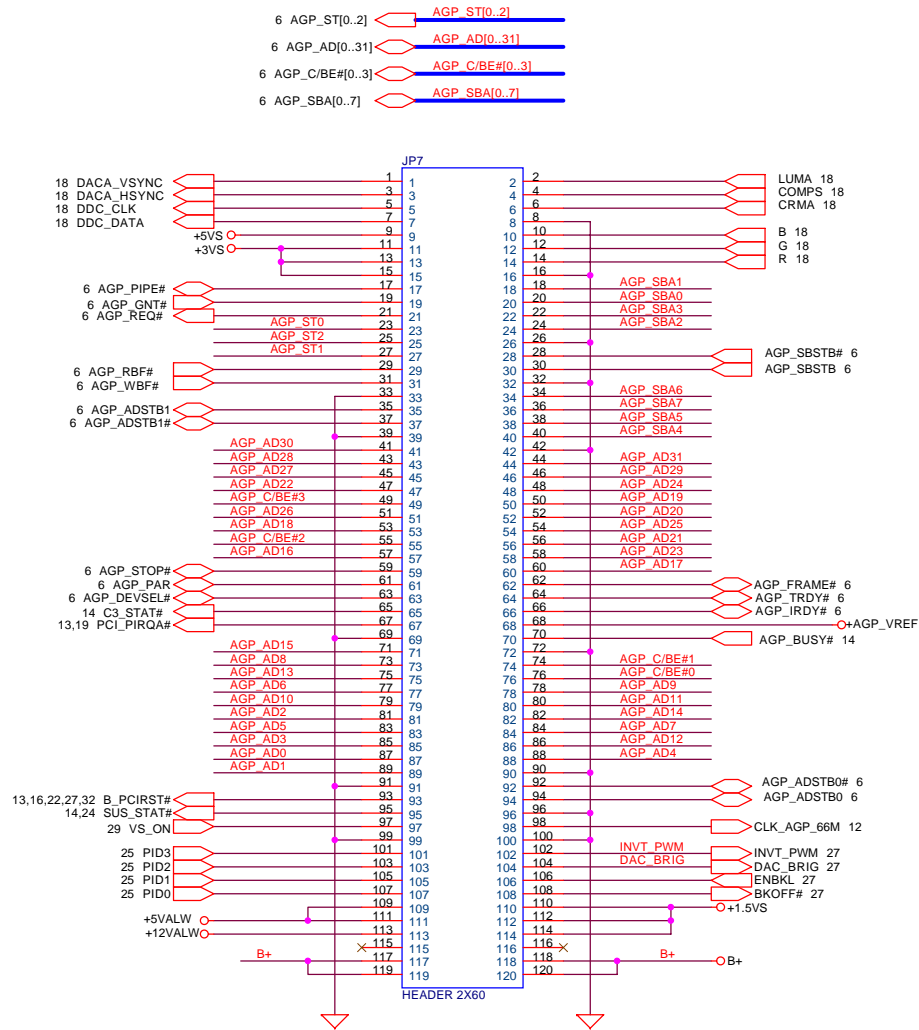
# CD-ROM Connector



Compal Electronics, Inc.

Title			IDE/CD-ROM Module
Size	Document Number	Rev	
Custom	DAT20 LA-1971	0.3	
Date:	Friday, September 26, 2003	Sheet	16 of 42

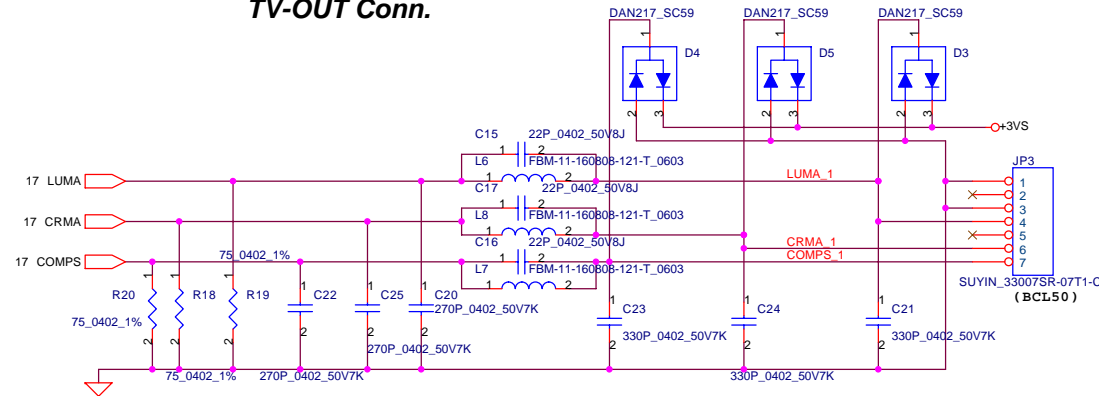
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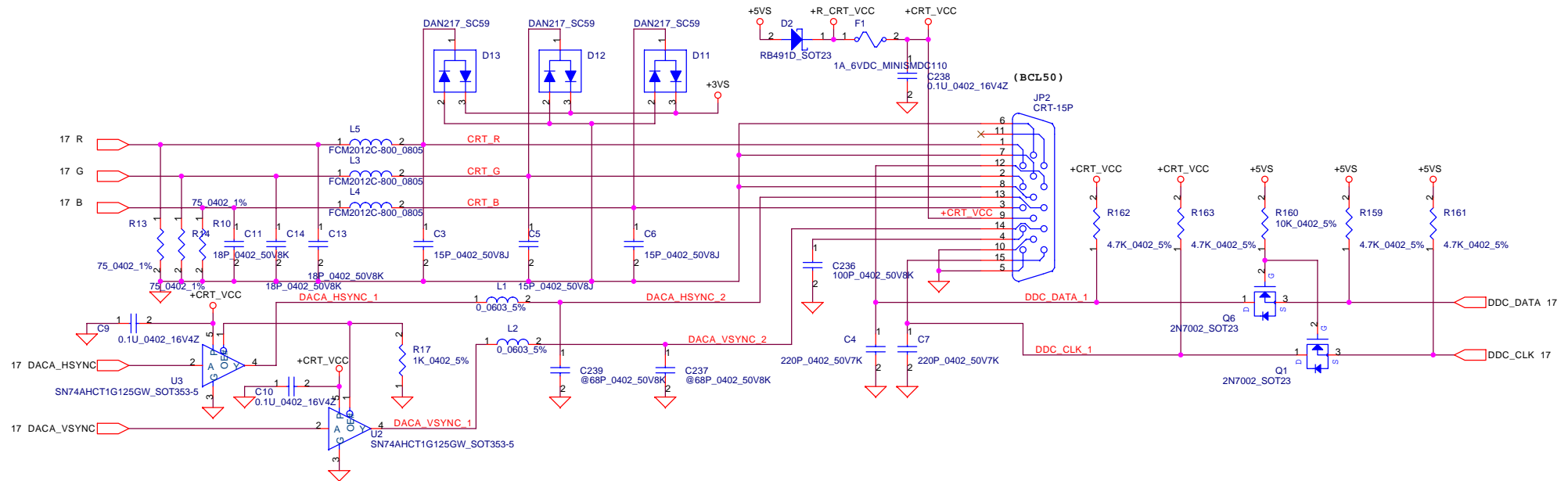
Compal Electronics, Inc.			
Title			
AGP Connector			
Size	Document Number	Rev	
Custom	DAT20 LA-1971	0.3	
Date:	Friday, September 26, 2003	Sheet	17 of 42

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## TV-OUT Conn.



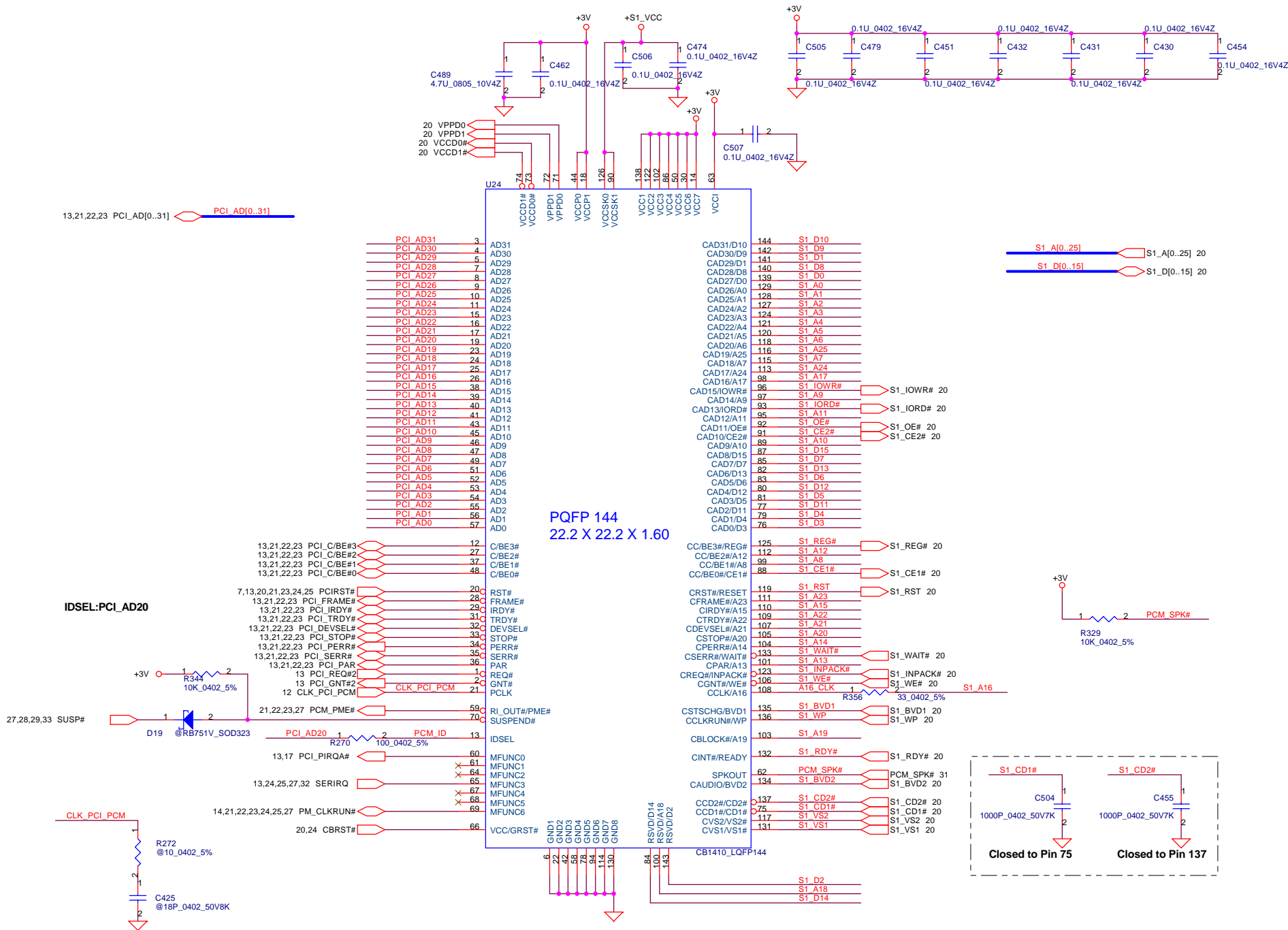
## CRT Conn.



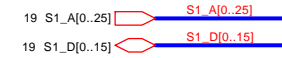
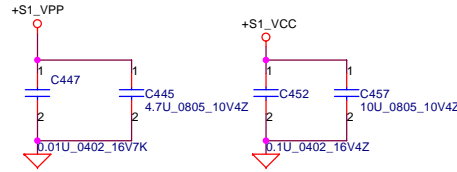
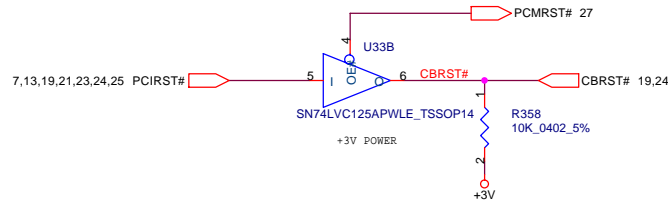
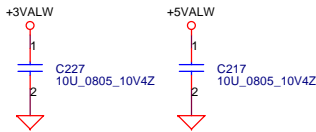
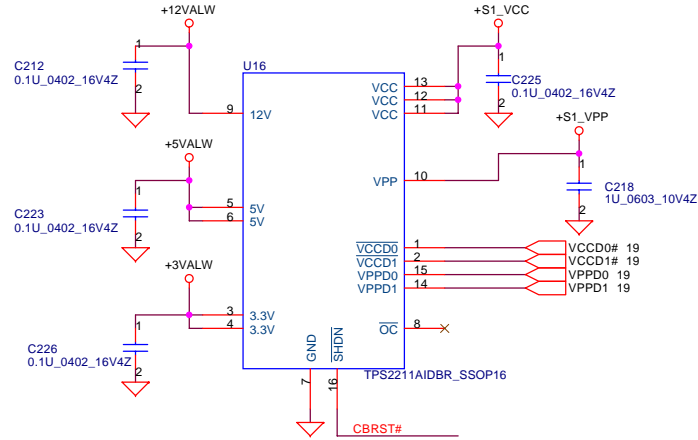
Compal Electronics, Inc.

Title			CRT,TV-OUT CONNECTOR
Size	Document Number	Rev	
Custom	DAT20 LA-1971	0.3	
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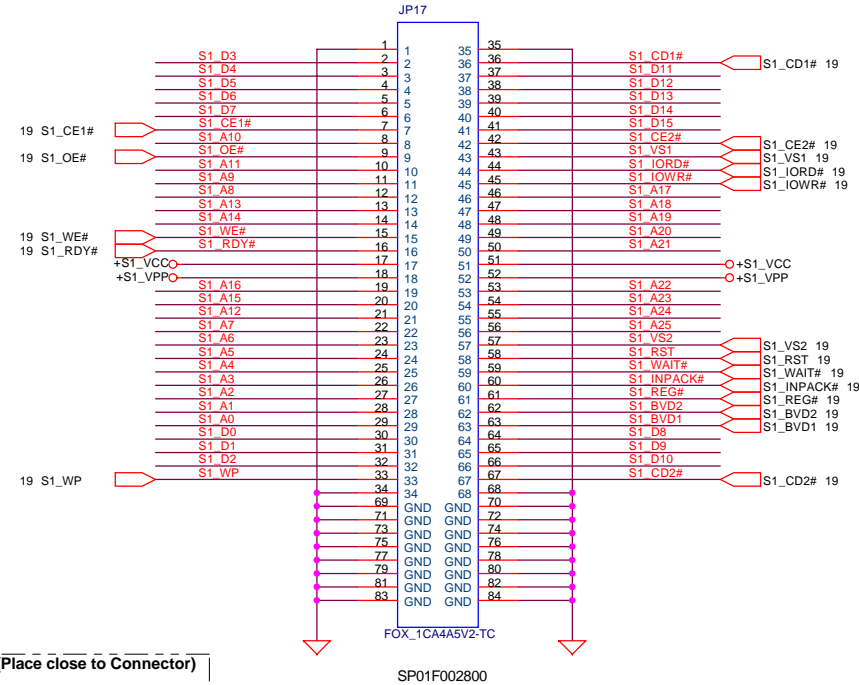
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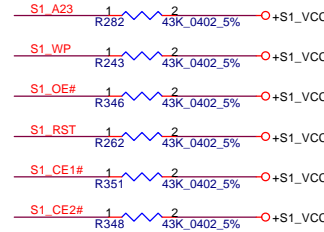
# PCMCIA Power Controller



# CardBus Socket



# For CB1410 Rev.B0 (Place close to Connector)



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CardBus Socket

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# TSB43AB21 (TSB43AB22)

## PCI BUS INTERFACE

## BIAS CURRENT

## OSCILLATOR

## FILTER

## EEPROM 2 WIRE BUS

## POWER CLASS

## PHY PORT 1

## TEST9

## TEST8

## TEST3

## TEST2

## TEST1

## TEST0

## TEST9

## TEST8

## TEST3

## TEST2

## TEST1

## TEST0

## TEST9

## TEST8

## TEST3

## TEST2

## TEST1

## TEST0

## TEST9

## TEST8

## TEST3

## TEST2

## TEST1

## TEST0

## TEST9

## TEST8

## TEST3

## TEST2

## TEST1

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## TEST9

## TEST8

## TEST3

## TEST2

## TEST1

## TEST0

## TEST9

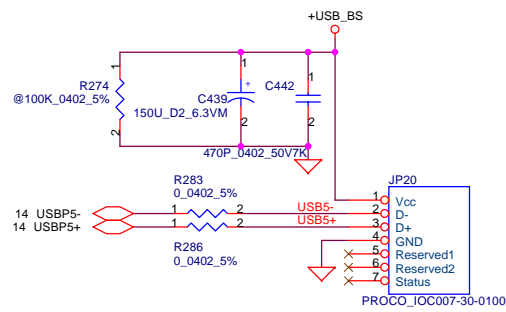
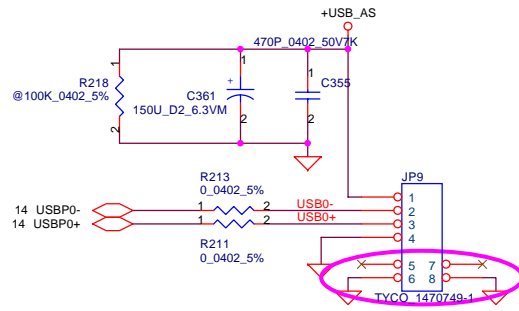
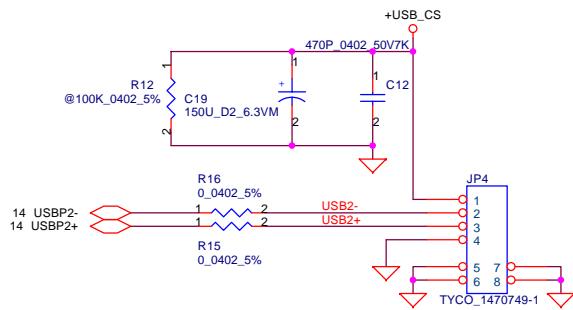
## TEST8

## TEST3

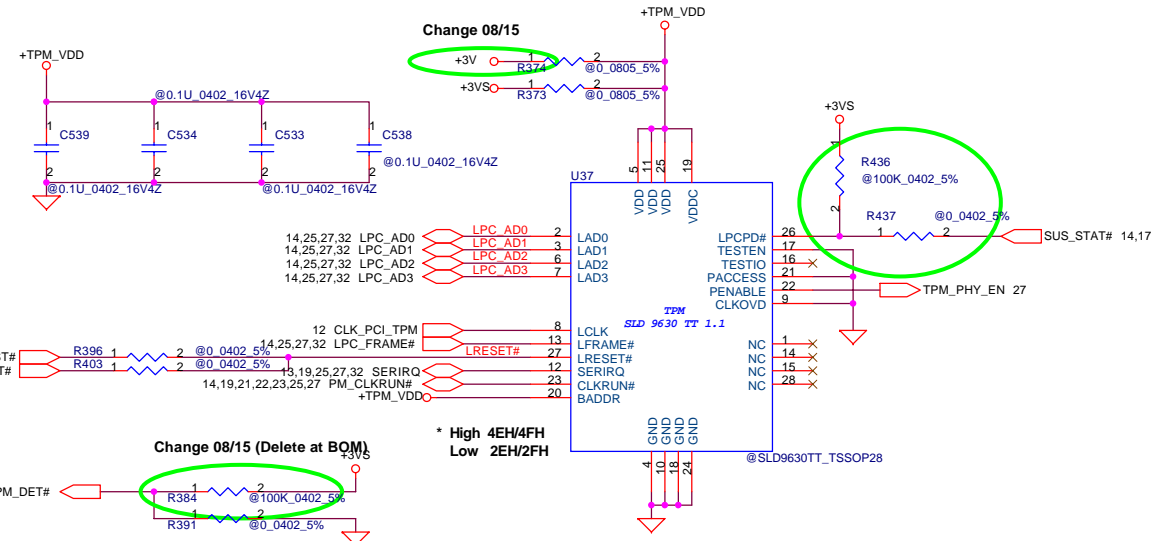
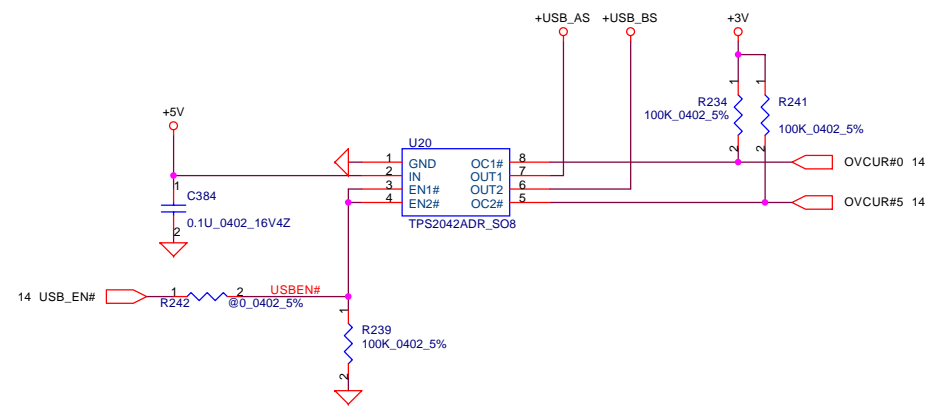
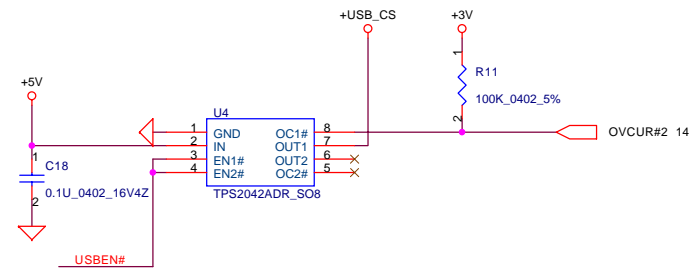
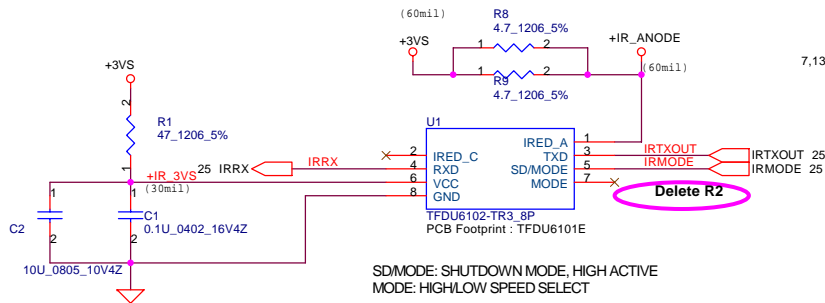
## TEST2







## FIR Module



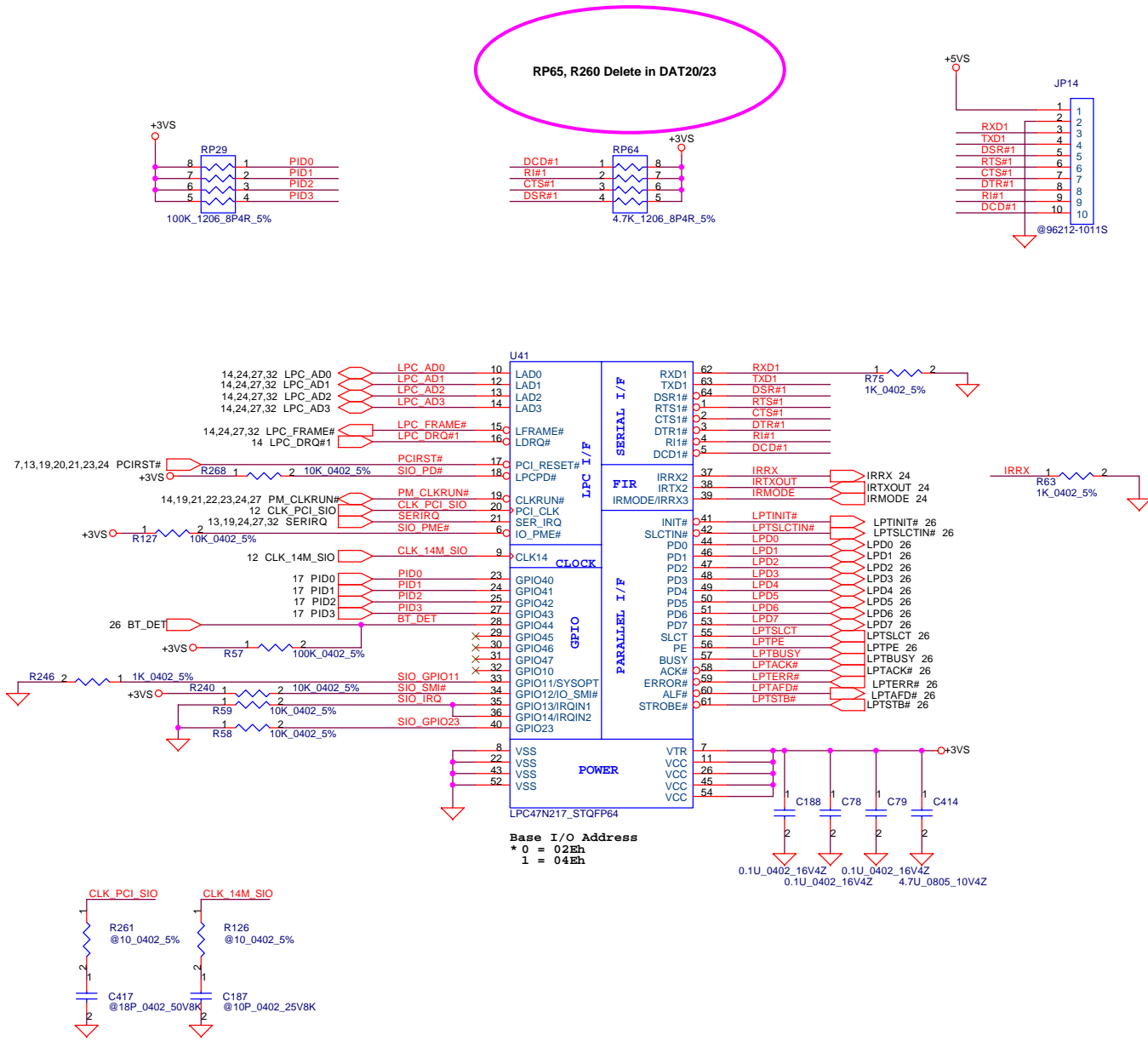
Compal Electronics, Inc.

USB / FIR / TPM

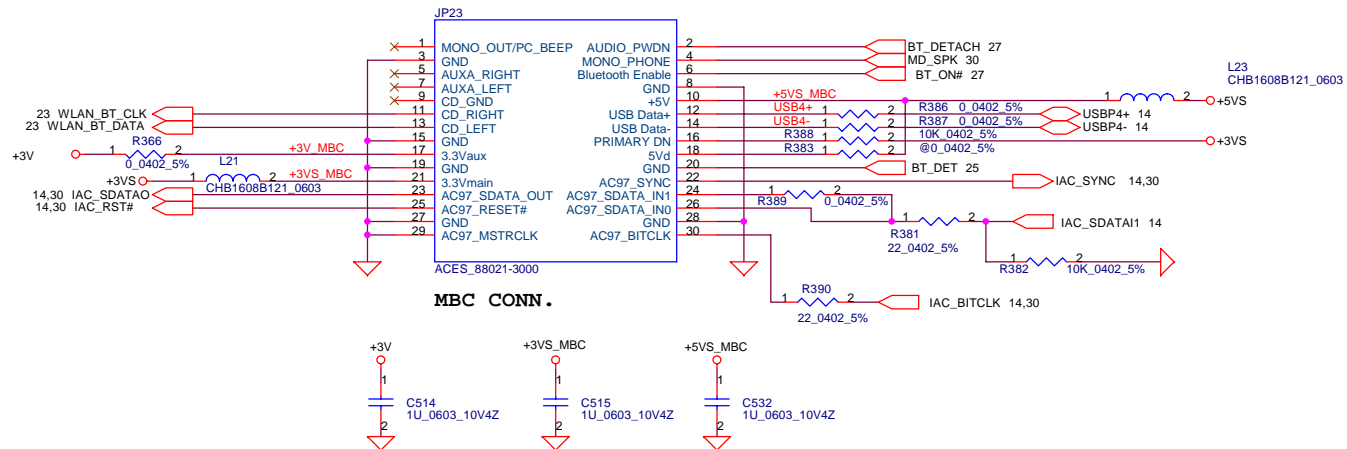
Size	Document Number	Rev
Custom	DAT20 LA-1971	0.3
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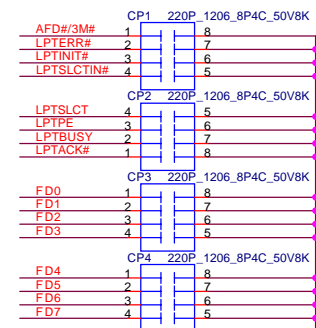
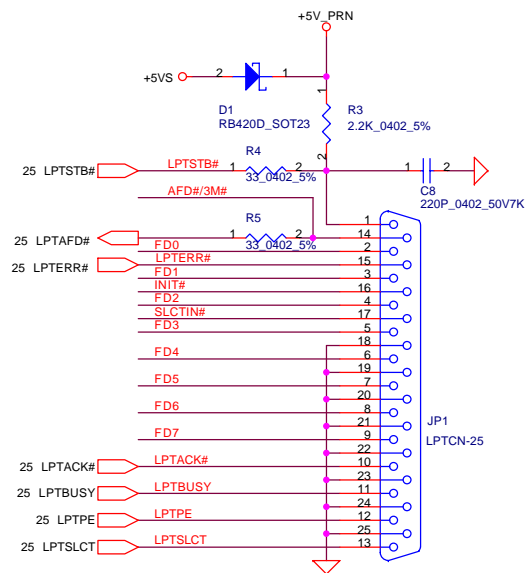
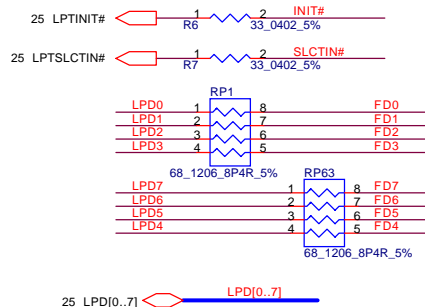
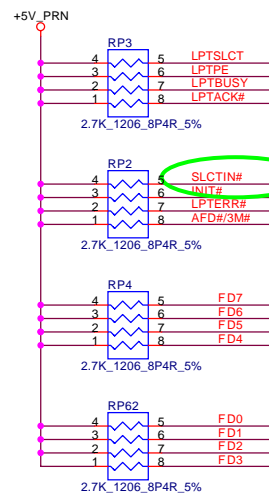
SUPER I/O SMsC LPC47N217



Compal Electronics, Inc.			
Title			
SUPER I/O LPC47N217			
Size	Document Number	Rev	
Custom	DAT20 LA-1971	0.3	
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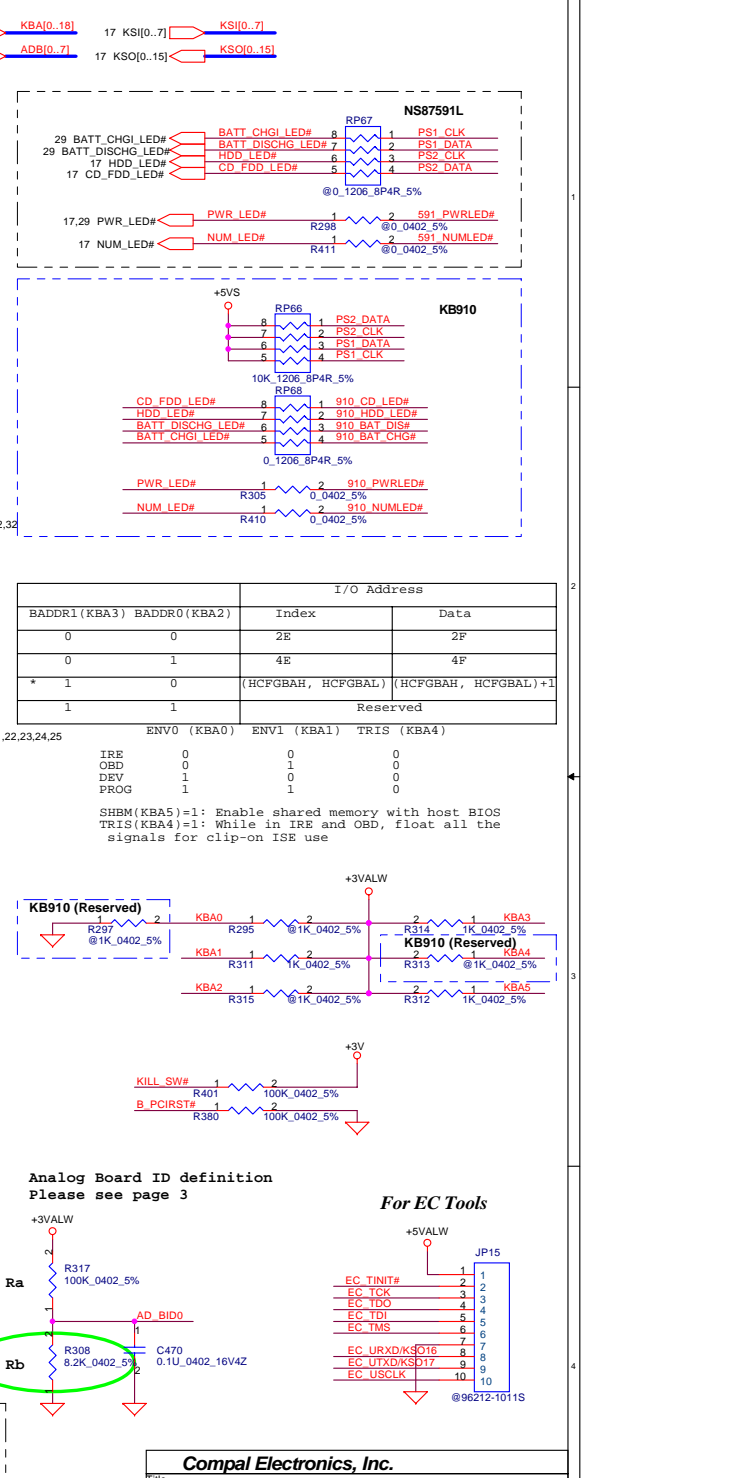
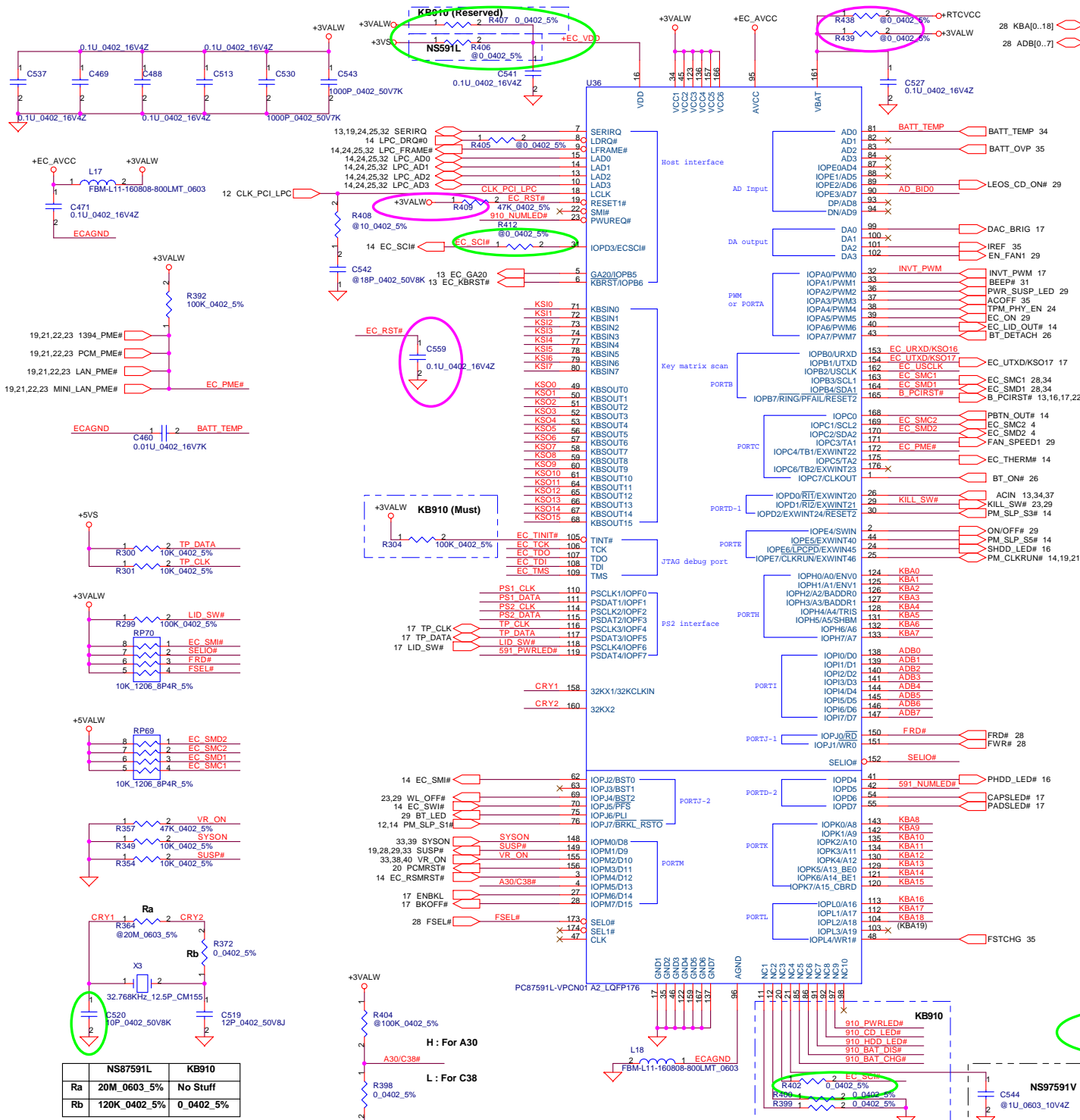


## PARALLEL PORT



Compal Electronics, Inc.			
Title			
PARALLEL / MDC PORT			
Size	Document Number	Rev	
Custom	DAT20 LA-1971	0.3	
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CF2 CF4 CF1 CF3 CF8  
SMDC40M80 SMDC40M80 SMDC40M80 SMDC40M80 SMDC40M80

CF15 CF5 CF6 CF9 CF12  
SMDC40M80 SMDC40M80 SMDC40M80 SMDC40M80 SMDC40M80

CF11 CF14 CF13 CF16  
SMDC40M80 SMDC40M80 SMDC40M80 SMDC40M80

FD1 FD2 FD3  
FIDUCAL FIDUCAL FIDUCAL

FD4 FD5 FD6  
FIDUCAL FIDUCAL FIDUCAL

H4 H3 H9 H22 H19  
H\_S315D138 H\_S315D138 H\_S315D138 H\_S315D138 H\_S315D138

H17 H21 H15 H14  
H\_S315D138 H\_S315D138 H\_S315D138 H\_S315D138

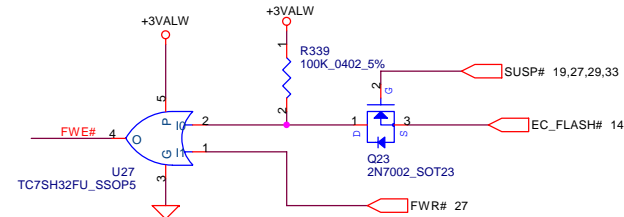
H1 H2 H8 H10  
H\_S315D165 H\_S315D165 H\_S315D165 H\_S315D165

H6 H7 H11 H12  
H\_C354D165 H\_C354D165 H\_C354D165 H\_C354D165

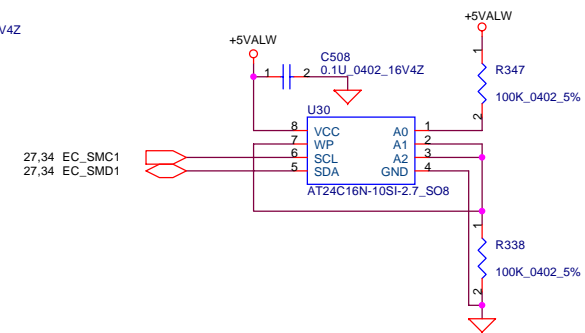
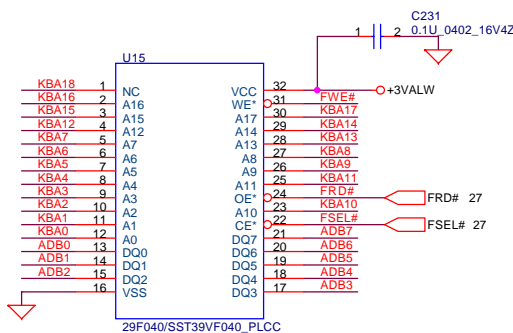
H18 H16 H20  
H\_C276D142 H\_C256D165 H\_R386X189D307X110

H13 H5  
H\_S315D138 H\_S394D165

H24 H23  
H\_O292X55D272X35 H\_O174X55D154X35



27 KBA[0..18] KBA[0..18]  
27 ADB[0..7] ADB[0..7]

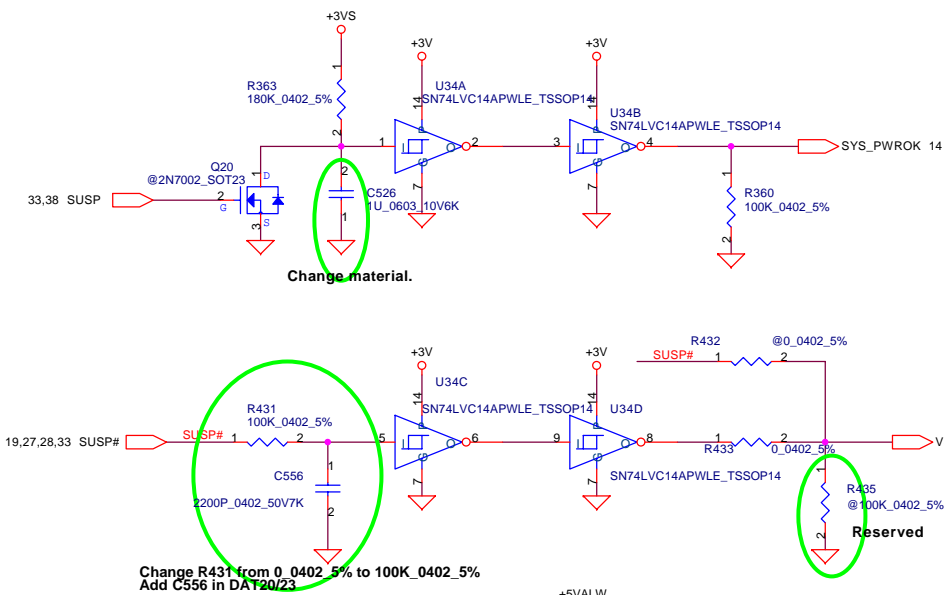


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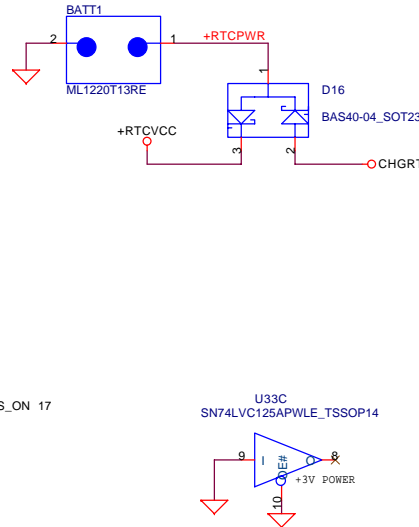
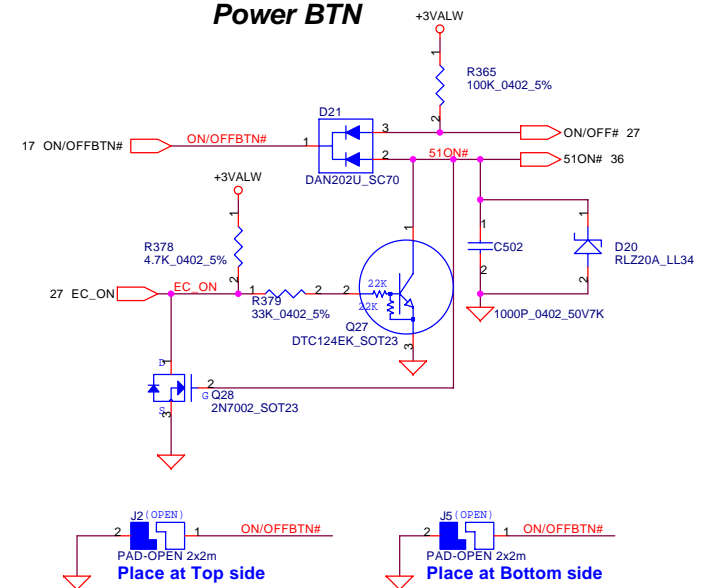
Title		BIOS & EXT. I/O PORT	
Size	Document Number	Rev	
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Date:	Friday, September 26, 2003	Sheet	28 of 42

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### ***Power ON Circuit***

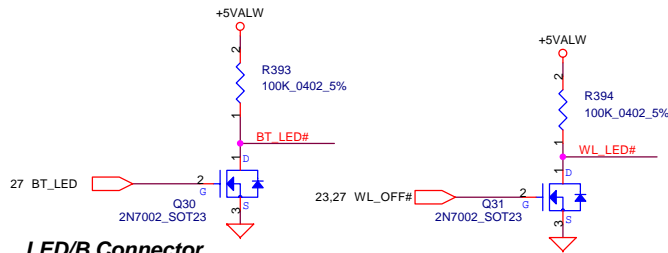


### RTC Battery

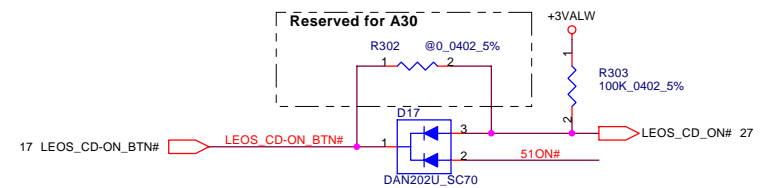
**Power BTN**

LED_INDICATOR	C38	30
PWR	Blue	Green
PWR_SUSP	AMB	AMB
BATT_CHGI	Blue	Green
BATT_DISCHG	AMB	AMB
WL_LED	Blue	Green
BT_LED	AMB	AMB
SD_LED	None	Green

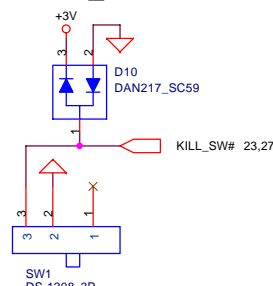
### LED/B Connector



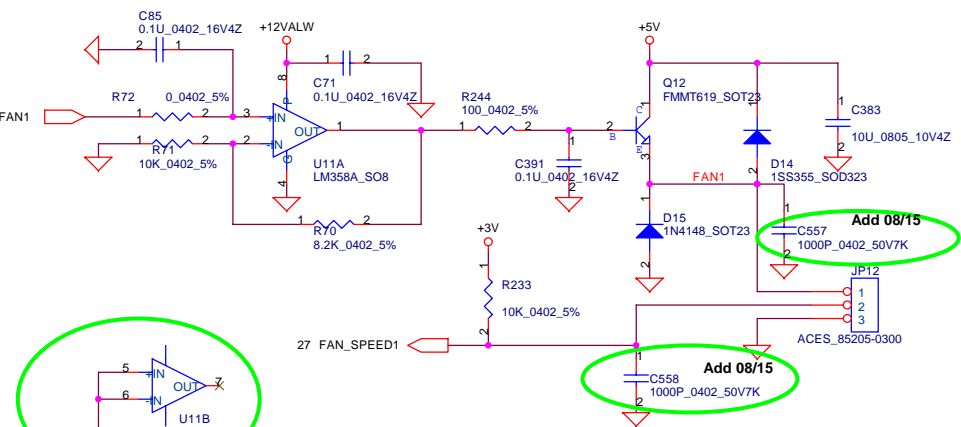
## Fan Control circuit



## KILL\_Switch



Change 08/15



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Title	Power OK/Reset/RTC battery
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Size	Document Number	Rev
Custom	<b>DAT20 LA-1971</b>	0.3

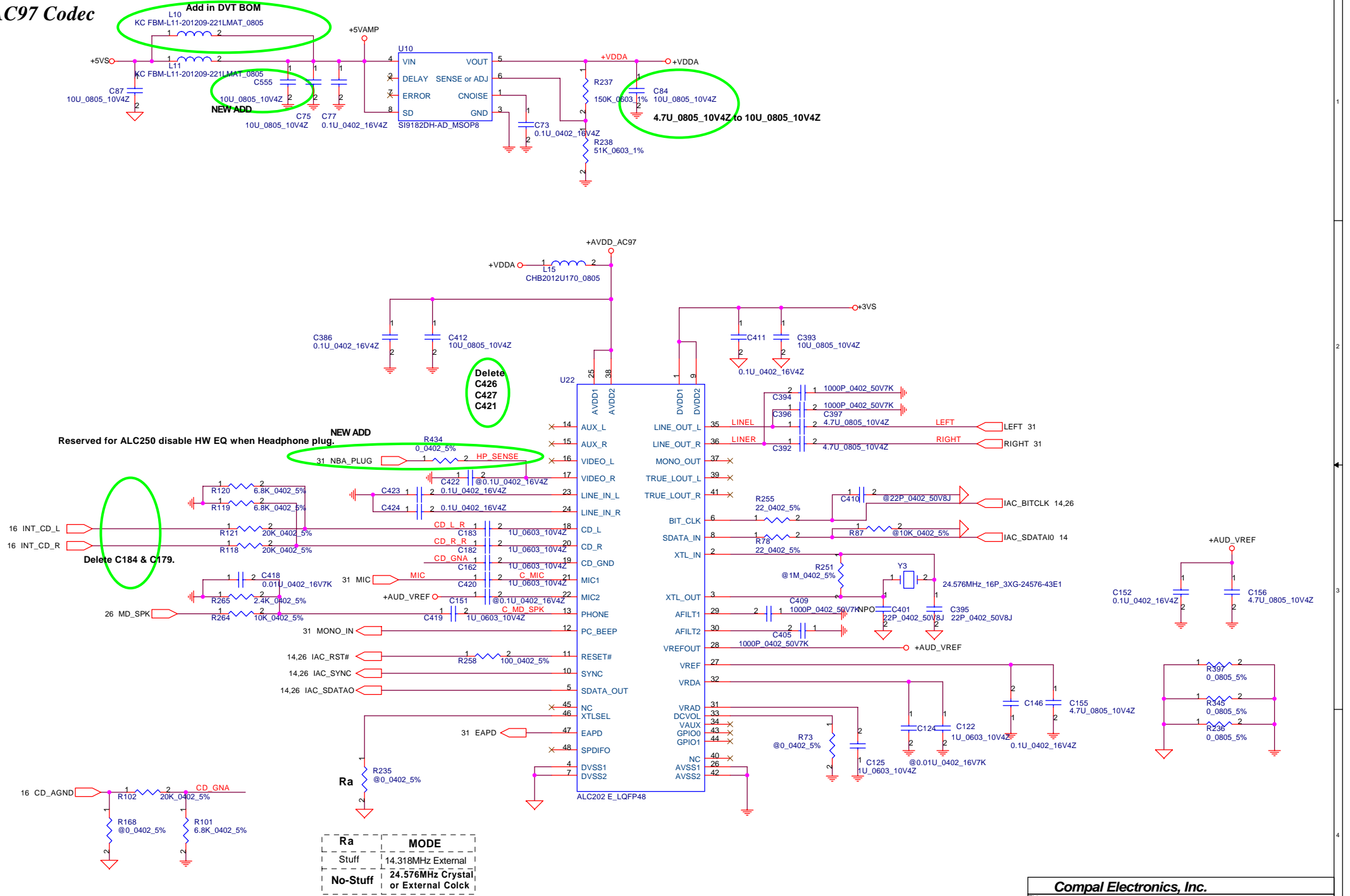
Date: Friday, September 26, 2003 Sheet 29 of 42

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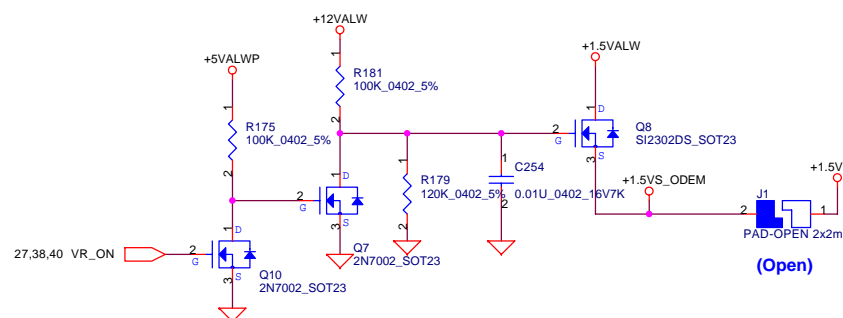
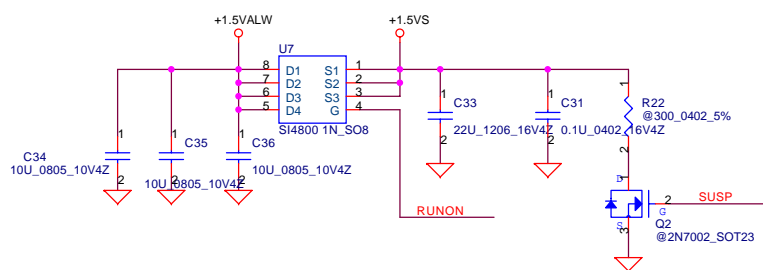
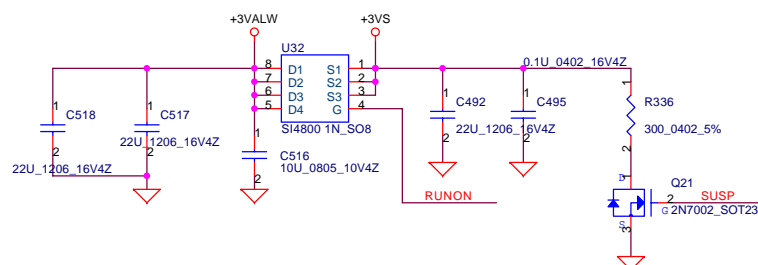
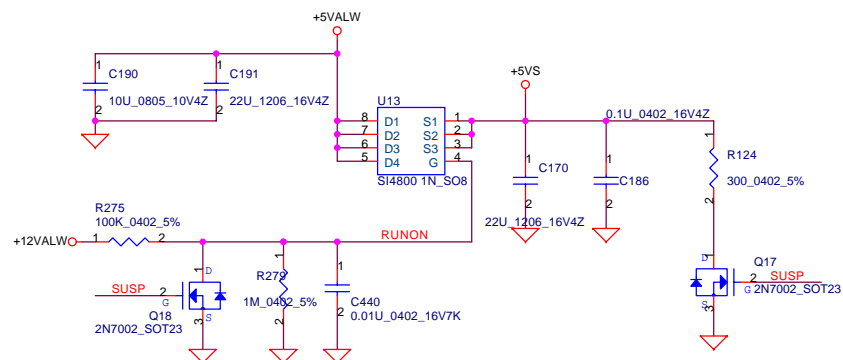
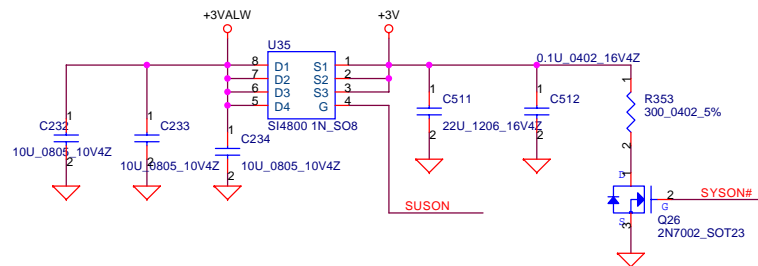
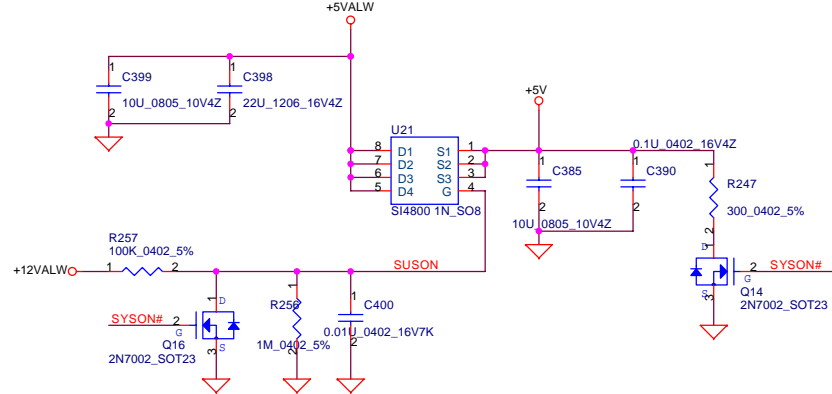
# AC97 Codec



Compal Electronics, Inc.			
Title			
AC97 Codec Realtek ALC202			
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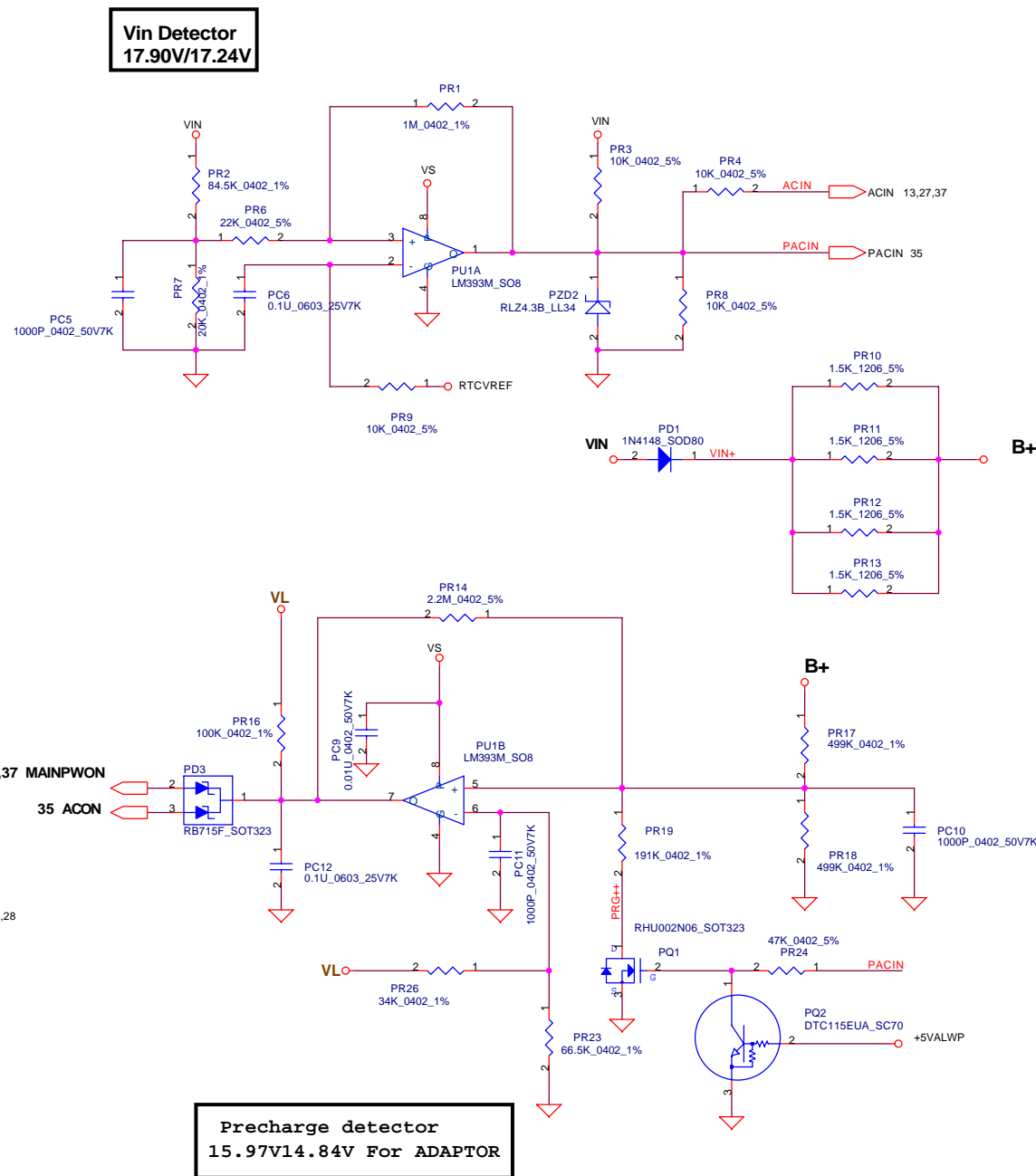






Title			
DC/DC Circuit Interface			
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27,28 EC\_SMC1

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$I_{adp}=0\sim 2.9A(60W)$   
 $I_{adp}=0\sim 2.9A(75W)$

$I_{REF}=1 \cdot I_{charge}$   
 $I_{REF}=0\sim 3.3V$

$2P3S:3800mAh/cell$   
 $0.7C=3.0A$

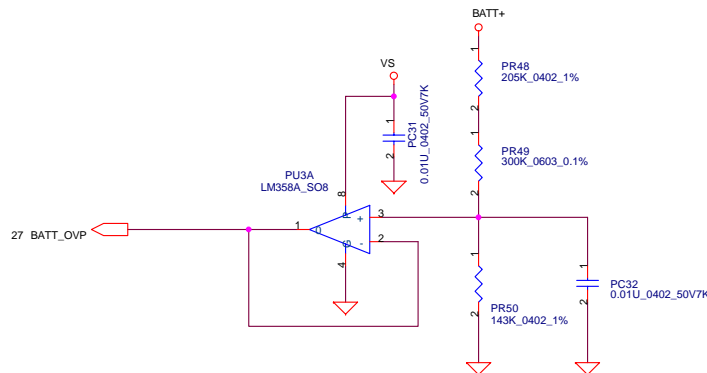
OVP voltage :

LI-3S :12.9V----BATT-OVP=2.84V

BATT-OVP=0.2206\*BATT+

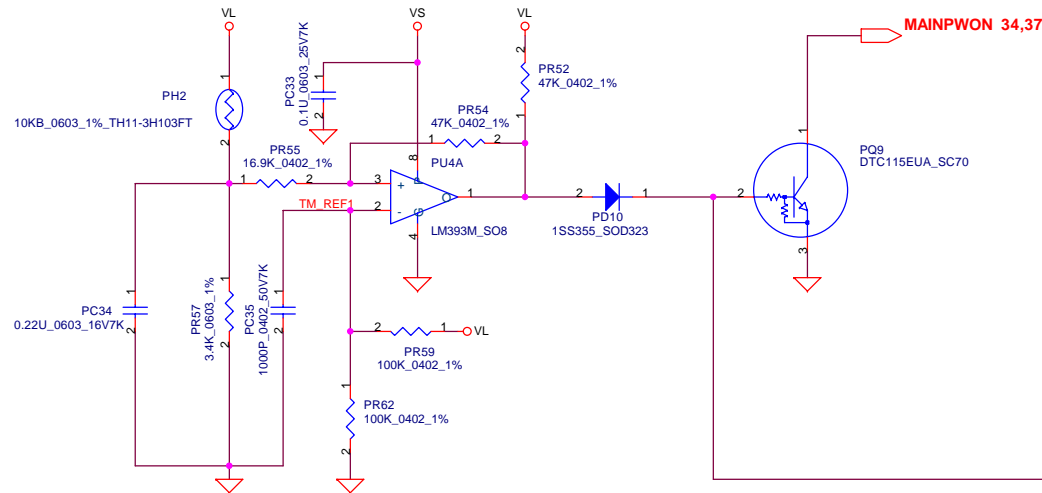
Charge voltage

3S CC-CV MODE : 12.6V



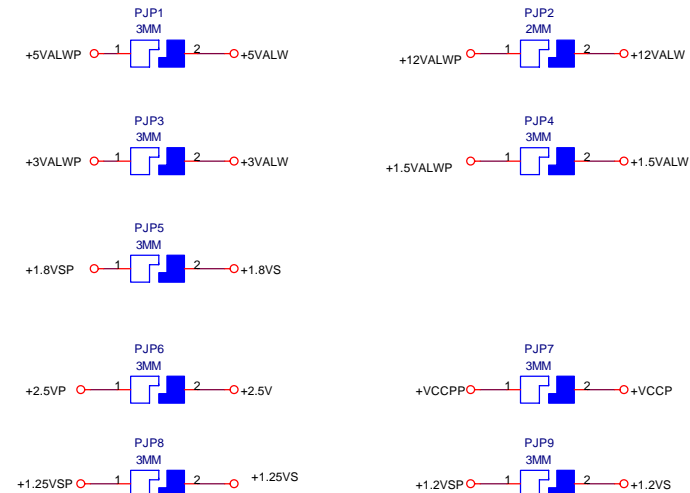
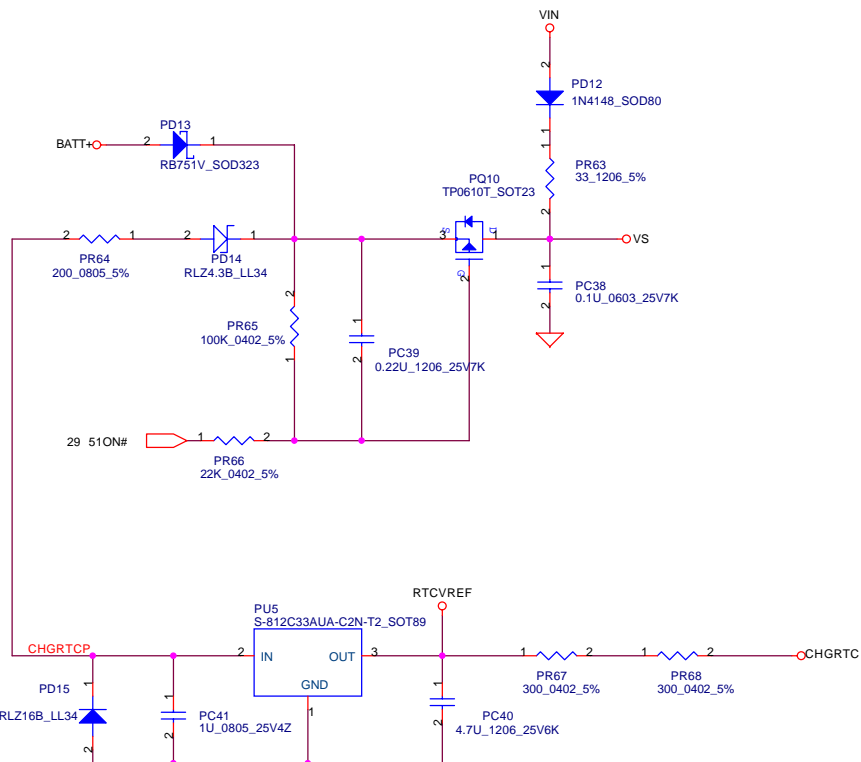
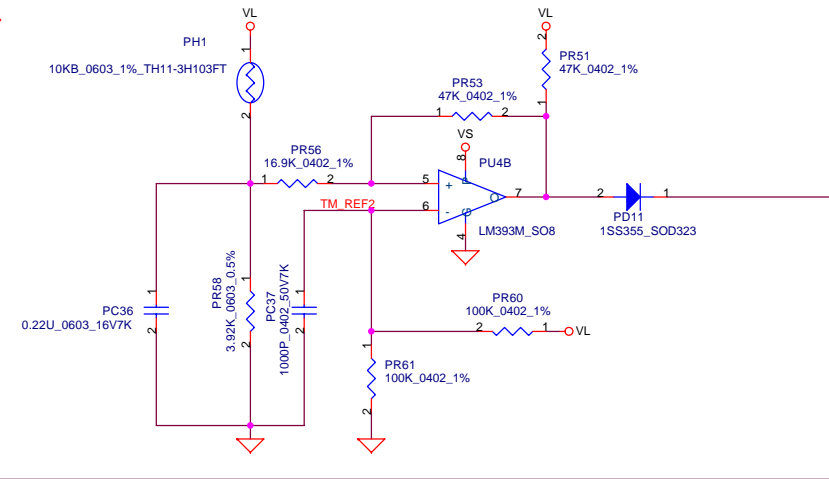
### PH1 under CPU botten side :

CPU thermal protection at 85 degree C  
Recovery at 44(45) degree C



### PH2 near main Battery CONN :

BAT. thermal protection at 78 degree C  
Recovery at 39(40) degree C



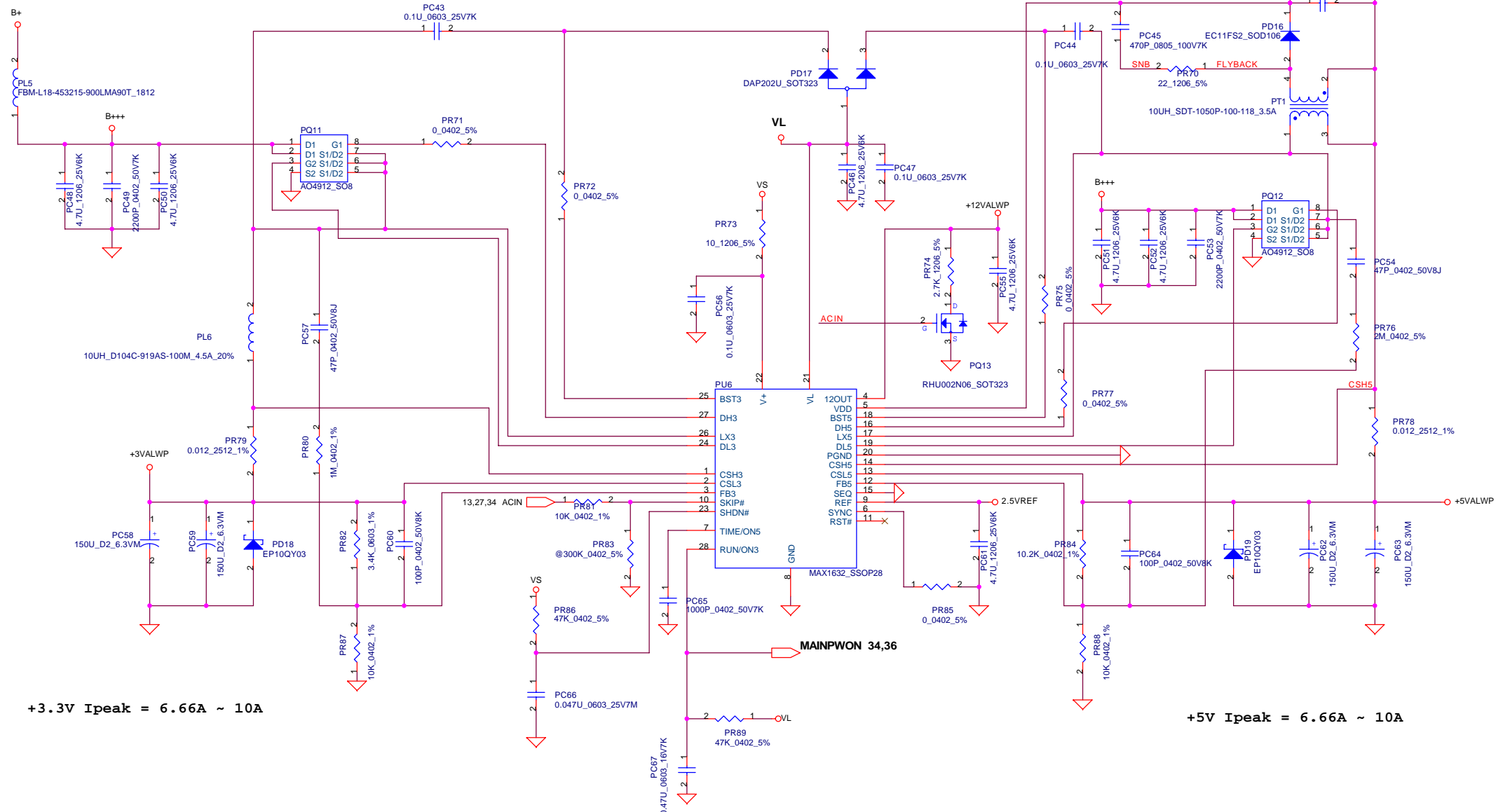
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**RTC Battery & OTP**

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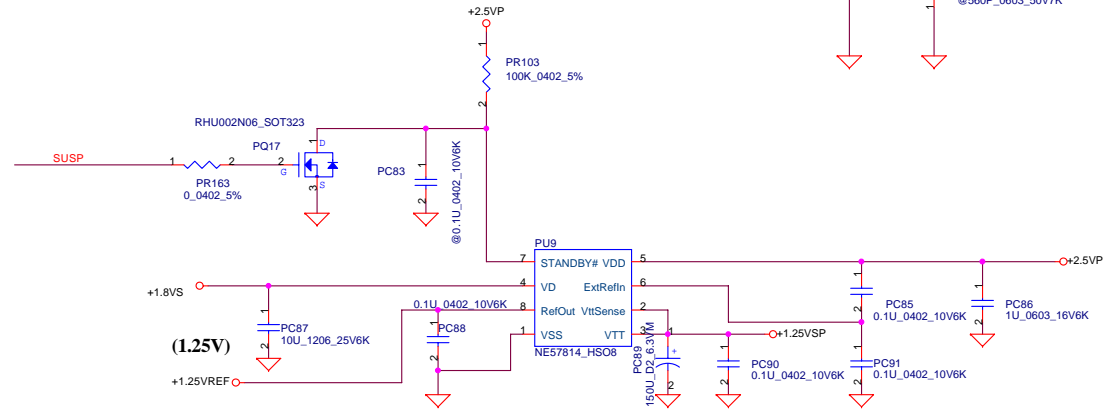
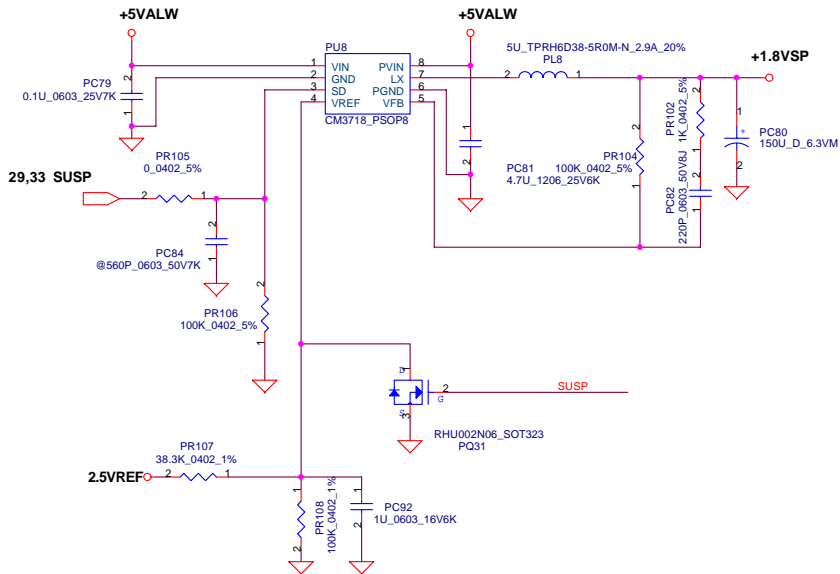
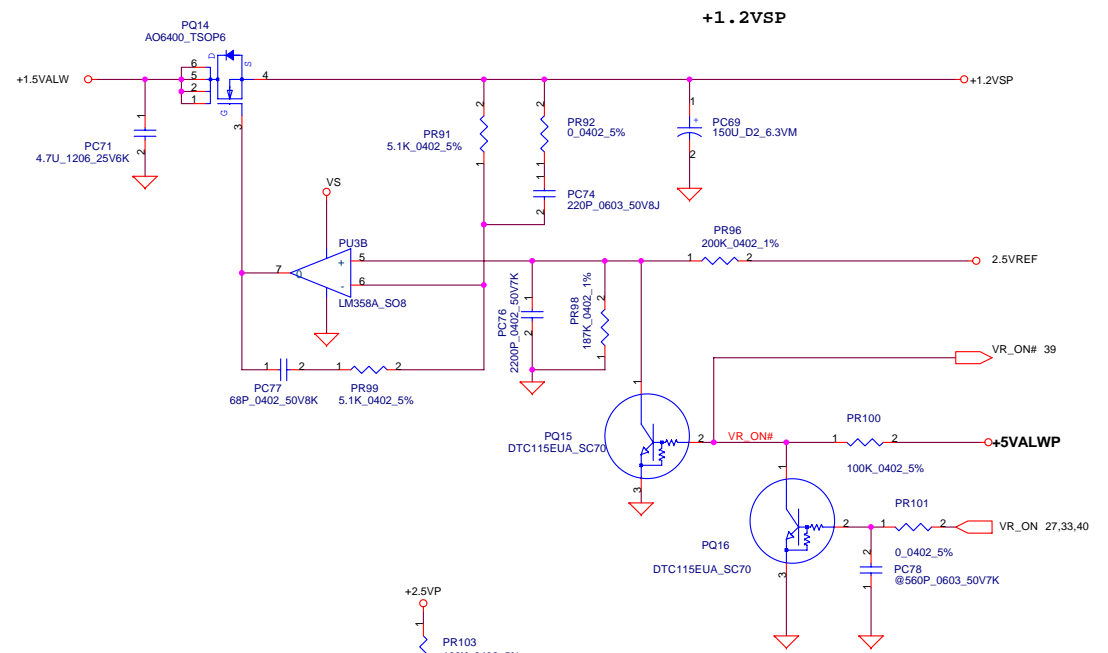
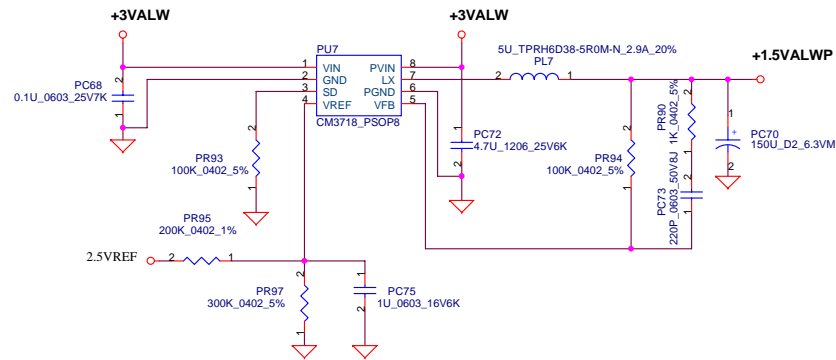


+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

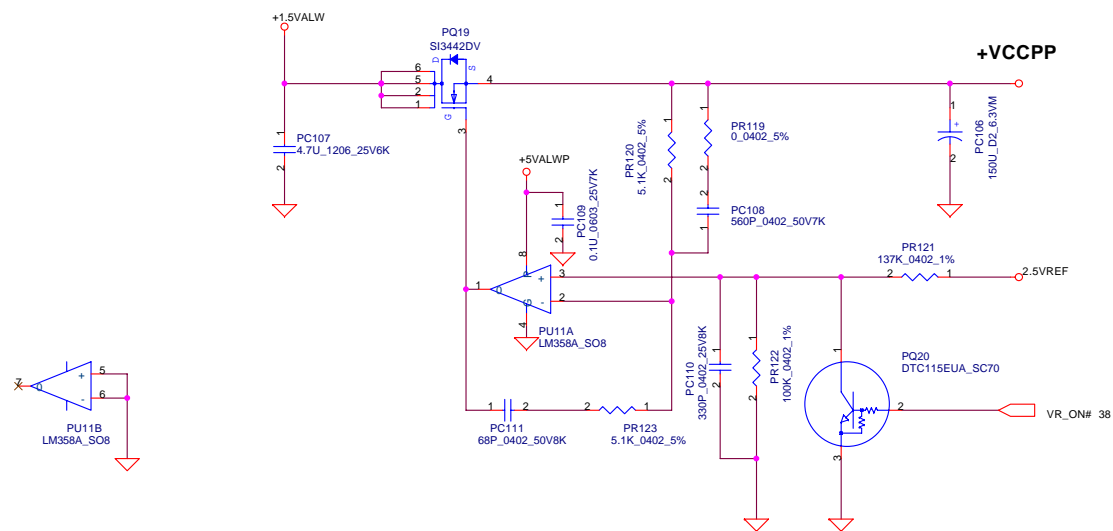
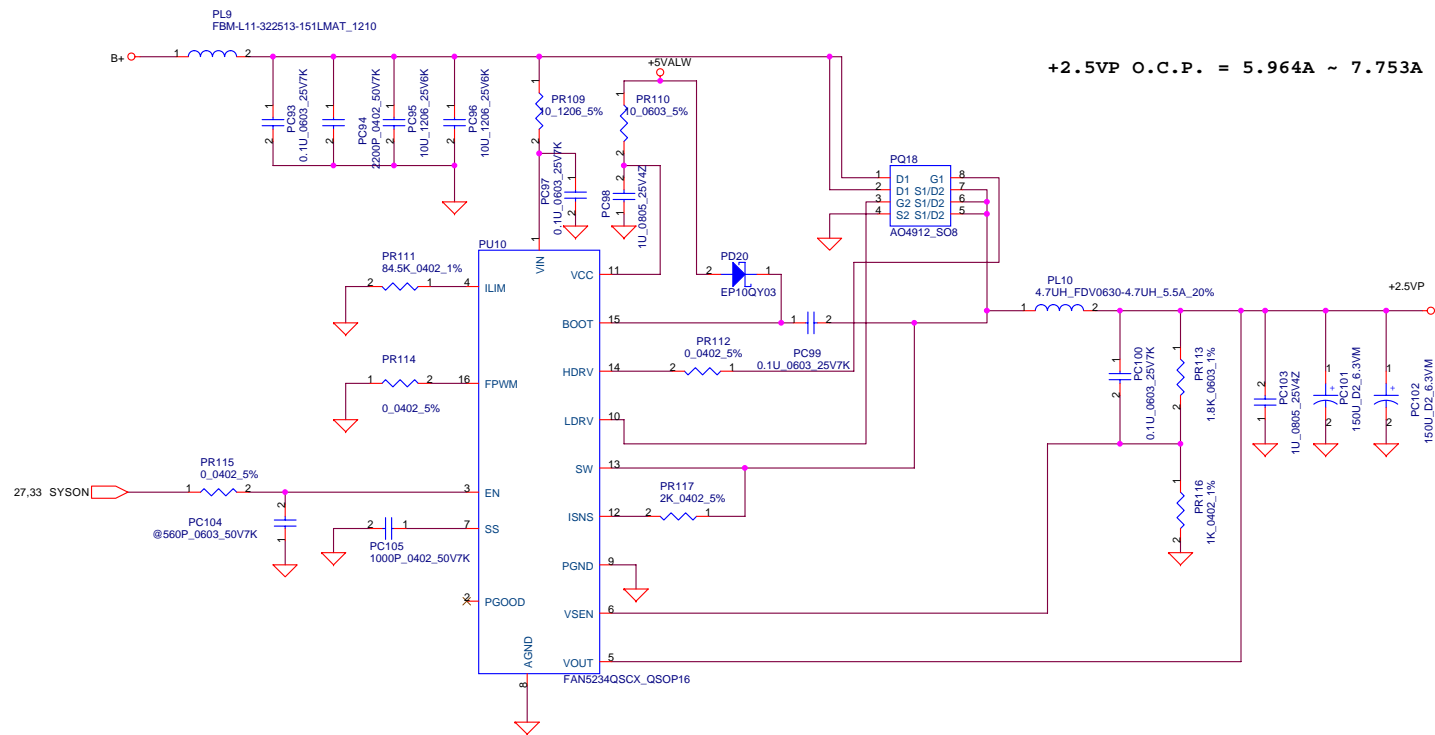
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Title			
+5VALWP / +3VALWP / +12VALWP			
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Title			
+1.8VSP & +1.25VSP & 1.5VALWP & +1.2VSP			
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File  
DDR +2.5VP & VCCPP

Size  
Custom  
Document Number  
DAT20 LA-1971

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A
B
C
D
E

# DAT20 PIR LIST

## HW PIR LIST

1

### EVT -> DVT

[Page 7 & 9] Change Material R33, R34, R200, R201 (75\_0603\_1%)

[Page 14] Change Material R38 (20\_0603\_1%)

[Page 16] Change Material U40

[Page 24] Modify R374 connected from +3VALW to +3V & delete R384 (Remove TPM detect function)

[Page 25] Delete RP65 & R260 which reserved for LPC47N227

[Page 26] Change SLCTIN# connection.

[Page 27] Change R308 from 0\_0402\_5% to 8.2K\_0402\_5% for DVT test AD\_BID0

[Page 29] Change material for C526 from 1U\_0603\_10V4Z to 1U\_0603\_10V6K  
 Add C556 2200P\_0402\_50V7K  
 Add C557, C558 1000P\_0402\_50V7K

[Page 30] Add L10  
 Change C84 from 4.7U\_0805\_10V4Z to 10U\_0805\_10V4Z  
 Add C555 10U\_0805\_10V4Z  
 Delete C184, C179 1U\_0603\_10V4Z

[Page 32] R156 from 390\_0402\_5% to 360\_0402\_5%

[Page 27] R409 from 10K\_0402\_5% to 47K\_0402\_5% & add C559 0.1U\_0402\_16V4Z

2

### DVT -> PVT

[Page 12] Delete C70, C80, C166, C167, C168

[Page 24] Delete R2 (Reserved for FIR)

[Page 31] Delete C476, C531, R319, R371 AudiooHigh pass filter.

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	M/B cannot power on.	RC delay time is not enough of Max1632 on3 pin.	0.2	34	1.Change PC67 from 0.047U_0805_10V6K to 0.47U _16V K X7R 0603.	0.2	DVT
2	Layout symbol error.	Layout symbol error.	0.2	37	1.Change PR26 PCB footprint from R_0603 to R_0402.	0.2	DVT
3	Layout symbol error.	Layout symbol error.	0.2	40	1.Change PD22 from EP10QY03 to EP31QS04.	0.2	DVT
4	System cannot re-start and Windows fail when into C4.	The CPU cannot into skip mode,happen the OVP when C4.	0.2	40	Swap the PR154 and PR155.	0.2	DVT
5	Rating not enough.	Rating not enough.	0.2	34	1.Change PC66 from 0.047U_00603_16V7K to 0.047U_00603_25V7M.	0.2	DVT
6.	Rating is not enough.	Surge power rating concerned.	0.2	39	1.Change PR109 from 10_0603 to 10_1206.	0.2	DVT
7.	Change size.	Change size.	0.2		1.Change PR149,PR44,PR48,PR82,PR36,PR107,PR39,PR121, PR140,PR145 and PR146 from 0603 to 0402.	0.2	DVT
8.	Change size.	Change size.	0.2		1.Change PC114,PC131,PC49,PC21,PC53,PC128,PC126,PC124,PC31, PC7 and PC9 from 0603 to 0402.	0.2	DVT
9.	Change size.	Change size.	0.2		1.Change PC56,PC24,0C38,PC100,PC16 and PC19 from 0805 to 0603.	0.2	DVT
10.	Choke rating is not enough.	Charge current power rating concerned.	0.2	35	1.Change PL4 from 22UH to 16UH.	0.2	DVT
11.	Appication of CM3718 has overshoot issue during system on.	Charge control signal SHDN# to reference.	0.2	38	1.Add PQ31.	0.2	DVT
12.	EMI issue of charger.	EMI issue of charger.	0.3	35	1.Change PQ6 from AO4407 to FDS6679. Add the PR164 on GATE pin of PQ6.	0.3	PVT
13.	EMI issue of CPU_CORE.	EMI issue of CPU_CORE.	0.3	40	1.Change PQ21 and PQ25 from IRF7821 to IRF7811A. Add the 2200P on PC134 and PC135.	0.3	PVT
14.							

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Title

PWR-PIR

Size

Document Number

Custom

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E

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