

# Compal Confidential

## JFWXX Schematics Document

Intel Merom Processor with SiSM672MX + DDRII + SiS968 + SiS307LV

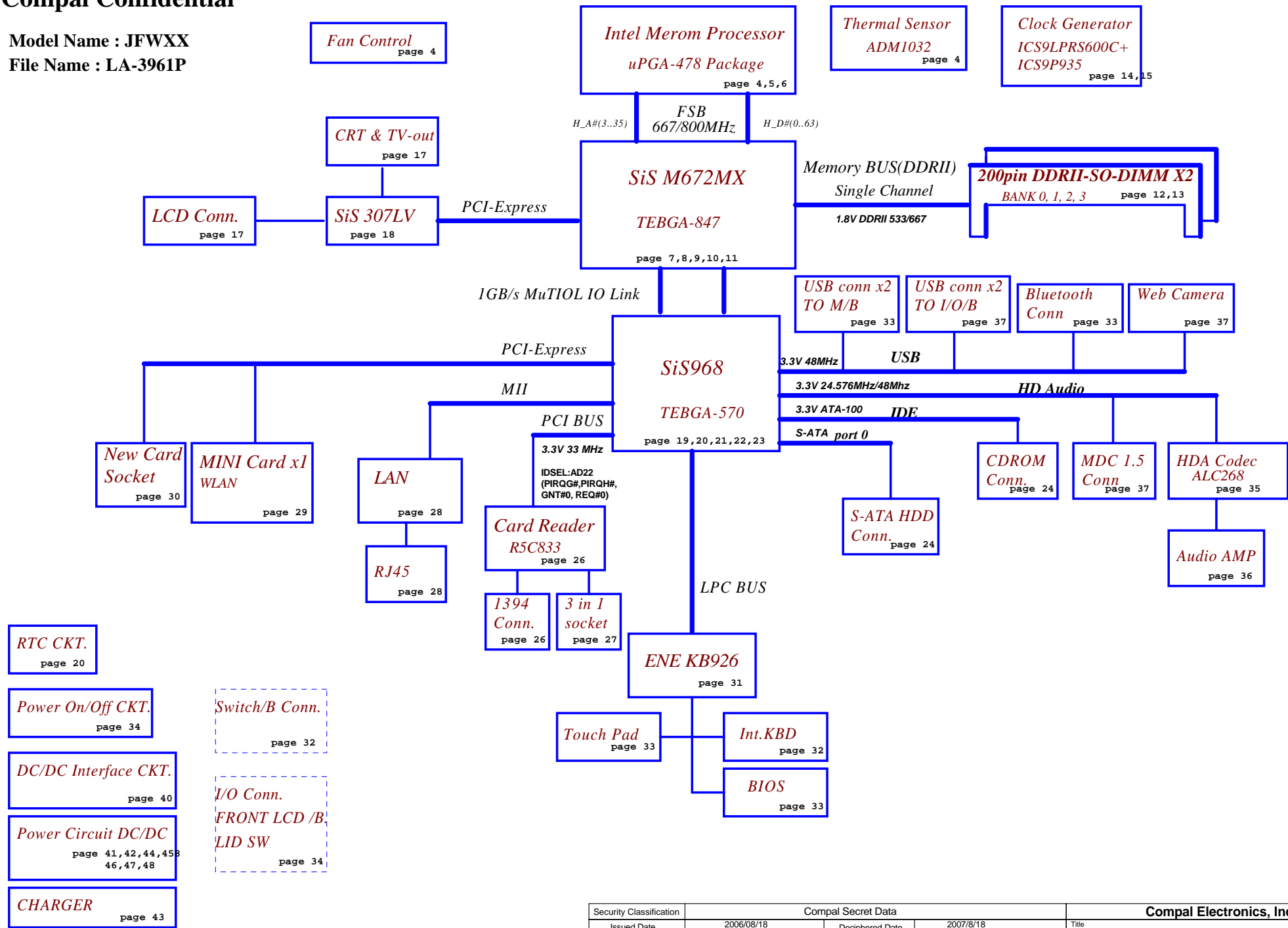
2007-09-06

REV: 0.3

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					JFWXX M/B LA-3961P Schematic
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				Rev	0.2

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Model Name : JFWXX  
File Name : LA-3961P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS ( Actual +0.9V )	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	PROJECT_ID
14W	R424 (Pull low)
15W	NA (Internal Pull High)

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+ Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH8M SM Bus address

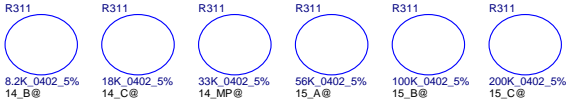
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Ra~ R312

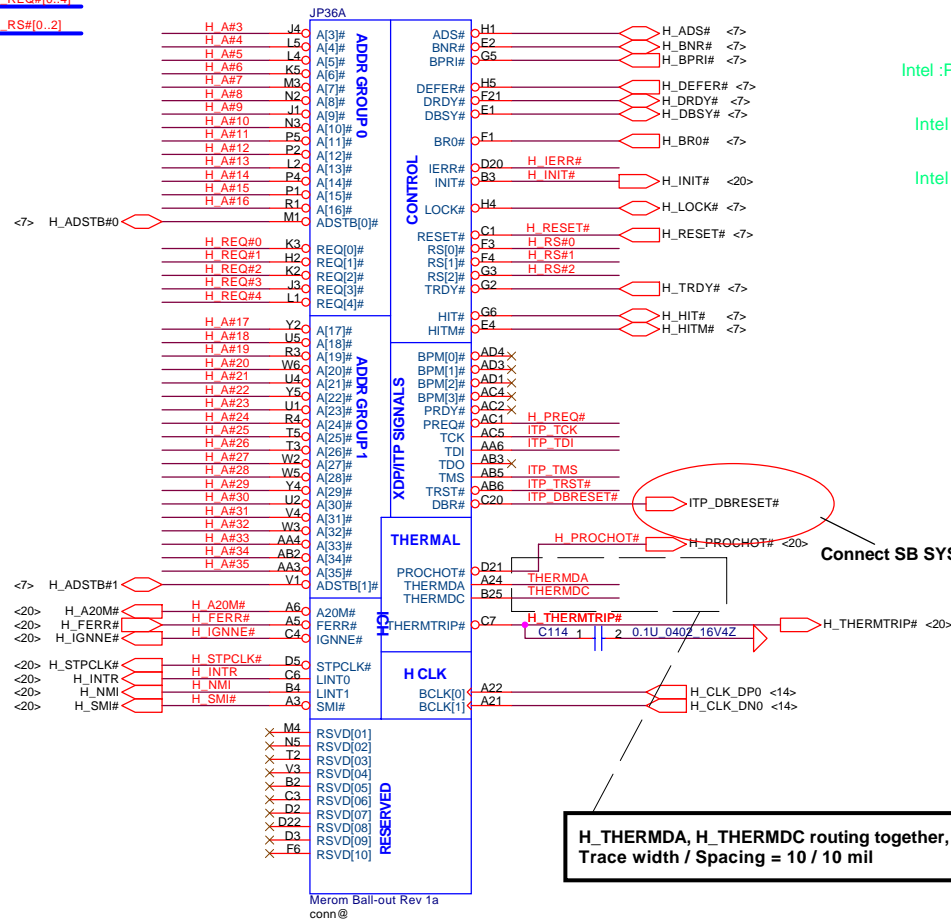
Rb~ R311



Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	Rb BOM Structure
0	0	0 V	0 V	0 V	14_A@
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	14_B@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	14_C@ ✓
3	33K +/- 5%	0.721 V	0.819 V	0.926 V	14_MP@
4	56K +/- 5%	1.054 V	1.185 V	1.325 V	15_A@
5	100K +/- 5%	1.489 V	1.650 V	1.819 V	15_B@
6	200K +/- 5%	2.019 V	2.200 V	2.386 V	15_C@ ✓
7	NC	3.135V	3.300 V	3.465 V	15_MP@

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<7> H\_A#[3..35] H\_A#[3..35]  
<7> H\_REQ#[0..4] H\_REQ#[0..4]  
<7> H\_RS#[0..2] H\_RS#[0..2]



H\_THERMDA, H\_THERMDC routing together,  
Trace width / Spacing = 10 / 10 mil

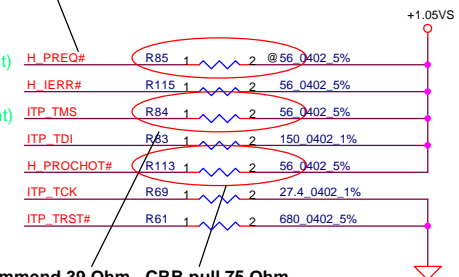
Trace length must short

Place close to CPU within 500mil

Intel :Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)

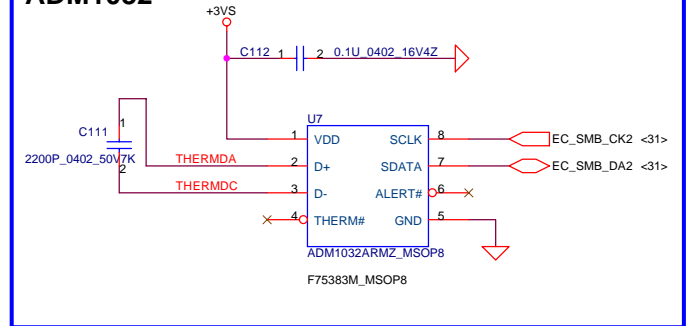
Intel :Pull-up 56ohm (Mount) SiS : Pull-up 54.9ohm (Mount)

Intel :Pull-up 56ohm (Mount) SiS : Pull-up 75ohm (Mount)

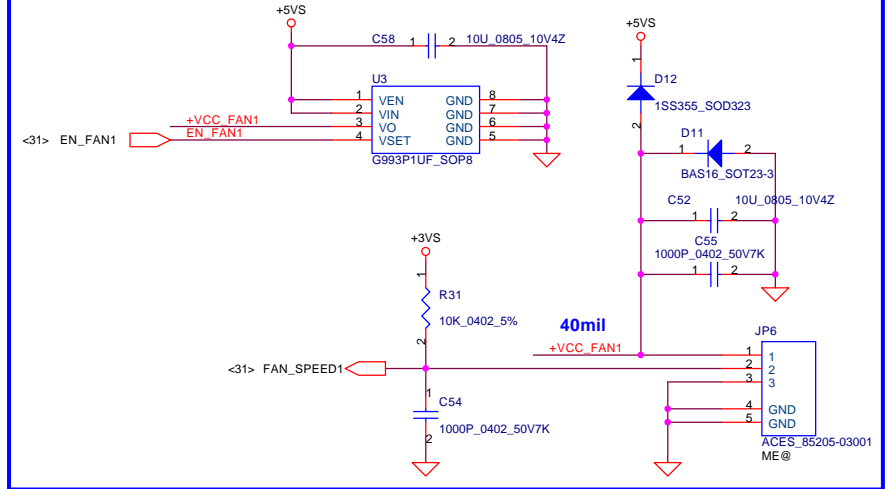


Checklist recommend 39 Ohm CRB pull 75 Ohm

ADM1032

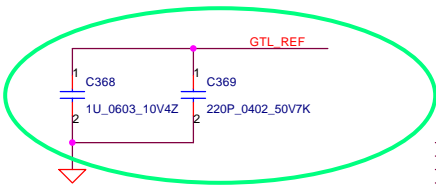


FAN1 Conn



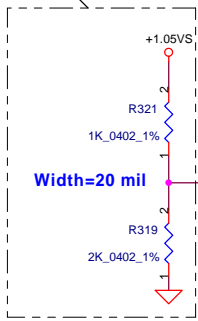
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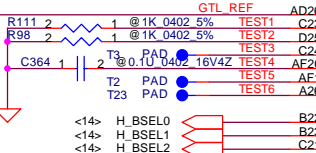


SiS Recommend

Close to CPU pin AD26 within 500mils.

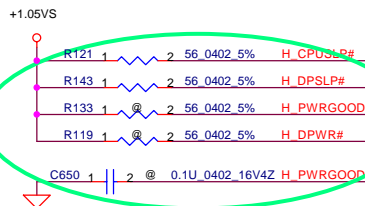


Width=20 mil



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0



Intel :Don't Pull-up SiS : Pull-up 56ohm (Mount)

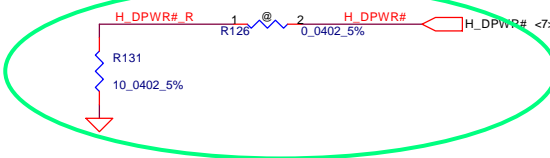
Intel :Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)

Intel :Don't Pull-up (Connecte to ICH) SiS : Pull-up 56ohm (Un-Mount)

Intel :Don't Pull-up SiS : Pull-up 56ohm (Un-Mount)

Intel :Don't Pull-down SiS :Pull-down Cap (Un-Mount)

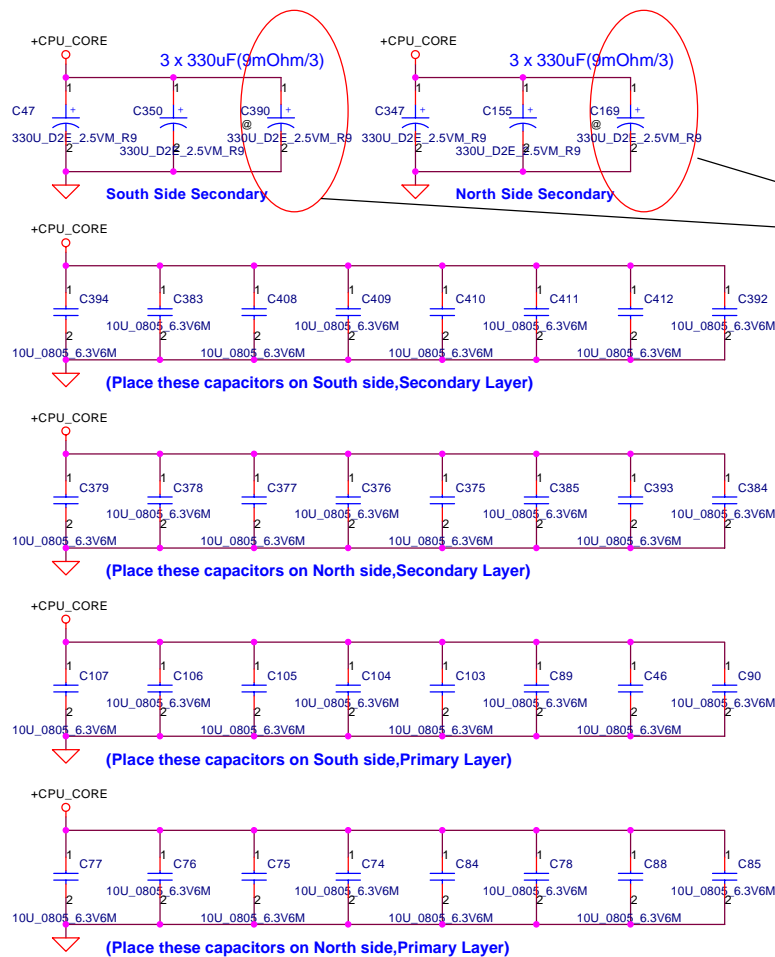
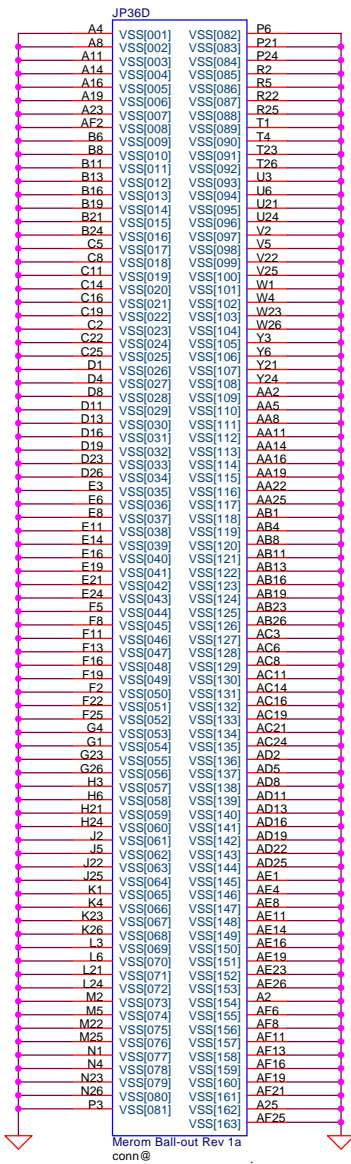
SiS Recommend



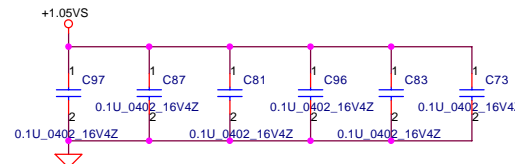
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

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+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

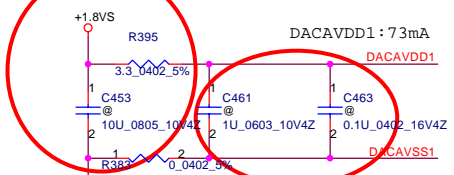
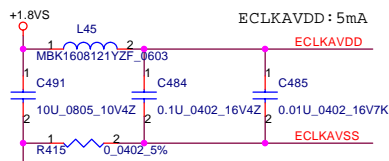
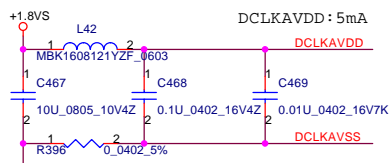
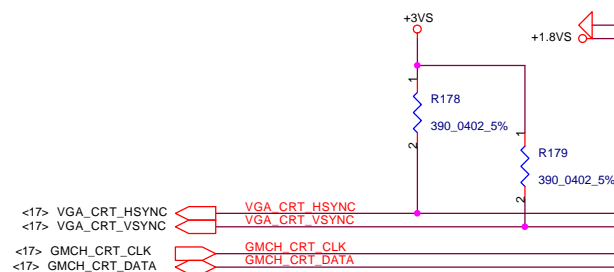
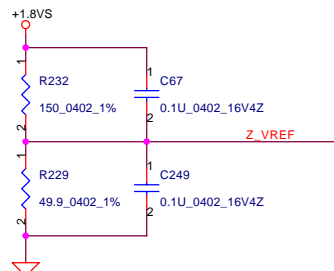
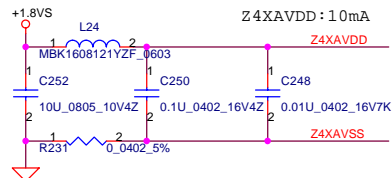


CRB no stuff. Reserved!

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DACAVDD1 Spec.  
Voltage : 1.5V +/- 5%  
Current : 100mA

7/30 modified to @

<19> ZAD[0..16] ZAD[0..16]

<14> Z\_CLK0 Z\_CLK0 AH10  
<19> ZDREQ ZDREQ AP8  
<19> ZUREQ ZUREQ AN8  
<19> ZSTB\_DP0 ZSTB\_DP0 AM7  
<19> ZSTB\_DN0 ZSTB\_DN0 AL7  
<19> ZSTB\_DP1 ZSTB\_DP1 AP4  
<19> ZSTB\_DN1 ZSTB\_DN1 AP5

ZAD0 AK10  
ZAD1 AM6  
ZAD2 AK11  
ZAD3 AK11  
ZAD4 AP7  
ZAD5 AJ9  
ZAD6 AP6  
ZAD7 AN6  
ZAD8 AK9  
ZAD9 AM4  
ZAD10 AK6  
ZAD11 AK8  
ZAD12 AN4  
ZAD13 AK7  
ZAD14 AL5  
ZAD15 AM5  
ZAD16 AM8

Z\_VREF AL9  
Z\_COMP\_P AP9  
Z\_COMP\_N AM9

Z4XAVDD AM10  
Z4XAVSS AN10

<17> VGA\_CRT\_R VGA\_CRT\_R D13  
<17> VGA\_CRT\_G VGA\_CRT\_G C12  
<17> VGA\_CRT\_B VGA\_CRT\_B C13

<17> GMCH\_CRT\_CLK GMCH\_CRT\_CLK R183  
<17> GMCH\_CRT\_DATA GMCH\_CRT\_DATA R182

VCOMP D15  
VVBWN C15  
VRSET C14

<7,19> INT\_N\_A INT\_N\_A R196  
<14> REF\_CLK0 REF\_CLK0 R195

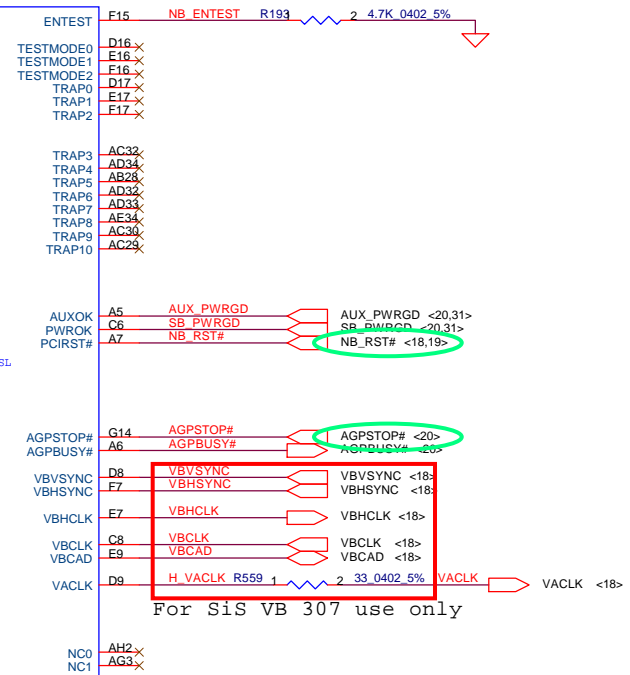
DACA\_VDD1 DACA\_VDD1 A12  
DACA\_VSS1 DACA\_VSS1 B12

DACA\_VDD2 DACA\_VDD2 A13  
DACA\_VSS2 DACA\_VSS2 B13

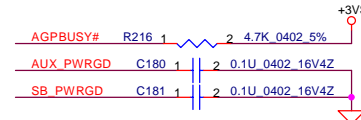
DCLKAVDD B10  
DCLKAVSS A11

ECLKAVDD A9  
ECLKAVSS B8

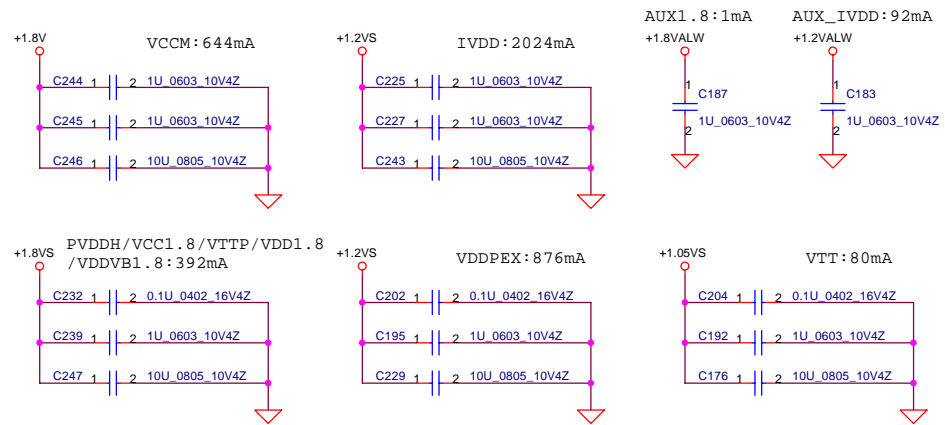
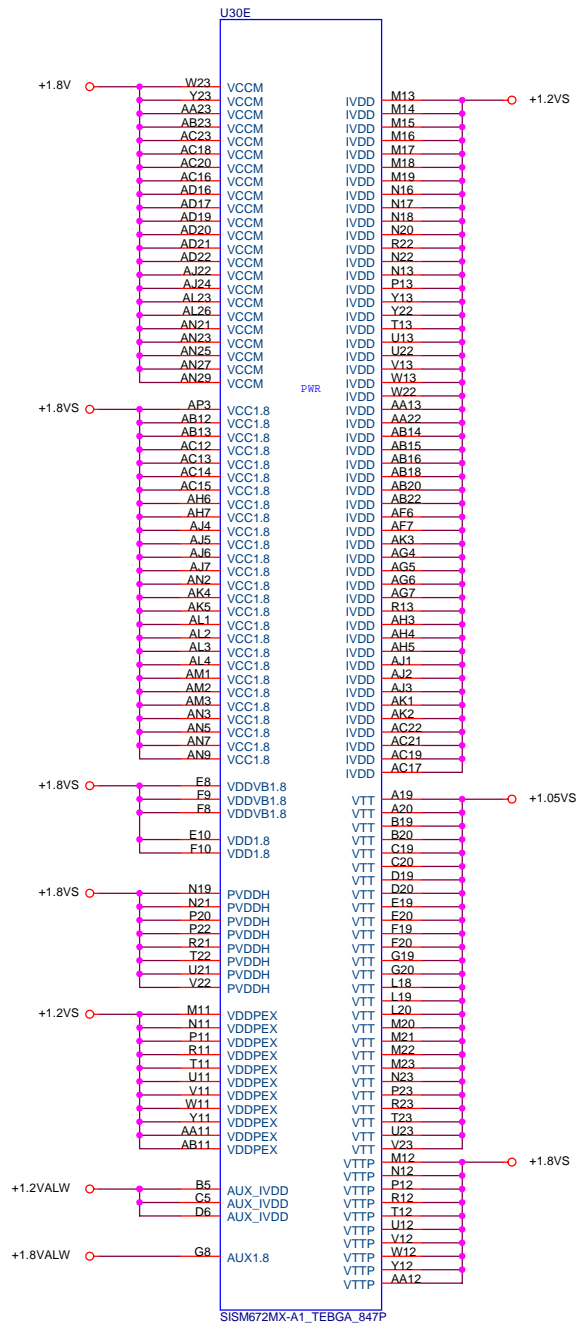
SISM672MX-A1\_TEBGA\_847P



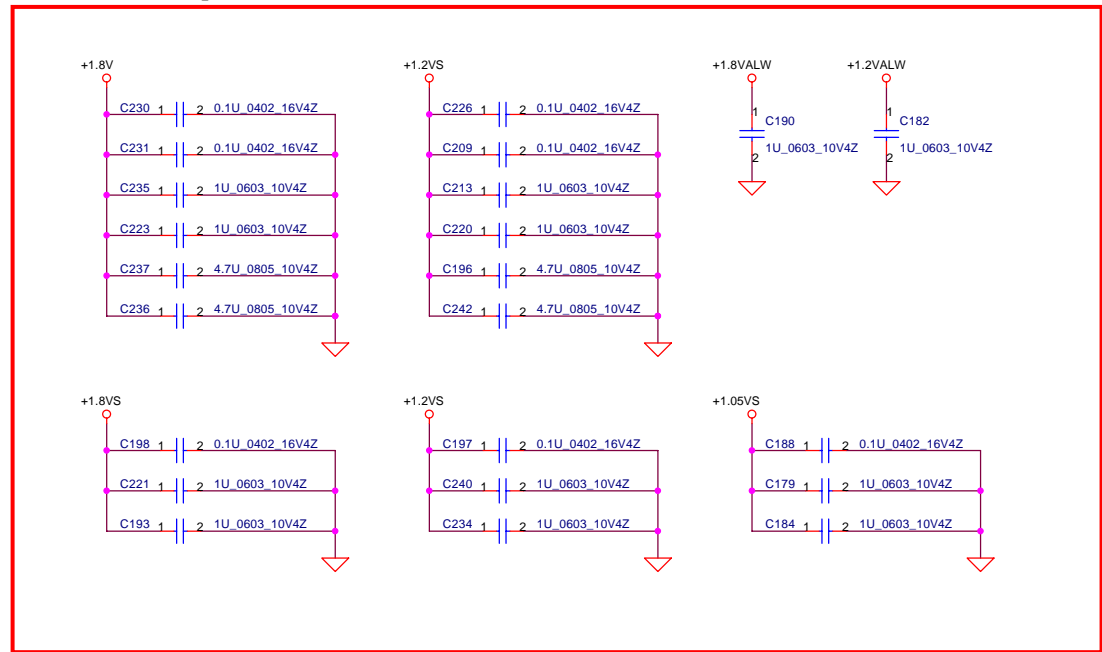
For Sis VB 307 use only



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Place these Cap under M672MX solder side.



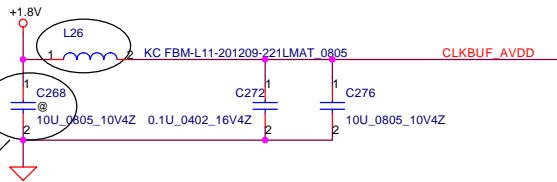
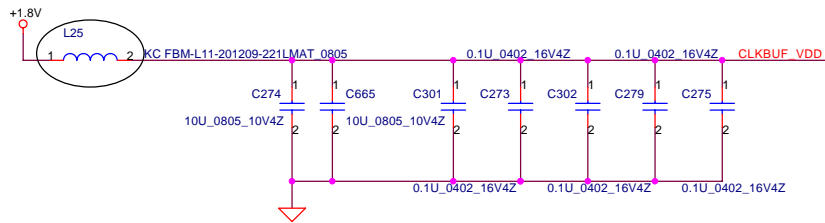
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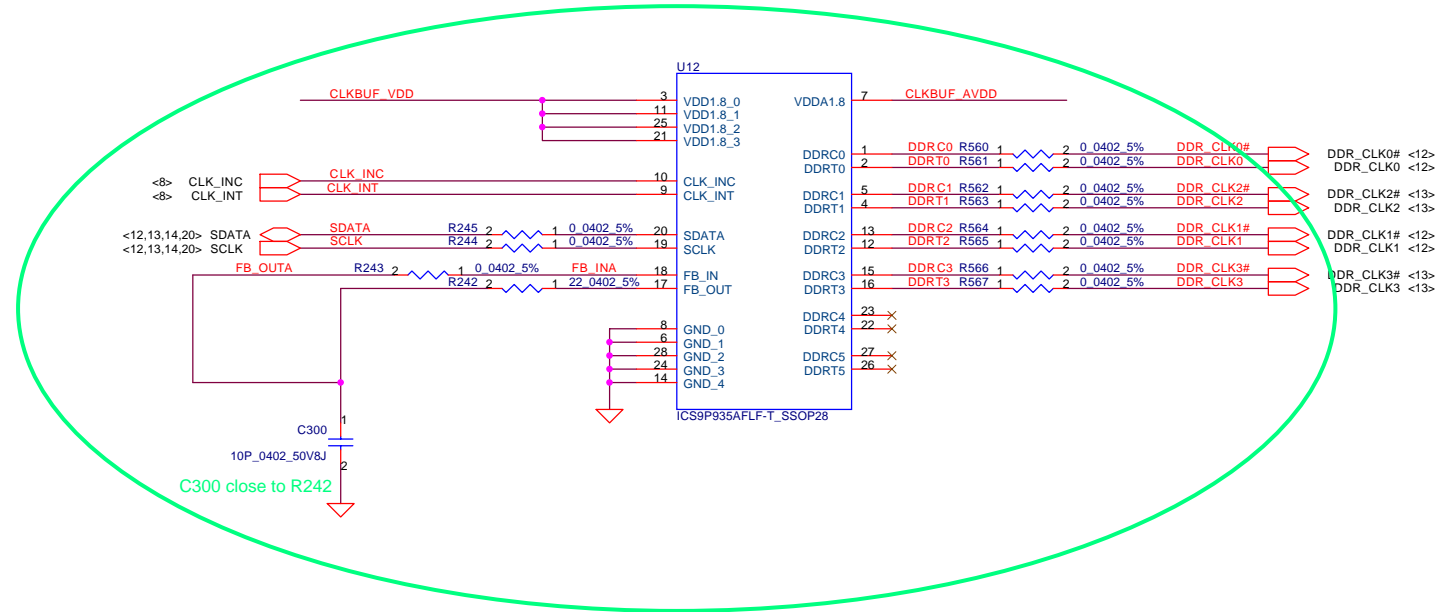






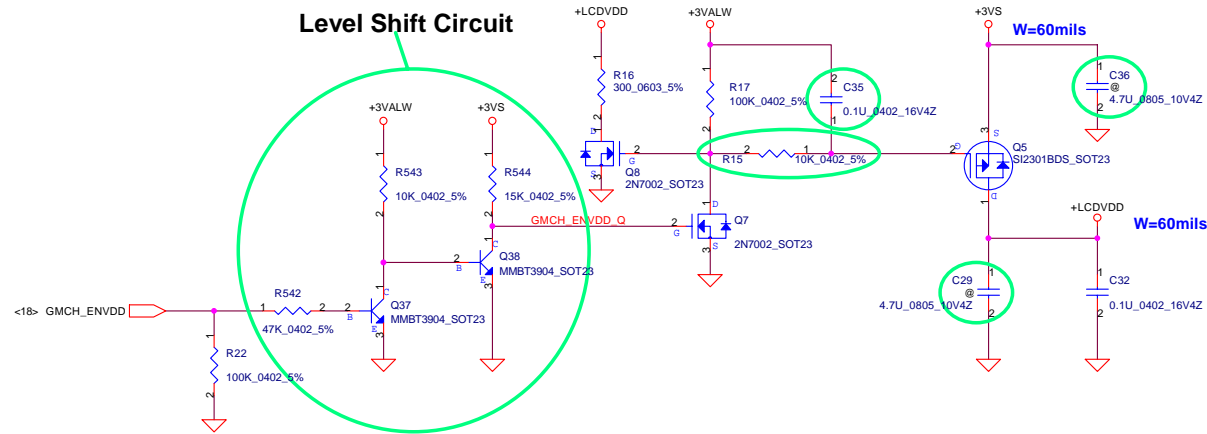
Reference schematic use 1206

Horizontal rotate

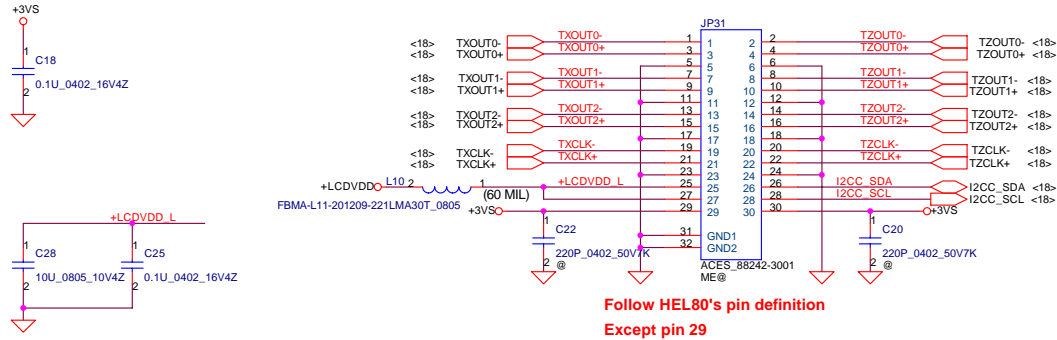


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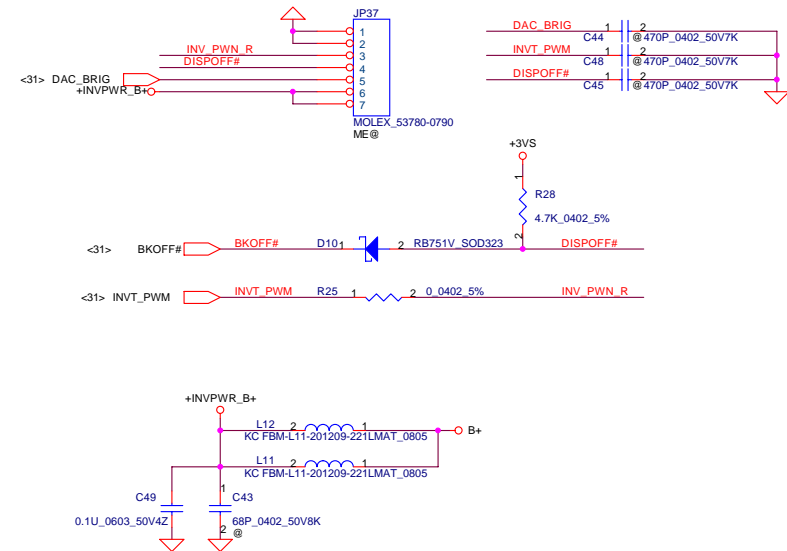
# LCD POWER CIRCUIT



## LCD/PANEL BD. Conn.

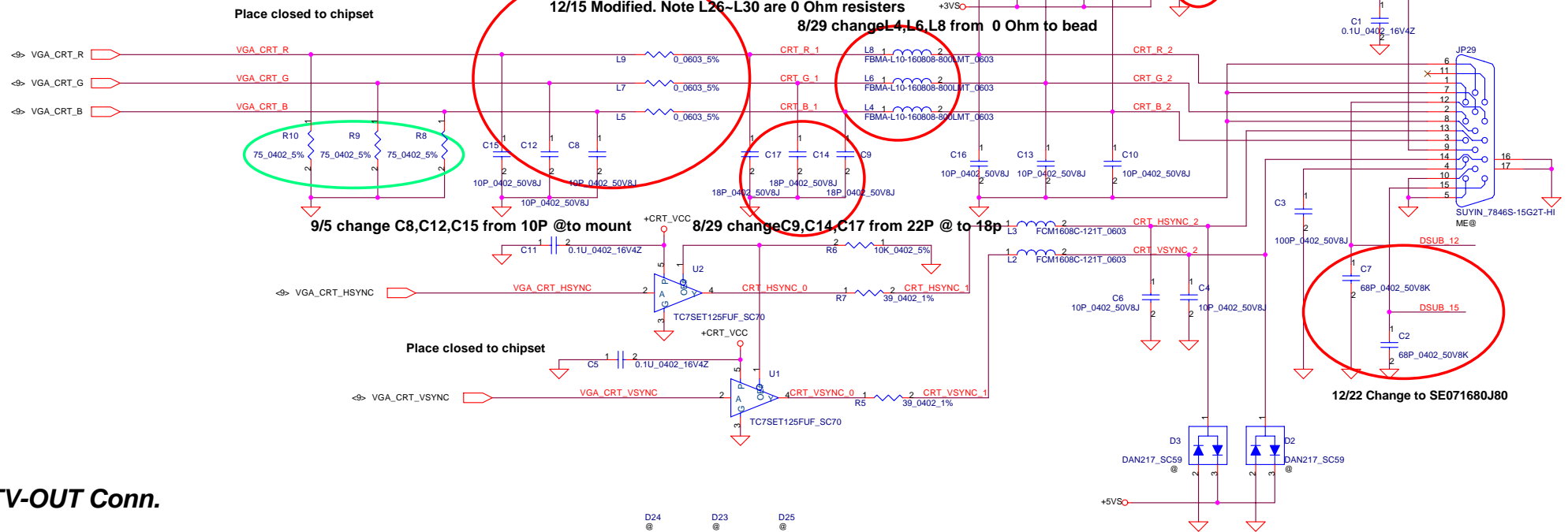


## INVERTER Conn.

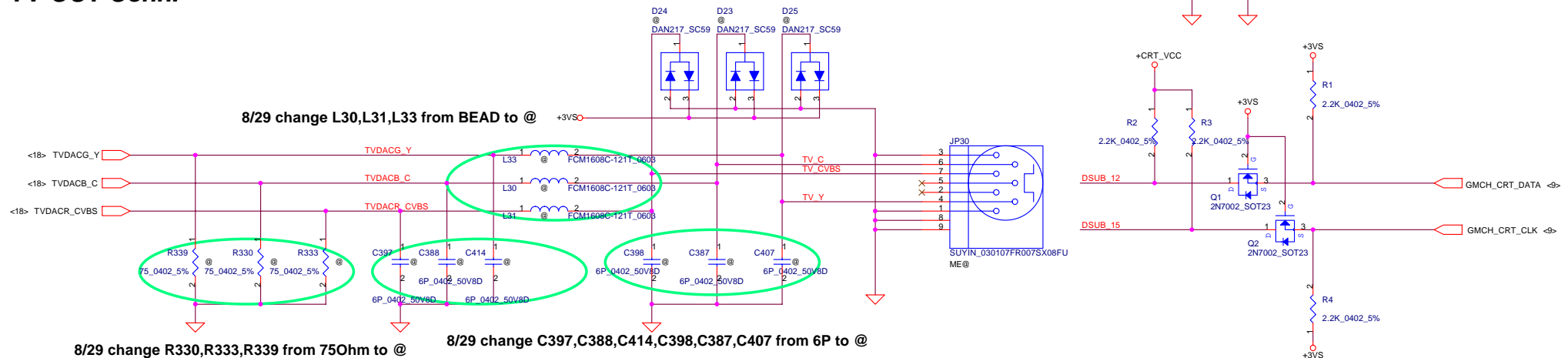


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# CRT Connector



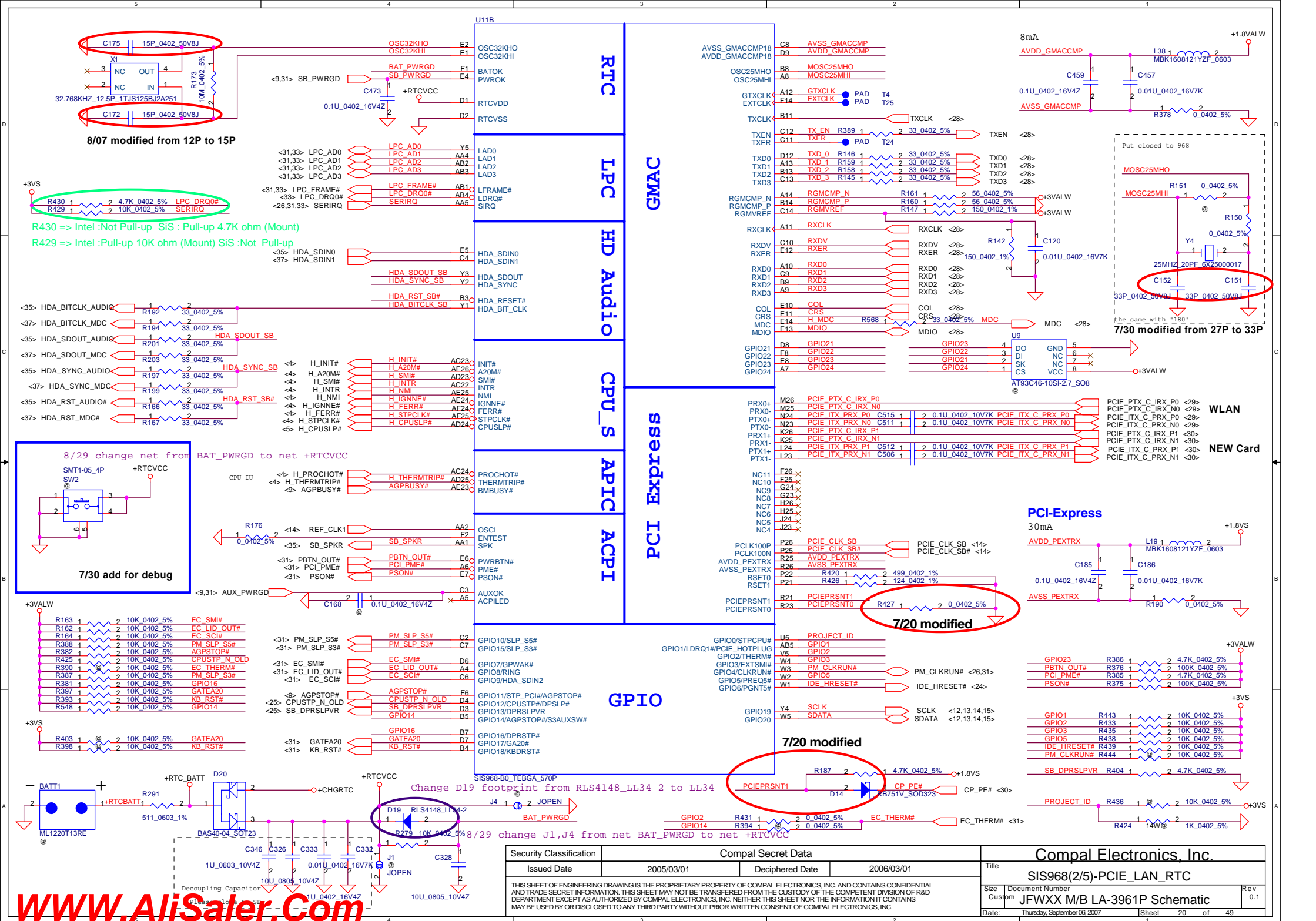
## TV-OUT Conn.

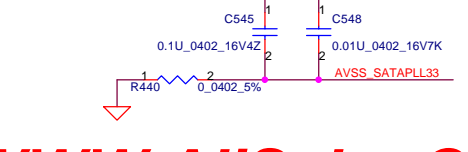
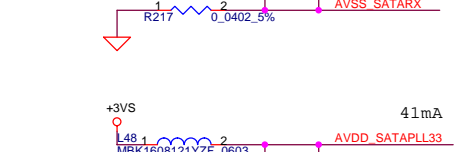
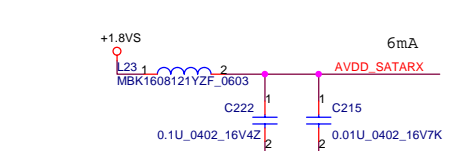
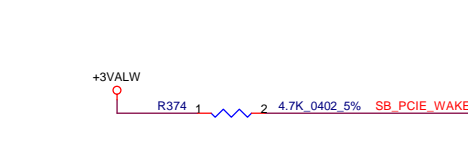
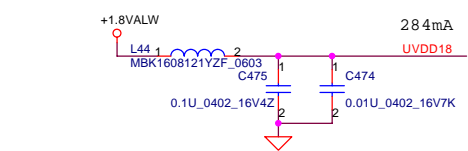
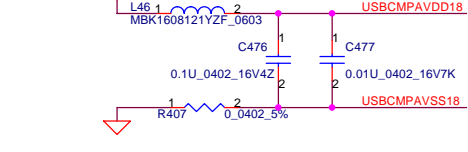
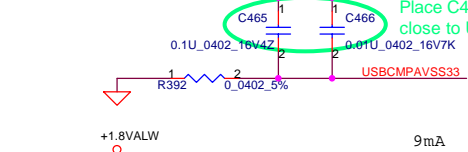
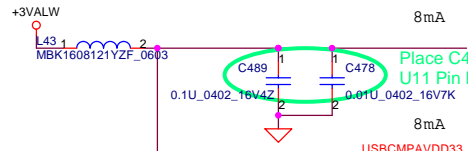
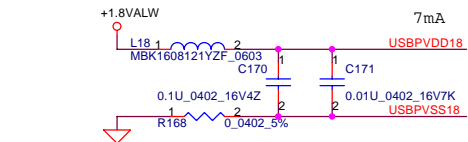


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				JFWXX M/B LA-3961P Schematic	Rev 0.1
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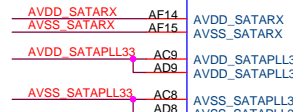
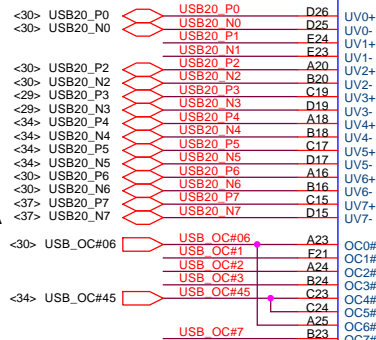




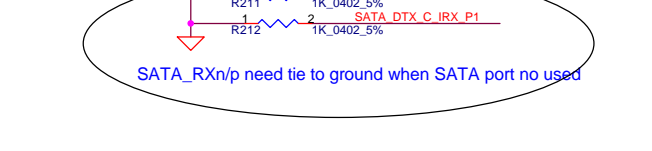
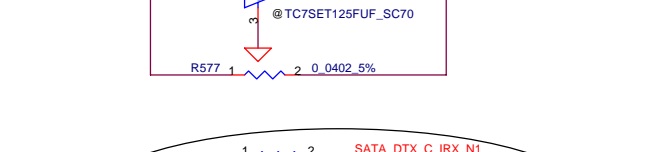
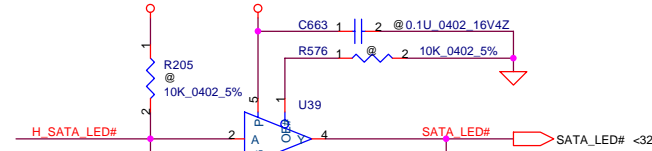
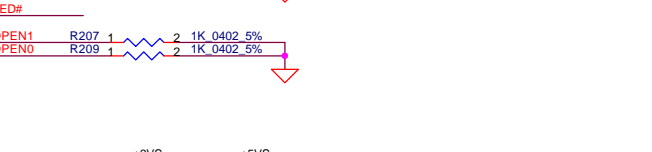
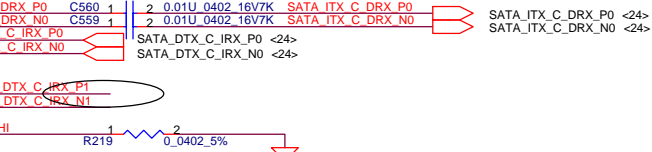
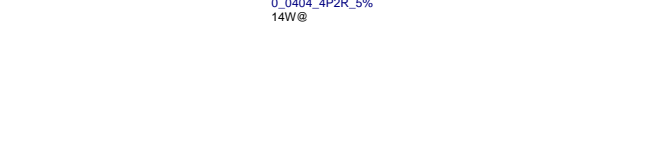
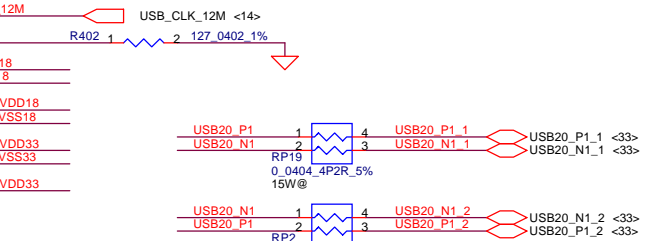
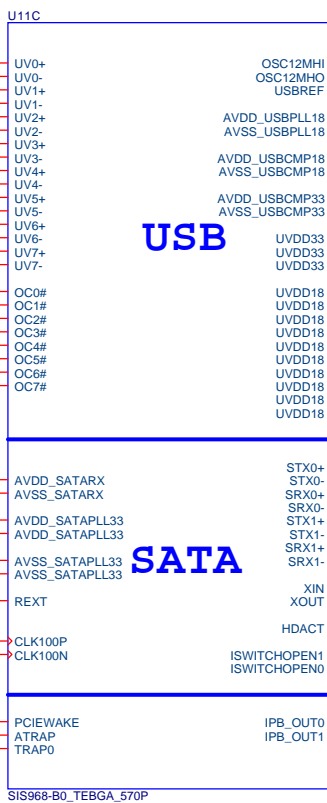
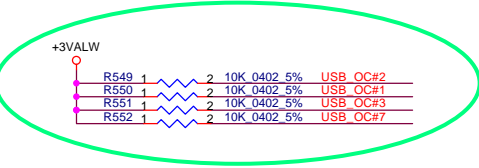
**USB BT**  
**New Card**  
**WLAN**  
**USB**  
**USB**  
**CAMERA**

Place C478,C489 close to U11 Pin F17,F19,F22

Place C465,C466 close to U11 Pin D2

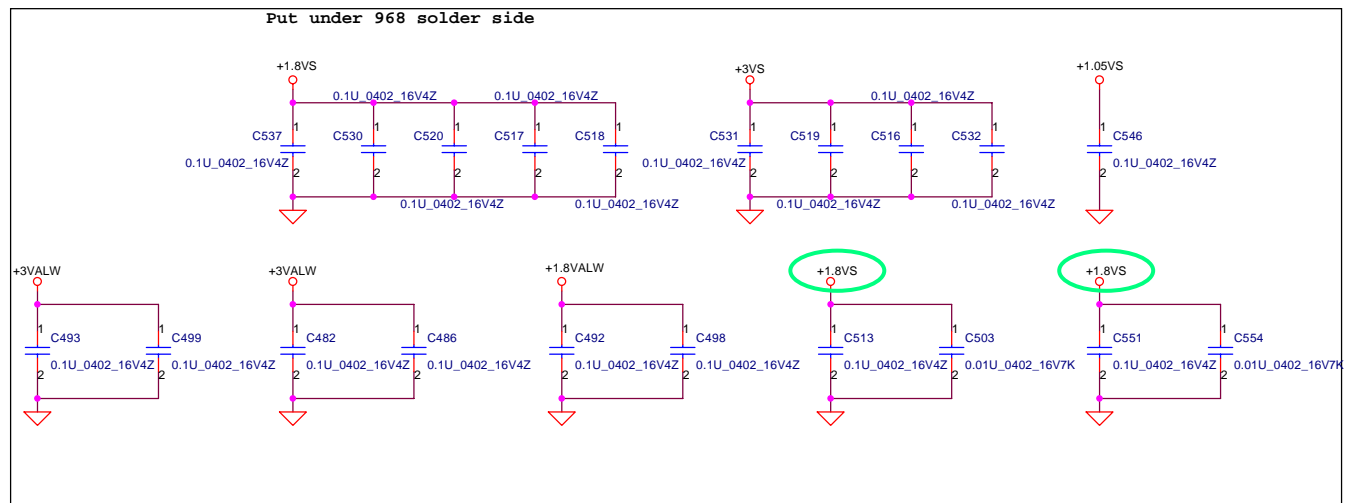
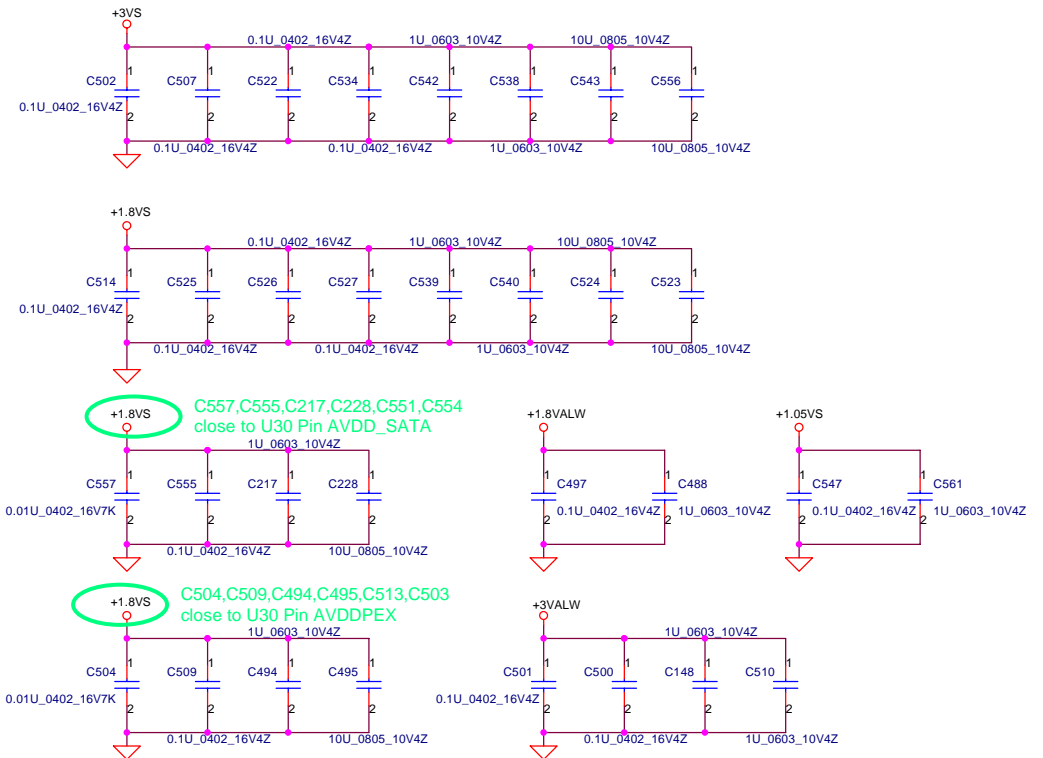
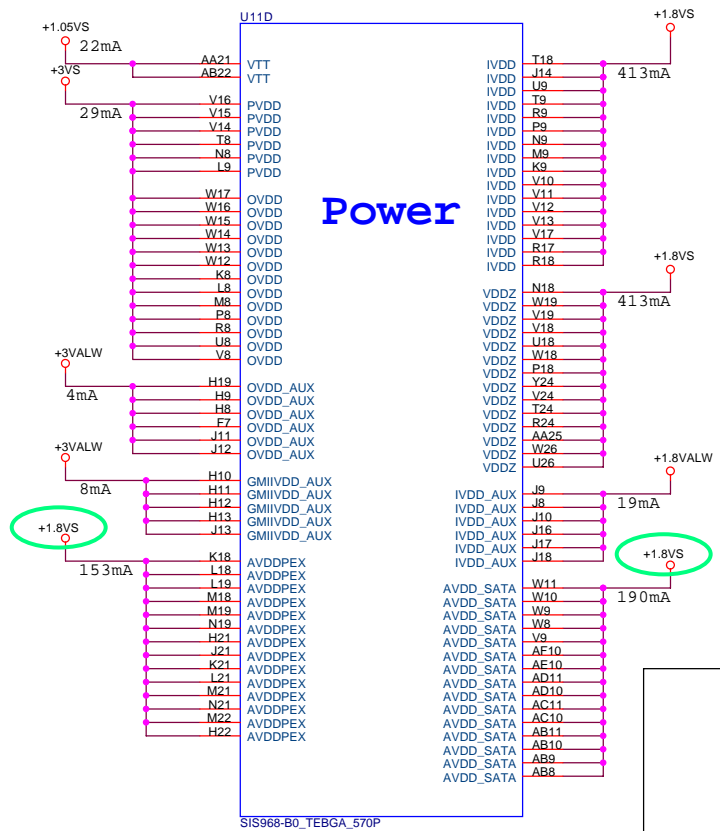


133MHz:Internal pull-down  
66MHz:External pull-up

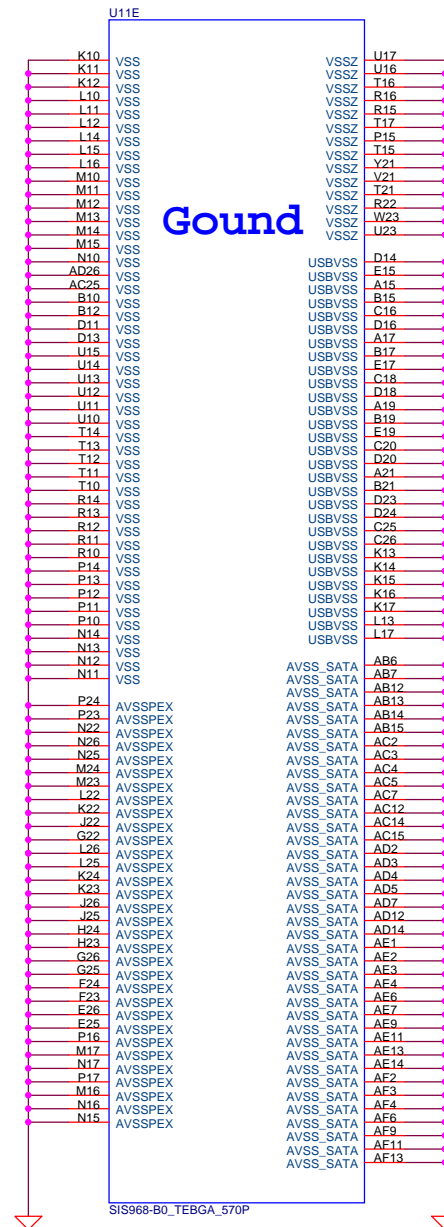


SATA\_RXn/p need tie to ground when SATA port no used

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Size	Document Number	JFWXX M/B LA-3961P Schematic		Rev	
Custom				0.1	
Date:	Thursday, September 06, 2007	Sheet	21	of 49	

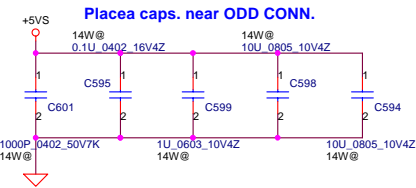


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Size	Document Number	JFWXX M/B LA-3961P Schematic		Rev	0.1
Date:	Thursday, September 06, 2007	Sheet	22	of	49

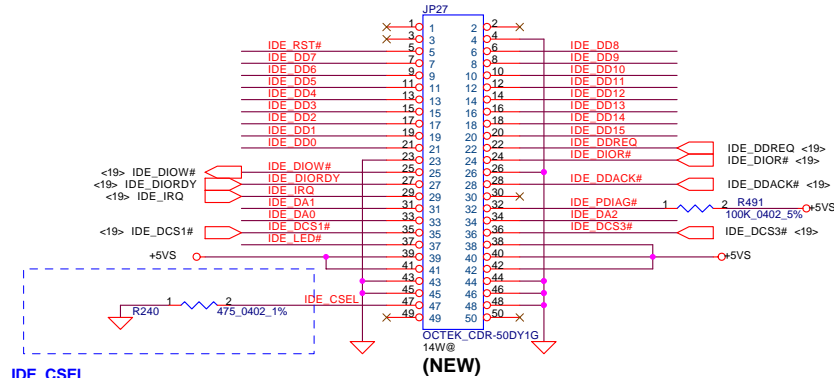


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	SIS968(5/5)-GND	
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				Custom	JFWXX M/B LA-3961P Schematic	0.1
				Date:	Thursday, September 06, 2007	Sheet 23 of 49

# 14W ODD Conn.

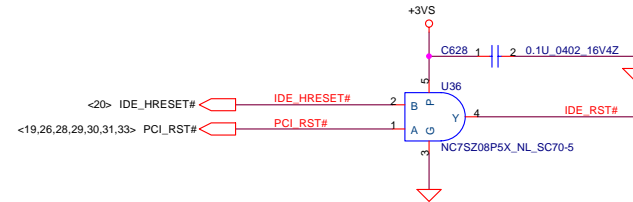


<19> IDE\_DD[0..15] IDE\_DD[0..15]  
<19> IDE\_DA[0..2] IDE\_DA[0..2]

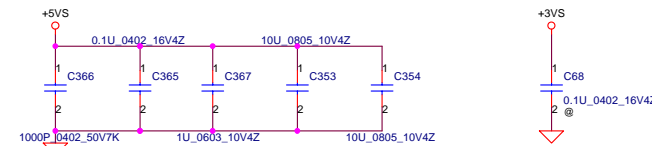


IDE\_CSEL  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)

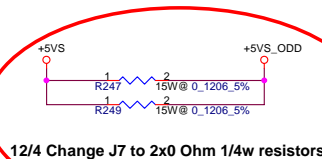
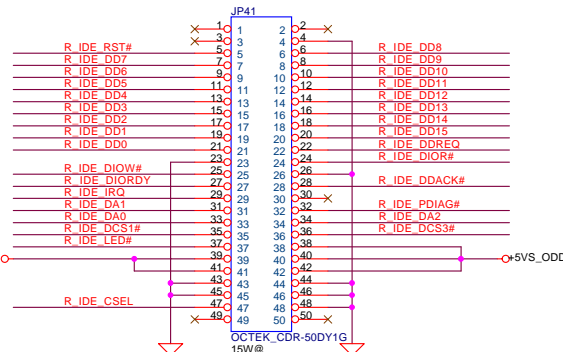
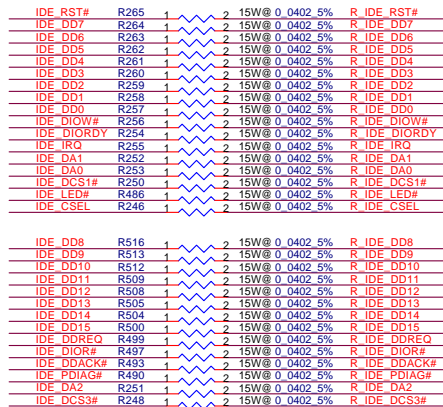
+5VS R487 100K\_0402\_5% IDE\_LED#



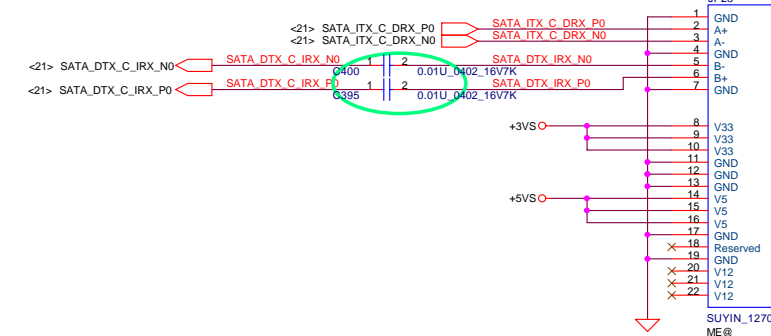
# SATA HDD Conn.



# 15W ODD Conn.



12/4 Change J7 to 2x0 Ohm 1/4W resistors



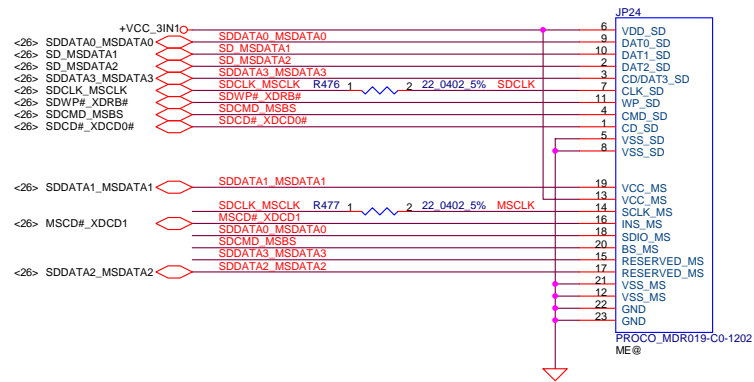
(NEW)  
Change Library

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		Size B		Document Number						Rev 0.1	
		JFWXX M/B LA-3961P Schematic									
		Date:		Thursday, September 06, 2007			Sheet		24 of 49		

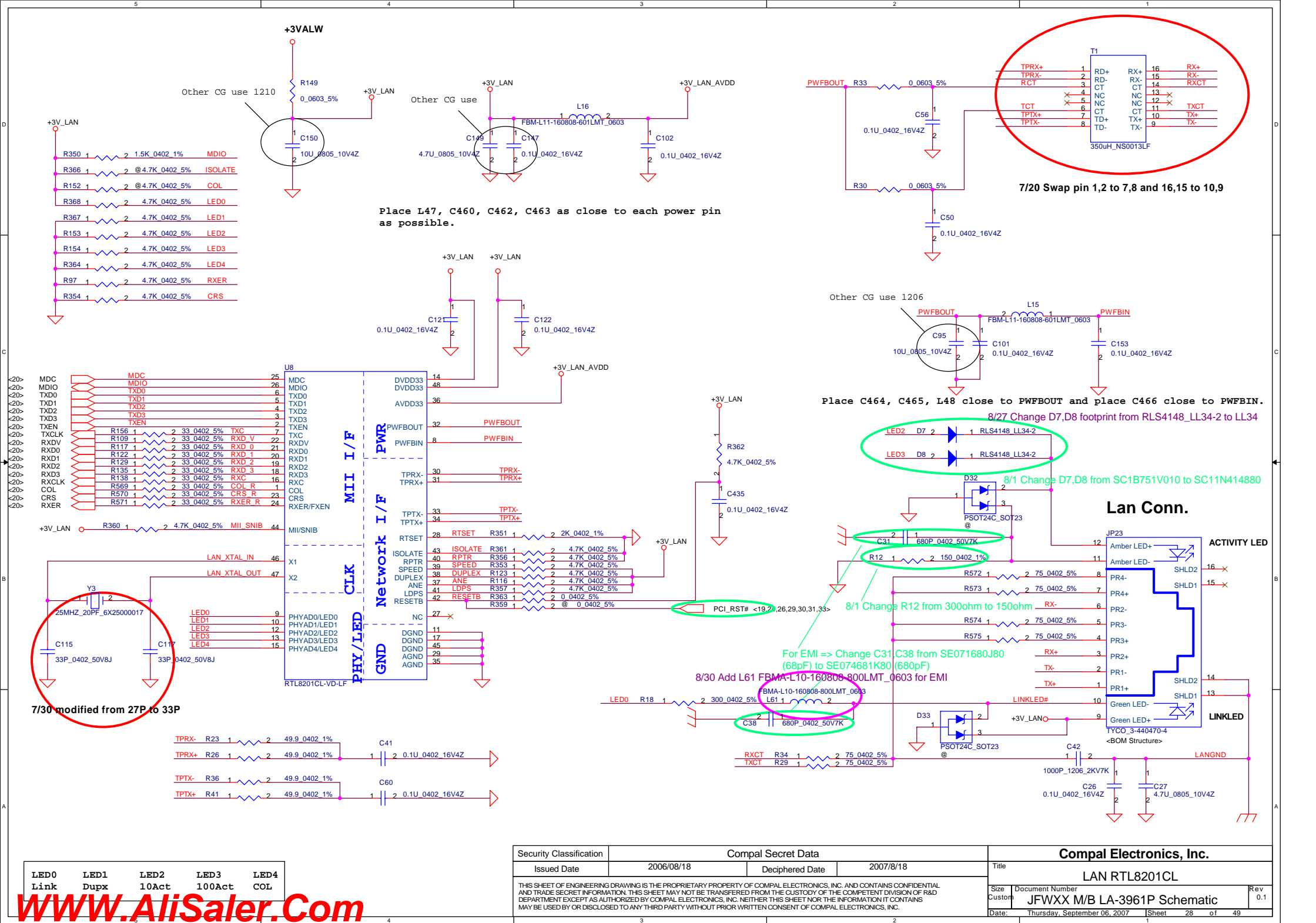




### 3 in 1 Card Reader

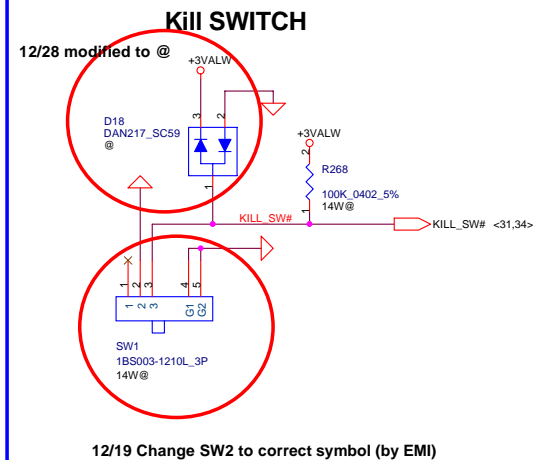
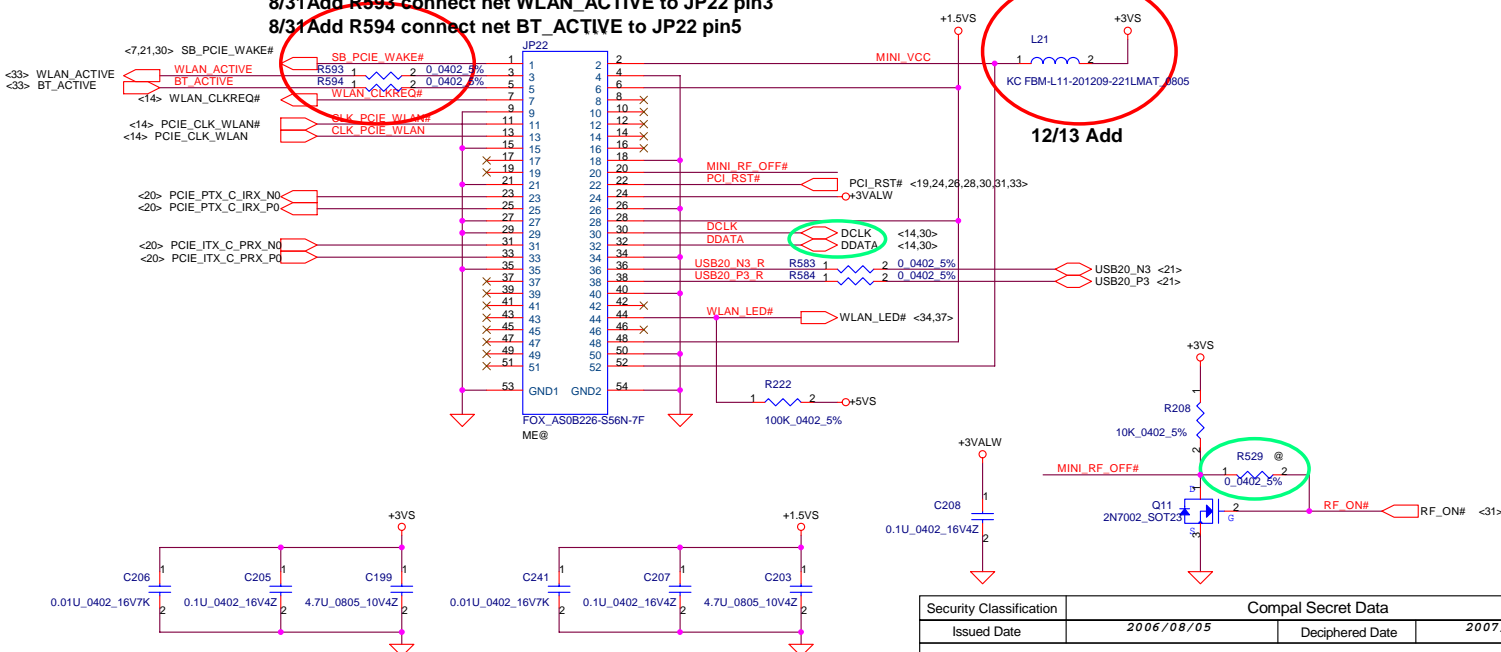


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				Custom	JFWXX M/B LA-3961P Schematic
				Date:	Thursday, September 06, 2007
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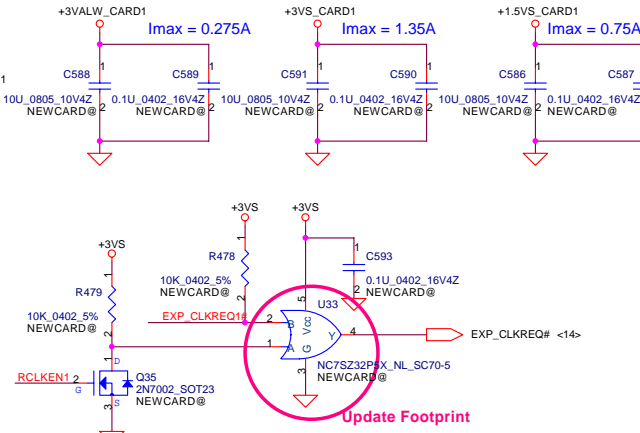
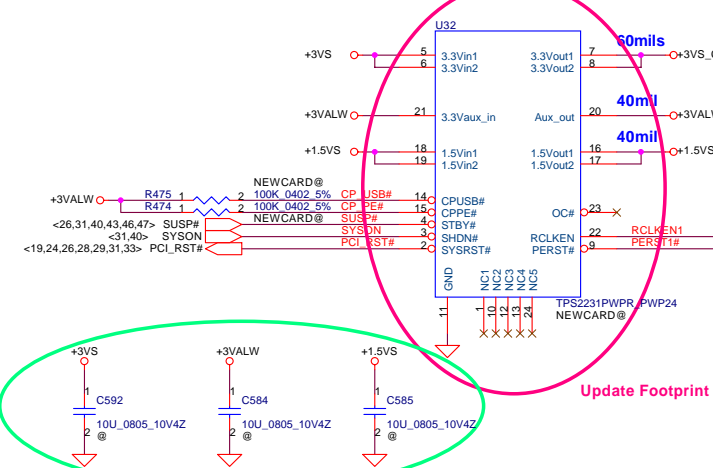
## Mini-Express Card for WLAN

8/31 Add R593 connect net WLAN\_ACTIVE to JP22 pin3  
8/31 Add R594 connect net BT\_ACTIVE to JP22 pin5

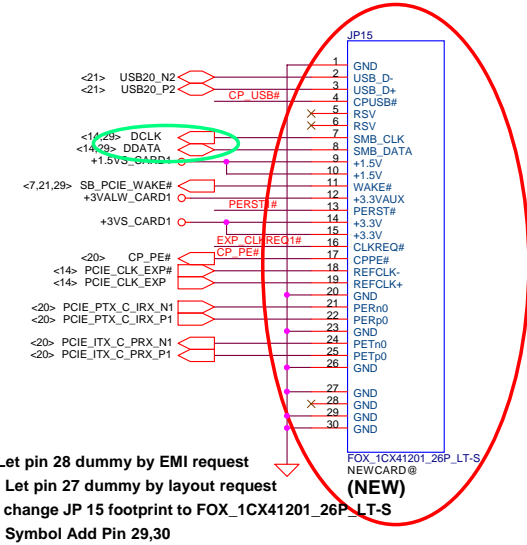


Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Mini-Card/Kill SW	
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				JFWXX	M/B LA-3961P Schematic
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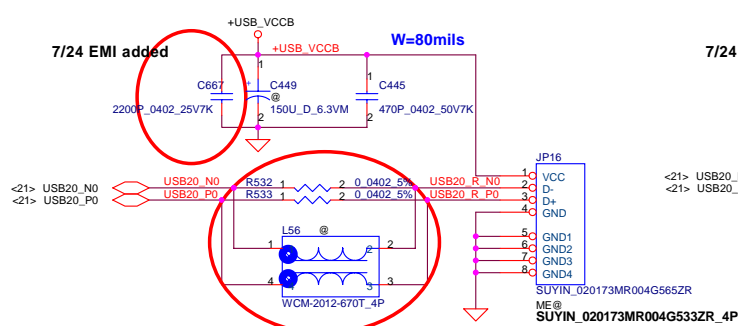
## New Card Power Switch



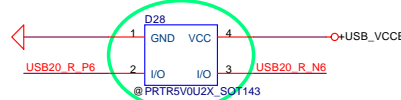
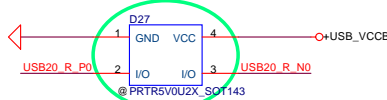
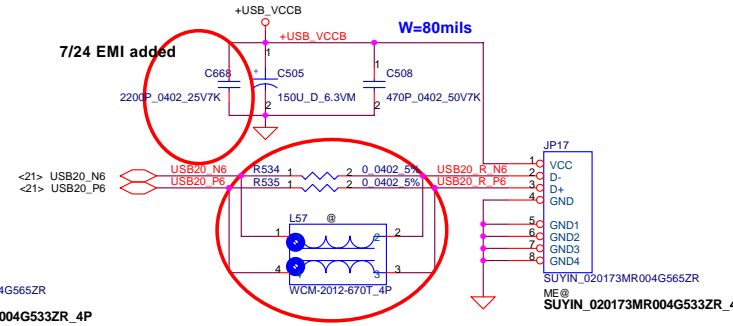
## New Card Socket (Left/TOP)



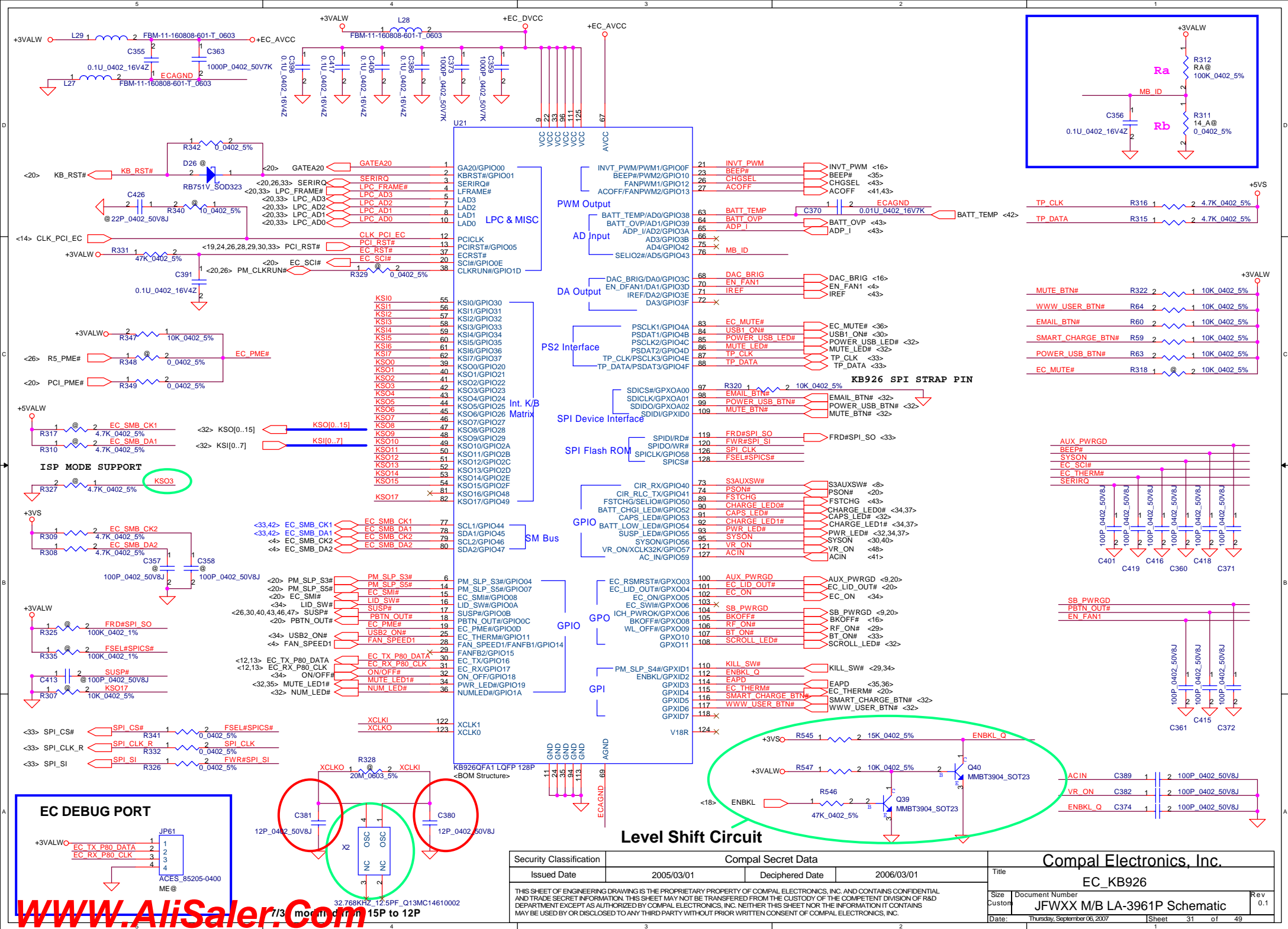
## USB CONN. 1



## USB CONN. 2

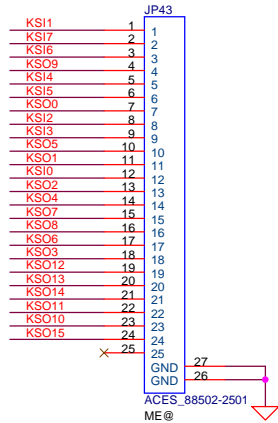


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size B	Document Number	JFWXX M/B LA-3961P Schematic		Rev 0.1	
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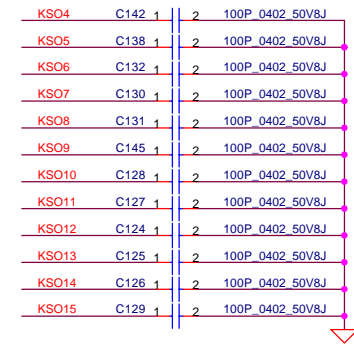
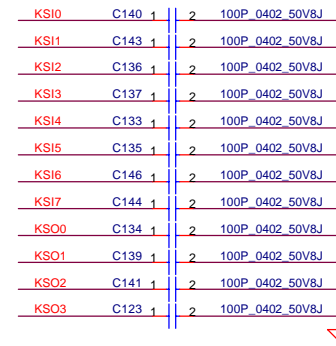
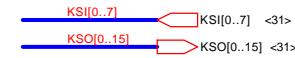
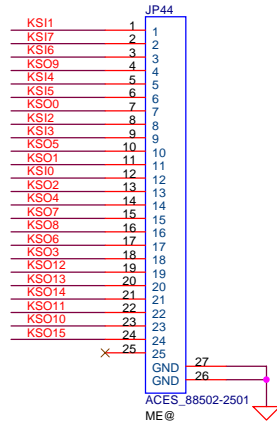


# INT\_KBD Conn.

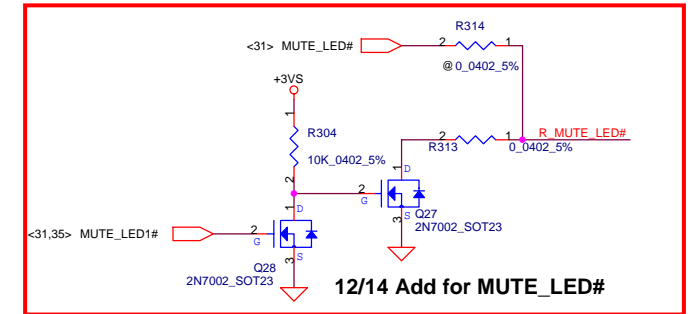
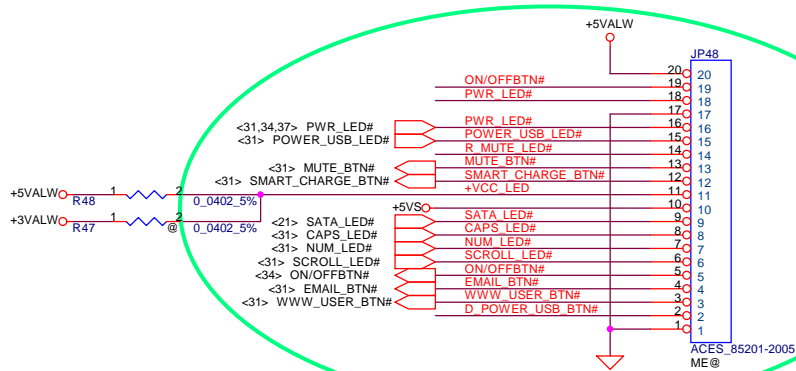
## For JFW91



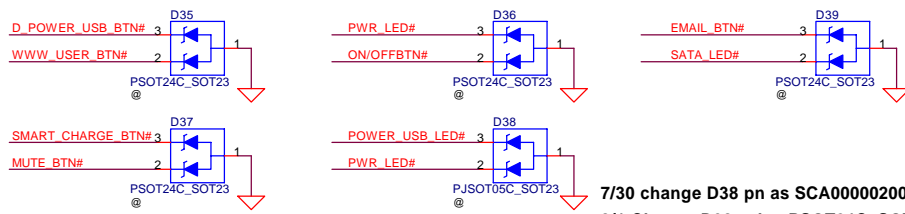
## For JFW01



## Switch Board Conn.



## 7/30 EMI added



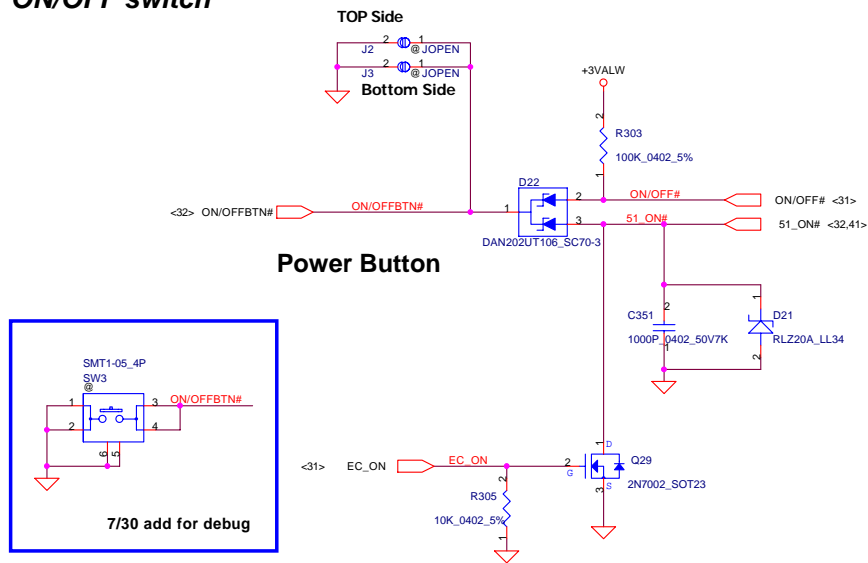
7/30 change D38 pn as SCA00000200

8/1 Change D38 value PSOT24C\_SOT23 from to PJSOT05C\_SOT23 , Add D39

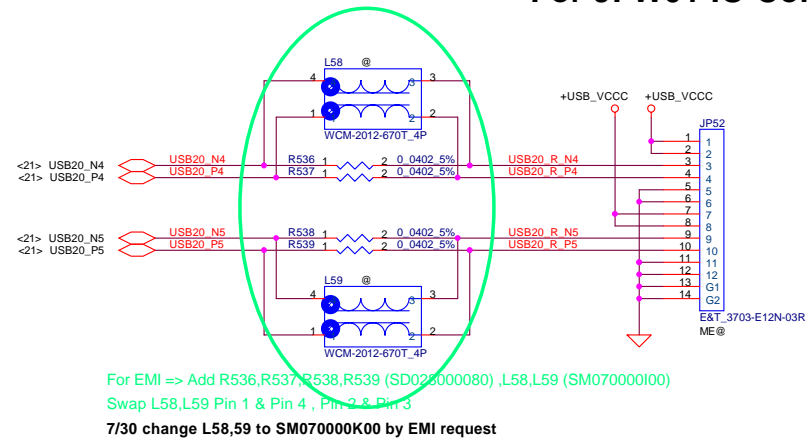
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	JFWXX M/B LA-3961P Schematic		Rev	
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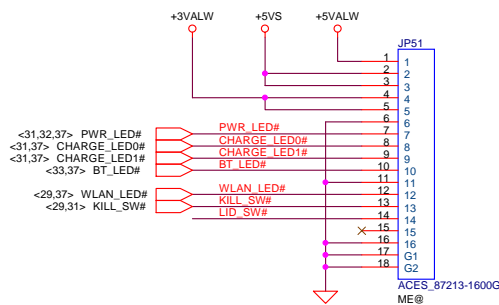
## ON/OFF switch



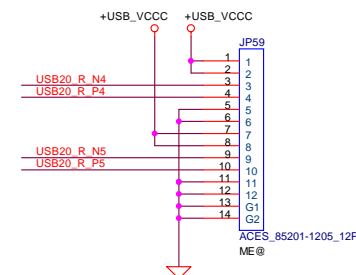
## For JFW01 IO Conn.



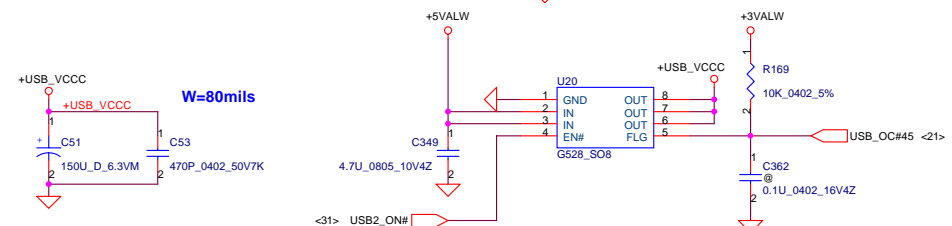
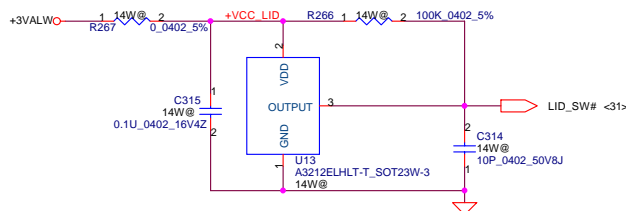
## Front LED Board



## For JFW91 IO Conn.



## Lid Switch



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								2007/8/18			
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								PWROK/LID/Front/IO Board			
								Document Number			
								JFWXX M/B LA-3961P Schematic			
								Rev			
								0.1			
								Date: Thursday, September 06, 2007			
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## +AVDD\_AC97 +3VS\_DVDD



**PCI Beep**

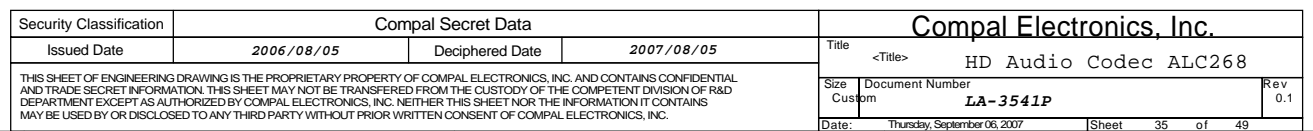
## CardBus Beep

9/19 Realtek suggest  
Add bypass schematic.

**SENSE FOR Ext. Mic.**

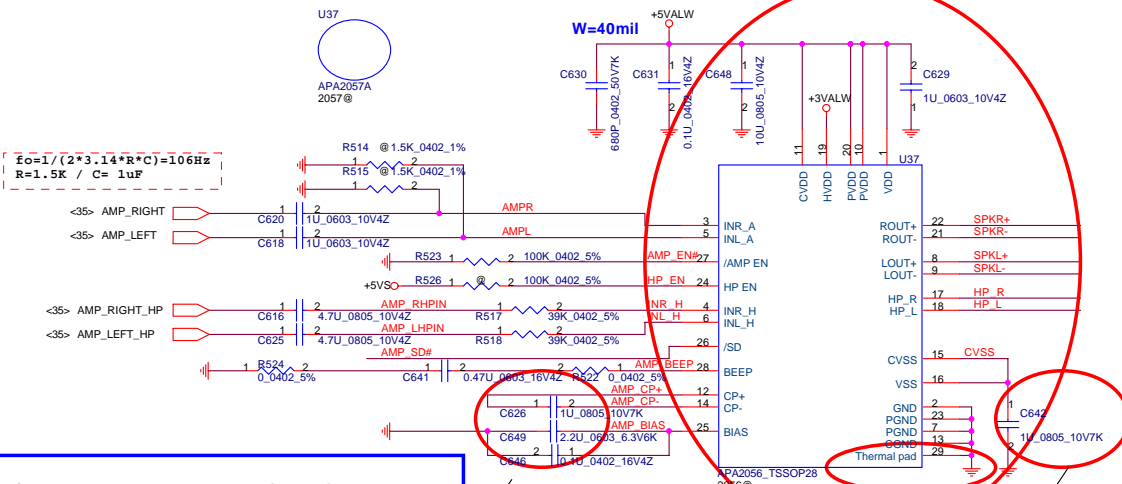


### Regulator for CODEC



# APA2056 SPK/HP Amplifier

7/20 Add U37 for APA2057A SA00001QD00



9/5 If implement AMP BEEP, Swap C641 and R524. R524 change from 0 Ohm to 47K

IN\_A Gain = 10dB (Internal Speaker)  
IN\_H Gain = 0dB (Headphone)

12/1 Modified to X7R

12/27 C46 change PN to SE092105K80

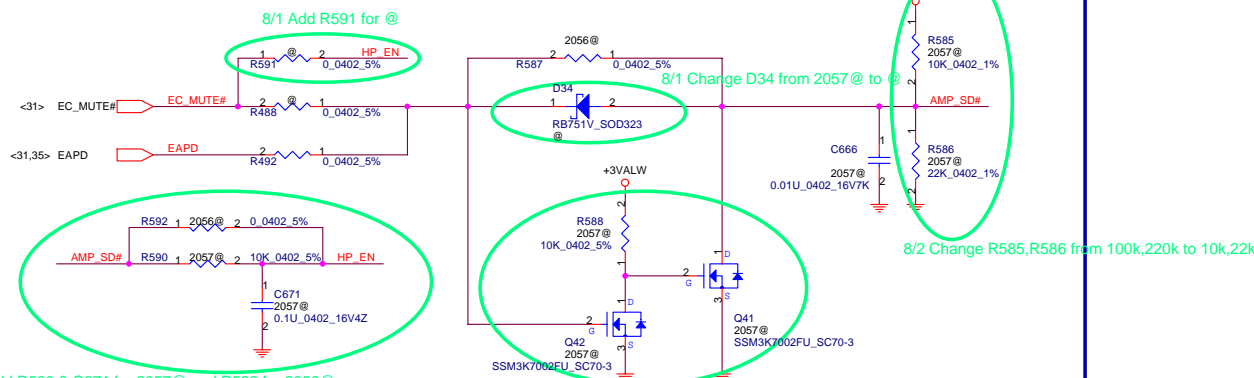
4/19 Modified this symbol to add pin29 for thermal pad use.

Do not re-copy this symbol for other use

12/1 Modified to X7R

12/27 C48 change PN to SE092105K80

7/20 Add below circuit for APA2057 gain tuning use



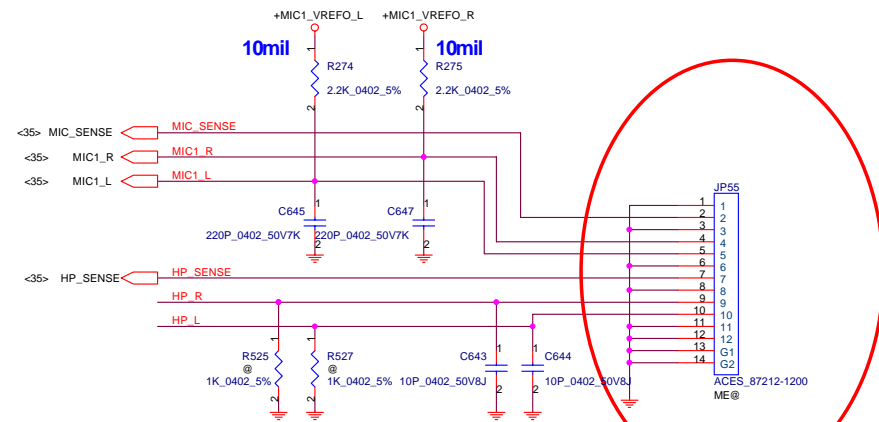
8/1 Add R590 & C671 for 2057@ and R592 for 2056@

Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

+5VALW assume equal 5.1V

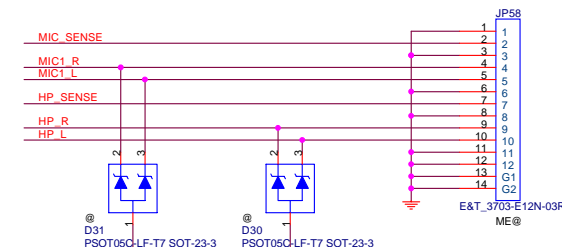
Gain= 10dB

10 x 220 / 320 = 3.5

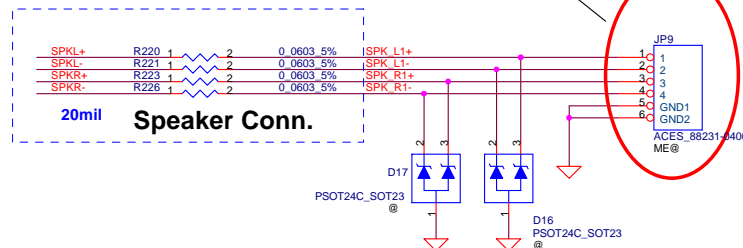


12/13 Modified this symbol for pin 13 and 14.  
Do not re-copy this symbol for other use

12/7 Added for 15w" use

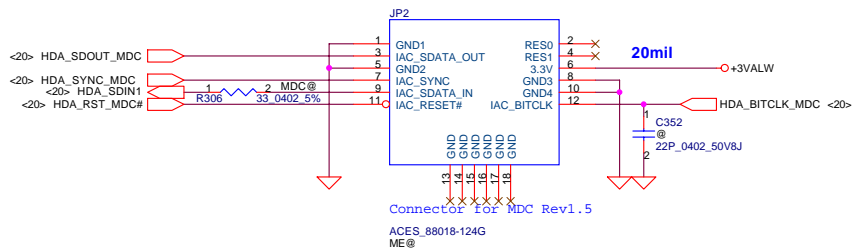


1/31 change JP9 following JP50

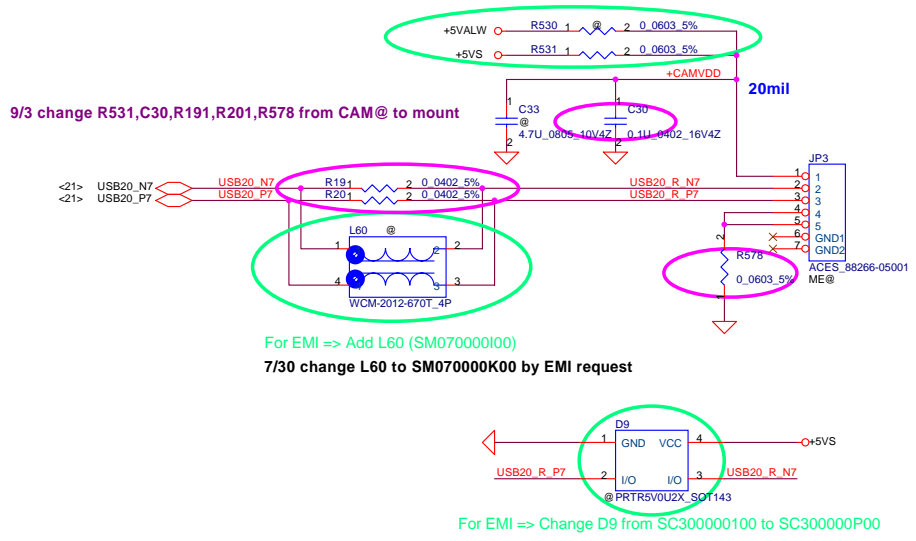


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				Date	Thursday, September 06, 2007
				Sheet	36 of 49

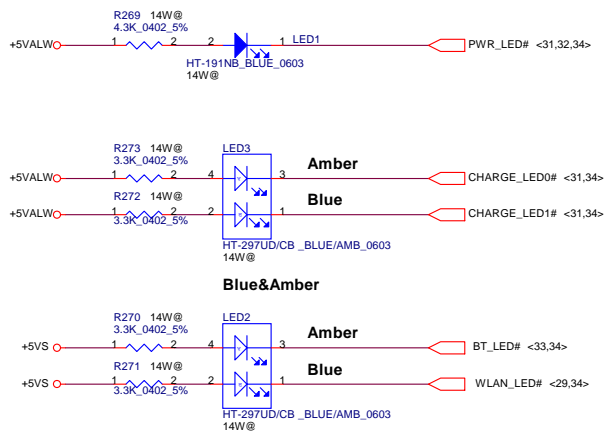
MDC Conn.



Camera Conn



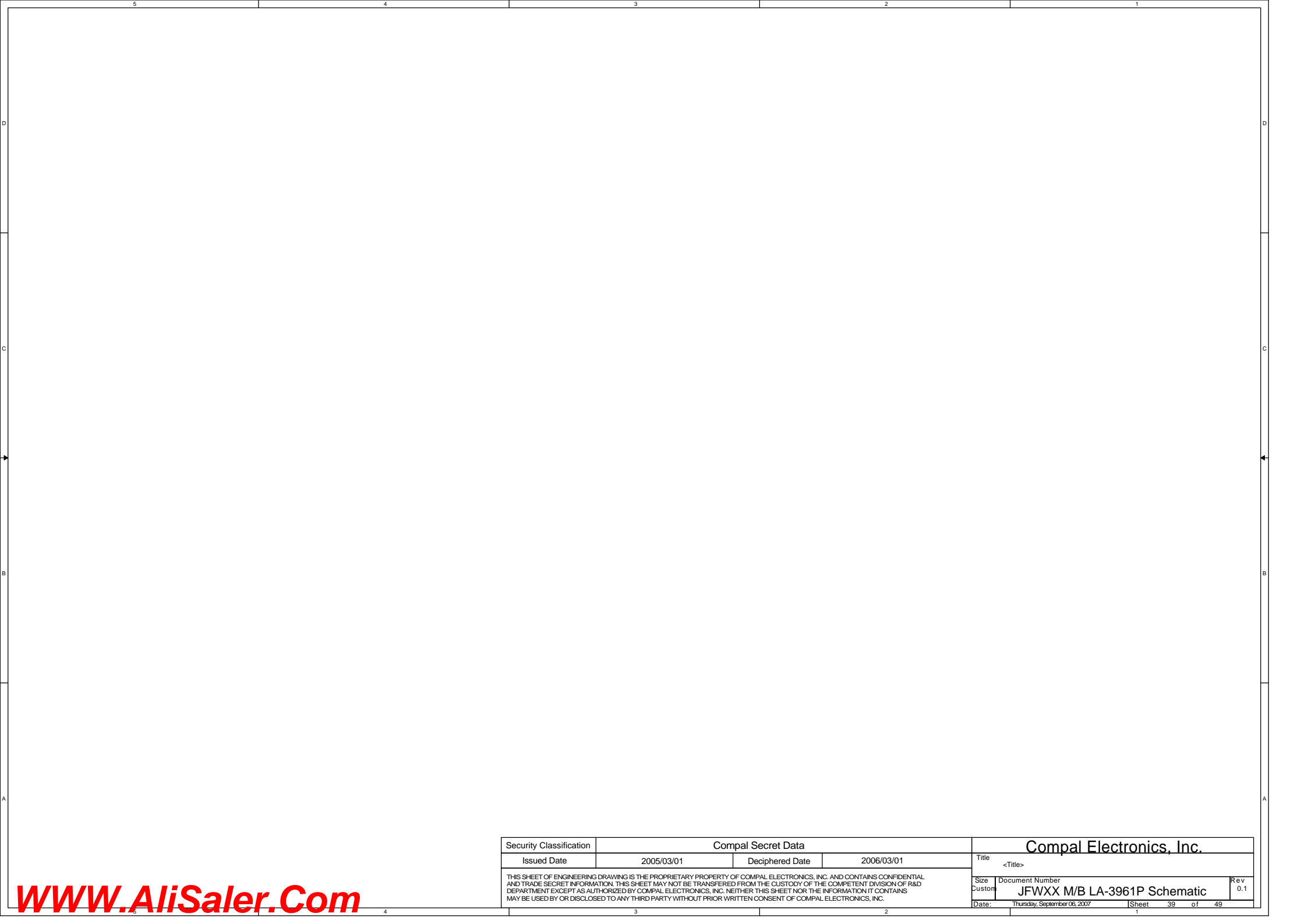
LED



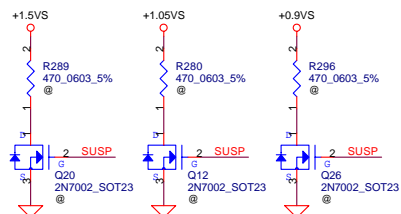
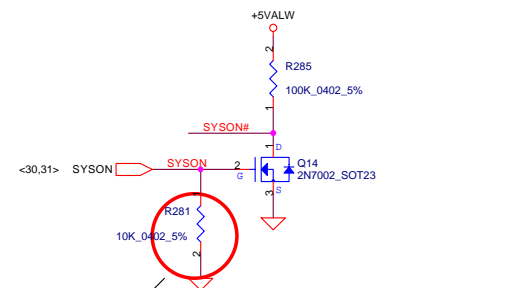
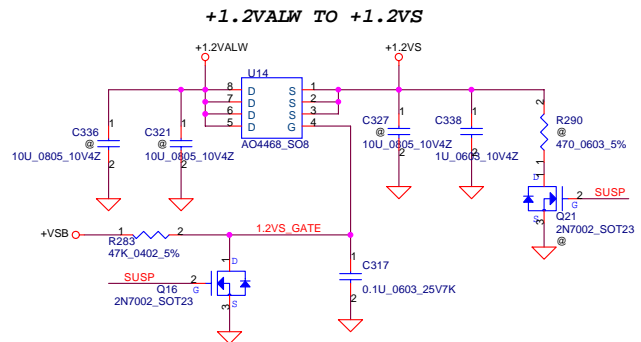
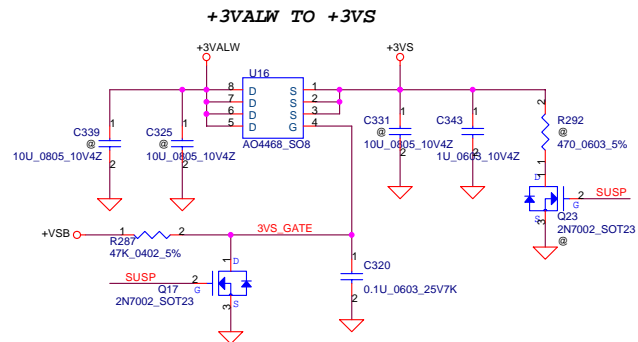
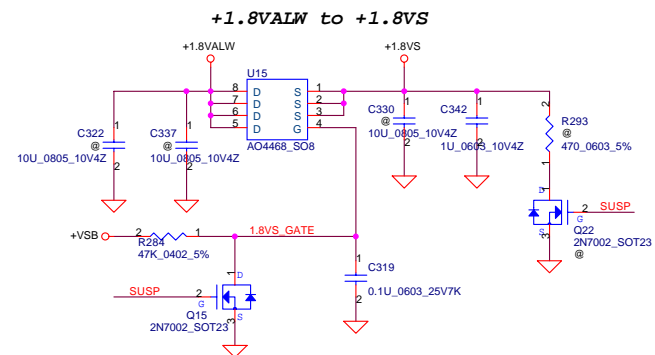
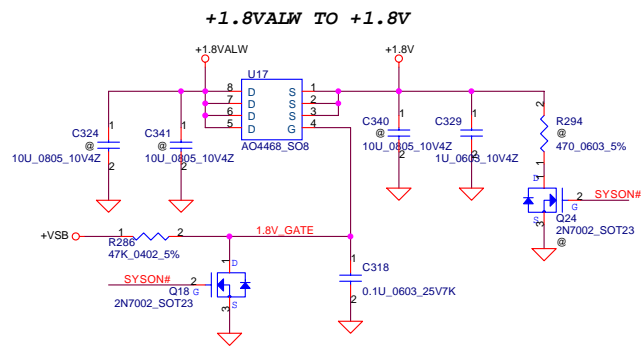
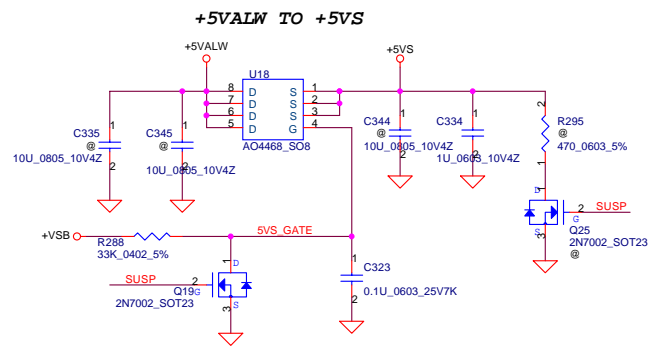
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										LED/MDC/CAMERA	
										JFWXX M/B LA-3961P Schematic	
										Rev 0.1	
										Date: Thursday, September 06, 2007	
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	JFWXX M/B LA-3961P Schematic			0.1	
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				Date: Thursday, September 06, 2007	Sheet 39 of 49
				Rev 0.1	

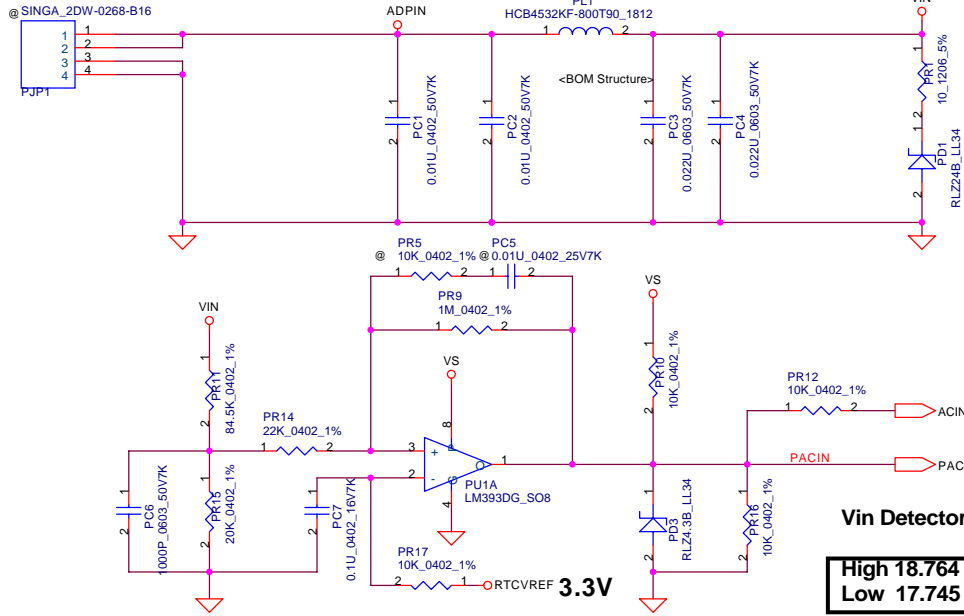


7/24 Change R281 from 100K to 10K

3/14 Change R16 from 100K to 10K

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				JFWXX M/B LA-3961P Schematic	
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DC301001Y00



Vin Detector

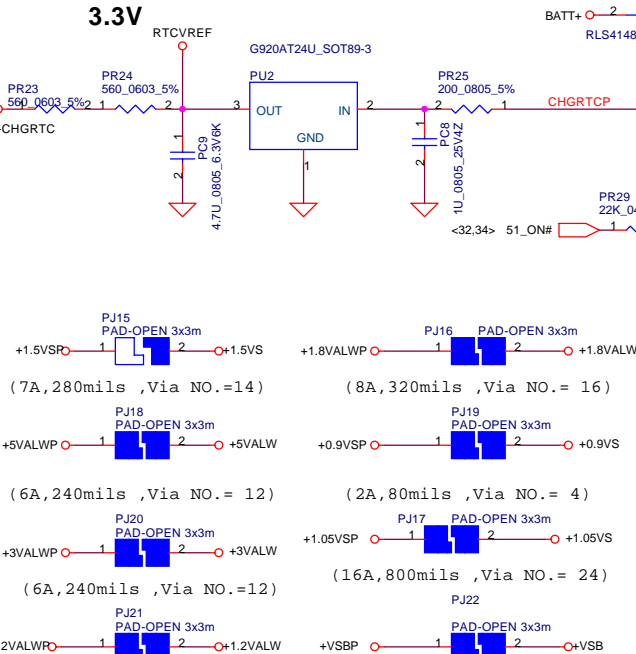
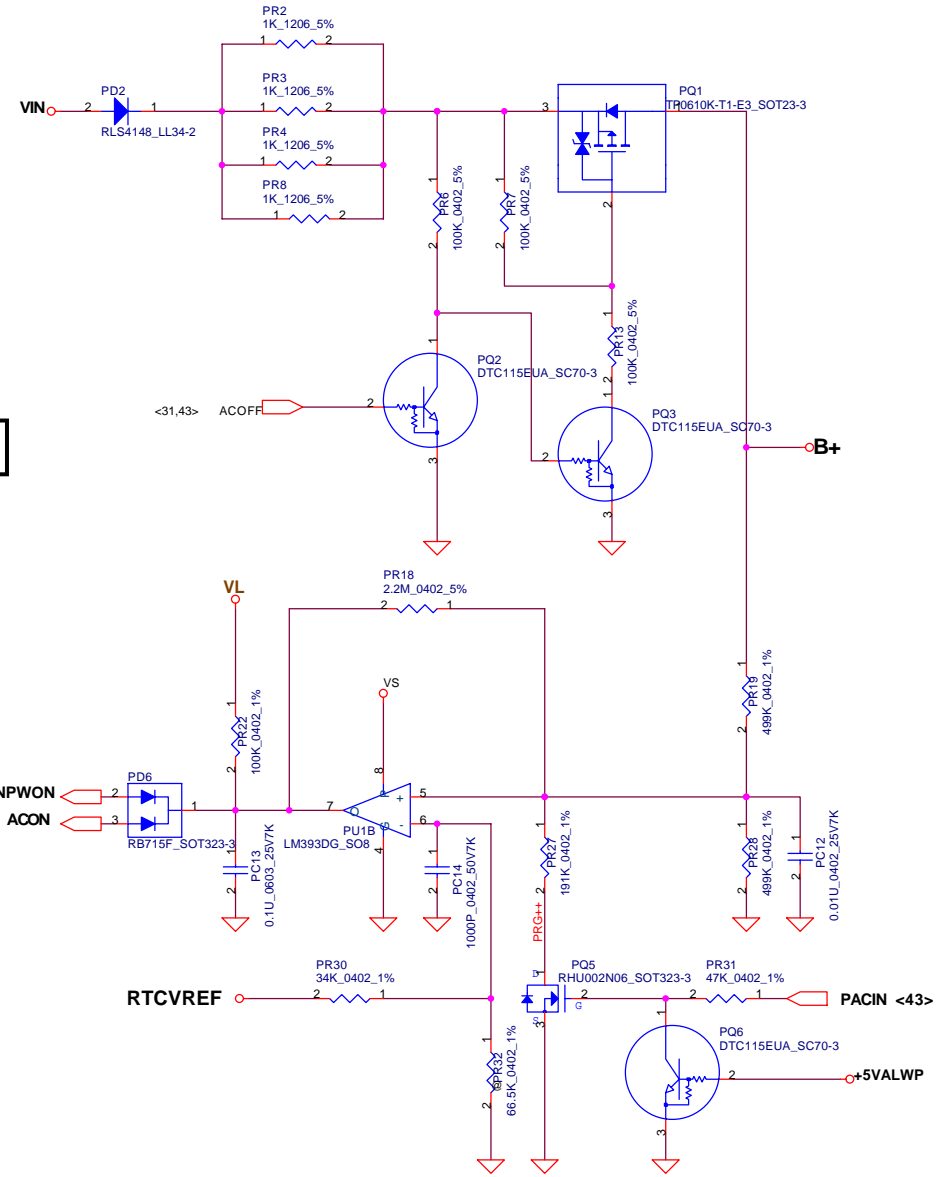
High	18.764	17.901	17.063
Low	17.745	16.9	16.03

ACIN

Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

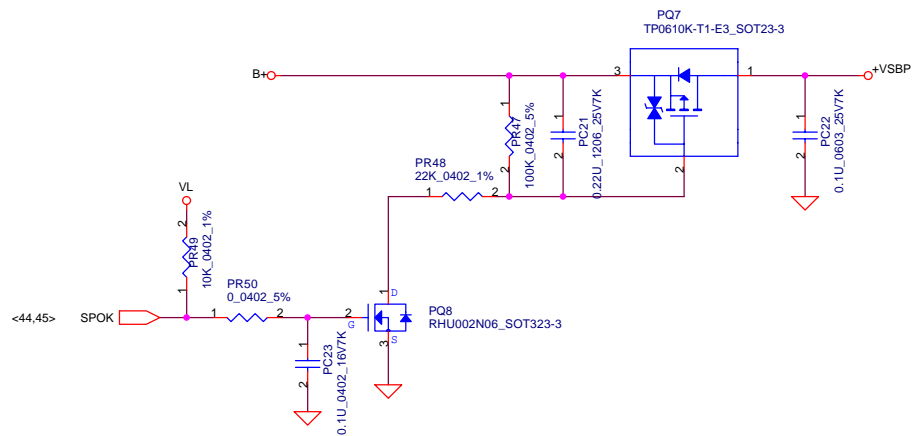
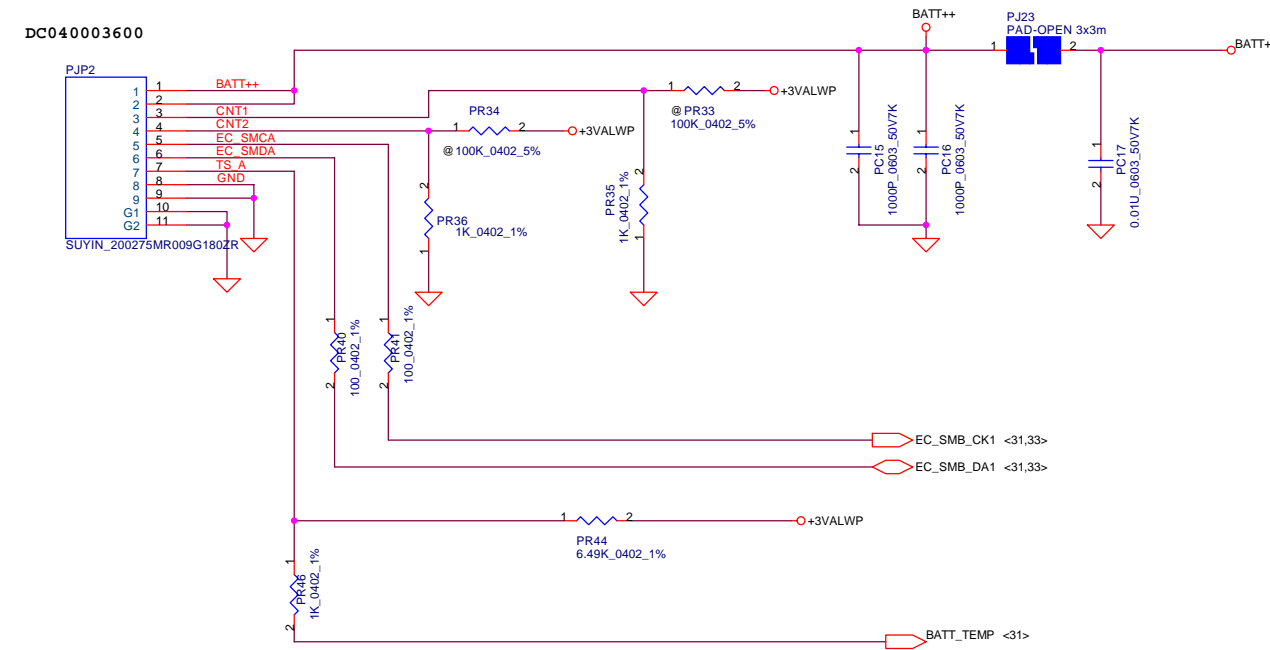
BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



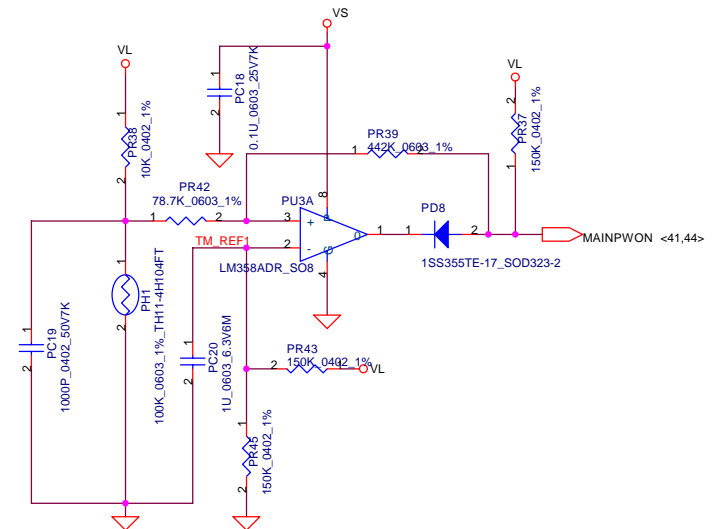
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DC040003600



2/16 Change to 89 degree C for thermal request

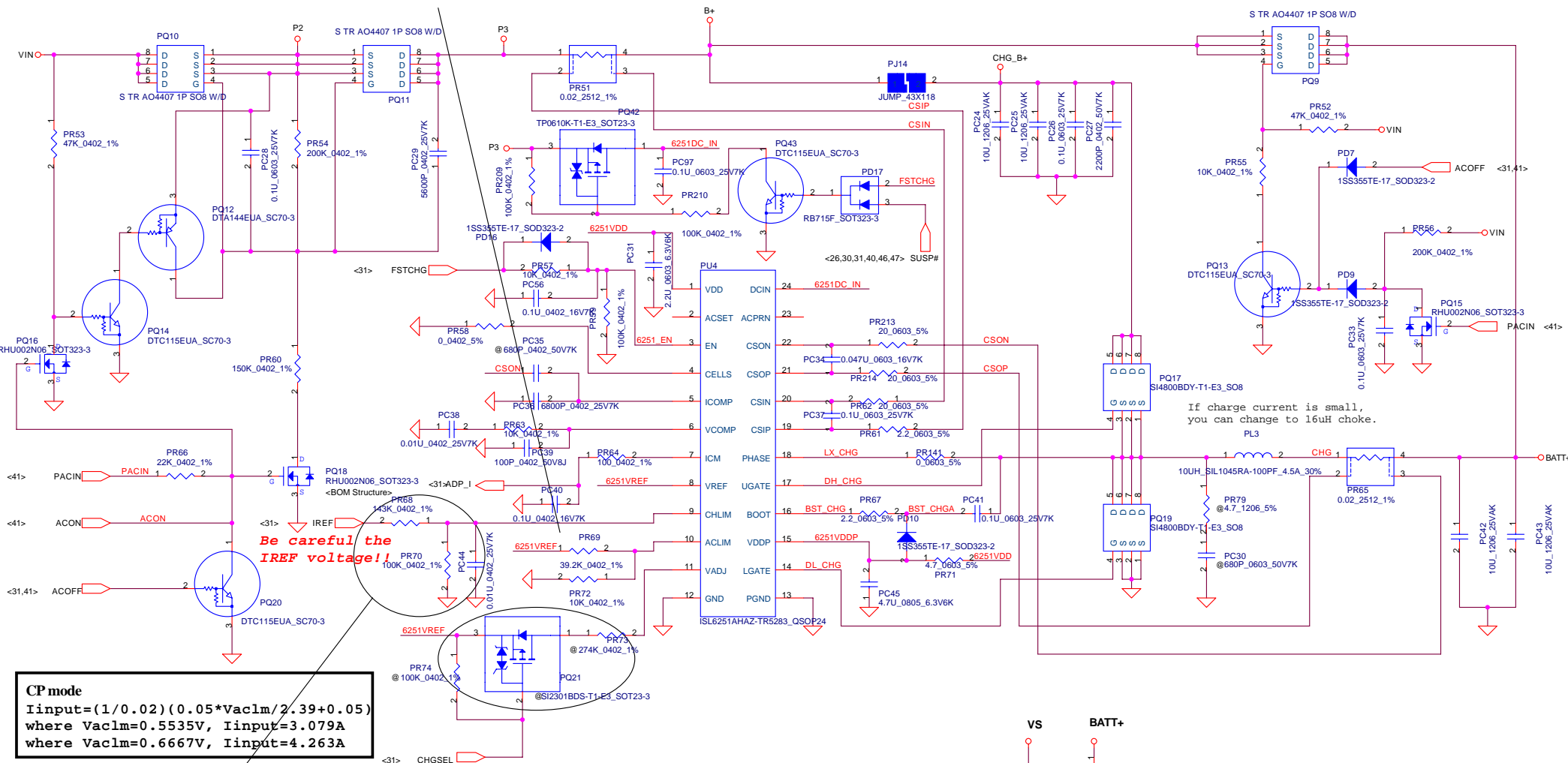
PH1 under CPU botten side :  
CPU thermal protection at 85 degree C  
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR74=39.2K, CP=3.079A

ADP\_I = 19.9\*Iadapter\*Rsense

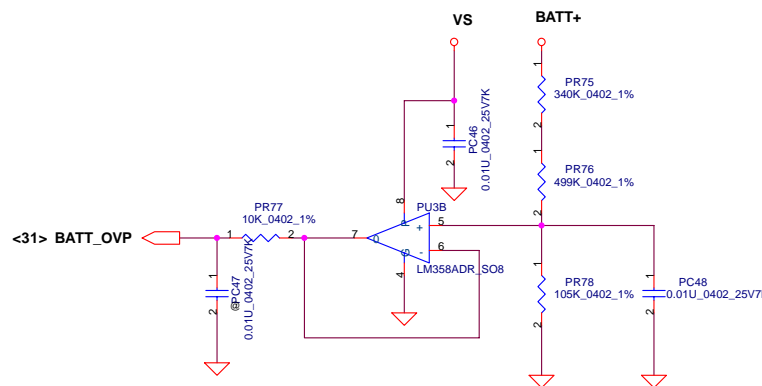


**CP mode**  
 $I_{input} = (1/0.02)(0.05 \cdot V_{ac1m}/2.39 + 0.05)$   
 where  $V_{ac1m} = 0.5535V$ ,  $I_{input} = 3.079A$   
 where  $V_{ac1m} = 0.6667V$ ,  $I_{input} = 4.263A$

**CC=0.6~3.4A**  
 $V_{CHLM} = 0.24V \sim 1.36V$   
 $I_{REF} = 0.972 \cdot I_{charge}$   
 $I_{REF} = 0.5832V \sim 3.3V$

If this area float, Charge voltage is 4.2V/cell

BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V



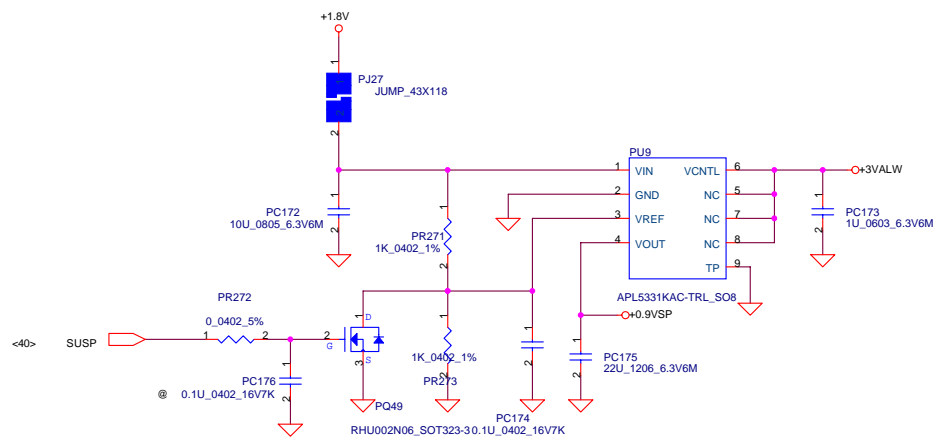
**OVP voltage :**  
 $LI-3S : 13.50V \sim BATT-OVP = 1.5V$   
 $BATT-OVP = 0.111 \cdot BATT+$

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