COMPAL CONFIDENTIAL

MODEL NAME : ***HDL75/76***

COMPAL P/N :

PCB NO :

Revision : ***0.1***

HDL75/76 Schematics Document

uFCBGA/uFCPGA Mobile Dothan
Intel Alviso + ICH6M

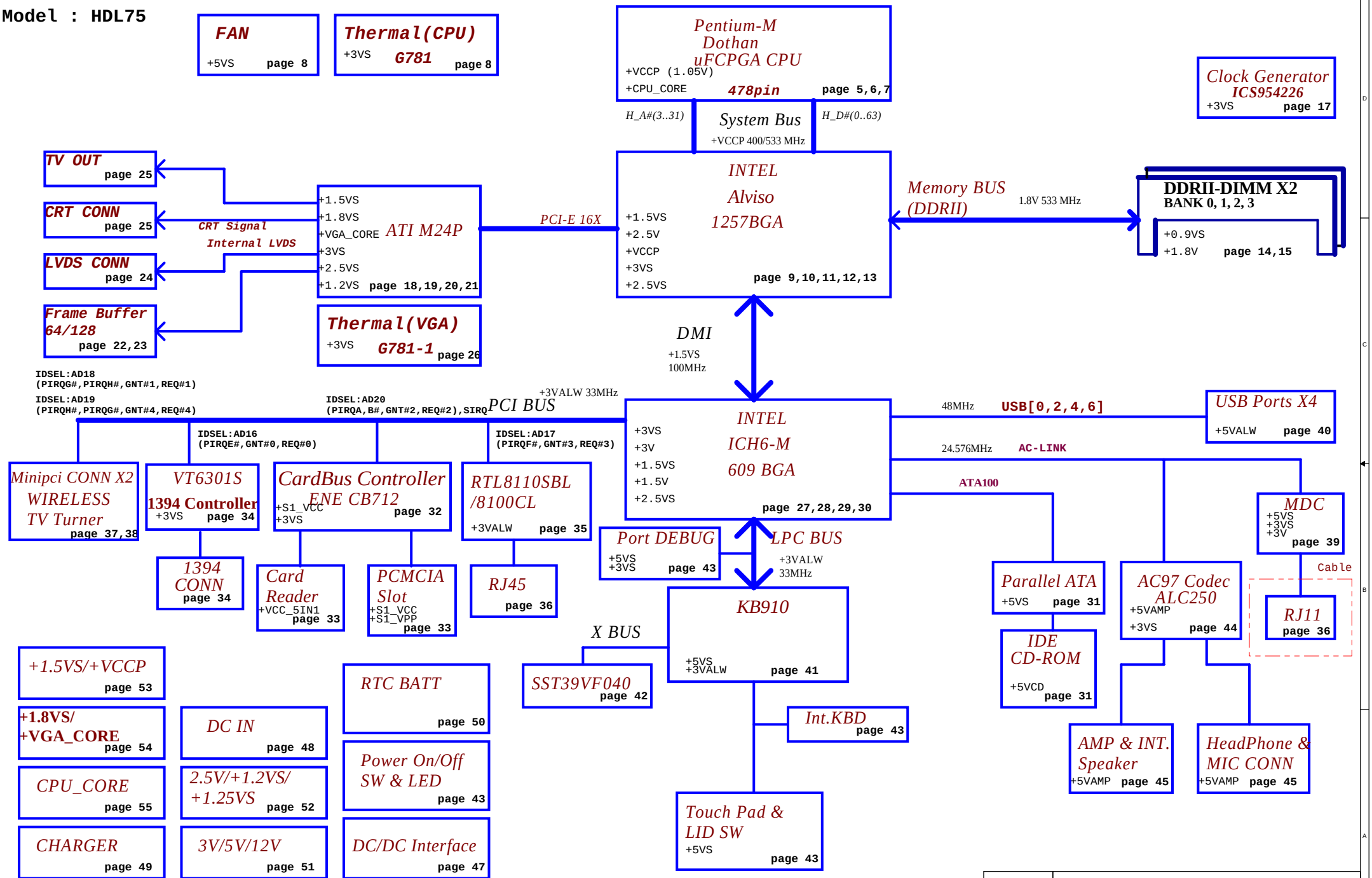
2005-07-14

REV : 1B

Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: HDL75 LA3041	Rev: 0.1
Date: Thursday, July 28, 2005	Sheet 1 of 60	

Compal confidential

Model : HDL75



Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: HDL75 LA3041 | Rev: 0.1

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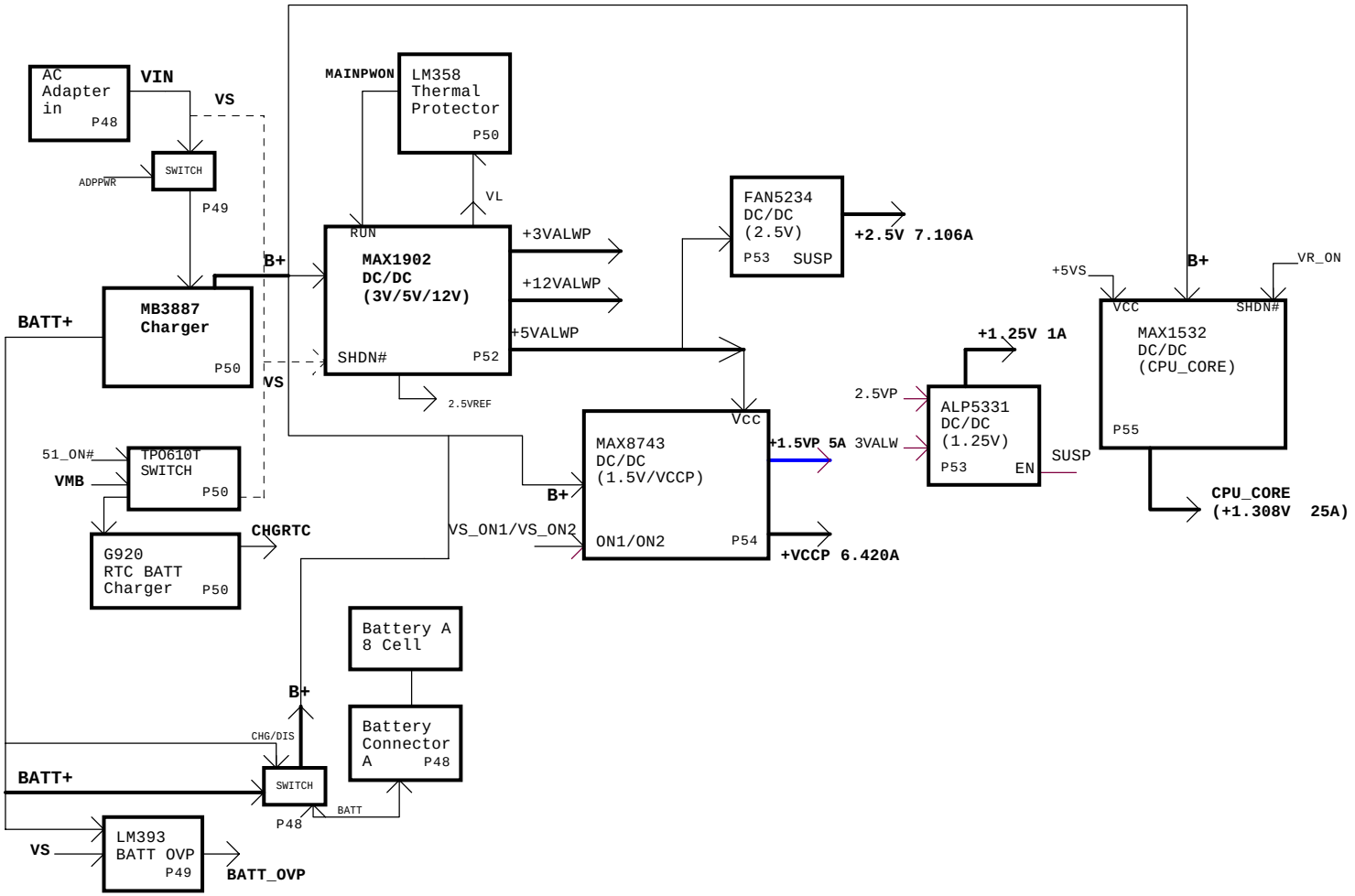

Compal Electronics, Inc.

Title: Power Rail

Size | Document Number: HDL75 LA3041 | Rev: 0.1

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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+PCIE_1.2VS	+PCIE_1.2VS power rail for VGA PCIExpress	ON	OFF	OFF
+0.9VS	0.9VS for DDR2 Termination	ON	OFF	OFF
+VGA_CORE	VGA Core Power	ON	OFF	OFF
+1.5VS	MCH & ICH Core Power	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5VS switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
1394	AD16	0	PIRQE
LAN	AD17	3	PIRQF
CardBus	AD20	2	PIRQA,B
Mini-PCI	AD18	1	PIRQG/PIRQH
Mini-PCI II for TV Turnner	AD19	4	PIRQH/PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
G781-1	1001 101X b

EC SM Bus2 address

Device	Address
G781	1001 100X b

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954206)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 001Xb

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	1.0
* 7	1.B

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	EDL71 SKU
* 0	EDL71 10/100 LAN WO/TV TUNER
1	EDL71 GIGA LAN W/TV TURNER
2	EDL71 10/100LAN W/TV TUNER
3	EDL71 GIGA WO/TV TUNER
4	EDL71 10/100 LAN WO/TV TUNER
5	EDL71 10/100LAN W/TV TUNER
6	EDL71 GIGA WO/TV TUNER
7	EDL71 GIGA LAN W/TV TURNER

NOTE1:

SWDJ@ : SWDJ
NOSWDJ@ : W/O SWDJ

@XX : Depop component
1@XX : Pop for Integrated Graphic
2@XX : Pop for External Graphic

TV@ : TV Tunner
100@ : 10/100M LAN
GIGA@ : 10/100M/1000M LAN

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Title: Notes List
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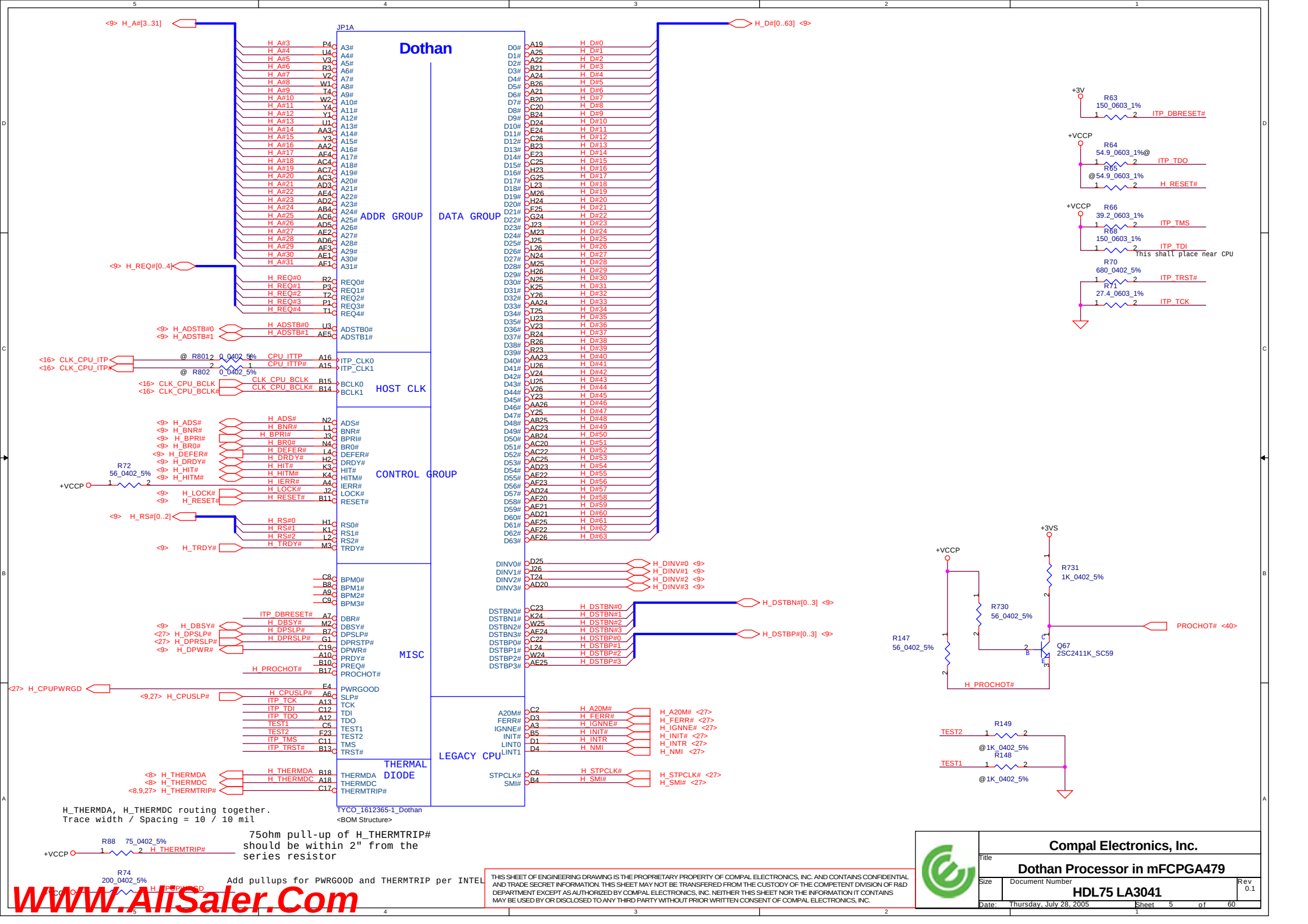

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Title: Dothan Processor in mFCPGA479

Size: | Document Number: HDL75 LA3041 | Rev: 0.1

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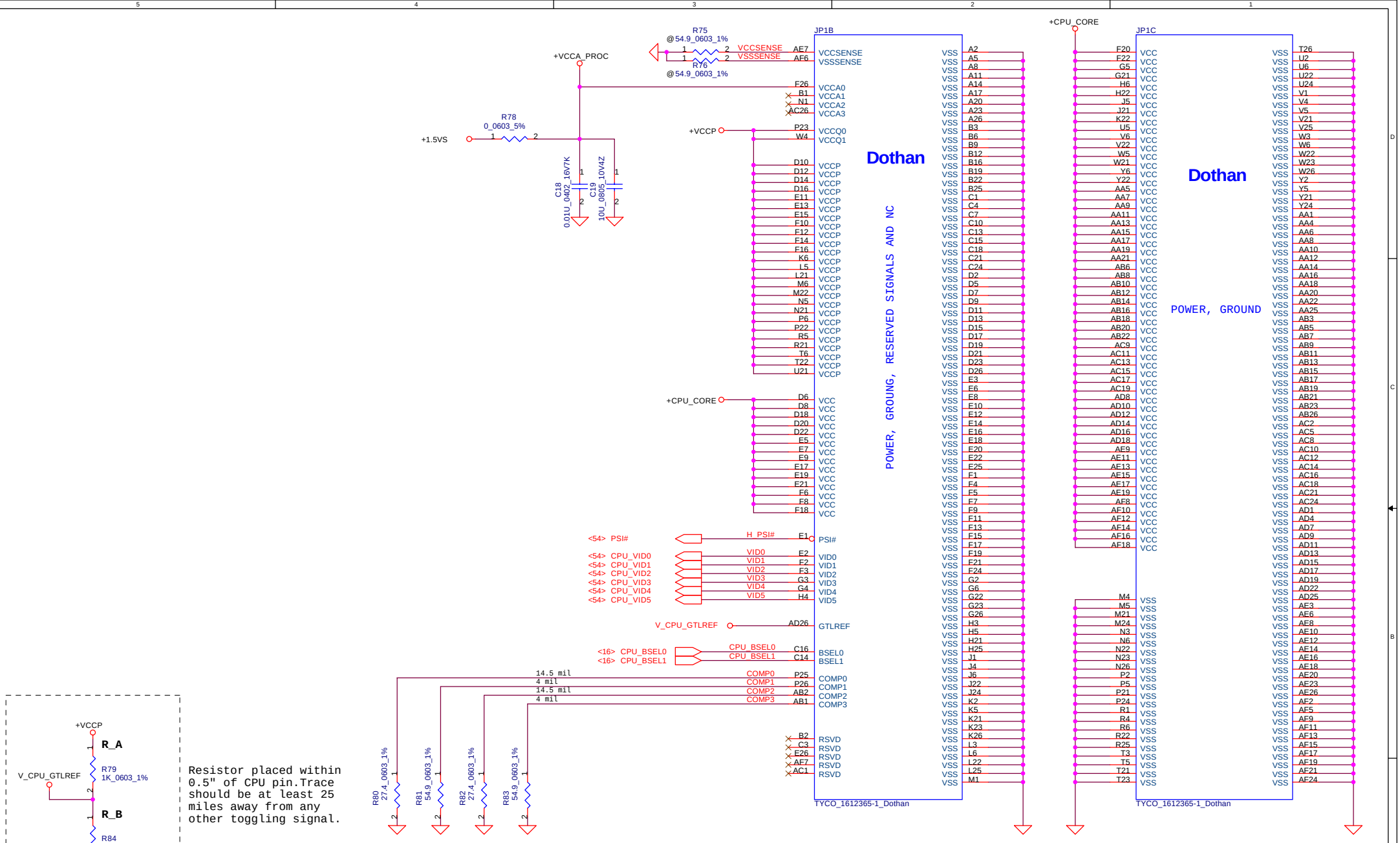

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Title: Dothan Processor in mFCPGA479
Size: Document Number: HDL75 LA3041
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Date: Thursday, July 28, 2005
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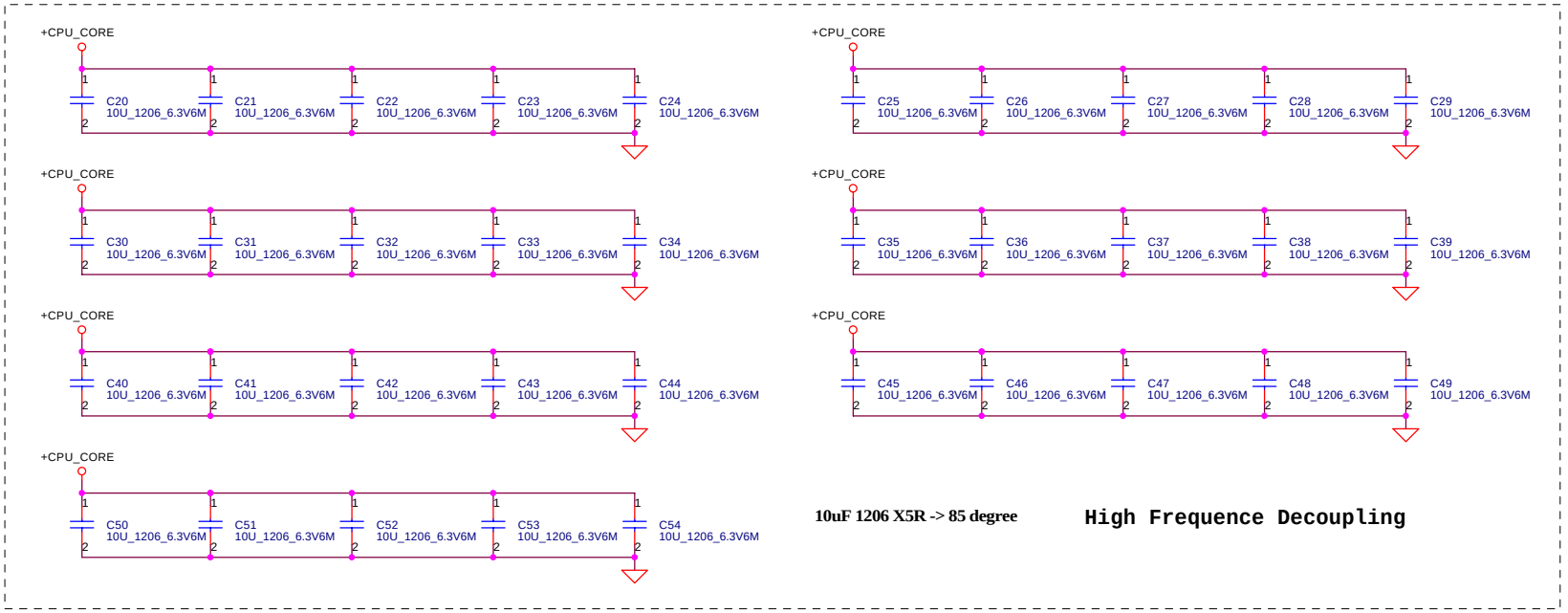
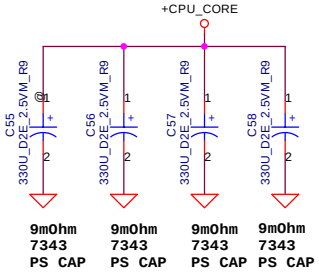
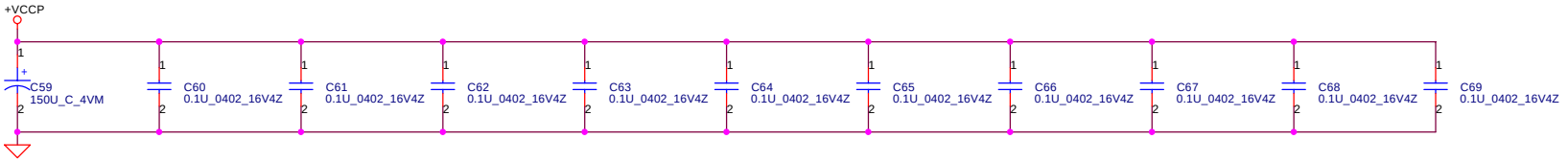


Near VCORE regulator.



ESR <= 3m ohm
Capacitor > 880uF



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Title: CPU Bypass

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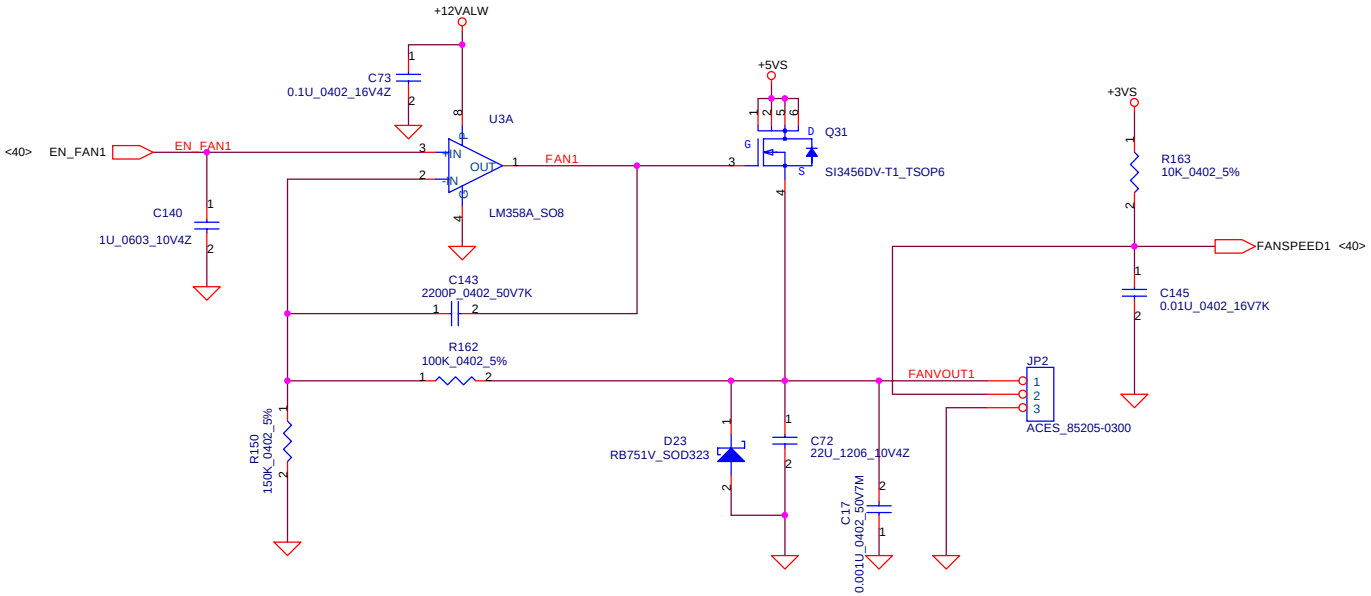
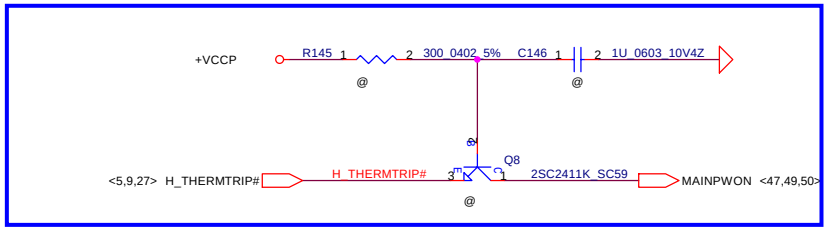
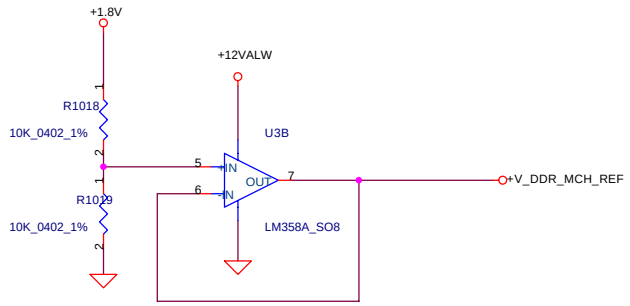
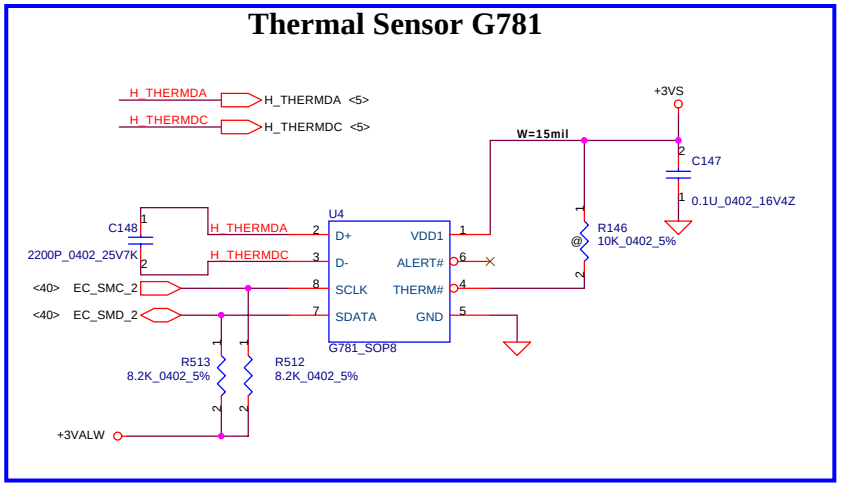
Fan Control circuit







Thermal Sensor G781



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Title: FAN & Thermal Sensor		
Size	Document Number: HDL75 LA3041	Rev: 0.1
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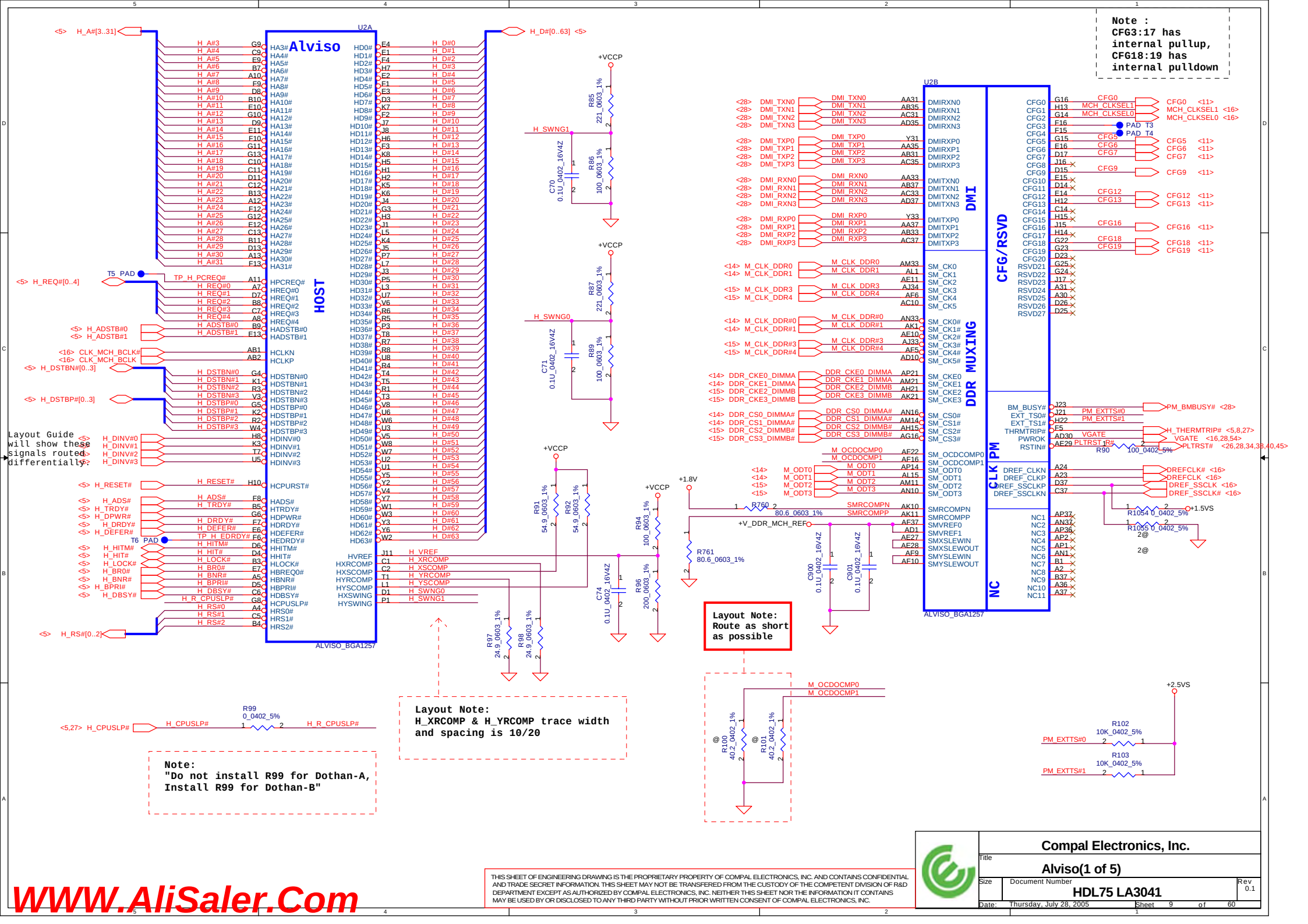
Note :
CFG3:17 has internal pullup,
CFG18:19 has internal pulldown
U2A
Alviso
HOST
ALVISO_BGA1257
U2B
DMI
DDR MUXING
CFG/RSVD
CLK PM
NC
Layout Guide will show these signals routed differentially.
Layout Note: Route as short as possible
Layout Note: H_XRCOMP & H_YRCOMP trace width and spacing is 10/20
Note: "Do not install R99 for Dothan-A, Install R99 for Dothan-B"
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Alviso(1 of 5)
HDL75 LA3041
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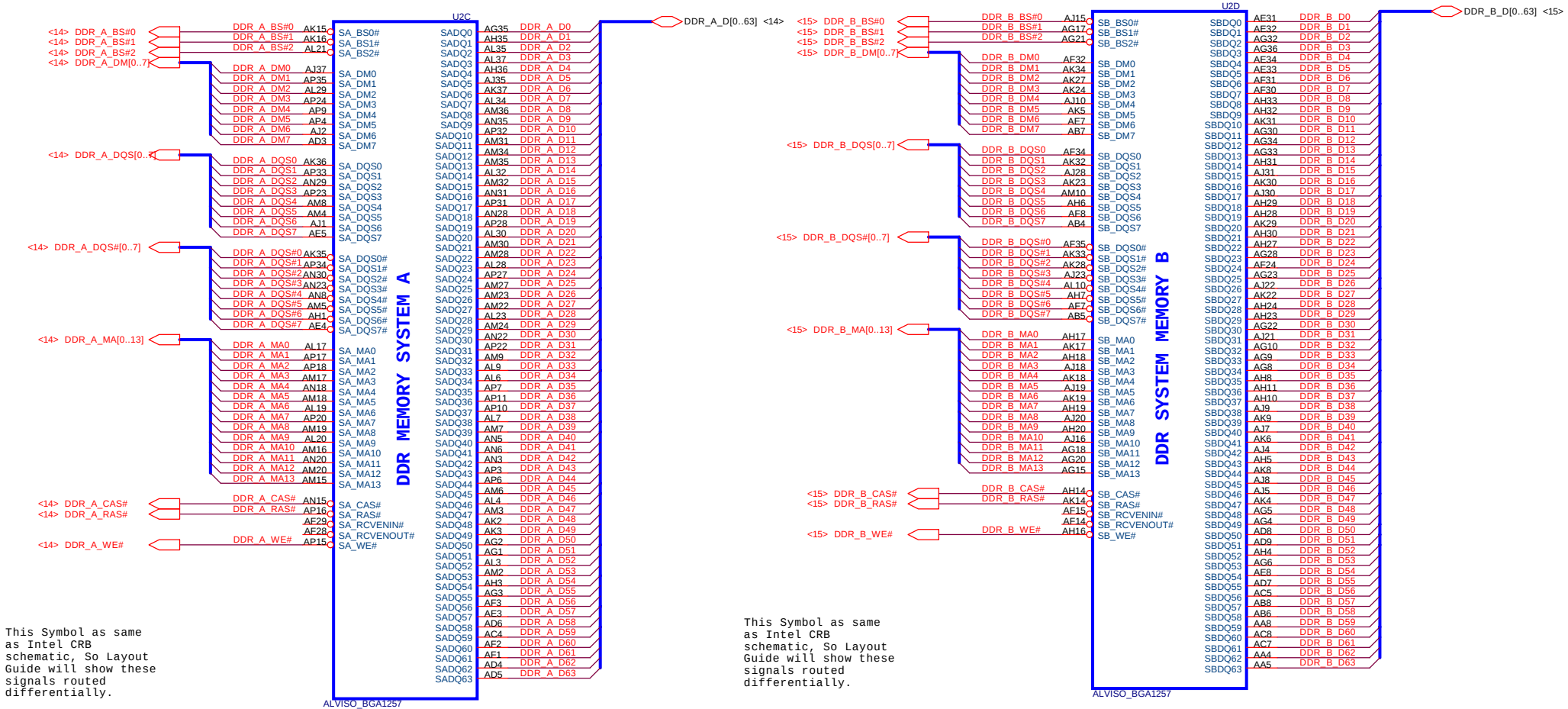

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Title: Alviso(2 of 5)

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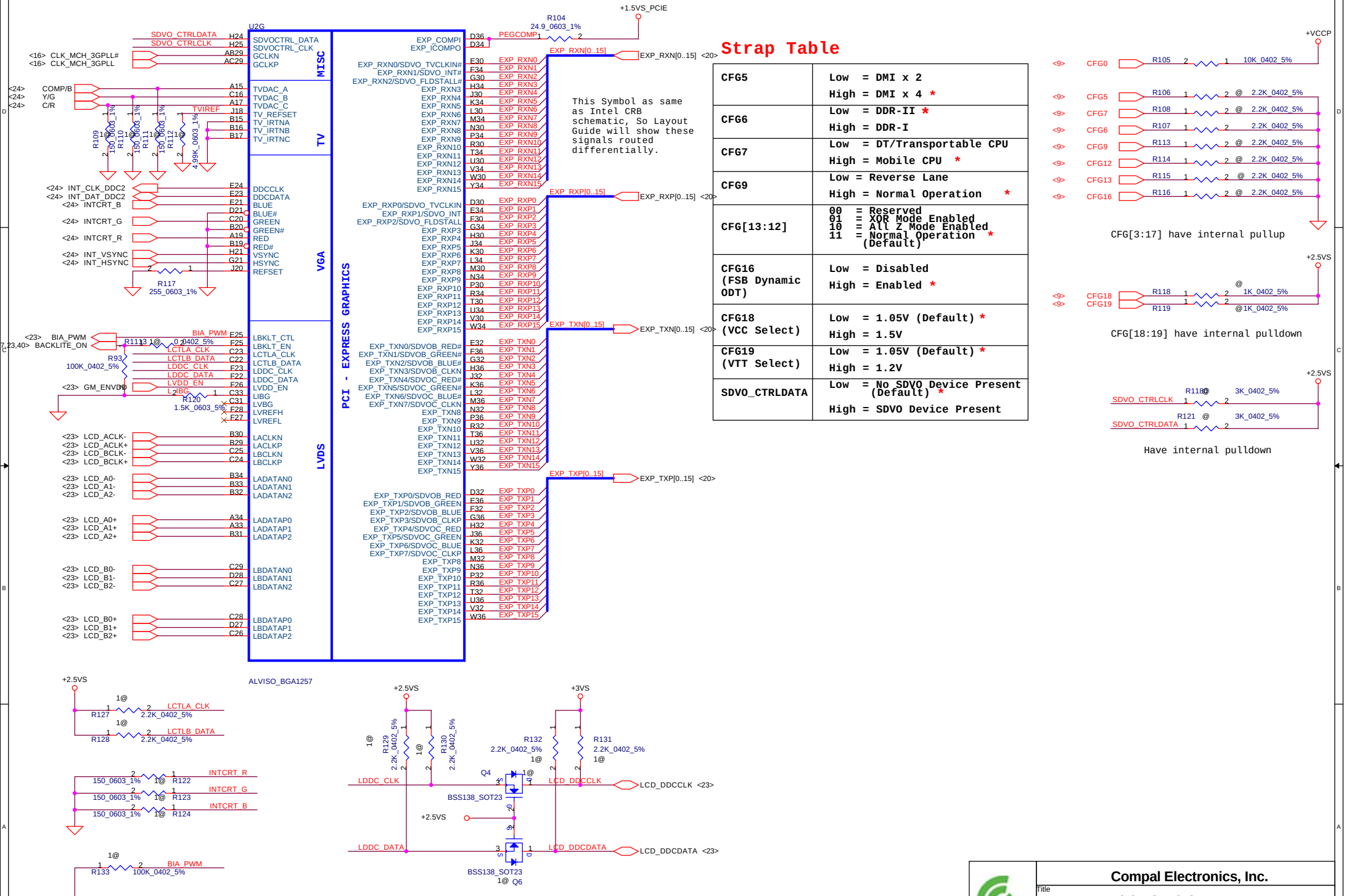

Strap Table

CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V
SDVO_CTRLDATA	Low = No SDVO Device Present (Default) * High = SDVO Device Present

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Title: Alviso(3 of 5)
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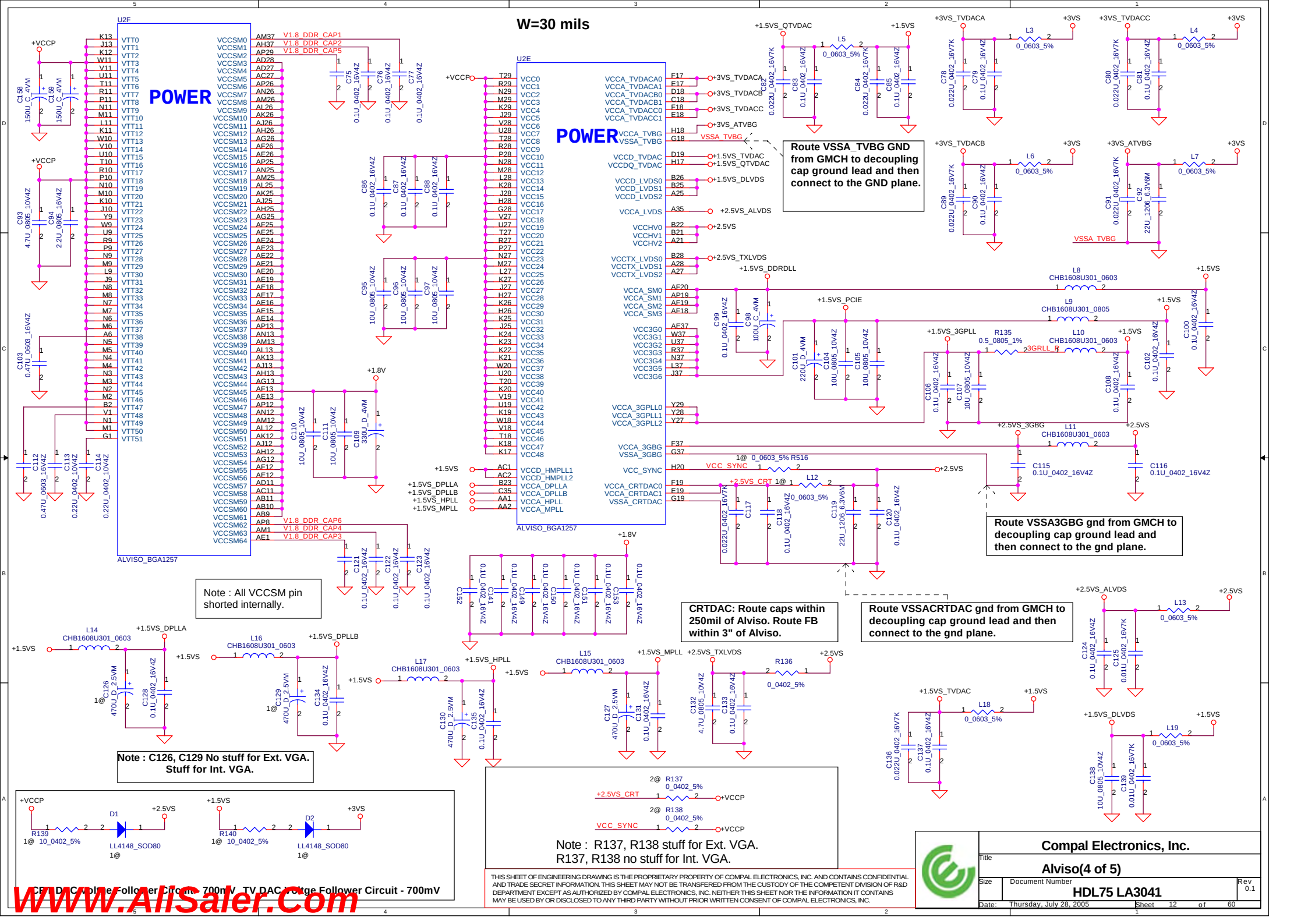
W=30 mils
U2F
POWER
ALVISO_BGA1257
U2E
POWER
ALVISO_BGA1257
Route VSSA_TVBG GND from GMCH to decoupling cap ground lead and then connect to the GND plane.
Route VSSA3GBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
Note : All VCCSM pin shorted internally.
CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
Note : C126, C129 No stuff for Ext. VGA. Stuff for Int. VGA.
Note : R137, R138 stuff for Ext. VGA. R137, R138 no stuff for Int. VGA.
CRT DAC Voltage Follower Circuit - 700mV TV DAC Voltage Follower Circuit - 700mV
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Title
Alviso(4 of 5)
Size
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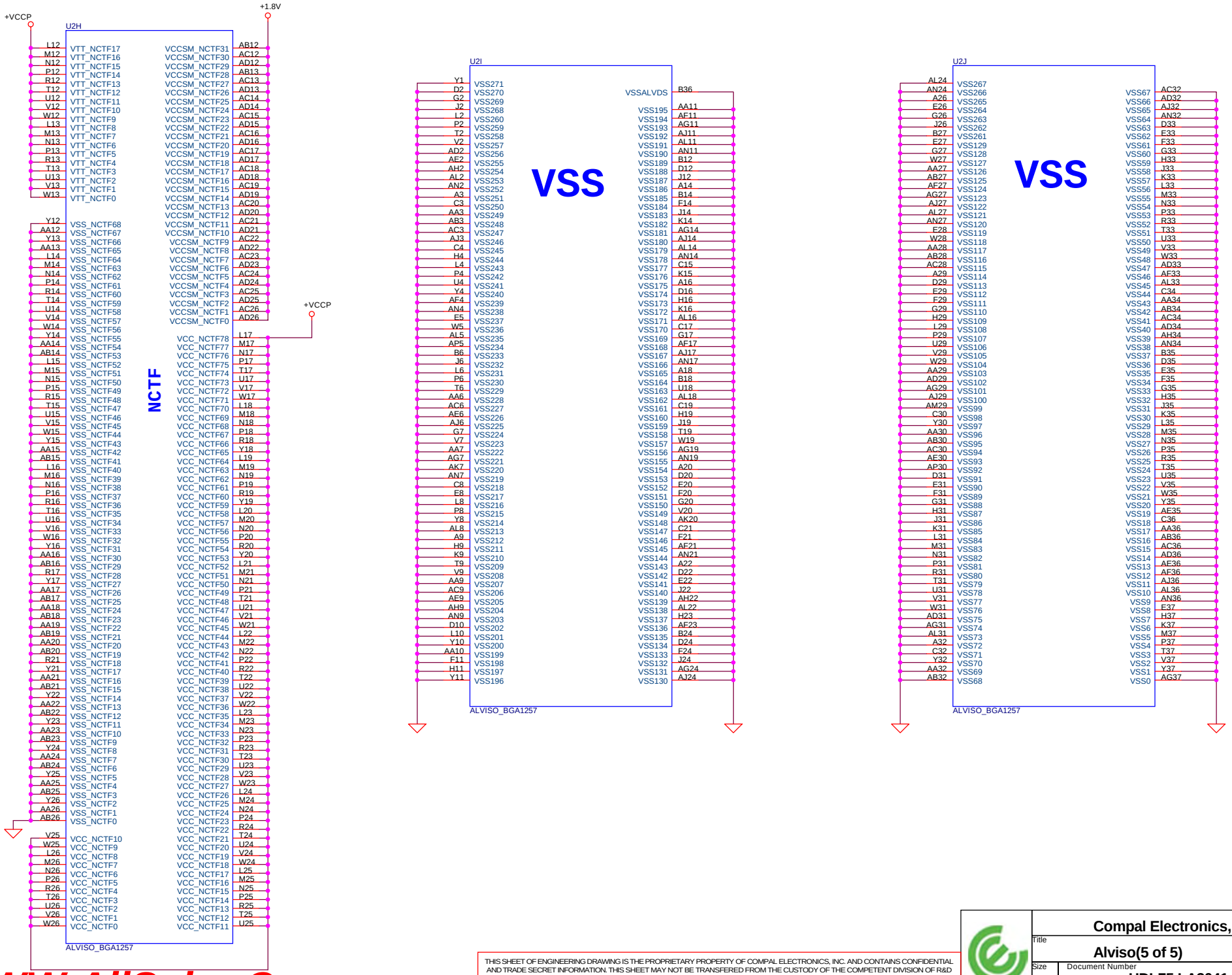

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Title: Alviso(5 of 5)

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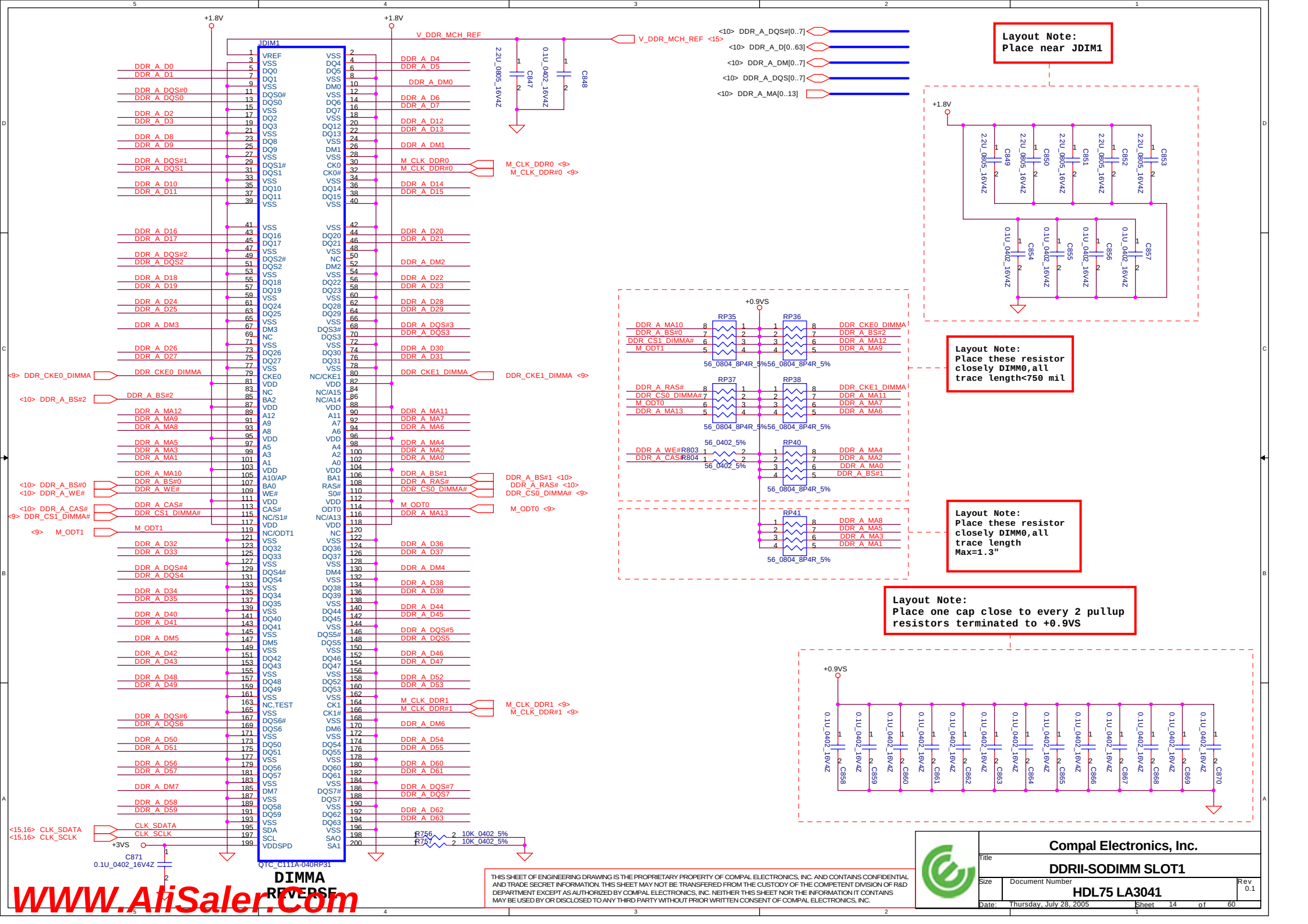

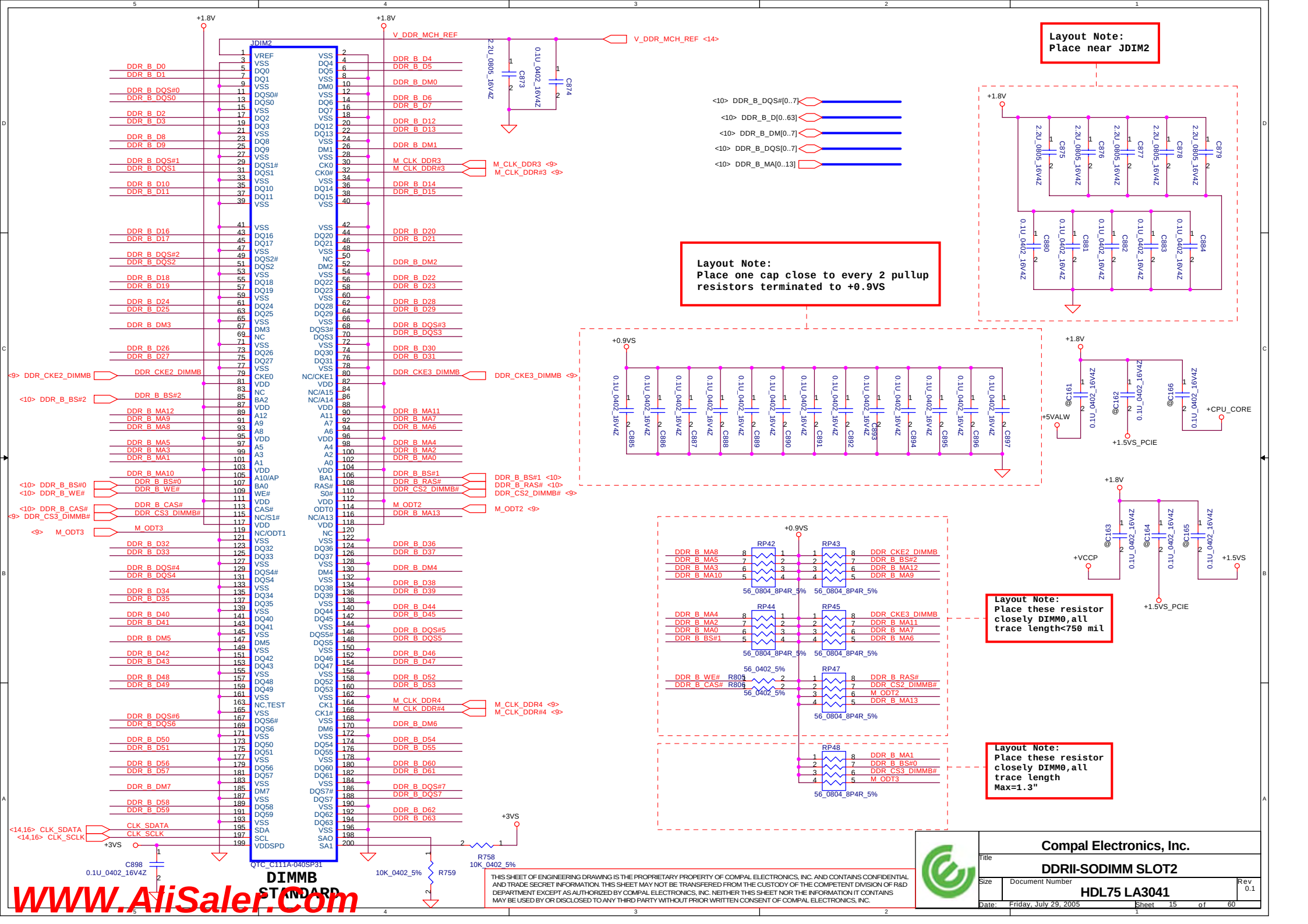

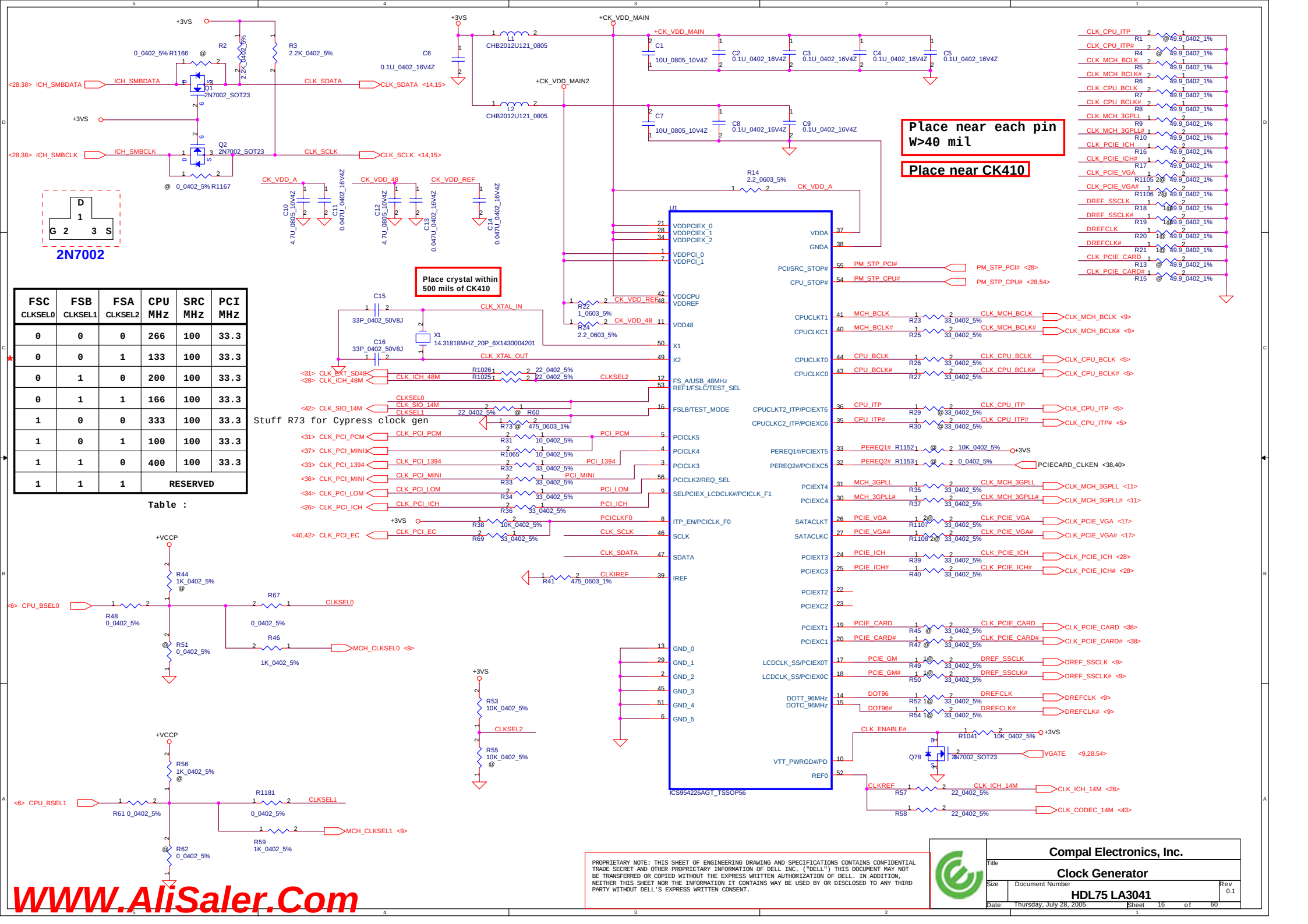

FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	RESERVED		

Compal Electronics, Inc.

Title: Clock Generator

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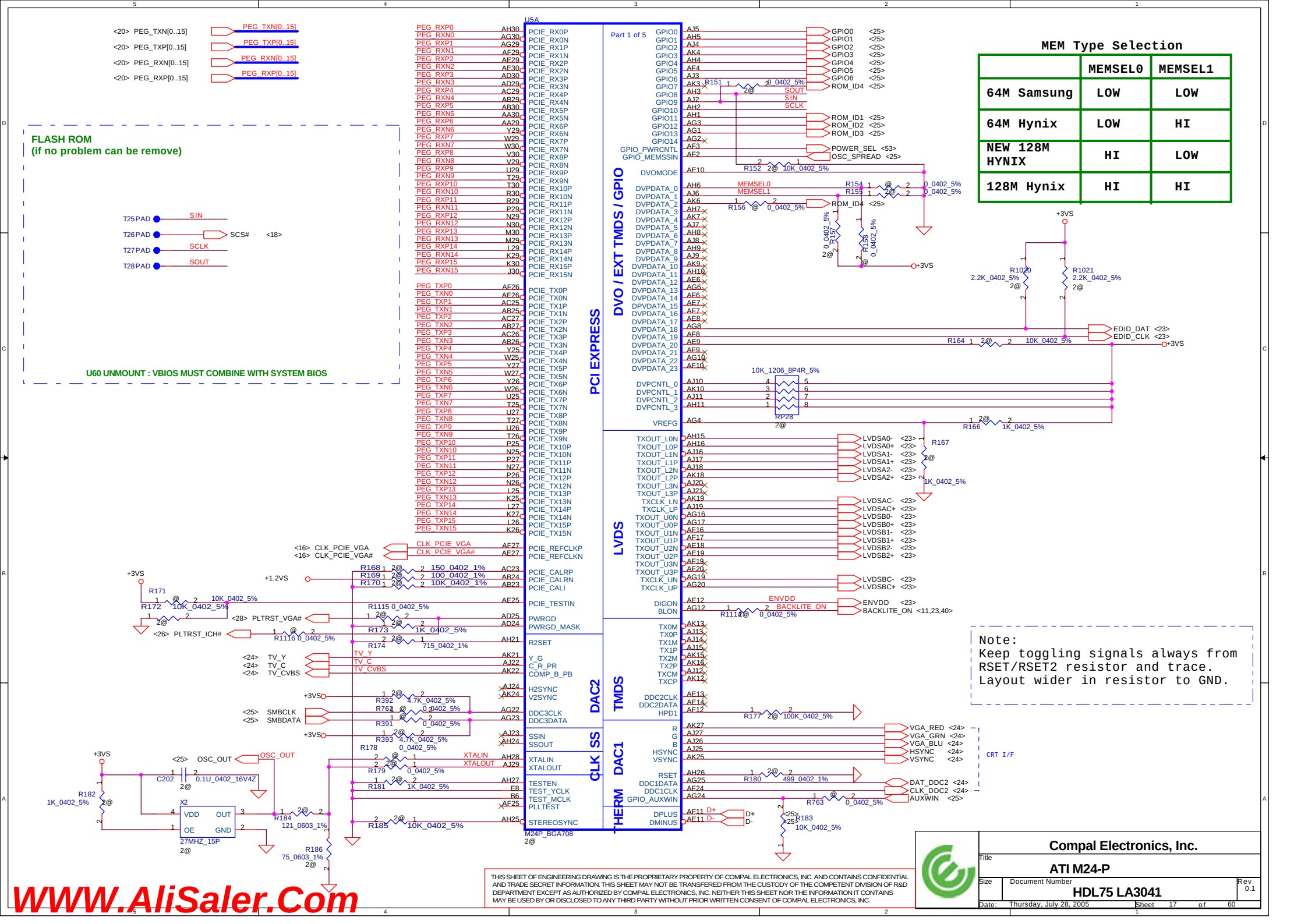


	MEMSEL0	MEMSEL1
64M Samsung	LOW	LOW
64M Hynix	LOW	HI
NEW 128M HYNIX	HI	LOW
128M Hynix	HI	HI

MDA[63:0] <21>

MAA[13:0] <21>

DQSA[7:0] <21>

DQMA#[7:0] <21>

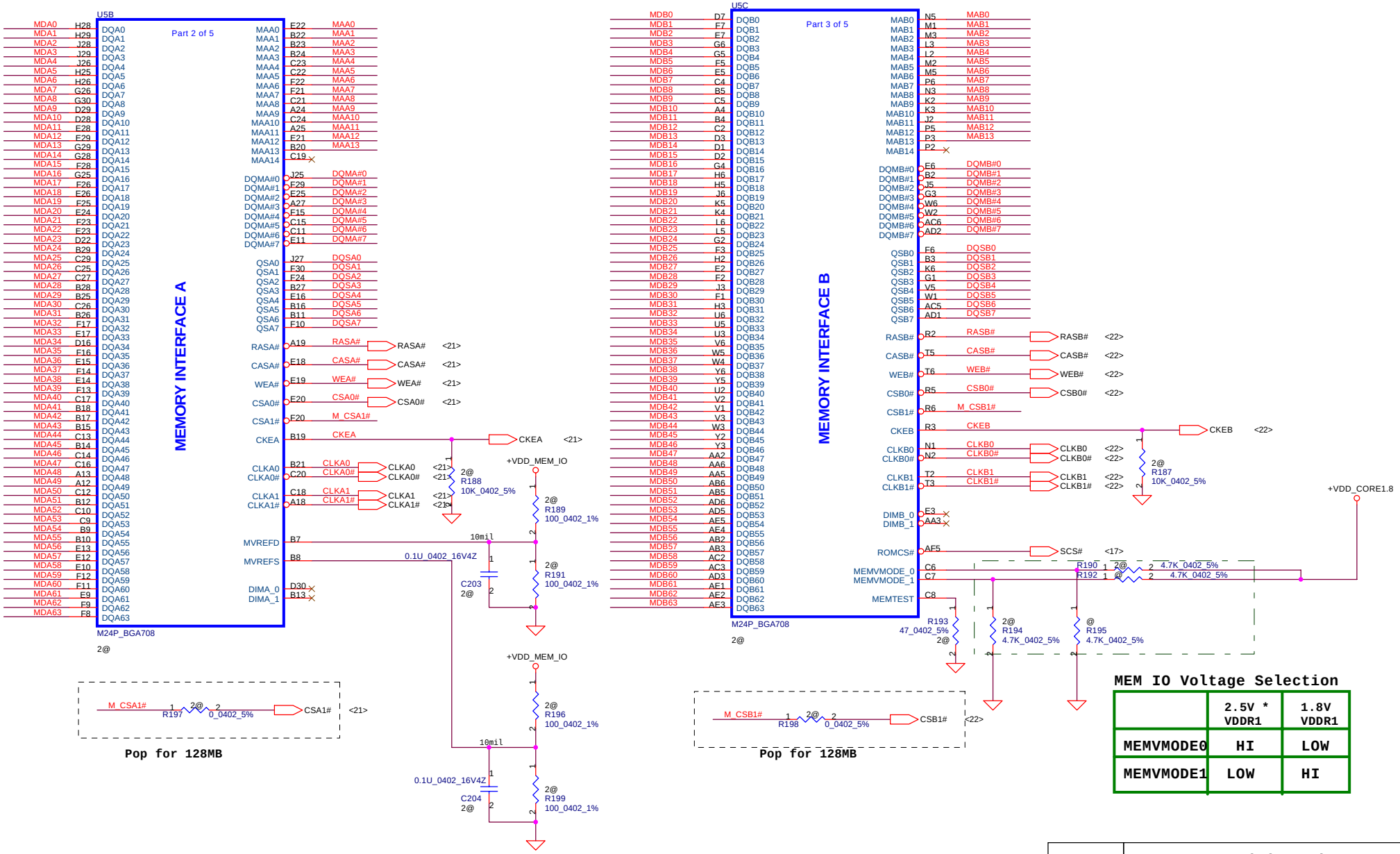
MDB[63:0] <22>

MAB[13:0] <22>

DQSB[7:0] <22>

DQMB#[7:0] <22>

NOTE :Elpida Memory Data Groups Swapping Possibilities-- Shaded group belonging to QS1 and QS5 can't be swapped with other groups (MD15:8) & (MD47:40)



MEM IO Voltage Selection

	2.5V * VDDR1	1.8V VDDR1
MEMVMODE0	HI	LOW
MEMVMODE1	LOW	HI

Compal Electronics, Inc.
Title: ATI M24P MEM_Interface
Size: Document Number: HDL75 LA3041 Rev: 0.1
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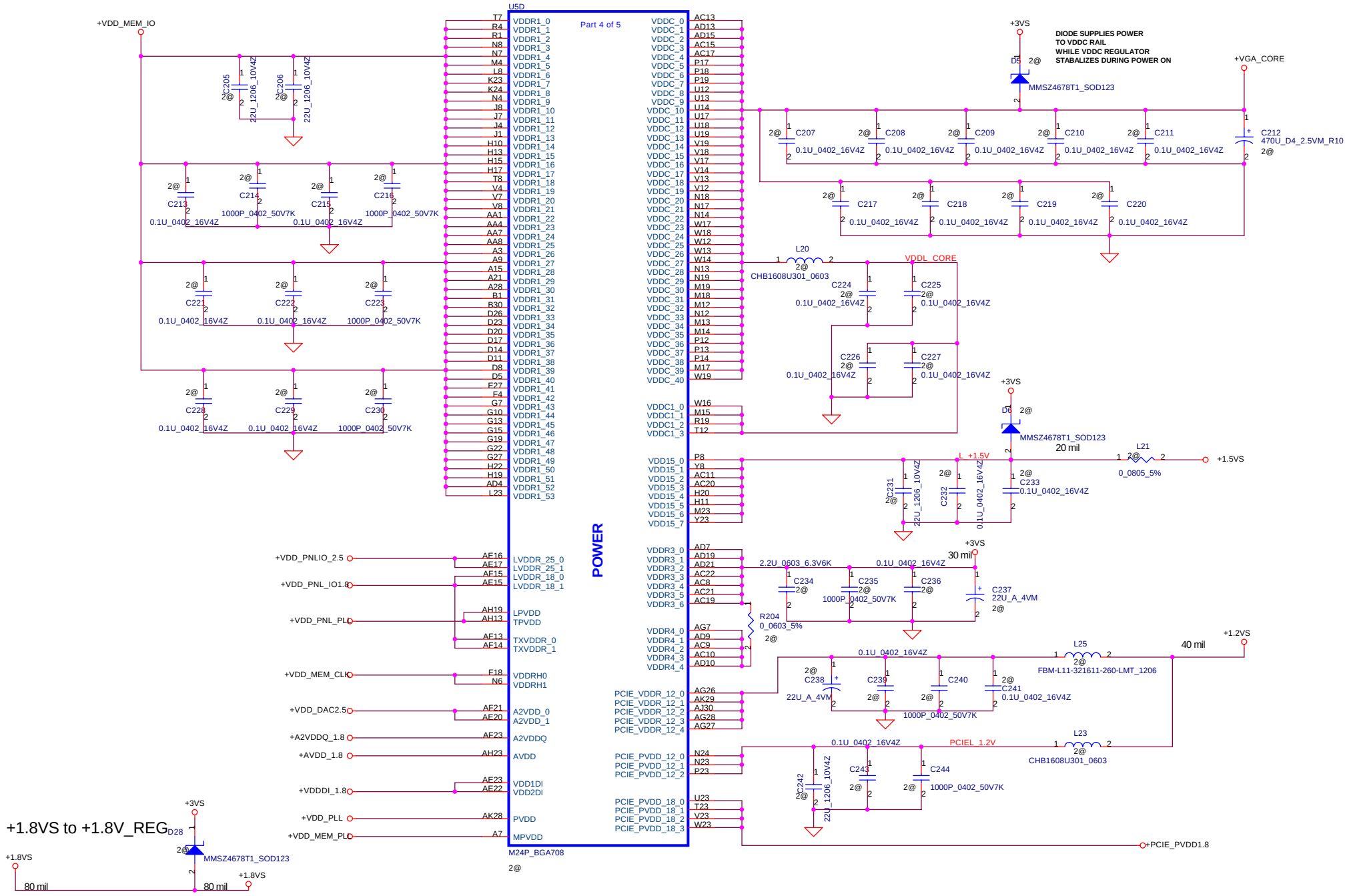

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Title: ATI M24P I/O PWR(1/2)

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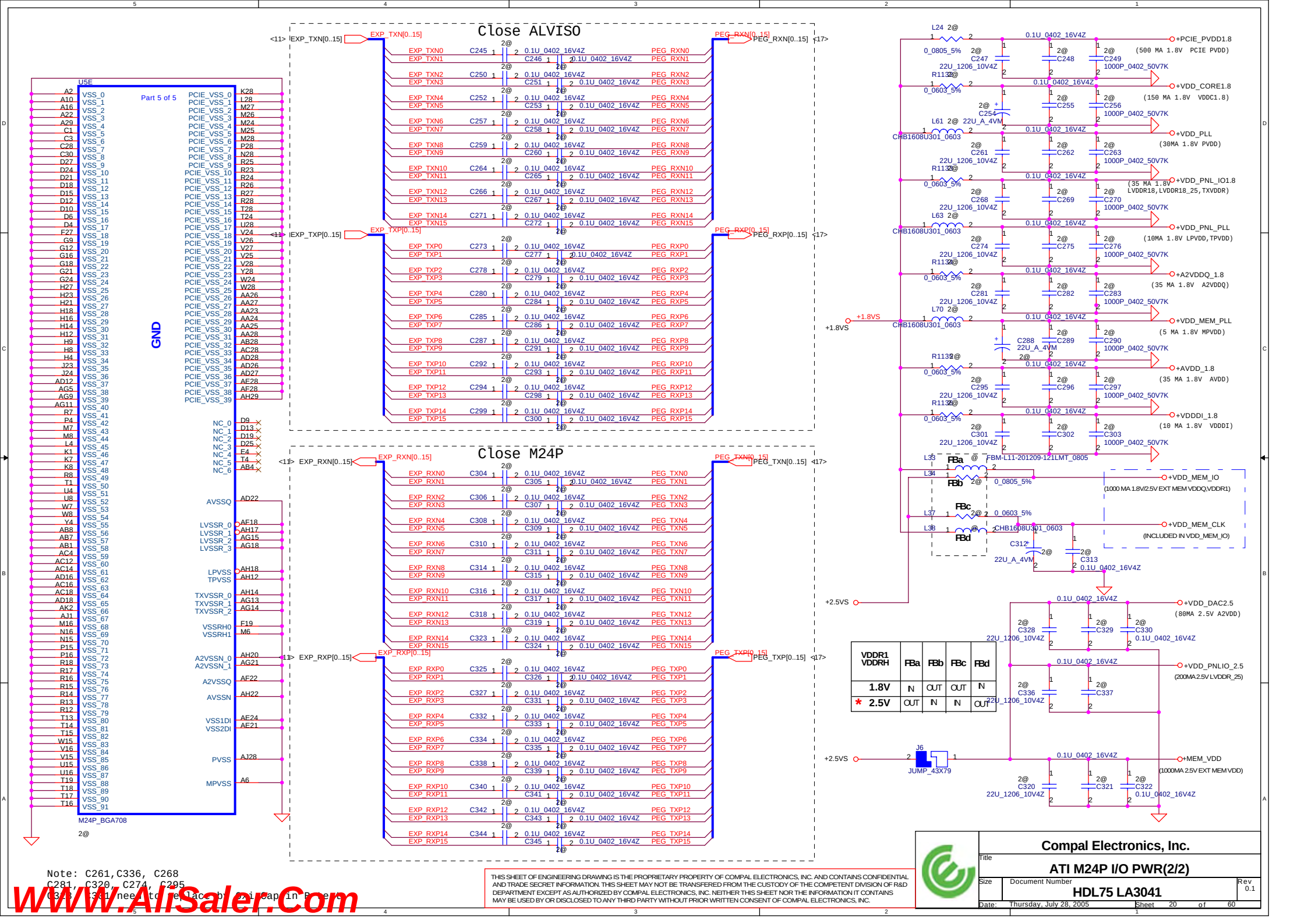

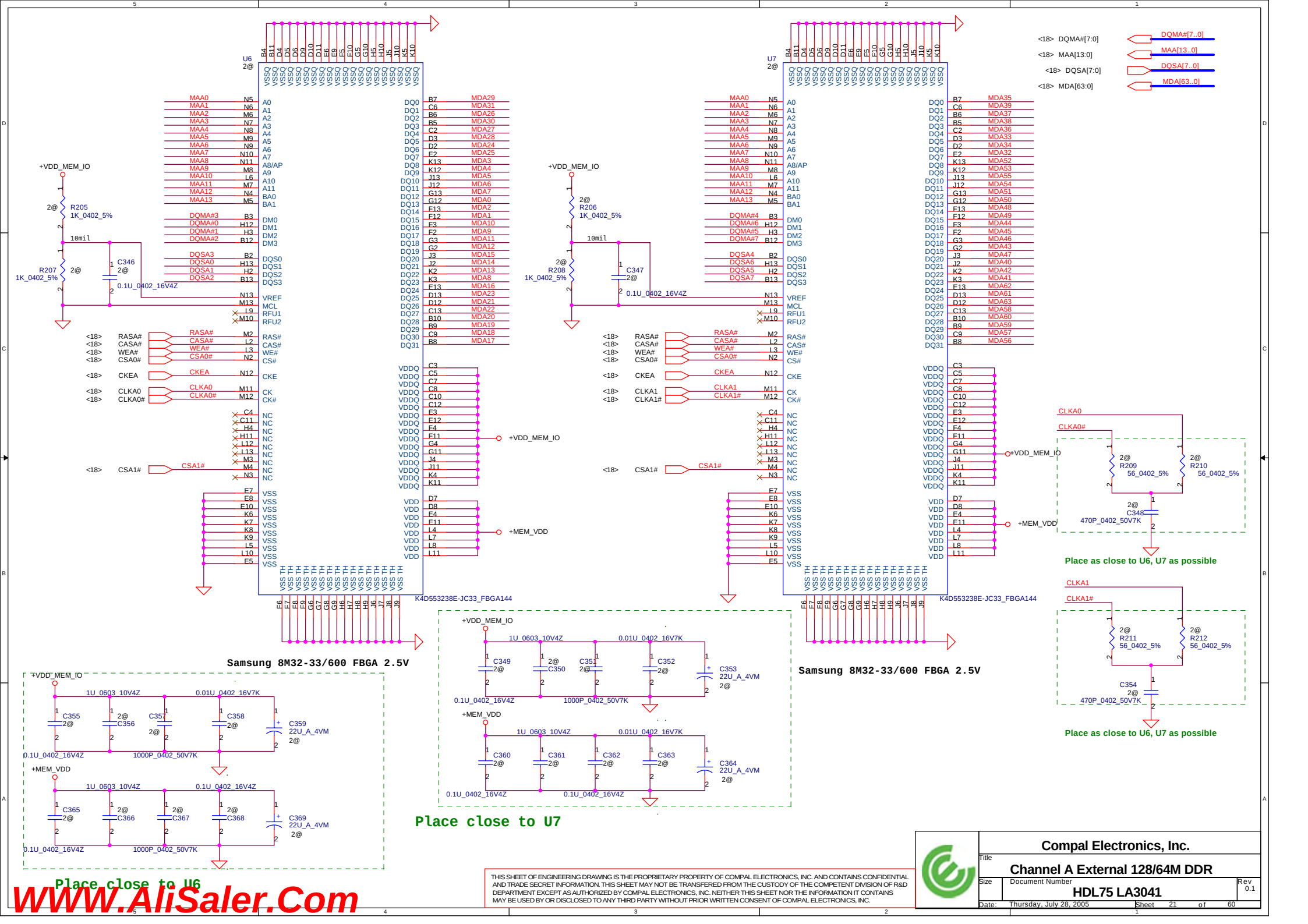

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Title: Channel A External 128/64M DDR

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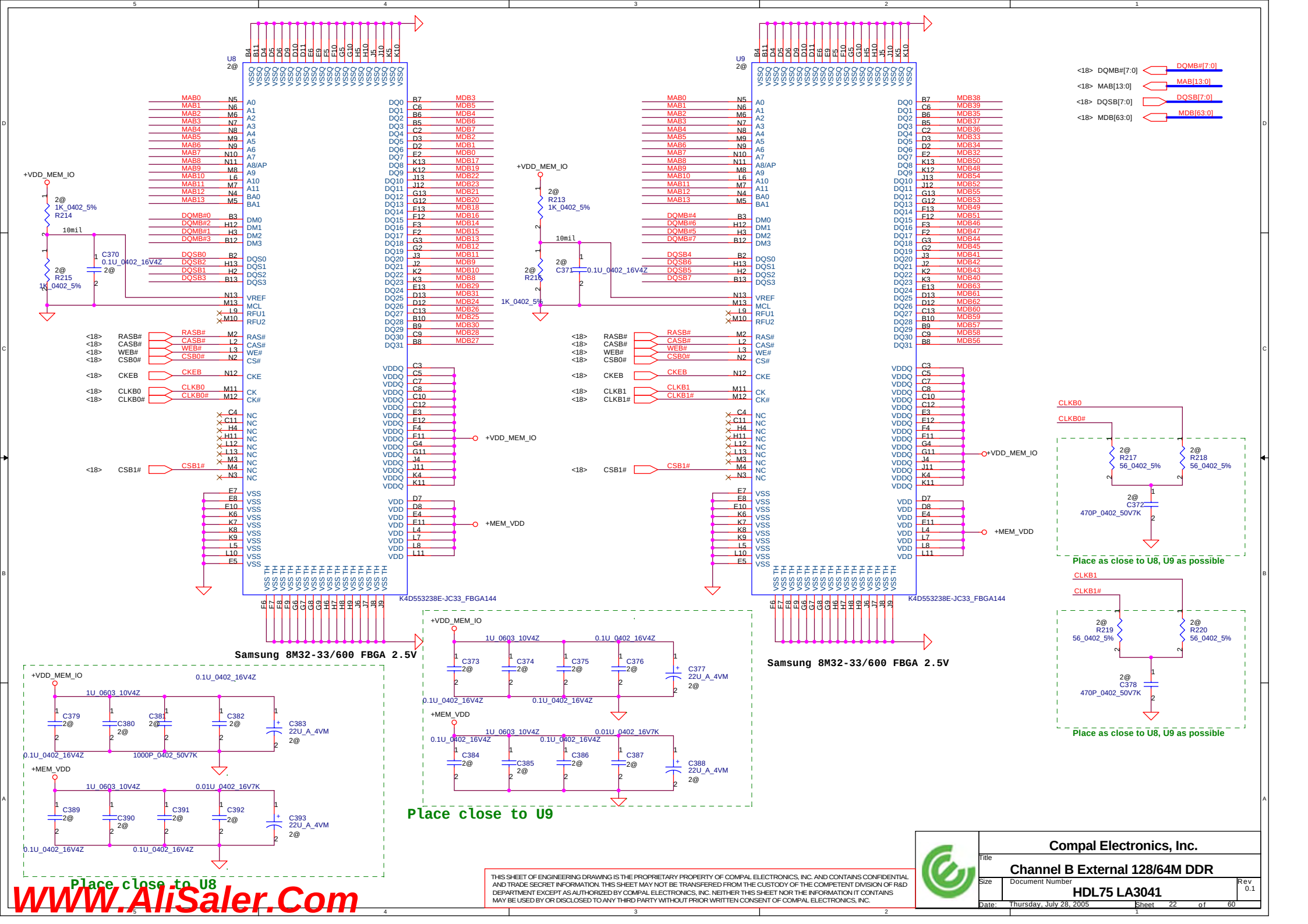

Compal Electronics, Inc.

Title: Channel B External 128/64M DDR

Size: | Document Number: HDL75 LA3041 | Rev: 0.1

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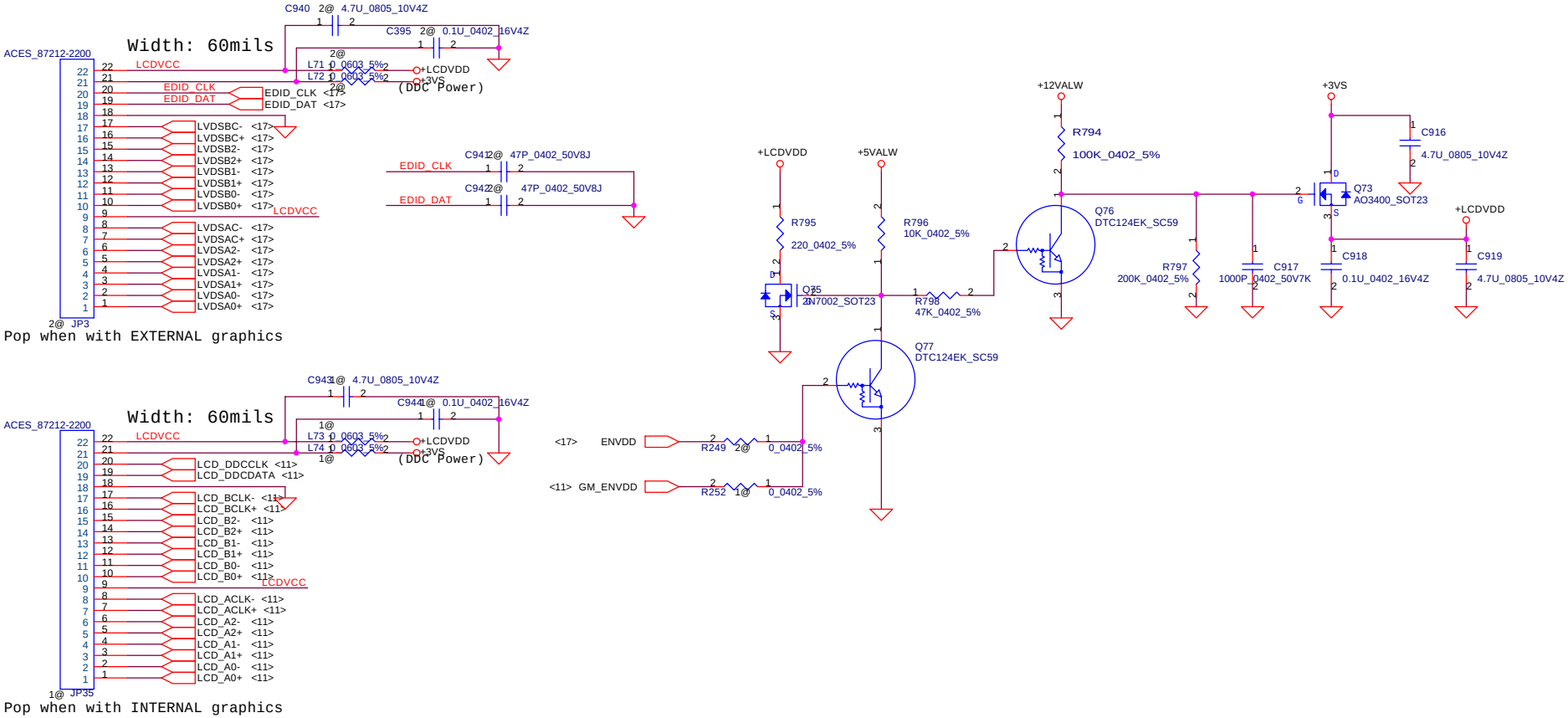
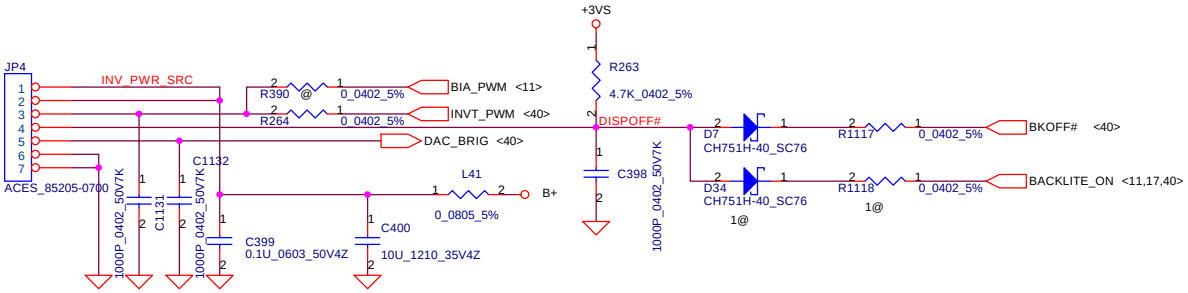
LCD CONN NOTE : place need to ASIC





INVERTER CONN

Compal Electronics, Inc.

Title: LVDS Connector

Size: | Document Number: HDL75 LA3041 | Rev: 0.1

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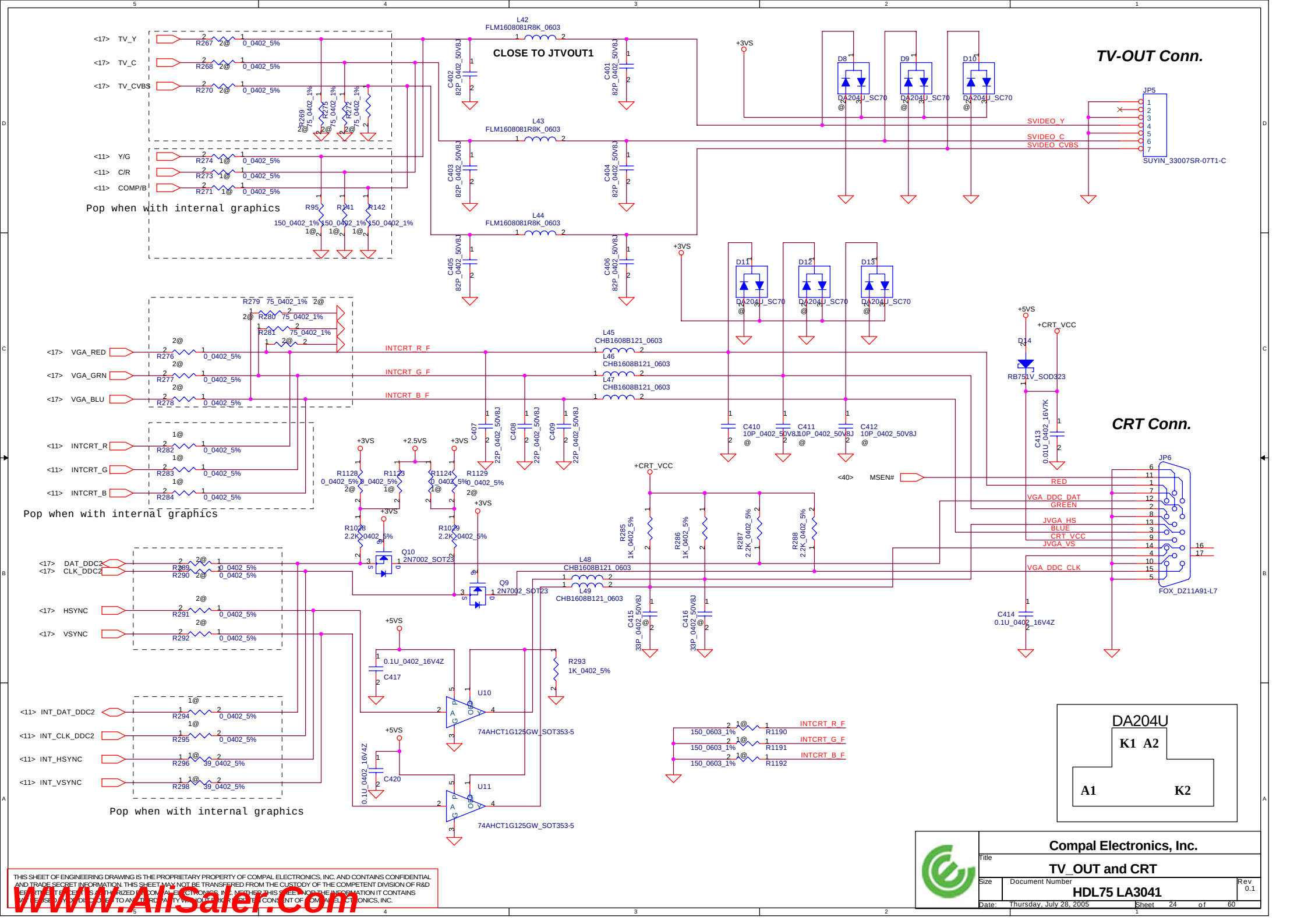
TV-OUT Conn.
CRT Conn.
CLOSE TO JTVOUT1
Pop when with internal graphics
Pop when with internal graphics
Pop when with internal graphics
SUYIN_33007SR-07T1-C
FOX_DZ11A91-L7
74AHCT1G125GW_SOT353-5
74AHCT1G125GW_SOT353-5
DA204U
K1 A2
A1 K2
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TV_OUT and CRT
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Thursday, July 28, 2005
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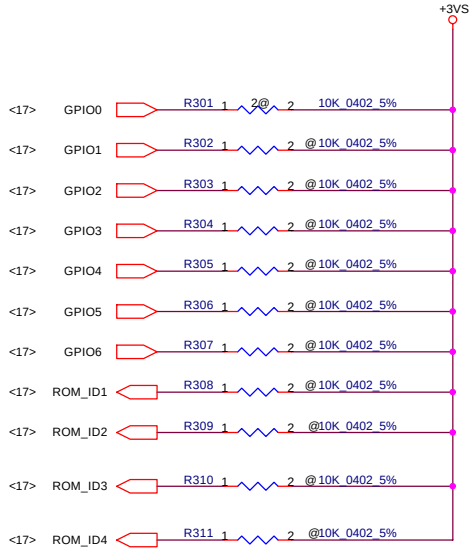
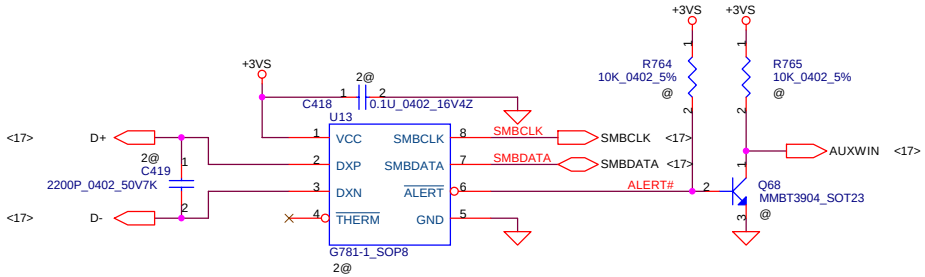


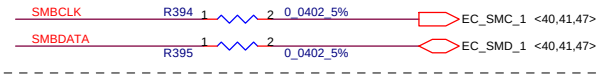
STRAPS	PIN	DESCRIPTION	DEFAULT
CAL_BG_BACKUP	GPIO0	PCI-EXPRESS CURRENT CALIBRATION BANDCAP BACKUP USING REFERENCE VOLTAGE FROM BANDGAP	0
PLL_CAL_FORCE_EN	GPIO1	PCI-EXPRESS FORCE PLL CALIBRATION DISABLED	0
PCIE_MODE(1:0)	GPIO(3:2)	PCI-EXPRESS 1:0A MODE	00
CAL_OFF	GPIO4	**ENABLE TURN OFFPCI-EXPRESS IMPEDENCE/STRRENGTH CALIBRATION**	0
BYPASS_PLL	GPIO5	BYPASS PCI-EXPRESS PLL	0
ICOMP	GPIO6	NORMAL PCI-EXPRESS TRANSMITTER CURRENT COMPENSATION	0
DEBUG_ACCESS	GPIO8	DEBUG SIGNALS NOT BROUGHT OUT	0
ROMIDCFG(3:0)	ROMID (4:1)	SERIAL M25P10 ROM	1011

THERMAL SENSOR

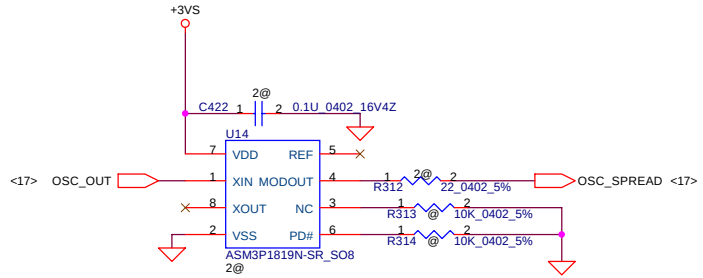
Theraml Chip for M24P only



Reserve for EC to monitor VGA temperature



DDR SPREAD SPECTRUM



Note: Pin3 Reserved for P1819 Spread Rate selection.

Compal Electronics, Inc.

Title: SS & Thermal Sensor

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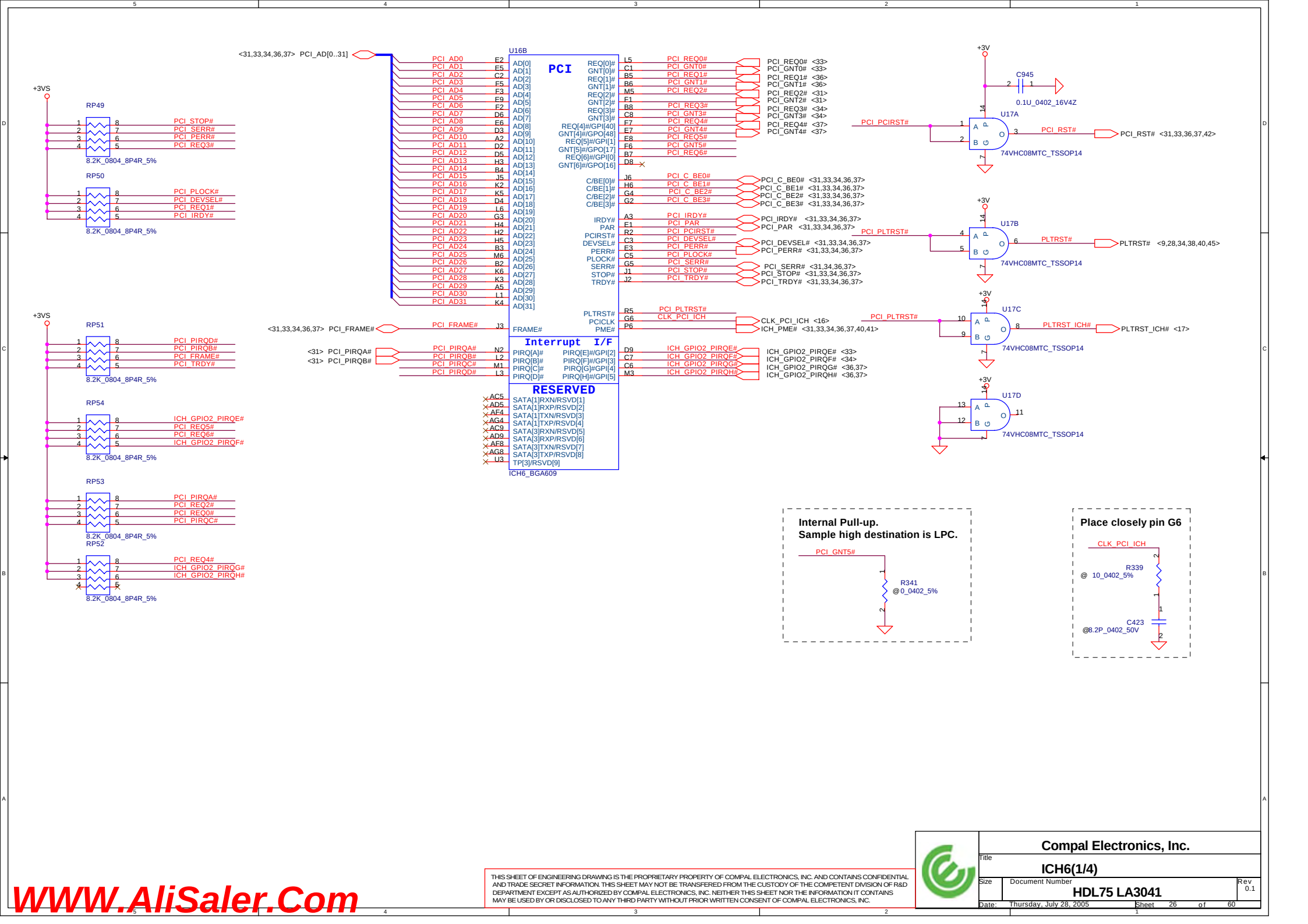
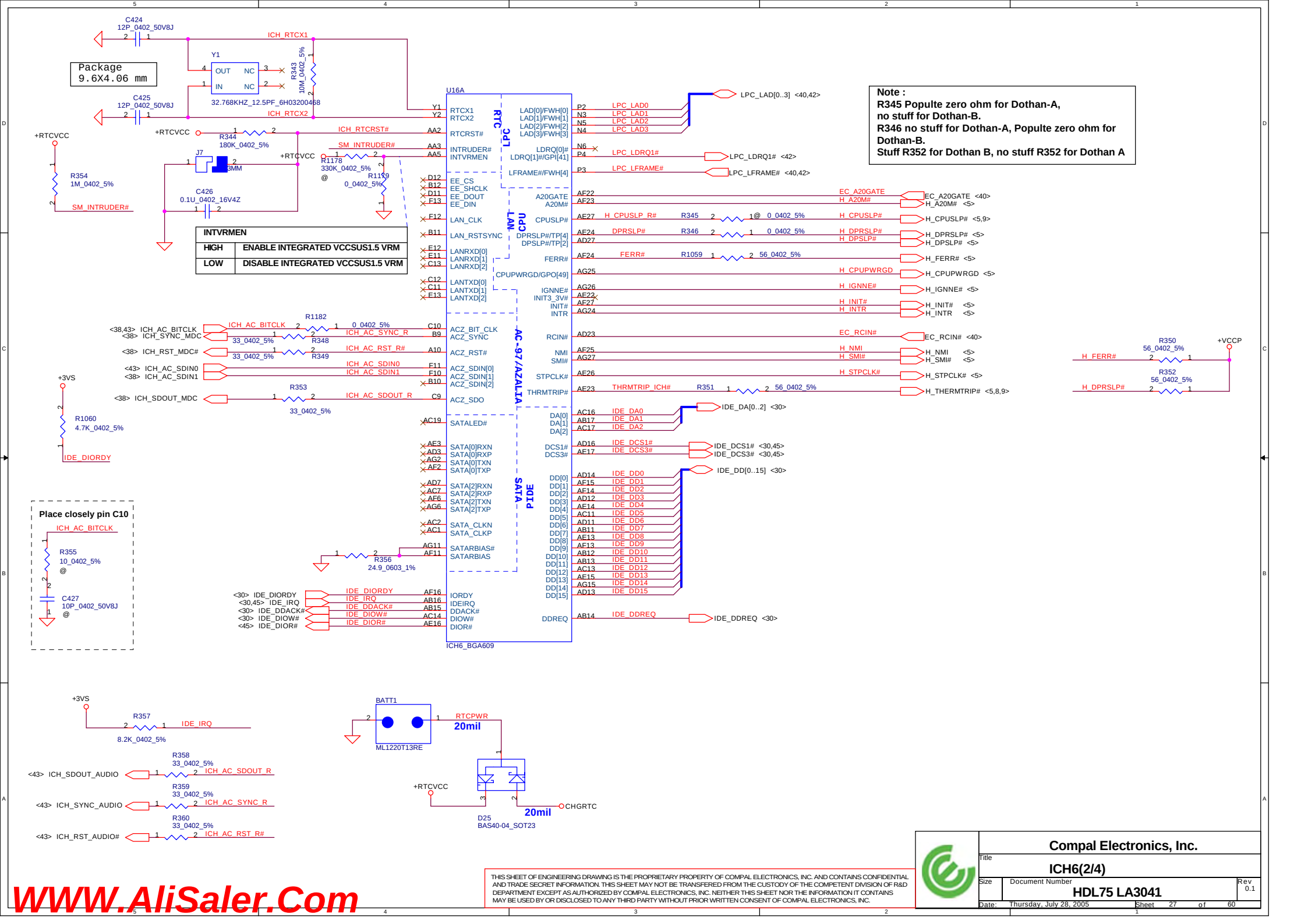


Compal Electronics, Inc.

Title: ICH6(1/4)

Size: | Document Number: HDL75 LA3041 | Rev: 0.1

Date: Thursday, July 28, 2005 | Sheet 26 of 60



Compal Electronics, Inc.	
Title	ICH6(2/4)
Size	Document Number: HDL75 LA3041
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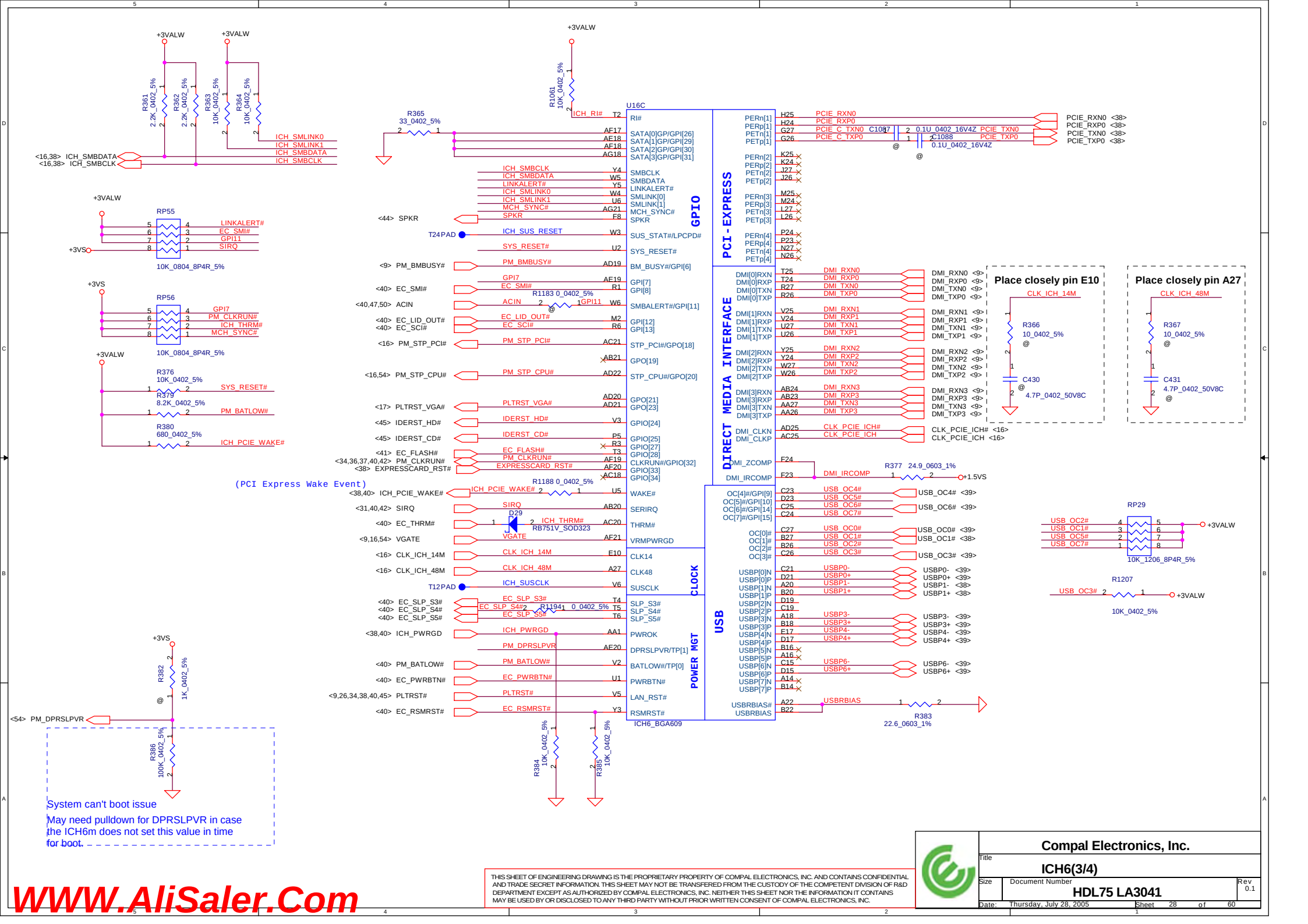

Compal Electronics, Inc.

Title: ICH6(3/4)

Size: | Document Number: HDL75 LA3041 | Rev: 0.1

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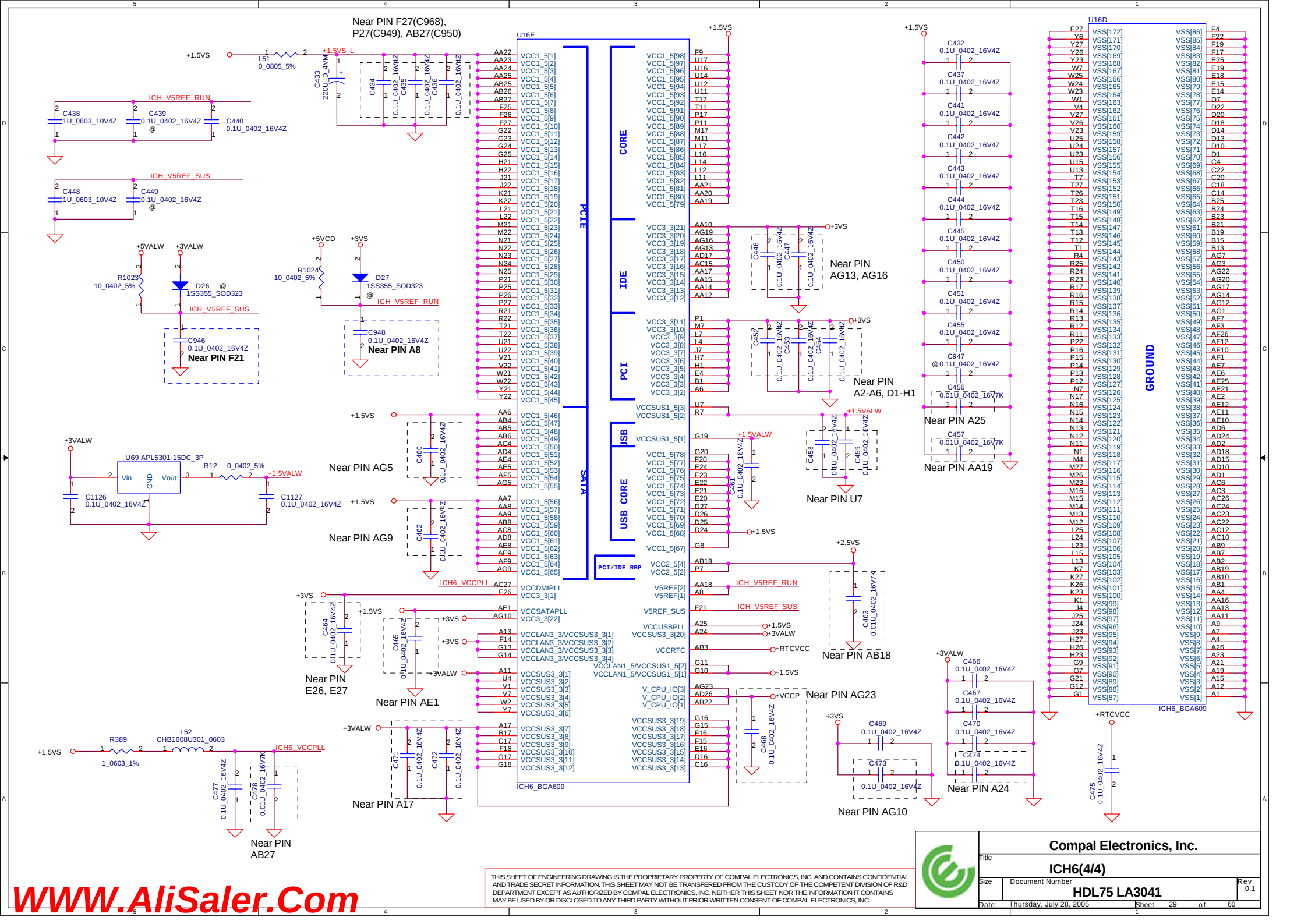
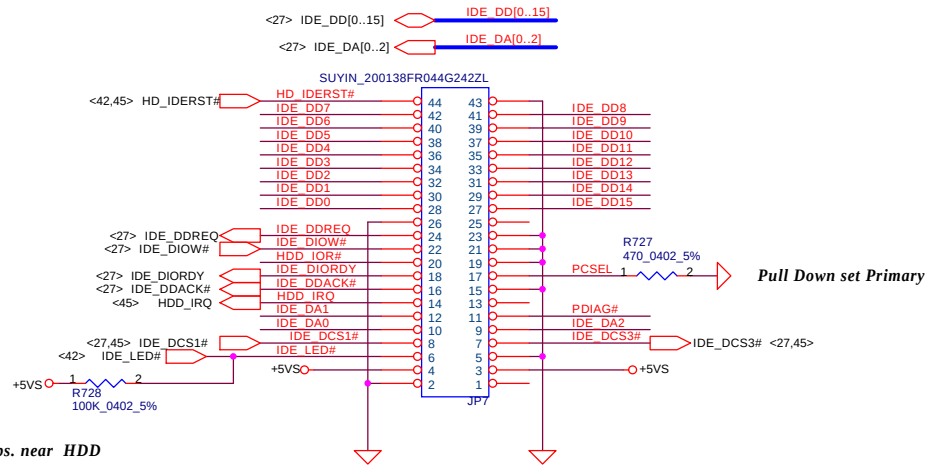
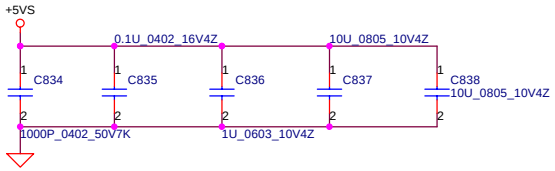


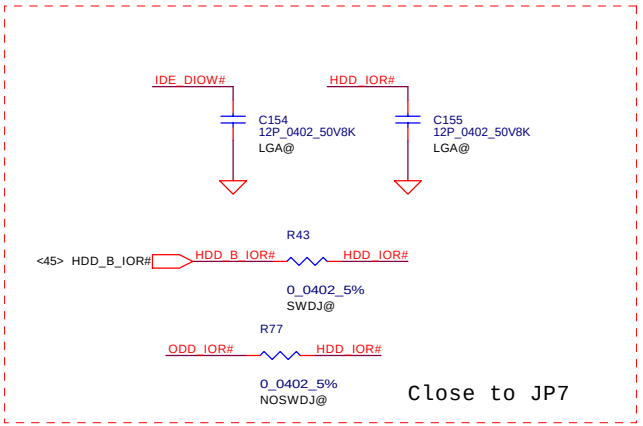
HDD Connector



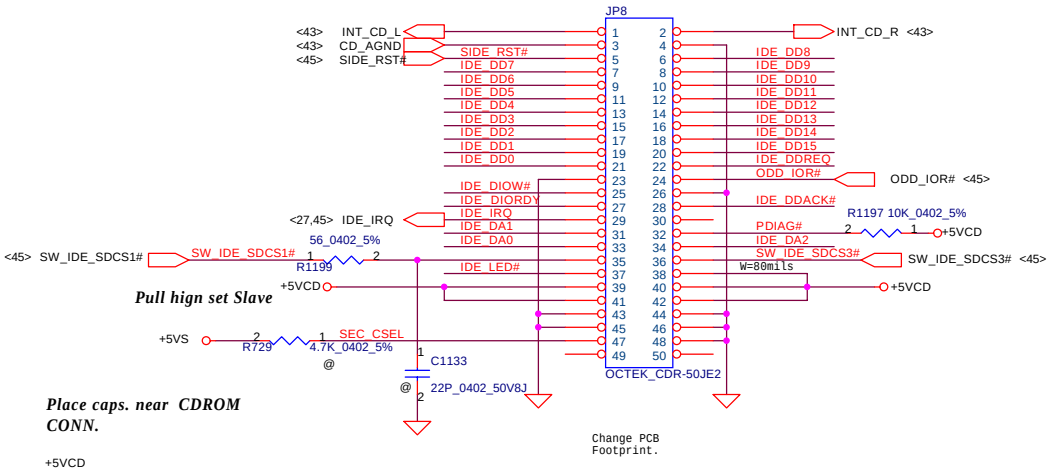
Pull Down set Primary

Placea caps. near HDD CONN.





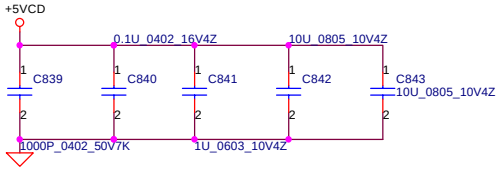
CD-ROM Connector

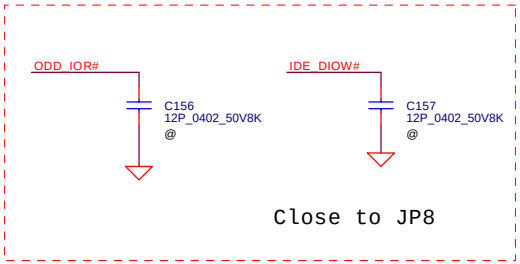


Pull hign set Slave

Place caps. near CDROM CONN.

Change PCB Footprint.





Compal Electronics, Inc.

Title: IDE CONNECTOR

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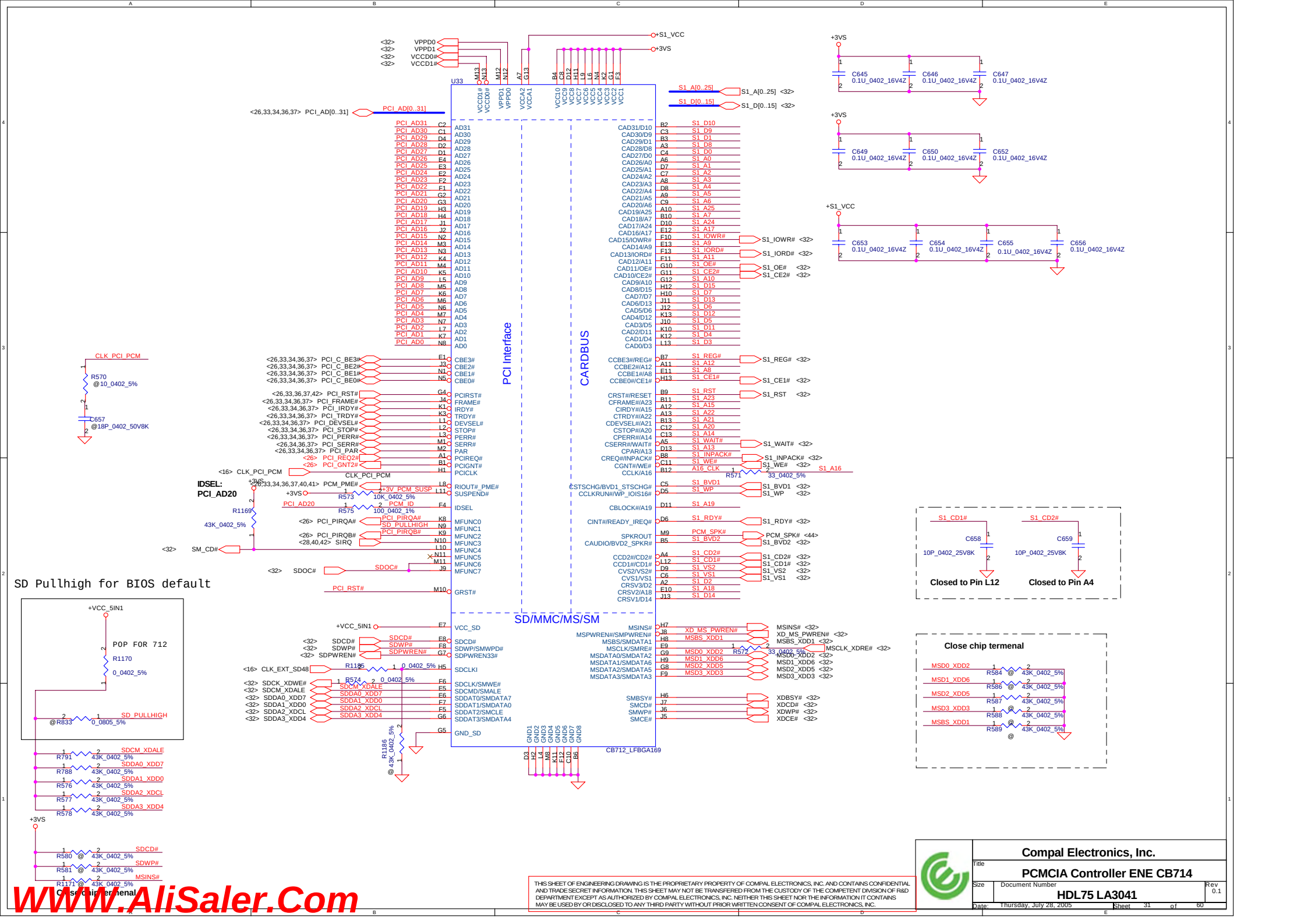
U33
PCI Interface
CARDBUS
SD/MMC/MS/SM
CB712_LFBGA169
PCI_AD[0..31]
S1_A[0..25]
S1_D[0..15]
SD Pullhigh for BIOS default
POP FOR 712
Close chip termenal
Closed to Pin L12
Closed to Pin A4
IDSEL:
PCI_AD20
Compal Electronics, Inc.
PCMCIA Controller ENE CB714
HDL75 LA3041
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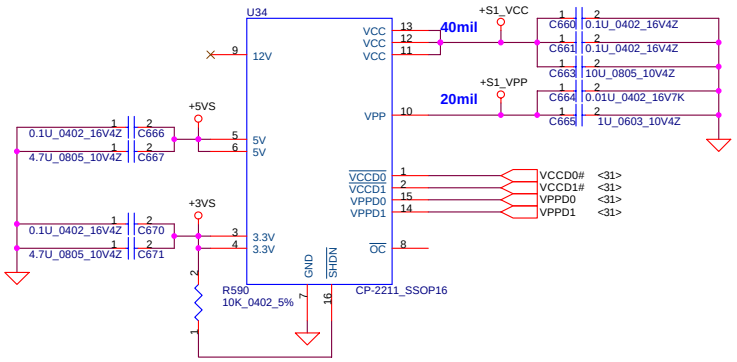
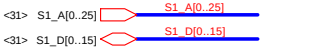
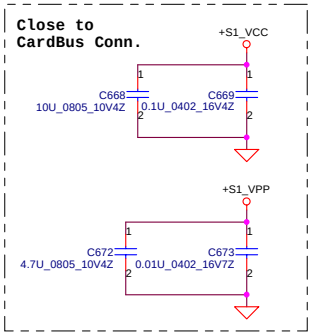
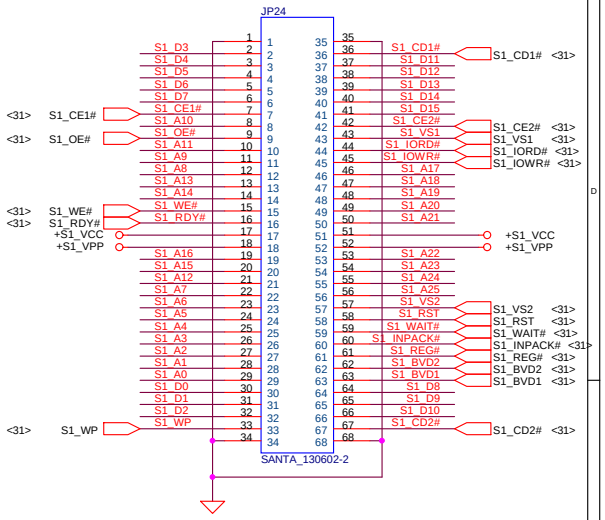
PCMCIA Power Controller

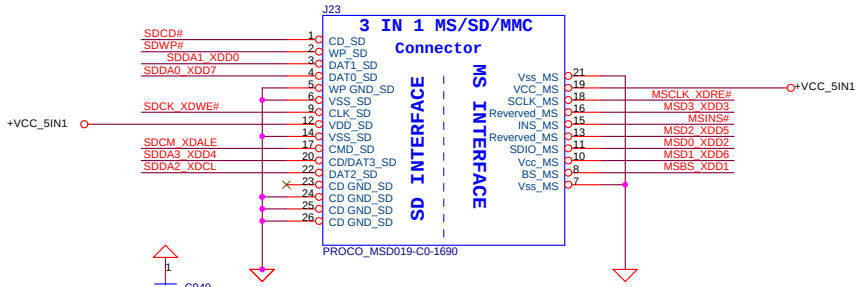


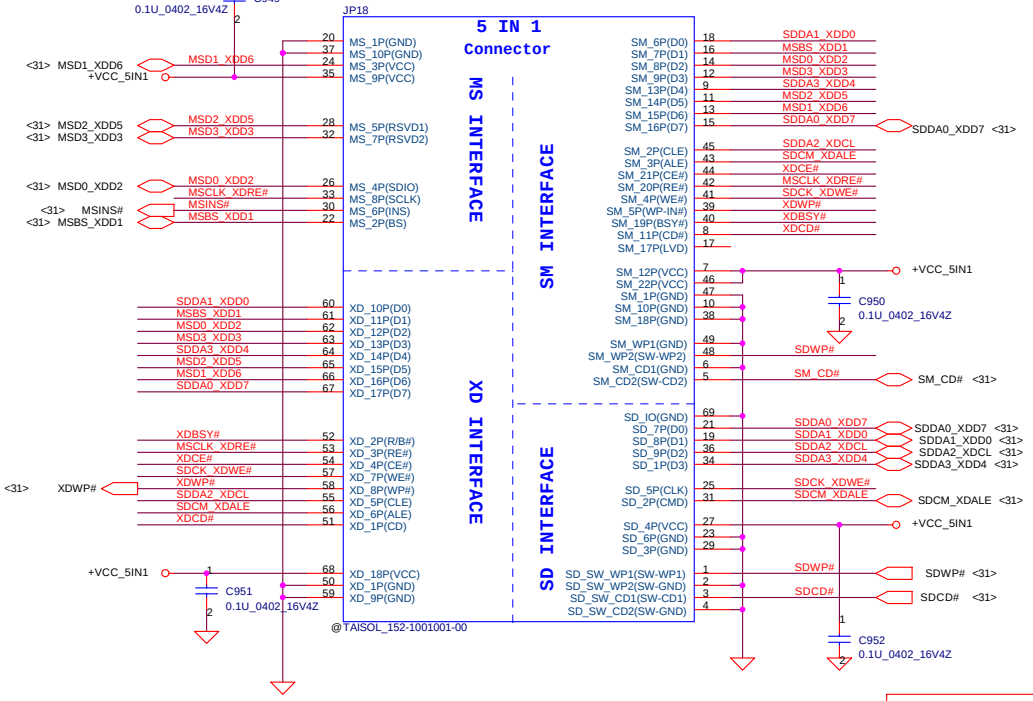
CardBus Socket

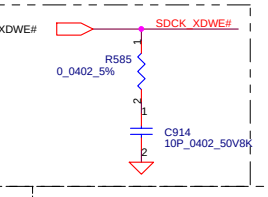


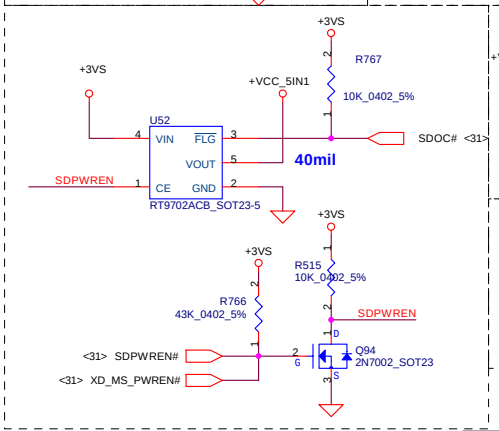


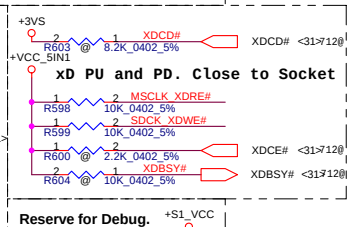


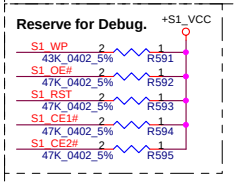












Compal Electronics, Inc.

Title: PCMCIA Socket

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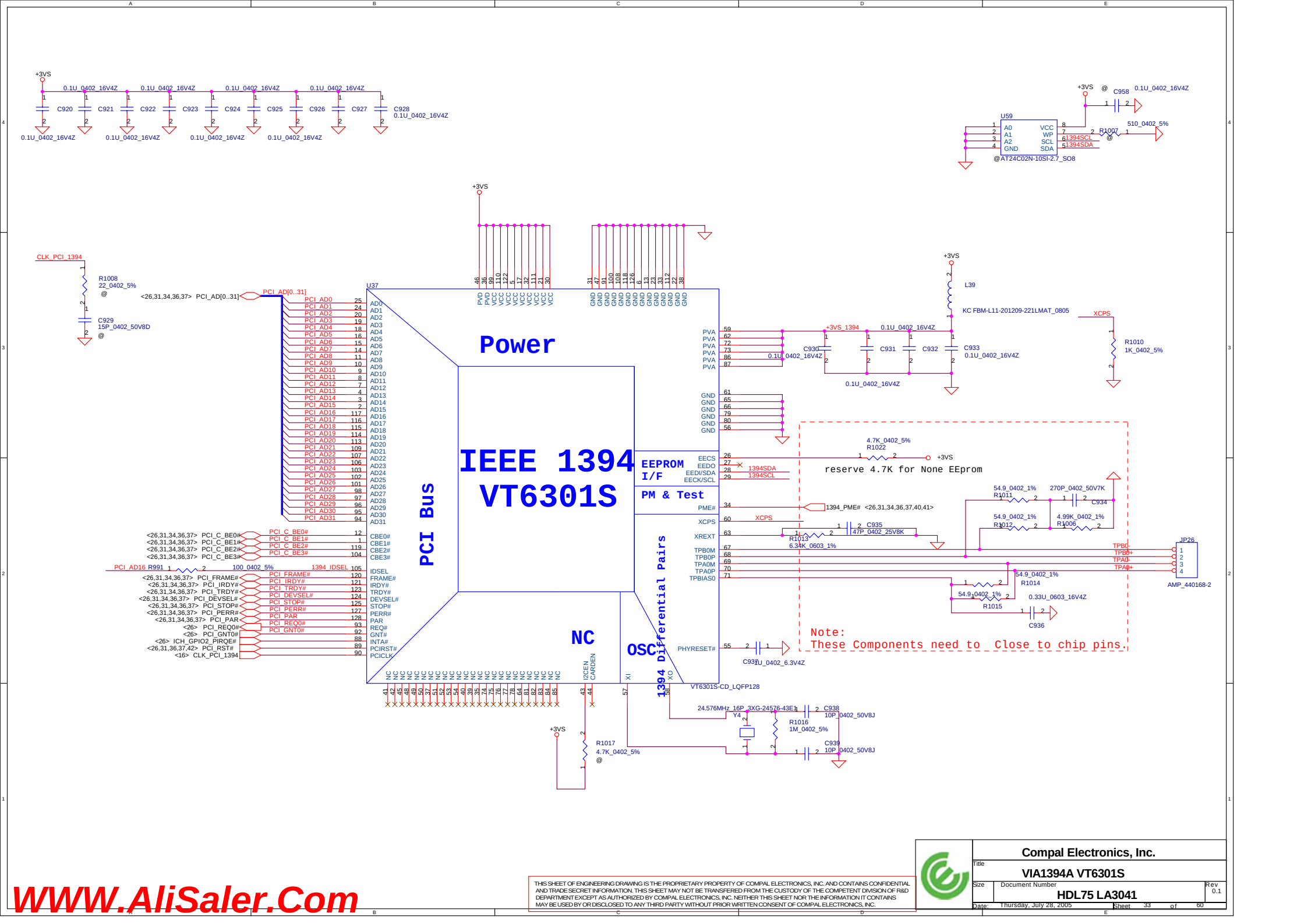
Power
IEEE 1394
VT6301S
PCI Bus
EEPROM I/F
PM & Test
1394 Differential Pairs
OSC
NC
U37
VT6301S-CD_LQFP128
reserve 4.7K for None EEprom
Note:
These Components need to _ Close to chip pins.
Compal Electronics, Inc.
VIA1394A VT6301S
HDL75 LA3041
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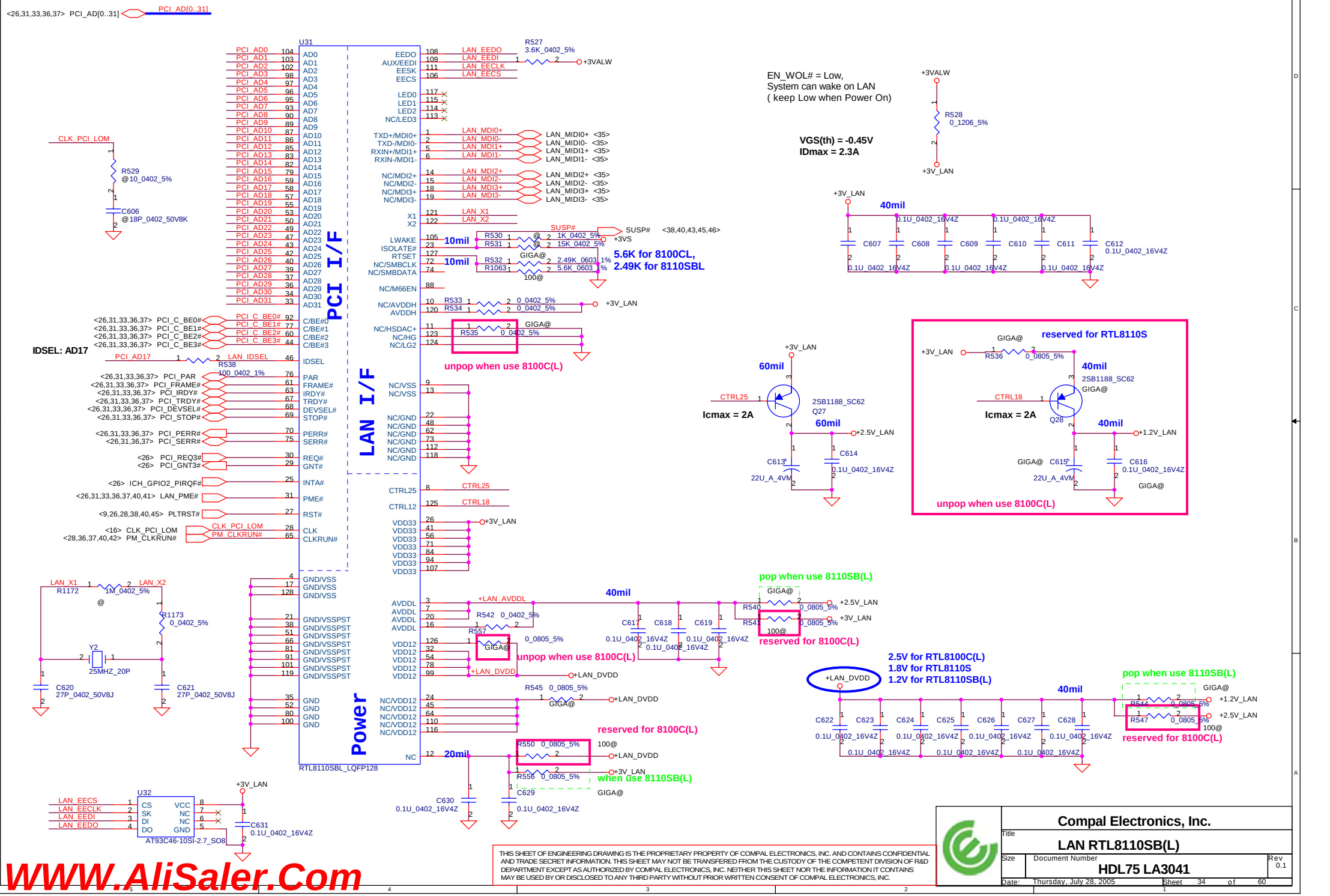
LAN RTL8110SB(L)



Compal Electronics, Inc.	
Title	LAN RTL8110SB(L)
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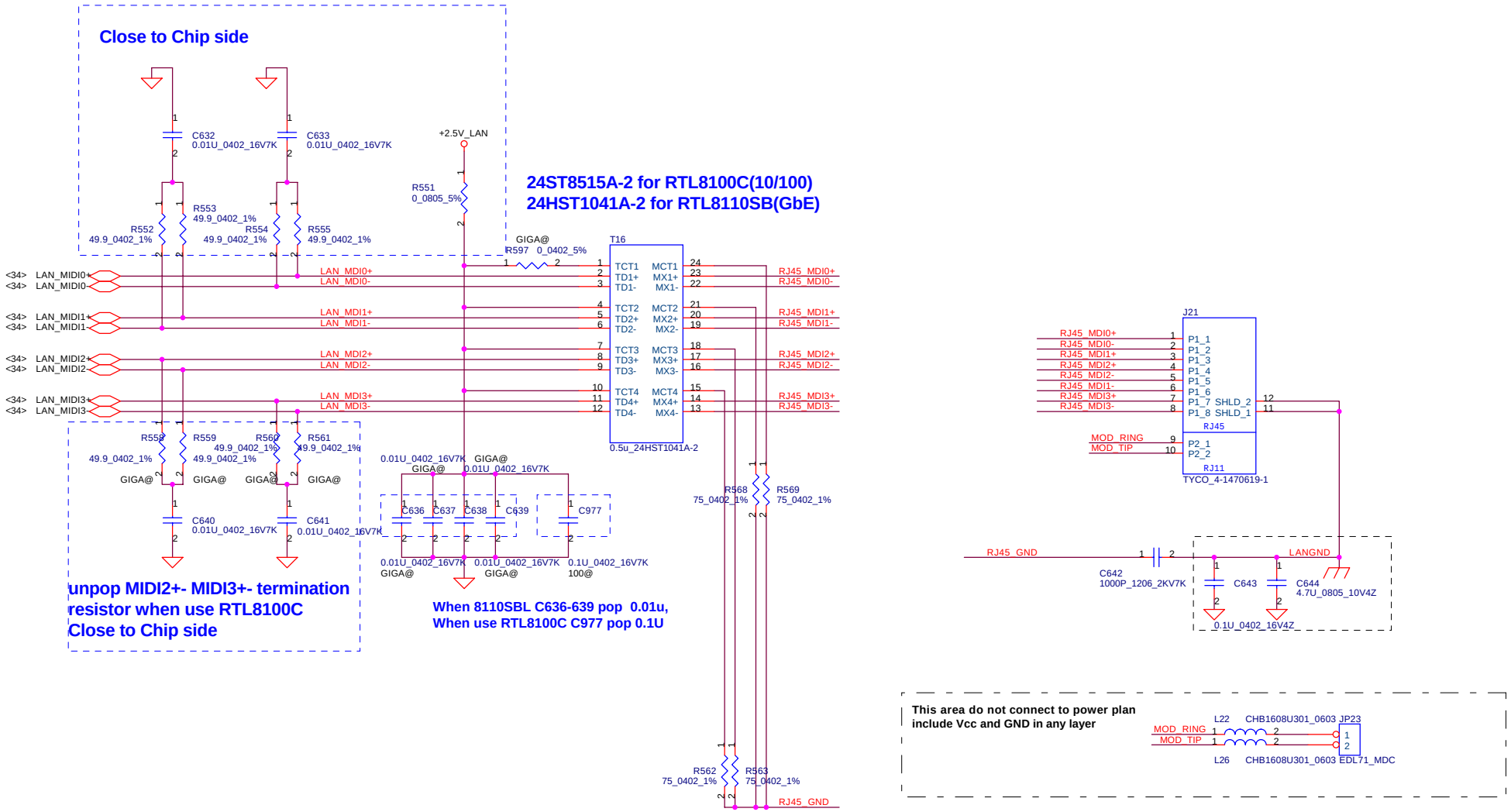

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45/RJ11

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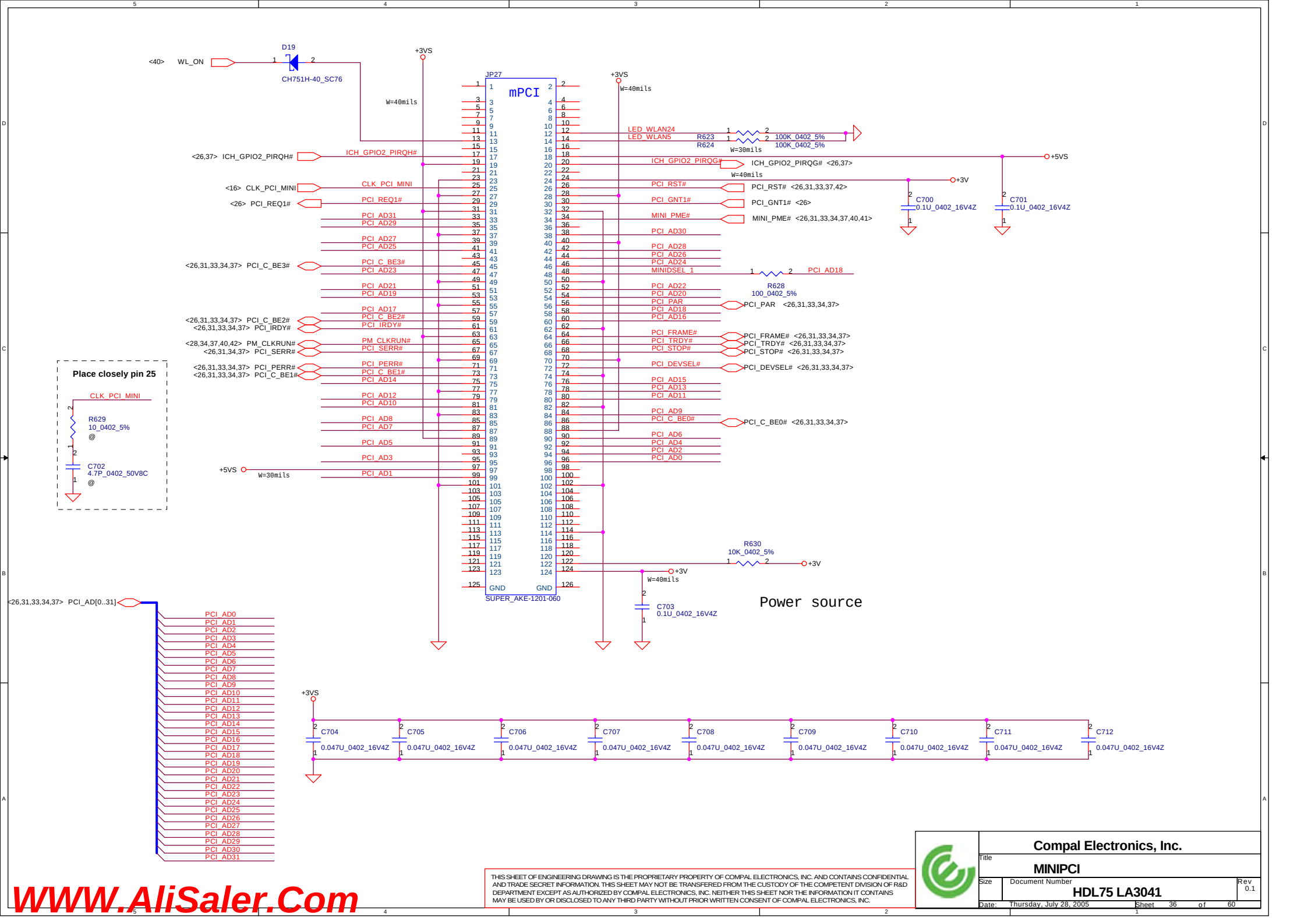

Compal Electronics, Inc.

Title: MINIPCI

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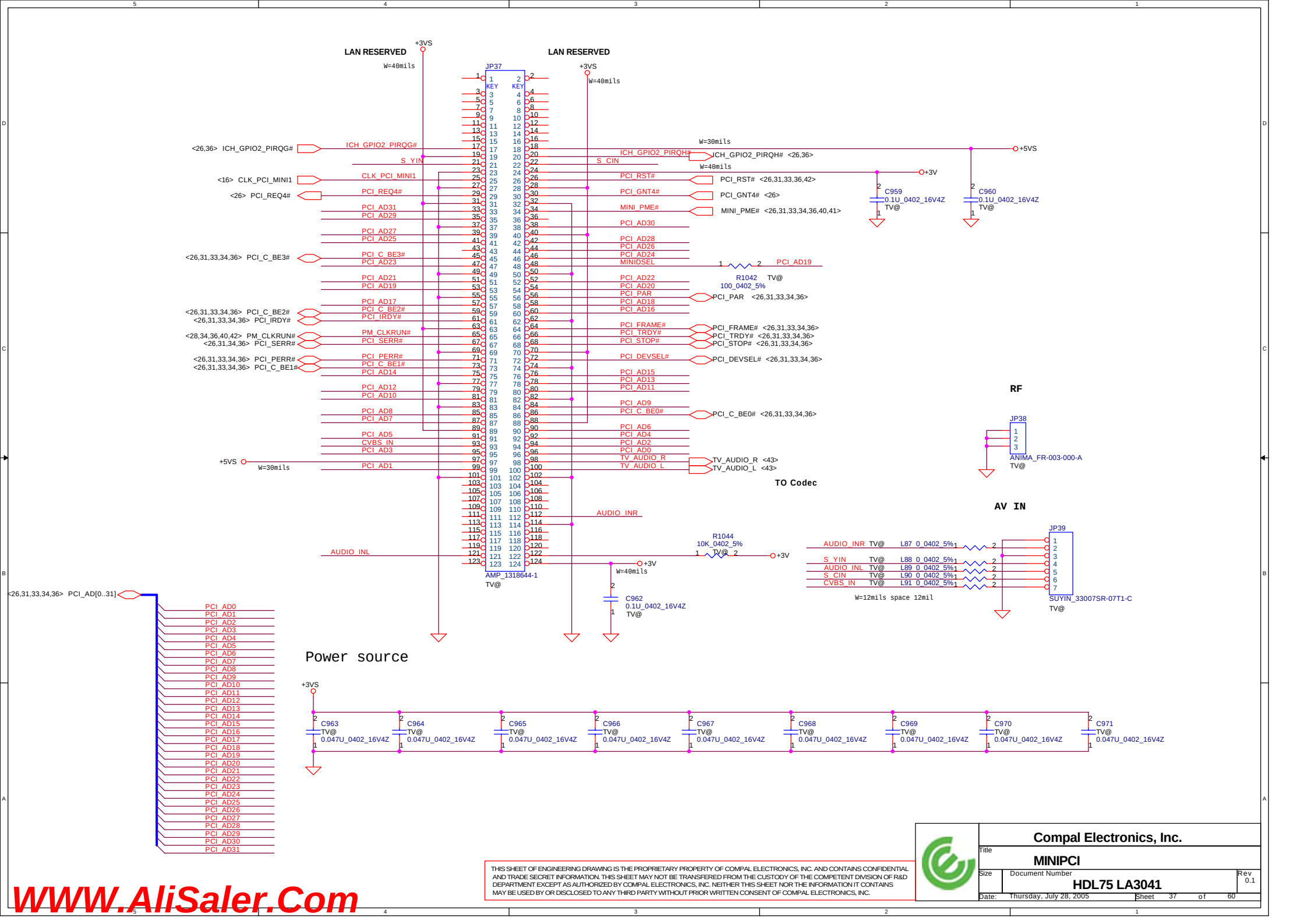

Compal Electronics, Inc.
Title: MINIPCI
Size: Document Number: HDL75 LA3041
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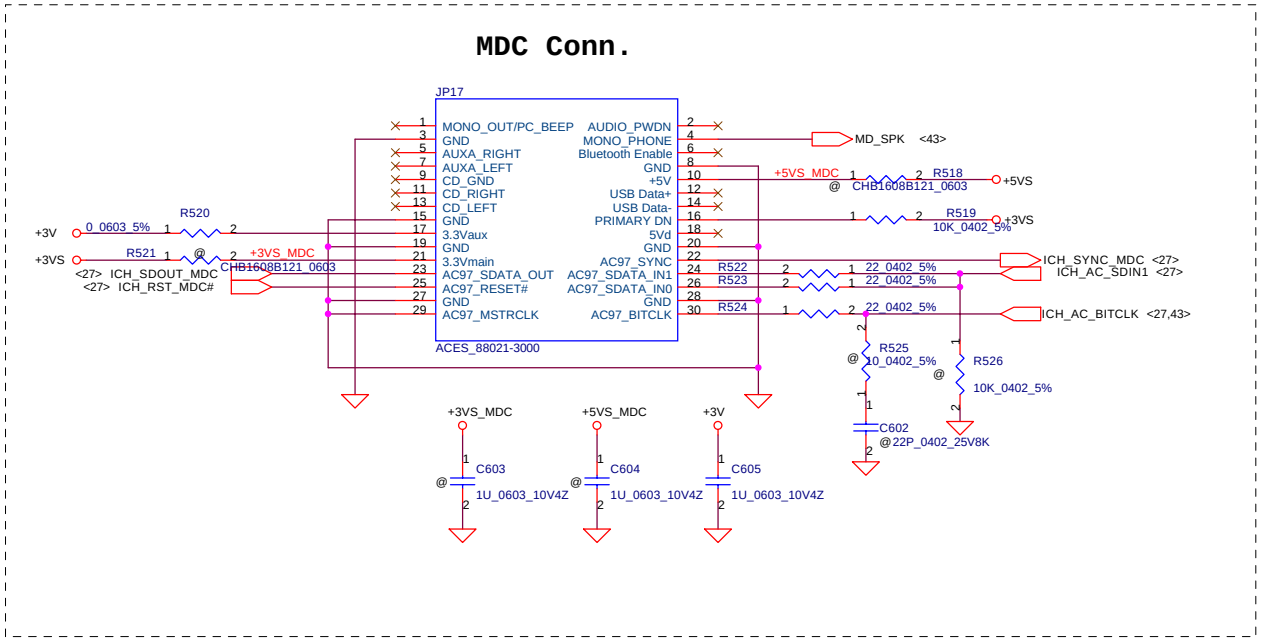

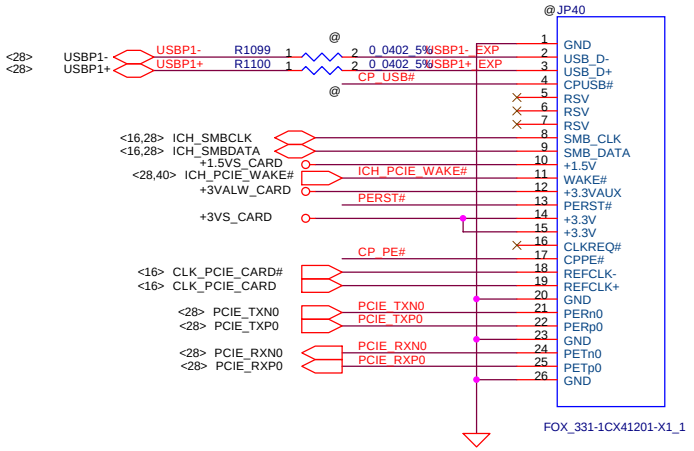

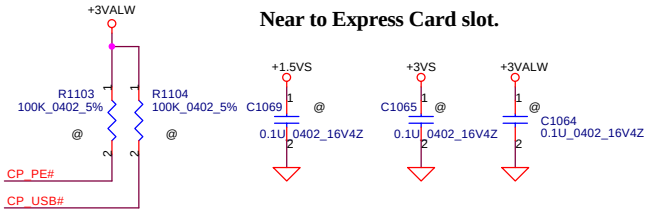

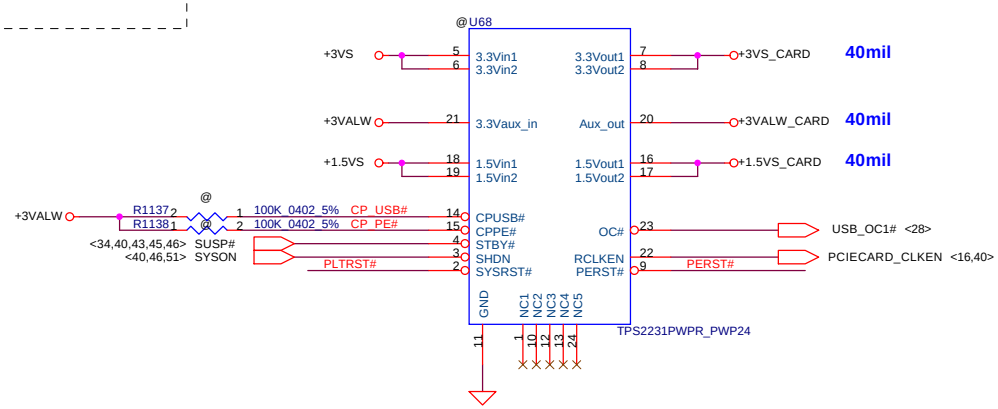

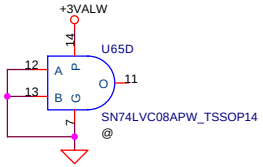

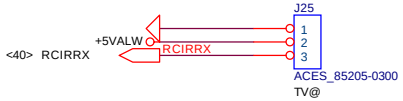

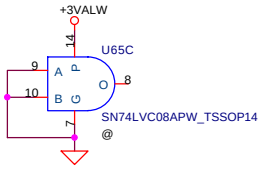

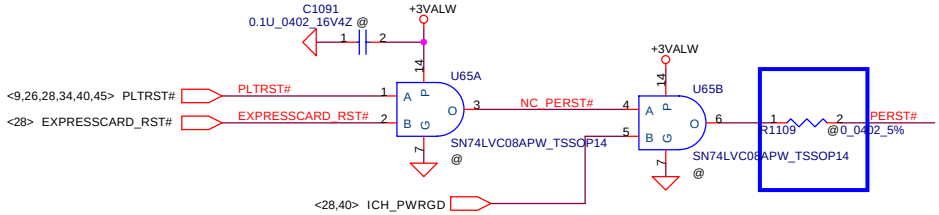

Compal Electronics, Inc.

Title: MDC Express Card Conn.

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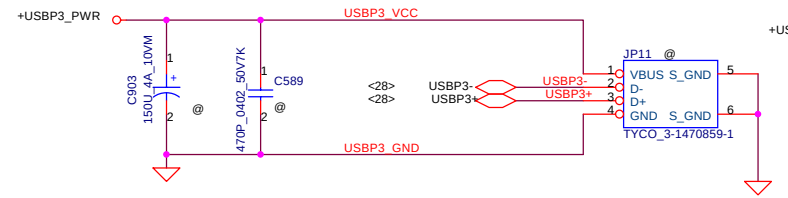
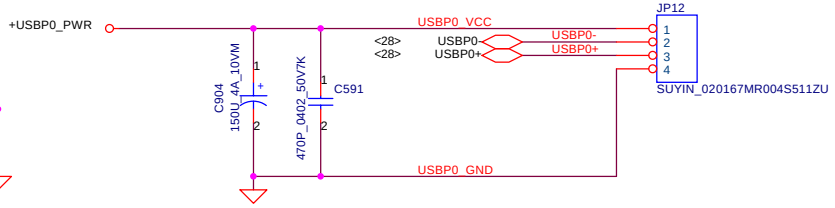
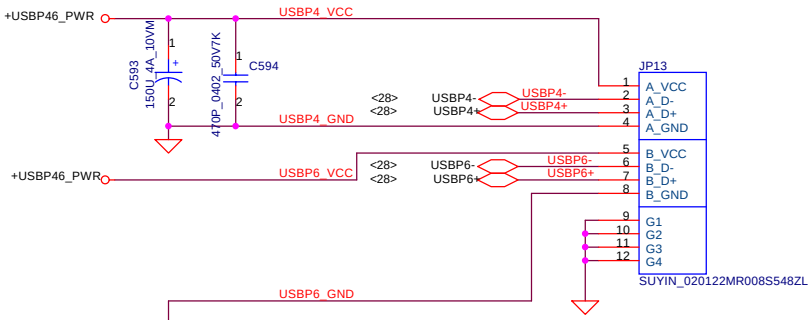
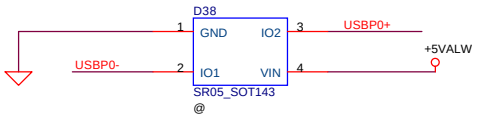
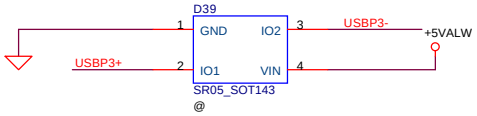
USB PORT#	DESTINATION
0	JUSB1(JP12)
1	Express Card
2	JUSB2(JP11)
3	Reserve
4	JUSB3(JP13UP)
5	Reserve
6	JUSB3(JP13LOW)
7	Reserve

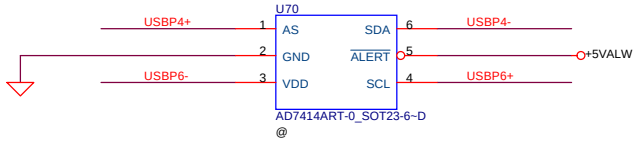


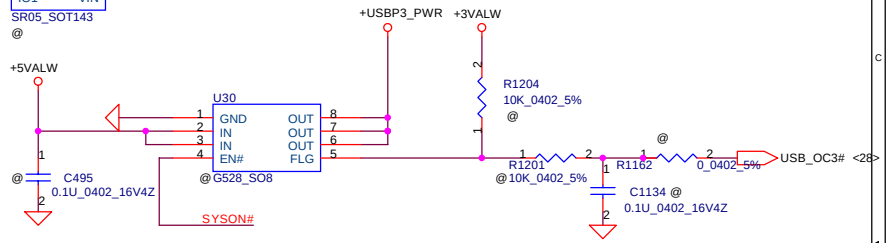




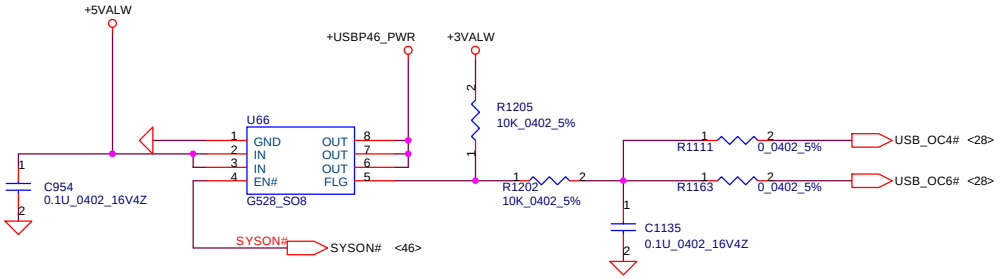


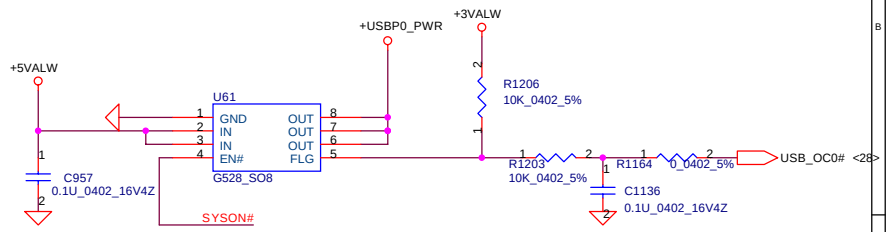






USB Over Current





Note:
USB_AS=USB_BS=Trace width=40mils

Compal Electronics, Inc.

Title: USB 2.0 Port

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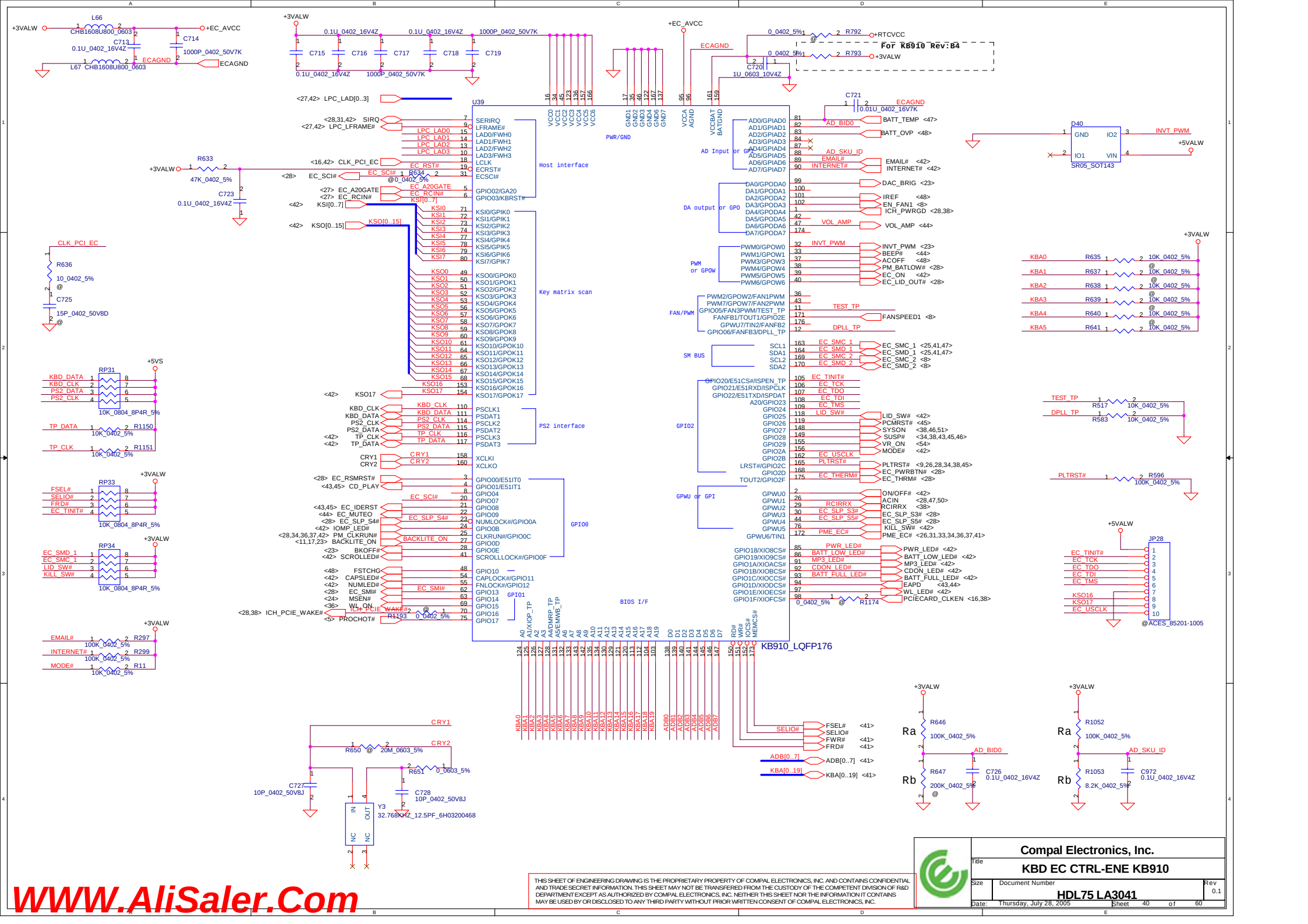
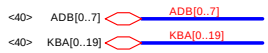
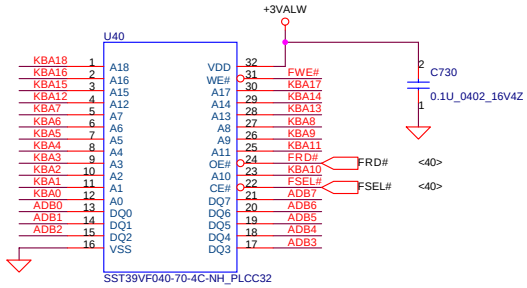
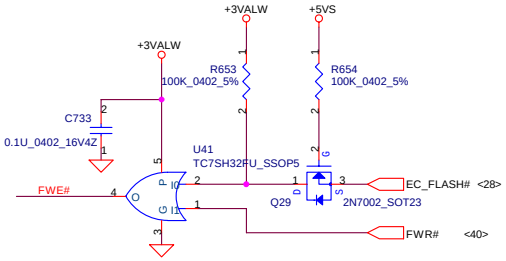
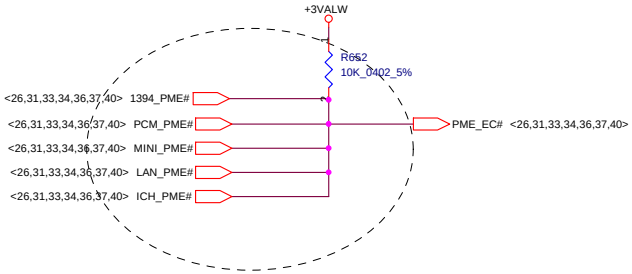


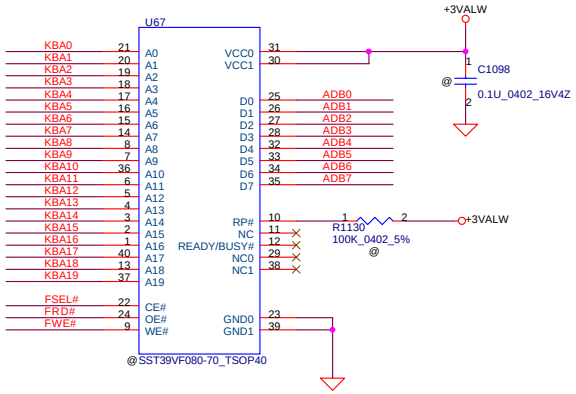


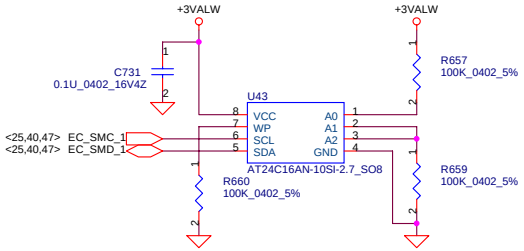


1MB Flash ROM









Compal Electronics, Inc.		
Title: BIOS & EC I/O Port		
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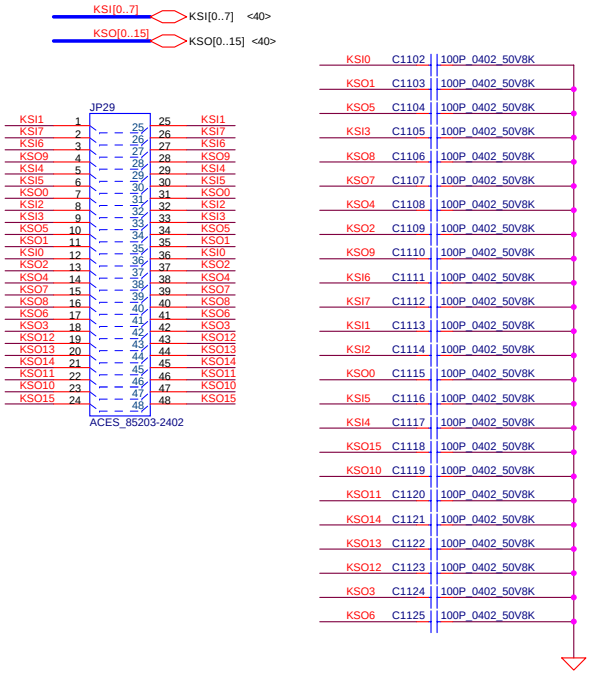
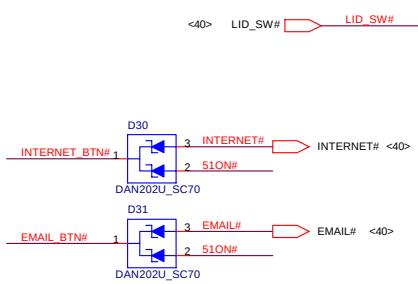
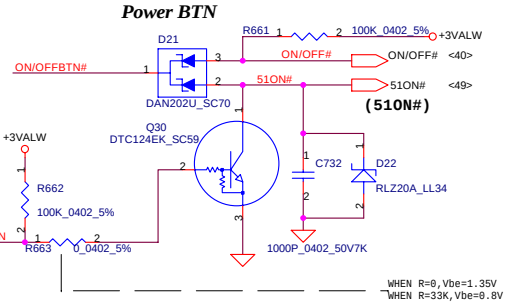
INT_KBD CONN.



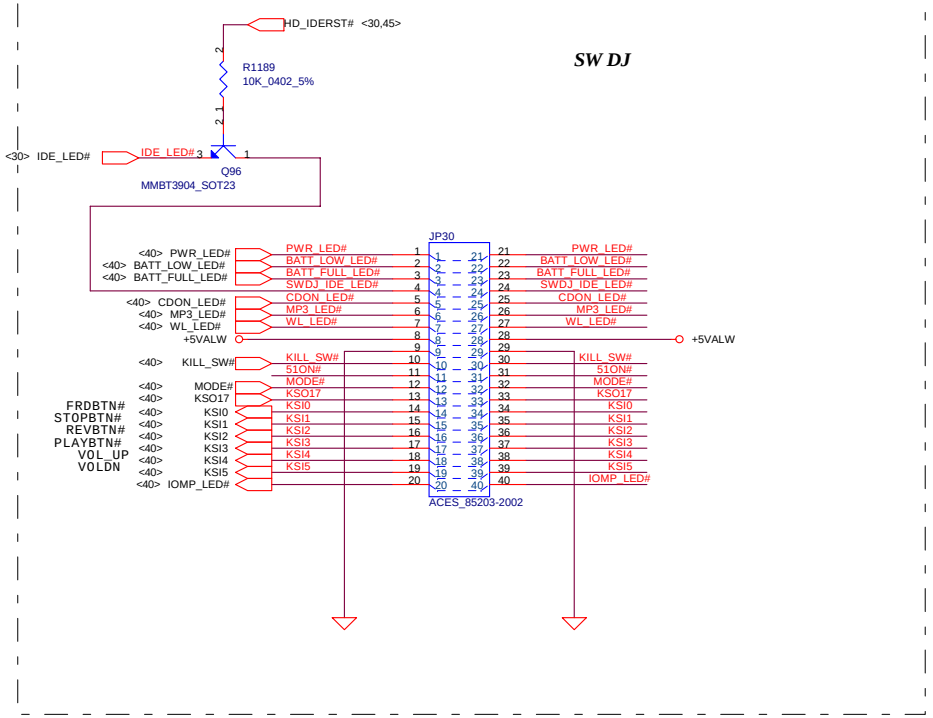
LID Switch



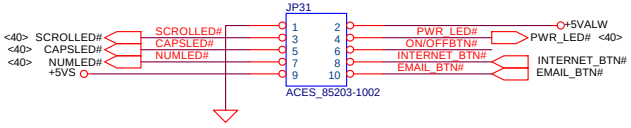
Power BTN



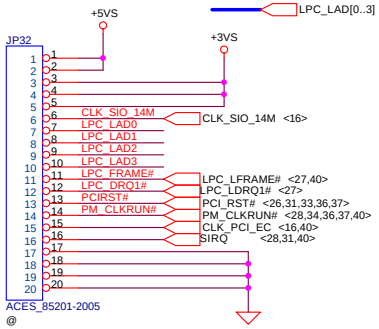
SW DJ

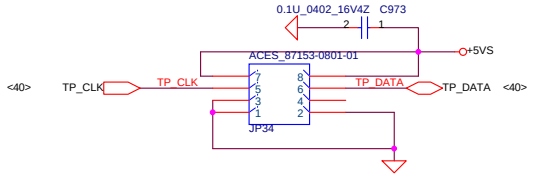


TO PWR /LED BOARD



FOR LPC SIO DEBUG PORT





T/P

Compal Electronics, Inc.	
Title	KBD,ON/OFF,T/P,LED & FIR
Size	Document Number: HDL75 LA3041
Rev	0.1
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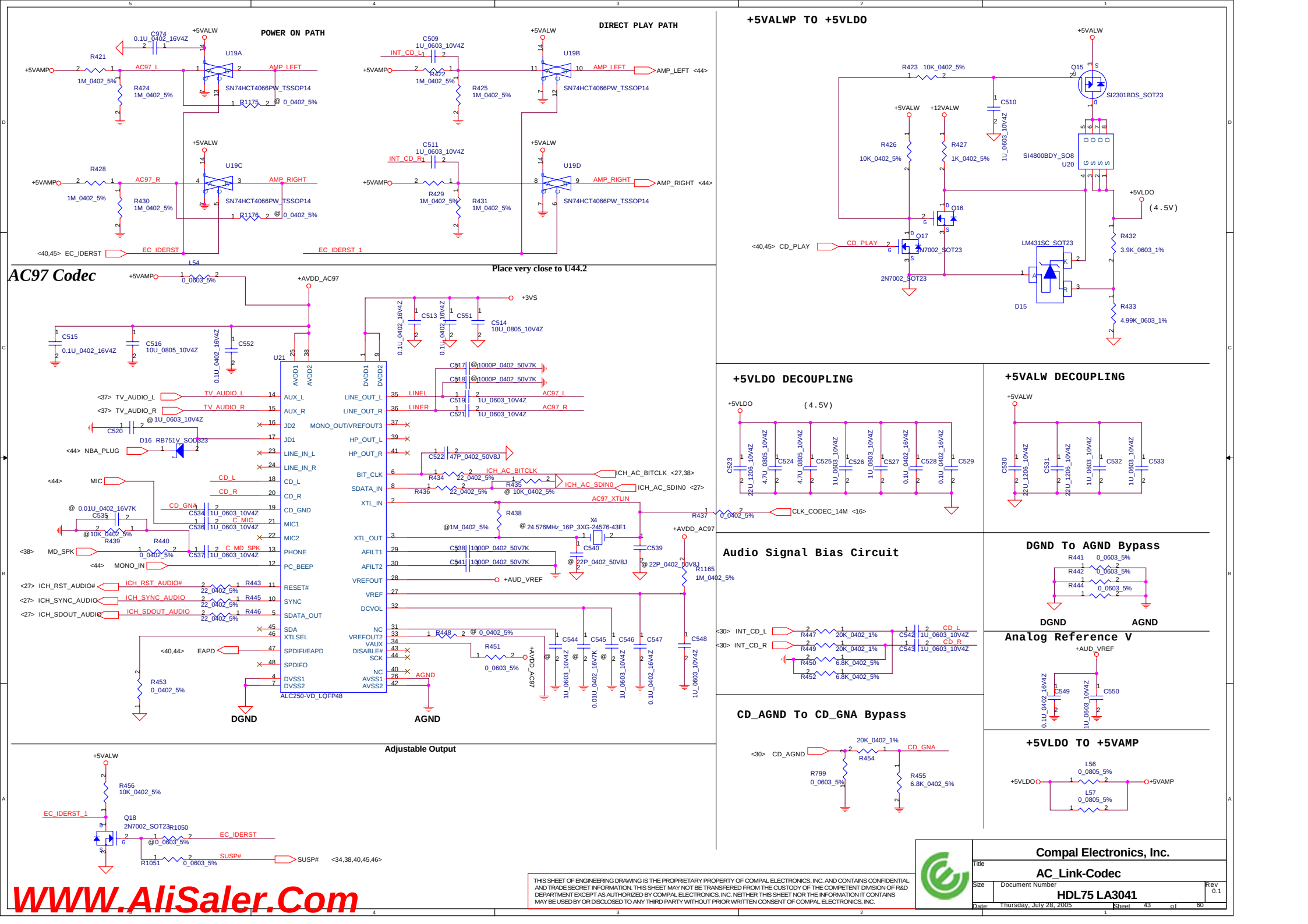
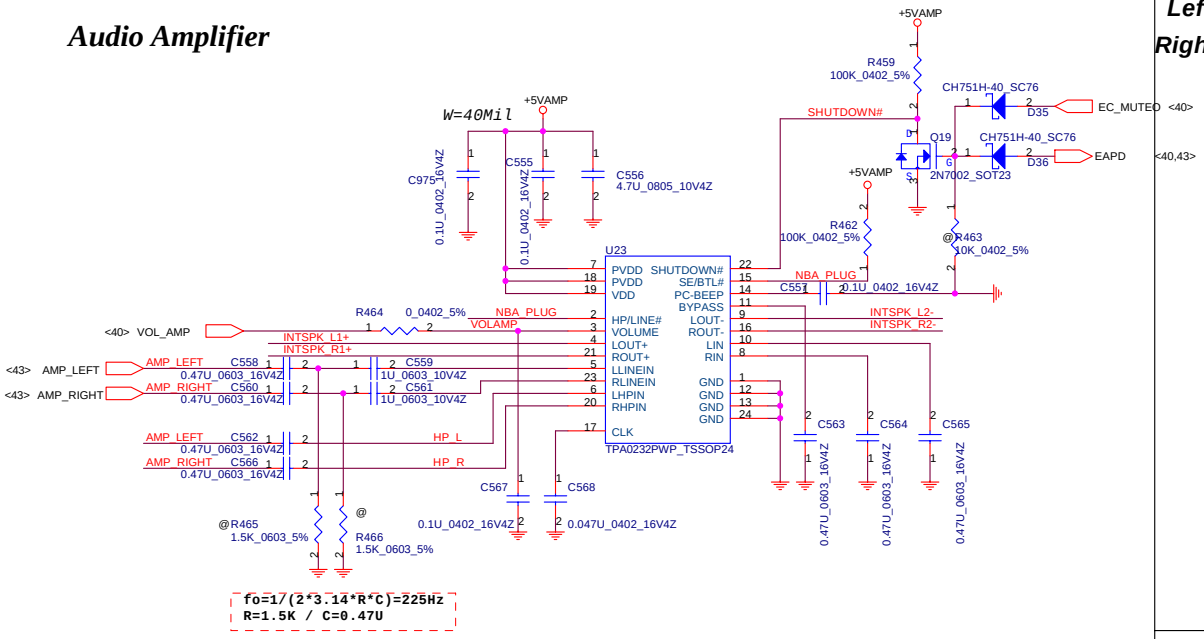
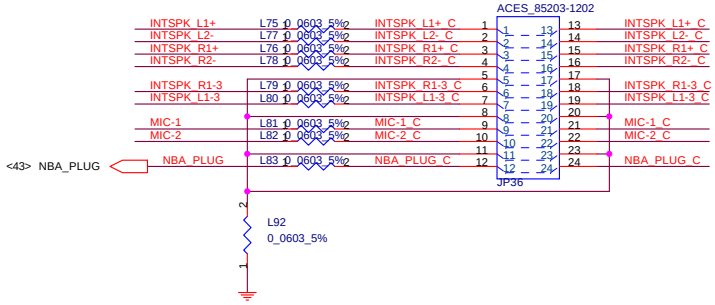

POWER ON PATH
DIRECT PLAY PATH
+5VALWP TO +5VLDO
AC97 Codec
Place very close to U44.2
+5VLDO DECOUPLING
+5VALW DECOUPLING
Audio Signal Bias Circuit
DGND To AGND Bypass
Analog Reference V
CD_AGND To CD_GNA Bypass
+5VLDO TO +5VAMP
Adjustable Output
ALC250-VD_LQFP48
SN74HCT4066PW_TSSOP14
SI2301BDS_SOT23
SI4800BDY_SO8
LM431SC_SOT23
2N7002_SOT23
DGND
AGND
Compal Electronics, Inc.
AC_Link-Codec
HDL75 LA3041
Rev 0.1
Thursday, July 28, 2005
Sheet 43 of 60
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
WWW.AliSaler.Com

Audio Amplifier



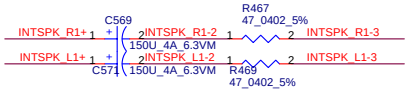
fo=1/(2*3.14*R*C)=225Hz
R=1.5K / C=0.47U

Left Speaker Connector
Right Speaker Connector

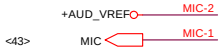


CHANGE CONN

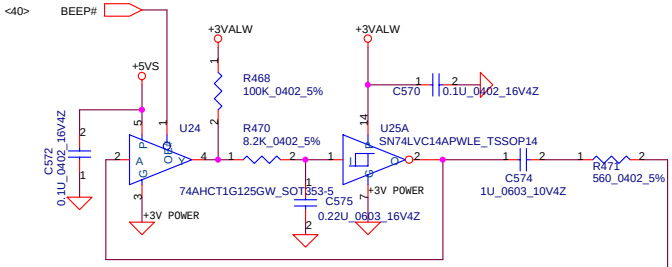
HEADPHONE OUT JACK



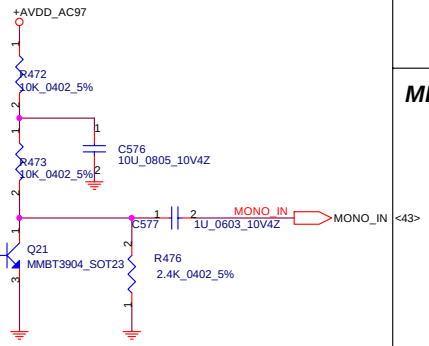
MICROPHONE IN JACK



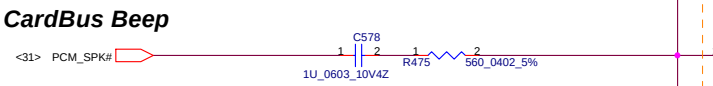
EC Beep



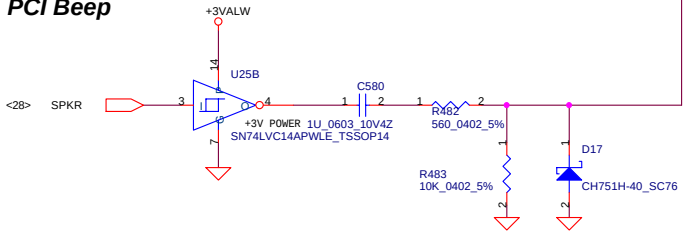
System Beep To AC97' Codec



CardBus Beep



PCI Beep



Compal Electronics, Inc.	
Title	Audio_AMP&JACKs
Size	Document Number: HDL75 LA3041 — Rev: 0.1
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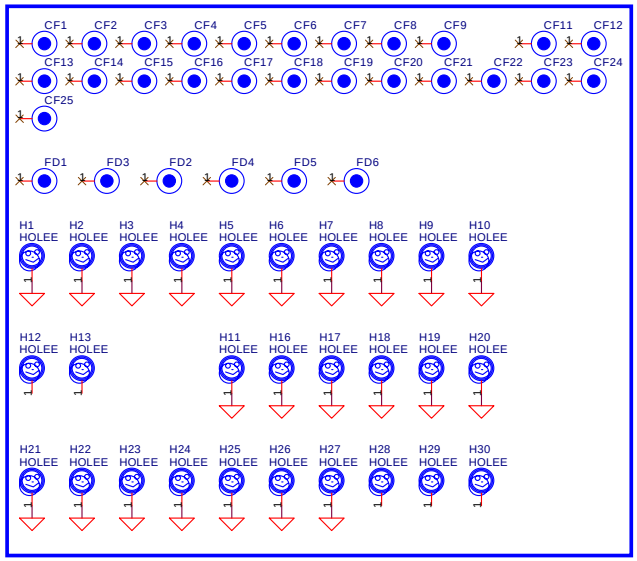
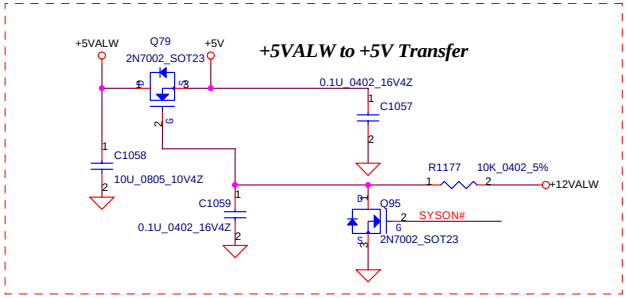


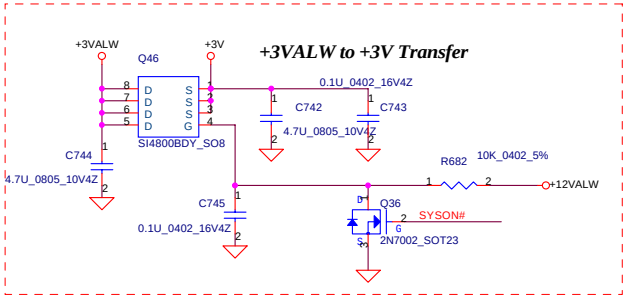
Compal Electronics, Inc.

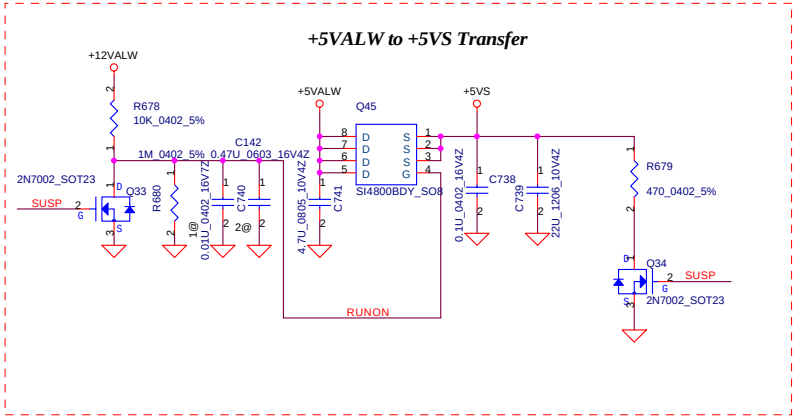
Title: SW DJ,RESET CKT,SW,LED BOAR

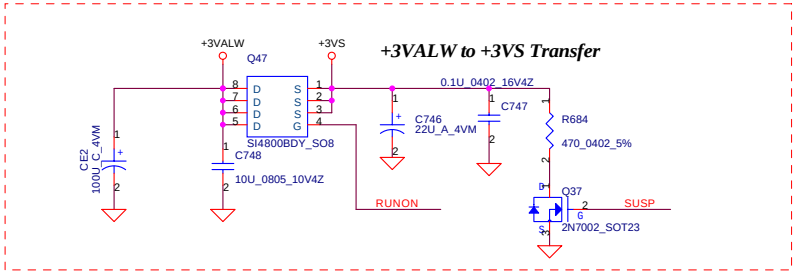
Size: | Document Number: HDL75 LA3041 | Rev: 0.1

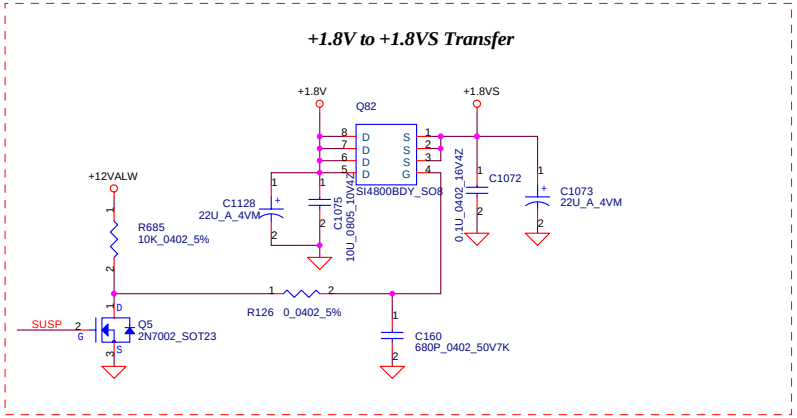
Date: Thursday, July 28, 2005 | Sheet 45 of 60

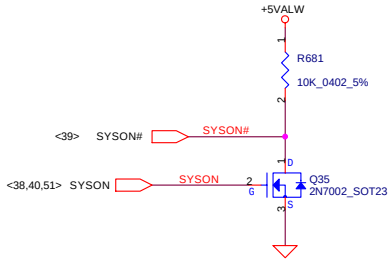


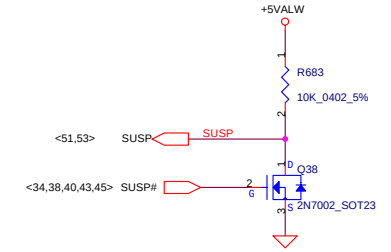


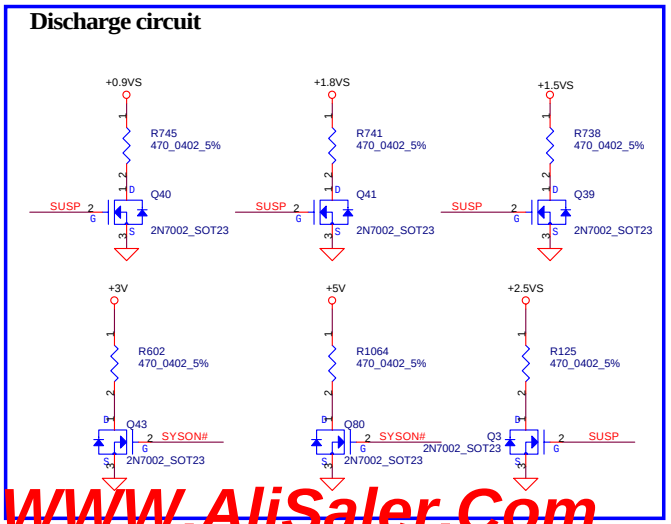












Compal Electronics, Inc.		
Title: DC/DC Circuits		
Size	Document Number: HDL75 LA3041	Rev: 0.1
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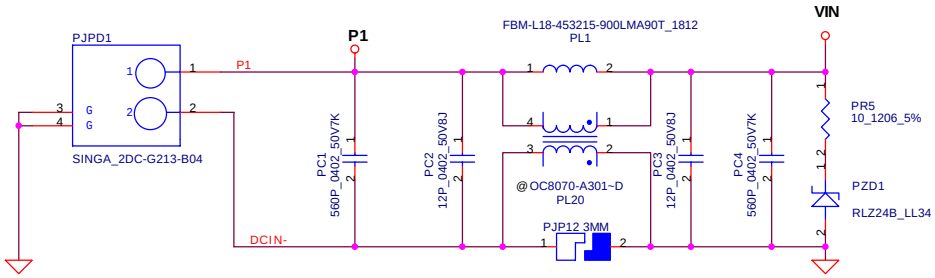
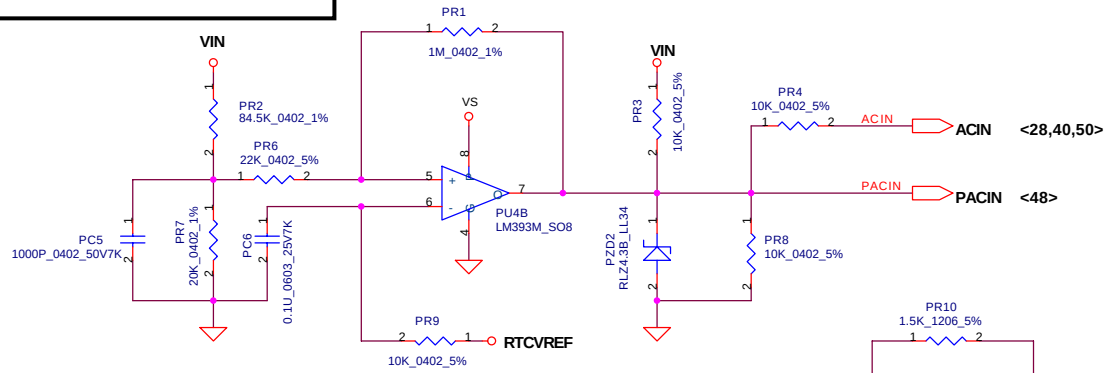
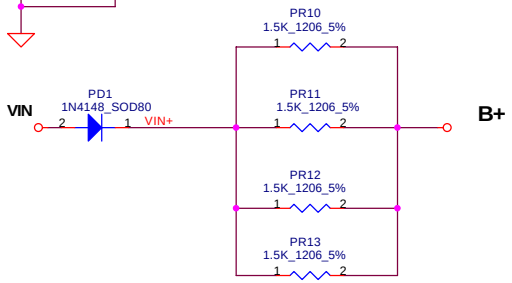
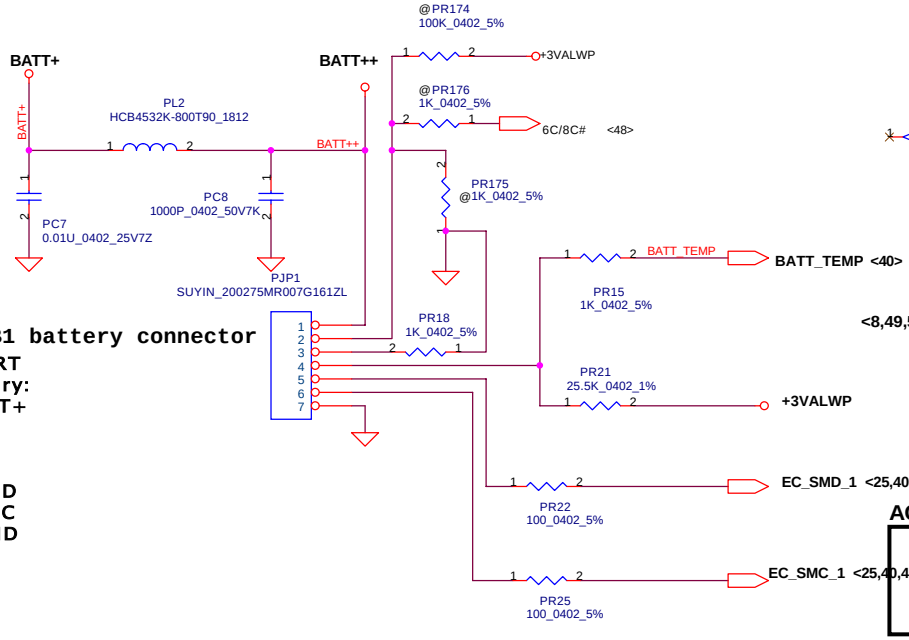
Vin Detector	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V

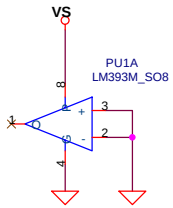








PJPB1 battery connector
SMART Battery:
1.BAT+
2.ID
3.B/I
4.TS
5.SMD
6.SMC
7.GND



ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Compal Electronics, Inc.
Title: DCIN & DETECTOR & Precharge
Size: B
Document Number: EDL75/76 LA-3041
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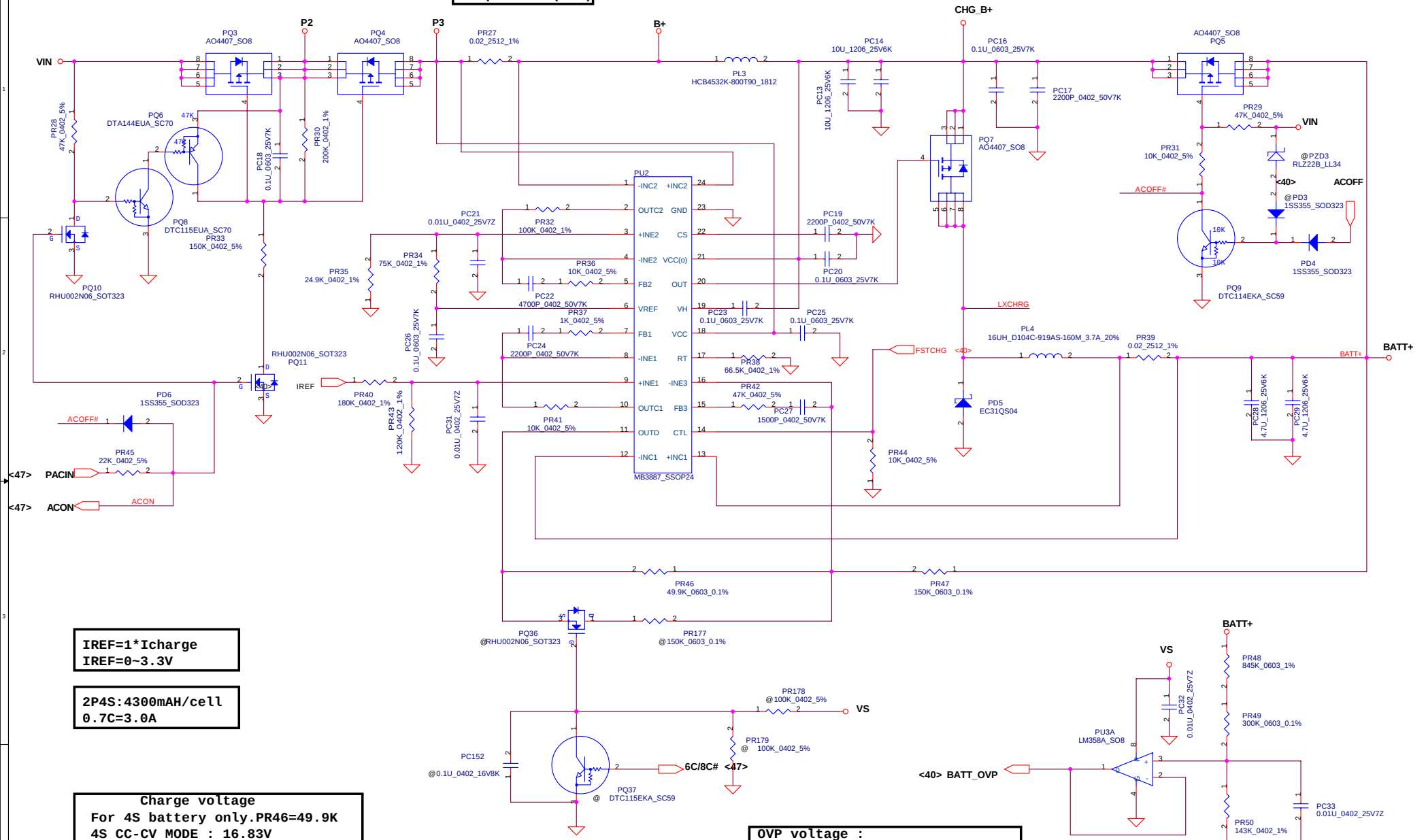
Charger

Iadp=0~2.9A(65W)



IREF=1*Icharge
IREF=0~3.3V

2P4S:4300mAH/cell
0.7C=3.0A

Charge voltage
For 4S battery only.PR46=49.9K
4S CC-CV MODE : 16.83V
For 3S/4S battery.PR46=75K,
PR177=150K,PQ36=2N7002,PR178=100K
PC152=0.1U,PQ37=DTC115EKA
PR174=100,PR176=1K.
4S CC-CV MODE : 16.8V
4S CC-CV MODE : 12.6V

OVP voltage :
LI-4S :18V----BATT-OVP=2V
BATT-OVP=0.111*BATT+

Compal Electronics, Inc.

Title: Charger

Size: B | Document Number: EDL75/76 LA-3041 | Rev: 0.2

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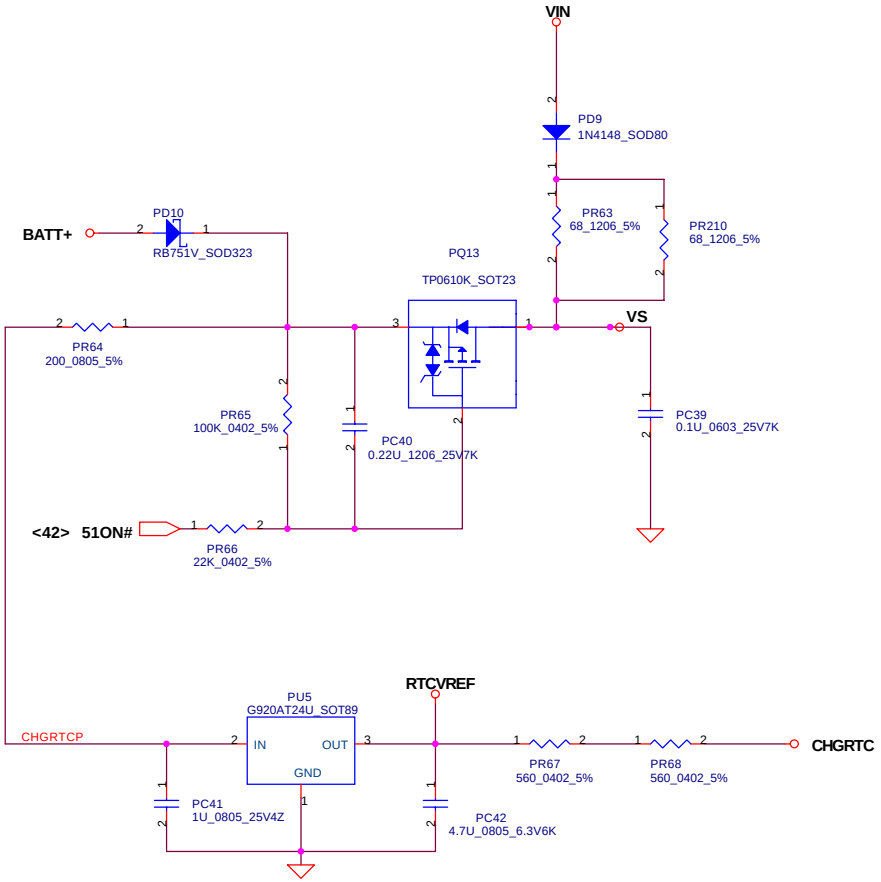
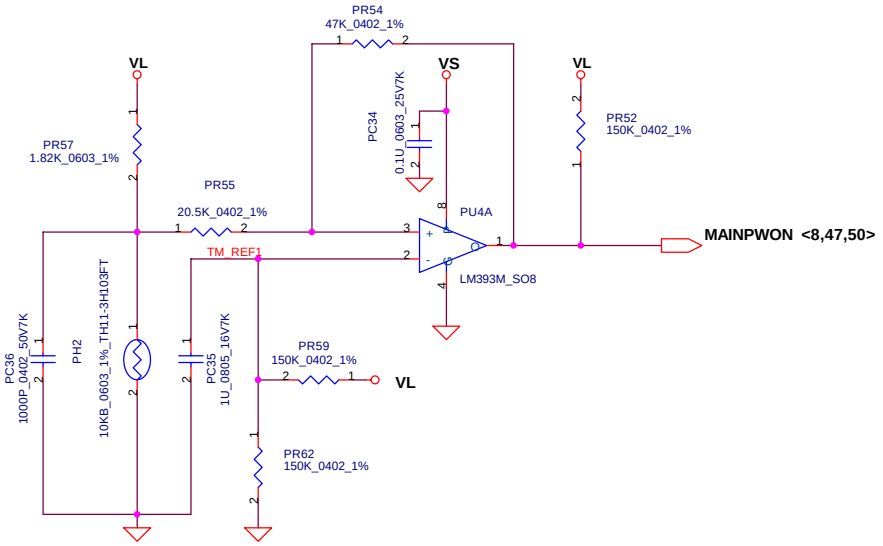


PH2 under CPU botten side :
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C



Compal Electronics, Inc.
Title: RTC Battery & OTP
Size: B
Document Number: EDL75/76 LA-3041
Rev: 0.2
Date: Thursday, July 28, 2005
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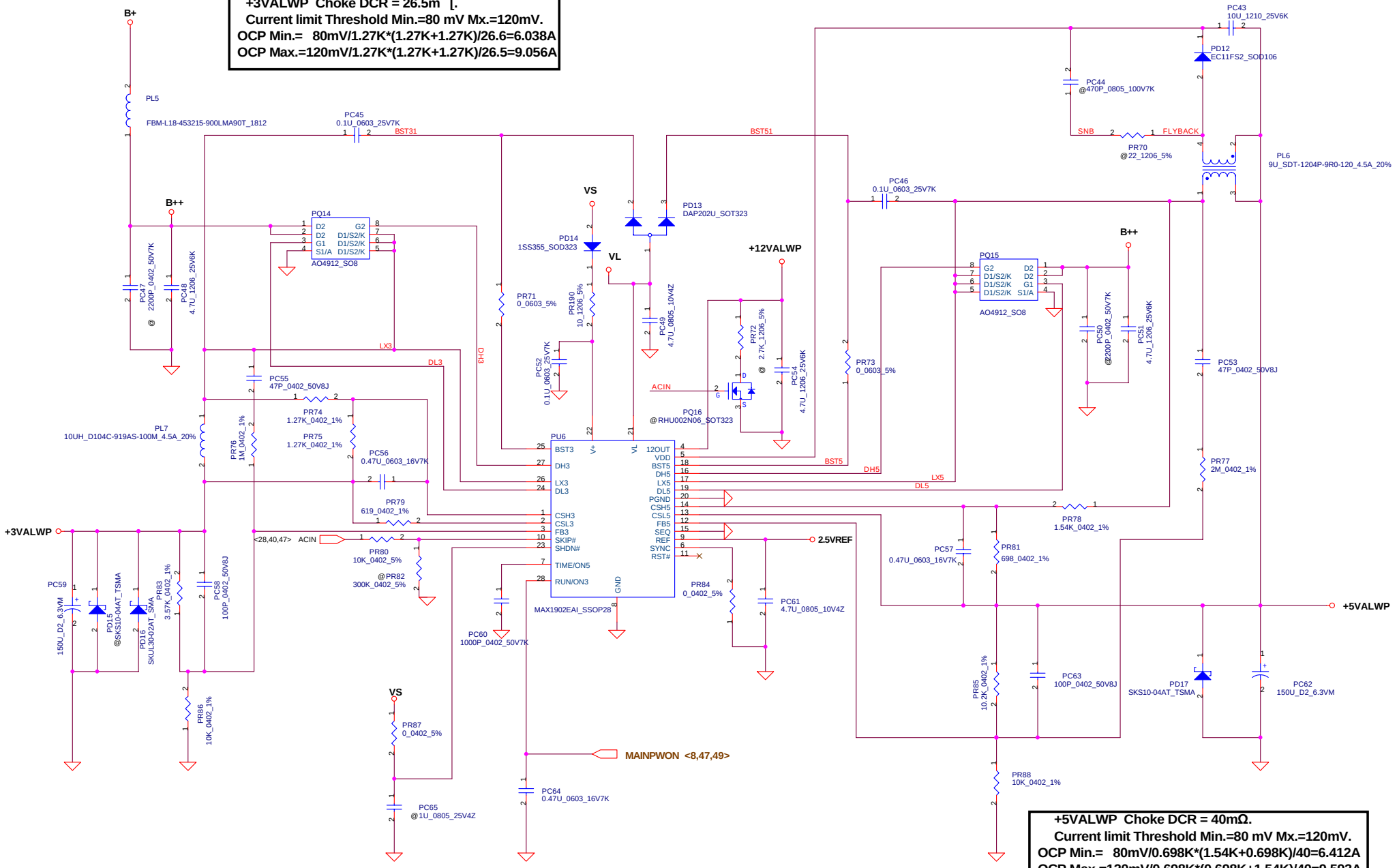
+3.3V/+5V/+12V

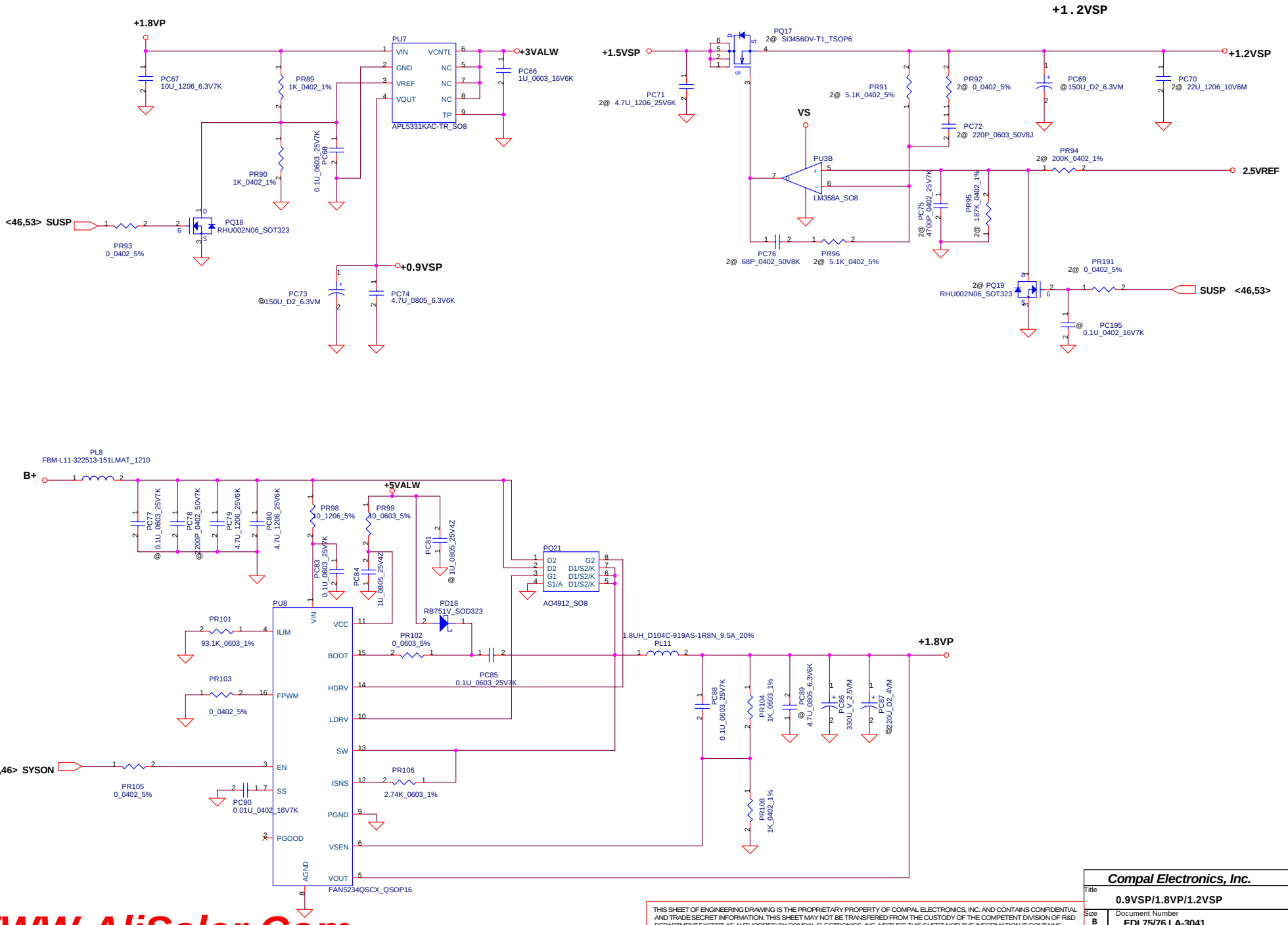
+3VALWP Choke DCR = 26.5m [.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/1.27K*(1.27K+1.27K)/26.6=6.038A
OCP Max.=120mV/1.27K*(1.27K+1.27K)/26.5=9.056A



+5VALWP Choke DCR = 40mΩ.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/0.698K*(1.54K+0.698K)/40=6.412A
OCP Max.=120mV/0.698K*(0.698K+1.54K)/40=9.593A

RS2(PR64)=RS1(PR58)*RS3(PR61)/(RS1+RS3)
L/RL(DCR)=RS1*RS3(PR61)/(RS1+RS3)*Cs(PC56)

Compal Electronics, Inc.		
Title: 3.3V / 5V / 12V		
Size: B	Document Number: EDL75/76 LA-3041	Rev: 0.2
Date: Thursday, July 28, 2005	Sheet 50 of 60	



Compal Electronics, Inc.	
Title	0.9VSP/1.8VP/1.2VSP
Size B	Document Number EDL75/76 LA-3041
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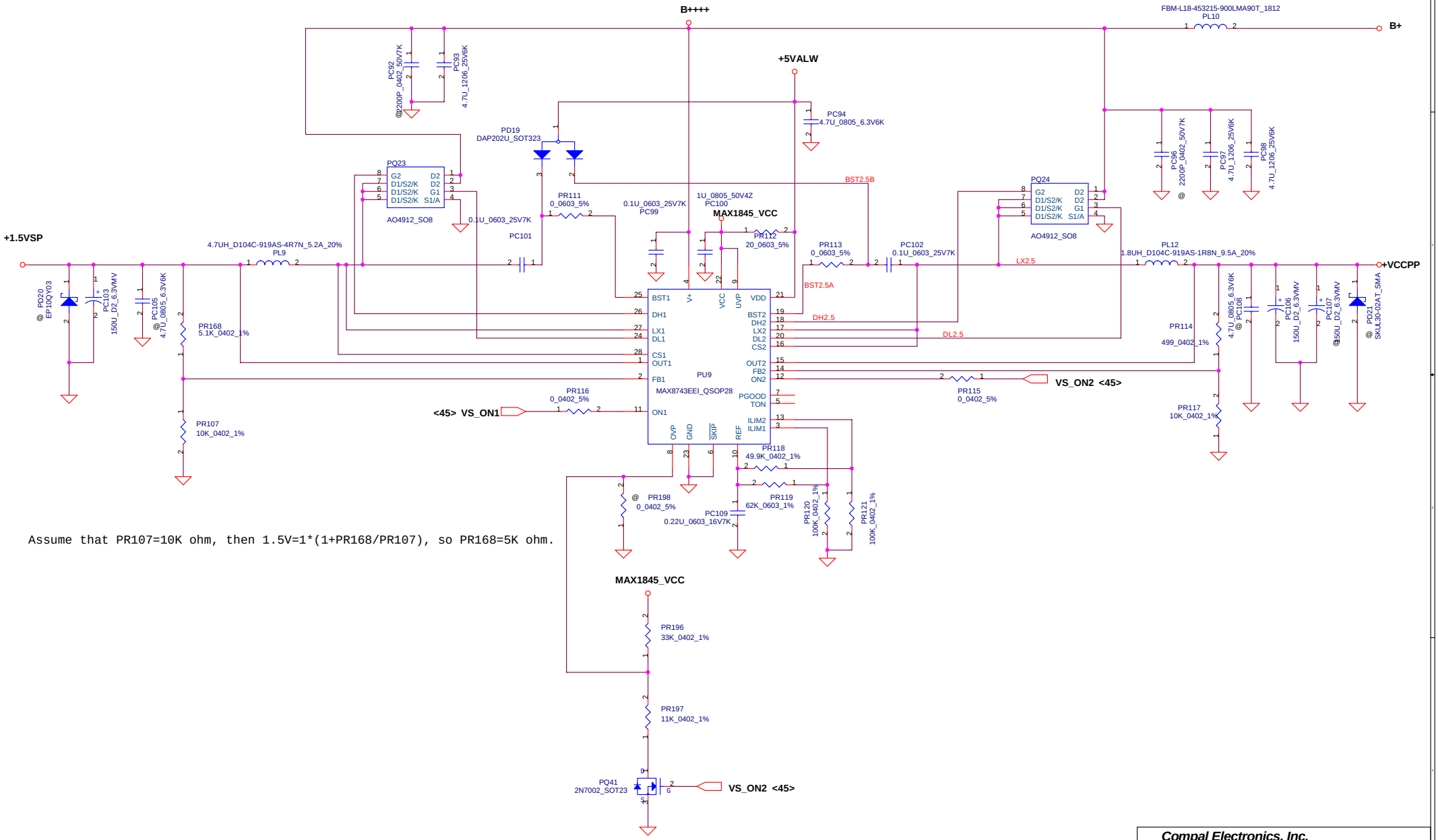

Assume that PR107=10K ohm, then 1.5V=1*(1+PR168/PR107), so PR168=5K ohm.

Compal Electronics, Inc.
Title: +VCCPP & +1.5VSP
Size: B
Document Number: EDL75/76 LA-3041
Rev: 0.2
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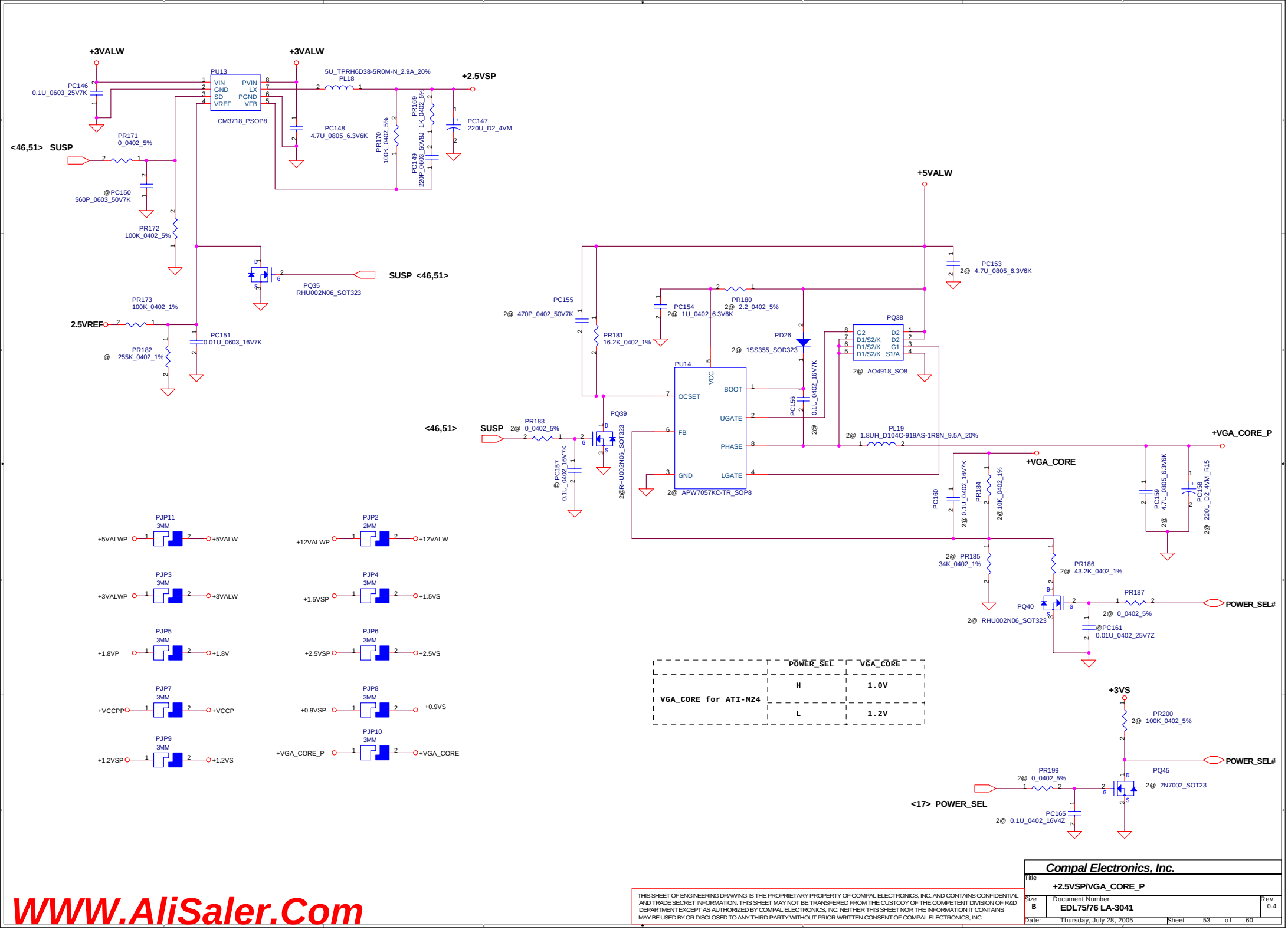

Compal Electronics, Inc.

Title: +2.5VSP/VGA_CORE_P

Size: B | Document Number: EDL75/76 LA-3041 | Rev: 0.4

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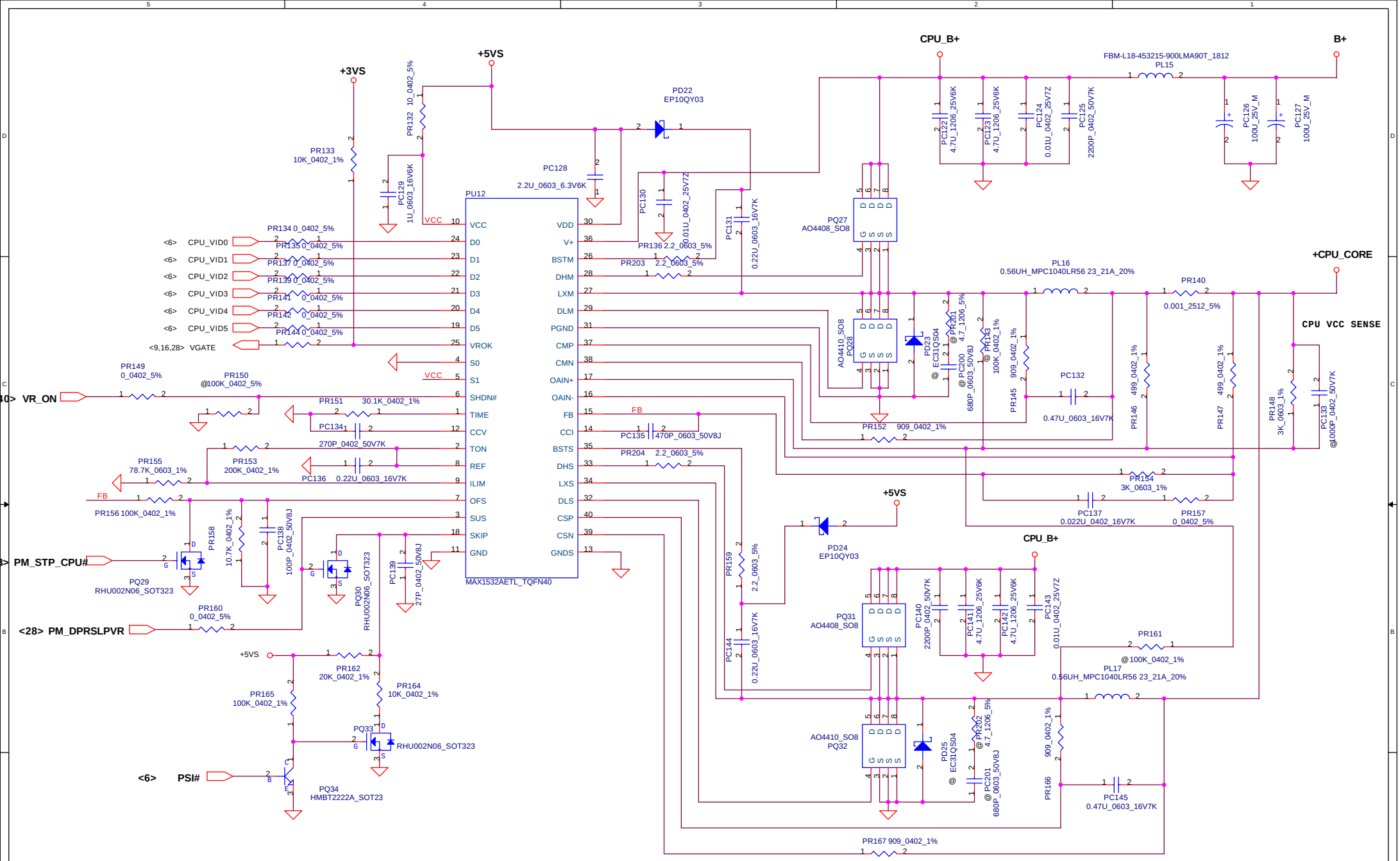

Compal Electronics, Inc.	
Title	+CPU_CORE
Size	B
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Date:	Thursday, July 28, 2005
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Change DDRII to DDRI.	Change DDRII to DDRI.	0.2	54	1.Change PR104 from 1K_0603_1% to 1.8K_0603_1% 2.Change PR106 from 2K_0402_5% to 2.74K_0603_1% 3.Change PR101 from 107K_0402_1% to 93.1K_0603_1%.	0.2	DVT
2	Ripple voltage of +1.2VSP is large	The output voltage is unstable, so increase capacitance to improve it.	0.2	54	1.Change PC70 from 4.7U_1206_25V6K to 22U_1206_10V6M	0.2	DVT
3	Ripple voltage of +VCCPP is large	Ripple voltage is over spec.	0.2	55	Change PC106 from 150U_D2_6.3VM(45m) to 150U_D2_6.3VMV(15m)		
4	+1.5VP is poor supply by using CM3718.	Use MAX1845 to convert +1.5VP	0.2	56	1.Delete PU11 CM3718. 2.Delete PQ26 RHU002N06. 3.Delete PL14 5U_TPRH6D38-5R0M 4.Delete PC113 150U_D_6.3V 5.Delete PC115 4.7U_1206_25V6K. 6.Delete PC111,PC117PC121,PR123,PR125,PR127, PR129,PR130,PR131.	0.2	DVT
5	+1.5VP is poor supply by using CM3718.	Use MAX1845 to convert +1.5VP	0.2	55	1.Delete the PQ22 RHU002N06. 2.Delete PR109 100K_0402_1% 3.Delete the PC91 0.01U_0402_25V7Z 4.Change PR168 from 2K_0402_1% to 5.1K_0402_1%. 5.Change PC103 from 150U_D2_6.3VM(45m) to 150U_D2_6.3VMV(15m) 6.Change PL9 from 1.8UH_D104C-919AS-1R8N to 4.7UH_D104C-919AS-4R7N	0.2	DVT
6	Change +2.5VSP to +1.8VP	Change +2.5VSP to +1.8VP	0.2	56	1.Change PR173 from 10K_0402_1% to 100K_0402_1%. 2..Add PR182 255K_0402_1%.	0.2	DVT
7	For UMA platform can no populate +1.2VSP.	For UMA platform can no populate +1.2VSP.	0.2	54	No populate PC71,PQ17,PR91,PR92,PC72,PR96,PC76,PC70,PR94, PR95,PC75,PQ19,PR97,PQ20,PR100 and PC82.	0.2	DVT
8	For UMA platform can no populate +1.8VSP.	For UMA platform can no populate +1.8VSP.	0.2	55	No populate PU13,PC146,PR171,PR172,PR173,PR182,PC151,PQ35, PL18,PC148,PR170,PR169,PC149 and PC147.	0.2	DVT
9	For charge current accuracy requirement	For charge current accuracy requirement	0.2	50	Change PR43 from 120K_0402_5% to 120K_0402_1%.	0.2	DVT
10	For charge voltage accuracy requirement	For charge voltage accuracy requirement	0.2	50	Change PR46 from 49.9K_0402_1% to 49.9K_0603_0.1%	0.2	DVT
11	Use lower rating capacitors to improve cost down.	Use lower rating capacitors to improve cost down.	0.2	50	1.Change PC42 from 4.7U_1206_25V6K to 4.7U_0805_6.3V6K. 2.Change PC74 from 4.7U_1206_25V6K to 4.7U_0805_6.3V6K. 3.Change PC94 from 4.7U_1206_25V6K to 4.7U_0805_6.3V6K. 4.Change PC148 from 4.7U_1206_25V6K to 4.7U_1206_6.3V6K without populate.	0.2	DVT
12	For pull high to VGATE.	For pull high to VGATE.	0.2	50	Populate PR133 with 10K_0402_1%.	0.2	DVT
13	To avoid inrush current.	To avoid inrush current.	0.2	50	Add PR190 between PD14 pin2 and VS with 10_1206_5%.	0.2	DVT
14	To solve the no load PWM waveform issue.	To solve the no load PWM waveform issue.	0.2	53	Change PC86 from 220U_D2_4VM to 220U_D2_4V_15m.	0.2	DVT
15	To solve the shutdown negtive voltage issue.	To solve the shutdown negtive voltage issue.	0.2	54	Add PQ41(2N7002_SOT23) and PR196(33K_0402_1%) and PR197(11K_0402_1%)	0.2	DVT

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
16	To cost down.	To cost down.	0.2	54	Change Max1845 to Max8743 and remove PD20 and PD21	0.2	DVT
17	To solve Max1902 can locked as adapter plug in and uproot out the electric socket continuous.	To solve Max1902 can locked as adapter plug in and uproot out the electric socket continuous.	0.2	52	Add Precharge circuit.	0.2	DVT
18	Power select action correct	Power select action correct	0.2	55	Add PQ45 and PR199 and PR200 and PC165.	0.2	DVT
19	Increase choke rating of 5VALWP.	Increase choke rating of 5VALWP.	0.3	52	Change PL6 from SH136100020 to SH13690AM00.	0.3	PVT
20	BOM Error of PD2	PD2 shows wrong location PD5 on SAP system, I update it.	0.3	49	Change its location from PD5 to PD2.	0.3	PVT
21	BOM Error of PQ41 and PQ45.	SAP system has quantity but shows no location of PQ41 and PQ45.	0.3	52,55	Update the location of PQ41 and delete PQ45.	0.3	PVT
22	EMI issue.	EMI's request.	0.3	56	Change PR136 and PR159 from SD028000000 to SB028220B00.	0.3	PVT
23	Production EOL.	SB906100109(TP0610T) will go EOL.	0.3	50	Change SB906100109 to SB906100200.	0.3	PVT
24	Time sequence error.	Time sequence is error such that B+ can't biuld.	0.3	51,52	Change PR52 from SD034470200 to SD028150300. Un-populate PC65. Change PR87 from SD028470200 to SD028000000.	0.3	PVT
25	OTP setting adjust.	Because we change PR52 such that OTP needs to reset.	0.3	50	1 Change PR55 from SD034169200 to SD034205200. 2 Change PR57 from SD014215108 to SD014182102.	0.3	PVT
26	Add other circuit of precharge.	Because we need to populate this circuit such that precharge can enable.	0.3	48	1 Add PD1 SC11N4148T8(S DIO 1N4148(SM)). 2 Add PR10 SD0111501T6(S RES 1/4W 1.5K +-5% 1206). 3 Add PR11 SD0111501T6(S RES 1/4W 1.5K +-5% 1206). 4 Add PR12 SD0111501T6(S RES 1/4W 1.5K +-5% 1206). 5 Add PR13 SD0111501T6(S RES 1/4W 1.5K +-5% 1206).	0.3	PVT
27	Un-populate VGA_CORE_P.	Because EDL71 is Aviso GM plate form, we don't populate PQ45, PR199, PR200, PC165.	0.3	54	Delete PQ45, PR199, PR200, PC165.	0.3	PVT
28	Adjust CP point.	Because we need to change CP point to improve CP mode.	0.4	49	Change PR35 from SD034226200 to SD034249200.	0.3	EVT
29	Add PC146 for EDL70.	We need to add PC146 such that Vin can more clear and stable.	0.4	54	Add PC146 for1.8VSP of EDL70.	0.3	EVT
30	To cost down.	To cost down.	0.4	54	Change PC147 from SG020151300 to SGA20221120.	0.3	EVT
31	Precharge circuit tolerance adjust.	Because the tolerance shuld be 1% but the metirial on BOM is 5% so we update it.	0.4	54	Change PR52 from SD028150300 to SD034150300.	0.4	EVT
32	UUT has Zi Zi noice issue.	Because we have UUT zi zi noice issue, we add two capacitor to solve it.	0.4	54	Add PC126 and PC127 with SF10004M008.	54	EVT
33	Noise on S3 mode.	Because we found noise on ceramic capacitor, we increase capacitance to decrease this noise.	0.4	54	Change PC43 from SE142475K00 to SE142106M00.	54	EVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Make PU8 can into skip mode as S3 mode.	Because the power consumption is too high as S3 mode, we found PU8 doesn't into skip mode, we now improve it.	0.4	52	change PU8 from SGA20221150 to SGA20331D20.	0.4	EVT
	Make 1.2VSP start up waveform more smooth	Because we found the start up waveform which has some delay such that the waveform does'nt smooth. We improve it.	0.5	52	Change PC75 from SE074222K00 to SE075472K00.	0.4	PVT
	Make 1.8VSP start up waveform more smooth	Because we found the start up waveform which has some delay such that the waveform does'nt smooth. We improve it.	0.5	54	Change PC151 from SE026223K00 to SE026103K00.	0.4	PVT
	To improve noise issue when system into S3 mode.	Because we found that noise occurs when system into S3 mode, so we need to improve and derease it.	0.5	51	Change PC43 from SE142106M00 to SE065106K00.	0.4	PVT
	To meet EMI request.	To meet EMI request.	0.5	55	Add PR203 and PR204 with SD0130000T4.	0.4	PVT
	For EDL72, Transfer ISPD BOM Error.	BOM error, update to correct value.	0.6	53	Change PR115 from SD028200000(S RES 1/16W 200 +-5% 0402) to SD028000000(S RES 1/16W 0 +- 5% 0402).	0.5	Pre-MP
	For EDL72, Transfer ISPD BOM Error.	BOM error, update to correct value.	0.6	53	Change PR115 from SD028200000(S RES 1/16W 200 +-5% 0402) to SD028000000(S RES 1/16W 0 +- 5% 0402).	0.5	Pre-MP
	For EDL72, Transfer ISPD BOM Error.	BOM error, update to correct value.	0.6	55	Change PC126 from SF06804M000(S ELE CAP 68U 25V M B(6.3*6.0) CV-GX) to SE10004M008(S ELE CAP 100U 25V M B(6.3*7.7) CV-GX).	0.5	Pre-MP
	For EDL72, Transfer ISPD BOM Error.	BOM error, update to correct value.	0.6	55	Change PC127 from SF06804M000(S ELE CAP 68U 25V M B(6.3*6.0) CV-GX) to SE10004M008(S ELE CAP 100U 25V M B(6.3*7.7) CV-GX).	0.5	Pre-MP
	For EDL70_72, change AL to AP material.	Change AL material to AP material.	0.6	55	Change PC124 from SE075103K00(S CER CAP 0.01U 25V K X7R) to SE075103Z00(S CER CAP 0.01U 25V K X7R 0402).	0.5	Pre-MP
	For EDL70_72, change AL to AP material.	Change AL material to AP material.	0.6	55	Change PC143 from SE075103K00(S CER CAP 0.01U 25V K X7R) to SE075103Z00(S CER CAP 0.01U 25V K X7R 0402).	0.5	Pre-MP
	For EDL72, change AL to AP material.	Change AL material to AP material.	0.6	52	Change PC66 from SE135105K00(S CER CAP 1U 16V +-10% X5R 0603) to SE135105KT0(S CER CAP 1U 16V K X5R 0603 TAIYO)	0.5	Pre-MP
	For EDL70_72, change OCP point.	Because EDL70_72 runs 3D Mark2003 will get black screen, we must increase OCP point from 6.8A~11.408A to 10.714A~17.975A.	0.6	54	Change PR181 from SD034806100(S RES 1/16W 8.06K +-1% 0402) to SD034127200(S RES 1/16W 12.7K +-1% 0402).	0.5	Pre-MP
	For EDL72, to meet EMI LGA request.	To meet EMI request and we can cost down.	0.6	54	Delete PR201 and PR202 SD011470BT9(S RES 1/4W 4.7 +-5% 1206).	0.5	Pre-MP
	For EDL72, to meet EMI LGA request.	To meet EMI request and we can cost down.	0.6	54	Delete PC200 and PC201 SE024681J00(S CER CAP 680P 50V J NPO 0603).	0.5	Pre-MP
	For EDL72, to meet EMI LGA request.	To meet EMI request and we can cost down.	0.6	54	Change PR203 and PR204 from SD0130000T4(S RES 1/16W 0 +-5% 0603) to SD013220B00(S RES 1/16W 2.2 +-5% 0603).	0.5	Pre-MP
	For EDL70, delete second source of PL7 and PL4.	Because second source vendor can't sent approve sheet on time, so delete it.	0.6	49	Delete PL4 SH035150000 and PL7 SH035100000.	0.5	Pre-MP
	For EDL71, delete second source of PL7 and PL4.	Because second source vendor can't sent approve sheet on time, so delete it.	0.6	49	Delete PL4 SH035150000 and PL7 SH035100000.	0.5	Pre-MP
	For EDL72, BOM transfer error.	Because BOM of EDL72 of PQ27 and PQ31 show SI4892.It is wrong type for original design.	0.6	54	Change PQ27 from SB54892(S TR SI4892DY 1N SO-8 W/D) to SB544080000(S TR AO4408 1N SO8 W/D).	0.5	Pre-MP
	For EDL72, BOM transfer error.	Because BOM of EDL72 of PQ27 and PQ31 show SI4892.It is wrong type for original design.	0.6	54	Change PQ27 from SB54892(S TR SI4892DY 1N SO-8 W/D) to SB544080000(S TR AO4408 1N SO8 W/D).	0.5	Pre-MP
	For EDL70_71_72, change RTC charing resistor.	Because RTC charge current needs to meet battery spec.	0.6	50	Change PR67 and PR68 from SD028300000(S RES 1/16W 300 +-5% 0402) to SD028560000(S RES 1/16W 560 +-5% 0402)	0.5	Pre-MP
	For EDL70_72, change VGA_COREP's voltage.	Because system runs 3D mark and QuakeIII will hang up, we increase the VGA_COREP's voltage level from 1.2V to 1.221V.	0.6	54	Change PR185 from SD034402200(S RES 1/16W 40.2k +-1% 0402) to SD034340200(S RES 1/16W 34K +-1% 0402).	0.5	Pre-MP
4	For EDL70_72, change VGA_COREP's voltage.	Because system runs 3D mark and QuakeIII will hang up, we increase the VGA_COREP's voltage level from 1.2V to 1.221V.	0.6	54	Change PR185 from SD034402200(S RES 1/16W 40.2k +-1% 0402) to SD034340200(S RES 1/16W 34K +-1% 0402).	0.5	Pre-MP

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	For EDL70_72, solve black screen issue.	Because EDL70_72 still has black screen pheonomeon. We increase it to 15.692A.	0.7	54	Change PR181 from SD034127200(S RES 1/16W 12.7K 0402 +-1%) to SD034162200(S RES 1/16W 16.2K +-1% 0402).	0.5	MP
2	For EDL70_72, solve 3D Mark hang up issue.	Because EDL70_72 runs 3D Mark will hang at 美人頭. We need to solve it.	0.7	54	Change PC154 from SE076104K00(S CER CAP 0.1U 16V K X7R 0402) to SE000000K00(S CER CAP 1U 6.3V K X5R 0402)	0.5	MP
3	For EDL70_72, solve 3D Mark hang up issue.	Because EDL70_72 runs 3D Mark will hang at 美人頭. We need to solve it.	0.7	54	Change PQ38 from SB549120000(S TR AO4912 2N SO8 W/D) to SB000003G00(S TR AO4918 2N SO8).	0.5	MP

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	S4 auto resume	Can't auto resume from S4	0.4	30	Change VCCSUS3_3 from +3V to +3VALW	0.5	PVT
2	C615 short	C615 short to logic low cause can't boot	0.4	35	Change C613 and C615 to SGN01220100	0.5	PVT
3	bo niose when shut down	speaker generate "bo" niose when system shut down	0.4	45	Change R460 to R461	0.5	PVT
4	C904 too close to JP12	C904 too close to JP12 if C904 fail can't repair	0.4	40	JP12 change to DC233104020	0.5	PVT
5	+1.5V rising edge	+1.5V 's rising edge is not smooth	0.4	30	Add R12	0.5	PVT
6	SW DJ can't play with Hitach HDD	Hitachi HDD send IDE_DIOR# in SW DJ S0 mode	0.4	31,46	Add Q97, R1197, R1198	0.5	PVT
7	Modem noise	Modem dial tone have noise	0.4	39	Change R518, R521 from SD0130000T4 to SM010012000	0.5	PVT
8	KB910 damage issue	KB910 INVT_PWM pin damage issue	0.5	41	Add D32,D33	0.6	PVT
9	S4 auto resume	Can't auto resume from S4	0.5	29,30	Change +3V to +3VALW for SMBUS and LINKALERT#, EC_SMI#, SYS_RESET# PM_BATLOW#, GPI11, ICH_PCIE_WAKE# 1.5V LDO	0.6	PVT
10	Bo noise	Bo noise gernerate in SWDJ mode and power up	0.5	45	Del R460 and R461, add D35 and D36	0.6	PVT
11	Backlight issue	backlight timing error	0.5	24	Add D34 and R1118	0.6	PVT
12	Sighting Alert	Alviso SMVREF Sighting Alert (# 68363)	0.5	9	No stuff R100 and R101	0.6	PVT
13	CRT ISSUE	CRT NOISE issue	0.5	12	Change C119 from SE053106Z00 to SE077226M10	0.6	PVT
14	SWDJ issue	SWDJ can't play	0.5	46	Add Q98	0.6	PVT
15	USB OC	Add USB OC delay circuit	0.5	40	Add R1201,R1202,R1203,R1204,R1205, R1206,C1134,C1135,C1136	0.6	PVT
16	SVIDEO ISSUE	SVIDEO out noise issue	0.5	12	Change C92 from SE107475M00 to SE077226M10	0.6	PVT
17	TV TUNNER	No sound in IOMP mode	0.5	38	ADD TV_AUDIO_R and TV_AUDIO_L	0.6	PVT
18	Power sequence	Power sequence	0.5	47	Add C172 for EDL70 power sequence	0.6	PVT
19	LCD Power sequence for EDL70/72	Power off white screen issue	1.0	24	Add 1@ on R1118 and D34	1.1	PVT
20	ESD	Add ESD diode for USB data and EC INVT_PWM pin	1.0	40, 41	Add U70, D38, D39 and D40	1.1	PVT

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
21	VGA_CORE over spec	VGA_CORE drop over 1.14V	1A	30	Change C212 to 470uF Cap	1B	MP
22	IDE IOR ISSUE	Data mismatch or Data lose issue	1B	46	Add C144, U71, R28, R1210, R42, R43, R77, No stuff R1200	1C	MP
23	LGA over spec	FIX LGA over spec	1B	31	Add C154, C155, C156, C157	1C	MP