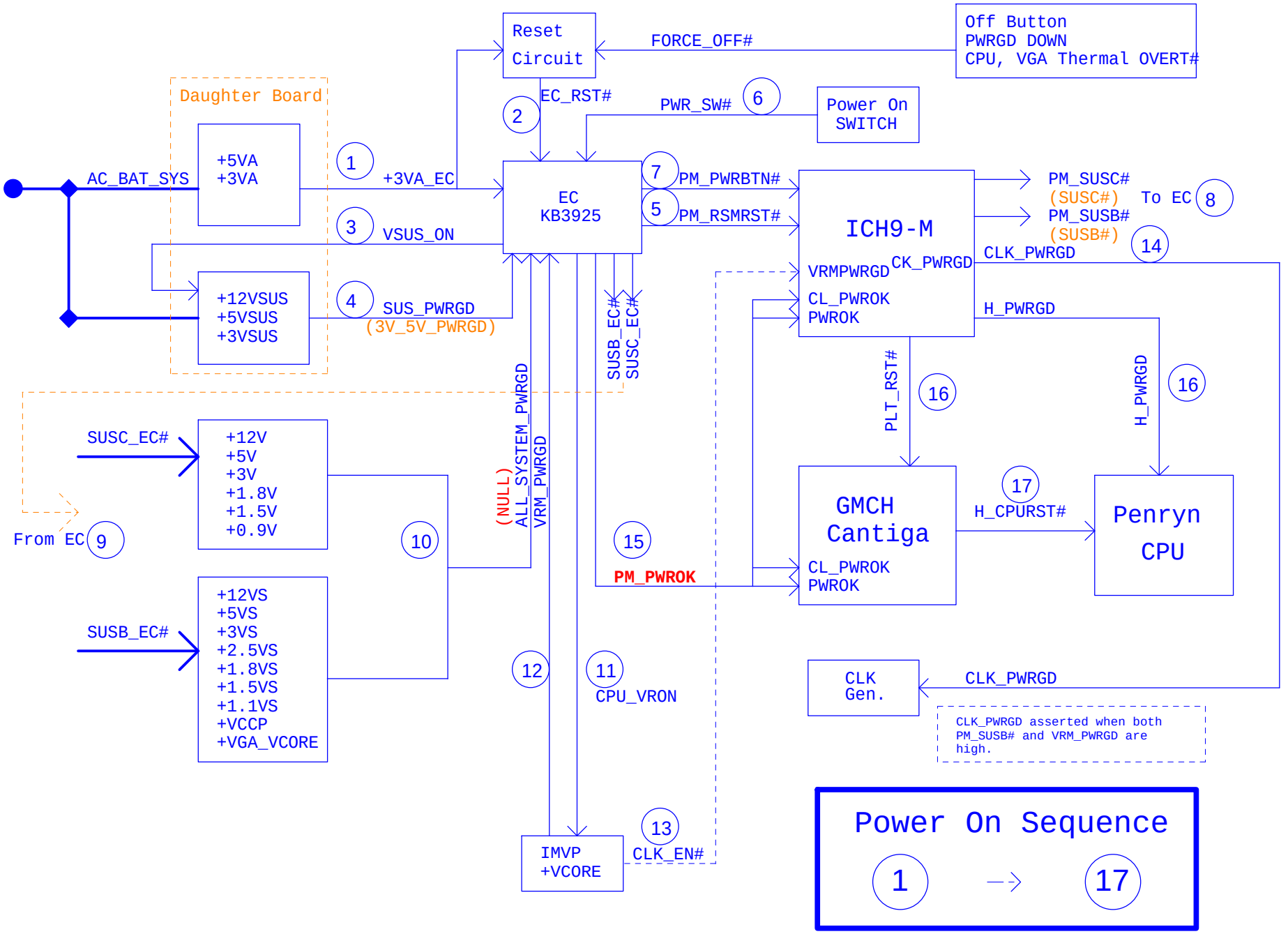
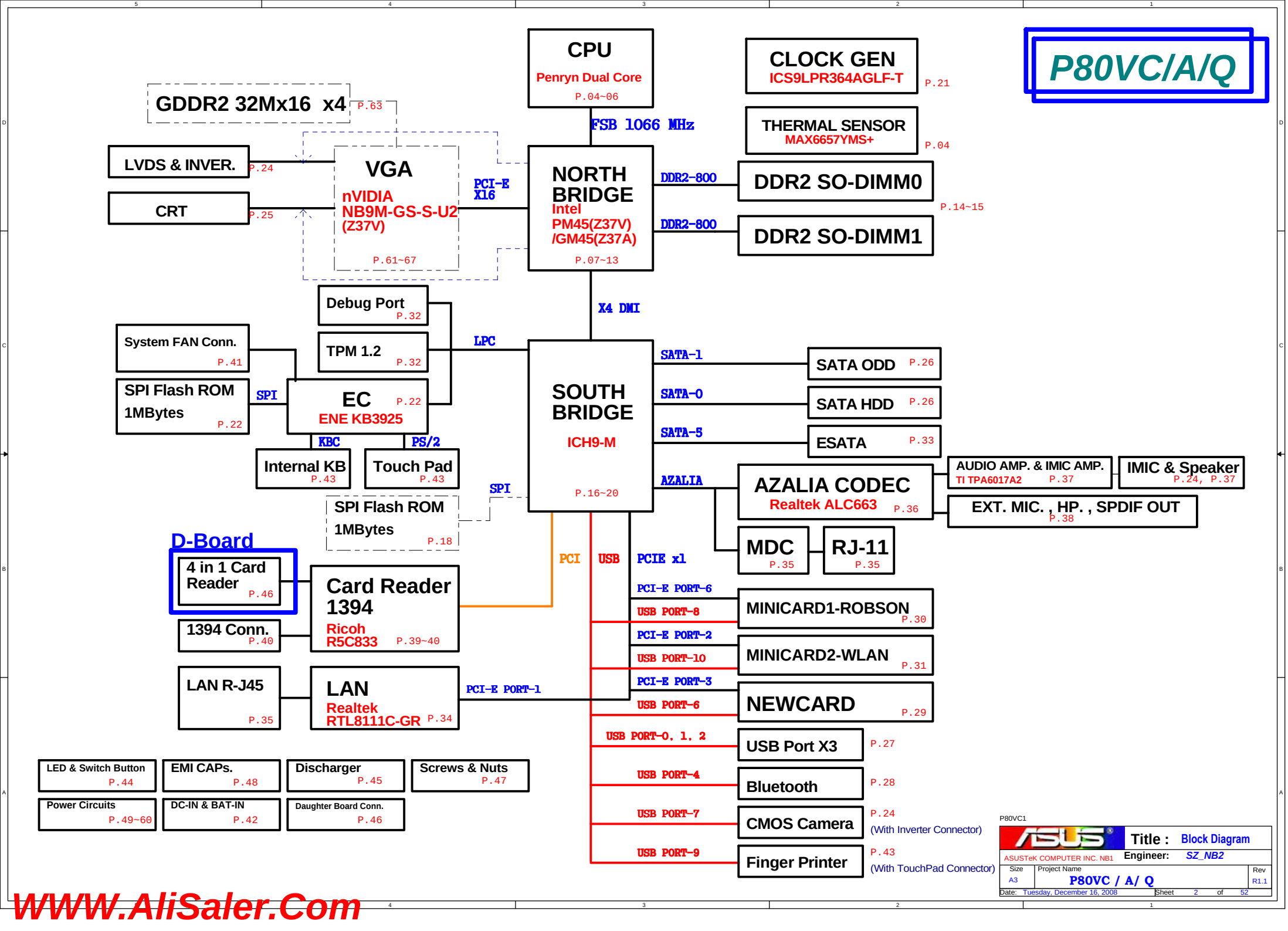


P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Power-On Sequence	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 1 of 52	



Z37V/A Schematic Index

Page	System page Ref.
01	Block Diagram
02	Schematic Information
03-05	CPU-Penryn
07-09	DDR II SO-DIMM
10-15	Cantiga
20-24	ICH9M
25	SPI ROM
29	CLK-ICS9LPR363CGLF-T
30-31	EC_IT8752
32	POWER-ON SEQUENCE
33	Realtek RTL8111C
34	RJ45 + RJ11
35	MDC
36	ALC663 Codec
37	AUDIO_G1431 & HP
38	MICROPHONE & Array MIC
~~39~~	~~FM2010 DSP~~
40	CARDBUS R5C833(PCI I/F)
41	CARDBUS R5C833(1394 & SD)
42	IEEE1394A & 4 IN1 CON
43	NewCard PWR SW & CON
44	Debug
45	LVDS & INVERTER CONNECTOR
46	CRT
48	HDMI
50	THER SENSOR & FAN
51	HDD & CDROM
52	USB Port x 4
53	MINICARD(Ebron/Robson/3G/TV)
~~54~~	~~PORT Docking~~
~~55~~	~~Super I/O & FIR~~
56	LED/TP/SW
57	DISCHARGE
58	UMB
60	DC power jack, Batter conn.
61	Blue Tooth
62	TPM
63	Finger Print
65	MDC NUT & Hinksink NUT
66	E-SATA
68	XDP
70-77	VGA (nVidia NB9P-GE)
80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.5V & 1.05VM
83	POWER_I/O_DDR & VTT
84	NONE
85	POWER_VGA_VCORE & 1.1VO
88	POWER_CHARGER
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

INT PU*: PU or PD in special time

GPIO33 Internal Pull High, Go Low= Flash Descriptor Security will be overriden

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	Native	PMSYNC#	+3VS
GPIO 01	GPI	- EXT PU to +3VS	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+5VS
GPIO 06	GPI	WLBT_SW# EXT PU	+3VS
GPIO 07	GPI	-	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN EXT PD	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	SMBALERT# EXT PU	+3VSUS
GPIO 12	GPI	EXT_SCI# EXT PU	+3VSUS
GPIO 13	GPI	-	+3VSUS
GPIO 14	Native	AC_PRESENT EXT PU	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	-	+3VS
GPIO 18	GPO	GPU_PWR_SB EXT PU NS	+3VS
GPIO 19	GPO	BT_LED EXT PU NS	+3VS
GPIO 20	GPO	GPU_RST_SB# EXT PU NS	+3VS
GPIO 21	GPO	WLAN_LED EXT PU NS	+3VS
GPIO 22	GPI	ODC# EXT PU	+3VS
GPIO 23	Native	LPC_LDRQ1# INT PU*	+3VS
GPIO 24	GPO	-	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	-	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5# EXT PU	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7# EXT PU	+3VSUS
GPIO 32	GPO	PM_CLKRUN# EXT PU	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPO	WLAN_ON EXT PU NS	+3VS
GPIO 37	GPO	BT_ON EXT PU NS	+3VS
GPIO 38	GPI	-	+3VS
GPIO 39	GPO	CLK_PWRSAVE# EXT PU	+3VS
GPIO 40	Native	USB_CON_OC01#	+3VSUS
GPIO 41	Native	USB_CON_OC2#	+3VSUS
GPIO 42	Native	USB_OC3# EXT PU	+3VSUS
GPIO 43	Native	USB_OC4# EXT PU	+3VSUS
GPIO 44	Native	USB_OC8# EXT PU	+3VSUS
GPIO 45	Native	USB_OC9# EXT PU	+3VSUS
GPIO 46	Native	USB_OC10# EXT PU	+3VSUS
GPIO 47	Native	USB_OC11# EXT PU	+3VSUS
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	- INT PU* EXT PU to +3VS	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU* EXT PU to +3VS	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU* EXT PU to +3VS	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_CON_OC01#	+3VSUS
GPIO 60	Native	PM_LINKALERT# EXT PU	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPIO02	GPO	PM_RSMRST#	
GPIO03	GPO	LCD_BACKOFF#	
GPIO04	GPI	EMAIL_SW#	
GPIO06	-	-	
GPIO07	-	-	
GPIO08	GPO	EXT_SMI#	
GPIO09	-	-	
GPIO0A	GPI	LID_EC#	
GPIO0B			
GPIO0C			
GPIO0D	GPI	DISTP_SW#	
GPIO11	GPO		
GPIO18			
GPIO19			

EC GPIO	Use As	Signal Name	Power

P80VC1

ASUSTeK COMPUTER INC. NB1

Title : System Information

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 3 of 52

R1.1 KL99 FOR P80Q
R1.1 KL1 FOR P80VC/A

+3V KL99 120Ohm/100Mhz /woAMT

+3VM /AMT KL1 120Ohm/100Mhz KC7 Do Not Stuff /X

+3VS_CLK KC8 10UF/6.3V KC9 0.1UF/10V KC10 0.1UF/10V KC11 0.1UF/10V KC12 0.1UF/10V KC30 0.1UF/10V KC31 0.1UF/10V

+3VS_CLKA KL3 120Ohm/100Mhz KC2 0.1UF/10V

GND

+1.5VS KL2 120Ohm/100Mhz KC1 Do Not Stuff /X

+1.5VS_CLK KC3 10UF/6.3V KC4 0.1UF/10V KC6 0.1UF/10V

R1.1

KR1 Do Not Stuff

KX1 14.318Mhz +/-30ppm/20PF H = 1.2mm XIN_CLK XOUT_CLK KC13 30PF/50V KC14 30PF/50V

GND

Tuning Cap. @ device sides

KC24 Do Not StuffX CLK_27M_GPU
KC25 Do Not StuffX CLK_27M_GPU_SS
KC18 Do Not StuffX CLK_48M_SB
KC22 Do Not StuffX CLK_33M_TPM
KC23 Do Not StuffX CLK_33M_EC
KC19 Do Not StuffX CLK_33M_SB
KC20 Do Not StuffX CLK_33M_DBG2
KC17 Do Not StuffX CLK_14M_ICH

GND

Close the end of devices

Close to CLK GEN

SMB_CLK_M
SMB_DAT_M

KC15 Do Not Stuff /X
KC16 Do Not Stuff /X

GND

+3VS_CLKA +1.5VS_CLK +3VS_CLK

KU1

VDDSRC_1 VDDSRC_IO1 VDDSRC_IO2 VDDPCI_1 VDDPCI_2 VDD4B VDDREF

FUC → **FUC

To ICH9 GPIO45

VDDCPU VDDA GNDA

XIN_CLK → X1
XOUT_CLK → X2

R1.1

CLK_100M_LVDS 33Ohm /GM 2 KRN8A
CLK_27M_GPU 33Ohm 2 KRN11A /PM
CLK_27M_FIX → 27MHZ/LCD_SSCG/SRC-0

CLK_100M_LVDS# 33Ohm /GM 4 KRN8B
CLK_27M_GPU_SS 33Ohm 4 KRN11B /PM
CLK_27M_SS → 27MHZSS/LCD_SSCG#/SRC-0#

CLK_48M_CR KR29 33Ohm
CLK_48M_SB KR17 33Ohm CLK_48M → **FSLA/USB_48MHz

FSLA

CLK_48M_SB,CLK_48M_CR layout 時 trace 長度相等

FSLB → **FSLB/TEST_MODE

LCDCK_SEL → *SELSRC0_LCD#/PCI-3

CLK_33M_TPM KR32 33Ohm CLK_33M2 → PCI-2

PCI-1

CLK_33M_DBG2 KR26 33Ohm REQ_SEL# → **PCI-0/REQ_SEL

SEL_27M#
CLK_33M_SB KR27 33Ohm CLK_33M_F1 → *SELLCD_27#/PCIF-1

EN_ITPCLK
CLK_33M_EC KR28 33Ohm CLK_33M_F0 → **ITP_EN/PCIF-0

SMB_CLK_M → SCLK
SMB_DAT_M → SDATA
FOC → **FOC

To ICH9 GPIO44

GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7

RTM875T-336-GRT

*INT-PU 120K ohm
**INT-PD 120K ohm.

PEREQ1# for SATA,SRC-0, SRC-6(LAN:PCIE6)
PEREQ2# for SRC-1, SRC-8(NC)
PEREQ3# for SRC-2,SRC-4(WLAN PCIE4)
PEREQ4# for SRC-3,SRC-5, SRC-7(NEWCARD PCIE5)

**PCI_SRC_STOP# → STP_PCI#
**CPU_STOP# → STP_CPU#

CPU-1 CPUCLK1 33OHM 2 KRN1A → CLK_MCH_BCLK
CPU-1# CPUCLK1# 33OHM 4 KRN1B → CLK_MCH_BCLK#

CPU-0 CPUCLK0 33OHM 2 KRN14A → CLK_CPU_BCLK
CPU-0# CPUCLK0# 33OHM 4 KRN14B → CLK_CPU_BCLK#

CPUITP/SRC-8 CPUCLK2 33OHM 2 KRN3A → CLK_XDP_BCLK
CPUITP#/SRC-8# CPUCLK2# 33OHM 4 KRN3B /ITP → CLK_XDP_BCLK#

*SRC_REQ1#/SRC-7 → LAN_CLKREQ#
*SRC_REQ2#/SRC-7# → MCH_CLKREQ#

R1.1 Remove 0ohm

SRC-6 CLK_PCIE6 33OHM 2 KRN2A → CLK_PCIE_LAN
SRC-6# CLK_PCIE6# 33OHM 4 KRN2B → CLK_PCIE_LAN#

SRC-5 CLK_PCIE5 33OHM 2 KRN6A → CLK_100M_NEW
SRC-5# CLK_PCIE5# 33OHM 4 KRN6B → CLK_100M_NEW#

SRC-4 CLK_PCIE4 33OHM 4 KRN13B → CLK_100M_MIN1
SRC-4# CLK_PCIE4# 33OHM 2 KRN13A → CLK_100M_MIN1#

SRC-3 CLK_PCIE3 33OHM 4 KRN9B → CLK_PCIE_GPU
SRC-3# CLK_PCIE3# 33OHM 2 KRN9A /PM → CLK_PCIE_GPU#

SRC-2 CLK_PCIE2 33OHM 4 KRN15B → CLK_PCIE_ICH
SRC-2# CLK_PCIE2# 33OHM 2 KRN15A → CLK_PCIE_ICH#

SRC-1 CLK_PCIE1 33OHM 4 KRN7B → CLK_PCIE_NB
SRC-1# CLK_PCIE1# 33OHM 2 KRN7A → CLK_PCIE_NB#

SATA CLK_SATA 33OHM 4 KRN16B → CLK_SATA_SB
SATA# CLK_SATA# 33OHM 2 KRN16A → CLK_SATA_SB#

SRC-9/DOT96 CLK_96M 33OHM 4 KRN10B → CLK_96M_NB
SRC-9#/DOT96# CLK_96M# 33OHM 2 KRN10A /GM → CLK_96M_NB#

R1.1

*SRC_REQ3# → WLAN_CLKREQ#
*SRC_REQ4# → NEW_CLKREQ#

**VtPWR_GD/PD# CLK_PWRGD KR35 0Ohm → SB_CLKPWRGD
KR36 Do Not Stuff /X → EC_CLKPWRGD

**REF-1/FSLC/TEST_SEL FSLC
REF-0 REF0 KR24 33Ohm → CLK_14M_ICH

FSB Freq. Strap

FSC	FSB	FSA	CPU
0	0	0	266
0	0	1	133
0	1	0	200
0	1	1	166
1	0	0	333
1	0	1	100
1	1	0	400
1	1	1	200

FSLA KR5 10KOhm → CPU_BSEL0
FSLB KR6 10KOhm → CPU_BSEL1
FSLC KR7 10KOhm → CPU_BSEL2

LCDCK_SEL	SEL_27M#				
PIN 5 (IPU)	PIN 9 (IPU)	PIN14, 15	PIN17	PIN18	
0	0	SRC-9	27FIX	27SS	
0	1	DOT96	DOT96SS	DOT96SS	
1	0	DOT96	27FIX	27SS	/PM
1	1	DOT96	SRC-0	SRC-0	/GM

R1.1 +3VS_CLK KR33 10KOhm /GM
SEL_27M# KR8 10KOhm /PM GND

R1.1 +3VS_CLK KR34 10KOhm
LCDCK_SEL KR9 Do Not Stuff GND

PIN 8 ITP_EN/PCIF-0
Select PIN43, 44 as CPUITP or SRC8

R1.1 +3VS_CLK KR20 10KOhm
EN_ITPCLK KR10 Do Not Stuff GND

0 :SRC8
1 :CPUITP

PIN 64 (IPD)PCI-0/REQ_SEL
Select PIN40, 41 as SRC_REQ# or SRC7

R1.1 +3VS_CLK KR15 10KOhm
REQ_SEL#

0 :SRC-7
1 :SRC_REQ#

P80VC1

Title : Main Clock-1
ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2
Size A2 | Project Name P80VC / A/ Q | Rev R1.1
Date: Tuesday, December 16, 2008 Sheet 4 of 52

CPU1A

SOCKET478B

12G010594786

CPU1B

SOCKET478B

12G010594786

AC mode : check PWRLIMT#
DC mode : check battery OTP / OCP

R1.1
Remove THRO_CPU from EC

Zo=55 Ohm, 0.5" max for GTL_REF

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1 degree

CPU Thermal Sensor

HU1

MAX6657YMS+

Place close to CPU Pin
Max: 1mA

ITP

BTOB_CON_31P
/ITP

12G161300310

Stuff when use ITP : HR12, HR13, HR14, HR17, HR18, HR19, HR20, HR21, HR22, HR23, HR24, KRN3

HR12, HR13, HR30, HR31 Place close to CPU

Route H_THERMDA and H_THERMDC in the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

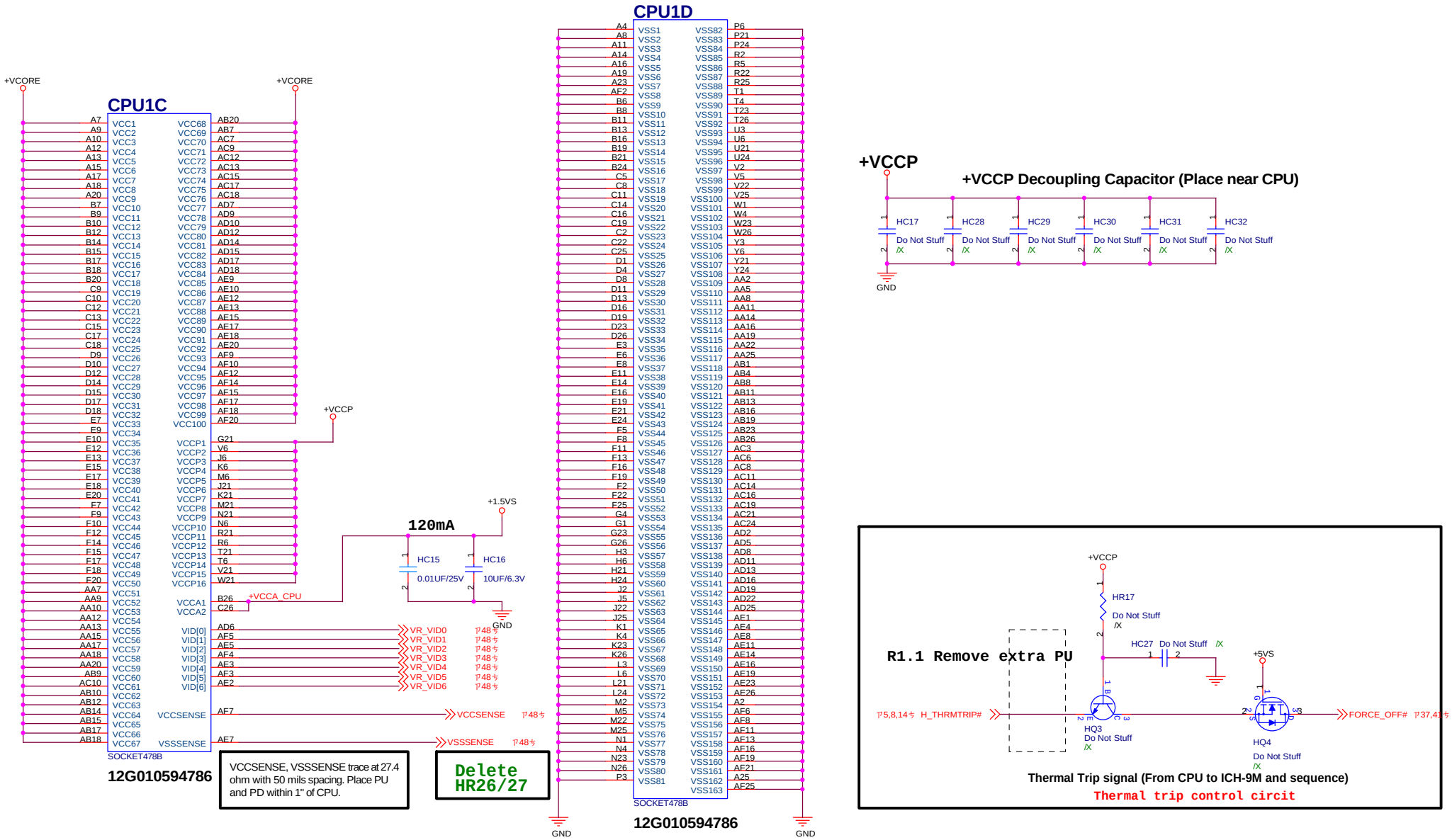
P80VC1

Title : CPU-Penryn (1)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 5 of 52



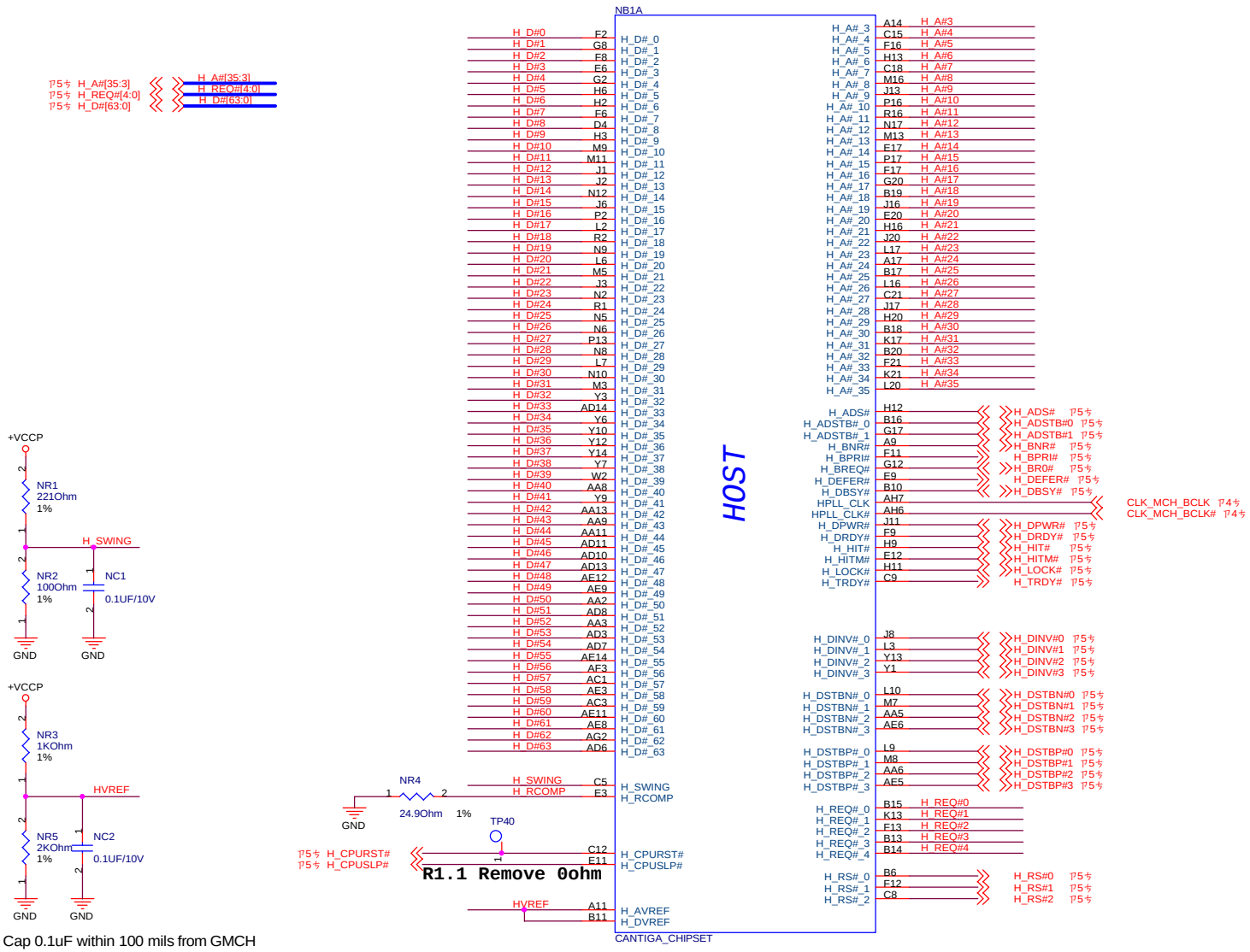
P80VC1

Title : CPU-Penryn (2)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 6 of 52



Cap 0.1uF within 100 mils from GMCH

BOM:
GM45:02G010020030
PM45:02G010022520
GL40:02G010023900
or 02G010017532

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - CPU(1)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 7 of 52	

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

CFG9 : PCIE GRAPHIC LANE

HIGH = Normal Operation (Default)

LOW = Reverse Lanes

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

CFG19 : DMI Lane Reversal

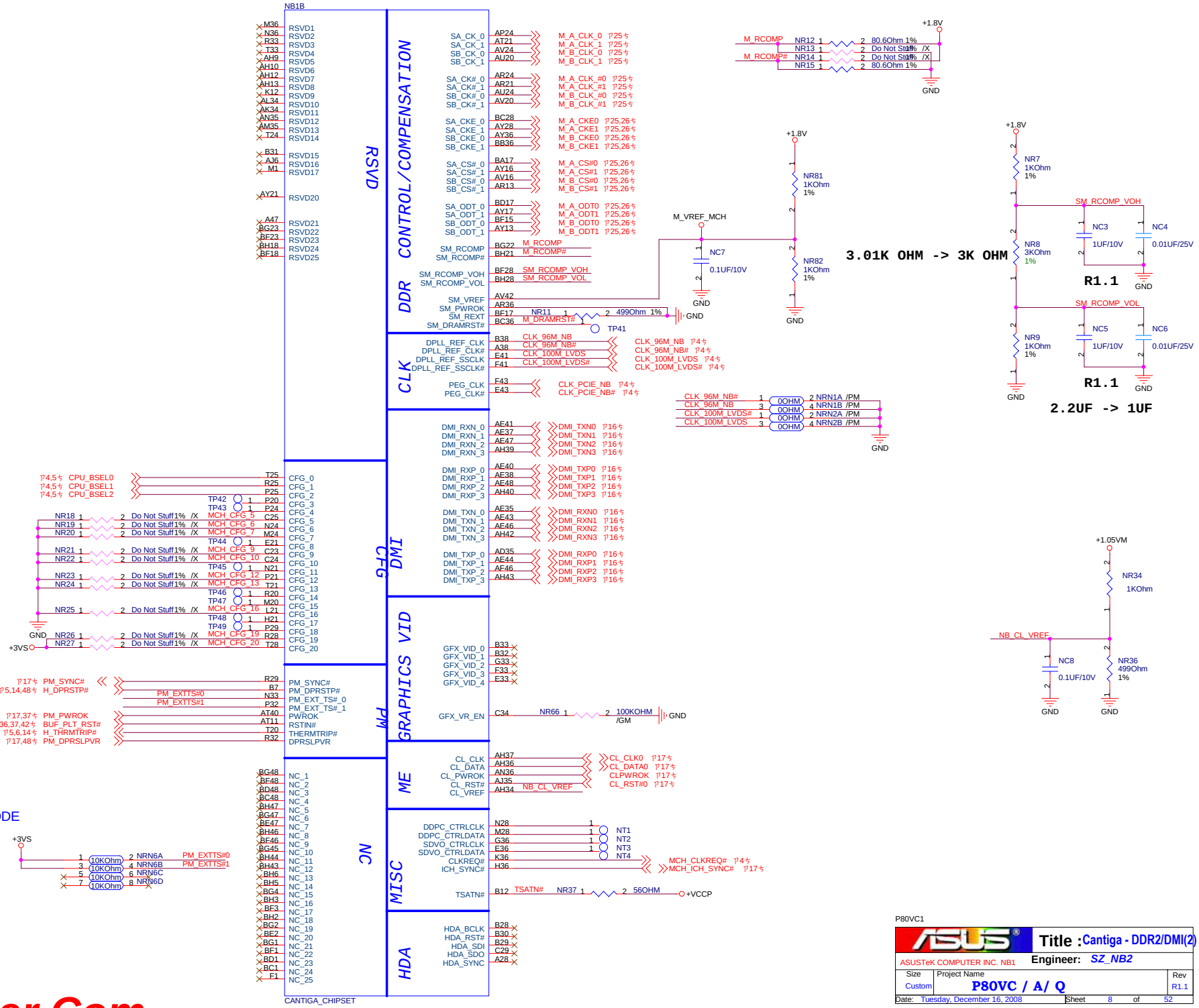
LOW = NORMAL (default)

HIGH = Reverse Lanes

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port



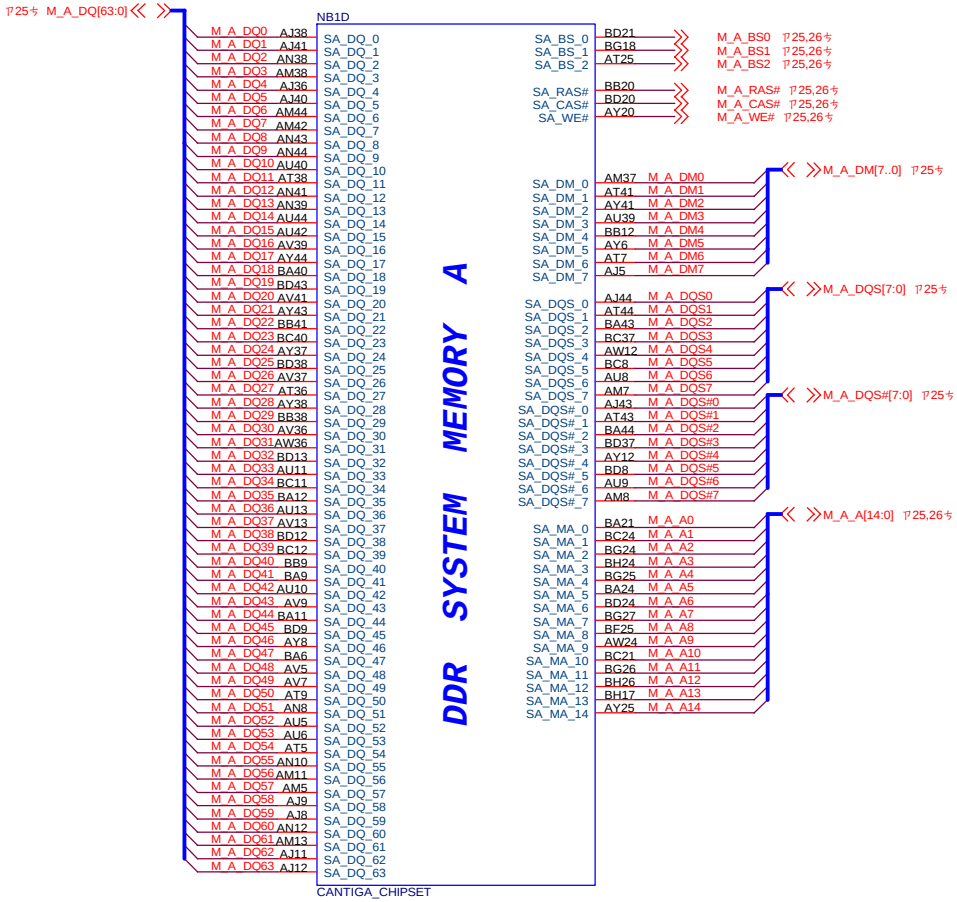
P80VC1

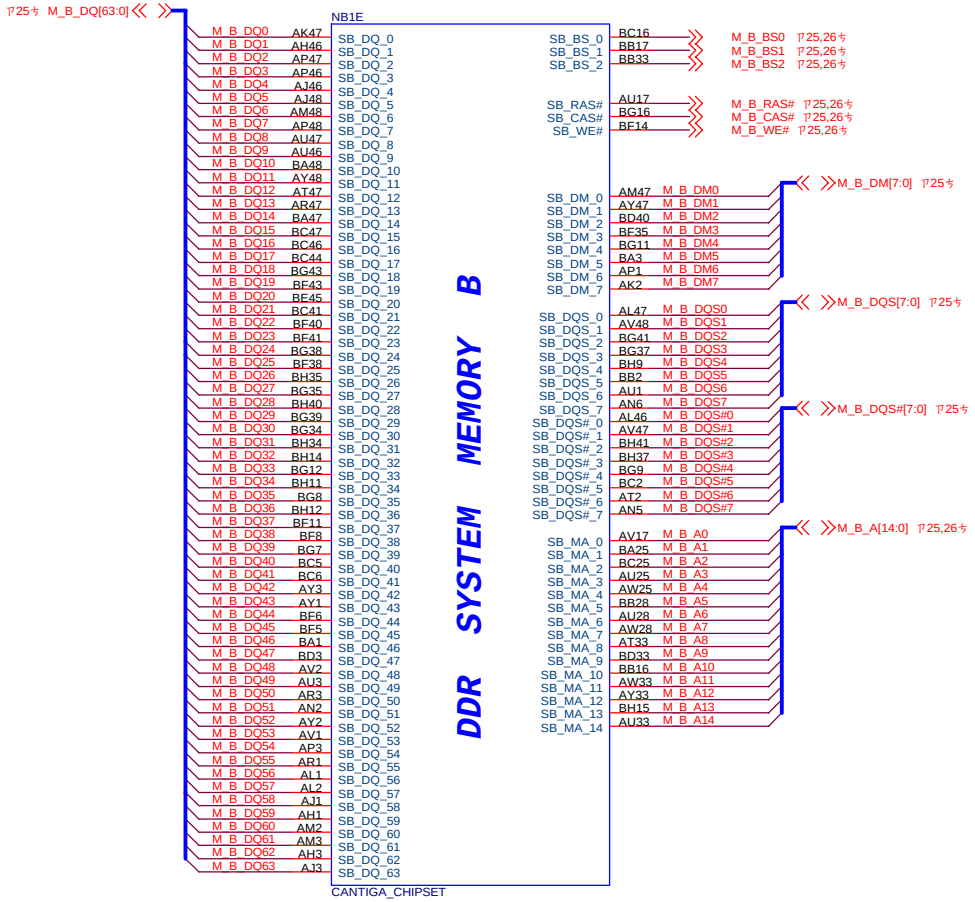
Title : Cantiga - DDR2/DMI(2)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

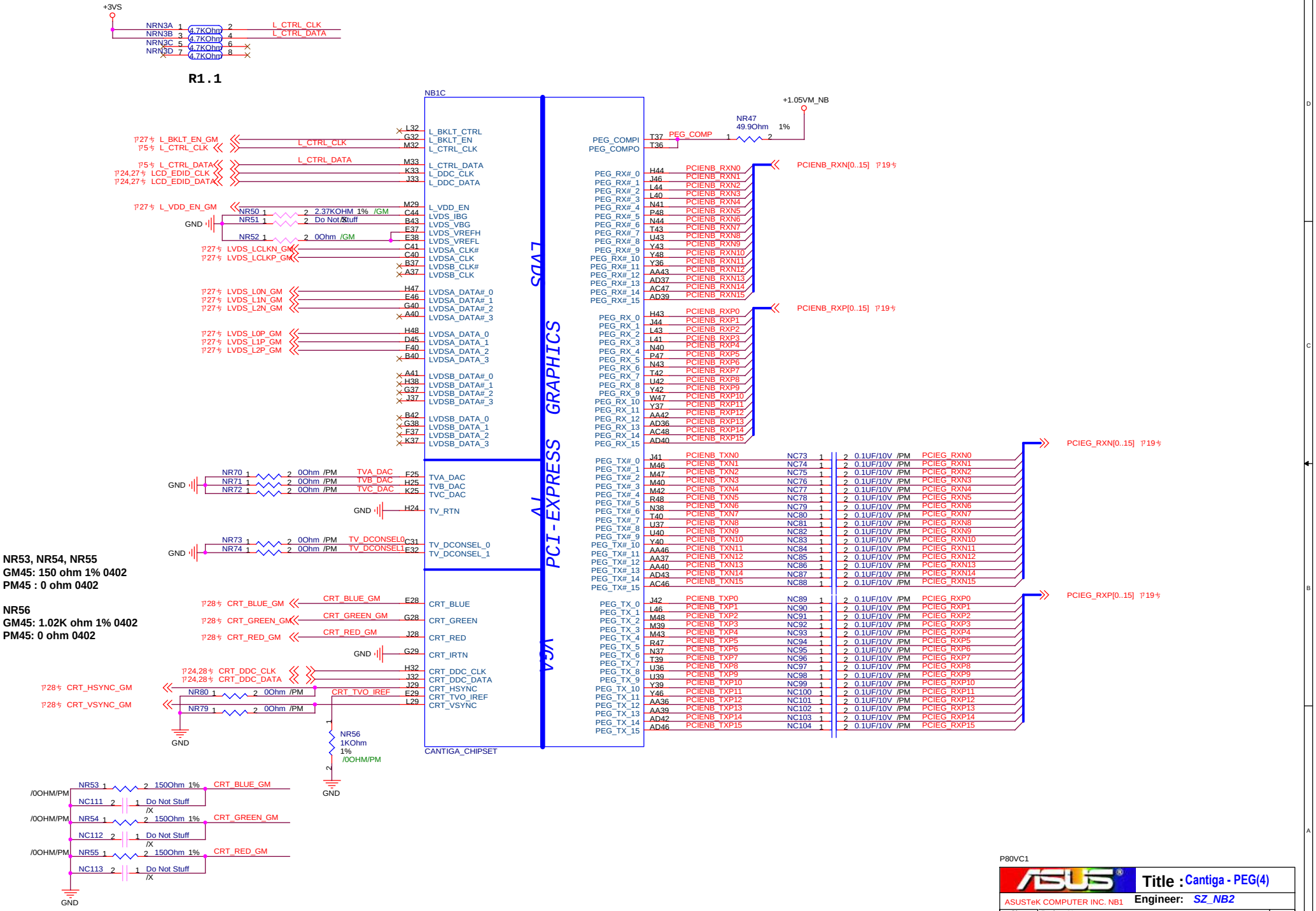
Date: Tuesday, December 16, 2008 Sheet 8 of 52





P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - DDR2(3)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 9 of 52	



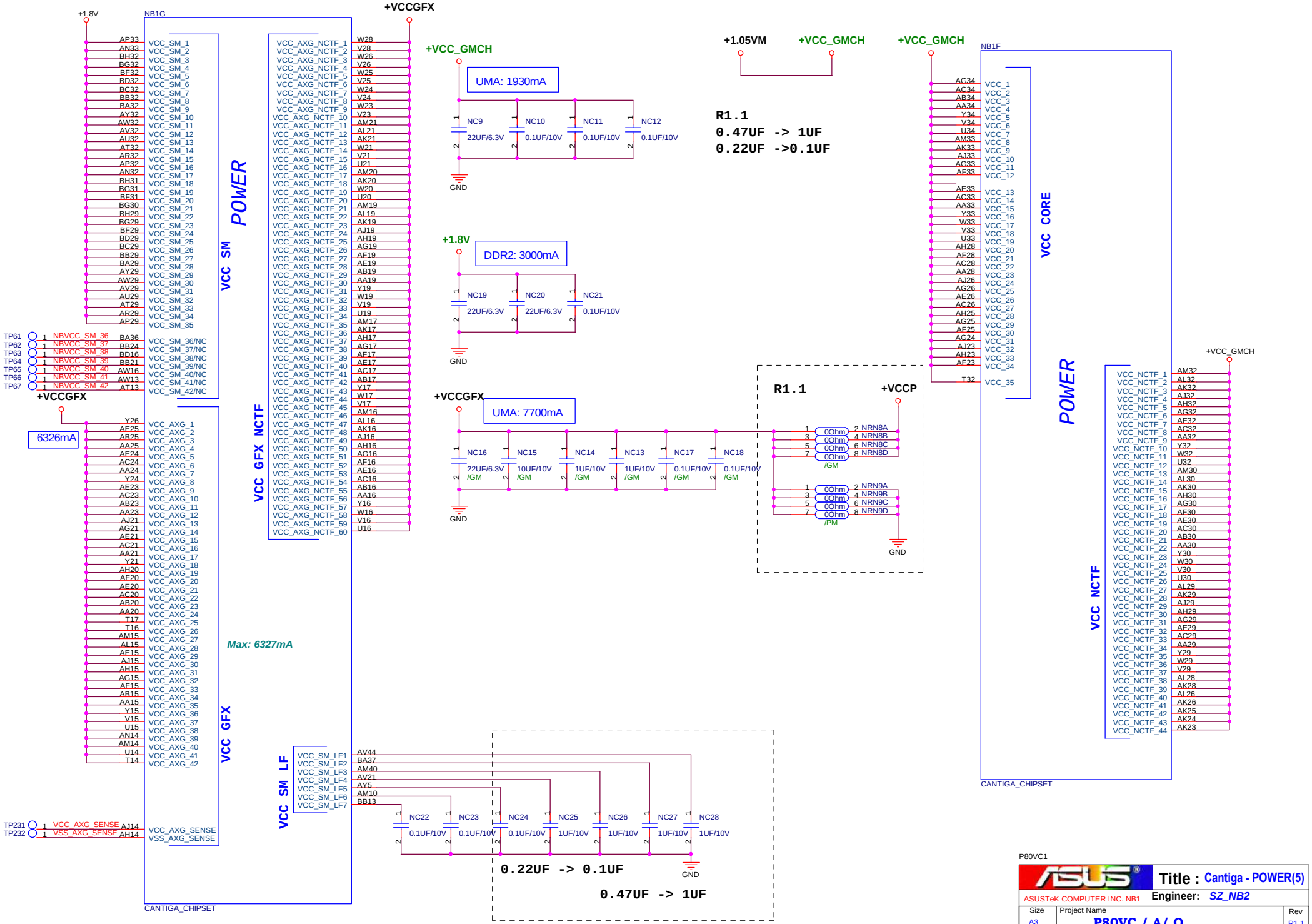
P80VC1

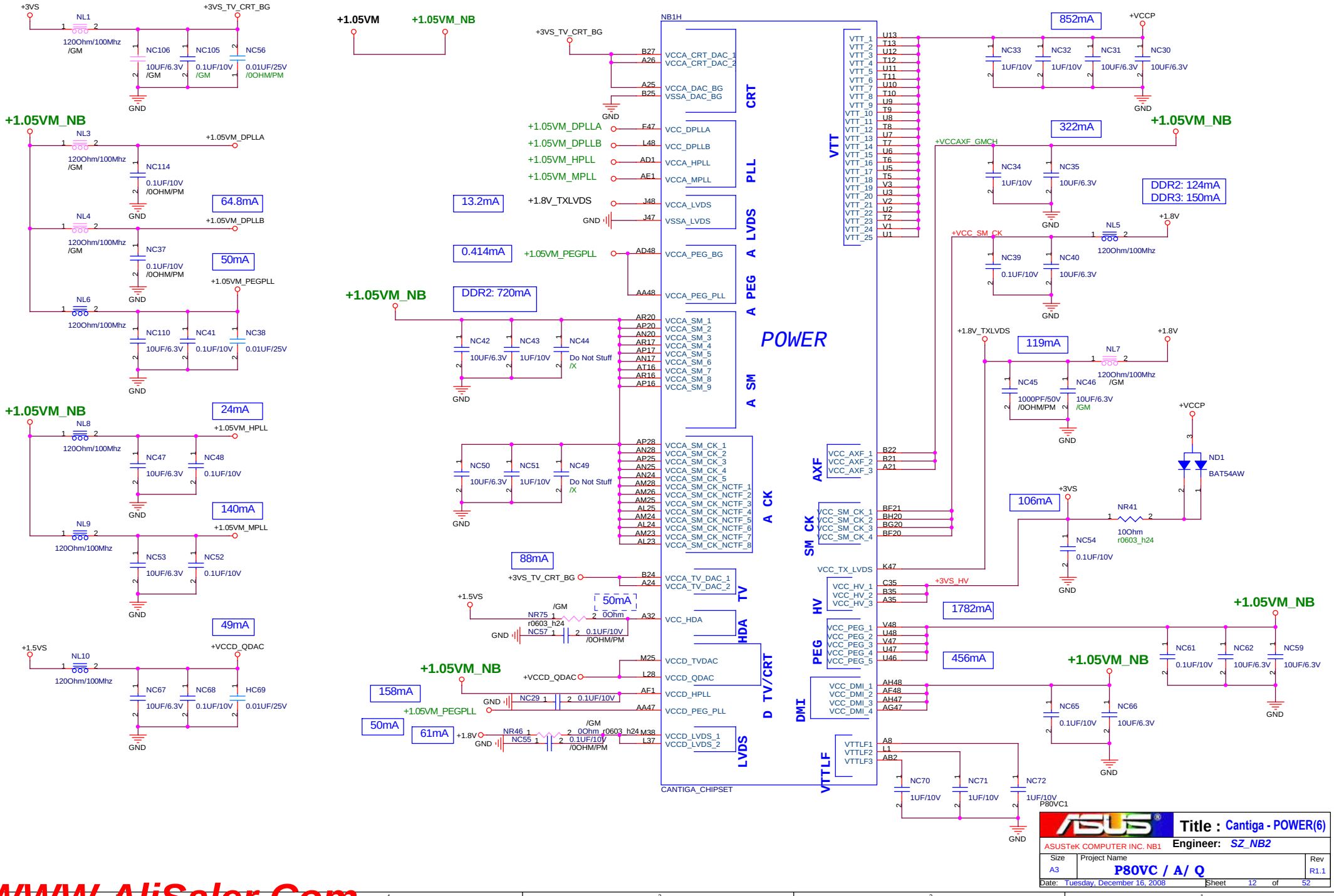
Title : Cantiga - PEG(4)

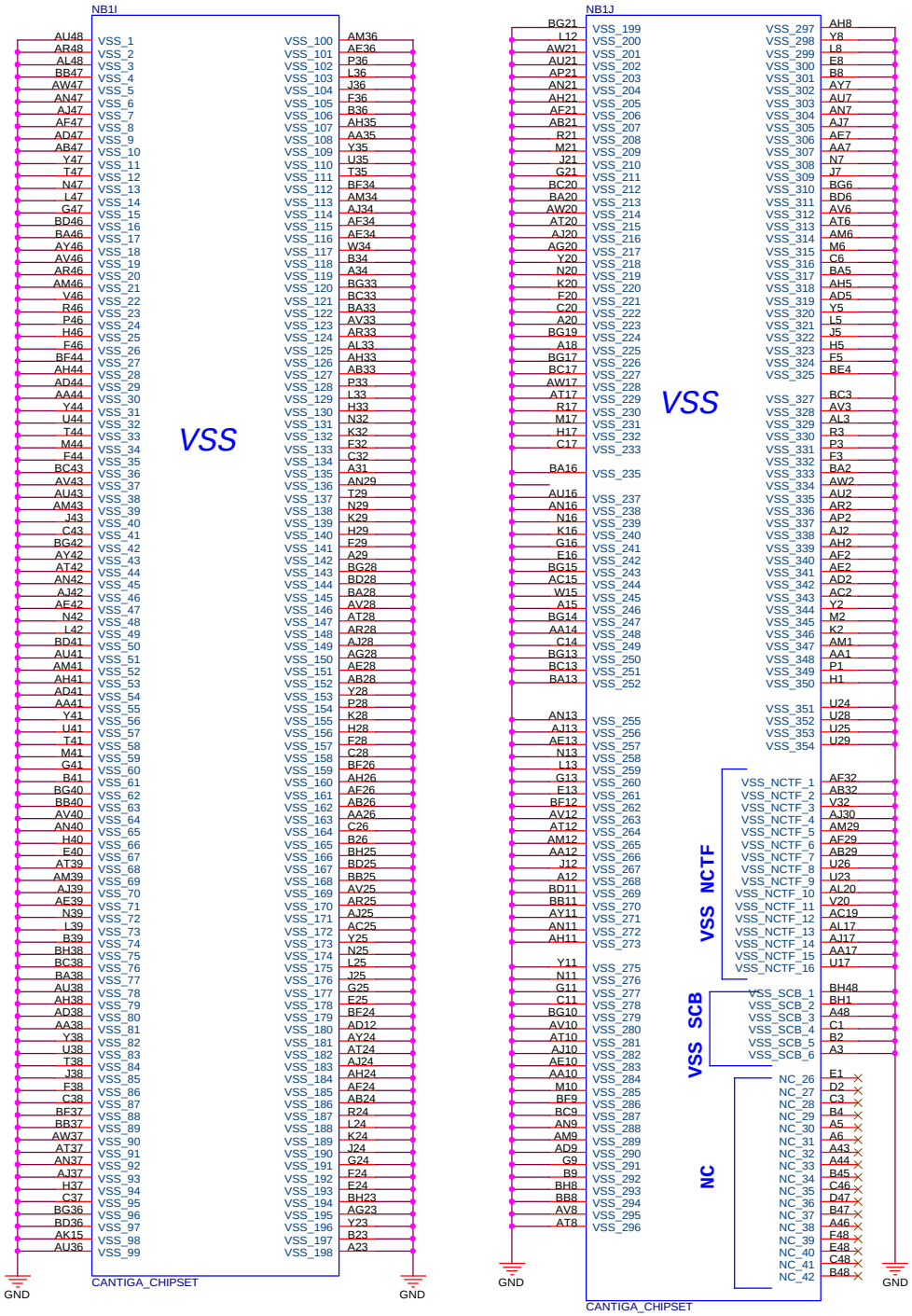
ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 10 of 52


+1.8V
NB1G
+VCCGFX
VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35
VCC SM
POWER
TP61 NBVCC_SM_36
TP62 NBVCC_SM_37
TP63 NBVCC_SM_38
TP64 NBVCC_SM_39
TP65 NBVCC_SM_40
TP66 NBVCC_SM_41
TP67 NBVCC_SM_42
VCC_SM_36/NC VCC_SM_37/NC VCC_SM_38/NC VCC_SM_39/NC VCC_SM_40/NC VCC_SM_41/NC VCC_SM_42/NC
+VCCGFX
6326mA
VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42
VCC GFX
Max: 6327mA
TP231 VCC_AXG_SENSE
TP232 VSS_AXG_SENSE
VCC_AXG_SENSE VSS_AXG_SENSE
CANTIGA_CHIPSET
VCC_AXG_NCTF_1 VCC_AXG_NCTF_2 VCC_AXG_NCTF_3 VCC_AXG_NCTF_4 VCC_AXG_NCTF_5 VCC_AXG_NCTF_6 VCC_AXG_NCTF_7 VCC_AXG_NCTF_8 VCC_AXG_NCTF_9 VCC_AXG_NCTF_10 VCC_AXG_NCTF_11 VCC_AXG_NCTF_12 VCC_AXG_NCTF_13 VCC_AXG_NCTF_14 VCC_AXG_NCTF_15 VCC_AXG_NCTF_16 VCC_AXG_NCTF_17 VCC_AXG_NCTF_18 VCC_AXG_NCTF_19 VCC_AXG_NCTF_20 VCC_AXG_NCTF_21 VCC_AXG_NCTF_22 VCC_AXG_NCTF_23 VCC_AXG_NCTF_24 VCC_AXG_NCTF_25 VCC_AXG_NCTF_26 VCC_AXG_NCTF_27 VCC_AXG_NCTF_28 VCC_AXG_NCTF_29 VCC_AXG_NCTF_30 VCC_AXG_NCTF_31 VCC_AXG_NCTF_32 VCC_AXG_NCTF_33 VCC_AXG_NCTF_34 VCC_AXG_NCTF_35 VCC_AXG_NCTF_36 VCC_AXG_NCTF_37 VCC_AXG_NCTF_38 VCC_AXG_NCTF_39 VCC_AXG_NCTF_40 VCC_AXG_NCTF_41 VCC_AXG_NCTF_42 VCC_AXG_NCTF_43 VCC_AXG_NCTF_44 VCC_AXG_NCTF_45 VCC_AXG_NCTF_46 VCC_AXG_NCTF_47 VCC_AXG_NCTF_48 VCC_AXG_NCTF_49 VCC_AXG_NCTF_50 VCC_AXG_NCTF_51 VCC_AXG_NCTF_52 VCC_AXG_NCTF_53 VCC_AXG_NCTF_54 VCC_AXG_NCTF_55 VCC_AXG_NCTF_56 VCC_AXG_NCTF_57 VCC_AXG_NCTF_58 VCC_AXG_NCTF_59 VCC_AXG_NCTF_60
VCC GFX NCTF
+VCC_GMCH
UMA: 1930mA
NC9 22UF/6.3V
NC10 0.1UF/10V
NC11 0.1UF/10V
NC12 0.1UF/10V
GND
+1.8V
DDR2: 3000mA
NC19 22UF/6.3V
NC20 22UF/6.3V
NC21 0.1UF/10V
GND
+VCCGFX
UMA: 7700mA
NC16 22UF/6.3V /GM
NC15 10UF/10V /GM
NC14 1UF/10V /GM
NC13 1UF/10V /GM
NC17 0.1UF/10V /GM
NC18 0.1UF/10V /GM
GND
+1.05VM
+VCC_GMCH
R1.1
0.47UF -> 1UF
0.22UF ->0.1UF
R1.1
+VCCP
0Ohm NRN8A NRN8B NRN8C NRN8D /GM
0Ohm NRN9A NRN9B NRN9C NRN9D /PM
GND
+VCC_GMCH
NB1F
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35
VCC CORE
POWER
VCC NCTF
VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38 VCC_NCTF_39 VCC_NCTF_40 VCC_NCTF_41 VCC_NCTF_42 VCC_NCTF_43 VCC_NCTF_44
+VCC_GMCH
CANTIGA_CHIPSET
VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7
VCC SM LF
NC22 0.1UF/10V
NC23 0.1UF/10V
NC24 0.1UF/10V
NC25 1UF/10V
NC26 1UF/10V
NC27 1UF/10V
NC28 1UF/10V
0.22UF -> 0.1UF
0.47UF -> 1UF
GND
P80VC1
Title : Cantiga - POWER(5)
ASUSTeK COMPUTER INC. NB1
Engineer: SZ_NB2
Size A3
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 11 of 52





Change NC-26/42 to NC from GND

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - GND(7)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 13 of 52	

Place Near the Open Door

RTCRST#

SC1 1UF/10V

JRST1 Do Not Stuff r0603_h24 /X

GND GND

R1.1

+VCC_RTC

100KOHM SRN6A SRN6B SRN6C SRN6D

VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR

VccLAN1_05 & VccCL1_05 Internal VR

High = Enable (Default)

Low = Disable

BOM: 02G010015342

SB Heatsink Screwhole

SH1 SH2

13GNJ510M190-1 13GNJ510M190-1

GND GND

SB1A

RTC_X1 RTC_X2 RTCRST# INTRUDER# ICH_INTVRMEN ICH_LAN100_SLP

RTCX1 RTCX2 RTCRST# SRTCRST# INTRUDER# INTVRMEN LAN100_SLP

RTC

FWH0/LAD0 FWH1/LAD1 FWH2/LAD2 FWH3/LAD3 FWH4/LFRAME# LDRQ0# LDRQ1#/GPIO23

LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_FRAME# LPC_DRQ0# ST68 LPC_DRQ1#

LPC

+3VSUS SR35 10KOhm GPIO56

GLAN_CLK LAN_RSTSYNC LAN_RXD0 LAN_RXD1 LAN_RXD2 LAN_TXD0 LAN_TXD1 LAN_TXD2 GLAN_DOCK#/GPIO56

+1.5VS_PCIE_ICH SR36 24.9Ohm 1%

GLAN_COMPI GLAN_COMPO

LAN / GLAN

A20GATE A20M# DPRSTP# DPSLP# FERR# CPUPWRGD IGNNE# INIT# INTR RCIN# NMI SMI# STPCLK# THRMTRIP# PECI

A20GATE A20M# DPRSTP# DPSLP# FERR# SRN4A CPUPWRGD IGNNE# INIT# INTR RC_IN# NMI SMI# STPCLK# PM_THRMTRIP# ST80

CPU

ACZ_BCLK_AUD ACZ_SYNC_AUD ACZ_RST#_AUD ACZ_SDOUT_AUD ACZ_BCLK_MDC ACZ_SYNC_MDC ACZ_RST#_MDC ACZ_SDOUT_MDC

33OHM SRN1A SRN1D SRN1B SRN1C SRN2D SRN2B SRN2C SRN2A

ACZ_BCLK ACZ_SYNC ACZ_RST# ACZ_SDOUT

ACZ_BCLK ACZ_SYNC ACZ_RST# SB_GPIO33 ST82

HDA_BIT_CLK HDA_SYNC HDA_RST# HDA_SDIN0 HDA_SDIN1 HDA_SDIN2 HDA_SDIN3 HDA_SDOUT HDA_DOCK_EN#/GPIO33 HDA_DOCK_RST#/GPIO34

ACZ_SDIN0_AUD ACZ_SDIN1_MDC

IHDA

SATA4RXN SATA4RXP SATA4TXN SATA4TXP SATA5RXN SATA5RXP SATA5TXN SATA5TXP SATA_CLKN SATA_CLKP SATARBIAS# SATARBIAS

ESATA_RXN_SB ESATA_RXP_SB ESATA_TXN_SB ESATA_TXP_SB CLK_SATA_SB# CLK_SATA_SB SATARBIAS# SR38 27.4Ohm 1% GND

Pass EA measurement

HDD

ODD

HDD_LED# SATALED#

SATA_RXN0 SATA_RXP0 SATA_TXN0 SATA_TXP0 SATA_RXN1 SATA_RXP1 SATA_TXN1 SATA_TXP1

SATA0RXN SATA0RXP SATA0TXN SATA0TXP SATA1RXN SATA1RXP SATA1TXN SATA1TXP

SATA

ICH9M

SC5 12PF/50V RTC_X1

SX1 32.768kMhz +/-20ppm/12.5PF

SR40 10MOhm

SC6 12PF/50V RTC_X2

GND

OD signal

+VCCP SRN4D 56OHM

H_FERR# SRN4B

PM_THRMTRIP# SRN4C H_THRMTRIP#

SC72 Do Not Stuff /X

GND

[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved

01= Enter XOR Chain

10= Normal Operation (Default)

11= Set PCIe Port Config Bit 1

Flash Descriptor Security Override

High = Enable (Default)

Low = Overridden

ACZ_SDOUT SR49 Do Not Stuff 1% +3VS

SR5 Do Not Stuff 1% ICH_TP3

GND

SR6 Do Not Stuff SB_GPIO33

GND

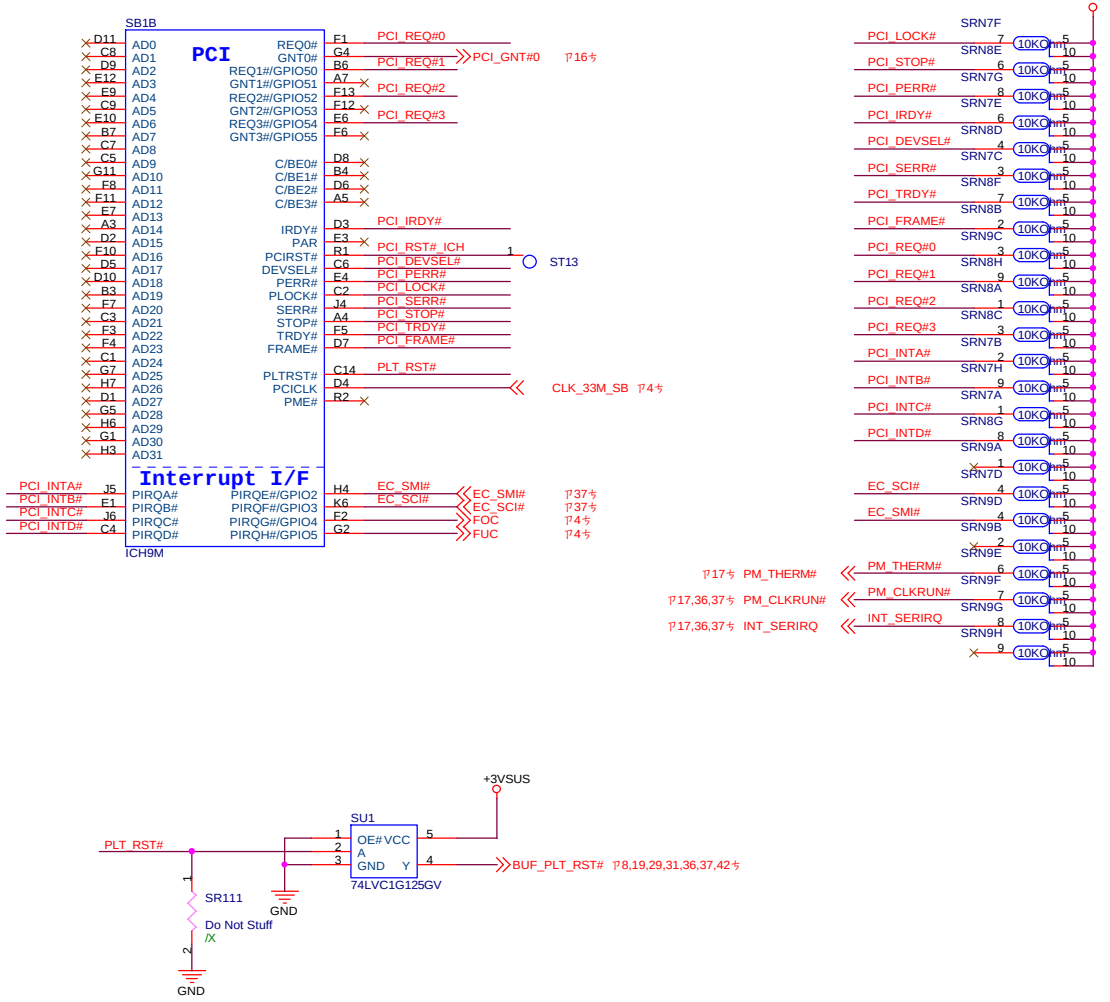
P80VC1

Title : SB-ICH9M(1)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size A3 | Project Name P80VC / A/ Q | Rev R1.1

Date: Tuesday, December 16, 2008 | Sheet 14 of 52



UNUSED PCI temination

AD [31:0]	Can be left unconnected
C/BE [3:0]#	Can be left unconnected
DEVSEL#	8.2-k weak pull-up resistor to Vcc3_3
FRAME#	8.2-k weak pull-up resistor to Vcc3_3
IRDY#	8.2-k weak pull-up resistor to Vcc3_3
TRDY#	8.2-k weak pull-up resistor to Vcc3_3
STOP#	8.2-k weak pull-up resistor to Vcc3_3
PAR	Can be left unconnected
PERR#	8.2-k weak pull-up resistor to Vcc3_3
REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54	Requires a 8.2-k weak pull-up resistor to Vcc3_3. REQ [3:1] can be configured as GPIO instead.
GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55	Can be left unconnected. GNT [3:1]# can be configured as GPIO instead. GNT [3:0] is sampled as a functional strapping;
PCICLK	Should remain connected to 33-MHz clock source
PCIRST#	Can be left unconnected
PLOCK#	8.2-k weak pull-up resistor to Vcc3_3
SERR#	8.2-k weak pull-up resistor to Vcc3_3
PIRQ [D:A]# PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5	Requires a 8.2-k weak pull-up resistor to Vcc3_3 PIRQ [H:E]# Can be left unconfigured as GPIO instead
SERIRQ	8.2-k pull-up to Vcc3_3
PME#	Can be left unconnected. Internally pull-up
CLKRUN#	8.2-k weak pull-up resistor to Vcc3_3

P80VC1

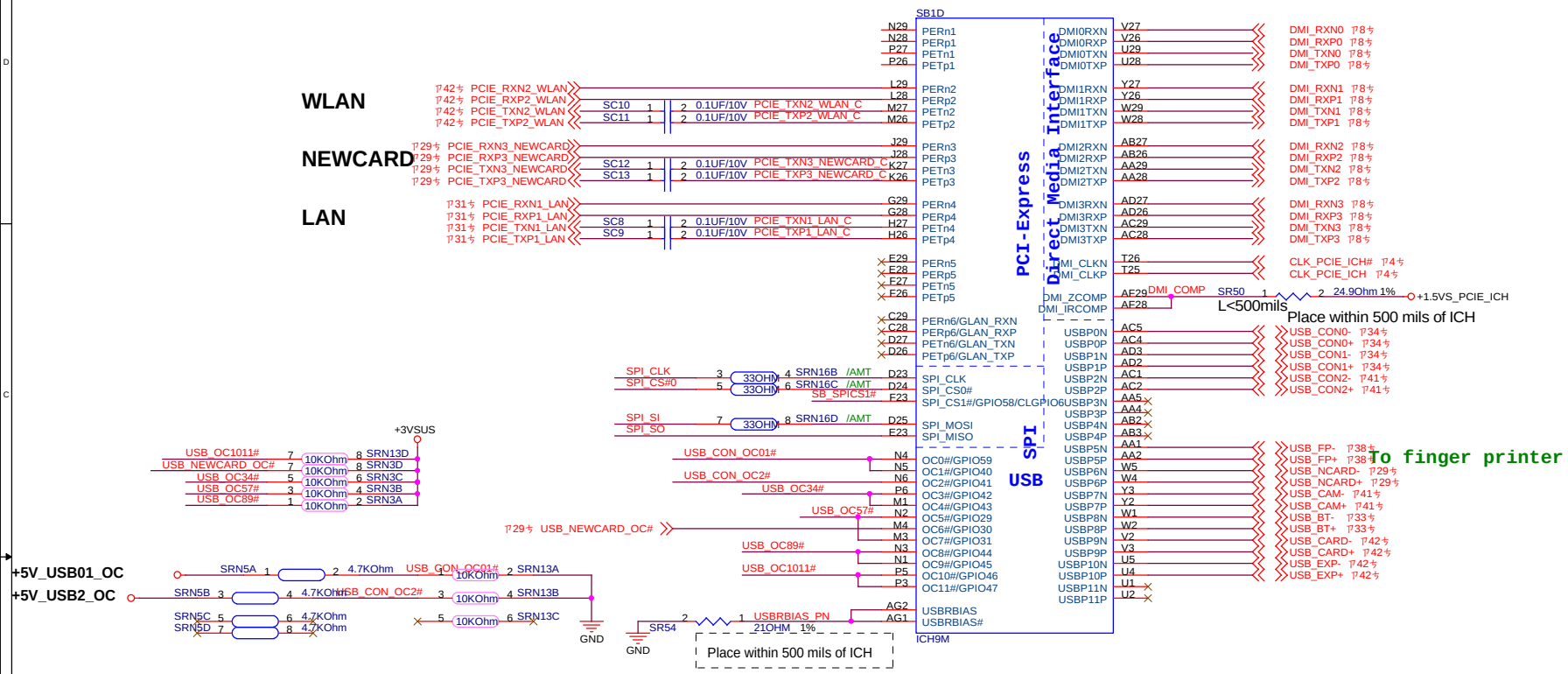
ASUSTeK COMPUTER INC. NB1

Title : SB-ICH9M(2)

Engineer: SZ_NB2

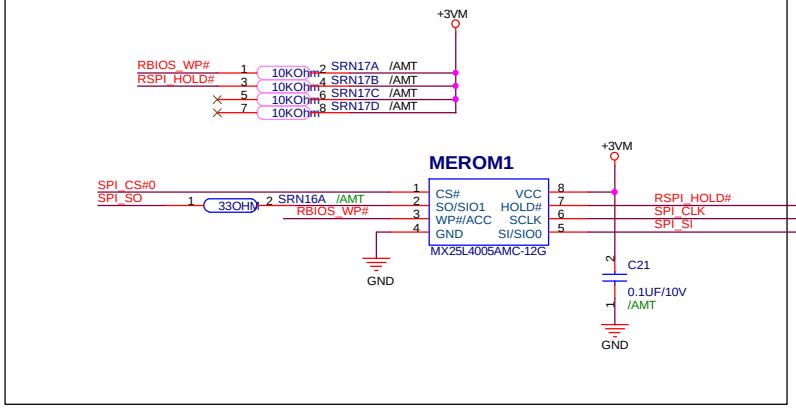
Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 15 of 52



USB0	CON
USB1	CON
USB2	CON
USB3	N/A
USB4	N/A
USB5	FingerPrint
USB6	NewCard
USB7	Camera
USB8	BT
USB9	Cardreader
USB10	MC (WLAN)
USB11	N/A

SB Flash for ME



ICH9 Boot BIOS select

		GNT#0	CS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

PCI_GNT#0 SR216 Do Not Stuff /X
SB_SPICS1# SR217 Do Not Stuff /X
GND

R1.1

SPI_MOSI
iTPM
Enable
High = Enable
Low = Disable(Default)

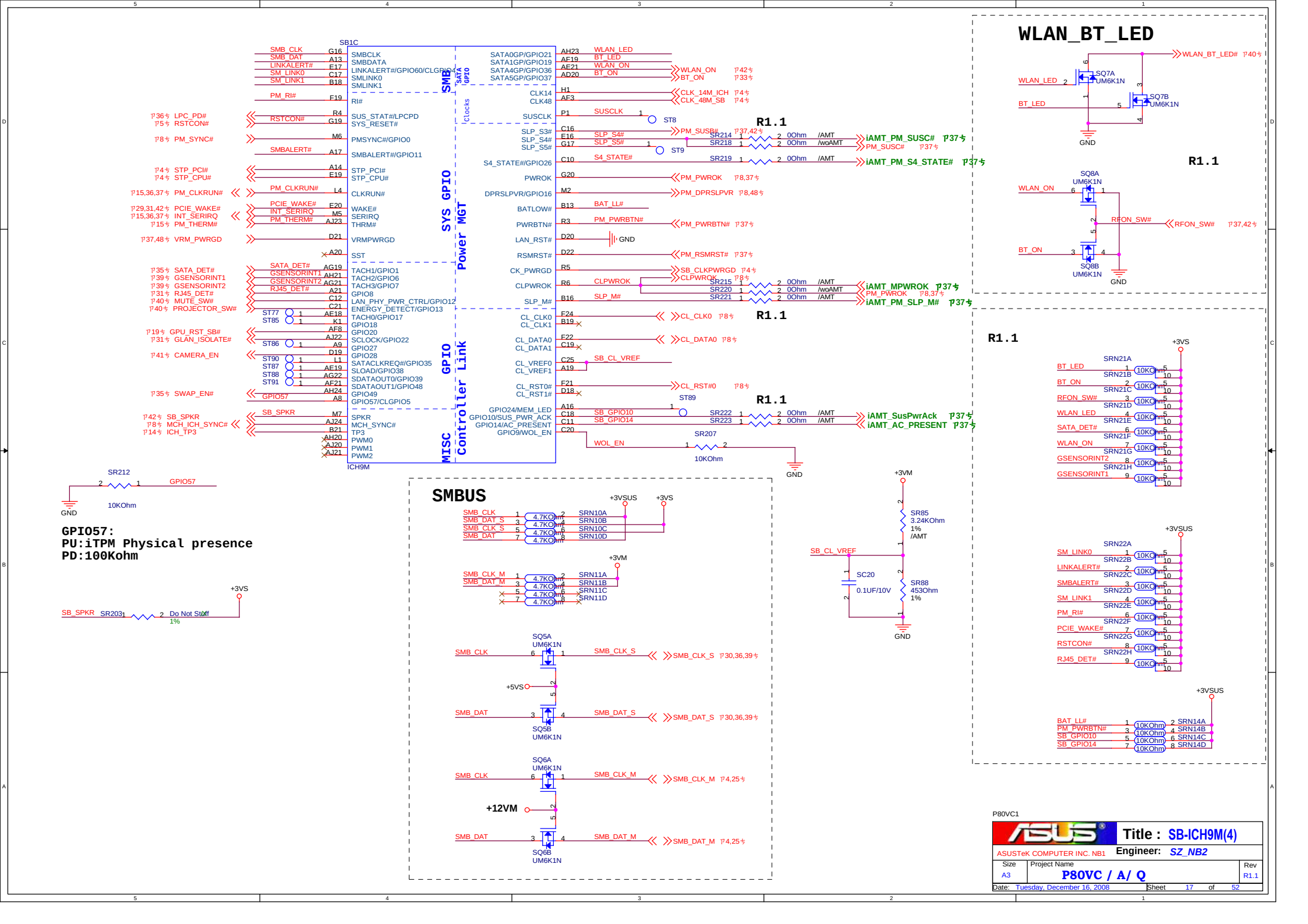
P80VC1

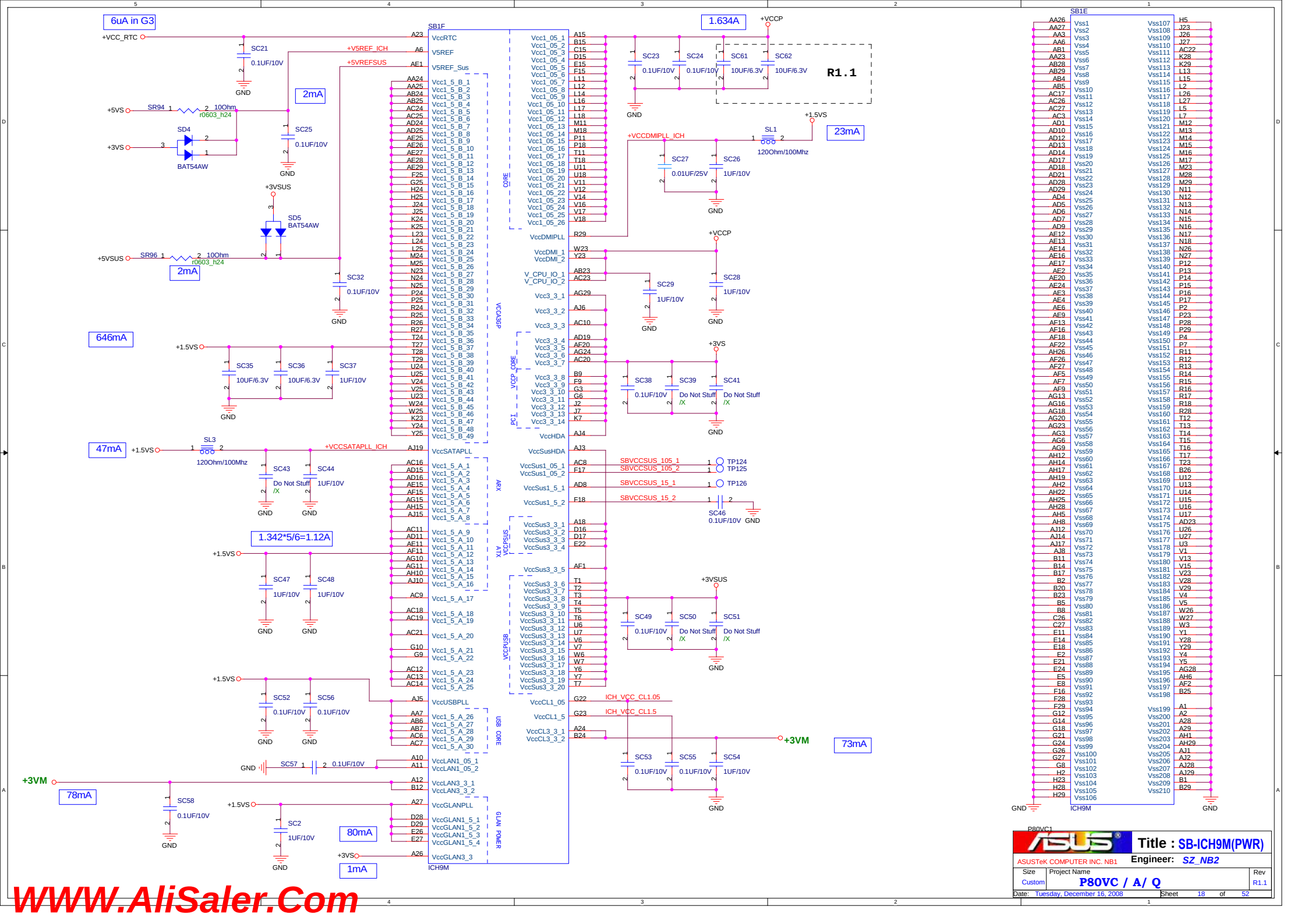
ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

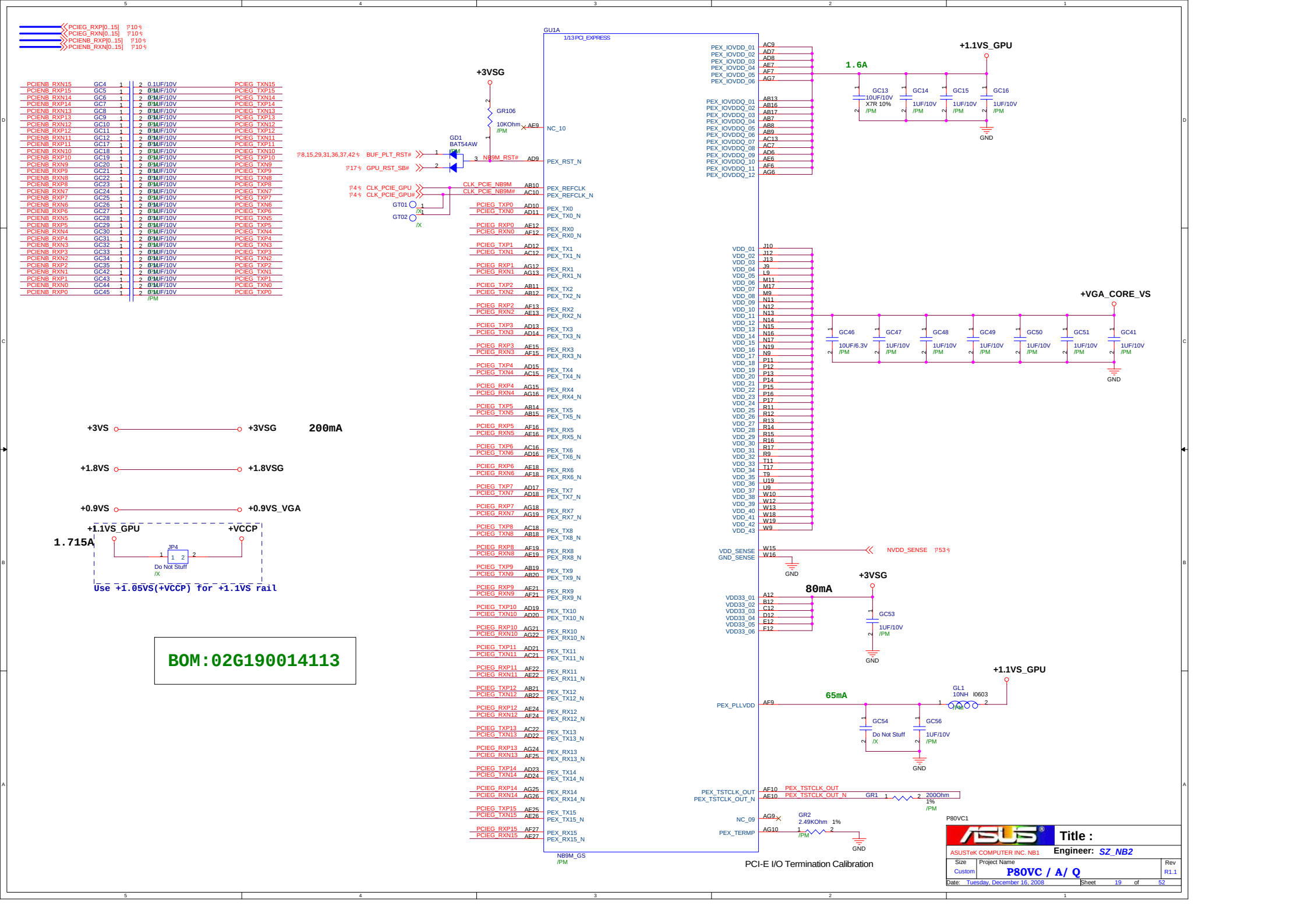
Title : SB-ICH9M(3)

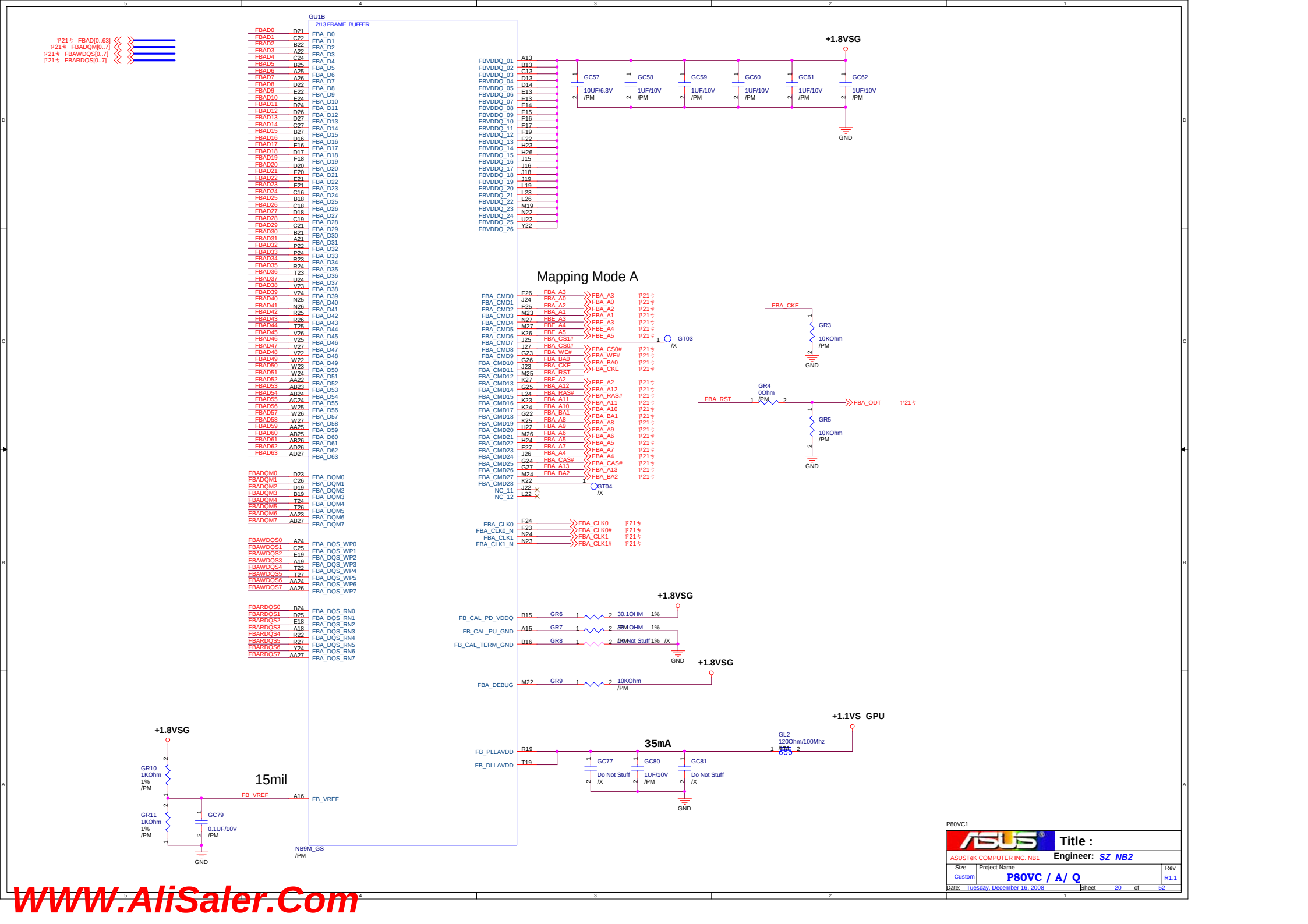
Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

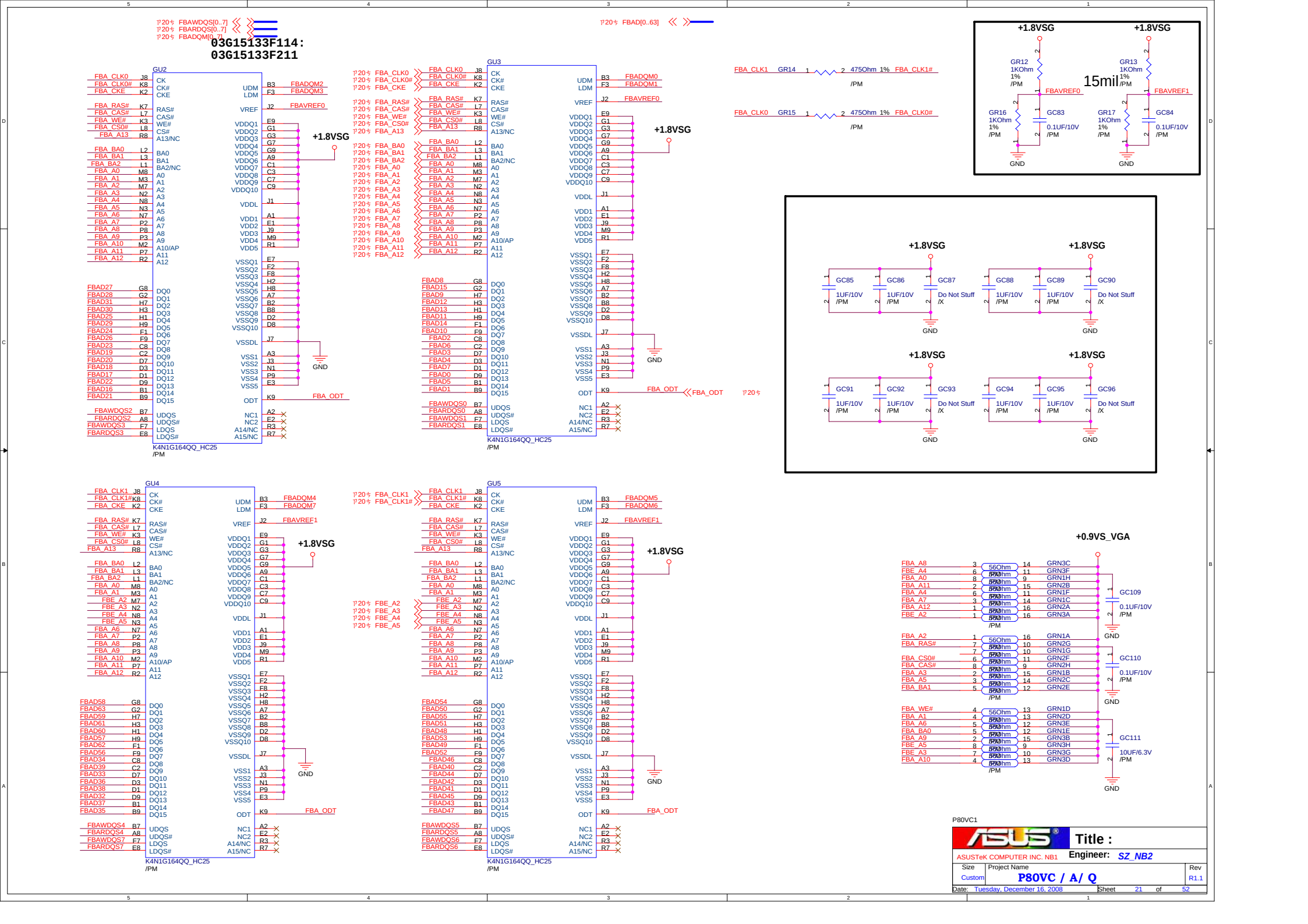
Date: Tuesday, December 16, 2008 Sheet 16 of 52


SB1C
SMB_CLK G16
SMB_DAT A13
LINKALERT# E17
SM_LINK0 C17
SM_LINK1 B18
PM_RI# F19
RSTCON# R4
G19
PM_SYNC# M6
SMBALERT# A17
STP_PCI# A14
STP_CPU# E19
PM_CLKRUN# L4
PCIE_WAKE# E20
INT_SERIRQ M5
PM_THERM# AJ23
VRM_PWRGD D21
A20
SATA_DET# AG19
GSENSORINT1 AH21
GSENSORINT2 AG21
RJ45_DET# A21
C12
C21
ST77 AE18
ST85 K1
AF8
GPU_RST_SB#
GLAN_ISOLATE# AJ22
ST86 A9
CAMERA_EN D19
ST90 L1
ST87 AE19
ST88 AG22
ST91 AE21
AH24
SWAP_EN# GPIO57 A8
SB_SPKR M7
MCH_ICH_SYNC# AJ24
ICH_TP3 B21
AH20
AJ20
AJ21
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
ICH9M
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21 AH23 WLAN_LED
SATA1GP/GPIO19 AF19 BT_LED
SATA4GP/GPIO36 AE21 WLAN_ON
SATA5GP/GPIO37 AD20 BT_ON
CLK14 H1 CLK_14M_ICH
CLK48 AF3 CLK_48M_SB
SUSCLK P1 SUSCLK
SLP_S3# C16 PM_SUSB#
SLP_S4# E16 SLP_S4#
SLP_S5# G17 SLP_S5#
S4_STATE#/GPIO26 C10 S4_STATE#
PWROK G20 PM_PWROK
DPRSLPVR/GPIO16 M2 PM_DPRSLPVR
BATLOW# B13 BAT_LL#
PWRBTN# R3 PM_PWRBTN#
LAN_RST# D20
RSMRST# D22 PM_RSMRST#
CK_PWRGD R5 SB_CLKPWRGD
CLPWROK R6 CLPWROK
SLP_M# B16 SLP_M#
CL_CLK0 F24 CL_CLK0
CL_CLK1 B19
CL_DATA0 F22 CL_DATA0
CL_DATA1 C19
CL_VREF0 C25 SB_CL_VREF
CL_VREF1 A19
CL_RST0# F21 CL_RST#0
CL_RST1# D18
GPIO24/MEM_LED A16
GPIO10/SUS_PWR_ACK C18 SB_GPIO10
GPIO14/AC_PRESENT C11 SB_GPIO14
GPIO9/WOL_EN C20 WOL_EN
ST8
ST9
ST89
SR214 SR218 SR219 SR215 SR220 SR221 SR222 SR223 SR207
0Ohm /AMT /woAMT
10KOhm
GND
R1.1
WLAN_ON
BT_ON
iAMT_PM_SUSC#
PM_SUSC#
iAMT_PM_S4_STATE#
iAMT_MPWROK
PM_PWROK
iAMT_PM_SLP_M#
iAMT_SusPwrAck
iAMT_AC_PRESENT
WLAN_BT_LED
WLAN_BT_LED# 42
WLAN_LED
BT_LED
SQ7A UM6K1N
SQ7B UM6K1N
SQ8A UM6K1N
SQ8B UM6K1N
RFON_SW#
RFON_SW# 37,42
SR212 GPIO57 10KOhm
GPIO57:
PU:iTPM Physical presence
PD:100Kohm
SR203 Do Not Stuff 1%
SMBUS
+3VSUS
+3VS
+3VM
+5VS
+12VM
SMB_CLK
SMB_DAT
SMB_CLK_S
SMB_DAT_S
SMB_CLK_M
SMB_DAT_M
SRN10A SRN10B SRN10C SRN10D
SRN11A SRN11B SRN11C SRN11D
4.7KOhm
SQ5A UM6K1N
SQ5B UM6K1N
SQ6A UM6K1N
SQ6B UM6K1N
SB_CL_VREF
SR85 3.24KOhm 1% /AMT
SC20 0.1UF/10V
SR88 453Ohm 1%
SRN21A SRN21B SRN21C SRN21D SRN21E SRN21F SRN21G SRN21H
SRN22A SRN22B SRN22C SRN22D SRN22E SRN22F SRN22G SRN22H
10KOhm
BT_LED
BT_ON
RFON_SW#
WLAN_LED
SATA_DET#
WLAN_ON
GSENSORINT2
GSENSORINT1
SM_LINK0
LINKALERT#
SMBALERT#
SM_LINK1
PM_RI#
PCIE_WAKE#
RSTCON#
RJ45_DET#
SRN14A SRN14B SRN14C SRN14D
BAT_LL#
PM_PWRBTN#
SB_GPIO10
SB_GPIO14
P80VC1
Title : SB-ICH9M(4)
ASUSTeK COMPUTER INC. NB1
Engineer: SZ_NB2
Size A3
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 17 of 52

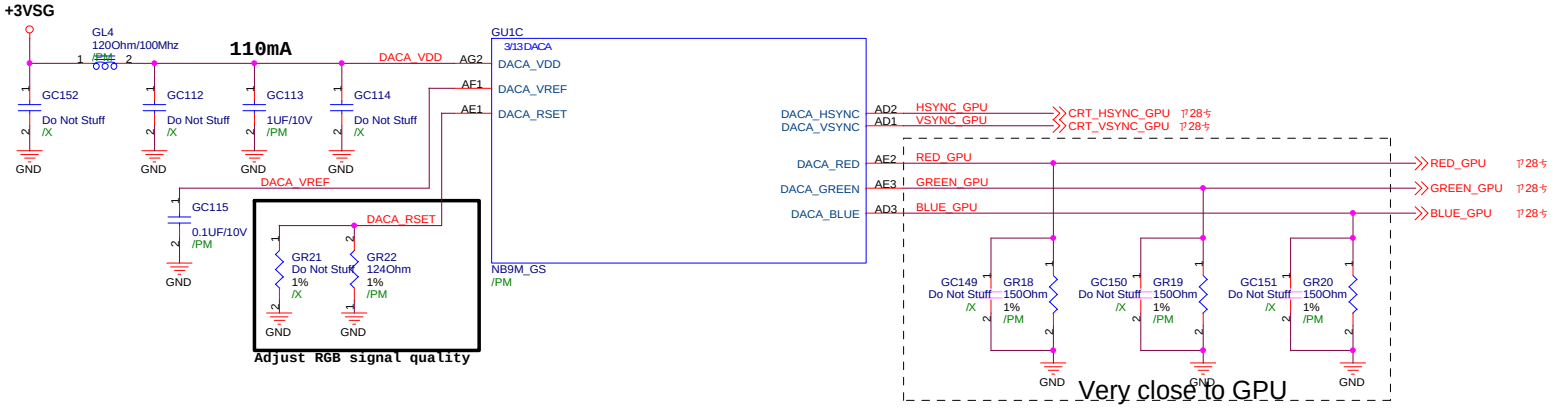



PCIEG_RXP[0..15] 『10』
PCIEG_RXN[0..15] 『10』
PCIENB_RXP[0..15] 『10』
PCIENB_RXN[0..15] 『10』
PCIENB_RXN15 GC4 0.1UF/10V PCIEG_TXN15
PCIENB_RXP15 GC5 0.1UF/10V PCIEG_TXP15
PCIENB_RXN14 GC6 0.1UF/10V PCIEG_TXN14
PCIENB_RXP14 GC7 0.1UF/10V PCIEG_TXP14
PCIENB_RXN13 GC8 0.1UF/10V PCIEG_TXN13
PCIENB_RXP13 GC9 0.1UF/10V PCIEG_TXP13
PCIENB_RXN12 GC10 0.1UF/10V PCIEG_TXN12
PCIENB_RXP12 GC11 0.1UF/10V PCIEG_TXP12
PCIENB_RXN11 GC12 0.1UF/10V PCIEG_TXN11
PCIENB_RXP11 GC17 0.1UF/10V PCIEG_TXP11
PCIENB_RXN10 GC18 0.1UF/10V PCIEG_TXN10
PCIENB_RXP10 GC19 0.1UF/10V PCIEG_TXP10
PCIENB_RXN9 GC20 0.1UF/10V PCIEG_TXN9
PCIENB_RXP9 GC21 0.1UF/10V PCIEG_TXP9
PCIENB_RXN8 GC22 0.1UF/10V PCIEG_TXN8
PCIENB_RXP8 GC23 0.1UF/10V PCIEG_TXP8
PCIENB_RXN7 GC24 0.1UF/10V PCIEG_TXN7
PCIENB_RXP7 GC25 0.1UF/10V PCIEG_TXP7
PCIENB_RXN6 GC26 0.1UF/10V PCIEG_TXN6
PCIENB_RXP6 GC27 0.1UF/10V PCIEG_TXP6
PCIENB_RXN5 GC28 0.1UF/10V PCIEG_TXN5
PCIENB_RXP5 GC29 0.1UF/10V PCIEG_TXP5
PCIENB_RXN4 GC30 0.1UF/10V PCIEG_TXN4
PCIENB_RXP4 GC31 0.1UF/10V PCIEG_TXP4
PCIENB_RXN3 GC32 0.1UF/10V PCIEG_TXN3
PCIENB_RXP3 GC33 0.1UF/10V PCIEG_TXP3
PCIENB_RXN2 GC34 0.1UF/10V PCIEG_TXN2
PCIENB_RXP2 GC35 0.1UF/10V PCIEG_TXP2
PCIENB_RXN1 GC42 0.1UF/10V PCIEG_TXN1
PCIENB_RXP1 GC43 0.1UF/10V PCIEG_TXP1
PCIENB_RXN0 GC44 0.1UF/10V PCIEG_TXN0
PCIENB_RXP0 GC45 0.1UF/10V PCIEG_TXP0
/PM
+3VSG
GR106
10KOhm
/PM
GD1
BAT54AW
/PM
『8,15,29,31,36,37,42』 BUF_PLT_RST#
『17』 GPU_RST_SB#
NB9M_RST#
GT01
GT02
/X
GU1A
1/13 PCI_EXPRESS
NC_10
PEX_RST_N
CLK_PCIE_NB9M
CLK_PCIE_NB9M#
『4』 CLK_PCIE_GPU
『4』 CLK_PCIE_GPU#
PEX_REFCLK
PEX_REFCLK_N
PCIEG_TXP0
PCIEG_TXN0
PEX_TX0
PEX_TX0_N
PCIEG_RXP0
PCIEG_RXN0
PEX_RX0
PEX_RX0_N
PCIEG_TXP1
PCIEG_TXN1
PEX_TX1
PEX_TX1_N
PCIEG_RXP1
PCIEG_RXN1
PEX_RX1
PEX_RX1_N
PCIEG_TXP2
PCIEG_TXN2
PEX_TX2
PEX_TX2_N
PCIEG_RXP2
PCIEG_RXN2
PEX_RX2
PEX_RX2_N
PCIEG_TXP3
PCIEG_TXN3
PEX_TX3
PEX_TX3_N
PCIEG_RXP3
PCIEG_RXN3
PEX_RX3
PEX_RX3_N
PCIEG_TXP4
PCIEG_TXN4
PEX_TX4
PEX_TX4_N
PCIEG_RXP4
PCIEG_RXN4
PEX_RX4
PEX_RX4_N
PCIEG_TXP5
PCIEG_TXN5
PEX_TX5
PEX_TX5_N
PCIEG_RXP5
PCIEG_RXN5
PEX_RX5
PEX_RX5_N
PCIEG_TXP6
PCIEG_TXN6
PEX_TX6
PEX_TX6_N
PCIEG_RXP6
PCIEG_RXN6
PEX_RX6
PEX_RX6_N
PCIEG_TXP7
PCIEG_TXN7
PEX_TX7
PEX_TX7_N
PCIEG_RXP7
PCIEG_RXN7
PEX_RX7
PEX_RX7_N
PCIEG_TXP8
PCIEG_TXN8
PEX_TX8
PEX_TX8_N
PCIEG_RXP8
PCIEG_RXN8
PEX_RX8
PEX_RX8_N
PCIEG_TXP9
PCIEG_TXN9
PEX_TX9
PEX_TX9_N
PCIEG_RXP9
PCIEG_RXN9
PEX_RX9
PEX_RX9_N
PCIEG_TXP10
PCIEG_TXN10
PEX_TX10
PEX_TX10_N
PCIEG_RXP10
PCIEG_RXN10
PEX_RX10
PEX_RX10_N
PCIEG_TXP11
PCIEG_TXN11
PEX_TX11
PEX_TX11_N
PCIEG_RXP11
PCIEG_RXN11
PEX_RX11
PEX_RX11_N
PCIEG_TXP12
PCIEG_TXN12
PEX_TX12
PEX_TX12_N
PCIEG_RXP12
PCIEG_RXN12
PEX_RX12
PEX_RX12_N
PCIEG_TXP13
PCIEG_TXN13
PEX_TX13
PEX_TX13_N
PCIEG_RXP13
PCIEG_RXN13
PEX_RX13
PEX_RX13_N
PCIEG_TXP14
PCIEG_TXN14
PEX_TX14
PEX_TX14_N
PCIEG_RXP14
PCIEG_RXN14
PEX_RX14
PEX_RX14_N
PCIEG_TXP15
PCIEG_TXN15
PEX_TX15
PEX_TX15_N
PCIEG_RXP15
PCIEG_RXN15
PEX_RX15
PEX_RX15_N
NB9M_GS
/PM
PEX_IOVDD_01 AC9
PEX_IOVDD_02 AD7
PEX_IOVDD_03 AD8
PEX_IOVDD_04 AE7
PEX_IOVDD_05 AF7
PEX_IOVDD_06 AG7
PEX_IOVDDQ_01 AB13
PEX_IOVDDQ_02 AB16
PEX_IOVDDQ_03 AB17
PEX_IOVDDQ_04 AB7
PEX_IOVDDQ_05 AB8
PEX_IOVDDQ_06 AB9
PEX_IOVDDQ_07 AC13
PEX_IOVDDQ_08 AC7
PEX_IOVDDQ_09 AD6
PEX_IOVDDQ_10 AE6
PEX_IOVDDQ_11 AF6
PEX_IOVDDQ_12 AG6
+1.1VS_GPU
1.6A
GC13 10UF/10V X7R 10% /PM
GC14 1UF/10V /PM
GC15 1UF/10V /PM
GC16 1UF/10V /PM
GND
VDD_01 J10
VDD_02 J12
VDD_03 J13
VDD_04 J9
VDD_05 L9
VDD_06 M11
VDD_07 M17
VDD_08 M9
VDD_09 N11
VDD_10 N12
VDD_11 N13
VDD_12 N14
VDD_13 N15
VDD_14 N16
VDD_15 N17
VDD_16 N19
VDD_17 N9
VDD_18 P11
VDD_19 P12
VDD_20 P13
VDD_21 P14
VDD_22 P15
VDD_23 P16
VDD_24 P17
VDD_25 R11
VDD_26 R12
VDD_27 R13
VDD_28 R14
VDD_29 R15
VDD_30 R16
VDD_31 R17
VDD_32 R9
VDD_33 T11
VDD_34 T17
VDD_35 T9
VDD_36 U19
VDD_37 U9
VDD_38 W10
VDD_39 W12
VDD_40 W13
VDD_41 W18
VDD_42 W19
VDD_43 W9
+VGA_CORE_VS
GC46 10UF/6.3V /PM
GC47 1UF/10V /PM
GC48 1UF/10V /PM
GC49 1UF/10V /PM
GC50 1UF/10V /PM
GC51 1UF/10V /PM
GC41 1UF/10V /PM
GND
VDD_SENSE W15
GND_SENSE W16
NVDD_SENSE 『53』
GND
80mA
+3VSG
VDD33_01 A12
VDD33_02 B12
VDD33_03 C12
VDD33_04 D12
VDD33_05 E12
VDD33_06 F12
GC53 1UF/10V /PM
GND
+1.1VS_GPU
65mA
PEX_PLLVDD AF9
GL1 10NH I0603 /PM
GC54 Do Not Stuff /X
GC56 1UF/10V /PM
GND
PEX_TSTCLK_OUT AF10
PEX_TSTCLK_OUT_N AE10
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
GR1 200Ohm 1% /PM
NC_09 AG9
PEX_TERMP AG10
GR2 2.49KOhm 1% /PM
GND
PCI-E I/O Termination Calibration
+3VS +3VSG 200mA
+1.8VS +1.8VSG
+0.9VS +0.9VS_VGA
+1.1VS_GPU +VCCP
1.715A
JP4
Do Not Stuff
/X
Use +1.05VS(+VCCP) for +1.1VS rail
BOM:02G190014113
P80VC1
Title :
ASUSTeK COMPUTER INC. NB1
Engineer: SZ_NB2
Size Custom
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 19 of 52

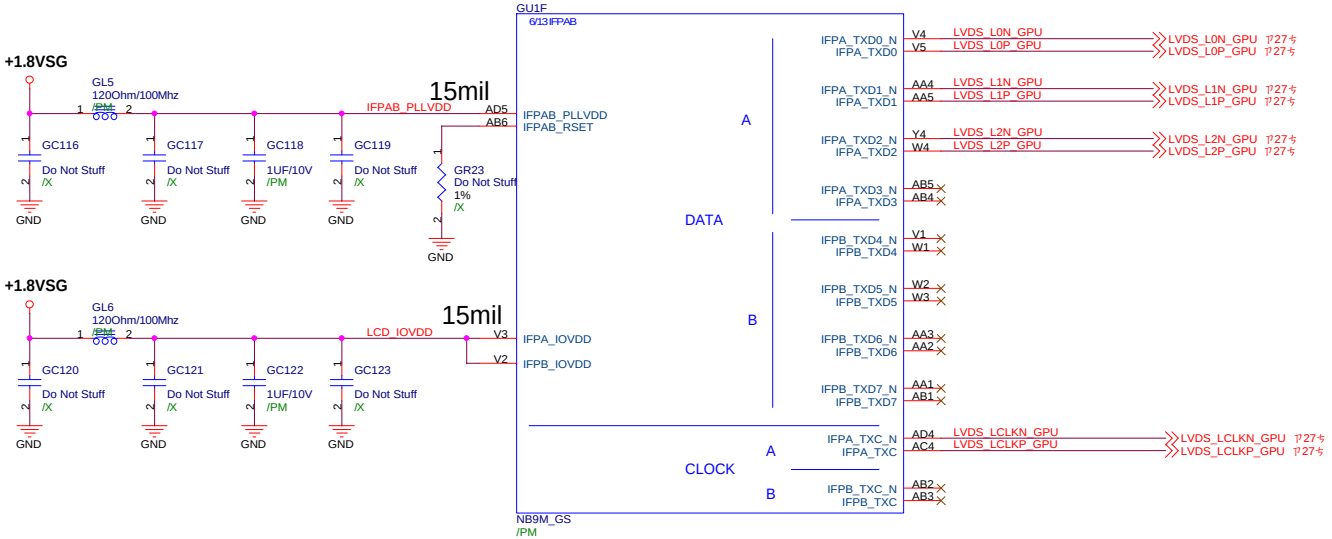



FBAWDQS[0..7]
FBARDQS[0..7]
FBADQM[0..7]
03G15133F114:
03G15133F211
FBAD[0..63]
GU2
GU3
GU4
GU5
K4N1G164QQ_HC25
/PM
+1.8VSG
GND
FBA_ODT
FBAVREF0
FBAVREF1
FBADQM0
FBADQM1
FBADQM2
FBADQM3
FBADQM4
FBADQM5
FBADQM6
FBADQM7
FBA_CLK1 GR14 1 2 475Ohm 1% FBA_CLK1#
FBA_CLK0 GR15 1 2 475Ohm 1% FBA_CLK0#
+1.8VSG
GR12 1KOhm 1% /PM
GR13 1KOhm 1% /PM
15mil
GR16 1KOhm 1% /PM
GR17 1KOhm 1% /PM
FBAVREF0
FBAVREF1
GC83
GC84
0.1UF/10V /PM
GC85
GC86
GC87
GC88
GC89
GC90
GC91
GC92
GC93
GC94
GC95
GC96
1UF/10V /PM
Do Not Stuff /X
+0.9VS_VGA
GC109
GC110
GC111
0.1UF/10V /PM
10UF/6.3V /PM
56Ohm
GRN1A
GRN1B
GRN1C
GRN1D
GRN1E
GRN1F
GRN1H
GRN2A
GRN2B
GRN2C
GRN2D
GRN2E
GRN2F
GRN2G
GRN2H
GRN3A
GRN3B
GRN3C
GRN3D
GRN3E
GRN3F
GRN3G
GRN3H
P80VC1
Title :
ASUSTeK COMPUTER INC. NB1
Engineer: SZ_NB2
Size Custom
Project Name P80VC / A/ Q
Rev R1.1
Date: Tuesday, December 16, 2008
Sheet 21 of 52

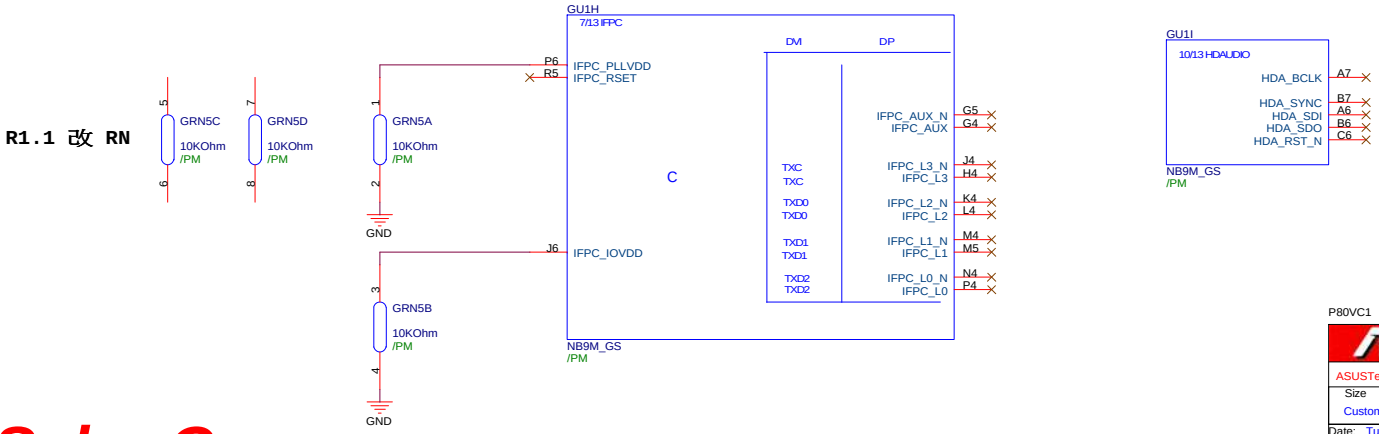
VGA



LVDS



HDMI



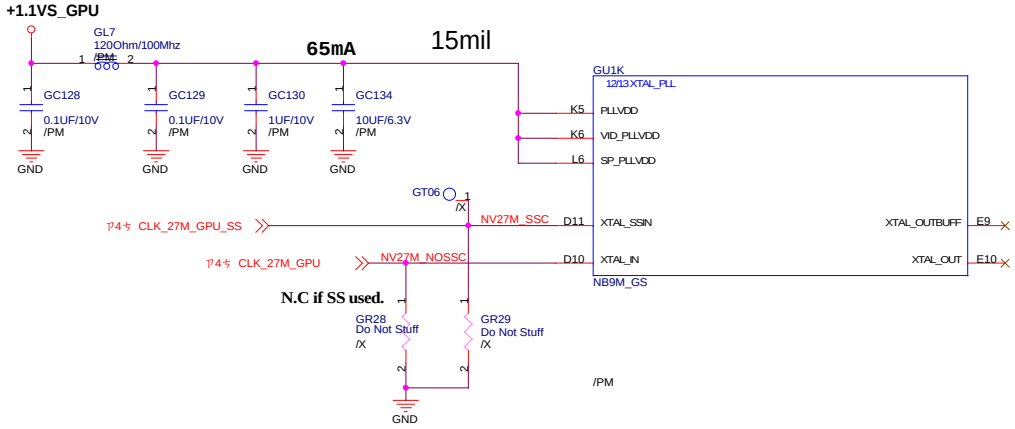
P80VC1

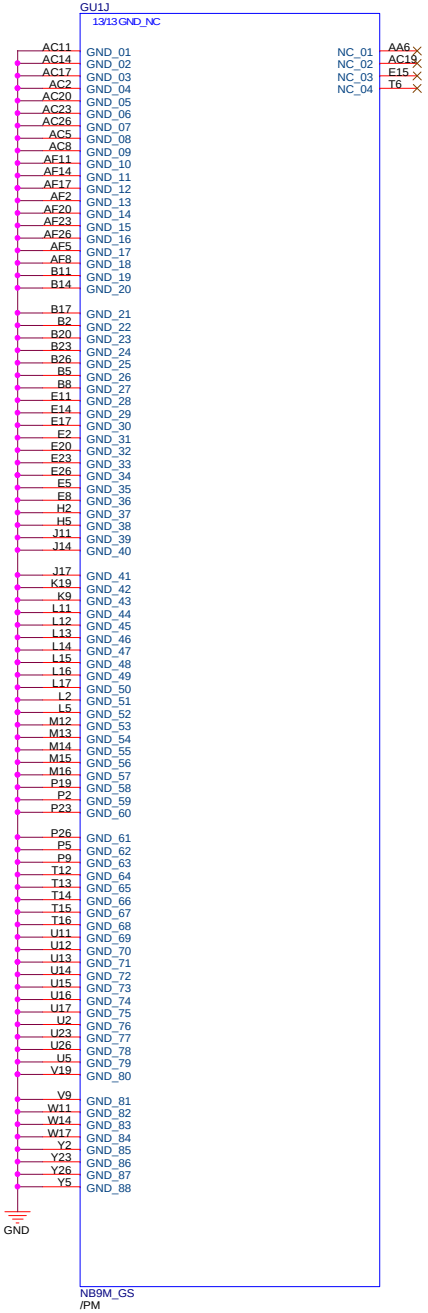
ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

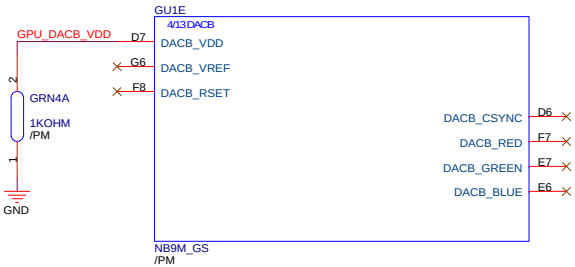
Date: Tuesday, December 16, 2008 Sheet 22 of 52

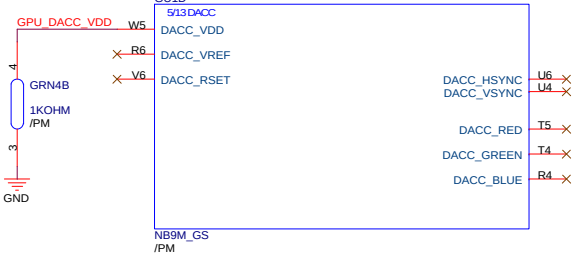
Xtal

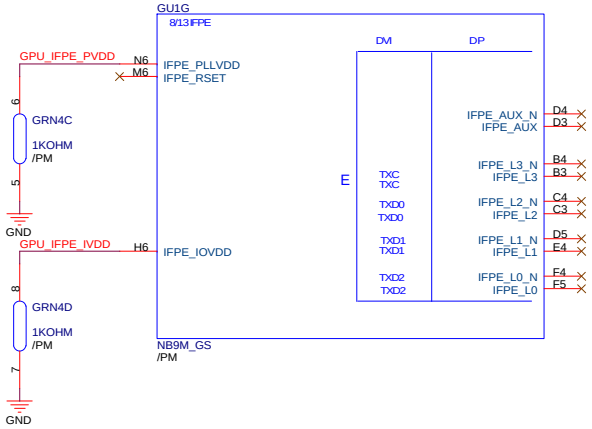




Other







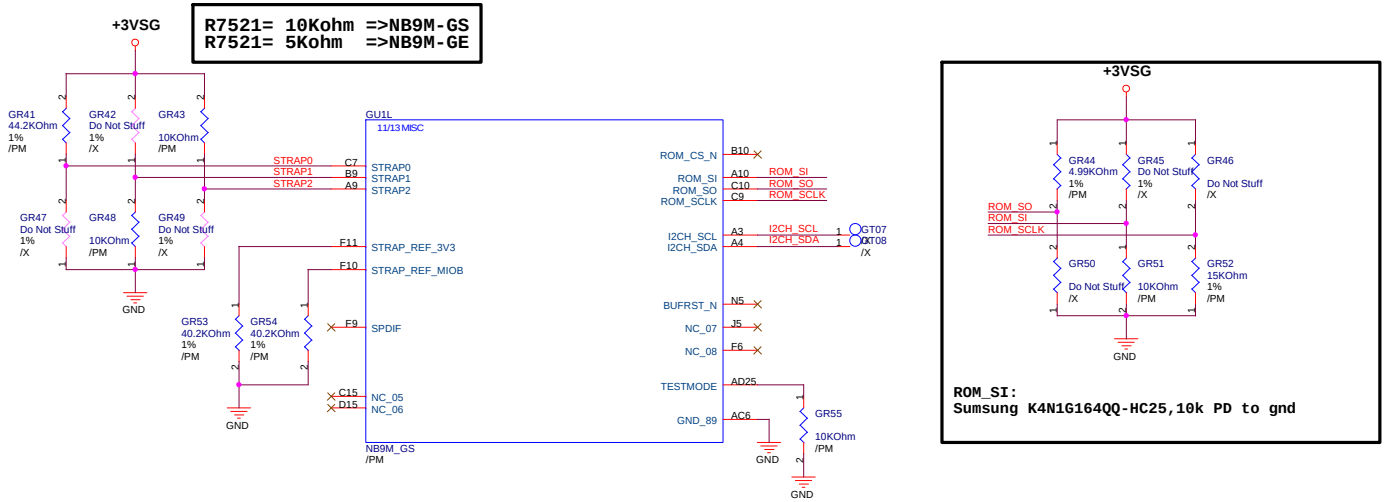
P80VC1

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A / Q	R1.1

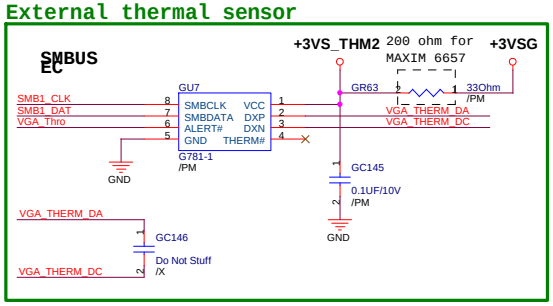
Date: Tuesday, December 16, 2008 Sheet 23 of 52

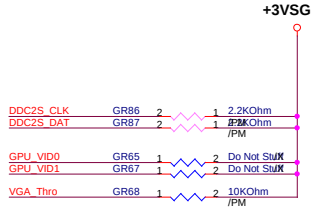
ROM

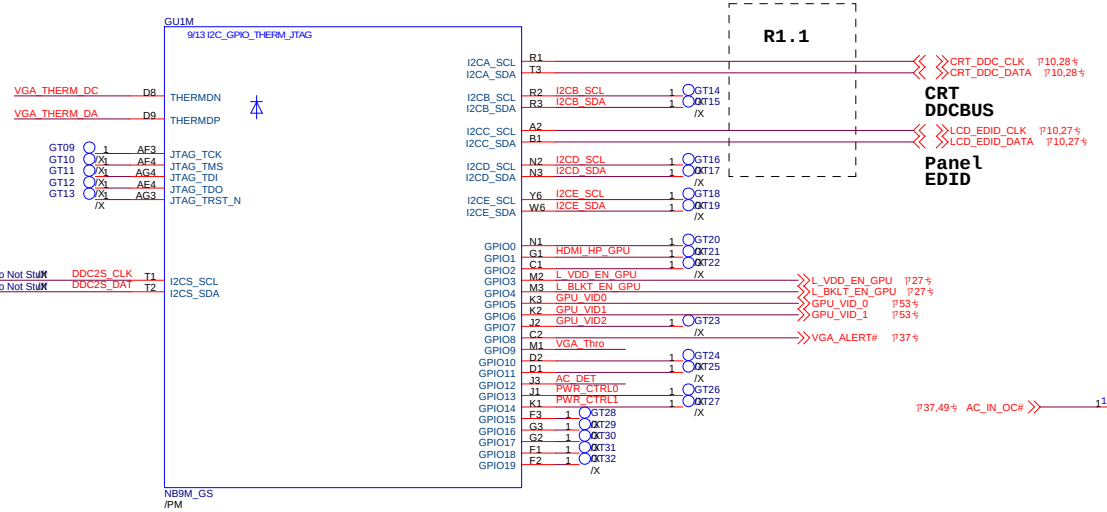


GPIO

External thermal sensor







GPIO ASSIGNMENTS

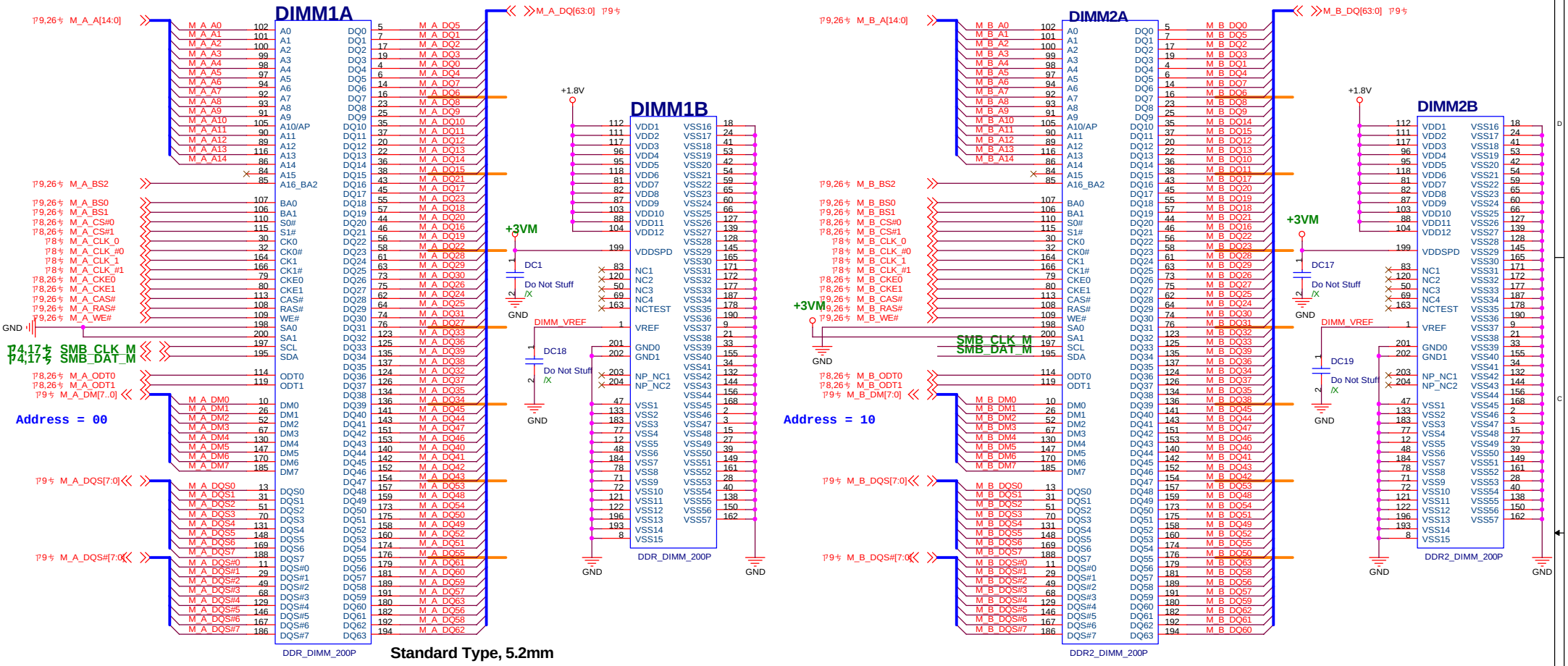
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL

P80VC1

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

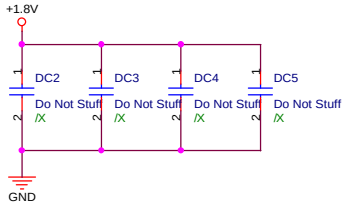
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 24 of 52



Power Cap

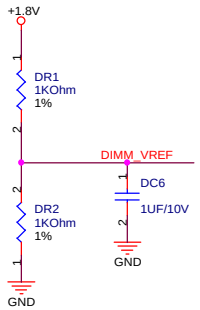
Close to DIMM



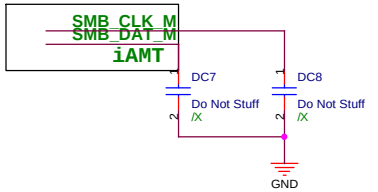
Placement at each DIMM each side by one

DIMM_VREF

Close to DIMM

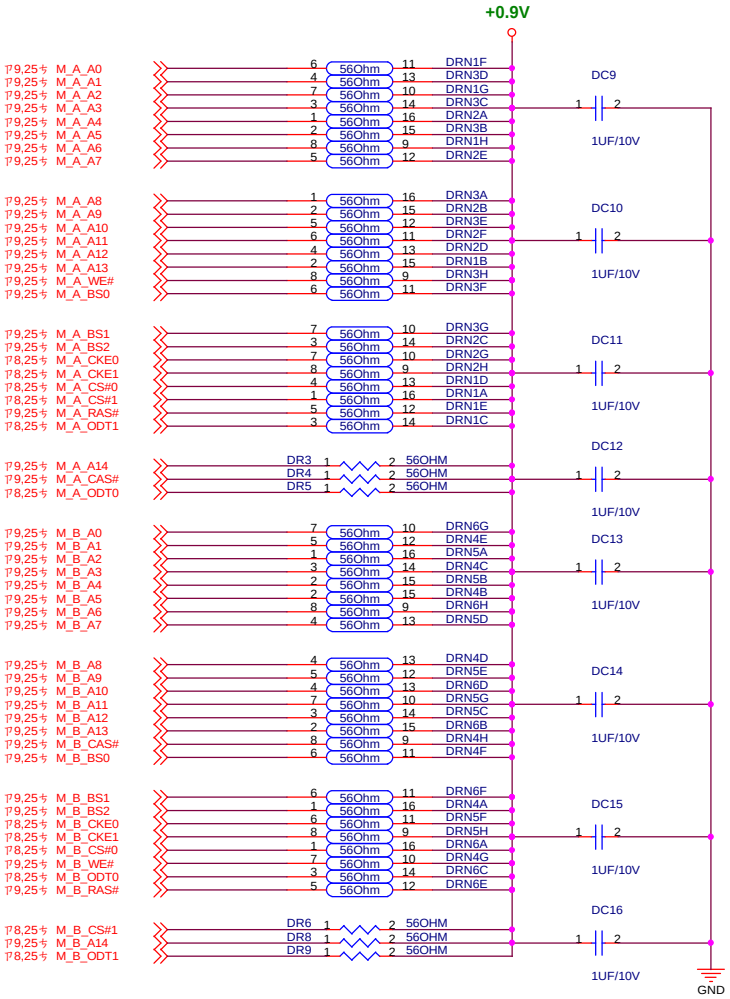


Close to DIMM



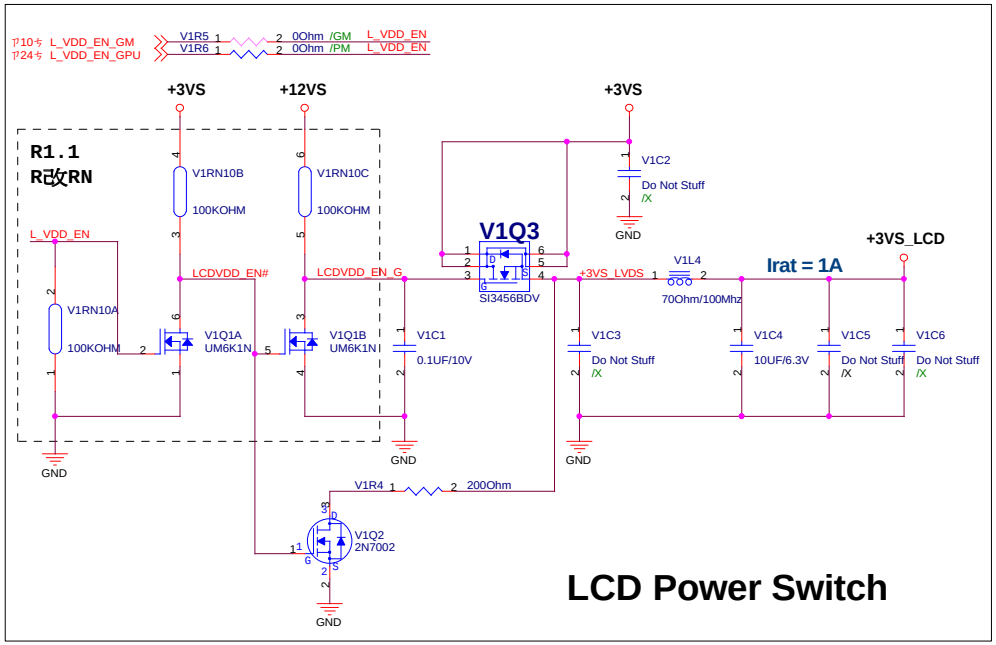
P80VC1

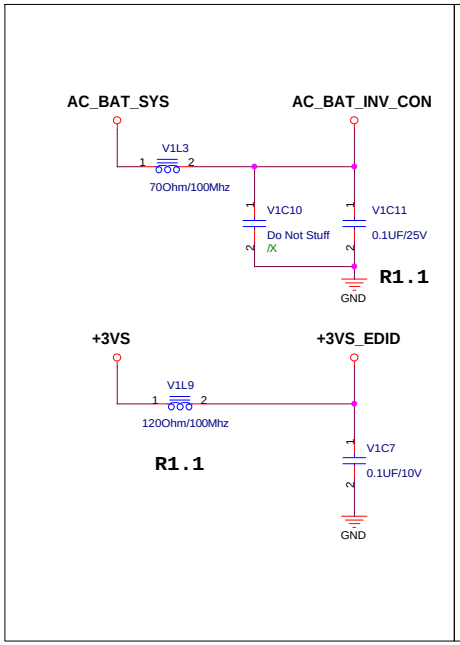
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMMs	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 25 of 52	

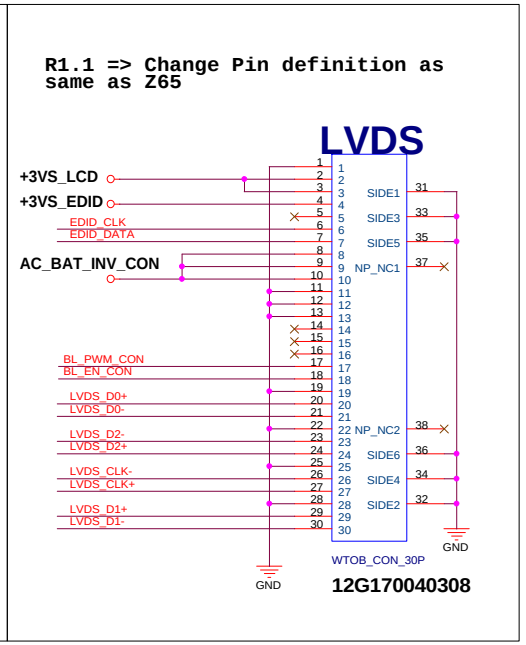


P80VC1

ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 26 of 52	





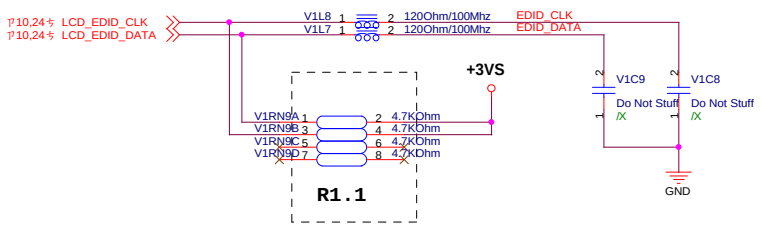


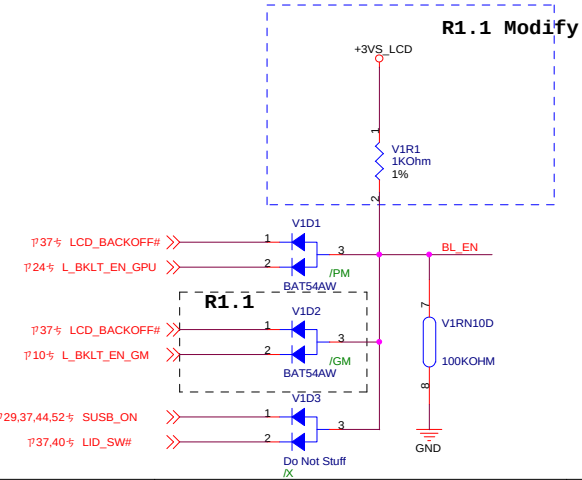
LVDS from GM

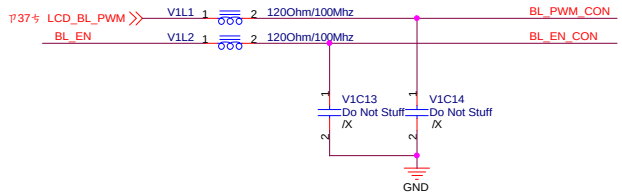
L_LCLKP_GM / L_LCLKN_GM — 0OHM /GM — V1RN1B / V1RN1A — LVDS_CLK+ / LVDS_CLK-
L_L2P_GM / L_L2N_GM — 0OHM /GM — V1RN2B / V1RN2A — LVDS_D2+ / LVDS_D2-
L_L1P_GM / L_L1N_GM — 0OHM /GM — V1RN3B / V1RN3A — LVDS_D1+ / LVDS_D1-
L_L0P_GM / L_L0N_GM — 0OHM /GM — V1RN4B / V1RN4A — LVDS_D0+ / LVDS_D0-

LVDS from GPU

L_LCLKP_GPU / L_LCLKN_GPU — 0OHM /PM — V1RN5A / V1RN5B — LVDS_CLK+ / LVDS_CLK-
L_L2P_GPU / L_L2N_GPU — 0OHM /PM — V1RN6A / V1RN6B — LVDS_D2+ / LVDS_D2-
L_L1P_GPU / L_L1N_GPU — 0OHM /PM — V1RN7A / V1RN7B — LVDS_D1+ / LVDS_D1-
L_L0P_GPU / L_L0N_GPU — 0OHM /PM — V1RN8A / V1RN8B — LVDS_D0+ / LVDS_D0-







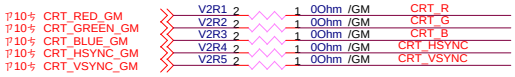
P80VC1

ASUSTeK COMPUTER INC. NB6 — Engineer: SZ_NB2

Title : LVDS conn

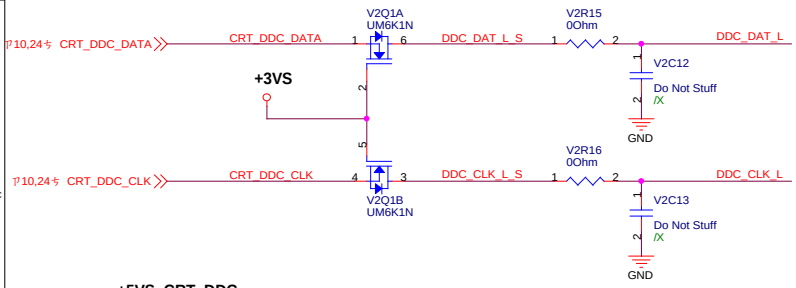
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

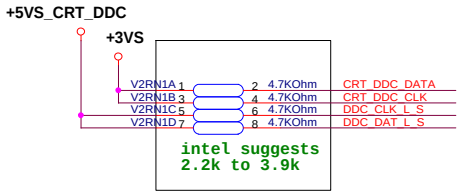
Date: Tuesday, December 16, 2008 — Sheet 27 of 52

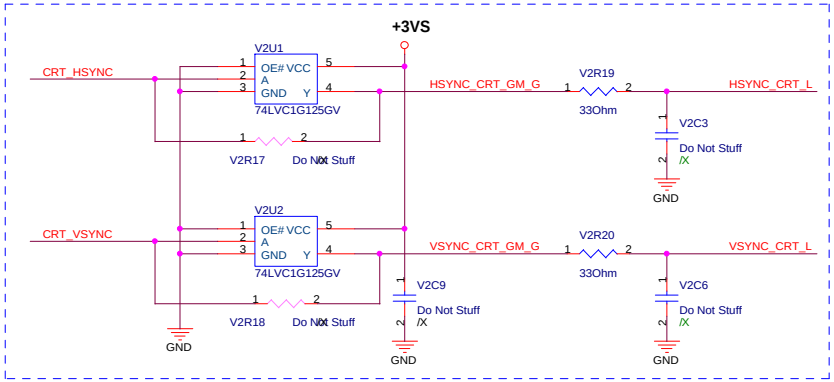


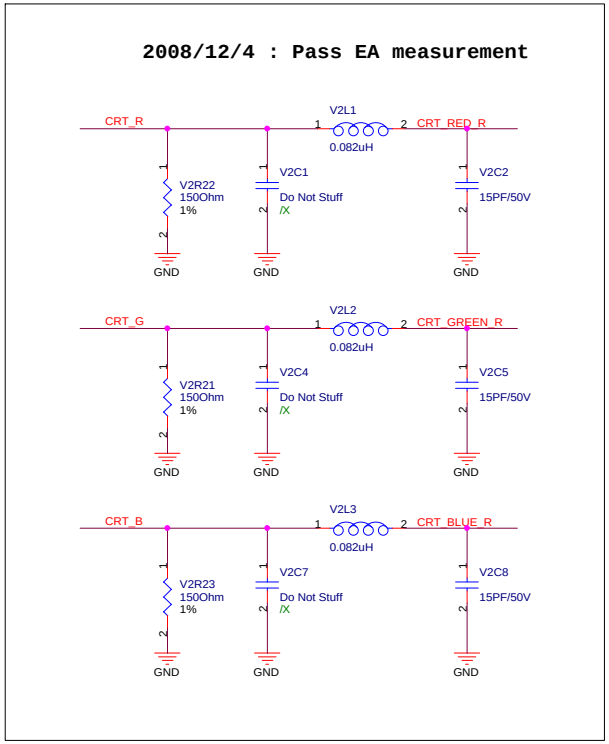
From GMCH

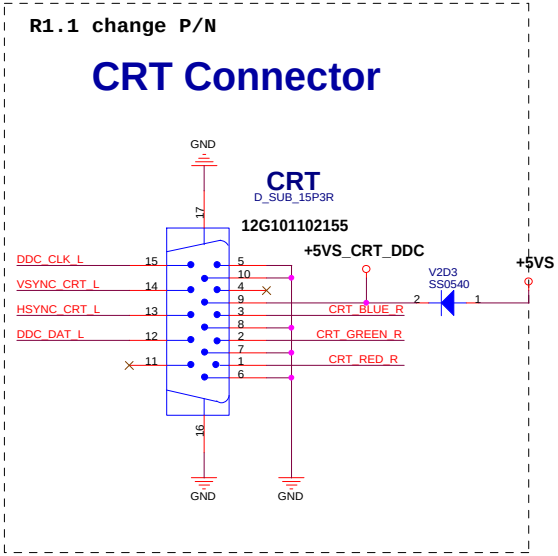
From GPU

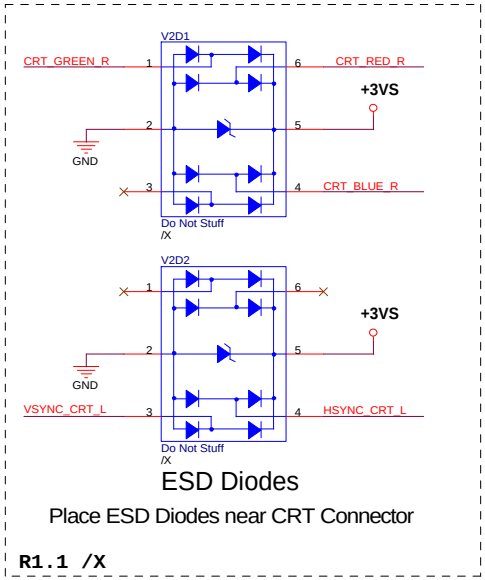






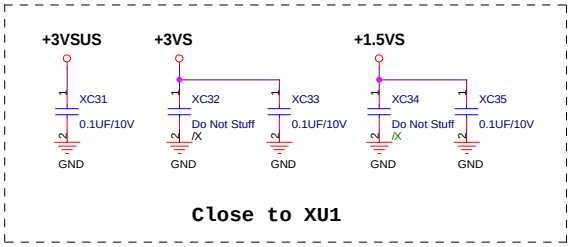


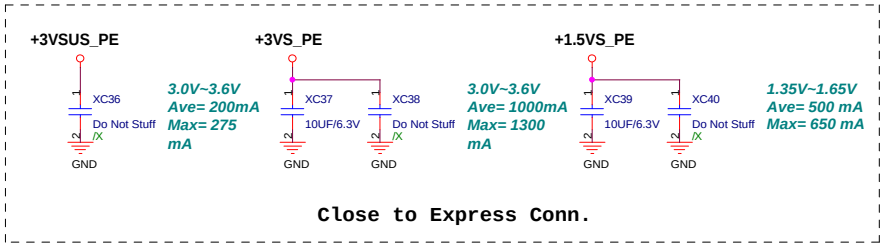




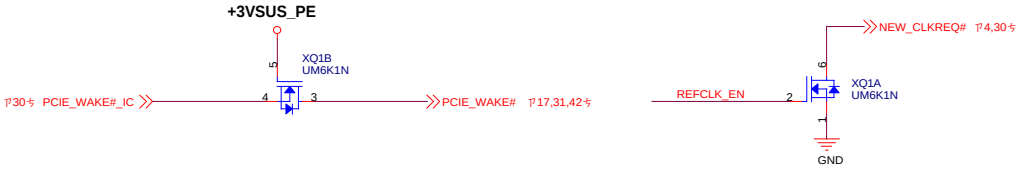
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : CRT conn	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 28 of 52	



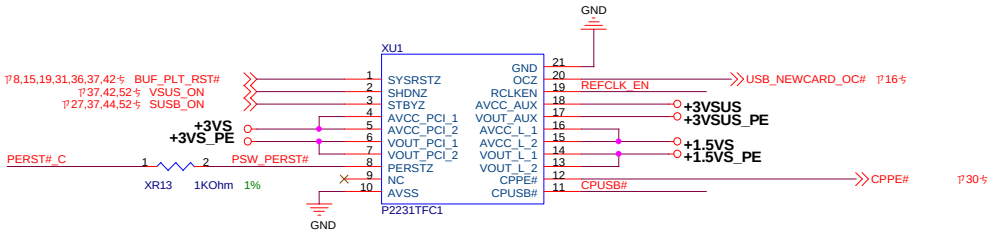


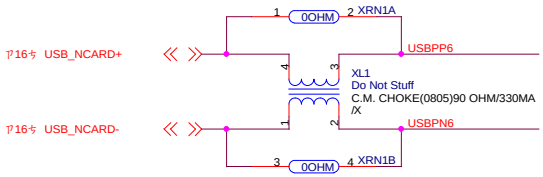
NewCard Header

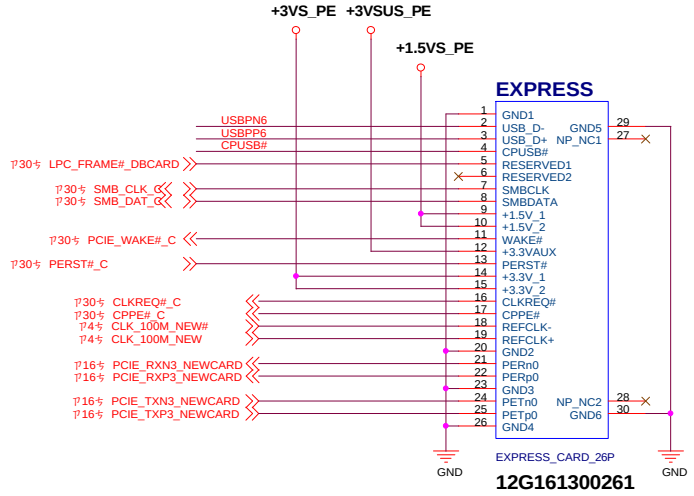


06G030057011 POWER SW. P2231TFC1 TSSOP-20 ENE P2231TFC1

06G030057012 POWER SW. P2231TFC2 TSSOP-20 ENE P2231TFC2

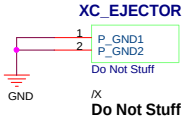






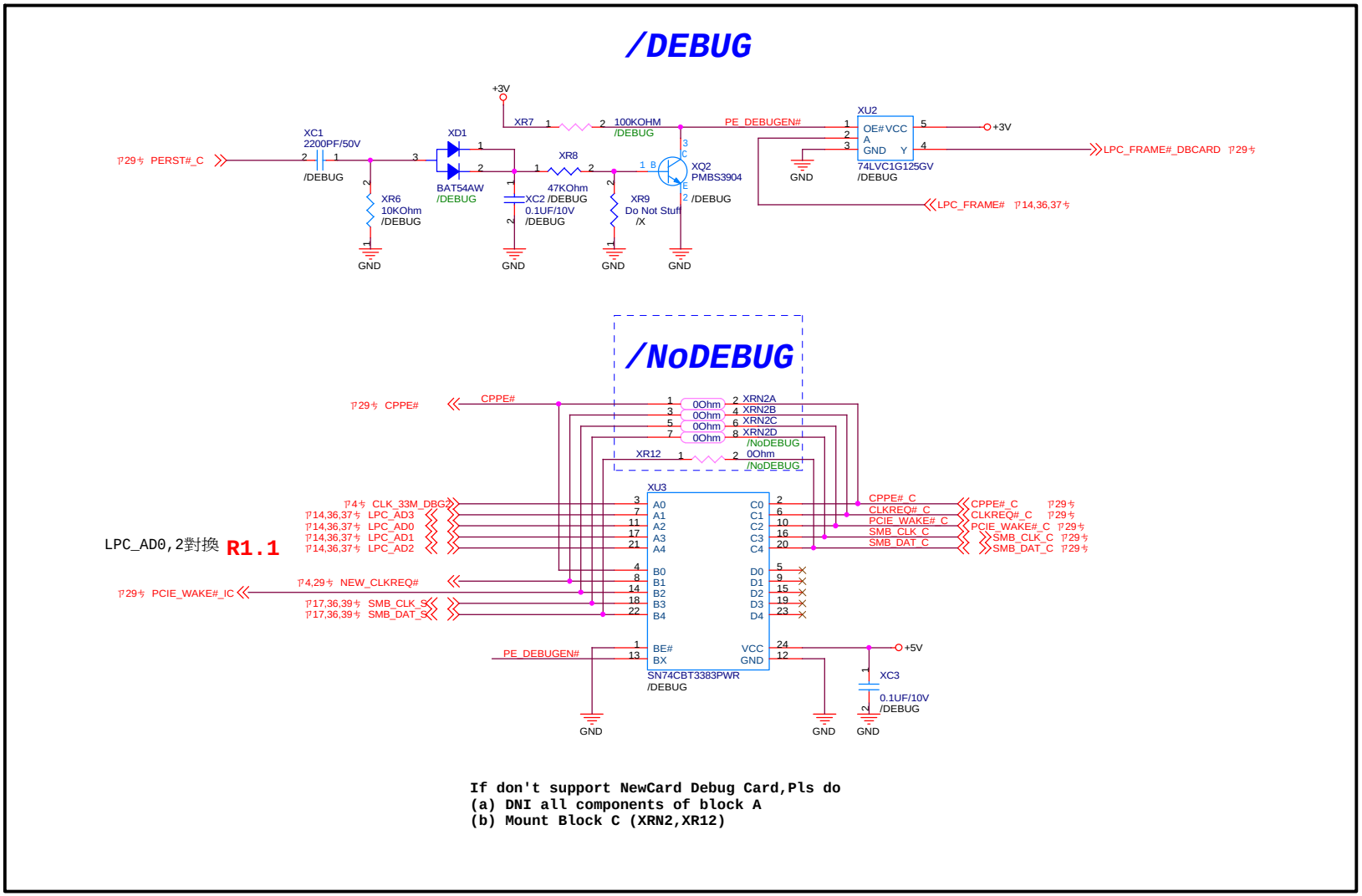
ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Ejector



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : NEWCARD	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 29 of 52	



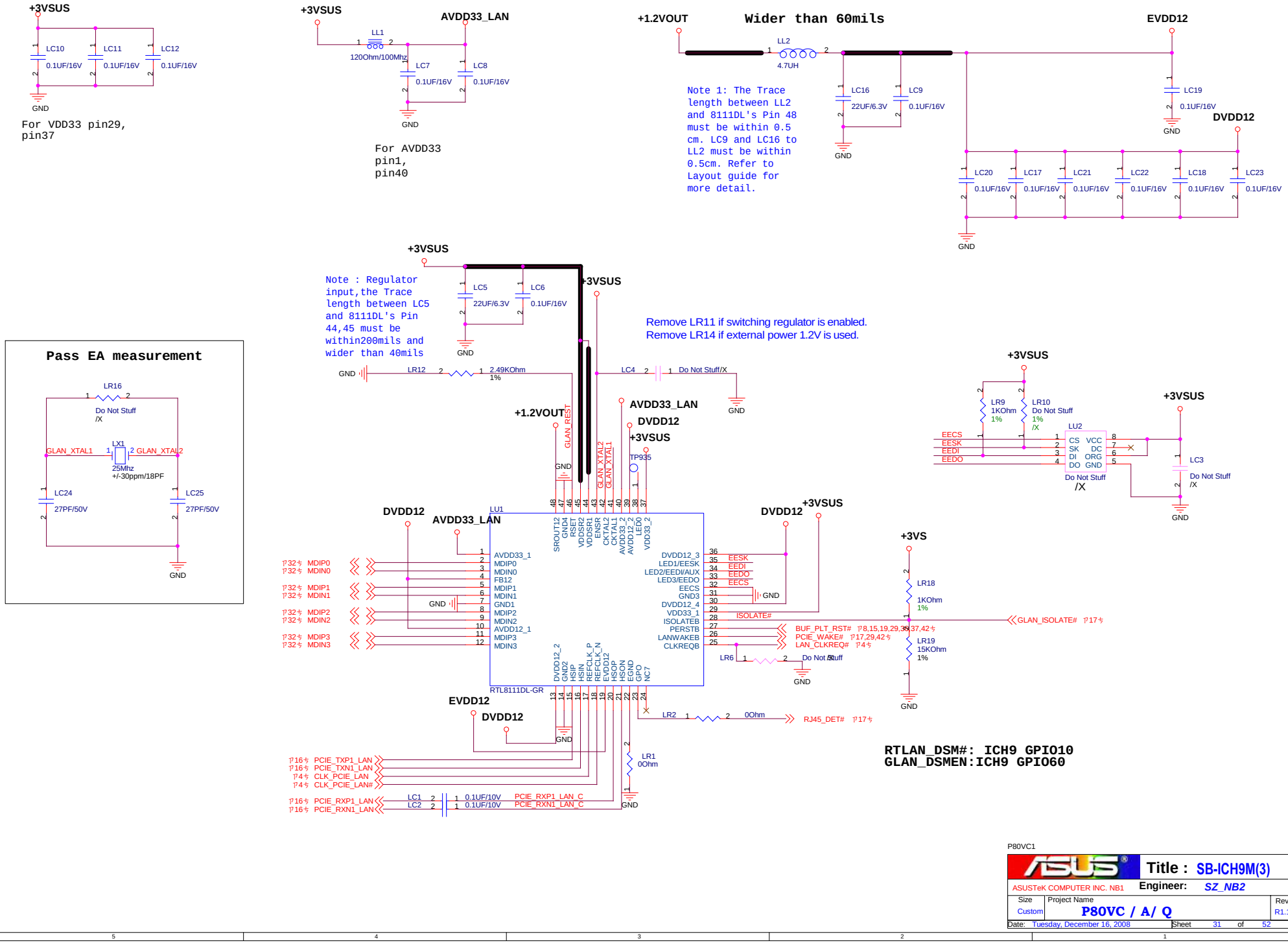
P80VC1

Title : NEWCARD_DEBUG

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 30 of 52



P80VC1

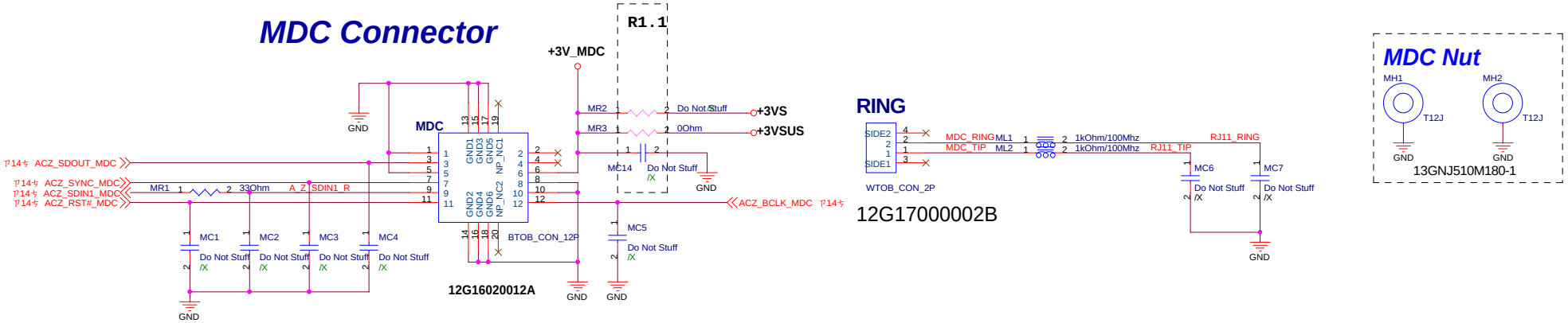
ASUSTeK COMPUTER INC. NB1

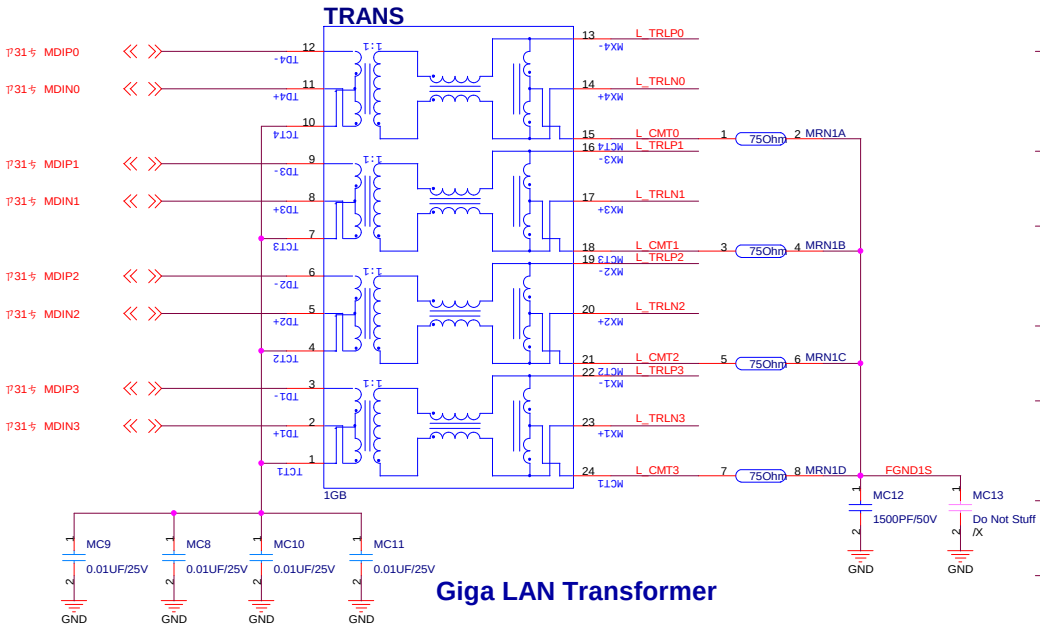
Title : SB-ICH9M(3)

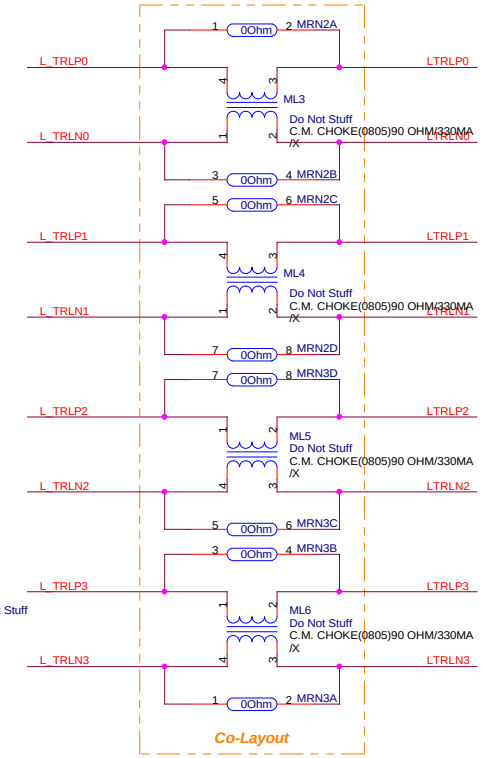
Engineer: SZ_NB2

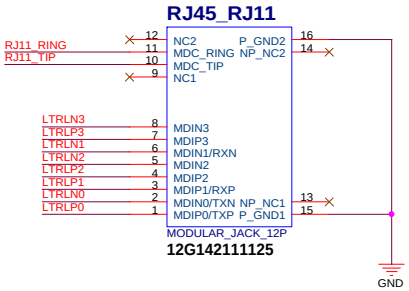
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 31 of 52









P80VC1

ASUSTeK COMPUTER INC. NB6

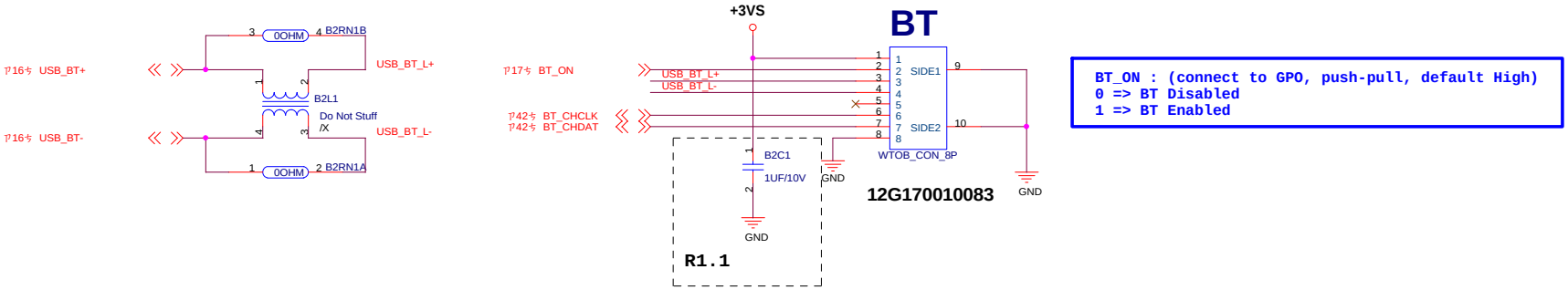
Title : RJ45-11&MDC

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 32 of 52

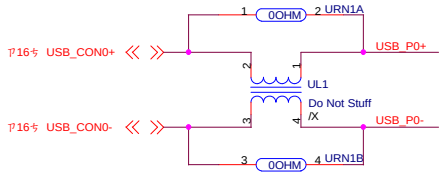
Bluetooth Connector

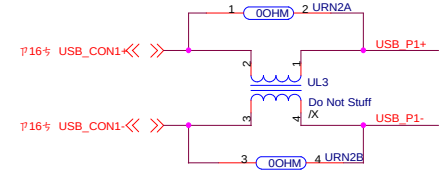


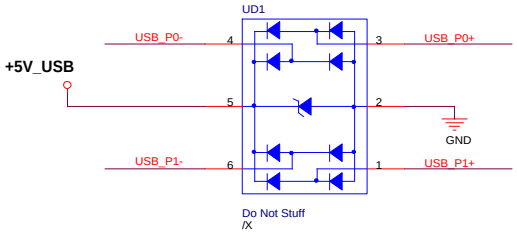

```
BT_ON : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled
```

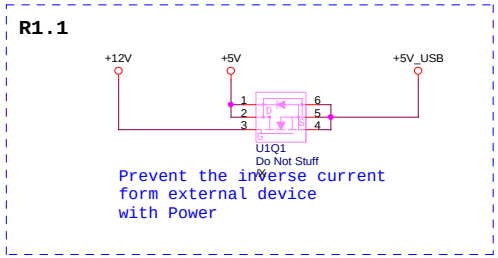
P80VC1

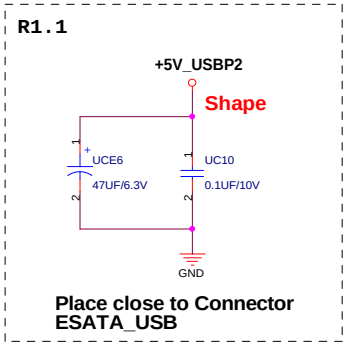
ASUSTeK COMPUTER INC. NB6	Title : BT&Launch	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 33 of 52	

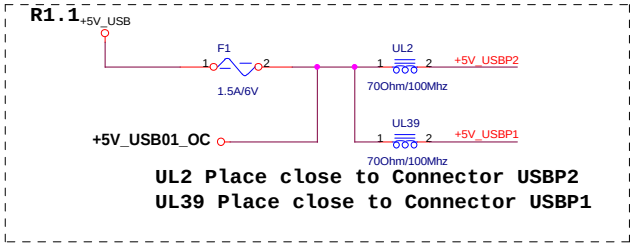


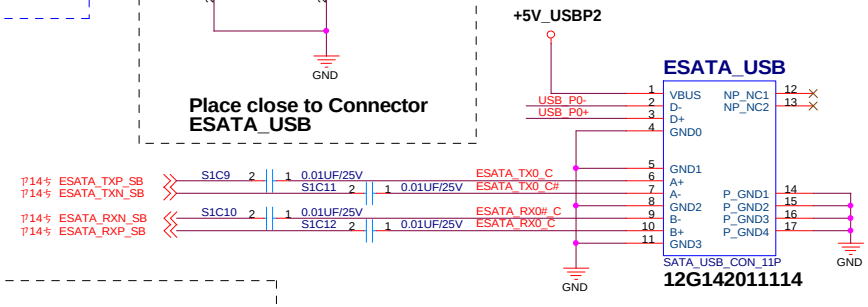


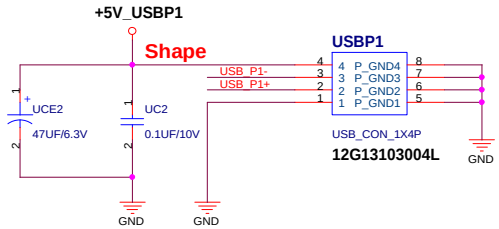








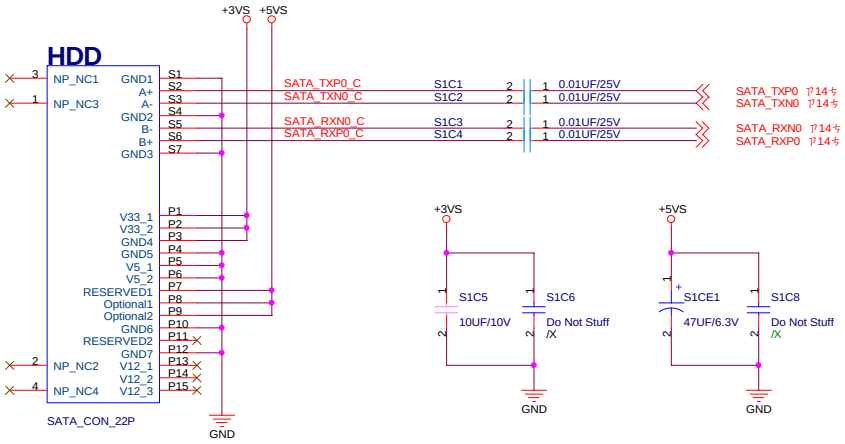




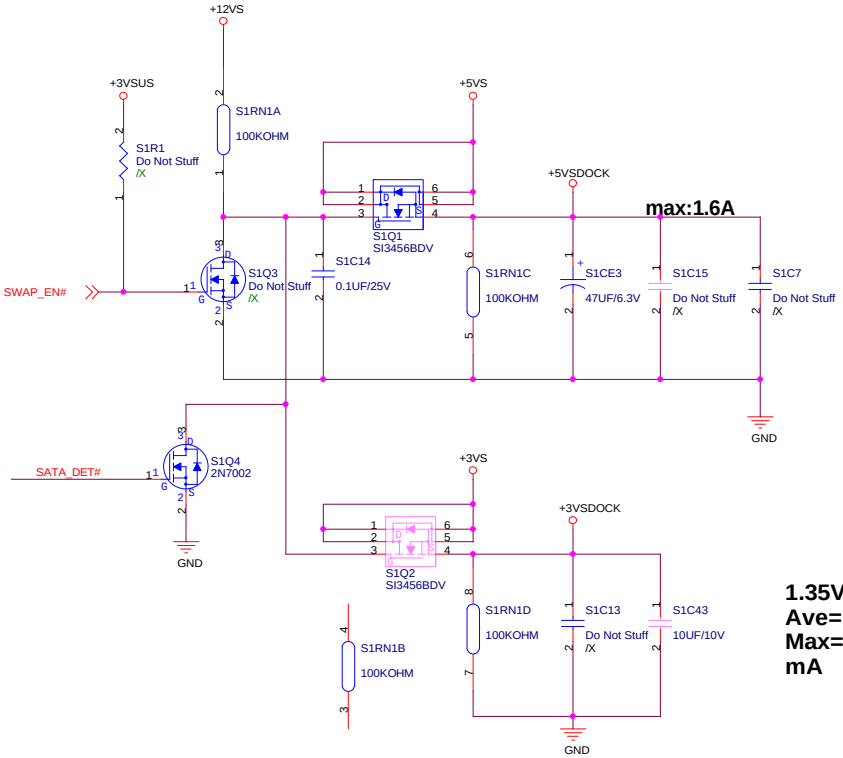
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Audio Brd con&USB x2	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 34 of 52	

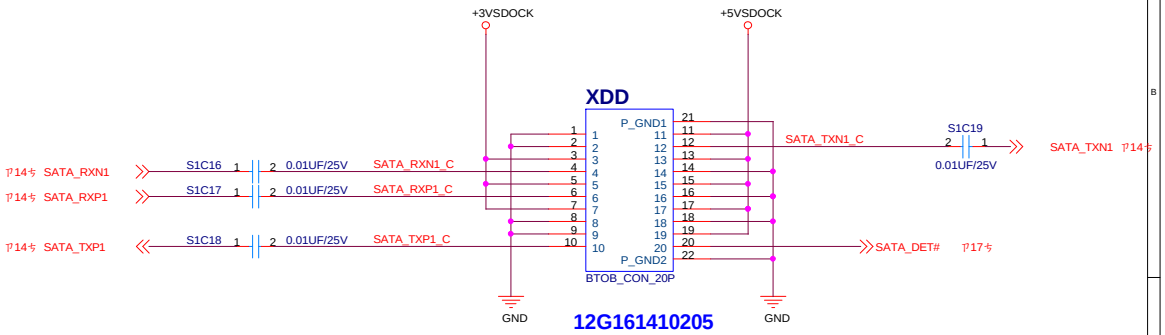
SATA HDD Connector



12G150200221



1.35V~1.65V
Ave= 500 mA
Max= 650
mA

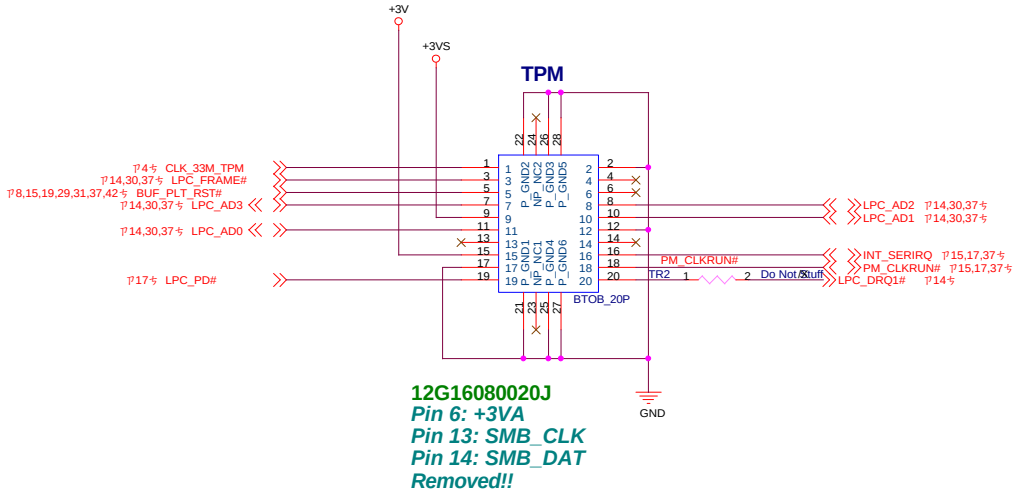


12G161410205

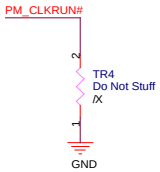
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : SATA HDD	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 35 of 52	

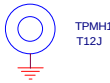
TPM Connector



12G16080020J
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
Removed!!

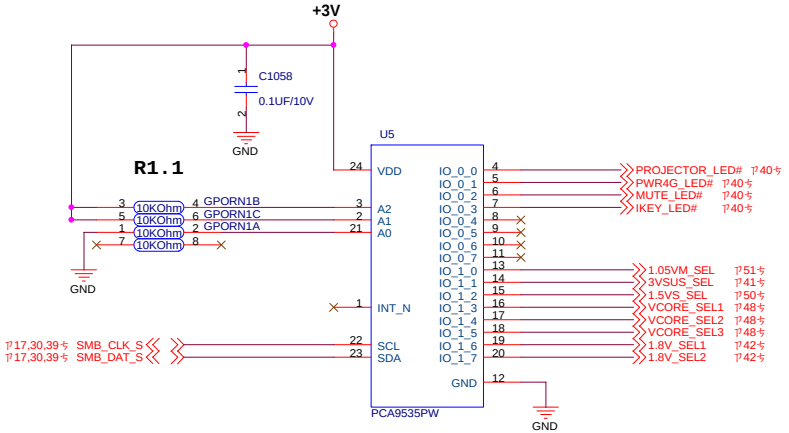


TPM Nut



13GNJ510M190-1

I2C GPIO Controller



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Debug&TPM&GPIO	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 36 of 52	

For Discrete VGA

For IT8512 Power

R1.1 POWER GOOD DETECT

For EC Reset

close to the WRST# (IT8752E pin19)

Oringinal R = 160K OHM

For PU / PD

For X'tal

Note:

Cload=12.5PF

place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

P80VC1

ASUSTeK COMPUTER INC. NB1

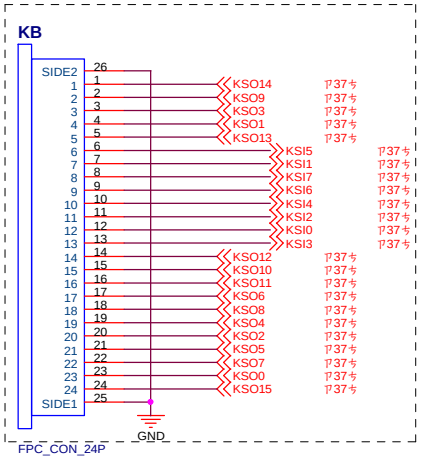
Title : EC ENE3925

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 37 of 52

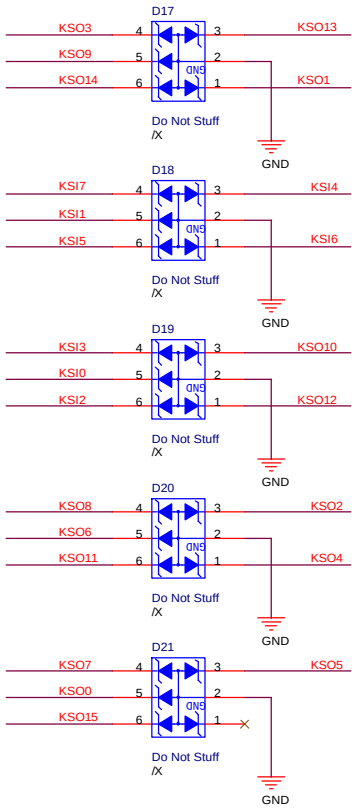
Keyboard Connector

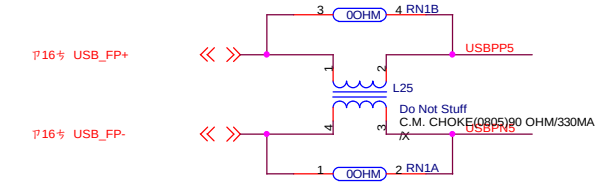


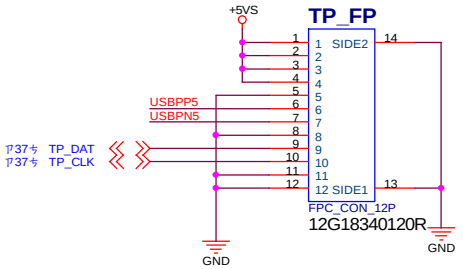
12G182102402

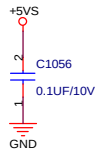
R1.1

FOR EMI/ESD

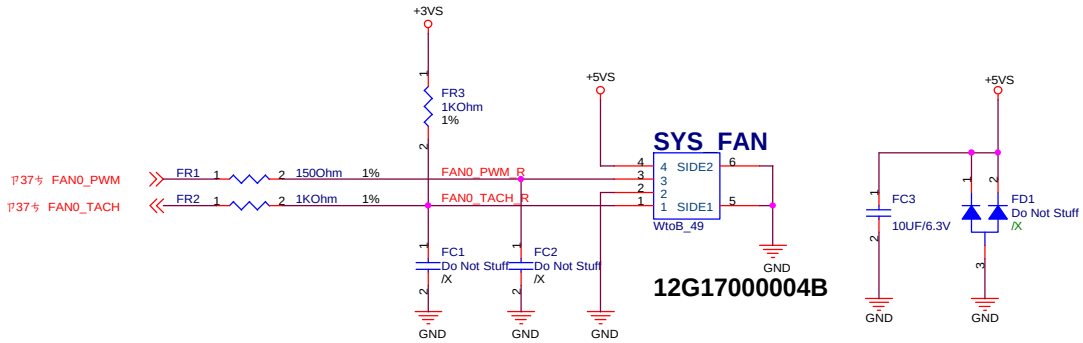








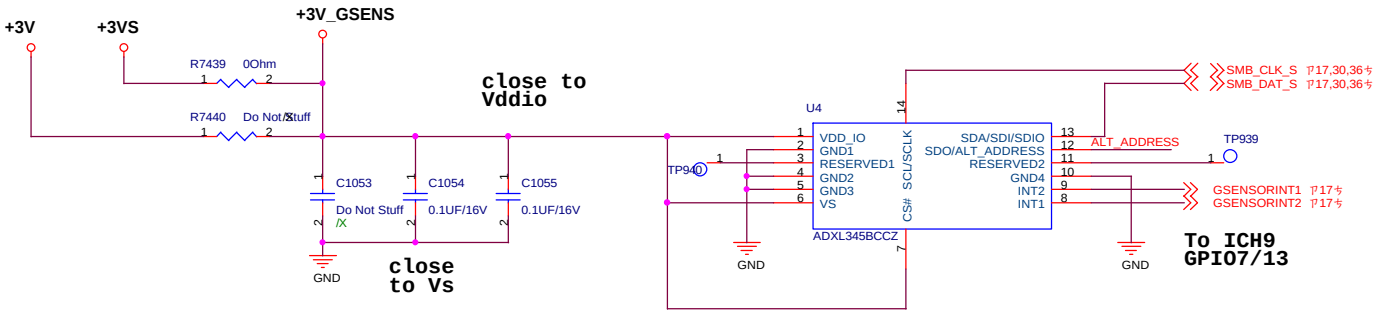
Place close to connector



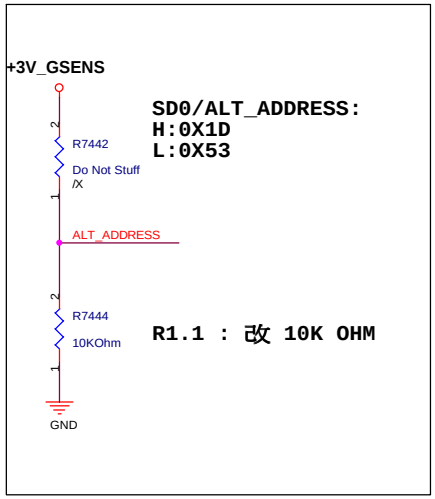
12G17000004B

P80VC1

ASUSTeK COMPUTER INC. NB6	Title : KB—TP	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 38 of 52	



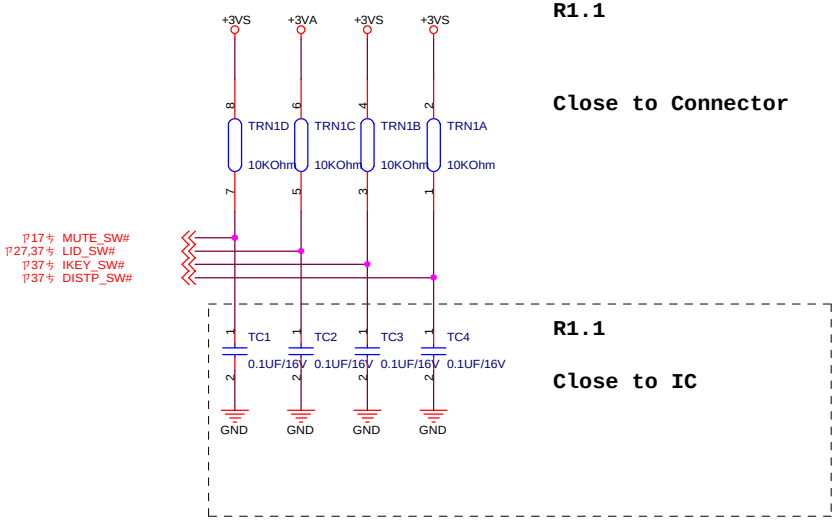
RESERVED
PIN3: connect to Vs or NC
PIN11: connect to GND or NC
CS#: Tie to Vddio to enable I2C mode.

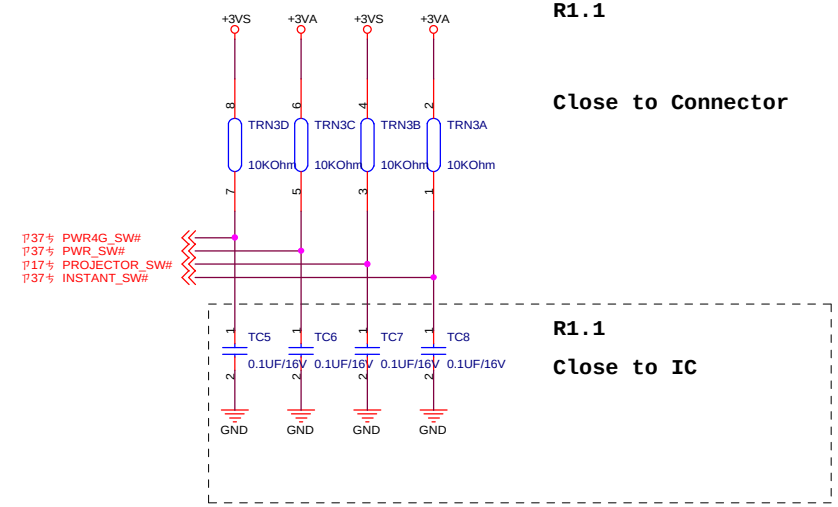


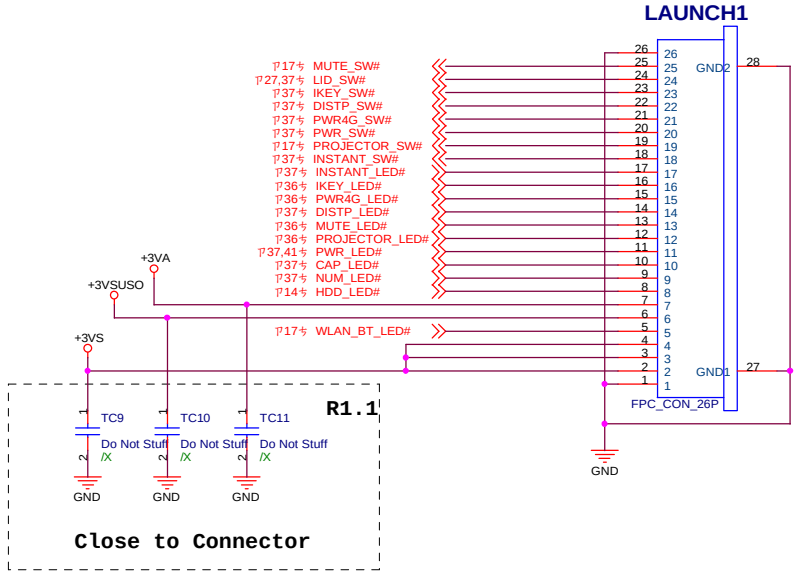
P80VC1

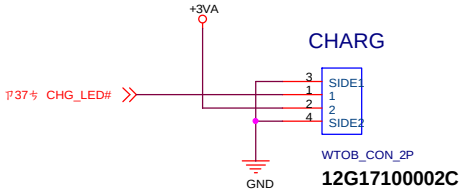
ASUSTeK COMPUTER INC. NB6	Title : Launch	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 39 of 52	

Debounced Circuits



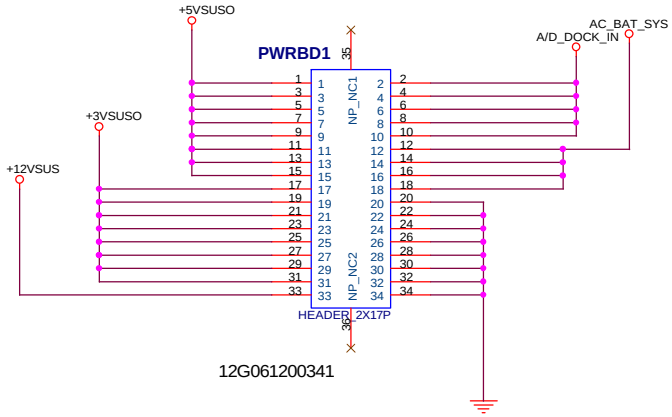




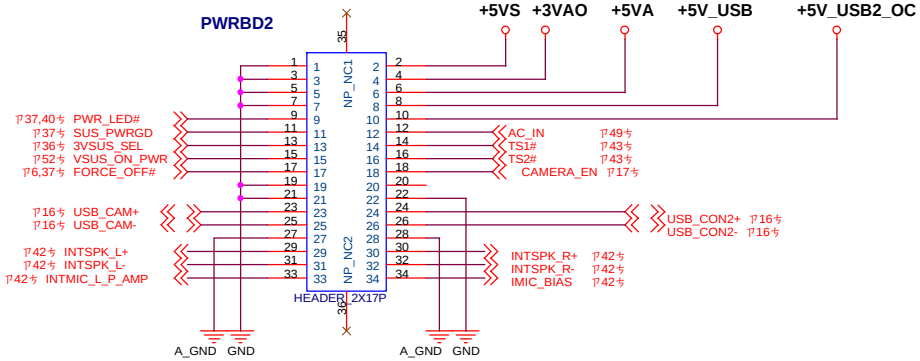


P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Launch	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 40 of 52	



12G061200341



12G061200341

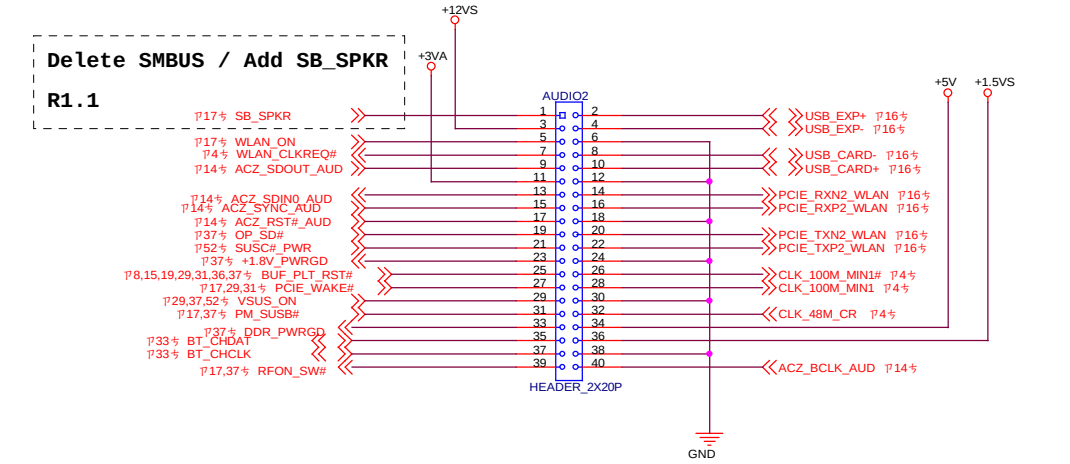
P80VC1

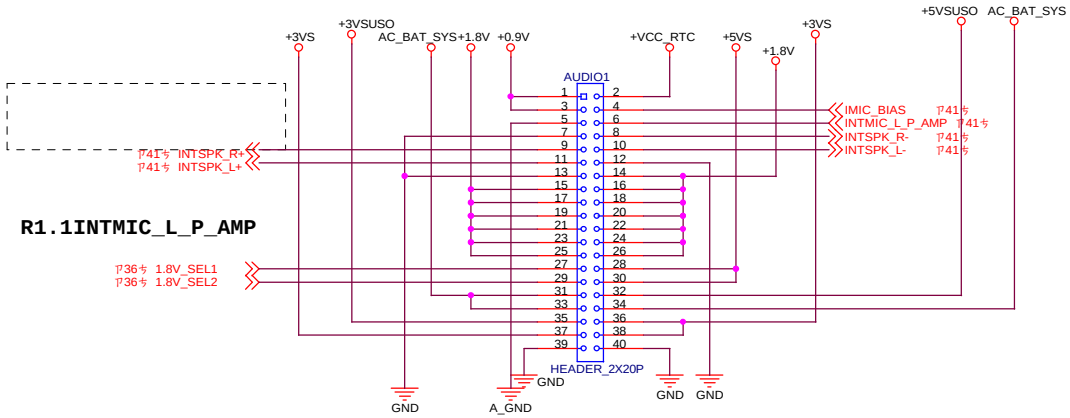
Title : other

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

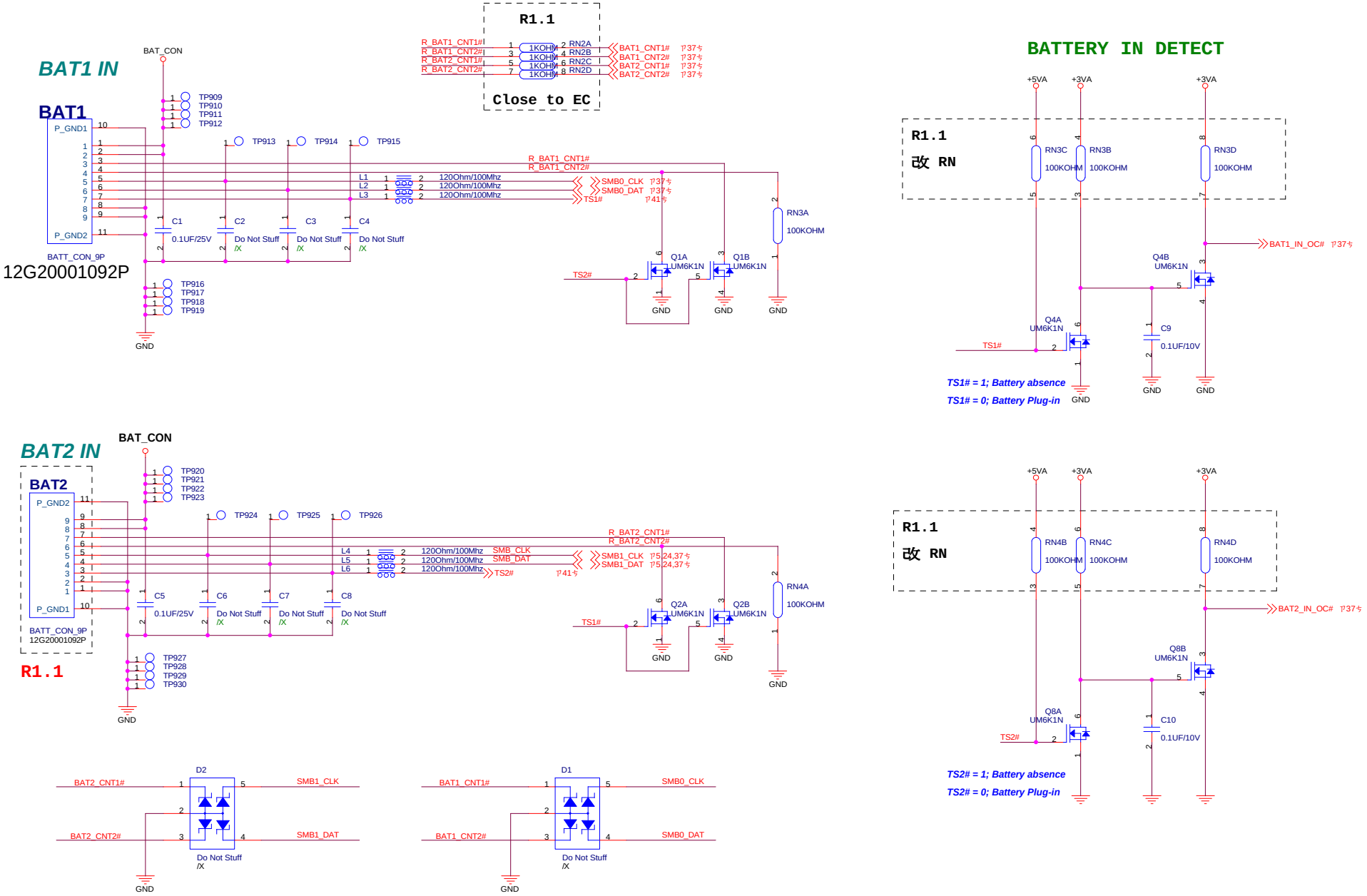
Date: Tuesday, December 16, 2008 Sheet 41 of 52





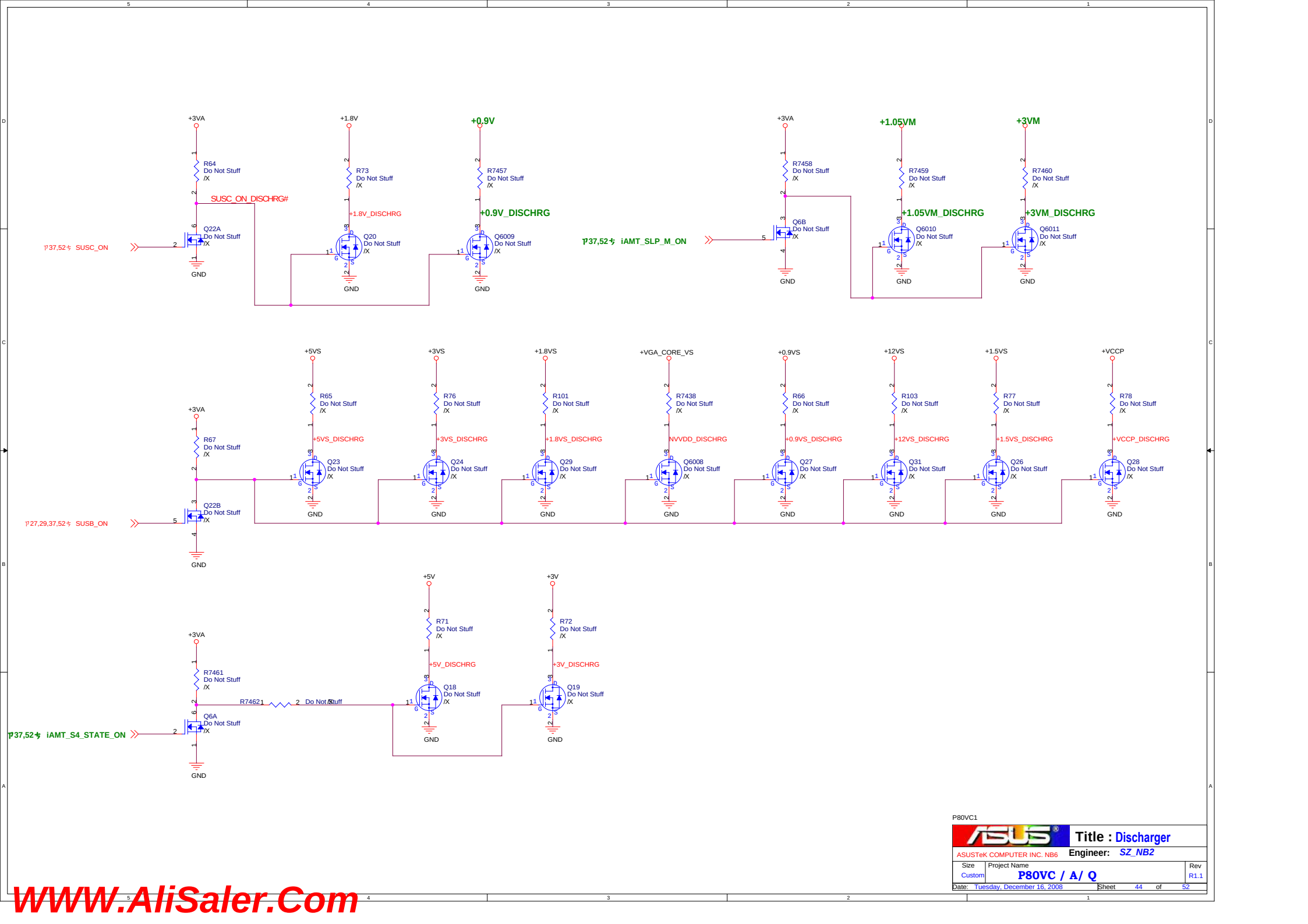
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : other	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 42 of 52	



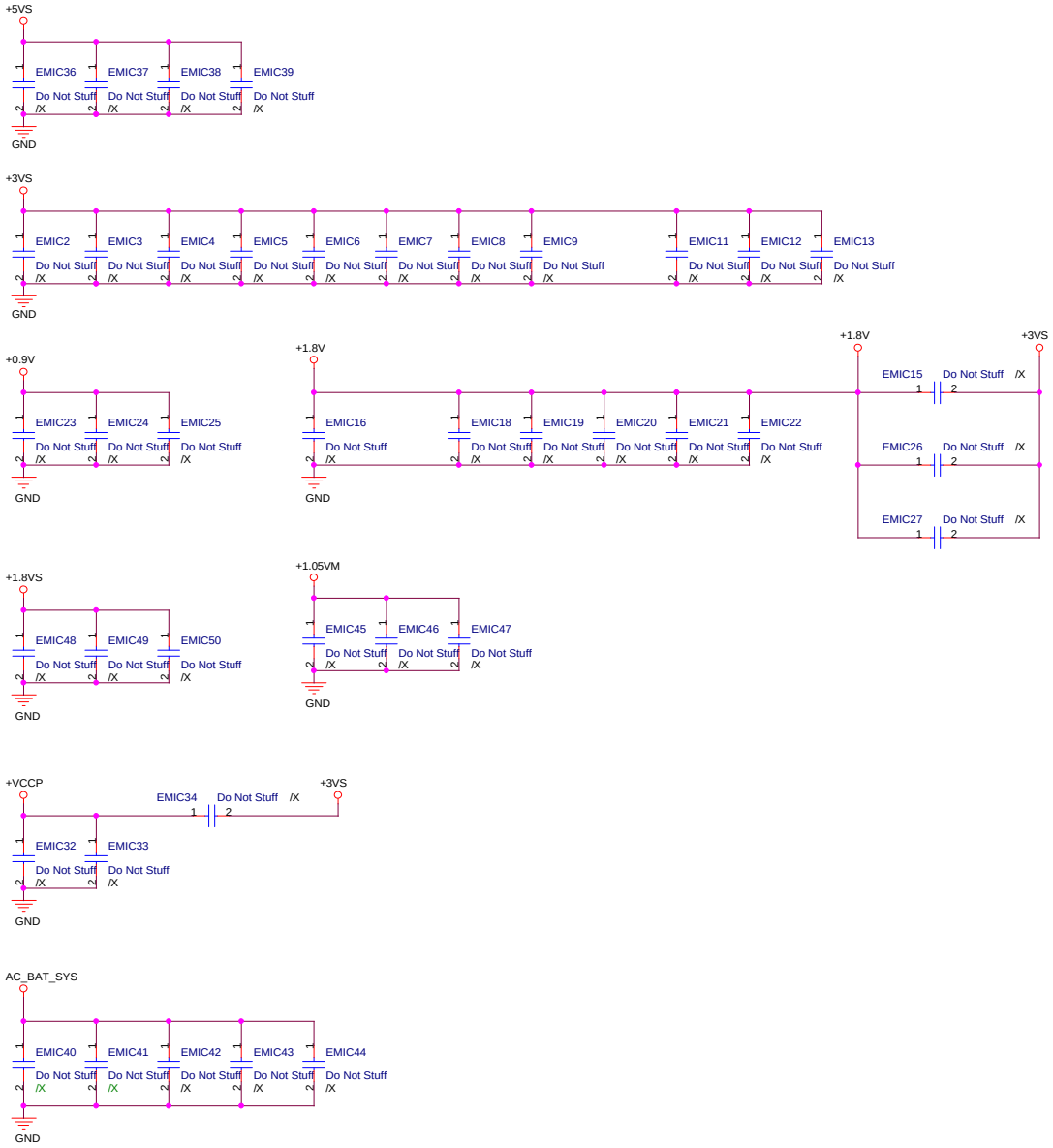
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : DC-IN&BAT-IN	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A / Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 43 of 52	



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Discharger	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 44 of 52	



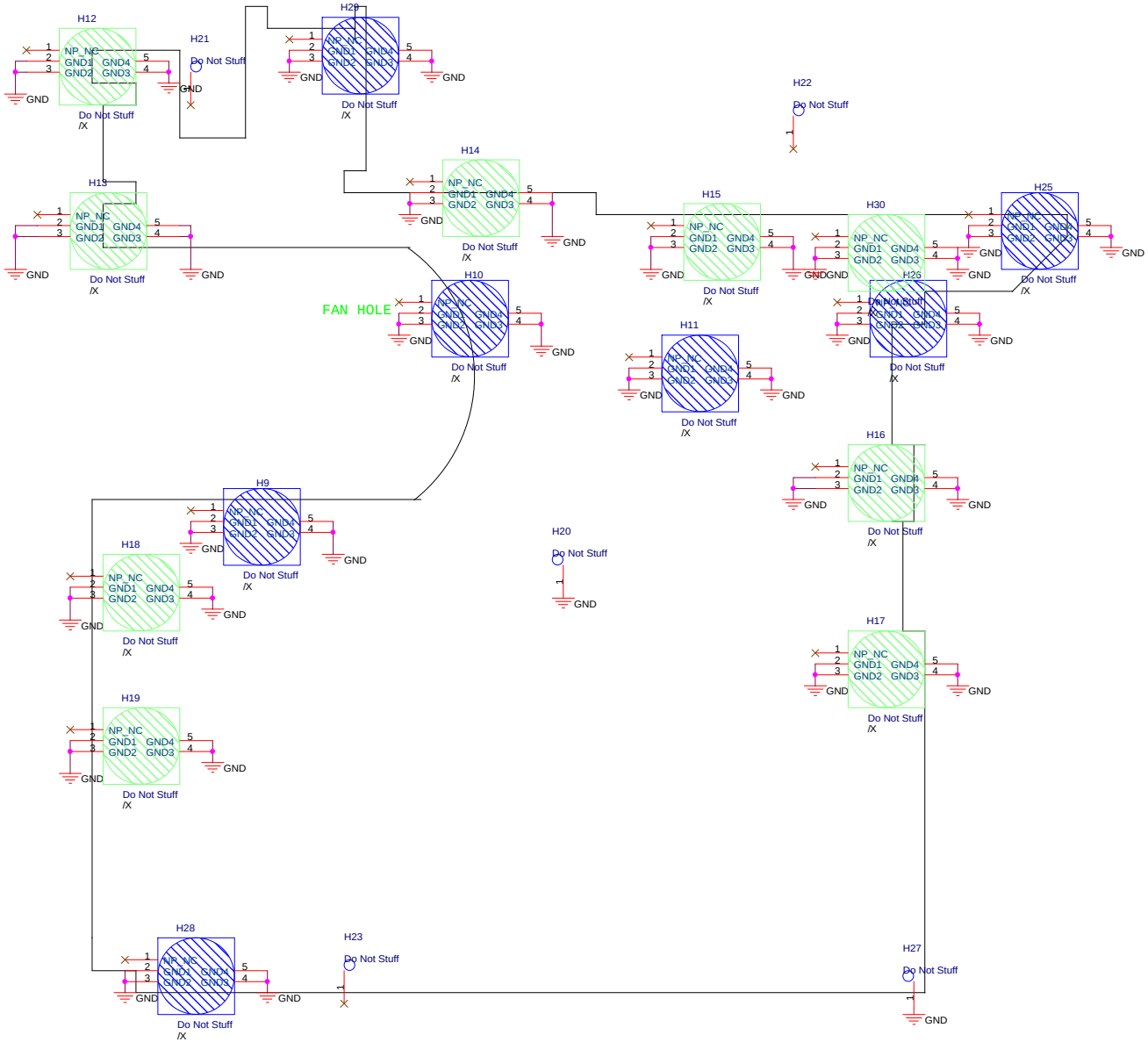
P80VC1

Title : EMI CAP

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 45 of 52



CPU HOLE

H1 H2 H3 H4

Do Not Stuff /X

NB+GPU HOLE

H5 H6 H7 H8

Do Not Stuff /X

GND

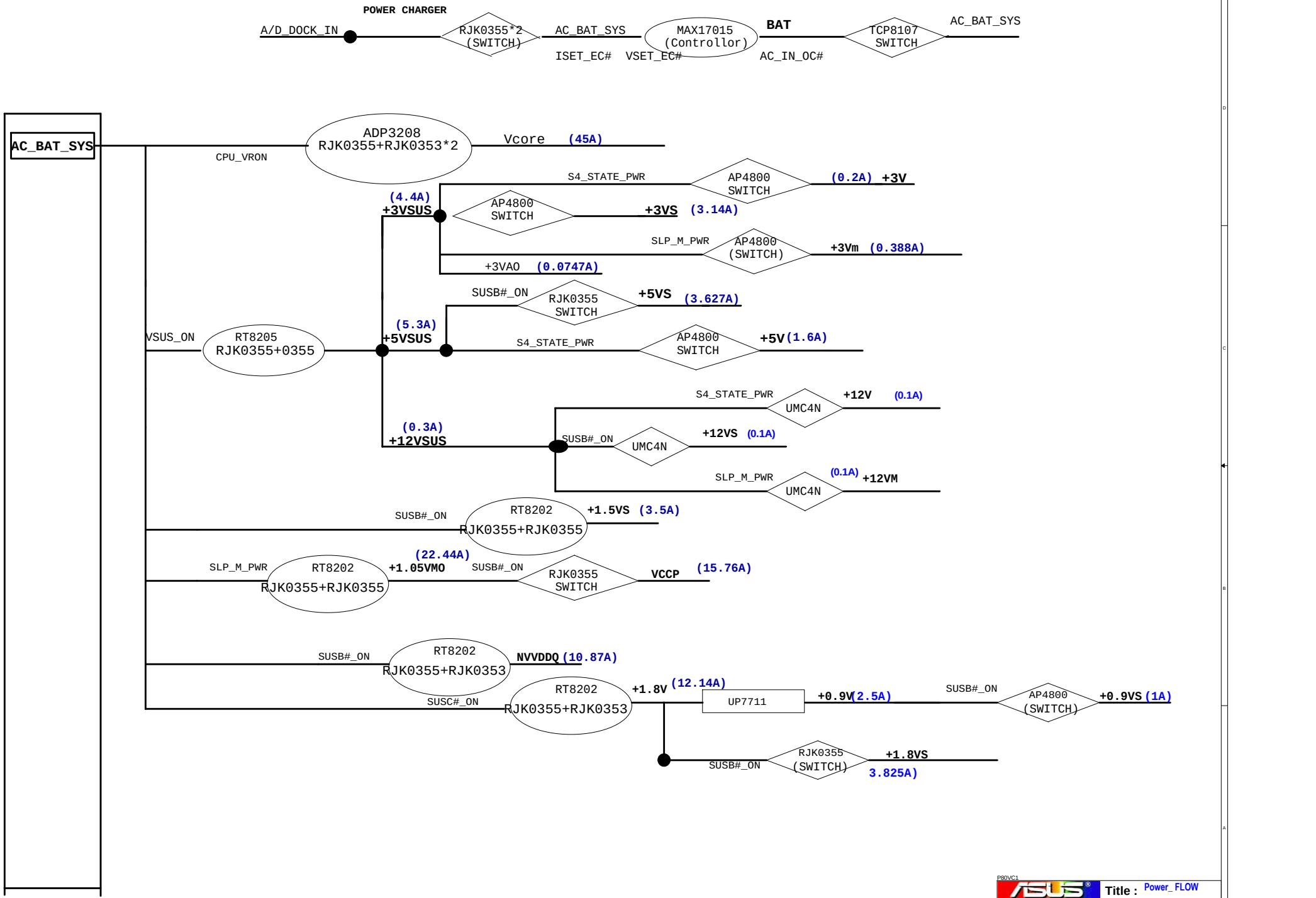
P80VC1

Title : Screw Hole

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 46 of 52



P80VC1

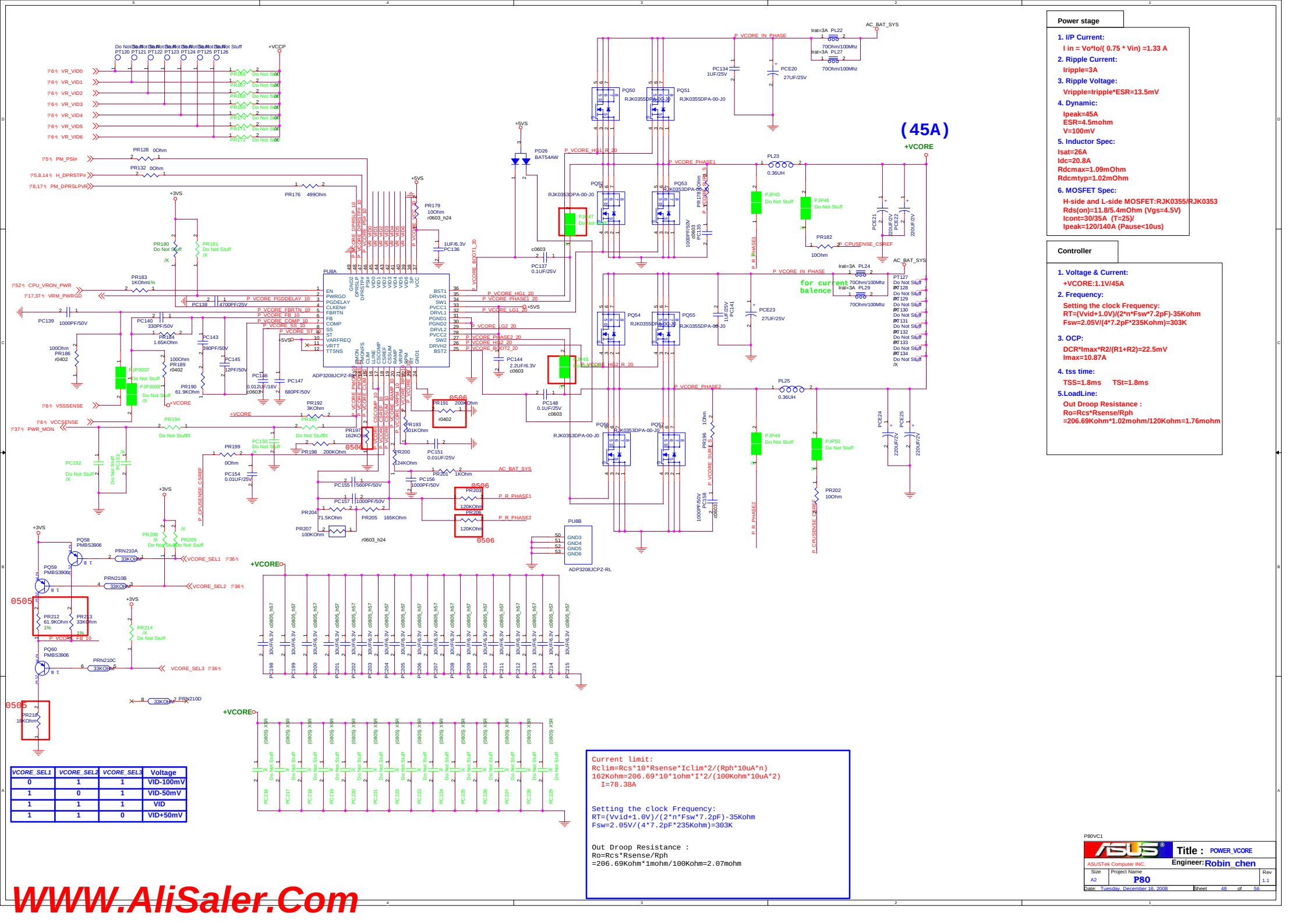
Title : Power_ FLOW

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
C	P80M	1.1

Date: Tuesday, December 16, 2008 Sheet 47 of 54



Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=45A
   ESR=4.5mohm
   V=100mV
5. Inductor Spec:
   Isat=26A
   Idc=20.8A
   Rdcmax=1.09mOhm
   Rdcmtyp=1.02mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355/RJK0353
   Rds(on)=11.8/5.4mOhm (Vgs=4.5V)
   Icont=30/35A (T=25)/
   Ipeak=120/140A (Pause<10us)

Controller

1. Voltage & Current:
   +VCORE:1.1V/45A
2. Frequency:
   Setting the clock Frequency:
   RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
   Fsw=2.05V/(4*7.2pF*235Kohm)=303K
3. OCP:
   DCR*Imax*R2/(R1+R2)=22.5mV
   Imax=10.87A
4. tss time:
   TSS=1.8ms TSt=1.8ms
5. LoadLine:
   Out Droop Resistance :
   Ro=Rcs*Rsense/Rph
   =206.69Kohm*1.02mohm/120Kohm=1.76mohm

VCORE_SEL1	VCORE_SEL2	VCORE_SEL3	Voltage
0	1	1	VID-100mV
1	0	1	VID-50mV
1	1	1	VID
1	1	0	VID+50mV

Current limit:
Rclim=Rcs*10*Rsense*Iclim*2/(Rph*10uA*n)
162Kohm=206.69*10*1ohm*I*2/(100Kohm*10uA*2)
I=78.38A

Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K

Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1mohm/100Kohm=2.07mohm

P80VC1

ASUSTek Computer INC.

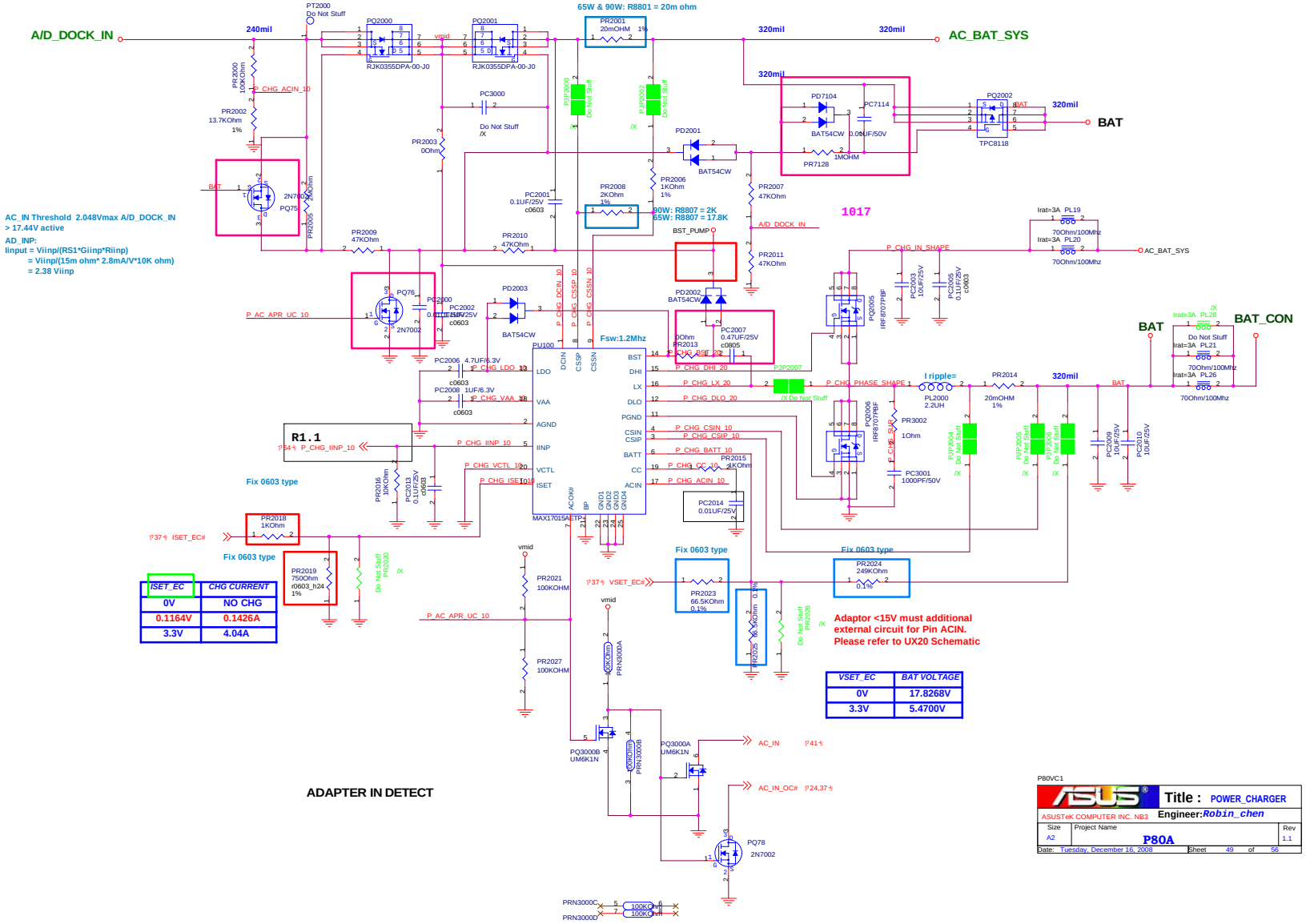
Title : POWER_VCORE

Engineer: Robin_chen

Size	Project Name	Rev
A2	P80	1.1

Date: Tuesday, December 16, 2008 Sheet 48 of 56

POWER PATH & BAT_LEARN



ISET_EC	CHG CURRENT
0V	NO CHG
0.1164V	0.1426A
3.3V	4.04A

VSET_EC	BAT VOLTAGE
0V	17.8268V
3.3V	5.4700V

Power stage

1. Ripple Current:
   Iripple=3A
2. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
3. MOSFET Spec:
   H-side and L-side MOSFET:AP4800
   Rds(on)=21mOhm (Vgs=4.5V)
   Icont=9.6 (T=25)
   Ipeak=40 (Pause<10us)

Controller

1. Frequency:
   1.2MHZ
2. Current limit
   4.5A(90W)
   3.16A(65W)

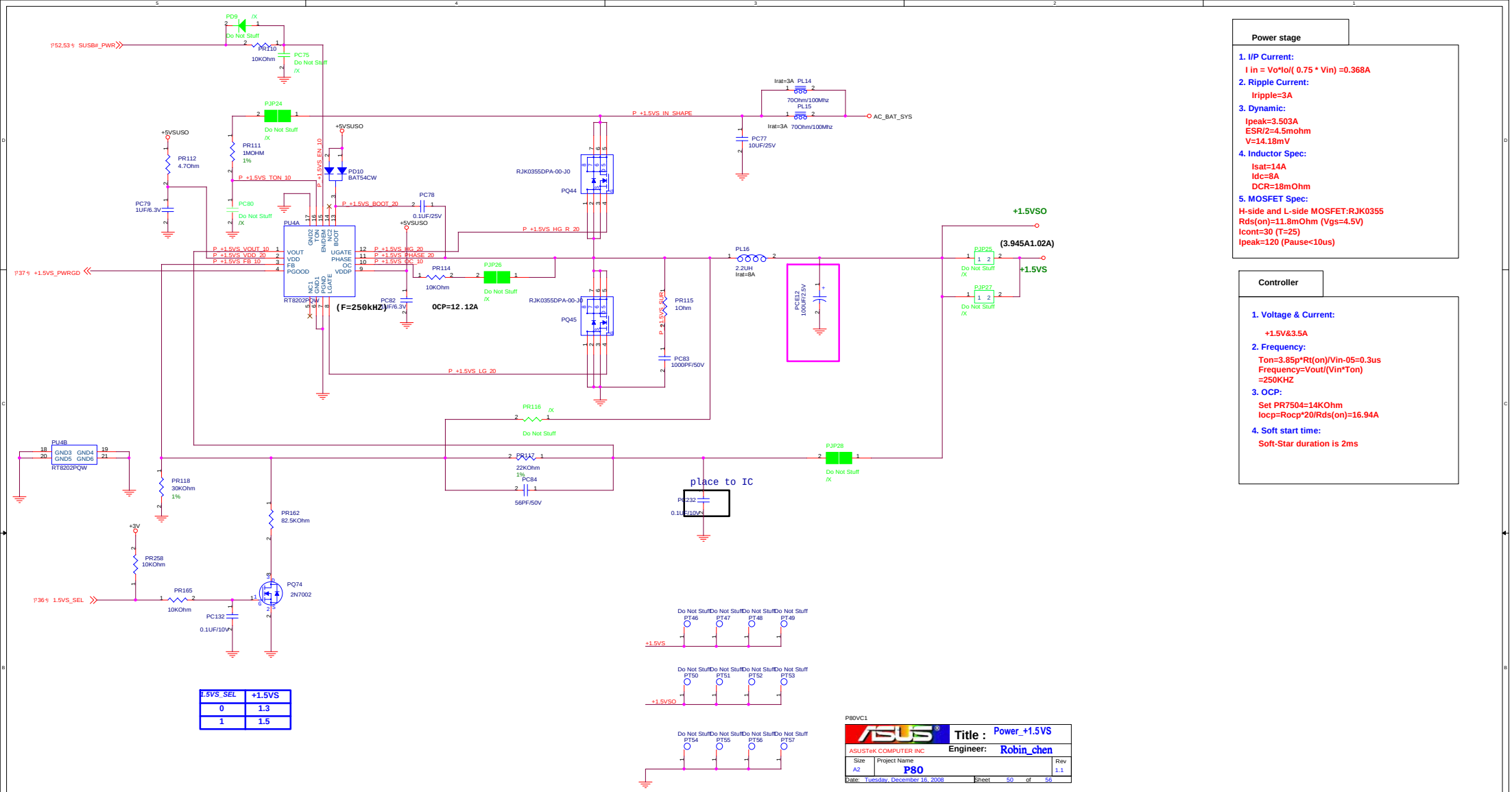
P80VC1

Title : POWER_CHARGER

ASUSTeK COMPUTER INC. NB3 Engineer:Robin_chen

Size	Project Name	Rev
A2	P80A	1.1

Date: Tuesday, December 16, 2008 Sheet 49 of 56



1.5VS_SEL	+1.5VS
0	1.3
1	1.5

Power stage

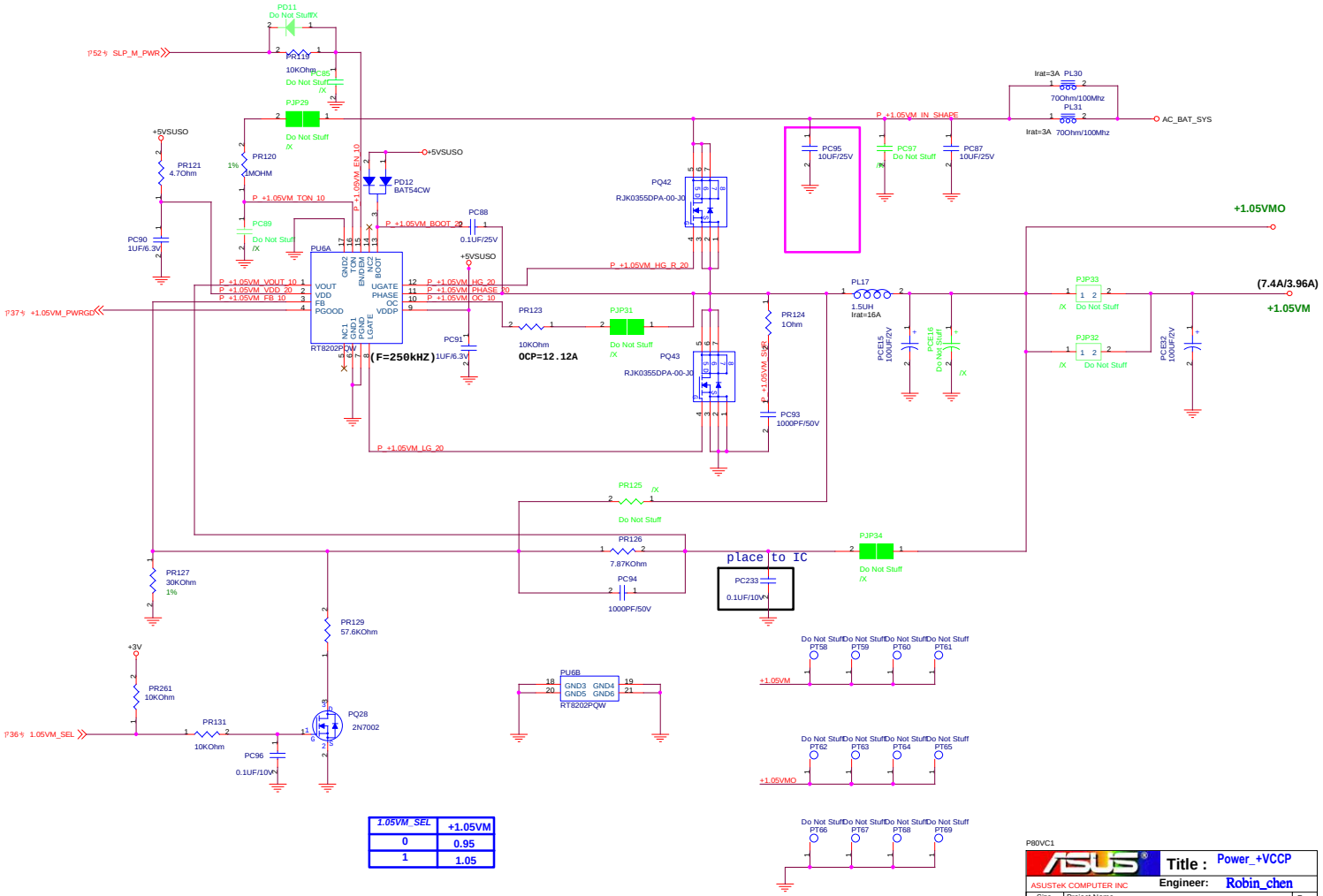
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.368A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=3.503A
   ESR/2=4.5mohm
   V=14.18mV
4. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355
   Rds(on)=11.8mOhm (Vgs=4.5V)
   Icont=30 (T=25)
   Ipeak=120 (Pause<10us)

Controller

1. Voltage & Current:
   +1.5V&3.5A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=16.94A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+1.5VS		
	Engineer: Robin_chen		
Size: A2	Project Name: P80		Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 50 of 56		



1.05VM_SEL	+1.05VM
0	0.95
1	1.05

Power stage

1. I/P Current:

I in = Vo*Io/(0.75 * Vin) =1.65A

2. Ripple Current:

Iripple=3A

3. Dynamic:

Ipeak=22.44A
ESR/2=9mohm
V=162mV

4. Inductor Spec:

Isat=33A
Idc=16A
DCR=3.8mOhm

5. MOSFET Spec:

H-side and L-side MOSFET:RJK0355
Rds(on)=11.8mOhm (Vgs=4.5V)
Icont=30 (T=25)
Ipeak=120 (Pause<10us)

Controller

1. Voltage & Current:

+1.05V&22.44A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=250KHZ

3. OCP:

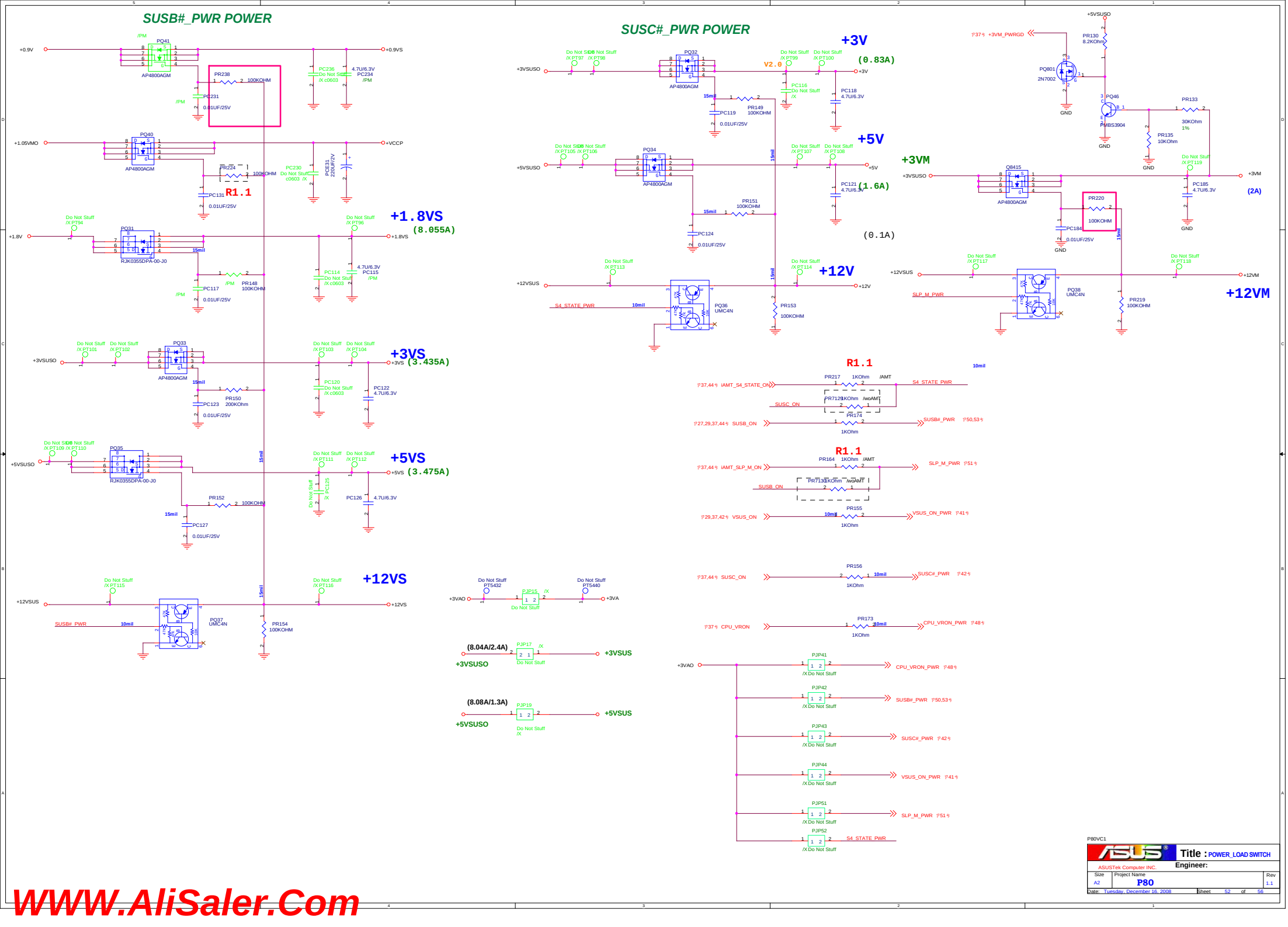
Set PR7504=14KOhm
Iocp=Rocp*20/Rds(on)=16.94A

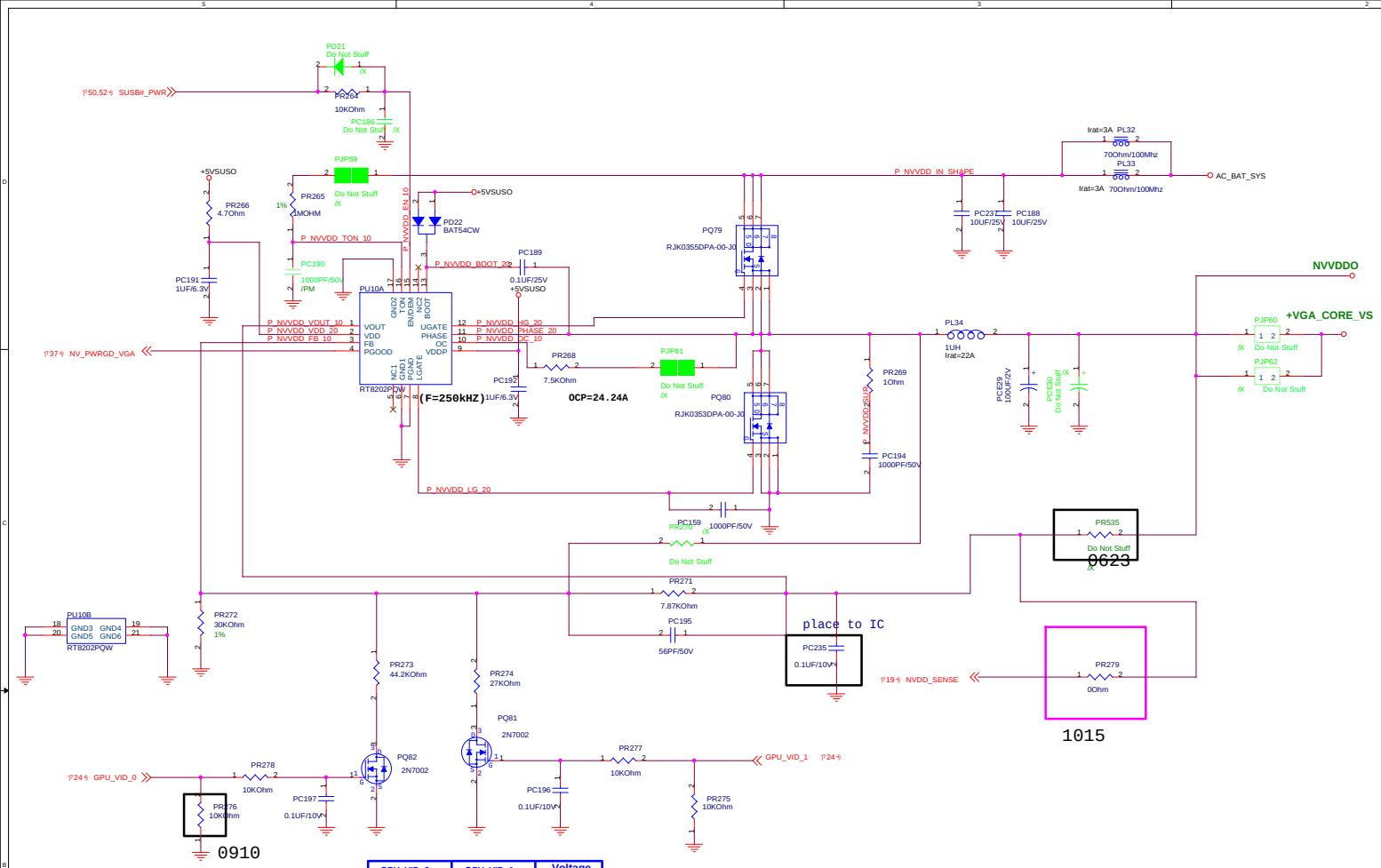
4. Soft start time:

Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+VCCP		
	Engineer: Robin_chen		
Size: A2	Project Name: P80		Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 51 of 56		





GPU_VID_0	GPU_VID_1	Voltage
L	L	0.946V
H	L	1.00V
L	H	1.17V
H	H	X

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.3 A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=10.87A
   ESR/2=4.5mohm
   V=44mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=9mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355/RJK0353
   Rds(on)=11.8/5.4mOhm (Vgs=10V)
   Icont=30/35A (T=25)
   Ipeak=120/140A (Pause<10us)

Controller

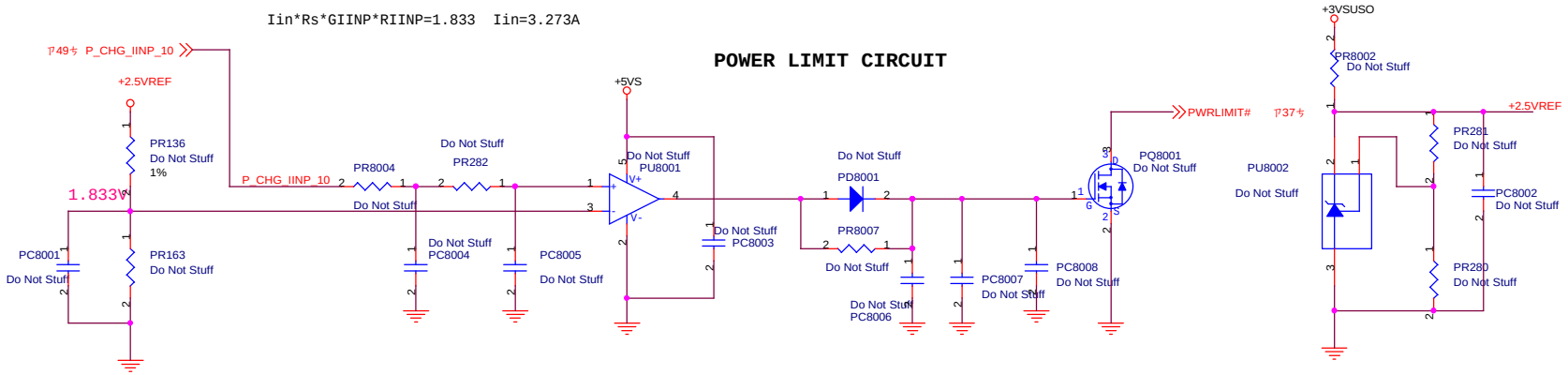
1. Voltage & Current:
   +VGA:0.94&10.08A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=24A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+VGA	
	Engineer: robin_chen	
Size: A2	Project Name: P80	Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 53 of 56	

Iin*Rs*GIINP*RIINP=1.833 Iin=3.273A

POWER LIMIT CIRCUIT



P80VC1

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Robin_chen	
Size: A3	Project Name: P80	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 54 of 80	