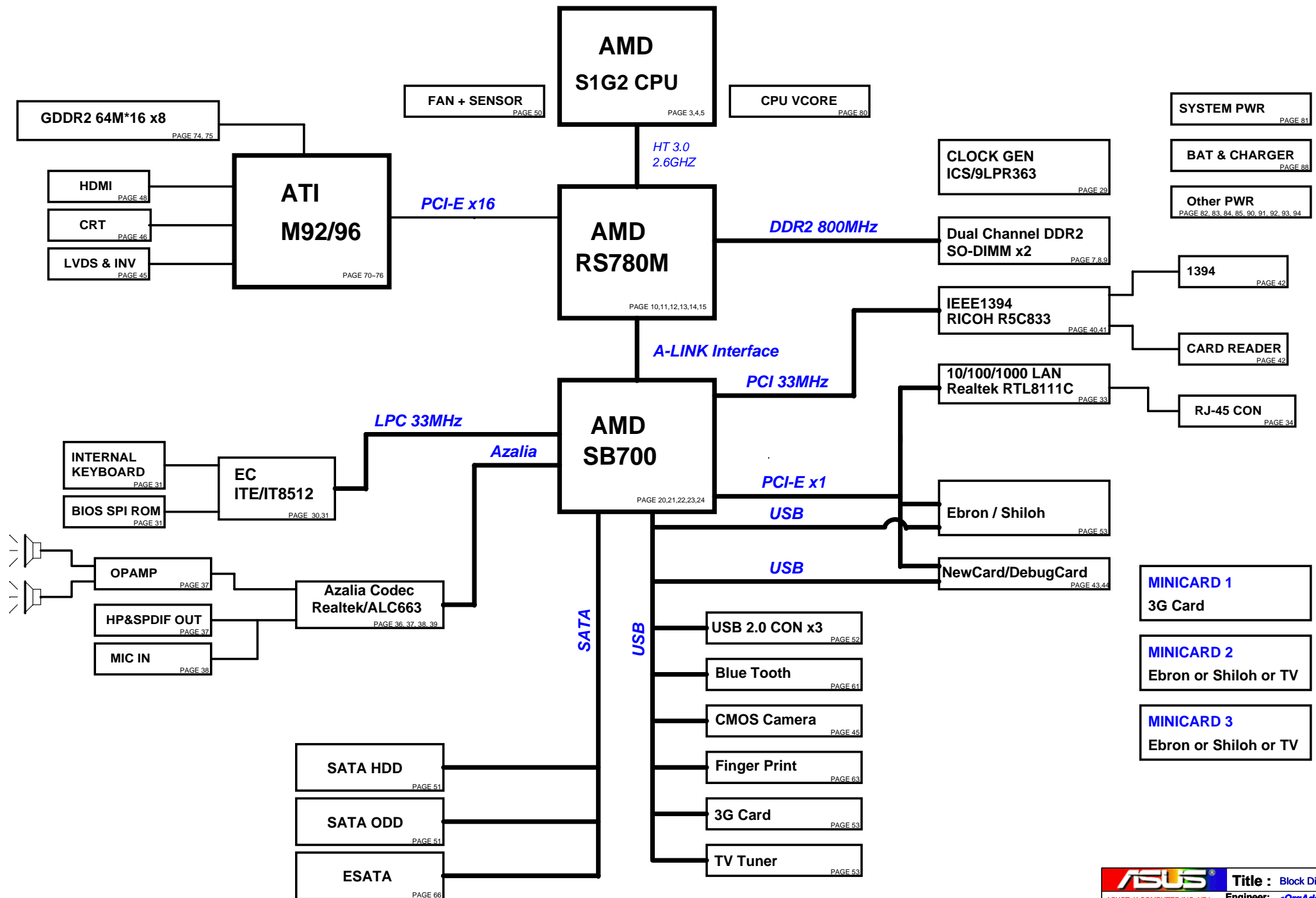
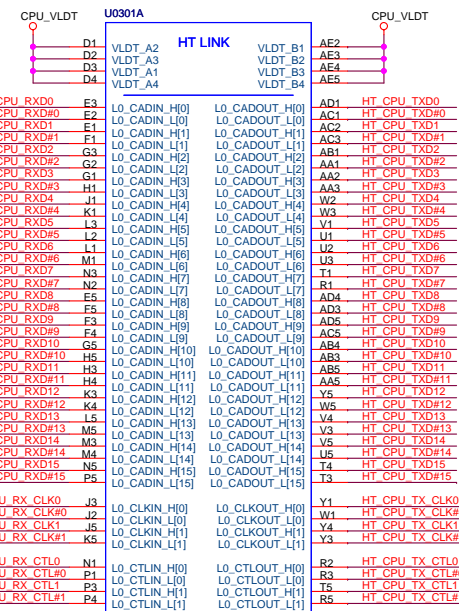


[illegible][illegible]

N50Tr Puma Block Diagram



1.5A

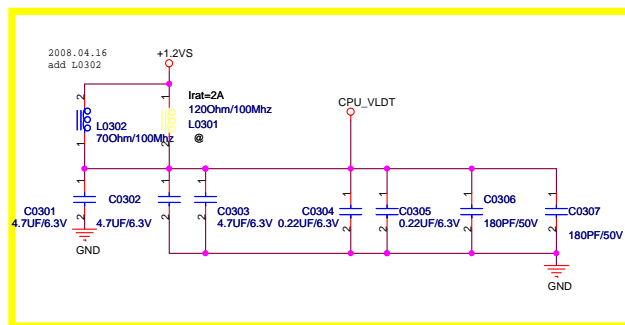


SOCKET638

Change P/N to 12G011306380

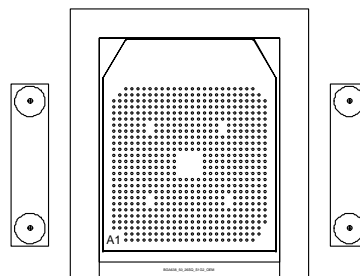
071113

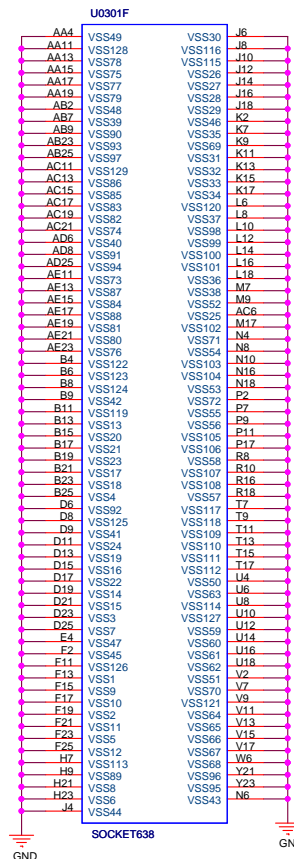
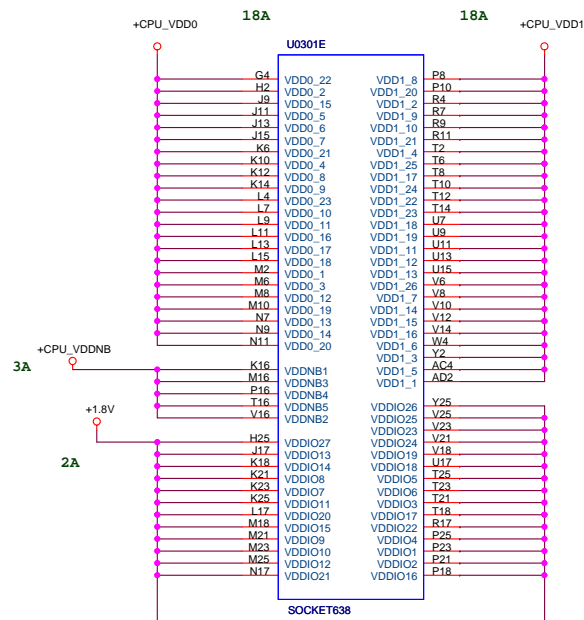
Do not cross plane.



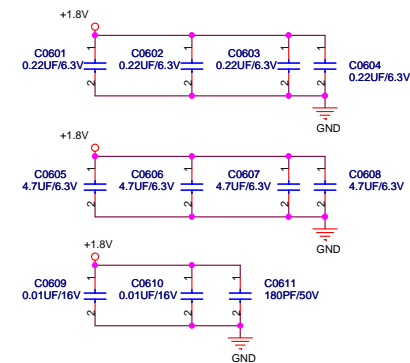
Place close to socket

* If VLDT is connected only on one side,
one 4.7uF cap should be added to
the island side

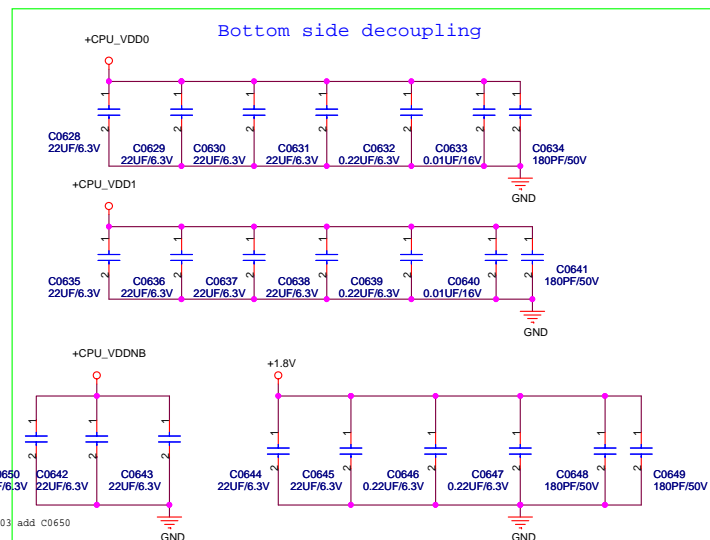
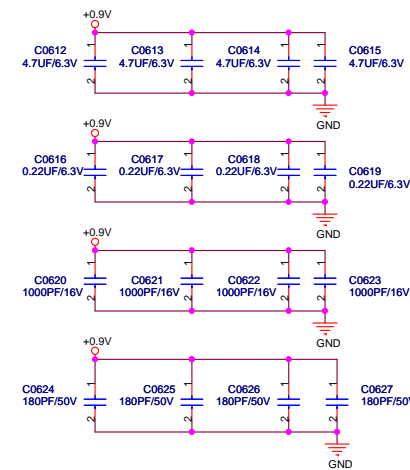




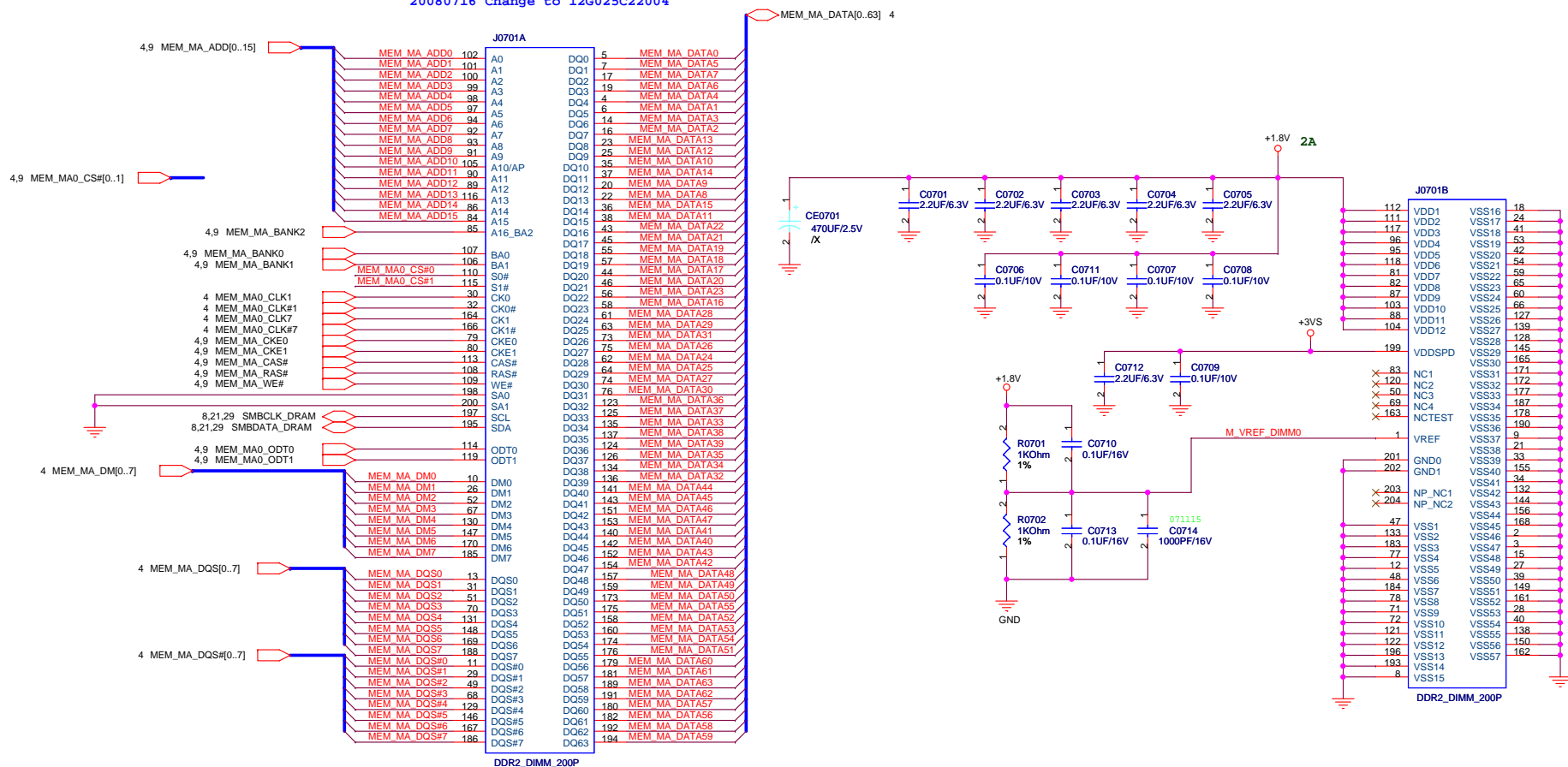
Decoupling between Processor and DIMMs, Place close to Porcessor as possible



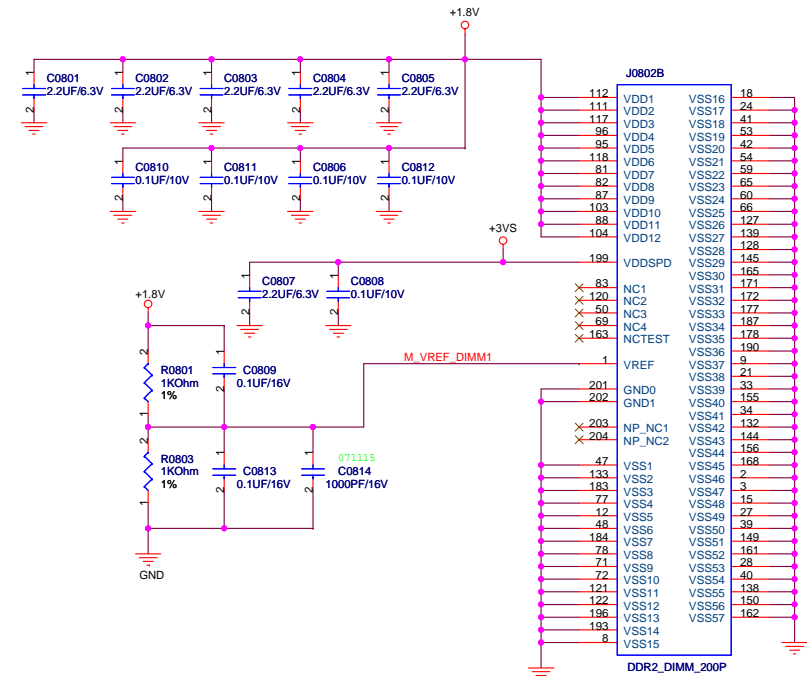
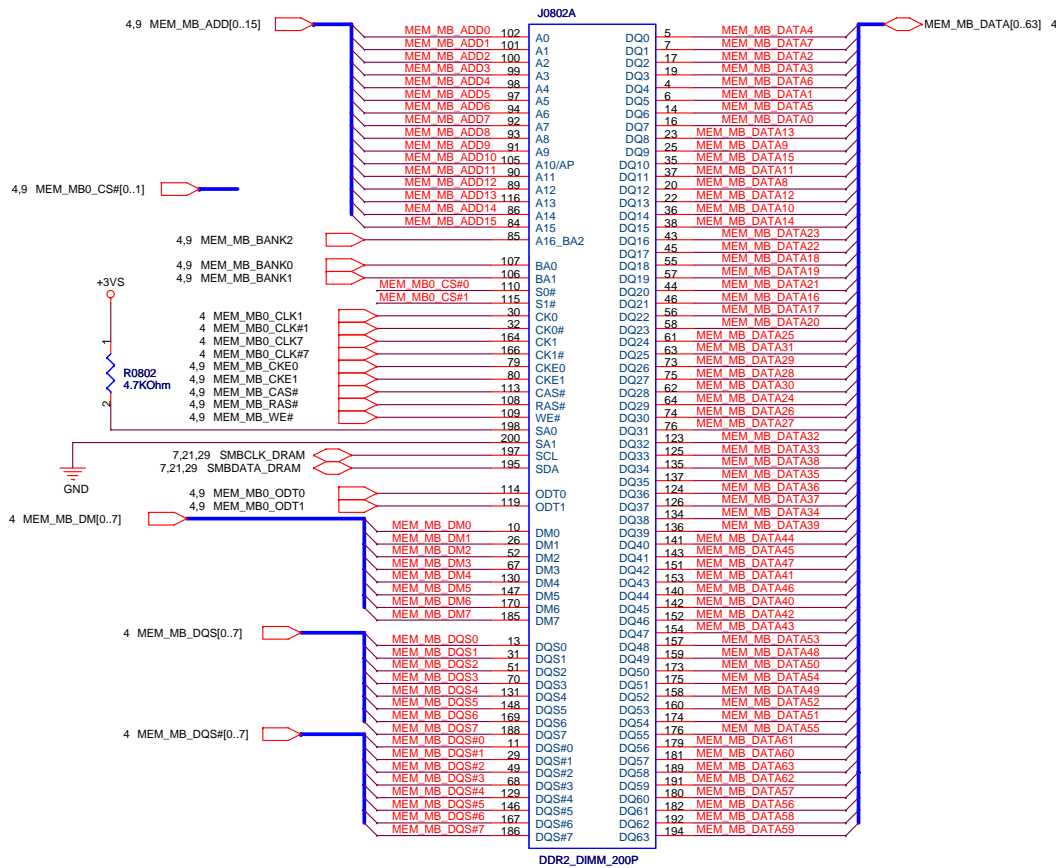
place close to socket



20080716 Change to 12G025C22004



High



DDR2_DIMM_200P

low

4.7 MEM_MA_CKE1 MEM_MA_CKE1 R903 470hm

4.7 MEM_MA_ADD11 MEM_MA_ADD11 R904 470hm

4.7 MEM_MA_ADD14 MEM_MA_ADD14 R905 470hm

4.7 MEM_MA_ADD15 MEM_MA_ADD15 R906 470hm

0.3A

4.7 MEM_MA_BANK0 MEM_MA_BANK0 RN0901A 470hm

4.7 MEM_MA_WEI MEM_MA_WEI RN0901B 470hm

1 2 3 4 5 6 7

C0901 1 2 0.1uF16V +0.8V

C0902 1 2 0.1uF16V +0.8V

4.7 MEM_MA_CS0 MEM_MA_CS0 RN0902A 470hm

4.7 MEM_MA_RAS0 MEM_MA_RAS0 RN0902B 470hm

4.7 MEM_MA_BANK1 MEM_MA_BANK1 RN0902C 470hm

4.7 MEM_MA_CAS0 MEM_MA_CAS0 RN0902D 470hm

4.7 MEM_MA_ADD13 MEM_MA_ADD13 RN0902E 470hm

4.7 MEM_MA_ODT0 MEM_MA_ODT0 RN0902G 470hm

4.7 MEM_MA_CS#1 MEM_MA_CS#1 RN0902G 470hm

4.7 MEM_MA_ODT1 MEM_MA_ODT1 RN0902H 470hm

1 2 3 4 5 6 7 8

C0903 1 2 0.1uF16V +0.8V

C0912 1 2 0.1uF16V +0.8V

4.7 MEM_MA_CKE0 MEM_MA_CKE0 RN0903A 470hm

4.7 MEM_MA_BANK2 MEM_MA_BANK2 RN0903B 470hm

4.7 MEM_MA_ADD12 MEM_MA_ADD12 RN0903C 470hm

4.7 MEM_MA_ADD9 MEM_MA_ADD9 RN0903D 470hm

4.7 MEM_MA_ADD6 MEM_MA_ADD6 RN0903E 470hm

4.7 MEM_MA_ADD5 MEM_MA_ADD5 RN0903F 470hm

4.7 MEM_MA_ADD3 MEM_MA_ADD3 RN0903G 470hm

4.7 MEM_MA_ADD1 MEM_MA_ADD1 RN0903H 470hm

1 2 3 4 5 6 7 8

C0913 1 2 0.1uF16V +0.8V

C0914 1 2 0.1uF16V +0.8V

4.7 MEM_MA_ADD4 MEM_MA_ADD4 RN0904A 470hm

4.7 MEM_MA_ADD6 MEM_MA_ADD6 RN0904B 470hm

4.7 MEM_MA_ADD7 MEM_MA_ADD7 RN0904C 470hm

MEM_MA_ADD2 MEM_MA_ADD2 RN0904D 470hm

MEM_MA_ADD2 MEM_MA_ADD2 RN0904E 470hm

4.7 MEM_MA_ADD2 MEM_MA_ADD2 RN0904F 470hm

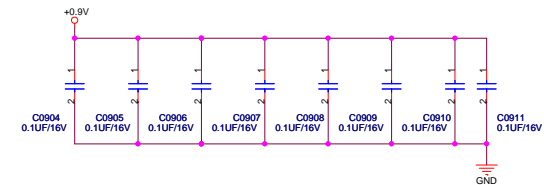
4.7 MEM_MA_ADD9 MEM_MA_ADD9 RN0904G 470hm

4.7 MEM_MA_ADD10 MEM_MA_ADD10 RN0904H 470hm

1 2 3 4 5 6 7 8

C0915 1 2 0.1uF16V +0.8V

C0916 1 2 0.1uF16V +0.8V



0.3A

+0.9V

4.8 MEM_MB_BANK2 MEM_MB_BANK2 R910 1 2 470Ohm

4.8 MEM_MB_OTD1 MEM_MB_OTD1 R909 1 2 470Ohm

4.8 MEM_MB_CKE0 MEM_MB_CKE0 R908 1 2 470Ohm

4.8 MEM_MB_ADD14 MEM_MB_ADD14 16 470Ohm 1 RN0905A

4.8 MEM_MB_ADD1 MEM_MB_ADD1 15 470Ohm 2 RN0905B

4.8 MEM_MB_ADD7 MEM_MB_ADD7 14 470Ohm 3 RN0905C

4.8 MEM_MB_ADD6 MEM_MB_ADD6 12 470Ohm 4 RN0905D

4.8 MEM_MB_ADD4 MEM_MB_ADD4 11 470Ohm 5 RN0905E

4.8 MEM_MB_ADD0 MEM_MB_ADD0 10 470Ohm 6 RN0905F

4.8 MEM_MB_ADD2 MEM_MB_ADD2 9 470Ohm 7 RN0905G

4.8 MEM_MB_ADD12 MEM_MB_ADD12 16 470Ohm 1 RN0906A

4.8 MEM_MB_ADD8 MEM_MB_ADD8 15 470Ohm 2 RN0906B

4.8 MEM_MB_CKE1 MEM_MB_CKE1 14 470Ohm 3 RN0906C

4.8 MEM_MB_ADD15 MEM_MB_ADD15 12 470Ohm 4 RN0906D

4.8 MEM_MB_ADD5 MEM_MB_ADD5 11 470Ohm 5 RN0906E

4.8 MEM_MB_ADD3 MEM_MB_ADD3 10 470Ohm 6 RN0906F

4.8 MEM_MB_ADD3 MEM_MB_ADD3 9 470Ohm 7 RN0906G

4.8 MEM_MB_ADD3 MEM_MB_ADD3 8 RN0906H

4.8 MEM_MB_RAS# MEM_MB_RAS# 16 470Ohm 1 RN0907A

4.8 MEM_MB_BANK1 MEM_MB_BANK1 15 470Ohm 2 RN0907B

4.8 MEM_MB_CAS# MEM_MB_CAS# 14 470Ohm 3 RN0907C

4.8 MEM_MB_VEF# MEM_MB_VEF# 12 470Ohm 4 RN0907D

4.8 MEM_MB_BANK0 MEM_MB_BANK0 11 470Ohm 5 RN0907E

4.8 MEM_MB_CS#1 MEM_MB_CS#1 10 470Ohm 6 RN0907F

4.8 MEM_MB_CS#1 MEM_MB_CS#1 9 470Ohm 7 RN0907G

4.8 MEM_MB_CS#1 MEM_MB_CS#1 8 RN0907H

4.8 MEM_MB_CS#0 MEM_MB_CS#0 2 470Ohm 1 RN0908A

4.8 MEM_MB_OTD0 MEM_MB_OTD0 4 470Ohm 3 RN0908B

4.8 MEM_MB_ADD13 MEM_MB_ADD13 3 470Ohm 5 RN0908C

4.8 MEM_MB_ADD13 MEM_MB_ADD13 2 470Ohm 7 RN0908D

C0917 1 2 0.1Uf16V

C0918 1 2 0.1Uf16V

C0919 1 2 0.1Uf16V

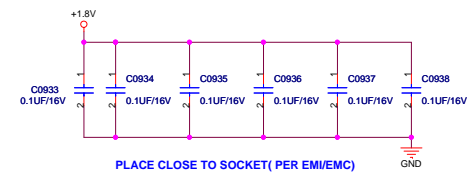
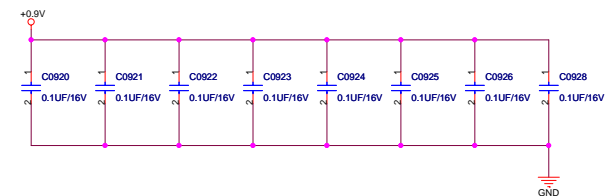
C0927 1 2 0.1Uf16V

C0929 1 2 0.1Uf16V

C0930 1 2 0.1Uf16V

C0931 1 2 0.1Uf16V

C0932 1 2 0.1Uf16V



		Title : DDR2_TERMINATIONS	
ASUSTeK COMPUTER INC. NBI		Engineer: <OrigAddr1>	
Size Custom	Project Name N50Tr/Ta	Rev 1.00	
Date: Thursday, September 25, 2008		Sheet 9	of 93

PART 1 OF 6

HYPER TRANSPORT CPU I/F

U1001A

HT_CPU_TXD0 Y25
HT_CPU_TXD0#0 V24
HT_CPU_TXD1 V23
HT_CPU_TXD#1 V23
HT_CPU_TXD2 V25
HT_CPU_TXD#2 V24
HT_CPU_TXD3 U24
HT_CPU_TXD#3 U25
HT_CPU_TXD4 T25
HT_CPU_TXD#4 T24
HT_CPU_TXD5 P22
HT_CPU_TXD#5 P23
HT_CPU_TXD6 P25
HT_CPU_TXD#6 P24
HT_CPU_TXD7 N24
HT_CPU_TXD#7 N25

HT_CPU_TXD8 AC24
HT_CPU_TXD#8 AC25
HT_CPU_TXD9 AB25
HT_CPU_TXD#9 AB24
HT_CPU_TXD10 AA24
HT_CPU_TXD#10 AA25
HT_CPU_TXD11 Y22
HT_CPU_TXD#11 Y23
HT_CPU_TXD12 W21
HT_CPU_TXD#12 W20
HT_CPU_TXD13 V21
HT_CPU_TXD#13 V20
HT_CPU_TXD14 U20
HT_CPU_TXD#14 U21
HT_CPU_TXD15 U19
HT_CPU_TXD#15 U18

HT_CPU_TX_CLK0 T22
HT_CPU_TX_CLK#0 T23
HT_CPU_TX_CLK1 AB23
HT_CPU_TX_CLK#1 AA22

HT_CPU_TX_CTL0 M22
HT_CPU_TX_CTL#0 M23
HT_CPU_TX_CTL1 R21
HT_CPU_TX_CTL#1 R20

HT_RXCALP C23
HT_RXCALN A24

RS780MN

02G050001122

HT_TXCAD0P
HT_TXCAD0N
HT_TXCAD1P
HT_TXCAD1N
HT_TXCAD2P
HT_TXCAD2N
HT_TXCAD3P
HT_TXCAD3N
HT_TXCAD4P
HT_TXCAD4N
HT_TXCAD5P
HT_TXCAD5N
HT_TXCAD6P
HT_TXCAD6N
HT_TXCAD7P
HT_TXCAD7N

HT_TXCAD8P
HT_TXCAD8N
HT_TXCAD9P
HT_TXCAD9N
HT_TXCAD10P
HT_TXCAD10N
HT_TXCAD11P
HT_TXCAD11N
HT_TXCAD12P
HT_TXCAD12N
HT_TXCAD13P
HT_TXCAD13N
HT_TXCAD14P
HT_TXCAD14N
HT_TXCAD15P
HT_TXCAD15N

HT_TXCLK0P
HT_TXCLK0N
HT_TXCLK1P
HT_TXCLK1N

HT_TXCTL0P
HT_TXCTL0N
HT_TXCTL1P
HT_TXCTL1N

HT_TXCALP
HT_TXCALN

D24 HT_CPU_RXD0
D25 HT_CPU_RXD#0
E24 HT_CPU_RXD1
E25 HT_CPU_RXD#1
F24 HT_CPU_RXD2
F25 HT_CPU_RXD#2
G23 HT_CPU_RXD3
G22 HT_CPU_RXD#3
H23 HT_CPU_RXD4
H22 HT_CPU_RXD#4
J25 HT_CPU_RXD5
J24 HT_CPU_RXD#5
K24 HT_CPU_RXD6
K25 HT_CPU_RXD#6
K23 HT_CPU_RXD7
K22 HT_CPU_RXD#7

F21 HT_CPU_RXD8
G21 HT_CPU_RXD#8
G20 HT_CPU_RXD9
H21 HT_CPU_RXD#9
J20 HT_CPU_RXD10
J21 HT_CPU_RXD#10
J18 HT_CPU_RXD11
K17 HT_CPU_RXD#11
L19 HT_CPU_RXD12
J19 HT_CPU_RXD#12
M19 HT_CPU_RXD13
L18 HT_CPU_RXD#13
M21 HT_CPU_RXD14
P21 HT_CPU_RXD#14
P18 HT_CPU_RXD15
M18 HT_CPU_RXD#15

H24 HT_CPU_RX_CLK0
H25 HT_CPU_RX_CLK#0
L21 HT_CPU_RX_CLK1
L20 HT_CPU_RX_CLK#1

M24 HT_CPU_RX_CTL0
M25 HT_CPU_RX_CTL#0
P19 HT_CPU_RX_CTL1
R18 HT_CPU_RX_CTL#1

B24 HT_TXCALP
B25 HT_TXCALN

HT_CPU_RXD[0..15] 3

HT_CPU_RXD#[0..15] 3

HT_CPU_RX_CLK0 3
HT_CPU_RX_CLK#0 3
HT_CPU_RX_CLK1 3
HT_CPU_RX_CLK#1 3

HT_CPU_RX_CTL0 3
HT_CPU_RX_CTL#0 3
HT_CPU_RX_CTL1 3
HT_CPU_RX_CTL#1 3

PCI-E:
0-3 HDMI@ RS780M
4-7 NC
8-15 VGA8x

Refer to RS780M datasheet Table 3-10

U1001B

PART 2 OF 6

PCI-E I/F GFX

PCI-E I/F GPP

PCI-E I/F SB

RS780MN

Caps on VGA card

PCIENB_RXN[0..15] 71
PCIENB_RXP[0..15] 71

53 PCIE_RXP0_TV
53 PCIE_RXN0_TV
33 PCIE_RXP1_LAN
33 PCIE_RXN1_LAN
53 PCIE_RXP3_WLAN
53 PCIE_RXN3_WLAN
43 PCIE_RXP2_NEWCARD
43 PCIE_RXN2_NEWCARD

080712 ADD 3G

0427:change wlan and newcard lane

20 PCIE_SB_NB_RX0P
20 PCIE_SB_NB_RX0N
20 PCIE_SB_NB_RX1P
20 PCIE_SB_NB_RX1N
20 PCIE_SB_NB_RX2P
20 PCIE_SB_NB_RX2N
20 PCIE_SB_NB_RX3P
20 PCIE_SB_NB_RX3N

AA8 SB_RX0P
Y8 SB_RX0N
AA7 SB_RX1P
Y7 SB_RX1N
AA6 SB_RX2P
Y6 SB_RX2N
W5 SB_RX3P
Y5 SB_RX3N

GFX_TX0P
GFX_TX0N
GFX_TX1P
GFX_TX1N
GFX_TX2P
GFX_TX2N
GFX_TX3P
GFX_TX3N
GFX_TX4P
GFX_TX4N
GFX_TX5P
GFX_TX5N
GFX_TX6P
GFX_TX6N
GFX_TX7P
GFX_TX7N
GFX_TX8P
GFX_TX8N
GFX_TX9P
GFX_TX9N
GFX_TX10P
GFX_TX10N
GFX_TX11P
GFX_TX11N
GFX_TX12P
GFX_TX12N
GFX_TX13P
GFX_TX13N
GFX_TX14P
GFX_TX14N
GFX_TX15P
GFX_TX15N

GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_TX4P
GPP_TX4N
GPP_TX5P
GPP_TX5N

SB_TX0P
SB_TX0N
SB_TX1P
SB_TX1N
SB_TX2P
SB_TX2N
SB_TX3P
SB_TX3N

AC8 1.27KOHM
AB8 2KOHM

R1101
R1102 +1.1V_NB

PCIENB_TXN0 C1142 2 1 0.1UF/10V PCIEG_RXN0
PCIENB_TXN1 C1144 2 1 0.1UF/10V PCIEG_RXN1
PCIENB_TXN2 C1141 2 1 0.1UF/10V PCIEG_RXN2
PCIENB_TXN3 C1148 2 1 0.1UF/10V PCIEG_RXN3
PCIENB_TXN4 C1145 2 1 0.1UF/10V PCIEG_RXN4
PCIENB_TXN5 C1147 2 1 0.1UF/10V PCIEG_RXN5
PCIENB_TXN6 C1143 2 1 0.1UF/10V PCIEG_RXN6
PCIENB_TXN7 C1146 2 1 0.1UF/10V PCIEG_RXN7
PCIENB_TXN8 C1119 2 1 0.1UF/10V PCIEG_RXN8
PCIENB_TXN9 C1120 2 1 0.1UF/10V PCIEG_RXN9
PCIENB_TXN10 C1121 2 1 0.1UF/10V PCIEG_RXN10
PCIENB_TXN11 C1122 2 1 0.1UF/10V PCIEG_RXN11
PCIENB_TXN12 C1123 2 1 0.1UF/10V PCIEG_RXN12
PCIENB_TXN13 C1124 2 1 0.1UF/10V PCIEG_RXN13
PCIENB_TXN14 C1125 2 1 0.1UF/10V PCIEG_RXN14
PCIENB_TXN15 C1126 2 1 0.1UF/10V PCIEG_RXN15

71 PCIEG_RXN[0..15]

AC1 GPP_TX0P C C1101 2 1 0.1UF/10V
AC2 GPP_TX0N C C1103 2 1 0.1UF/10V
AB4 GPP_TX1P C C1102 2 1 0.1UF/10V
AB3 GPP_TX1N C C1105 2 1 0.1UF/10V
AA2 GPP_TX2P C C1128 2 1 0.1UF/10V
AA1 GPP_TX2N C C1129 2 1 0.1UF/10V
Y1 GPP_TX3P C C1104 2 1 0.1UF/10V
Y2 GPP_TX3N C C1106 2 1 0.1UF/10V
Y4
Y3
Y1
Y2

AD7 A_TX0P C C1107 2 1 0.1UF/10V
AE7 A_TX0N C C1109 2 1 0.1UF/10V
AE6 A_TX1P C C1108 2 1 0.1UF/10V
AD6 A_TX1N C C1112 2 1 0.1UF/10V
AB6 A_TX2P C C1110 2 1 0.1UF/10V
AC6 A_TX2N C C1114 2 1 0.1UF/10V
AD5 A_TX3P C C1111 2 1 0.1UF/10V
AE5 A_TX3N C C1116 2 1 0.1UF/10V

PCIE_NB_SB_TX0P 20
PCIE_NB_SB_TX0N 20
PCIE_NB_SB_TX1P 20
PCIE_NB_SB_TX1N 20
PCIE_NB_SB_TX2P 20
PCIE_NB_SB_TX2N 20
PCIE_NB_SB_TX3P 20
PCIE_NB_SB_TX3N 20

PCIENB_TXP0 C1149 2 1 0.1UF/10V PCIEG_RXP0
PCIENB_TXP1 C1150 2 1 0.1UF/10V PCIEG_RXP1
PCIENB_TXP2 C1151 2 1 0.1UF/10V PCIEG_RXP2
PCIENB_TXP3 C1156 2 1 0.1UF/10V PCIEG_RXP3
PCIENB_TXP4 C1152 2 1 0.1UF/10V PCIEG_RXP4
PCIENB_TXP5 C1155 2 1 0.1UF/10V PCIEG_RXP5
PCIENB_TXP6 C1153 2 1 0.1UF/10V PCIEG_RXP6
PCIENB_TXP7 C1154 2 1 0.1UF/10V PCIEG_RXP7
PCIENB_TXP8 C1133 2 1 0.1UF/10V PCIEG_RXP8
PCIENB_TXP9 C1134 2 1 0.1UF/10V PCIEG_RXP9
PCIENB_TXP10 C1135 2 1 0.1UF/10V PCIEG_RXP10
PCIENB_TXP11 C1136 2 1 0.1UF/10V PCIEG_RXP11
PCIENB_TXP12 C1137 2 1 0.1UF/10V PCIEG_RXP12
PCIENB_TXP13 C1138 2 1 0.1UF/10V PCIEG_RXP13
PCIENB_TXP14 C1139 2 1 0.1UF/10V PCIEG_RXP14
PCIENB_TXP15 C1140 2 1 0.1UF/10V PCIEG_RXP15

71 PCIEG_RXP[0..15]

PCIE_TXP0_TV 53
PCIE_TXN0_TV 53
PCIE_TXP1_LAN 33
PCIE_TXN1_LAN 33
PCIE_TXP3_WLAN 53
PCIE_TXN3_WLAN 53
PCIE_TXP2_NEWCARD 43
PCIE_TXN2_NEWCARD 43

NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

2008.03.03 add R1203 R1204 R1205 R1203 14009 for RS780 A13
70 CRT_RED_GM
70 CRT_GREEN_GM
70 CRT_BLUE_GM

RS780 POWERGOOD
is 1.8VS rail

OSC_14M_NB 1.1V 158R/90.9R

70 EDID_DAT_GM
70 EDID_CLK_GM

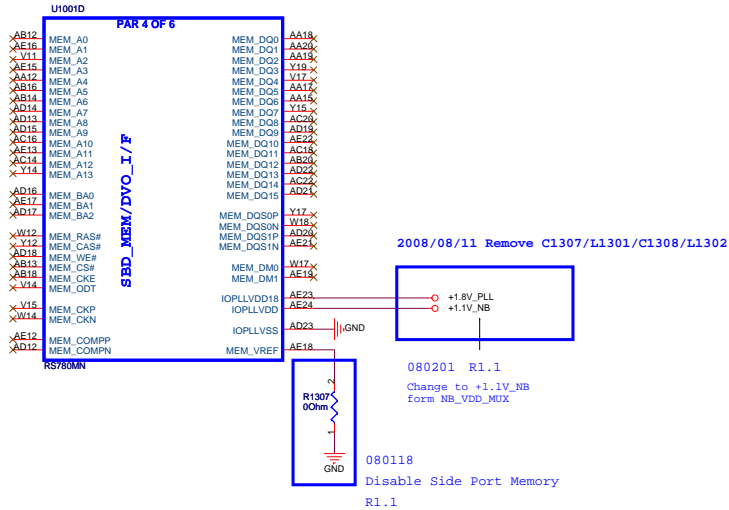
20080716 HDMI Power DDC???
PU@ conn side.
2008/0805 Remove HDMI DDC
STRP_DATA
VCC_NB

0104 ADD

5.20 CPU_LDT_STOP#
5.20 NB_ALLOW_LDTSTOP

?? for external graphic

R1.11 080319
Change the NB Part number to RS780 (A13)



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

Enables the Test Debug Bus using PCIE bus:

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

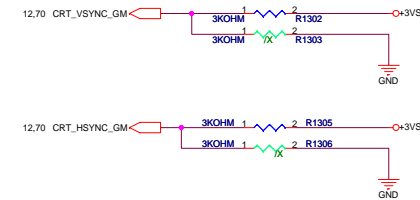
RS780: configurable thru register setting only

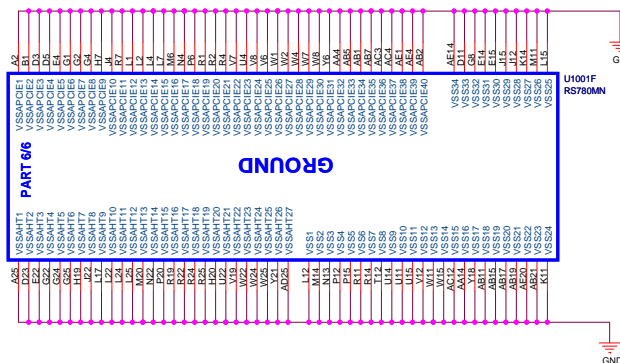
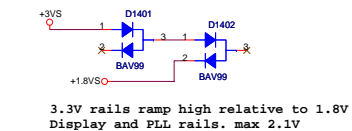
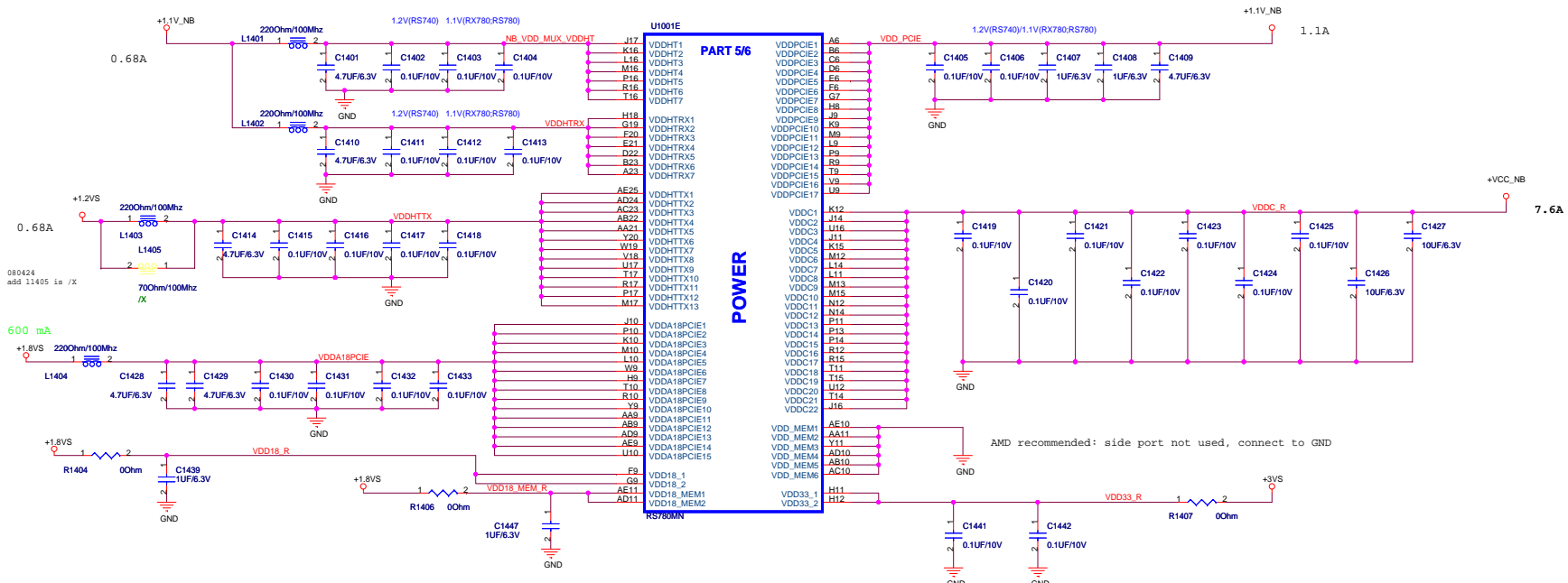
RS740/RS780: Enables Side port memory

RS780:HSYNCH

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]







	5	4	3	2	1
D					D
C					C
B					B
A					A
<div>ASUS®</div> <div>Title :</div>					
ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr1>					
Size	Project Name			Rev	
A	N50Tr/TA			1.00	
Date: Thursday, September 25, 2008			Sheet 15 of 93		


WWW.AliSaler.Com


5	4	3	2	1
D				D
C				C
B				B
A				A

			Title : BLANK		
ASUSTeK COMPUTER INC			Engineer:		
Size	Project Name				Rev
A	N50Tr/TA				1.00
Date: Thursday, September 25, 2008		Sheet 16 of 93			

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	N50Tr/TA		1.00
Date: Thursday, September 25, 2008		Sheet 17 of 93	

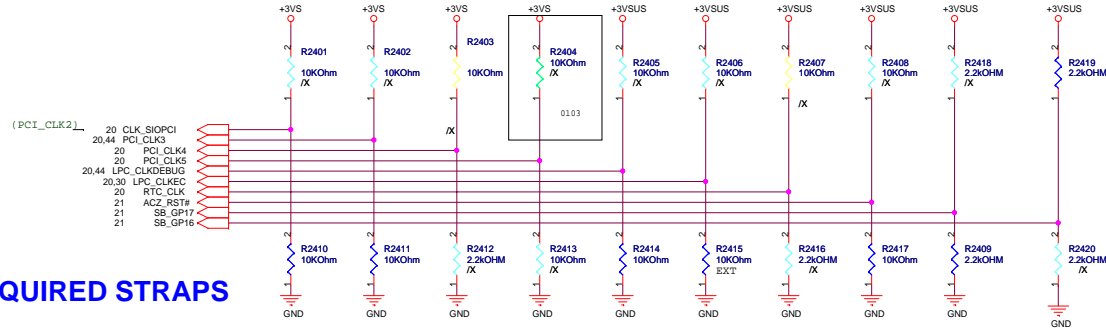
5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name N50Tr/TA		Rev 1.00
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name N50Tr/TA		Rev 1.00
Date: Thursday, September 25, 2008		Sheet 19 of 93	




NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEBUG	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.


5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	N50Tr/TA		1.00
Date: Thursday, September 25, 2008		Sheet 25 of 93	

5	4	3	2	1
D				D
C				C
B				B
A				A

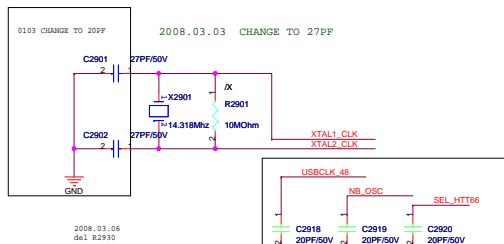
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name N50Tr/TA		Rev 1.00
Date: Thursday, September 25, 2008		Sheet 26 of 93	

5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	N50Tr/TA		1.00
Date: Thursday, September 25, 2008		Sheet 27 of 93	

5	4	3	2	1
D				D
C				C
B				B
A				A

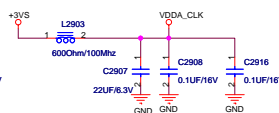
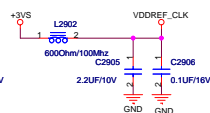
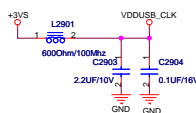
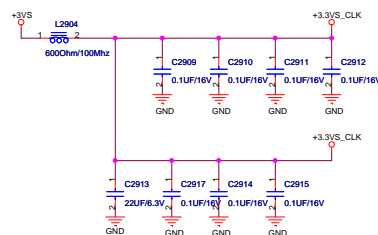
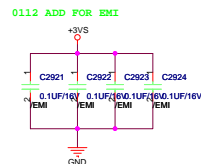
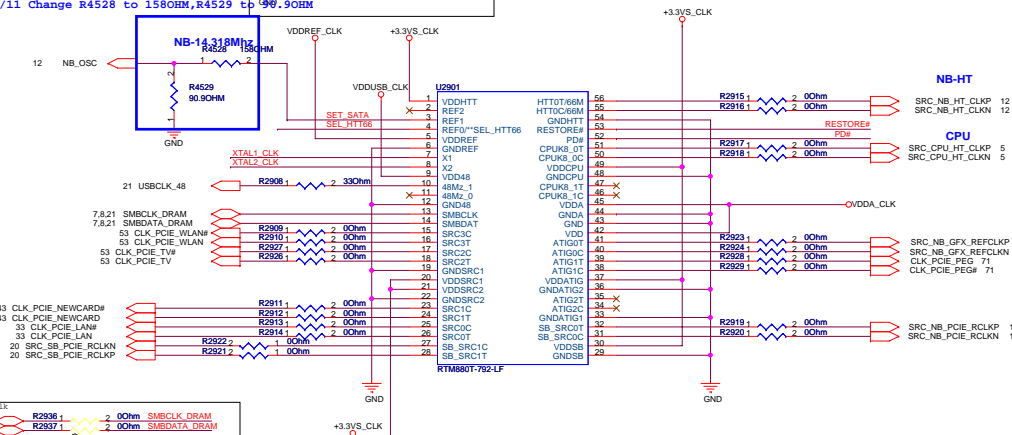
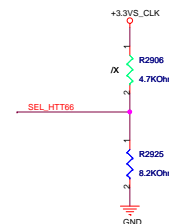
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	N50Tr/TA		1.00
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2008/08/11 Change R4528 to 1580HM,R4529 to 90.90HM

SEL_27	0	100 MHz differential Spread SRC clock
	1	27MHz 3.3V 27MHz spread clock

SEL_HIT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock



<Variant Name>

ASUS		Title : IC95LPRS489AGLFT	
ASUSTek COMPUTER INC		Engineer:	
Size A2	Project Name N507/TA	Rev 1.00	
Date: Thursday, September 26, 2008		Sheet 29 of 93	

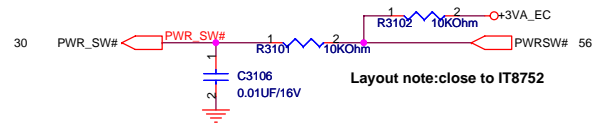
For Battery

Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

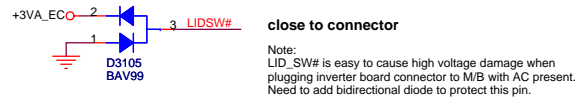
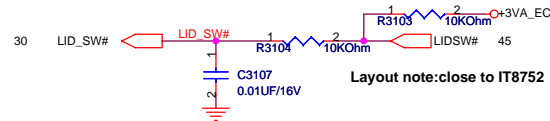
In Page 60

For Switch

PWR SWITCH



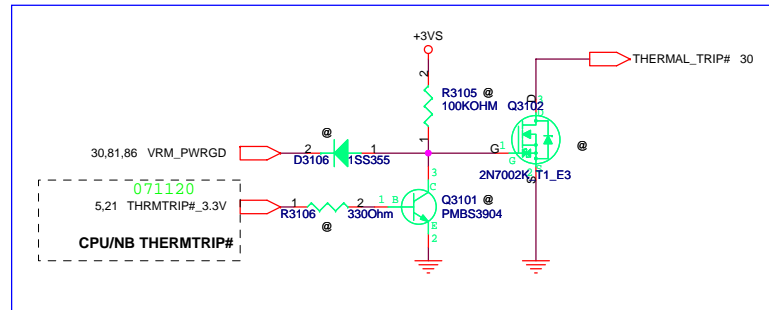
LID SWITCH



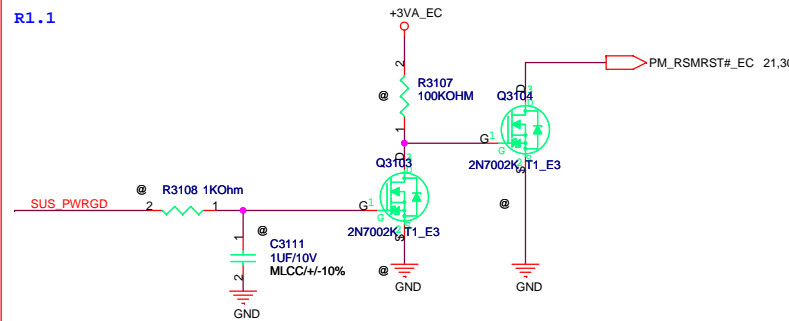
For Thermal Control Method

R2.0 080325

Unmount Thermal_trip component
D3106, R3105, R3106, Q3101, and Q3102, for cost down



R1.1

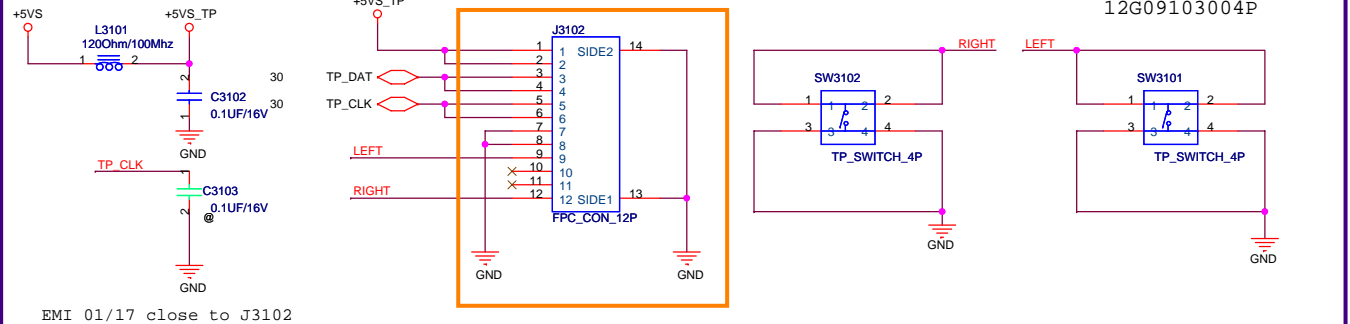


080121 Q3103 & Q3104 pin2 and pin3 Reverse

080123 Reserve for SB700 interface



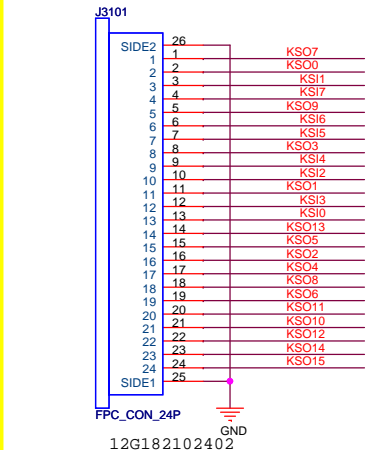
Touchpad Connector



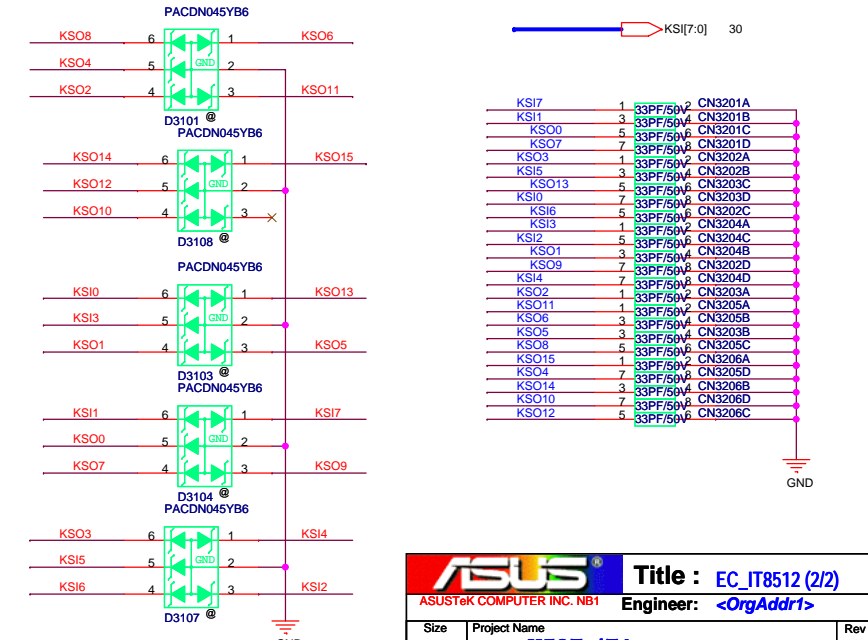
EMI 01/17 close to J3102

Keyboard Connector

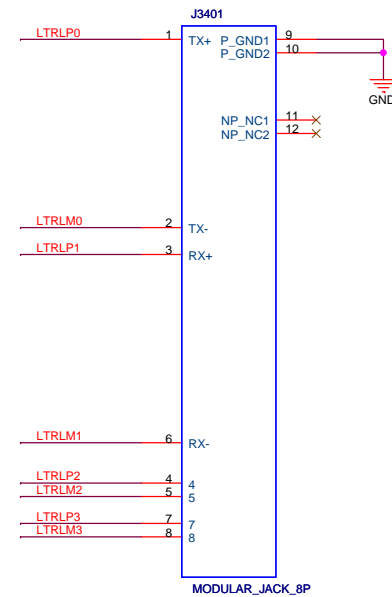
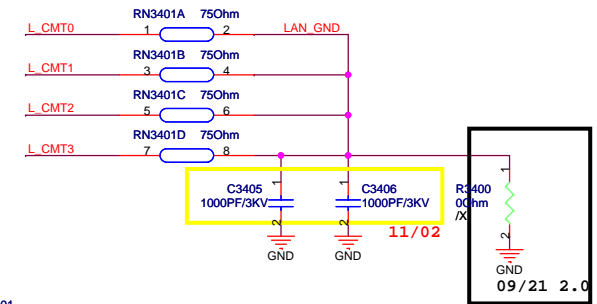
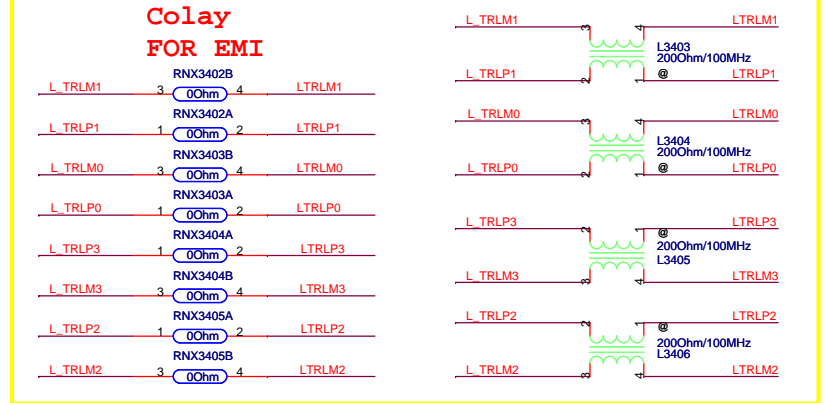
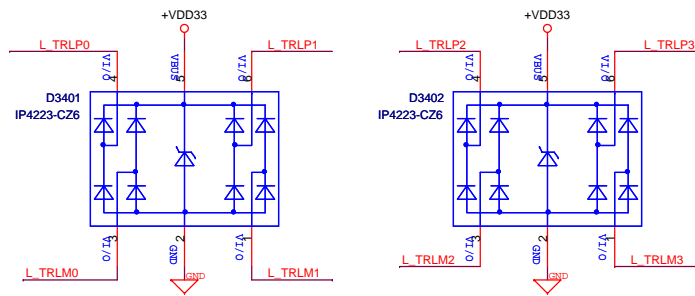
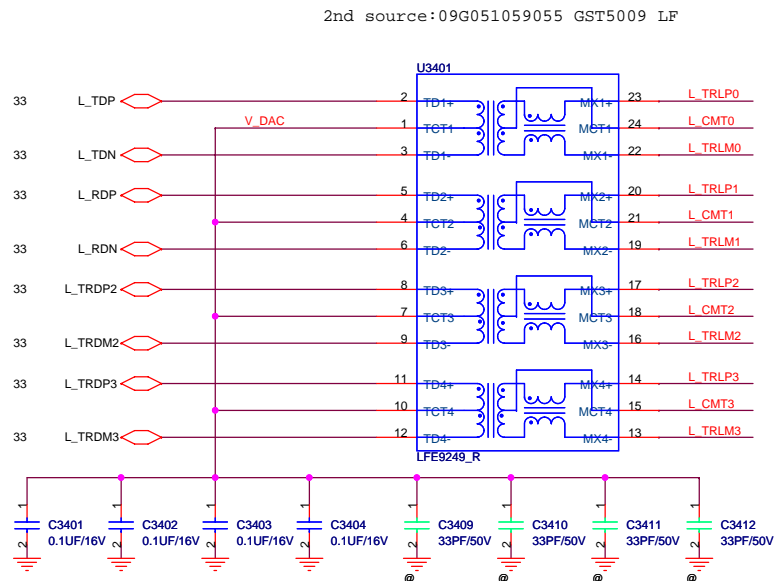
F7/N1 Keyboard



11/02








12G142111083

R2.0 06/11 remove MDC

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ASUSTeK COMPUTER INC		Engineer:	
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PC BEEP

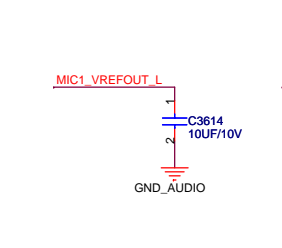
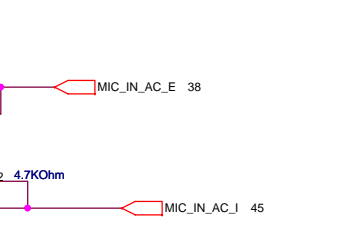
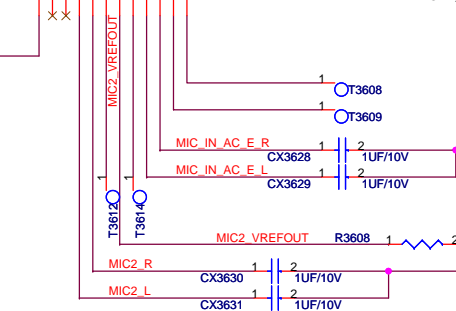
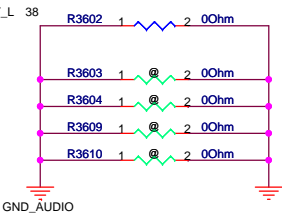
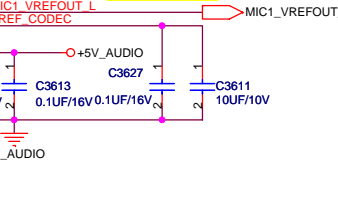
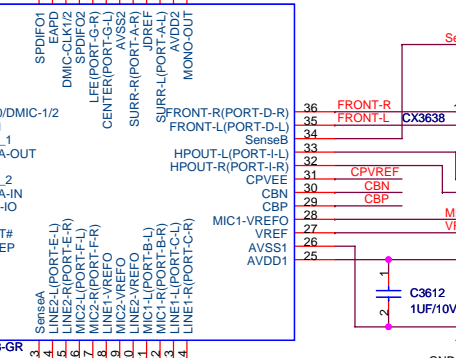
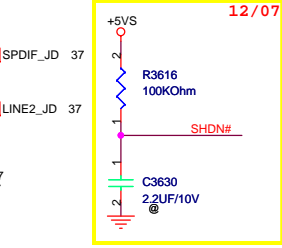
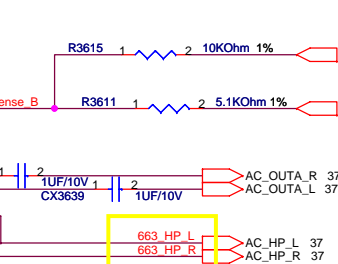
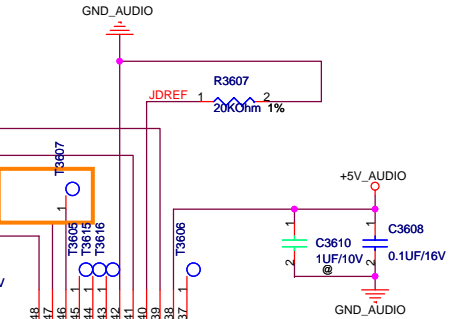
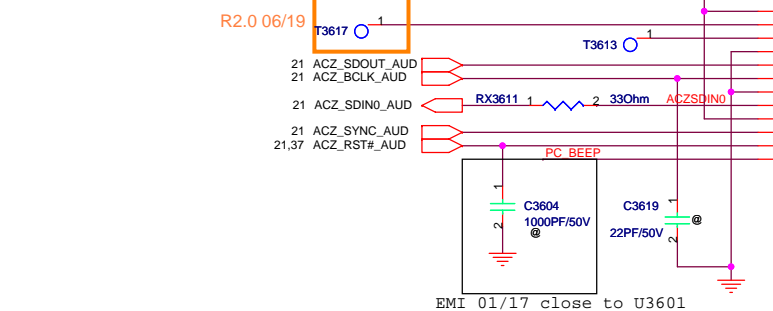
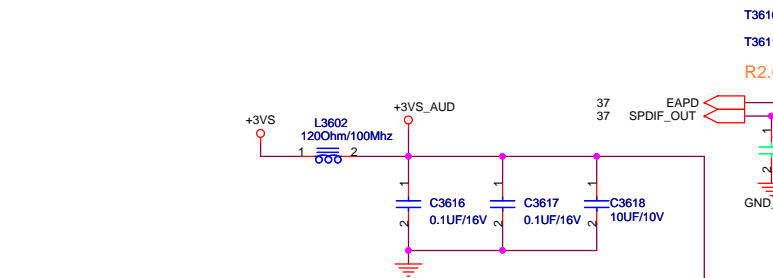
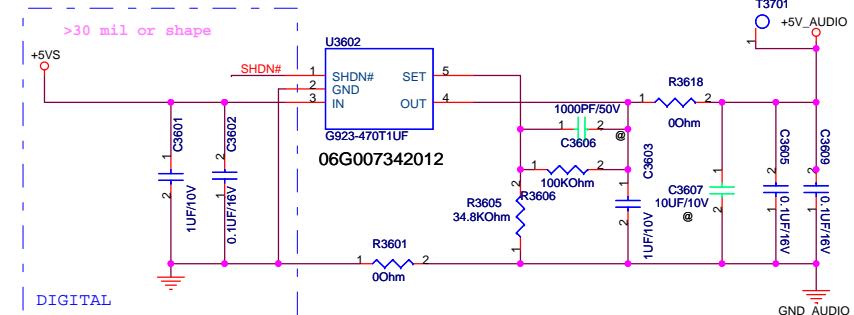
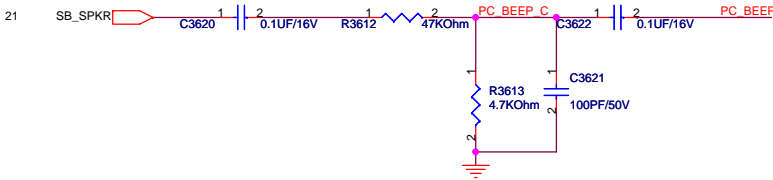
update 08/0714

Audio Power

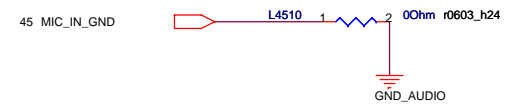
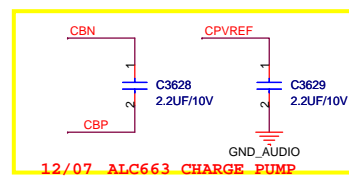
FOR ADJUST MODE:

$$V_o = 1.25 * (1 + R_{3706} / R_{3705})$$

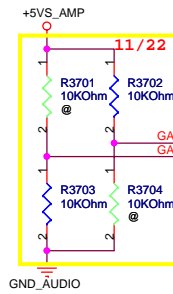
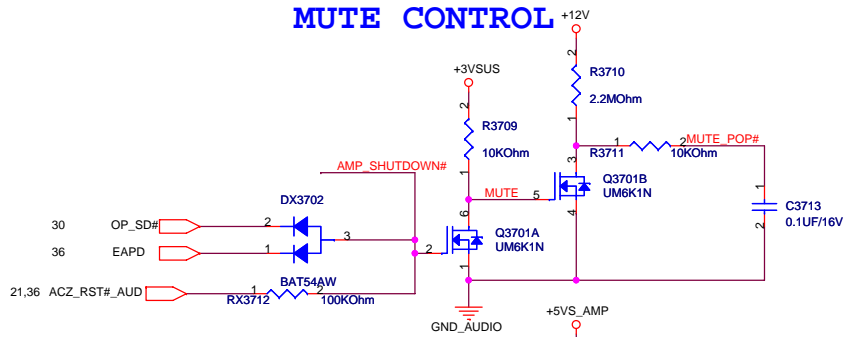
$$= 1.25 * (1 + 100K / 34.8K) = 4.84$$



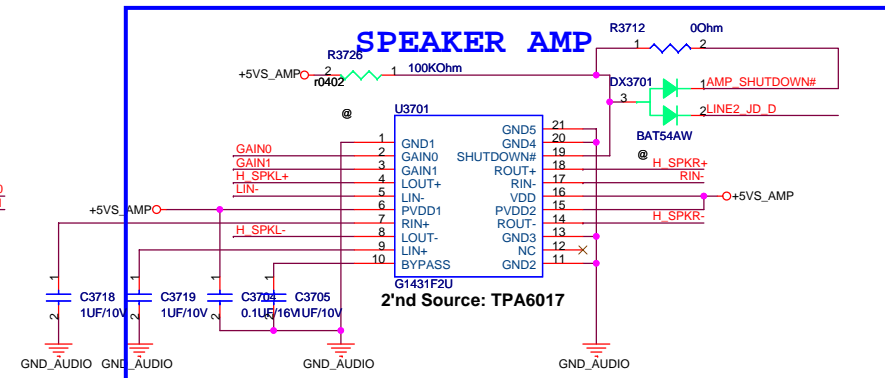
Input impedance: 64K ohm (Typical)



MUTE CONTROL

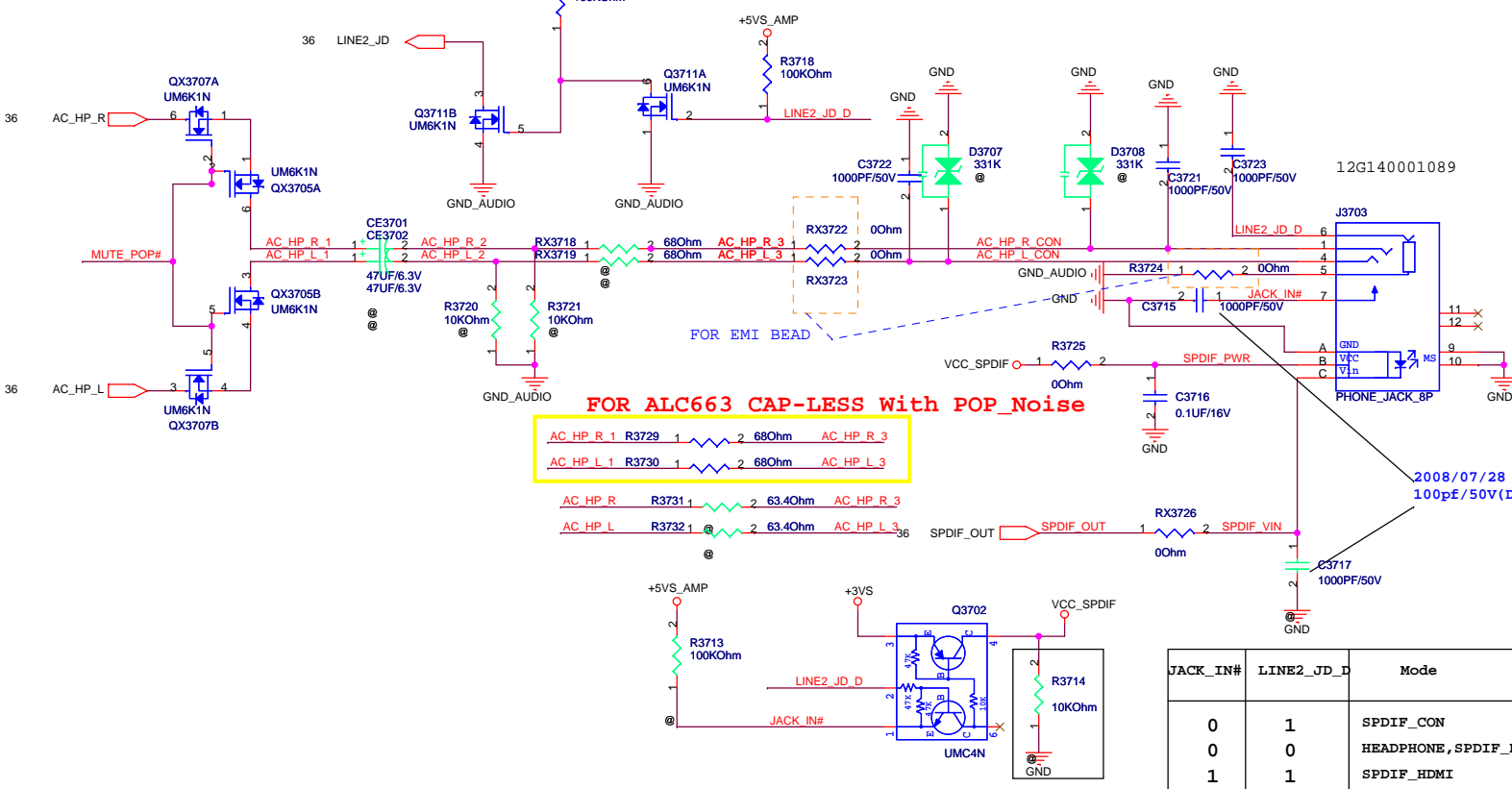


SPEAKER AMP

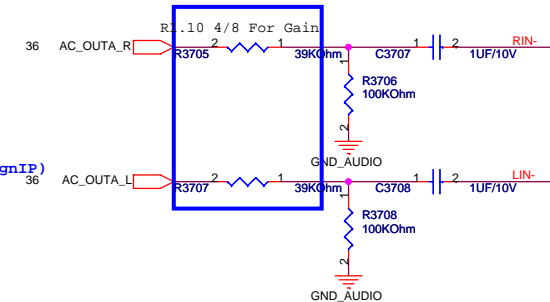
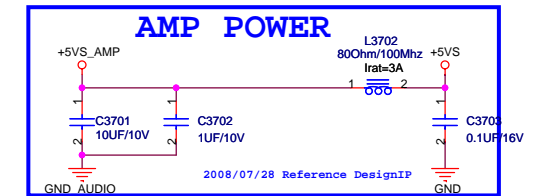


GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

HP & SPDIF CONN

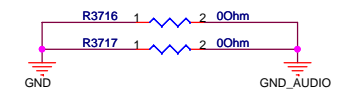


AMP POWER

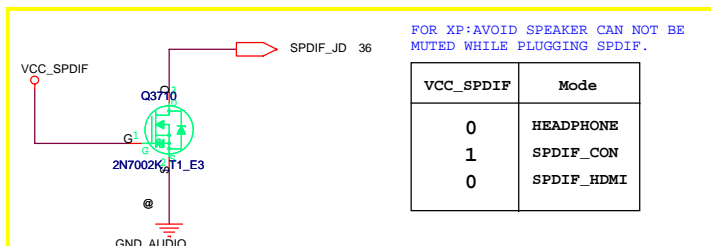
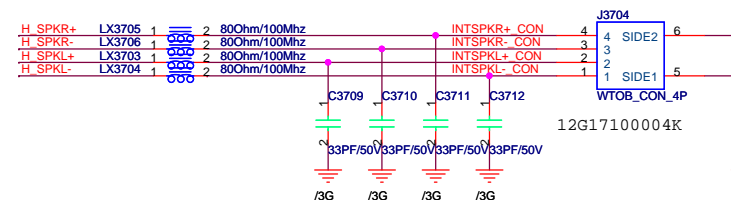


JACK_IN#	LINE2_JD_D	Mode
0	1	SPDIF_CON
0	0	HEADPHONE, SPDIF_HDM
1	1	SPDIF_HDMI

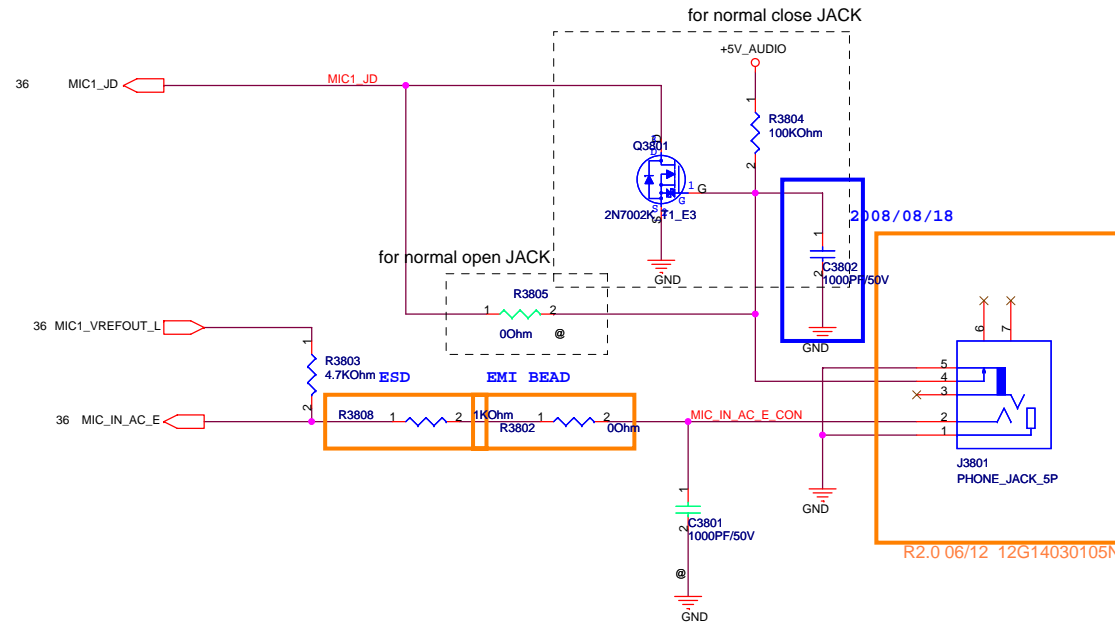
JACK GND




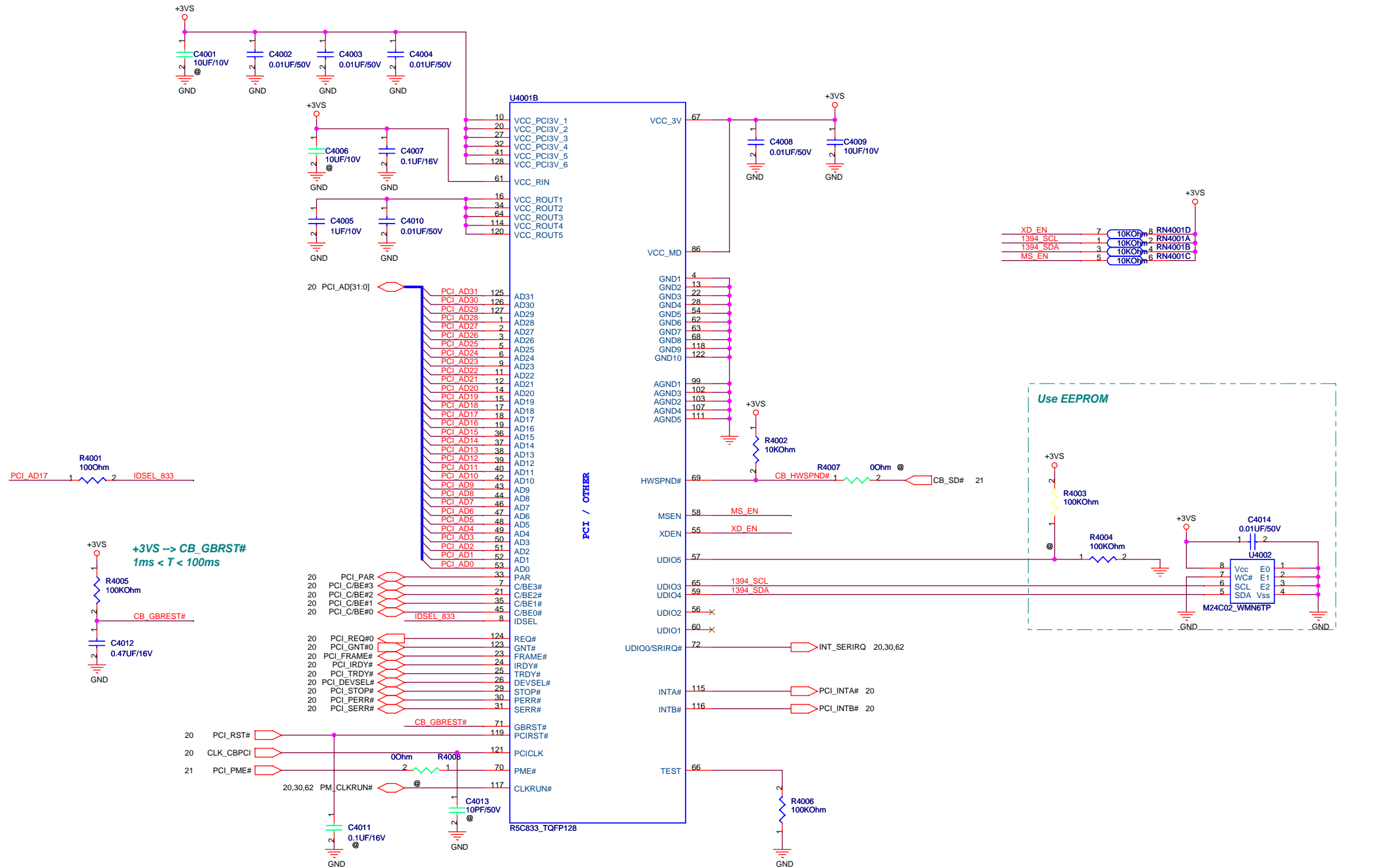
SPEAKER CONNECTOR (2W)



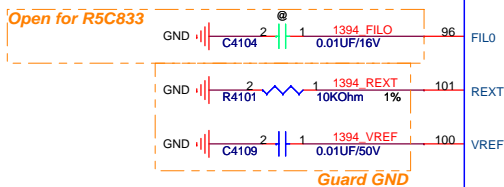
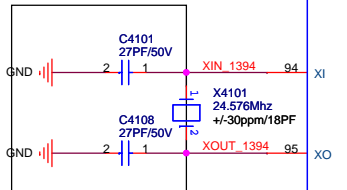
EXTERNAL MICROPHONE



		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
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R1.10 4/8 Item1



AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4

TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0

IREF1394/SD

- MDIO17 87 xD_DAT7 42
- MDIO16 92 xD_DAT6 42
- MDIO15 89 xD_DAT5 42
- MDIO14 91 xD_DAT4 42
- MDIO13 90 SD/MS/xD_DAT3 42
- MDIO12 93 SD/MS/xD_DAT2 42
- MDIO11 81 SD/MS/xD_DAT1 42
- MDIO10 82 SD/MMC/MS/xD_DAT0 42
- MDIO05 75 SDPWR1/xD_WP# 42
- MDIO08 88 SD/MMCCMD_MSBS_xDWE# 42
- MDIO19 83 xD_ALE 42
- MDIO18 85 xD_CLE 42
- MDIO02 78 xD_CE# 42
- MDIO03 77 SDWP#/xDRB# 42
- MDIO00 80 SD/MMCCD#_xDCD0# 42
- MDIO01 79 MSCD#/xDCD1# 42
- MDIO09 84 SD/MMC/MCLK_xDRE# 42
- MDIO04 76 SD/MS/MMC/xDPWR0 42
- MDIO06 74 TPC26T 1 T4101
- MDIO07 73

RSV 97

R5C833_TQFP128

GND

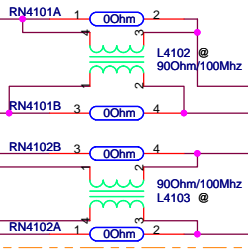
+3VS

L4101
120Ohm/100Mhz

C4105 0.01UF/50V
C4106 0.1UF/16V
C4102 1UF/10V

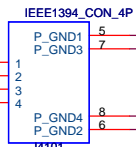
R4102 56Ohm
R4103 56Ohm
C4103 0.01UF/50V
C4107 0.22UF/6.3V

R4104 5.1KOhm
C4110 270PF/50V
R4105 56Ohm
R4106 56Ohm



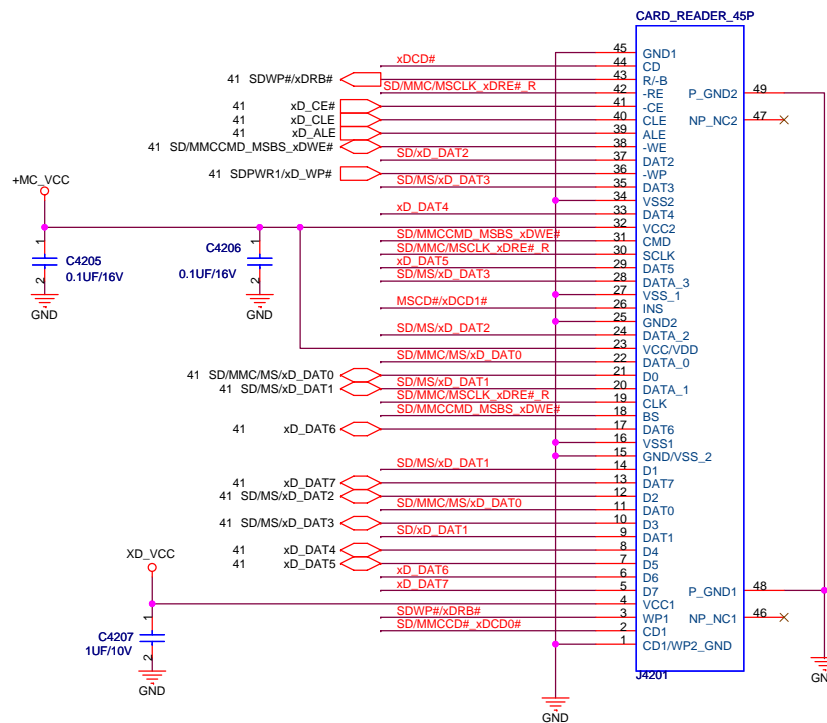
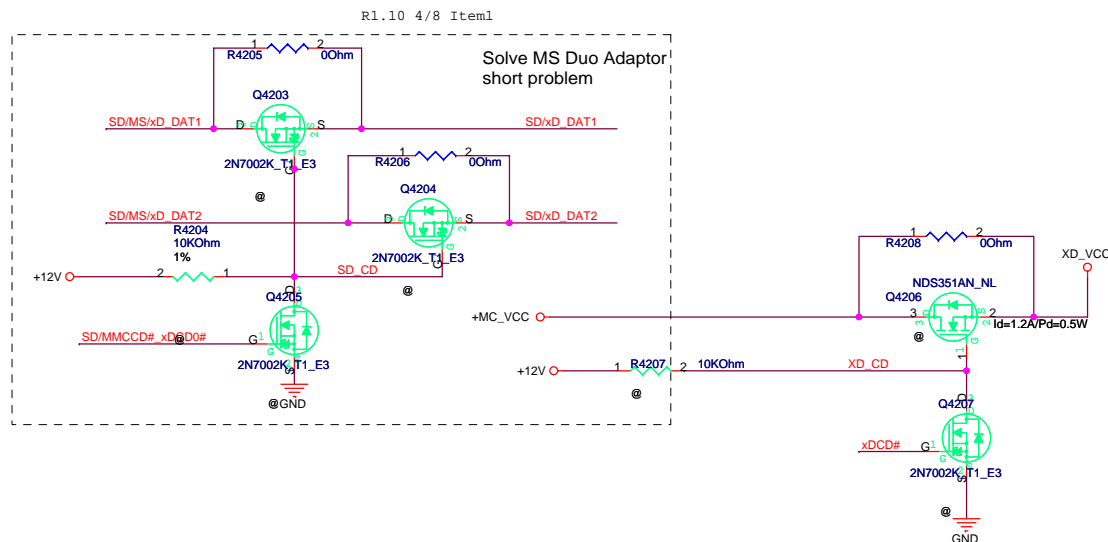
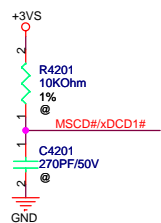
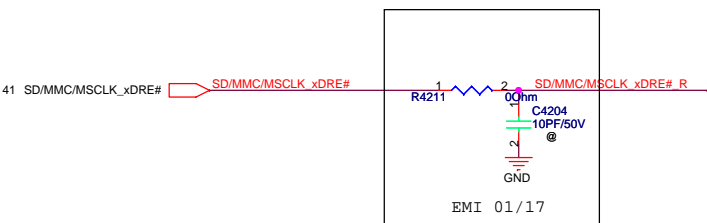
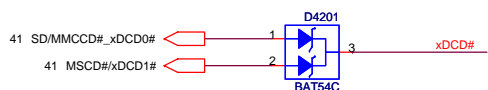
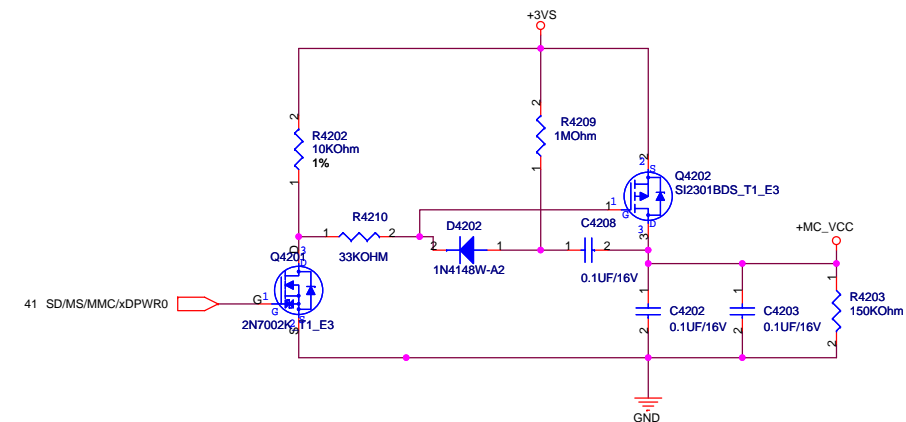
Closed to 1394 Connector
Co-Layout

Closed to
R5C832/R5C833



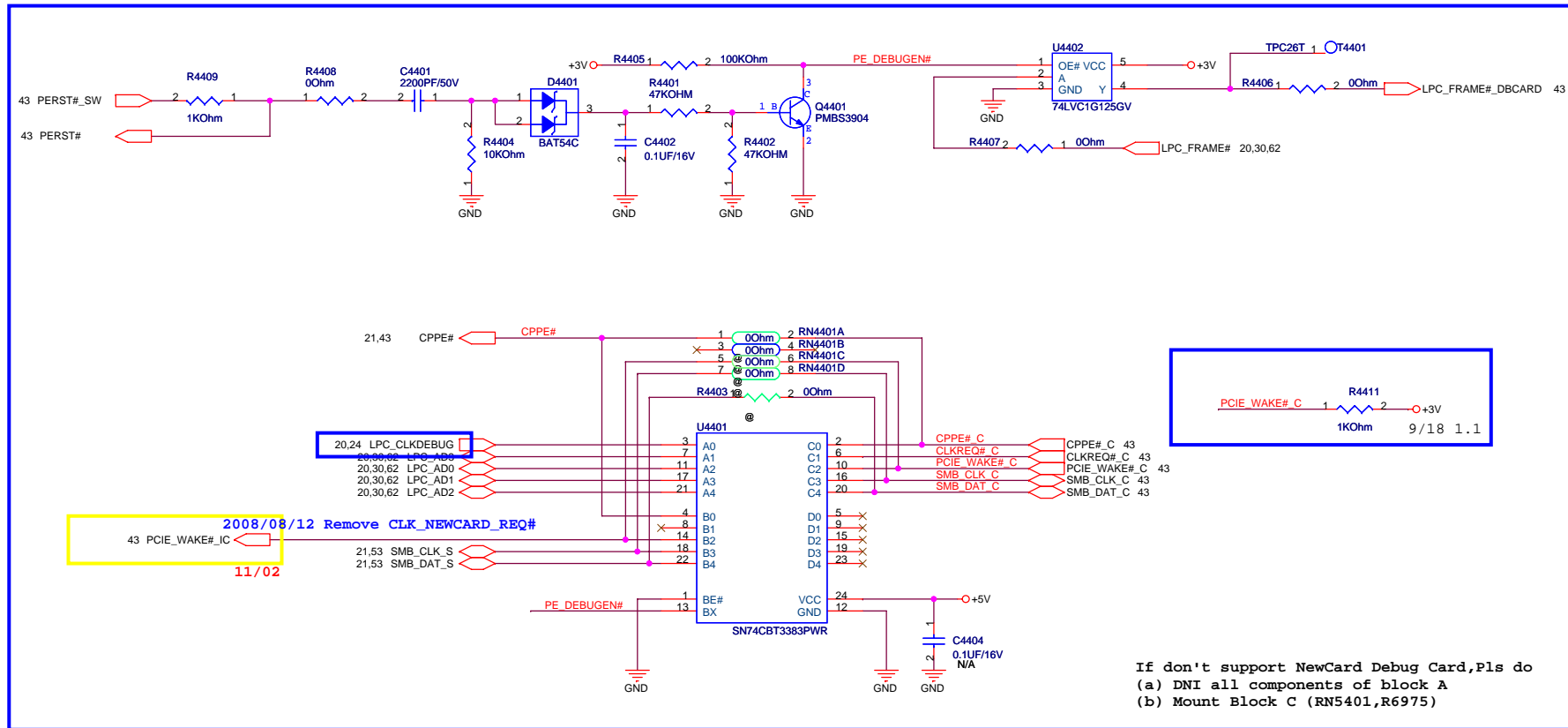
12G13102004Q

GND



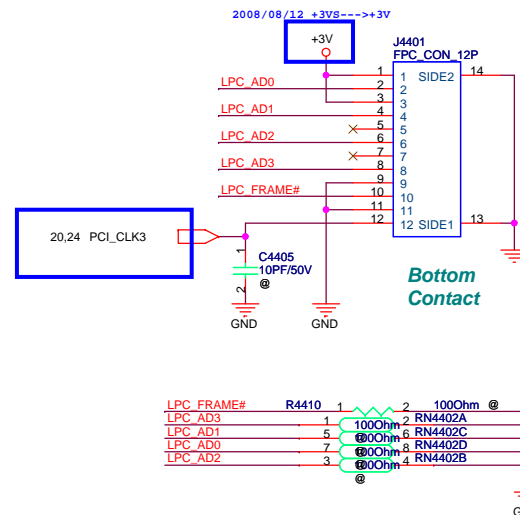


Block A



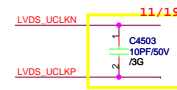
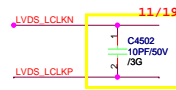
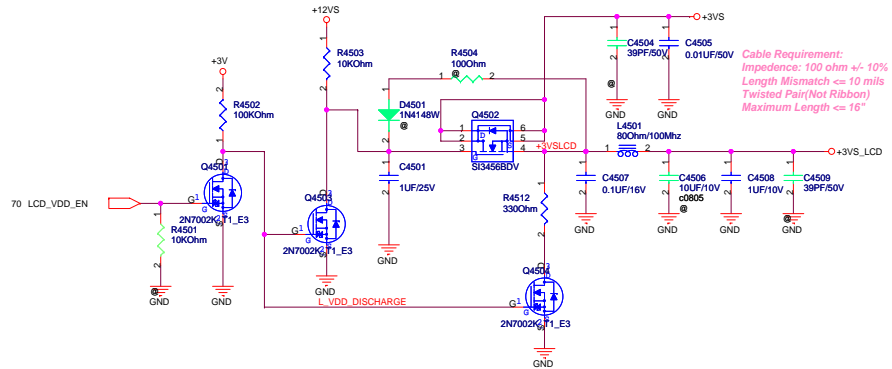
For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.



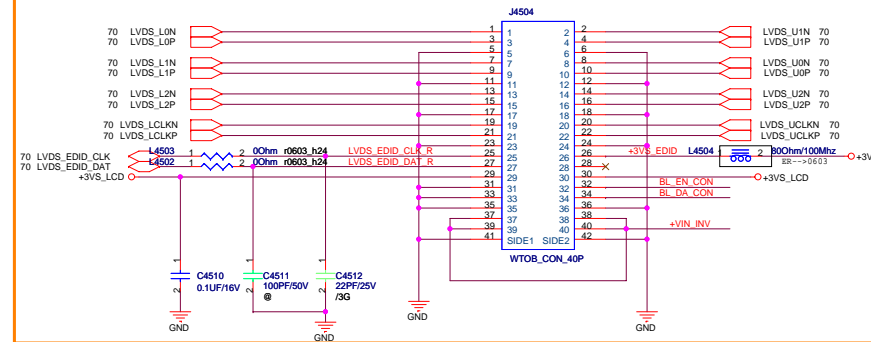
LCD Backlight Control

LCD Power

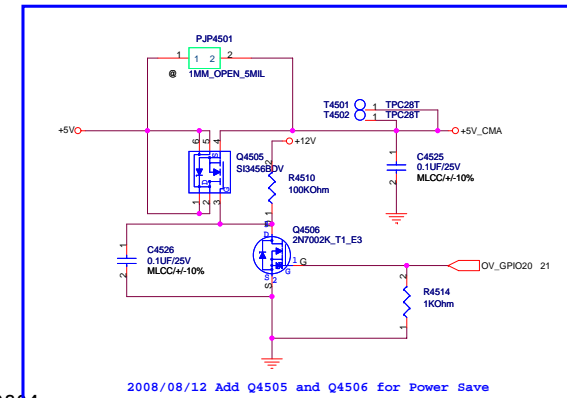
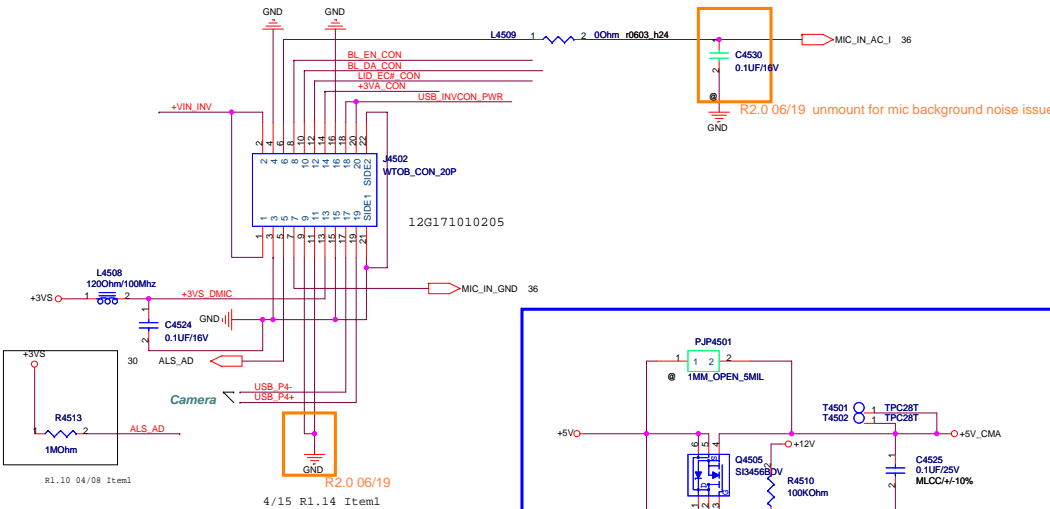
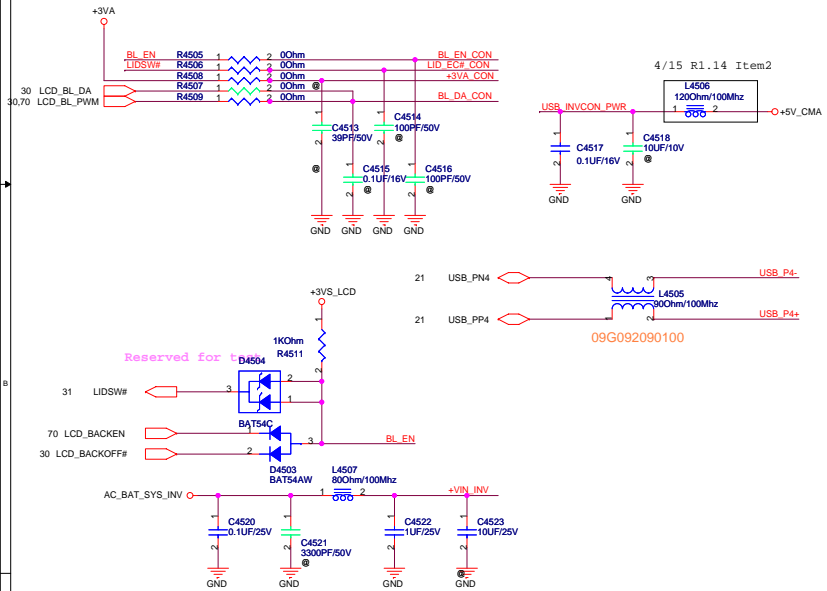


LCD LVDS Interface

R2.0 06/09 12G171010405

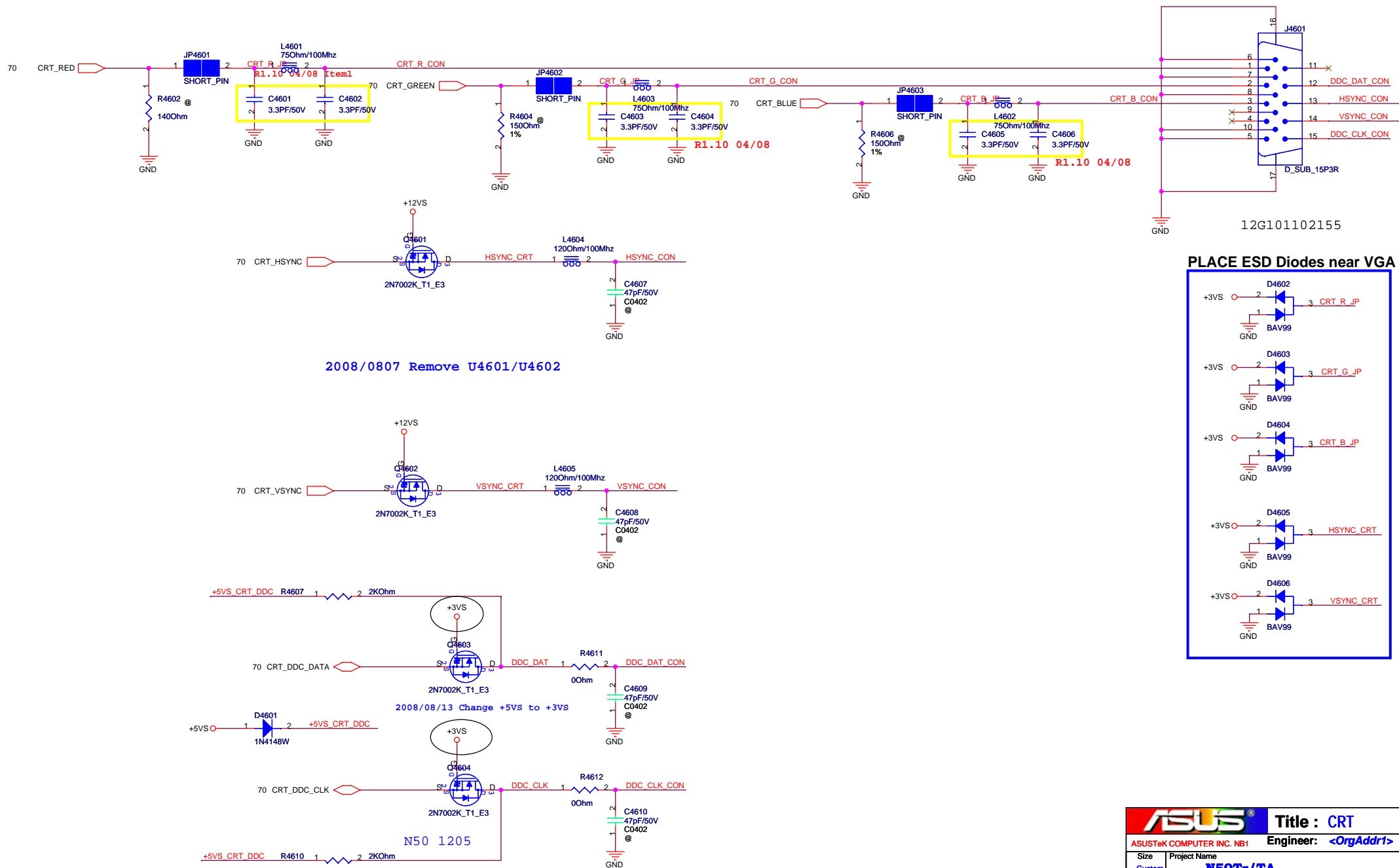


INVERTER
Interface/Speaker CONN.

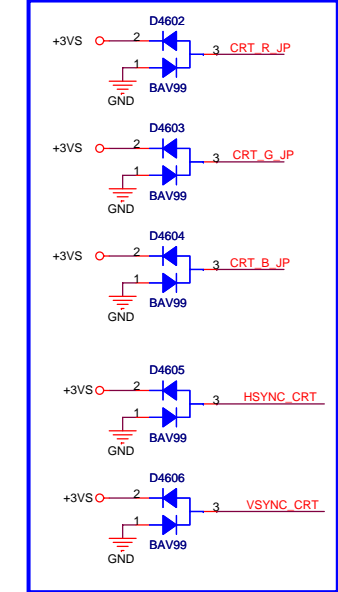


```
delete sim card function 20080804
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2008/08/12 Add Q4505 and Q4506 for Power Save

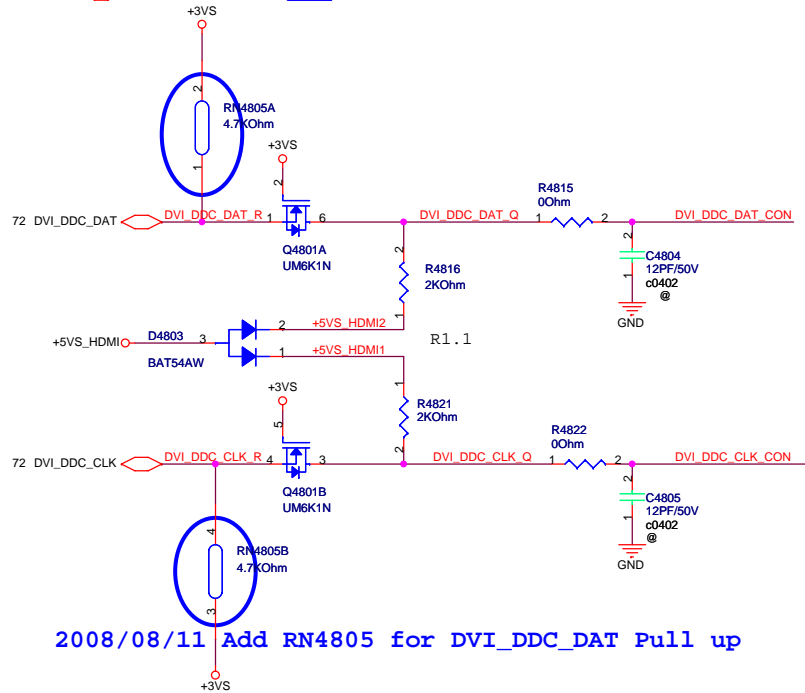
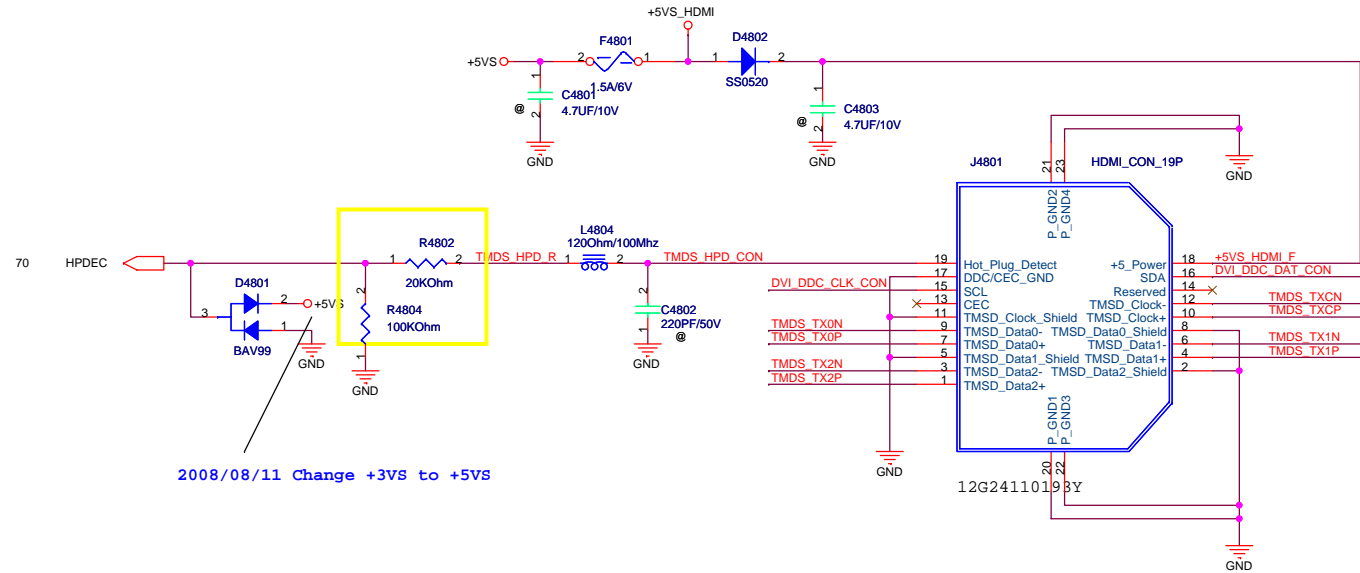
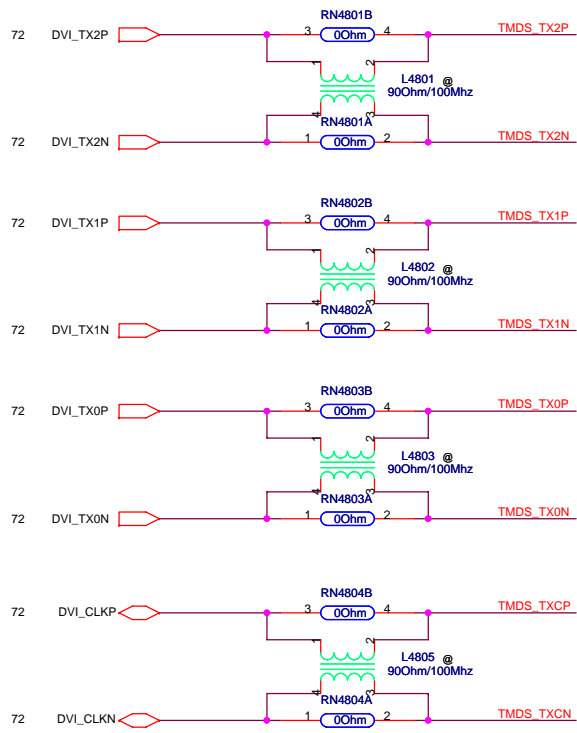


PLACE ESD Diodes near VGA port

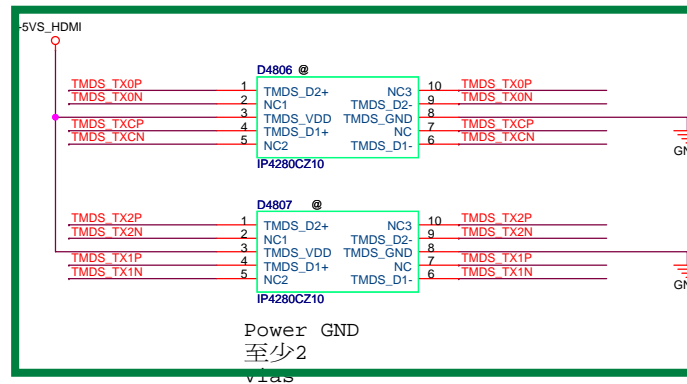


	5	4	3	2	1
D					
C					
B					
A					


		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name N50Tr/TA		Rev 1.00
Date: Thursday, September 25, 2008		Sheet 47 of 93	



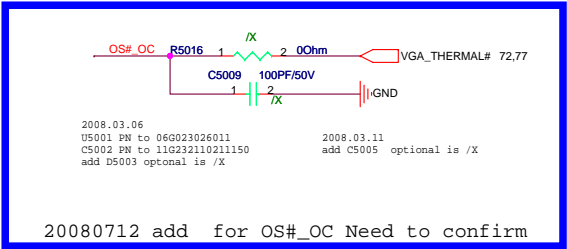
2008/08/11 Add RN4805 for DVI_DDC_DAT Pull up



	5	4	3	2	1
D					
C					
B					
A					

 Title : BLANK		
ASUSTeK COMPUTER INC Engineer:		
Size A	Project Name N50Tr/TA	Rev 1.00
Date: Thursday, September 25, 2008 Sheet 49 of 93		

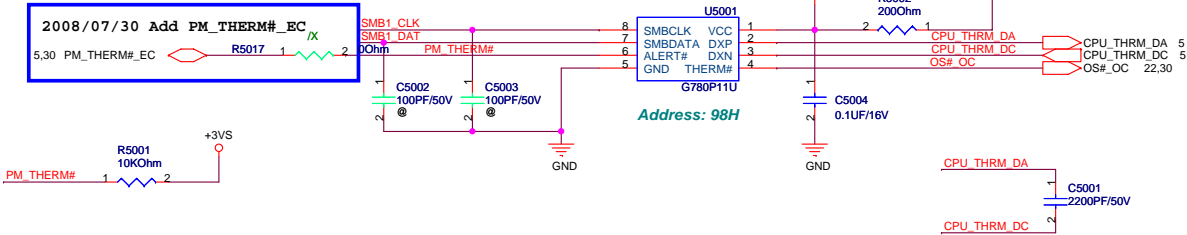
Thermal Sensor



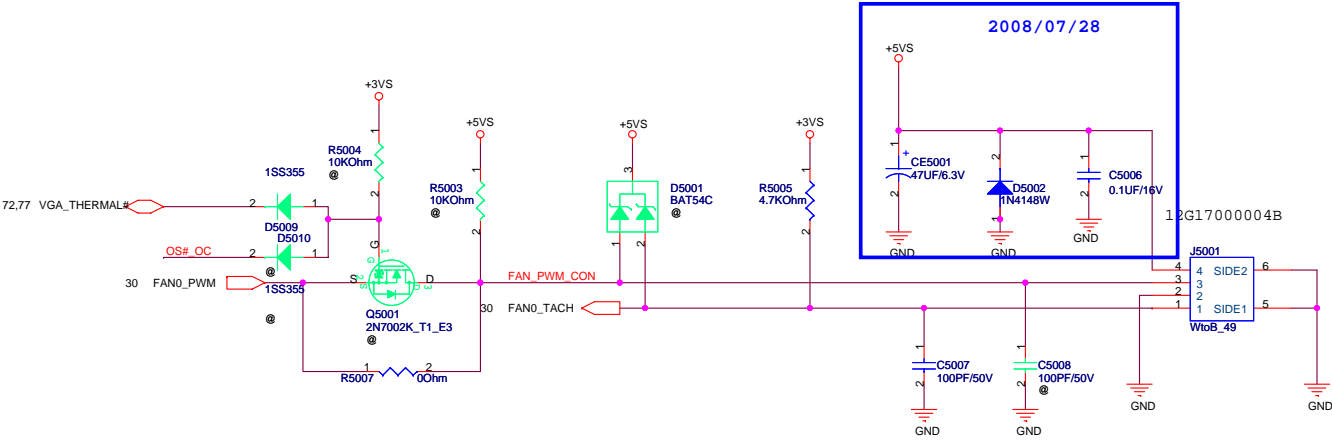
29,30,62,77 SMB1_CLK
29,30,62,77 SMB1_DAT

1st source: 06G023096010
2nd source: 06G023026012

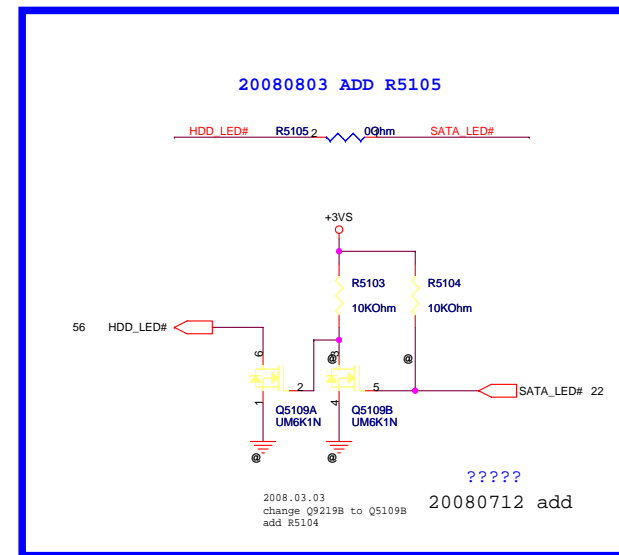
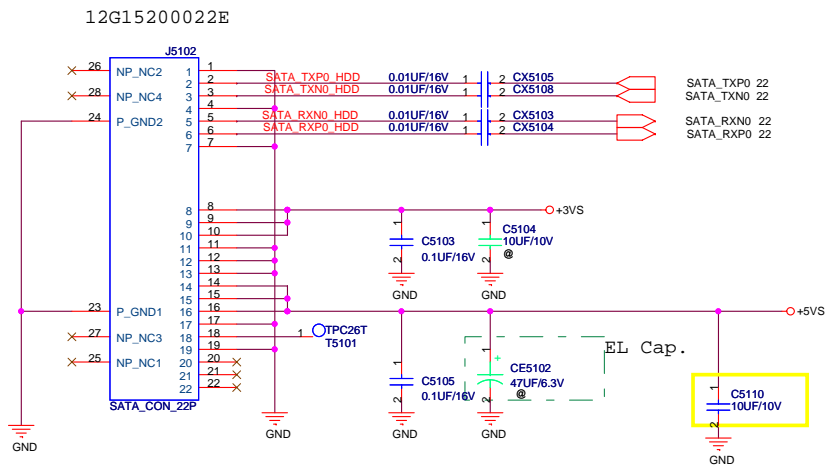
TEMP.SENSOR G780P11U SOP-8 GMT
TEMP SENSOR MAX6657YMS+ SOP-8 MAXIM



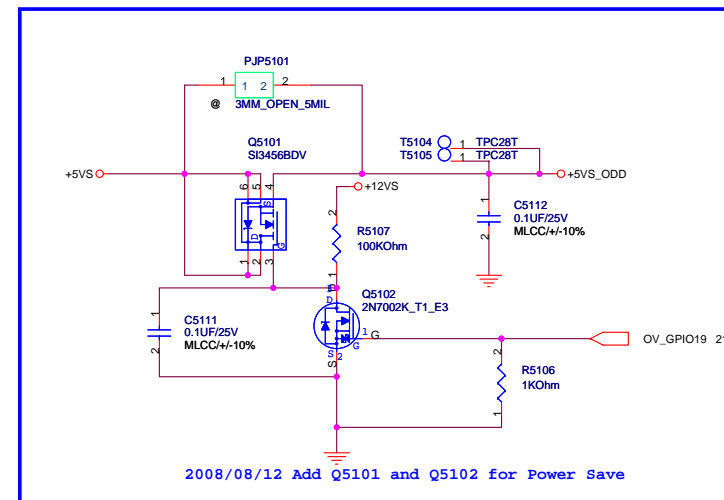
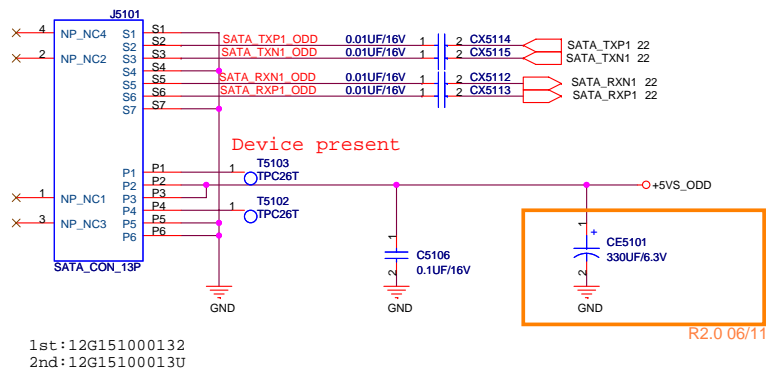
DC FAN Control

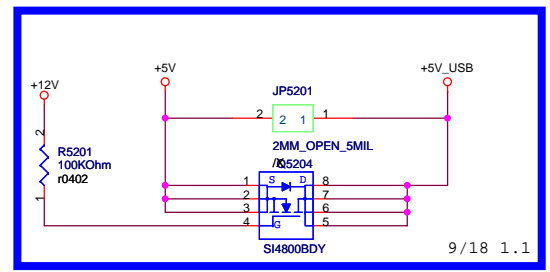
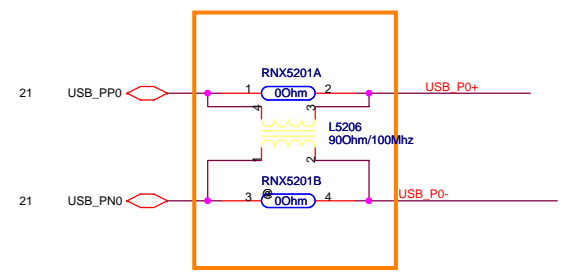
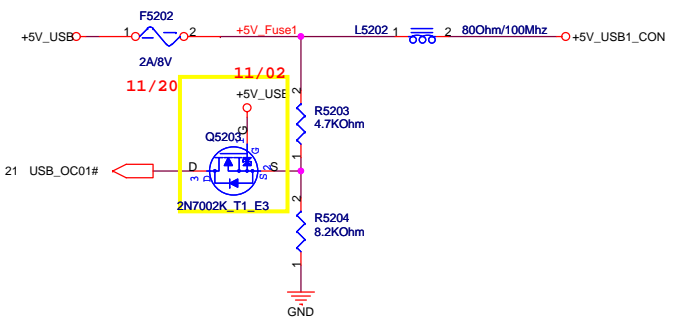
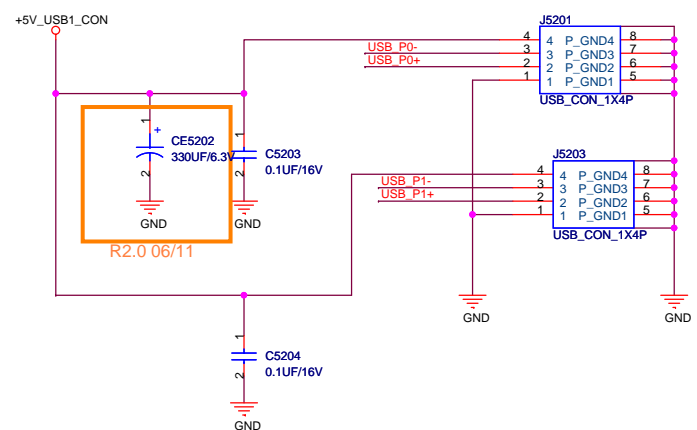
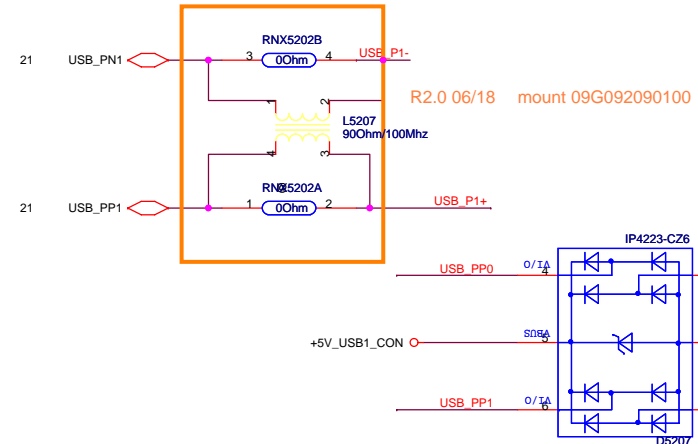
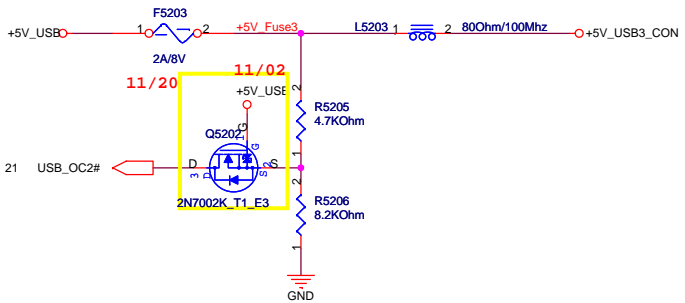
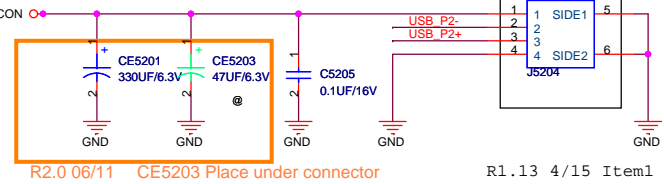
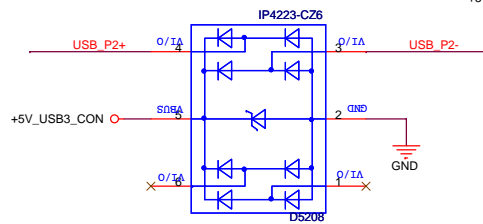
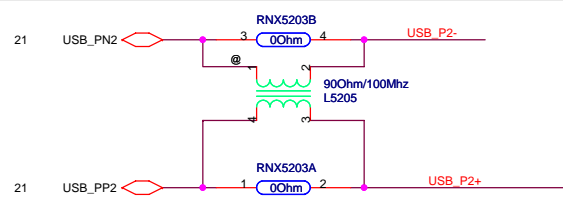


SATA HDD



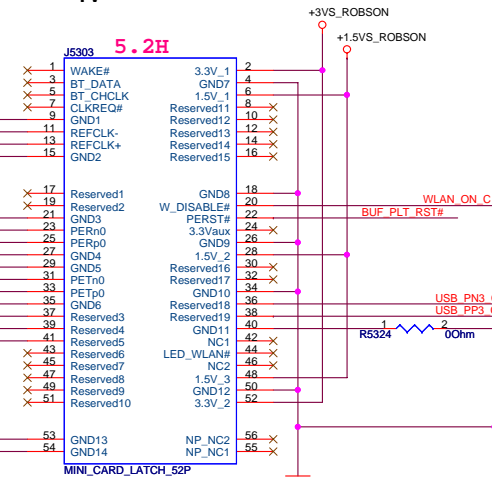
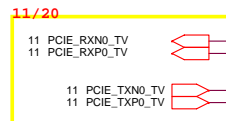
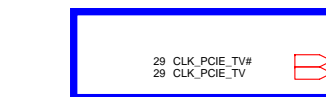
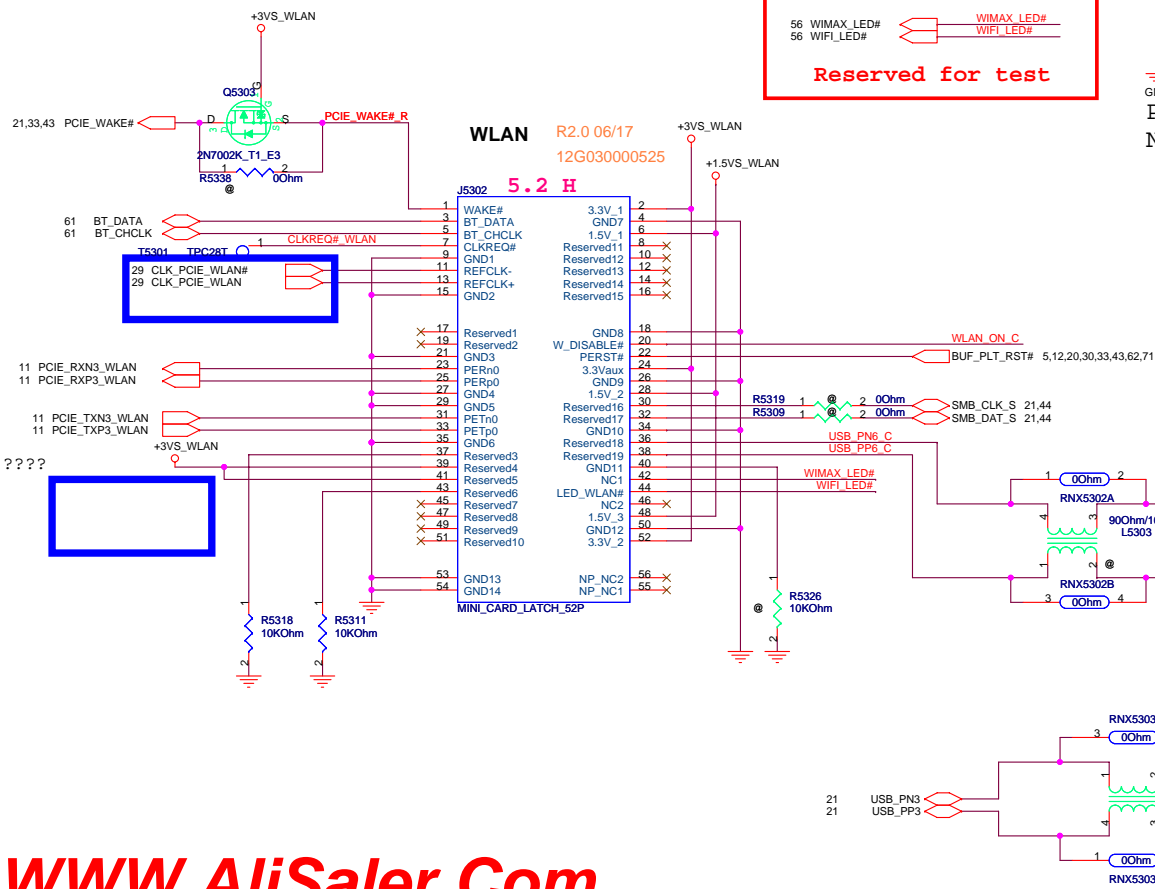
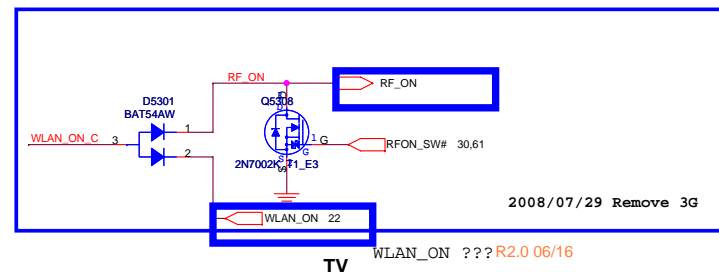
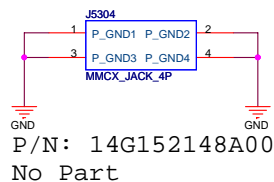
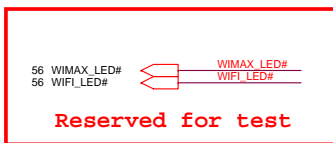
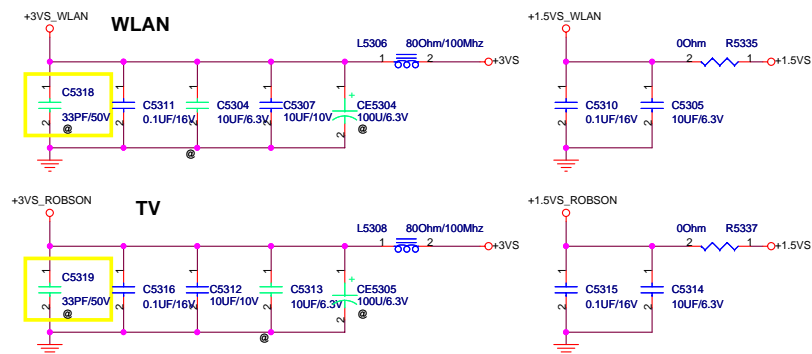
ODD






2008/08/04 Remove SIM Schematic


2008/07/29 Remove 3G



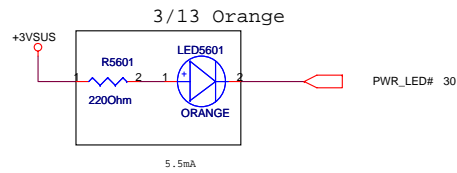
5	4	3	2	1
D				D
C				C
B				B
A				A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
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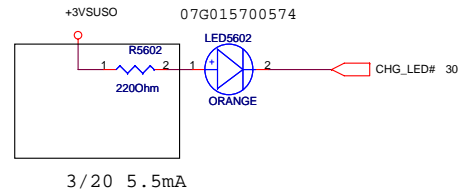
	A	B	C	D	E
1					
2					
3					
4					
5					

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name N50Tr/TA		Rev 1.00
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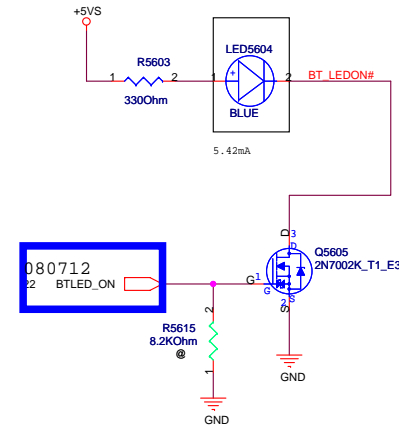
For Power LED



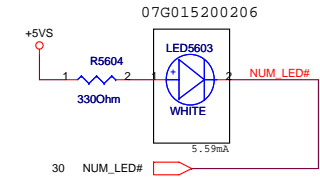
For Battery LED



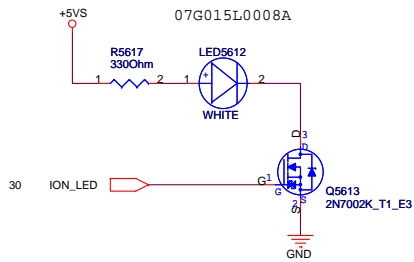
For BT LED



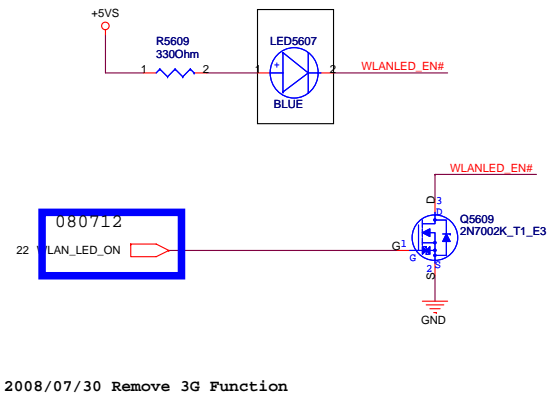
For Number Lock



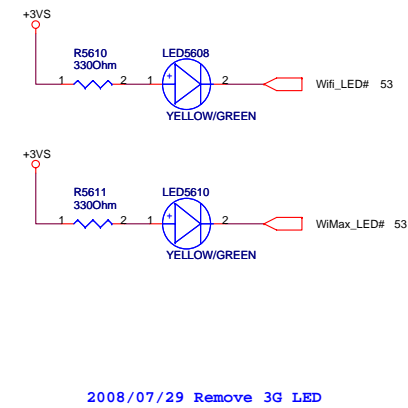
For Ionizer



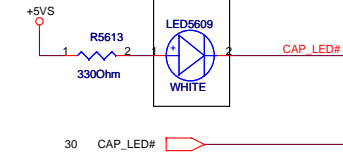
For WireLess LED



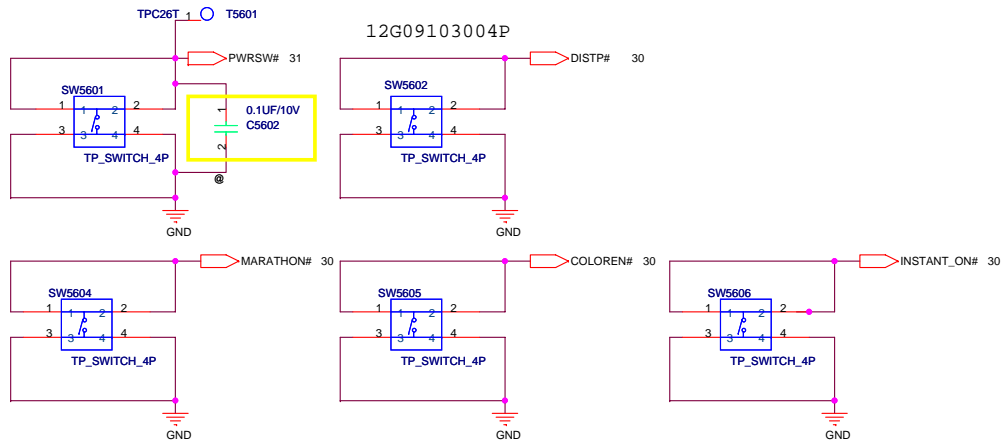
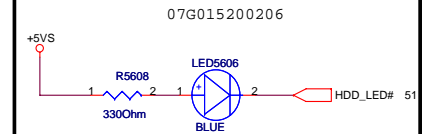
LEDs for testing



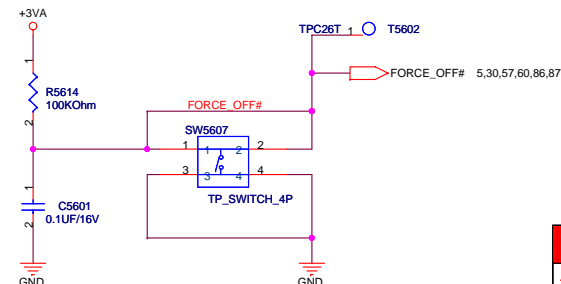
For Caps. Lock

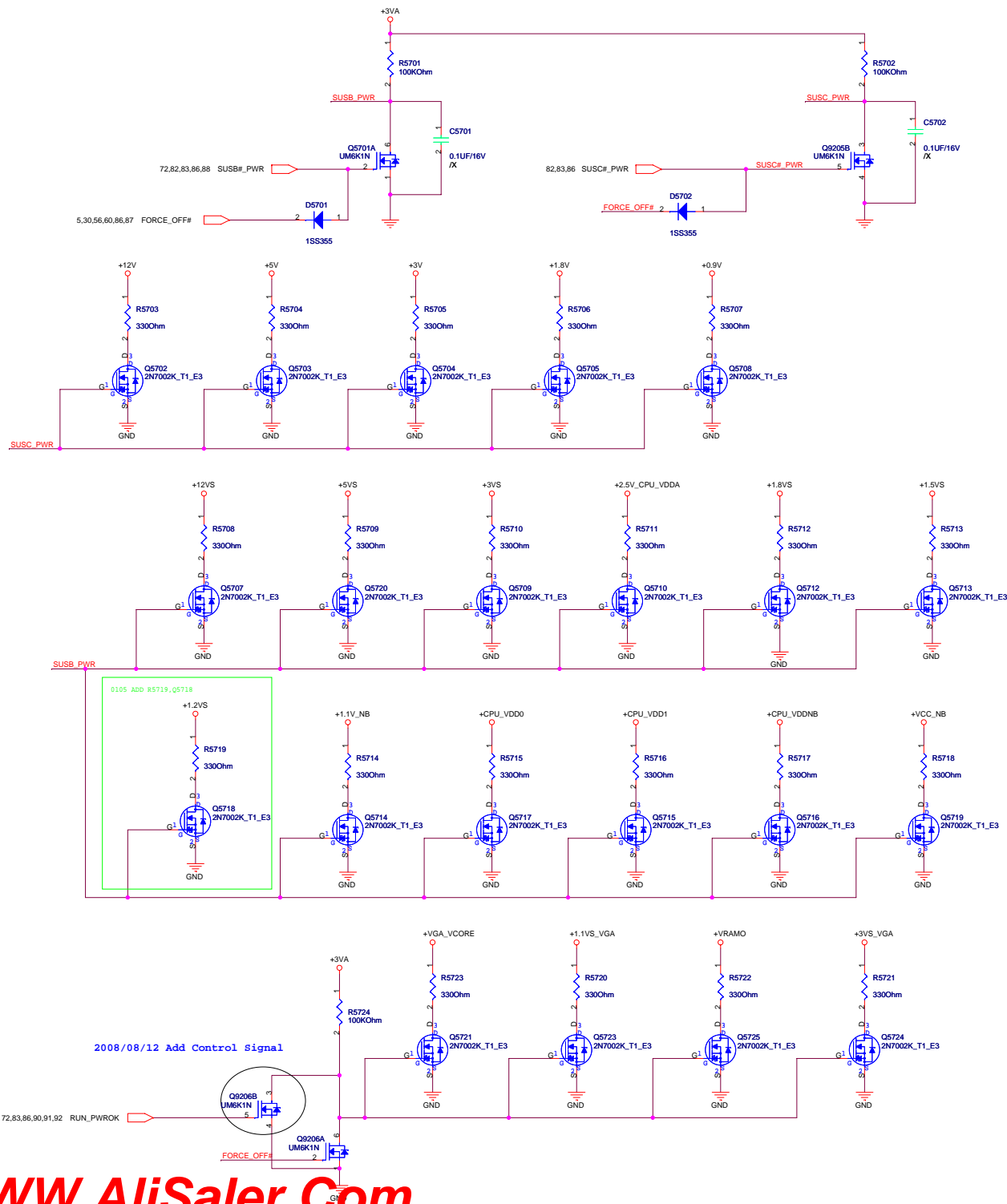


For SATA/IDE LED




SHUT_DOWN#

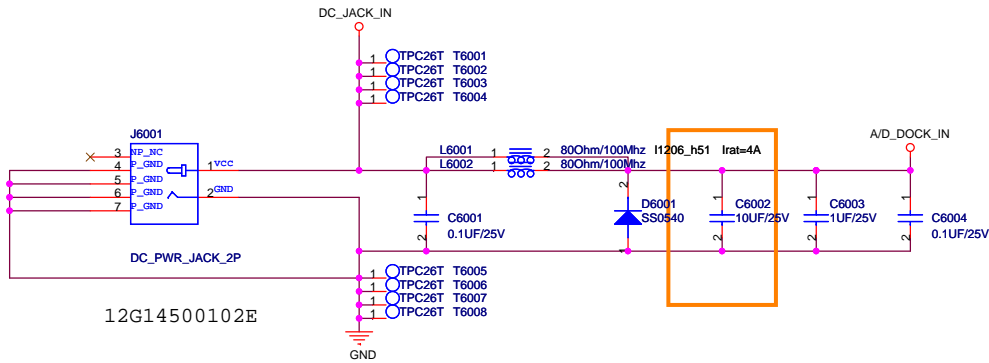




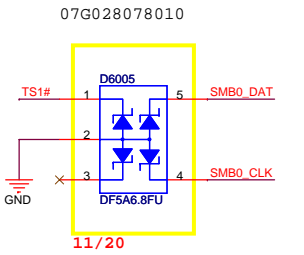
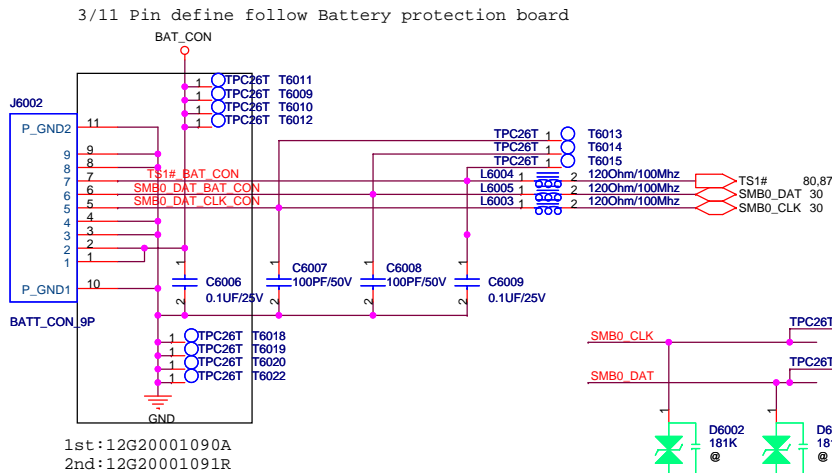


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ASUSTeK COMPUTER INC		Engineer:	
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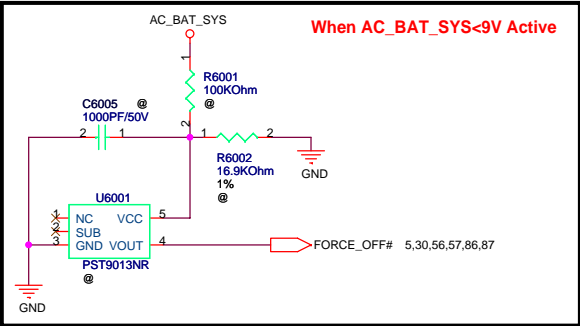
DC IN



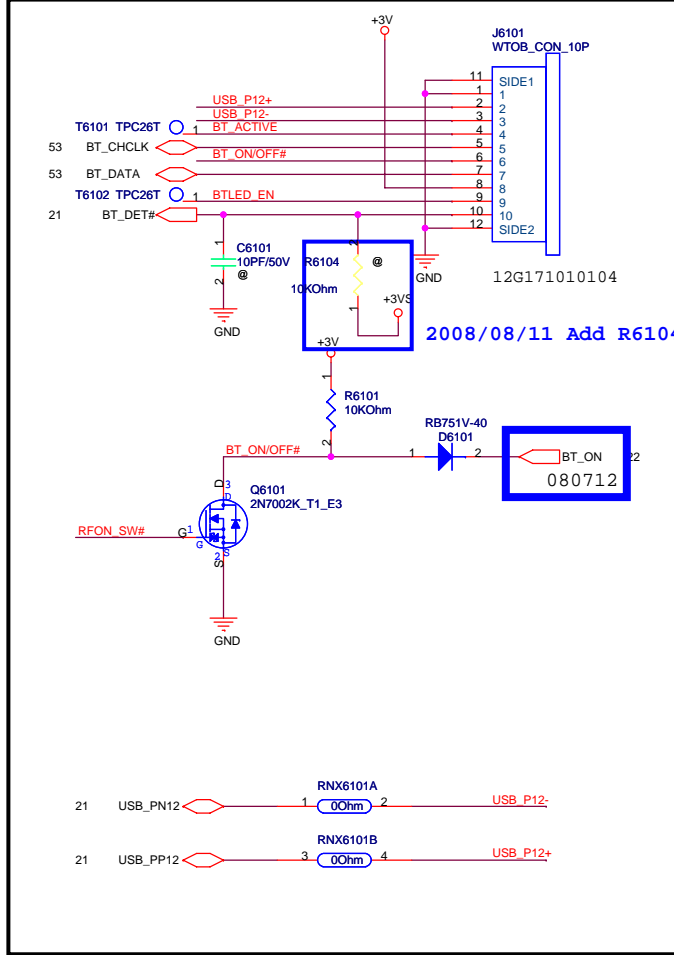
BAT IN



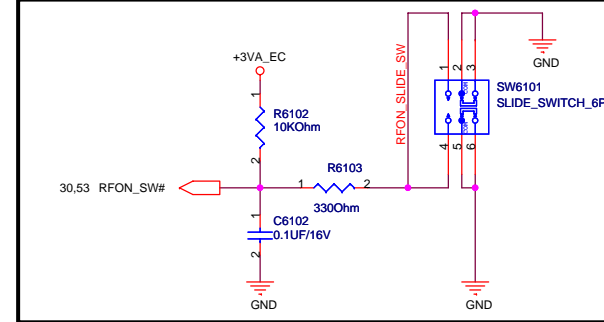
Without Battery & Pull out Adapter



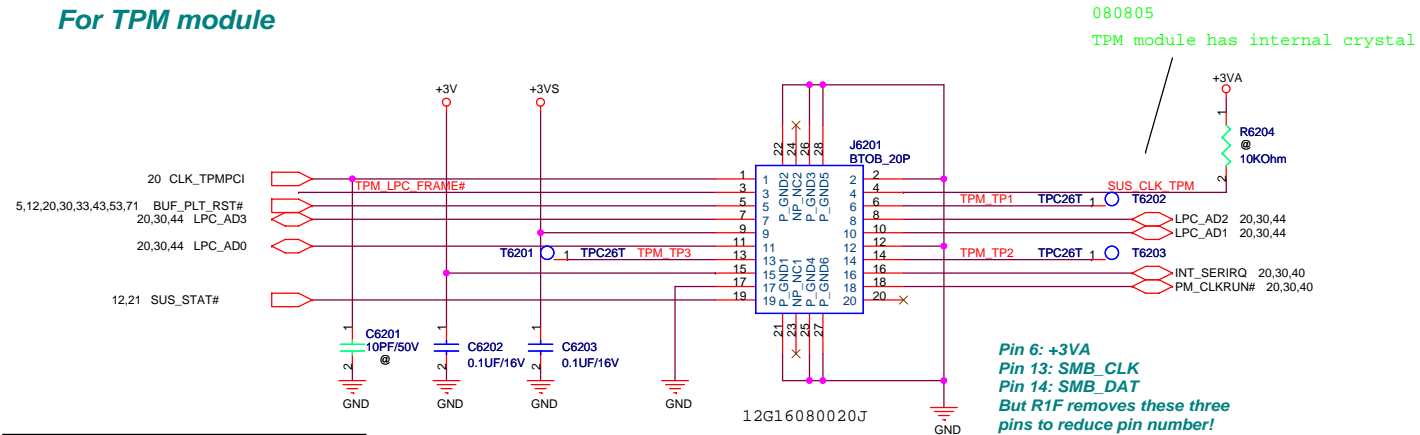
For bluetooth



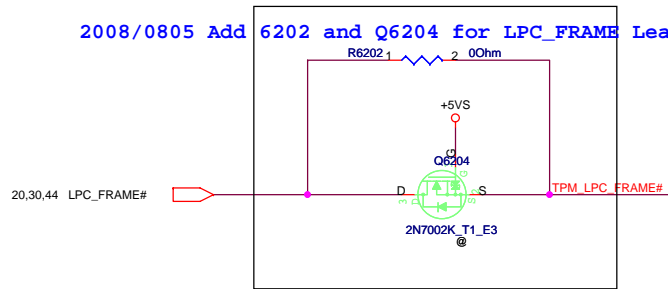
For side SW



For TPM module

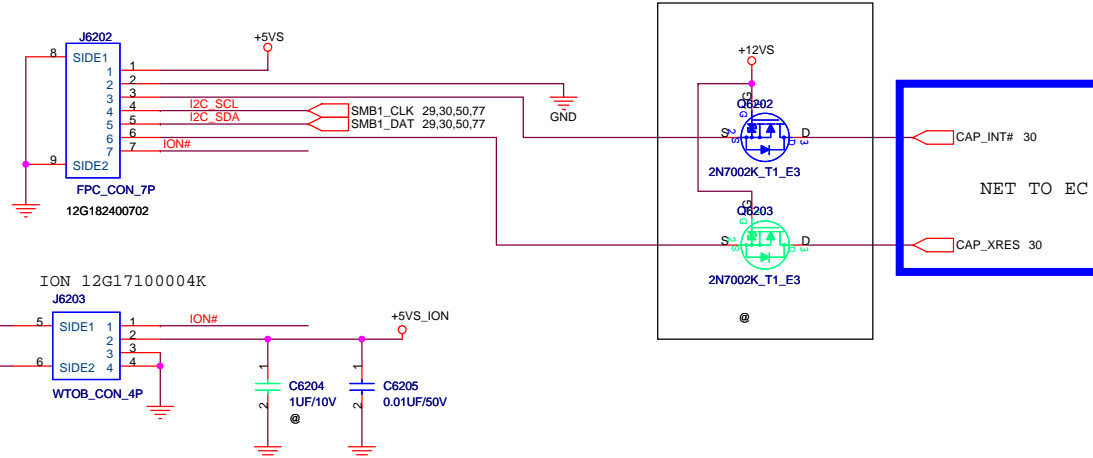


2008/0805 Add 6202 and Q6204 for LPC_FRAME# Leak Current from TPM

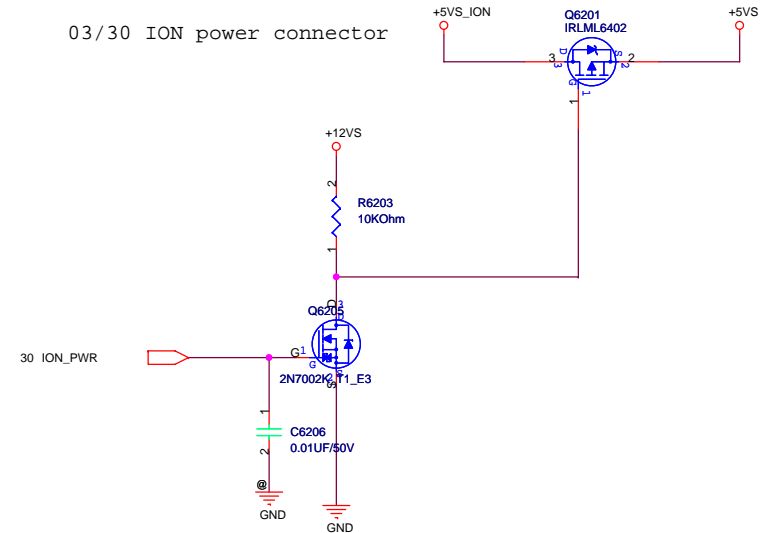


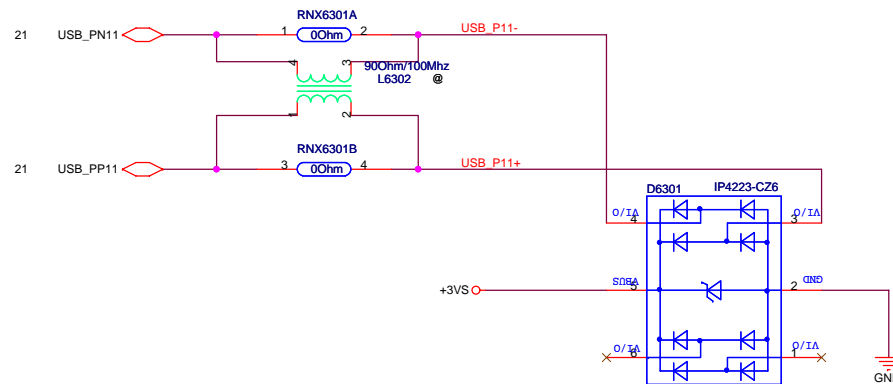
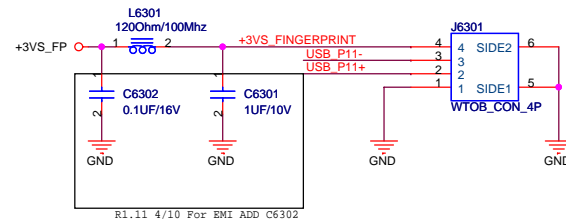
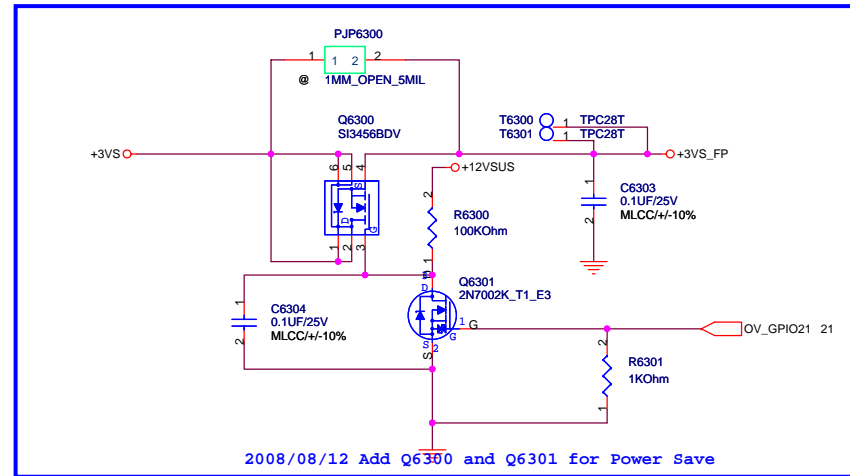
Cap Sensor 12G182400702

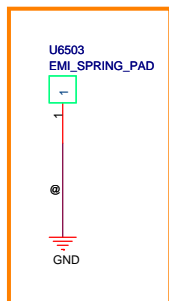
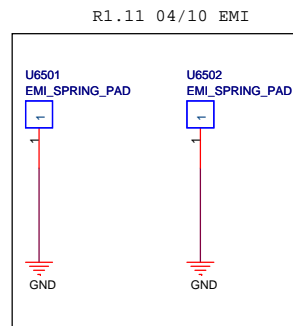
03/21 Cap sensor



03/30 ION power connector

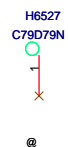




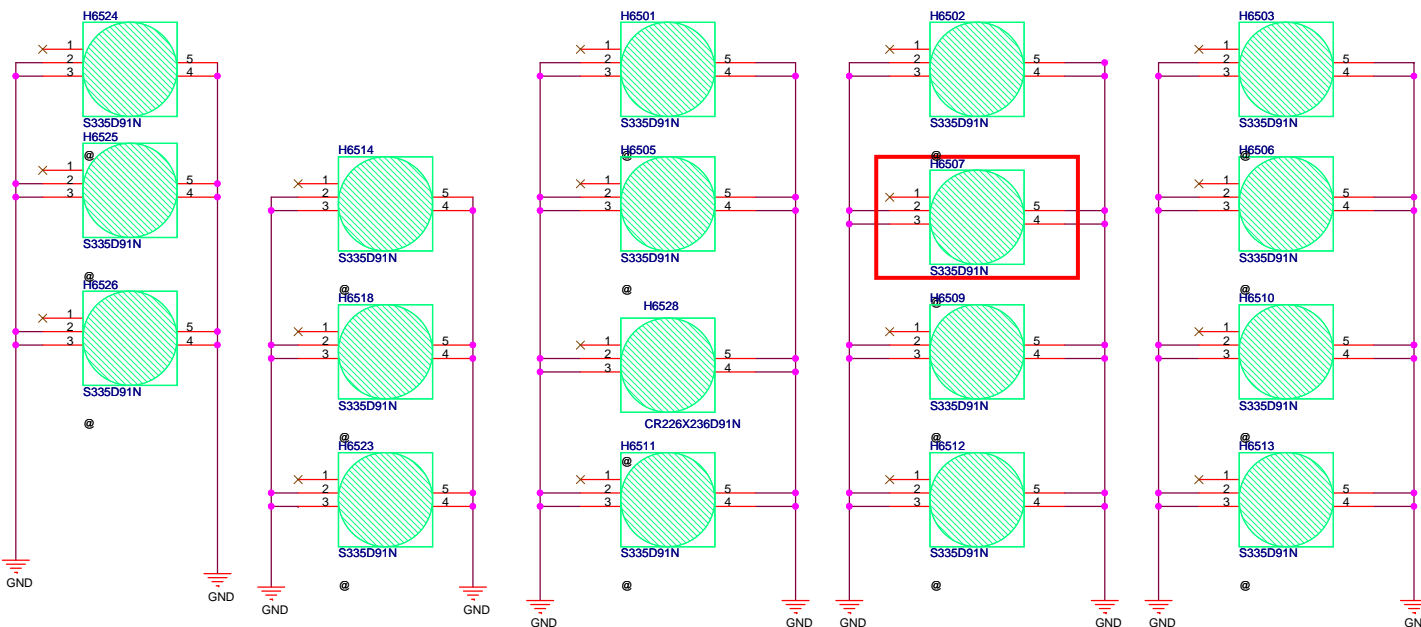


R2.0 06/18 reserve for EMI

固定孔



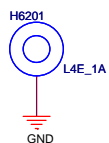
FOR SCREW HOLE



FOR TPM (BOT)

13GN7510M270

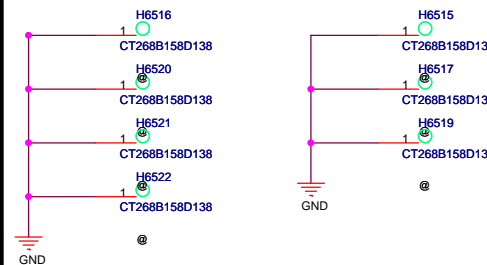
FOR MDC (TOP)



R2.0 06/11 MDC nuts removed

FOR CPU

FOR VGA



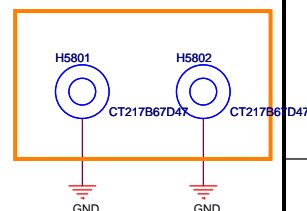
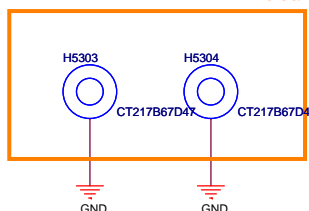
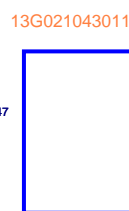
R1.13 4/15 Item1

FOR ROBSON (BOT)

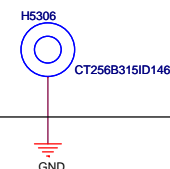
R2.0 06/17

FOR WLAN (BOT)

FOR UWB (BOT)



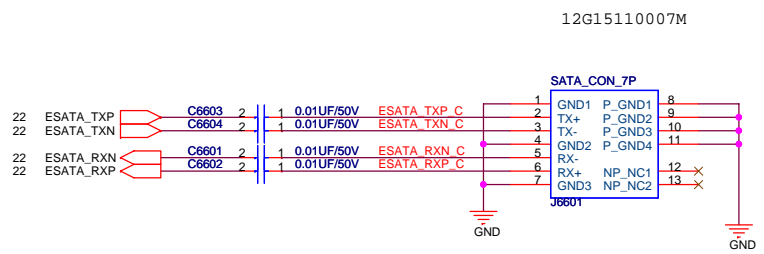
FAN NUT




2008/07/29 Remove 3G

20080723 Remove H5305

MINI PCI-E CON



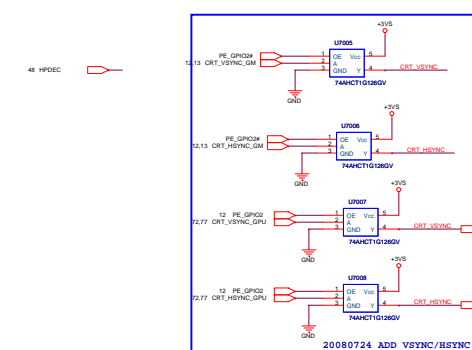
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ASUSTeK COMPUTER INC		Engineer:	
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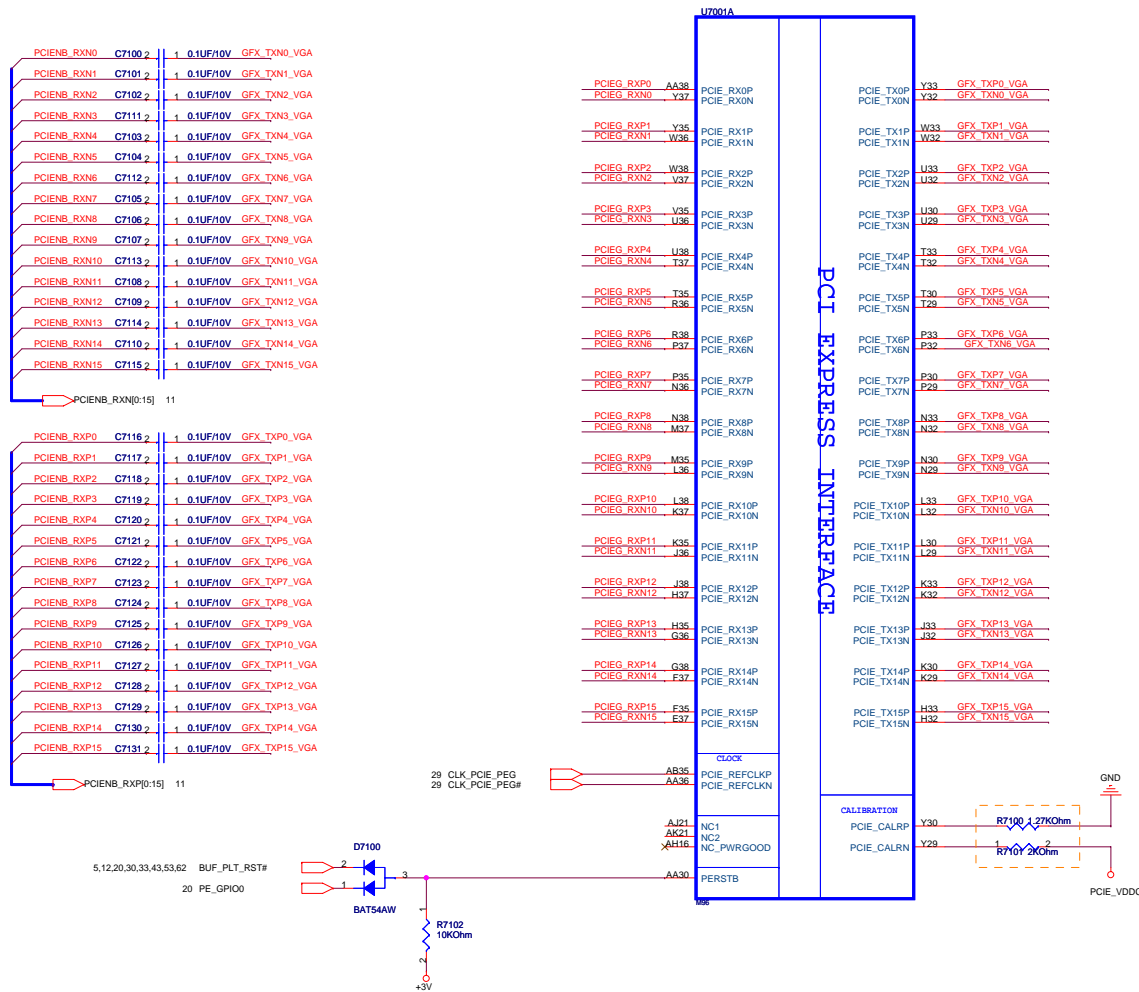
N50Vm Revision History

Rev	Date	Description
1.0	2008/7/24	Swap DDR0/DD1 DATA Signal
1.0	2008/8/03	ADD R5105 for SATA_LED#
1.0	2008/8/03	86_Power_GOOD_DETECTOR → Change +VCC_NB_PWRGD Signal
1.0	2008/8/03	Add U1203.. For AMD PowerGood Glitch
1.0	2008/8/03	Remove R0901,R903,R907
1.0	2008/8/03	Add R3619 for PM_SUSB#
1.0	2008/8/04	1, To support Express Card at E/R,mount Block A except RN4401 & R4403. 2, Unmount C4523 3, Unmount D5009 & 5010 4, Remove L5205,L5206,L5207 and mount RNX5201,RNX5202,RNX5203. 5, Remove CE5203 6, Remove Sim Card:unmount RN5304,R5340,J4503,C4527,C4528,C4529,C4519 7, Mount LED for Test:LED5608,LED5610,R5610,R5611 8, Mount Switch for E/R:SW5601,SW5602,SW5607,SW5605,SW5604 and R5614,C5601
1.0	2008/8/04	Page 70 ADD Q7009,Q7010 FOR leak Current Remove Co-Lay 0 OHM
1.0	2008/8/04	Page 12 the U and L of LVDS exchange
1.0	2008/8/05	Page 80 Add PJP8009 for AC_BAT_SYS_INV
1.0	2008/8/05	Page 70 Exchange LCD_BACKEN and LCD_VDD_EN
1.0	2008/8/05	Page20 Add C2024 for NB_RST# Glitch
1.0	2008/8/05	Page 62 Add 6202 and Q6204 for LPC_FRAME Leak Current from TPM
1.0	2008/8/05	Page 62 Add R6204 for SUS_CLK_TPM
1.0	2008/8/05	Page 72 Add R7253 and R7254
1.0	2008/8/07	Page 70 Add R7039,R7040,R7041,R7042
1.0	2008/8/07	Page 46 Remove U4601/U4602
1.0	2008/8/07	Page 46 Add JP2101 for Warm Reset
1.0	2008/8/07	Page 21 Remove R2144,R2143
1.0	2008/8/11	Page 73,76 PCIE_VDDR Change to PCIE_VDDR_G
1.0	2008/8/11	Page61 Add R6104 for BT_DET#
1.0	2008/8/11	Page30 Add T3010,T3011
1.0	2008/8/11	Page70 Remove RN7009,RN7010,RN7011,RN7012,R7034,R7036
1.0	2008/8/11	Page 77Add R7732/R7731/R7730/R7729/R7735/R7734/R7733/R7728
1.0	2008/8/11	Page 76 Add RN4805 for DVI_DDC_DAT/DVI_DDC_CLK Pull up
1.0	2008/8/11	Page13 Remove C1307/L1301/C1308/L1302

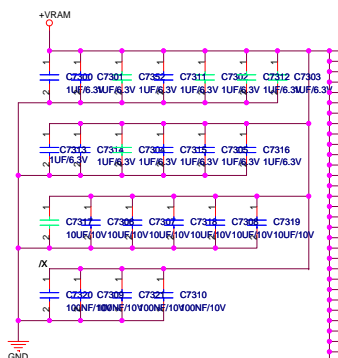
Rev	Date	Description
1.0	2008/8/12	Page70 AMD Review Add Q7011,Q7012,Q7013,Q7014
1.0	2008/8/12	Page53 Remove Q5309
1.0	2008/8/12	Page45 Add Q4505 and Q4506 for Power Save
1.0	2008/8/12	Page51 Add Q5101 and Q5102 for Power Save
1.0	2008/8/12	Page53 Add Q6300 and Q6301 for Power Save
1.0	2008/8/17	Page72 Add Q7202 Remove D7201



11 PCIEG_RXP[0:15]
11 PCIEG_RXN[0:15]



2008/08/12 Change +3V to +3VS_VGA



U7001F

MEM I/O

AC7	VDDR1_1
AD11	VDDR1_2
AE7	VDDR1_3
AG10	VDDR1_4
AI7	VDDR1_5
AK6	VDDR1_6
AL9	VDDR1_7
GI11	VDDR1_8
G14	VDDR1_9
G17	VDDR1_10
G20	VDDR1_11
G23	VDDR1_12
G26	VDDR1_13
G29	VDDR1_14
G32	VDDR1_15
J7	VDDR1_16
K11	VDDR1_17
K13	VDDR1_18
K8	VDDR1_19
L12	VDDR1_20
L16	VDDR1_21
L21	VDDR1_22
L23	VDDR1_23
L26	VDDR1_24
L7	VDDR1_25
M11	VDDR1_26
N11	VDDR1_27
R7	VDDR1_28
R11	VDDR1_29
U7	VDDR1_30
Y11	VDDR1_31
Y7	VDDR1_32
	VDDR1_33
	VDDR1_34

POWER

LEVEL TRANSLATION

AF26	VDD_CT_1
AF27	VDD_CT_2
AG26	VDD_CT_3
AG27	VDD_CT_4

POWER

I/O

AF24	VDDR3_1
AF24	VDDR3_2
AG23	VDDR3_3
AG24	VDDR3_4

POWER

MEM CLK

AD12	VDDR4_1
AE11	VDDR4_2
AE12	VDDR4_3
AG11	VDDR4_4

POWER

PLL

AB37	PCIE_PVDD
H7	NC_MPV18_1
H8	NC_MPV18_2

POWER

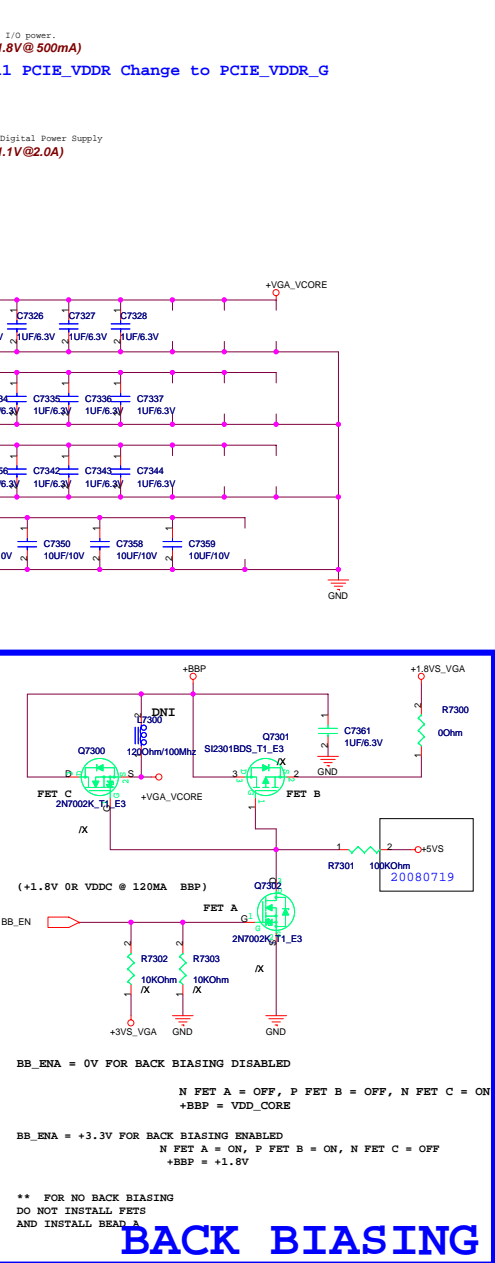
BACK BIAS

AA13	BBP1
Y13	BBP2

POWER

ISOLATED CORE I/O

M15	VDDCI1
N13	VDDCI2
T12	VDDCI3

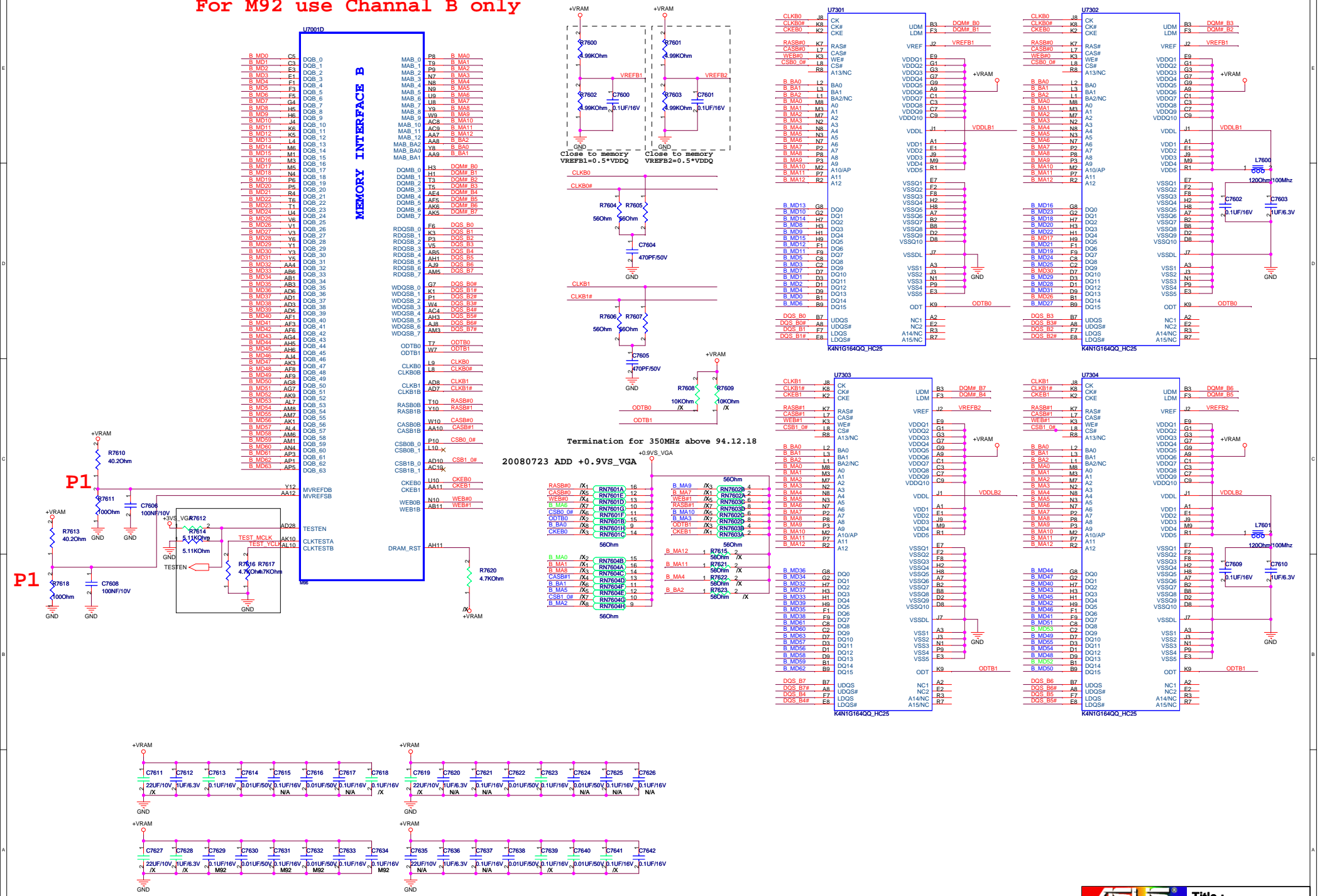


U7001F

AB39	PCIE_VSS1
E39	PCIE_VSS2
F34	PCIE_VSS3
F39	PCIE_VSS4
G33	PCIE_VSS5
G34	PCIE_VSS6
H31	PCIE_VSS7
H34	PCIE_VSS8
H39	PCIE_VSS9
J31	PCIE_VSS10
J34	PCIE_VSS11
K31	PCIE_VSS12
K34	PCIE_VSS13
K39	PCIE_VSS14
L31	PCIE_VSS15
L34	PCIE_VSS16
M39	PCIE_VSS17
N31	PCIE_VSS18
N34	PCIE_VSS19
P31	PCIE_VSS20
P34	PCIE_VSS21
P39	PCIE_VSS22
R34	PCIE_VSS23
T34	PCIE_VSS24
T39	PCIE_VSS25
U31	PCIE_VSS26
U34	PCIE_VSS27
U39	PCIE_VSS28
V34	PCIE_VSS29
V39	PCIE_VSS30
W31	PCIE_VSS31
W34	PCIE_VSS32
W39	PCIE_VSS33
Y34	PCIE_VSS34
Y39	PCIE_VSS35



For M92 use Channal B only



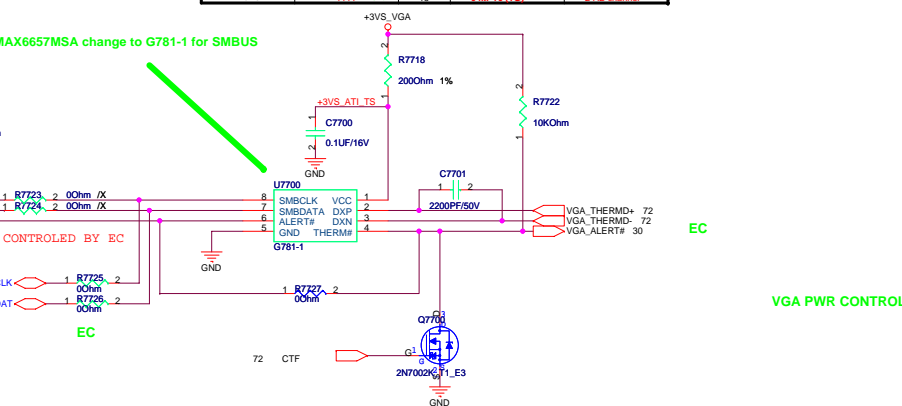
OPTION STRAPS

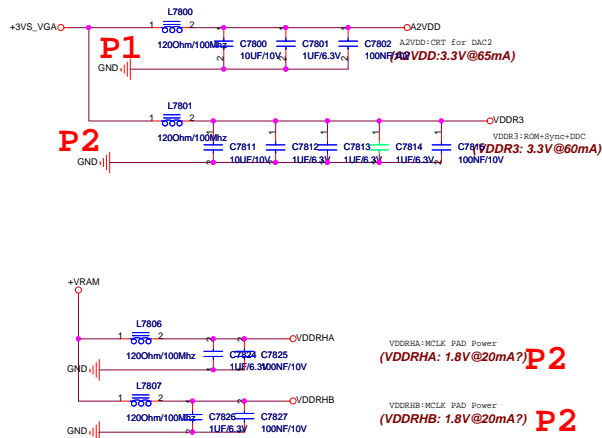
M96/M92M Straps

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT	RECOMMEND
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIe bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)	
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled MXM and add-in boards	0 (internal pull-down)	
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 ----Disable 1-----Enable	0 (internal pull-down)	
BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0	
Reserved	H2SYNC	ATI internal use only . Other logic must not affect this signal during RESET Recommended to 0	0 (internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
Reserved	GPIO_21_BB_EN GENERICC	Internal use only. INTERNALPULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0 (internal pull-down)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
VIP_DEVICE_STRAP_EN	V2SYNC	0 - Ignore VIP device straps 1 - Use VIP device straps	0 (internal pull-down)	
VGA_DIS	GPIO_9_ROMSI	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)	
BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0	
ROMIDCFG(3:0)	GPIO(9,13:11)	If BIOS_ROM_EN=1, then Config[3:0] defines the ROM type. If BIOS_ROM_EN=0, then Config[2:0] defines the primary memoru aperture size. 128MB---x000 32MB---x011 2GB---x110 256MB---x001 512MB---x100 4GB---x111 64MB---x010 1GB---x101	0000 (internal pull-down)	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00 - No audio function; 01 - Audio for DisplayPort and HDMI if adapter is detected; 10 - Audio for DisplayPort only; 11 - Audio for both DisplayPort and HDMI.	0 (internal pull-down) 0 (internal pull-down)	Design dependent.

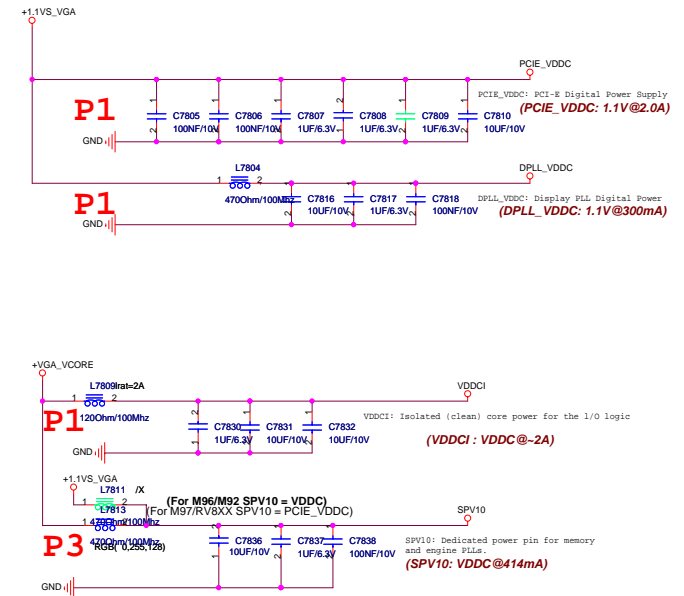
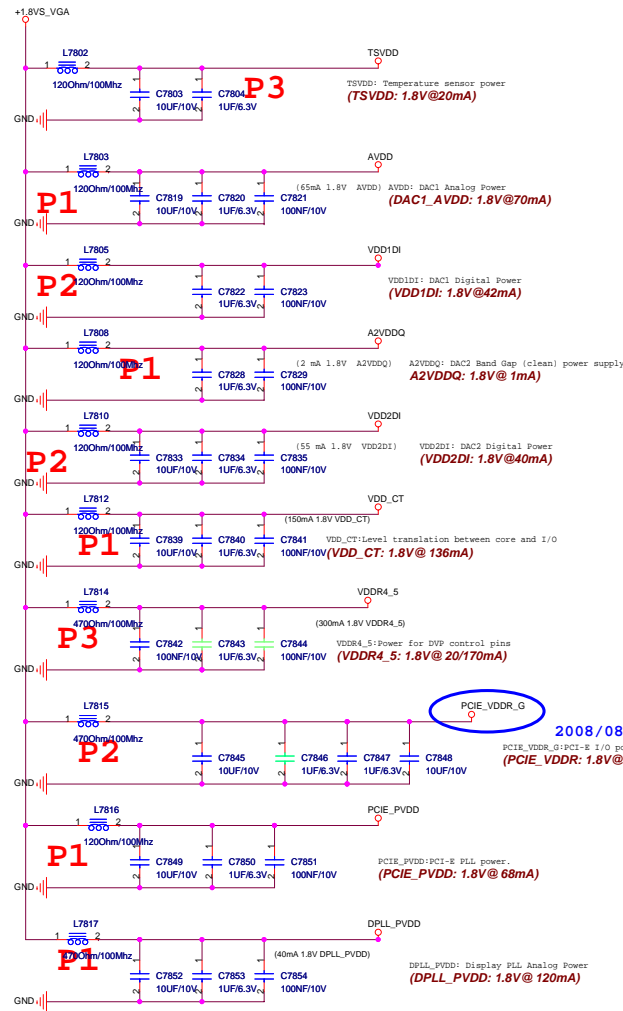
Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Infineon (Qimonda)	0000	0	32M*16 (256M)	A channel
	0001	1	32M*16 (512M)	2-AB channel
	0010	2	64M*16 (512M)	A channel
	0011	3	64M*16 (1G)	2-AB channel
	0100	4	16M*16 (128M)	A channel
Samsung	0101	5	16M*16 (256M)	2-AB channel
	0110	6	32M*16 (256M)	A channel
	0111	7	32M*16 (512M)	2-AB channel
Hynix	1000	8	32M*16 (256M)	A channel
	1001	9	32M*16 (512M)	2-AB channel
	1010	10	64M*16 (512M)	A channel
	1011	11	64M*16 (1G)	2-AB channel
	1100	12	16M*16 (128M)	A channel
	1101	13	16M*16 (256M)	2-AB channel
	1110	14		
Micron	1111	15	64M*16 (1G)	2-AB channel

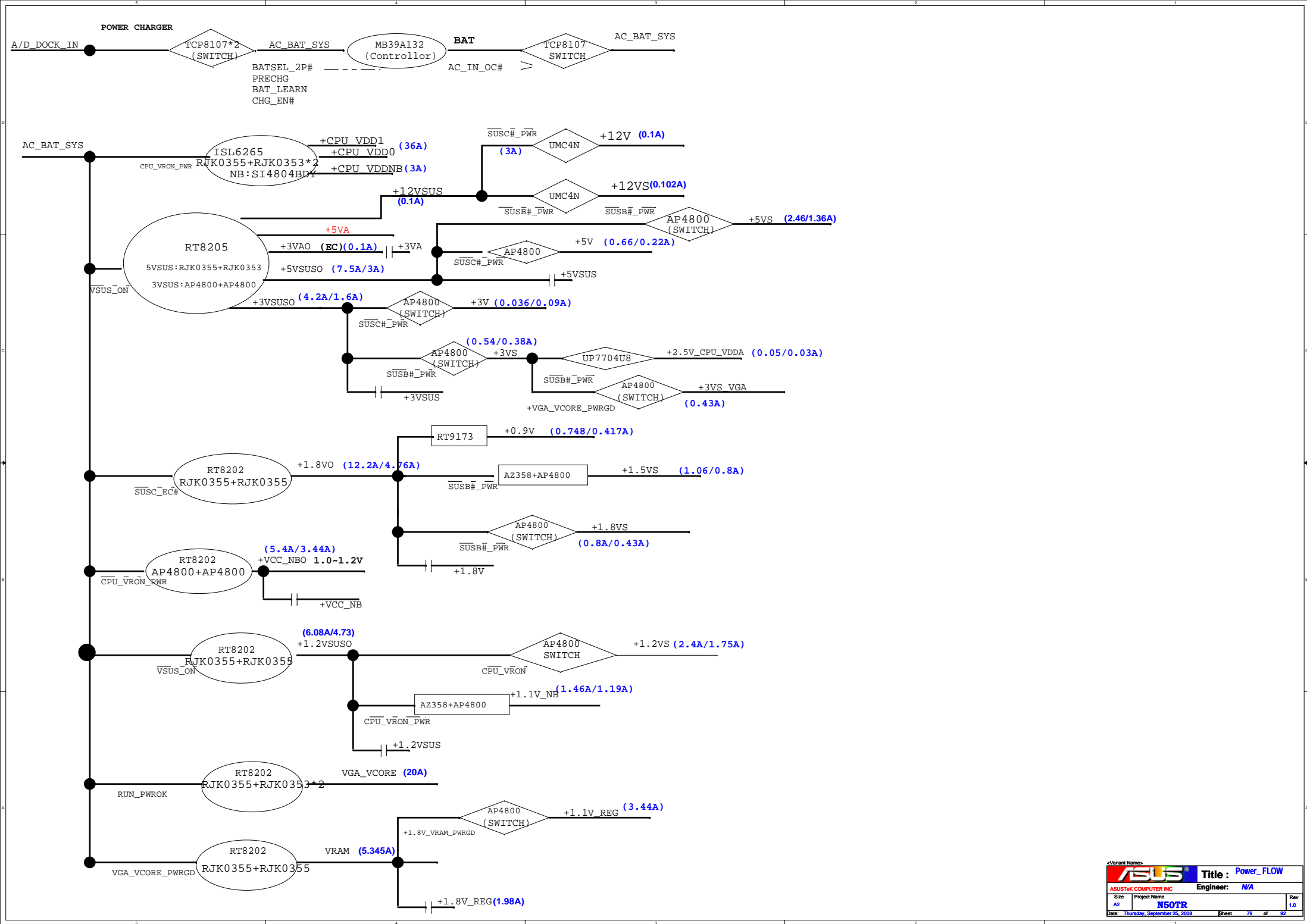


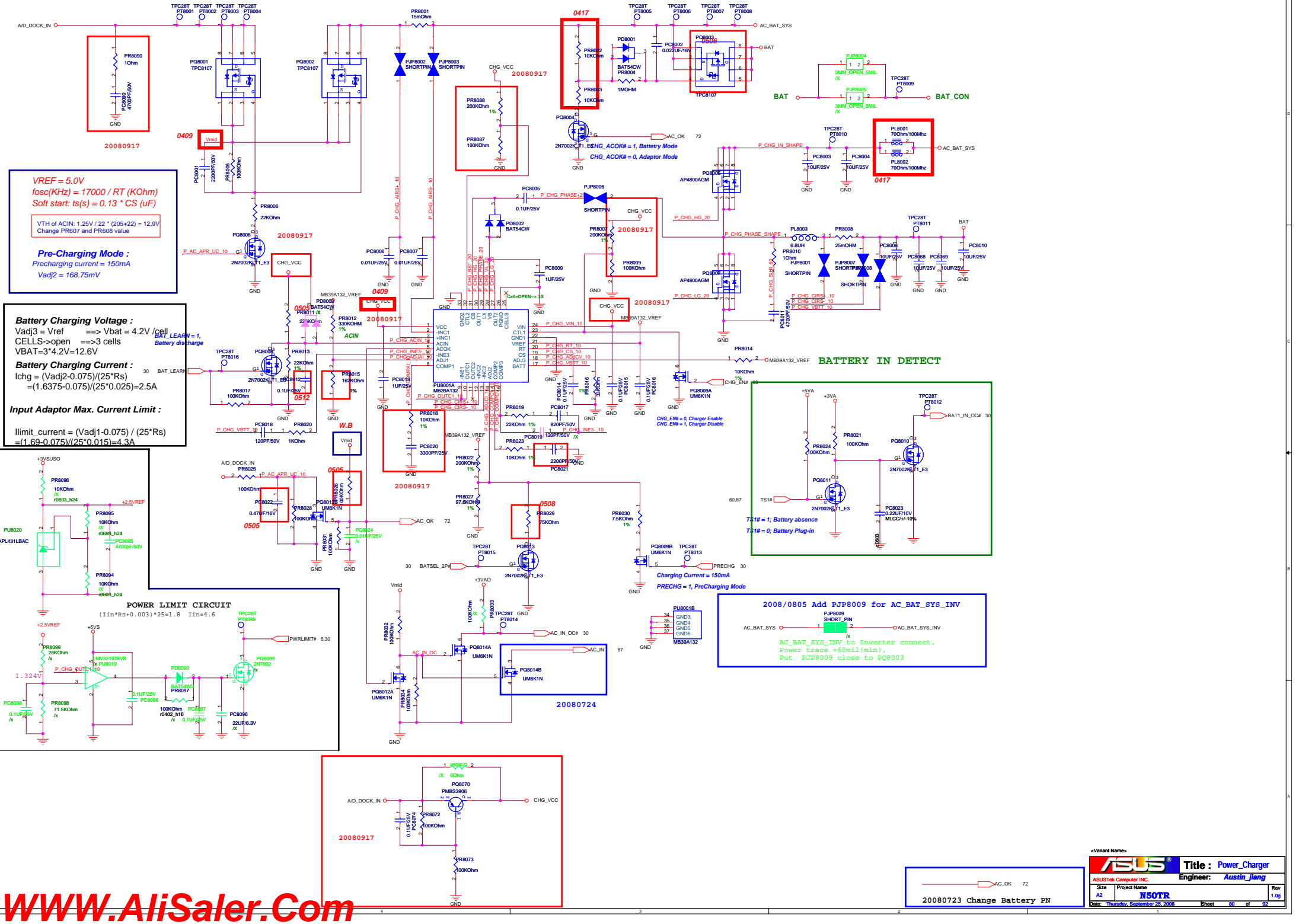


For Placement: P1 is
Priority 1, P2
Second Priority and
so on.....



2008/08/11 PCIE_VDDR Change to PCIE_VDDR_G





Design Current : 2.1A
Maximum current : 3A +CPU_VDDNB
OCP point Typ. : 6A

Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 30A

Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 30A

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	X
5V	X	X

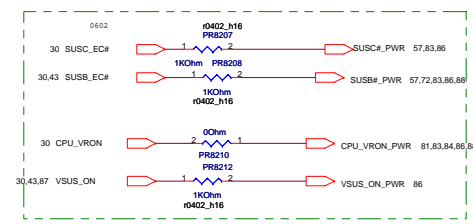
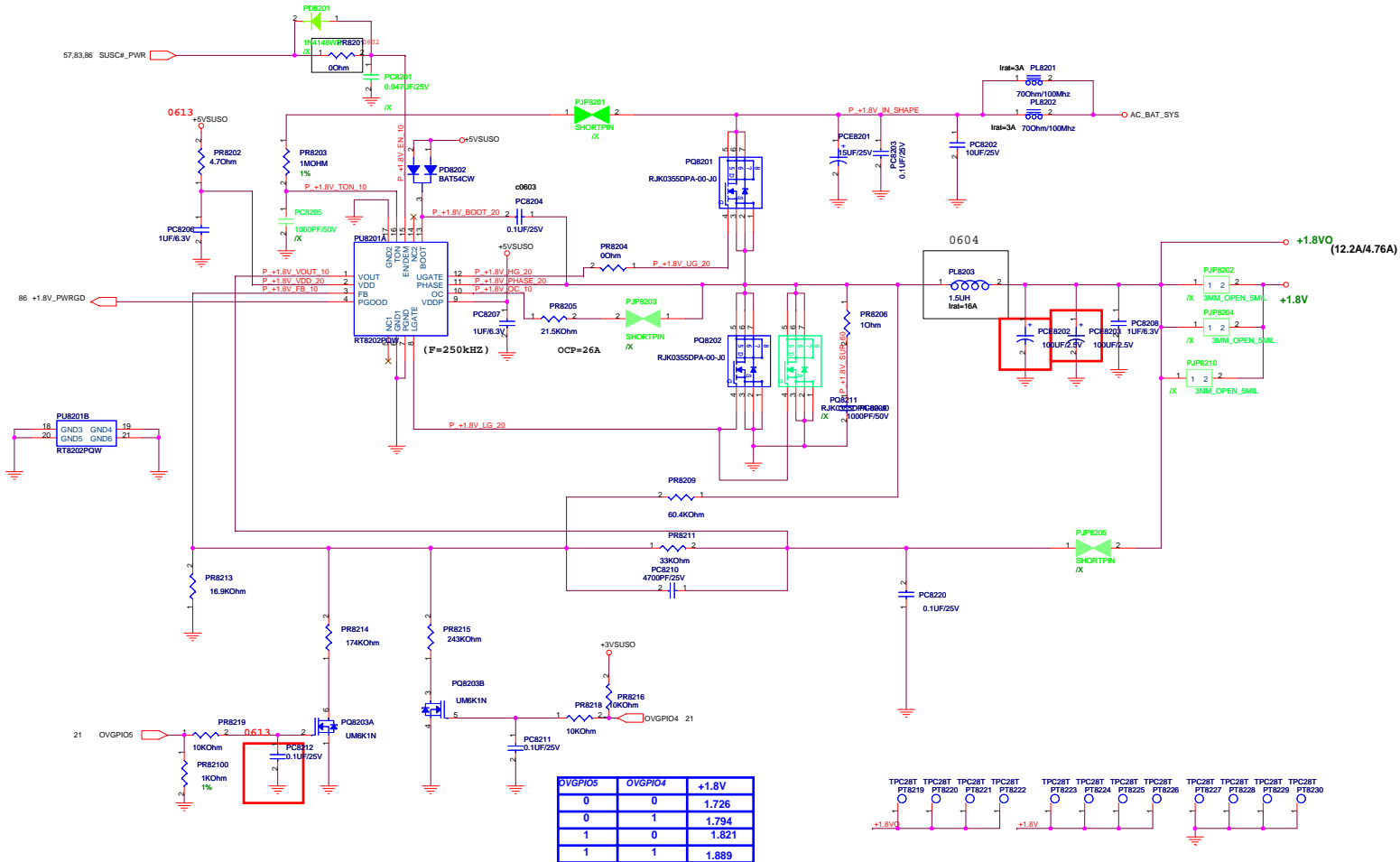
VFIXEN VID Codes

SVC	SVD	Output	Pre_metal
0	0	1.4	1.1
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.8	0.8

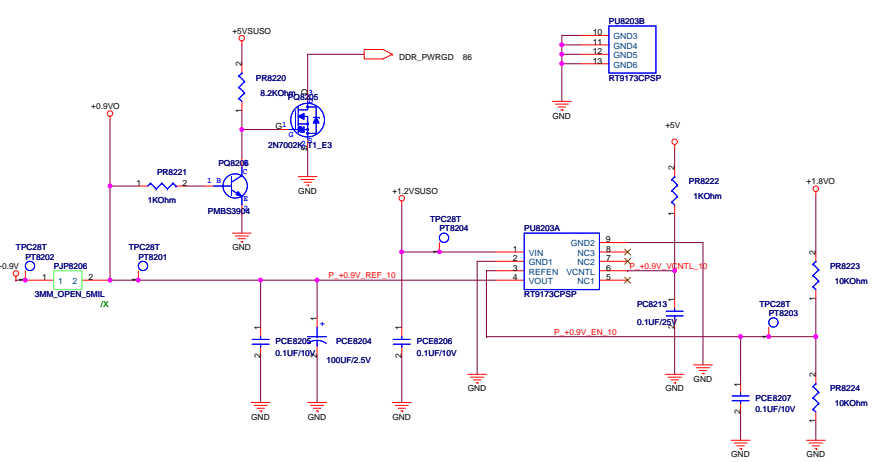
OVGPIO1	OVGPIO0	+CPU_VDD0	+CPU_VDD1
0	0	NO DEFINE	NO DEFINE
0	1	-5%	-5%
1	0	+5%	+5%
1	1	NORMAL	NORMAL

OVGPIO3	OVGPIO2	+CPU_VDDNB
0	0	NO DEFINE
0	1	-5%
1	0	+5%
1	1	NORMAL

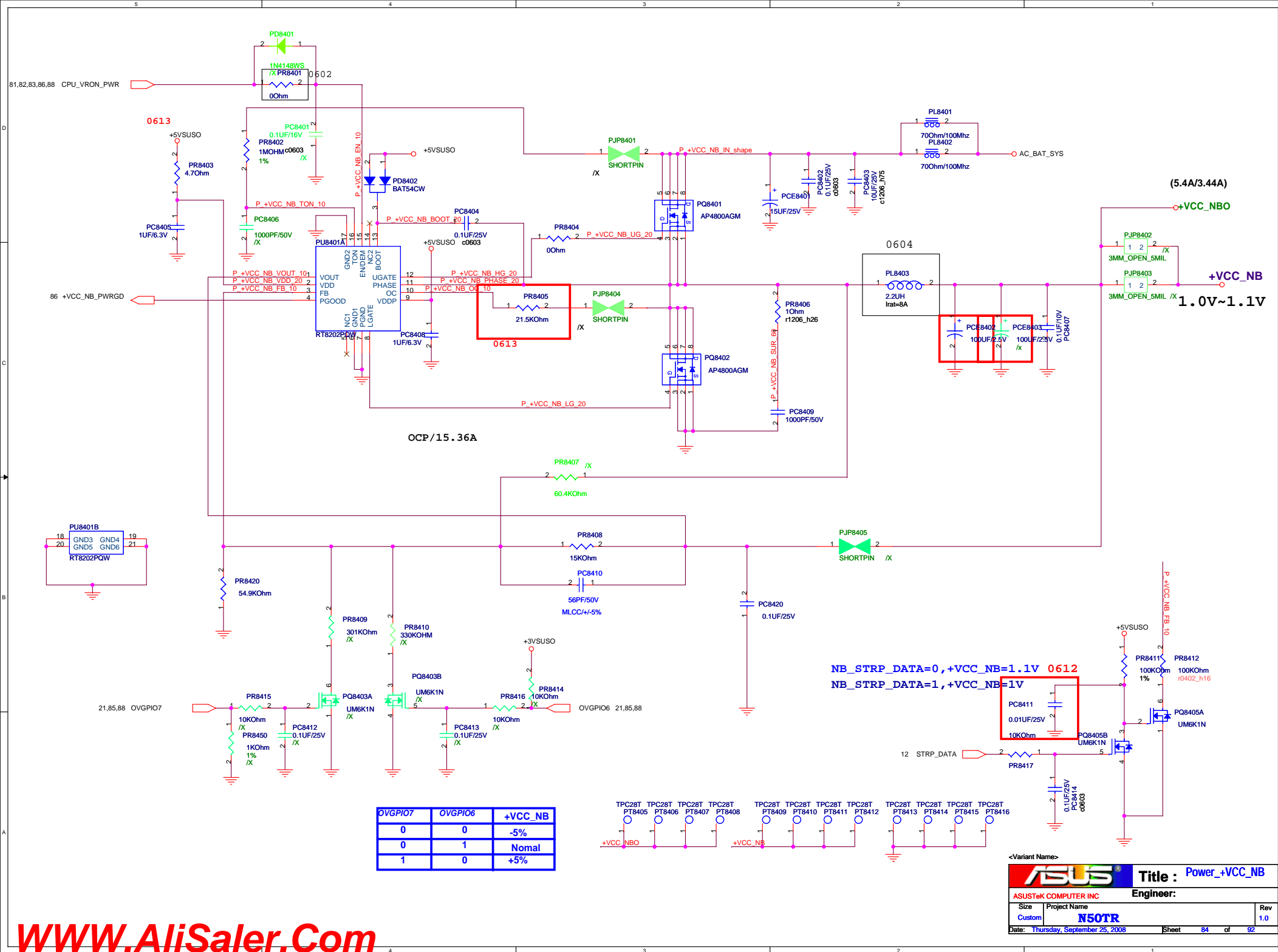
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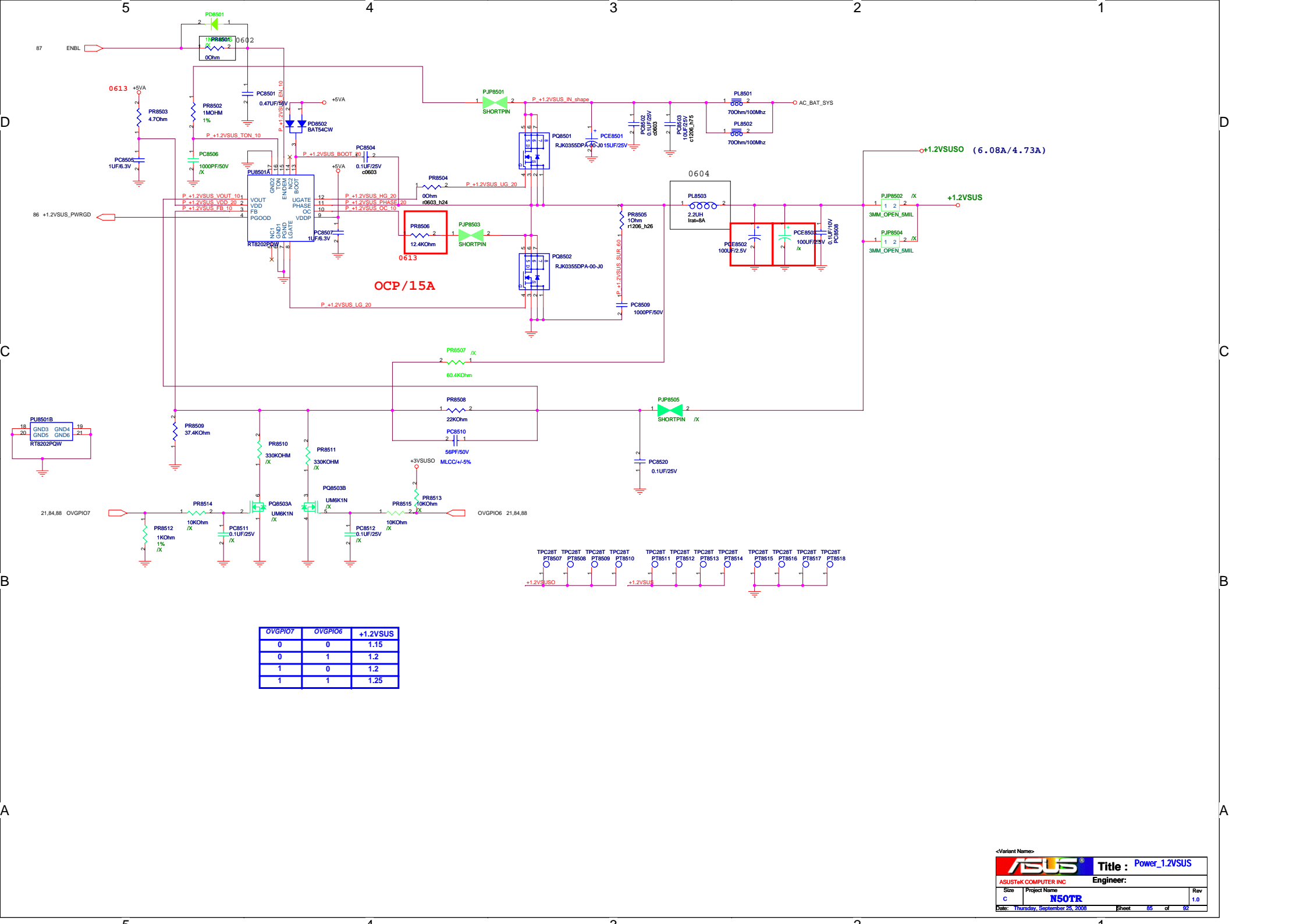


DVGPIO5	DVGPIO4	+1.8V
0	0	1.726
0	1	1.794
1	0	1.821
1	1	1.889



$R_{lim} = I_{lim} \cdot R_{sense} / 20\mu A$
 $21.5K = I_{lim} \cdot 16.5m\Omega / 20\mu A$
 $I_{lim} = 26A$

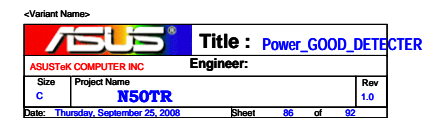


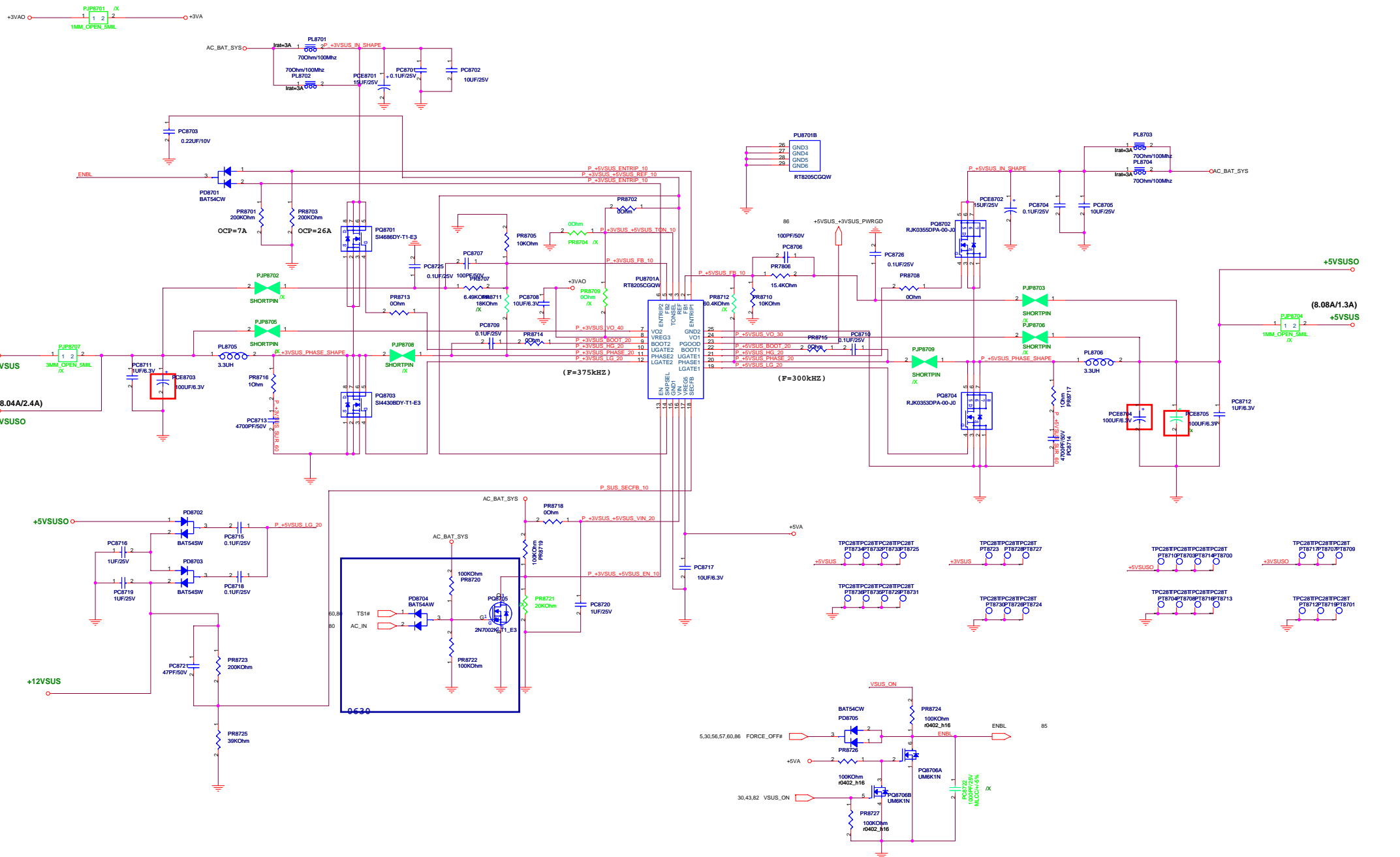


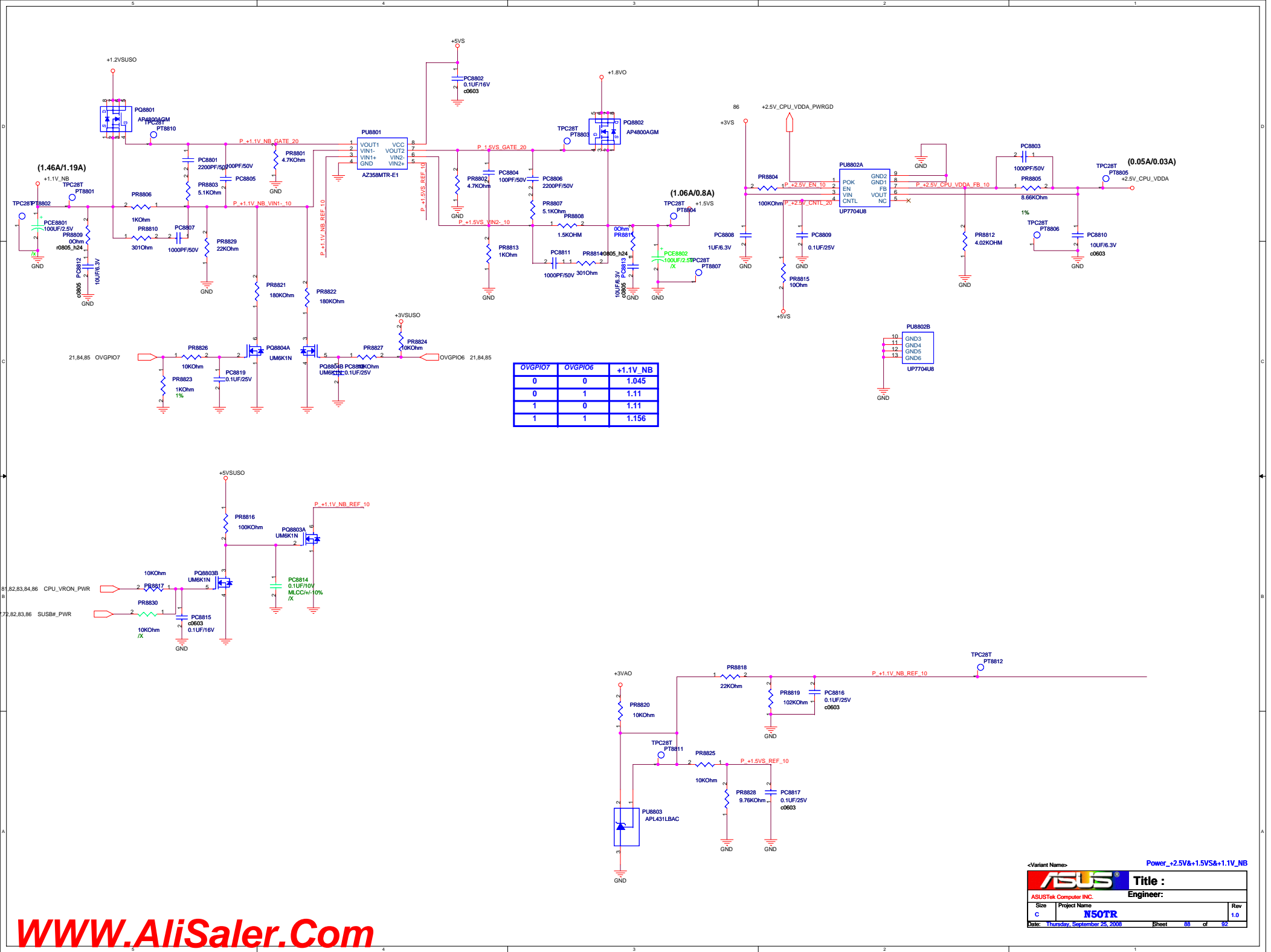
OCP/15A

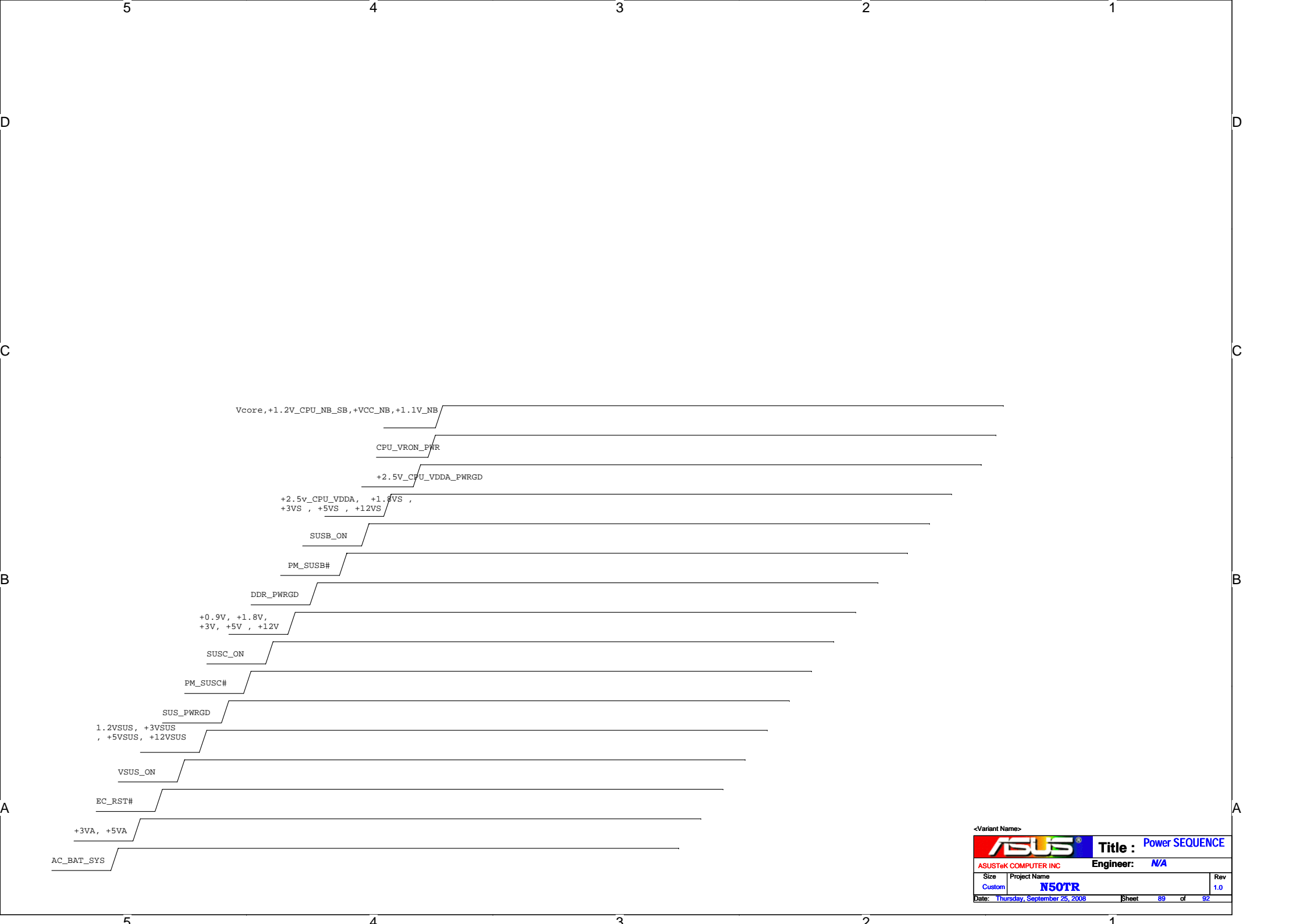
OVGPI07	OVGPI06	+1.2VSUS
0	0	1.15
0	1	1.2
1	0	1.2
1	1	1.25

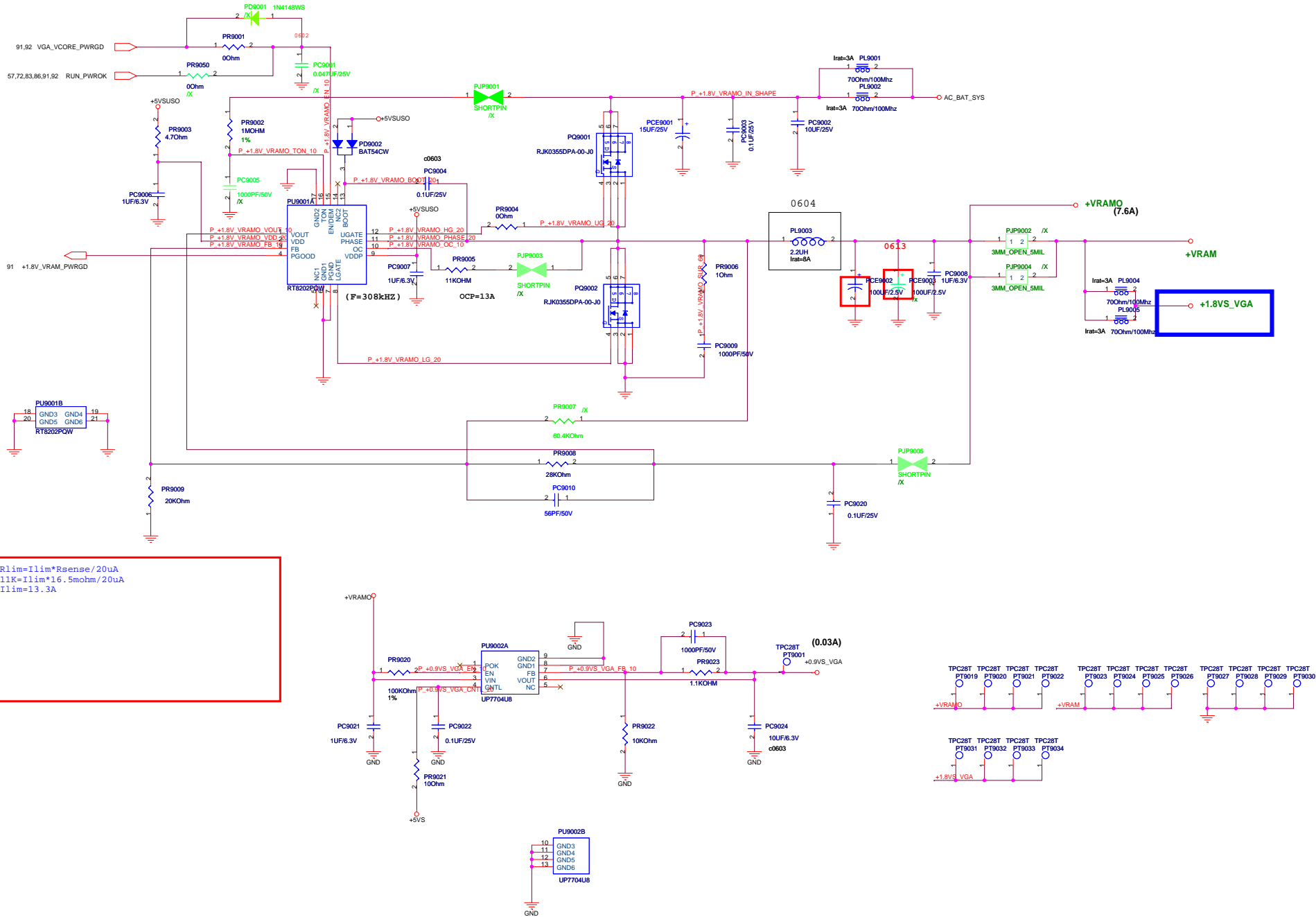
WWW.AliSaler.Com

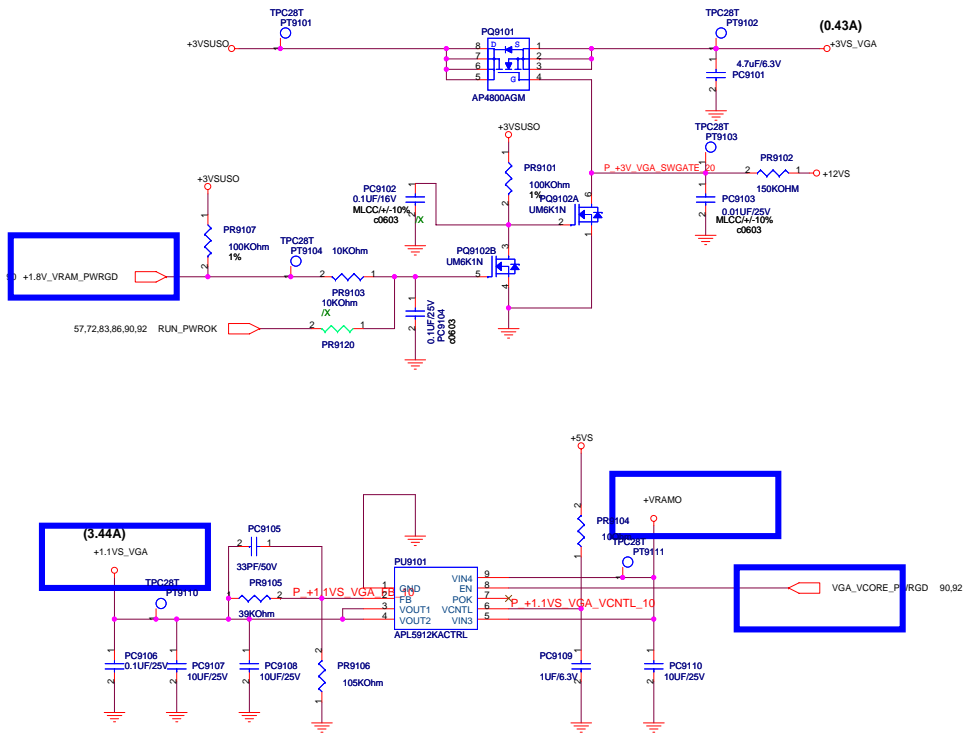












0814 ADD FOR EMI

