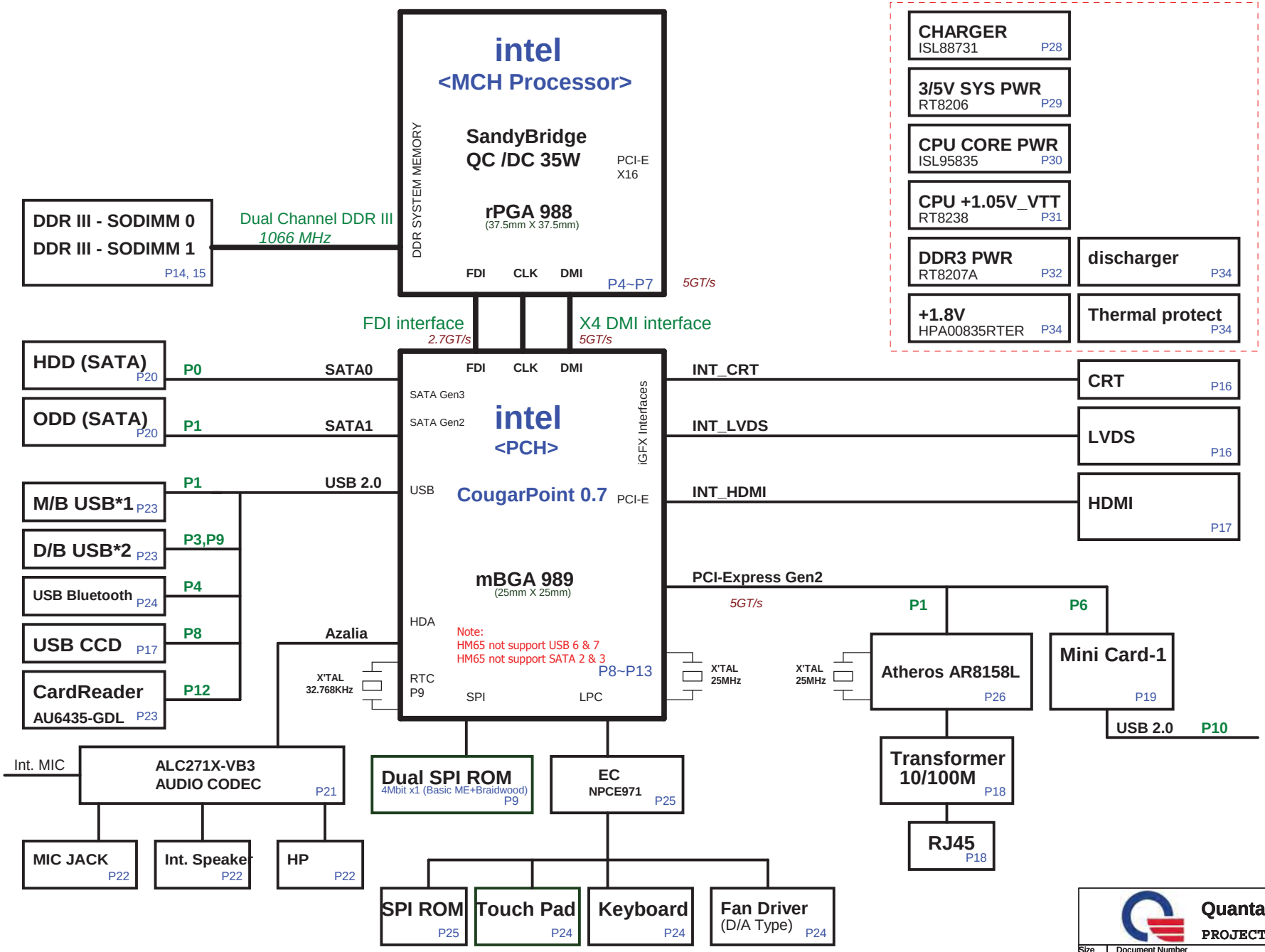
# ZQR BLOCK DIAGRAM




Quanta Computer Inc.

PROJECT : ZQR

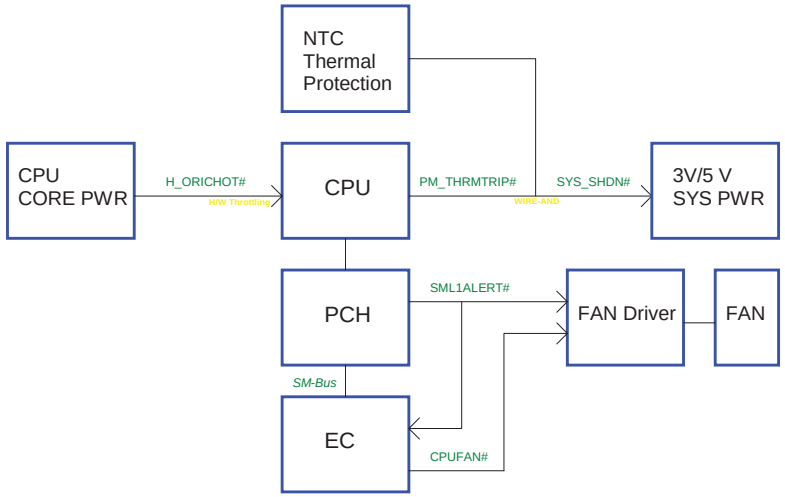
| Size | Document Number | Rev |
|---|---|---|
| | Block Diagram | 1A |

Date: Monday, May 09, 2011 Sheet 1 of 35

## Power States

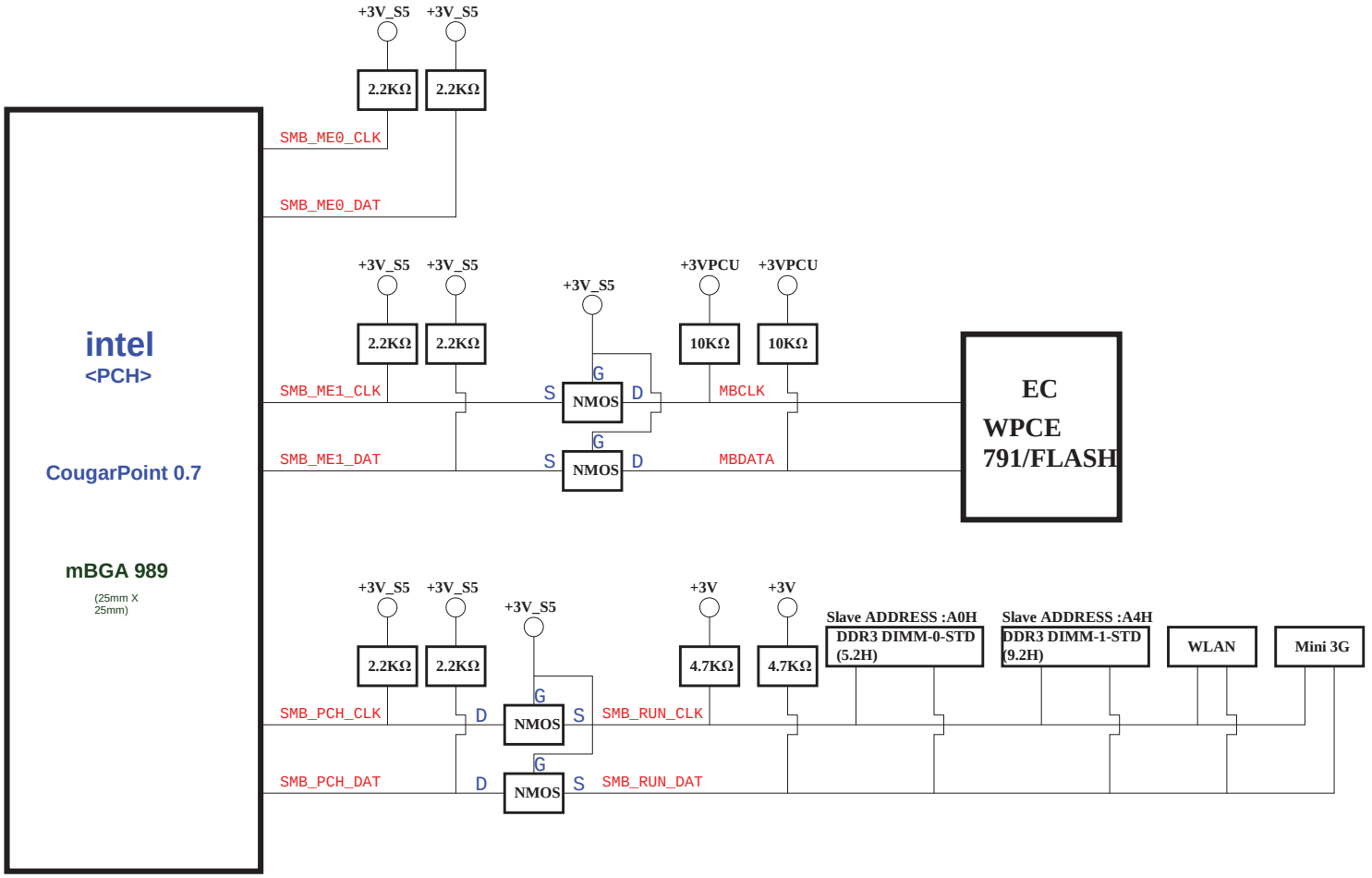
| POWER PLANE | VOLTAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|---|---|---|---|---|
| VIN | +10V~+19V | MAIN POWER | ALWAYS | ALWAYS |
| +VCCRTC | +3V~+3.3V | RTC POWER | ALWAYS | ALWAYS |
| +3VPCU | +3.3V | EC POWER | ALWAYS | ALWAYS |
| +5VPCU | +5V | CHARGE POWER | ALWAYS | ALWAYS |
| +15V | +15V | CHARGE PUMP POWER | ALWAYS | ALWAYS |
| +3V_S5 | +3.3V | LAN/BT/CIR POWER | S5_ON | S0-S5 |
| +5V_S5 | +5V | USB POWER | S5_ON | S0-S5 |
| +5V | +5V | HDD/ODD/Codec/TP/CRT/HDMI POWER | MAINON | S0 |
| +3V | +3.3V | PCH/GPU/Peripheral component POWER | MAINON | S0 |
| +1.5VSUS | +1.5V | CPU/SODIMM CORE POWER | SUSON | S0-S3 |
| +0.75V_DDR_VTT | +0.75V | SODIMM Termination POWER | MAINON | S0 |
| +VGFX_AXG | variation | Internal GPU POWER | GFX_ON | S0 |
| +1.8V | +1.8V | CPU/PCH/Braidwood POWER | MAINON | S0 |
| +1.5V | +1.5V | MINI CARD/NEW CARD POWER | MAINON | S0 |
| +1.1V_VTT | +1.05V or +1.1V | CPU VTT POWER | MAINON | S0 |
| +1.05V | +1.05V | PCH CORE POWER | MAINON | S0 |
| +VCC_CORE | variation | CPU CORE POWER | VRON | S0 |
| LCDVCC | +3.3V | LCD POWER | LVDS_VDDEN | S0 |
| +5V_GPU | +5V | SWITCHABLE PWM IC POWER | dGPU_PWR_EN# | Discrete enable |
| +GPU_CORE | +0.9V~+1.1V | GPU CORE POWER | +3V_D | Discrete enable |
| +GPU_IO | +0.9V~+1.1V | GPU I/O POWER | PG_GPUIO_EN | Discrete enable |
| +1.5V_GPU | +1.5V | VRAM CORE POWER | PG_1.5V_EN | Discrete enable |
| +1.8V_GPU | +1.8V | GPU_CRE/LVDS/PLL POWER | +1.5V_GPU | Discrete enable |
| +1V | +1V | DP/PEG POWER | PG_1V_EN | Discrete enable |

## Thermal Follow Chart






Quanta Computer Inc.
PROJECT : ZQR
Size | Document Number: PWR Status & GPU PWR CRL & THRM | Rev 1A
Date: Monday, May 09, 2011 | Sheet 2 of 35



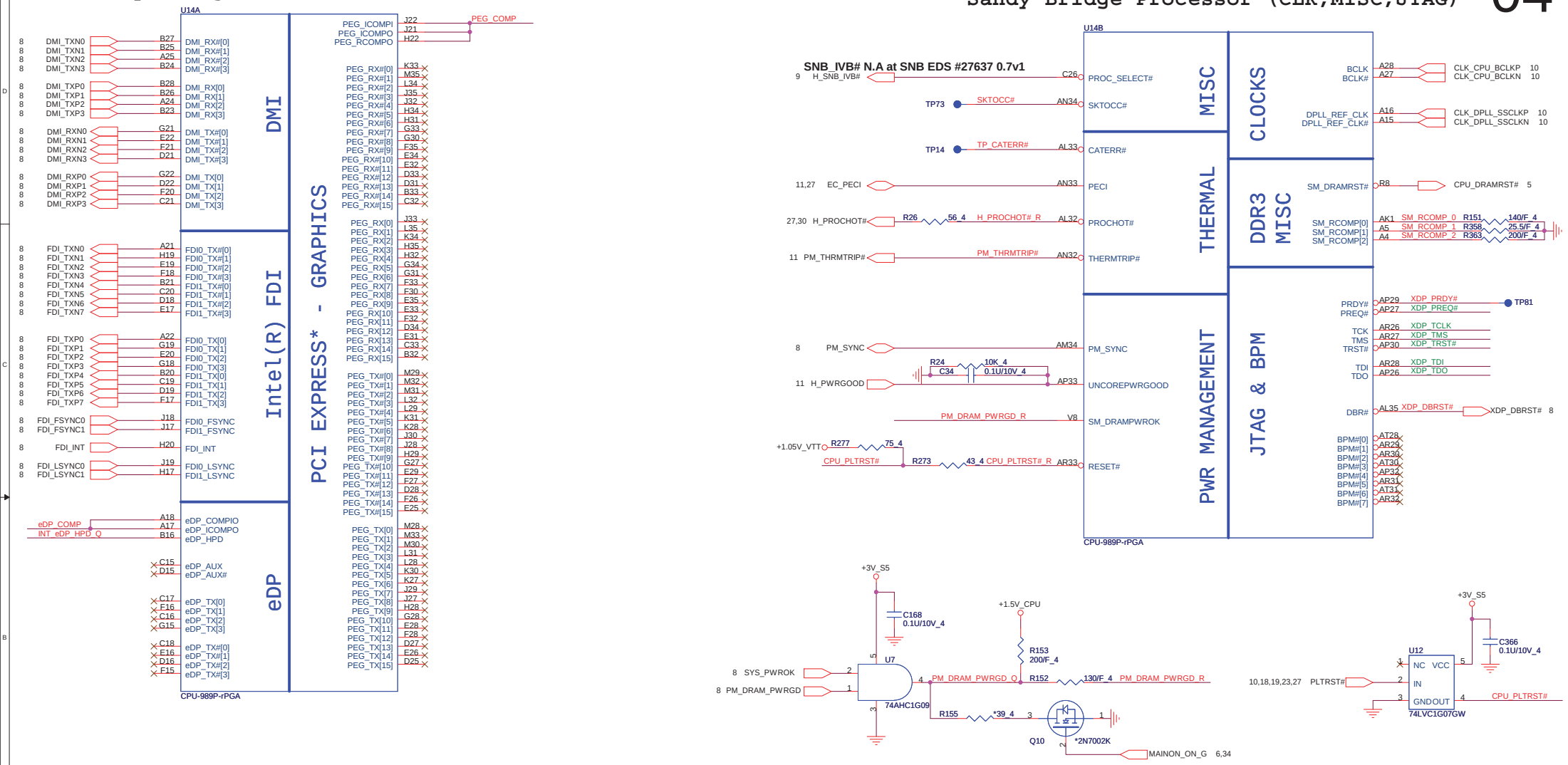

Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | SMBus Address | 1A |
| Date: Monday, May 09, 2011 | Sheet 3 of 35 | |

# Sandy Bridge Processor (DMI,PEG,FDI)

# Sandy Bridge Processor (CLK,MISC,JTAG)

04




## DP & PEG Compensation

+1.05V_VTT — R300 24.9/F_4 — eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V_VTT — R70 24.9/F_4 — PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

## Processor pull-up(CPU)

+1.05V_VTT

| | | |
|---|---|---|
| H_PROCHOT# | R39 | 62_4 |
| XDP_TDO | R57 | 51_4 |
| XDP_TMS | R285 | 51_4 |
| XDP_TDI | R283 | 51_4 |
| XDP_PREQ# | R55 | *51_4 |
| XDP_TCLK | R286 | 51_4 |
| XDP_TRST# | R56 | 51_4 |

## eDP Hot-plug

HPD disable

+1.05V_VTT — R306 10K_4 — INT_eDP_HPD_Q

Quanta Computer Inc.

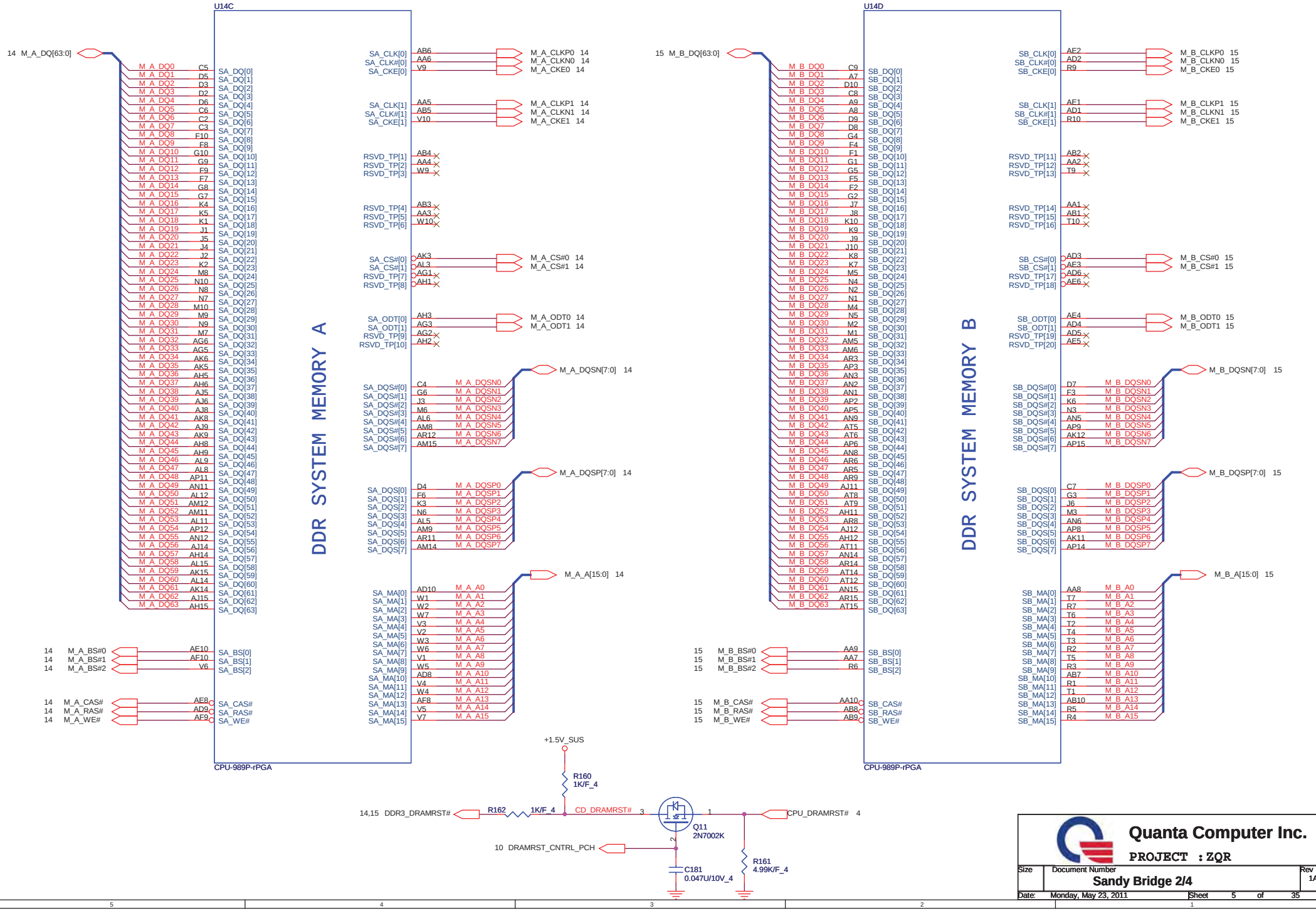
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | Sandy Bridge 1/4 | 1A |

Date: Monday, May 23, 2011 Sheet 4 of 35

# Sandy Bridge Processor (DDR3)

05




| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : ZQR | | | |
| Size | Document Number | | Rev |
| | Sandy Bridge 2/4 | | 1A |
| Date: Monday, May 23, 2011 | | Sheet 5 of 35 | |

# Sandy Bridge Processor (POWER)

# Sandy Bridge Processor (GRAPHIC POWER)

06

## CPU Core Power

SNB 45W:52A

Spec

470uF/4mohm x 4

22uF x 16

10uF x 10

## CPU VTT

SNB 45W:8.5A

Spec

330uF/6mohm x 2

22uF x 12

22uF x 7 (Non-stuff)

## CPU VGT

SNB 45W:21.5A

Spec

470uF/4mohm x 2

22uF x 12

## CPU VCCPL

SNB 45W:1.5A

Spec

330uF/7mohm x 1

10uF x 1

1uF x 2

## CPU MCH

SNB 45W: 5A

Spec

330uF/6mohm x 1

10uF x 6

Real

10uF x 6

## CPU SA

SNB 45W: 6A

Spec

330uF/7mohm x 1

10uF x 3

U14F

POWER

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

U14G

POWER

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

CPU-989P-rPGA

B23 Mount C70, C71 for +Vcc_core overshoot issue. 5/18

B45 Remove C315 for cost issue. 5/19

B54 Del C442. 5/20

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

SVID DATA

SVID ALERT

Place PU resistor close to CPU

4.5A

Q8 *AO4496

Q9 *DMN601K-7

Q17 *2N7002E



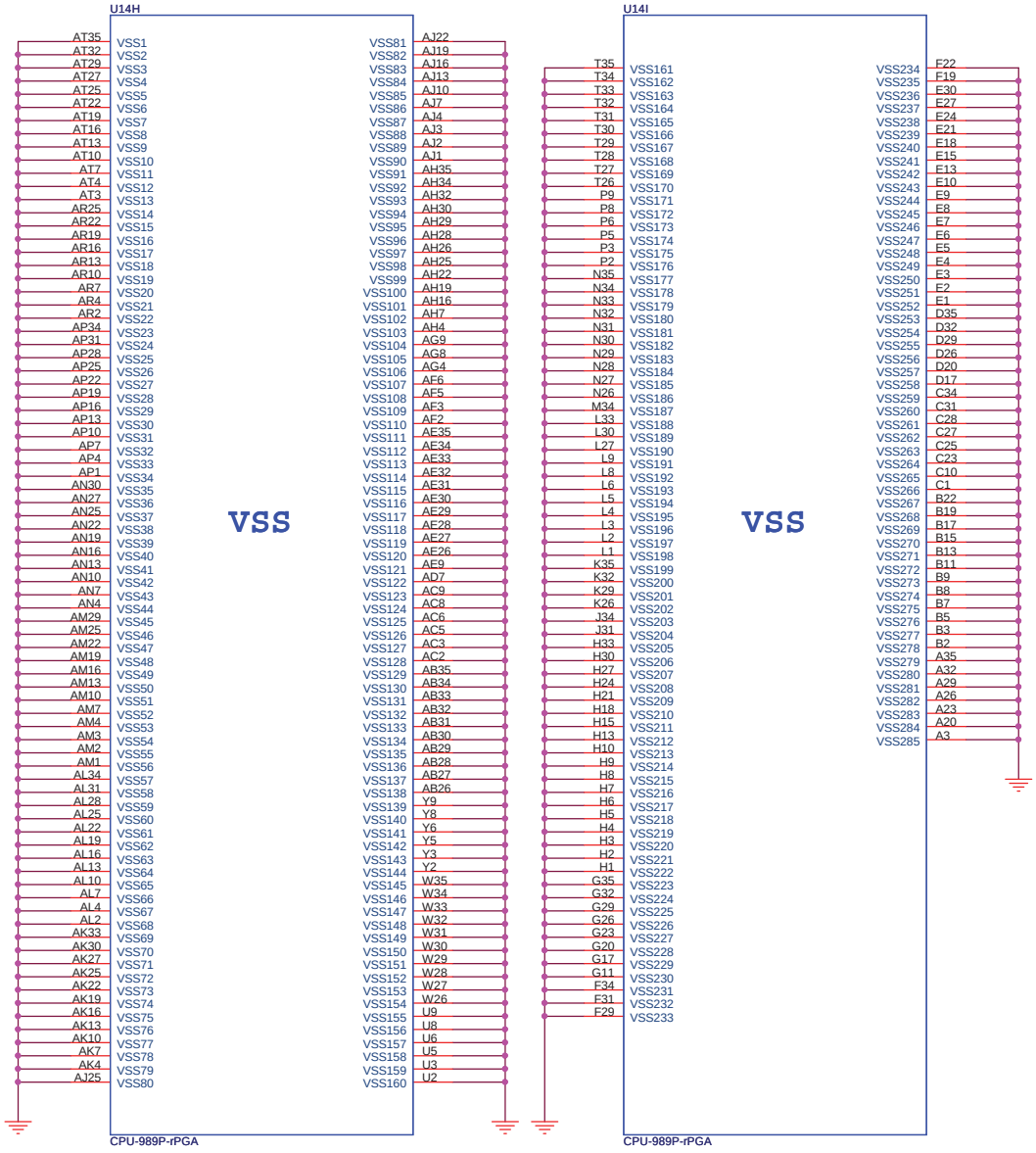
Quanta Computer Inc.

PROJECT : ZQR

Size | Document Number: Sandy Bridge 3/4 | Rev 1A

Date: Monday, May 23, 2011 | Sheet 6 of 35

# Sandy Bridge Processor (GND)



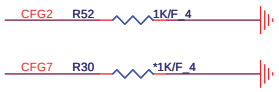

# Sandy Bridge Processor (RESERVED, CFG)

07


## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |




CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.

PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | Sandy Bridge 4/4 | 1A |
| Date: Monday, May 09, 2011 | Sheet 7 of 35 | |

# Cougar Point (DMI,FDI,PM)

U13C

DMI_RXN0 BC24 DMI0RXN
DMI_RXN1 BE20 DMI1RXN
DMI_RXN2 BG18 DMI2RXN
DMI_RXN3 BG20 DMI3RXN
DMI_RXP0 BE24 DMI0RXP
DMI_RXP1 BC20 DMI1RXP
DMI_RXP2 BJ18 DMI2RXP
DMI_RXP3 BJ20 DMI3RXP
DMI_TXN0 AW24 DMI0TXN
DMI_TXN1 AW20 DMI1TXN
DMI_TXN2 BB18 DMI2TXN
DMI_TXN3 AV18 DMI3TXN
DMI_TXP0 AY24 DMI0TXP
DMI_TXP1 AY20 DMI1TXP
DMI_TXP2 AY18 DMI2TXP
DMI_TXP3 AU18 DMI3TXP

DMI

+1.05V_VTT R302 49.9/F_4 DMI_COMP BJ24 DMI_ZCOMP
R307 750/F_4 DMI2RBIAS BG25 DMI_IRCOMP
BH21 DMI2RBIAS

FDI_RXN0 BJ14 FDI_TXN0
FDI_RXN1 AY14 FDI_TXN1
FDI_RXN2 BE14 FDI_TXN2
FDI_RXN3 BH13 FDI_TXN3
FDI_RXN4 BC12 FDI_TXN4
FDI_RXN5 BJ12 FDI_TXN5
FDI_RXN6 BG10 FDI_TXN6
FDI_RXN7 BG9 FDI_TXN7
FDI_RXP0 BG14 FDI_TXP0
FDI_RXP1 BB14 FDI_TXP1
FDI_RXP2 BF14 FDI_TXP2
FDI_RXP3 BG13 FDI_TXP3
FDI_RXP4 BE12 FDI_TXP4
FDI_RXP5 BG12 FDI_TXP5
FDI_RXP6 BJ10 FDI_TXP6
FDI_RXP7 BH9 FDI_TXP7

FDI

FDI_INT AW16 FDI_INT
FDI_FSYNC0 AV12 FDI_FSYNC0
FDI_FSYNC1 BC10 FDI_FSYNC1
FDI_LSYNC0 AV14 FDI_LSYNC0
FDI_LSYNC1 BB10 FDI_LSYNC1

System Power Management

DSWVRMEN A18 DSWVREN
SUS_PWR_ACK C12 SUSACK#
DPWROK E22 ICH_RSMRST#
4 XDP_DBRST# XDP_DBRST# K3 SYS_RESET# WAKE# B9 PCIE_WAKE# PCIE_WAKE# 18,19
SYS_PWROK P12 SYS_PWROK
+3V CLKRUN# / GPIO32 N3 CLKRUN# CLKRUN# 27
27 PWROK_EC PWROK_EC L22 PWROK
+3V_S5 SUS_STAT# / GPIO61 G8 SUS_STAT# TP43
L10 APWROK
+3V_S5 SUSCLK / GPIO62 N14 PCH_SUSCLK 27
4 PM_DRAM_PWRGD PM_DRAM_PWRGD B13 DRAMPWROK
+3V_S5 SLP_S5# / GPIO63 D10 TP34
27 ICH_RSMRST# ICH_RSMRST# C21 RSMRST#
SLP_S4# H4 SUSC# 27
SUS_PWR_ACK K16 SUSWARN#/SUSPWRDNACK/GPIO30
+3V_S5 SLP_S3# F4 SUSB# 27
27 DNBSWON# E20 PWRBTN#
G10 SLP_A# TP38
AC_PRESENT H20 ACPRESENT / GPIO31
DSW SLP_SUS# G16 TP33
PM_BATLOW# E10 BATLOW# / GPIO72
+3V_S5 PMSYNCH AP14 PM_SYNC 4
PM_RI# A10 RI#
+3V_S5 SLP_LAN# / GPIO29 K14 SLP_LAN#

CougarPoint_R1P0

SYNC RS
33ohm for Direct Connect
20ohm for Dock Support
20ohm for Switchable Graphics Device Down Topology
10ohm for Switchable Graphics Dock Support

# Cougar Point (LVDS,DDI)

+3V R10 2.2K_4 INT_LVDS_EDIDCLK R12 2.2K_4 INT_LVDS_EDIDDATA

U13D

16 INT_LVDS_BLON J47 L_BKLTEN
16 INT_LVDS_DIGON M45 L_VDD_EN
16 INT_LVDS_BRIGHT P45 L_BKLTCTL
16 INT_LVDS_EDIDCLK INT_LVDS_EDIDCLK T40 L_DDC_CLK
16 INT_LVDS_EDIDDATA INT_LVDS_EDIDDATA K47 L_DDC_DATA
+3V R33 2.2K_4 T45 L_CTRL_CLK
R32 2.2K_4 P39 L_CTRL_DATA
R51 2.37K/F_4 AE37 LVD_IBG
TP20 AF36 LVD_VBG
AE48 LVD_VREFH
AE47 LVD_VREFL

LVDS

16 INT_TXLCLKOUTN INT_TXLCLKOUTN AK39 LVDSA_CLK#
16 INT_TXLCLKOUTP INT_TXLCLKOUTP AK40 LVDSA_CLK
16 INT_TXLOUTN0 INT_TXLOUTN0 AN48 LVDSA_DATA#0
16 INT_TXLOUTN1 INT_TXLOUTN1 AM47 LVDSA_DATA#1
16 INT_TXLOUTN2 INT_TXLOUTN2 AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
16 INT_TXLOUTP0 INT_TXLOUTP0 AN47 LVDSA_DATA0
16 INT_TXLOUTP1 INT_TXLOUTP1 AM49 LVDSA_DATA1
16 INT_TXLOUTP2 INT_TXLOUTP2 AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3

R place close to PCH
R259 150/F_4 INT_CRT_BLU
R258 150/F_4 INT_CRT_GRE
R257 150/F_4 INT_CRT_RED

AF40 LVDSB_CLK#
AF39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

+3V R34 2.7K_4 INT_CRT_DDCCLK R35 2.7K_4 INT_CRT_DDCDAT

CRT

16 INT_CRT_BLU INT_CRT_BLU N48 CRT_BLUE
16 INT_CRT_GRE INT_CRT_GRE P49 CRT_GREEN
16 INT_CRT_RED INT_CRT_RED T49 CRT_RED
16 INT_CRT_DDCCLK INT_CRT_DDCCLK T39 CRT_DDC_CLK
16 INT_CRT_DDCDAT INT_CRT_DDCDAT M40 CRT_DDC_DATA
16 INT_CRT_HSYNC R261 33_4 INT_CRT_HSYNC_R M47 CRT_HSYNC
16 INT_CRT_VSYNC R260 33_4 INT_CRT_VSYNC_R M49 CRT_VSYNC
DAC_IREF T43 DAC_IREF
T42 CRT_IRTN
R53 1K/F_4

CougarPoint_R1P0

Digital Display Interface

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 INT_HDMI_SCL 17
SDVO_CTRLDATA M39 INT_HDMI_SDA 17

INT. HDMI

DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 INT_HDMI_HPD 17
DDPB_0N AV42 INT_HDMI_TXDN2 17
DDPB_0P AV40 INT_HDMI_TXDP2 17
DDPB_1N AV45 INT_HDMI_TXDN1 17
DDPB_1P AV46 INT_HDMI_TXDP1 17
DDPB_2N AU48 INT_HDMI_TXDN0 17
DDPB_2P AU47 INT_HDMI_TXDP0 17
DDPB_3N AV47 INT_HDMI_TXCN 17
DDPB_3P AV49 INT_HDMI_TXCP 17

DDPC_CTRLCLK P46
DDPC_CTRLDATA P42

INT. DP

DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38 DDPC_HPD_PU
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA49
DDPC_3N BB47
DDPC_3P BB49

DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41 DDPD_HPD_PU
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF43
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

+3V
DDPC_HPD_PU R48 10K_4
DDPD_HPD_PU R287 10K_4

Follow PDG eDP disable guide

## PCH Pull-high/low(CLG)

+3V
CLKRUN# R350 8.2K_4
XDP_DBRST# R353 10K_4
R337 *1K_4
ICH_RSMRST# R303 10K_4
SYS_PWROK R111 10K_4

+3V_S5
PM_RI# R326 10K_4
PM_BATLOW# R105 8.2K_4
PCIE_WAKE# R329 10K_4
SLP_LAN# R91 *10K_4
SUS_PWR_ACK R324 10K_4
AC_PRESENT R83 10K_4
PM_DRAM_PWRGD R319 200/F_4

## System PWR_OK(CLG)

+3V_S5 C150 *0.1U/10V_4
U6 TC7SH08
4 SYS_PWROK SYS_PWROK 4
IMVP_PWRGD_R
PWROK_EC
R145 100K_4

R409 0_4
C142 *2.2U/6.3V_4
U5 *TC7SH08
IMVP_PWRGD 4,30
GFX_PWRGD 30

B05 Use R409 to exchange U5, C142 for saving cost 05/17

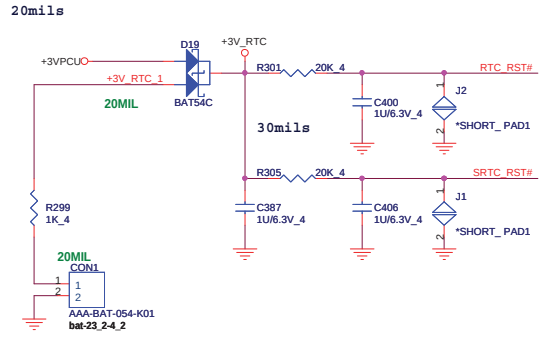
+3V_RTC
R309 330K_4
DSWVREN
R310 *330K_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

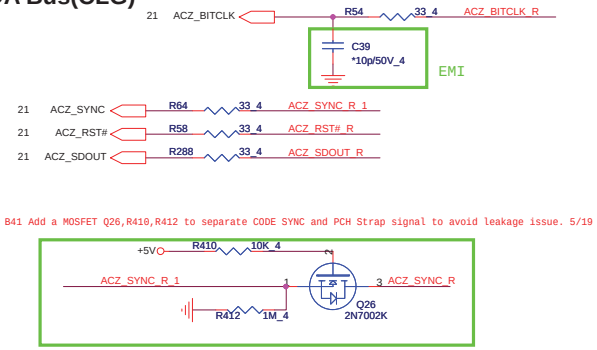
Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 1/6 | 1A |
| Date: Monday, May 23, 2011 | Sheet 8 of 35 | |

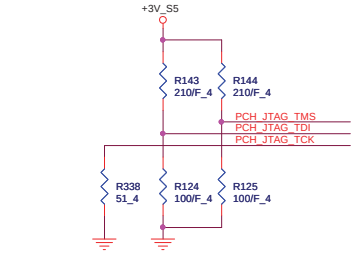
## RTC Circuitry(RTC)




## HDA Bus(CLG)

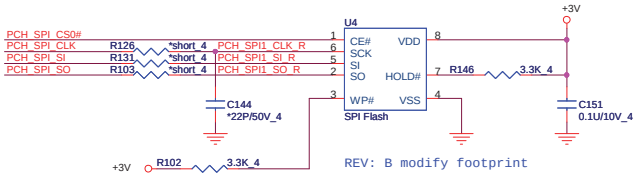



## PCH JTAG Debug (CLG)




## PCH Dual SPI (CLG)

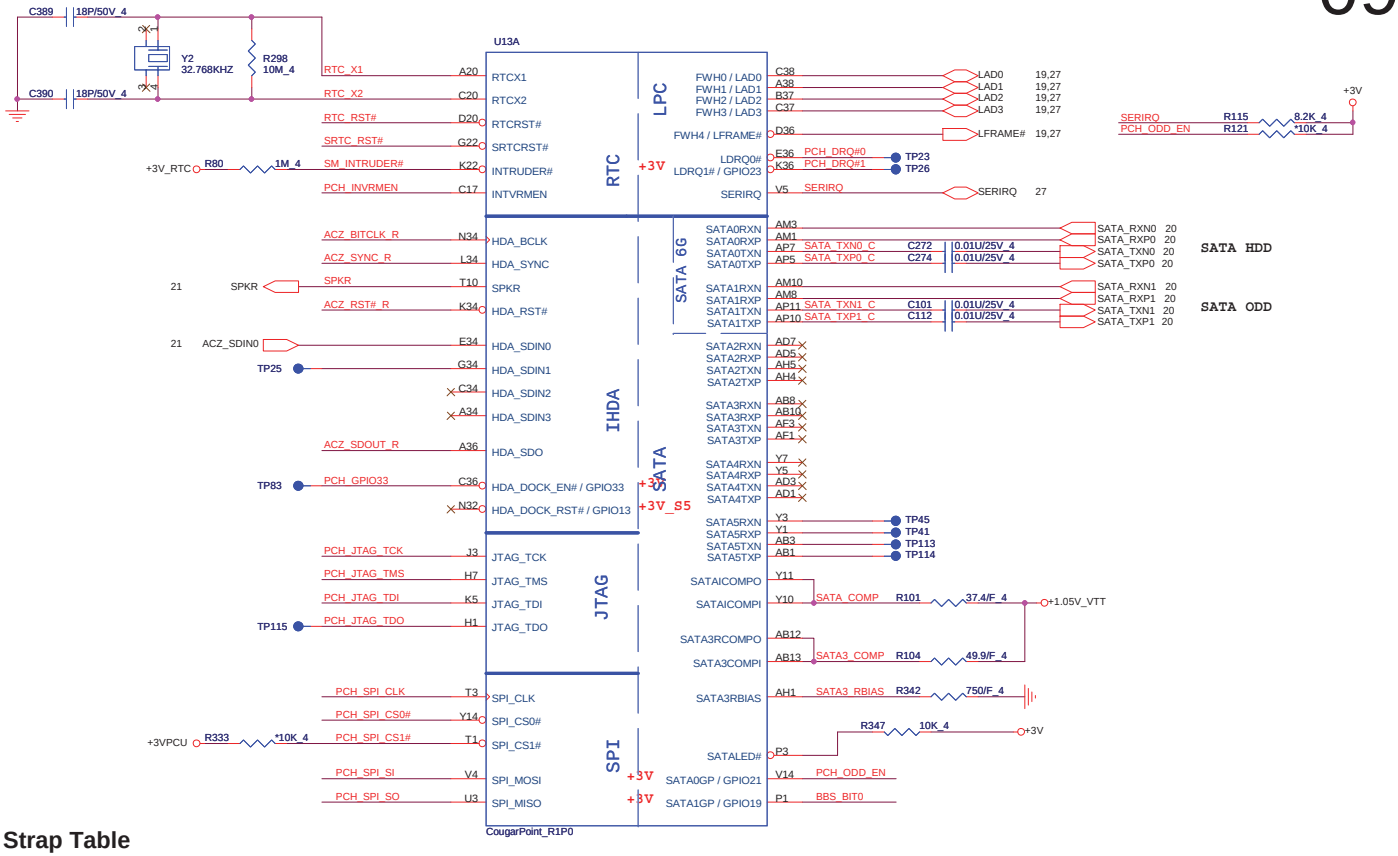
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00




## PCH2 (CLG)

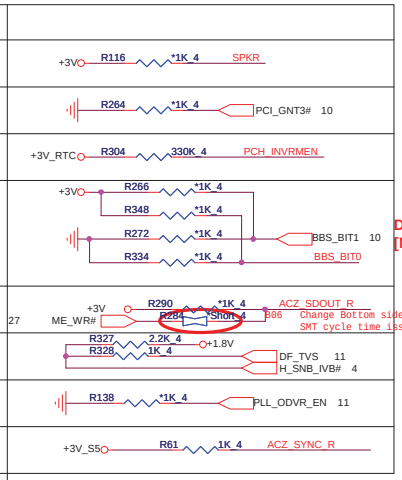
# Cougar Point (HDA,JTAG,SATA)

09




## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration |
|---|---|---|---|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# / GNT0# / Boot Location<br>1 / 1 / SPI *<br>0 / 0 / LPC |
| GPIO19 | Boot BIOS Selection 0 [bit-0] | PWROK | |
| HDA_SDO | Flash Descriptor Security | RSMRST | 0 = Override<br>1 = Default (weak pull-up 20K) |
| DF_TVS | DMI/FDI Termination voltage | PWROK | 0 = Set to Vss<br>1 = Set to Vcc (weak pull-down 20K) |
| GPIO28 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V |
| GPIO8 | Integrated Clock Chip Enable | RSMRST# | Should be pull-down<br>(weak pull-up 20K) |
| SPI_MOSI | iTPM function Disable | APWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable |
| NV_ALE | Intel Anti-Theft HDD protection | PWROK | 0 = Disable (Internal pull-down 20kohm) |

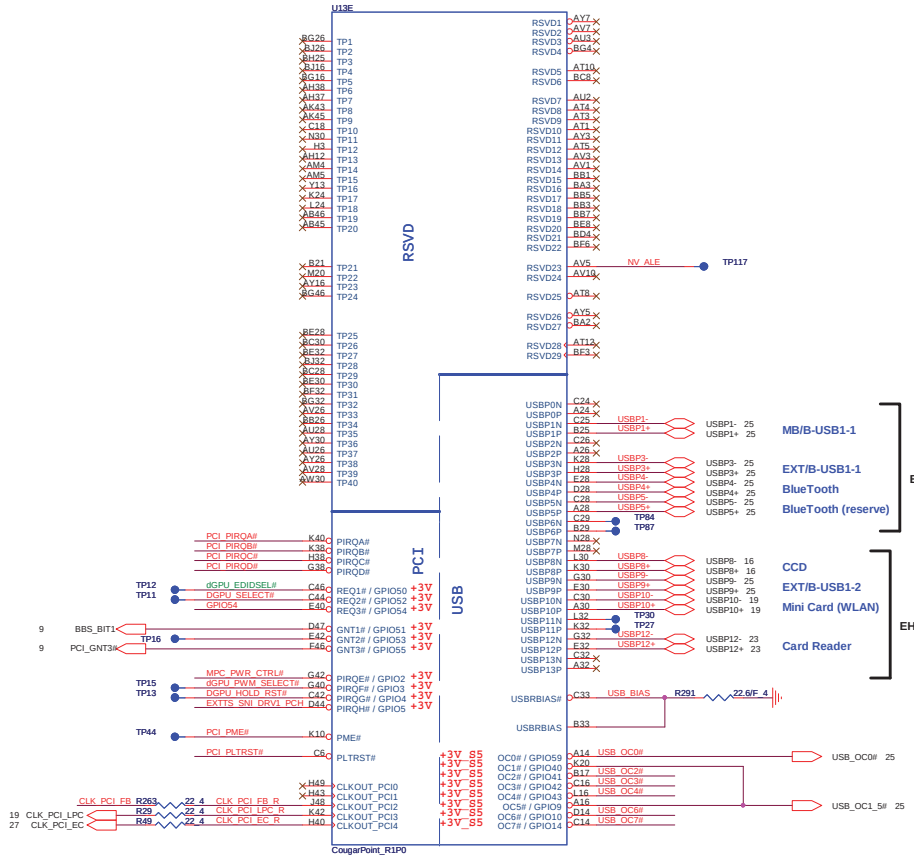



Quanta Computer Inc.

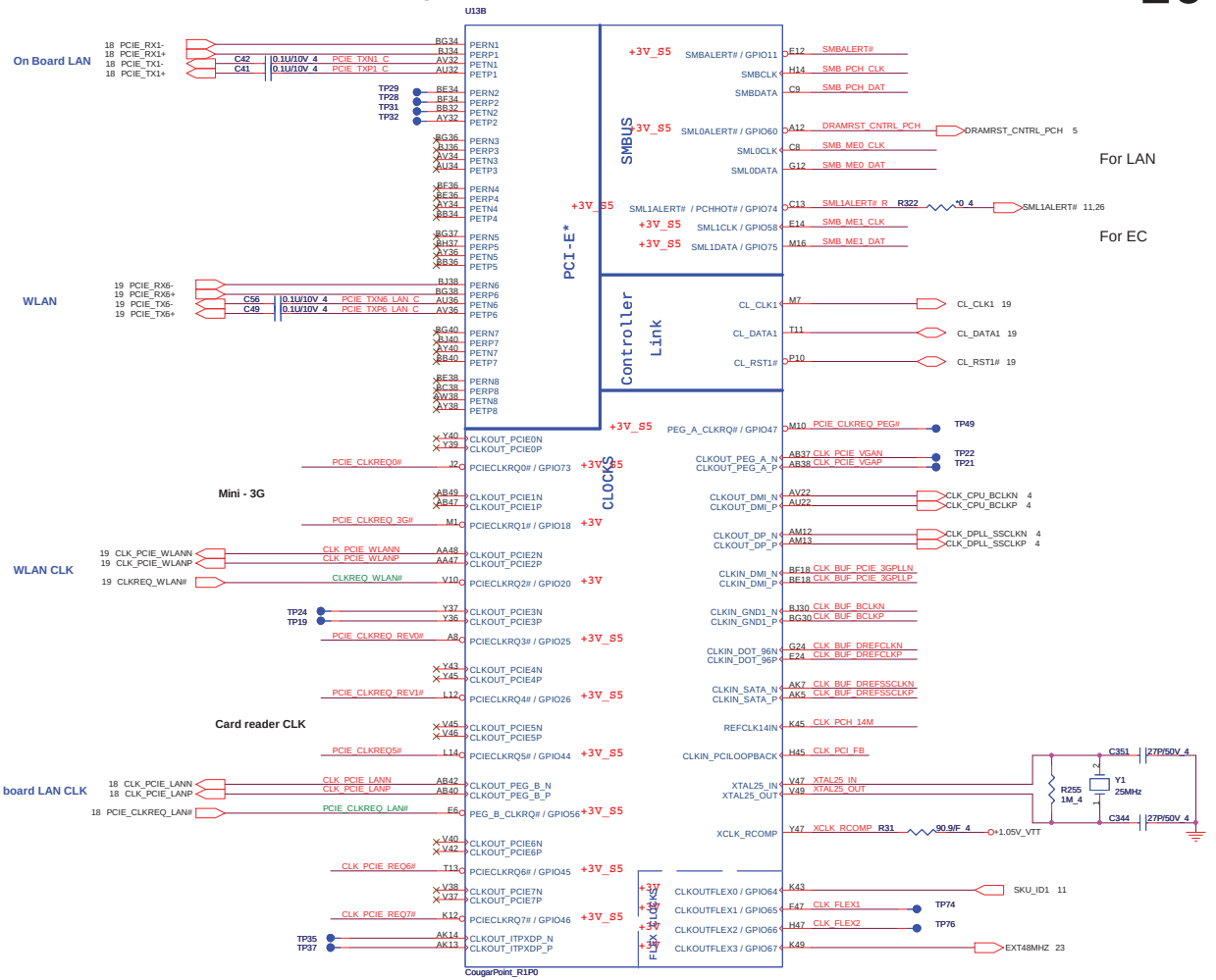
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 2/6 | 1A |
| Date: Monday, May 23, 2011 | Sheet 9 of 35 | |

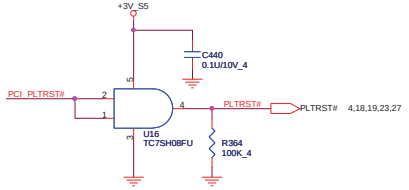
# Cougar Point-M (PCI,USB,NVRAM)



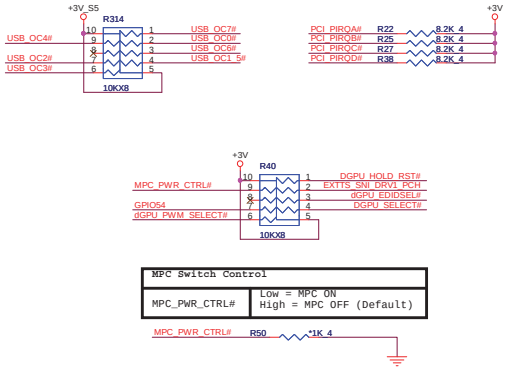

# Cougar Point-M (PCI-E,SMBUS,CLK)



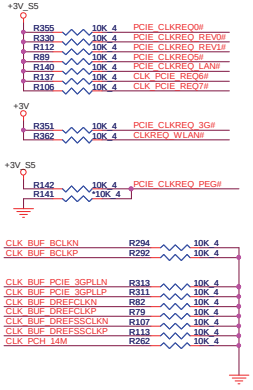

## PLTRST#(CLG)



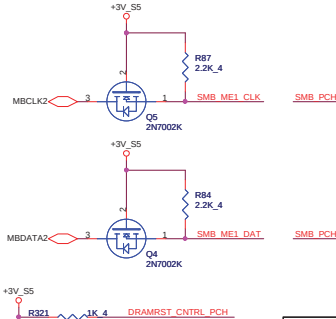

## PCI/USBOC# Pull-up(CLG)




## CLK_REQ/Strap Pin(CLG)




## SMBus/Pull-up(CLG)




## SMBus(PCH)



Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 3/6 | 1A |

Date: Monday, May 23, 2011 Sheet 10 of 35

# Cougar Point (GPIO,VSS_NCTF,RSVD)



U13F

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | S_GPIO | T7 | BMBUSY# / GPIO0 | +3V | +3V | TACH4 / GPIO68 | C40 | DGPU_PRSNT# |
| 27 EC_EXT_SMI# | EC_EXT_SMI# | A42 | TACH1 / GPIO1 | +3V | +3V | TACH5 / GPIO69 | B41 | R280 1.5K/F_4 |
| | BOARD_ID1 | H36 | TACH2 / GPIO6 | +3V | +3V | TACH6 / GPIO70 | C41 | R276 1.5K/F_4 +3V |
| 27 EC_EXT_SCI# | EC_EXT_SCI# | E38 | TACH3 / GPIO7 | +3V | +3V | TACH7 / GPIO71 | A40 | R279 1.5K/F_4 |
| TP111 | | C10 | GPIO8 | +3V_S5 | | | | |
| | SMIB# | C4 | LAN_PHY_PWR_CTRL / GPIO12 | | +3V_S5 | | | |
| | PCH_GPIO15 | G2 | GPIO15 | +3V_S5 | | A20GATE | P4 | EC_A20GATE → EC_A20GATE 27 |
| check VR_ON GPIO | SKU_ID0 | U2 | SATA4GP / GPIO16 | +3V | | PECI | AU16 | R325 *0_4 → EC_PECI 4,27 |
| | | | | | | RCIN# | P5 | EC_RCIN# → EC_RCIN# 27 |
| TP10 | dGPU_PWROK | D40 | TACH0 / GPIO17 | +3V | | PROCPWRGD | AY11 | TP36 → H_PWRGOOD 4 |
| | BIOS_REC | T5 | SCLOCK / GPIO22 | +3V | | THRMTRIP# | AY10 | PCH_THRMTRIP# R323 390_4 → PM_THRMTRIP# 4 |
| | CR_WAKER# | E8 | GPIO24 / MEM_LED | +3V_S5 | | INIT3_3V# | T14 | |
| | GPIO27 | E16 | GPIO27 | DSW | | DF_TVS | AY1 | DF_TVS 9 |
| 9 PLL_ODVR_EN | PLL_ODVR_EN | P8 | GPIO28 | +3V_S5 | | TS_VSS1 | AH8 | |
| Need Check | STP_PCI# | K1 | STP_PCI# / GPIO34 | +3V | | TS_VSS2 | AK11 | |
| TP40 | dGPU_VRON | K4 | GPIO35 | +3V | | TS_VSS3 | AH10 | |
| TP42 | DMI_OVRVLTG | V8 | SATA2GP / GPIO36 | +3V | | TS_VSS4 | AK10 | |
| | FDI_OVRVLTG | M5 | SATA3GP / GPIO37 | +3V | | NC_1 | P37 | |
| | MFG_MODE | N2 | SLOAD / GPIO38 | +3V | | | | |
| | BOARD_ID0 | M3 | SDATAOUT0 / GPIO39 | +3V | | VSS_NCTF_15 | BG2 | |
| | TEST_SET_UP | V13 | SDATAOUT1 / GPIO48 | +3V | | VSS_NCTF_16 | BG48 | |
| 10,26 SML1ALERT# | R148 *short_4 CRIT_TEMP_REP# | V3 | SATA5GP / GPIO49 | +3V | | VSS_NCTF_17 | BH3 | |
| | BOARD_ID2 | D6 | GPIO57 | +3V_S5 | | VSS_NCTF_18 | BH47 | |
| | | A4 | VSS_NCTF_1 | | | VSS_NCTF_19 | BJ4 | |
| | | A44 | VSS_NCTF_2 | | | VSS_NCTF_20 | BJ44 | |
| | | A45 | VSS_NCTF_3 | | | VSS_NCTF_21 | BJ45 | |
| | | A46 | VSS_NCTF_4 | | | VSS_NCTF_22 | BJ46 | |
| | | A5 | VSS_NCTF_5 | | | VSS_NCTF_23 | BJ5 | |
| | | A6 | VSS_NCTF_6 | | | VSS_NCTF_24 | BJ6 | |
| | | B3 | VSS_NCTF_7 | | | VSS_NCTF_25 | C2 | |
| | | B47 | VSS_NCTF_8 | | | VSS_NCTF_26 | C48 | |
| | | BD1 | VSS_NCTF_9 | | | VSS_NCTF_27 | D1 | |
| | | BD49 | VSS_NCTF_10 | | | VSS_NCTF_28 | D49 | |
| | | BE1 | VSS_NCTF_11 | | | VSS_NCTF_29 | E1 | |
| | | BE49 | VSS_NCTF_12 | | | VSS_NCTF_30 | E49 | |
| | | BF1 | VSS_NCTF_13 | | | VSS_NCTF_31 | F1 | |
| | | BF49 | VSS_NCTF_14 | | | VSS_NCTF_32 | F49 | |

GPIO CPU/MISC NCTF

CougarPoint_R1P0

R353??

| | DGPU_PRSNT# (GPIO68) | SKU_ID1 (GPIO64) | SKU_ID0 (GPIO16) | VGA H/W Signal | Setup Menu | |
|---|---|---|---|---|---|---|
| UMA Only | 1 | 0 | 0 | UMA | Hidden | UMA boot |

SV_SET_UP

High = Strong (Default)

TEST_SET_UP R136 10K_4 R120 *0_4 +3V

SGPIO

S_GPIO R135 1K/F_4 R118 *100_4 +3V

PCH_GPIO15 R356 1K_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

MFG-TEST

MFG_MODE R349 10K_4 R335 *0_4 +3V

*GPIO27:*

*Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep.*

*If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.*

GPIO Pull-up/Pull-down(CLG)

| | | | |
|---|---|---|---|
| CR_WAKER# | R108 | 10K/F_4 | +3V_S5 |
| SMB# | R341 | 10K_4 | |
| PLL_ODVR_EN | R139 | *10K_4 | |
| EC_EXT_SMI# | R278 | 10K_4 | +3V |
| EC_EXT_SCI# | R41 | 10K_4 | |
| STP_PCI# | R354 | *10K_4 | |
| EC_A20GATE | R119 | 10K_4 | |
| EC_RCIN# | R123 | 10K_4 | |
| CRIT_TEMP_REP# | R147 | 10K_4 | |
| dGPU_PWROK | R23 | *10K_4 | |
| GPIO27 | R86 | *10K_4 | |

+3V R281 IV@10K_4 R282 *EV@100K_4 DGPU_PRSNT#

+3V R37 *EV@10K_4 R36 IV@10K_4 SKU_ID1 10

+3V R345 *10K_4 R332 IV@10K_4 SKU_ID0

+3V R336 10K_4 BOARD_ID0 R352 *10K_4

R45 10K_4 BOARD_ID1 R46 *10K_4

+3V_S5 R339 100K_4 BOARD_ID2 R340 *10K_4

FDI_OVRVLTG R122 *10K/F_4 +3V

| | |
|---|---|
| FDI TERMINATION VOLTAGE OVERRIDE | LOW - Tx, Rx terminated to same voltage |

DMI_OVRVLTG R128 *200K/F_4 +3V

| | |
|---|---|
| DMI TERMINATION VOLTAGE OVERRIDE | Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT) |

BIOS_REC R134 10K_4 R117 *0_4 +3V

| | |
|---|---|
| BIOS RECOVERY | High = Disable (Default) Low = Enable |

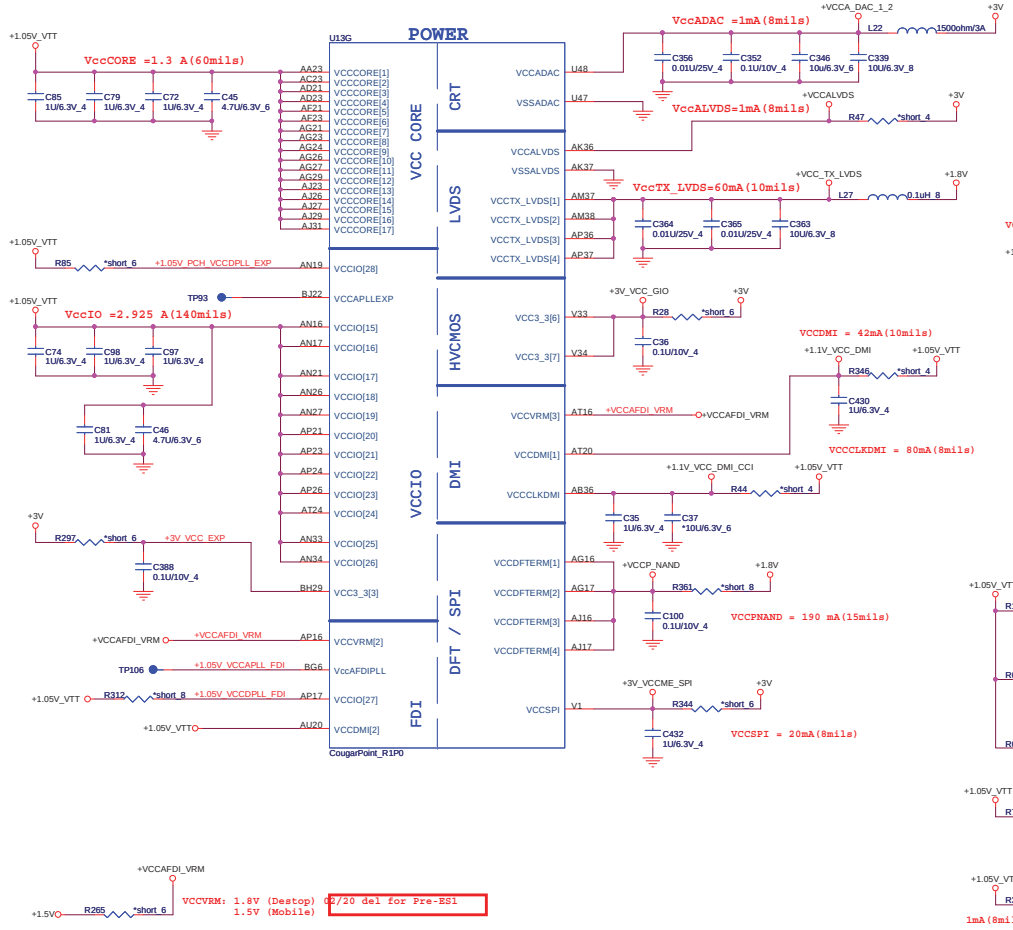
Quanta Computer Inc.

PROJECT : ZQR

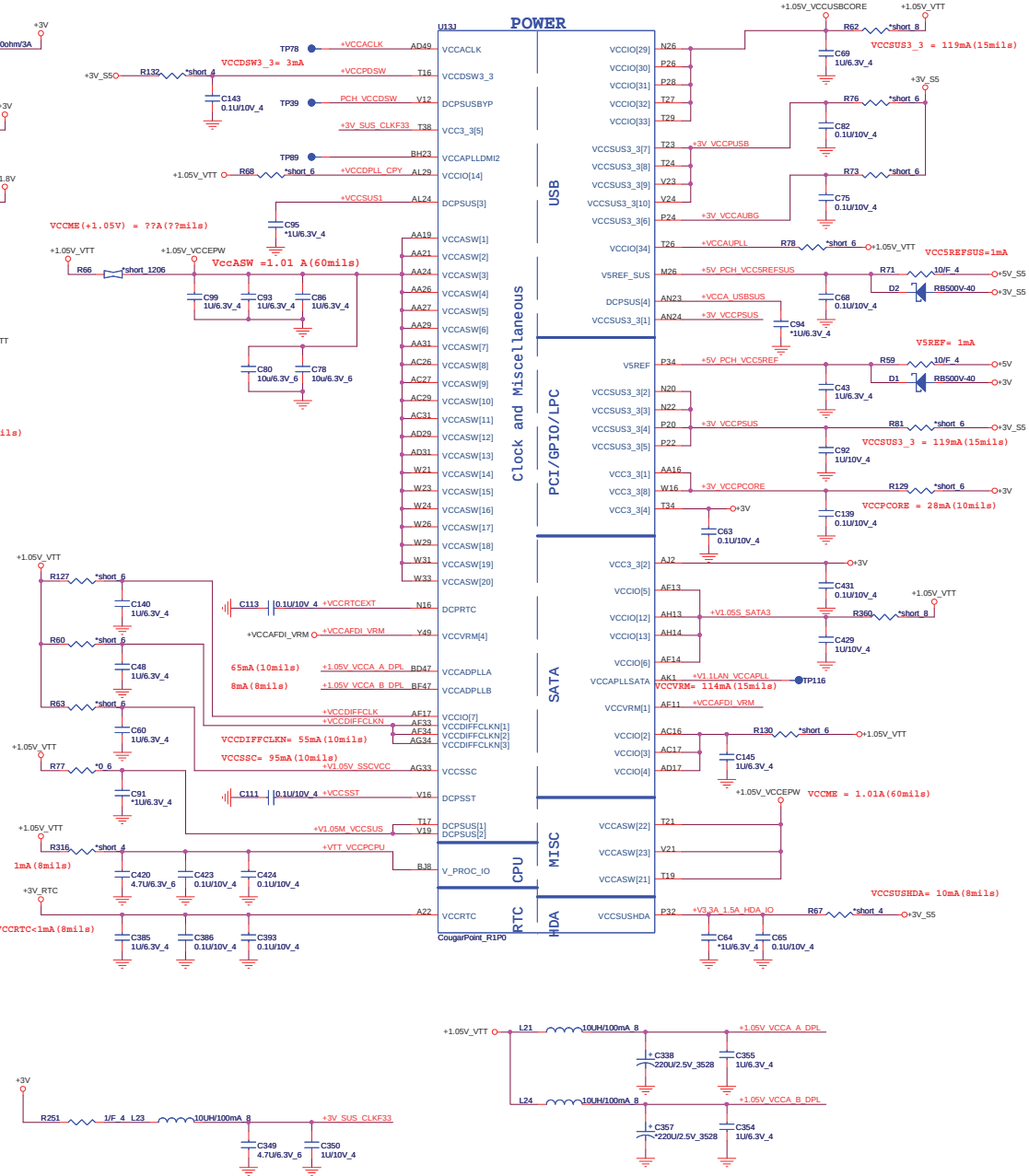
| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 4/6 | 1A |

Date: Monday, May 23, 2011 Sheet 11 of 35

## COUGAR POINT (POWER)




## Cougar Point-M (POWER)






Quanta Computer Inc.

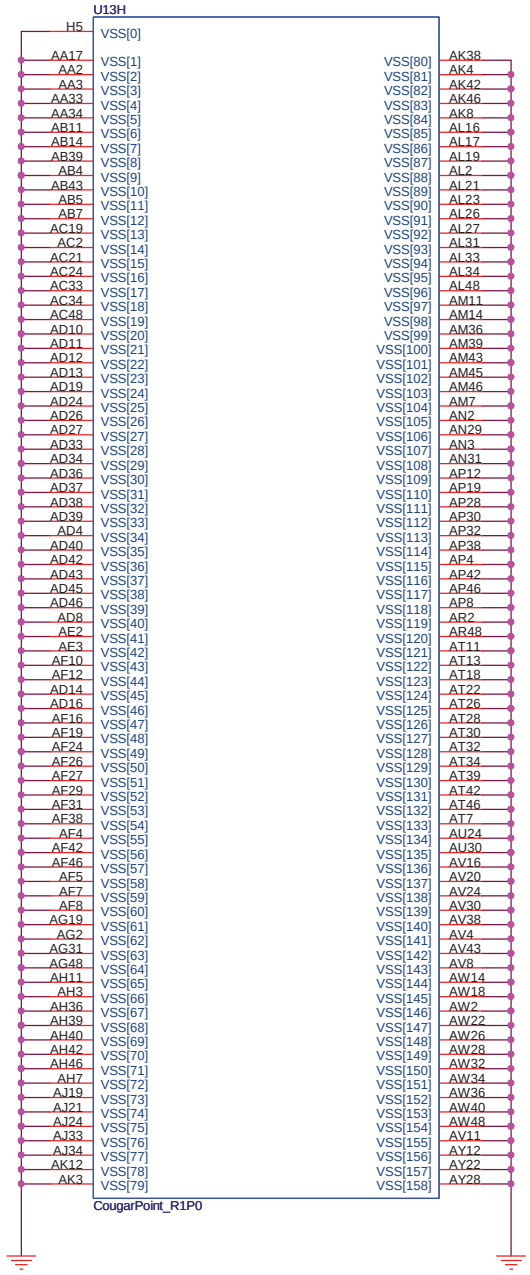
PROJECT : ZQR

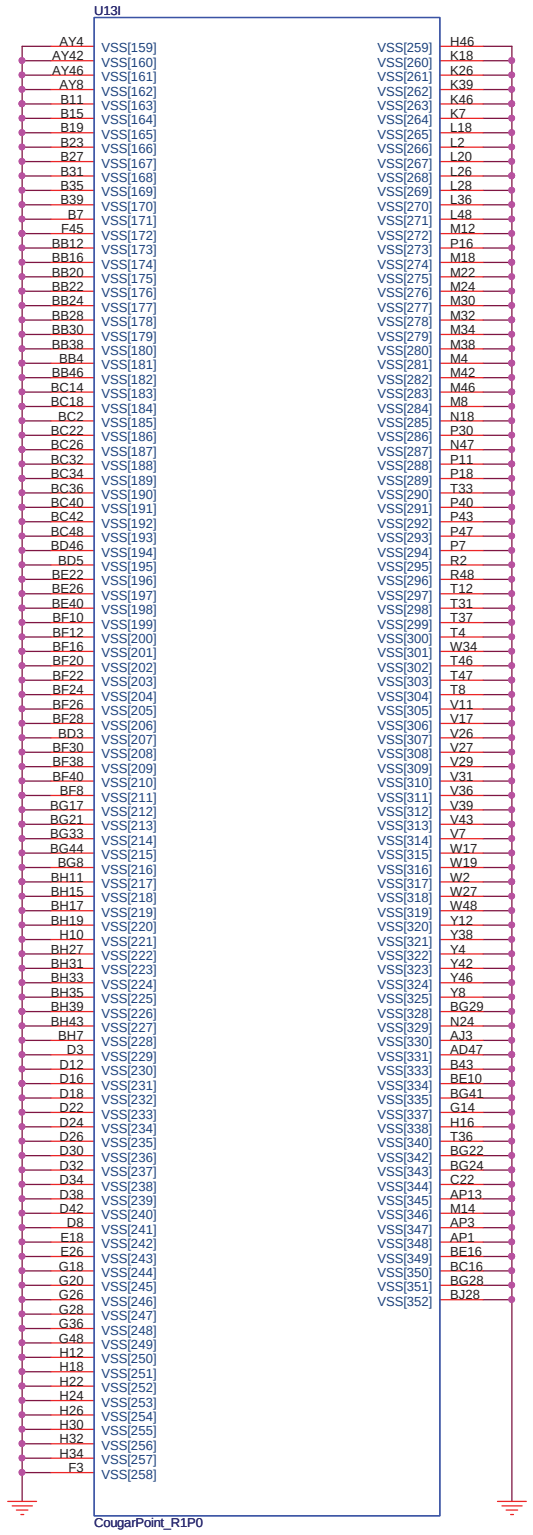
| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 5/6 | 1A |

Date: Monday, May 09, 2011 Sheet 12 of 35

PCH6 (CLG)

# IBEX PEAK-M (GND)




13

Quanta Computer Inc.

PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 6/6 | 1A |
| Date: Monday, May 09, 2011 | Sheet 13 of 35 | |

# DDR RVS 4H



5 M_A_A[15:0]

JDIM2A

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

5 M_A_BS#0 109 BA0
5 M_A_BS#1 108 BA1
5 M_A_BS#2 79 BA2
5 M_A_CS#0 114 S0#
5 M_A_CS#1 121 S1#
5 M_A_CLKP0 101 CK0
5 M_A_CLKN0 103 CK0#
5 M_A_CLKP1 102 CK1
5 M_A_CLKN1 104 CK1#
5 M_A_CKE0 73 CKE0
5 M_A_CKE1 74 CKE1
5 M_A_CAS# 115 CAS#
5 M_A_RAS# 110 RAS#
5 M_A_WE# 113 WE#

R186 10K_4
R185 10K_4
DIMM0_SA0 197 SA0
DIMM0_SA1 201 SA1
10,15,19 SMB_RUN_CLK SMB_RUN_CLK 202 SCL
10,15,19 SMB_RUN_DAT SMB_RUN_DAT 200 SDA

5 M_A_ODT0 116 ODT0
5 M_A_ODT1 120 ODT1

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_RVS_LTS

M_A_DQ[63:0] 5

M_A_DQ4 5 DQ0
M_A_DQ5 7 DQ1
M_A_DQ7 15 DQ2
M_A_DQ6 17 DQ3
M_A_DQ1 4 DQ4
M_A_DQ0 6 DQ5
M_A_DQ3 16 DQ6
M_A_DQ2 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ15 33 DQ10
M_A_DQ10 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ11 34 DQ14
M_A_DQ14 36 DQ15
M_A_DQ20 39 DQ16
M_A_DQ21 41 DQ17
M_A_DQ19 51 DQ18
M_A_DQ18 53 DQ19
M_A_DQ16 40 DQ20
M_A_DQ17 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ25 57 DQ24
M_A_DQ24 59 DQ25
M_A_DQ27 67 DQ26
M_A_DQ31 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ26 68 DQ30
M_A_DQ30 70 DQ31
M_A_DQ37 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ38 143 DQ35
M_A_DQ32 130 DQ36
M_A_DQ36 132 DQ37
M_A_DQ35 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ41 147 DQ40
M_A_DQ45 149 DQ41
M_A_DQ47 157 DQ42
M_A_DQ46 159 DQ43
M_A_DQ40 146 DQ44
M_A_DQ44 148 DQ45
M_A_DQ42 158 DQ46
M_A_DQ43 160 DQ47
M_A_DQ49 163 DQ48
M_A_DQ48 165 DQ49
M_A_DQ54 175 DQ50
M_A_DQ55 177 DQ51
M_A_DQ53 164 DQ52
M_A_DQ52 166 DQ53
M_A_DQ51 174 DQ54
M_A_DQ50 176 DQ55
M_A_DQ61 181 DQ56
M_A_DQ60 183 DQ57
M_A_DQ62 191 DQ58
M_A_DQ63 193 DQ59
M_A_DQ56 180 DQ60
M_A_DQ57 182 DQ61
M_A_DQ59 192 DQ62
M_A_DQ58 194 DQ63

11 DM0
28 DM1
46 DM2
63 DM3
136 DM4
153 DM5
170 DM6
187 DM7

5 M_A_DQSP[7:0]

M_A_DQSP0 12 DQS0
M_A_DQSP1 29 DQS1
M_A_DQSP2 47 DQS2
M_A_DQSP3 64 DQS3
M_A_DQSP4 137 DQS4
M_A_DQSP5 154 DQS5
M_A_DQSP6 171 DQS6
M_A_DQSP7 188 DQS7
M_A_DQSN0 10 DQS#0
M_A_DQSN1 27 DQS#1
M_A_DQSN2 45 DQS#2
M_A_DQSN3 62 DQS#3
M_A_DQSN4 135 DQS#4
M_A_DQSN5 152 DQS#5
M_A_DQSN6 169 DQS#6
M_A_DQSN7 186 DQS#7

5 M_A_DQSN[7:0]

**02/23 Remove 0ohm to GND**

+1.5V_SUS

JDIM2B

2.48A

75 VDD1
76 VDD2
81 VDD3
82 VDD4
87 VDD5
88 VDD6
93 VDD7
94 VDD8
99 VDD9
100 VDD10
105 VDD11
106 VDD12
111 VDD13
112 VDD14
117 VDD15
118 VDD16
123 VDD17
124 VDD18

+3V 199 VDDSPD

77 NC1
122 NC2
125 NCTEST

+3V R176 10K_4
198 EVENT#
5,15 DDR3_DRAMRST# DDR3_DRAMRST# 30 RESET#

SMDDR_VREF_DQ0_M1 SMDDR_VREF_DQ0_M1 1 VREF_DQ
+SMDDR_VREF_DIMM +SMDDR_VREF_DIMM 126 VREF_CA

2 VSS1
3 VSS2
8 VSS3
9 VSS4
13 VSS5
14 VSS6
19 VSS7
20 VSS8
25 VSS9
26 VSS10
31 VSS11
32 VSS12
37 VSS13
38 VSS14
43 VSS15

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203 +0.75V_DDR_VTT
VTT2 204

GND 205
GND 206

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4_RVS_LTS

**CAD Note: All VREF traces should have 10 mil trace width**

DDR3_DRAMRST#
C180
0.1u/10V_4

**VREF DQ0 M1 Solution**

+1.5V_SUS
R183 1K/F_4
SMDDR_VREF_DQ0_M1
R184 1K/F_4

+1.5V_SUS
R173 10K/F_4
+SMDDR_VREF_DIMM
R177 10K/F_4
C224 470P/50V_4

**Place these Caps near So-Dimm0.**

+1.5V_SUS
C221 4.7U/6.3V_6
C190 4.7U/6.3V_6
C203 4.7U/6.3V_6
C202 4.7U/6.3V_6
C187 4.7U/6.3V_6
C189 4.7U/6.3V_6
C188 *10U/6.3V_6
C205 1U/10V_4
C185 1U/10V_4
C186 1U/10V_4
C204 1U/10V_4
C157 *330U/2V_7343
C178 4.7U/25V_8
C184 4.7U/25V_8

+3V
C240 2.2U/6.3V_6
C242 0.1u/10V_4

+0.75V_DDR_VTT
C235 1U/6.3V_4
C236 1U/6.3V_4
C227 1u/6.3V_4
C226 1U/6.3V_4
C229 4.7U/6.3V_6
C237 *10U/6.3V_6

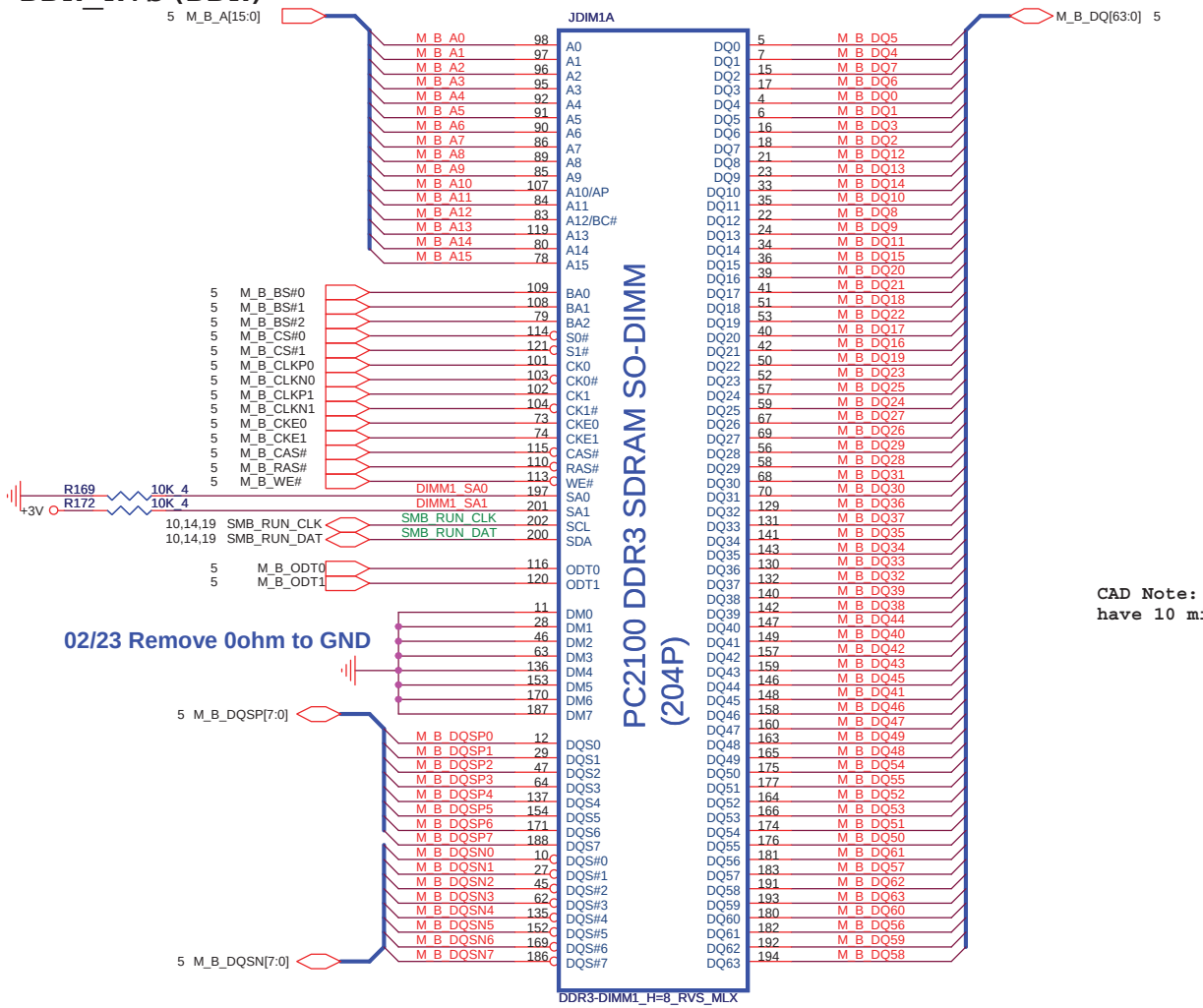
+SMDDR_VREF_DIMM
C196 0.1u/10V_4
C215 2.2U/6.3V_6

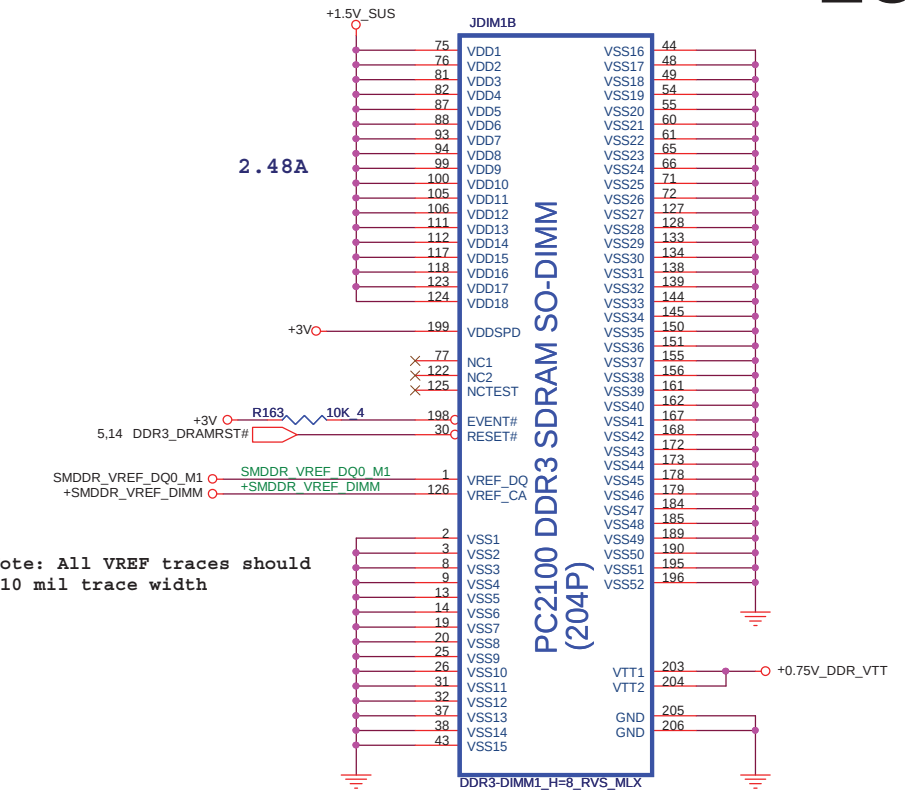
SMDDR_VREF_DQ0_M1
C244 0.1u/10V_4
C243 2.2U/6.3V_6

Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-0 | 1A |
| Date: Monday, May 23, 2011 | Sheet 14 of 35 | |

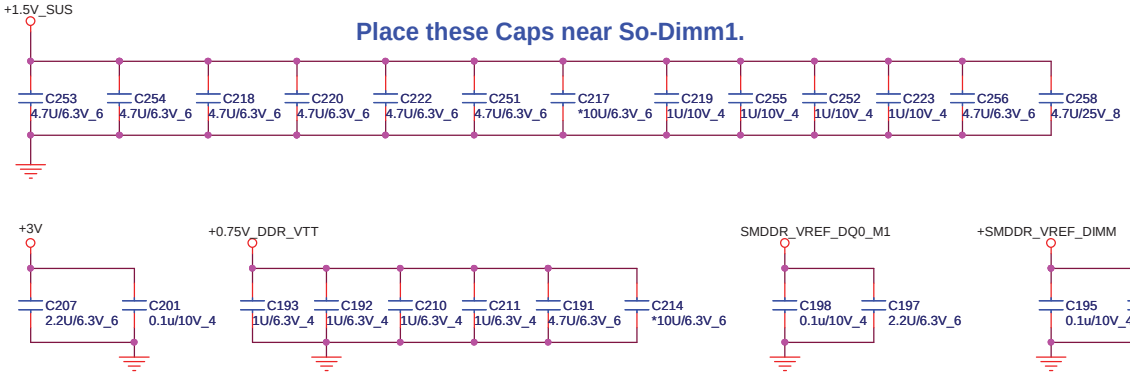
# DDR_RVS (DDR)




**CAD Note: All VREF traces should have 10 mil trace width**

## Place these Caps near So-Dimm1.




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQR | | |
| Size | Document Number: DDRIII SO-DIMM-1 | Rev: 1A |
| Date: Monday, May 23, 2011 | Sheet 15 of 35 | |

## CRT Switch

0_ohm Resistor place close to Joint-Point

8 INT_CRT_RED — INT_CRT_RED
8 INT_CRT_GRE — INT_CRT_GRE
8 INT_CRT_BLU — INT_CRT_BLU

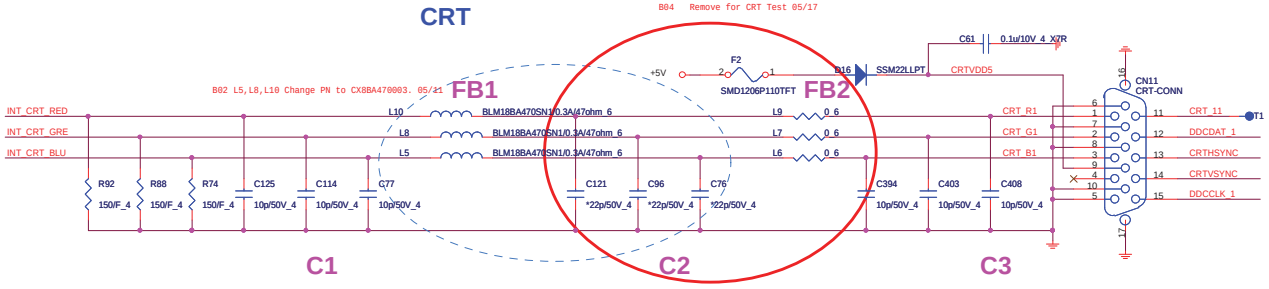
8 INT_CRT_VSYNC — INT_CRT_VSYNC
8 INT_CRT_HSYNC — INT_CRT_HSYNC

8 INT_CRT_DDCDAT — INT_CRT_DDCDAT
8 INT_CRT_DDCCLK — INT_CRT_DDCCLK

## CRT

B04 Remove for CRT Test 05/17

B02 L5,L8,L10 Change PN to CX8BA470003. 05/11

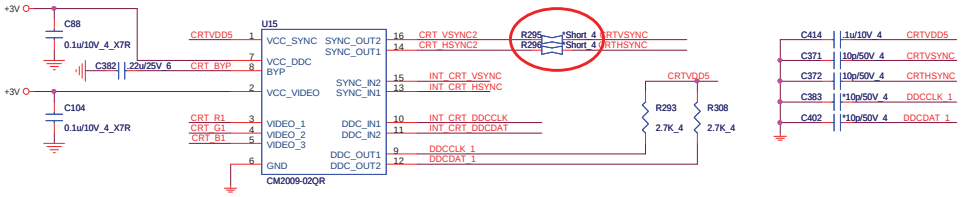



Note:this video filter is a 2-pole,low-pass filter configuration with a target design cutoff frequency of ~200MHZ

C1: 10pF ,C2 : 22pF , C3 :10pF,

FB1:47ohm@100MHZ , FB2:47ohm@100MHZ

B06 Change R295,R296 to short pad. 5/17




## LVDS

0_ohm Resistor place close to Joint-Point

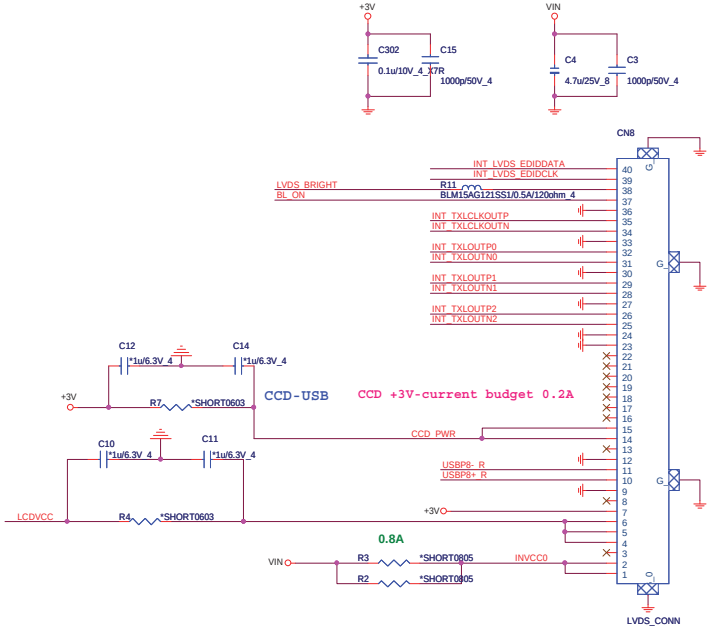
8 INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK
8 INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA

C18 2200p/50V_4
C17 2200p/50V_4
EMI

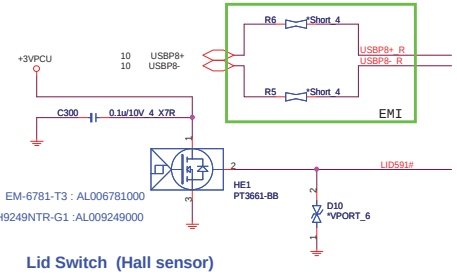
8 INT_LVDS_DIGON — INT_LVDS_DIGON
8 INT_LVDS_BLON — INT_LVDS_BLON

8 INT_TXLCLKOUTP — INT_TXLCLKOUTP
8 INT_TXLCLKOUTN — INT_TXLCLKOUTN
8 INT_TXLOUTP0 — INT_TXLOUTP0
8 INT_TXLOUTN0 — INT_TXLOUTN0
8 INT_TXLOUTP1 — INT_TXLOUTP1
8 INT_TXLOUTN1 — INT_TXLOUTN1
8 INT_TXLOUTP2 — INT_TXLOUTP2
8 INT_TXLOUTN2 — INT_TXLOUTN2

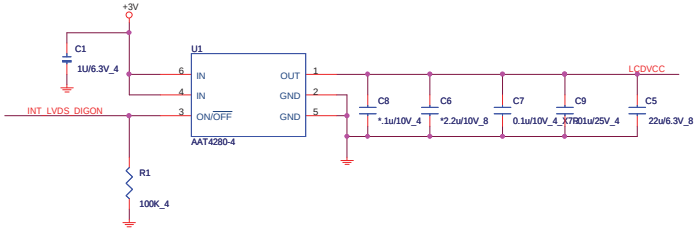
27 CONTRAST — R8 *0_4 — LVDS_BRIGHT
8 INT_LVDS_BRIGHT — R9 0_4



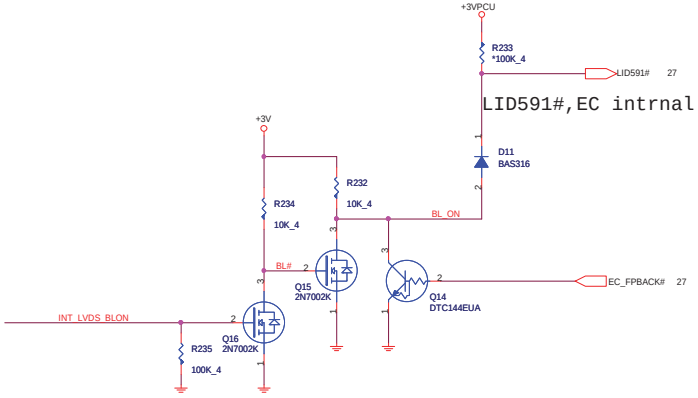

B43 Change 0: R5,R6 to short pad, remove CMC L1. 5/19




## LCD Power



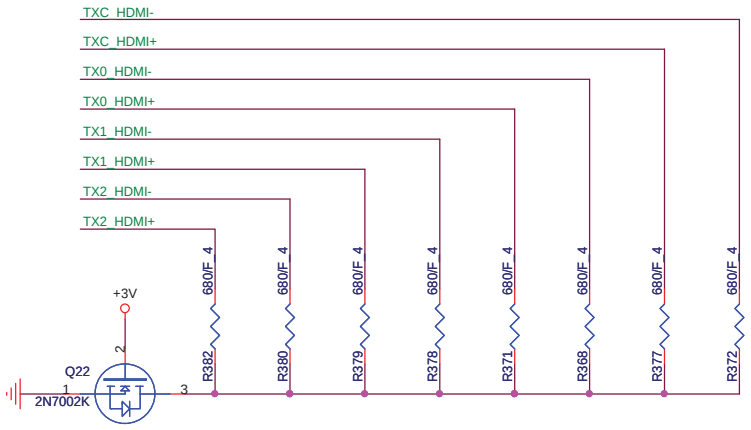

## Backlight Control






Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | CRT/LVDS/CAMERA/LID | 1A |
| Date: Monday, May 23, 2011 | Sheet 16 of 35 | |

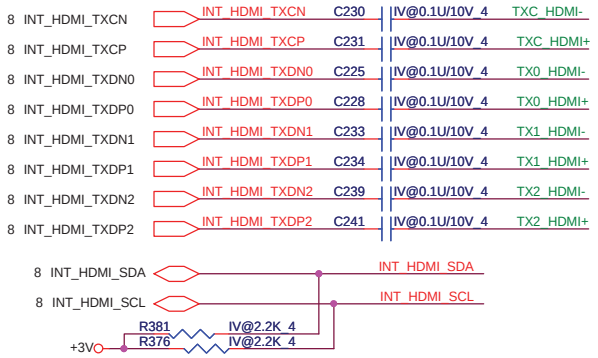



| | EV@ | IV@ |
|---|---|---|
| SP@ | 500 ohm | 680 ohm |

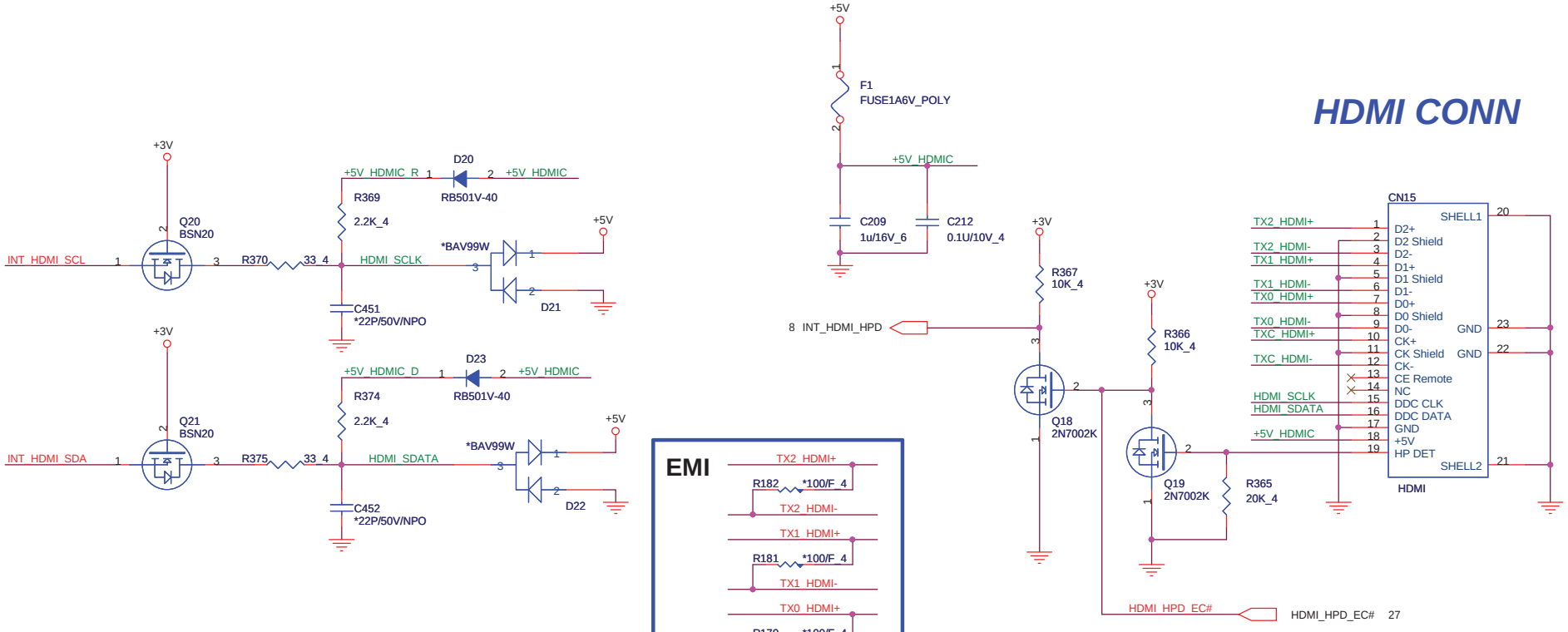
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

## INT-HDMI

PLACE AC CAP CLOSE TO CONNECTOR




## HDMI CONN




## EMI




Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | HDMI | 1A |
| Date: Monday, May 23, 2011 | Sheet 17 of 35 | |

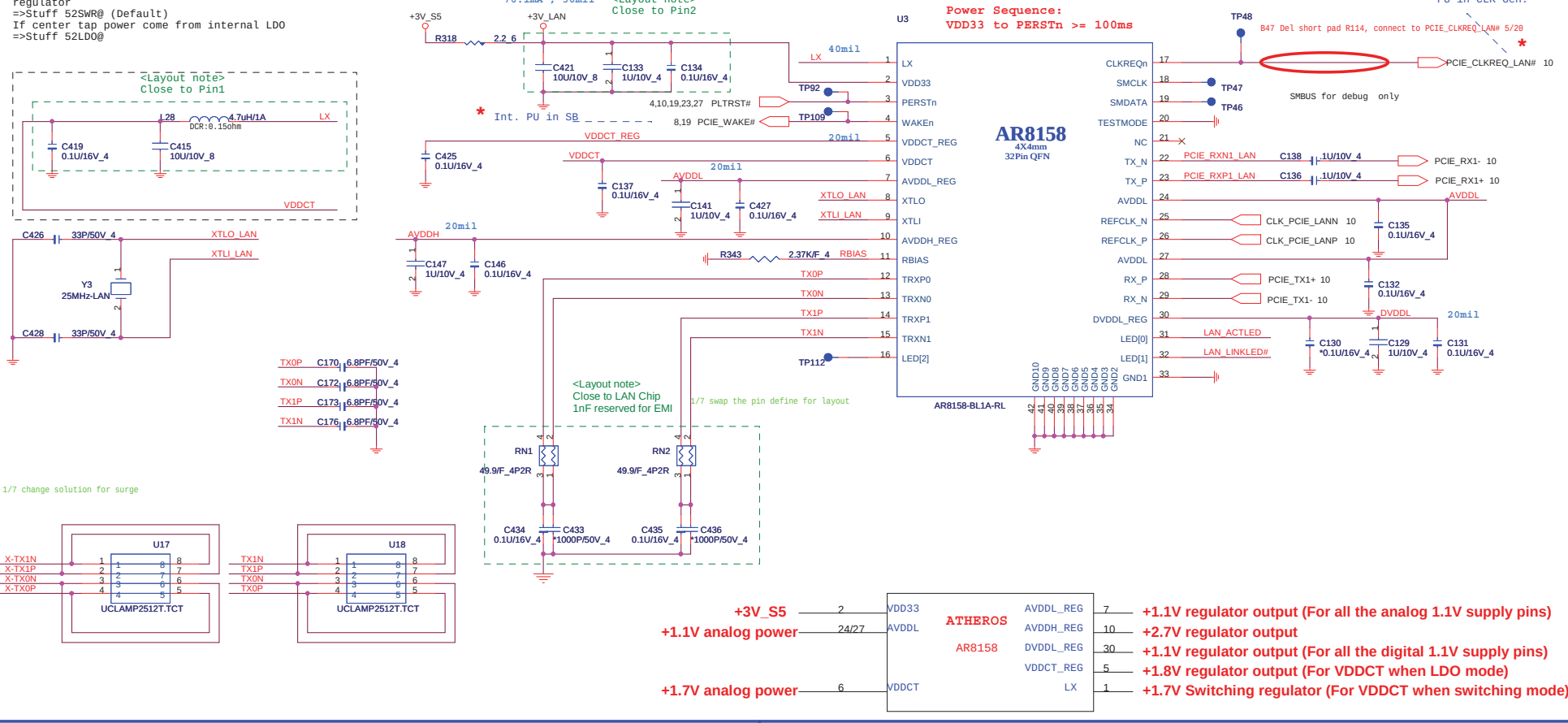
# LAN (LAN)

<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms

PU in CLK Gen.

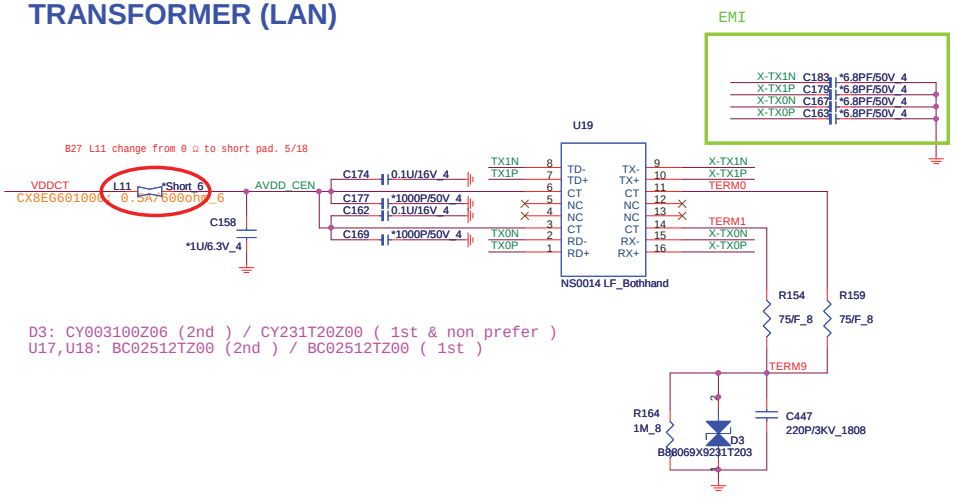



| | | | |
|---|---|---|---|
| +3V_S5 | 2 | AVDDL_REG | 7 |
| +1.1V analog power | 24/27 | AVDDH_REG | 10 |
| | | DVDDL_REG | 30 |
| | | VDDCT_REG | 5 |
| +1.7V analog power | 6 | LX | 1 |

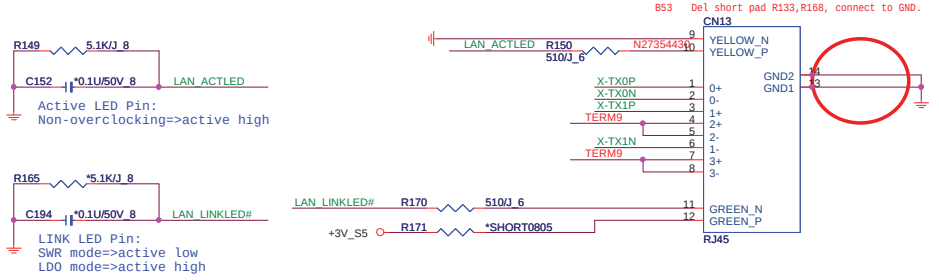
ATHEROS AR8158

- +1.1V regulator output (For all the analog 1.1V supply pins)
- +2.7V regulator output
- +1.1V regulator output (For all the digital 1.1V supply pins)
- +1.8V regulator output (For VDDCT when LDO mode)
- +1.7V Switching regulator (For VDDCT when switching mode)

# TRANSFORMER (LAN)




# RJ45 Connector (LAN)





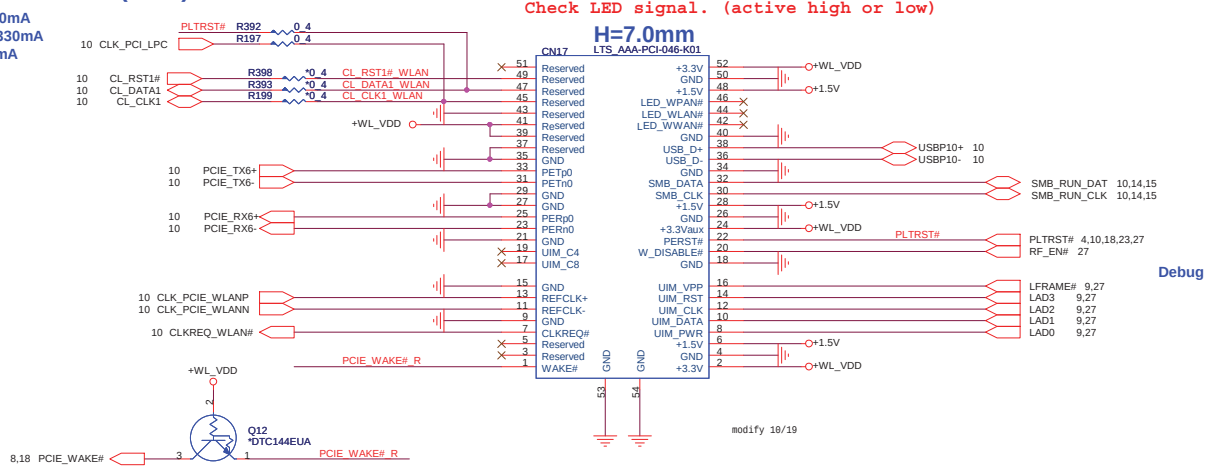

Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | LAN AR8158L | 1A |
| Date: Monday, May 23, 2011 | Sheet 18 of 35 | |

# MINI-CARD WLAN(MPC)

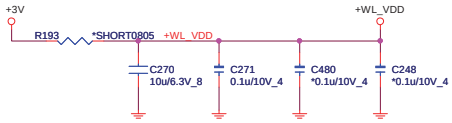
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

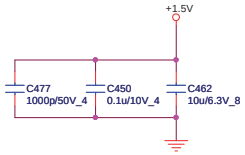
Check LED signal. (active high or low)




Debug

modify 10/19



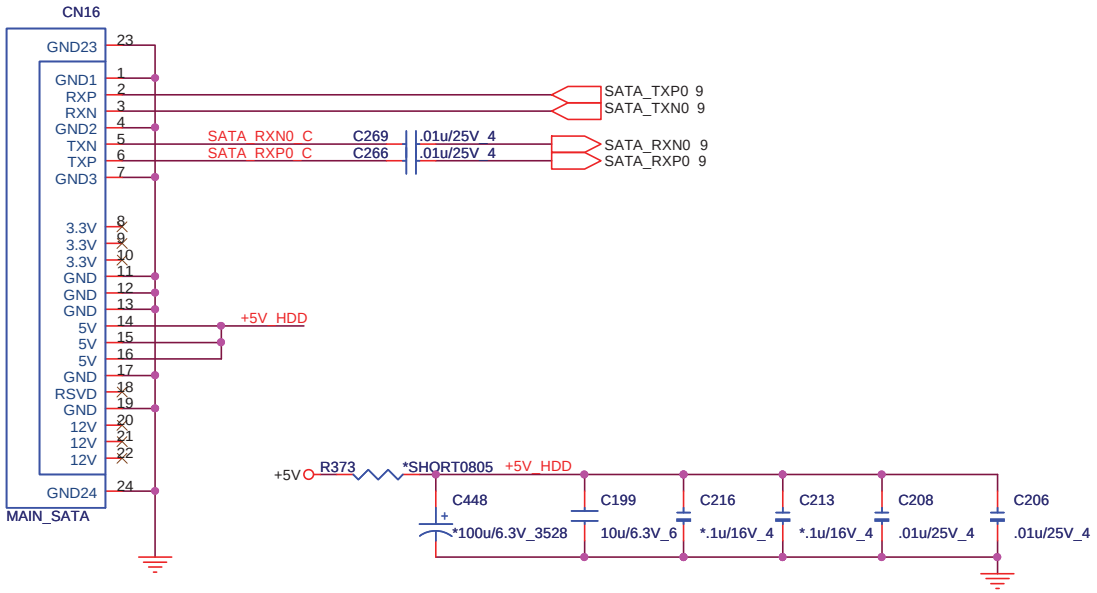




Quanta Computer Inc.
PROJECT : ZQR

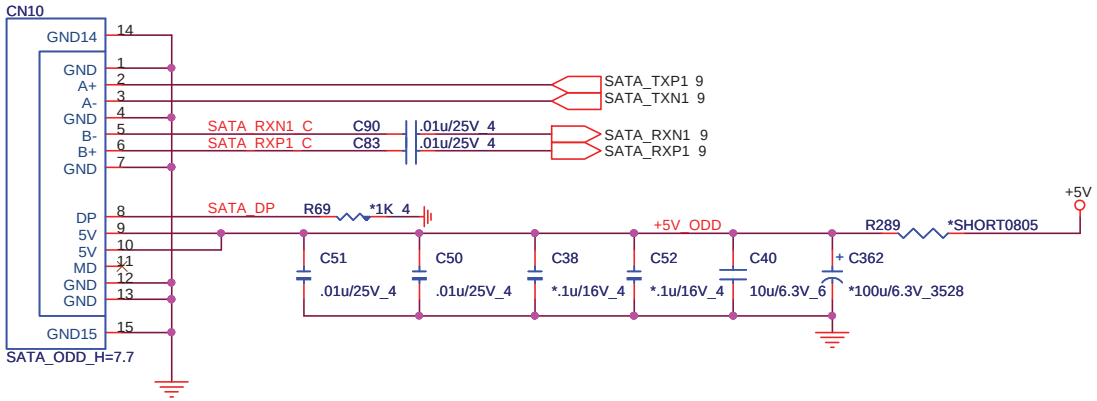
| Size | Document Number | Rev |
|---|---|---|
| | MINI PCI-E card/TV | 1A |

Date: Monday, May 23, 2011 Sheet 19 of 35

# MAIN SATA HDD

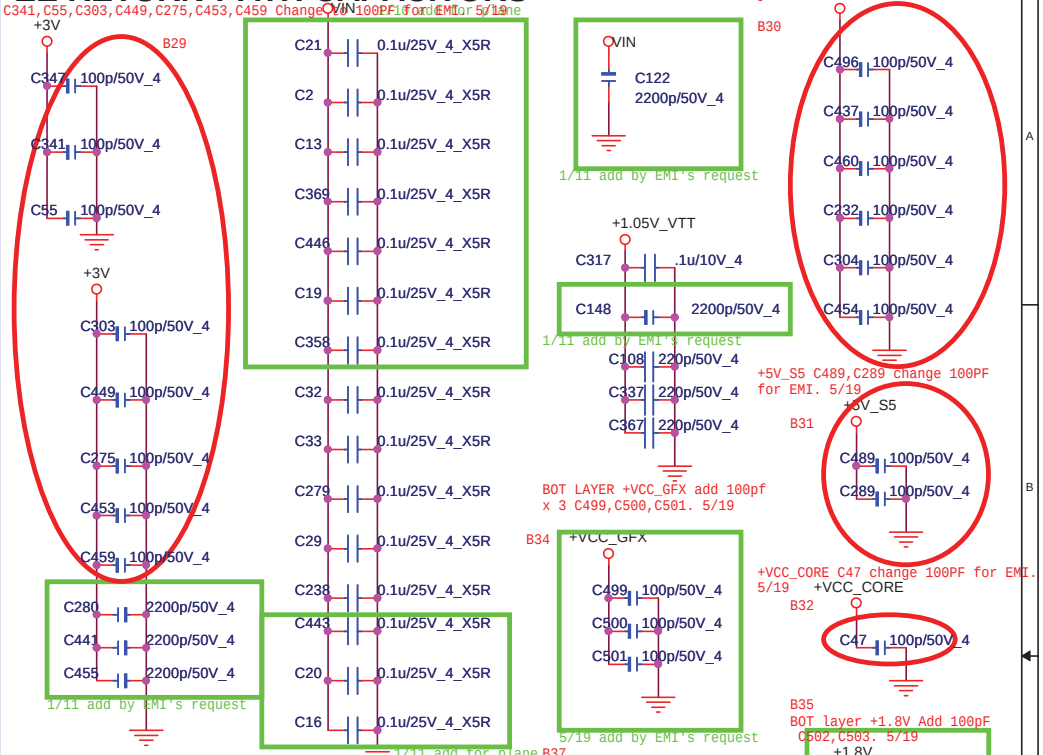



# ODD (SATA)

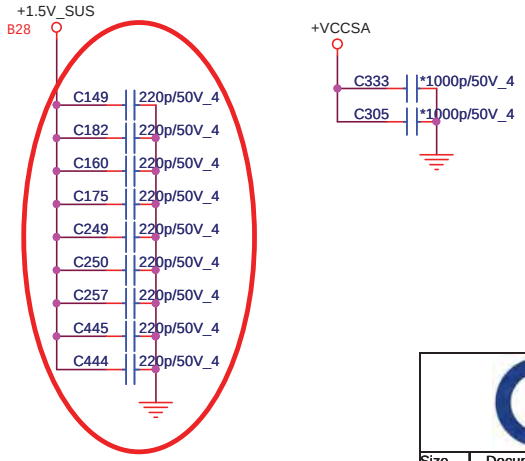



# EE RETURN-PATH CAPACITORS

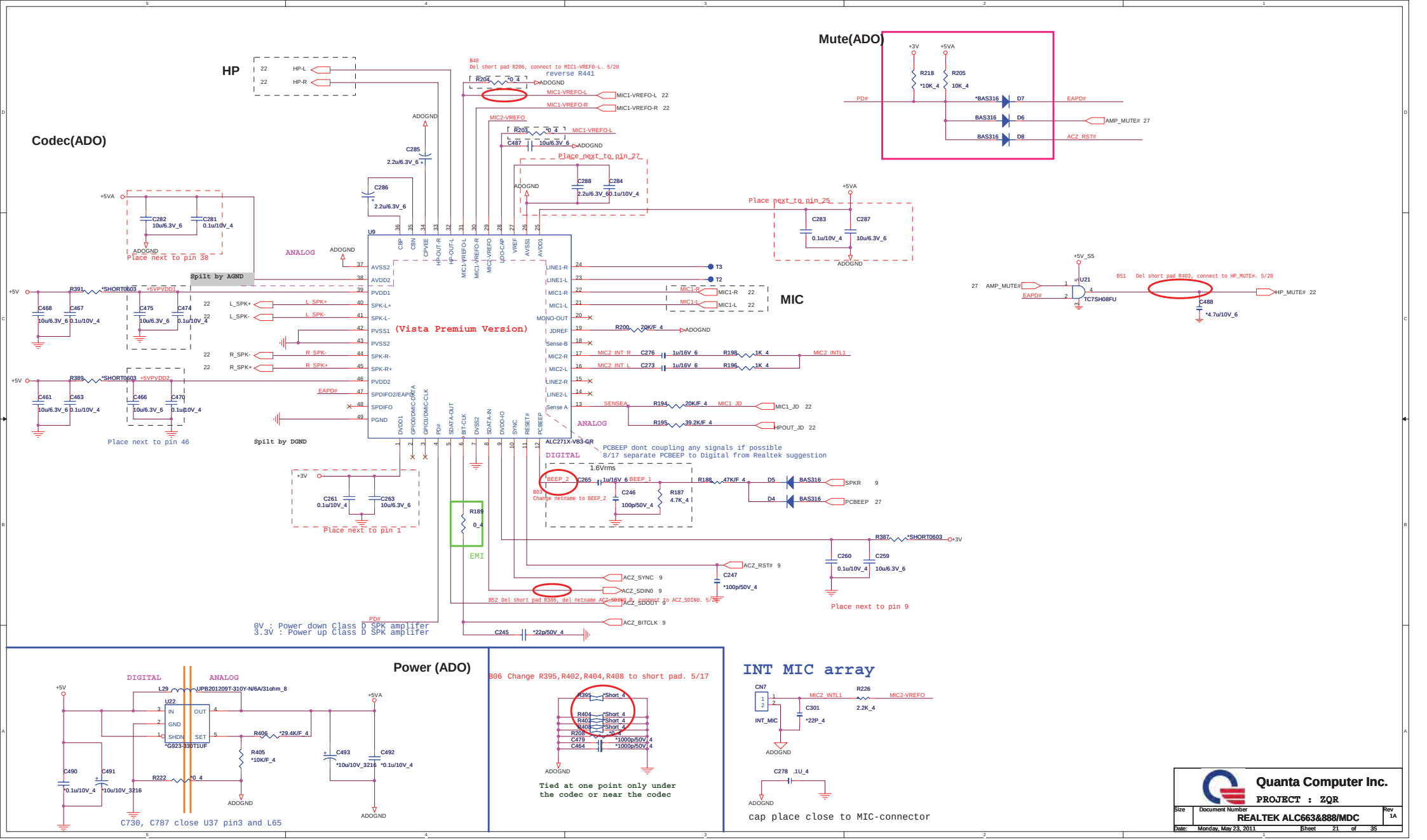
+3V C347,C341,C55,C303,C449,C275,C453,C459 Change 100PF for EMI. 5/19



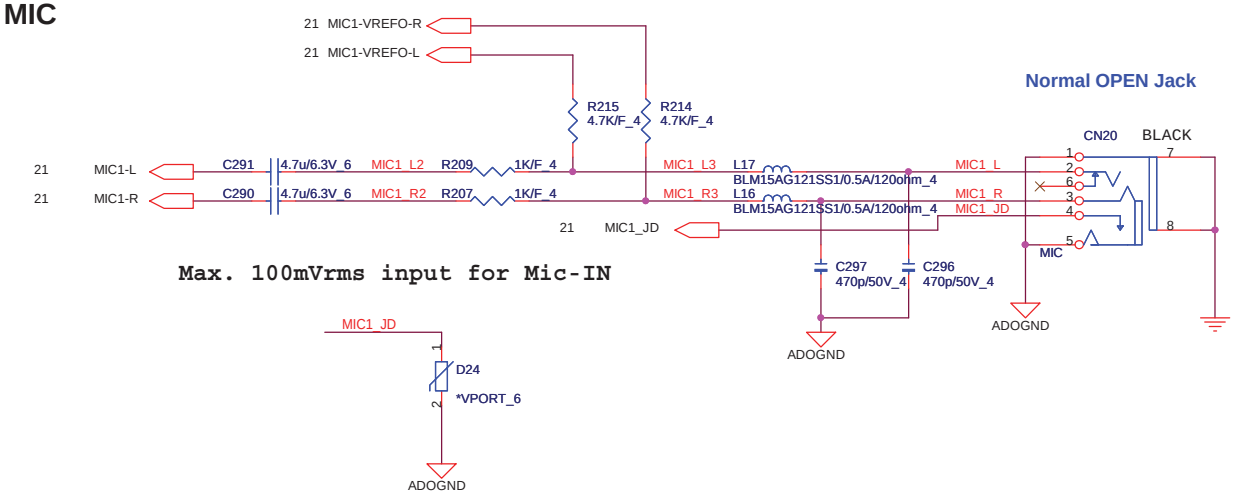

+1.5V_SUS mount C149,C182,C160,C175,C249,C250,C257,C445,C444 Cap for EMI. 5/19




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQR | | |
| Size | Document Number: SATA-HDD/ODD | Rev: 1A |
| Date: Monday, May 23, 2011 | Sheet 20 of 35 | |

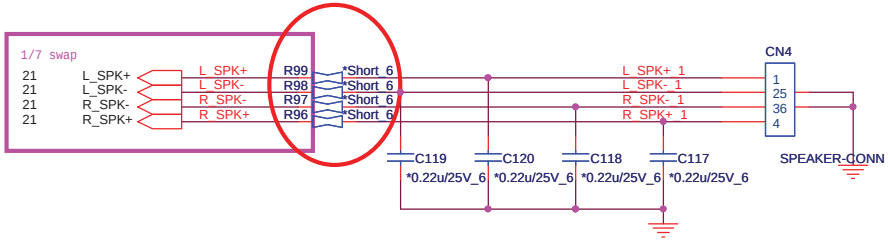

HP
Codec(ADO)
Mute(ADO)
MIC
ANALOG
DIGITAL
(Vista Premium Version)
ALC271X-VB3-GR
Spilt by AGND
Spilt by DGND
Place next to pin 38
Place next to pin 46
Place next to pin 1
Place next to pin 25
Place next to pin 27
Place next to pin 9
reverse R441
PCBEEP dont coupling any signals if possible
8/17 separate PCBEEP to Digital from Realtek suggestion
1.6Vrms
EMI
0V : Power down Class D SPK amplifier
3.3V : Power up Class D SPK amplifier
Power (ADO)
C730, C787 close U37 pin3 and L65
B06 Change R395,R402,R404,R408 to short pad. 5/17
Tied at one point only under
the codec or near the codec
INT MIC array
cap place close to MIC-connector
Quanta Computer Inc.
PROJECT : ZQR
REALTEK ALC663&888/MDC
Size
Document Number
Rev
1A
Date: Monday, May 23, 2011
Sheet 21 of 35

## MIC

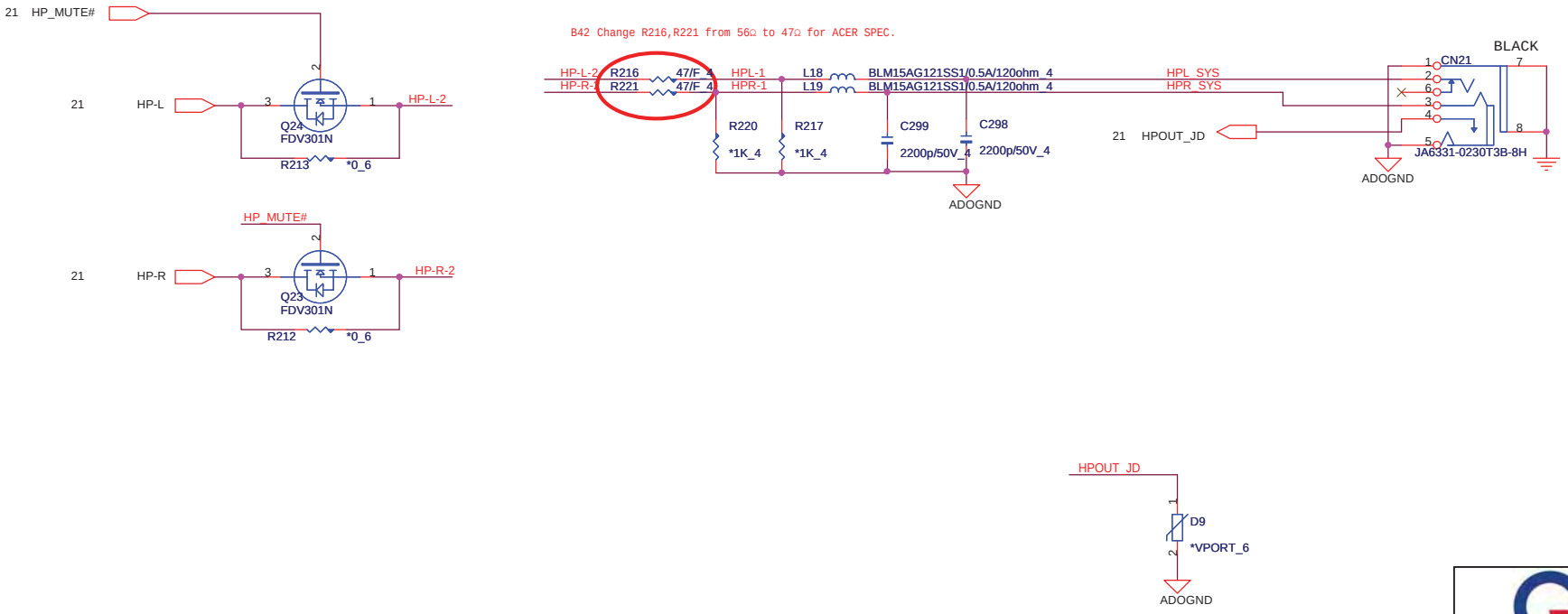



## Internal Speaker

B27 R96,R97,R98,R99 change from 0 Ω to short pad. 5/18




## HP/SPDIF




Quanta Computer Inc.

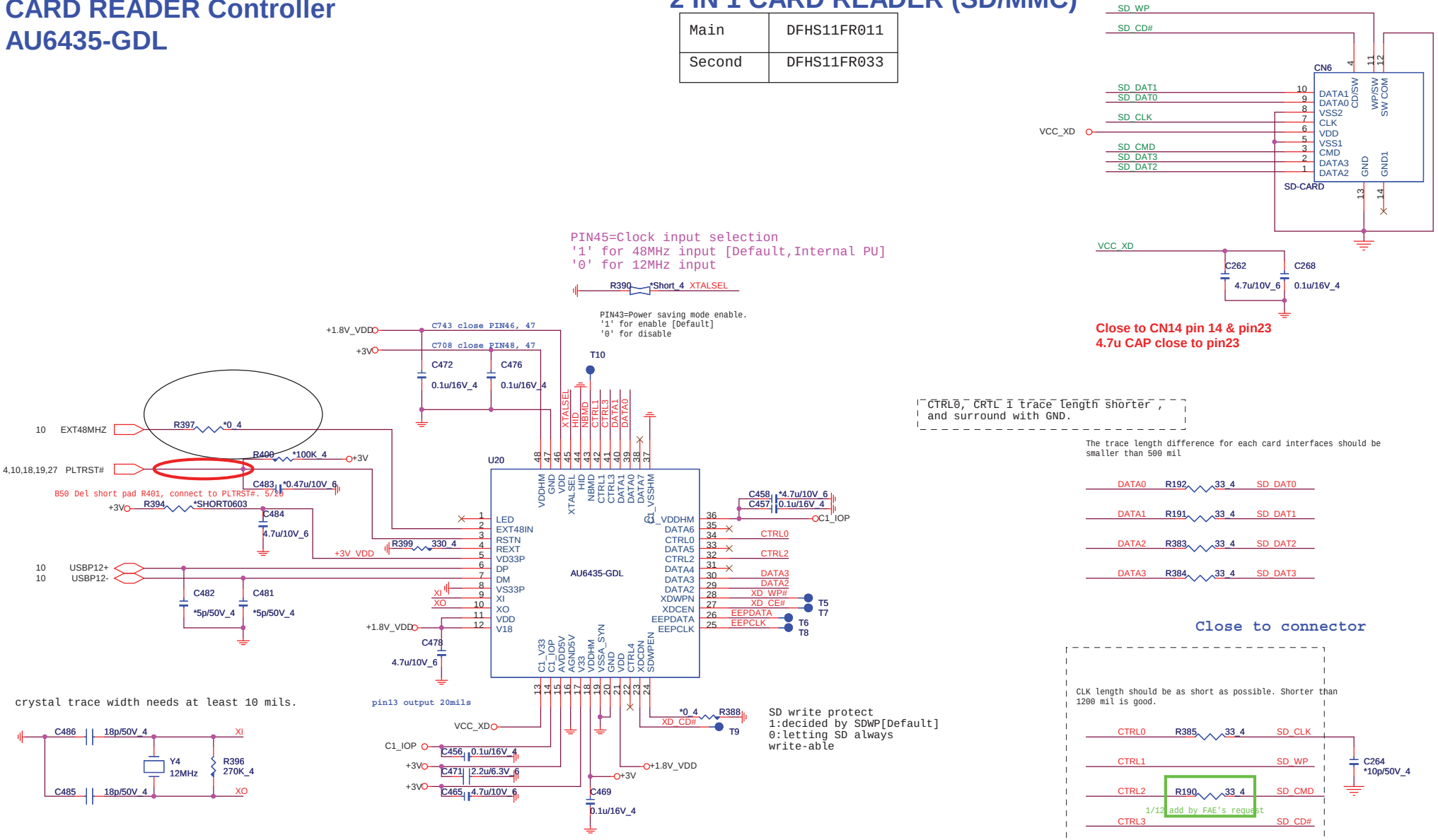
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | AMP /AUDIO JACK CONN | 1A |
| Date: Monday, May 23, 2011 | Sheet 22 of 35 | |

# CARD READER Controller
# AU6435-GDL

## 2 IN 1 CARD READER (SD/MMC)

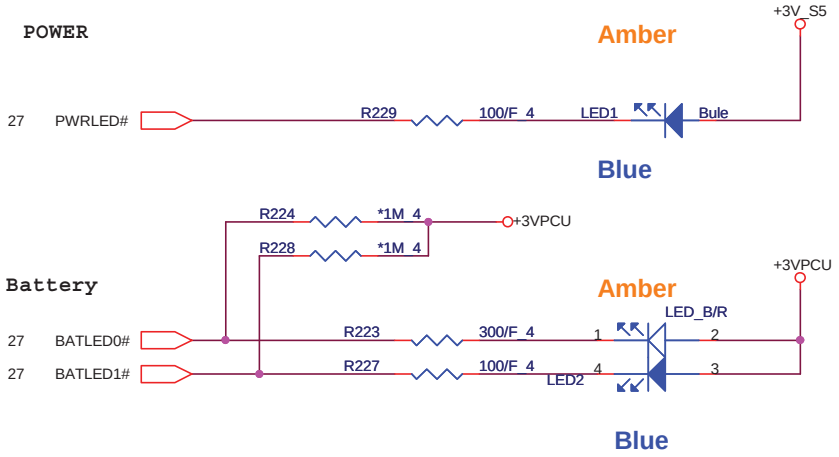
| | |
|---|---|
| Main | DFHS11FR011 |
| Second | DFHS11FR033 |




**PROJECT : ZQ5**
Quanta Computer Inc.

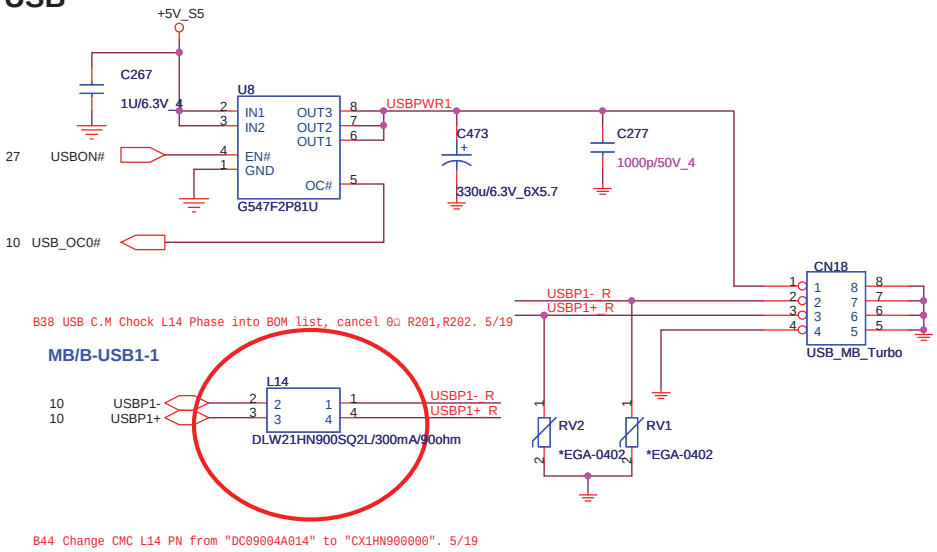
| Size | Document Number | Rev |
|---|---|---|
| | AU6433 CardReader | 1A |
| Date: Monday, May 23, 2011 | Sheet 23 of 43 | |

# LED

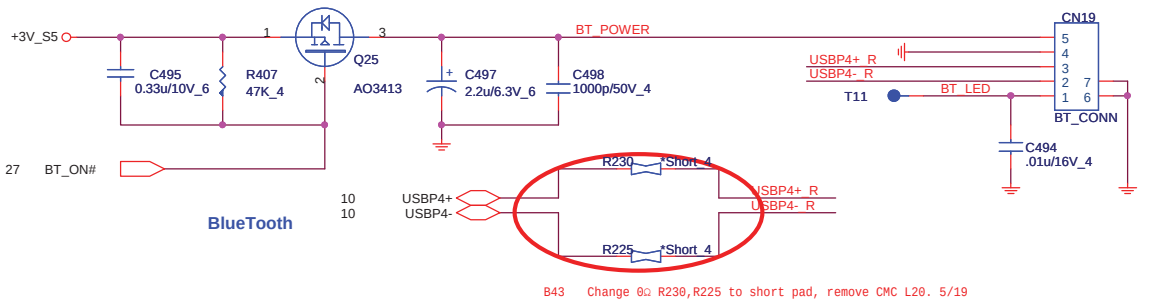



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQR | | |
| Size | Document Number: POWER/MMB/LAUNCH/LED | Rev: 1A |
| Date: Monday, May 23, 2011 | Sheet 24 of 35 | |

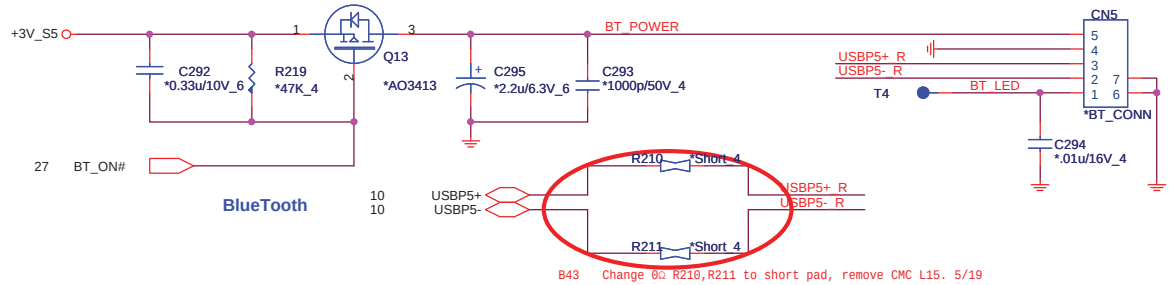
## USB



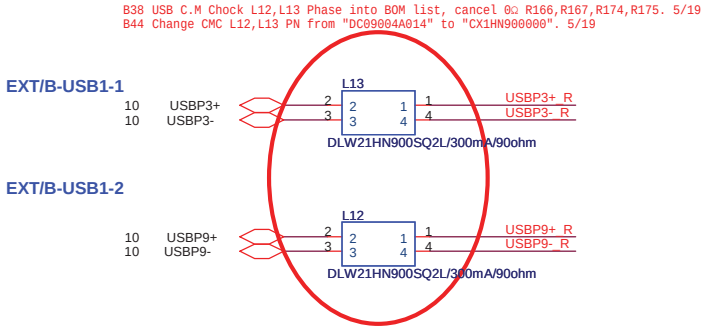

## BLUETOOTH CONNECTOR for 3.0

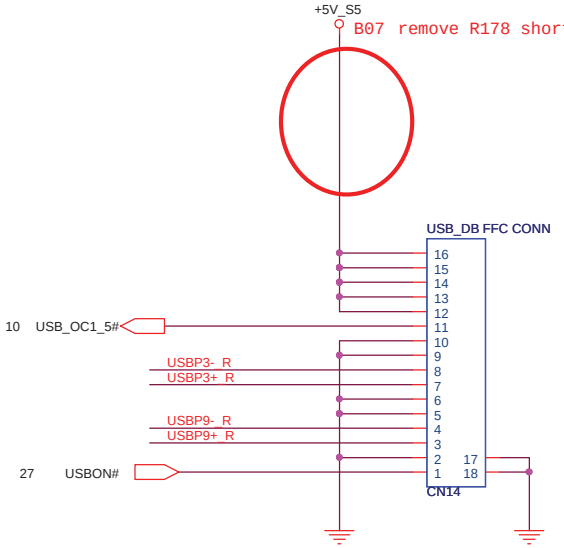



## Reserve




## USB/B

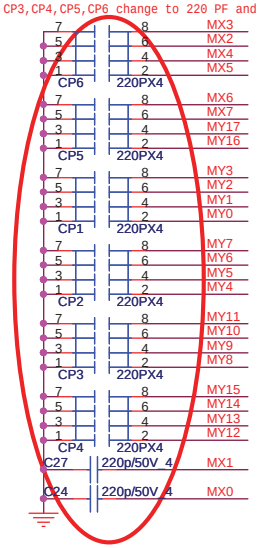


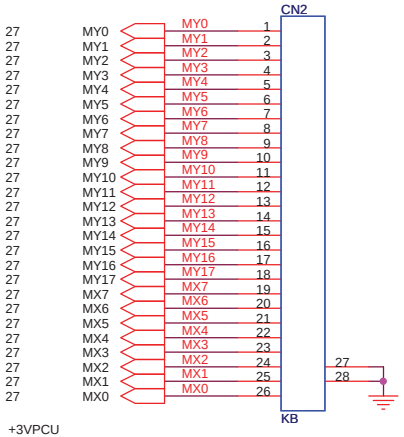



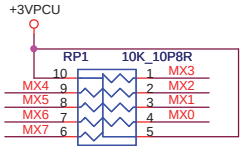

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQR | | |
| Size | Document Number: USB/ BT | Rev: 1A |
| Date: Monday, May 23, 2011 | Sheet 25 of 35 | |

## K/B

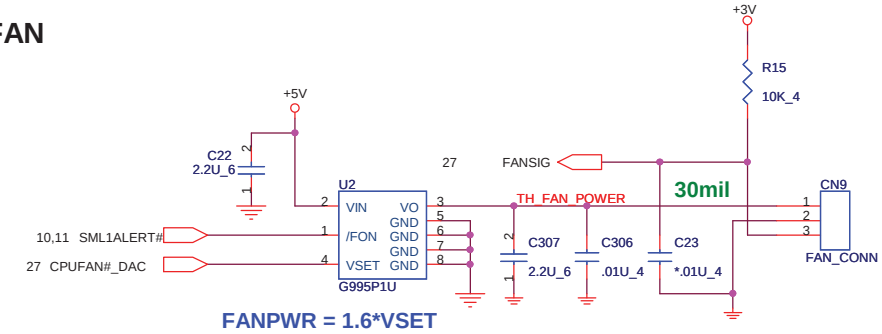
KB Cap CP1,CP2,CP3,CP4,CP5,CP6 change to 220 PF and phase into BOM list. 5/19
B33



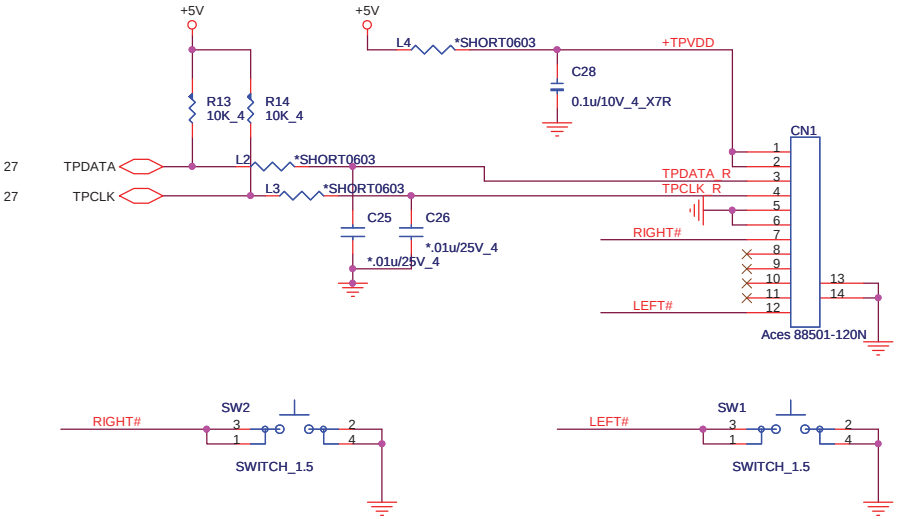




## CPU FAN

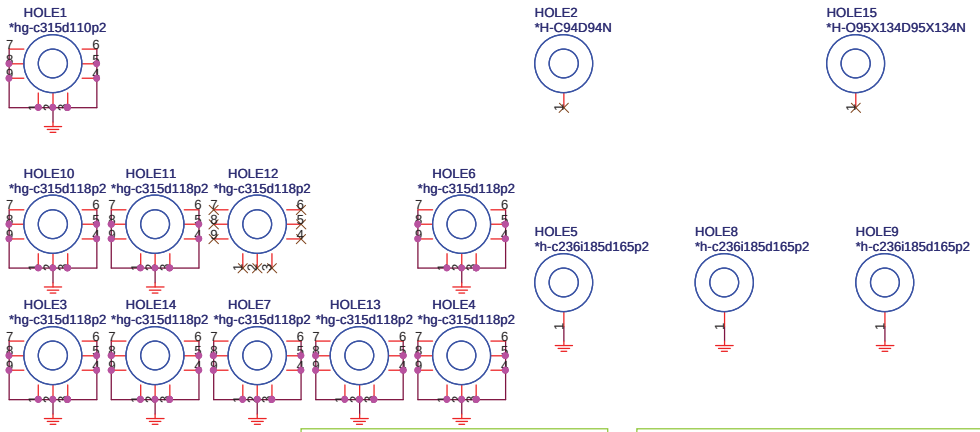



FANPWR = 1.6*VSET

## TOUCHPAD & Switch CONN.




## HOLE




Holex1 @ mini card

HOLE18
H-C197D87P2

Holex2 @PCH

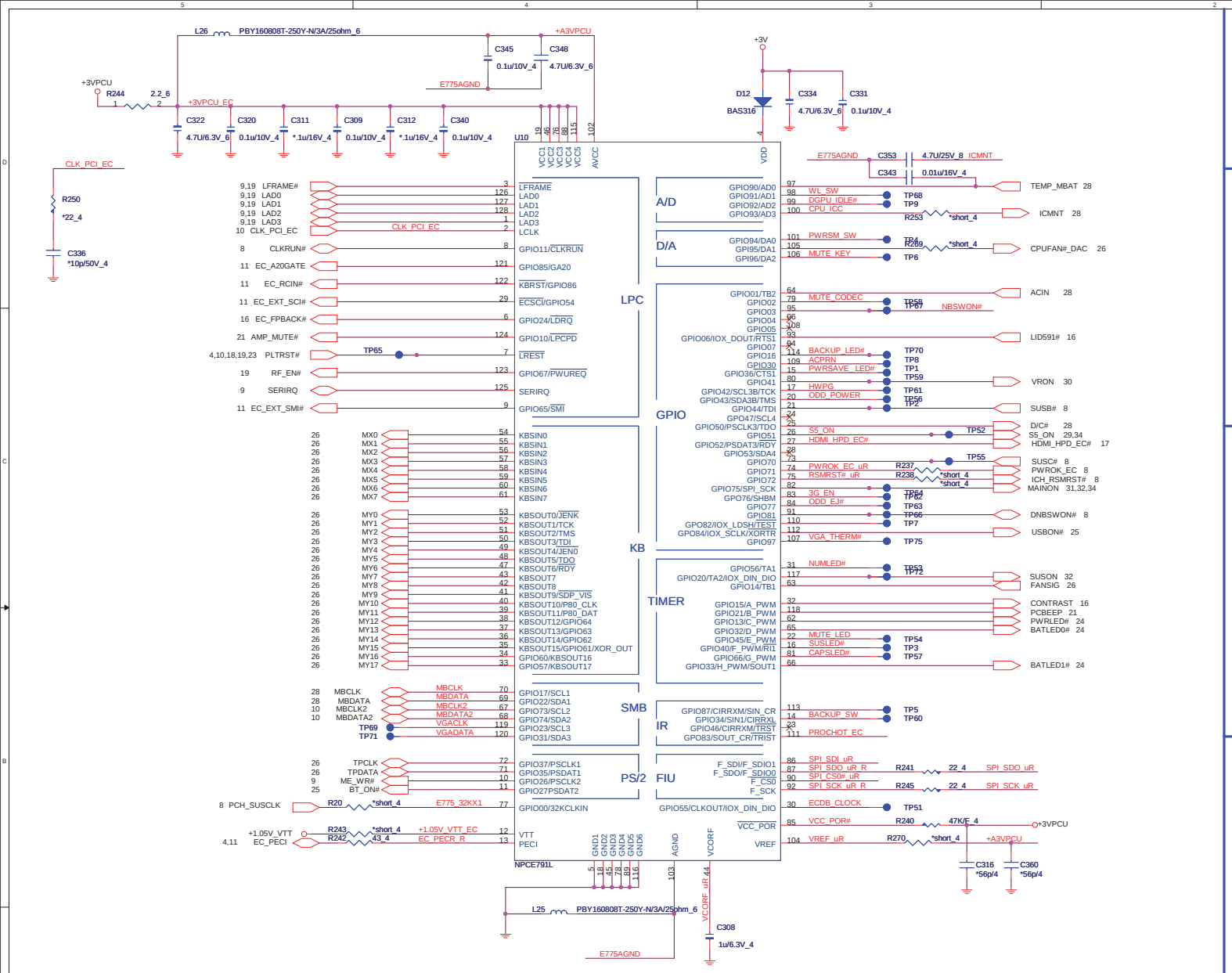
HOLE16
H-C228D142P2

HOLE17
H-C228D142P2

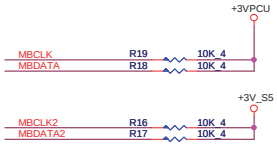
**Quanta Computer Inc.**

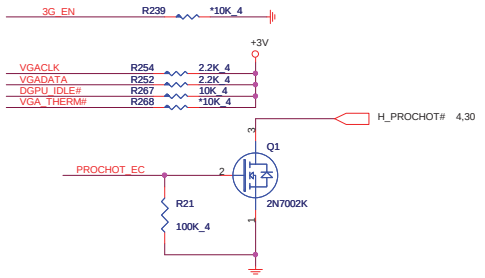
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | KB/FAN/TP+FP | 1A |
| Date: Monday, May 23, 2011 | Sheet 26 of 35 | |

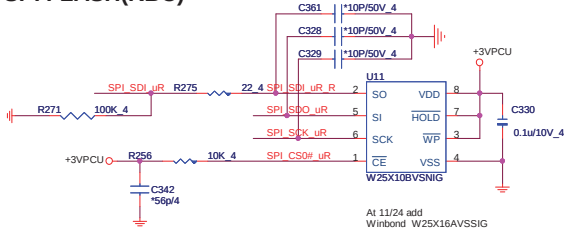



## SM BUS PU(KBC)



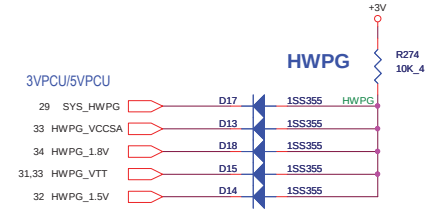




## SPI FLASH(KBC)

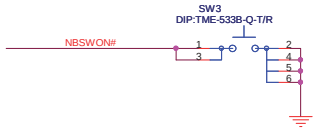



At 11/24 add
Winbond W25X16AVSSIG
AKE38ZP0N01
EON EN25F16-100HIP
AKE38ZA0Q00
AMIC A25L016
AKE38ZN0800

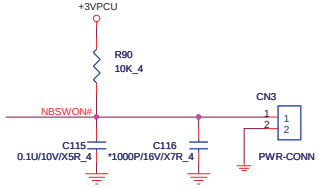
## HWPG(KBC)



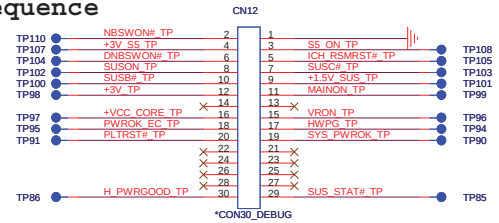

## POWER-ON Switch(KBC)




## PWR/B




## Power sequence

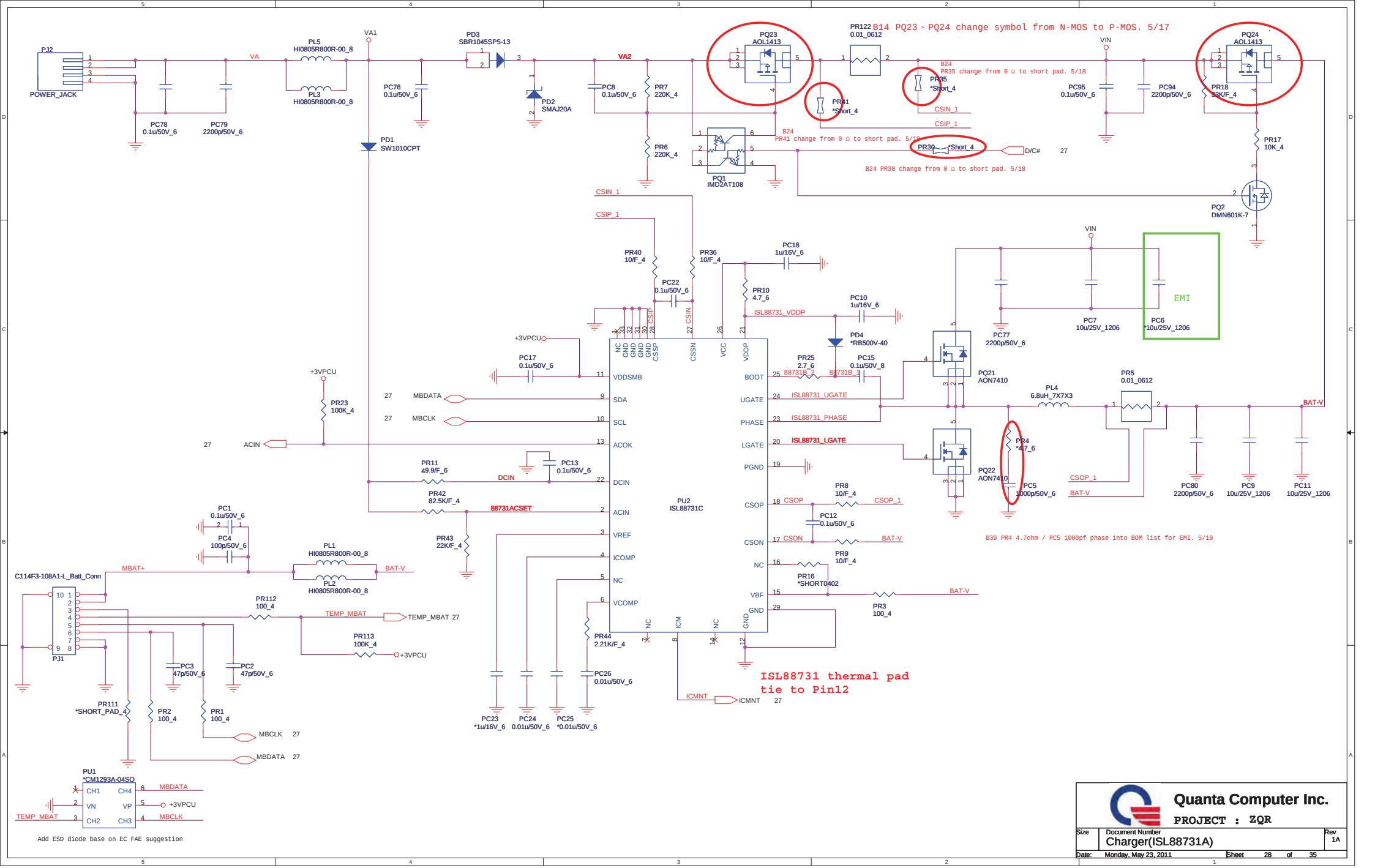




Quanta Computer Inc.
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | WPCE791 & FLASH | 1A |

Date: Monday, May 23, 2011 Sheet 27 of 35



MAIND → MAIND 6,32,34

SYS_SHDN# → SYS_SHDN# 4,34

Ven=7.23V

27 SYS_HWPG

B11 Del JP9, connect to VIN. 5/17

B11 Del JP10, connect to VIN. 5/17

B13
Del JP12, connect to +5VPCU. 5/17

B12 Del JP11, connect to +3VPCU. 5/17

Del net "+5VPCU_SRC". 5/17

B24
PR93 change from 0 Ω to short pad. 5/18

## +5VPCU
5 Volt +/- 5%
TDC : 4.125A
PEAK : 5.5A
OCP : 6.6A
Width : 170mil

## +3VPCU
3.3 Volt +/- 5%
TDC : 3.86A
PEAK : 5.15A
OCP : 6.2A
Width : 160mil

## OCP:6.6A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=6.6-(2.525/2)=5.34A
Vth=5.34A*14mOhm=0.07472mV
R(Ilim)=(74.72mV*10)/10uA
~74.723K

## OCP:6.2A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6.2-(1.9/2)=5.25A
Vth=5.25A*14mOhm=0.0735V
R(Ilim)=(73.5mV*10)/10uA
=73.5K

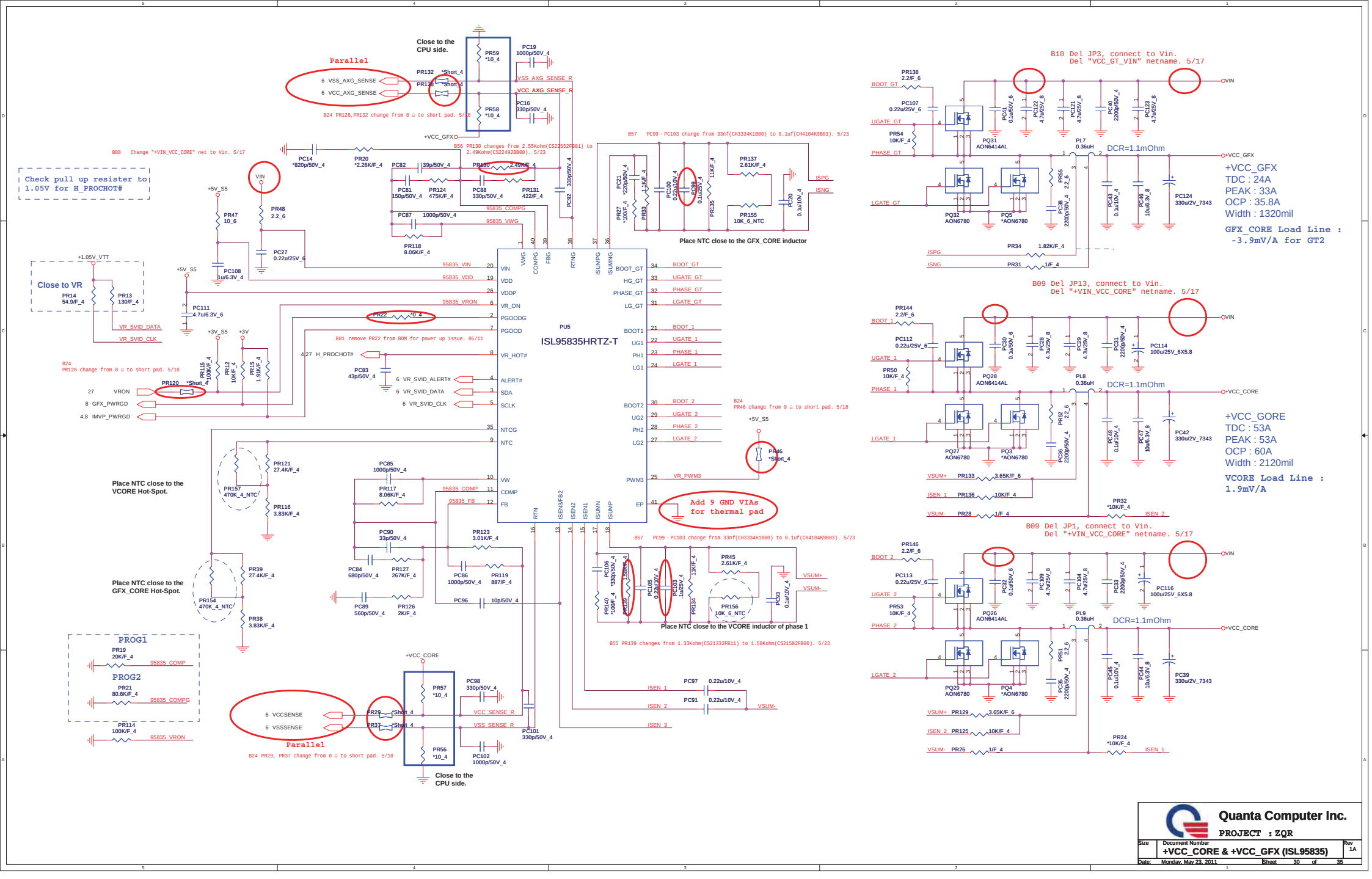
TDC : 2.25A
PEAK : 3A
Width : 100mil

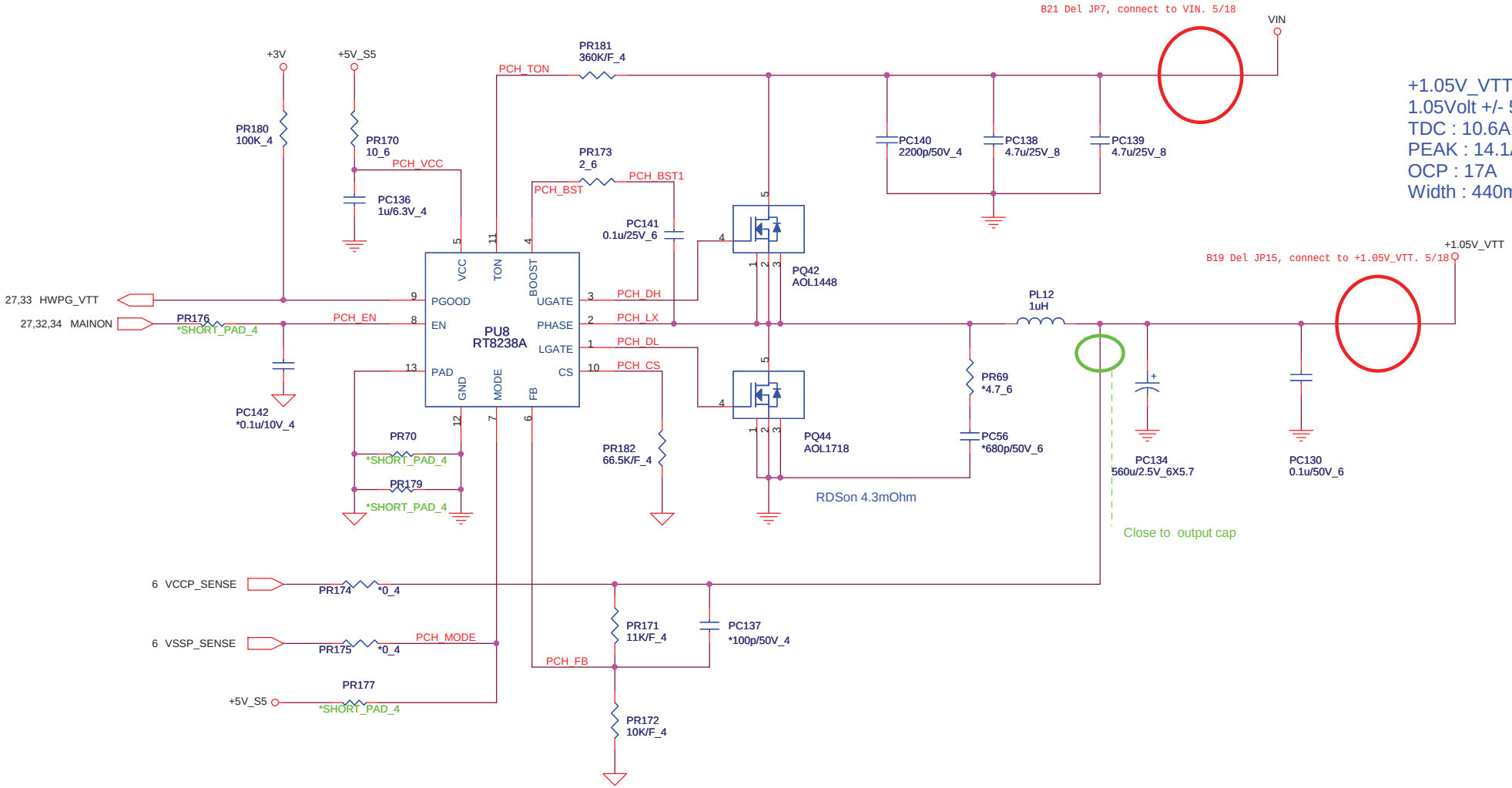
TDC : 1.88A
PEAK : 2.5A
Width : 80mil

TDC : 2.74A
PEAK : 3.65A
Width : 110mil

TDC : 0.16A
PEAK : 0.21A
Width : 10mil

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQR | | |
| Size | Document Number: SYSTEM 5V/3V (RT8223M) | Rev: 1A |
| Date: Monday, May 23, 2011 | Sheet 29 of 35 | |





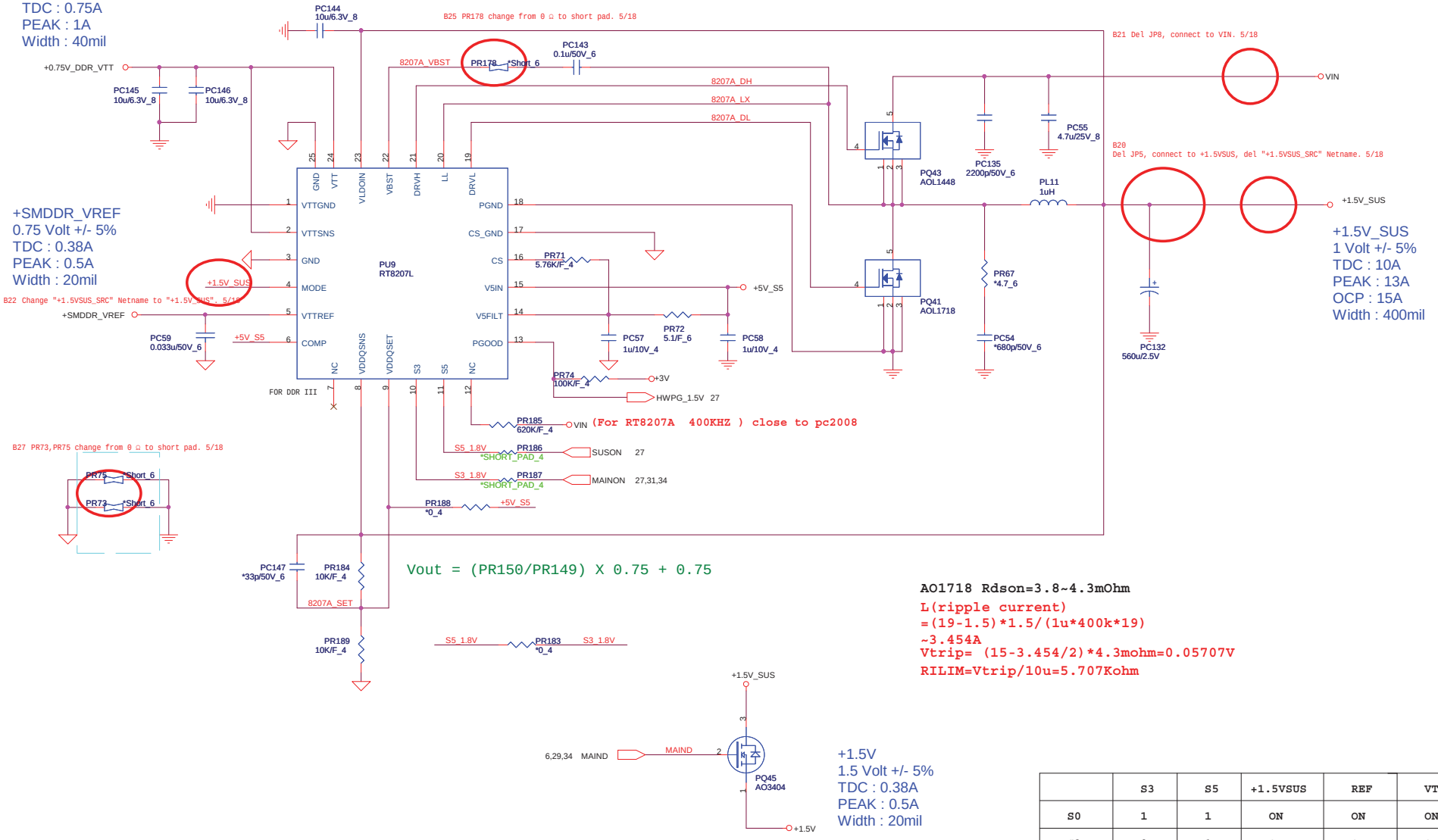

Ton=(8.8p*360K*1.05)/19-0.5=179.81ns
Lcurrent=(19-1.05)*179ns/1uH=3.228A
Iocp=17-3.228/2=15.386A
Vcs=15.386*4.3mohm=0.06616V
Rcs=0.06616/1u=66.16Kohm

VOUT=(1+R1/R2)*0.5

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZQR | | |
| Size | Document Number: +PCH&VTT (RT8238A) | Rev: 1A |
| Date: Monday, May 23, 2011 | Sheet 31 of 35 | |

+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil




+1.5V_SUS
1 Volt +/- 5%
TDC : 10A
PEAK : 13A
OCP : 15A
Width : 400mil

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (15-3.454/2)*4.3mohm=0.05707V
RILIM=Vtrip/10u=5.707Kohm

+1.5V
1.5 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil

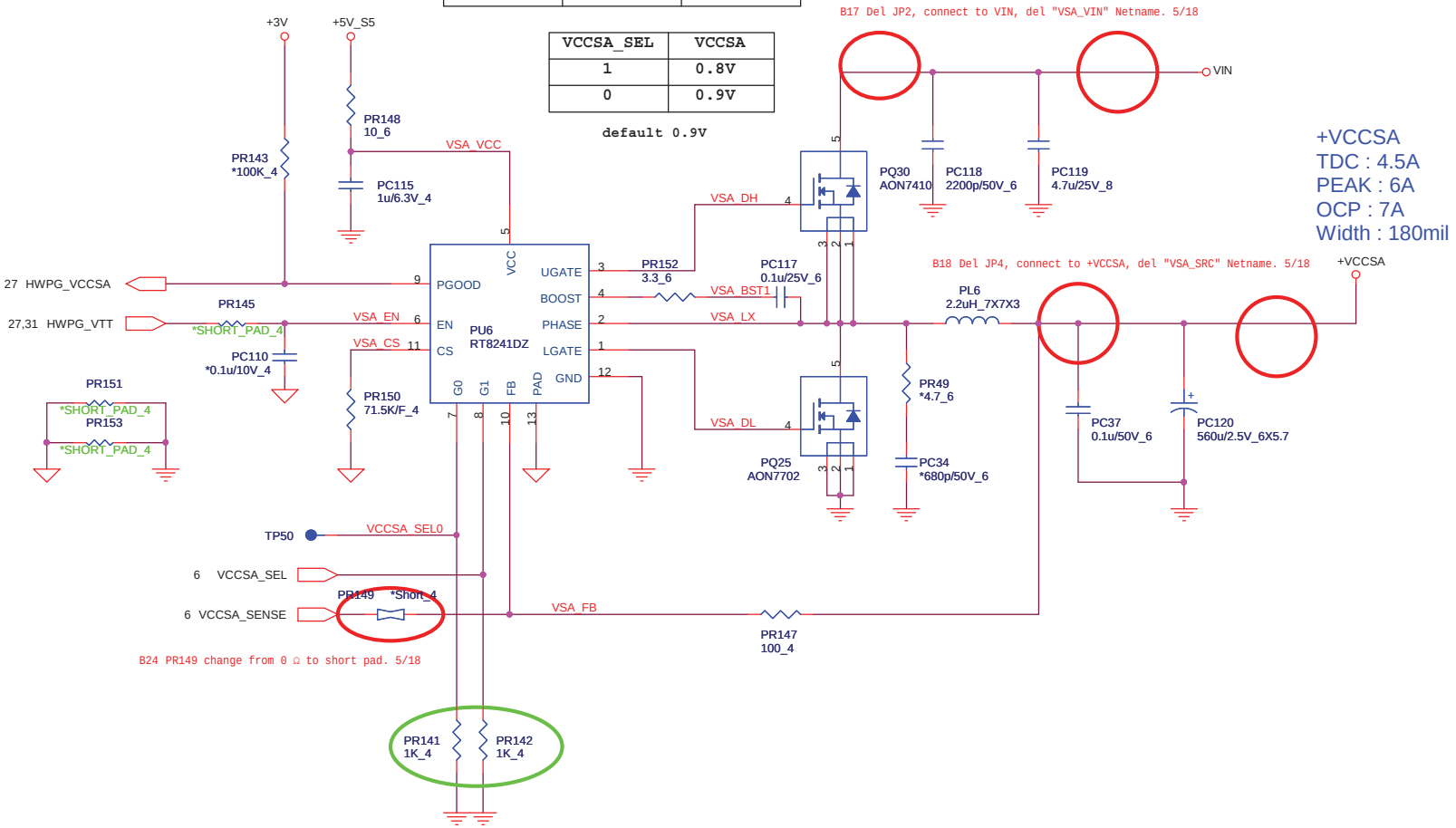
| | S3 | S5 | +1.5VSUS | REF | VTT |
|---|---|---|---|---|---|
| S0 | 1 | 1 | ON | ON | ON |
| S3 | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |

Quanta Computer Inc.
PROJECT : ZQR
Size | Document Number: DDR 1.5V(RT8207A) | Rev 1A
Date: Monday, May 23, 2011 | Sheet 32 of 35

| G0 | G1 | VCCSA |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

| VCCSA_SEL | VCCSA |
|---|---|
| 1 | 0.8V |
| 0 | 0.9V |

default 0.9V

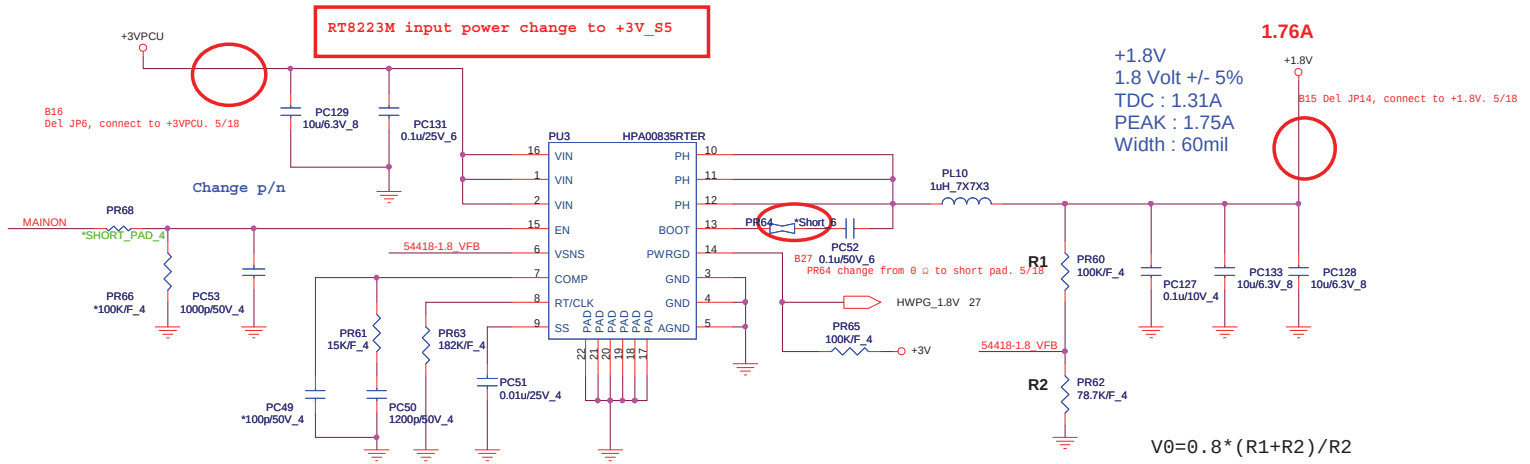



+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

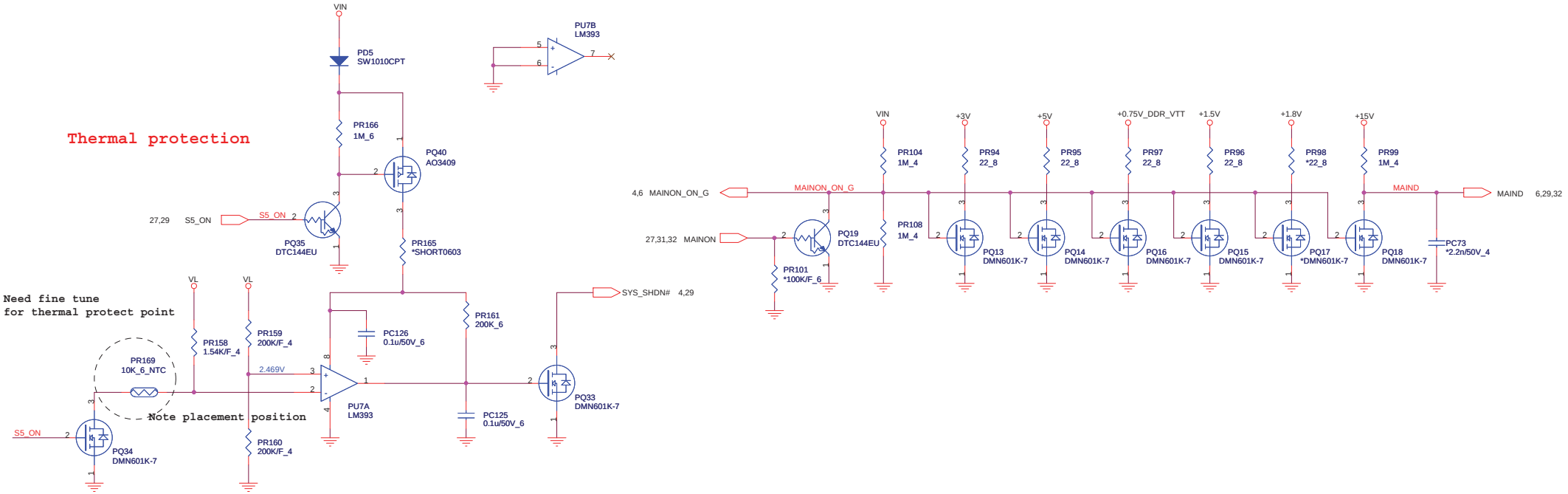
OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

**Quanta Computer Inc.**
PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | +VCCSA(RT8241A) | 1A |
| Date: Monday, May 23, 2011 | Sheet 33 of 35 | |




For EC control thermal protection (output 3.3V)




Quanta Computer Inc.

PROJECT : ZQR

| Size | Document Number | Rev |
|---|---|---|
| | Discharge/1.8V) | 1A |

Date: Monday, May 23, 2011 Sheet 34 of 35

1 7/7 modify

Model

ZQR MB

| REV | CHANGE LIST |
|---|---|
| B | 2011/05/11<br>B01 remove PR22 from BOM for power up issue.<br>B02 L5,L8,L10 Change PN to CX8BA470003.<br><br>2011/05/16<br>B03 Change net closed to Audio Codec PCBEEP netname to BEEP_2<br><br>2011/05/17<br>B04 Change L6,L7,L9 to 0Ω, remove C76,C96,C121 for CRT Test.<br>B05 Add R409, remove U5, C142 for saving cost.<br>B06 Change Bottom side 0Ω to short pad for cost and SMT cycle time issue;<br>R284,R295,R296,R392,R395,R401,R402,R403,R404,R408.<br>B07 Remove R178 short pad, connect to +5V_S5.<br>B08 Change "+VIN_VCC_CORE" net to Vin.<br>B09 Del JP1,JP13, connect to Vin, del "+VIN_VCC_CORE" netname.<br>B10 Del JP3, connect to Vin. Del "VCC_GT_VIN" netname.<br>B11 Del JP9,JP10 connect to Vin.<br>B12 Del JP11, connect to +3VPCU.<br>B13 Del JP12, connect to +5VPCU.<br>B14 PQ23、PQ24 change symbol from N-MOS to P-MOS<br><br>2011/05/18<br>B15 Del JP14, connect to +1.8V.<br>B16 Del JP6, connect to +3VPCU.<br>B17 Del JP2, connect to VIN, del "VSA_VIN" Netname.<br>B18 Del JP4, connect to +VCCSA, del "VSA_SRC" Netname.<br>B19 Del JP15, connect to +1.05V_VTT.<br>B20 Del JP5, connect to +1.5VSUS, del "+1.5VSUS_SRC" Netname.<br>B21 Del JP7,JP8 connect to VIN.<br>B22 Change "+1.5VSUS_SRC" Netname to "+1.5V_SUS".<br>B23 Mount C70, C71 for +Vcc_core overshoot issue.<br>B24 PR29,PR30,PR35,PR37,PR41,PR46,PR93,PR120,PR128,PR132,PR149(0_4) change from 0ohm to short-pad.<br>B25 PR178(0_6) change from 0ohm to short-pad.<br>B26 R114,R197,R206(0_4) change from 0ohm to short-pad.<br>B27 L11,PR64,PR73,PR75,R96,R97,R98,R99,R133,R168(0_6) change from 0ohm to short-pad.<br><br>2011/05/19<br>B28 Page 20 +1.5V_SUS mount C149,C182,C160,C175,C249,C250,C257,C445,C444 Cap for EMI<br>B29 Page 20 +3V C347,C341,C55,C303,C449,C275,C453,C459 Change to 100PF for EMI.<br>B30 Page 20 +5V C496,C437,C460,C232,C304,C454 change 100PF for EMI.<br>B31 Page 20 +5V_S5 C489,C289 change 100PF for EMI.<br>B32 Page 20 +VCC_CORE C47 change 100PF for EMI.<br>B33 KB Cap CP1,CP2,CP3,CP4,CP5,CP6 change to 220 PF and phase into BOM list for EMI.<br>B34 BOT layer +VCC_GFX add 100pf x 3 C499,C500,C501 for EMI.<br>B35 BOT layer +1.8V Add 100pF X2 C502,C503 for EMI.<br>B36 TOP layer +1.8V Add 100pF X2 C506,C507 for EMI.<br>B37 TOP layer +1.5V Add 100pF X2 C504,C505 for EMI.<br>B38 USB C.M Chock L12,L13,L14 Phase into BOM list, cancel 0Ω R166,R167,R174,R175,R201,R202 for EMI.<br>B39 PR4 4.7ohm / PC5 1000pf phase into BOM list for EMI.<br>B40 Change R386 from 22Ω to short pad.<br>B41 Add a MOSFET Q26,R410,R412 to separate CODE SYNC and PCH Strap signal to avoid leakage issue.<br>B42 Change R216,R221 from 56Ω to 47Ω for ACER SPEC.<br>B43 Change 0Ω R5,R6,R210,R211,R225,R230 to short pad, remove CMC L1,L15,L20 for SMT.<br>B44 Change CMC L12,L13,L14 PN from "DC09004A014" to "CX1HN900000".<br>B45 Remove C315 for cost issue.<br><br>2011/05/20<br>B46 R392,R197 change from short pad to 0Ω.<br>B47 Del short pad R114, connect to PCIE_CLKREQ_LAN#.<br>B48 Del short pad R206, connect to MIC1-VREFO-L.<br>B49 Del short pad R284, connect to ME_WR#.<br>B50 Del short pad R401, connect to PLTRST#.<br>B51 Del short pad R403, connect to HP_MUTE#.<br>B52 Del short pad R386, del netname ACZ_SDIN0_R, connect to ACZ_SDIN0.<br>B53 Del short pad R133,R168, connect to GND.<br>B54 Del C442.<br><br>2011/05/23<br>B55 PR139 changes from 1.33Kohm(CS21332FB11) to 1.58Kohm(CS21582FB00).<br>B56 PR130 changes from 2.55Kohm(CS22552FB01) to 2.49Kohm(CS22492BB00).<br>B57 PC99、PC103 change from 33nf(CH3334K1B00) to 0.1uf(CH4104K9B03). |
| 3C | |

Quanta Computer Inc.

PROJECT : ZQR

Size: Document Number: Change list — Rev: 1A

Date: Monday, May 23, 2011 — Sheet 35 of 35

| DOC NO. | | | | | |
|---|---|---|---|---|---|
| PROJECT MODEL : | ZQR | APPROVED BY: | | DATE: | 2011/05/09 |
| PART NUMBER: | | DRAWING BY: | | REVISON: | 1A |