MODEL:	REV:	CHANGE LIST:
Z01 MotherBoard	1A	FIRST RELEASE
	1B	PAGE02. 1. R447,455,456 MODIFY to EP P/N:CS14752FB11 PAGE03. 1. STUFF HOLE6 P/N:FBZ01007010 , 2. STUFF HOLE7,8,15 P/N:FBED8001016 , 3. STUFF HOLE5 P/N:FBZ01006010 PAGE03. 1. STUFF HOLE23,25 P/N:FBZ01003010 , 2. STUFF HOLE18 P/N:FBZ01004010 , 3. STUFF HOLE31 P/N:FBZ01005010 PAGE05. 1. U22 MODIFY to GM965 P/N:AJ0QN120f04 , 2. R193,194 MODIFY to EP P/N:CS03902FB11 PAGE06. 1. R242 MODIFY to EP P/N:CS33002JB23 PAGE08. 1. L52,53 MODIFY to EP P/N:CV01004KN00 PAGE11. 1. R332 MODIFY to EP P/N:CS23243F930 , 2. U6 MODIFY to ICH8 P/N:AJ0QM740T03 PAGE12. 1. R244,R347,R353 MODIFY to EP P/N:CS00004JA40 , 2. L28 MODIFY to P/N:CV-1005MZ01 PAGE13. 1. CN10 MODIFY to CRT P/N:DFDS15FR611 PAGE15. 1. R467 MODIFY to EP P/N:CS00004JA40,2. R50 MODIFY to EP P/N:CS31003J941,3.CN27 MODIFY to SATA P/N:DFHS22FR005 PAGE16. 1. CN16 MODIFY to RJ45/11 P/N:DFTJ15FR057 PAGE18. 1. R317,323 MODIFY to 0603 P/N:CS31003F949 , 2. R310 MODIFY to EP P/N:CS31003J941 PAGE20. 1. PR100 MODIFY to EP P/N:CS51002FB11 PAGE21. 1. PR86 MODIFY to EP P/N:CS24022FB13 , 2. PR38,82 MODIFY to 1% P/N:CS31002FB26 , 3. PR83 MODIFY to EP P/N:CS00004JA40 PAGE22. 1. PR1 MODIFY to EP P/N:CS32002FB29 , 2. PR6 MODIFY to 1% P/N:CS51003F934 PAGE23. 1. PR106 MODIFY to 0 ohm P/N:CS00002JB38 , 2. UN-STUFF PR107,PC111 PAGE24. 1. PR29 MODIFY to EP P/N:CS31003J941 2. PJ1 MODIFY to BATTERY P/N:DFHD07MR006 PAGE25. 1. PR70 MODIFY to EP P/N:CS32002FB29
	2A	PAGE02. 1. Connect VDDIO_CLK to +1.25V 2. un-stuff R292;R445;R308 3. stuff C575,C574,C576,C578,C573,C546 for EMI issue PAGE06. 1. Connect ICH_PWROK SIGNAL TO NB CLPWROK 2.un-stuff R242;R235;R422;R222;R421;R423 3. R360,R361 only stuff for UMA PAGE07. 1. MODIFY 22u to 10u PAGE08. 1. R489 MODIFY to 0805 2. Stuff L50;R182;C238 for EV@ (MXM) PAGE09. 1. Add PU for SMA_MA14 : SMB_MA14 PAGE10. 1. un-stuff R337,C115,C127,C129,C298,C302,C294,C283,C291 PAGE11. 1. Q18 MODIFY to P/N:AL07SZ04C27 2.R395 connect to VCCRTC 3.R336;R251;R419;R255 un-stuff 4.R226 connect to +3V_S5 5.ICH_PWROK to SB_CLPWROK PAGE11. 1. Stuff C500,C509,C300,C513 33pF P/N:CH03306JB04 2. C507,C508 10pF change to 15pF P/N:CH01506JB06 , 3. stuff R238,R392,C2989 for Contr-LINK1 PAGE12. 1. VCCHDA & VCCSUSHDA change to 3V PAGE13. 1. ADD CRT_DDC IN PU , 2. L8,L9,L10 P/N change to 0.47UH for MXM , 3. C22,C24,C25,C27,C31,C32 P/N change to 47pF for MXM PAGE14. 1. CN6 MODIFY CONN. to 5 PIN P/N:DFHD05MRD98 PAGE15. 1. MODIFY SWITCH BOARD PIN DEFINE 2. Modify FAN circuit , 2. MR1 P/N change to AL000268000 PAGE16. 1. C46,C47 27pF change to 33pF P/N:CH03306JB04 2. stuff C104,C105,C119,C112 0.1uF P/N:CH41003ZB35 PAGE17. 1. CARD READER COLAY TO CN28, DEL CN30 2. C311 change to 27pF P/N:CH02706JB06 3. stuff R209 4. un-stff R213,C325,U11 PAGE18. 1. CHANGE MDC & CODEC to 3V 2.Delete D12 3. stuff R314,R483,C393,C595 PAGE19. 1. SWAP NBSWON# & ACIN 2. C363,C364 5.6pF change to 18pF P/N:CH01806JB07 PAGE20. 1. Modify PQ19 P/N PAGE21. 1. Modify Capacitor P/N to meet ME height limit PAGE22. 1. stuff PR74,PC69 2. Remove JP Pad PAGE23. 1. stuff PR126,PC131,PC137 2. Remove JP Pad 3. un-stuff +1.8V PAGE25. 1. un-stuff PR101,PQ21,PR22,PQ2,PR26,PR9,PR5,PC33,PC38,PC39,PC19,PC22,PU2
	2B	PAGE02. 1. Change R293 to 2.2K for meet Intel Design checklist PAGE03. 1. Change XDP PU/PD resistors value to meet Intel Design checklist PAGE04. 1. Un-stuff C28,C457 PAGE05. 1. Add LVDS_VREF strap PAGE06. 1. Add SDVO_I2C strap PAGE07. 1. Remove NB resistors to GND PAGE08. 1. Remove DIODE for D27 2. Remove VCCA_DPLLA&B for external VGA PAGE10. 1. Add CRT & LVDS I2C Strap PAGE11. 1. Un-stuff Control Link Vref1 PAGE12. 1. Remove reserve ICH8 HDA 1.5V power rail PAGE13. 1. Modify LCD_VCC enable power rail 2. Add LVDS INV I2C Strap PAGE14. 1. Add EMI solution for debug port PCI clock PAGE15. 1. Change Q33,Q34 to MOSFET PAGE16. 1. Add PIN 59 & 3 PAGE18. 1. Change CN31 pin2 to +3V_S5 for Modem can't wake up from S3 PAGE19. 1. Add GPIO46 , 47 PAGE20~25. 1. Add EMI solution 2. Update Power component P/N
	3A	PAGE10. 1. Add +2.5V & +1.8V capacitors for nVIDIA MXM card PAGE11. 1. Change C507,C508 to 15pF for RTC PAGE13. 1. Add C609 & C610 to meet CM2009 specification PAGE14. 1. Reserve +5VPCU & Add Q40,R540 for CIR PAGE15. 1. Add C611 for PLC hall IC 2. Stuff R60 for G995 PAGE19. 1. CN24 un-stuff , 2. D322,D332 reserve for ESD PAGE21. 1. Modify PC85 value PAGE22. 1. Modify PR4,PC13 value for sequence PAGE23. 1. Add PQ22 for nVIDIA MXM +1.8V PAGE24. 1. Modify PF1 P/N PAGE25. 1. Add PU2 for nVIDIA MXM +2.5V
	3B	PAGE10. 1. Remove R337 & Add R542,Q41,Q42 for Nvidia ACIN function PAGE13. 1. Add D34~D36,D40 for ESD solution PAGE15. 1. R484,R485,R486 from 330 change to 220 ohm for LED light issue 2. Add D41,D42,D43 for ESD 3. Stuff Q39 PAGE16. 1. Add C621,C622 for EMI solution 2. C112,C119 change to 100pF/50V for EMI PAGE18. 1. Un-Stuff L55, Stuff U16,R470,R471 for internal Mic. issue PAGE19. 1. Modify D32,D33 package to 0402 for ESD PAGE23. 1. Add PR140,PR141 for +1.8V voltage PAGE25. 1. Stuff PR22,PR101,PQ2,PQ21 for nVIDIA MXM +1.8V & +2.5V Discharge

MODEL : Z01 MB

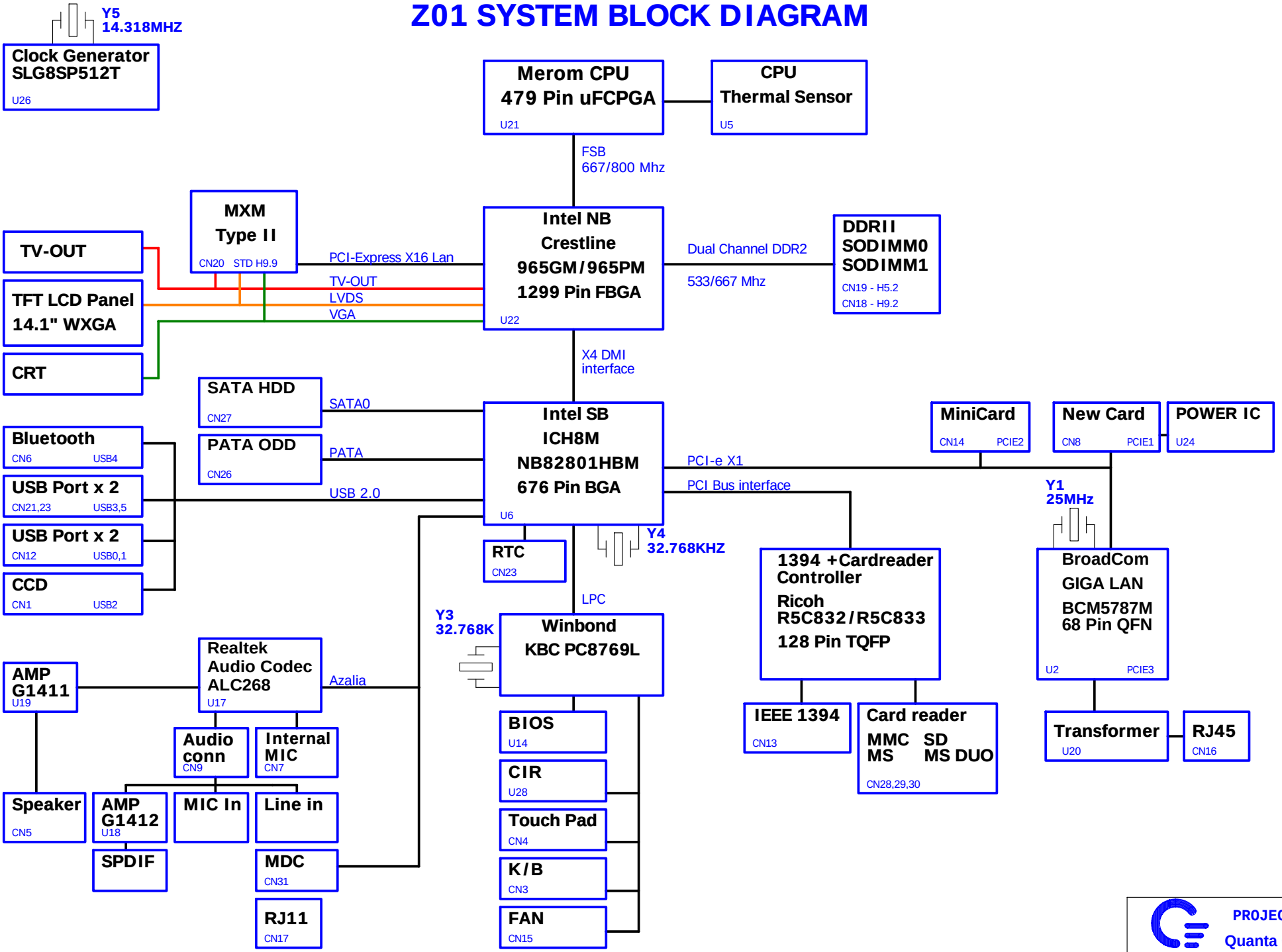
PAGE	FROM	TO
1	1A	
2	2B	
3	2B	
4	2B	
5	2B	
6	2B	
7	2B	
8	2B	
9	2A	
10	3A	3B
11	2B	
12	2B	
13	3A	3B
14	3A	
15	3A	3B
16	3A	3B
17	2A	
18	2B	3A
19	3A	3B
20	2B	
21	3A	
22	3A	
23	3A	3B
24	3A	
25	3A	3B

Quanta Computer Inc.

PROJECT : ZO1	APPROVE BY: JIM HSU	DRAWING BY:JACKY CHENG	REV 3A
MB ASSY'S P/N : 31Z01MB00XX	PROJECT LEADER: JIM HSU	DOCUMENT NO: 204	DATE :2007/04/14

COVER SHEET 1 OF 1

Z01 SYSTEM BLOCK DIAGRAM

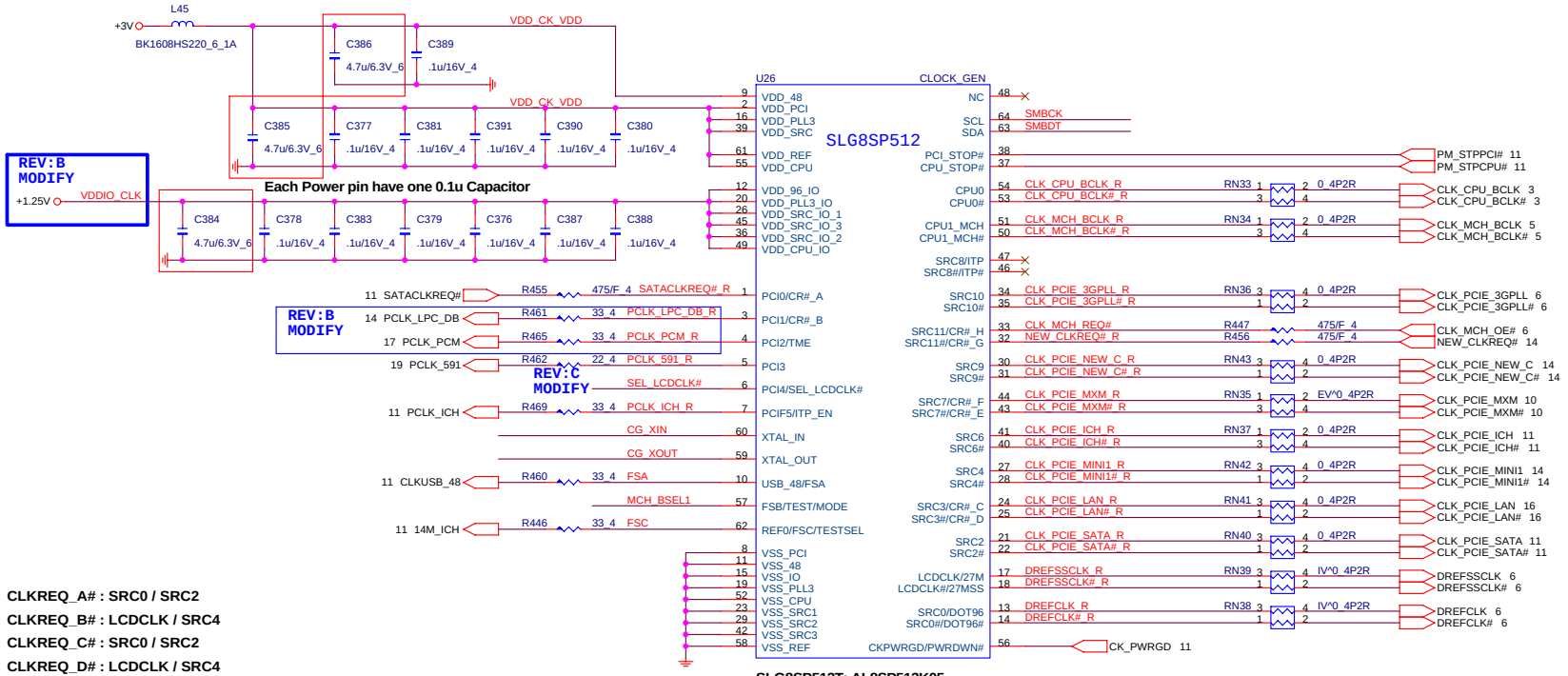


PROJECT : Z01

Quanta Computer Inc.

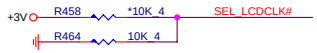
Size	Document Number	Rev
	Block Diagram	1A
Date: Thursday, May 17, 2007	Sheet 2 of 26	

Clock Generator



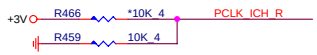
SLG8SP512T: AL8SP512K05

CLKREQ_A# : SRC0 / SRC2
CLKREQ_B# : LCDCLK / SRC4
CLKREQ_C# : SRC0 / SRC2
CLKREQ_D# : LCDCLK / SRC4
CLKREQ_E# : SRC6
CLKREQ_F# : SRC8
CLKREQ_G# : SRC9
CLKREQ_H# : SRC10



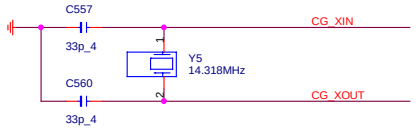
CK505
0 : Pin 37,38 as SRC5 output
1 : pin 37,38 as PCI_STOP# & CPU_STOP

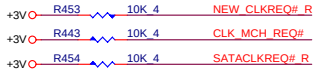
SILEGO
0 : Pin 13,14 & 17,18 for Internal VGA
1 : 27M & 27M_SS & SRC0 for external VGA



CK505
0 : Pin 46,47 as SRC output
1 : Pin 46,47 as CPU output

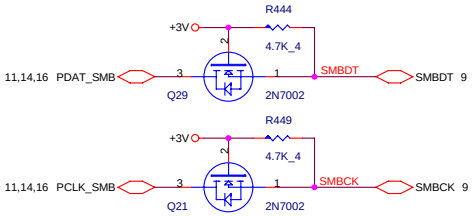
SILEGO
0 : Pin 46,47 as SRC output
1 : Pin 46,47 as CPU output



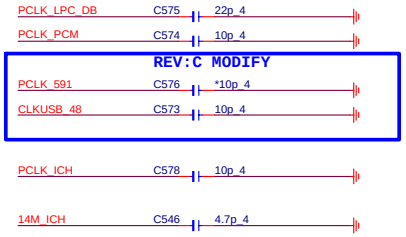


PU for ICS CLK GEN
0 : CPU & SRC overclock allow
1 : CPU & SRC overclock not allow

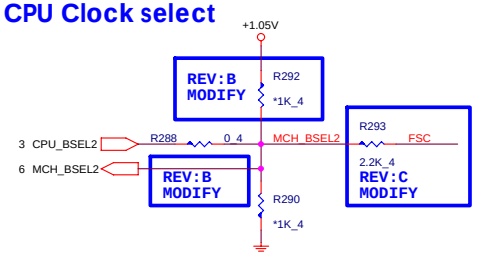
Clock Gen I2C

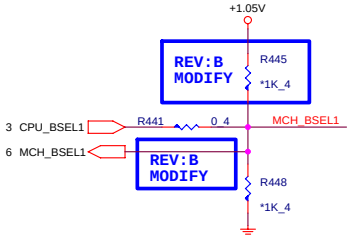


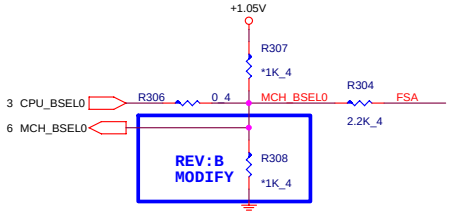
Reserved for EMI



CPU Clock select







BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	0	200Mhz
0	1	1	166Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved

PROJECT : ZO1
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	2B
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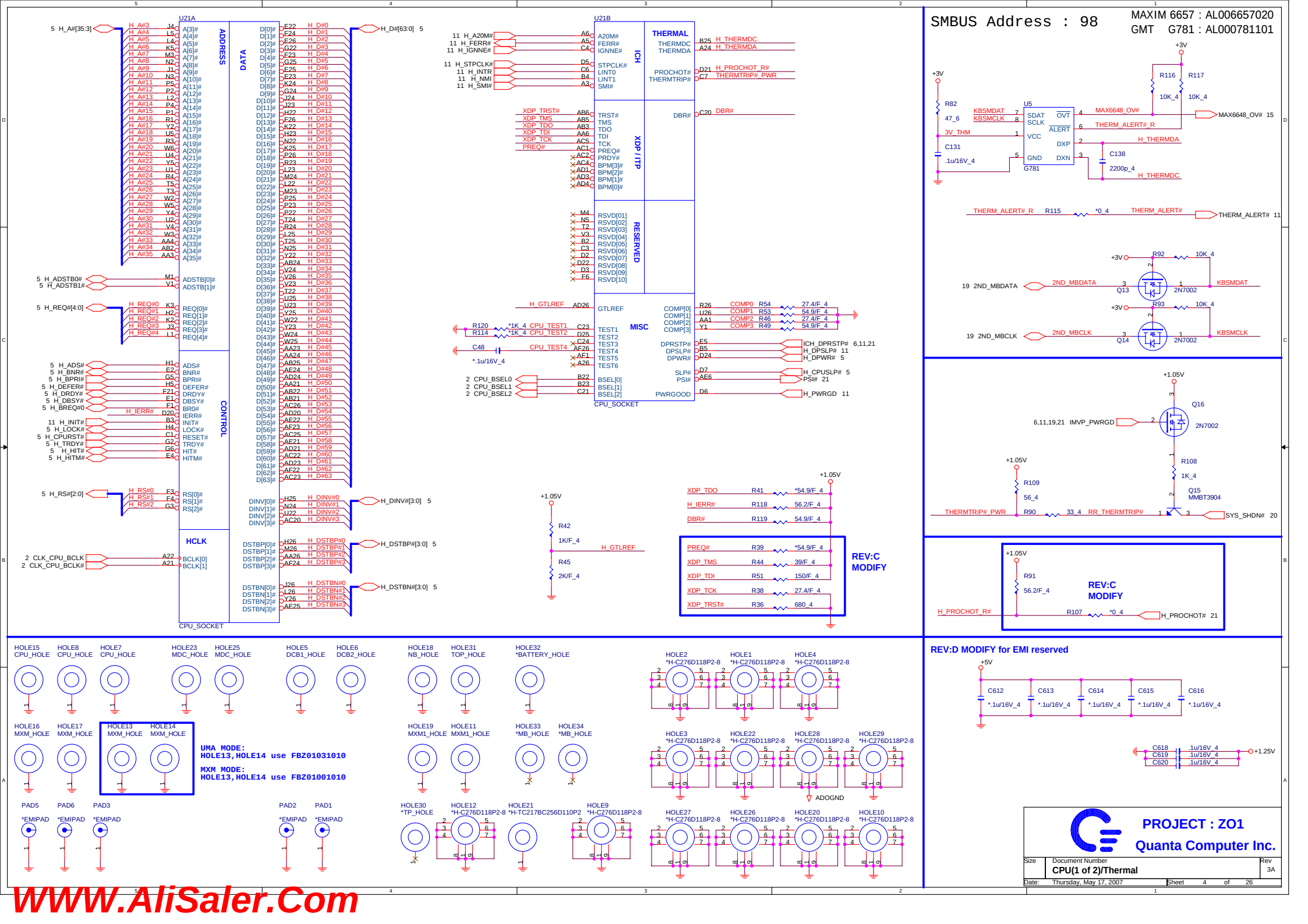
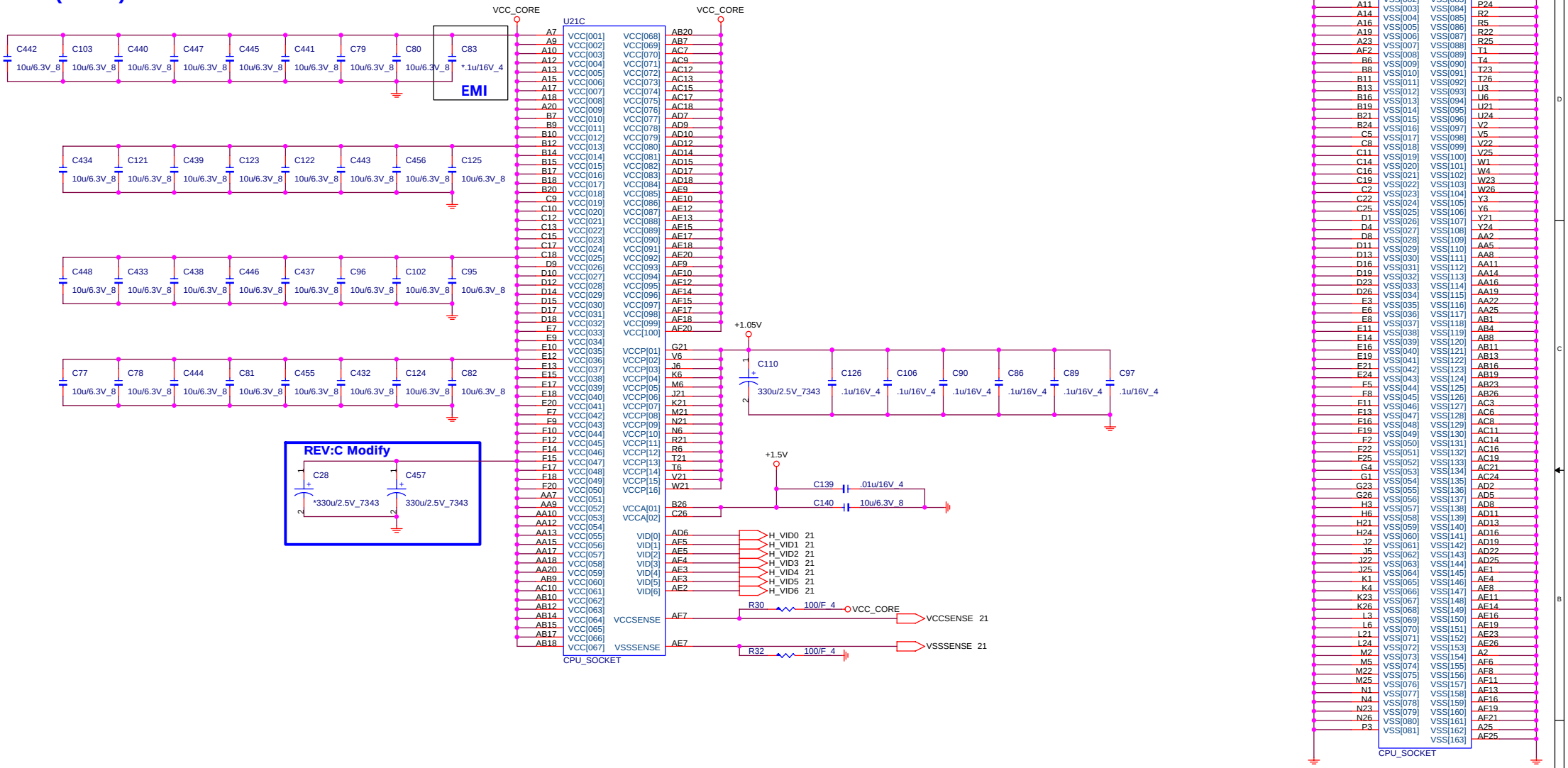

SMBUS Address : 98
MAXIM 6657 : AL006657020
GMT G781 : AL000781101
U21A
ADDRESS
DATA
CONTROL
HCLK
CPU_SOCKET
U21B
THERMAL
ICH
XDP / ITP
RESERVED
MISC
CPU_SOCKET
REV:C MODIFY
REV:C MODIFY
REV:D MODIFY for EMI reserved
UMA MODE: HOLE13,HOLE14 use FBZ01031010
MXM MODE: HOLE13,HOLE14 use FBZ01001010
ADOGND
PROJECT : ZO1
Quanta Computer Inc.
Document Number
CPU(1 of 2)/Thermal
Thursday, May 17, 2007
WWW.AliSaler.Com

CPU(Power)



PROJECT : ZO1

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(2 of 2)Power	2B
Date: Thursday, May 17, 2007	Sheet 5 of 26	

GM965 QN12 : AJ0QN120T04
PM965 QN14 : AJ0QN140T04

U22A

HOST

CRESTLINE

U22C

PCI-EXPRESS GRAPHICS SDVO

VGA

CRESTLINE

W: 10 mil

REV:C MODIFY

REV:B MODIFY

REV:C MODIFY

W: 10 mil / S: 20 mil

W: 10 mil / S: 20 mil

<check list>
For EV@
Connect to GND
CRT R/G/B
TV A/B/C
HSYNC/VSYNC

<check list>
For IV@
Connect to 150ohm:
CRT R/G/B
TV A/B/C
Connect to 30ohm:
HSYNC/VSYNC

0OHM (PD) FOR EV (TV)

0OHM (PD) FOR EV (RGB)

<check list & CRB>
For Calero : 1.5K
For Cresstline:2.4K

IV&EV Dis/Enable setting

<check list & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0

<FAE>
Flexible and safe

HVREF
Width : 20mil
Length < 100mil

REV:C MODIFY

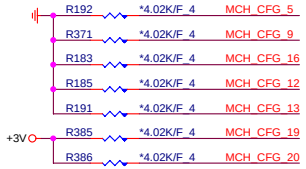
PROJECT : ZO1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST & GRAPHICS	2B

Date: Thursday, May 17, 2007 Sheet 6 of 26

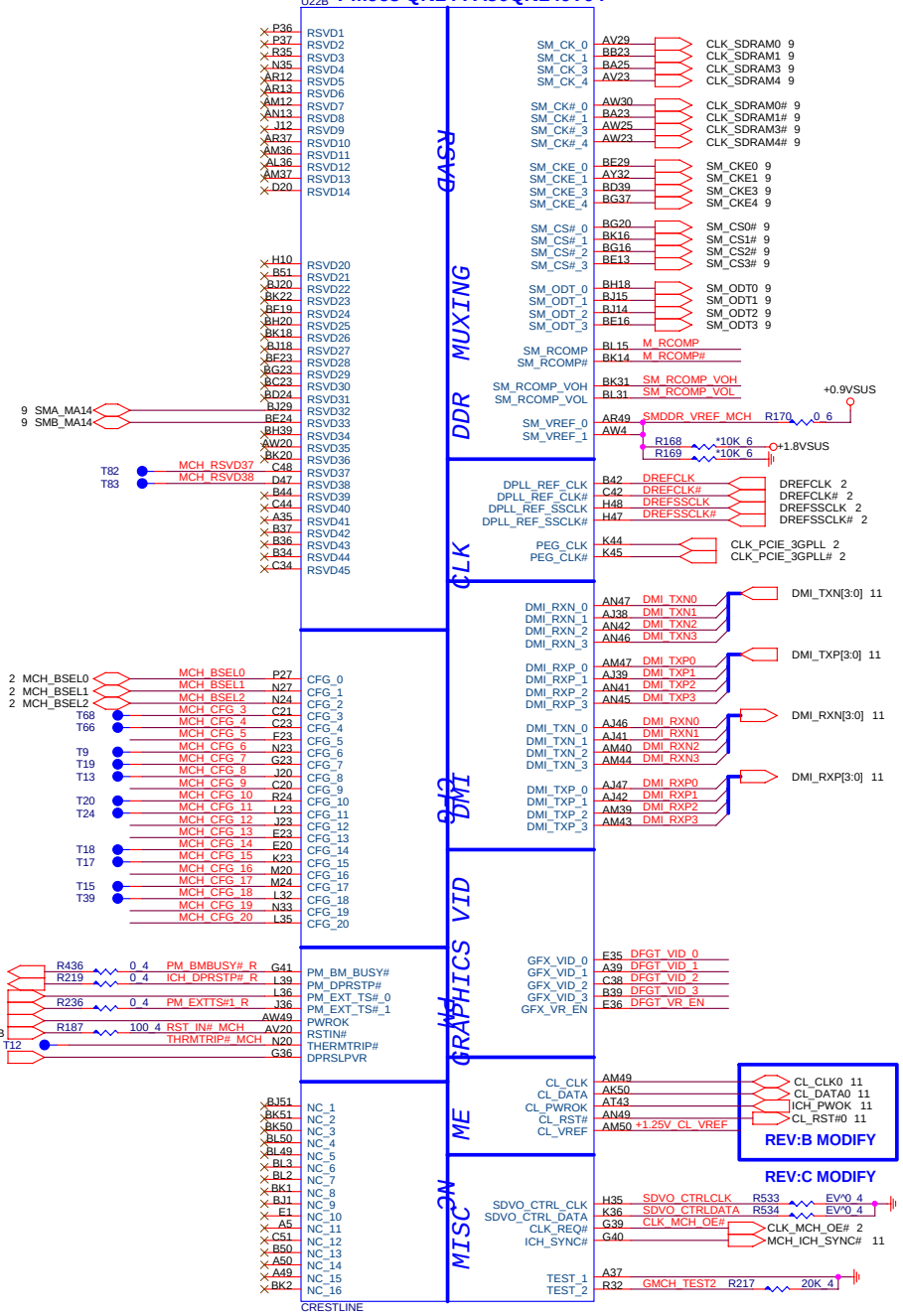
All strap are sampled with respect to the leading edge of the GMCH PWROK Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

CFG[2:0]	FSB Frequency Select	001 = FSB 533 MHz 010 = FSB 800 MHz 011 = FSB 667 MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG18	VCC select	0 = 1.05V (Default) 1 = 1.5V
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



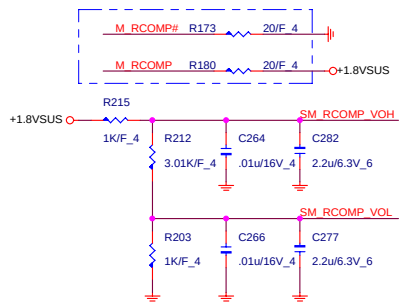
GM965 QN12 : AJ0QN120T04
PM965 QN14 : AJ0QN140T04

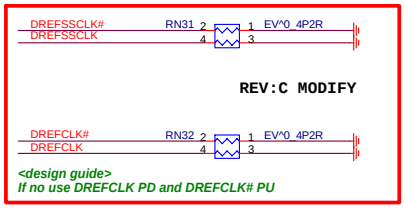
U22B

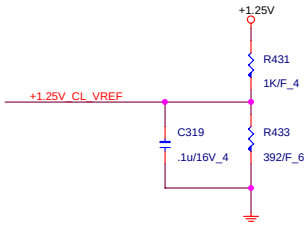


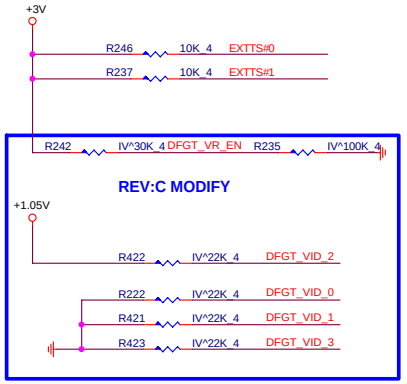
Width : 20mil
Length < 500mil

<check list & CRB>
R Value select
For Calero : 80.6ohm
For Cresstline:20ohm
But check list use 80.6ohm









PROJECT : ZO1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DMI & STRAP	2B
Date: Thursday, May 17, 2007	Sheet 7 of 26	

GM965 QN12 : AJ0QN120T04
PM965 QN14 : AJ0QN140T04

REV:C MODIFY
REV:B MODIFY
REV:B MODIFY

DDR SYSTEM MEMORY A
DDR SYSTEM MEMORY B
POWER
VSS
VSS
VSS_NCTF
VCC_NCTF
VSS_SCB
VCC_AXM_NCTF

CRESTLINE

PROJECT : ZO1
Quanta Computer Inc.
Size | Document Number: GMCH DDR & GND | Rev: 2B
Date: Thursday, May 17, 2007 | Sheet 8 of 26

GM965 QN12 : AJ0QN120T04
PM965 QN14 : AJ0QN140T04

REV:B MODIFY

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

CRT/TV Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL | INTERNAL

POWER

VCC CORE | VCC SM | VCC GFX NCTF | VCC GFX | VCC SM LF

REV:C MODIFY

REV:B MODIFY

Stuff 0 ohm for External VGA

CRESTLINE

VOUT = 1.25 (1+R1/R2)

	R1	R2
3.3V	33K	20K

2nd source : G923-330T1U AL000923003

SUSB# 11.19

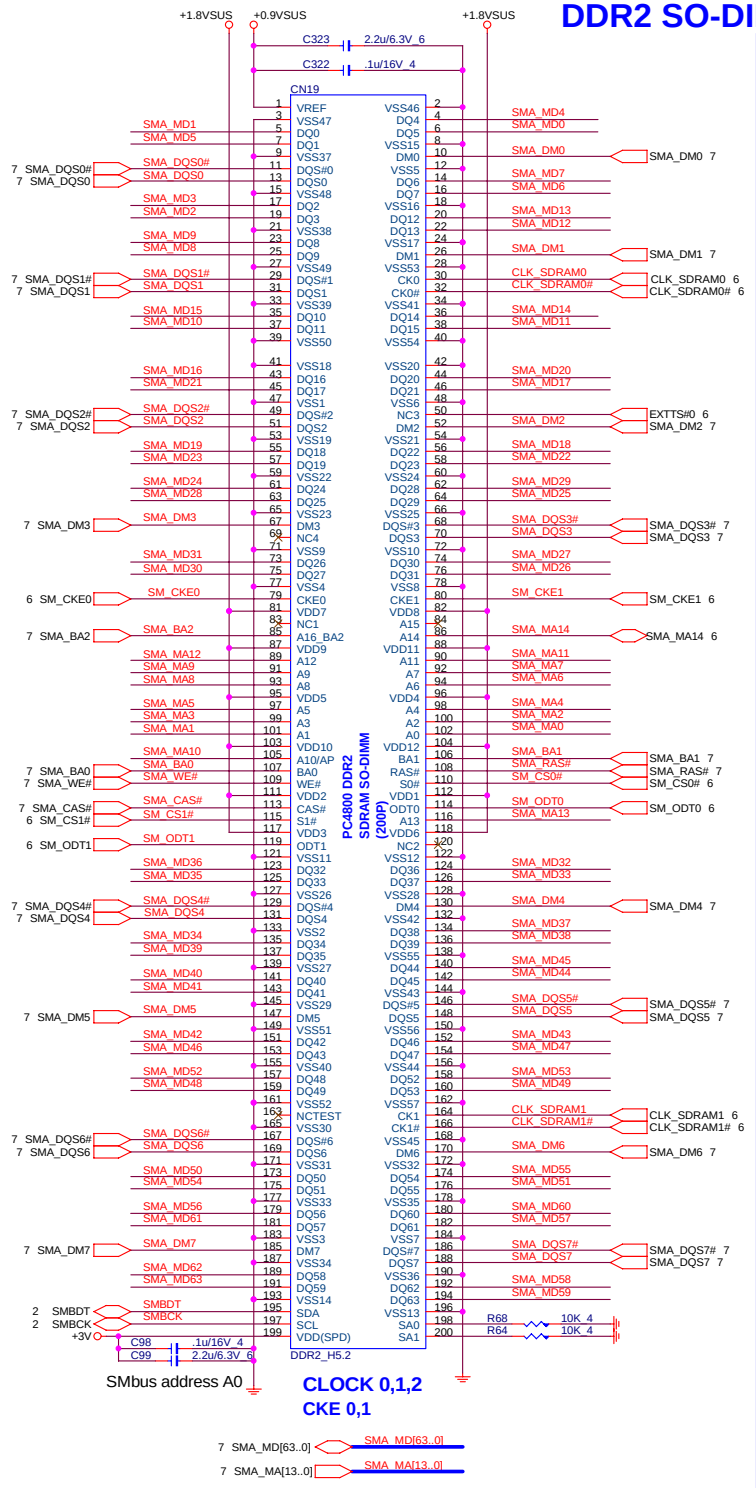
PROJECT : ZO1

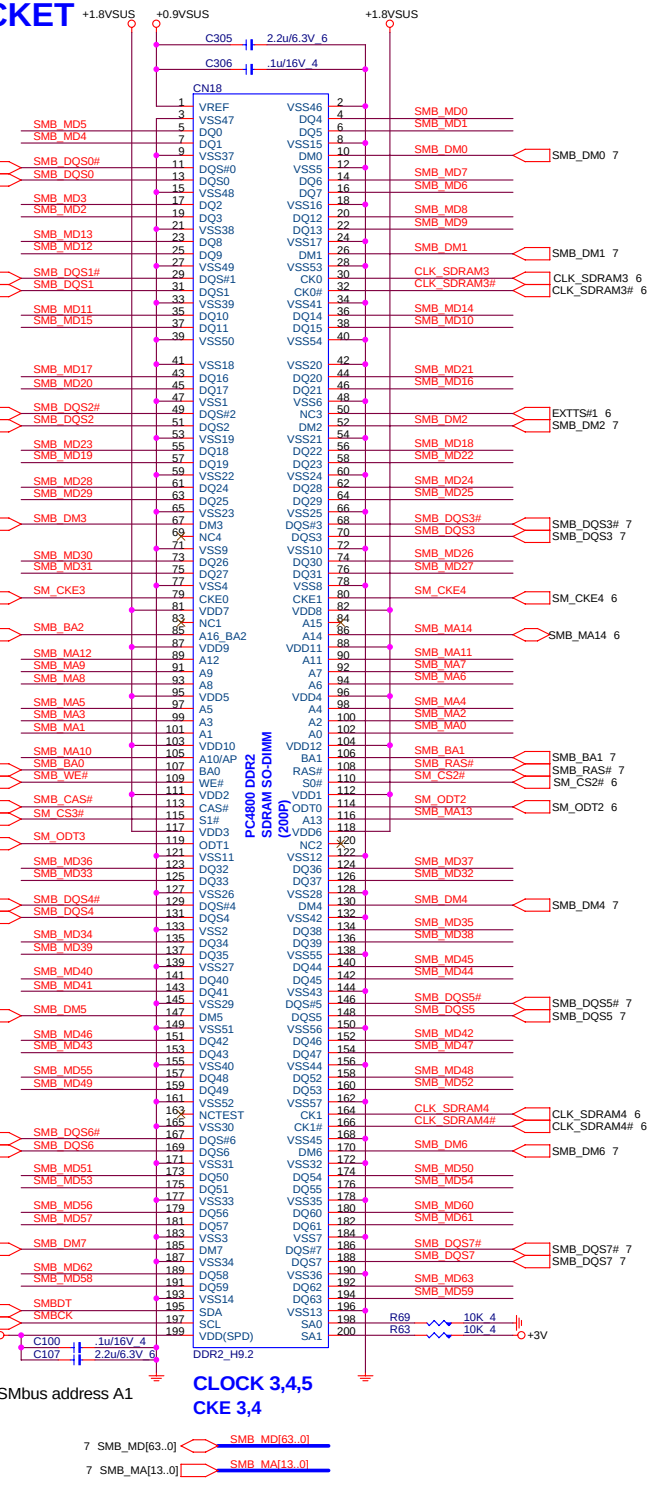
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-1(4 of 7)	2B

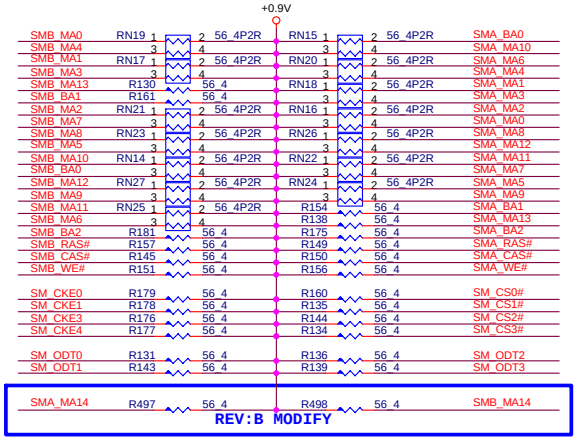
Date: Thursday, May 17, 2007 Sheet 9 of 26

DDR2 SO-DIMM SOCKET

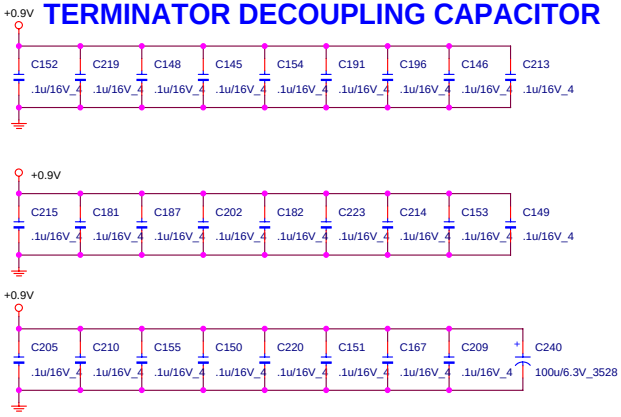




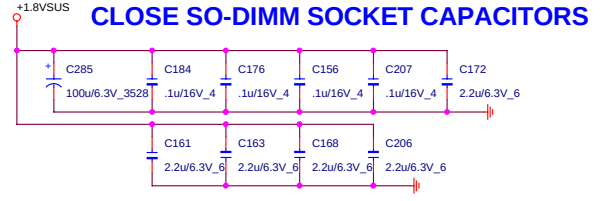
DDR2 TERMINATOR



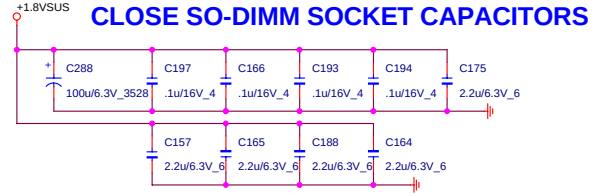
TERMINATOR DECOUPLING CAPACITOR



CLOSE SO-DIMM SOCKET CAPACITORS



CLOSE SO-DIMM SOCKET CAPACITORS



PROJECT : ZO1
Quanta Computer Inc.

Size	Document Number	Rev
	DDR SO-DIMM(200P)	2A

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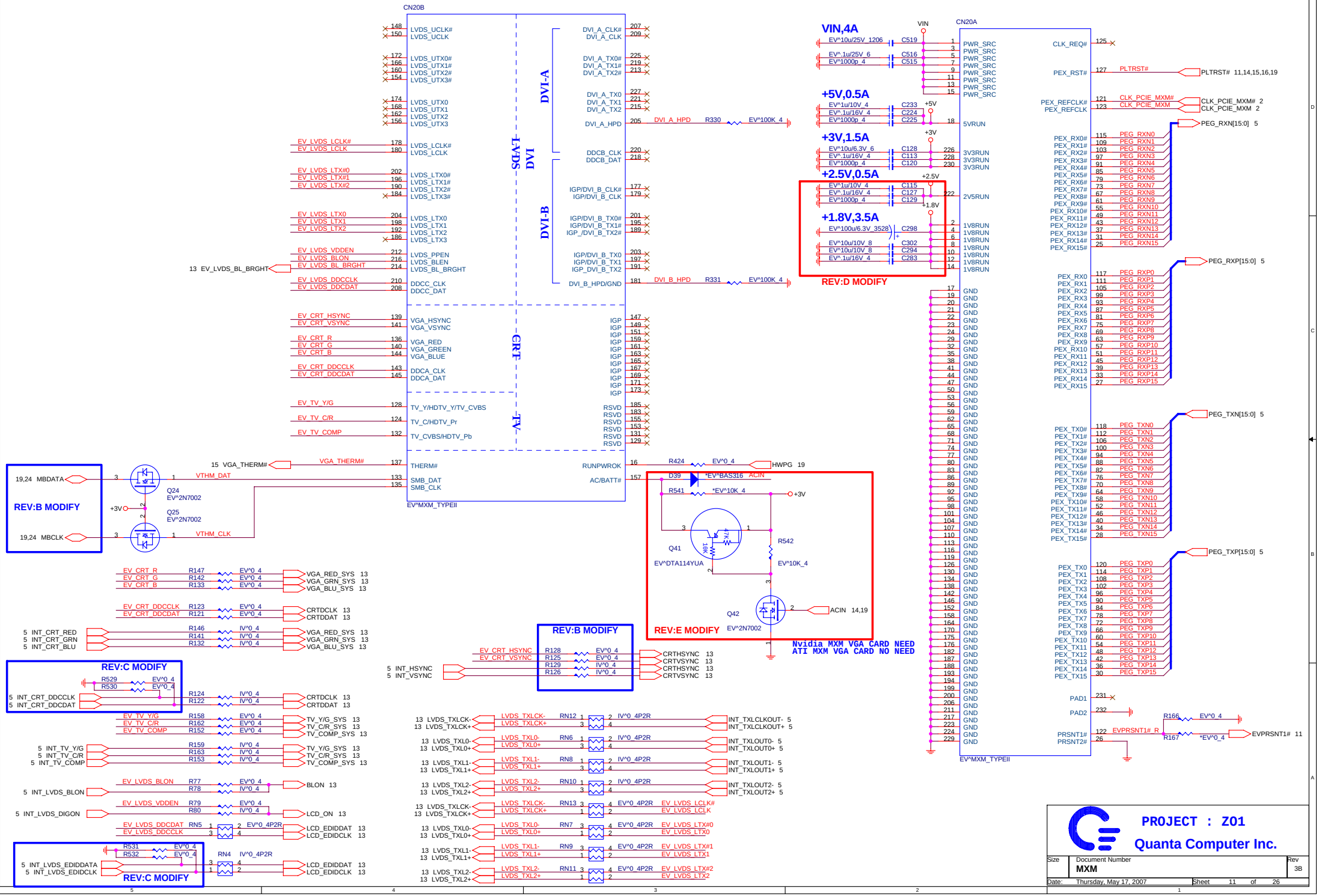
CN20B
LVDS_UCLK#
LVDS_UCLK
LVDS_UTX0#
LVDS_UTX1#
LVDS_UTX2#
LVDS_UTX3#
LVDS_UTX0
LVDS_UTX1
LVDS_UTX2
LVDS_UTX3
LVDS_LCLK#
LVDS_LCLK
LVDS_LTX0#
LVDS_LTX1#
LVDS_LTX2#
LVDS_LTX3#
LVDS_LTX0
LVDS_LTX1
LVDS_LTX2
LVDS_LTX3
LVDS_PPEN
LVDS_BLEN
LVDS_BL_BRGHT
DDCC_CLK
DDCC_DAT
LVDS
DVI
DVI-A
DVI-B
CRT
TV
DVI_A_CLK#
DVI_A_CLK
DVI_A_TX0#
DVI_A_TX1#
DVI_A_TX2#
DVI_A_TX0
DVI_A_TX1
DVI_A_TX2
DVI_A_HPD
DDCB_CLK
DDCB_DAT
IGP/DVI_B_CLK#
IGP/DVI_B_CLK
IGP/DVI_B_TX0#
IGP/DVI_B_TX1#
IGP_/DVI_B_TX2#
IGP/DVI_B_TX0
IGP/DVI_B_TX1
IGP_DVI_B_TX2
DVI_B_HPD/GND
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
DDCA_CLK
DDCA_DAT
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb
THERM#
SMB_DAT
SMB_CLK
RUNPWROK
AC/BATT#
IGP
RSVD
EV^MXM_TYPEII
EV_LVDS_LCLK#
EV_LVDS_LCLK
EV_LVDS_LTX#0
EV_LVDS_LTX#1
EV_LVDS_LTX#2
EV_LVDS_LTX0
EV_LVDS_LTX1
EV_LVDS_LTX2
EV_LVDS_VDDEN
EV_LVDS_BLON
EV_LVDS_BL_BRGHT
EV_LVDS_DDCCLK
EV_LVDS_DDCDAT
13 EV_LVDS_BL_BRGHT
EV_CRT_HSYNC
EV_CRT_VSYNC
EV_CRT_R
EV_CRT_G
EV_CRT_B
EV_CRT_DDCCLK
EV_CRT_DDCDAT
EV_TV_Y/G
EV_TV_C/R
EV_TV_COMP
15 VGA_THERM#
VGA_THERM#
DVI_A_HPD
DVI_B_HPD
R330
R331
R424
EV^100K_4
EV^0_4
HWPG 19
D39
*EV^BAS316
ACIN
R541
*EV^10K_4
+3V
Q41
EV^DTA114YUA
10K
47K
R542
EV^10K_4
Q42
EV^2N7002
ACIN 14,19
REV:E MODIFY
Nvidia MXM VGA CARD NEED
ATI MXM VGA CARD NO NEED
REV:D MODIFY
VIN,4A
VIN
EV^10u/25V_1206
EV^.1u/25V_6
EV^1000p_4
C519
C516
C515
+5V,0.5A
EV^1u/10V_4
EV^.1u/16V_4
EV^1000p_4
C233
C224
C225
+5V
5VRUN
+3V,1.5A
EV^10u/6.3V_6
EV^.1u/16V_4
EV^1000p_4
C128
C113
C120
+3V
3V3RUN
+2.5V,0.5A
EV^1u/10V_4
EV^.1u/16V_4
EV^1000p_4
C115
C127
C129
+2.5V
2V5RUN
+1.8V,3.5A
EV^100u/6.3V_3528
C298
EV^10u/10V_8
EV^10u/10V_8
EV^.1u/16V_4
C302
C294
C283
+1.8V
1V8RUN
CN20A
PWR_SRC
GND
CLK_REQ#
PEX_RST#
PEX_REFCLK#
PEX_REFCLK
PEX_RX0#
PEX_RX1#
PEX_RX2#
PEX_RX3#
PEX_RX4#
PEX_RX5#
PEX_RX6#
PEX_RX7#
PEX_RX8#
PEX_RX9#
PEX_RX10#
PEX_RX11#
PEX_RX12#
PEX_RX13#
PEX_RX14#
PEX_RX15#
PEX_RX0
PEX_RX1
PEX_RX2
PEX_RX3
PEX_RX4
PEX_RX5
PEX_RX6
PEX_RX7
PEX_RX8
PEX_RX9
PEX_RX10
PEX_RX11
PEX_RX12
PEX_RX13
PEX_RX14
PEX_RX15
PEX_TX0#
PEX_TX1#
PEX_TX2#
PEX_TX3#
PEX_TX4#
PEX_TX5#
PEX_TX6#
PEX_TX7#
PEX_TX8#
PEX_TX9#
PEX_TX10#
PEX_TX11#
PEX_TX12#
PEX_TX13#
PEX_TX14#
PEX_TX15#
PEX_TX0
PEX_TX1
PEX_TX2
PEX_TX3
PEX_TX4
PEX_TX5
PEX_TX6
PEX_TX7
PEX_TX8
PEX_TX9
PEX_TX10
PEX_TX11
PEX_TX12
PEX_TX13
PEX_TX14
PEX_TX15
PAD1
PAD2
PRSNT1#
PRSNT2#
CLK_PCIE_MXM#
CLK_PCIE_MXM
EVPRSNT1#
PEG_RXN[15:0] 5
PEG_RXP[15:0] 5
PEG_TXN[15:0] 5
PEG_TXP[15:0] 5
PLTRST# 11,14,15,16,19
CLK_PCIE_MXM# 2
CLK_PCIE_MXM 2
EVPRSNT1# 11
EV^MXM_TYPEII
19,24 MBDATA
19,24 MBCLK
VTHM_DAT
VTHM_CLK
Q24
EV^2N7002
Q25
EV^2N7002
REV:B MODIFY
REV:B MODIFY
REV:C MODIFY
REV:C MODIFY
5 INT_CRT_RED
5 INT_CRT_GRN
5 INT_CRT_BLU
5 INT_CRT_DDCCLK
5 INT_CRT_DDCDAT
5 INT_TV_Y/G
5 INT_TV_C/R
5 INT_TV_COMP
5 INT_LVDS_BLON
5 INT_LVDS_DIGON
5 INT_LVDS_EDIDDATA
5 INT_LVDS_EDIDCLK
5 INT_HSYNC
5 INT_VSYNC
VGA_RED_SYS 13
VGA_GRN_SYS 13
VGA_BLU_SYS 13
CRTDCLK 13
CRTDDAT 13
TV_Y/G_SYS 13
TV_C/R_SYS 13
TV_COMP_SYS 13
BLON 13
LCD_ON 13
LCD_EDIDDAT 13
LCD_EDIDCLK 13
CRTHSYNC 13
CRTVSYNC 13
13 LVDS_TXLCK-
13 LVDS_TXLCK+
13 LVDS_TXL0-
13 LVDS_TXL0+
13 LVDS_TXL1-
13 LVDS_TXL1+
13 LVDS_TXL2-
13 LVDS_TXL2+
INT_TXLCLKOUT- 5
INT_TXLCLKOUT+ 5
INT_TXLOUT0- 5
INT_TXLOUT0+ 5
INT_TXLOUT1- 5
INT_TXLOUT1+ 5
INT_TXLOUT2- 5
INT_TXLOUT2+ 5
EV_LVDS_LCLK#
EV_LVDS_LCLK
EV_LVDS_LTX#0
EV_LVDS_LTX0
EV_LVDS_LTX#1
EV_LVDS_LTX1
EV_LVDS_LTX#2
EV_LVDS_LTX2
PROJECT : Z01
Quanta Computer Inc.
Size
Document Number
MXM
Rev
3B
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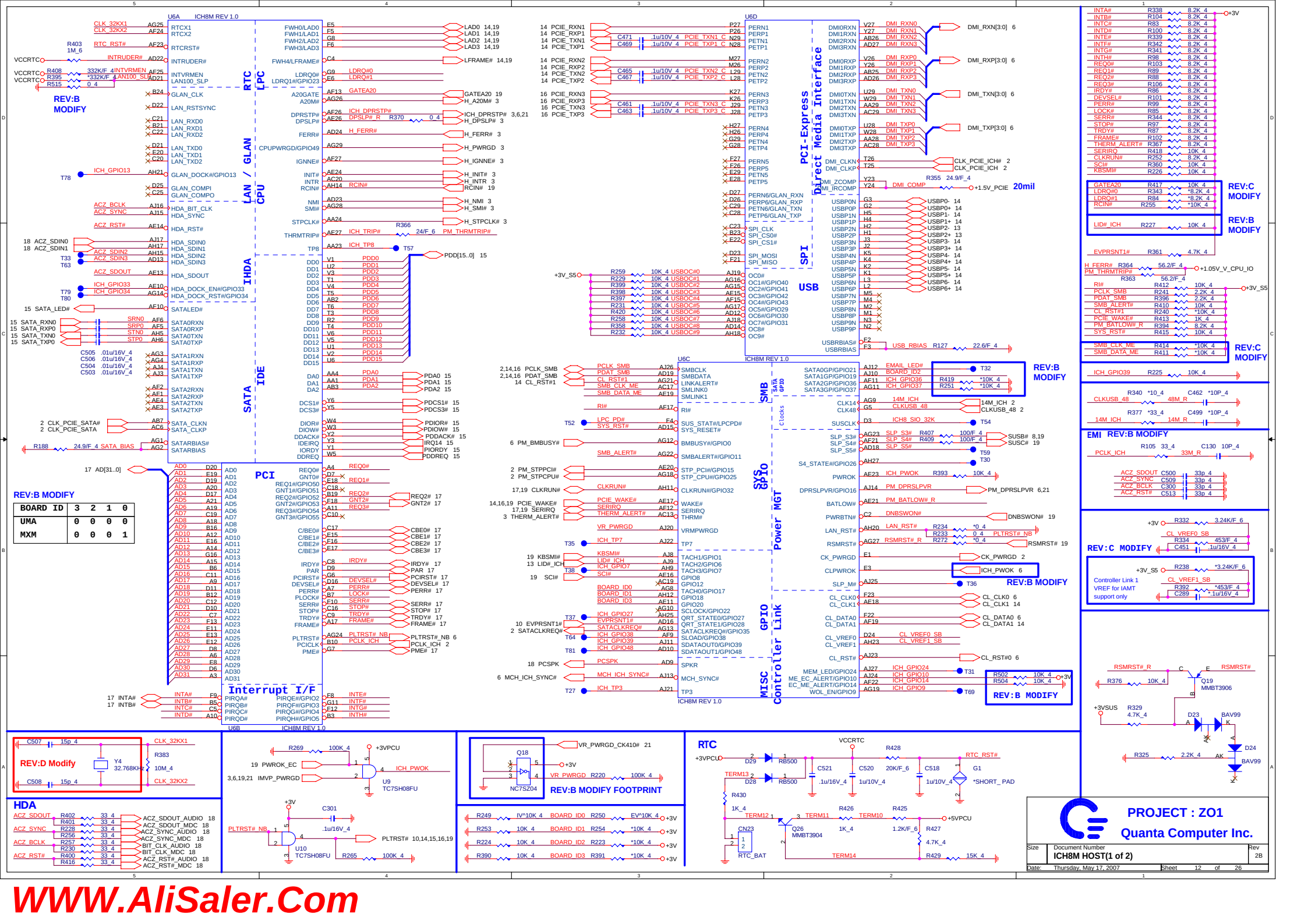

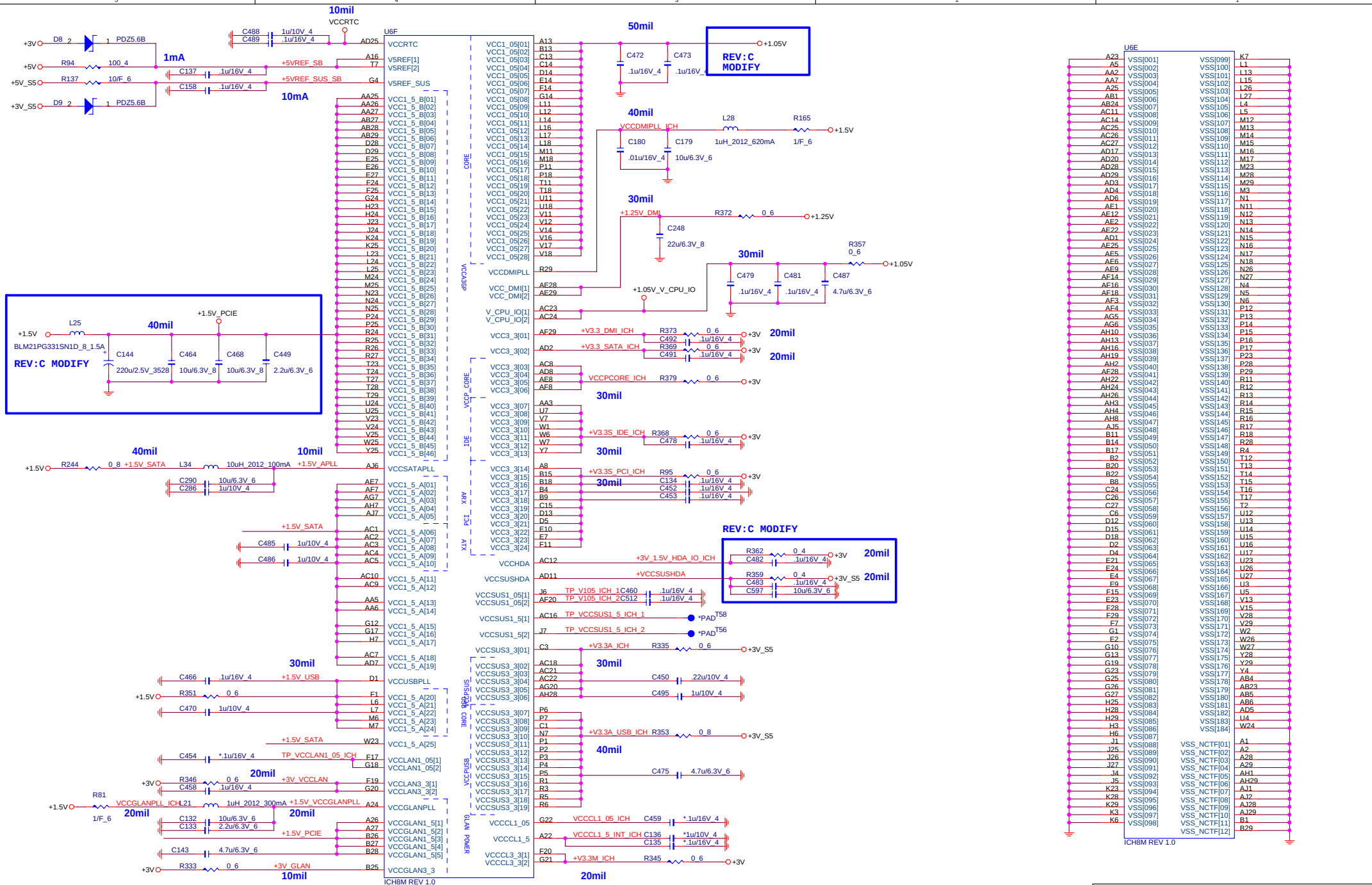

PROJECT : ZO1			
Quanta Computer Inc.			
Size	Document Number		Rev
	ICH8M Power(2 of 2)		2B
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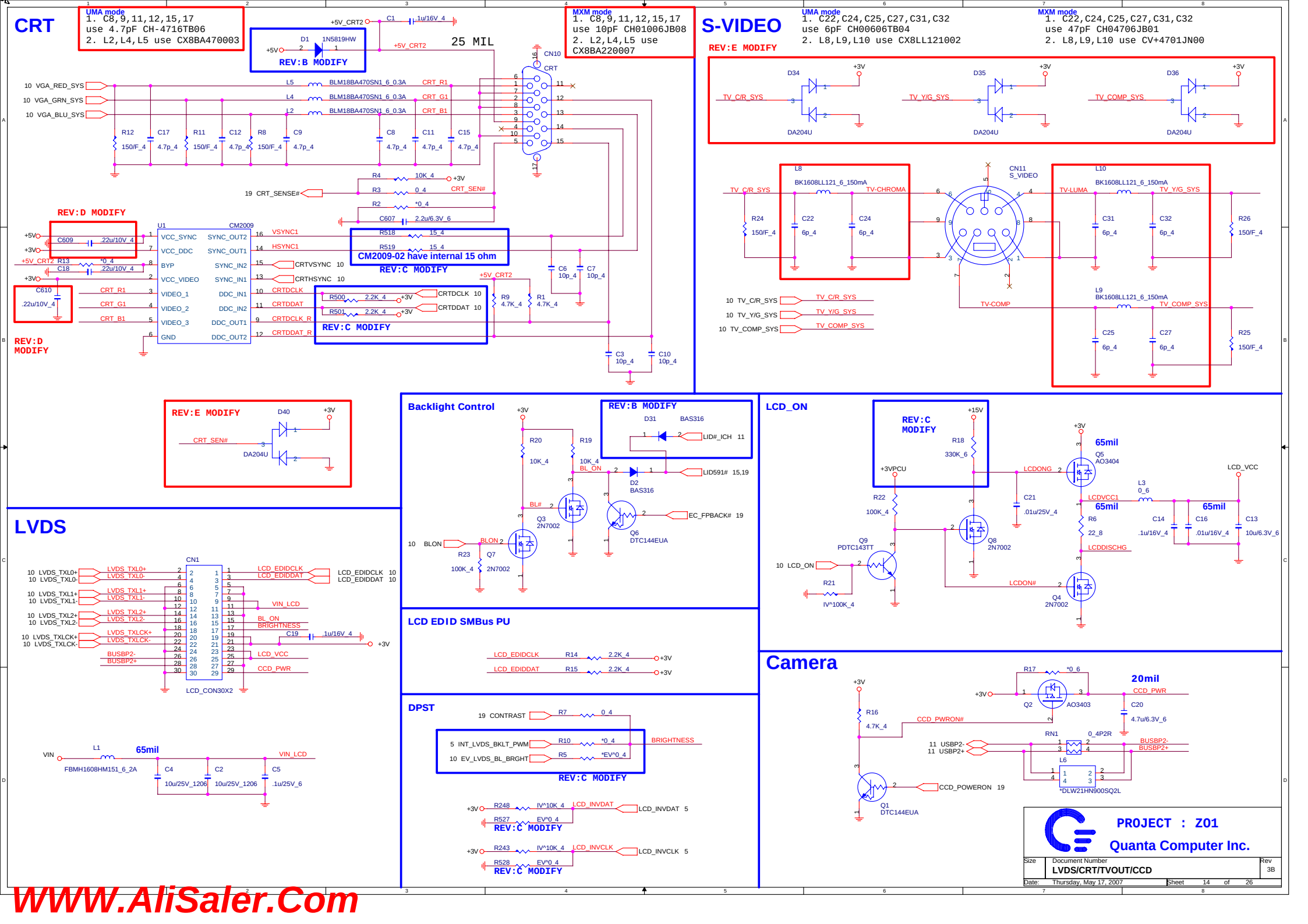
CRT
UMA mode
1. C8,9,11,12,15,17
use 4.7pF CH-4716TB06
2. L2,L4,L5 use CX8BA470003
MXM mode
1. C8,9,11,12,15,17
use 10pF CH01006JB08
2. L2,L4,L5 use
CX8BA220007
REV:B MODIFY
25 MIL
REV:D MODIFY
CM2009-02 have internal 15 ohm
REV:C MODIFY
REV:D
MODIFY
REV:E MODIFY
S-VIDEO
UMA mode
1. C22,C24,C25,C27,C31,C32
use 6pF CH00606TB04
2. L8,L9,L10 use CX8LL121002
MXM mode
1. C22,C24,C25,C27,C31,C32
use 47pF CH04706JB01
2. L8,L9,L10 use CV+4701JN00
REV:E MODIFY
Backlight Control
REV:B MODIFY
LCD_ON
REV:C
MODIFY
65mil
LVDS
LCD EDID SMBus PU
DPST
REV:C MODIFY
Camera
20mil
PROJECT : Z01
Quanta Computer Inc.
LVDS/CRT/TVOUT/CCD
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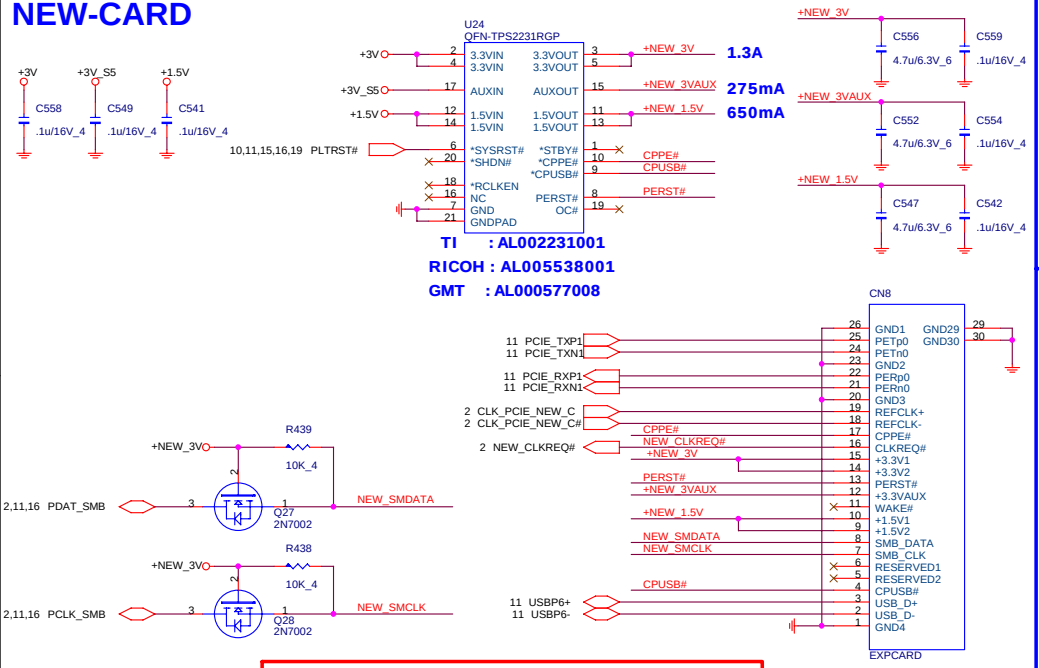
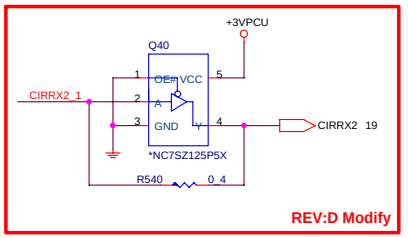
WWW.AliSaler.Com

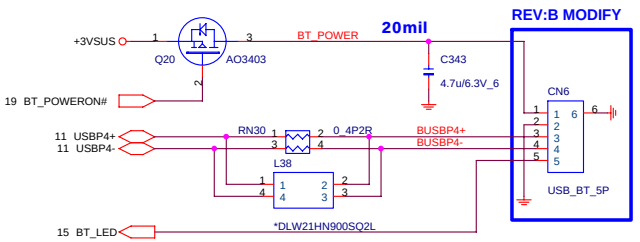
NEW-CARD

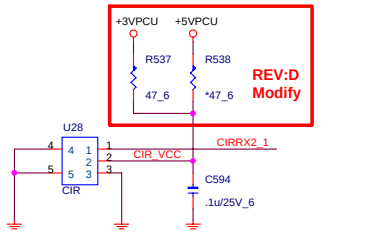


CIR



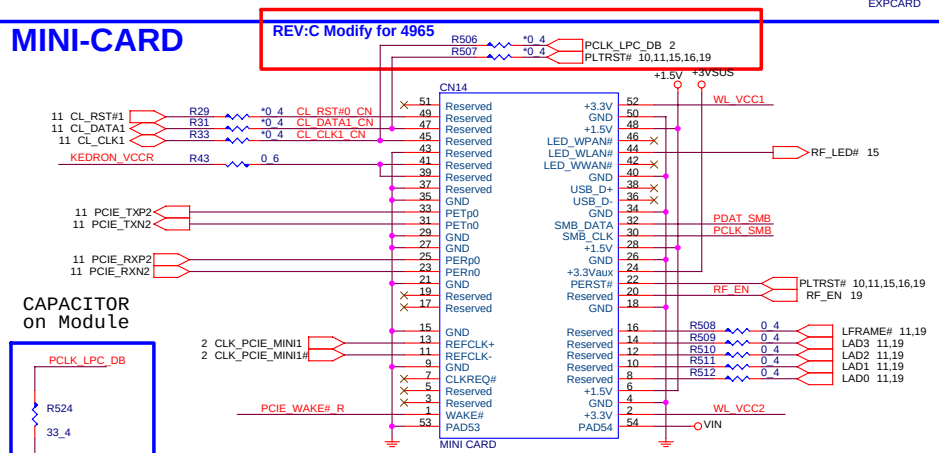
Bluetooth



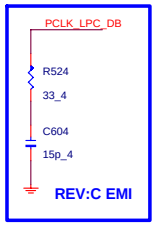


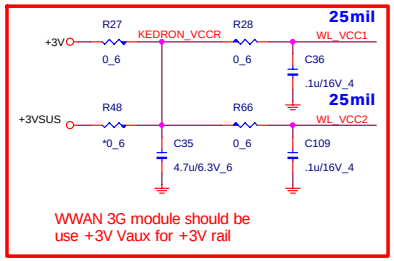
MINI-CARD

REV:C Modify for 4965

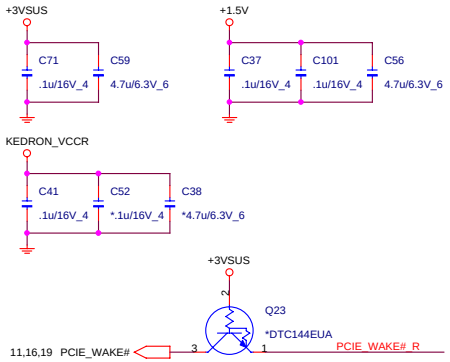


CAPACITOR on Module

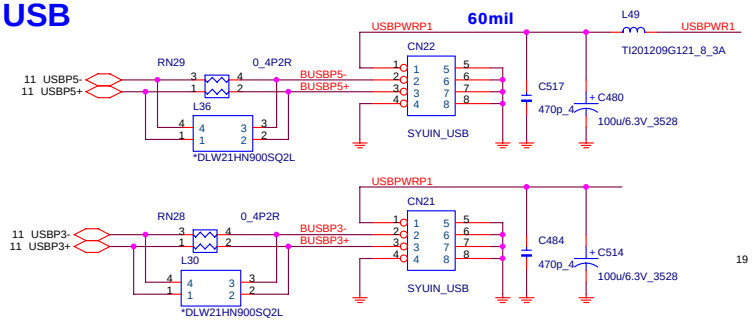


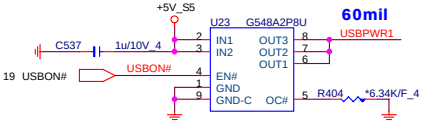


+3V_S5 for WWAN card is 2.75A

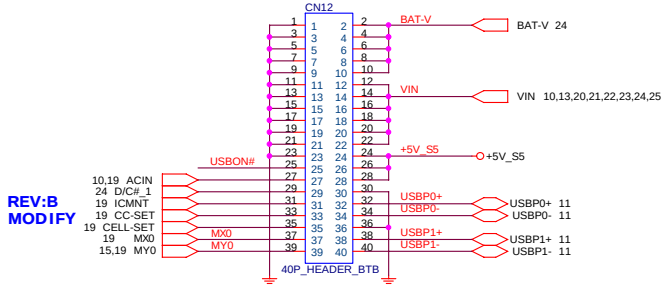


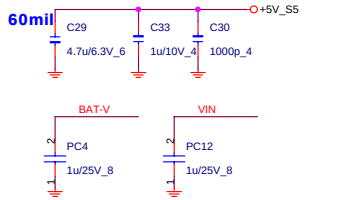
USB





TO POWER/B





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Quanta Computer Inc.

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	NEW&MINICARD/USB/BT/CIR/ACIN	3A
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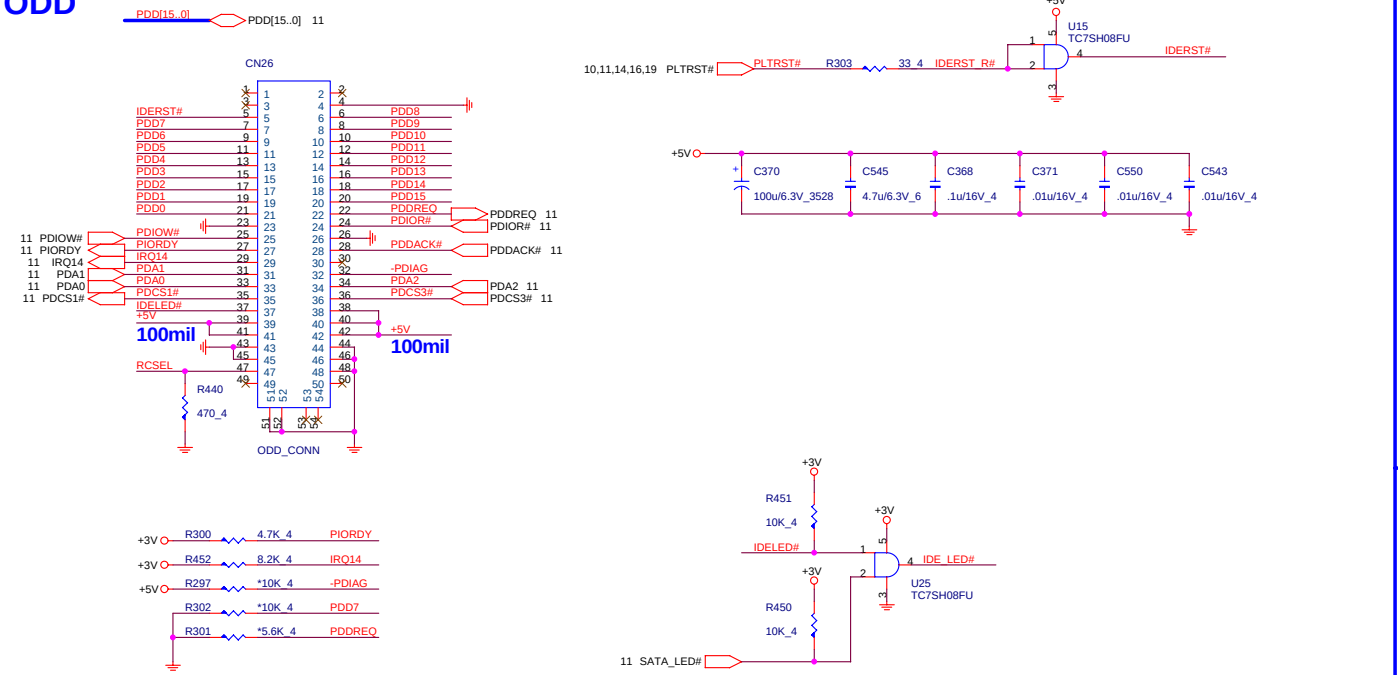
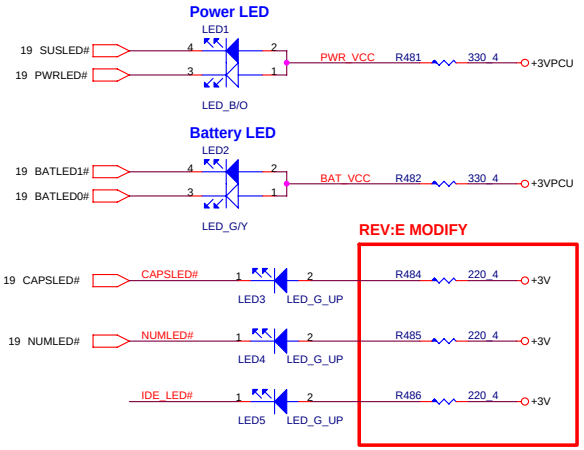
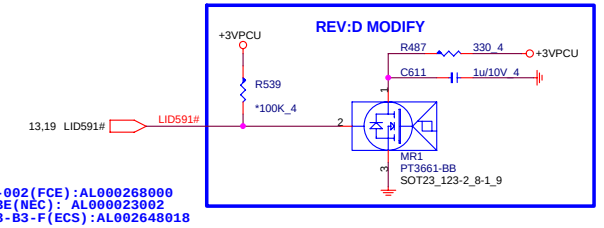
ODD



LED

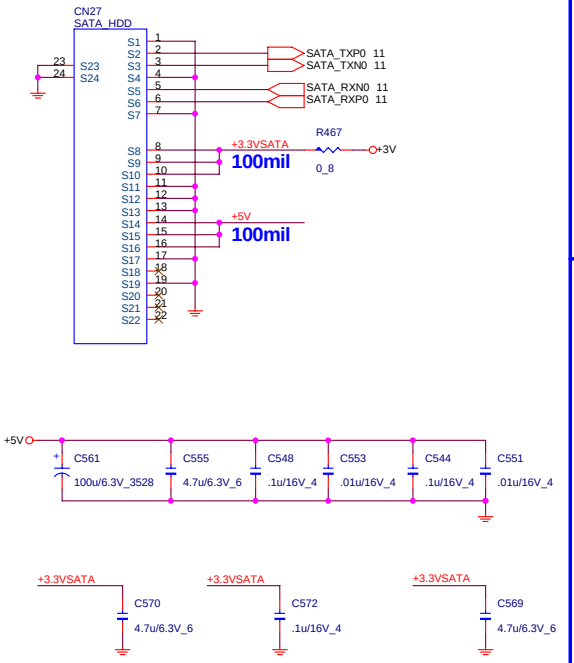


LID

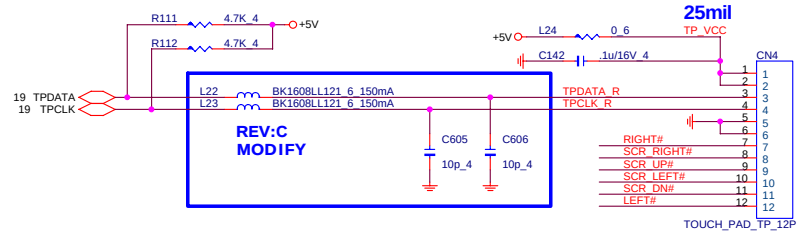


ME268-002(FCE):AL000268000
MRSS23E(NEC): AL000023002
EC2648-B3-F(ECS):AL002648018

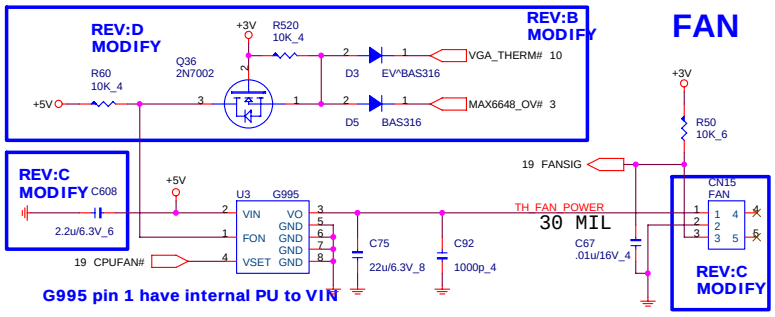
SATA



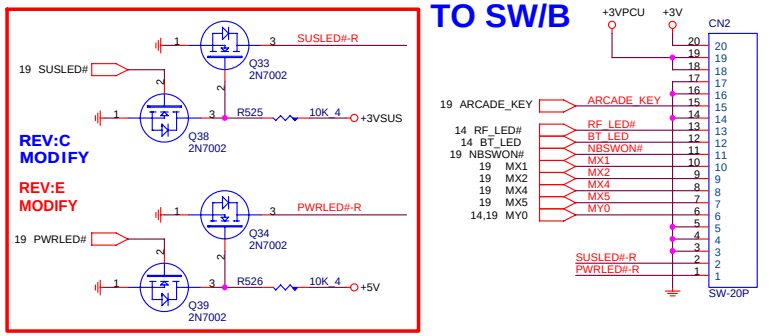
TP CONN



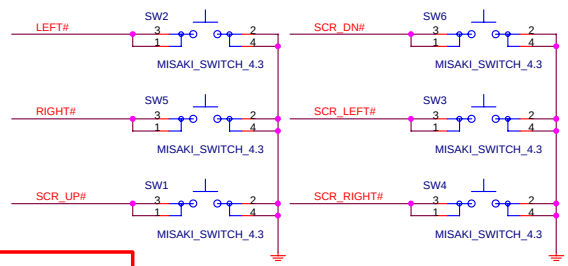
FAN



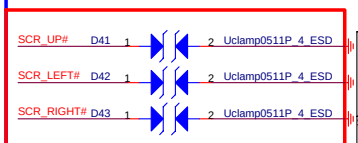
TO SW/B



TP SWITCH



REV:E Modify



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Quanta Computer Inc.

Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN	3B
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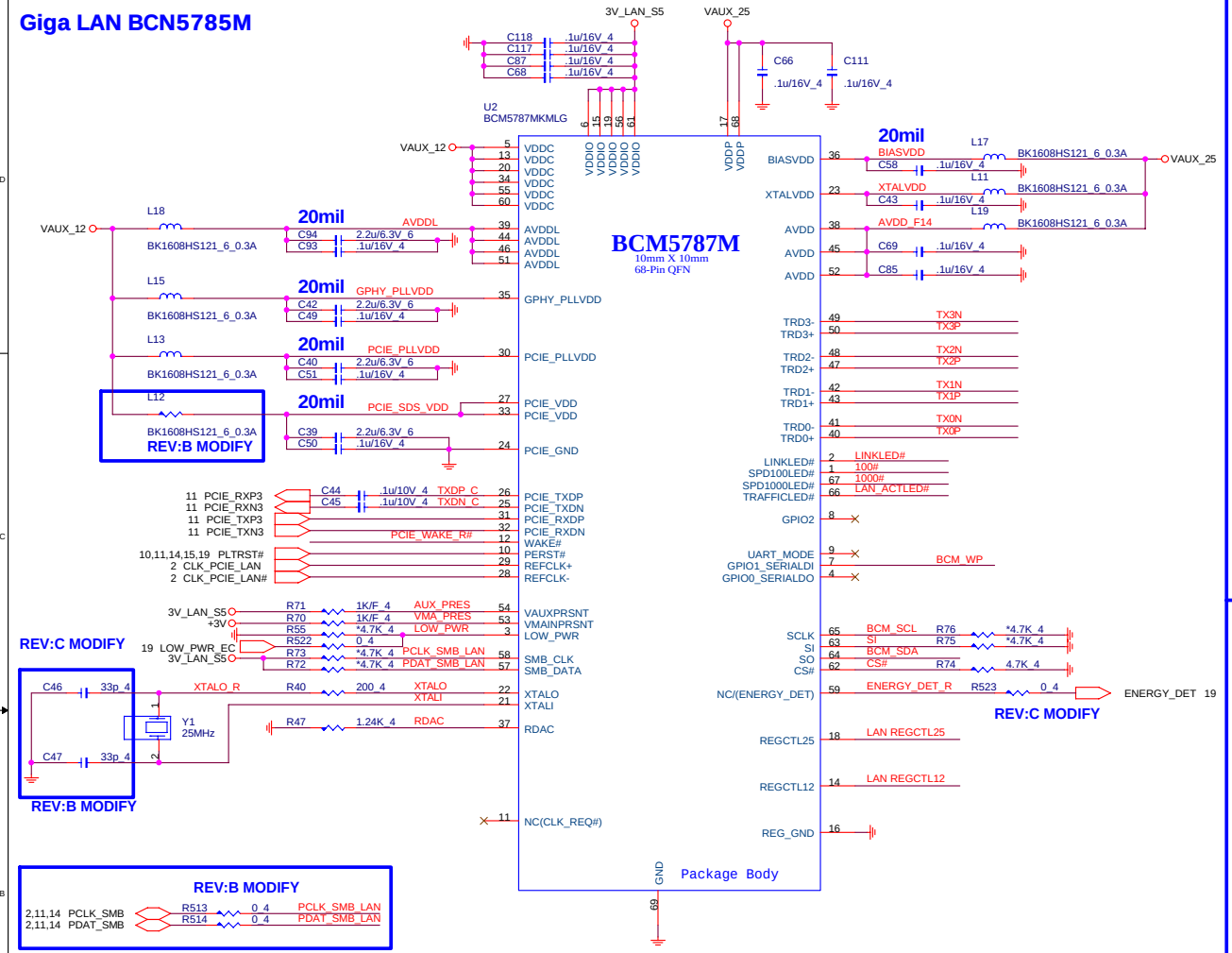
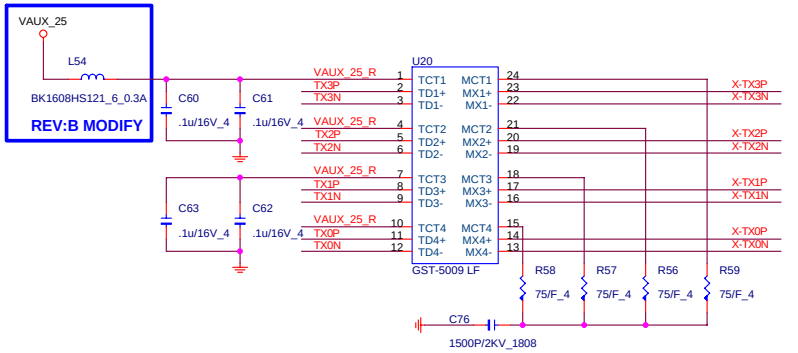
Giga LAN BCN5785M

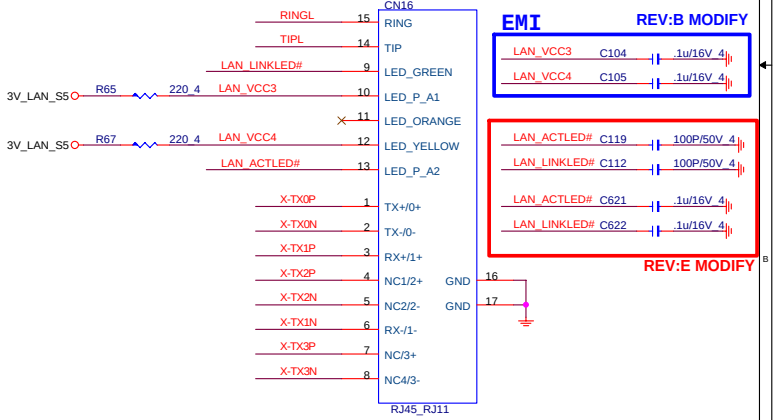


Transfomer

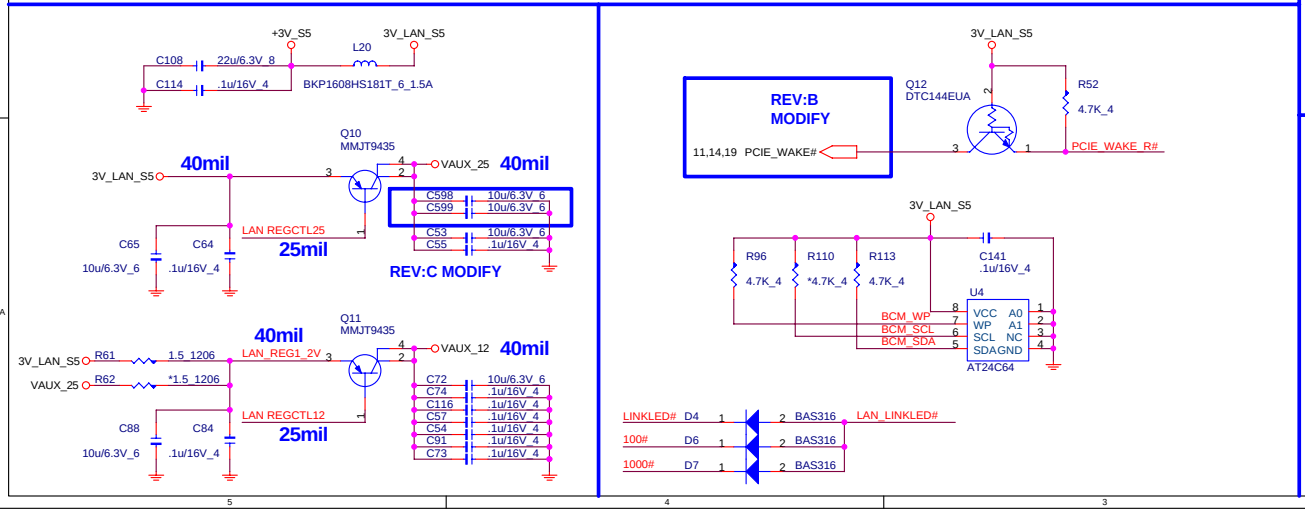
Source 1:	DELTA	LFE9249	DB0ZR1LAN11
Source 2:	Bothand	GST5009	DBKN1NLAN03
Source 3:	FCE	NS892402	DB0ZH1LAN06



RJ45 & RJ11 connector



RJ11 cable



PROJECT : ZO1

Quanta Computer Inc.

Size	Document Number	Rev
	GigaLAN BCM5787M & RJ45/11	3A

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R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05

U8B R5C832T_V00

PCI / OTHER

IEEE1394/SD

U8A R5C832T_V00

PowerOnReset for VccCore

When GRESET# is controlled by system, the pull-up resistor(R4066) and capacitor(C4093) do not need to apply.

REV:B MODIFY

When HWSPND# is controlled by system, the pull-up resistor(R4059) dose not need to apply.

REV:B MODIFY

REV:B MODIFY

Ground guard

AS CLOSE AS POSSIBLE TO R5C833 and GUARD GND

REV:B MODIFY

XD_RE#/CLK should shield GND.

REV:B MODIFY

* NOT Use EEPROM :
R4063 : installed
R4064,U38,C4106 : NOT installed
* Use EEPROM :
R4064,U38,C4106 : installed
R4063 : NOT installed

*24LC08

> 1 ms | >60 ns

VCC

GRST#

PRST#

> 100 ns

HWSPND#

PCLK(33MHz)

1394

AS CLOSE AS POSSIBLE TO R5C833

*CL-2M2012-900JT

COMMON MODE CHOKE NEAR CONN.

Shield GND Required Separatedly, for Pairs of TPA+/- and TPB+/-

GND
TPB0-
TPB0+
GND
TPA0-
TPA0+
GND

SUYIN_1394

5 IN 1 CARD READER

Memory Card Power Supply

*CARD_READER_TTN

CARD_READER_PROCONN

EMI REV:B MODIFY

PROJECT : Z01

Quanta Computer Inc.

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	R5C832/833(5IN1/1394)	2A
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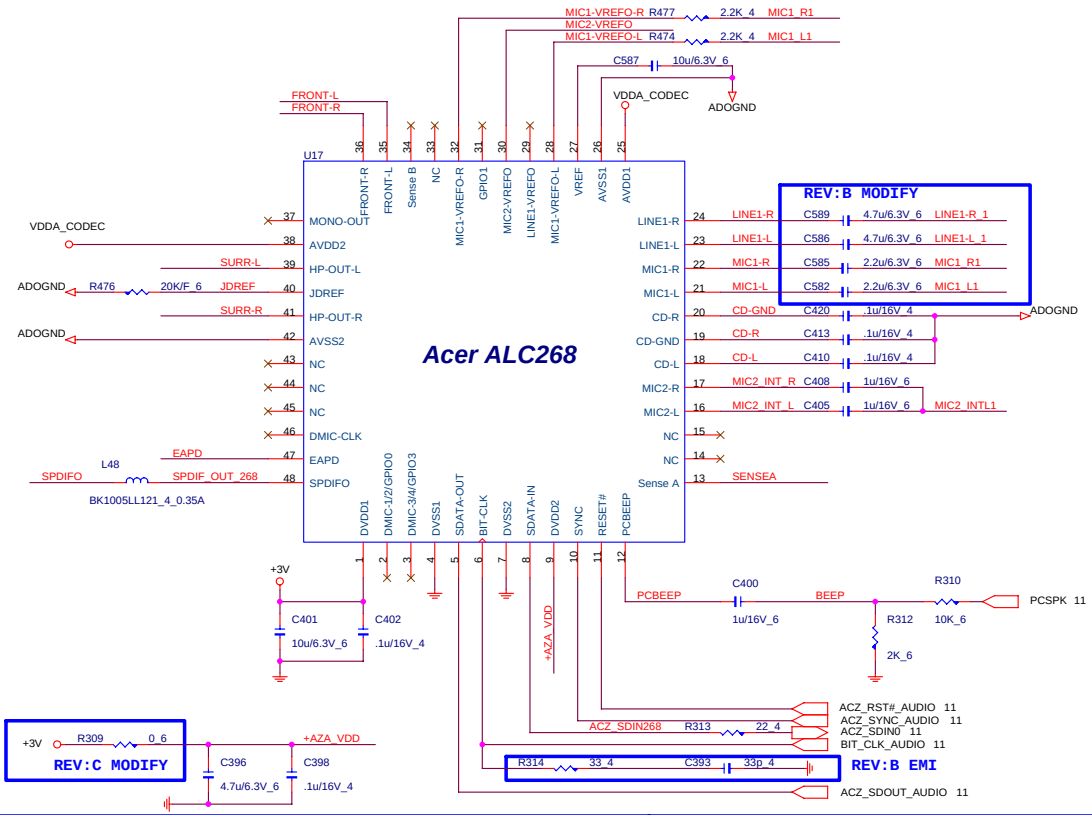
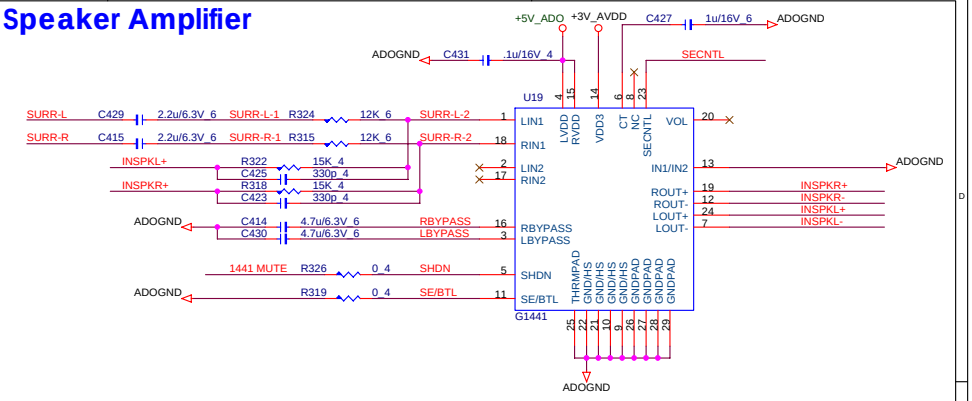
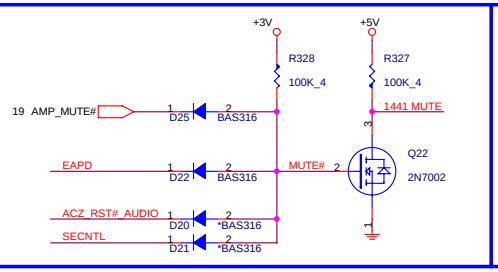
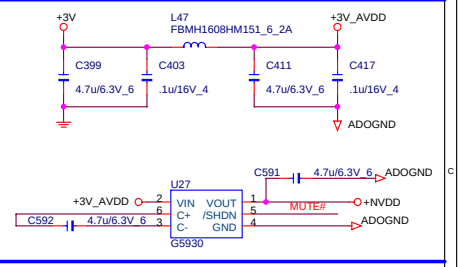
CODEC(ALC268)



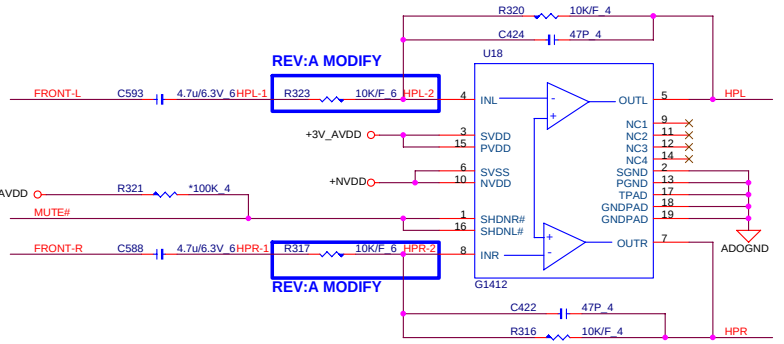
Speaker Amplifier



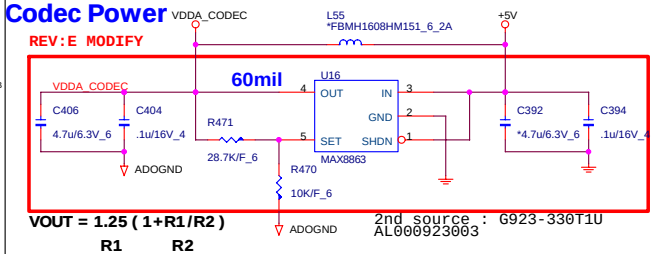


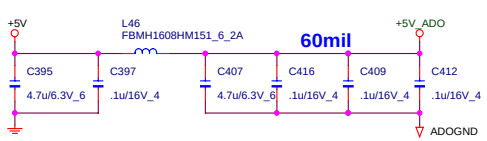


LINE OUT Amplifier

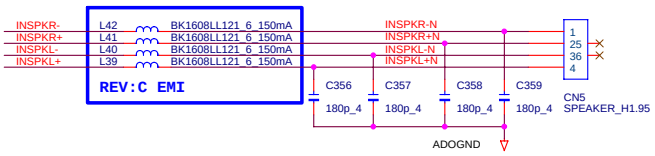


Codec Power

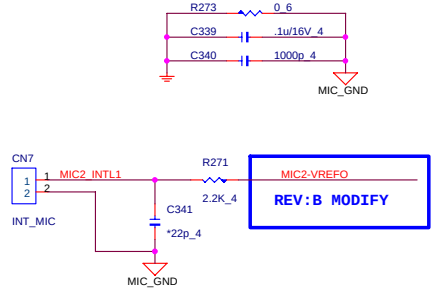




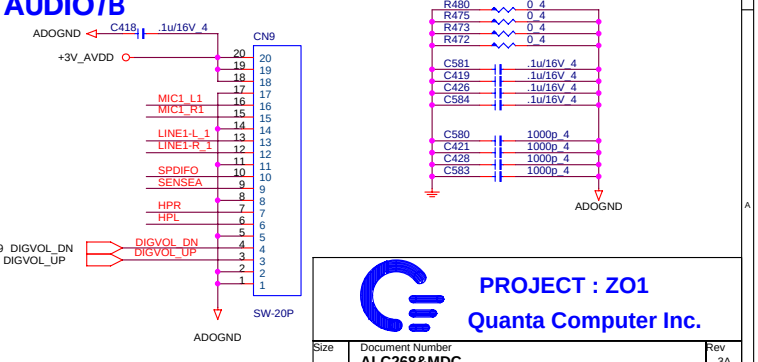
SPEAKER



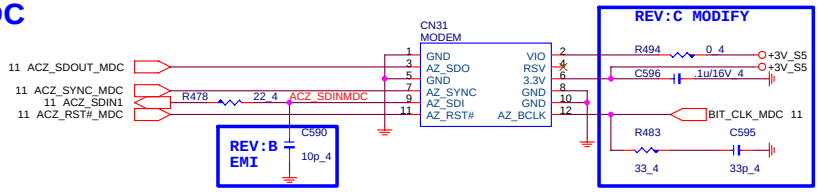
INT MIC array



AUDIO/B



MDC



PROJECT : ZO1
Quanta Computer Inc.

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	ALC268&MDC	3A
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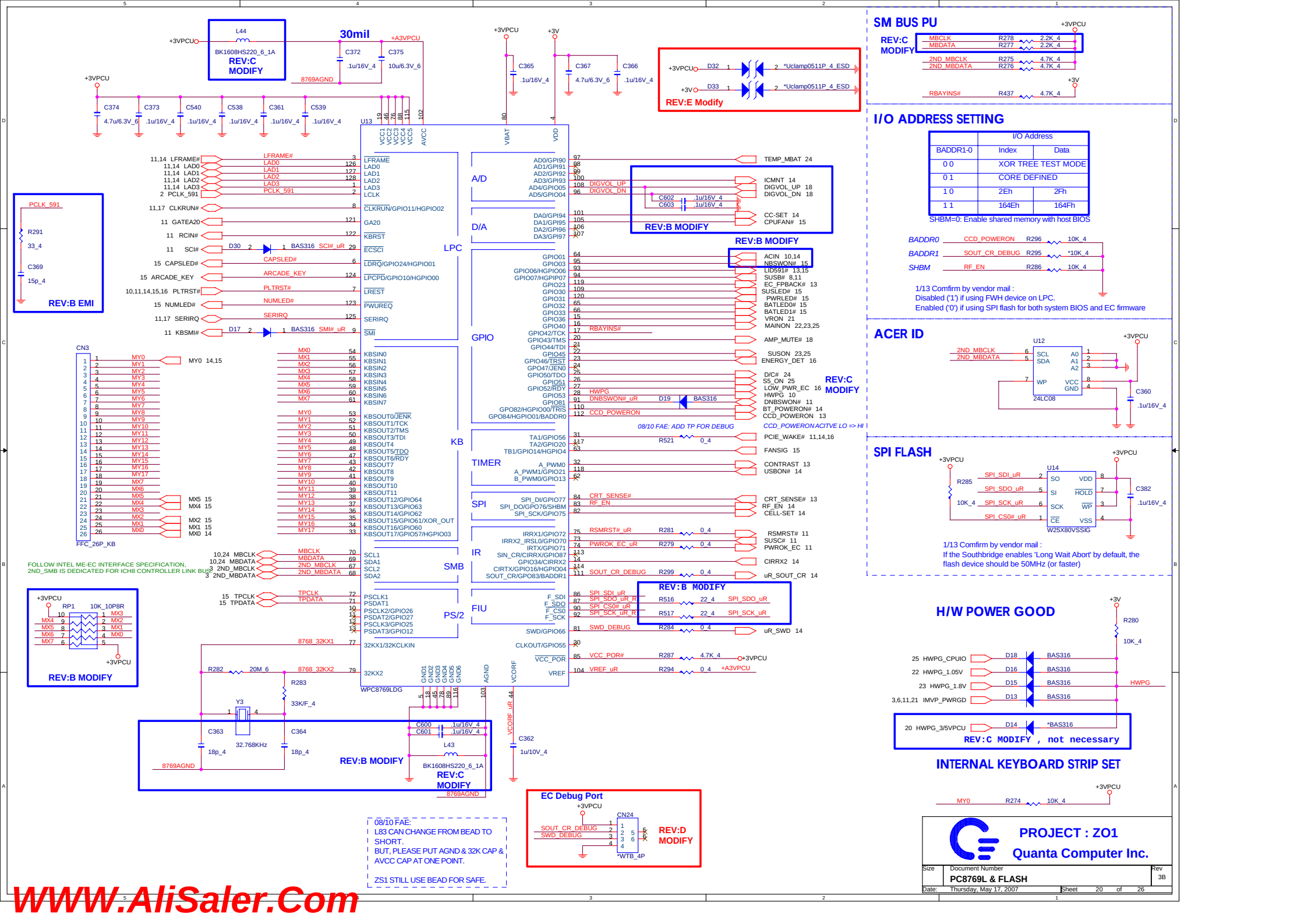

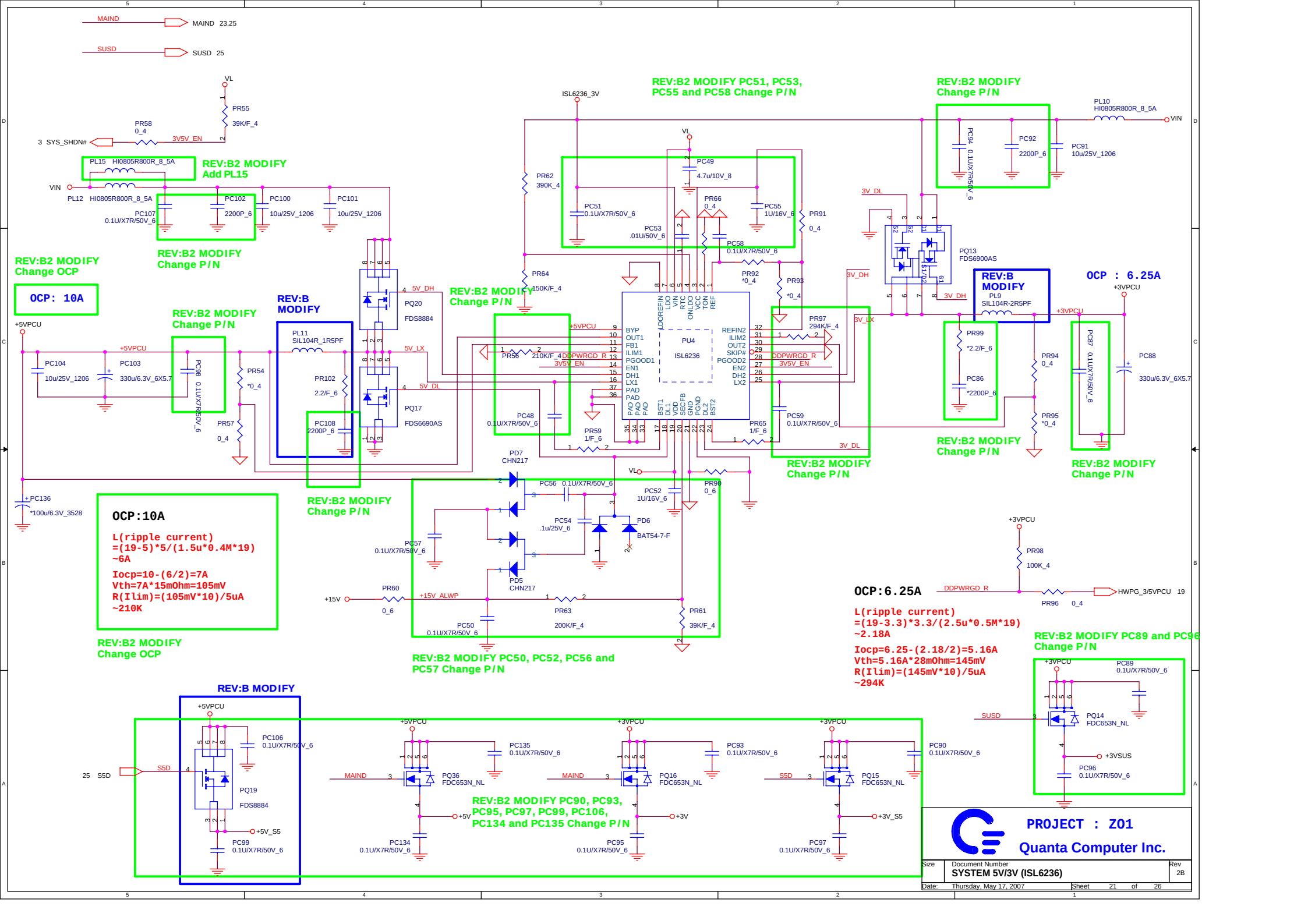
MAIND
MAIND 23,25
SUSD
SUSD 25
VL
PR55
39K/F_4
PR58
0_4
3 SYS_SHDN#
3V5V_EN
PL15 HI0805R800R_8_5A
REV:B2 MODIFY
Add PL15
VIN
PL12 HI0805R800R_8_5A
PC102
2200P_6
PC100
10u/25V_1206
PC101
10u/25V_1206
PC107
0.1U/X7R/50V_6
REV:B2 MODIFY
Change P/N
REV:B2 MODIFY
Change OCP
OCP: 10A
+5VPCU
PC104
10u/25V_1206
PC103
330u/6.3V_6X5.7
PC98
0.1U/X7R/50V_6
REV:B2 MODIFY
Change P/N
PR54
*0_4
PR57
0_4
REV:B
MODIFY
PL11
SIL104R_1R5PF
PR102
2.2/F_6
PC108
2200P_6
REV:B2 MODIFY
Change P/N
PC136
*100u/6.3V_3528
OCP:10A
L(ripple current)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp=10-(6/2)=7A
Vth=7A*15mOhm=105mV
R(Ilim)=(105mV*10)/5uA
~210K
REV:B2 MODIFY
Change OCP
5V_DH
PQ20
FDS8884
5V_LX
5V_DL
PQ17
FDS6690AS
ISL6236_3V
REV:B2 MODIFY PC51, PC53,
PC55 and PC58 Change P/N
PR62
390K_4
PC49
4.7u/10V_8
PC51
0.1U/X7R/50V_6
PC53
.01U/50V_6
PR66
0_4
PC55
1U/16V_6
PR91
0_4
PC58
0.1U/X7R/50V_6
PR64
150K/F_4
PR92
*0_4
PR93
*0_4
REV:B2 MODIFY
Change P/N
PR56
210K/F_4
DDPWRGD_R
3V5V_EN
PU4
ISL6236
LDOREFIN
LDO
VIN
RTC
ONLDO
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
VDD
SECFB
GND
PGND
DL2
BST2
PC48
0.1U/X7R/50V_6
PR59
1/F_6
PR65
1/F_6
PC59
0.1U/X7R/50V_6
PR97
294K/F_4
3V_DH
3V_LX
3V_DL
REV:B2 MODIFY
Change P/N
PD7
CHN217
PC56 0.1U/X7R/50V_6
PC54
.1u/25V_6
PD6
BAT54-7-F
PC57
0.1U/X7R/50V_6
PR60
0_6
+15V
+15V_ALWP
PR63
200K/F_4
PR61
39K/F_4
PC50
0.1U/X7R/50V_6
PC52
1U/16V_6
PR90
0_6
REV:B2 MODIFY PC50, PC52, PC56 and
PC57 Change P/N
REV:B2 MODIFY
Change P/N
PL10
HI0805R800R_8_5A
VIN
PC94
0.1U/X7R/50V_6
PC92
2200P_6
PC91
10u/25V_1206
PQ13
FDS6900AS
REV:B
MODIFY
PL9
SIL104R-2R5PF
OCP : 6.25A
+3VPCU
PR99
*2.2/F_6
PC86
*2200P_6
PR94
0_4
PR95
*0_4
PC87
0.1U/X7R/50V_6
PC88
330u/6.3V_6X5.7
REV:B2 MODIFY
Change P/N
REV:B2 MODIFY
Change P/N
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
PR98
100K_4
DDPWRGD_R
PR96
0_4
HWPG_3/5VPCU 19
REV:B2 MODIFY PC89 and PC96
Change P/N
PC89
0.1U/X7R/50V_6
SUSD
PQ14
FDC653N_NL
+3VSUS
PC96
0.1U/X7R/50V_6
REV:B MODIFY
25 S5D
PC106
0.1U/X7R/50V_6
PQ19
FDS8884
+5V_S5
PC99
0.1U/X7R/50V_6
PC135
0.1U/X7R/50V_6
PQ36
FDC653N_NL
+5V
PC134
0.1U/X7R/50V_6
PC93
0.1U/X7R/50V_6
PQ16
FDC653N_NL
+3V
PC95
0.1U/X7R/50V_6
PC90
0.1U/X7R/50V_6
PQ15
FDC653N_NL
+3V_S5
PC97
0.1U/X7R/50V_6
REV:B2 MODIFY PC90, PC93,
PC95, PC97, PC99, PC106,
PC134 and PC135 Change P/N
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Quanta Computer Inc.
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SYSTEM 5V/3V (ISL6236)
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2B
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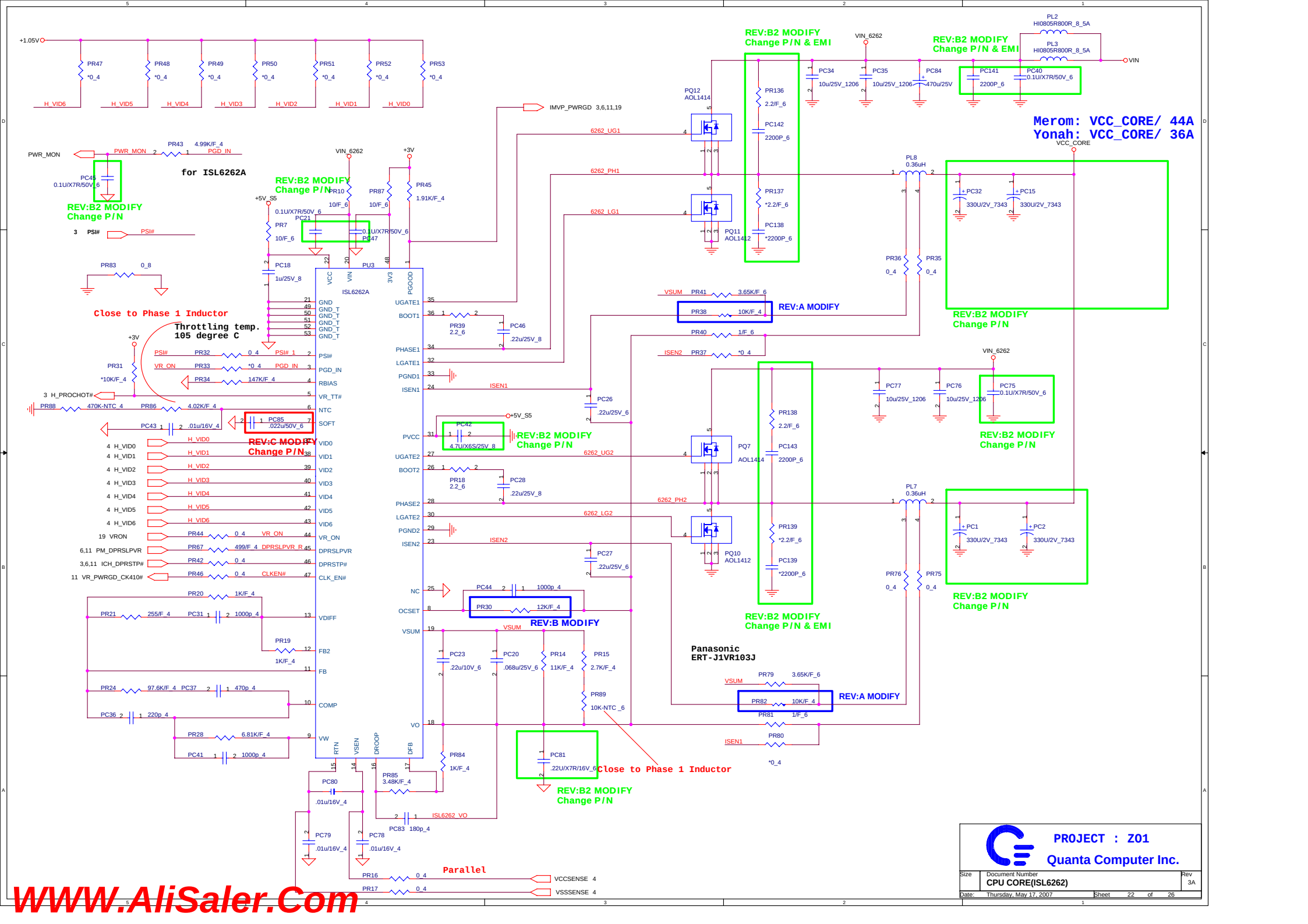

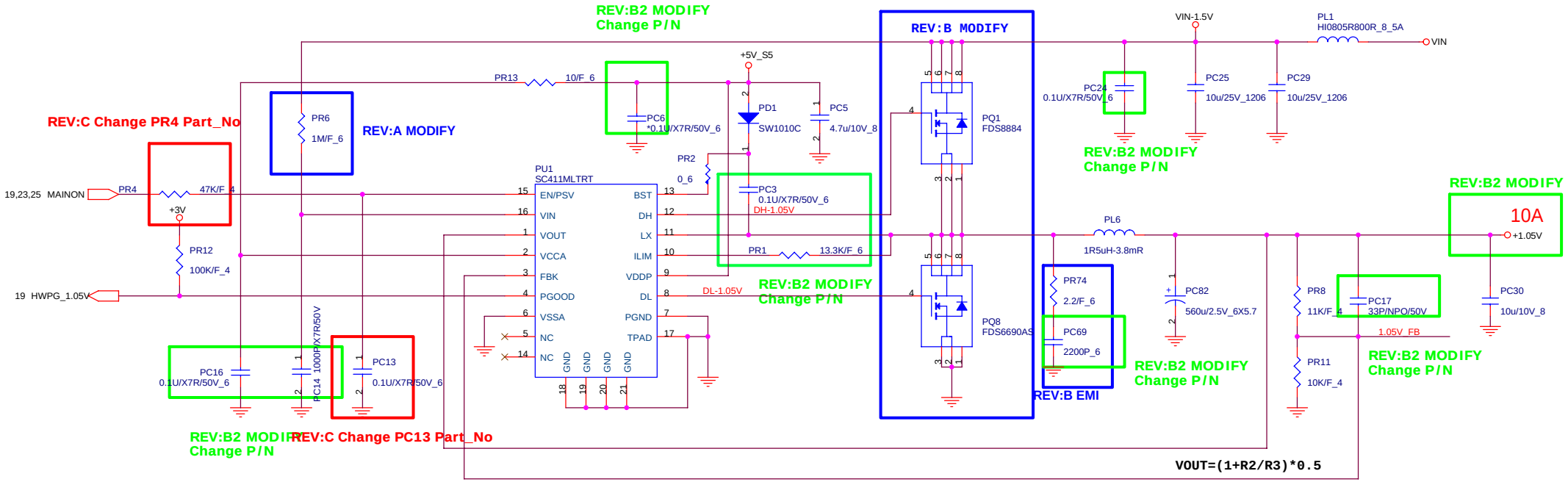

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Quanta Computer Inc.

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	VTT 1.05V(SC411)	3A

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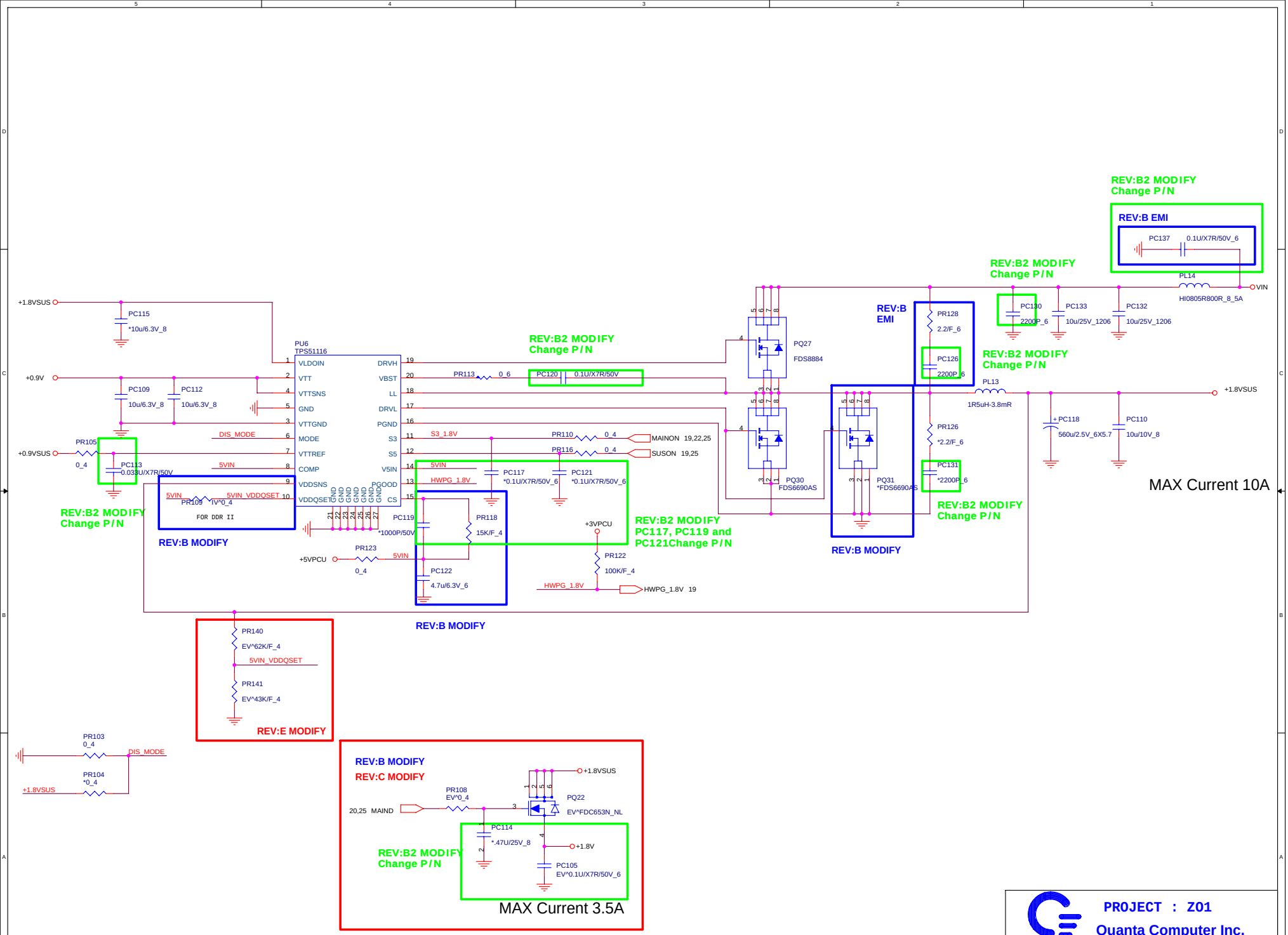

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Quanta Computer Inc.

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	DDR 1.8V(TPS51116)	3B
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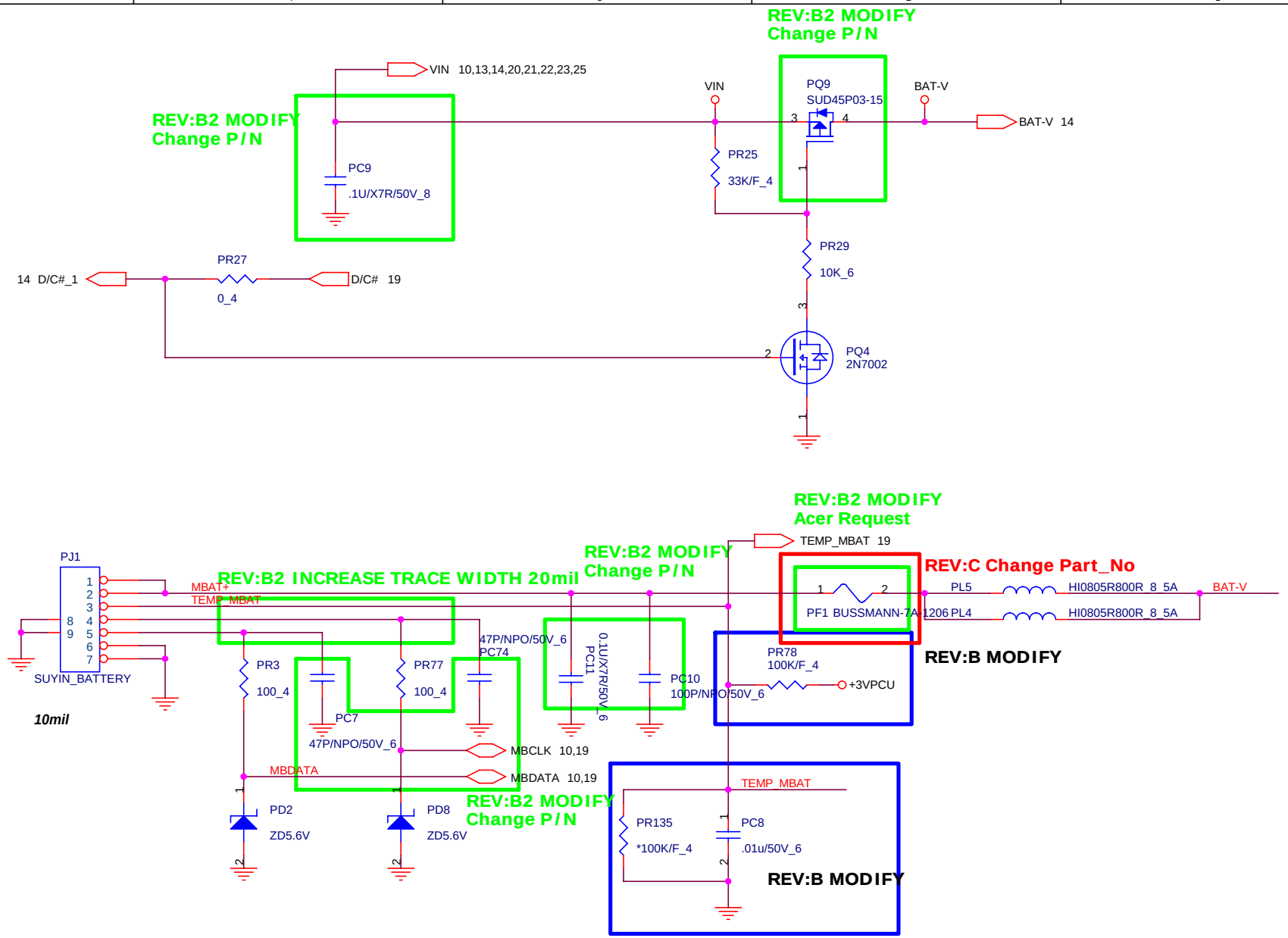

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	CHARGER (ISL6251A)	3A
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