

LCFC Confidential

CE575 NM-A871 Rev1.0 Schematic

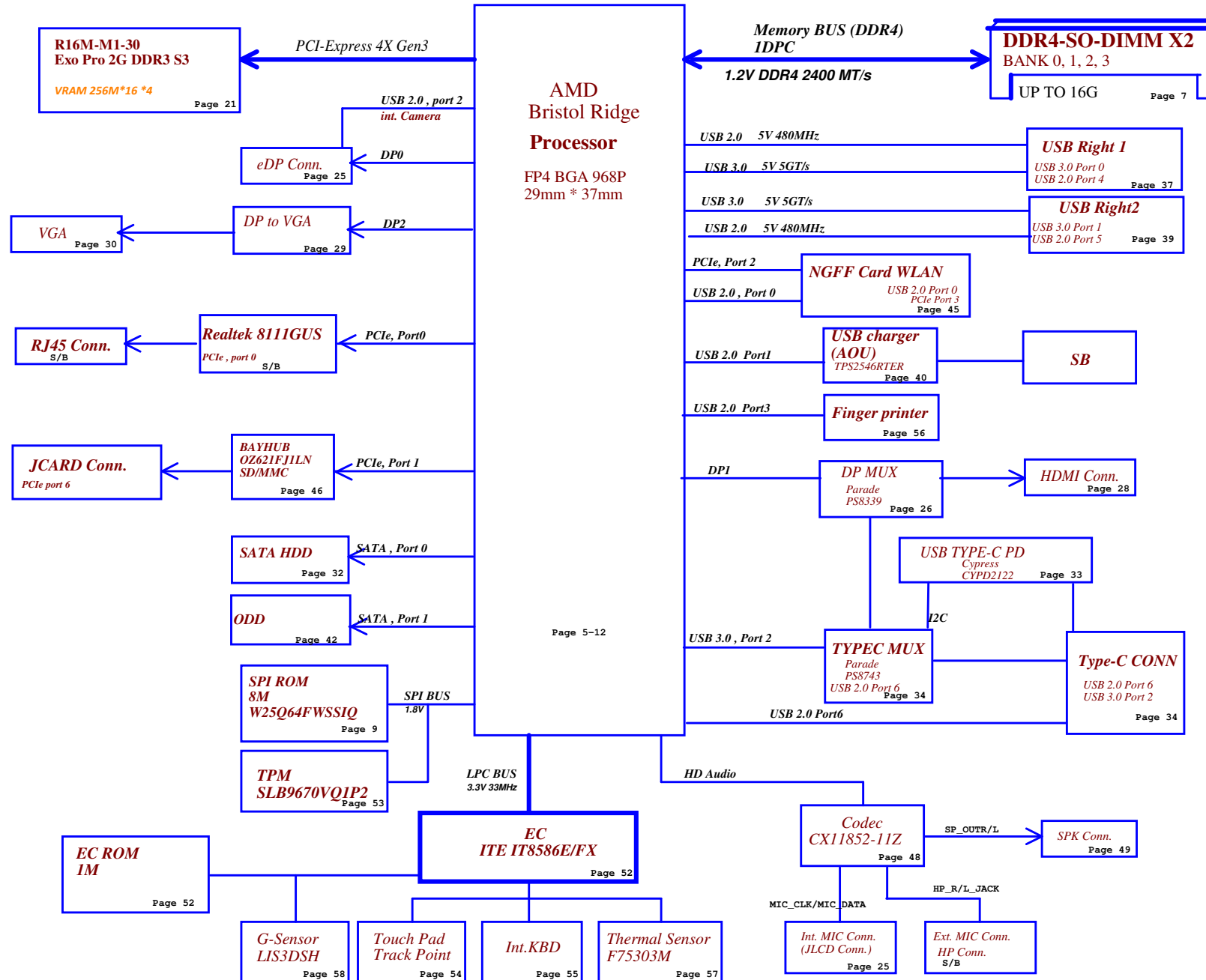
AMD Bristol Ridge Processor with DDR4

R16M-M1-30 with DDR3 4GB

2016-07-20 Rev1.0

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/5	Deciphered Date	2016/10/31	COVER PAGE	
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AMD Bristol Ridge FP4



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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane \ State	B+	+3VALW +5VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +1.5VS +1.05VS +0.6VS +VCC_CORE +VGA_CORE +3.3VS_VGA +1.8VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON	EC_ON2	SUSP#
S0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

USB2 Port

Port	Device
1	On Board
2	On Board
3	On Board
4	On Board
5	On Board
6	SB
7	On Board
8	On Board

USB3 Port

Port	Device
1	On Board
2	On Board
3	X
4	On Board

PCIE Port

Port	Device
1	
2	X
3	WLAN
4	LAN
5	X
6	CardReader
7	X
8	X
9	GPU
10	GPU
11	GPU
12	GPU

SATA Port

Port	Device
0	HDD
1	ODD

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY	G-Sensor	TYPEC
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VALW_PCH	X	X	X	V +3VALW	X
EC_SMB_CK2 EC_SMB_DA2	IT8580F	X	X	X	X	X	X	X	X	X	X	CYPD2122 +3VPD_VDD

ZZZ1 PCB@
NM-A871
DA800002000

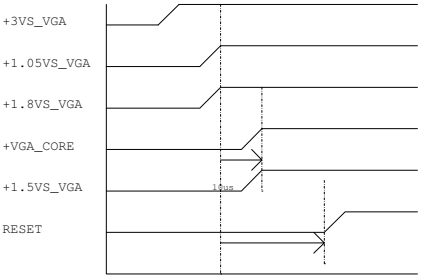
VGA and DDR3 Voltage Rails (JET TOPAZ R16M-M1-30 GPIO)

20151117

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	SVI2_SVC
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	

BOM Structure Table

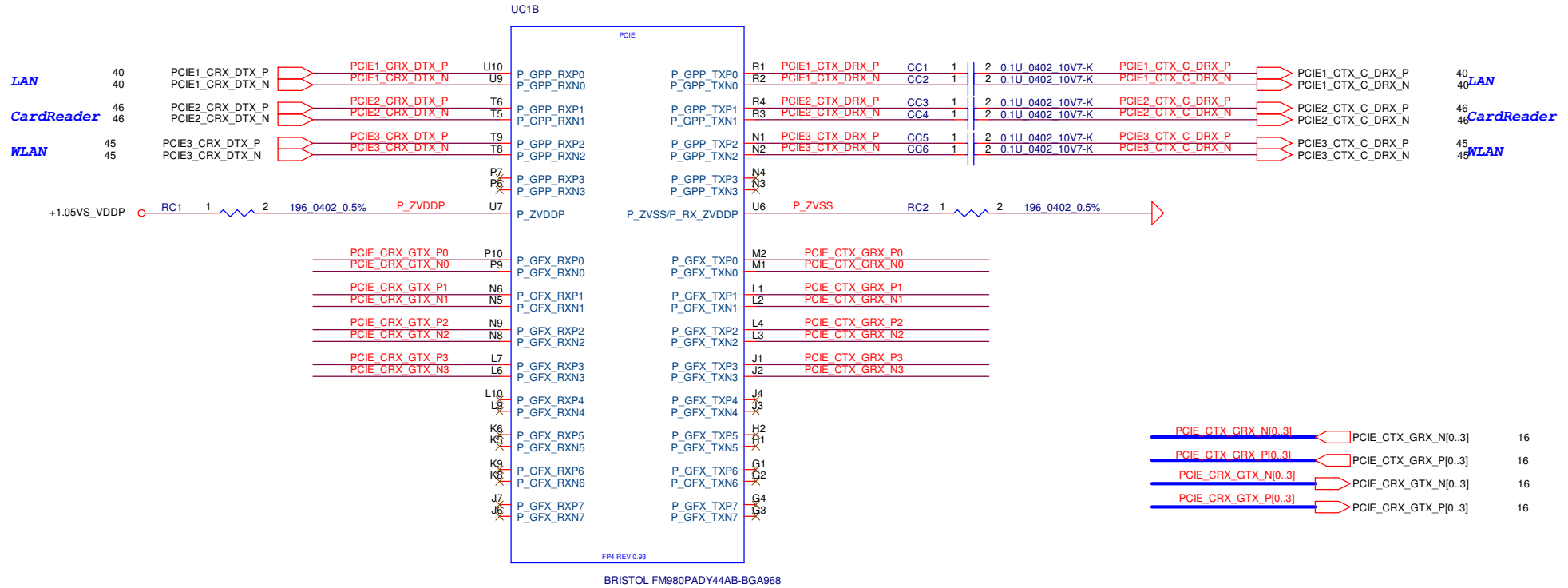
BOM Structure	NOTE
TYPEC@	For TYPEC
EMC_TC@	For TYPEC EMC
DIS@	For GPU function
X76@	GPU VRAM Setting
TPM@	Trusted Platform Module(TPM)
SA@	SATA redriver function
RESA@	Disable SATA re-driver
UMA@	UMA SKU ID
DPRE@	DP re-driver function
RE@	Disable HDMI re-driver
HD@	HDMI repeater function
ME@	ME Connector
ESD@	For ESD function
EMI@	For EMI function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
U31@	For U3 port1 redriver function
U32@	For U3 port2 redriver function
U33@	For U3 port3 redriver function




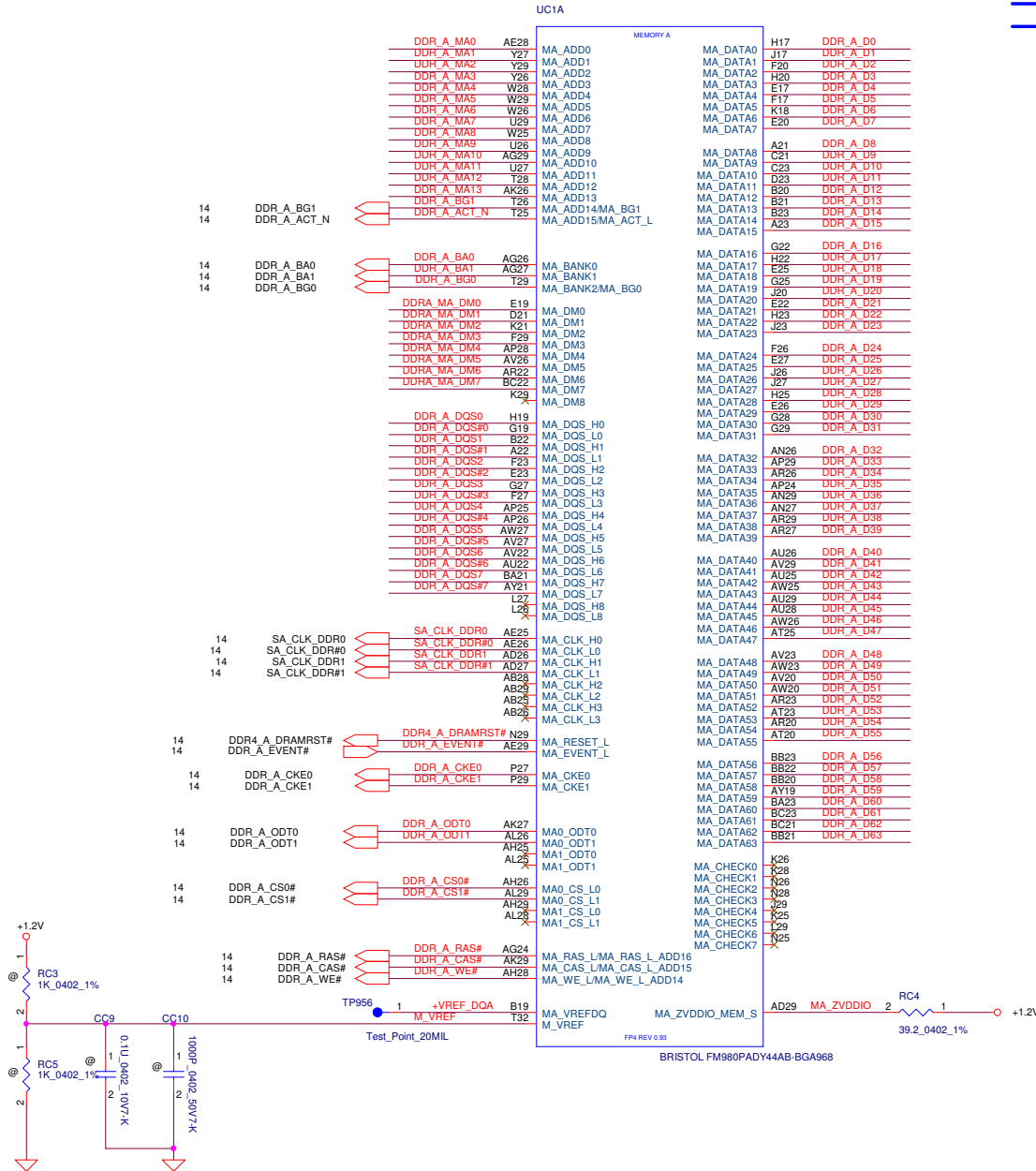
1. all power rail ramp up time should be within 20ms

	Device ID
JET-XT	0x6664
TOPAZ XT	0x6900

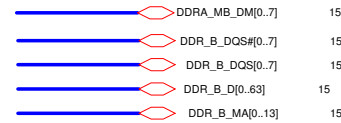
			RV104	RV105
Memory (GDDR3)				
Samsung	1G	SA22225SH30*4	PU 8.45K	PD 2K
	2G	SA000063F00*4	PU 3.4K	PD 10K
Hynix	1G	SA00005VS10*4	PU 4.53K	PD 2K
	2G	SA00005YL10*4	PU 4.75K	NC
Micron	1G	SA00005M100*4	NC	PD 4.75K
	2G	SA000060I00*4	PU 3.24K	PD 5.62K




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DP2 USED FOR VGA ON 15"

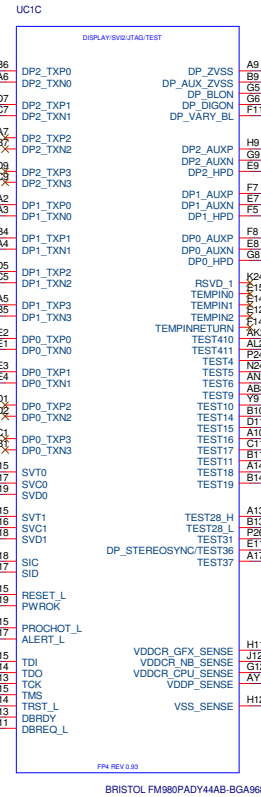
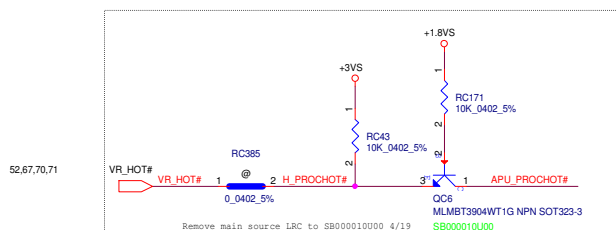
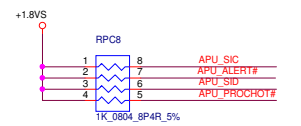
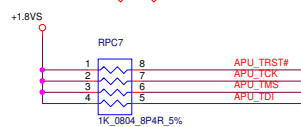
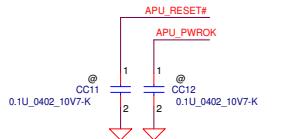
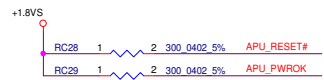
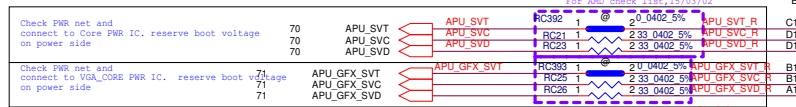
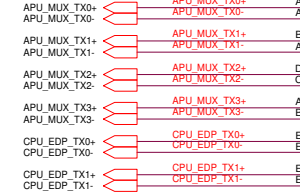
VGA

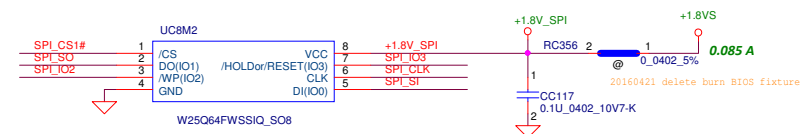
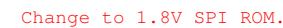



DP1 USED FOR TYPE C/ HDMI ON 15"

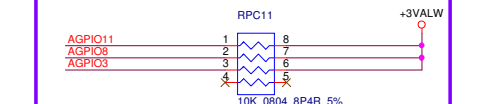
TYPE C/ HDMI

eDP



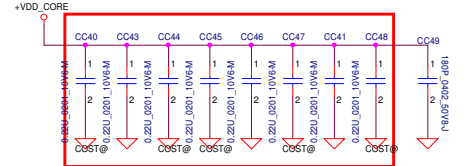


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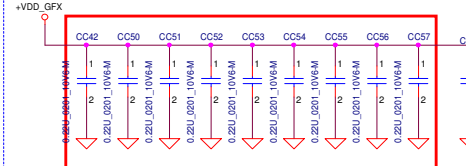
20151126

change from 0.22U_0402_10V6-K to 0201



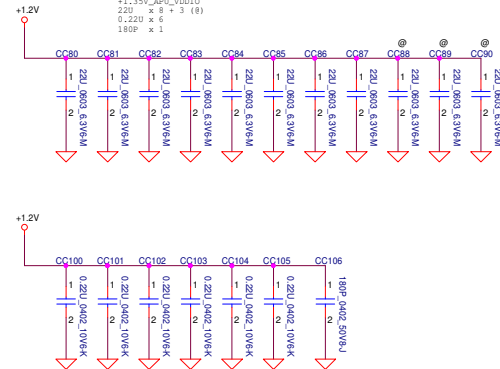
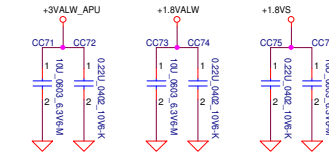
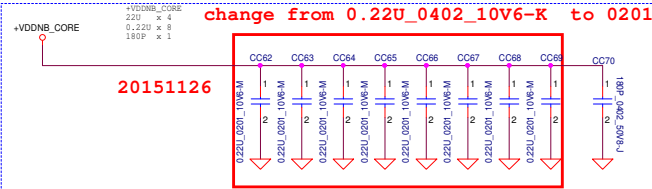
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change from 0.22U_0402_10V6-K to 0201

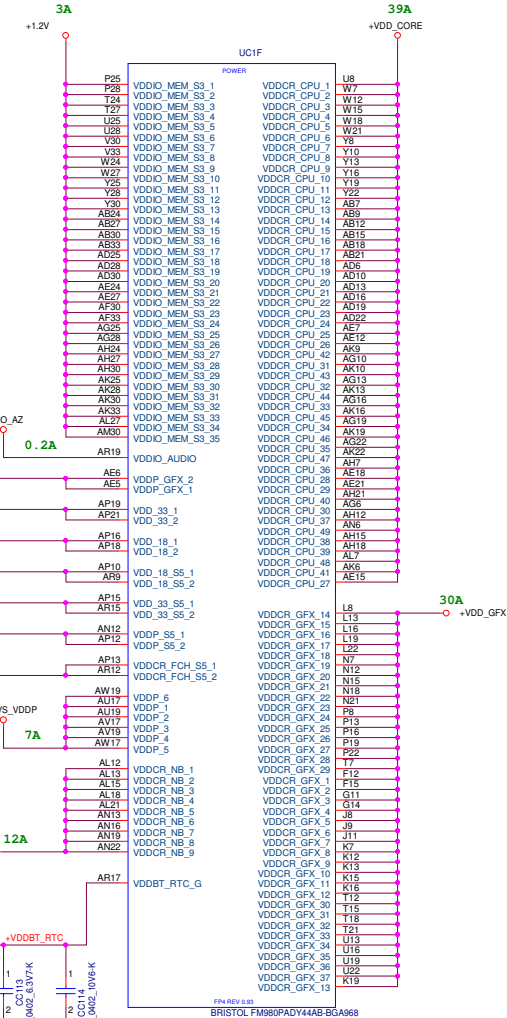
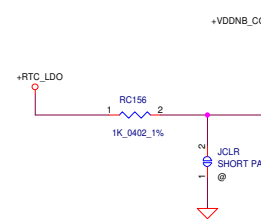
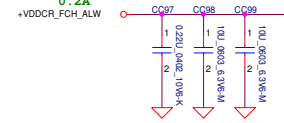
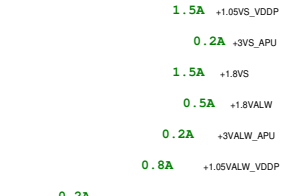
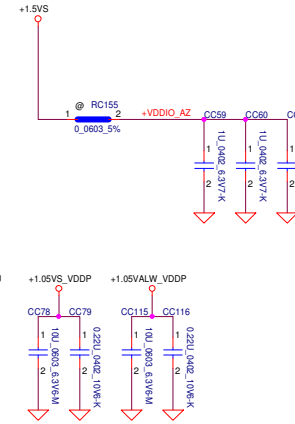
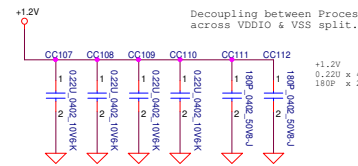


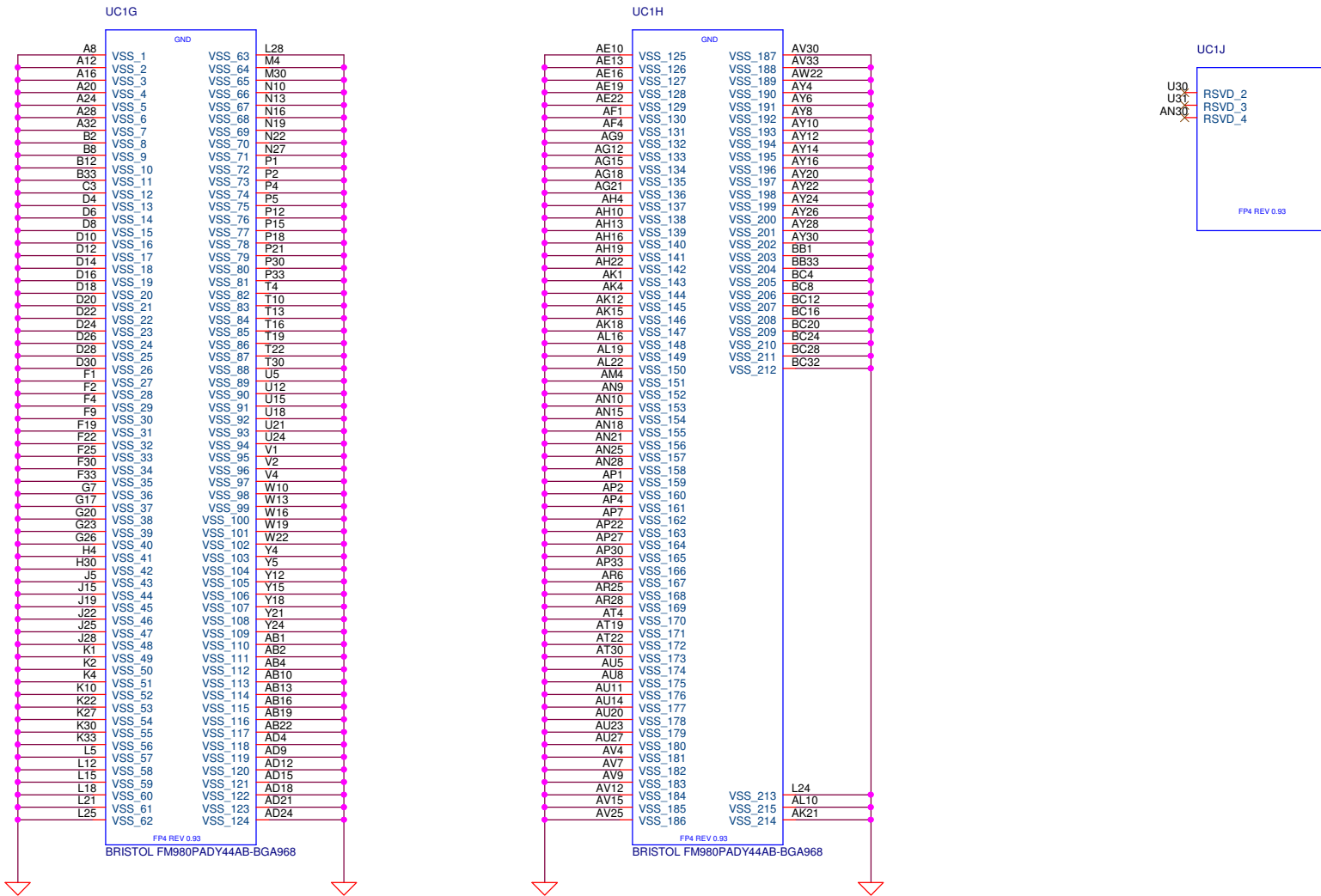
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change from 0.22U_0402_10V6-K to 0201




Decoupling between Processor & DIMMs across VDDIO & VSS split.

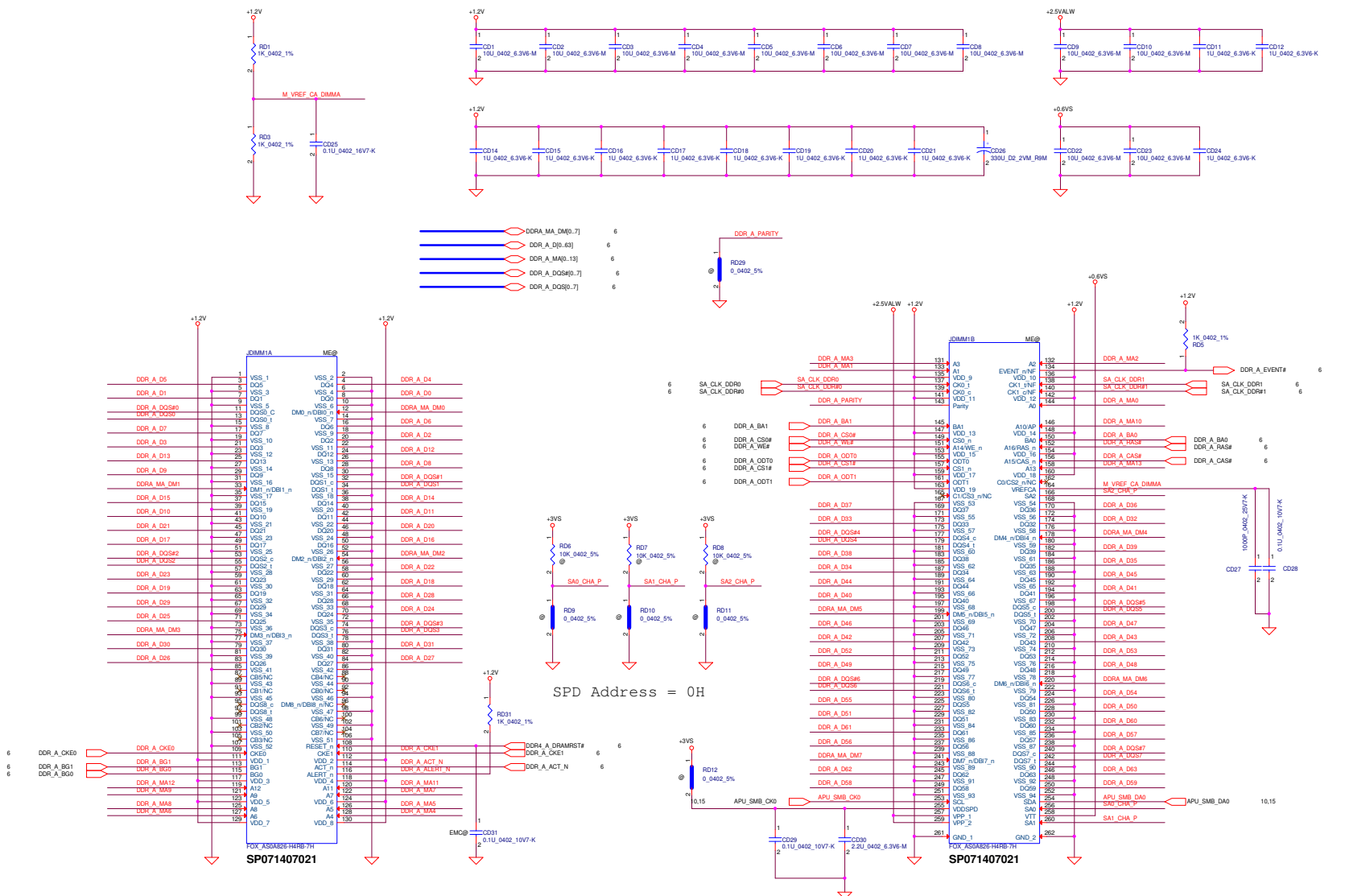


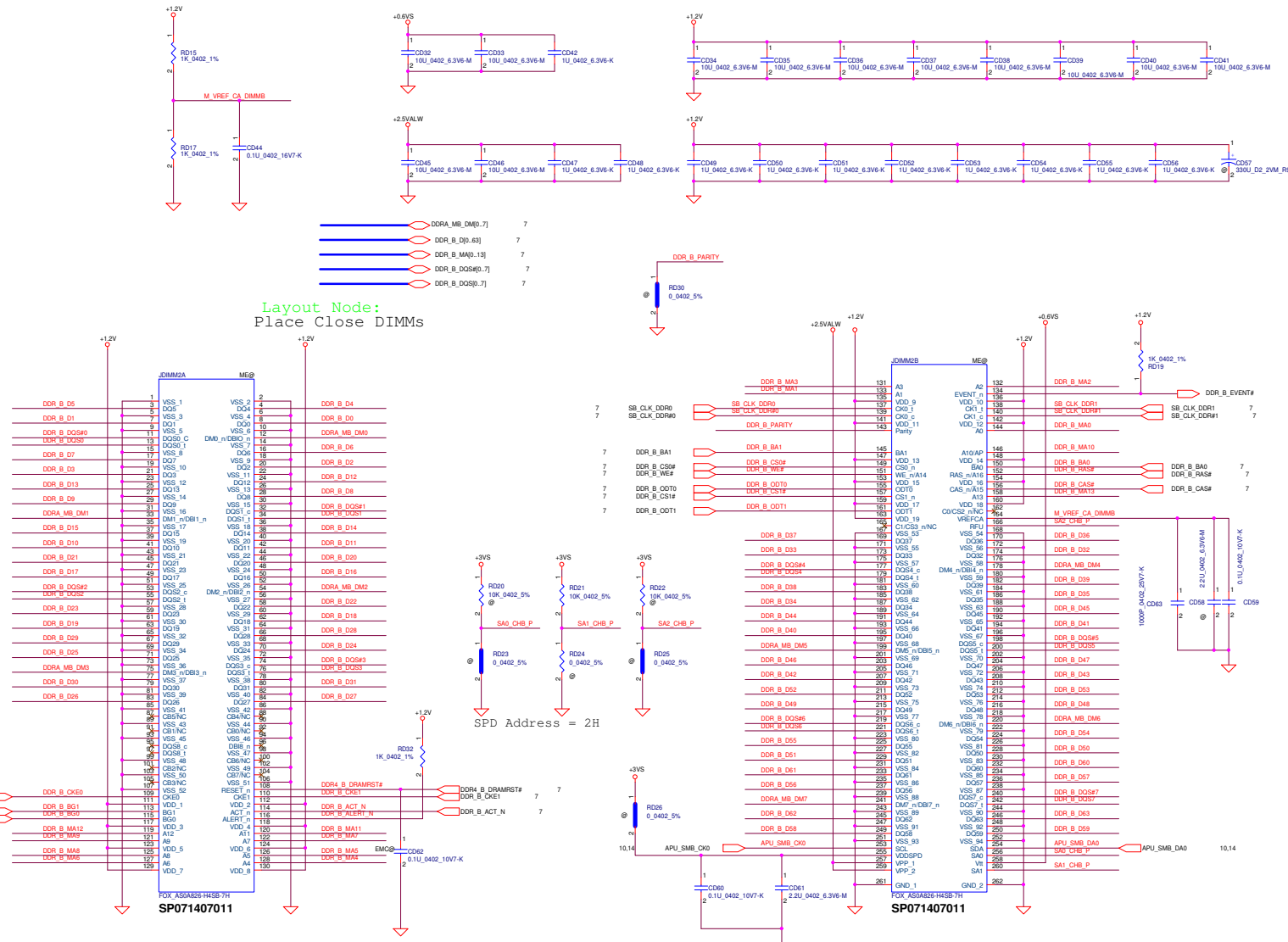


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5	PCIE_CTX_GRX_N[0..3]	PCIE_CTX_GRX_N[0..3]
5	PCIE_CTX_GRX_P[0..3]	PCIE_CTX_GRX_P[0..3]
5	PCIE_CRX_GTX_N[0..3]	PCIE_CRX_GTX_N[0..3]
5	PCIE_CRX_GTX_P[0..3]	PCIE_CRX_GTX_P[0..3]

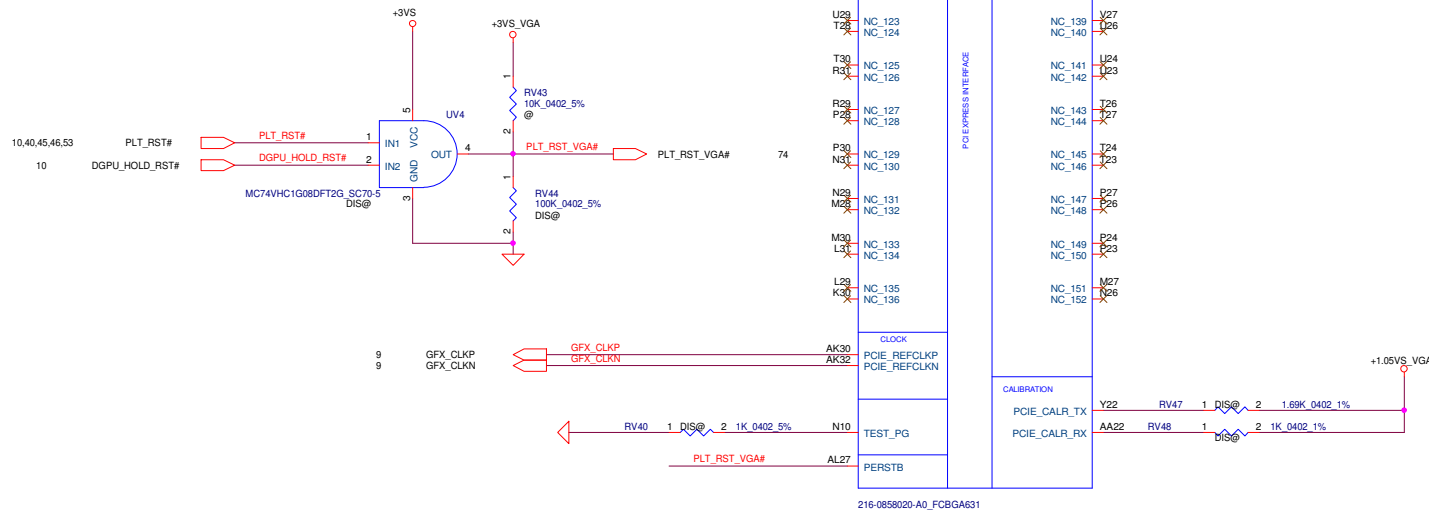
DIS@ support GEN3; 20151120

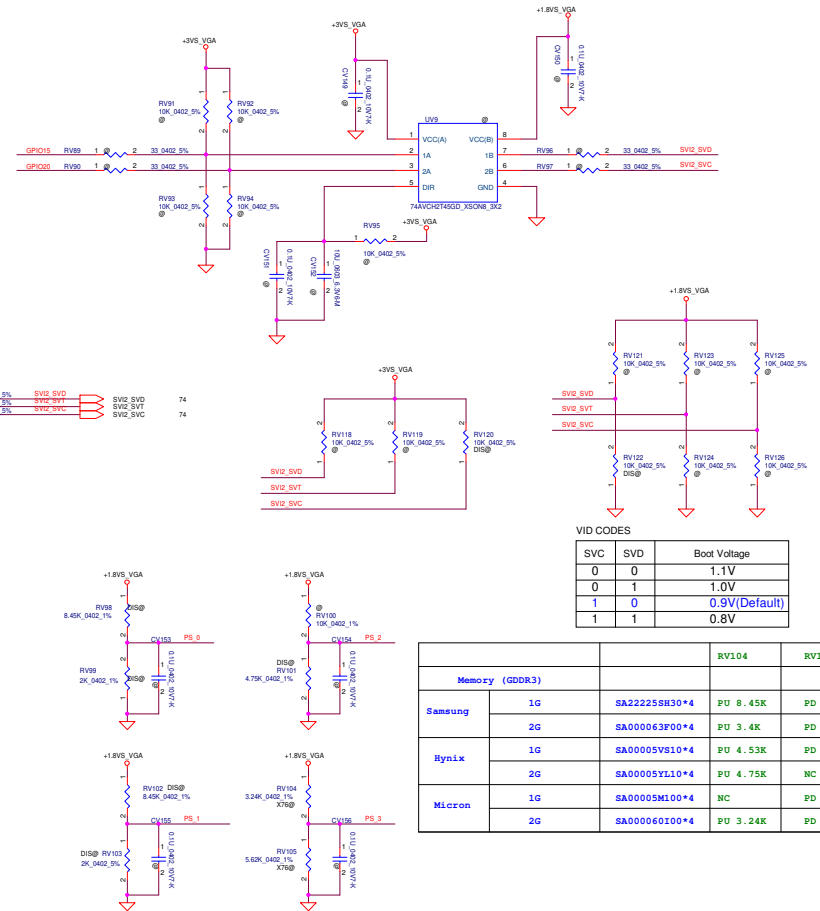
PCIE_CTX_GRX_P0	CV132	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P0
PCIE_CTX_GRX_N0	CV133	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N0
PCIE_CTX_GRX_P1	CV134	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P1
PCIE_CTX_GRX_N1	CV135	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N1
PCIE_CTX_GRX_P2	CV136	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P2
PCIE_CTX_GRX_N2	CV137	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N2
PCIE_CTX_GRX_P3	CV138	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_P3
PCIE_CTX_GRX_N3	CV139	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CTX_C_GRX_N3

DIS@

support GEN3;20151920




PCIE_CRX_GTX_P0	CV191	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P0
PCIE_CRX_GTX_N0	CV192	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N0
PCIE_CRX_GTX_P1	CV193	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P1
PCIE_CRX_GTX_N1	CV194	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N1
PCIE_CRX_GTX_P2	CV195	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P2
PCIE_CRX_GTX_N2	CV196	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N2
PCIE_CRX_GTX_P3	CV197	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_P3
PCIE_CRX_GTX_N3	CV198	DIS@ 1	2 0.22U 0402 10V6-K	PCIE_CRX_C_GTX_N3

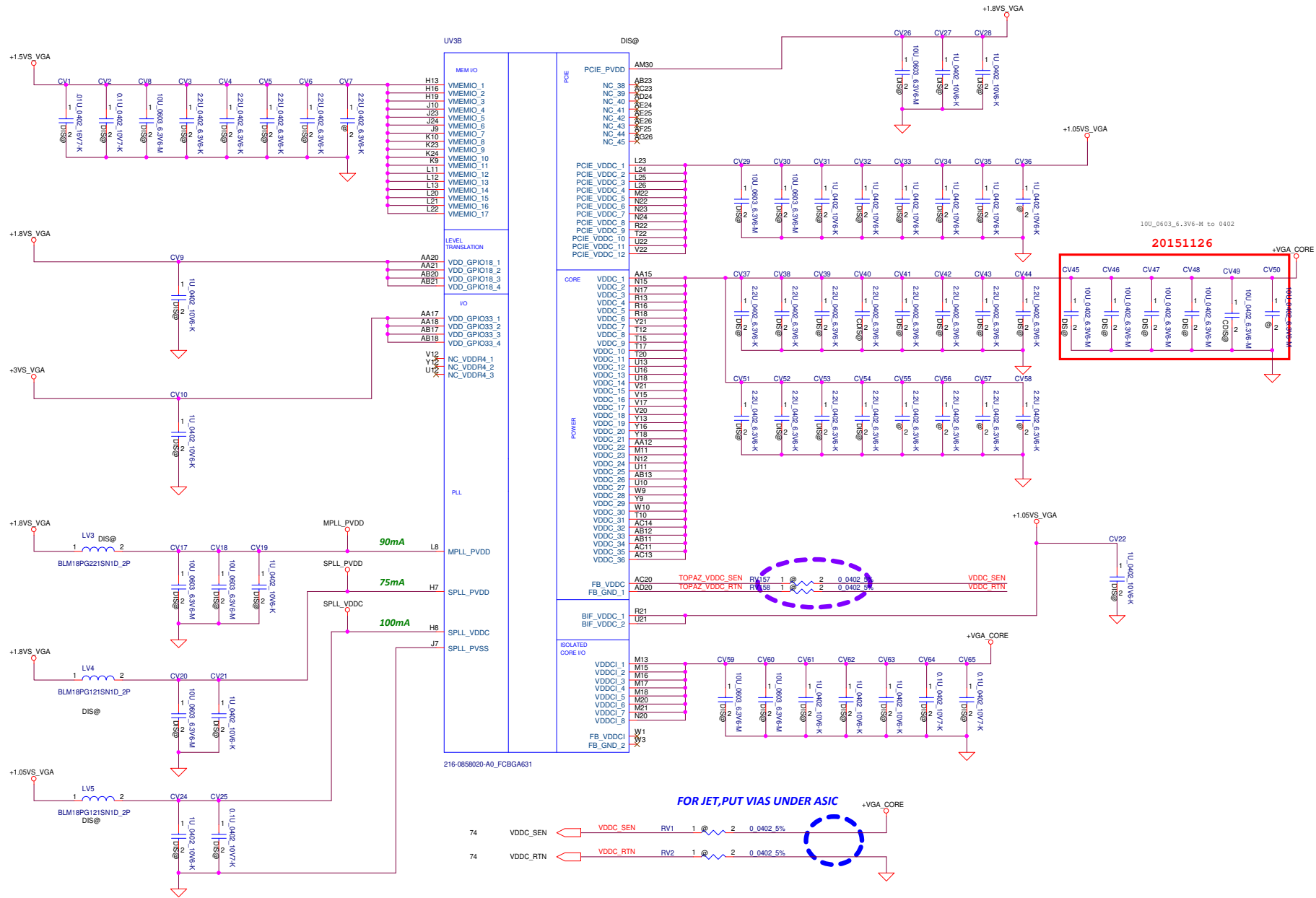




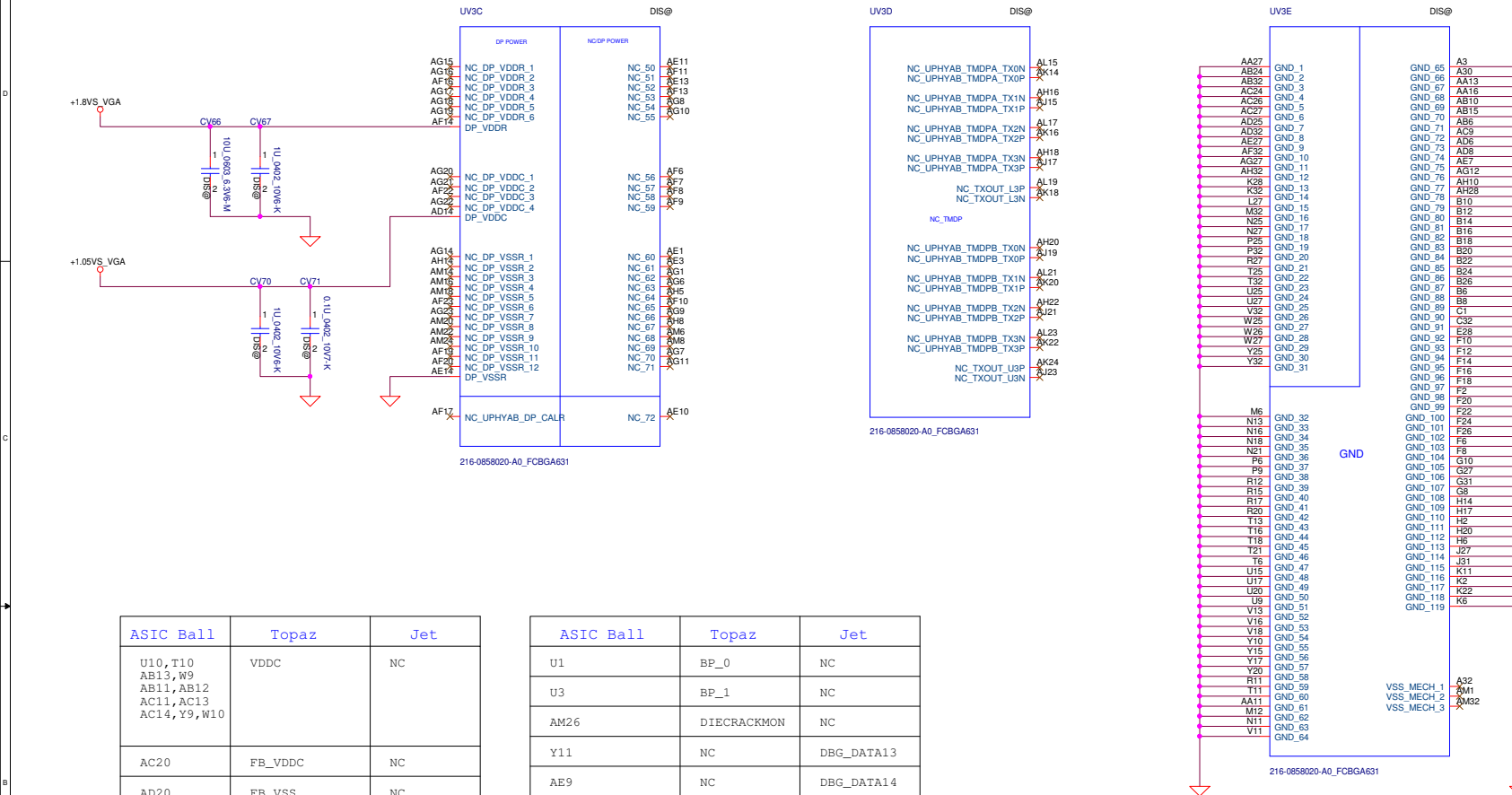
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

			RV104	RV105
	Memory (GDDR3)			
Samsung	1G	SA2225SH30*4	PU 6.45K	PD 2K
	2G	SA00063F00*4	PU 3.4K	PD 10K
Rynix	1G	SA00005YS10*4	PU 4.53K	PD 2K
	2G	SA00005YL10*4	PU 4.75K	NC
Micron	1G	SA00005ML00*4	NC	PD 4.75K
	2G	SA00006I00*4	PU 3.24K	PD 5.62K

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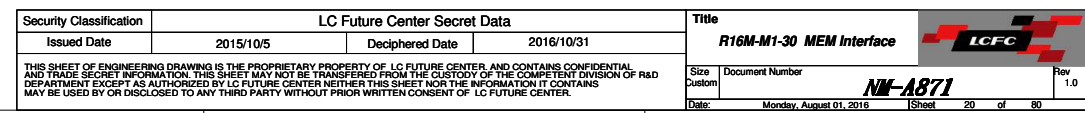


ASIC Ball	Topaz	Jet
U10, T10 AB13, W9 AB11, AB12 AC11, AC13 AC14, Y9, W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

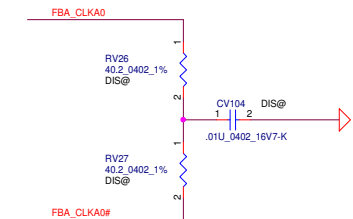
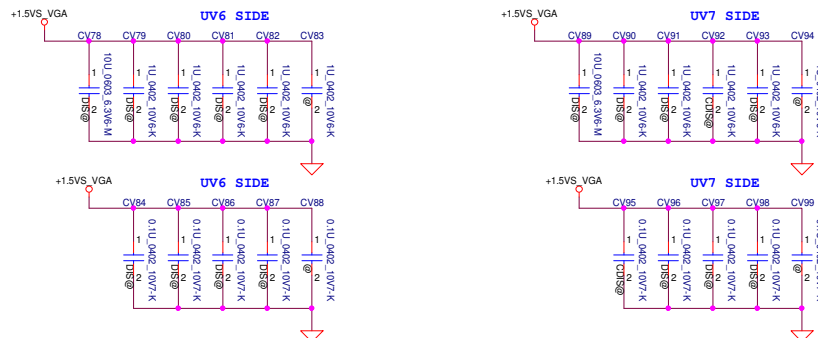
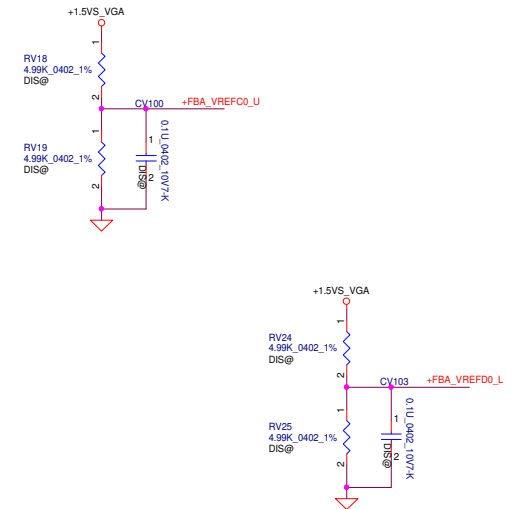
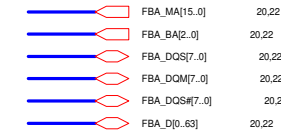
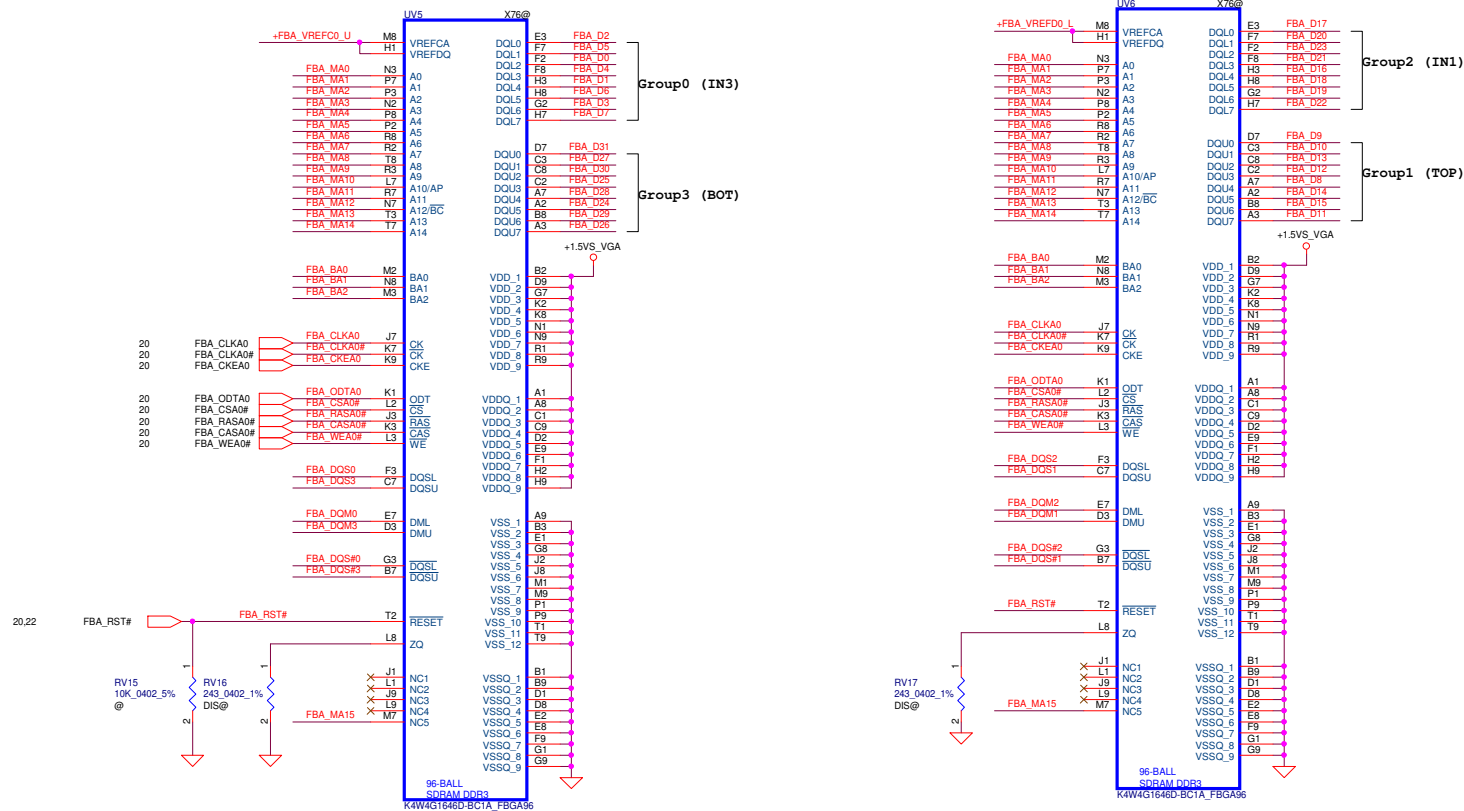
ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13, H16, H19, J10 J23, J24, J9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VMEMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT

	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	0	0	1	1	1
PS2	0	0	0	0	0
PS3	1	1	?	?	?

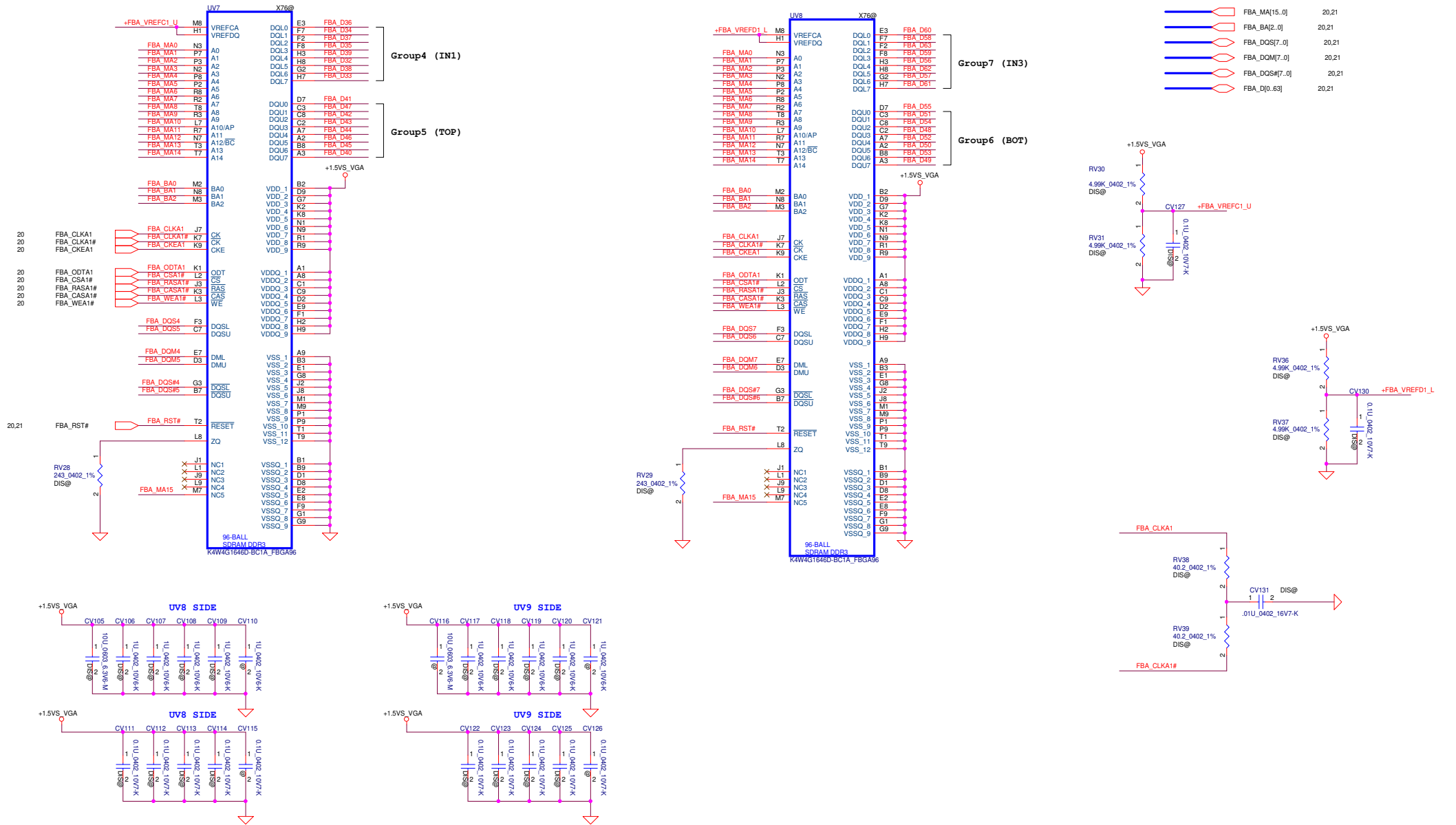
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/10/5	Deciphered Date	2016/10/31	R16M-M1-30 DP Power/GND	
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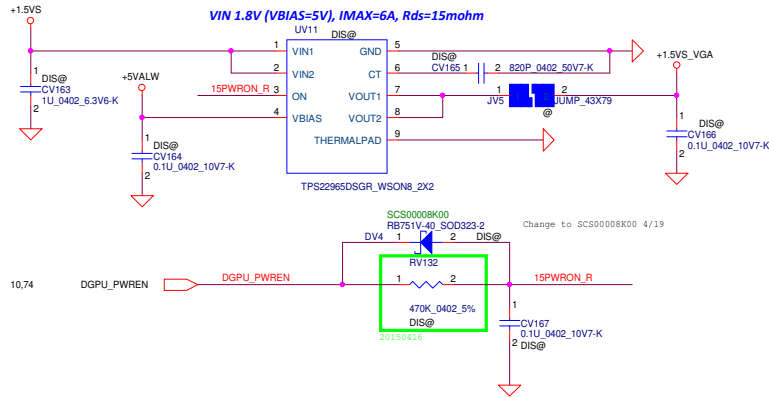
Memory Partition A - Lower 32 bits



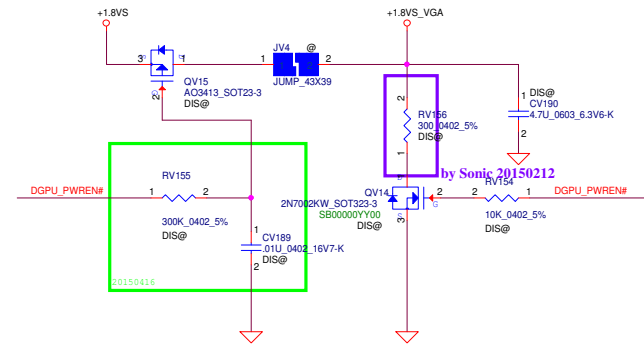
Memory Partition A - Upper 32 bits



+1.5VS to +1.5VS_VGA

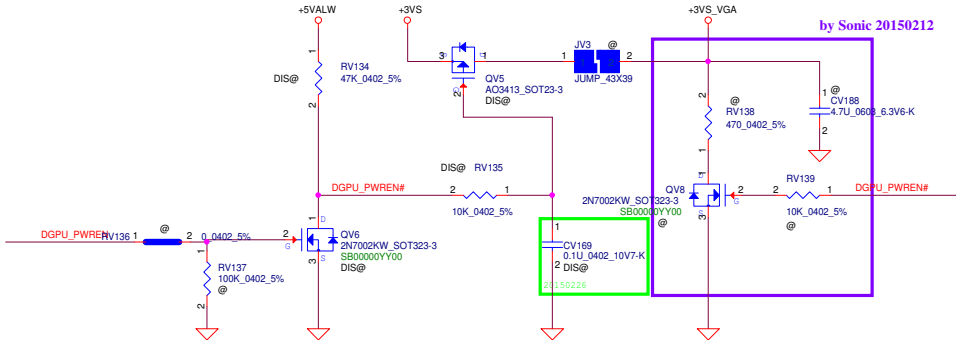


+1.8VS to +1.8VS_VGA

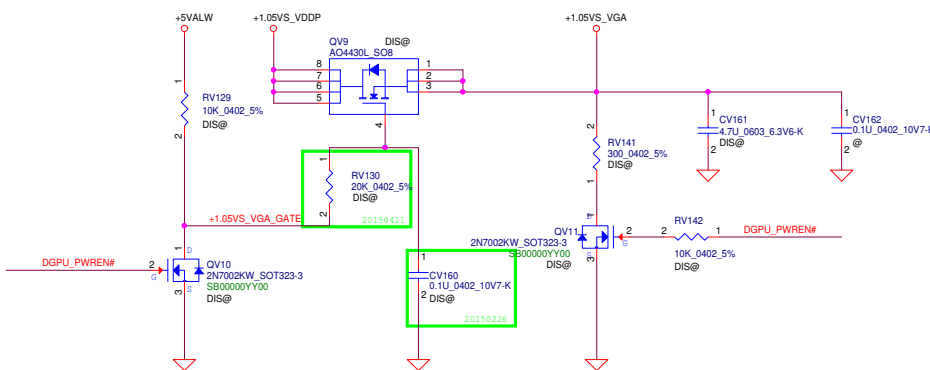


MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

+3VS to +3VS_VGA




+1.05VS_VDDP to ++1.05VS_VGA



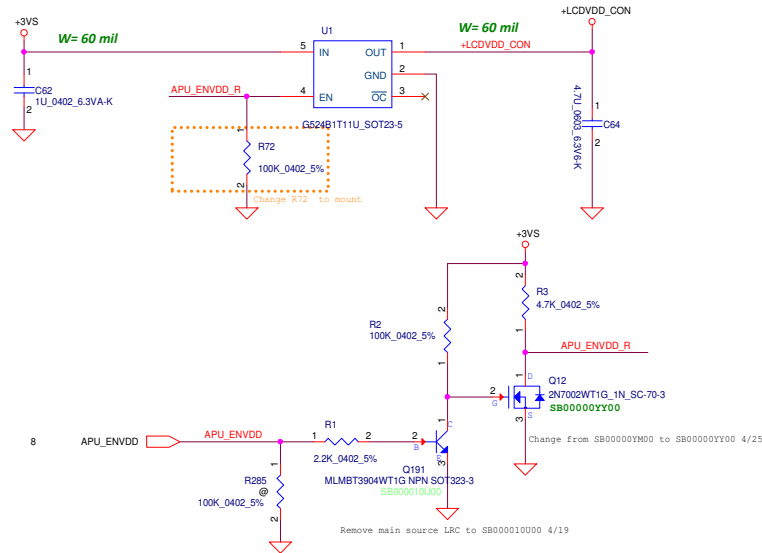
PS_0[1]	ROM_CONFIG[0]	STRAP BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[2]	ROM_CONFIG[1]	
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1]	BOARD_CONFIG[0]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[2]	BOARD_CONFIG[1]	
PS_3[3]	BOARD_CONFIG[2]	
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

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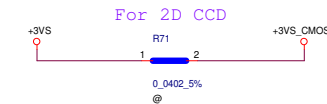
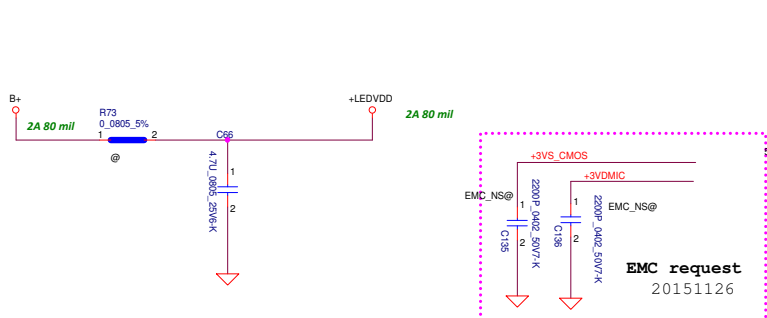
Security Classification		LC Future Center Secret Data		Title							
Issued Date		2015/10/5		Deciphered Date			2016/10/31				
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NW-A871

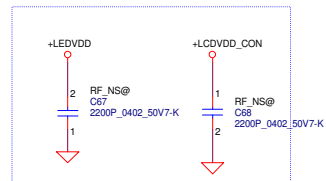
LCDVDD Circuit



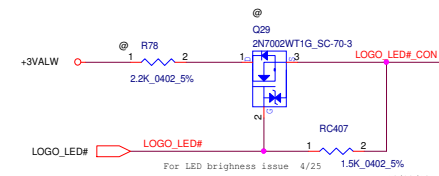
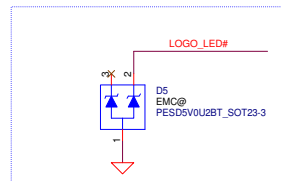
CMOS Camera

**eDP CONN.**

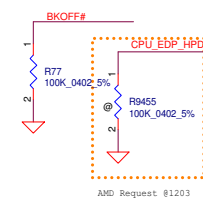
EMC request. Close to JLCD



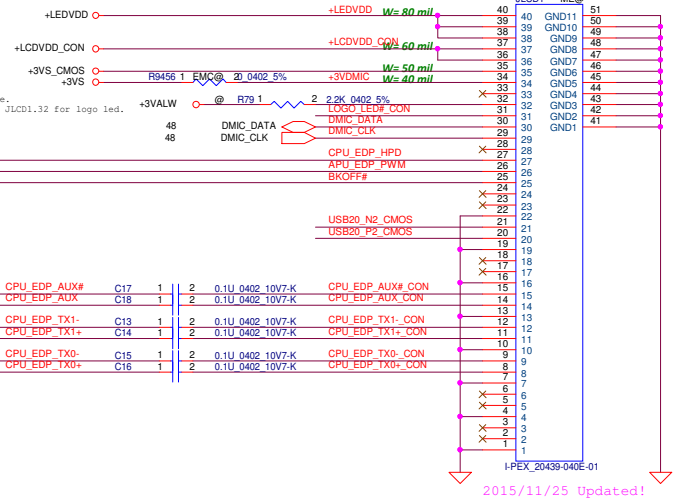
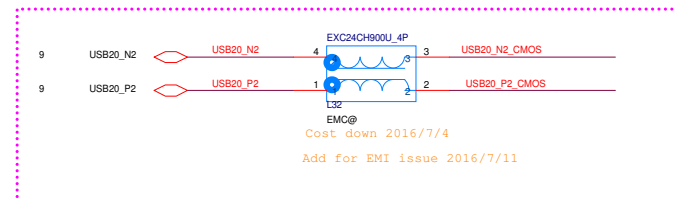
ESD request





16/02/13 LOGO_LED blink issue.
1. Reserve +3VALW and R79 on JLCD1.32 for logo led.
2. Reserve Q29 and R78.

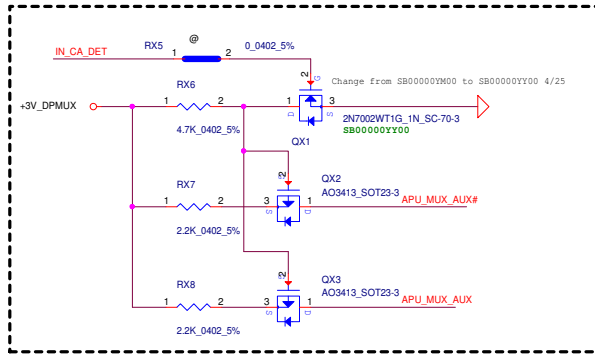
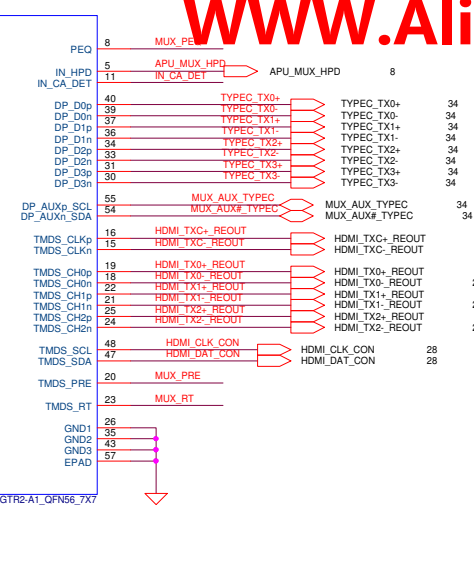
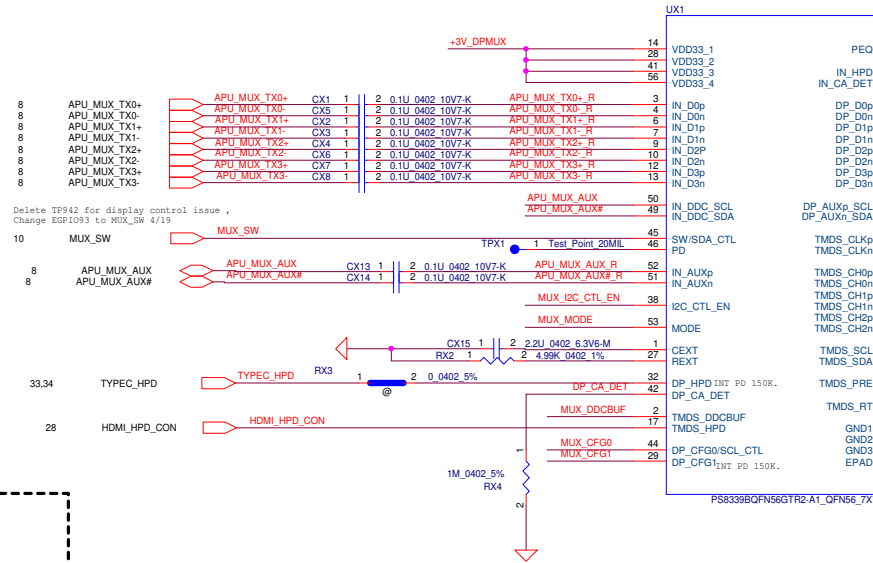
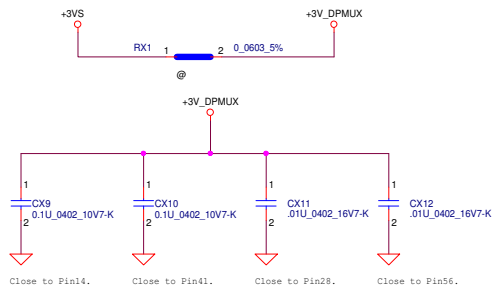


CMOS USB Port 2



2015/11/25 Updated!

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DP_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable

DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing.

MODE = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable

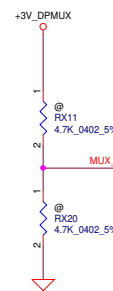
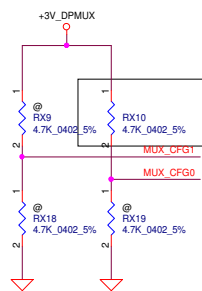
TMDS_PRE = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis

TMDS_RT = L: Standard open drain driver
= H: Open drain driver with termination resistors

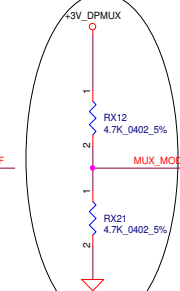
TMDS_DDCBUF = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2

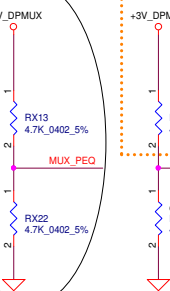
20151118 mount RX10



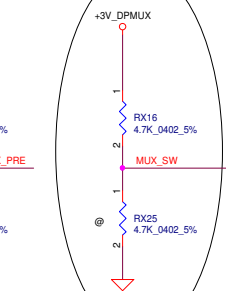
Automatic Switching Mode
HDMI ID enable



20151118 mount RX13&RX22



Auto mode, DP Higher Priority





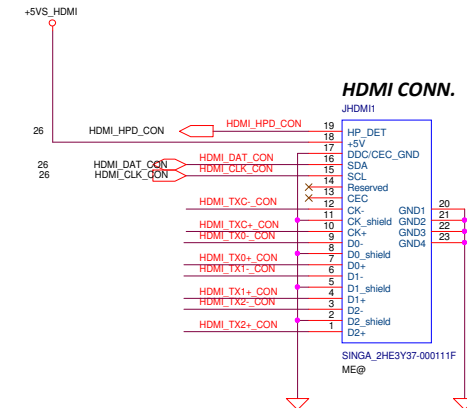
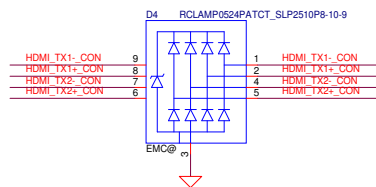
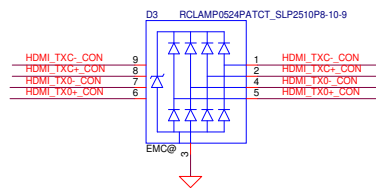
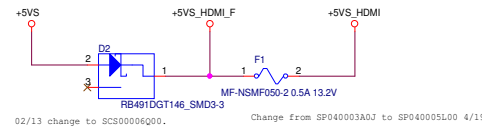
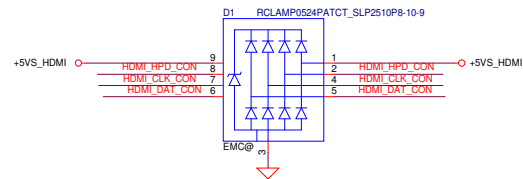
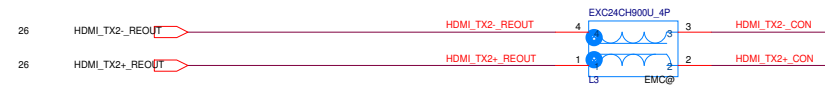
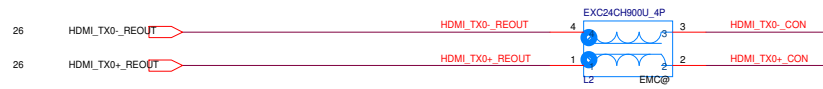
Delete TP942 for display control issue ,
Change EGP1093 to MUX_SW 4/19
Change RX16 to mount , RX25 to unmount

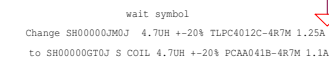
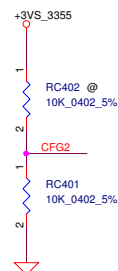
For Control Switching:
MUX_SW = L: DP output is selected
MUX_SW = H: TMDS output is selected
For Automatic Switching:
MUX_SW = L: DP output has higher priority.
MUX_SW = H: TMDS output has higher priority.

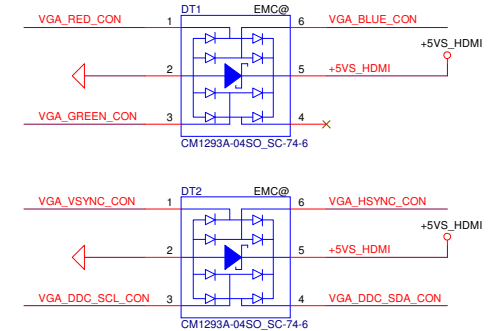
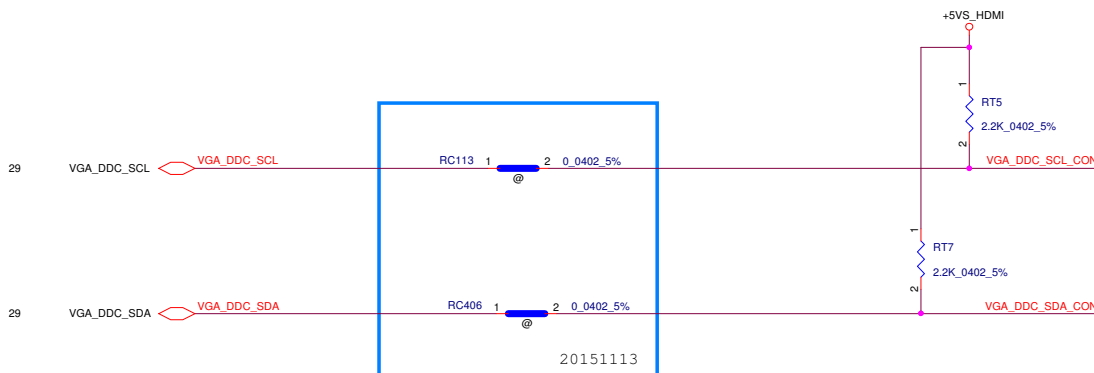
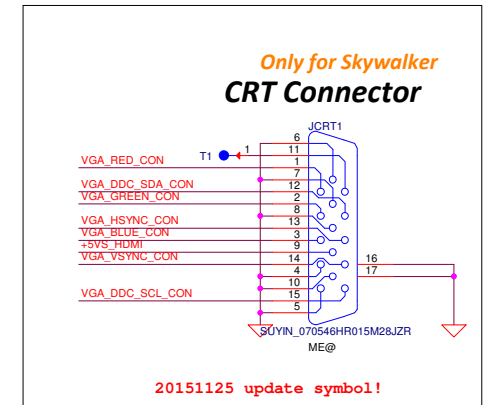
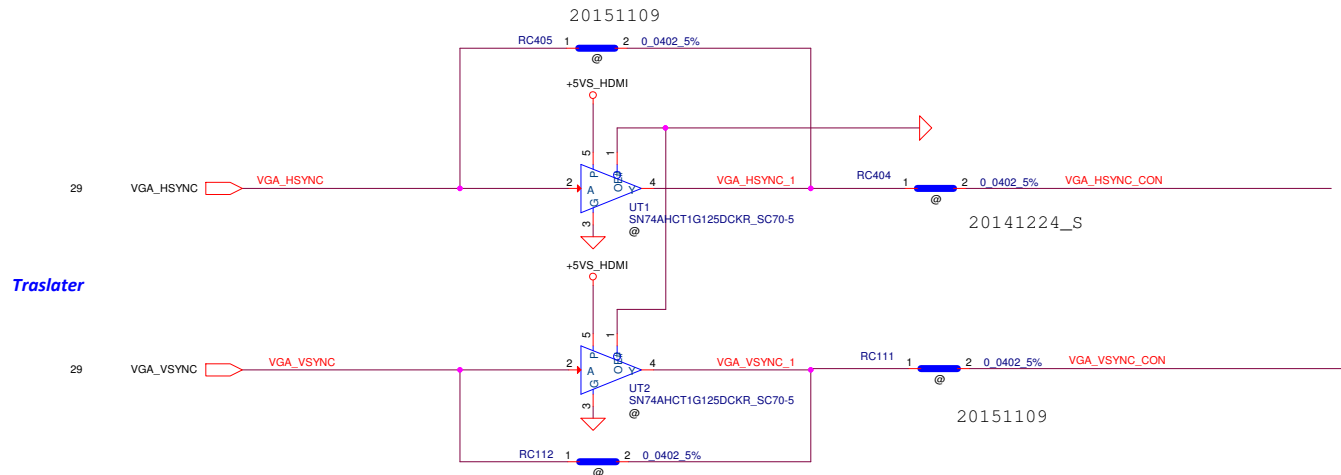
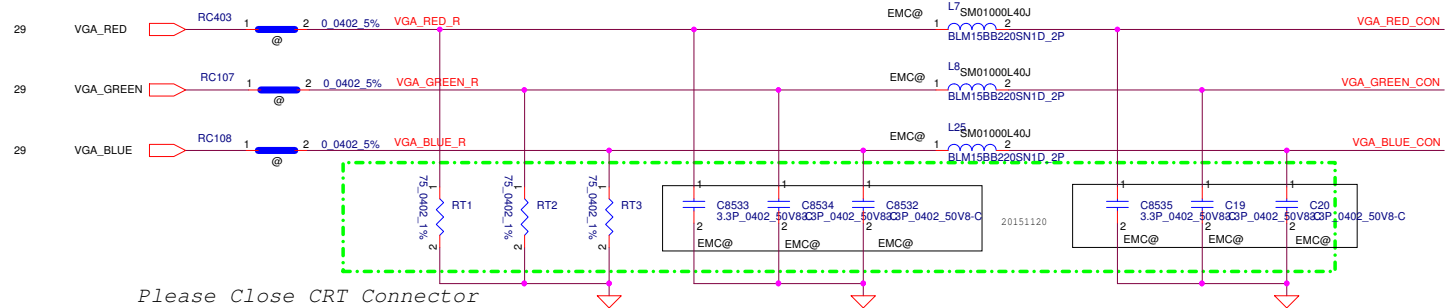
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Issued Date		2015/10/5		Deciphered Date	
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				Date:	Monday, August 01, 2016	Sheet	27 of 80






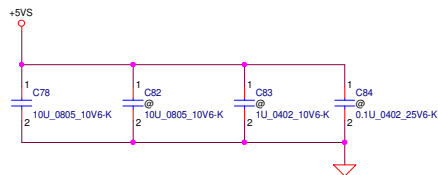


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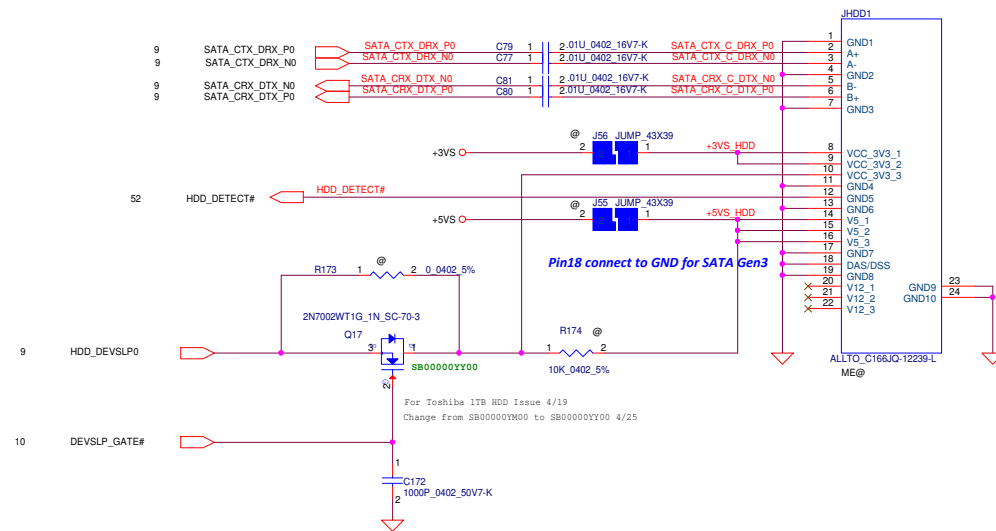
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Custom		NW-A871		Sheet 31 of 80		1.0

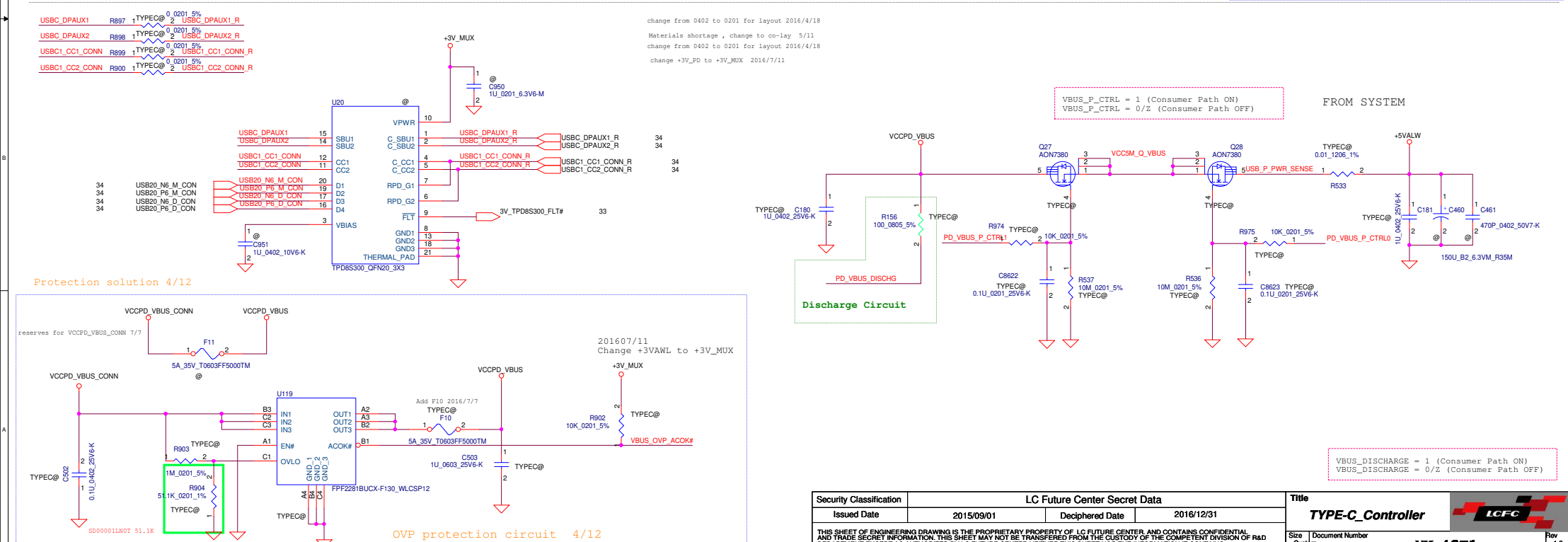
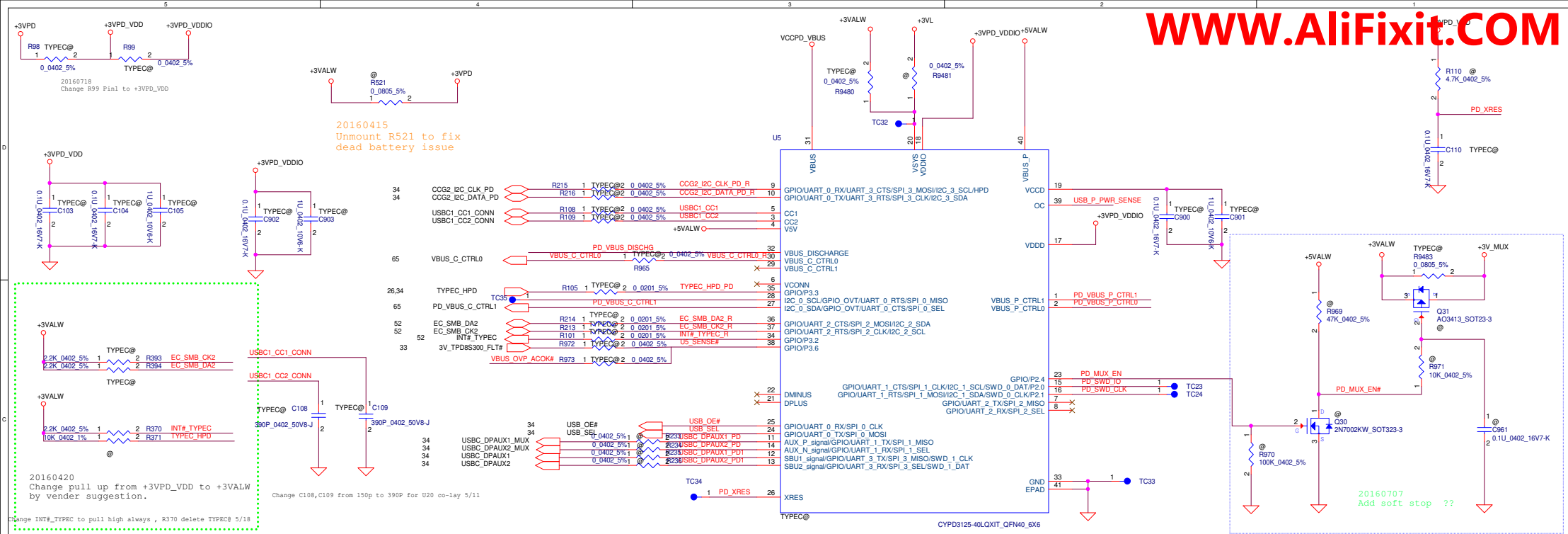
SATA HDD CONN.

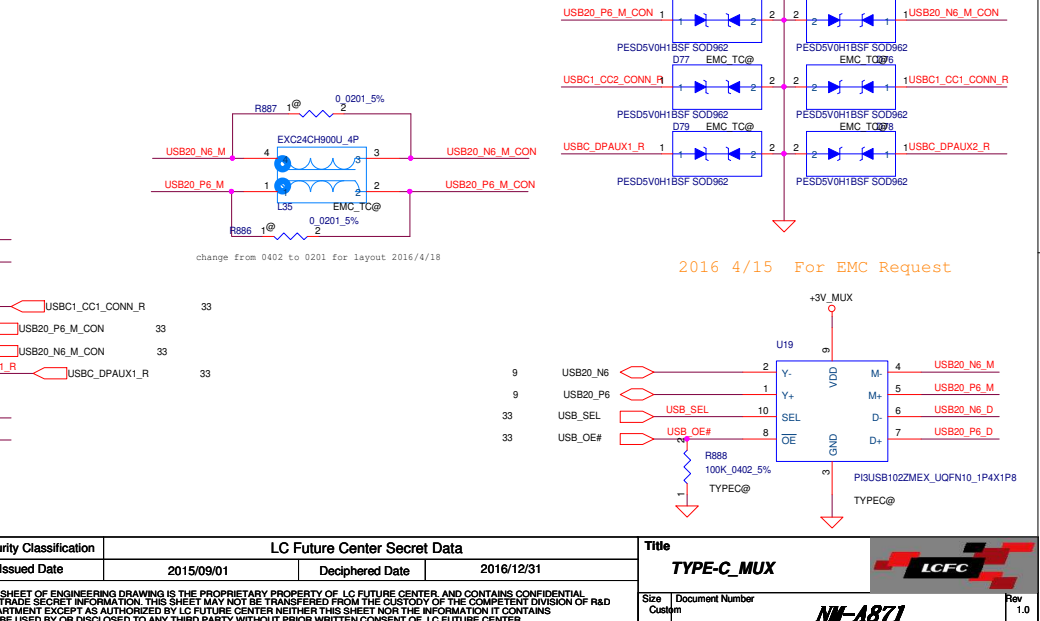
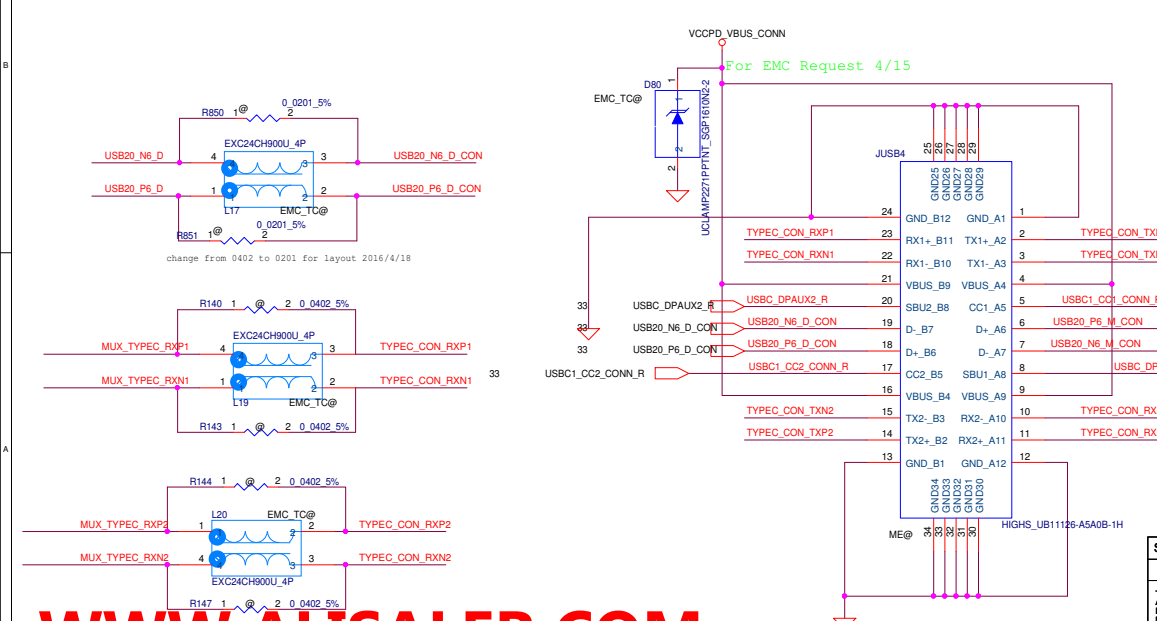
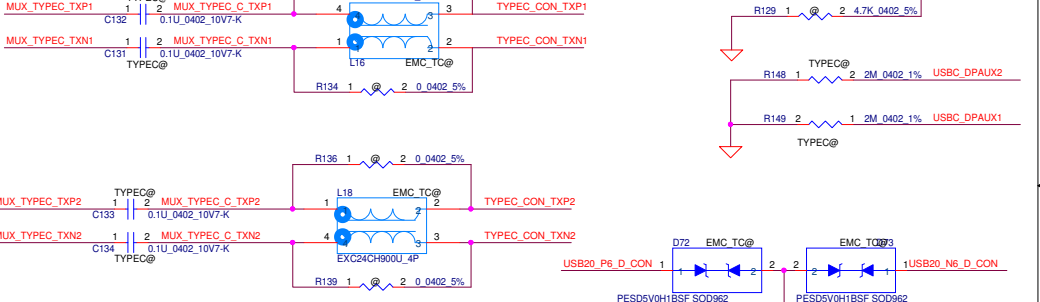
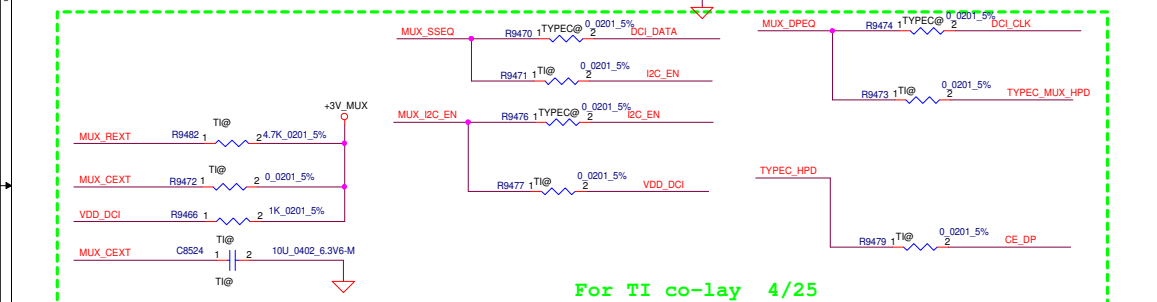
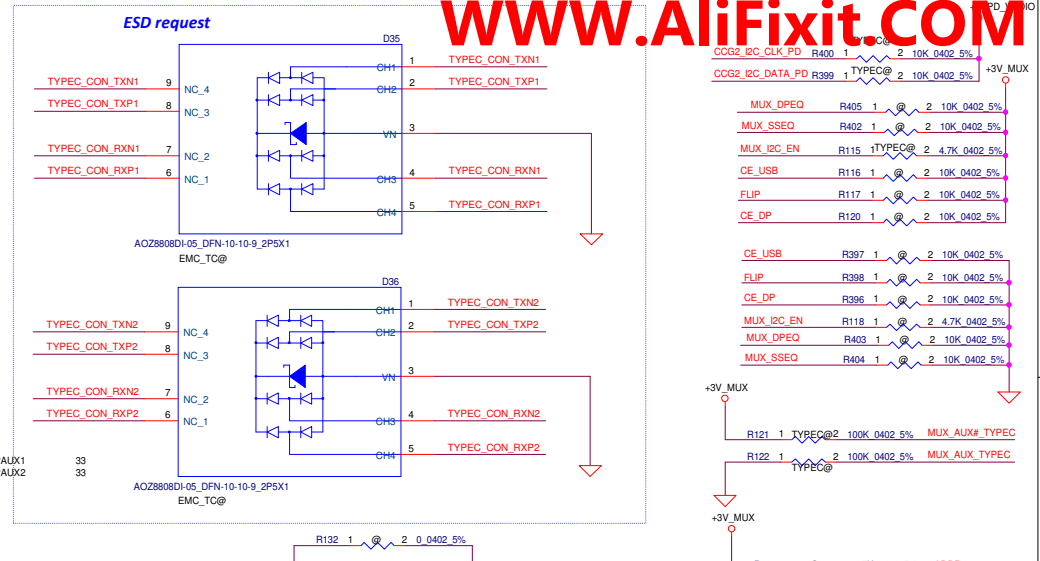
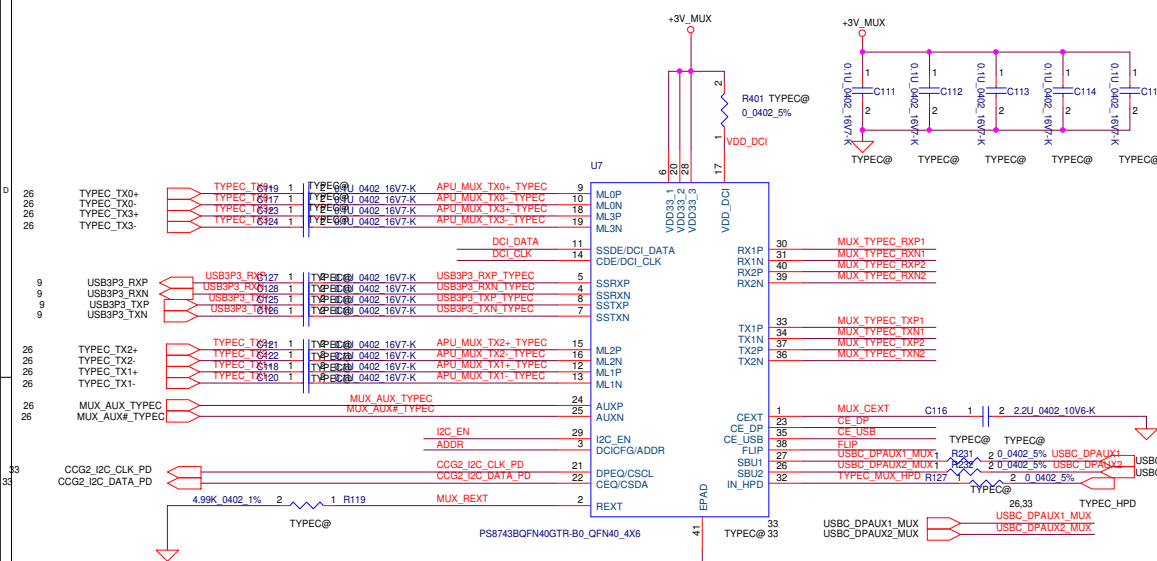



SATA HDD CONN.




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						1.0		Monday, August 01, 2016		NW-A871	






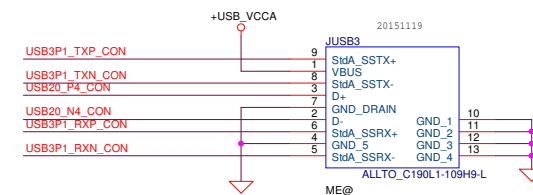
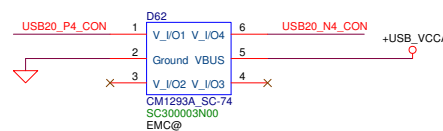
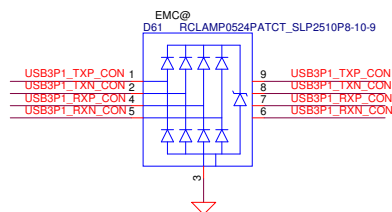
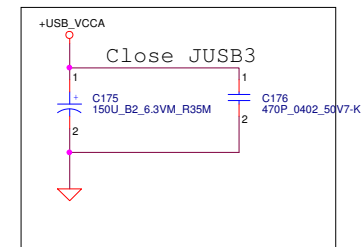
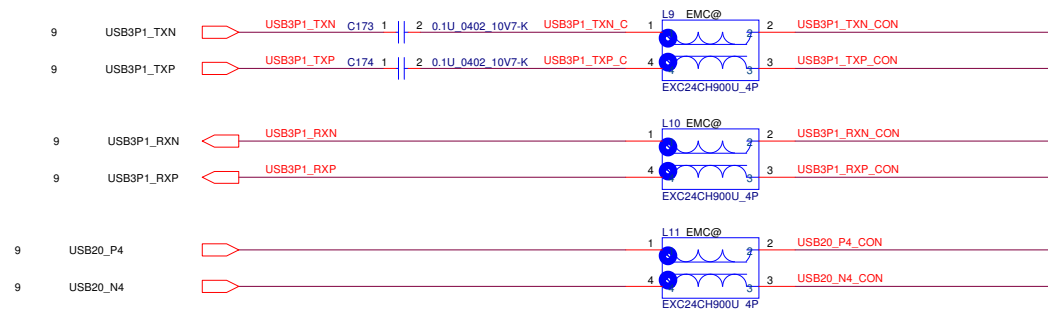
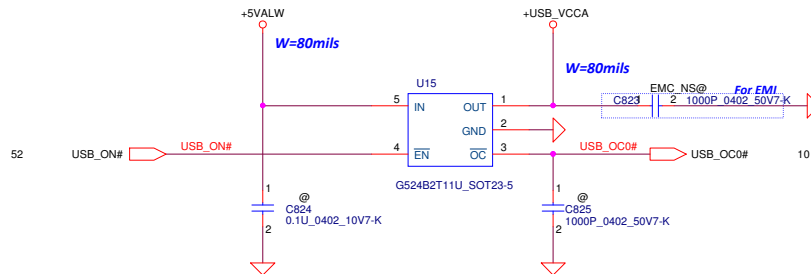
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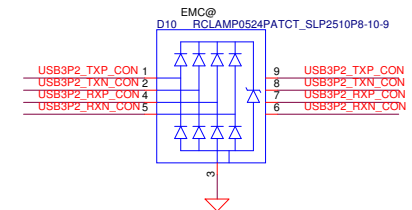
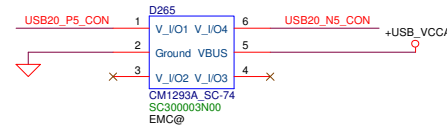
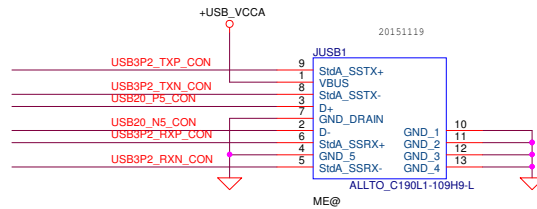
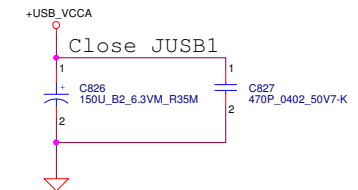
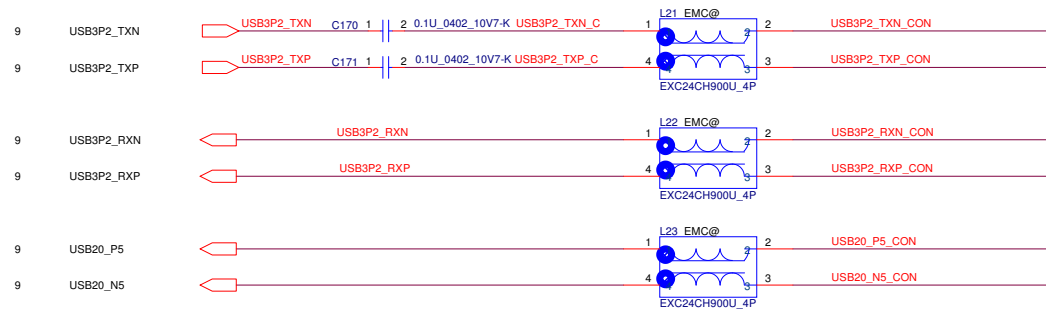
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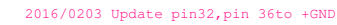
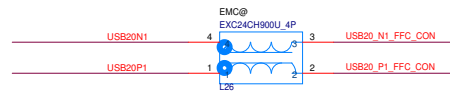
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20151117



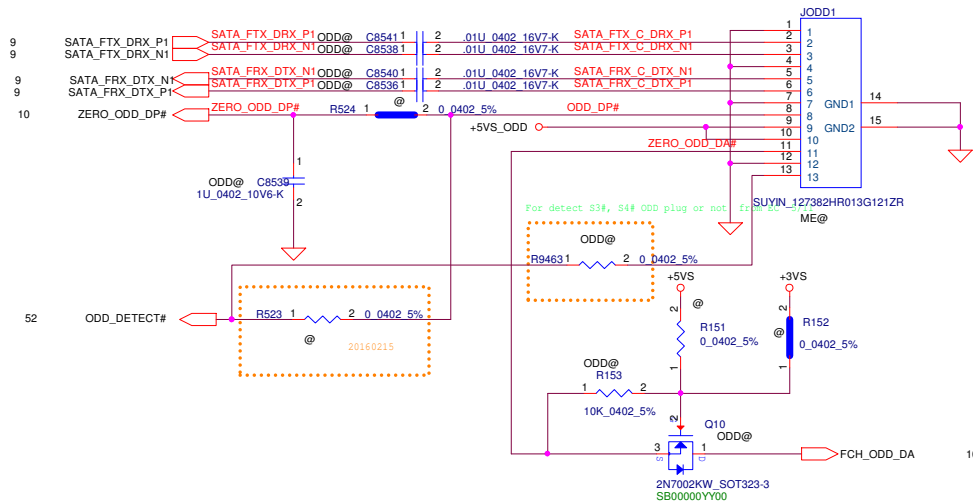
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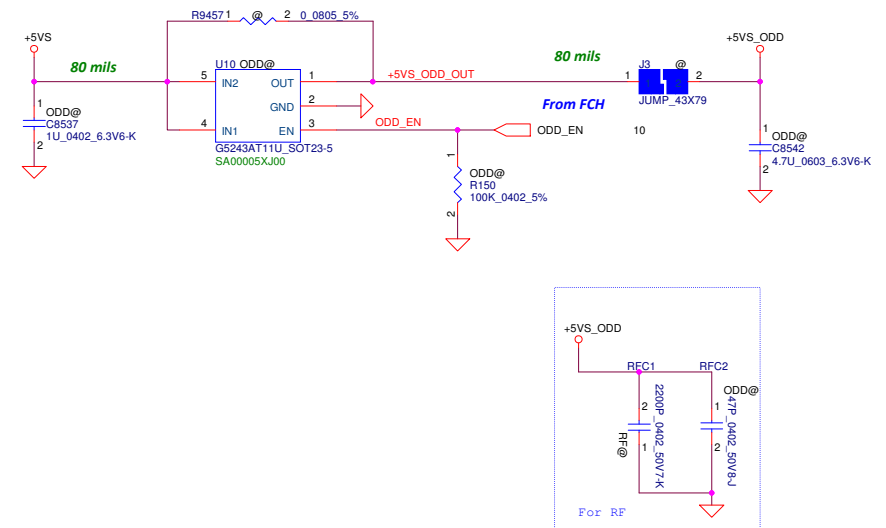


SATA ODD & ODD Power Control

Only for Skywalker



+5VS TO +5VS_ODD



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20151110

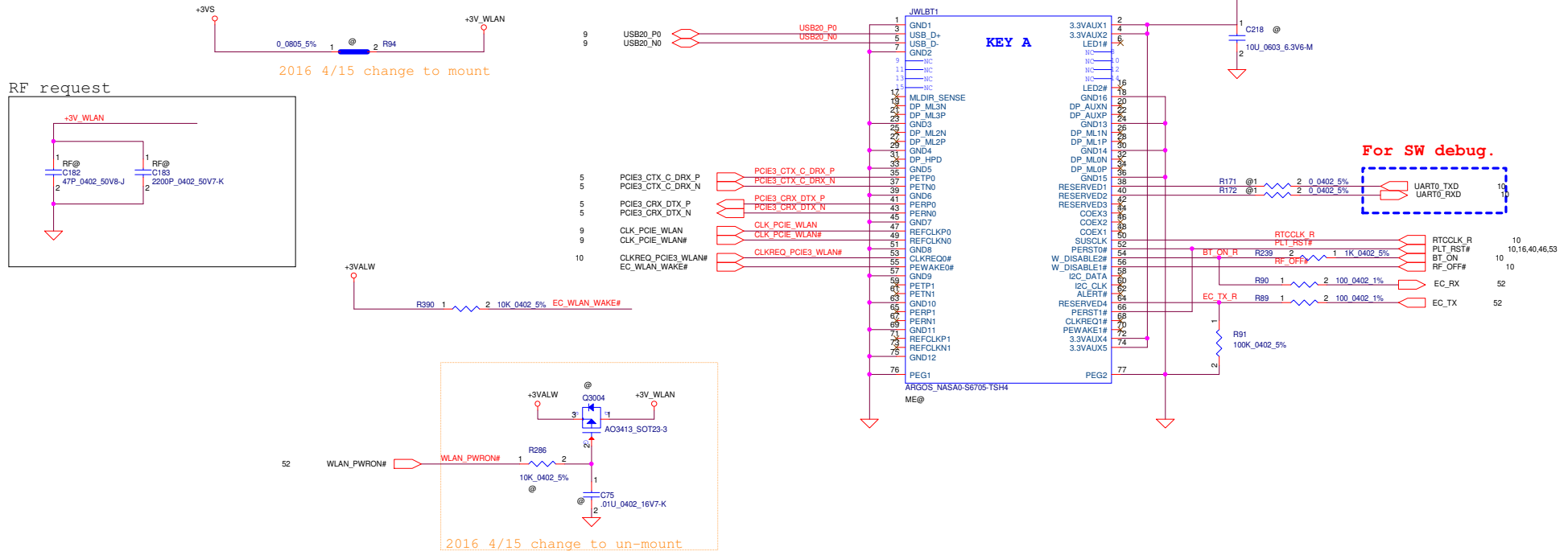
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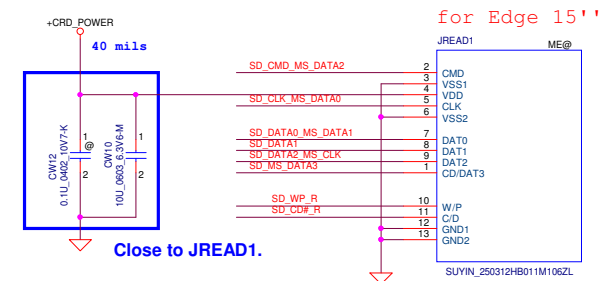
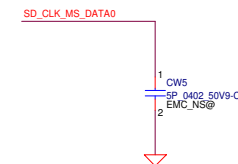
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TYPE-A NGFF CCARD FOR WLAN 3.2H CONNECTOR




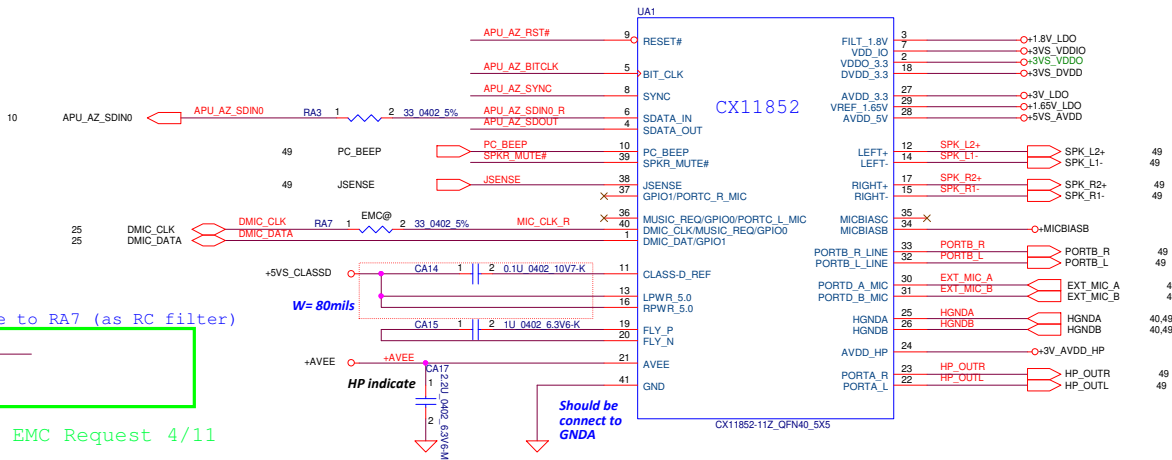
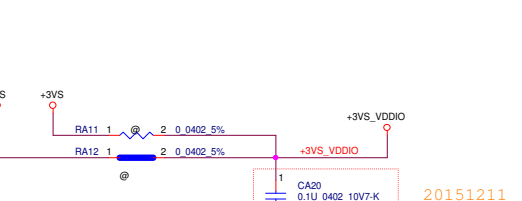
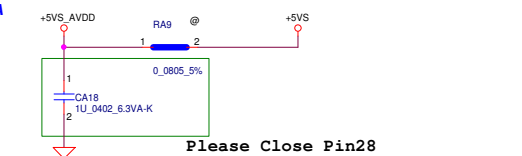
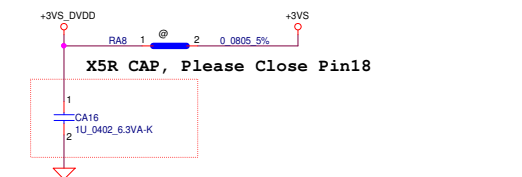
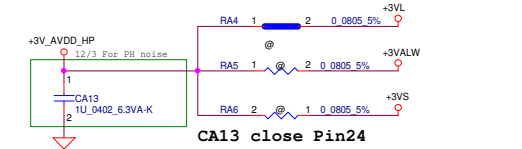
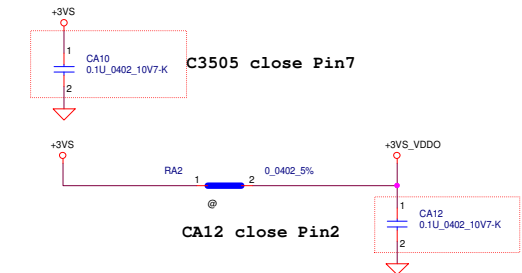
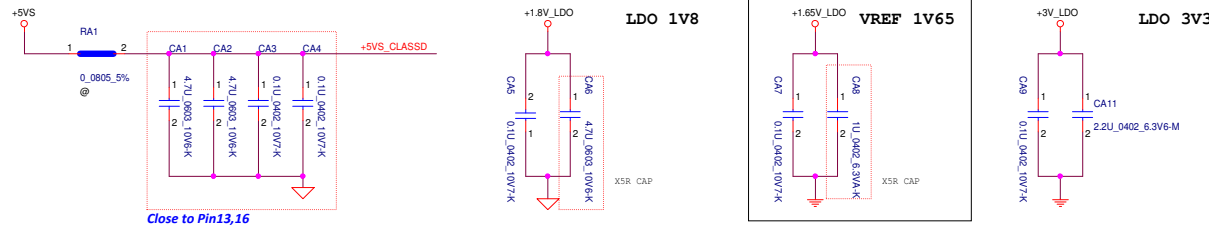
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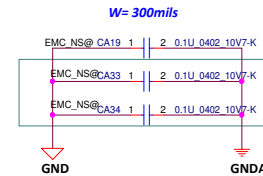
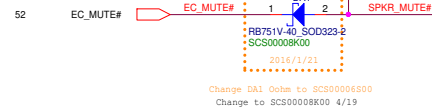
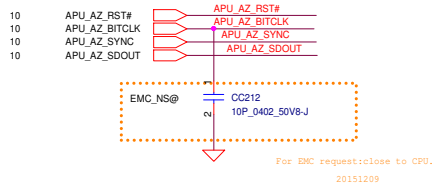
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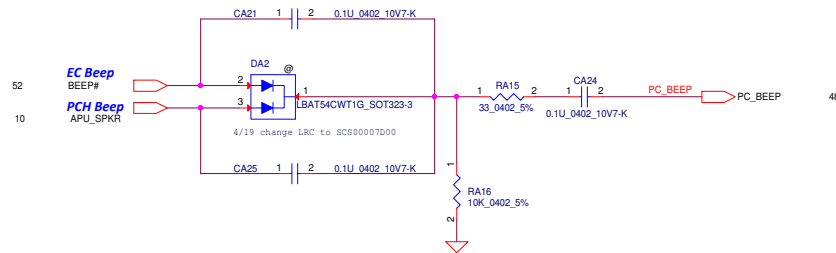


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Nokia --> EXT_MIC_B, HGND A

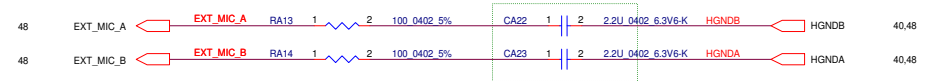


Base on EMC request
2015/11/25

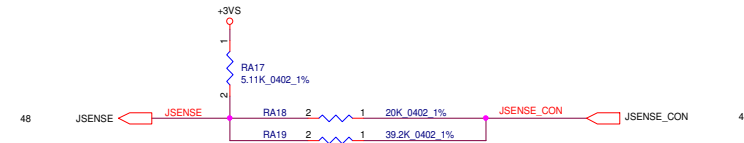
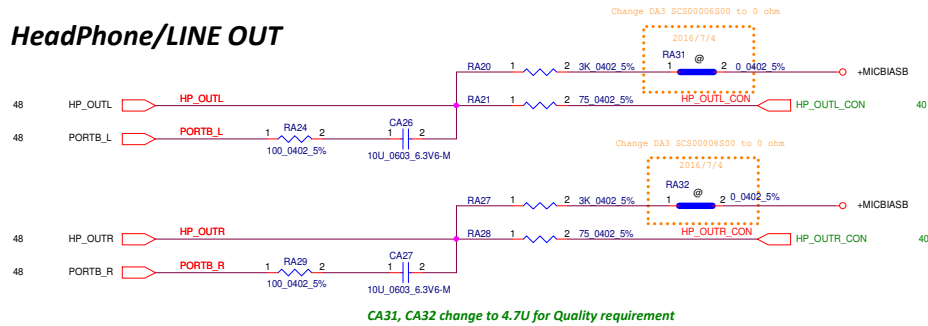
PC Beep



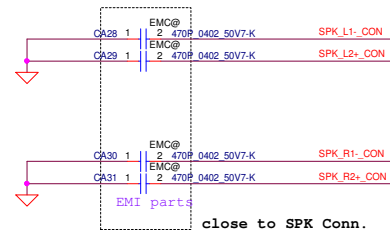
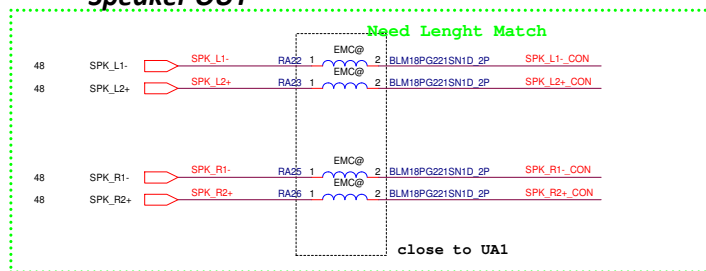
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Nokia --> EXT_MIC_B, HGND A



HeadPhone/LINE OUT

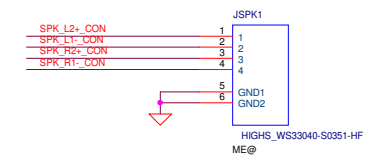


Speaker OUT



SPK CONN.

ME update PN




Change SPK conn. to 4 pins.


20151119

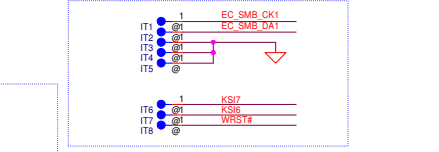
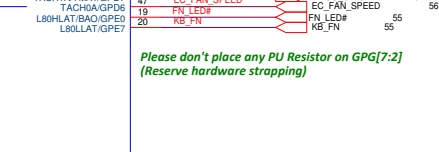
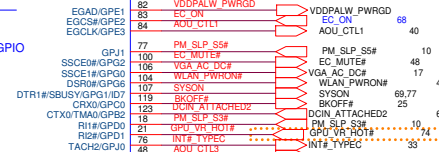
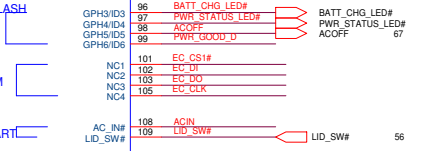
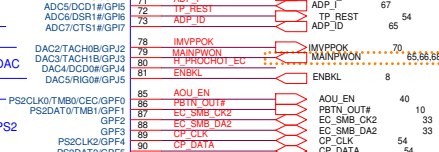
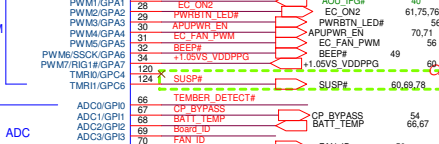
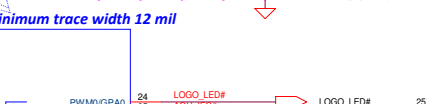
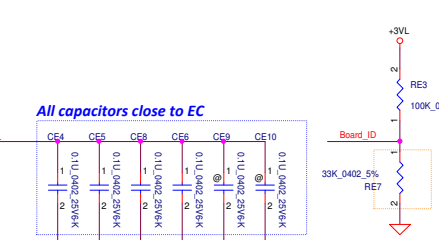
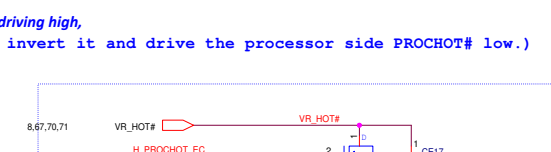
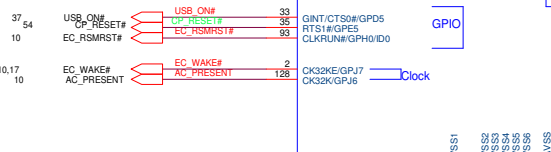
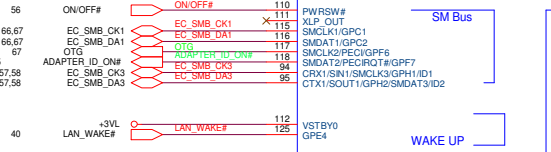
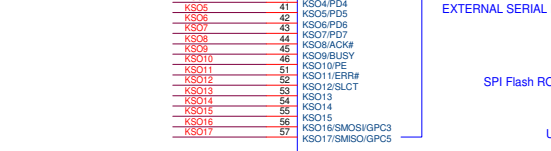
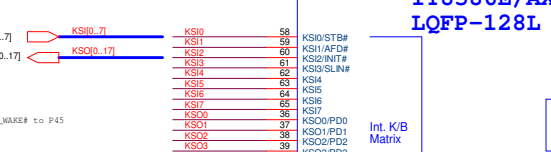
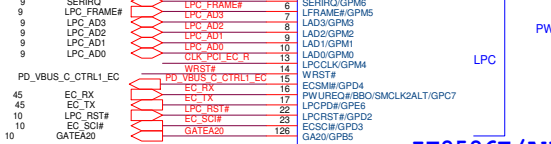
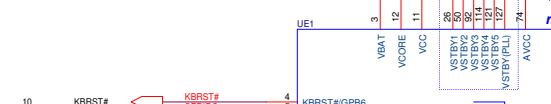
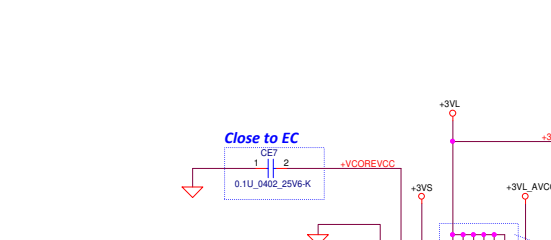
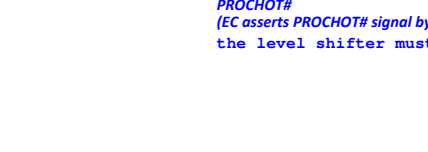
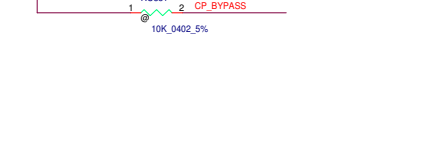
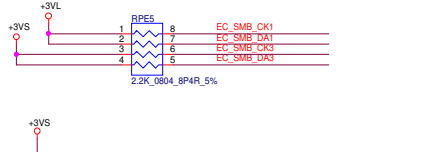
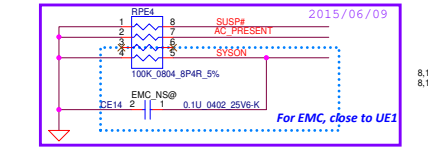
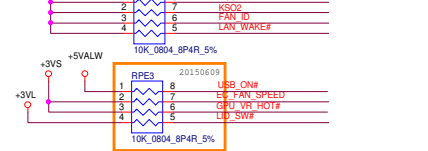
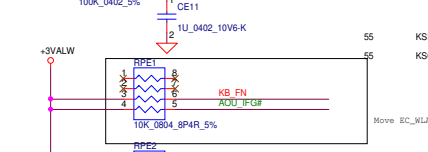
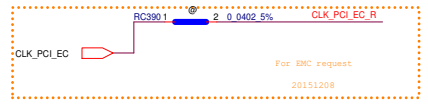
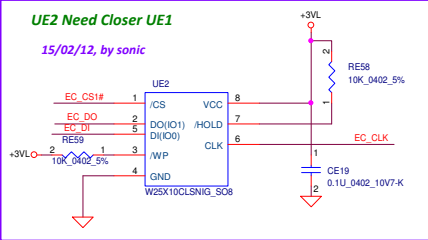
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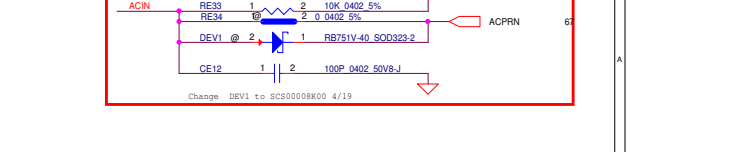
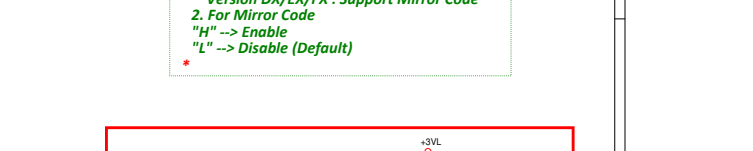
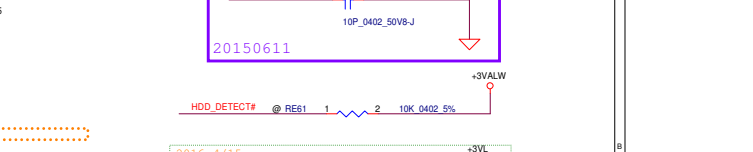
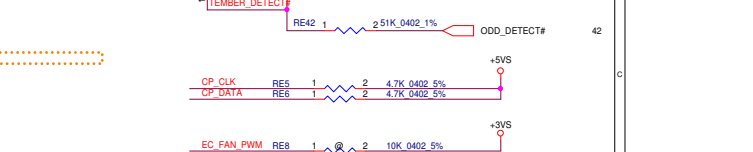
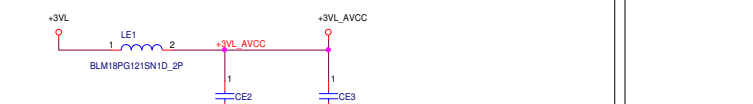
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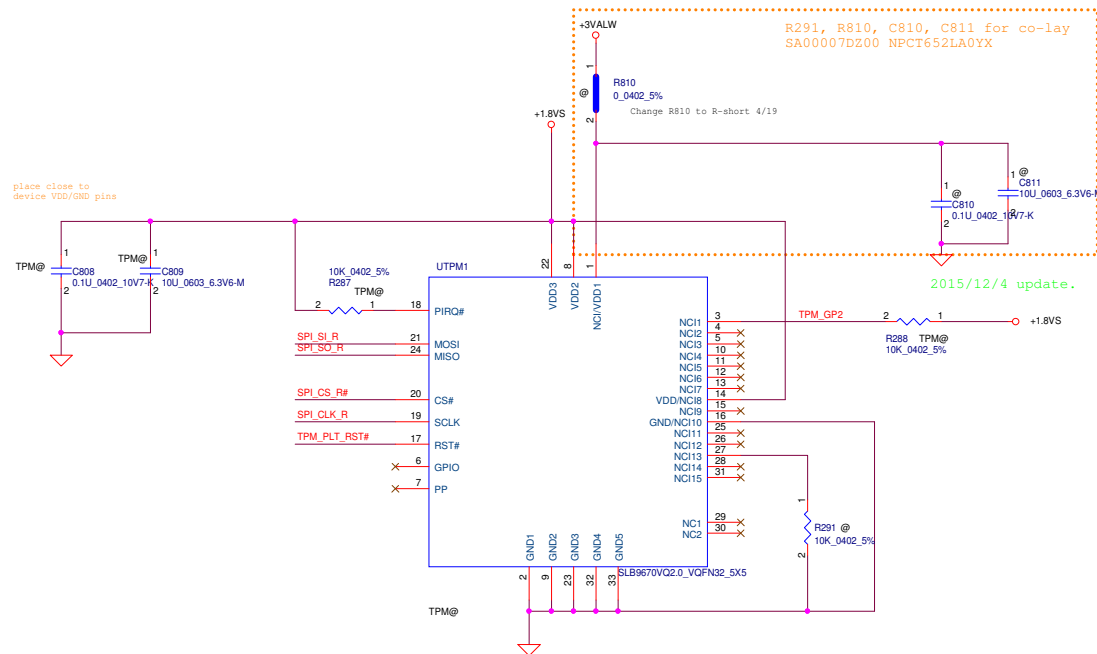
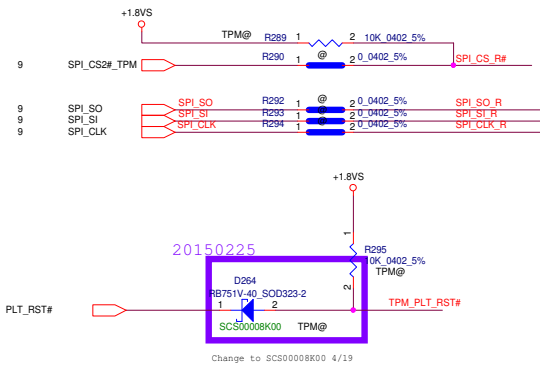
2.1%

Vcc	3.3V +/- 5%				
RE3	100K +/- 1%				
Board ID	RE7	VAD_BID_min	VAD_BID_tYP	VAD_BID_max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

0



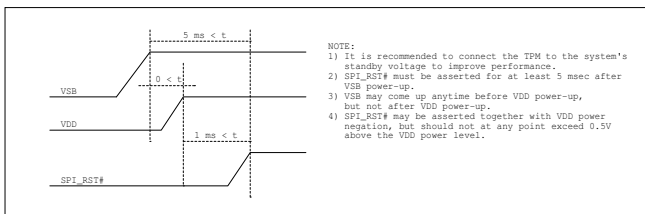
Only for UMA SKU



Change UTPM1 SA000075L00 to SA000075L10 4/15

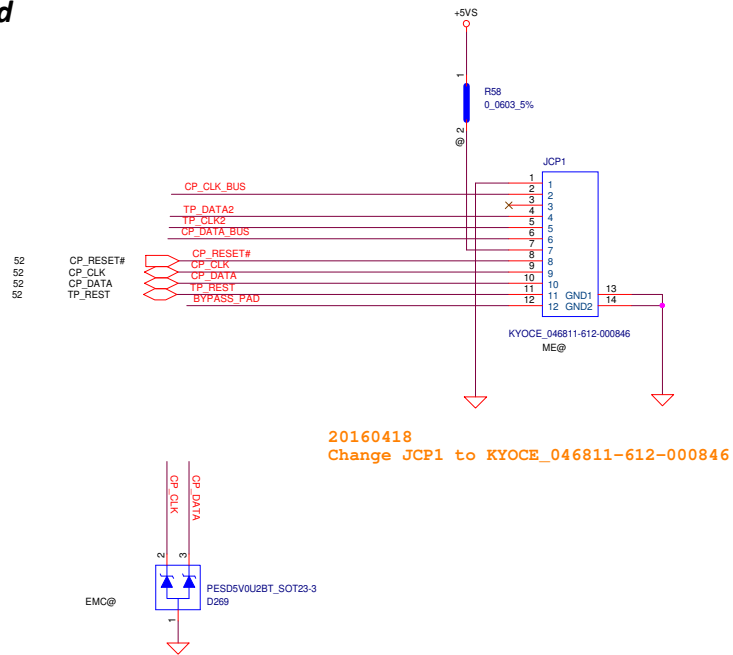
11/19 Change TPM vender
12/7 update SCH

NOTE:
Check timing sequence in SDV phase.

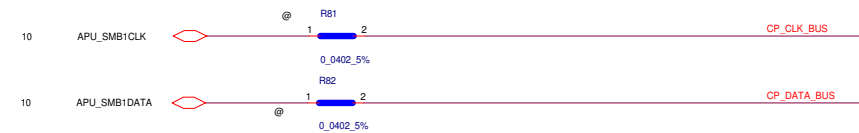
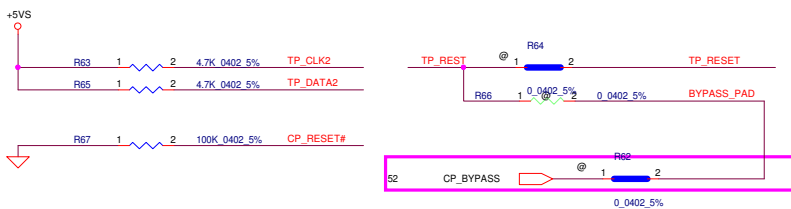
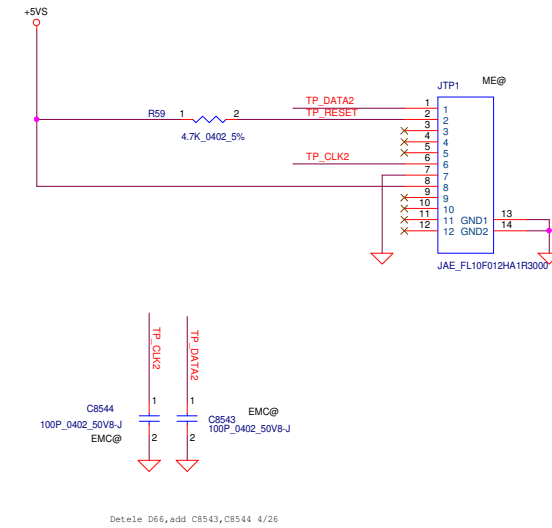


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Click Pad



Track point

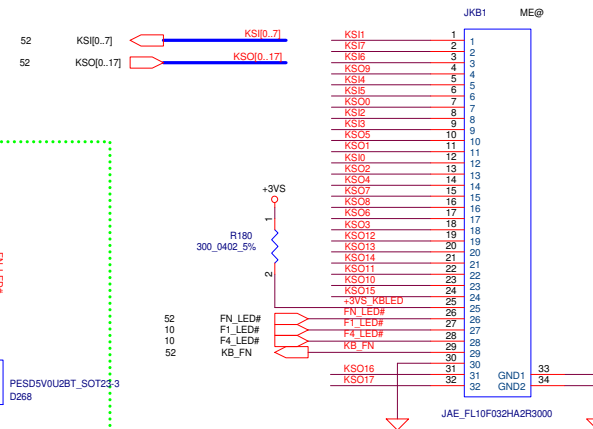



5VSB KBL ESD+

FN L ESD+

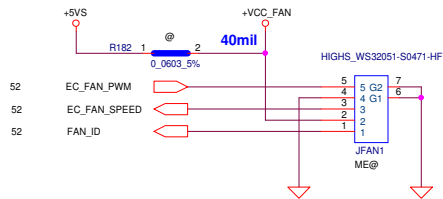
EMC@

PESD5V0U2BT_SOT2 D268



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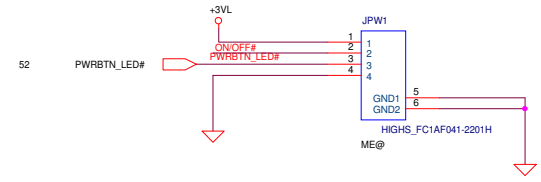
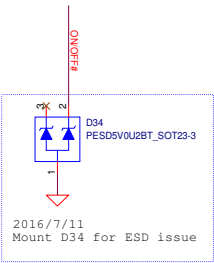
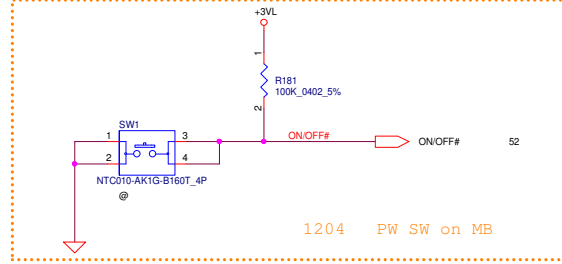
FAN CONN.



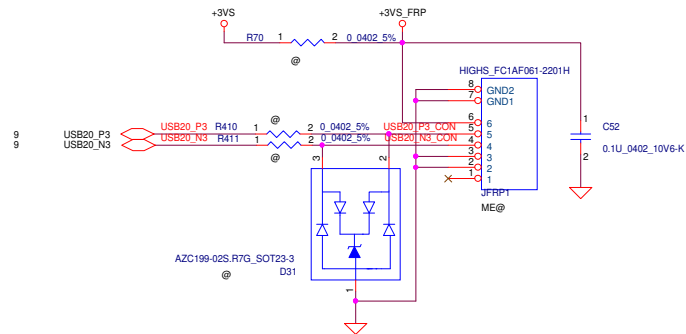
1125 update symbol !!

PWR B

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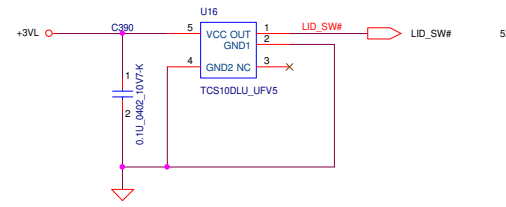
FingerPrint CONN.



Check pin define.1202

Lid Switch

Dual lay for hall sensor



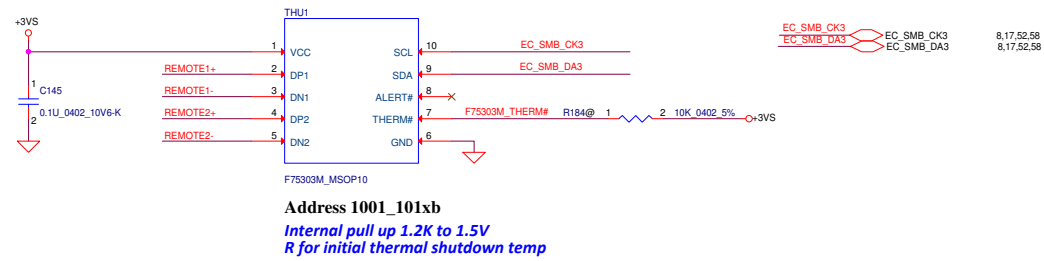
2015/12/10 Update

Delete U16 4/26

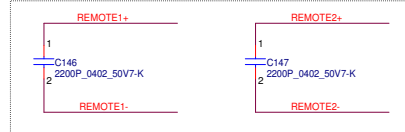
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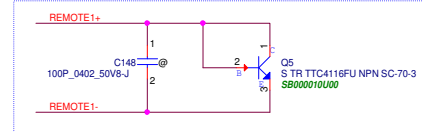
**Thermal Sensor
placed near by VRAM**



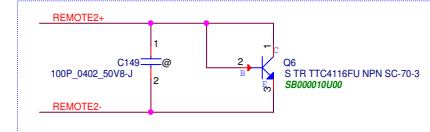
Close to U1



Close to +VCC_CORE

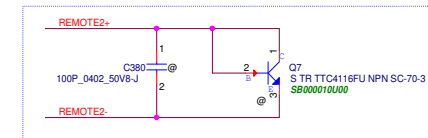



Close JDIMM1&JDIMM2



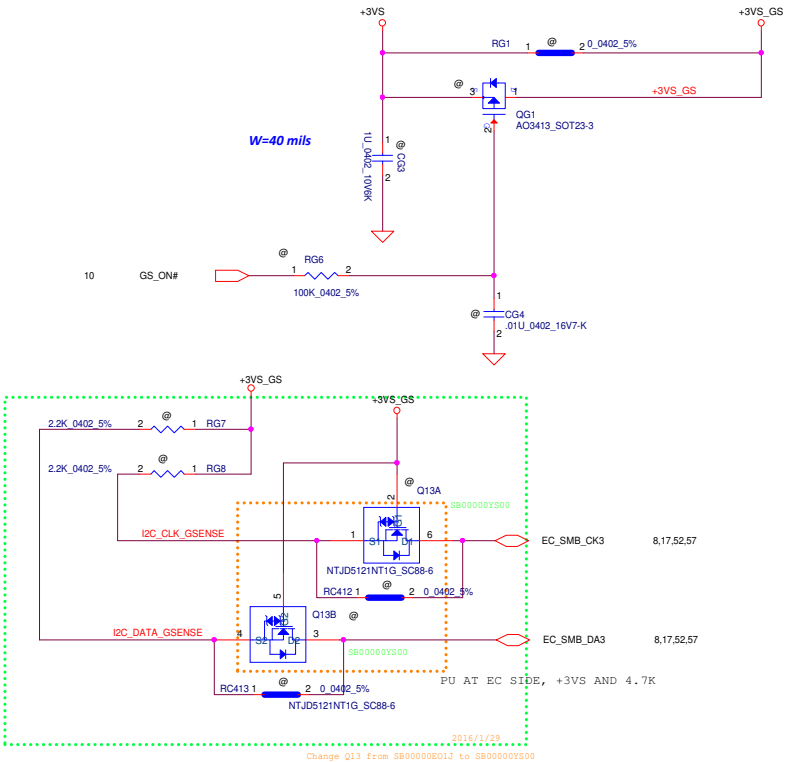
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

20151120



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APS G-Sensor



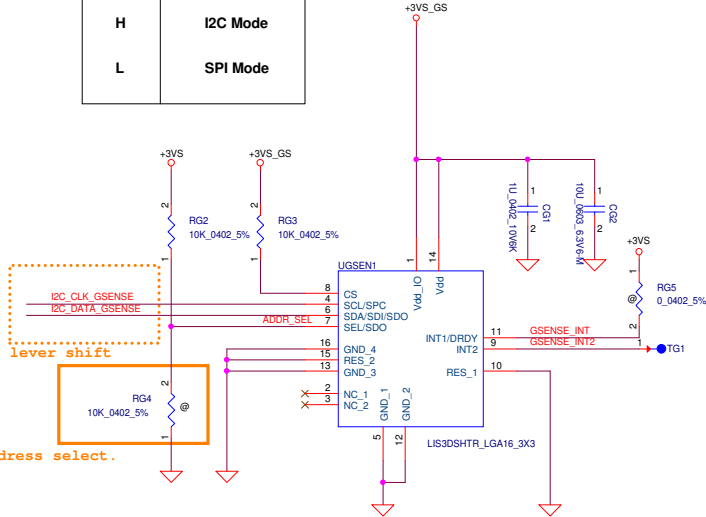
TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode

2016/1/27

Change net name for co-lay lever shift

un-mount RG4, address select.



TABLE

P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

5

4

3

2

1

D

C

B

A

Security Classification

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Issued Date

2015/10/5

Deciphered Date

2016/10/31

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LCFC

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5

4

3

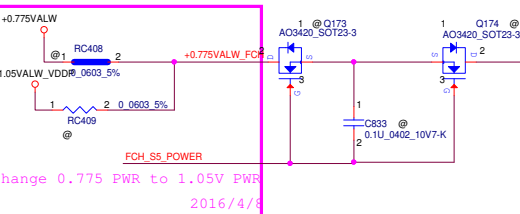
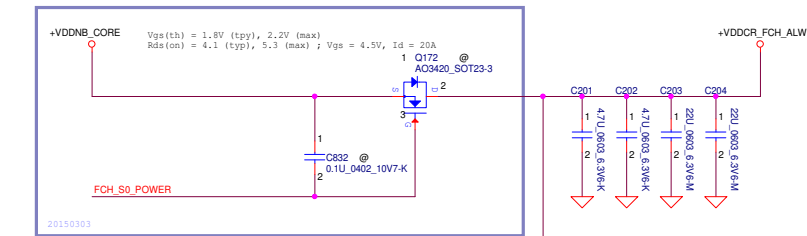
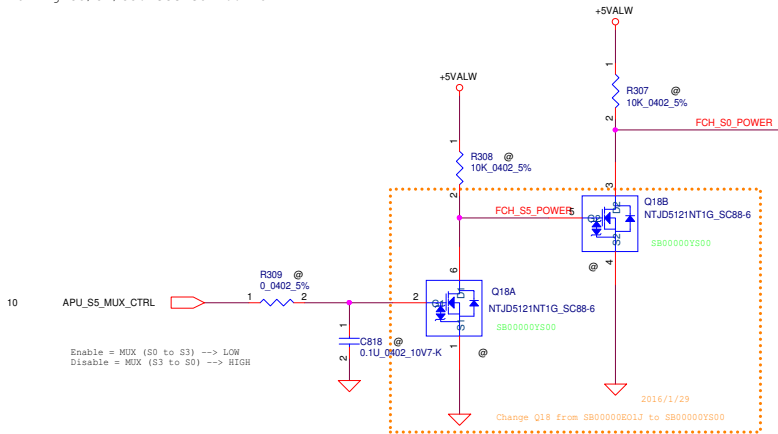
2

1

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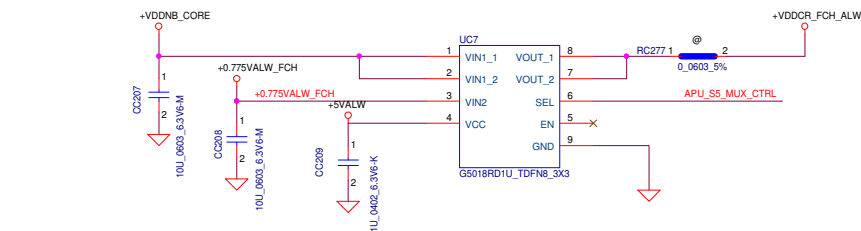
+VDDCR_FCH_ALW

During S0: track +VDDNB_CORE
During S5/S4/S3: set to +0.775V



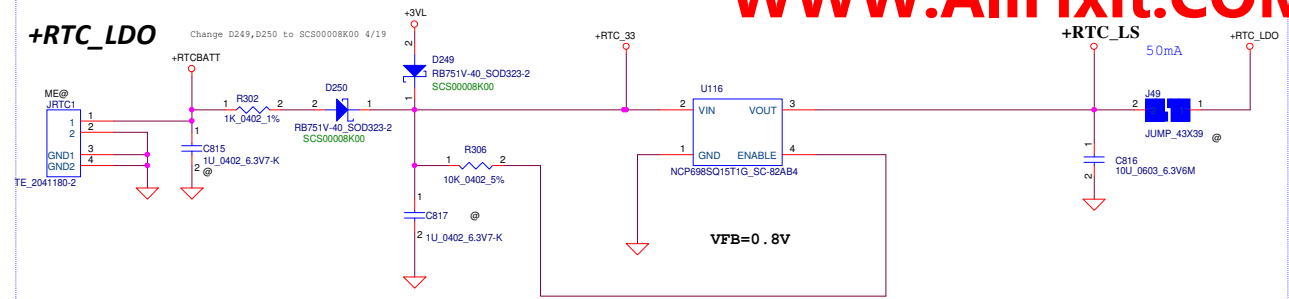
Co-lay

2015/11/05

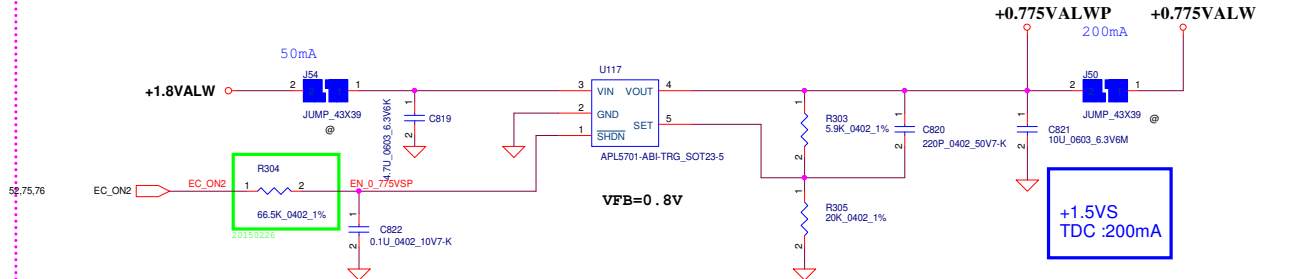


+RTC_LDO

Change D249,D250 to SC500008K00 4/19




+0.775VALW



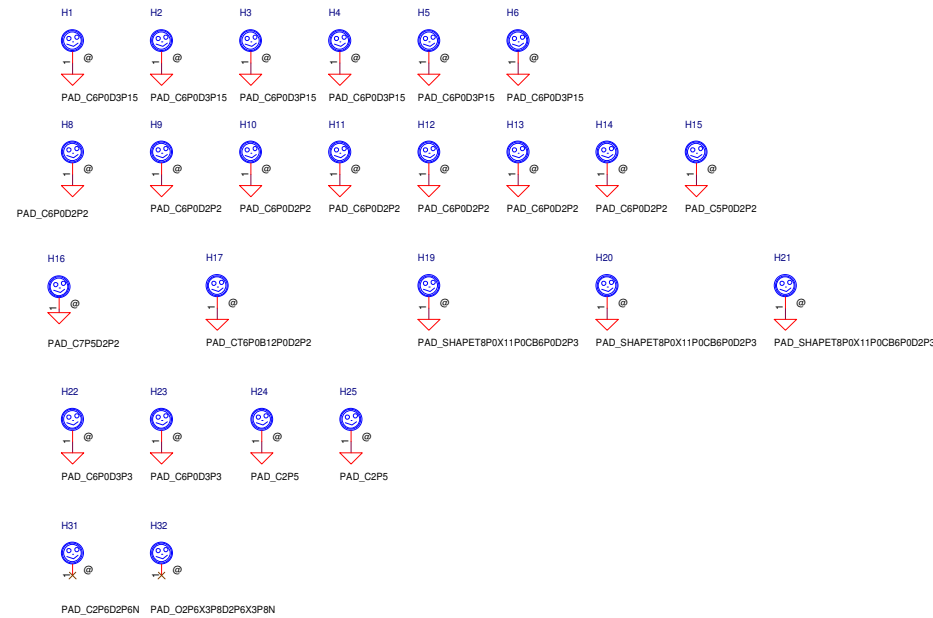
Reserves 2016/4/8

add 0.775 W ALW PWR 5/18

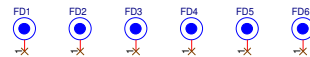
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Issued Date	2015/10/5	Deciphered Date	2016/10/31	Size		
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Issued Date	2015/10/5	Deciphered Date	2016/10/31	XXXX			
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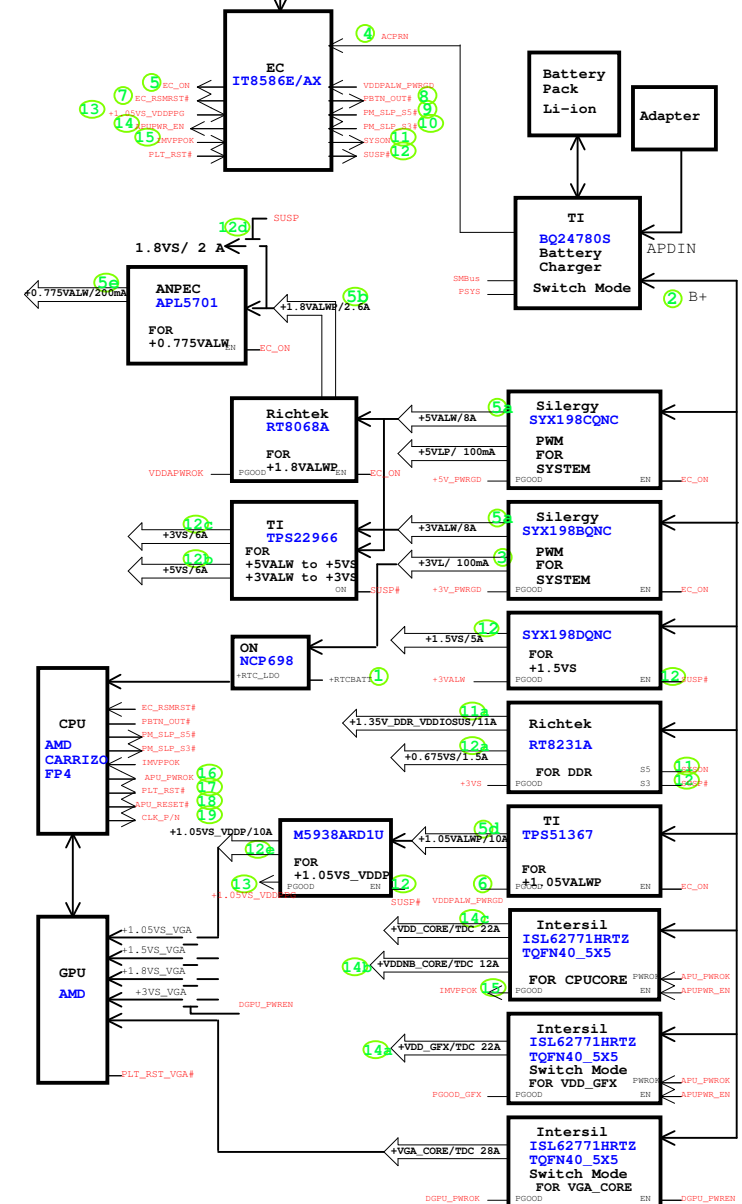
20151119 UPDATE




Screw Hole

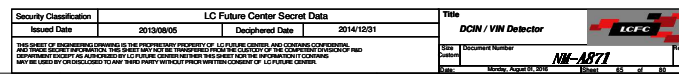
Center Zero

PCB Fedical Mark PAD

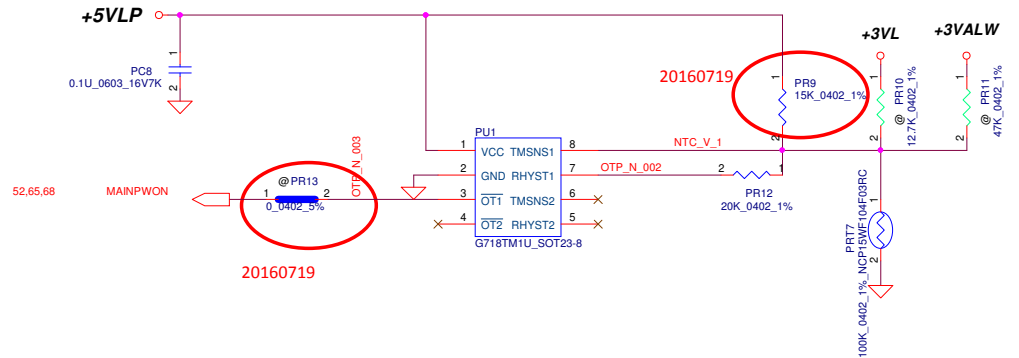
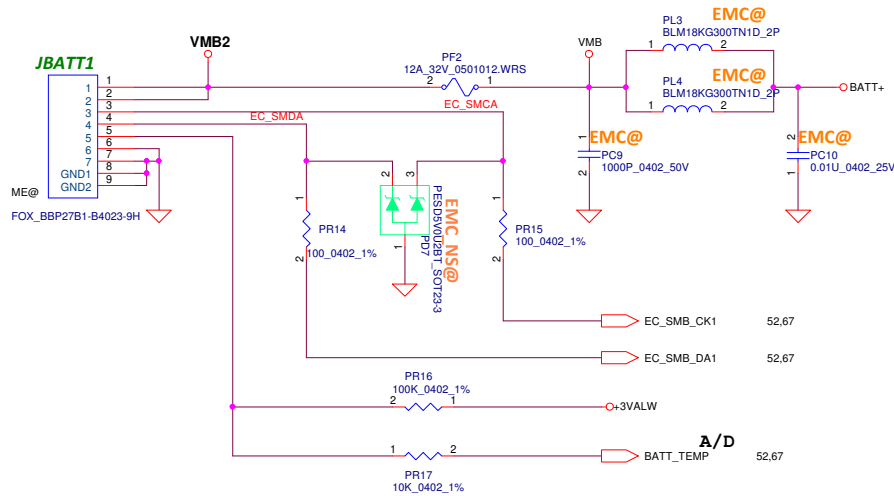
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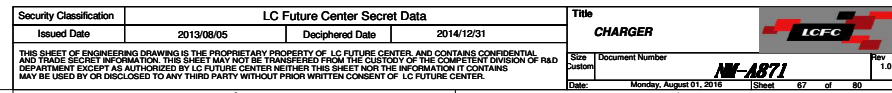
PRT7 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

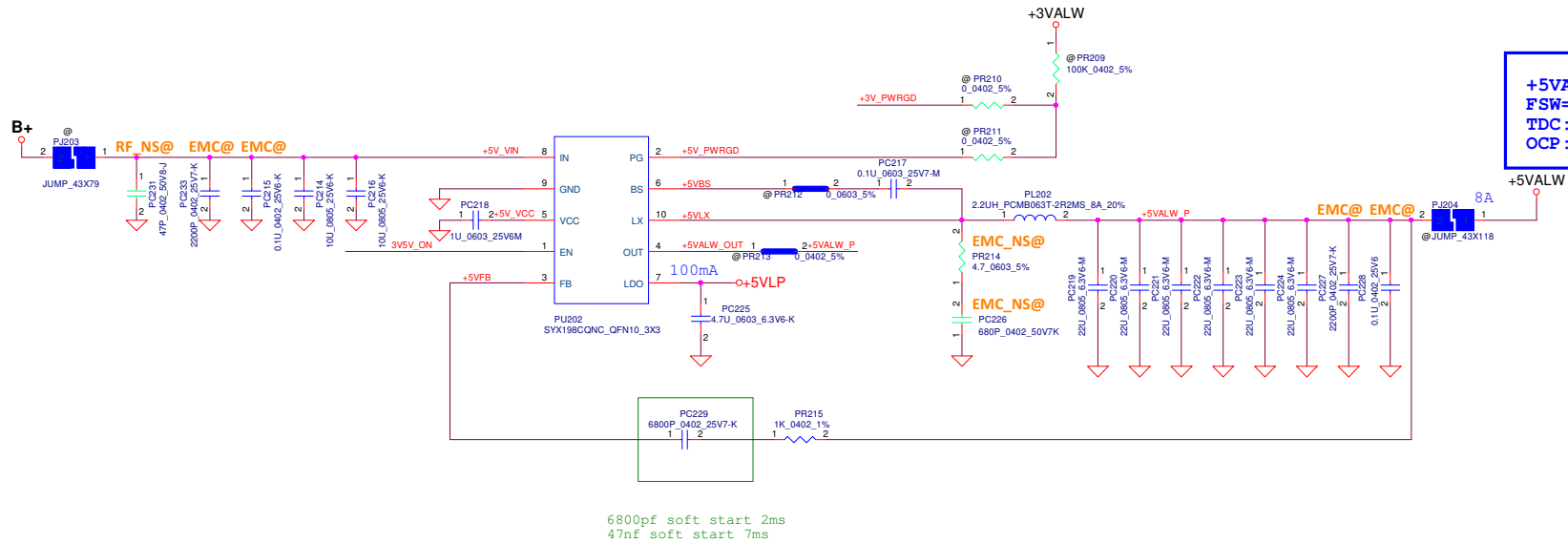
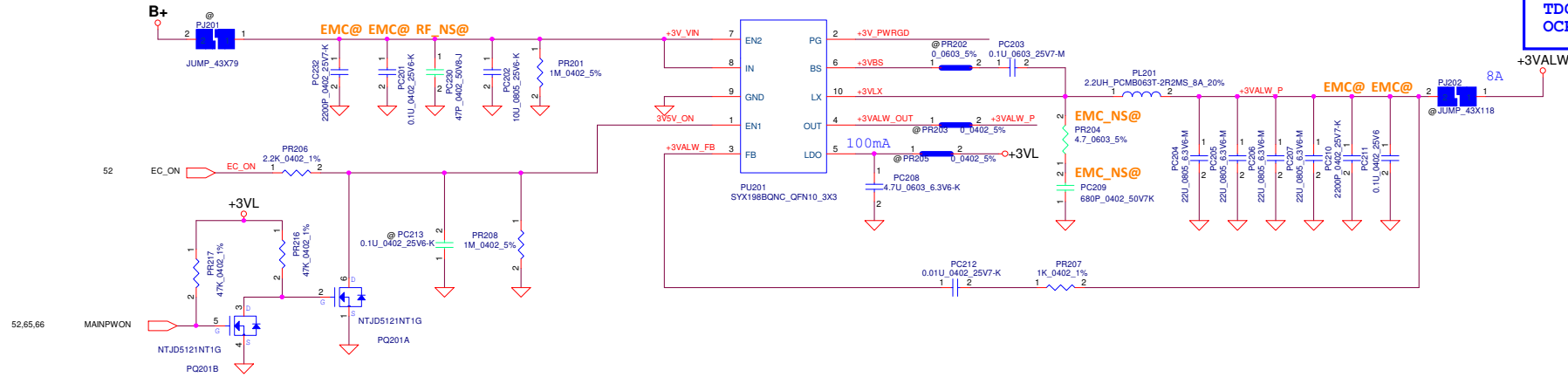


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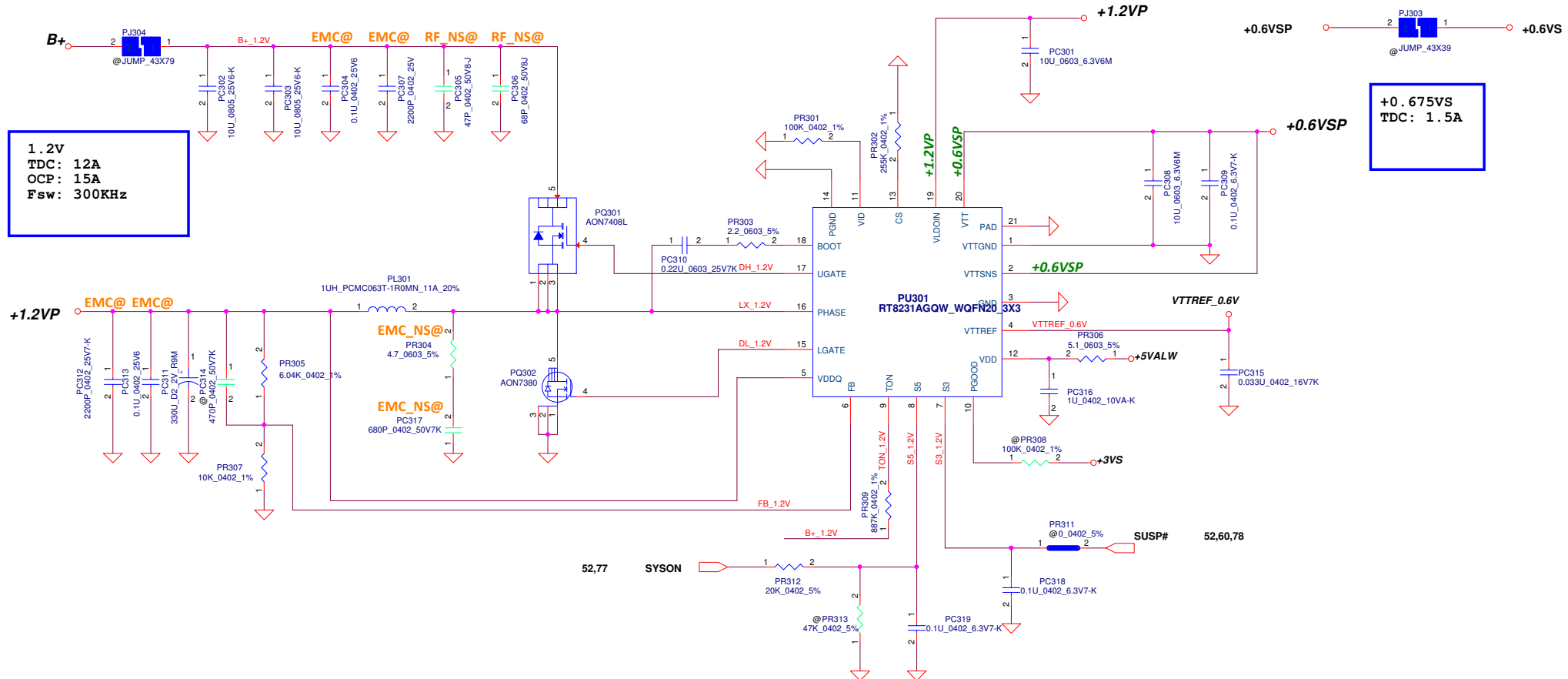
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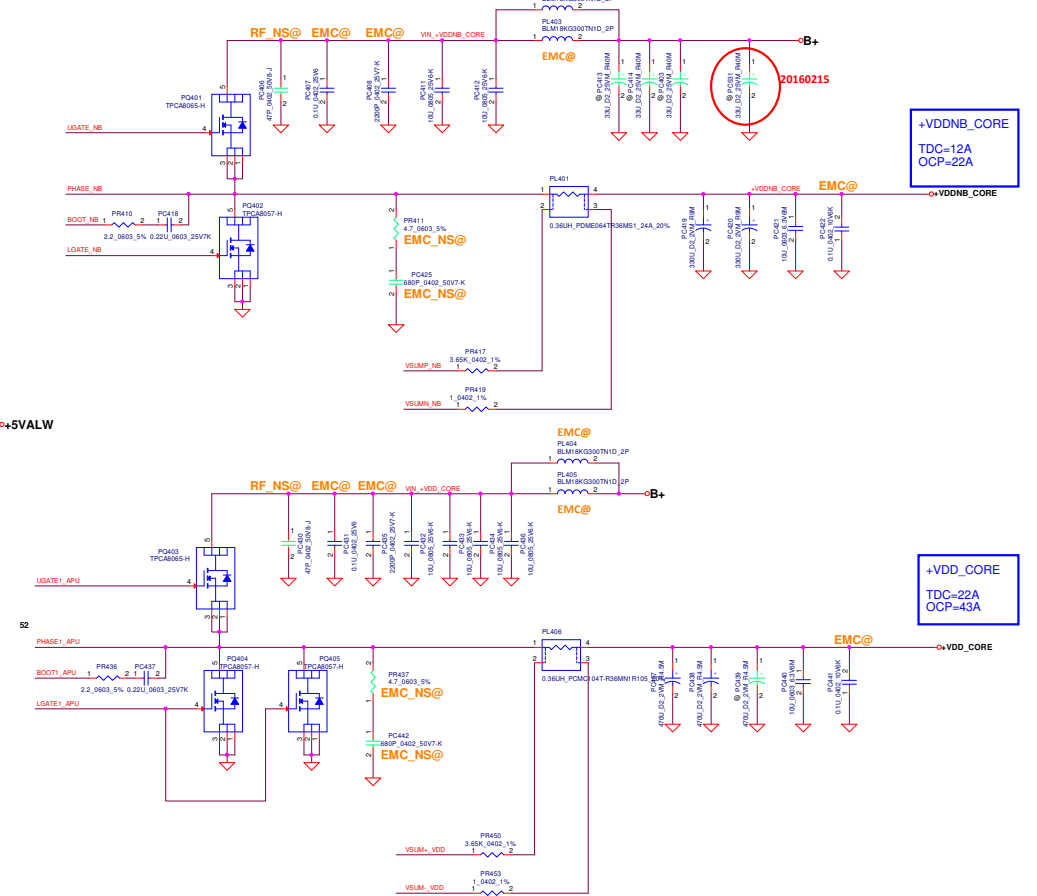




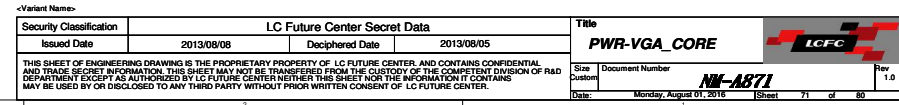
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				1.0
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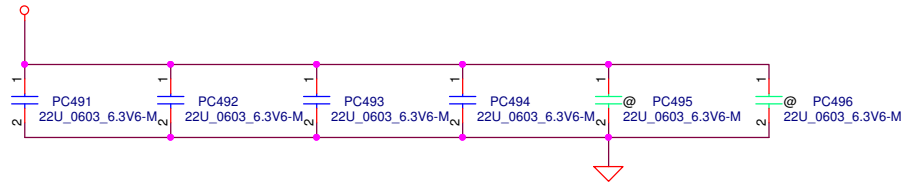




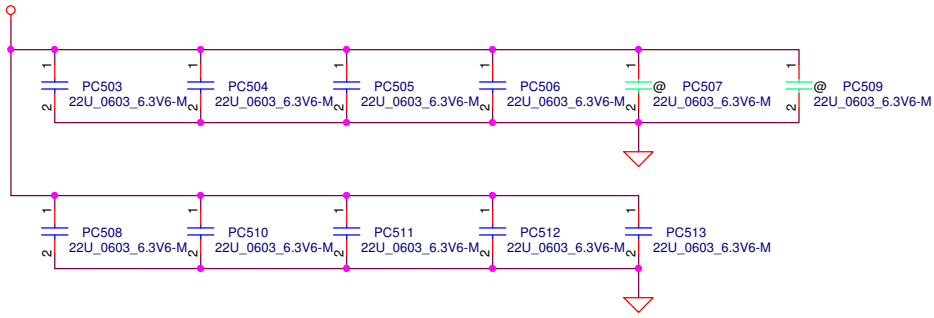
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V(Default)
1	0	0.9V
1	1	0.8V



+VDDNB_CORE

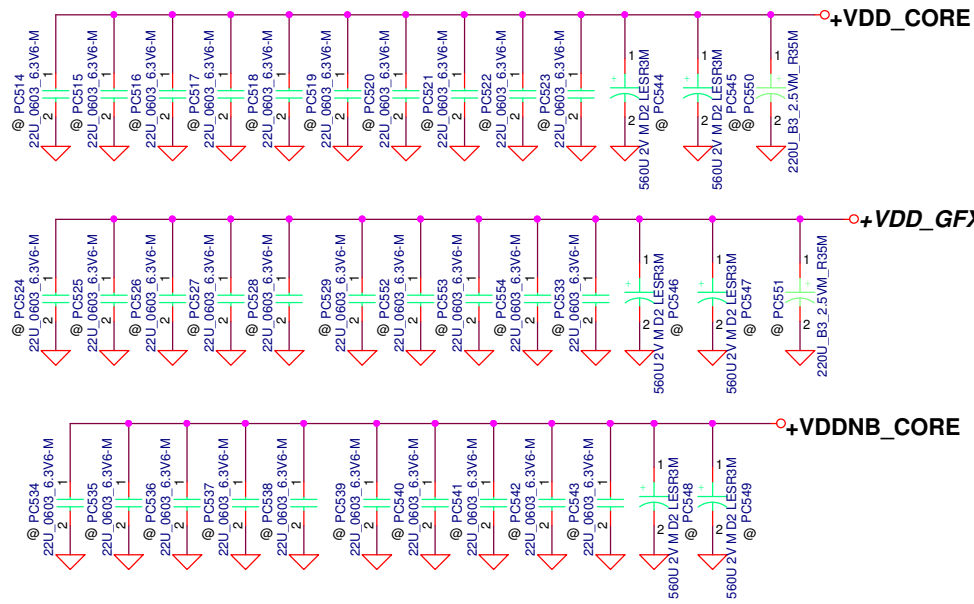


+VDD_CORE




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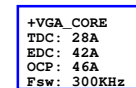


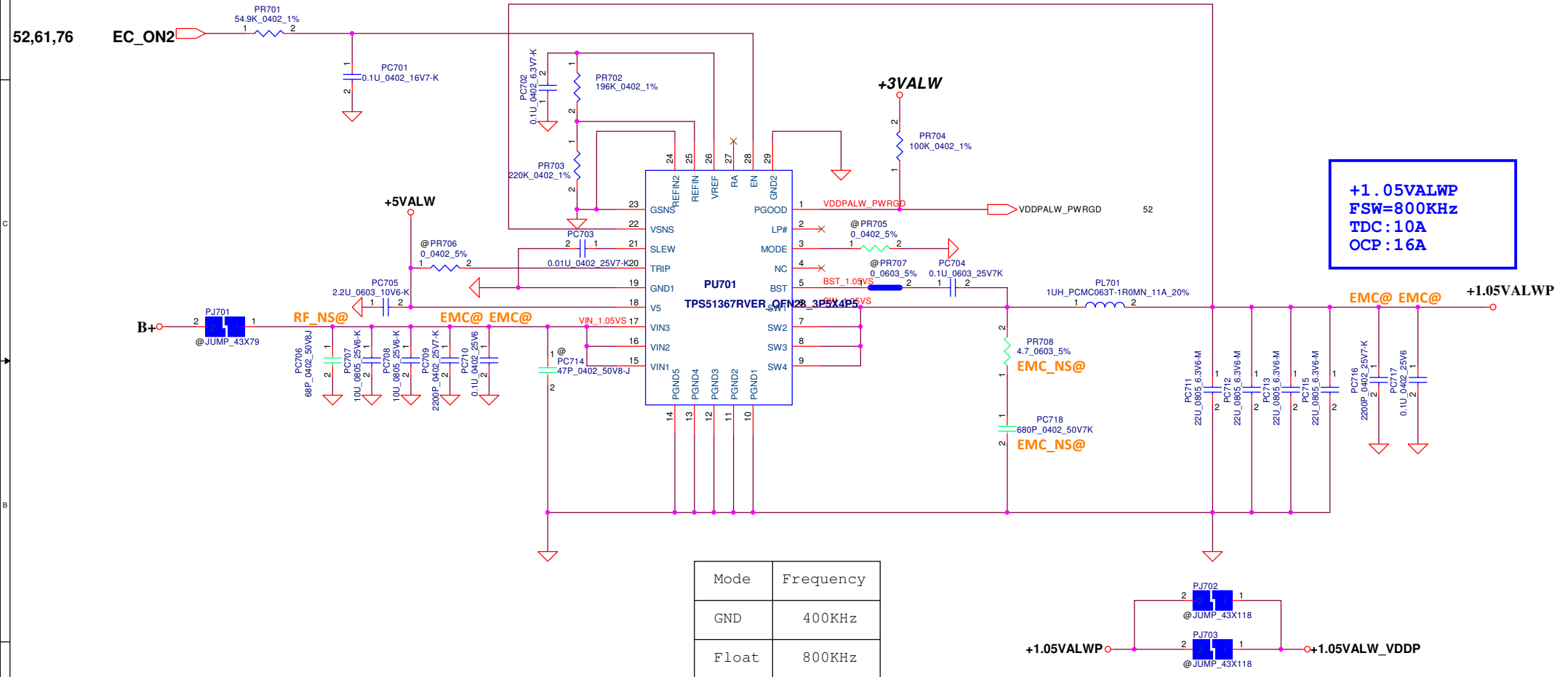
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Title			
VCCCPUCORE DECOUPLING			
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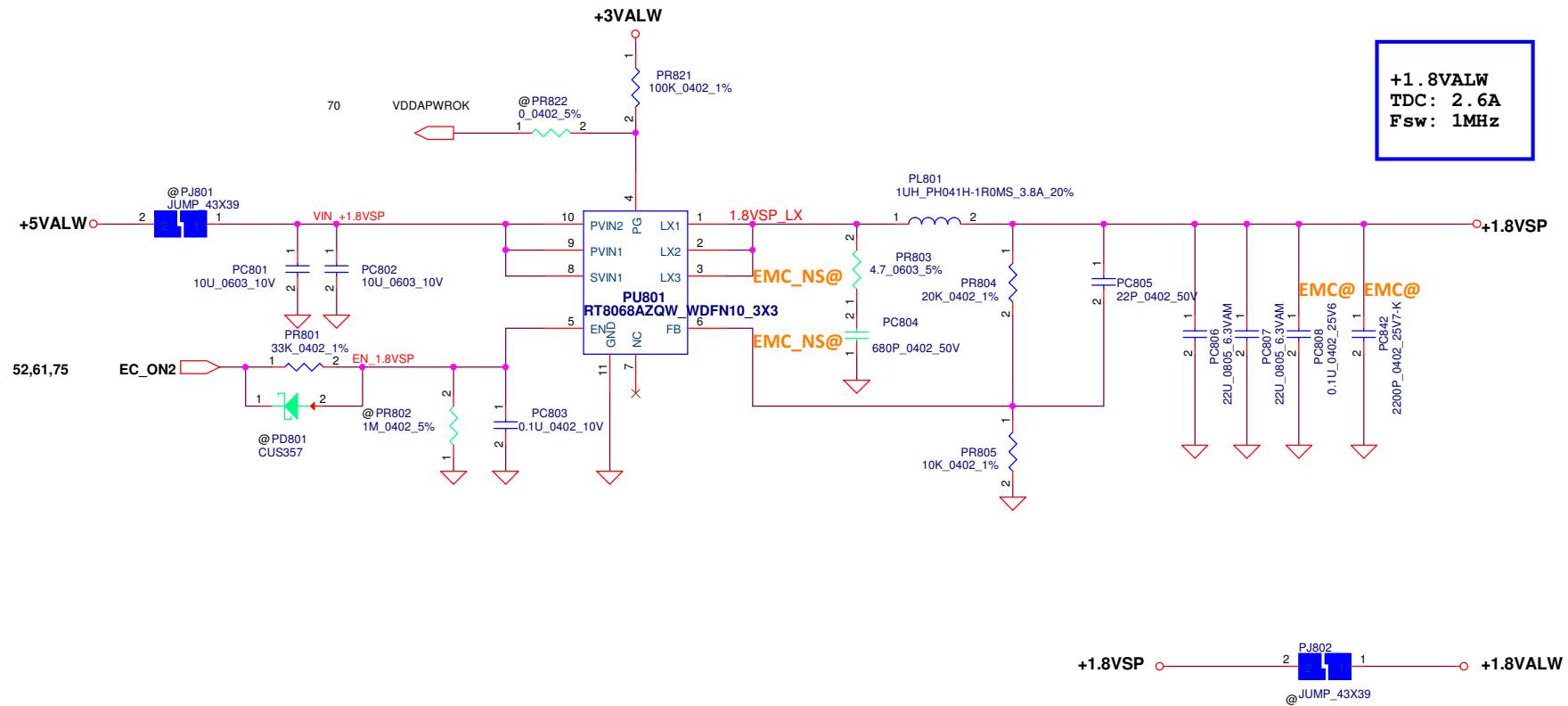




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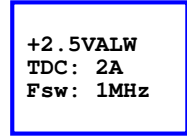
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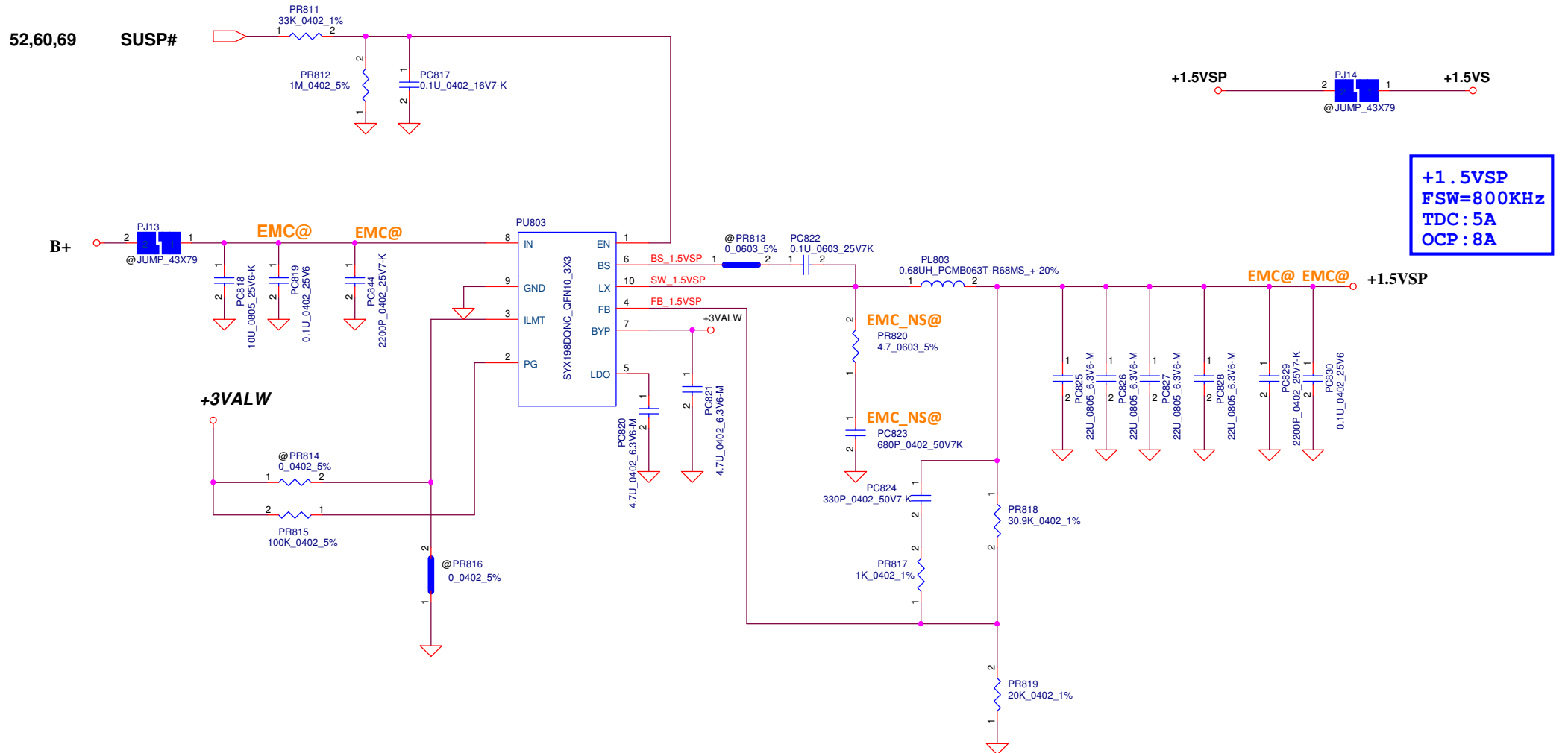
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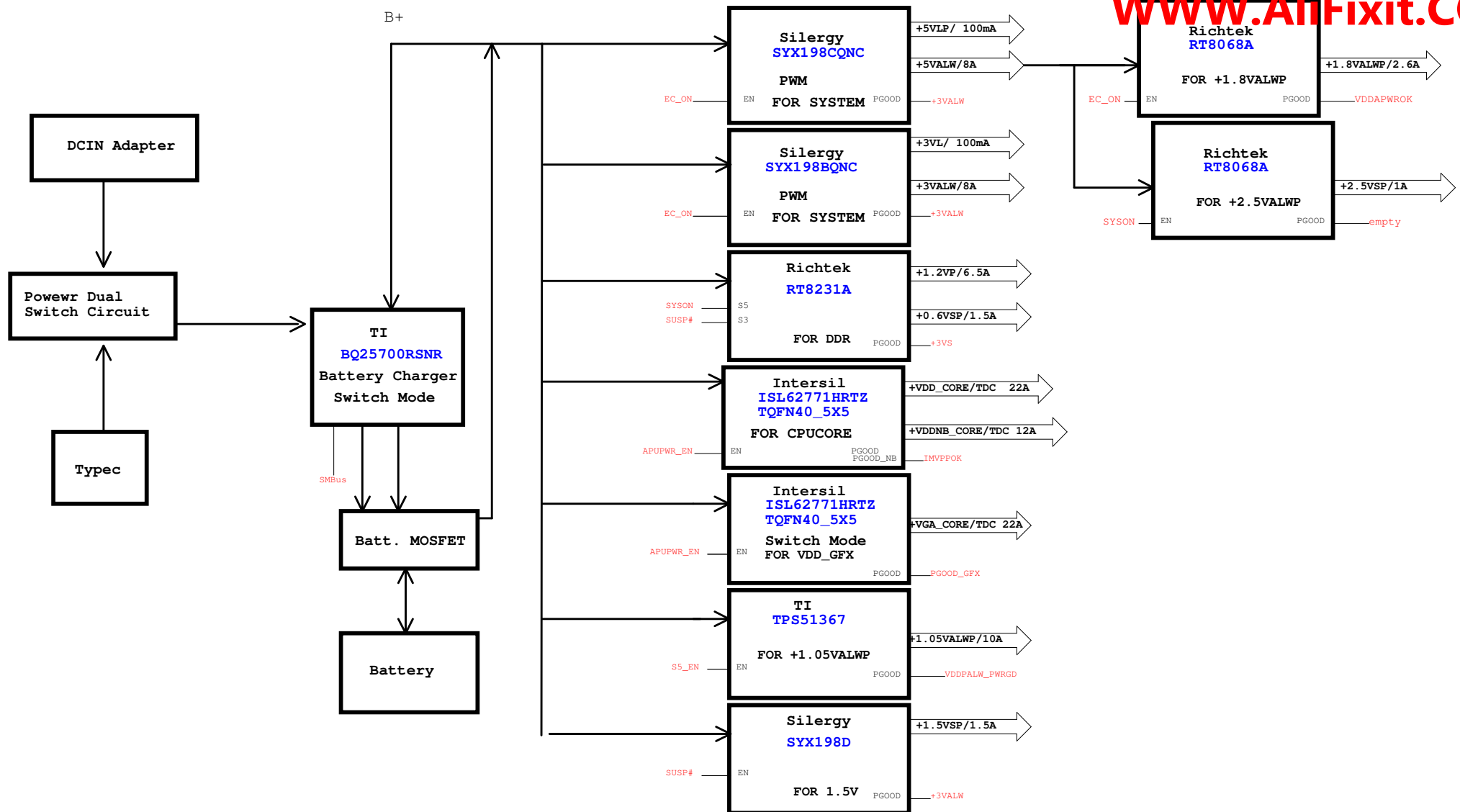
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