LCFC Confidential

DG421/DG521/DG721 MB Schematics Document

Kabylake-U22 with DDR4 + Nvidia N16S-GTR/N16V-GMR1 GPU

2017-01-18

REV:1.0

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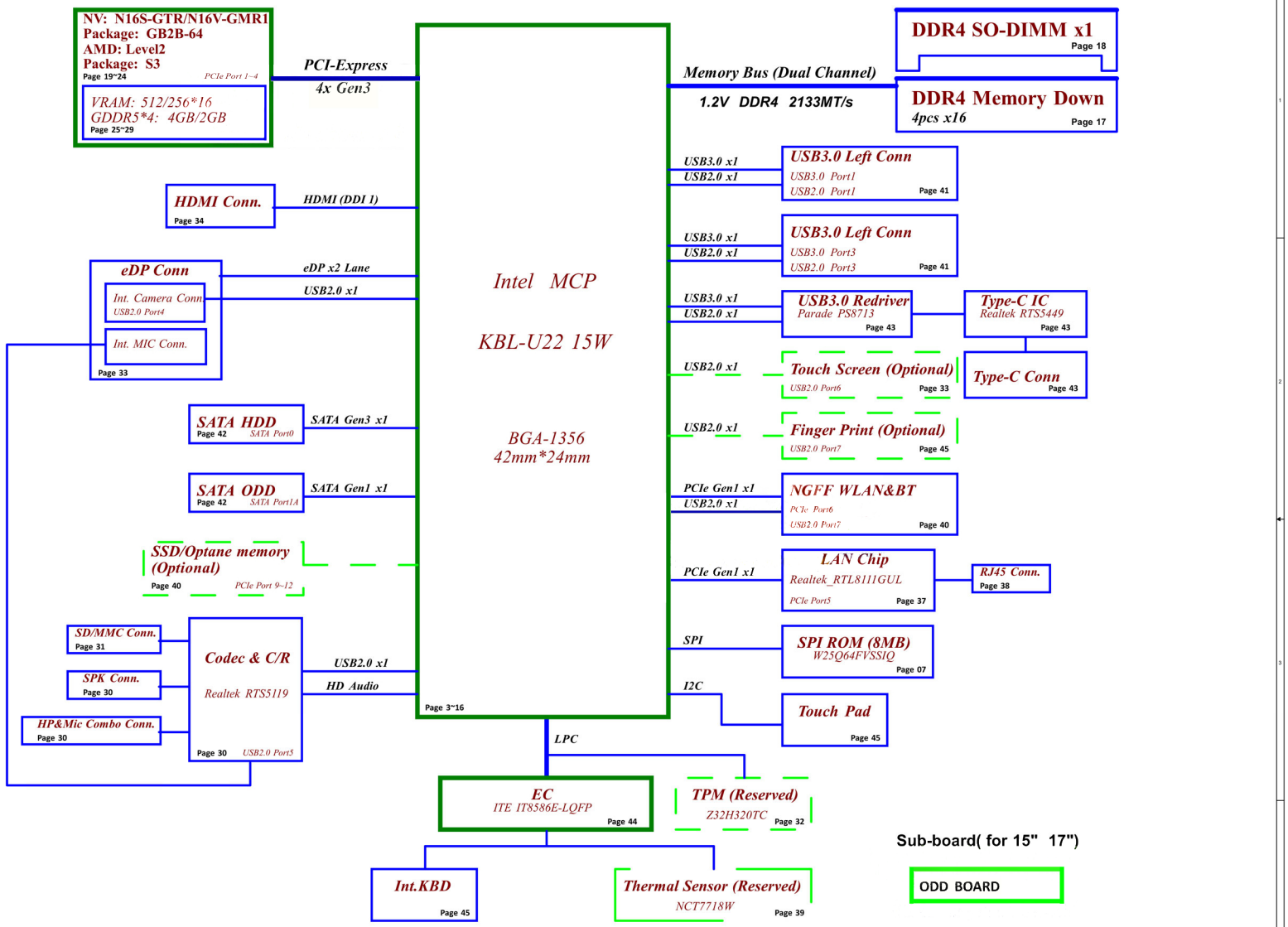

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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4 X4 PCIE	DGPU
	5	LAN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

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Title: **Notes List**

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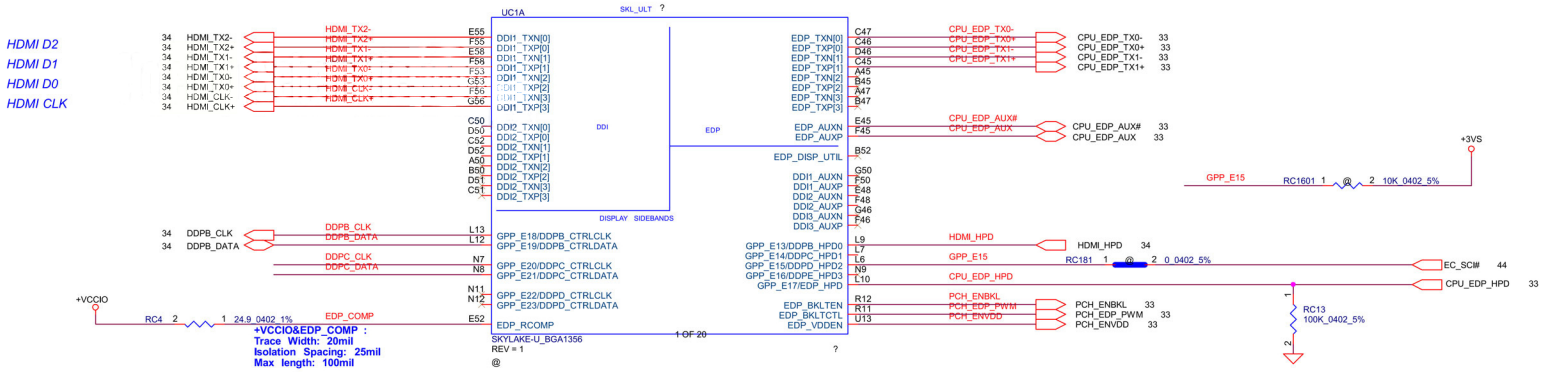
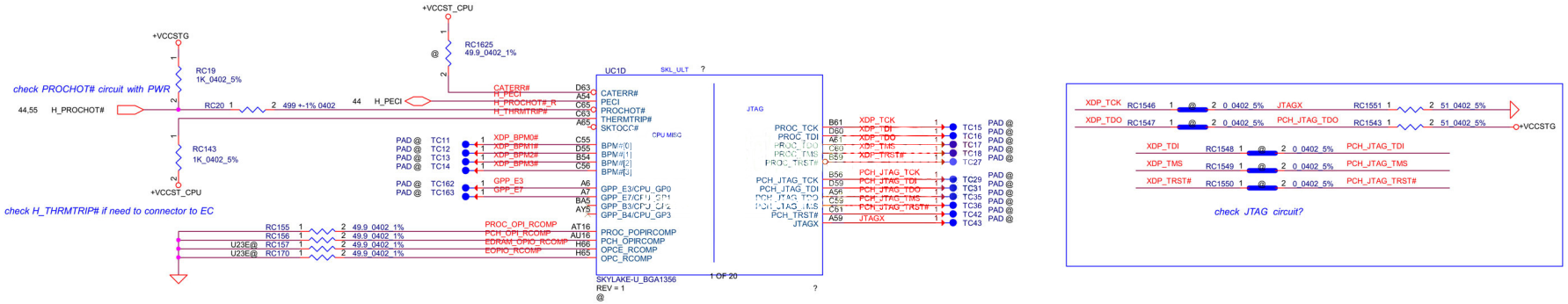
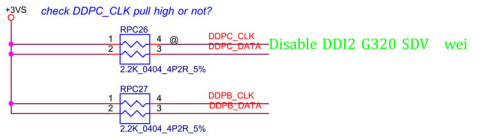




DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC



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Title: **MCP (DDI,EDP)**

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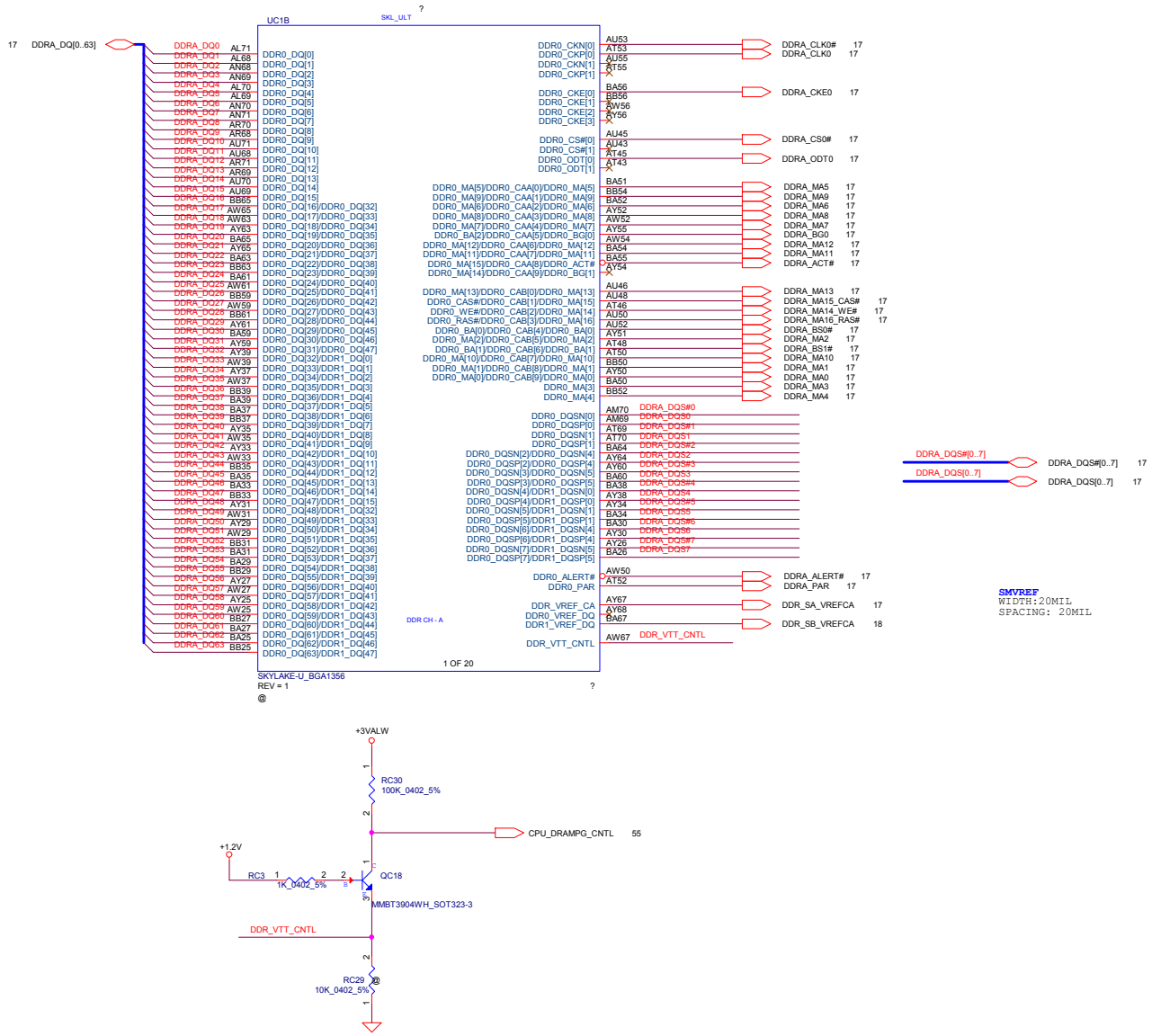

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Title: **MCP (DDR4)**

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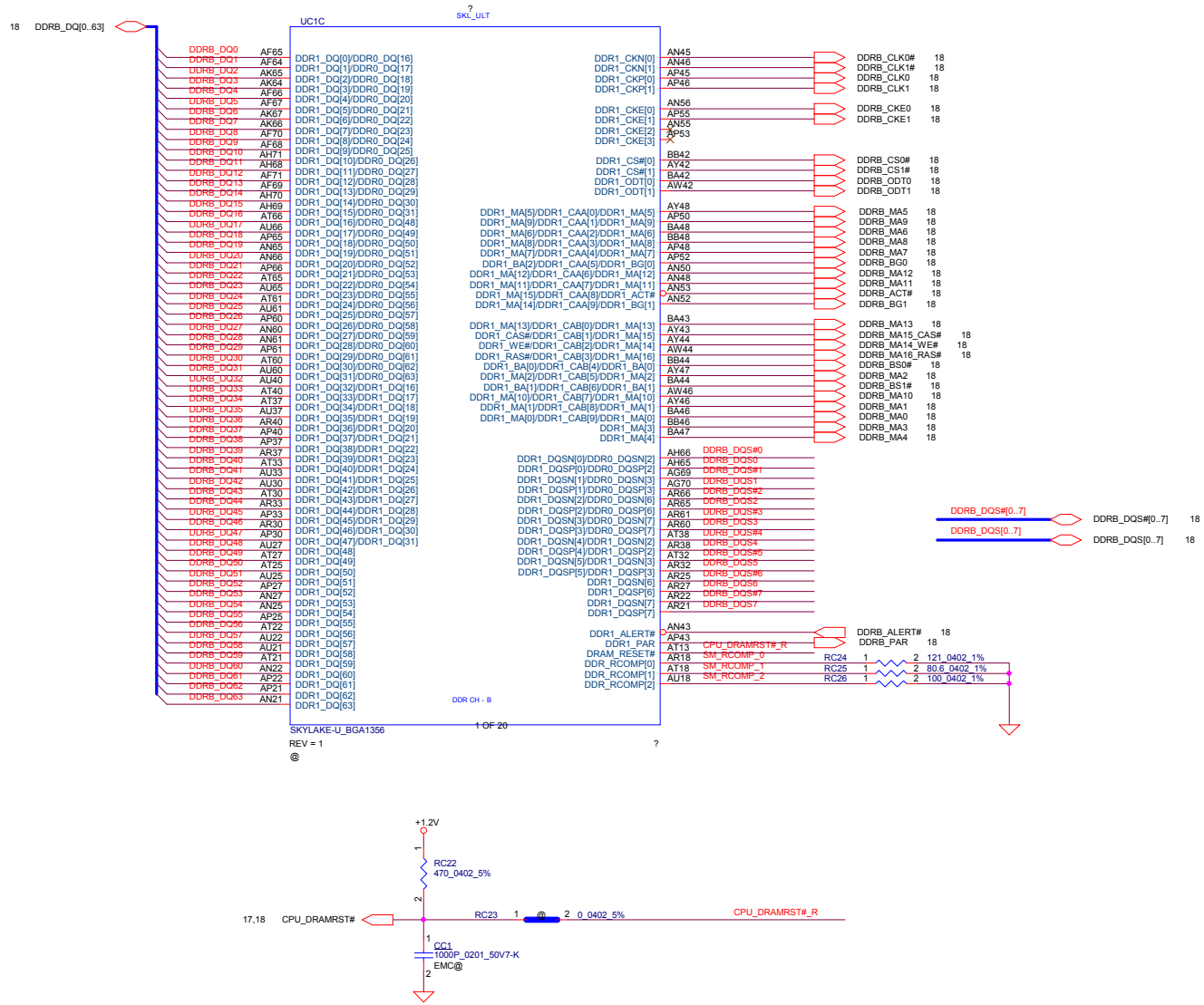

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Title: **MCP (DDR4)**

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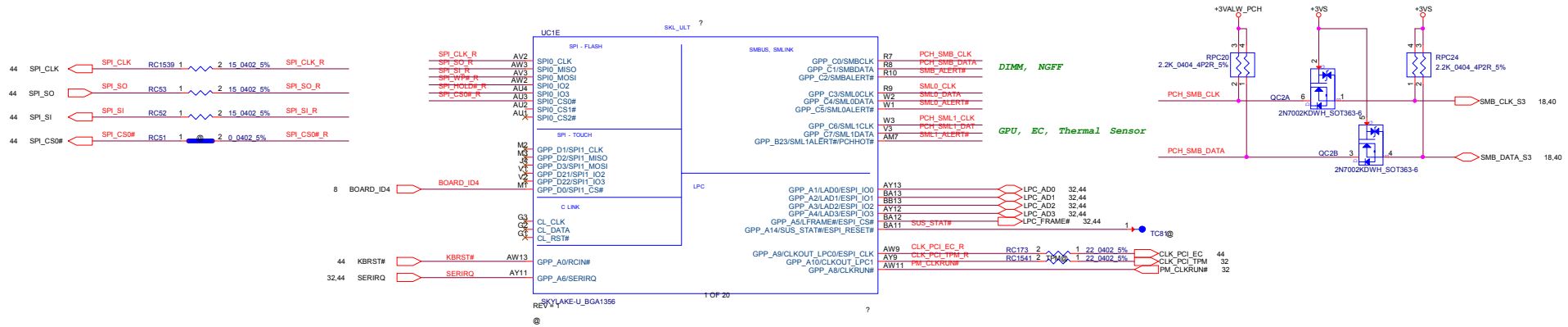
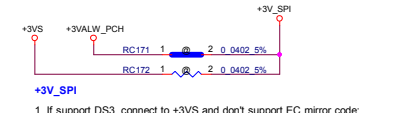
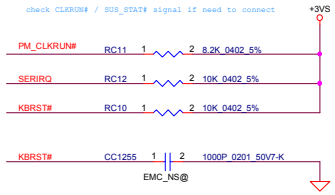
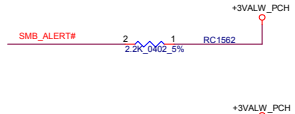
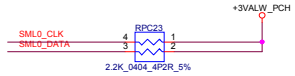


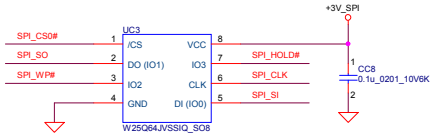


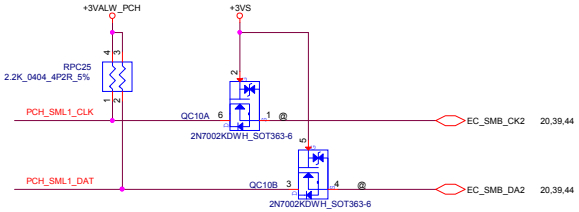


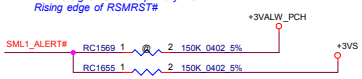




This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary wel Rising edge of RSMRST#







To enable Direct Connect Interface (DCI), a 150K pull up resistor will need to be added to PCHHOT# pin. This pin must be low during the rising edge of RSMRST#. (Refer to WW52_MOW)

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Title: **MCP (MISC,JTAG,SPI,LPC,**

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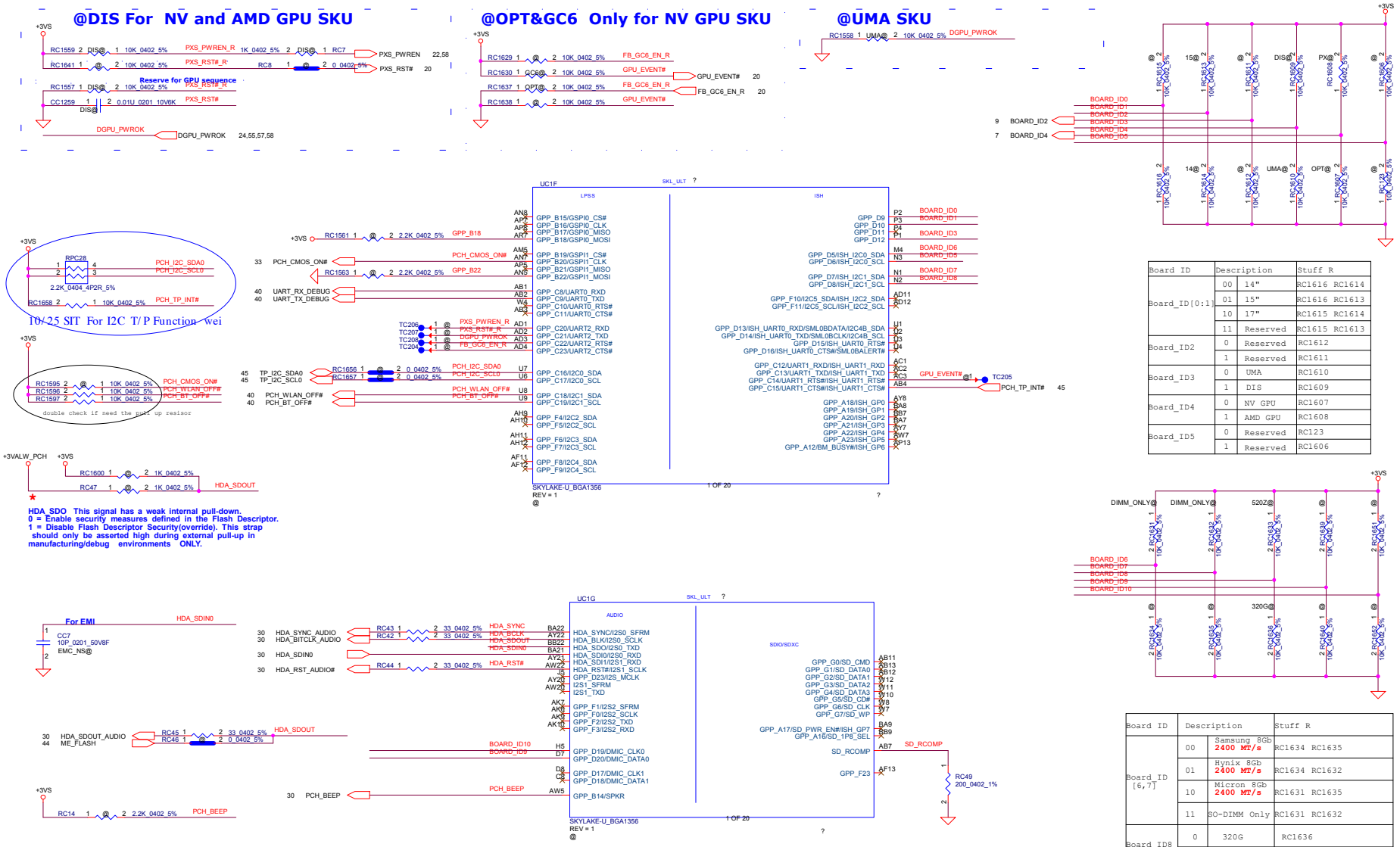

Board ID	Description		Stuff R
Board_ID[0:1]	00	14"	RC1616 RC1614
	01	15"	RC1616 RC1613
	10	17"	RC1615 RC1614
	11	Reserved	RC1615 RC1613
Board_ID2	0	Reserved	RC1612
	1	Reserved	RC1611
Board_ID3	0	UMA	RC1610
	1	DIS	RC1609
Board_ID4	0	NV GPU	RC1607
	1	AMD GPU	RC1608
Board_ID5	0	Reserved	RC123
	1	Reserved	RC1606

Board ID	Description		Stuff R
Board_ID [6,7]	00	Samsung 8Gb 2400 MT/s	RC1634 RC1635
	01	Hynix 8Gb 2400 MT/s	RC1634 RC1632
	10	Micron 8Gb 2400 MT/s	RC1631 RC1635
	11	SO-DIMM Only	RC1631 RC1632
Board_ID8	0	320G	RC1636
	1	520Z	RC1633
Board_ID9	0	Reserved	RC1640
	1	Reserved	RC1639
Board_ID10	0	Reserved	RC1652
	1	Reserved	RC1651

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit SBS	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK

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Title: MCP (LPSS,ISH,AUDIO,SDI

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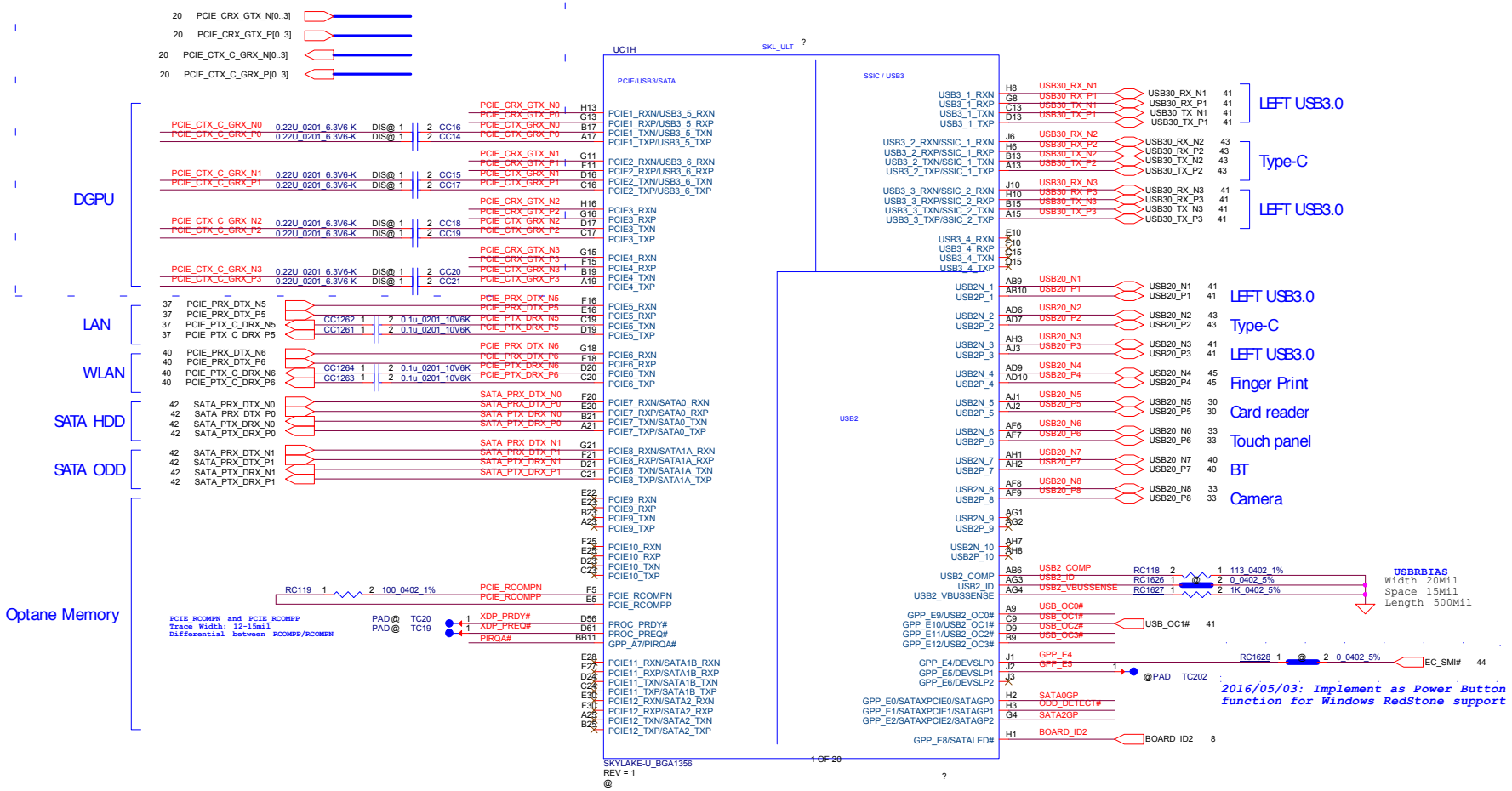
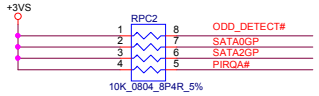
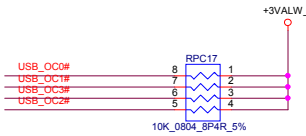
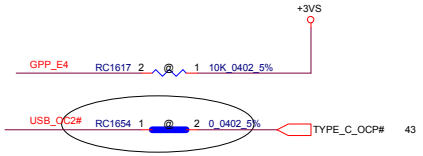
@DIS For NV and AMD GPU SKU









8/ 24 Reserve TYPE_C_OCP# to CPU USB_OC2# wei

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Title: MCP (PCIE,SATA,USB3,US

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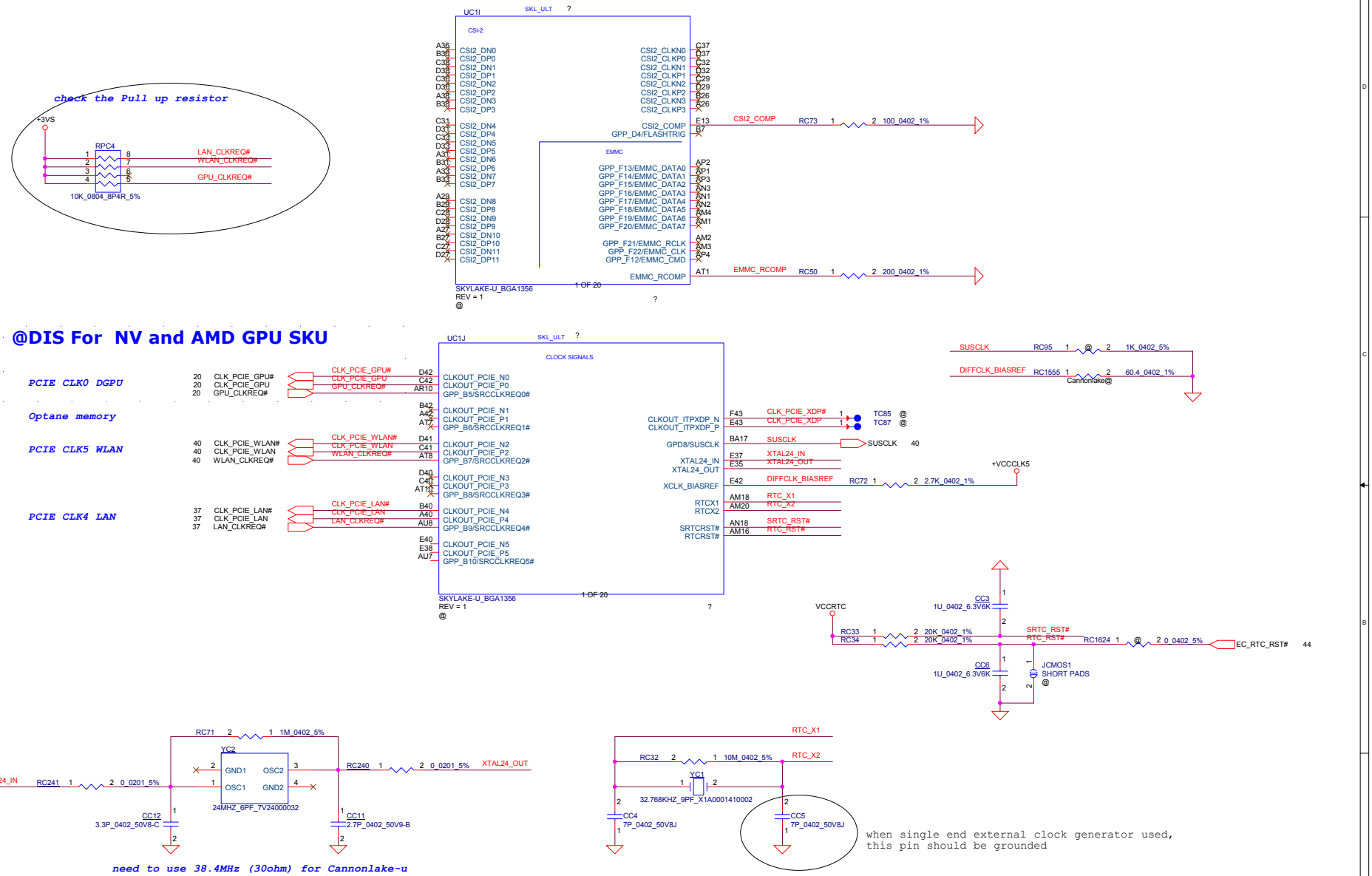

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Title: MCP (CSI2,EMMC,CLOCK)

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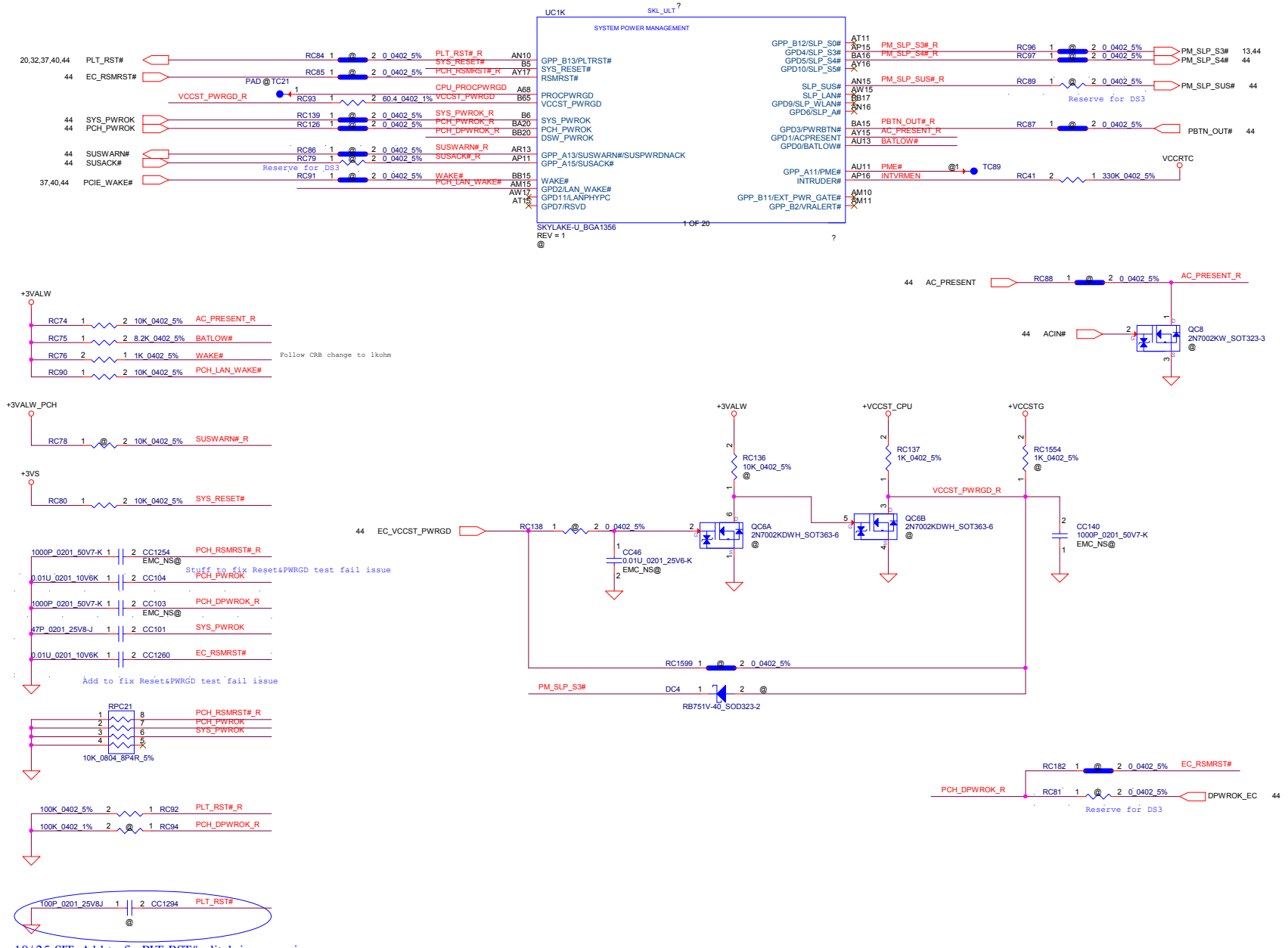

10/25 SIT Add to fix PLT_RST# glitch issue wei

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Title: MCP (SYSTEM PWR MANAGEMENT)

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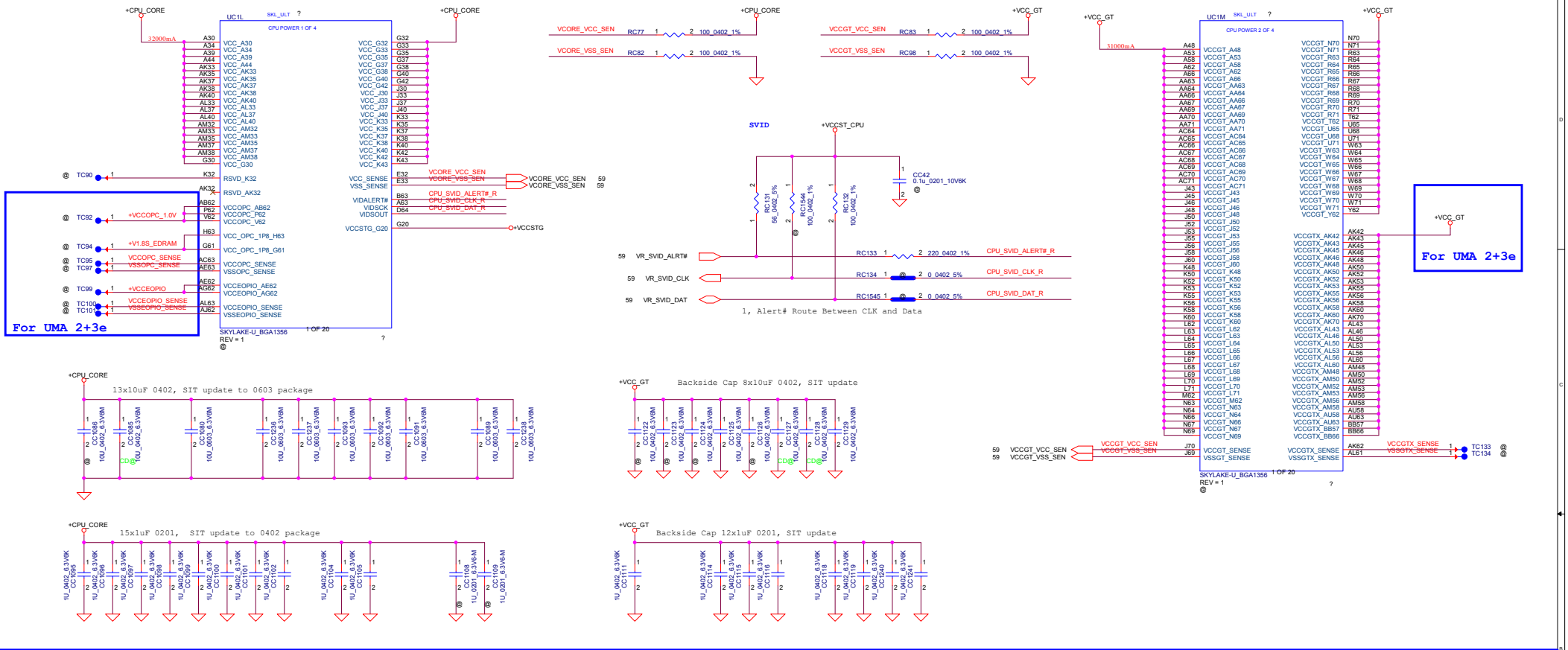

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Title: MCP (CPU PWR1)

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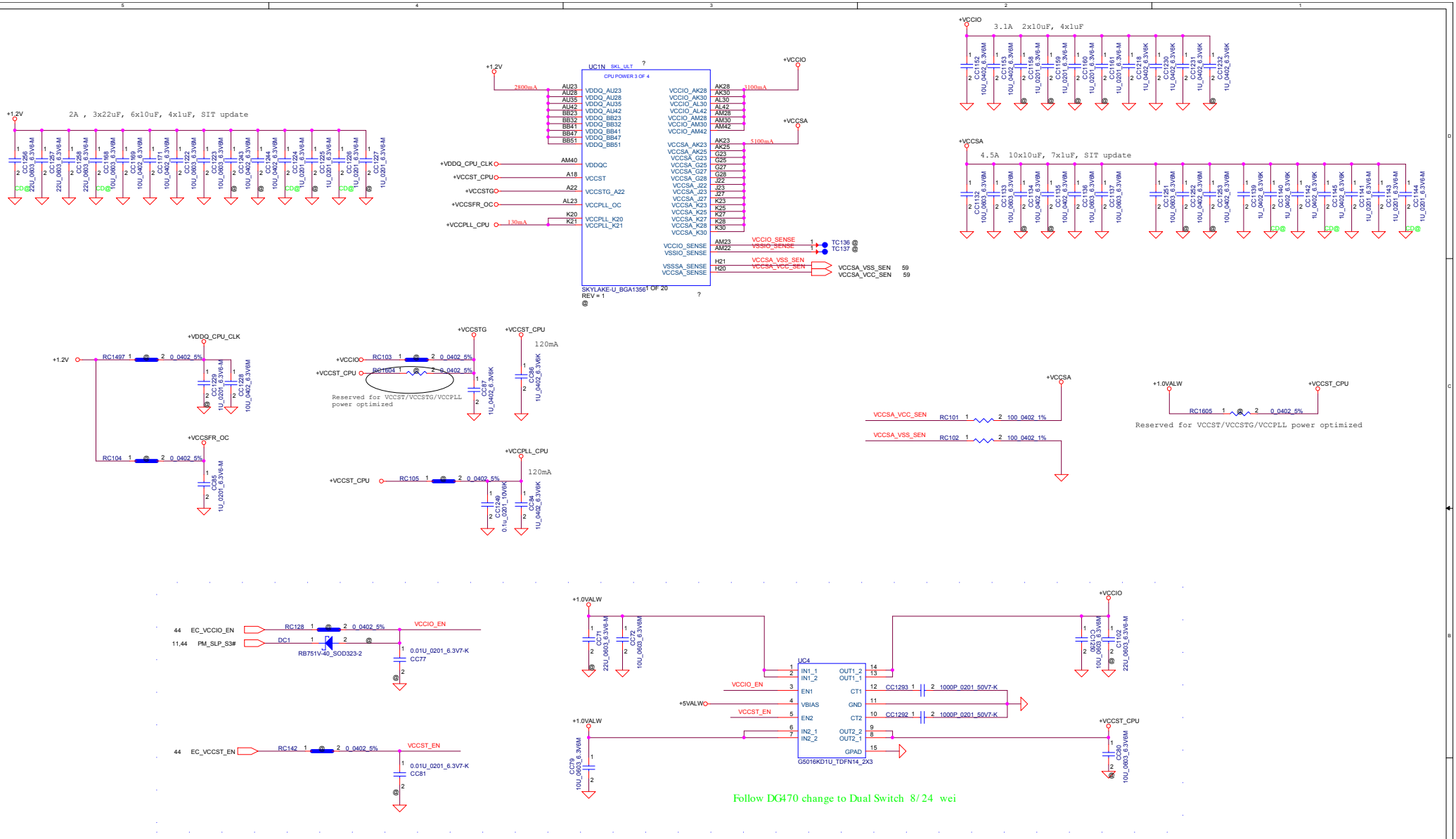

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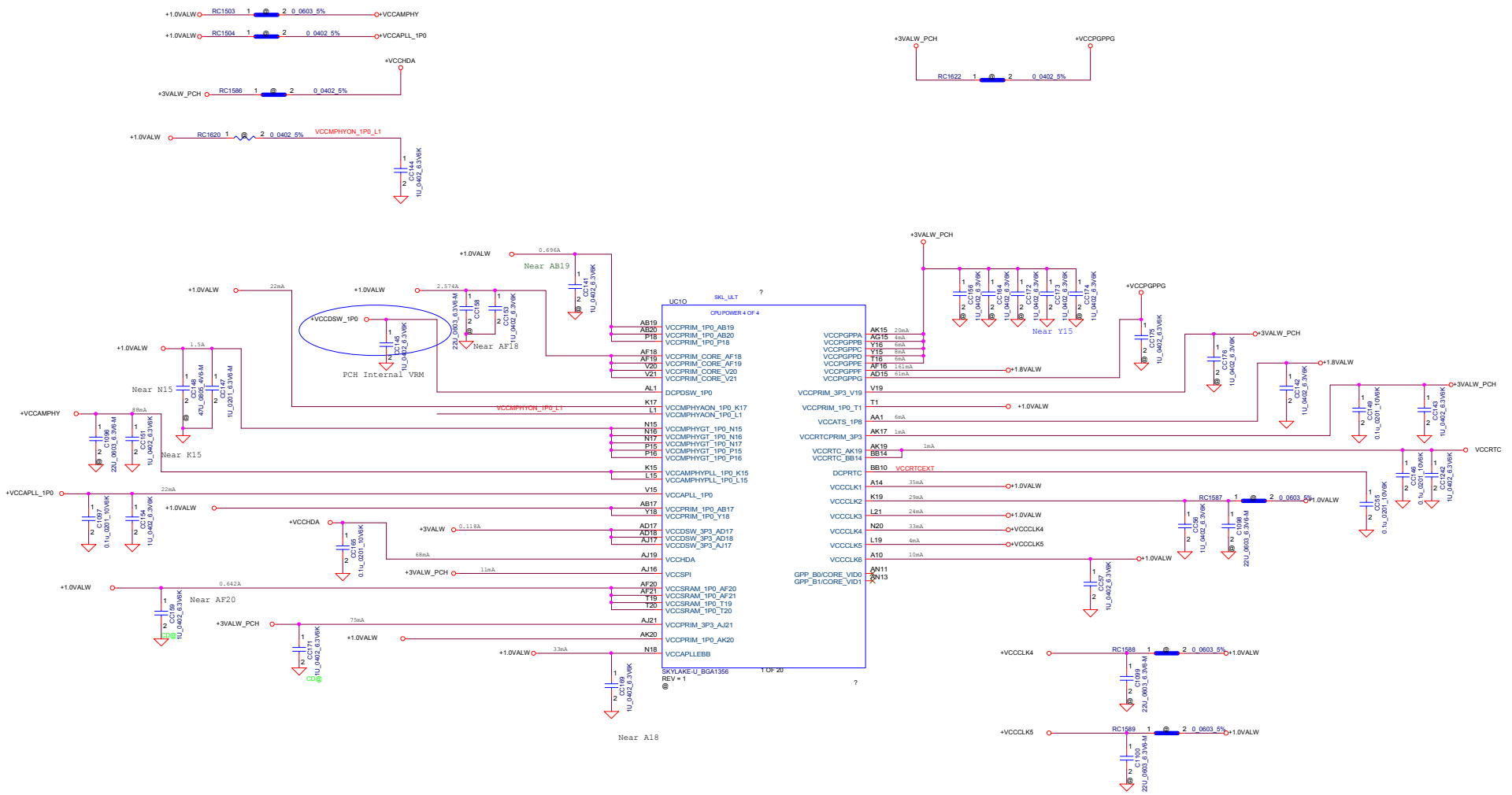
Title: **MCP (CPU PWR2)**

Size: Custom	Document Number: DG421	Rev: 1.0
Date: Sunday, January 22, 2017	Sheet 13 of 60	



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Title: MCP (PCH PWR)

Size	Document Number	Rev
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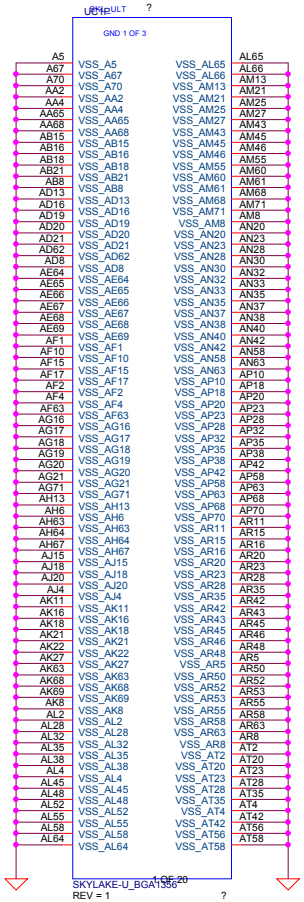

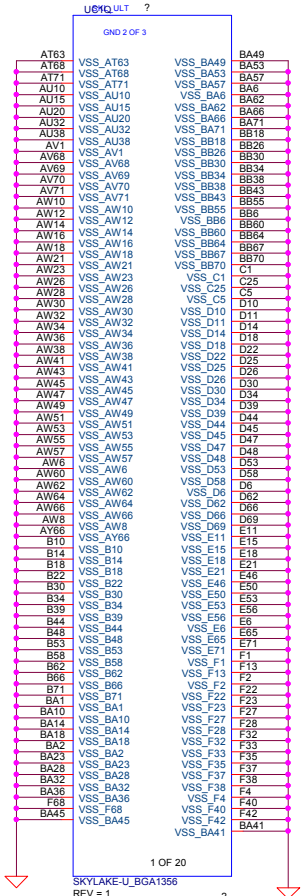

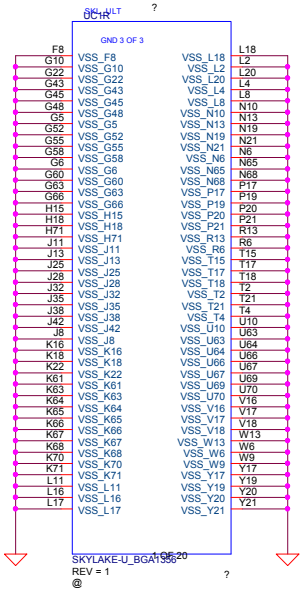

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Title: **MCP (VSS)**

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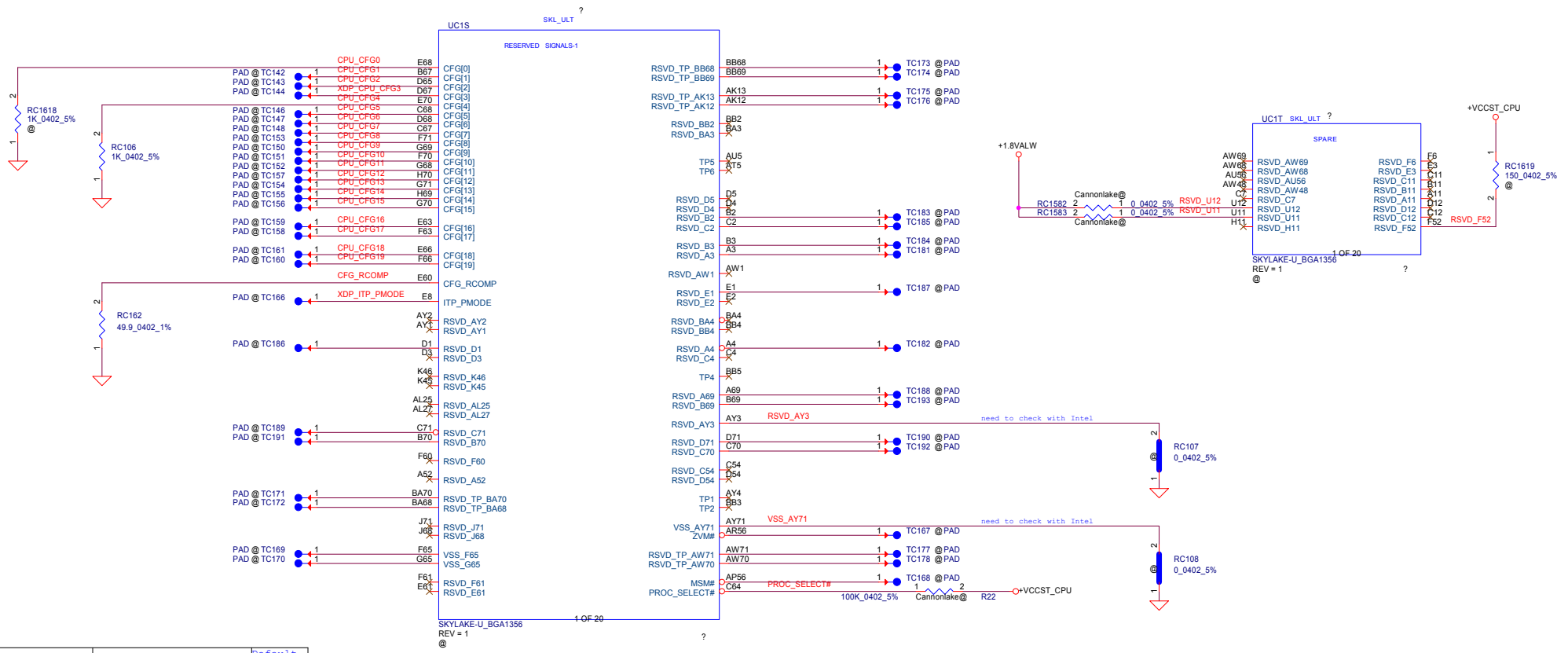

Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	– 1 = eDP Disabled – 0 = eDP Enabled ★	1

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Title: **MCP (CFG,RESERVED)**

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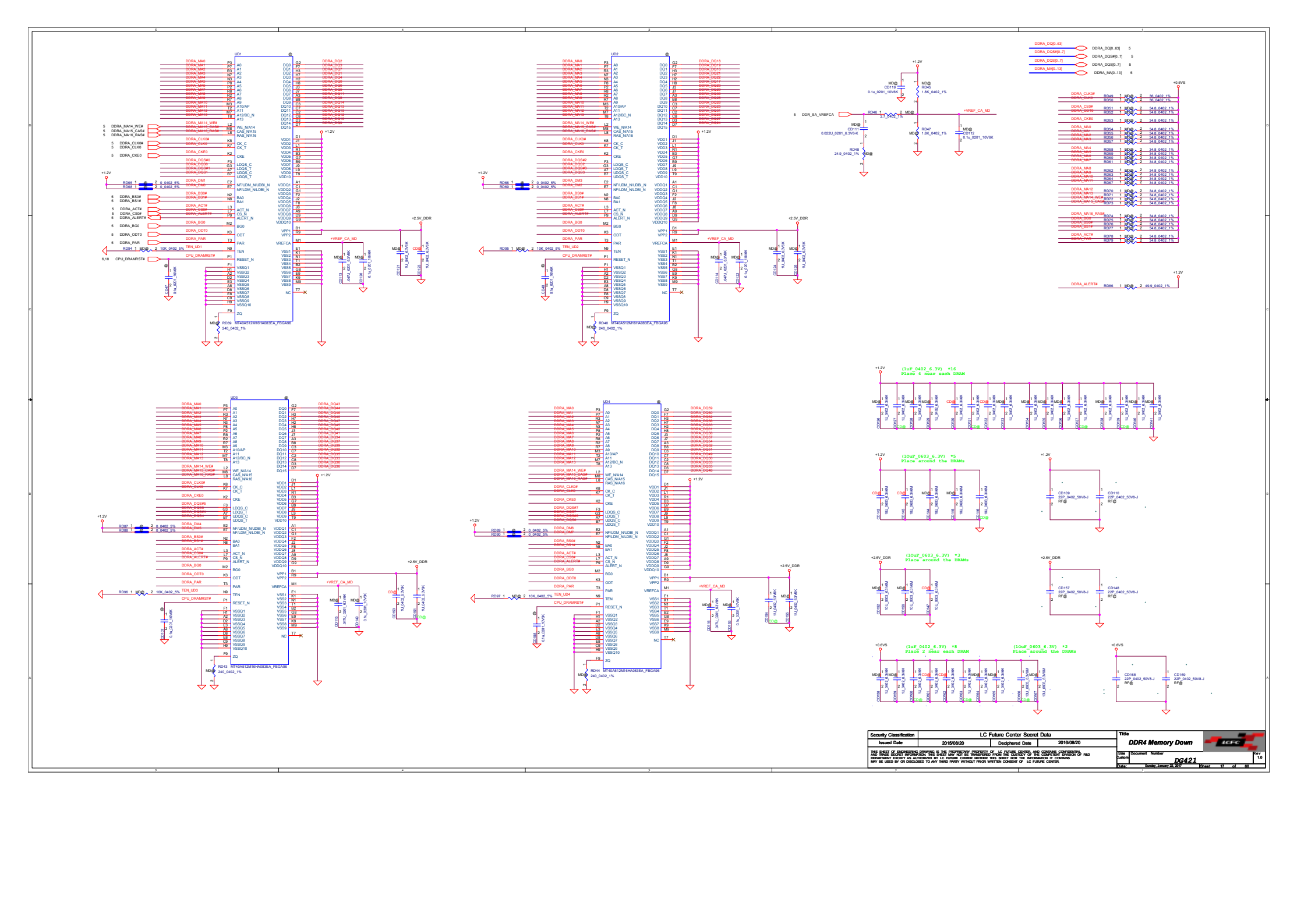

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Title: **DDR4 Memory Down**

Size	Document Number	Rev
Custom	DG421	1.0

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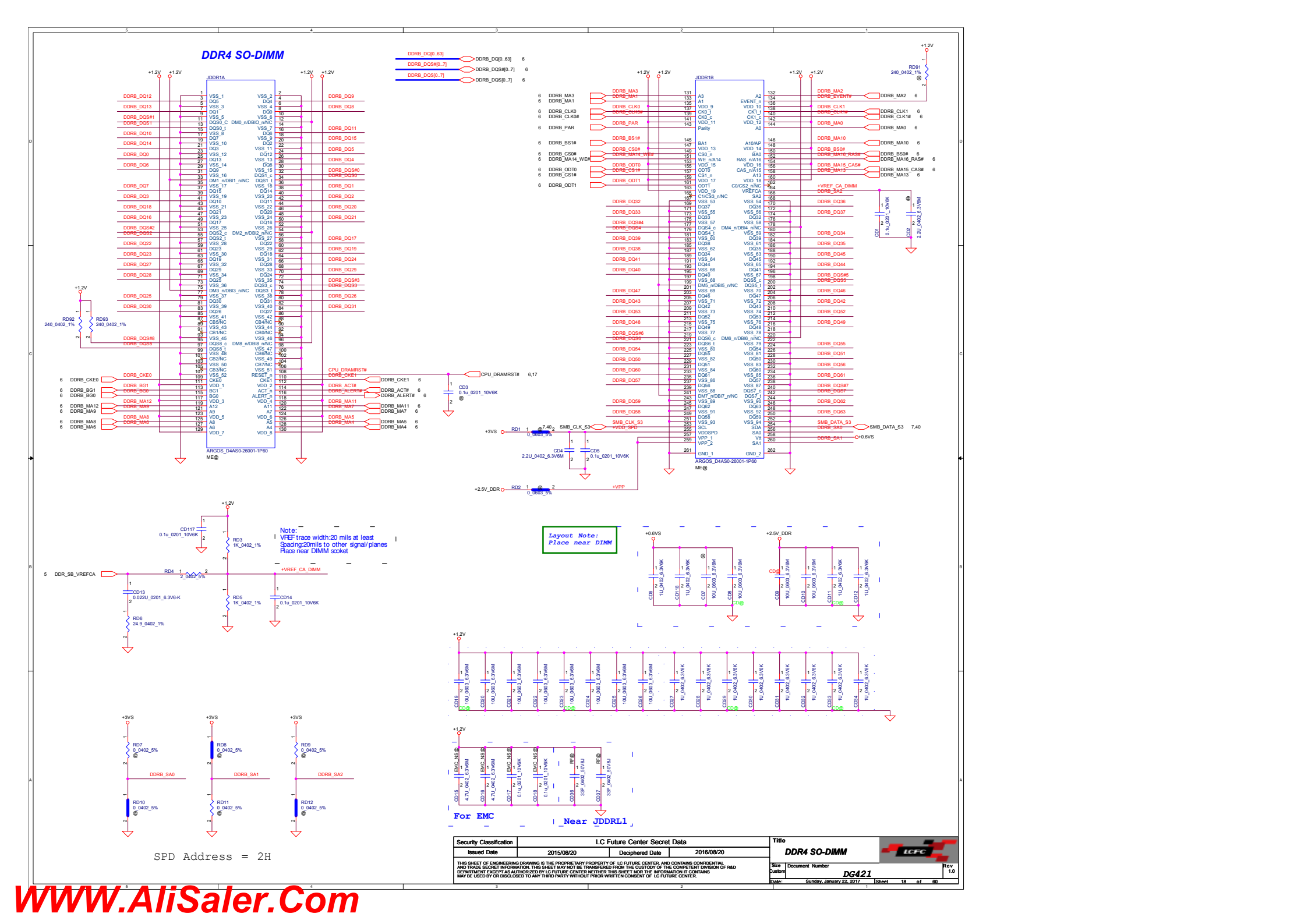

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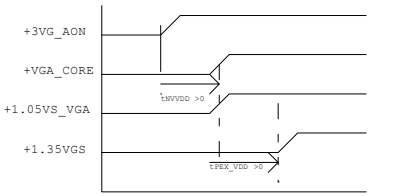
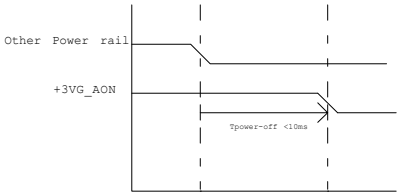
N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence



1. all power rail ramp up time should be larger than 40us~4ms



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	(1.05V) (6) (mA)	(1.05V) (6) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

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Title: VGA Notes List

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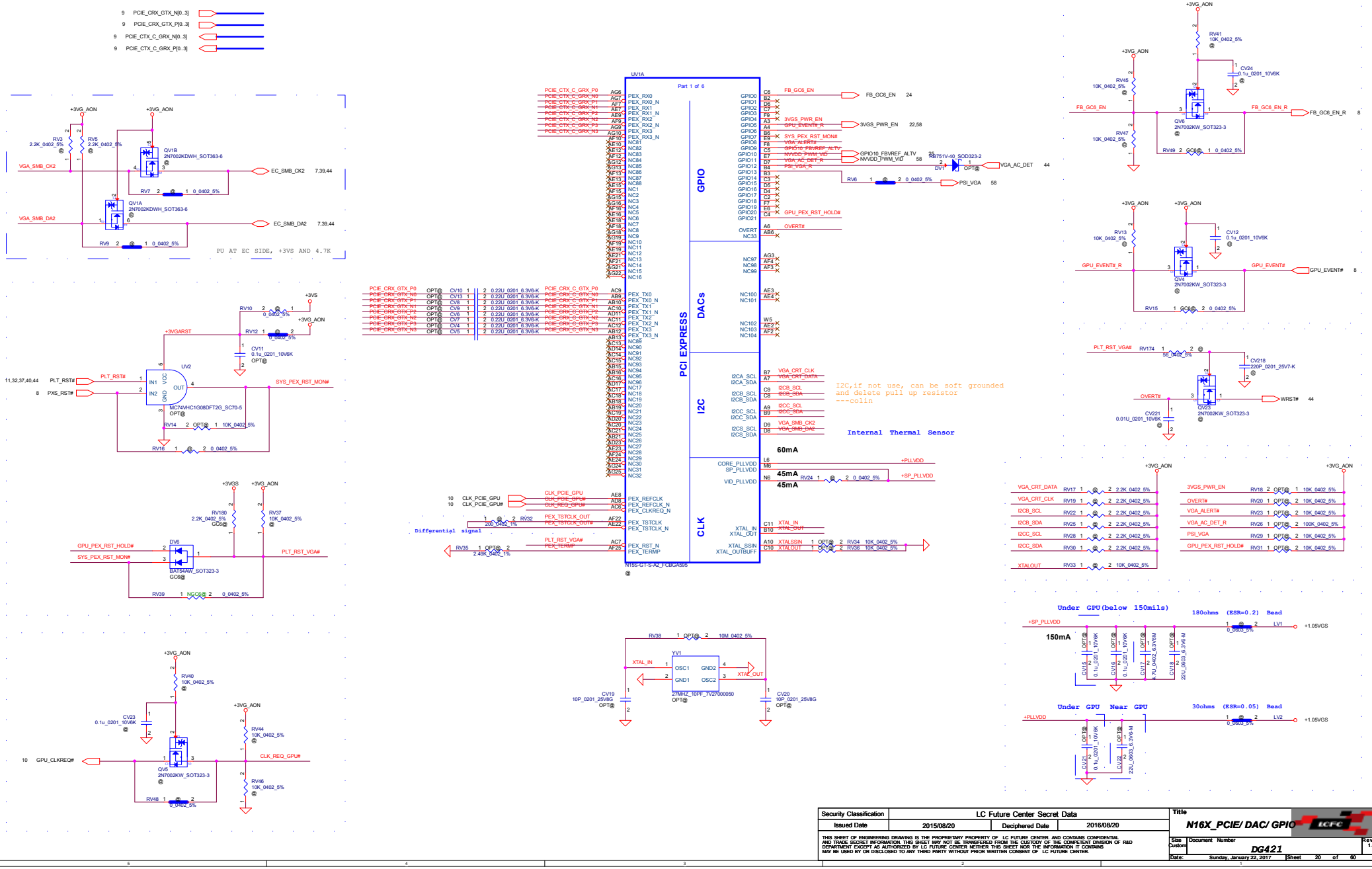

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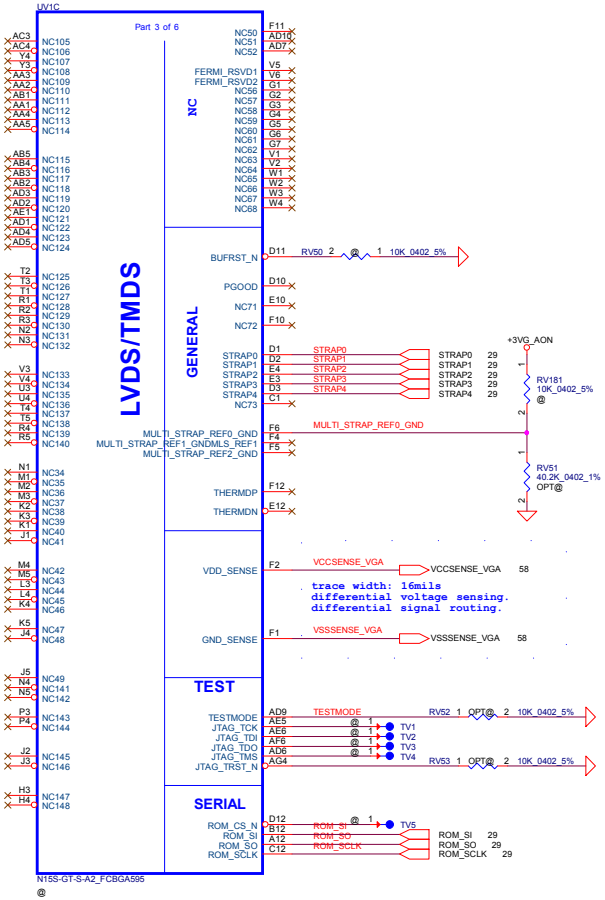

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Title: N16X_LVDS/ HDMI/ THERM

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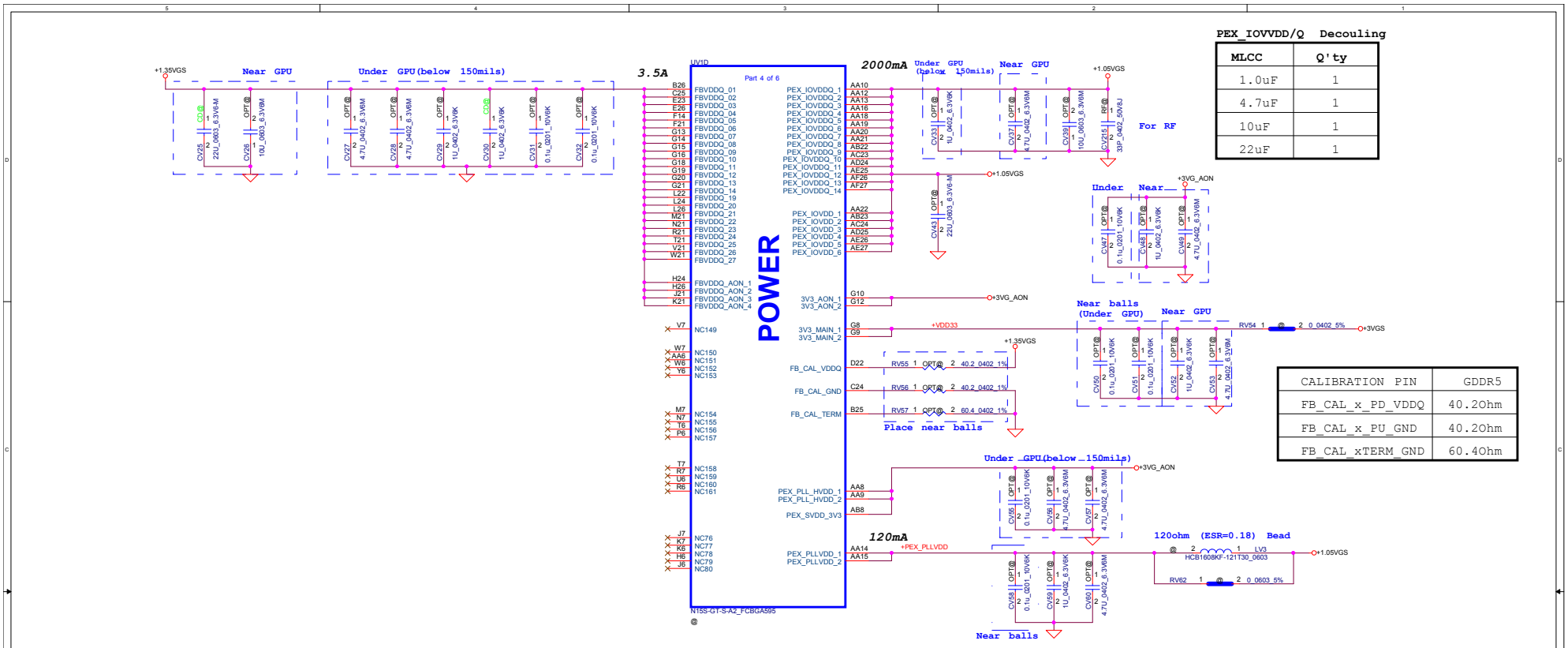
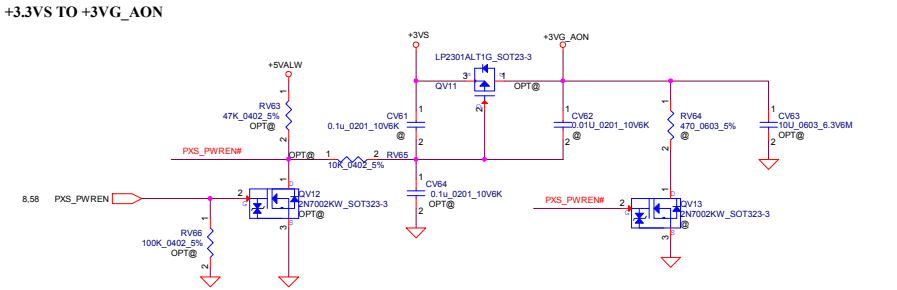
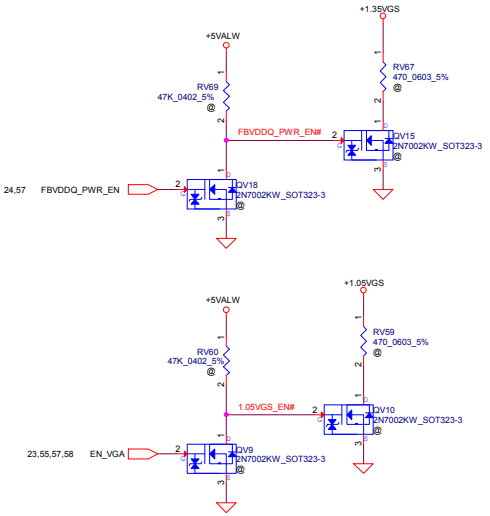


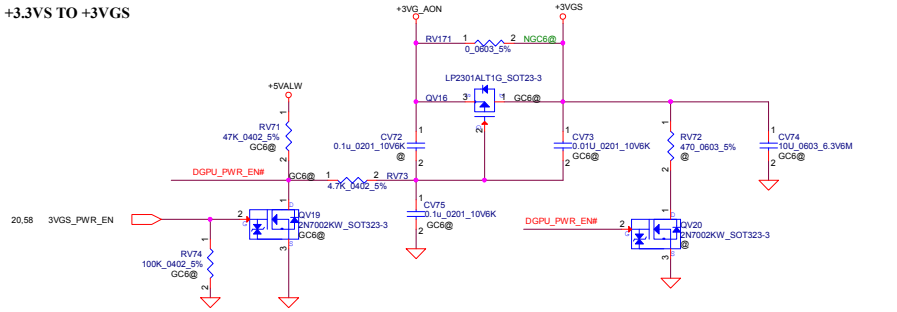
PEX_IOVVDD/Q Decouling

MLCC	Q'ty
1.0uF	1
4.7uF	1
10uF	1
22uF	1

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm







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Title: **N16X_Power**

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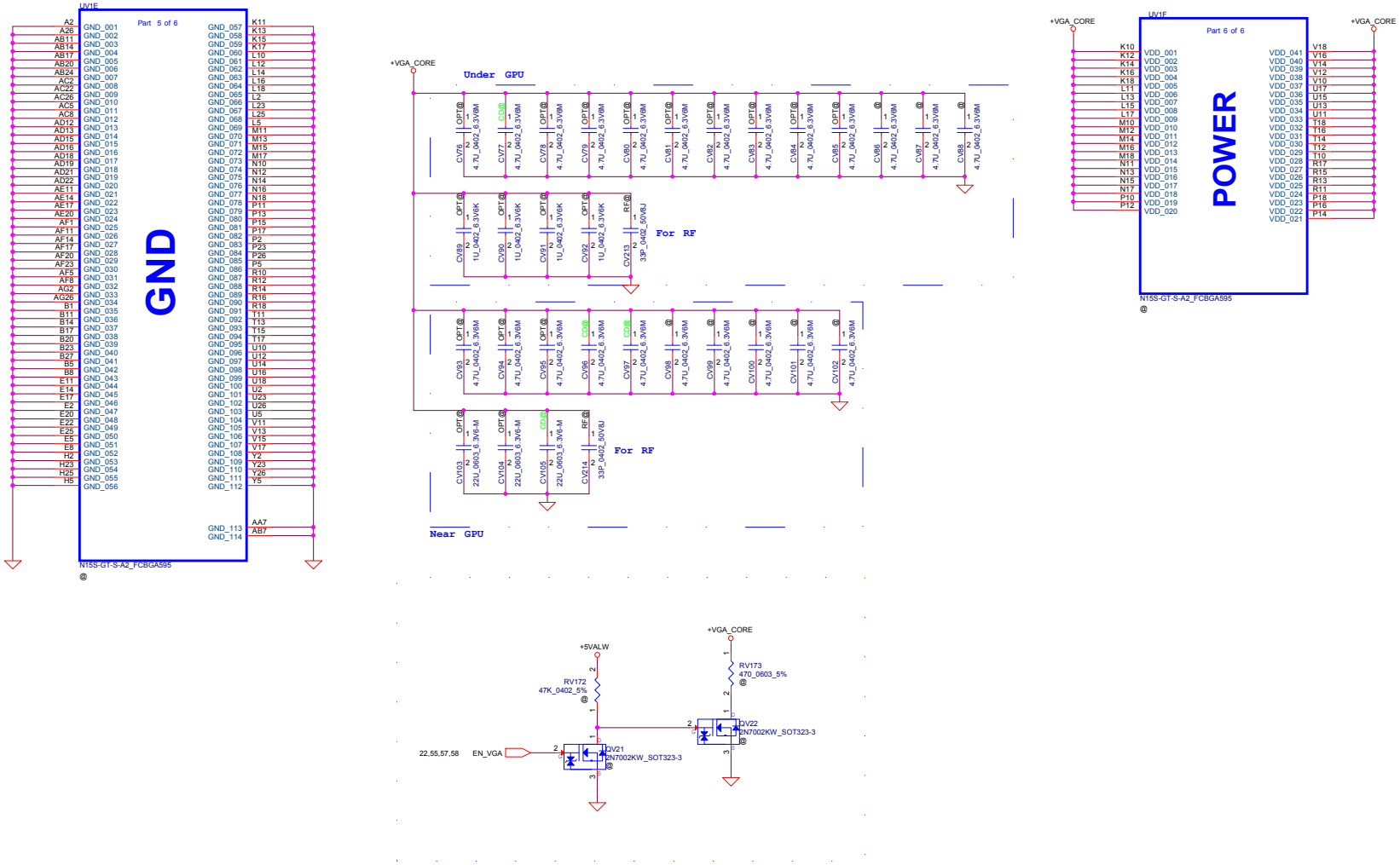

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Title: N16X_+VGA CORE, GND

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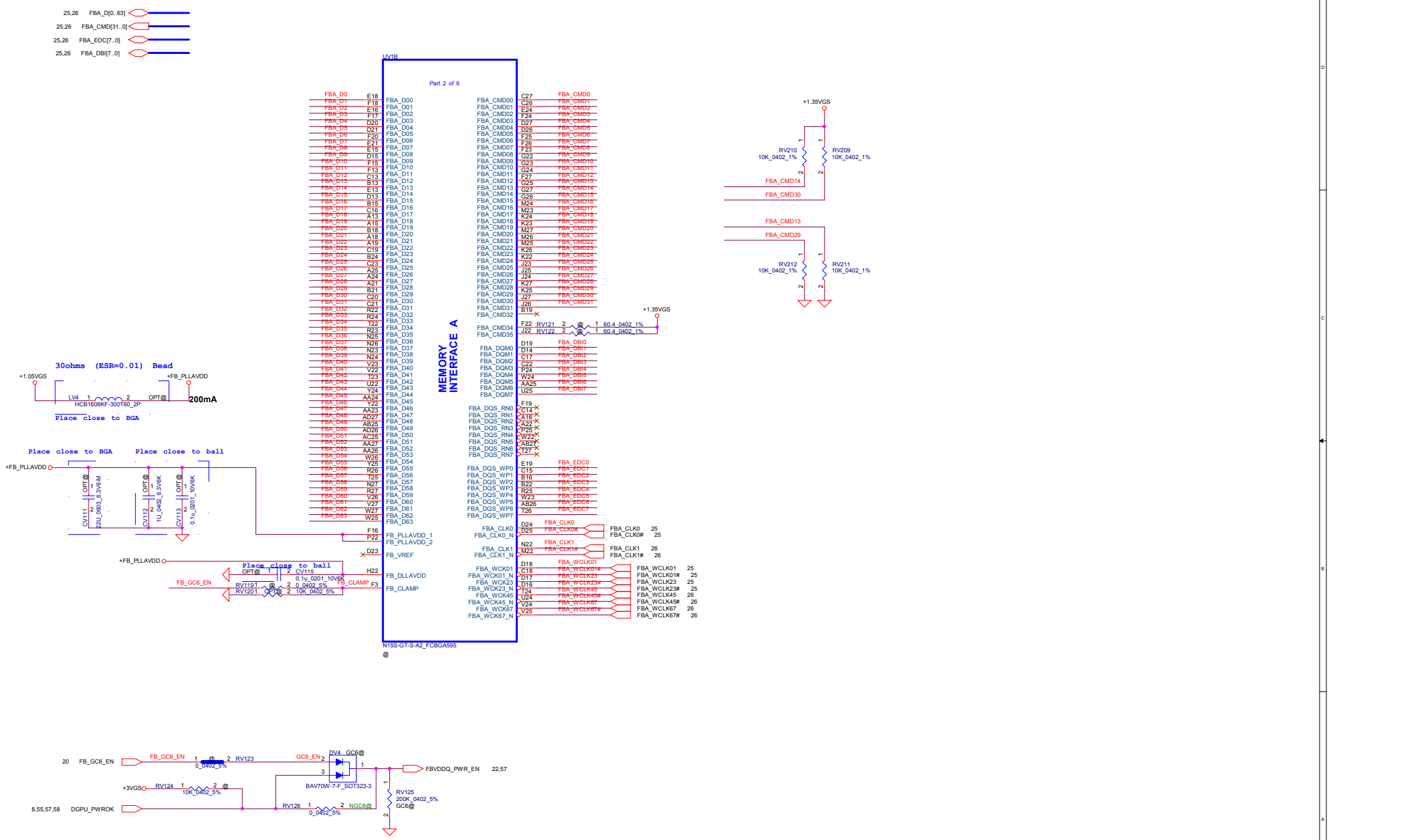

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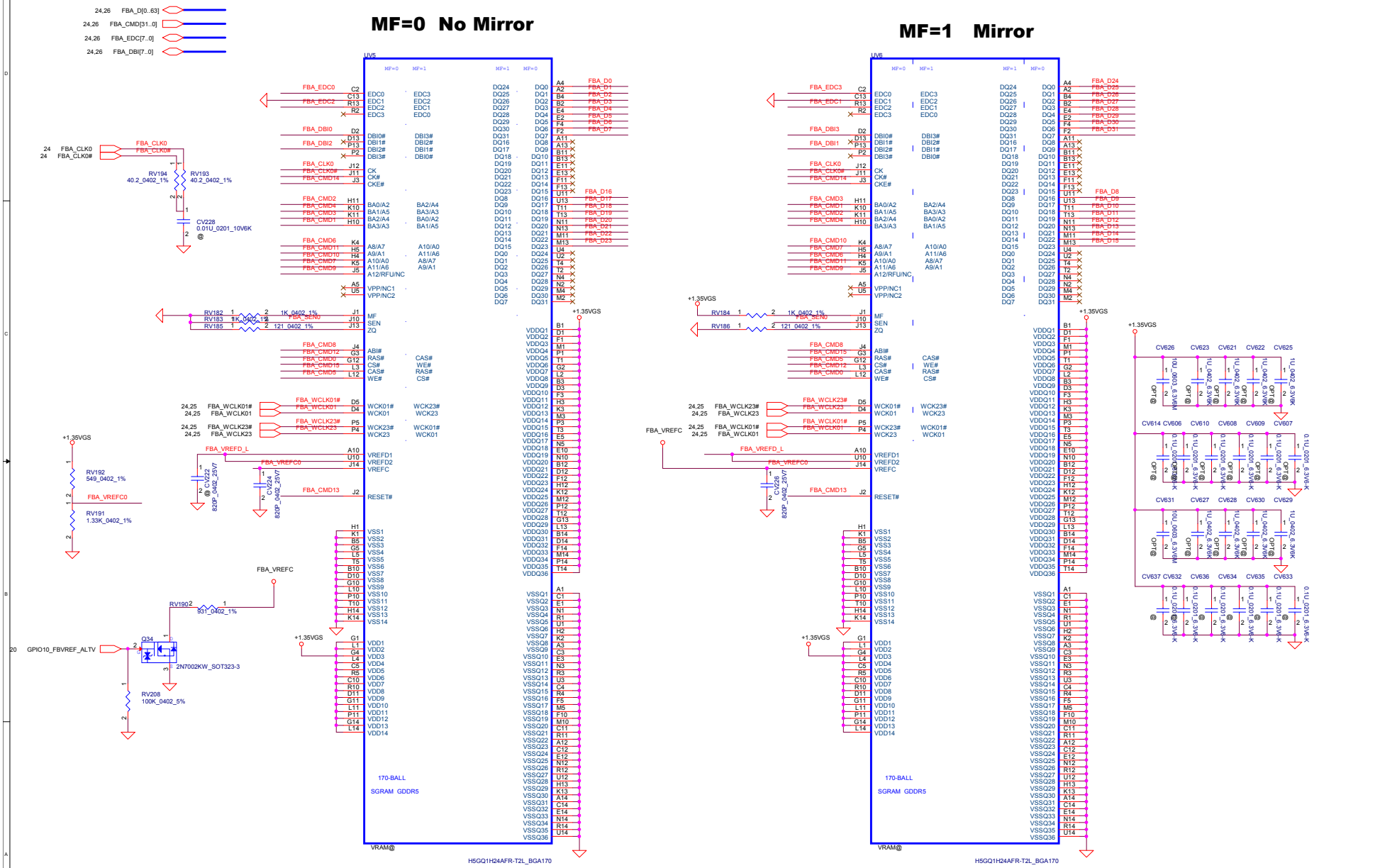
Lower 32 bits



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Title: N16X_GDDR5_Rank0_[31:0]

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C	DG421	1.0

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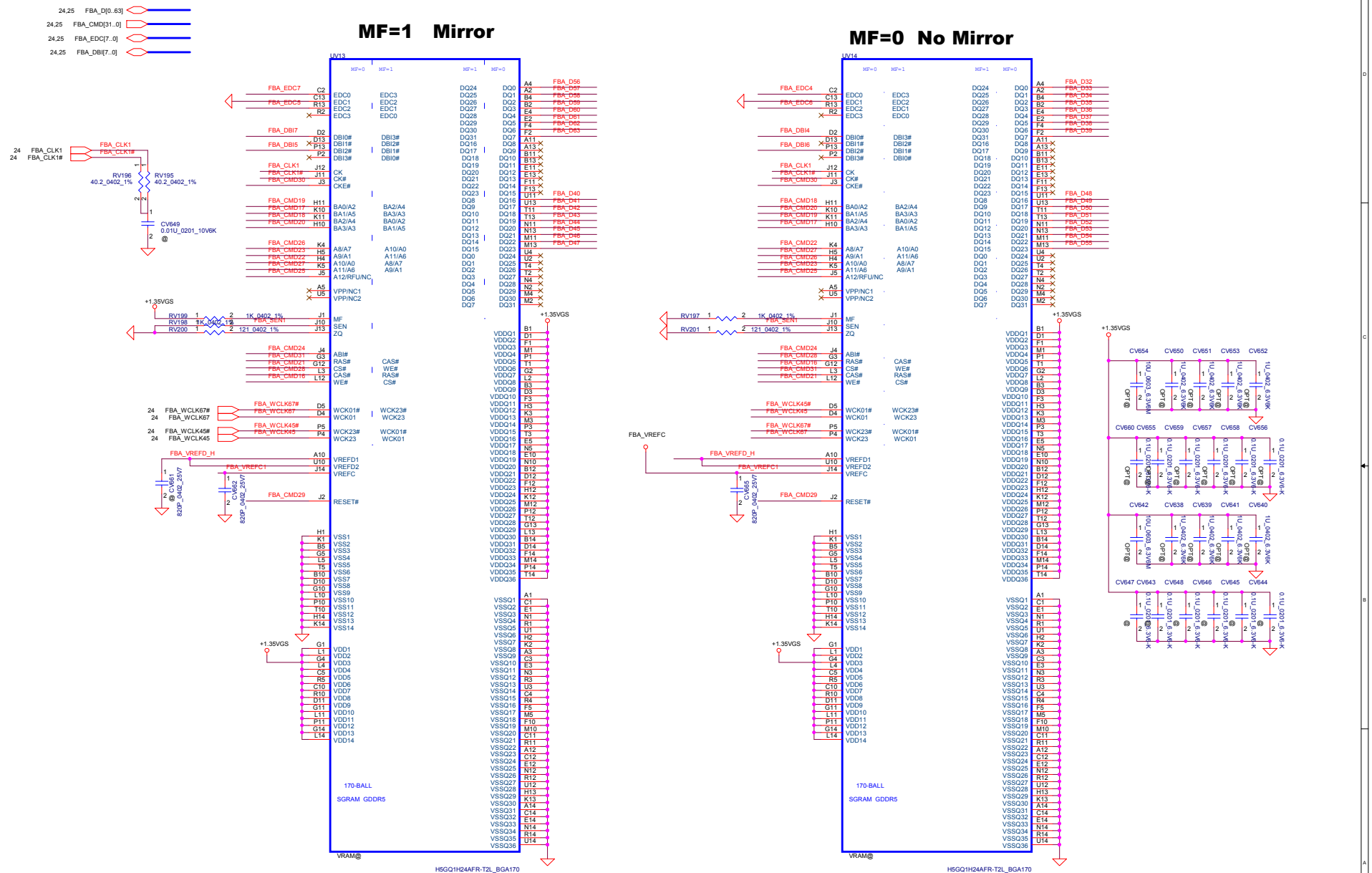
upper 32 bits



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Title

N16X_DDR3_Rank1_[31:0]

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Title

N16X_DDR3_Rank1_[64:32]

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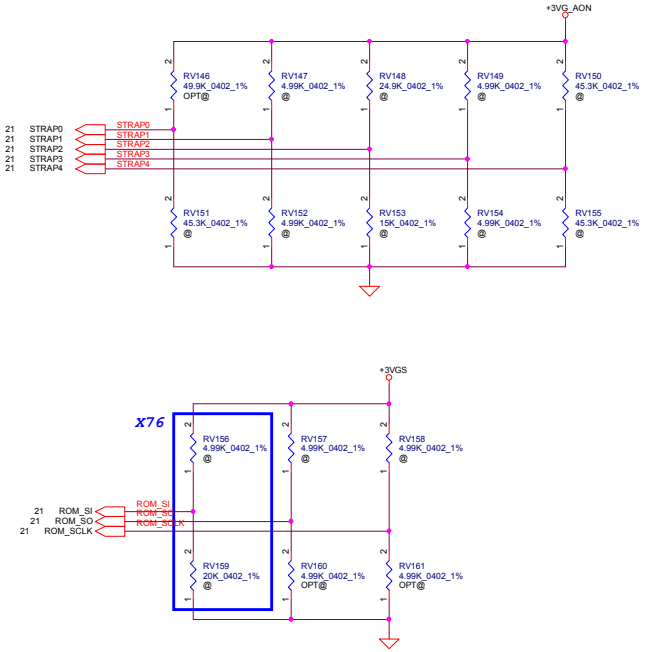

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

GPU	Configuration	FB Memory (DDR3L)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR1	2G VRAM	Samsung 2500MHz	K4G41325FE-HC28	0x7	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
			256M x 16	PD 45.3K							
		Hynix 2500MHz	H5GC4H24AJR-T2C	0x6							
			256M x 16	PD 34.8K							
		Micron 2500MHz	EDW4032BABG-60-F	0x4							
			256M x 16	PD 24.9K							
	4G VRAM	Samsung 2500MHz	K4G80325FB-HC03	0x0							
			512M x 16	PD 4.99K							
		Hynix 2500MHz	H5GC8H24MJR-T2C	0x5							
			512M x 16	PD 30.1K							
		Micron 2500MHz	MT51J256M32HF-60:A	0x1							
			512M x 16	PD 10K							

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Title: N16X_MISC

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Digital power for HDA link

Analog power for mixers, & IO ports

Power supply for full-bridge left/ Right channel

8/ 29 Add +1.8VS Circuit for Audio wei

Analog power for DACs, ADCs

Digital power for digital I/ O circuit

Power for card reader controller

Power for combo jack depop circuit at system shutdown mode

To solve the background noise while combojack connecting to an active speaker and system entry into S3/ S4/ S5 without analog power.

11/ 8 SIT Vendor suggestion form 47 ohm change to 51om wei

11/ 8 SIT Cost down to 0ohm wei

8/ 16 Update Audio Jack P/ N SP011509163 wei

FOR EMI

For EMI

Audio Jack

8/ 16 Update Audio Jack P/ N DC021608101 wei

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Title: Codec & CR_RTS5199

Size: C | Document Number: DG421 | Rev: 1.0

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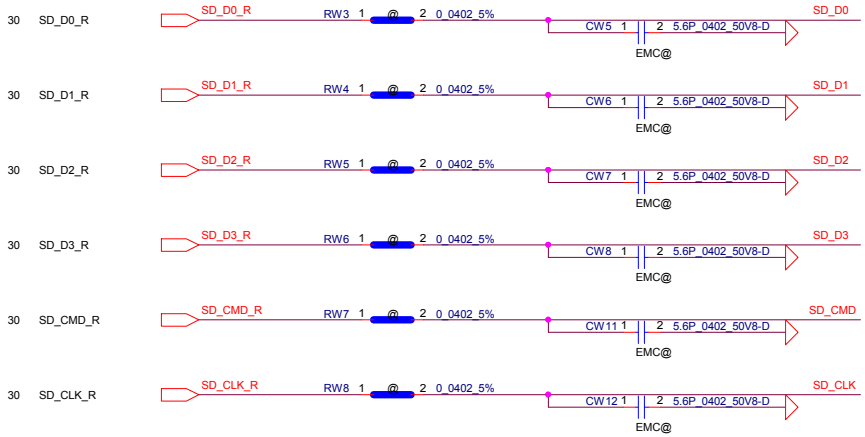

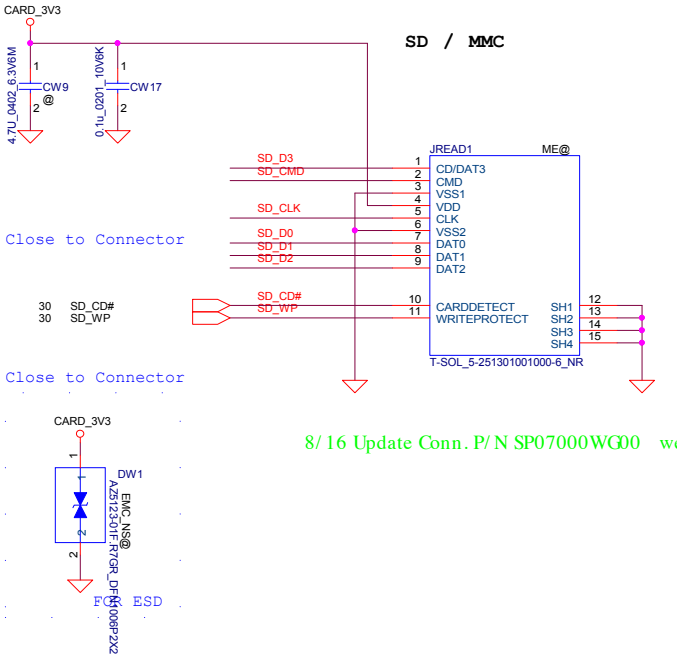

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Title: **Cardreader**

Size	Document Number	Rev
Custom	DG421	1.0

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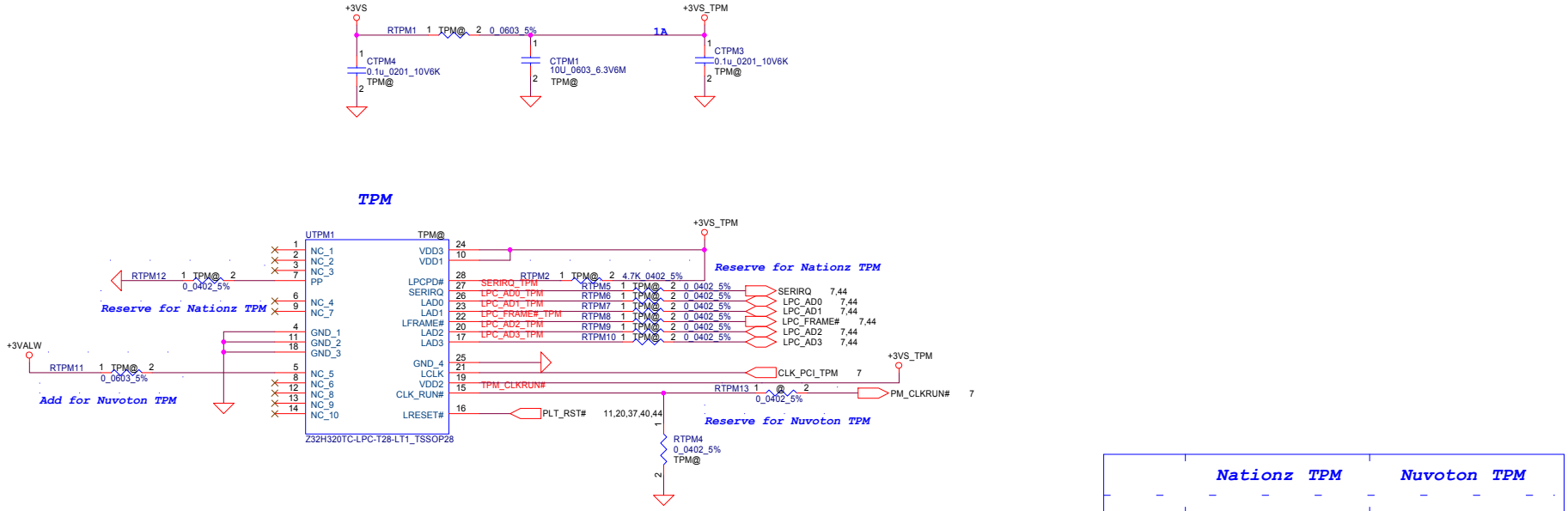

	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: TPM

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Custom	DG421	1.0

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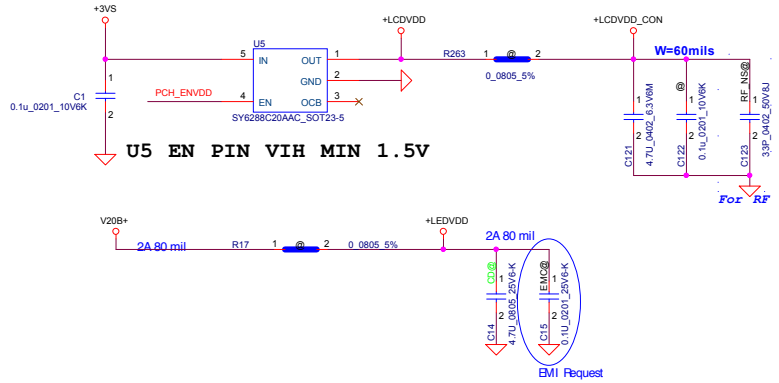
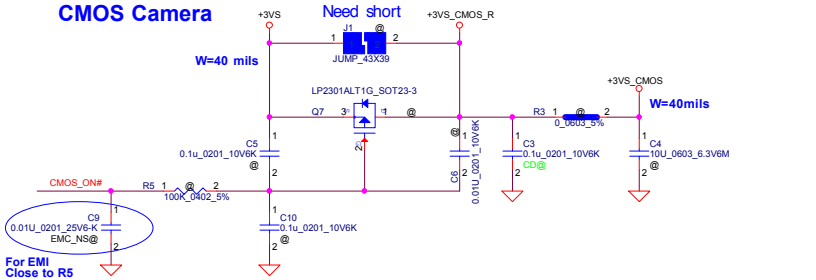
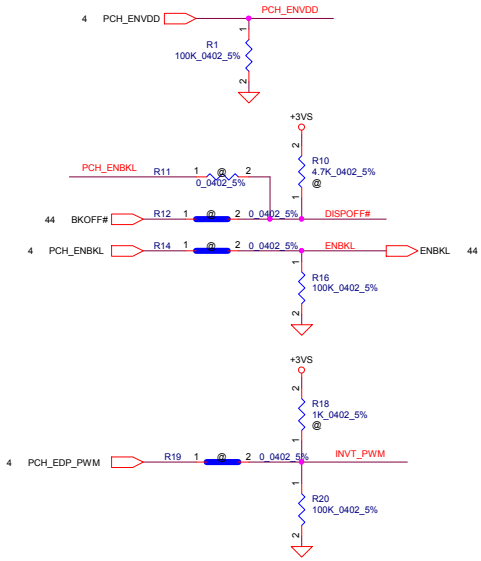
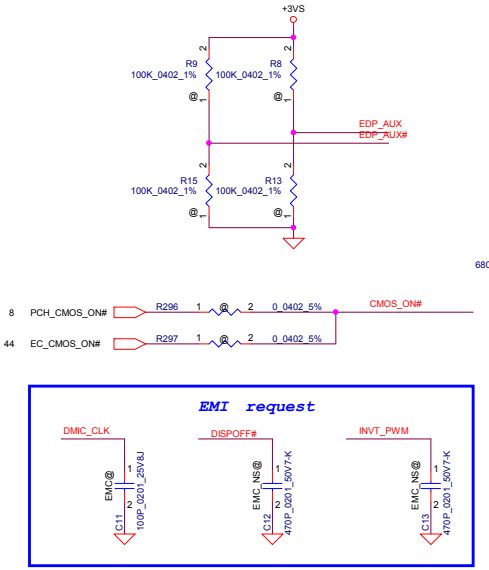
LCD POWER CIRCUIT

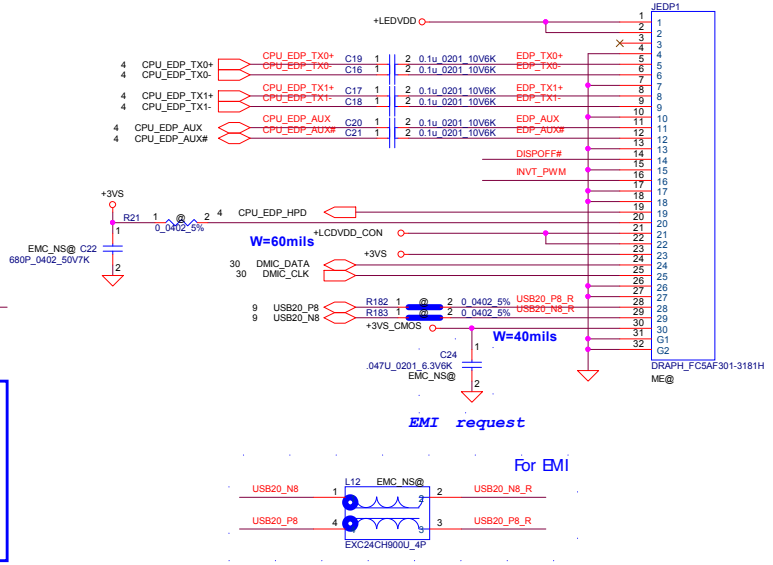


CMOS Camera

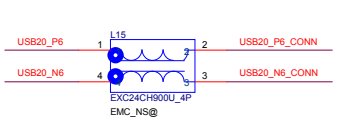




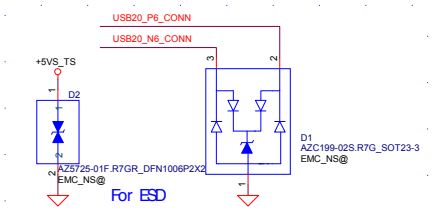


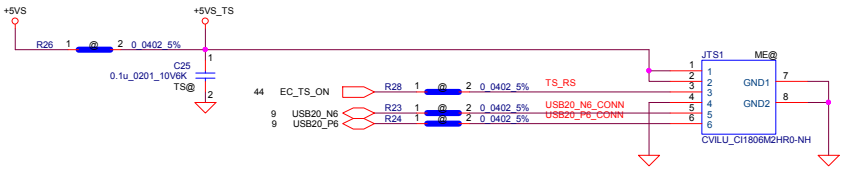


Touch Screen



Touch Screen





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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: eDP/CMOS/Touch screen

Size	Document Number	Rev
Custom	DG421	1.0

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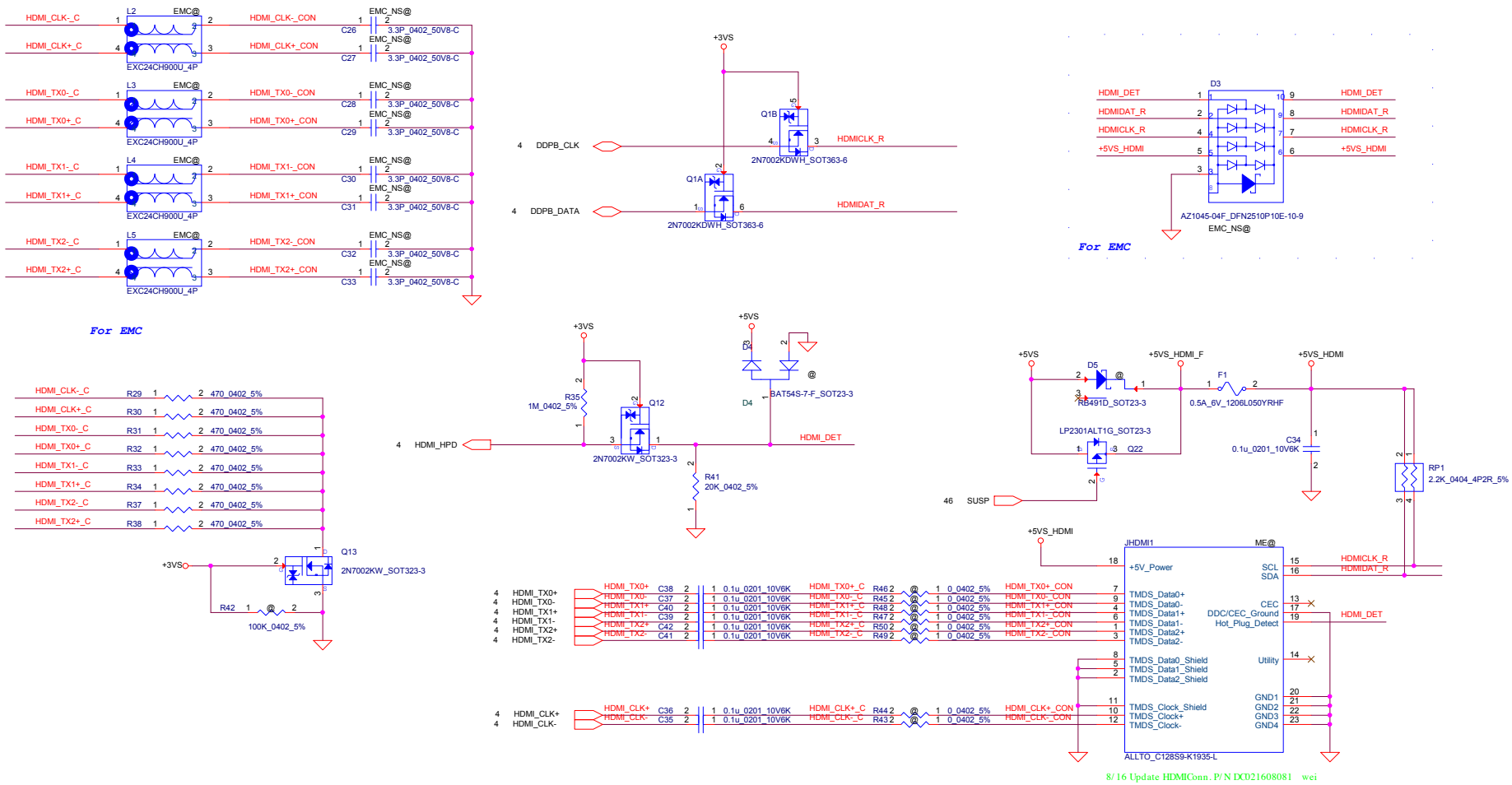

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title	HDMI_CONN		
Size	Document Number		Rev
Custom	DG421		1.0
Date:	Sunday, January 22, 2017	Sheet	34 of 60

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Title

P35-Blank

Size	Document Number	Rev
Custom	*DG421*	1.0

Date: Sunday, January 22, 2017 Sheet 35 of 60

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Title

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Size	Document Number	Rev
Custom	*DG421*	1.0

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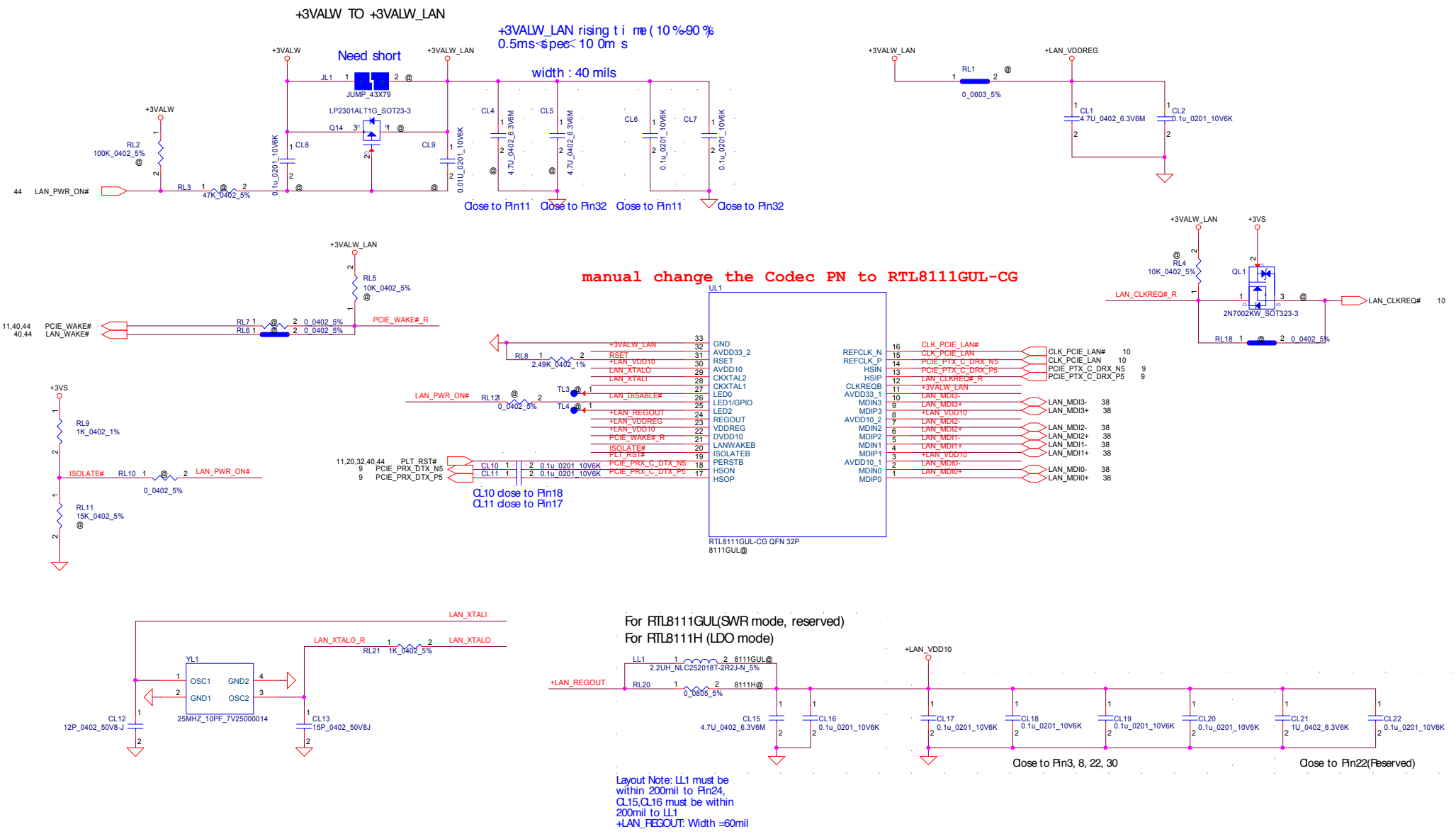

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: **LAN_RTL8111H_CG**

Size	Document Number	Rev
Custom	DG421	1.0

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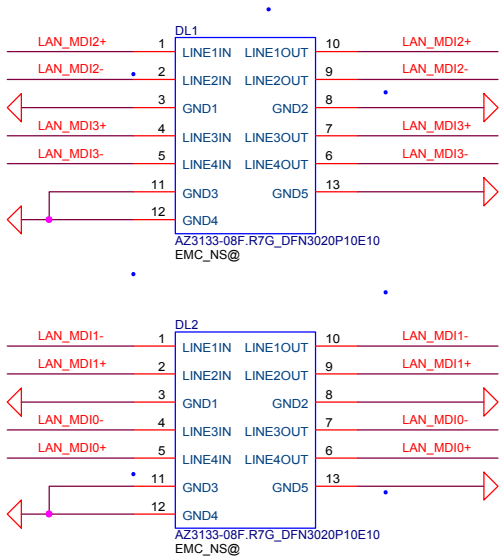
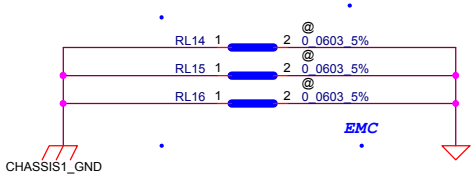
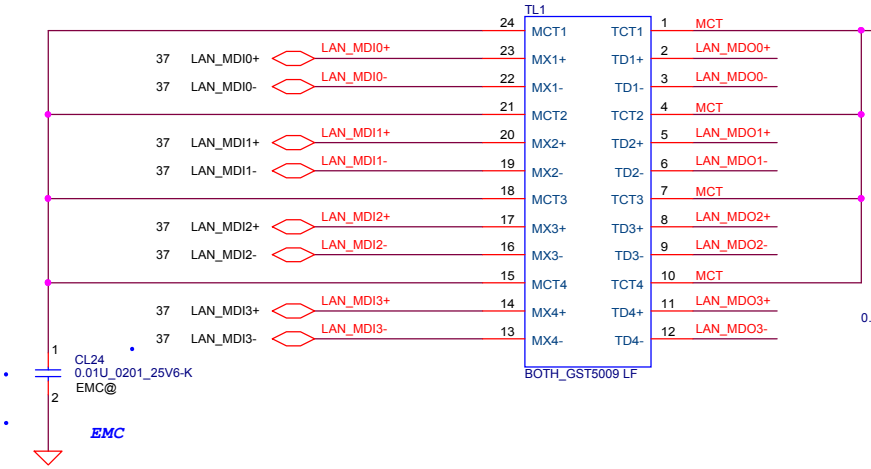
DL1/DL2
1'S PN:SC300003M00

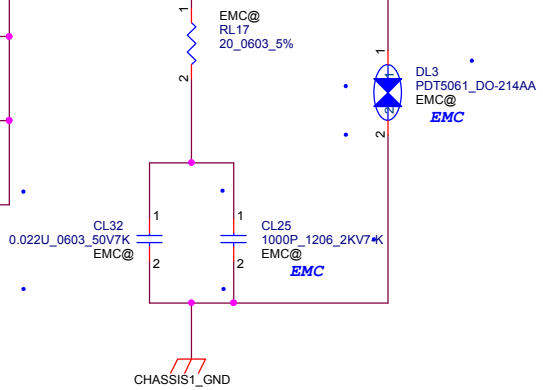


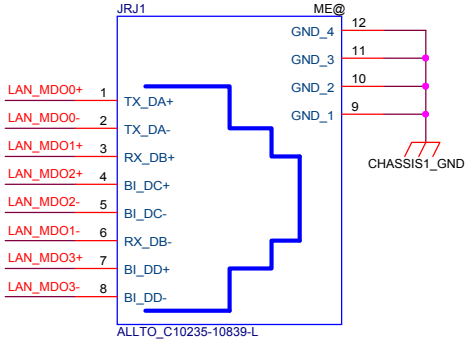
Place Close to TL1

EMC









8/16 Update RJ45 P/N DC021608091 wei

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Title: LAN_Transformer

Size	Document Number	Rev
B	DG421	1.0

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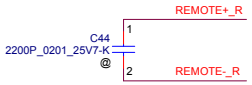
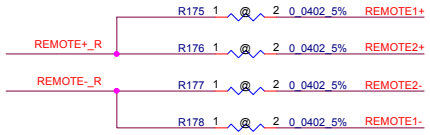
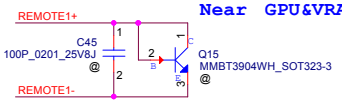
Close to U1



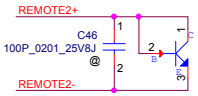


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

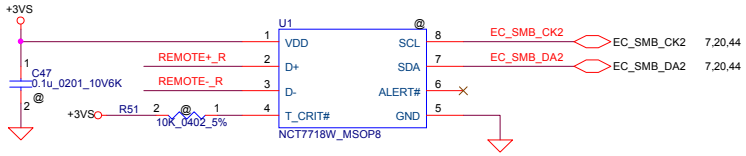
Near GPU&VRAM



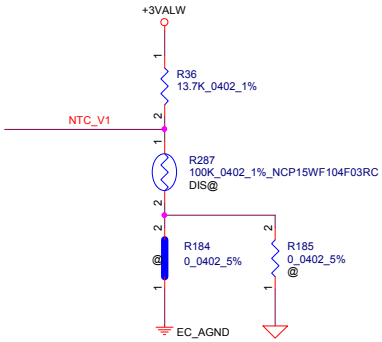
Near CPU core



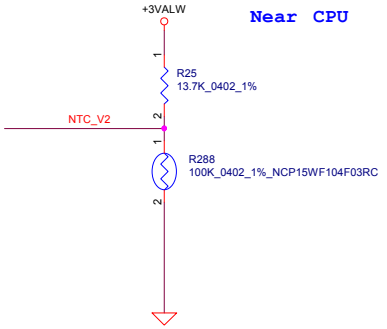
SMSC thermal sensor
placed near DIMM



Address 1001_101xb

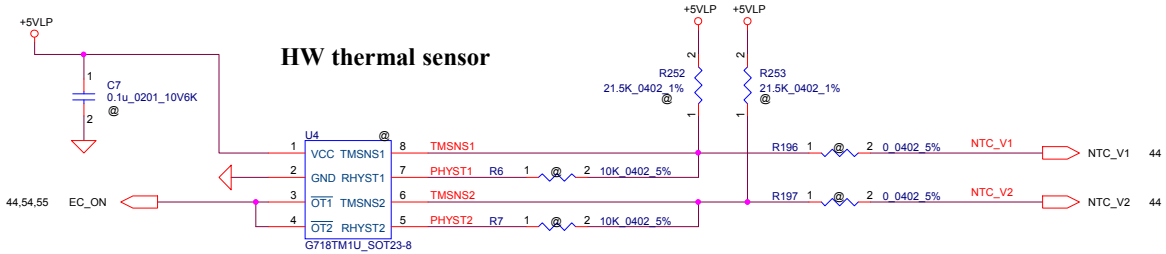


Near CPU



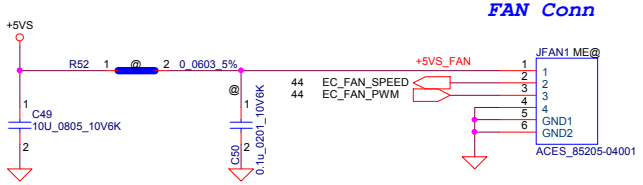
for layout optimized, change the EC_AGND to GND

HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

FAN Conn



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Title: Thermal sensor/FAN CONN

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Custom	DG421	1.0

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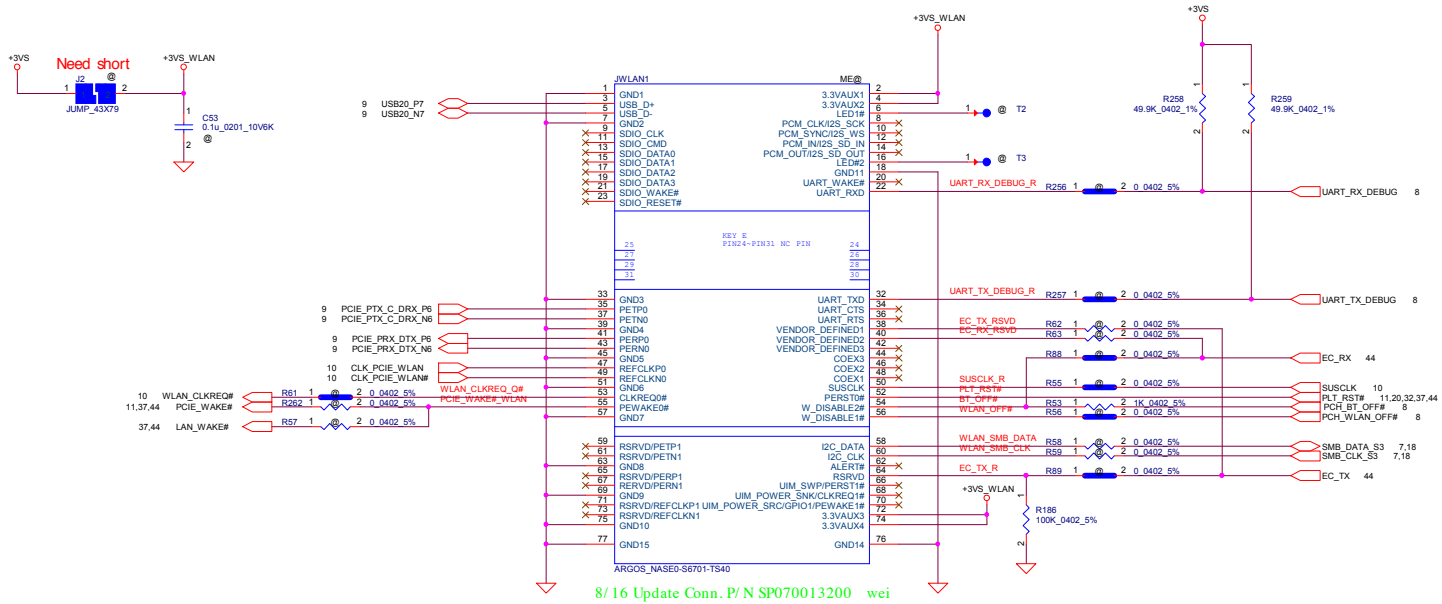
Mini-Express Card(WLAN/WiMAX)



8/16 Update Conn. P/N SP070013200 wei

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Title	NGFF WLAN&SSD	
Size: C	Document Number: DG421	Rev: 1.0
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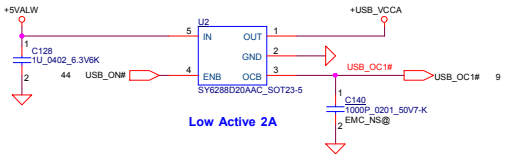
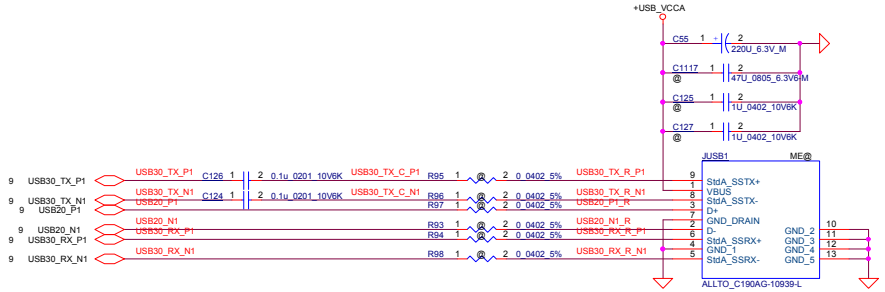
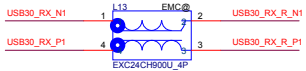
LEFT SIDE USB3.0 PORT x2





09/05 Update USBConn. P/N DC021609011 wei



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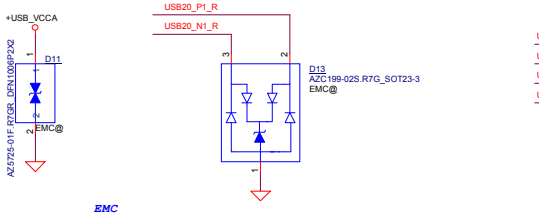

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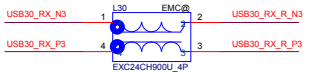
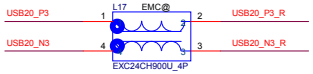
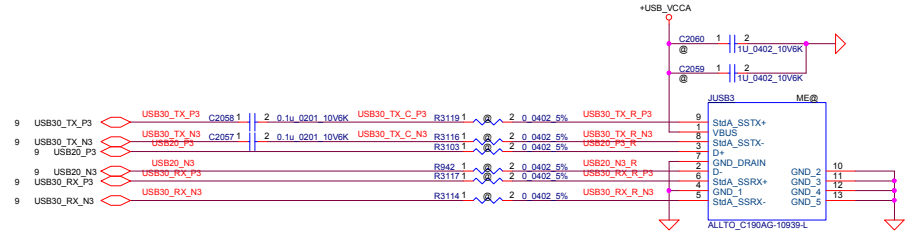
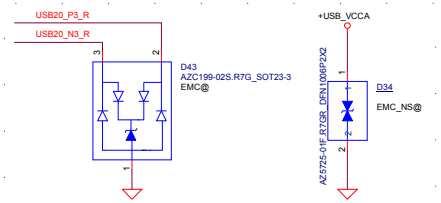


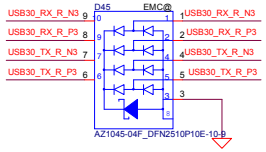




09/05 Update USBConn. P/N DC021609011 wei

FOR ESD Close to Connector





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Title: **USB3.0 PORT (LEFT)**

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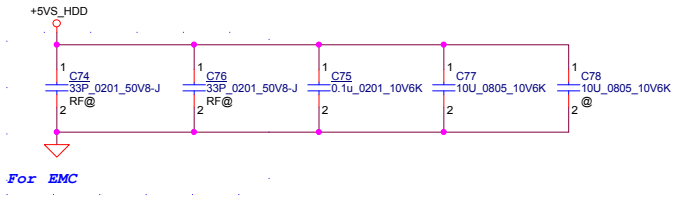
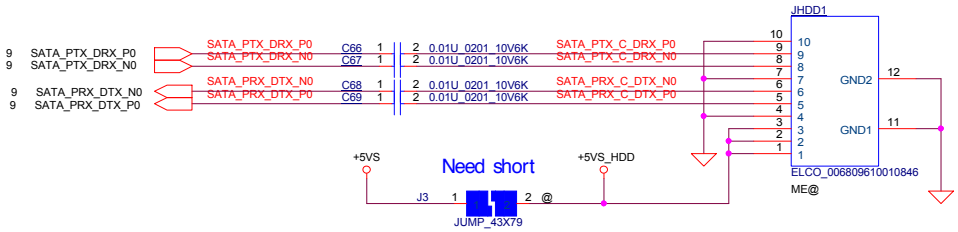
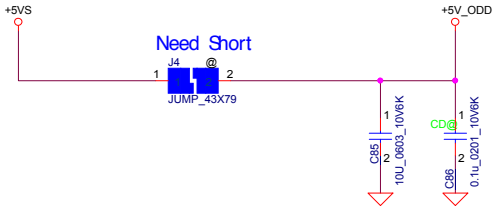
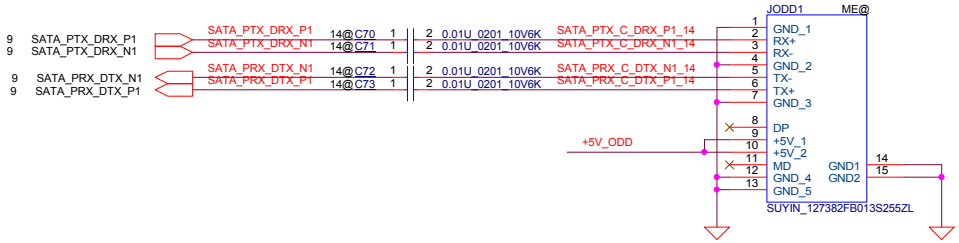
SATA HDD Conn.



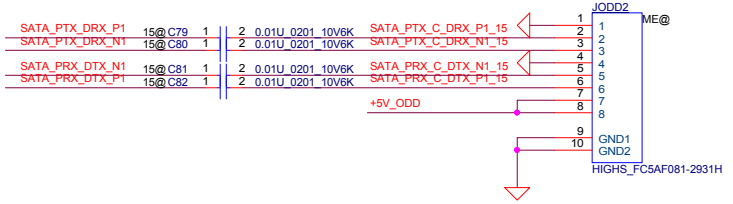




FOR 14"
SATA ODD Conn.



FOR 15" 17"
SATA ODD FFC Conn



8/16 Update Conn. P/N SP01001YV00 wei

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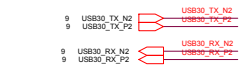
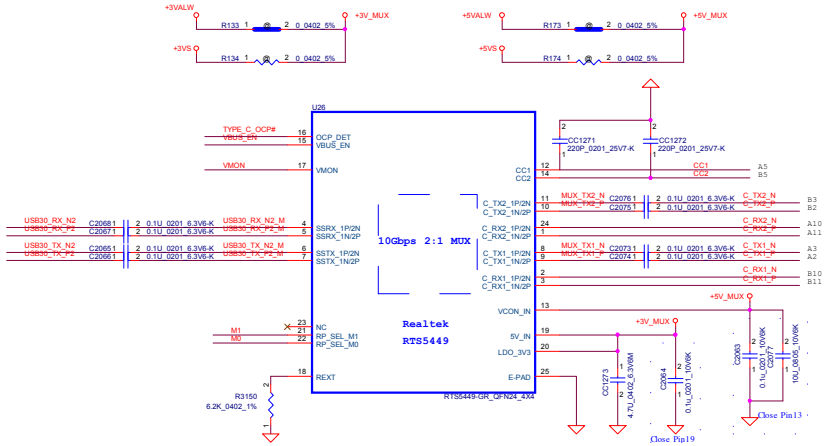
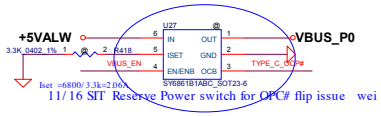
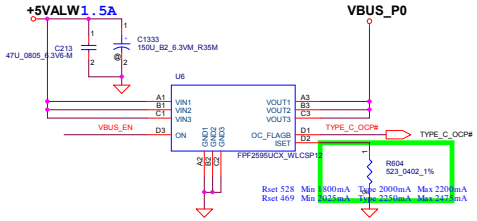
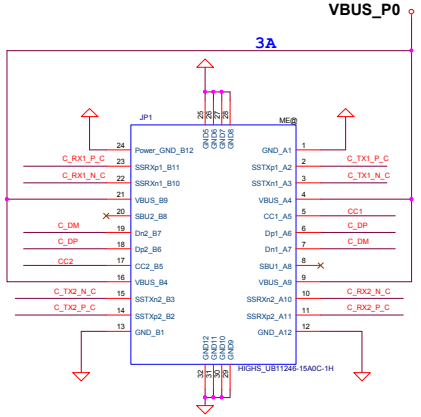




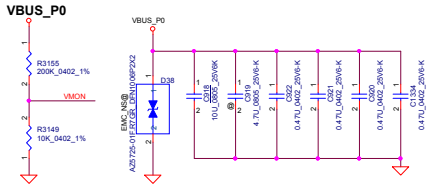


11/16 SIT Reserve Power switch for OPC# flip issue wei

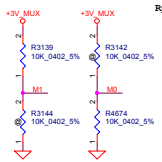




09/02 Update Type-C Conn. DC021608291 wei

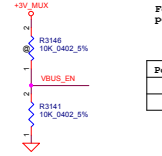


Rp configuration



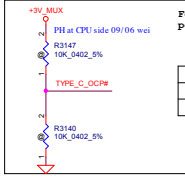
Rp:1.5A (now)

	M1	M0	Note
Rp:900mA	0	1	R3144/R3142 mount
Rp:1.5A	1	0	R3139/R3143 mount
Rp:3.0A	1	1	R3139/R3142 mount



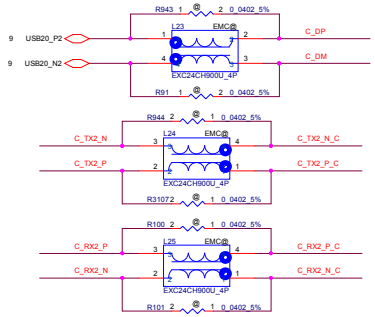
For C_VBUS
power switch enable pin

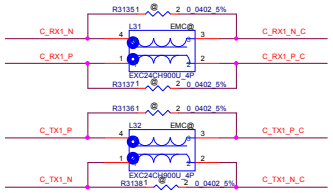
Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount

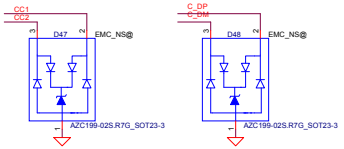


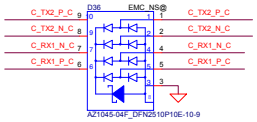
For C_VBUS
power switch OCP pin

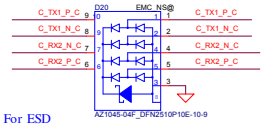
Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount











For ESD

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Title: 3D Camera

Size	Document Number	Rev
Custom	DG421	1.0

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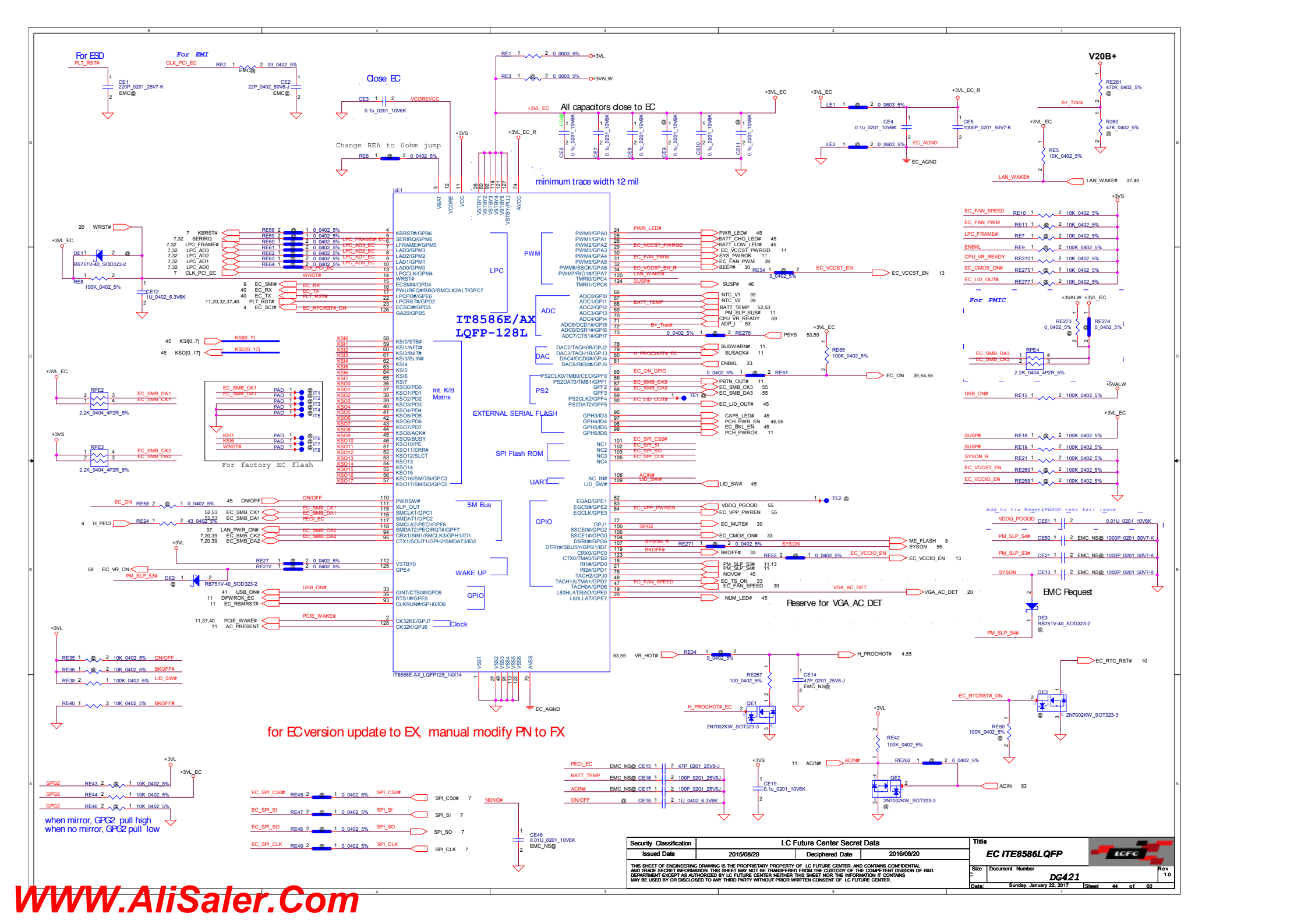
For ESD
For EMI
Close EC
Change RE6 to 0ohm jump
minimum trace width 12 mil
All capacitors close to EC
V20B+
IT8586E/AX
LQFP-128L
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
GPIO
SM Bus
WAKE UP
Clock
Int. K/B Matrix
For factory EC flash
For PMIC
EMC Request
Reserve for VGA_AC_DET
for ECversion update to EX, manual modify PN to FX
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Add to fix Reset&PWRGD test fail issue
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
Title
EC ITE8586LQFP
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Rev 1.0
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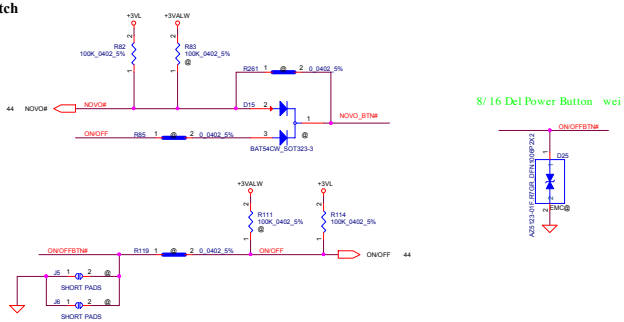
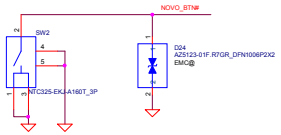
ON/OFF switch



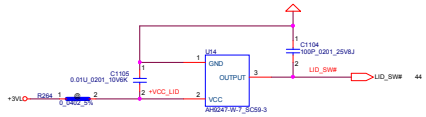
8/16 Del Power Button wei

Novo button

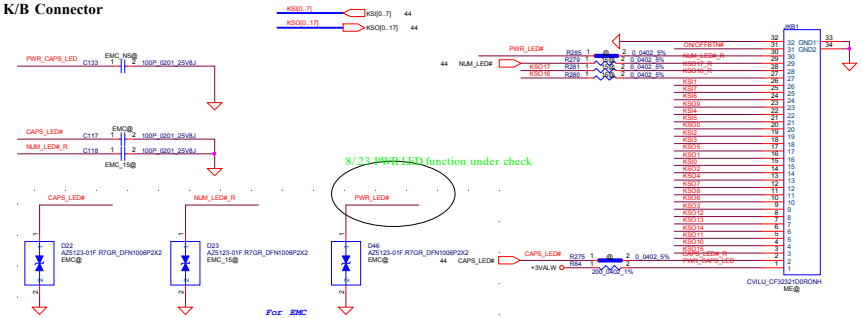


8/31 Update the P/N SN100008W00 wei

LID switch

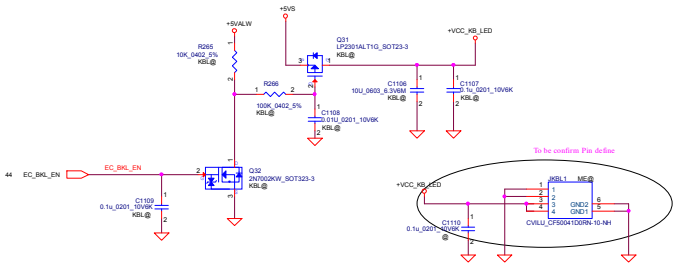


K/B Connector



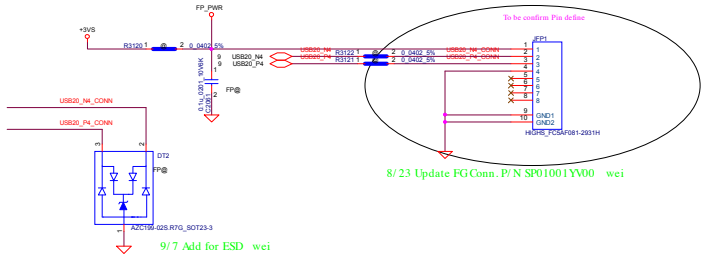
8/23 PWR LED function under check

KB Backlight Connector



8/31 Update KBL Conn. P/N SP011608241 wei

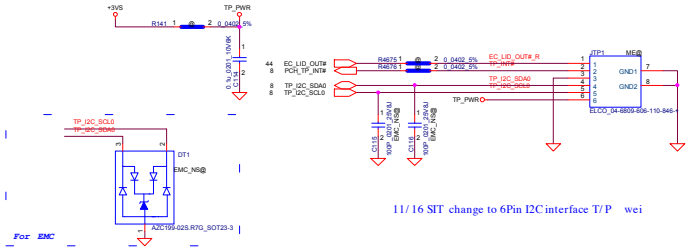
Finger Print Connector



8/23 Update FG Conn. P/N SP01001YV00 wei

9/7 Add for ESD wei

TP/B Connector



11/16 SIT change to 6Pin I2C interface T/P wei

PWR_LED Change to M/B (310->320) 08/17

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Title	KBD/PWR/IO/LED/TP Conn		
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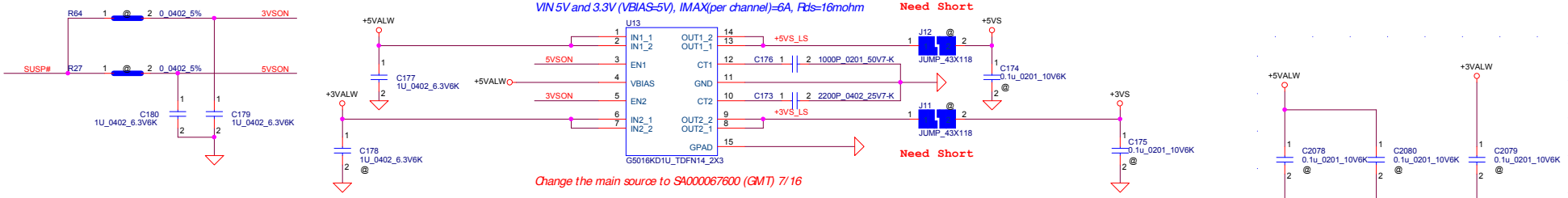
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

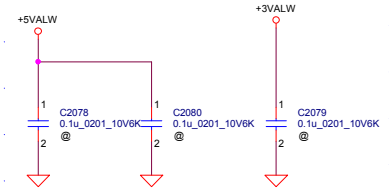
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

Need Short

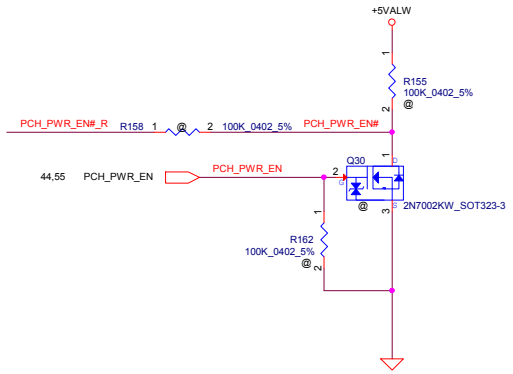


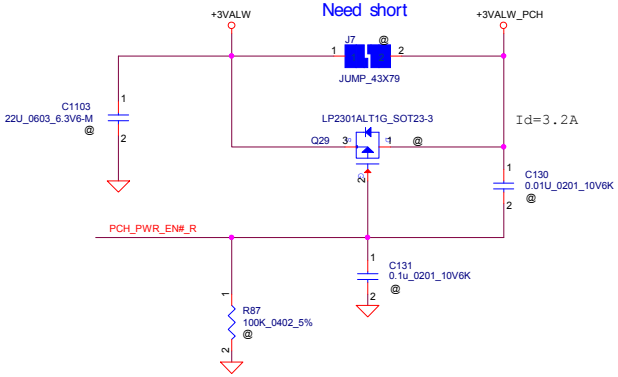
Need Short

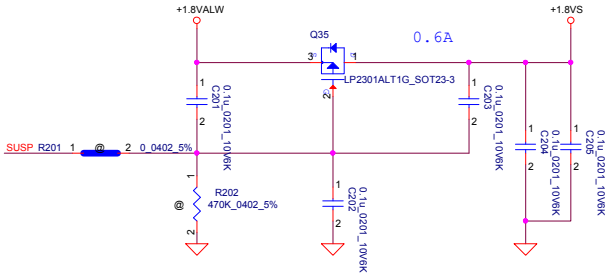
Change the main source to SA000067600 (GMT) 7/16



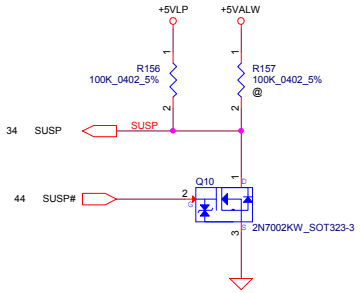
EMC



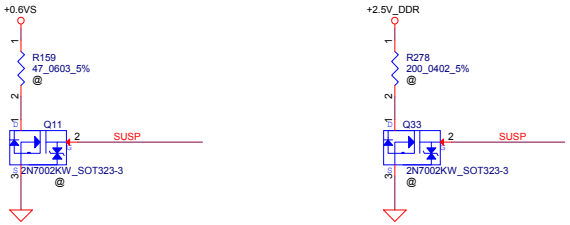




8/29 Add +1.8VS Circuit for Audio wei



For DisCharge



08/29: Need double check enable signal and the resistance

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Title: DC V TO VS INTERFACE

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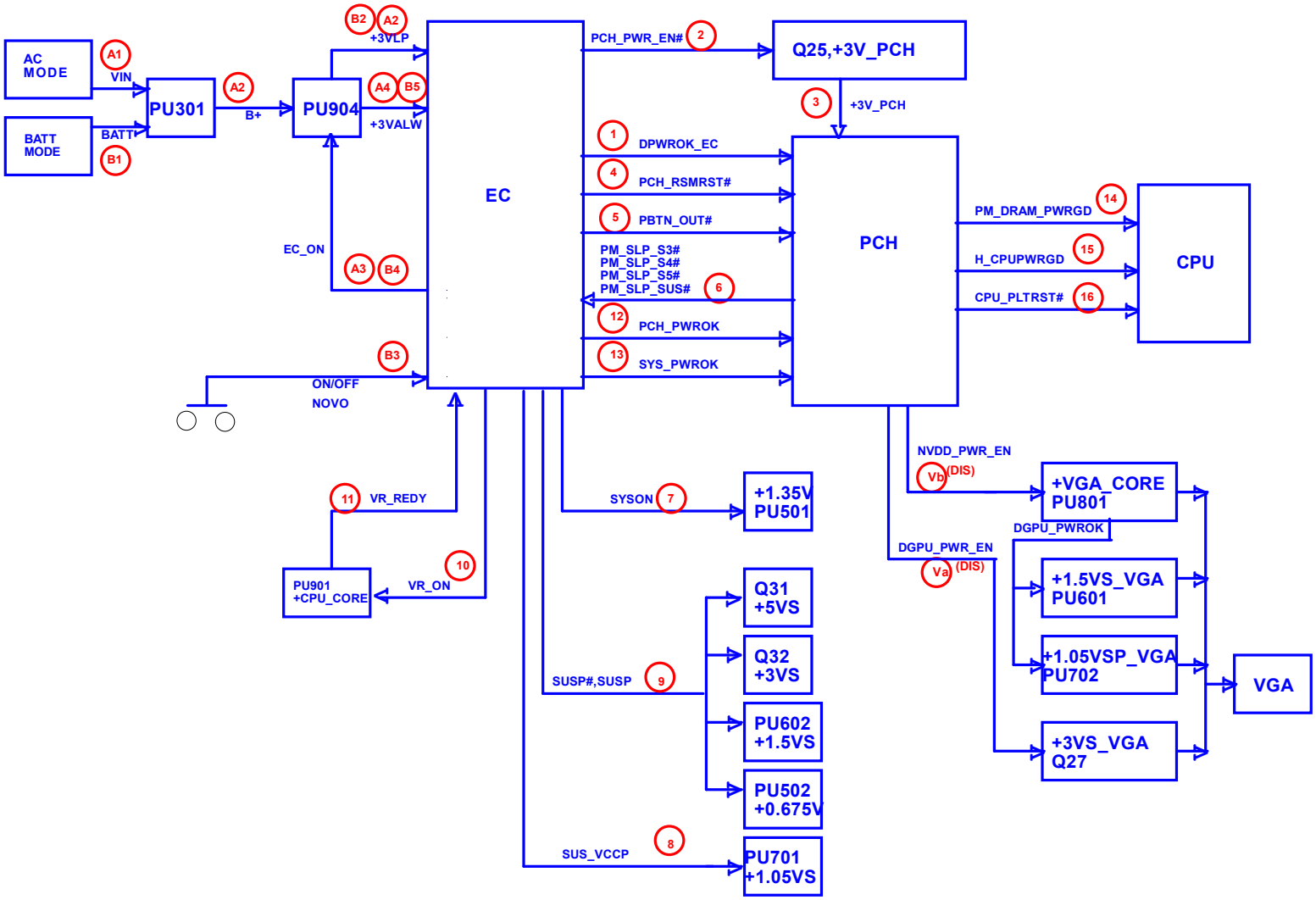

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title: **Power sequence block**

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Title: ***Virtual symbol***

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CPU Thermal Holex3

H1 HOLEA — pad_c6p0d4p0
H2 HOLEA — pad_c6p0d4p0
H3 HOLEA — pad_c6p0d4p0

GPU Thermal Holex2

H4 HOLEA — pad_c7p0d3p3
H5 HOLEA — pad_c7p0d3p3

Close to RJ45

H6 HOLEA — CHASSIS1_GND, pad_ct7p0b8p0d3p0

Close to Audio jack

H7 HOLEA — pad_ct7p0b8p0d3p0

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

DC-IN x2

H10 HOLEA — pad_ct5p5d2p5

WLAN Standoff

H11 HOLEA — pad_ct7p0b6p0d3p3
H12 HOLEA — pad_ct7p0d3p0
H13 HOLEA — pad_ct7p0d3p0
H15 HOLEA — pad_ct5p0d2p5
H16 HOLEA — pad_cb5p5d2p5

H17 HOLEA — pad_o2p6x2p9d2p6x2p9n
H18 HOLEA — PAD_CT7P0D3P0
H19 HOLEA — PAD_CT7P0D3P0
H20 HOLEA — pad_c3p3d3p3n

USB3.0 Shielding

SH1 ME@ — SPRING_FINGER_6.2X1.64
SH2 ME@ — SPRING_FINGER_6.2X1.64
SH3 ME@ — SPRING_FINGER_6.2X1.64
SH4 ME@ — SPRING_FINGER_6.2X1.64
SH5 ME@ — SPRING_FINGER_6.2X1.64
SH6 ME@ — SPRING_FINGER_6.2X1.64

DDR4 Shielding

SH12 ME@ — SPRING_FINGER_6.2X1.64
SH7 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH8 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 ME@ — SPRING_FINGER_6.2X1.64
SH9 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

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Title: **Hole**

Size	Document Number	Rev
B	DG421	1.0

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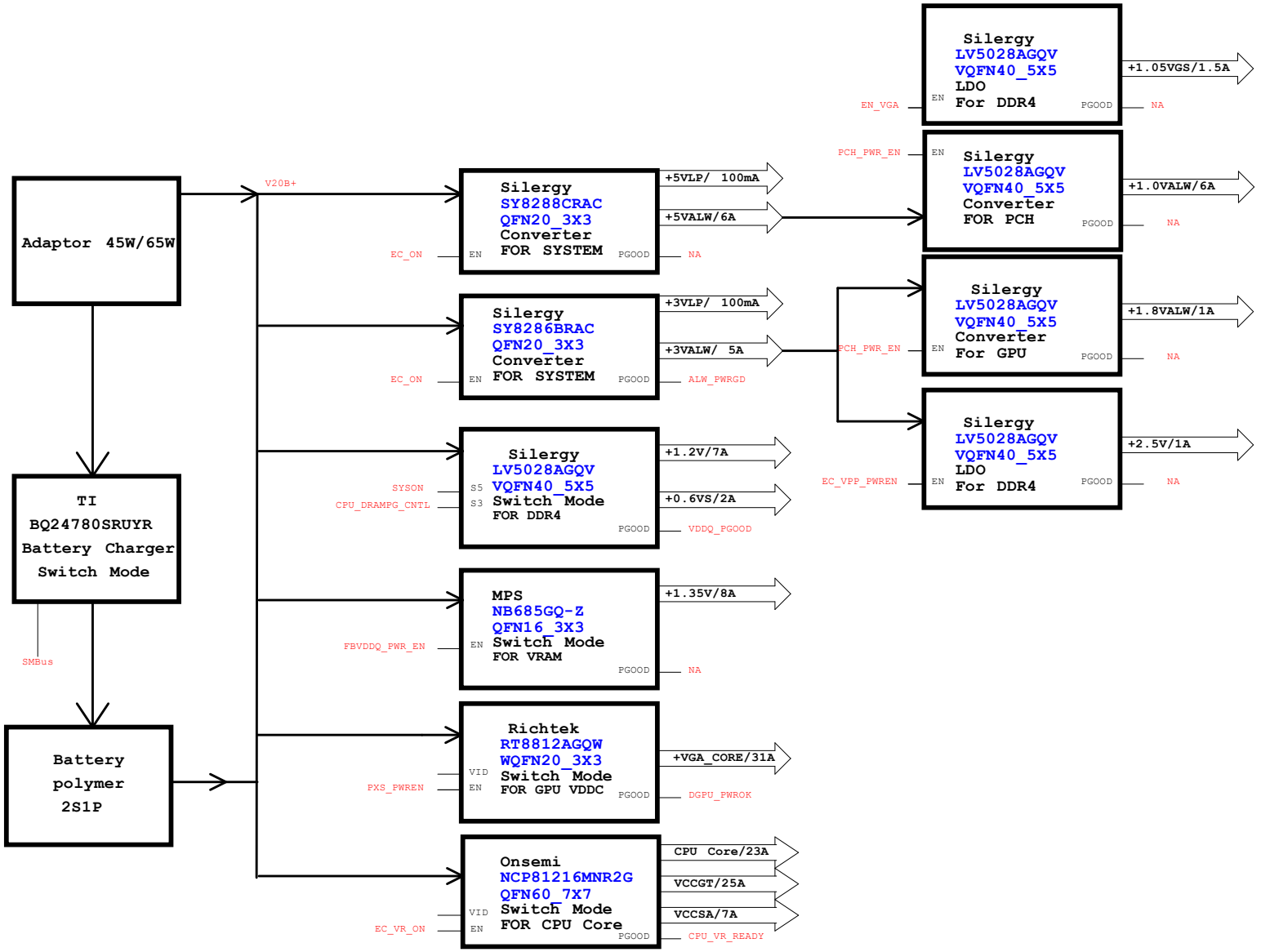

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Title: **PWR-Power Diagram**

Size	Document Number	Rev
Custom	DG421	1.0

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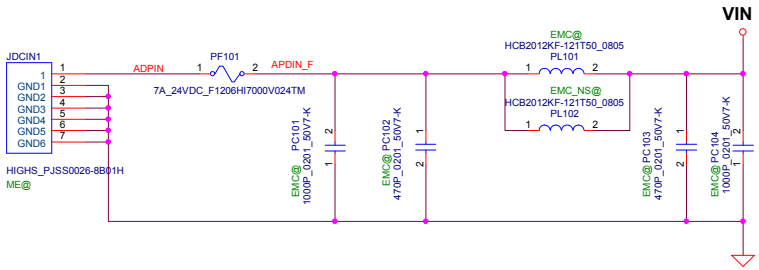

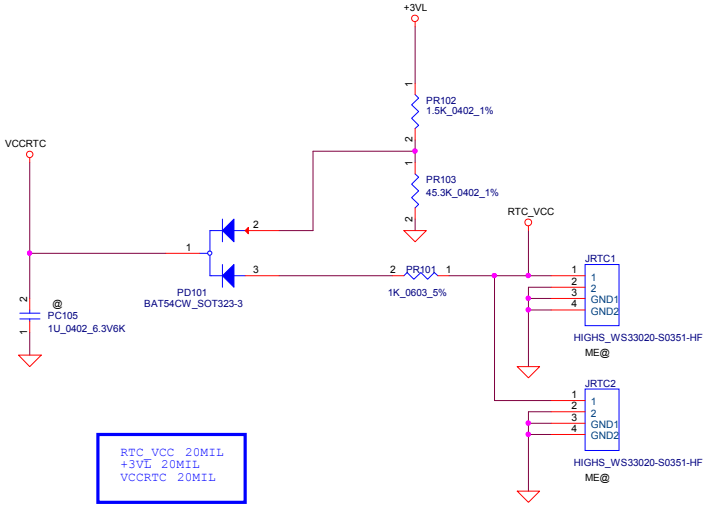

RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

No charge RTC with 35mm cable

RTC Battery for GCM BOM
(2nd source and quoted price)

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Title: ***PWR-DCIN / RTC charger***

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Custom	***DG421***	1.0

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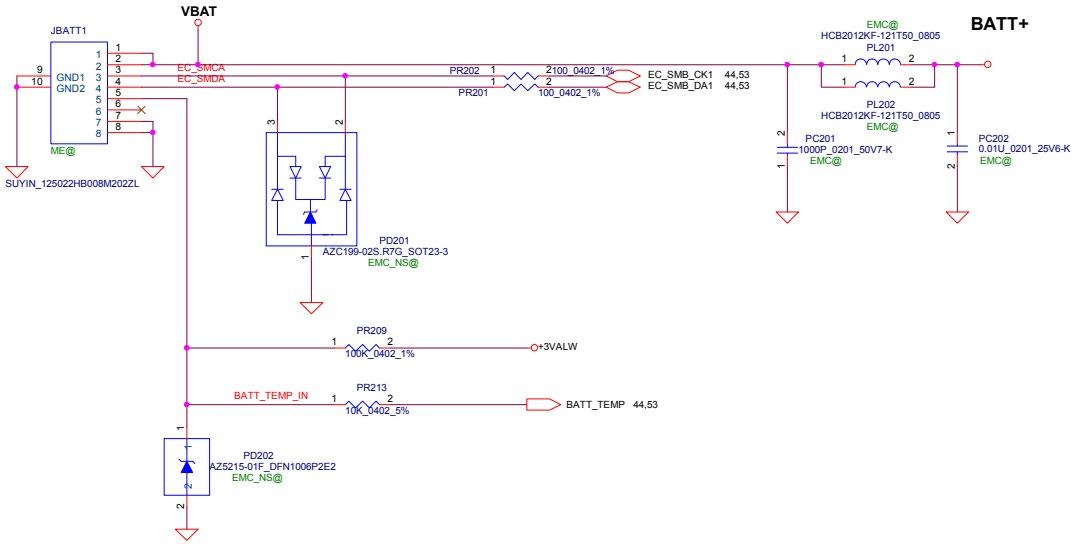

2S1P polymer battery voltage level: +6V ~ 8.4 V

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Title: PWR-BATTERY CONN/OTP

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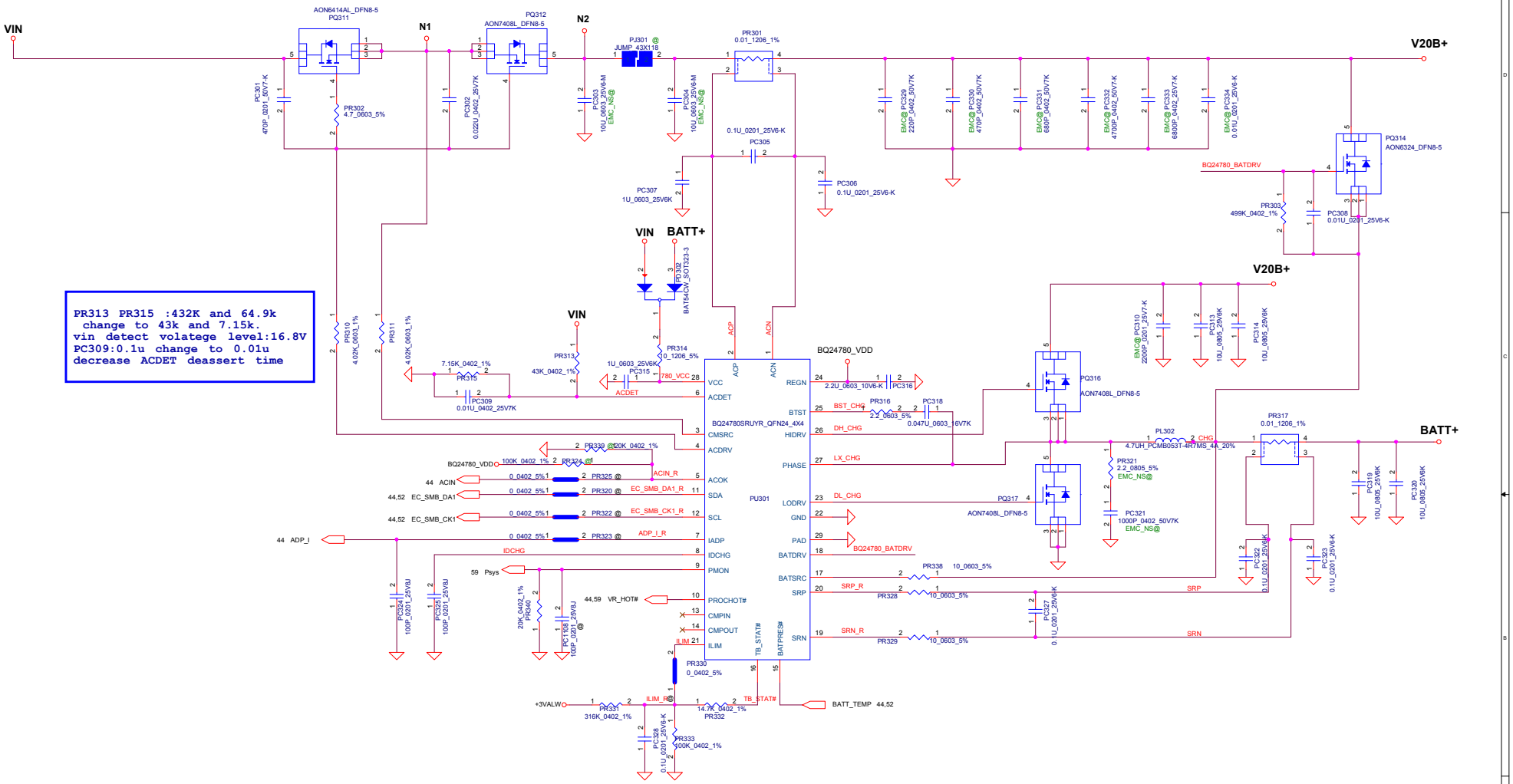

PR313 PR315 :432K and 64.9k
change to 43k and 7.15k.
vin detect volatege level:16.8V
PC309:0.1u change to 0.01u
decrease ACDET deassert time

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Title: PWR-CHARGER

Size	Document Number	Rev
C	DG421	1.0

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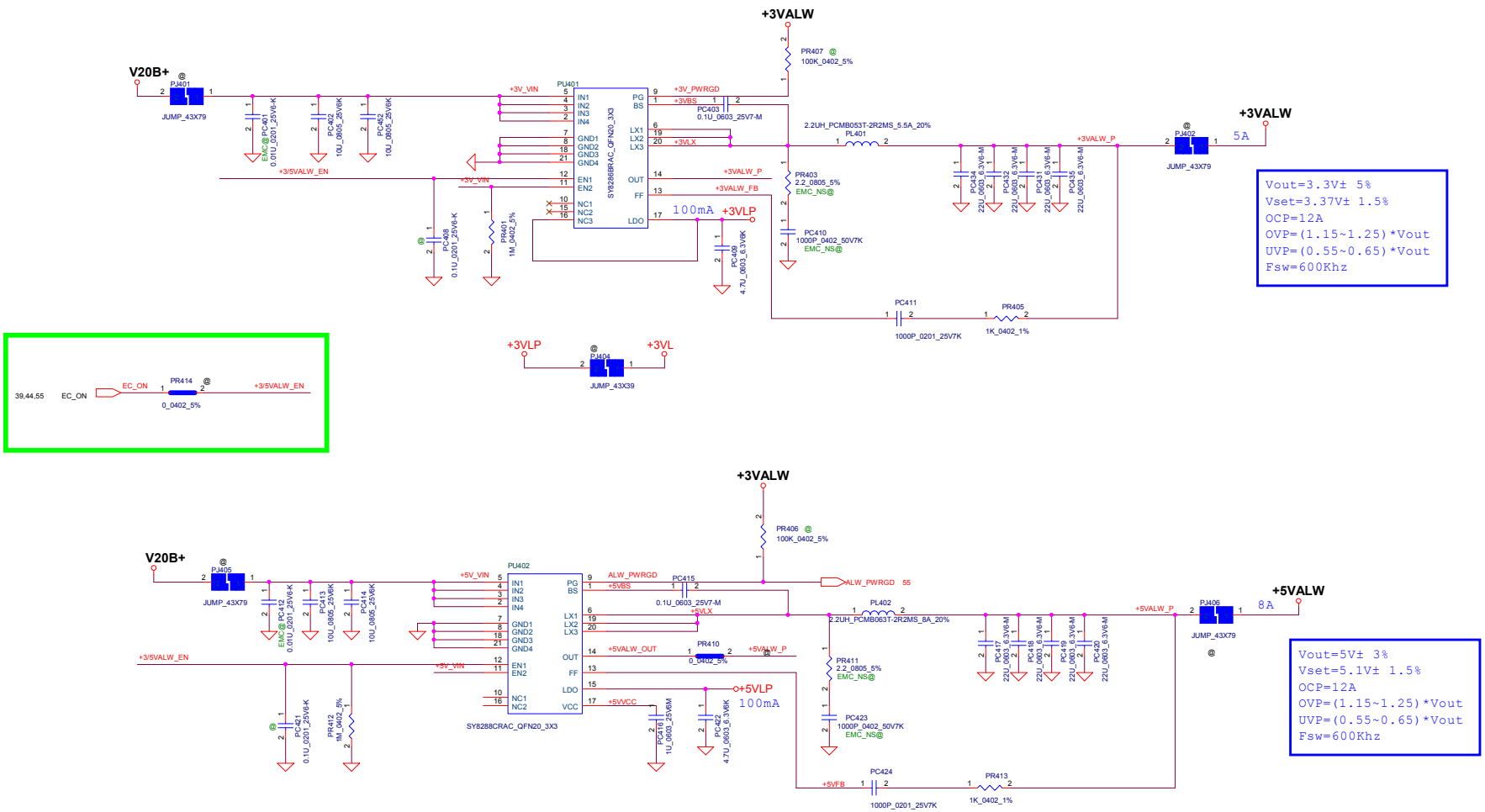

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Title: PWR_3VALW/5VALW

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C	DG421	1.0

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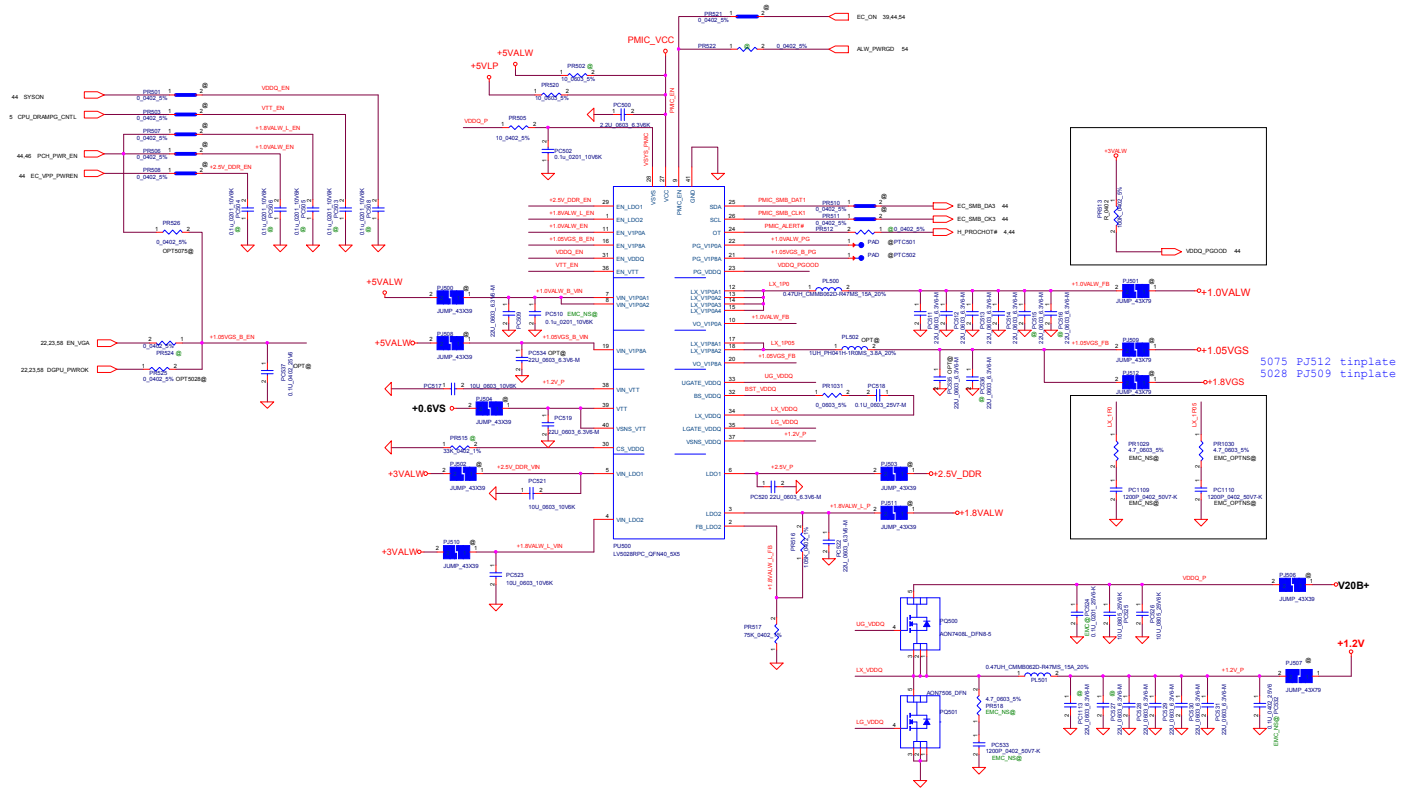

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Title: PWR PMIC-DDR4/1.0ALW/1.8ALW

Size	Document Number	Rev
D	DG421	1.0

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Title

PWR

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Custom	DG421	1.0

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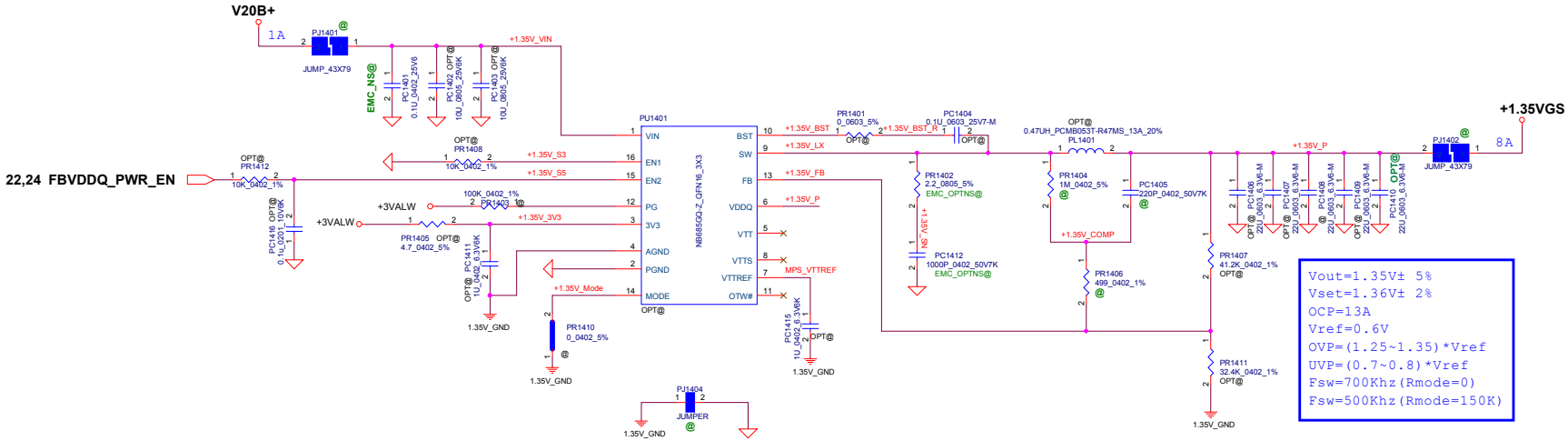

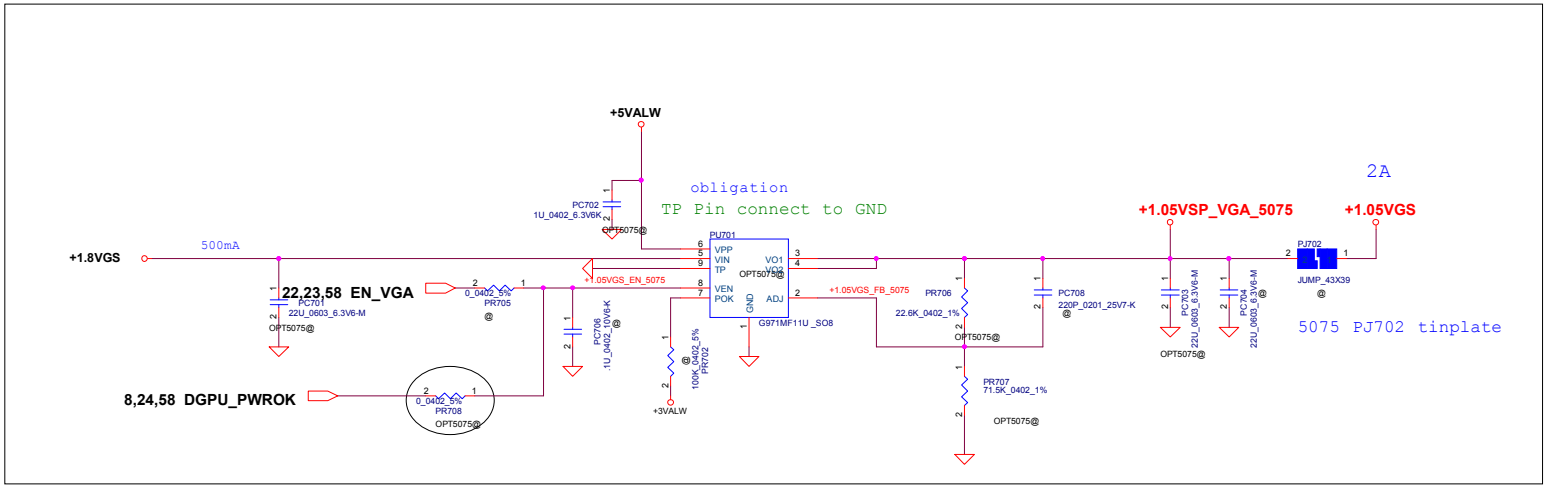

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Title: PWR-+1.05VGS/+1.35V_VR

Size	Document Number	Rev
C	DG421	1.0

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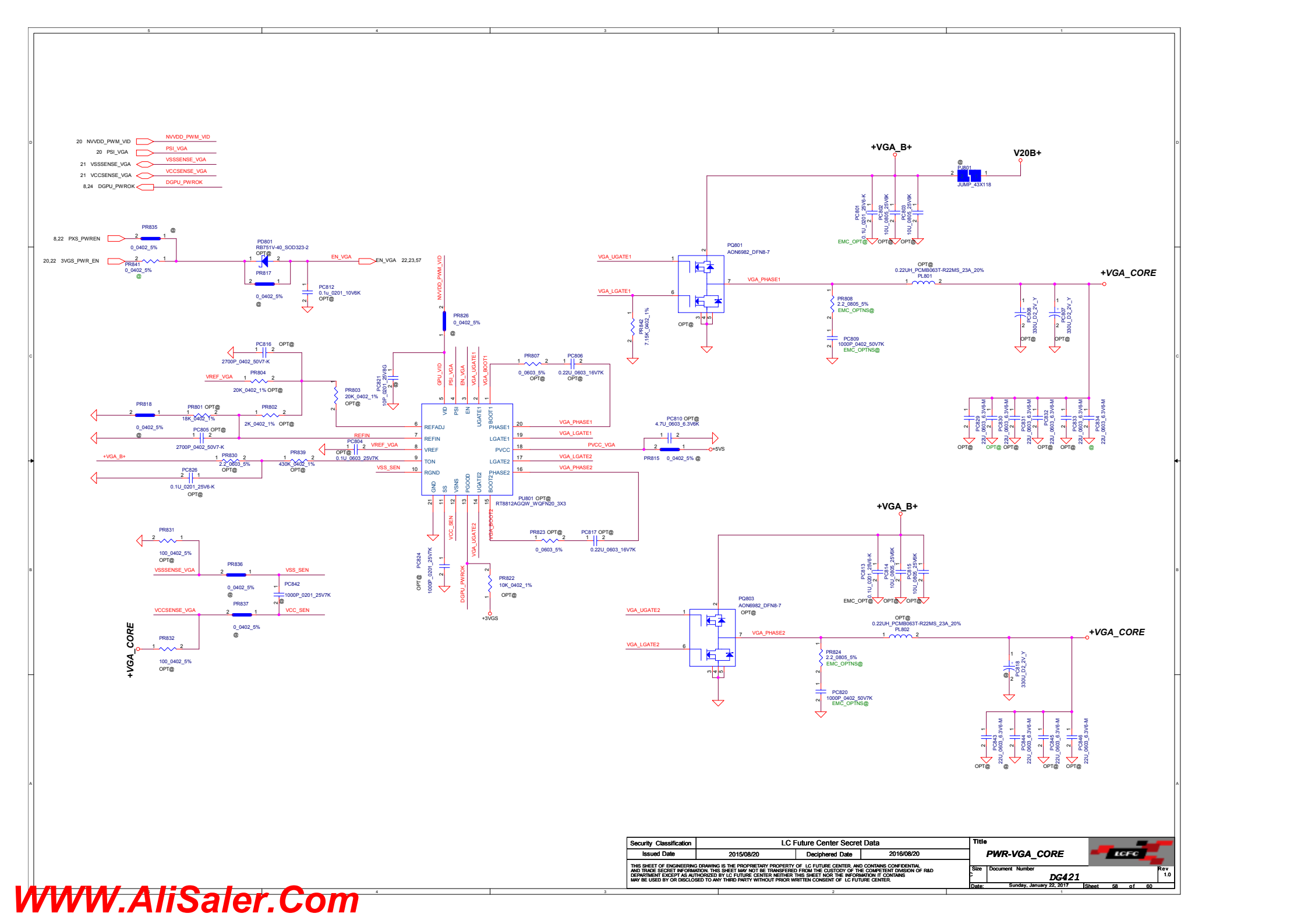

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Title	PWR-VGA_CORE	
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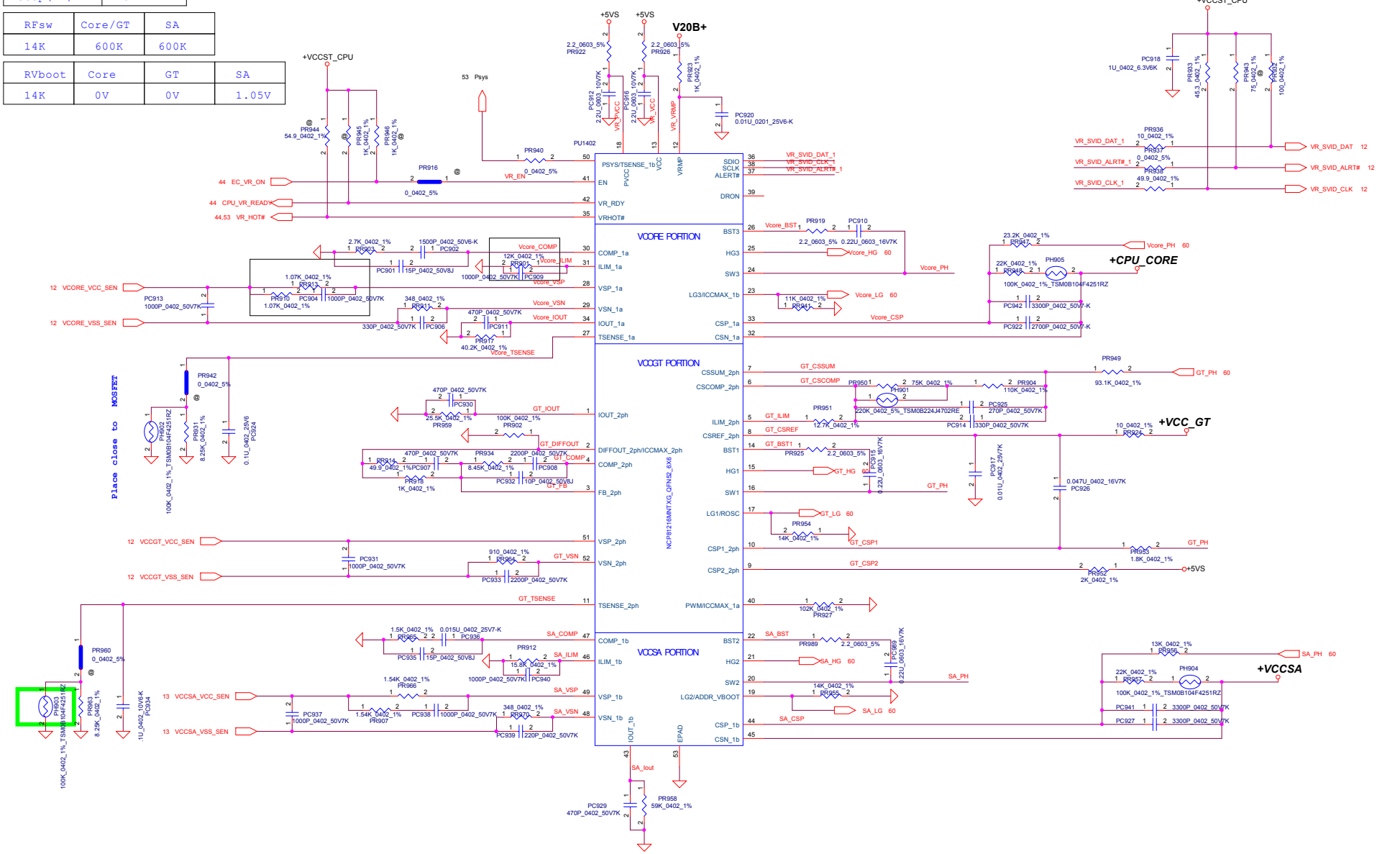
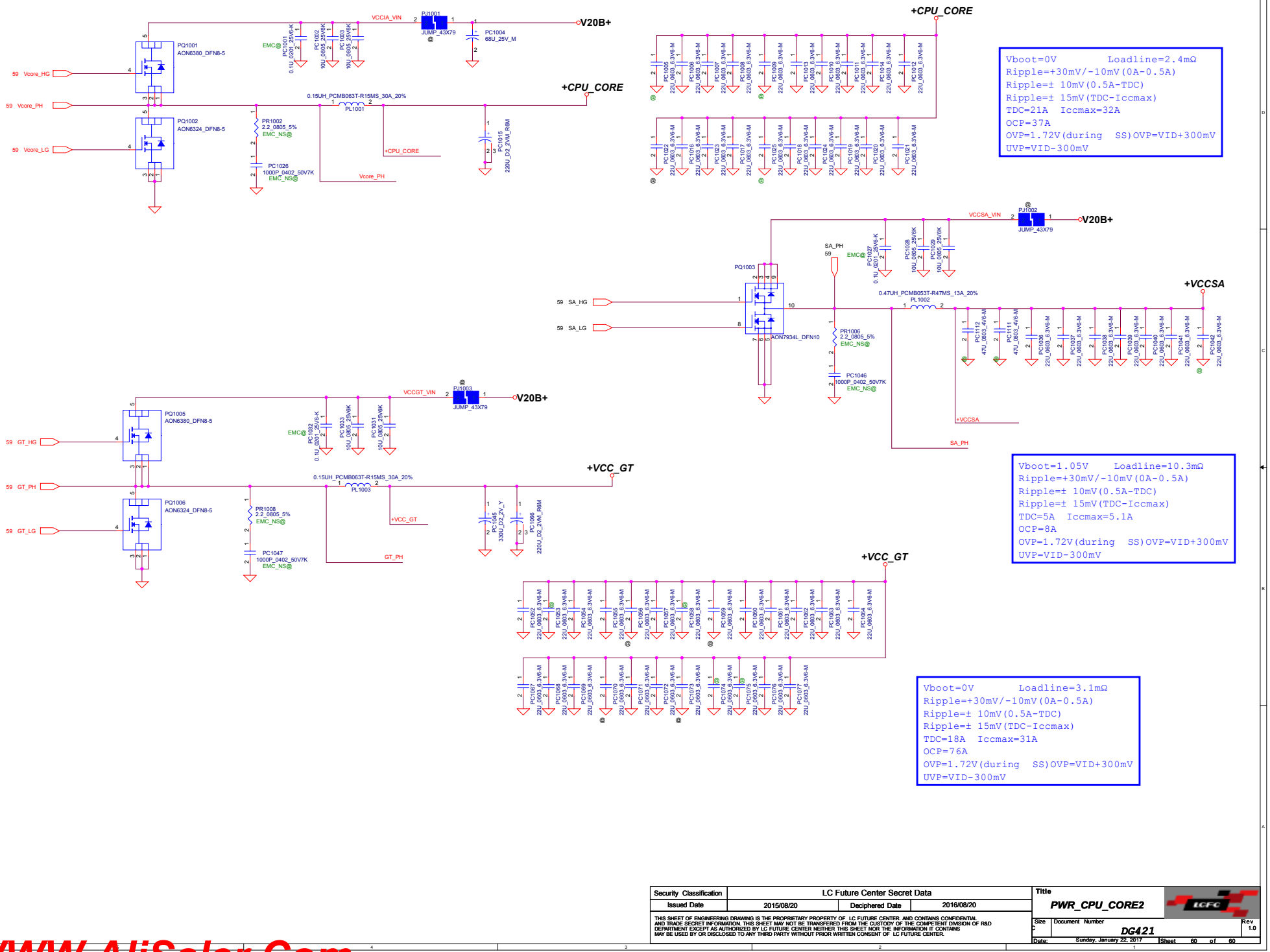
SVID Specification	
	Config
Vmin(V)	0
Vmax(V)	1.52
Vstep(mV)	5

RFsw	Core/GT	SA
14K	600K	600K

RVboot	Core	GT	SA
14K	0V	0V	1.05V





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Title	PWR_CPU_CORE2		
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