

# Compal Confidential

DIUYA/YB/SA/SB/SD (KBL-R)

DIS M/B Schematics Document

Intel KabyLake U/KabyLake R Processor with DDR4

N16S-GTR(940) (23x23mm)  
N16V-GMR1(920) (23x23mm)

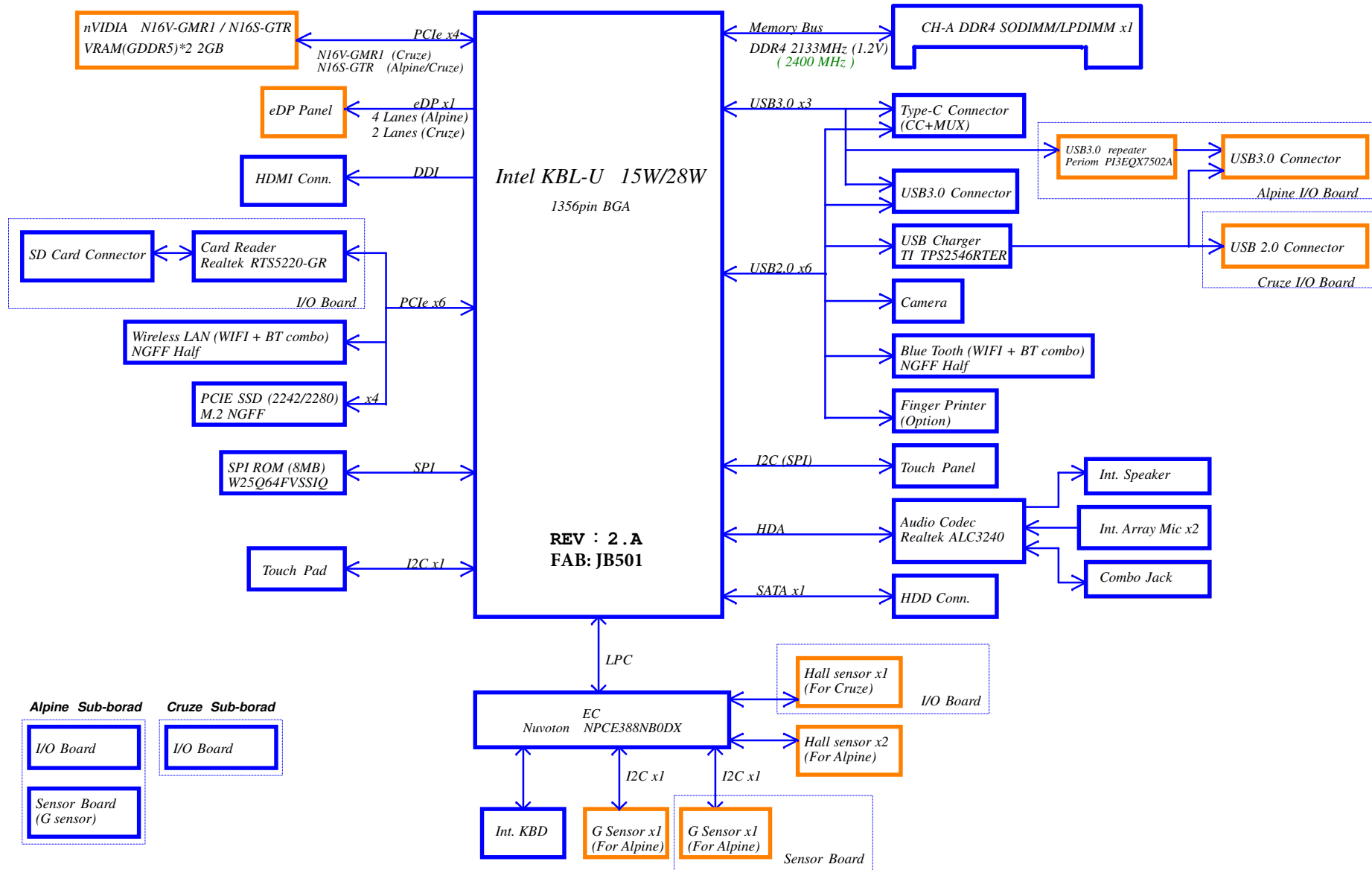
2017-06-05

LA-E541P

REV : 2.A

FAB: JB501

|   |                    |                 |            |                          |                          |
|---|--------------------|-----------------|------------|--------------------------|--------------------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                          |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 | Cover Page               |                          |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size                     | Document Number          |
|   |                    |                 |            | Custom                   | LA-E541P                 |
|   |                    |                 |            | Date:                    | Wednesday, June 21, 2017 |
|   |                    |                 |            | Sheet                    | 1 of 51                  |
|   |                    |                 |            | Rev                      | 2A                       |



## Voltage Rails

| power plane                    | B+ | +5VALW | +1.2V | +5VS<br>+3VS<br>+1.35VS<br>+VCC_CORE<br>+VGA_CORE<br>+VCC_GFXCORE_AXG |
|--------------------------------|----|--------|-------|---|
| State                          |    | +3VALW |       | +1.8VS<br>+0.6VS<br>+1.0VALW  |
| S0                             | O  | O      | O     | O   |
| S3                             | O  | O      | O     | X   |
| S5 S4/AC                       | O  | O      | X     | X   |
| S5 S4/ Battery only            | O  | X      | X     | X   |
| S5 S4/AC & Battery don't exist | X  | X      | X     | X   |

## BOM Structure Table

| Item                     | BOM Structure  |
|--------------------------|--|
| For DIS                  | DIS@   |
| For UMA                  | UMA@   |
| For Touch Panel with SPI | TS_SPI@  |
| For Touch Panel with I2C | TS_I2C@  |
| For Keyboard backlight   | KBL@   |
| No Keyboard backlight    | NOKBL@   |
| For Samsung VRAM         | S2G@   |
| For Micron VRAM          | M2G@   |
| For Hynix VRAM           | H2G@   |
| For UHD Panel            | UHD@   |
| For Finger Printer       | FP@  |
| For SSD                  | SSD@   |
| For EMI                  | EMI@   |
| For ESD                  | ESD@   |
| For RF                   | RF@  |
| No EMI                   | @EMI@  |
| No ESD                   | @ESD@  |
| No RF                    | @RF@   |
| Connector                | ME@  |
| For VARM X76             | X76@   |
| For Test Point           | TP@  |
| For Debug                | @DCI@  |
| For S series only        | S_AL@  |
| For S IMR series only    | S_IMR@   |
| For YOGA series only     | YOGA@  |
| For CPU Type             | 17_7500U_R1@<br>15_7200U_R1@<br>i3_7100U_R1@<br>17_7500U_R3@<br>15_7200U_R3@<br>i3_7100U_R3@<br>pt_4415U_R1@<br>pt_4415U_R3@<br>i3_6006U_R3@ |

## USB 2.0 Port Table

| Port | External USB Port       |
|------|-------------------------|
| 1    | USB3 Type-C Port        |
| 2    | USB2/3 Port (MB)        |
| 3    | USB2/3 Port (IO/B)      |
| 4    | USB3 Type-C Port        |
| 5    | Camera                  |
| 6    | Finger Printer (Option) |
| 7    | NGFF WLAN+BT            |

## USB 3.0 Port Table

| Port | External USB Port  |
|------|--------------------|
| 1    | USB3 Type-C (MUX)  |
| 2    | USB2/3 Port (MB)   |
| 3    | USB2/3 Port (IO/B) |
| 4    |                    |
| 5    |                    |
| 6    |                    |

## SATA Port Table

| Port | External SATA Port |
|------|--------------------|
| 0    | HDD                |
| 1    |                    |

## PCIe Port Table

| Lane | Port | External PCIe Port |
|------|------|--------------------|
| 1    |      |                    |
| 2    |      |                    |
| 3    | 1    | GPU                |
| 4    |      |                    |
| 5    |      |                    |
| 6    |      | Card Reader        |
| 7    |      | NGFF WLAN+BT       |
| 8    |      |                    |
| 9    |      |                    |
| 10   |      |                    |
| 11   | 3    | SSD                |
| 12   |      |                    |

## EC SM Bus1 address EC SM Bus2 address EC SM Bus4 address

| Device        | Address       | Device  | Address       | Device  | Address       |
|---------------|---------------|---------|---------------|---------|---------------|
| Smart Battery | 0001 011x 16h | NC7718W | 1001 100x 98h | BMA250E | 0001 100x 18h |

## PCH SM Bus address

| Device               | Address       |
|----------------------|---------------|
| DDR_JDIMM1 Touch Pad | 1010 000x A0h |

## GPU SM Bus address

| Device                  | Address       |
|-------------------------|---------------|
| Internal thermal sensor | 1001 111x 9Eh |

## SMBUS Control Table

|             | SOURCE  | VGA | BATT   | CHARGER  | NECP388 | SODIMM | Thermal Sensor | DGPU |   |   | TP | PCH | G-SENSOR |
|-------------|---------|-----|--------|----------|---------|--------|----------------|------|---|---|----|-----|----------|
| SMB_EC_CK1  | NECP388 | X   | V      | V        | X       | X      | X              | X    | X | X | X  | X   | X        |
| SMB_EC_DA1  | +3VALW  |     | +3VALW | +19V_VIN |         |        |                |      |   |   |    |     |          |
| SMB_EC_CK2  | NECP388 | X   | X      | X        | X       | X      | X              | X    | X | X | X  | X   | X        |
| SMB_EC_DA2  | +3VGS   |     |        |          |         |        |                |      |   |   |    |     |          |
| SMB_EC_CK4  | NECP388 | X   | X      | X        | X       | X      | X              | X    | X | X | X  | X   | X        |
| SMB_EC_DA4  | +3VALW  |     |        |          |         |        |                |      |   |   |    |     |          |
| PCH_SMBCLK  | PCH     | X   | X      | X        | X       | X      | X              | X    | X | X | X  | X   | X        |
| PCH_SMBDATA | +3VALW  |     |        |          |         |        |                |      |   |   |    |     |          |
| SML0CLK     | PCH     | X   | X      | X        | X       | X      | X              | X    | X | X | X  | X   | X        |
| SML0DATA    | +3VALW  |     |        |          |         |        |                |      |   |   |    |     |          |
| SML1CLK     | PCH     | X   | X      | X        | X       | X      | X              | X    | X | X | X  | X   | X        |
| SML1DATA    | +3VALW  |     |        |          |         |        |                |      |   |   |    |     |          |

| STATE                 | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS | Clock |
|-----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON               | HIGH   | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | ON    |
| S1 (Power On Suspend) | LOW    | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | LOW   |
| S3 (Suspend to RAM)   | LOW    | LOW     | HIGH    | HIGH    | HIGH    | ON    | ON  | OFF | OFF   |
| S4 (Suspend to Disk)  | LOW    | LOW     | LOW     | HIGH    | HIGH    | ON    | OFF | OFF | OFF   |
| S5 (Soft OFF)         | LOW    | LOW     | LOW     | LOW     | LOW     | ON    | OFF | OFF | OFF   |

## X4E

## Yoga Series

|                             |                                    |                                     |  |
|-----------------------------|------------------------------------|-------------------------------------|--|
| ZZZ4 X4E_YA@                | ZZZ3 X4E_YA_FP@                    | ZZZ5 X4E_YB@                        | ZZZ6 X4E_YB_FP@                        |
| X4E Y Series<br>X4EASR3BLA1 | X4E Y Series FP SKU<br>X4EASR3BLA2 | X4E Y Series UHD SKU<br>X4EASR3BLA2 | X4E Y Series UHD+FP SKU<br>X4EASR3BLA1 |

## Yoga Series (U42)

|                             |                                    |                                     |  |
|-----------------------------|------------------------------------|-------------------------------------|--|
| ZZZ X4E_U42_YA@             | ZZZ X4E_U42_YA_FP@                 | ZZZ1 X4E_U42_YB@                    | ZZZ2 X4E_U42_YB_FP@                    |
| X4E Y Series<br>X4EASR3BLA2 | X4E Y Series FP SKU<br>X4EASR3BLA1 | X4E Y Series UHD SKU<br>X4EASR3BLA2 | X4E Y Series UHD+FP SKU<br>X4EASR3BLA1 |

## GDDR5 VRAM \* 2

## X7671138L03

|  |  |
|--|--|
| U6 S2G@                                      | U7 S2G@                                      |
| K4G80325FB-HC03<br>SA000094R20               | K4G80325FB-HC03<br>SA000094R20               |
| RV65<br>SDQ344991B0<br>1.99K_0402_1%<br>S2G@ | RV65<br>SDQ344991B0<br>1.99K_0402_1%<br>S2G@ |

## X7671138L02

|  |  |
|--|--|
| U6 M2G@                                      | U7 M2G@                                      |
| MT51J256M32HF<br>SA000096R20                 | MT51J256M32HF<br>SA000096R20                 |
| RV65<br>SDQ344991B0<br>1.99K_0402_1%<br>M2G@ | RV65<br>SDQ344991B0<br>1.99K_0402_1%<br>M2G@ |

## X7671138L01

|  |  |
|--|--|
| U6 H2G@                                      | U7 H2G@                                      |
| H5GCBH24MJR-T2C<br>SA000092G10               | H5GCBH24MJR-T2C<br>SA000092G10               |
| RV65<br>SDQ344991B0<br>1.99K_0402_1%<br>H2G@ | RV65<br>SDQ344991B0<br>1.99K_0402_1%<br>H2G@ |

## HDMI Logo

|                          |
|--------------------------|
| ZZZ 45@                  |
| HDMI Logo<br>RC0000003HM |

## PCB part

|                             |
|-----------------------------|
| ZZZ YOGA@                   |
| PCB Y Series<br>DA800195G2A |
| ZZZ S_AL@                   |
| PCB S Series<br>DA800195G2A |
| ZZZ S_IMR@                  |
| PCB S Series<br>DA800195G2A |

## GPU part

|                                       |  |
|---------------------------------------|--|
| U1 N16S_R1@                           | U1 N16V_R1@                            |
| N16S-GTR-S-A2 BGA 595P<br>SA000097P00 | N16V-GMR1-S-A2 BGA 595P<br>SA000097P00 |
| U1 N16S_R3@                           | U1 N16V_R3@                            |
| N16S-GTR-S-A2 BGA 595P<br>SA000097P00 | N16V-GMR1-S-A2 BGA 595P<br>SA000097P00 |

## CPU part

## KBL U22 (= U22@)

|                              |                              |                              |                              |
|------------------------------|------------------------------|------------------------------|------------------------------|
| U1 i3_7100U_R1@              | U1 i5_7200U_R1@              | U1 i7_7500U_R1@              | U1 i7_4415U_R1@              |
| QLYKH H0 2.4G<br>SA0000A3B80 | QLYYH H0 2.5G<br>SA0000A3B80 | QLYYH H0 2.7G<br>SA0000A3B80 | QLYYH H0 2.9G<br>SA0000A3B80 |
| U1 i3_7100U_R3@              | U1 i5_7200U_R3@              | U1 i7_7500U_R3@              | U1 i7_4415U_R3@              |
| SR343 H0 2.4G<br>SA0000A3B80 | SR342 H0 2.5G<br>SA0000A3B80 | SR341 H0 2.7G<br>SA0000A3B80 | SR348 H0 2.9G<br>SA0000A3B80 |

## SKL U22 (= U22@)

|  |
|--|
| U1 i3_6006U_R3@                            |
| SR2JG R1 i3-6006U 2.0G C381<br>SA0000ACN10 |

## KBL U42 (= U42@)

|                                    |                                    |
|------------------------------------|------------------------------------|
| U1 i5_QNFB_R1@                     | U1 i7_QNFB_R1@                     |
| QNEFY Y0 1.6G FCBGA<br>SA0000AWB00 | QNEFY Y0 1.6G FCBGA<br>SA0000AWC00 |
| U1 i5_QNFB_R3@                     | U1 i7_QNFB_R3@                     |
| QNEFY Y0 1.6G FCBGA<br>SA0000AWB50 | QNEFY Y0 1.6G FCBGA<br>SA0000AWC50 |

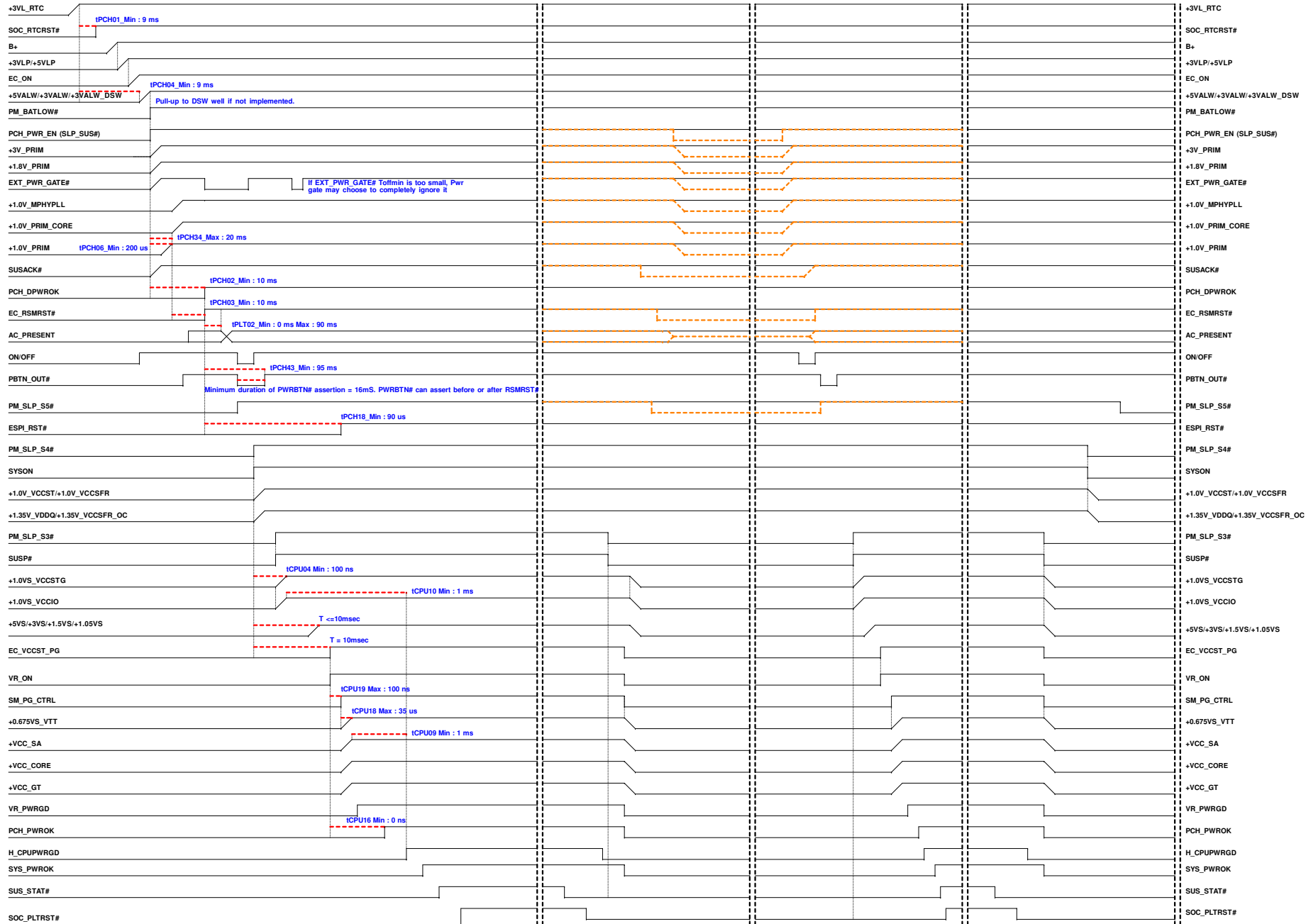


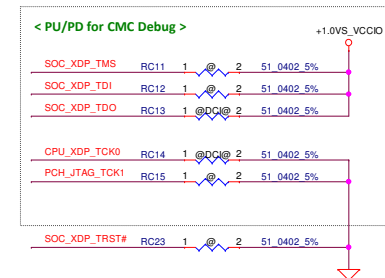
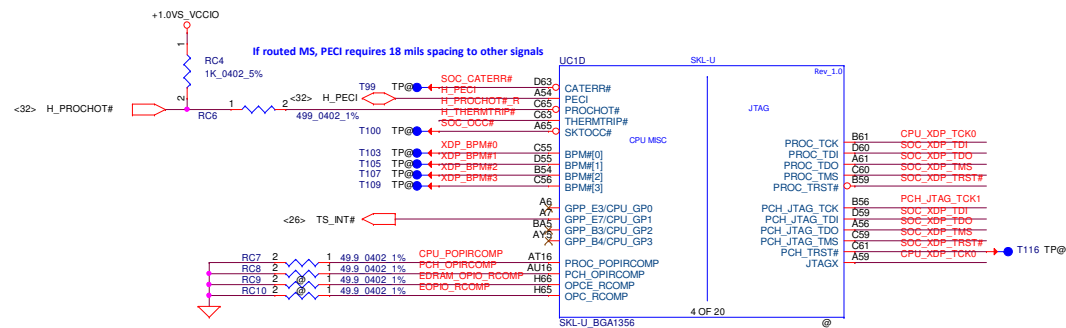
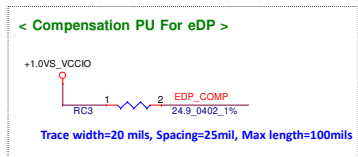
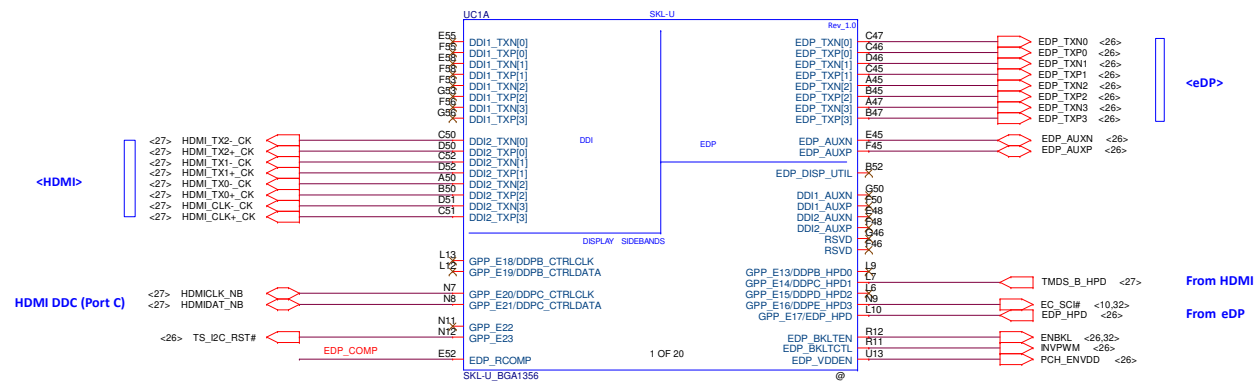
## G3-&gt;S0

## S0-&gt;S3/DS3

## S0/DS3-&gt;S0

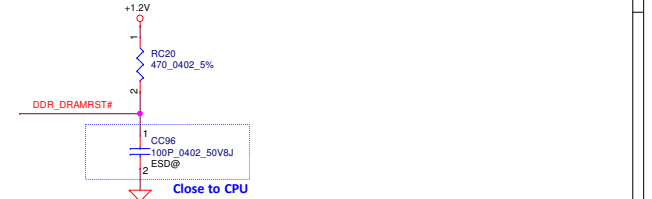
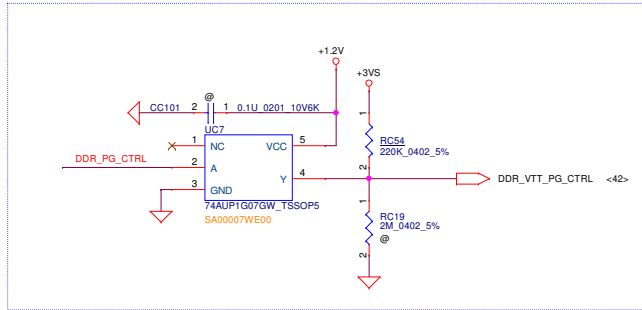
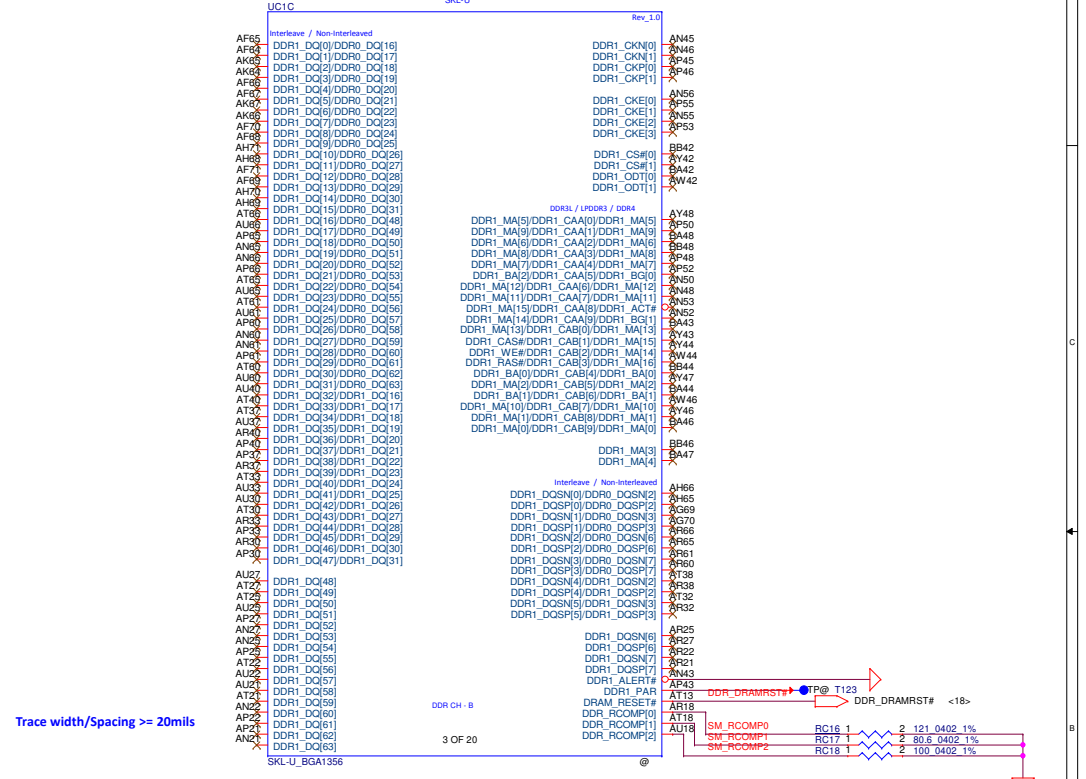
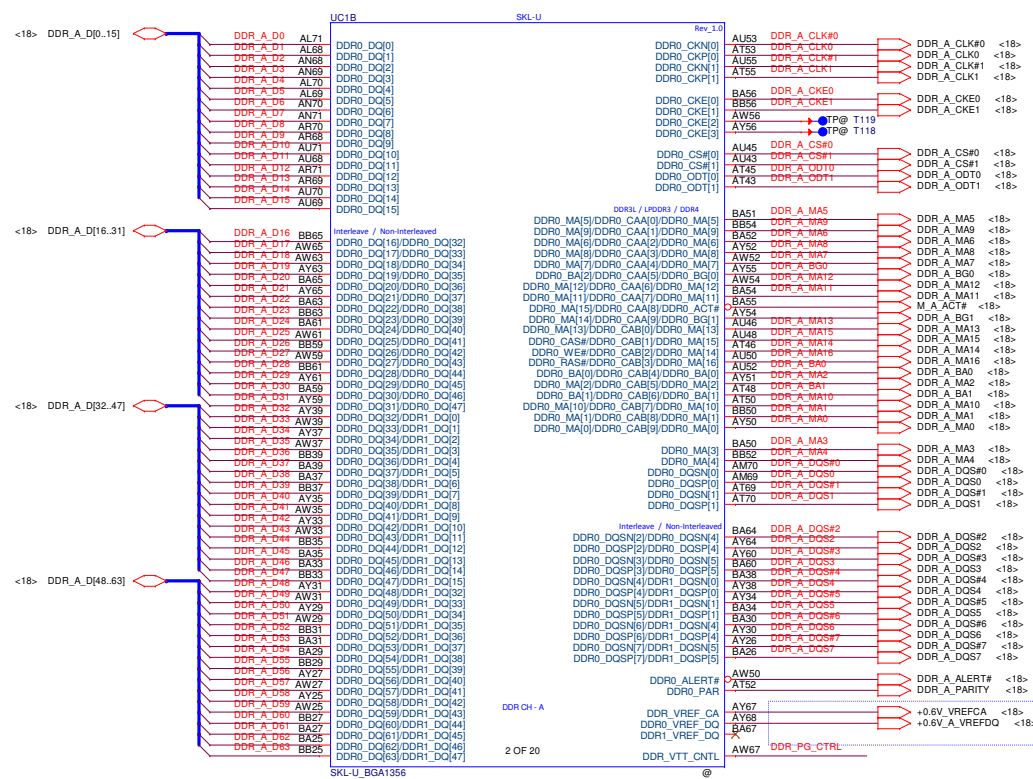
## S0-&gt;S5



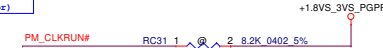
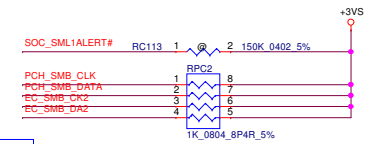
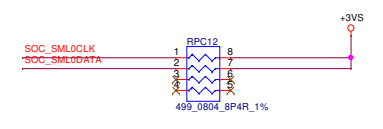
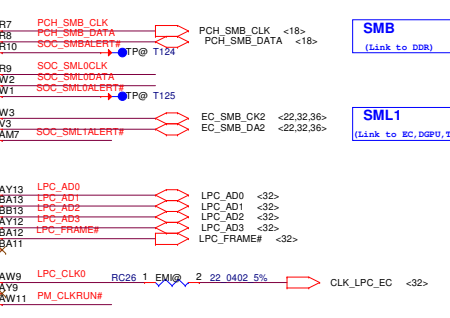
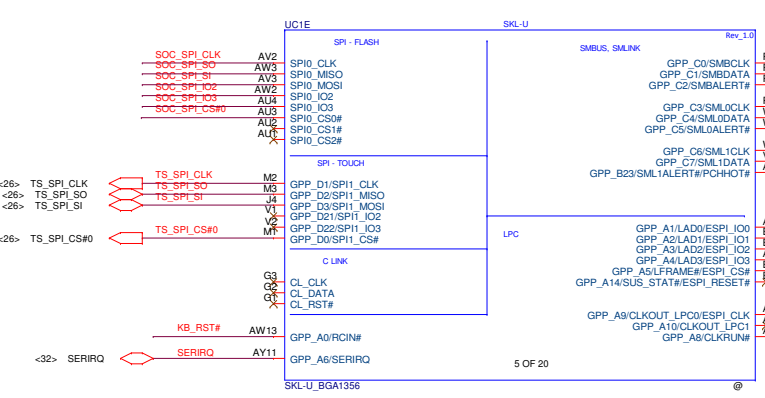
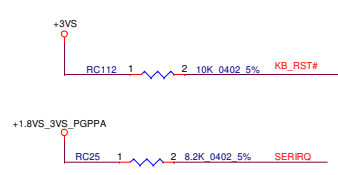
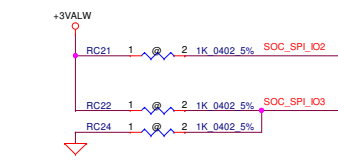


|  |                    |                 |            |                                 |                                    |           |
|--|--------------------|-----------------|------------|---------------------------------|------------------------------------|-----------|
| Security Classification  | Compal Secret Data |                 |            | <b>Compal Electronics, Inc.</b> |                                    |           |
| Issued Date  | 2017/06/05         | Deciphered Date | 2018/06/05 | Title                           | <b>SKL-U(1/12)DDI,EDP,MISC,CMC</b> |           |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size                            | Document Number                    | Rev<br>2A |
|  |                    |                 |            | Custm                           | <b>LA-E541P</b>                    |           |
| Date: Wednesday, June 21, 2017   |                    |                 |            | Sheet                           | 6                                  | of 51     |

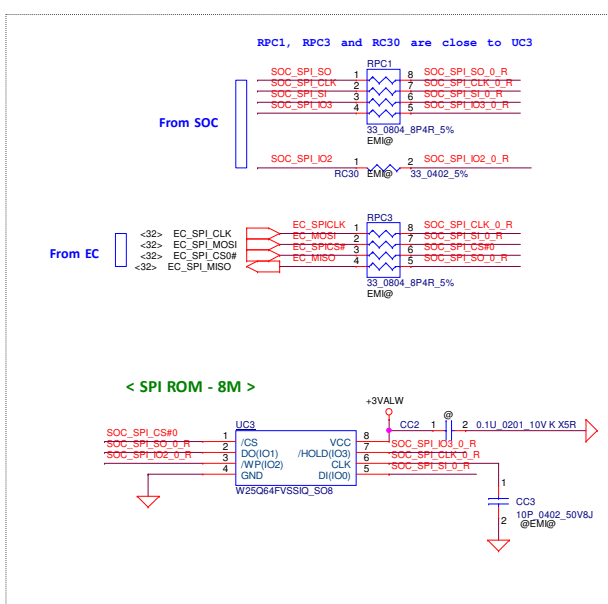
# Interleaved Memory



| Security Classification   |            | Compal Secret Data |            | Title            |        |
|---|------------|--------------------|------------|------------------|--------|
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | SKL-U(2/12)DDR3L |        |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            | Customer           |            | Size             | Rev 2A |
| Date: Wednesday, June 21, 2017  |            | Sheet 7 of 51      |            | LA-E541P         |        |

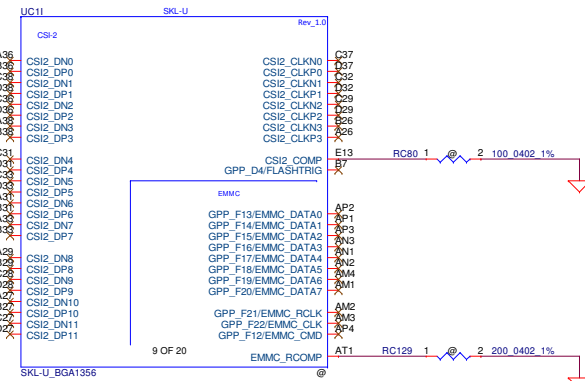
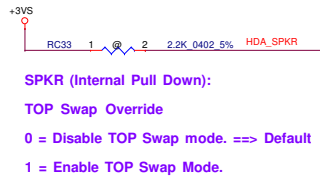
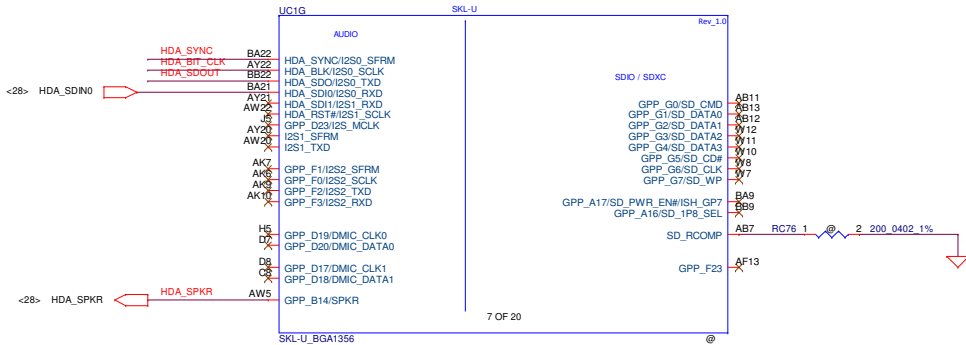
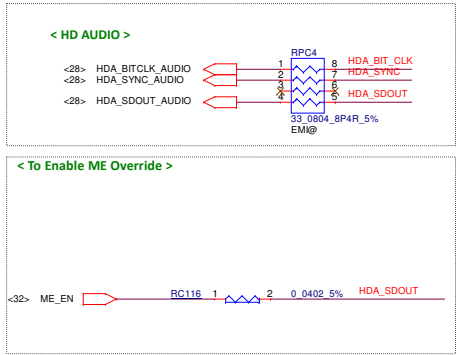


Follow 543016\_SKI\_U\_Y\_PDG\_0\_9

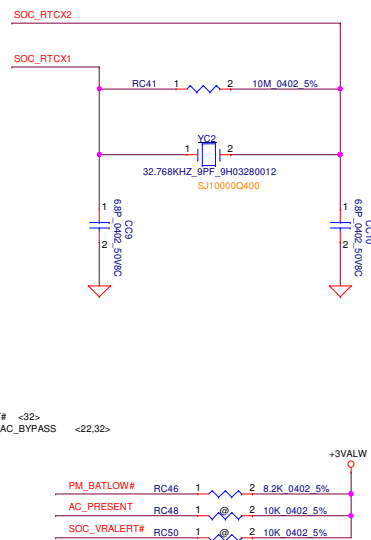
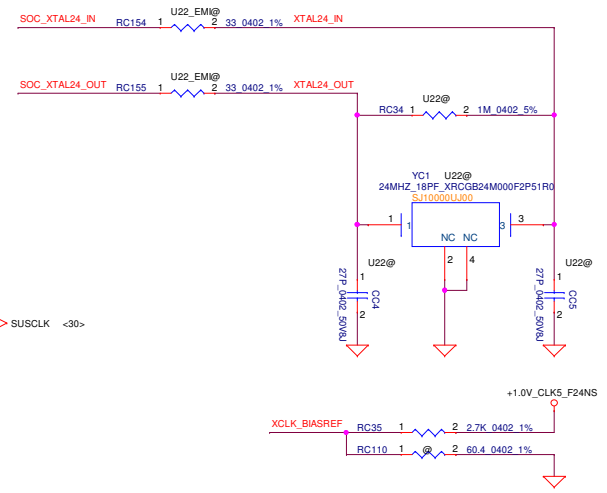
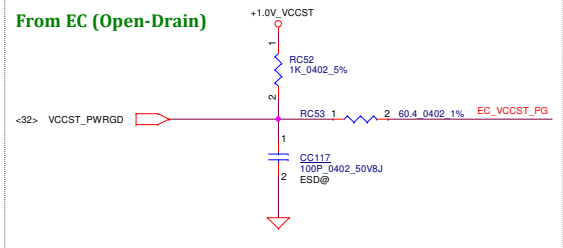
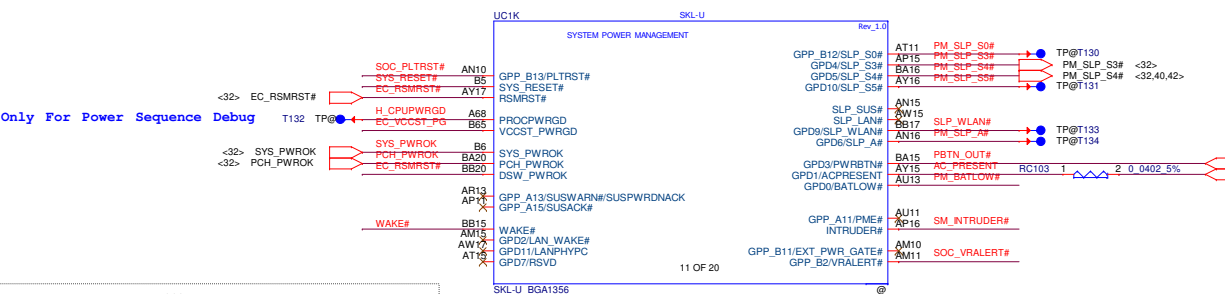
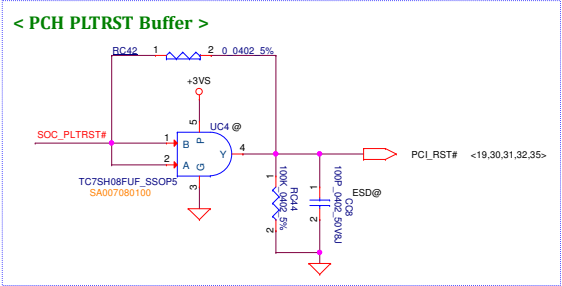
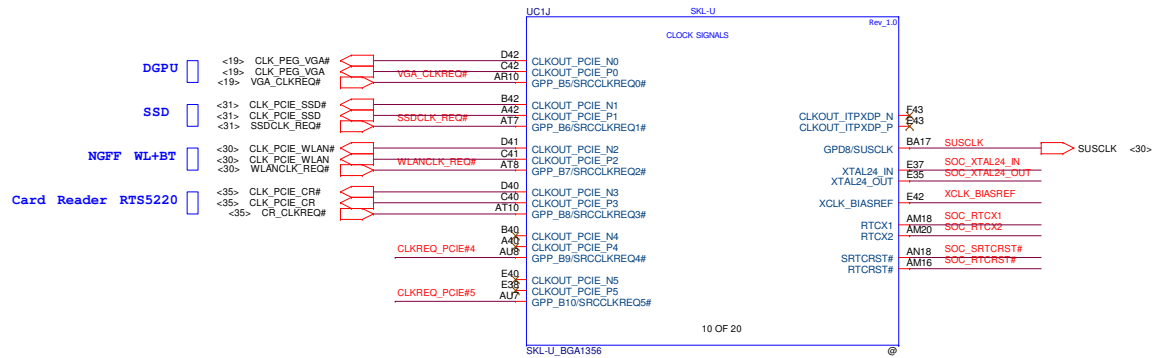
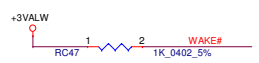
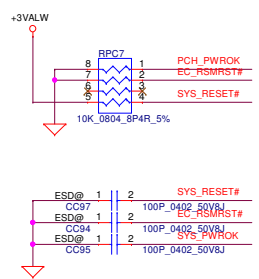
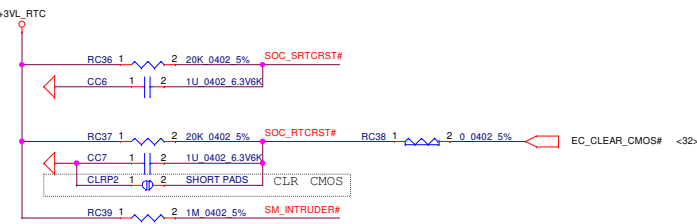
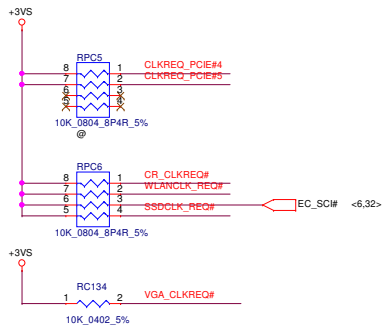


|   |                    |                 |            |                          |                             |
|---|--------------------|-----------------|------------|--------------------------|-----------------------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                             |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 | Title                    | SKL-U(3/12)SPI,SMB,LPC,ESPI |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size                     | Rev                         |
|   |                    |                 |            | Custom                   | 2A                          |
|   |                    |                 |            | Date:                    | Wednesday, June 21, 2017    |
|   |                    |                 |            | Sheet                    | 8 of 51                     |





|   |            |                    |            |                               |                          |
|---|------------|--------------------|------------|-------------------------------|--------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.      |                          |
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | Title                         |                          |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | SKL-U(4/12)HDA,EMMC,SDIO,CSI2 |                          |
|   |            |                    |            | Size                          | Rev                      |
|   |            |                    |            | Custom                        | 2A                       |
|   |            |                    |            | LA-E541P                      |                          |
|   |            |                    |            | Date:                         | Wednesday, June 21, 2017 |
|   |            |                    |            | Sheet                         | 9 of 51                  |



|   |            |                    |            |                       |                          |
|---|------------|--------------------|------------|-----------------------|--------------------------|
| Security Classification   |            | Compal Secret Data |            | Title                 |                          |
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | SKL-U(S12)CLK,PM,GPIO |                          |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | Size                  | Document Number          |
|   |            |                    |            | Custom                | LA-E541P                 |
|   |            |                    |            | Date                  | Wednesday, June 21, 2017 |
|   |            |                    |            | Sheet                 | 10 of 51                 |

GPIO\_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

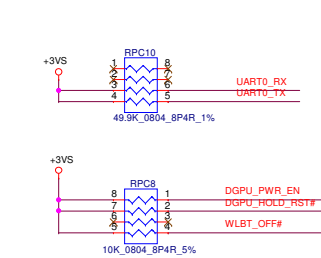
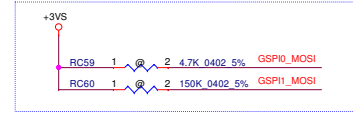
1 = Enable No Reboot Mode. (PCH will disable the TCO  
Timer system reboot feature). This function is used  
when running ITP/XDP.

GPIO11\_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

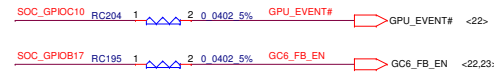
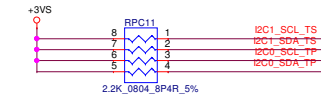
1 = LPC Mode



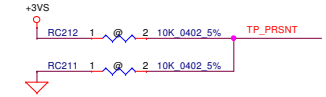
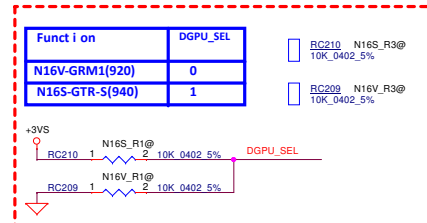
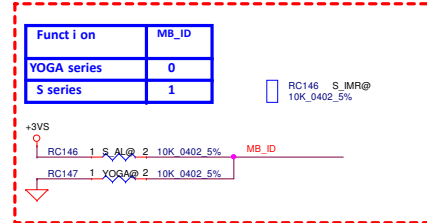
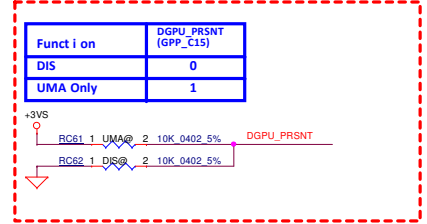
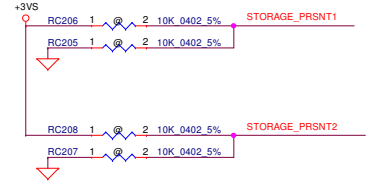
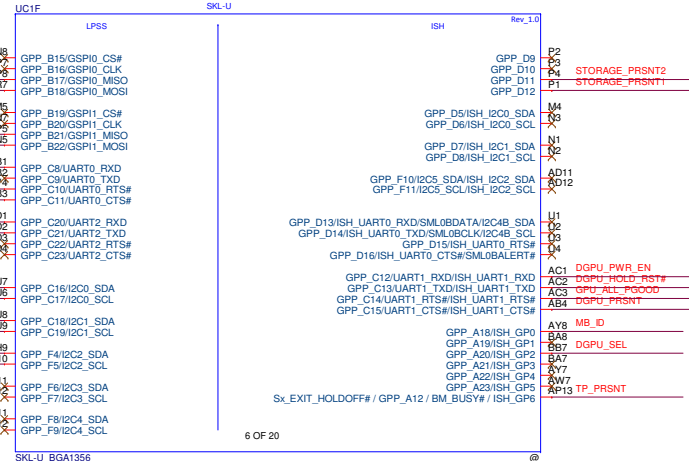
Touch PAD ☐

Touch Panel ☐

EC Sensor ☐



TO DGPU



dGPU

Card Reader

NGFF WLAN+BT

HDD

SSD

<19> PCIE\_PRX\_DTX\_N1  
<19> PCIE\_PRX\_DTX\_P1  
<19> PCIE\_PTX\_C\_DRX\_N1  
<19> PCIE\_PTX\_C\_DRX\_P1

<19> PCIE\_PRX\_DTX\_N2  
<19> PCIE\_PRX\_DTX\_P2  
<19> PCIE\_PTX\_C\_DRX\_N2  
<19> PCIE\_PTX\_C\_DRX\_P2

<19> PCIE\_PRX\_DTX\_N3  
<19> PCIE\_PRX\_DTX\_P3  
<19> PCIE\_PTX\_C\_DRX\_N3  
<19> PCIE\_PTX\_C\_DRX\_P3

<19> PCIE\_PRX\_DTX\_N4  
<19> PCIE\_PRX\_DTX\_P4  
<19> PCIE\_PTX\_C\_DRX\_N4  
<19> PCIE\_PTX\_C\_DRX\_P4

<35> PCIE\_PRX\_DTX\_N5  
<35> PCIE\_PRX\_DTX\_P5  
<35> PCIE\_PTX\_C\_DRX\_N5  
<35> PCIE\_PTX\_C\_DRX\_P5

<30> PCIE\_PRX\_DTX\_N6  
<30> PCIE\_PRX\_DTX\_P6  
<30> PCIE\_PTX\_C\_DRX\_N6  
<30> PCIE\_PTX\_C\_DRX\_P6

<29> SATA\_PRX\_DTX\_N0  
<29> SATA\_PRX\_DTX\_P0  
<29> SATA\_PTX\_C\_DRX\_N0  
<29> SATA\_PTX\_C\_DRX\_P0

<31> PCIE\_PRX\_DTX\_N9  
<31> PCIE\_PRX\_DTX\_P9  
<31> PCIE\_PTX\_C\_DRX\_N9  
<31> PCIE\_PTX\_C\_DRX\_P9

<31> PCIE\_PRX\_DTX\_N10  
<31> PCIE\_PRX\_DTX\_P10  
<31> PCIE\_PTX\_C\_DRX\_N10  
<31> PCIE\_PTX\_C\_DRX\_P10

<31> PCIE\_PRX\_DTX\_N11  
<31> PCIE\_PRX\_DTX\_P11  
<31> PCIE\_PTX\_C\_DRX\_N11  
<31> PCIE\_PTX\_C\_DRX\_P11  
<31> PCIE\_PRX\_DTX\_N12  
<31> PCIE\_PRX\_DTX\_P12  
<31> PCIE\_PTX\_C\_DRX\_N12  
<31> PCIE\_PTX\_C\_DRX\_P12

CC11 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N1  
CC14 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P1

CC15 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N2  
CC16 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P2

CC18 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N3  
CC13 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P3

CC17 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N4  
CC18 DIS@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P4

CC19 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_N5  
CC20 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_P5

CC102 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_N6  
CC103 1 2 0.1U 0201 10V K XSR PCIE\_PTX\_DRX\_P6

CC110 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N9  
CC109 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P9

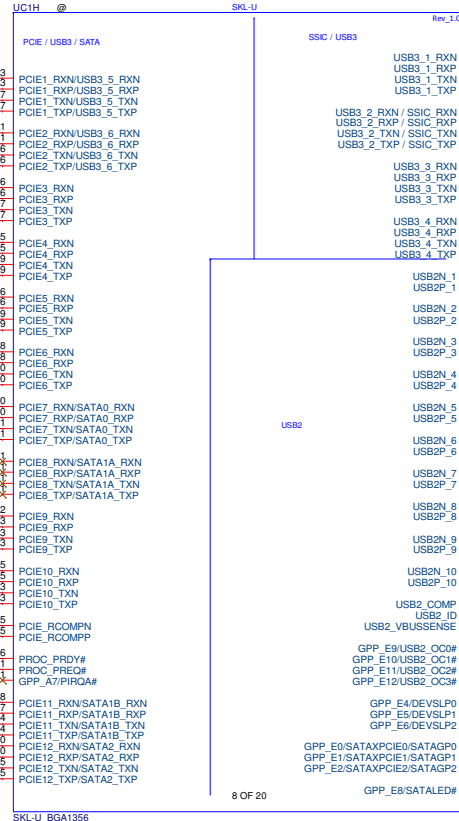
CC114 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N10  
CC113 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P10

RC71 1 2 100 0402 1% PCIE\_ROMPN  
PCIE\_ROMPP

T147 TP@ XDP\_PRODM#  
T148 TP@ XDP\_PRCDF#

CC116 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N11  
CC115 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P11

CC112 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_N12  
CC111 SSD@ 1 2 0.22U 0402 6.3V6K PCIE\_PTX\_DRX\_P12



USB3 Type-C (MUX)

USB2/3 Port (MB)

USB2/3 Port (IO/B)

USB3 Type-C Port

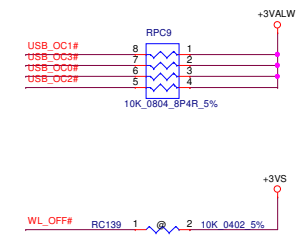
USB2/3 Port (MB)

USB2/3 Port (IO/B)

Camera

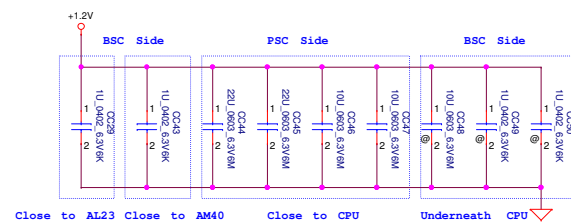
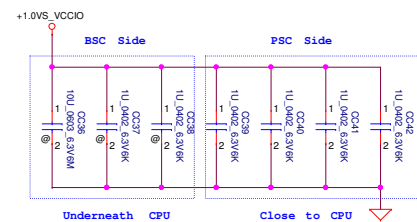
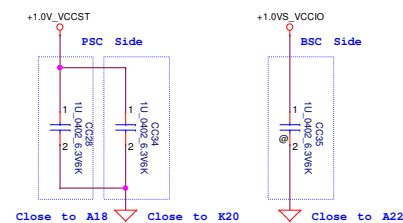
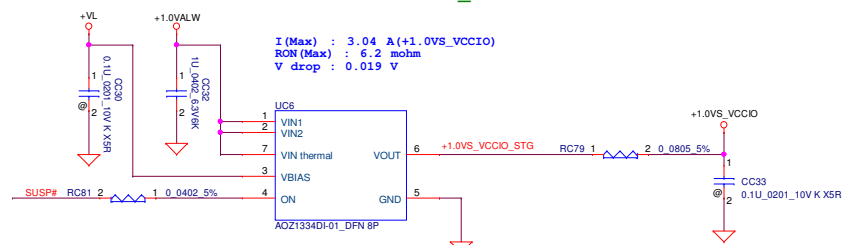
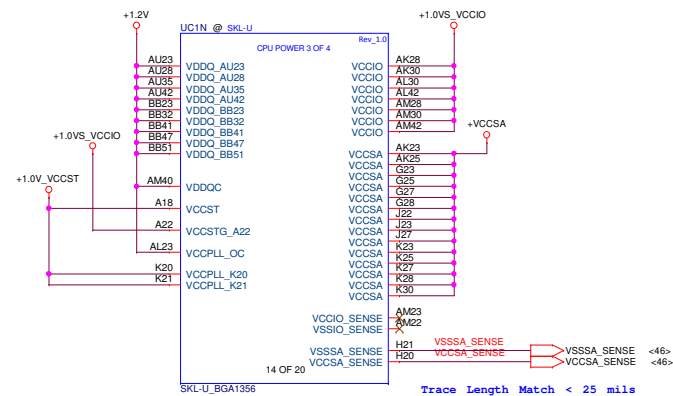
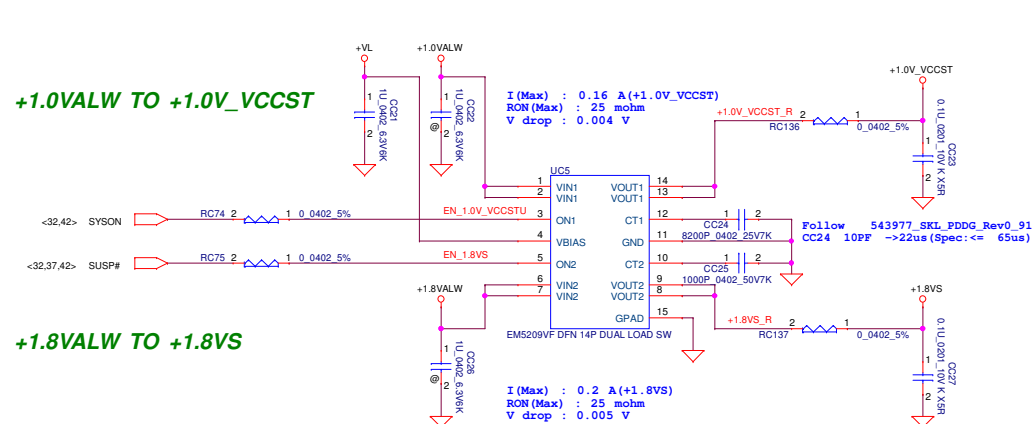
Finger Printer

NGFF WLAN+BT



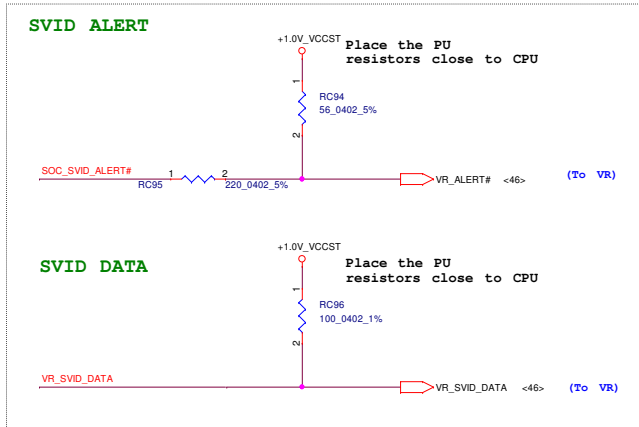
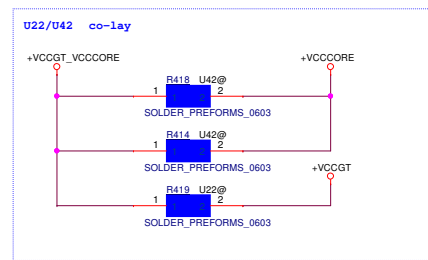
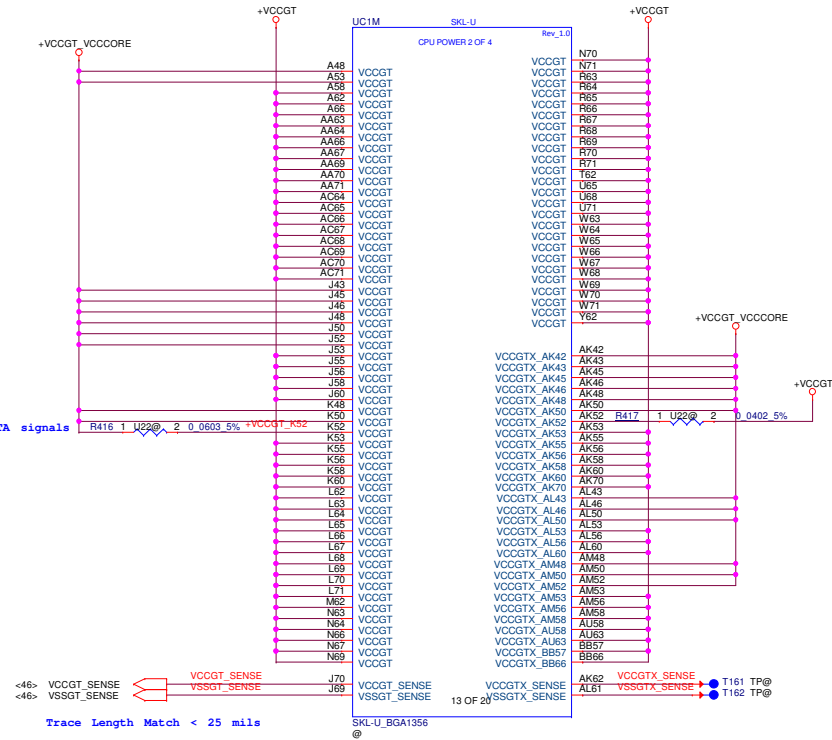
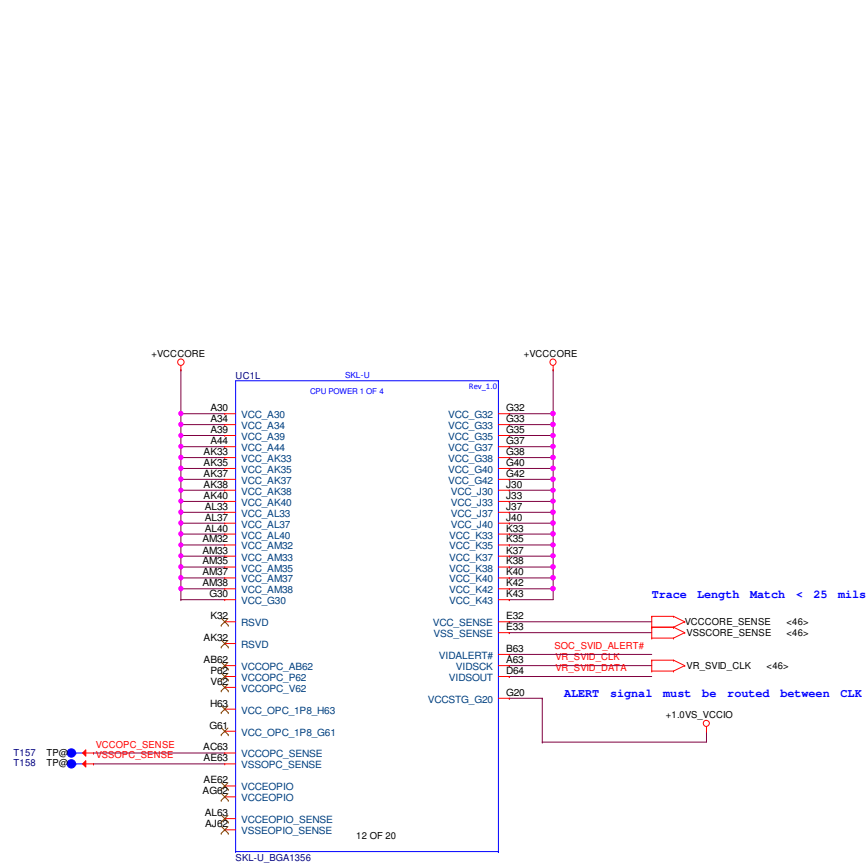
When PCIE8/SATA1A is used as SATA Port 1 (ODD), then  
PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

| Security Classification   | Compal Secret Data |                 | Title      |                                |
|---|--------------------|-----------------|------------|--------------------------------|
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 |                                |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size<br>Custom                 |
|   |                    |                 |            | Document Number<br>LA-E541P    |
|   |                    |                 |            | Rev<br>2A                      |
|   |                    |                 |            | Date: Wednesday, June 21, 2017 |
|   |                    |                 |            | Sheet 12 of 51                 |

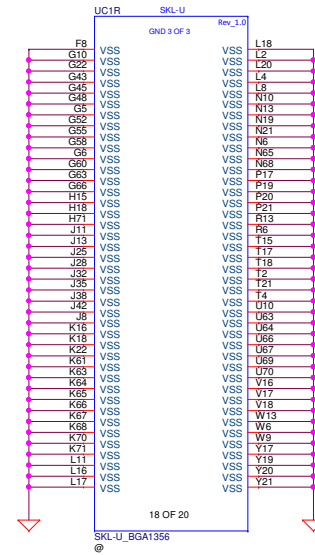
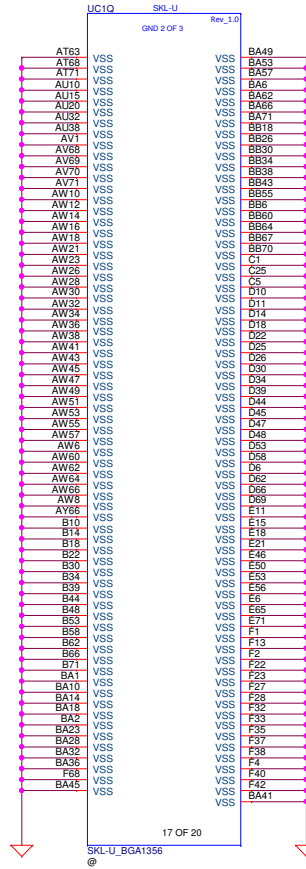
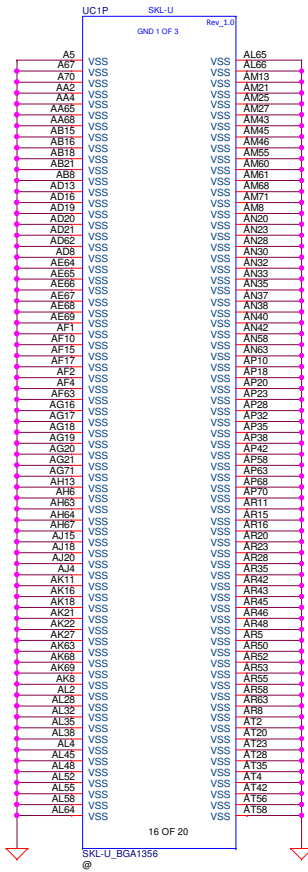


|   |            |                    |            |                                 |                          |
|---|------------|--------------------|------------|---------------------------------|--------------------------|
| Security Classification   |            | Compal Secret Data |            | <b>Compal Electronics, Inc.</b> |                          |
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | Title                           | <b>SKL-U(8/12)Power</b>  |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | Size                            | Document Number          |
|   |            |                    |            | Customer                        | LA-E541P                 |
|   |            |                    |            | Date:                           | Wednesday, June 21, 2017 |
|   |            |                    |            | Sheet                           | 13 of 51                 |



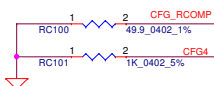


| Security Classification   |  |            |  | Compal Secret Data |  |            |  | Compal Electronics, Inc.       |  |  |  |
|---|--|------------|--|--------------------|--|------------|--|--------------------------------|--|--|--|
| Issued Date   |  | 2017/06/05 |  | Deciphered Date    |  | 2018/06/05 |  | Title                          |  |  |  |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |  |            |  |                    |  |            |  | Size                           |  |  |  |
|   |  |            |  |                    |  |            |  | Document Number                |  |  |  |
|   |  |            |  |                    |  |            |  | Rev                            |  |  |  |
|   |  |            |  |                    |  |            |  | 2A                             |  |  |  |
|   |  |            |  |                    |  |            |  | Date: Wednesday, June 21, 2017 |  |  |  |
|   |  |            |  |                    |  |            |  | Sheet 15 of 51                 |  |  |  |



|   |                    |                 |            |                                |                |
|---|--------------------|-----------------|------------|--------------------------------|----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc.       |                |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 | Title                          |                |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size                           | Rev            |
|   |                    |                 |            | Document Number                | 2A             |
|   |                    |                 |            | LA-E541P                       |                |
|   |                    |                 |            | Date: Wednesday, June 21, 2017 | Sheet 16 of 51 |





| Display Port Presence Strap |   |
|-----------------------------|---|
| CFG4                        | <p>1 : Disabled;<br/>No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled;<br/>An external Display Port device is connected to the Embedded Display Port</p> |

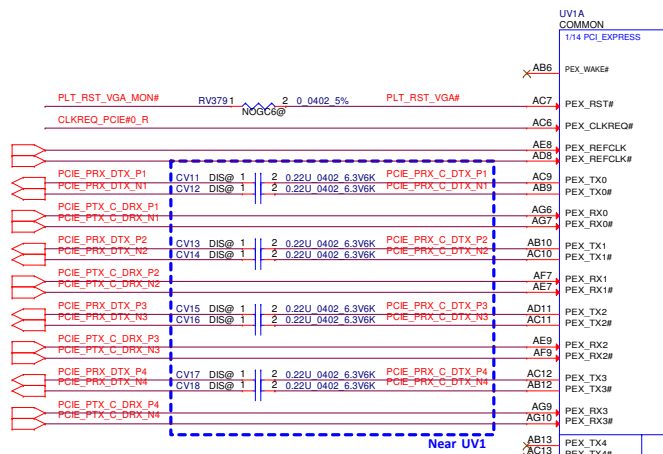
|  |            |                    |            |  |                |
|--|------------|--------------------|------------|--|----------------|
| Security Classification  |            | Compal Secret Data |            | <b>Compal Electronics, Inc.</b><br><b>SKL-U(12/12)CFG,RSVD</b> |                |
| Issued Date  | 2017/06/05 | Deciphered Date    | 2018/06/05 | Title  |                |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | Size   | Rev            |
|  |            |                    |            | Document Number  | 2.A            |
|  |            |                    |            | LA-E541P   |                |
| Date:  |            |                    |            | Wednesday, June 21, 2017                                       | Sheet 17 of 51 |



# PCIE CLK

# PCIE X4 Bus

- <10> CLK\_PEG\_VGA
- <10> CLK\_PEG\_VGA#
- <12> PCIE\_PRX\_DTX\_P1
- <12> PCIE\_PRX\_DTX\_N1
- <12> PCIE\_PTX\_C\_DRX\_P1
- <12> PCIE\_PTX\_C\_DRX\_N1
- <12> PCIE\_PRX\_DTX\_P2
- <12> PCIE\_PRX\_DTX\_N2
- <12> PCIE\_PTX\_C\_DRX\_P2
- <12> PCIE\_PTX\_C\_DRX\_N2
- <12> PCIE\_PRX\_DTX\_P3
- <12> PCIE\_PRX\_DTX\_N3
- <12> PCIE\_PTX\_C\_DRX\_P3
- <12> PCIE\_PTX\_C\_DRX\_N3
- <12> PCIE\_PRX\_DTX\_P4
- <12> PCIE\_PRX\_DTX\_N4
- <12> PCIE\_PTX\_C\_DRX\_P4
- <12> PCIE\_PTX\_C\_DRX\_N4

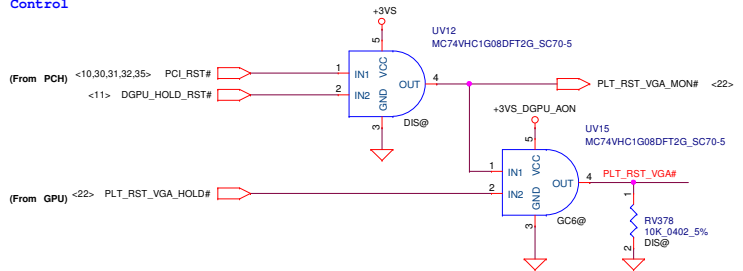


Near UV1

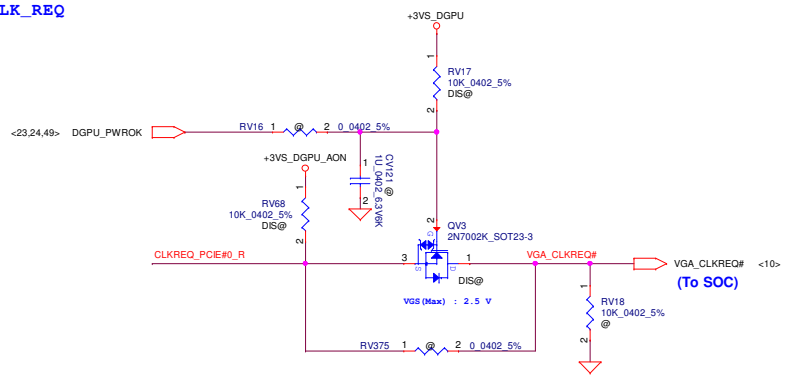
NC FOR GM108

NC FOR GF117/GK208/GM108

# Reset Control



# CLK\_REQ



VGS (Max) : 2.5 V

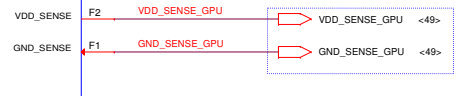
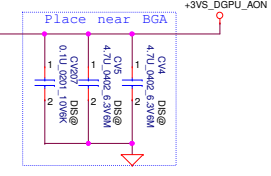
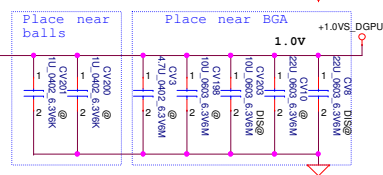
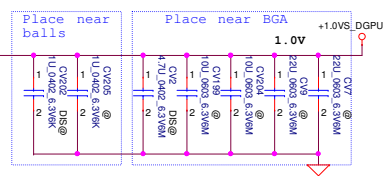
(To SOC)

UV1A COMMON

1/14 PCI\_EXPRESS

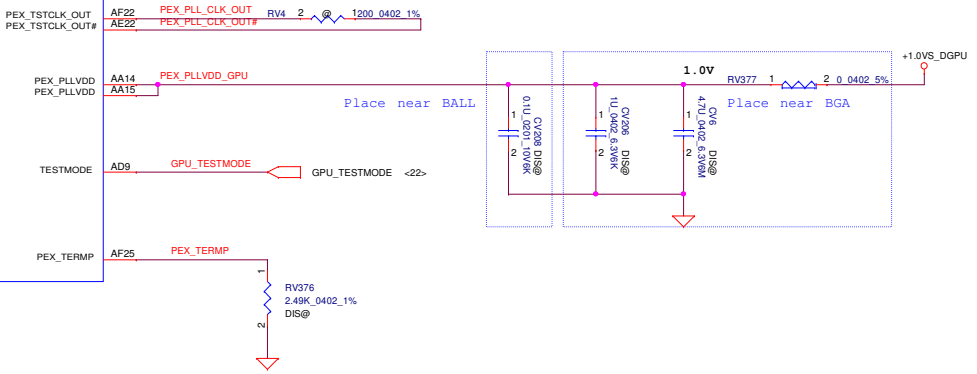
- AB6 PEX\_WAKE#
- AC7 PEX\_RST#
- AC6 PEX\_CLKREQ#
- AE8 PEX\_REFCLK#
- AC9 PEX\_TX0#
- AB9 PEX\_TX0#
- AG6 PEX\_RX0#
- AG7 PEX\_RX0#
- AC10 PEX\_TX1#
- AF7 PEX\_RX1#
- AE7 PEX\_RX1#
- AD11 PEX\_TX2#
- AC11 PEX\_TX2#
- AE9 PEX\_RX2#
- AF9 PEX\_RX2#
- AC12 PEX\_TX3#
- AB12 PEX\_TX3#
- AG9 PEX\_RX3#
- AG10 PEX\_RX3#
- AB13 PEX\_TX4#
- AC13 PEX\_TX4#
- AF10 PEX\_RX4#
- AE10 PEX\_RX4#
- AD14 PEX\_TX5#
- AC14 PEX\_TX5#
- AE12 PEX\_RX5#
- AF12 PEX\_RX5#
- AC15 PEX\_TX6#
- AB15 PEX\_TX6#
- AG12 PEX\_RX6#
- AG13 PEX\_RX6#
- AB16 PEX\_TX7#
- AC16 PEX\_TX7#
- AF13 PEX\_RX7#
- AE13 PEX\_RX7#
- AD17 PEX\_TX8#
- AC17 PEX\_TX8#
- AE15 PEX\_RX8#
- AF15 PEX\_RX8#
- AG15 PEX\_TX9#
- AG16 PEX\_TX9#
- AC19 PEX\_RX9#
- AC19 PEX\_RX9#
- AF16 PEX\_TX10#
- AE16 PEX\_TX10#
- AD20 PEX\_RX10#
- AC20 PEX\_RX10#
- AE18 PEX\_TX11#
- AF18 PEX\_TX11#
- AC21 PEX\_RX11#
- AB21 PEX\_RX11#
- AG18 PEX\_TX12#
- AG19 PEX\_TX12#
- AD23 PEX\_RX12#
- AE23 PEX\_RX12#
- AD23 PEX\_TX13#
- AE23 PEX\_TX13#
- AF19 PEX\_RX13#
- AE19 PEX\_RX13#
- AG24 PEX\_TX14#
- AG24 PEX\_TX14#
- AF21 PEX\_RX14#
- AG24 PEX\_RX14#
- AG25 PEX\_TX15#
- AG25 PEX\_TX15#
- AC21 PEX\_RX15#
- AG22 PEX\_RX15#

N16S-GT-S-A2\_BGA595

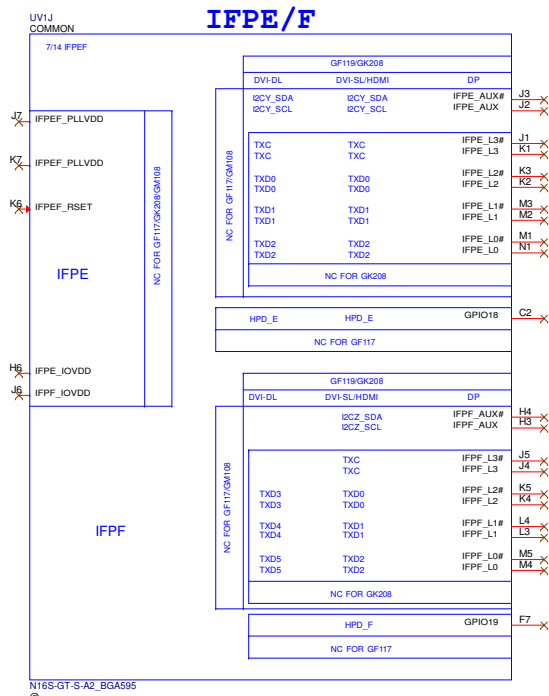
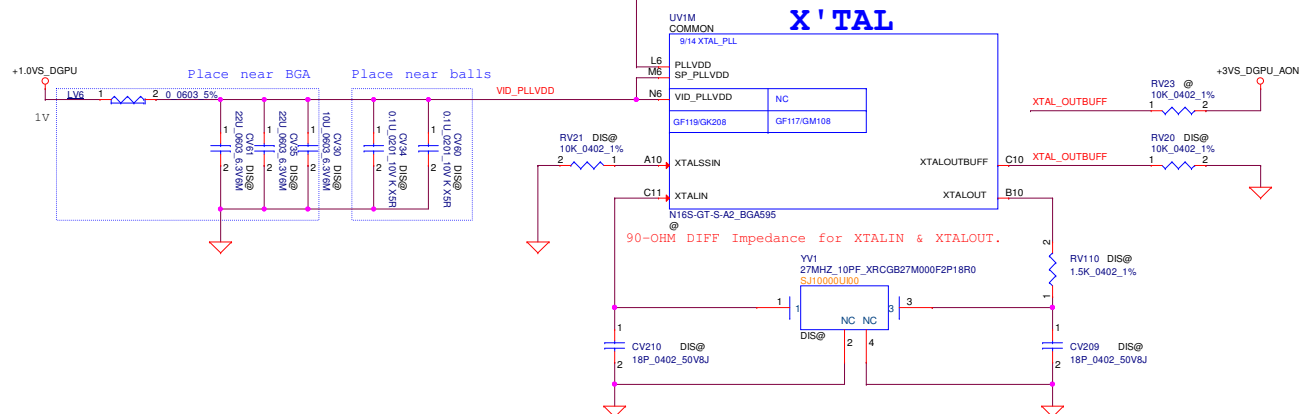
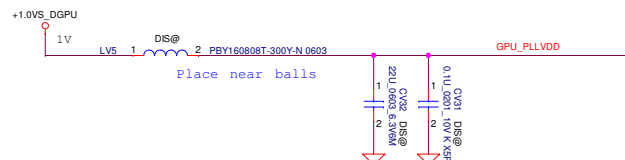
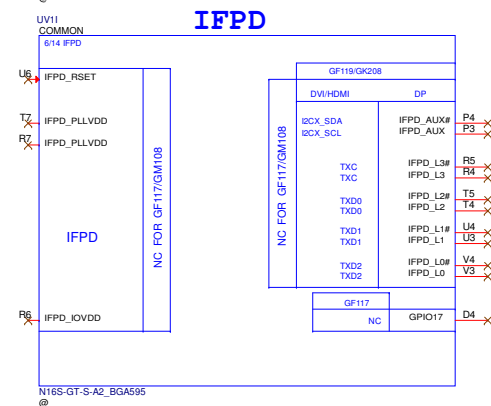
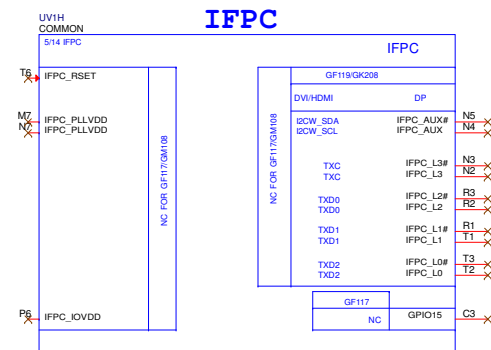
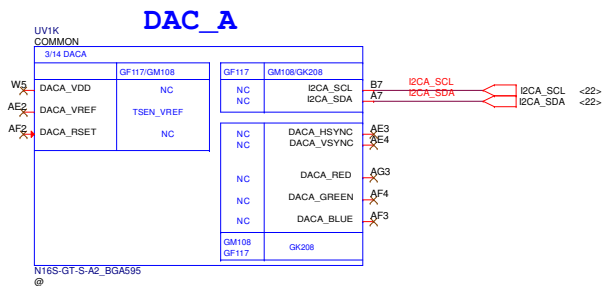
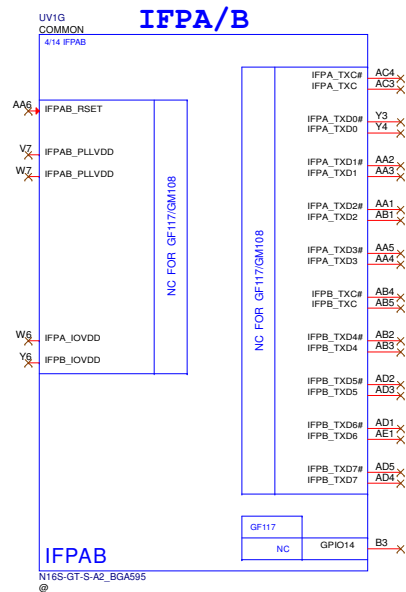


# To POWER

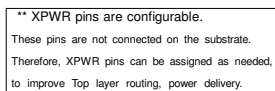
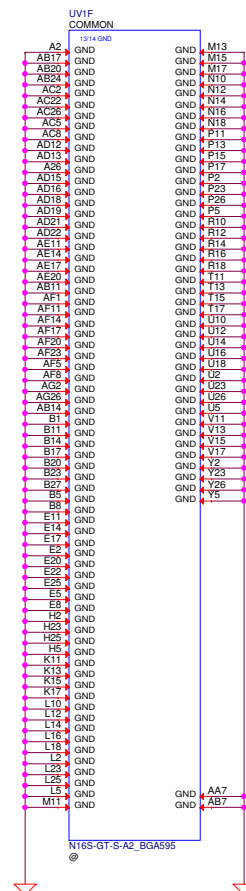
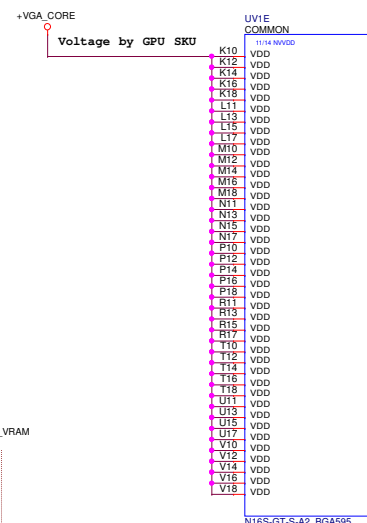
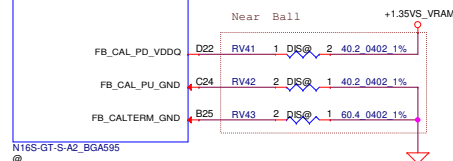
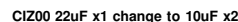
trace width: 16mils  
differential voltage sensing.  
differential signal routing.



|   |            |                    |            |                          |                          |
|---|------------|--------------------|------------|--------------------------|--------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                          |
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | Title                    | NV(1/5)-PCIE             |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | Size                     | Document Number          |
|   |            |                    |            | Date:                    | Wednesday, June 21, 2017 |
|   |            |                    |            | Sheet                    | 19 of 51                 |
|   |            |                    |            | Rev                      | 2A                       |

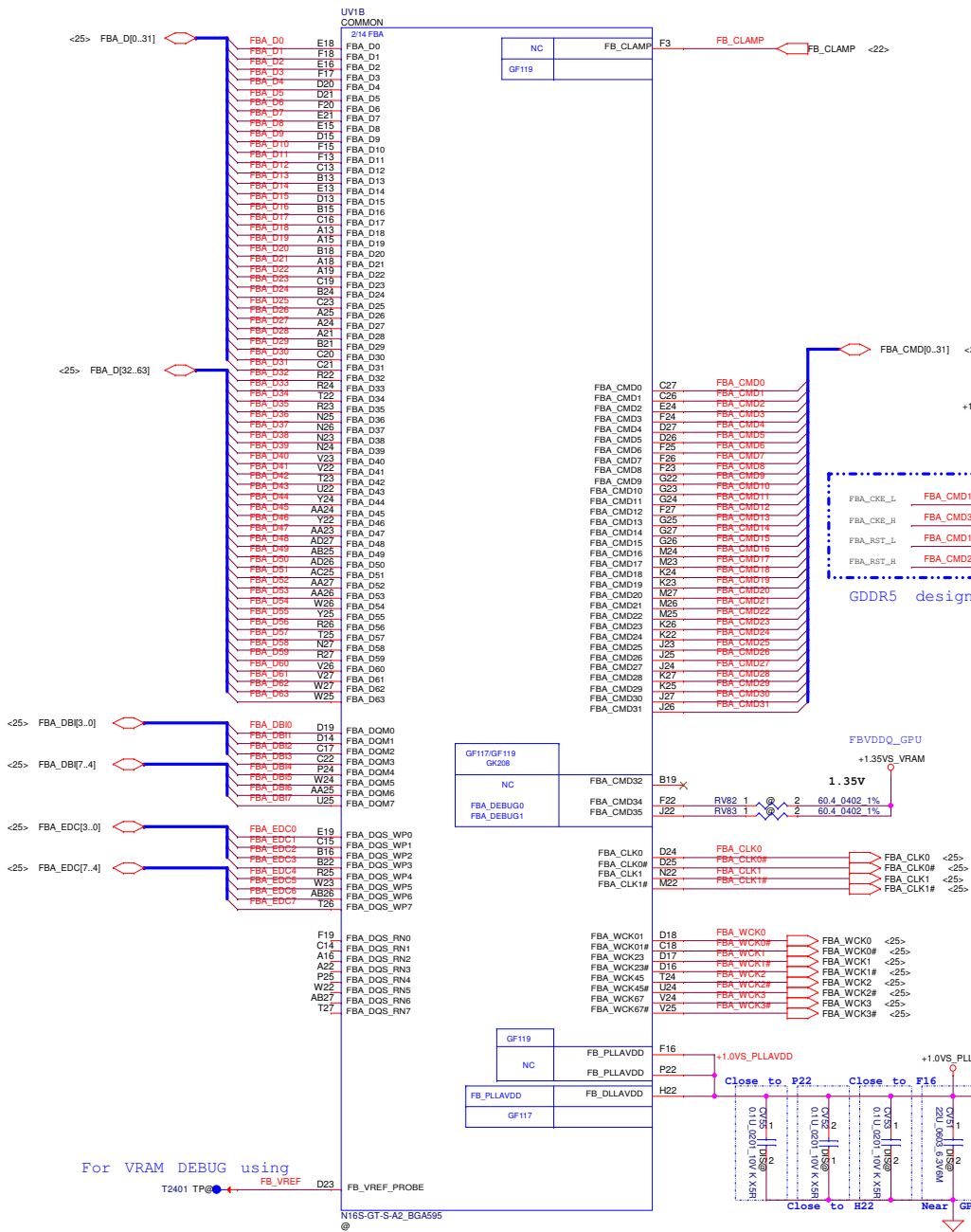


| Security Classification |  |                 |  | Compal Secret Data |  |                          |  | Compal Electronics, Inc. |  |                             |  |
|-------------------------|--|-----------------|--|--------------------|--|--------------------------|--|--------------------------|--|-----------------------------|--|
| Issued Date             |  | 2017/06/05      |  | Deciphered Date    |  | 2018/06/05               |  | Title                    |  | NV(2/5)-IFP ABCDEF DAC XTAL |  |
| Size                    |  | Document Number |  | Date               |  | Wednesday, June 21, 2017 |  | Sheet                    |  | 20 of 51                    |  |
| Rev                     |  | LA-E541P        |  | Rev                |  | 2A                       |  |                          |  |                             |  |



|   |                    |                 |            |                          |                          |                |
|---|--------------------|-----------------|------------|--------------------------|--------------------------|----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                          |                |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 | Title                    | NV(3/5)-POWER            |                |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size                     | Document Number          | Rev            |
|   |                    |                 |            | LA-E541P                 |                          | 2A             |
|   |                    |                 |            | Date:                    | Wednesday, June 21, 2017 | Sheet 21 of 51 |

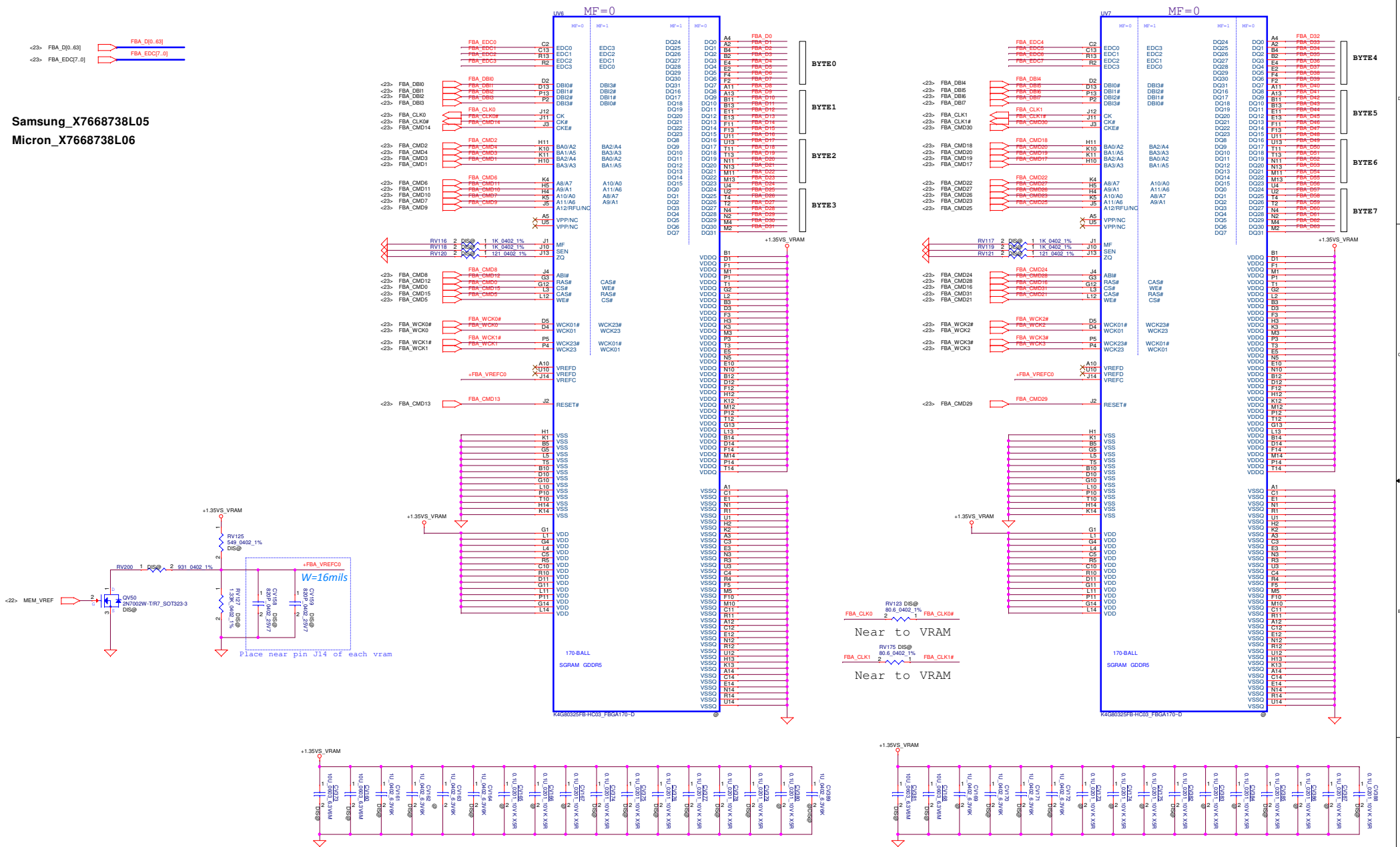




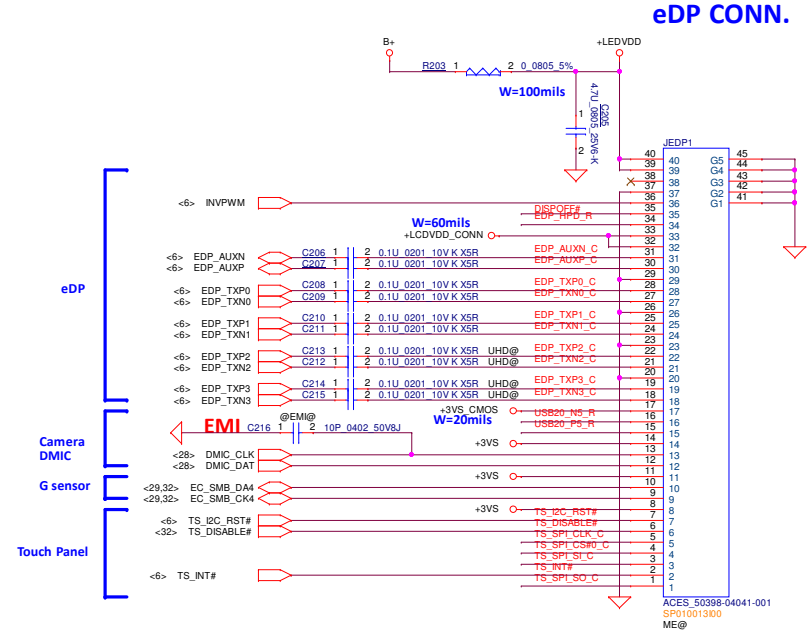
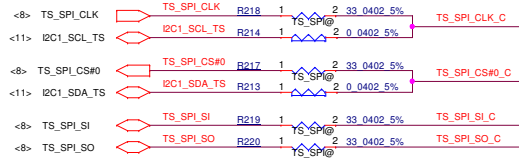
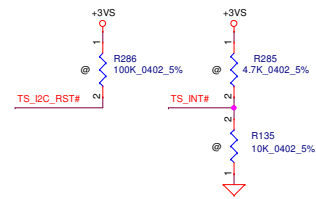
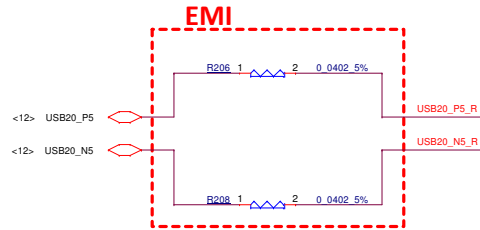
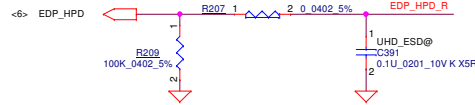
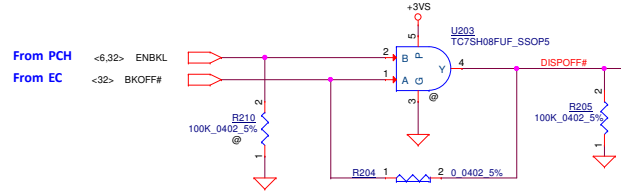
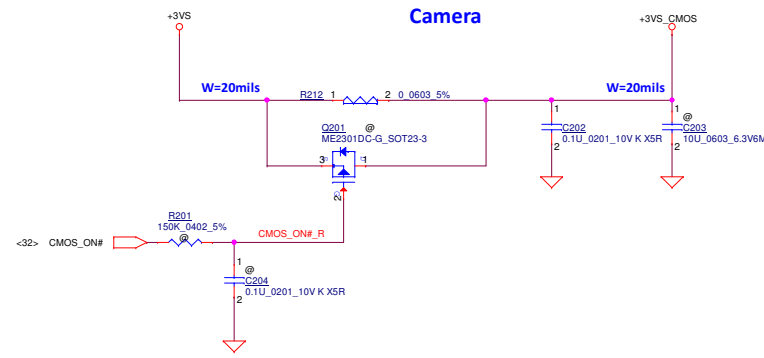
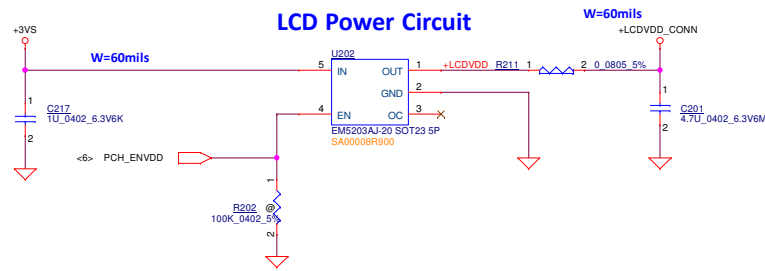




## Memory Partition A



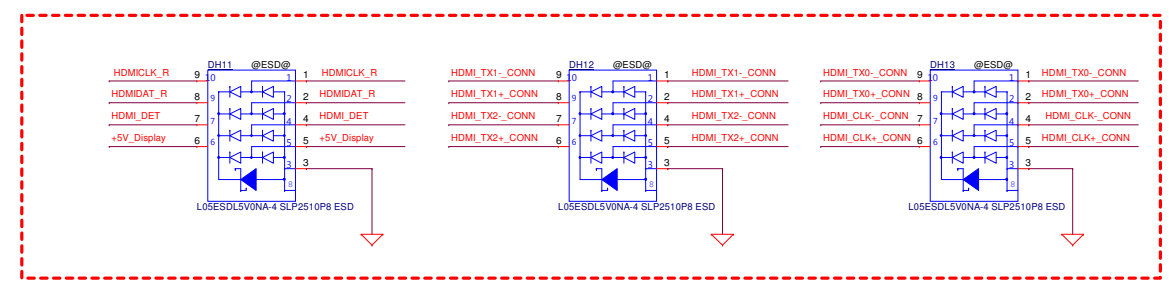
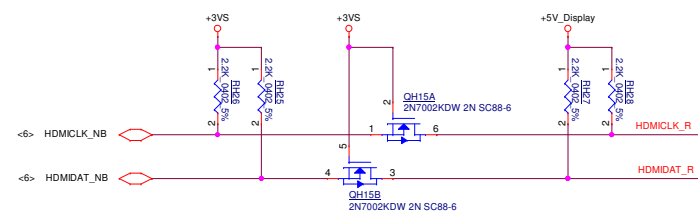
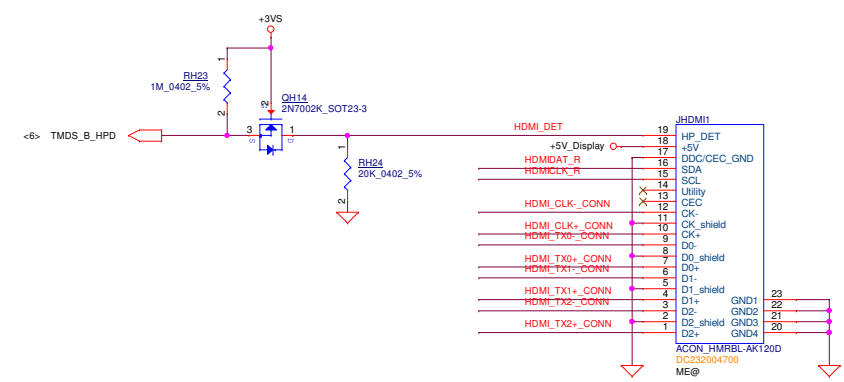
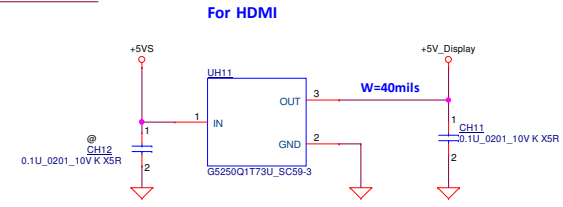
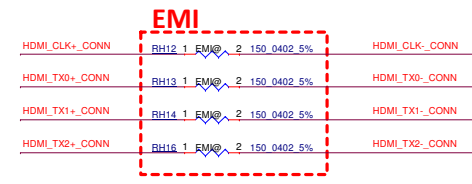
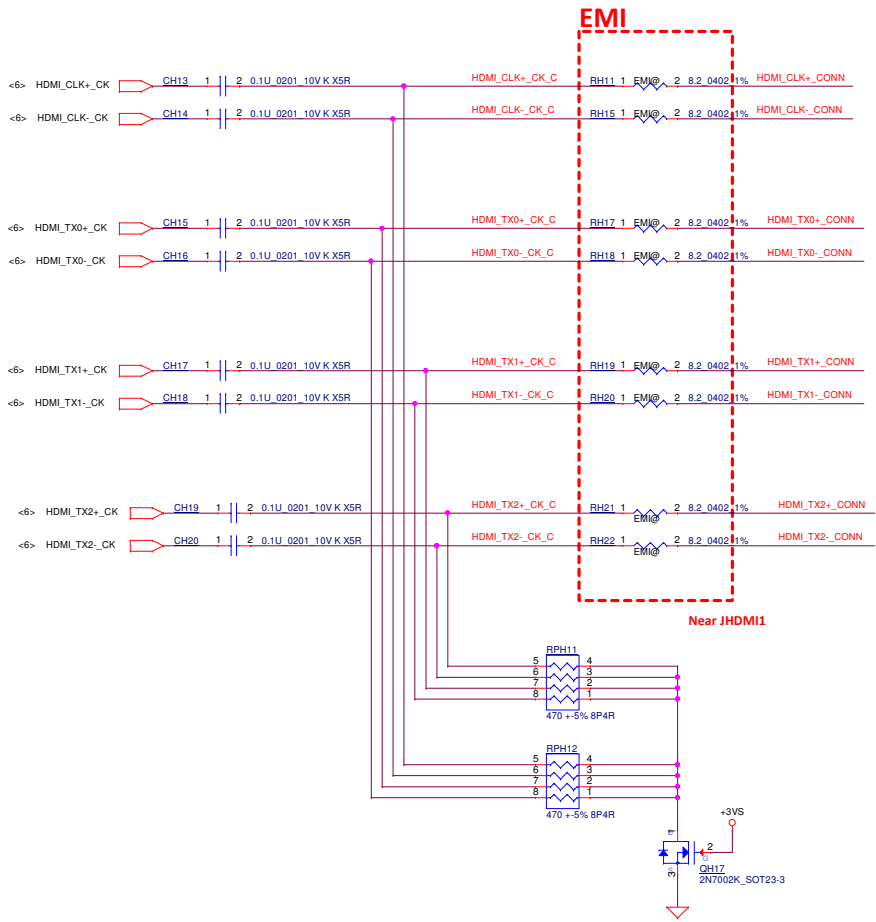
|   |                          |                    |            |                          |              |
|---|--------------------------|--------------------|------------|--------------------------|--------------|
| Security Classification   |                          | Compal Secret Data |            | Compal Electronics, Inc. |              |
| Issued Date   | 2017/06/05               | Deciphered Date    | 2018/06/05 | Title                    | N16P GDDR5 A |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF TWO DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                          |                    |            |                          |              |
| Size  | Document Number          |                    |            | Rev                      | 2A           |
| LA-E541P  |                          |                    |            |                          |              |
| Date:   | Wednesday, June 21, 2017 |                    |            | Sheet                    | 25 of 51     |



| Elan Precise select by BOM (10 pins) |               |               |
|--------------------------------------|---------------|---------------|
| 1                                    | PWR           | PWR           |
| 2                                    | CS            | SCL           |
| 3                                    | SCK           | SDA           |
| 4                                    | MOSI          | Report switch |
| 5                                    | MISO          | INT           |
| 6                                    | Report switch | Reset         |
| 7                                    | INT           | Hsync         |
| 8                                    | Reset         | GND           |
| 9                                    | Hsync         |               |
| 10                                   | GND           |               |
| Total                                | SPI (10 pins) | I2C (8 pins)  |

| SPI & I2C PIN define |                     |
|----------------------|---------------------|
| 1                    | PWR                 |
| 2                    | SPI_Reset/I2C_Reset |
| 3                    | Report_switch       |
| 4                    | GND                 |
| 5                    | SPI_SCK/I2C_SCL     |
| 6                    | SPI_CS/I2C_SDA      |
| 7                    | SPI_MOSI            |
| 8                    | SPI_INT/I2C_INT     |
| 9                    | SPI_MISO            |
| 10                   | GND                 |

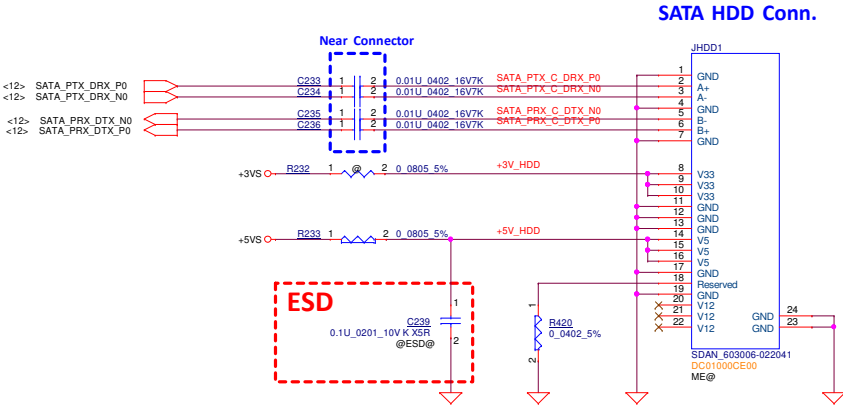
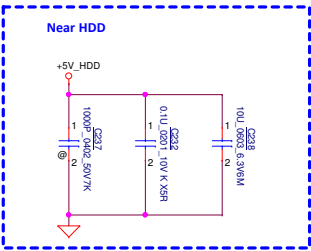
| Security Classification   |  |  |  | Compal Secret Data |  |  |  | Compal Electronics, Inc. |  |  |  |
|---|--|--|--|--------------------|--|--|--|--------------------------|--|--|--|
| Issued Date   |  |  |  | 2017/06/05         |  |  |  | Deciphered Date          |  |  |  |
| 2017/06/05  |  |  |  | 2018/06/05         |  |  |  | Title                    |  |  |  |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |  |  |  | eDP / Camera       |  |  |  | LA-E541P                 |  |  |  |
| Date: Wednesday, June 21, 2017  |  |  |  | Sheet 26 of 51     |  |  |  | Rev 2A                   |  |  |  |



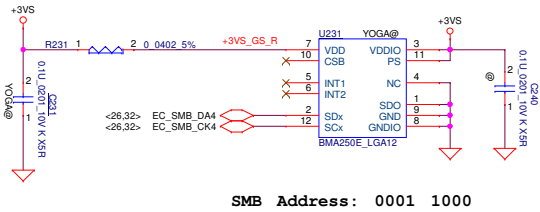
| Security Classification   |  |  |  | Compal Secret Data             |  |  |  | Compal Electronics, Inc. |  |  |  |
|---|--|--|--|--------------------------------|--|--|--|--------------------------|--|--|--|
| Issued Date   |  |  |  | Deciphered Date                |  |  |  | Title                    |  |  |  |
| 2017/06/05  |  |  |  | 2018/06/05                     |  |  |  | HDMI                     |  |  |  |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |  |  |  | Size                           |  |  |  | Rev                      |  |  |  |
|   |  |  |  | Custom                         |  |  |  | 2A                       |  |  |  |
|   |  |  |  | Date: Wednesday, June 21, 2017 |  |  |  | Sheet 27 of 51           |  |  |  |



HDD

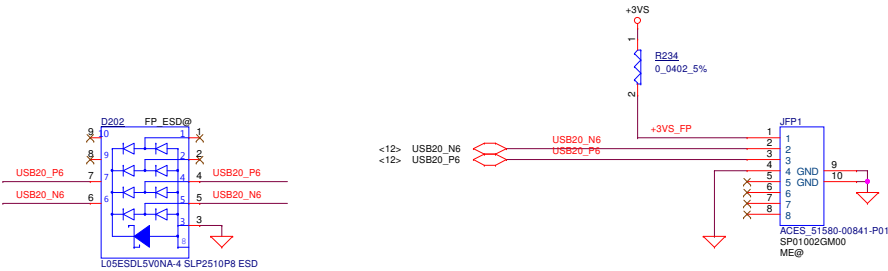


(G-Sensor for 360-degree reverse)

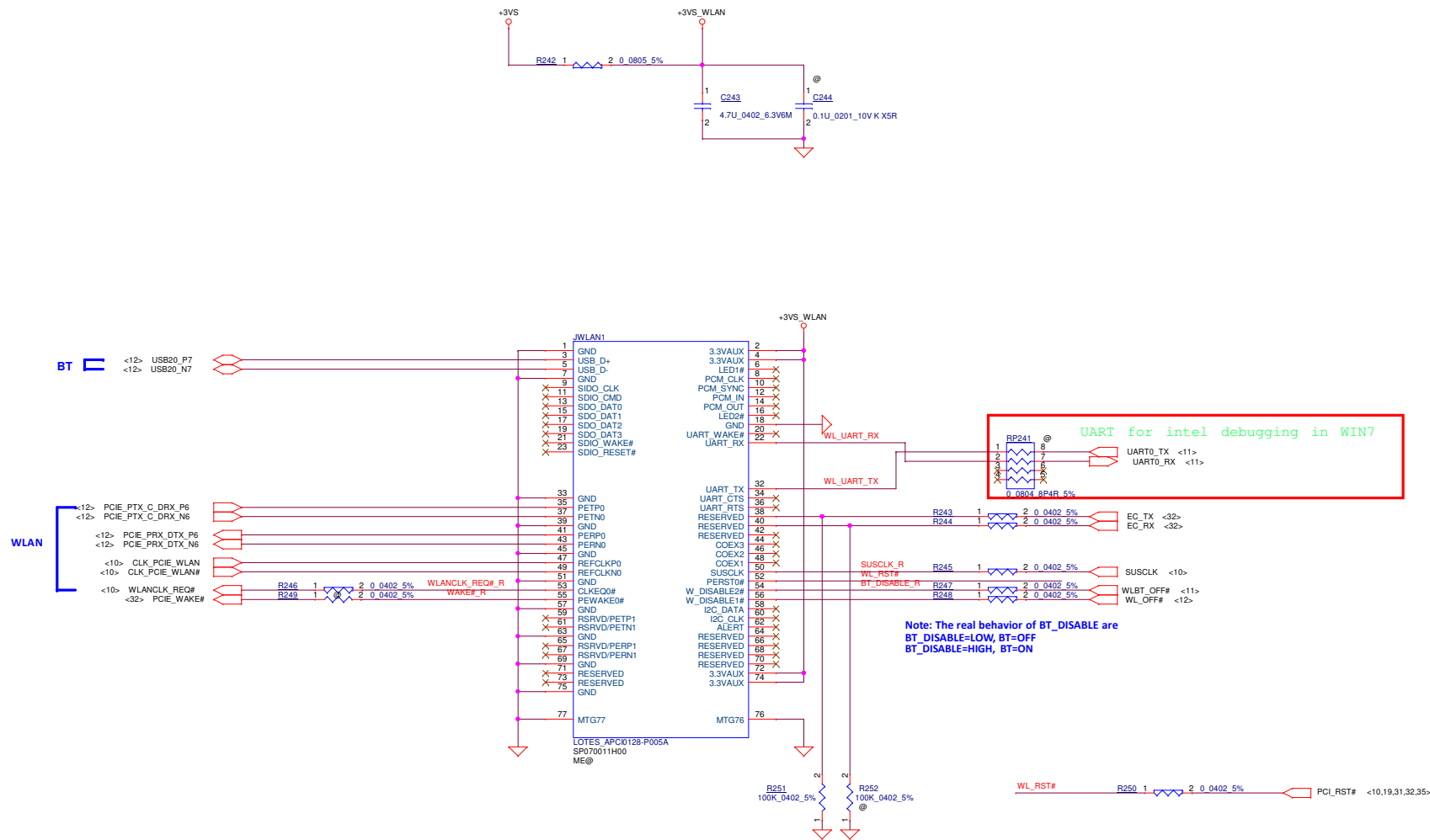


SMB Address: 0001 1000

Finger Printer

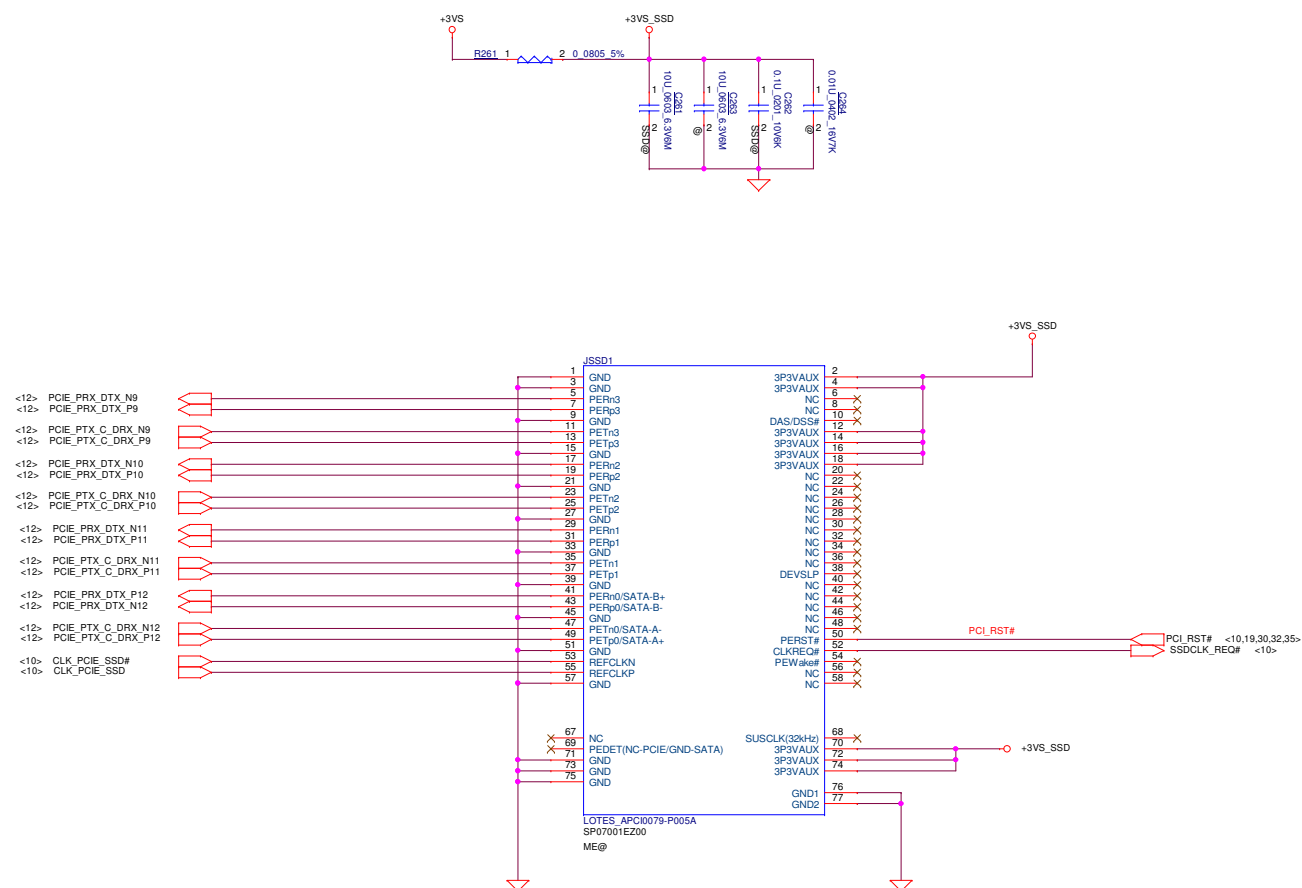


# NGFF for WLAN / BT (E- KEY)



|   |                    |                 |                          |                |
|---|--------------------|-----------------|--------------------------|----------------|
| Security Classification   | Compal Secret Data |                 | Compal Electronics, Inc. |                |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05               | Title          |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |                          | NGFF WLAN / BT |
| LA-E541P  |                    |                 |                          | Rev 2A         |
| Date: Wednesday, June 21, 2017  |                    |                 |                          | Sheet 30 of 51 |

## NGFF for SSD (M-KEY)



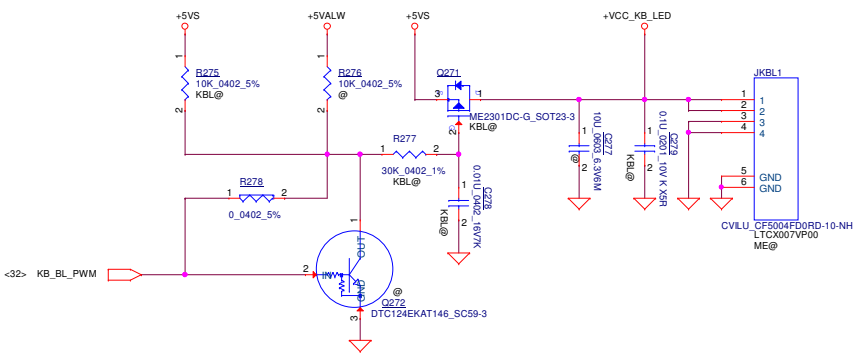
|   |                    |                 |            |                                 |                          |                |
|---|--------------------|-----------------|------------|---------------------------------|--------------------------|----------------|
| Security Classification   | Compal Secret Data |                 |            | <b>Compal Electronics, Inc.</b> |                          |                |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 | Title                           | <b>NGFF SSD</b>          |                |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size                            | Document Number          | Rev            |
|   |                    |                 |            |                                 | <b>LA-E541P</b>          | 2/1            |
|   |                    |                 |            | Date:                           | Wednesday, June 21, 2017 | Sheet 31 of 51 |



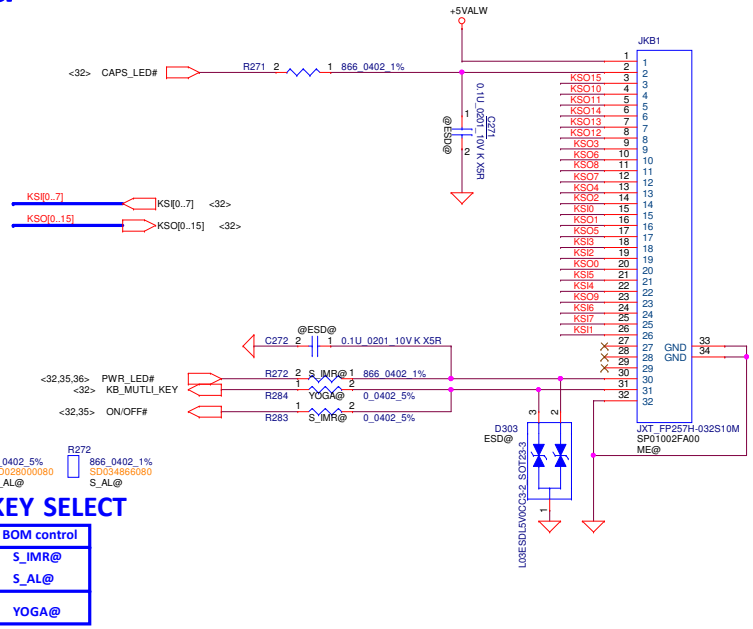
|   |            |                    |            |  |                 |
|---|------------|--------------------|------------|--|-----------------|
| Security Classification   |            | Compal Secret Data |            | <b>Compal Electronics, Inc.</b><br><b>EC NPCE388</b> |                 |
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | Title  |                 |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | Size   | Document Number |
|   |            |                    |            | Customer   | LA-E541P        |
|   |            |                    |            | Date: Wednesday, June 21, 2017                       | Sheet 32 of 51  |



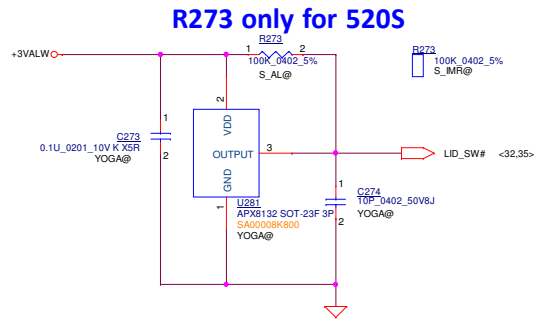
Keyboard Backlight



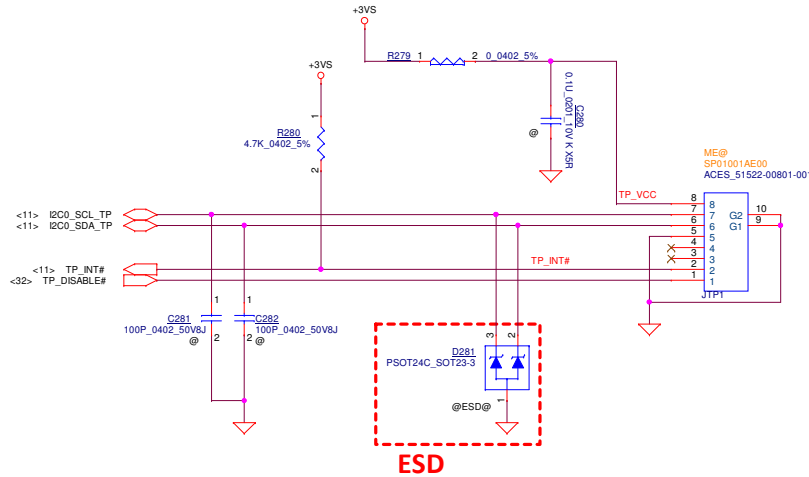
Keyboard



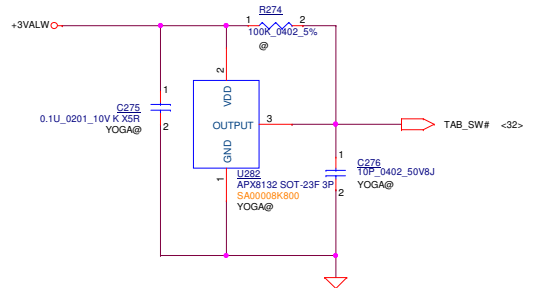
Hall -Sensor for 0-deg reverse (TOP)



Touch Pad

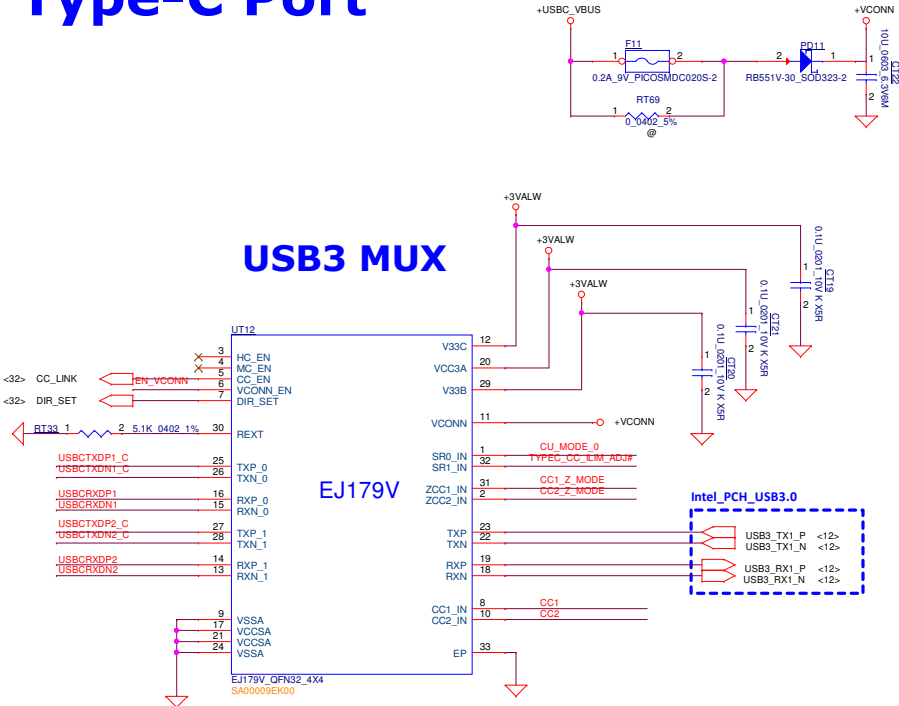


Hall -Sensor for 360-deg reverse (BOT)



# USB Type-C Port

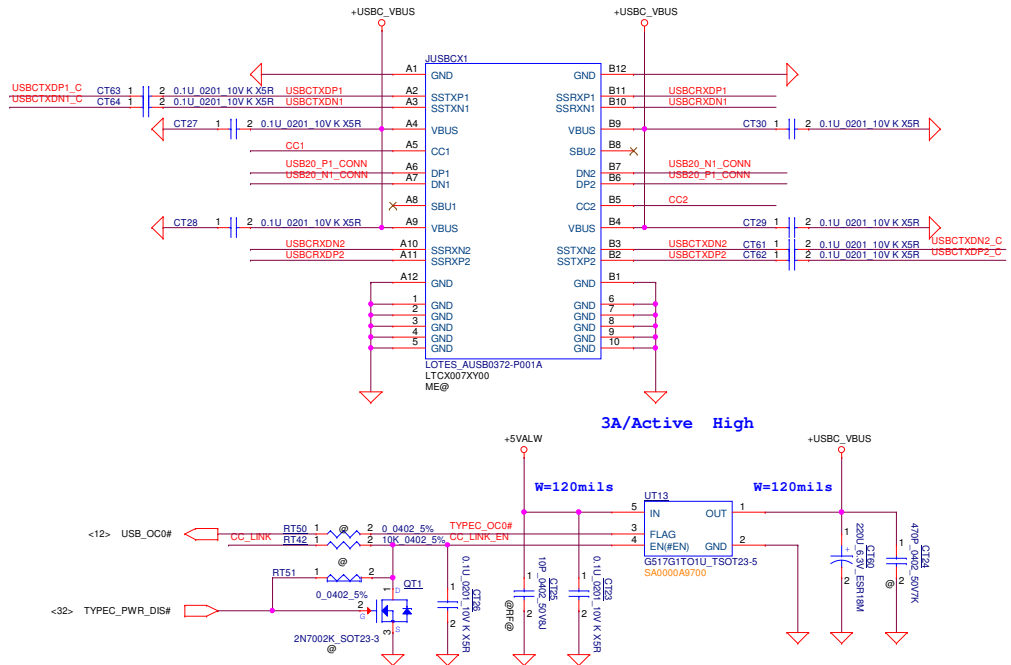
## USB3 MUX



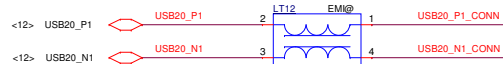
## Profile Selection

| EN_VCONN | CU_MODE_0 | TYPECC_ILIM_ADJ# | CC[1:2]_Z_MODE | CURRNET SELECT    |
|----------|-----------|------------------|----------------|-------------------|
| 1        | 0         | 0                | 00             | DFP 900mA         |
| 1        | 1         | 0                | 00             | DFP 1.5A          |
| 1        | 0         | 1                | 00             | DFP 3A            |
| 0        | 1         | 1                | 00             | UFP               |
| 0        | X         | X                | 01 10 11       | EXTERNAL RESISTER |

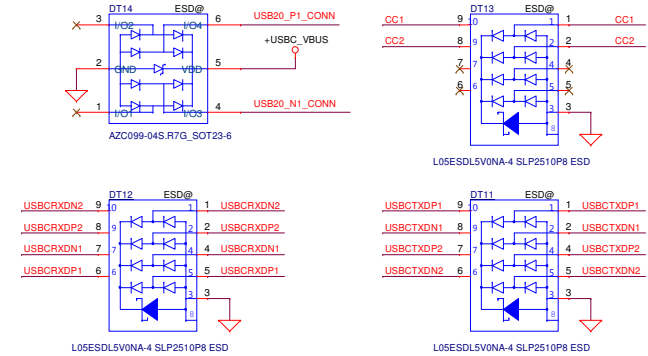
Currently setting



## EMI

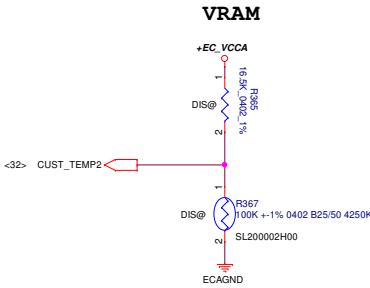
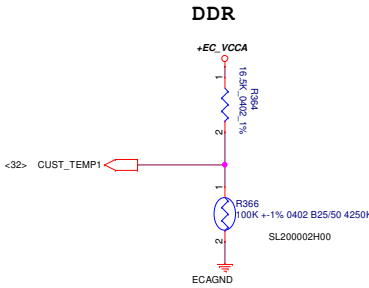
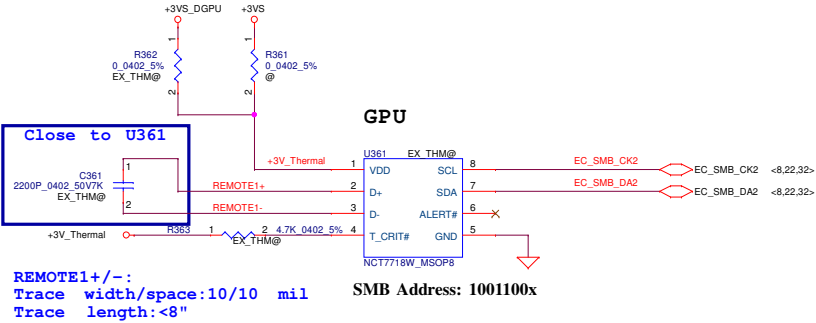


## ESD

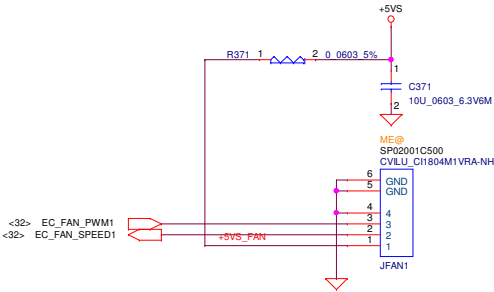




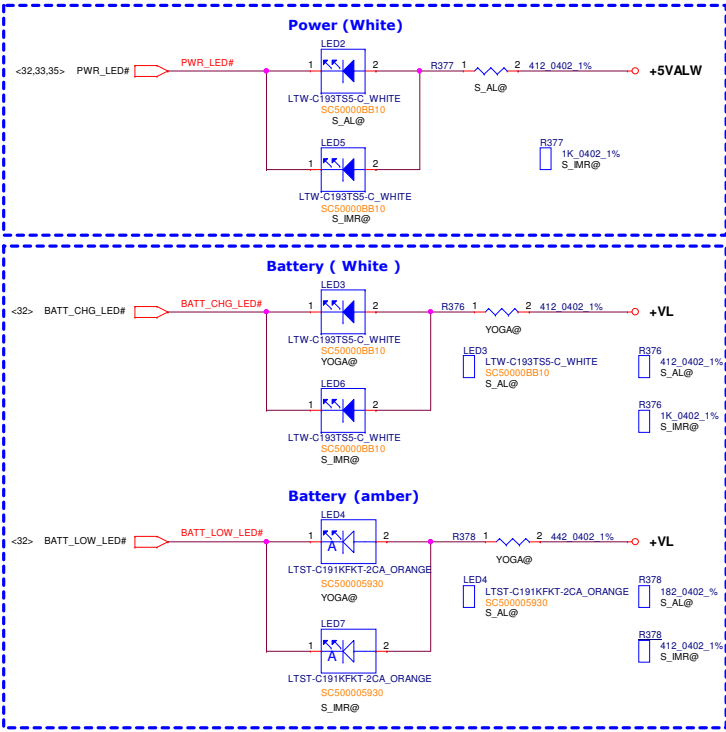
Thermal Sensor



FAN

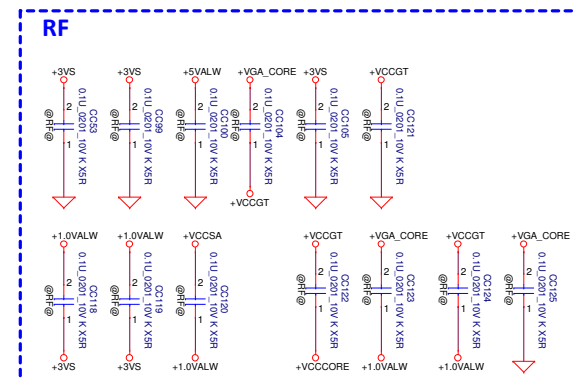


Power LED & Battery LED

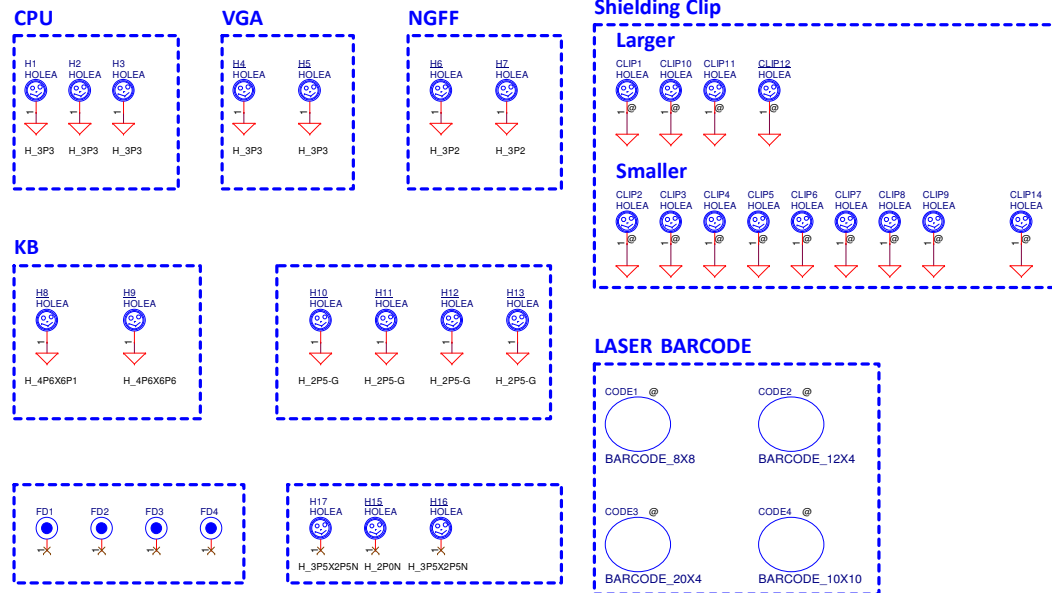
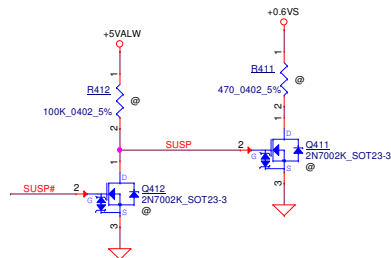


|          |          | Power (White)<br>LED / Res. | Battery (White)<br>LED / Res. | Battery (amber)<br>LED / Res. |
|----------|----------|-----------------------------|-------------------------------|-------------------------------|
| TOP      | YOGA@    | IO Board                    | LED3<br>412 Ω                 | LED4<br>442 Ω                 |
| S series | (S_AL@)  | R377<br>412 Ω               | LED3<br>412 Ω                 | LED4<br>182 Ω                 |
| S IMR    | (S_IMR@) | R377<br>1K Ω                | LED6<br>1K Ω                  | LED7<br>412 Ω                 |

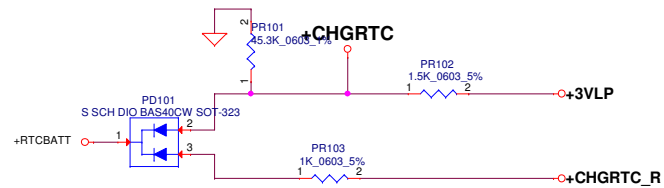
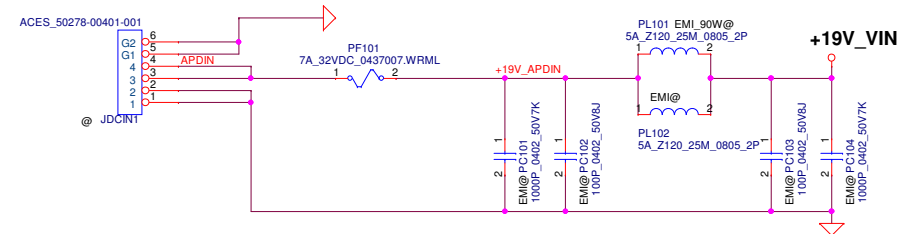
|   |   |   |   |   |
|---|---|---|---|---|
| A | B | C | D | E |
|---|---|---|---|---|



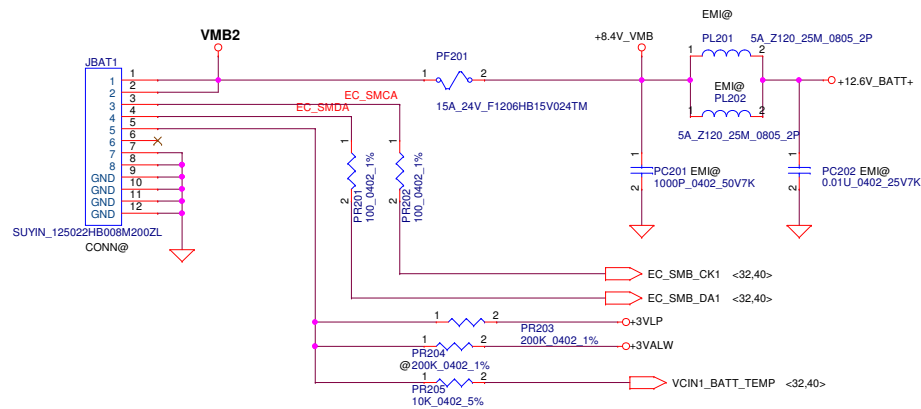
## Screw Hold



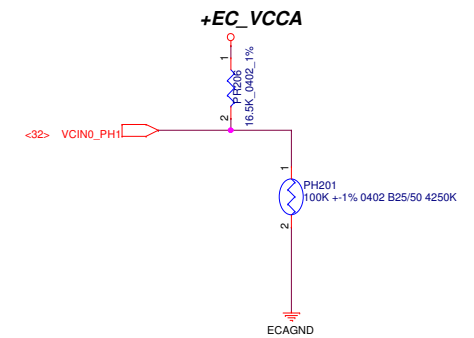
|   |                    |                 |            |                          |                 |     |       |
|---|--------------------|-----------------|------------|--------------------------|-----------------|-----|-------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                 |     |       |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 | Title                    |                 |     |       |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT. RECEIPT IS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | DC to DC                 |                 |     |       |
|   |                    |                 |            | Size                     | Document Number | Rev |       |
|   |                    |                 |            | Custom                   | LA-E541P        |     | 2     |
| Date:   |                    |                 |            | Wednesday, June 21, 2017 | Sheet           | 37  | of 51 |



|   |                    |                 |                          |                          |
|---|--------------------|-----------------|--------------------------|--------------------------|
| Security Classification   | Compal Secret Data |                 | Compal Electronics, Inc. |                          |
| Issued Date   |                    | Deciphered Date |                          | Title                    |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 | Size Custom              | Document Number          |
|   |                    |                 |                          | KBL                      |
|   |                    |                 | Date:                    | Wednesday, June 21, 2017 |
|   |                    |                 | Sheet                    | 38 of 38                 |

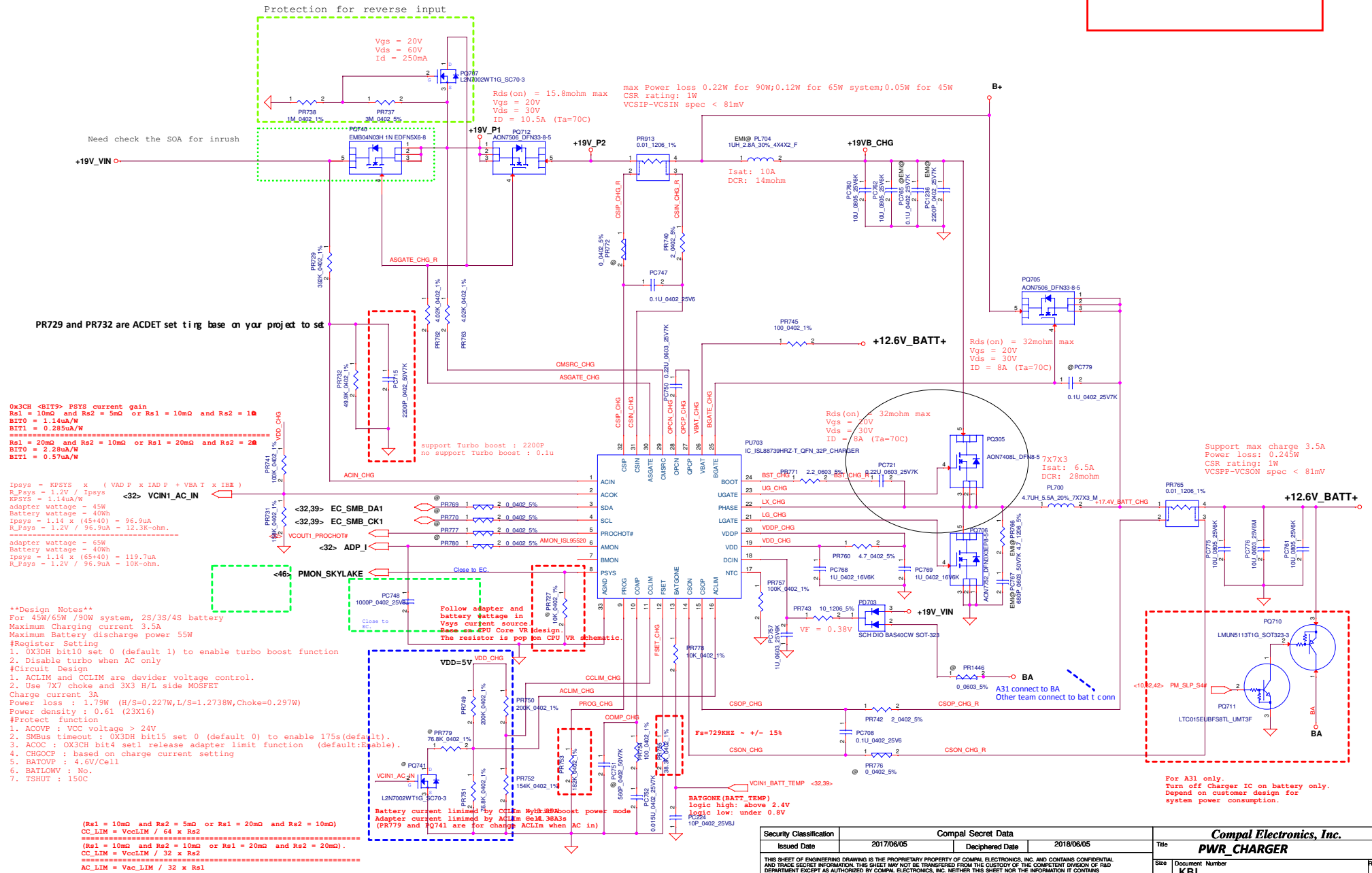


**PH201 under CPU bottom side :**  
**CPU thermal protection at 93  $\pm$  3 degree C**  
**Recovery at 56  $\pm$  3 degree C**



|   |  |                    |  |                 |  |                          |                 |                |  |     |  |
|---|--|--------------------|--|-----------------|--|--------------------------|-----------------|----------------|--|-----|--|
| Security Classification   |  | Compal Secret Data |  |                 |  | Compal Electronics, Inc. |                 |                |  |     |  |
| Issued Date   |  | 2017/06/05         |  | Deciphered Date |  | 2018/06/05               |                 | Title          |  |     |  |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |  |                    |  |                 |  | PWR- BATTERY CONN/OTP    |                 |                |  |     |  |
|   |  |                    |  |                 |  | Size                     | Document Number |                |  | Rev |  |
|   |  |                    |  |                 |  | Custom                   | KBL             |                |  | 2A  |  |
|   |  |                    |  |                 |  |                          |                 |                |  |     |  |
|   |  |                    |  |                 |  |                          |                 |                |  |     |  |
| Date:   |  |                    |  |                 |  | Wednesday, June 21, 2017 |                 | Sheet 39 of 51 |  |     |  |

Module model information  
ISL95520\_Hybrid\_Boost\_V2.mdd





# Module model information

SY8286B\_V3\_single.mdd  
SY8286B\_V3\_dual.mdd

Check pull up resistor of SP0K at HW side

keep short pad,  
snubber is for EMI only.

Use 7x7x3 size when the layout space is enough.

Vout is 3.234V~3.366V

TDC=6A

Iocp=10A

<32,35> EC\_ON

EN1 and EN2 don't be floating.  
EN :H>0.8V ; L<0.4V

Fsw : 600K Hz

+3VALWP

+3VLP

Fsw : 600K Hz

EN1 and EN2 don't be floating.  
EN :H>0.8V ; L<0.4V

2 Cell battery : Cin=10uF\*2pcs  
3 Cell ~ 4 Cell battery : Cin=10uF\*1pcs

keep short pad,  
snubber is for EMI only.

Vout is 4.998V~5.202V

TDC=6A

Iocp=10A

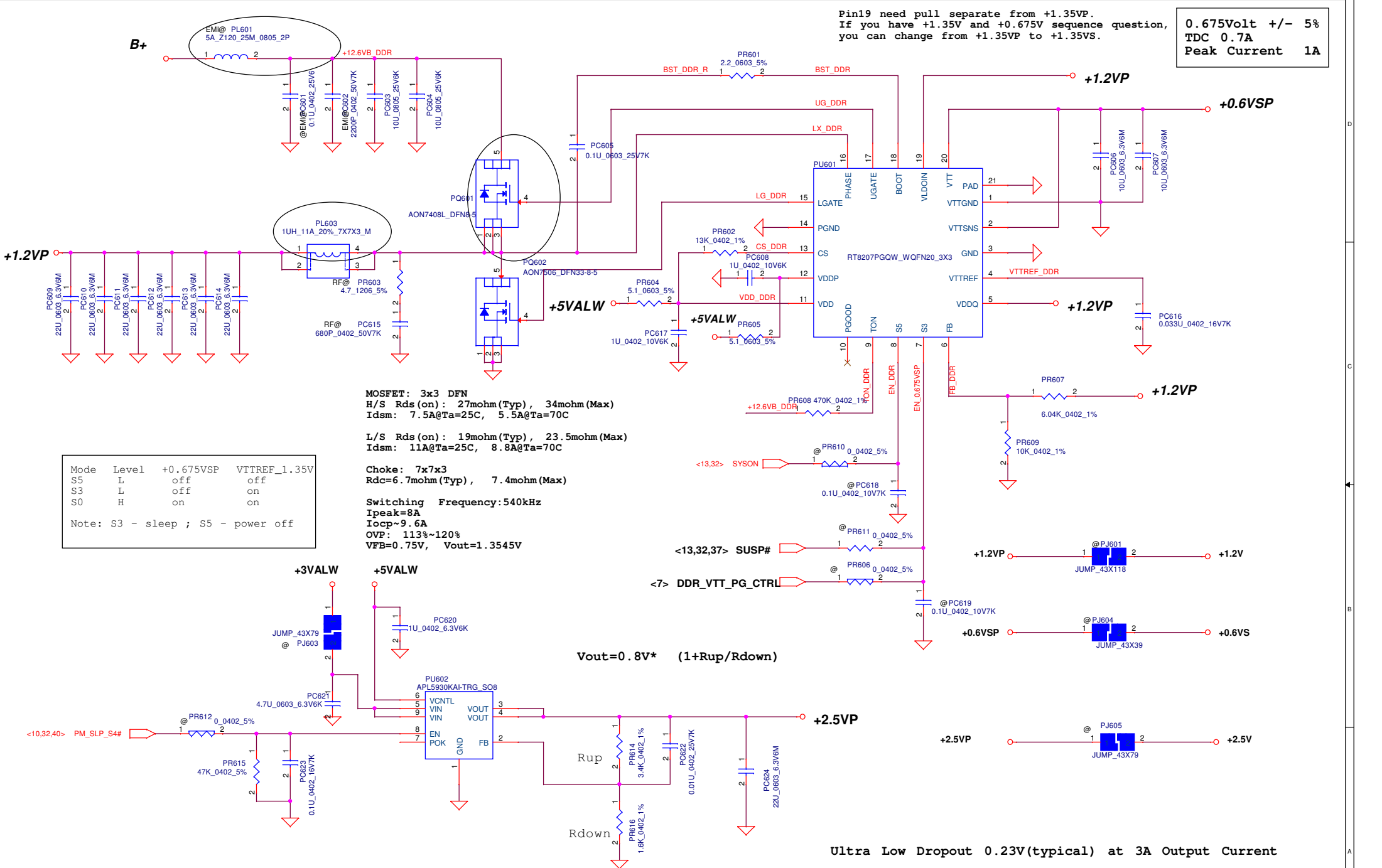
+5VALWP

+5VLP

+19VB\_5V

VCIN1\_BATT\_DROP <32>

| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                          |
|---|------------|--------------------|------------|--------------------------|--------------------------|
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | Title                    | +3VALW/+5VALW            |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | Size                     | Document Number          |
|   |            |                    |            | Custom                   | KBL                      |
|   |            |                    |            | Date                     | Wednesday, June 21, 2017 |
|   |            |                    |            | Sheet                    | 41 of 51                 |
|   |            |                    |            | Rev                      | 2A                       |



Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A

|      |       |           |              |
|------|-------|-----------|--------------|
| Mode | Level | +0.675VSP | VTTREF_1.35V |
| S5   | L     | off       | off          |
| S3   | L     | off       | on           |
| S0   | H     | on        | on           |

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN  
H/S Rds(on): 27mohm(Typ), 34mohm(Max)  
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 19mohm(Typ), 23.5mohm(Max)  
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

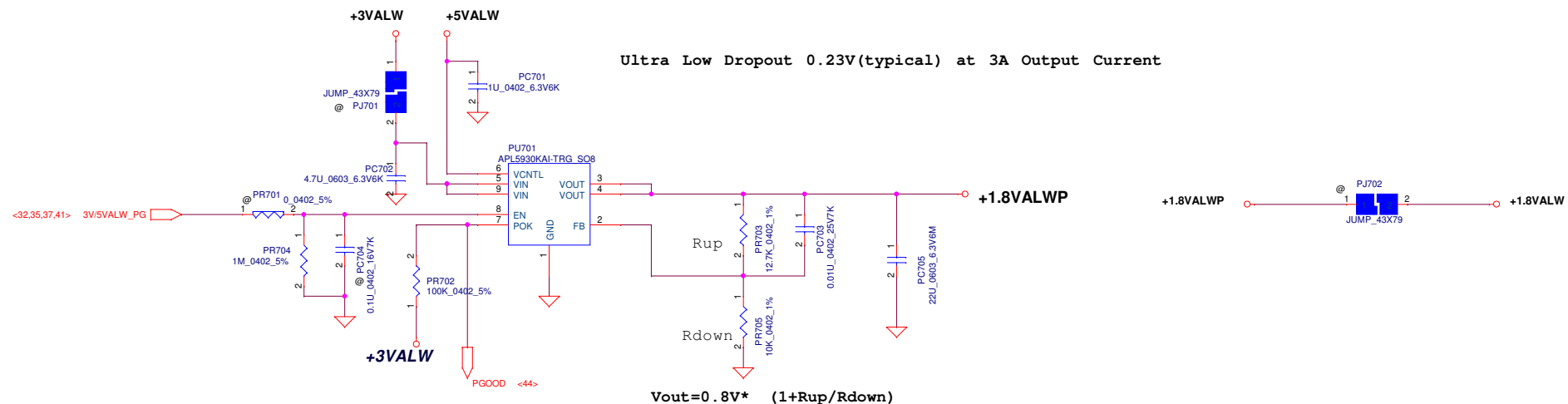
Choke: 7x7x3  
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency: 540kHz  
Ipeak=8A  
Iocp~9.6A  
OVP: 113%~120%  
VFB=0.75V, Vout=1.3545V

|   |            |                    |            |                          |                          |
|---|------------|--------------------|------------|--------------------------|--------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                          |
| Issued Date   | 2017/06/05 | Deciphered Date    | 2018/06/05 | Title                    | RT8207P                  |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |            |                    |            | Size                     | Document Number          |
|   |            |                    |            | Custom                   | KBL                      |
|   |            |                    |            | Date:                    | Wednesday, June 21, 2017 |
|   |            |                    |            | Sheet                    | 42 of 51                 |

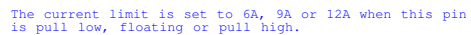
# Module model information

APL5930\_V2.mdd

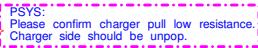


|   |                    |                 |            |                                |                |
|---|--------------------|-----------------|------------|--------------------------------|----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc.       |                |
| Issued Date   | 2017/06/05         | Deciphered Date | 2018/06/05 | Title                          | APL5930        |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |                 |            | Size Document Number           | Rev 2A         |
|   |                    |                 |            | Customer                       | KBL            |
|   |                    |                 |            | Date: Wednesday, June 21, 2017 | Sheet 43 of 51 |

SY8286\_V1\_single.mdd  
SY8286\_V1\_dual.mdd

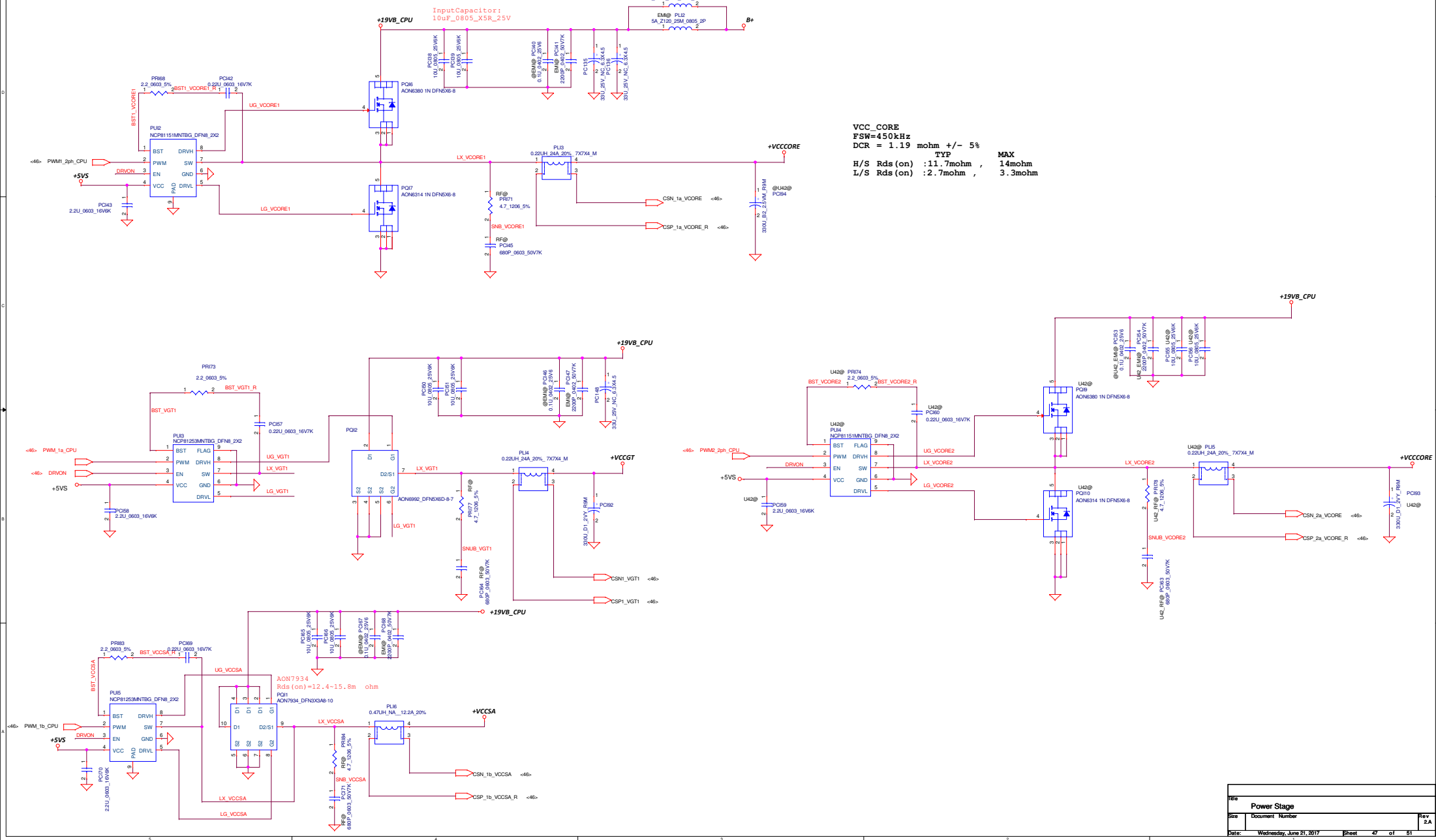


|   |                    |  |                 |                                 |  |       |                          |       |
|---|--------------------|--|-----------------|---------------------------------|--|-------|--------------------------|-------|
| Security Classification   | Compal Secret Data |  |                 | <b>Compal Electronics, Inc.</b> |  |       |                          |       |
| Issued Date   | 2017/06/05         |  | Deciphered Date | 2018/06/05                      |  | Title | <b>SY8286</b>            |       |
| THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. |                    |  |                 |                                 |  | Size  | Document Number          | Rev   |
|   |                    |  |                 |                                 |  | C     | KBL                      | 2A    |
|   |                    |  |                 |                                 |  | Date: | Wednesday, June 21, 2017 | Sheet |



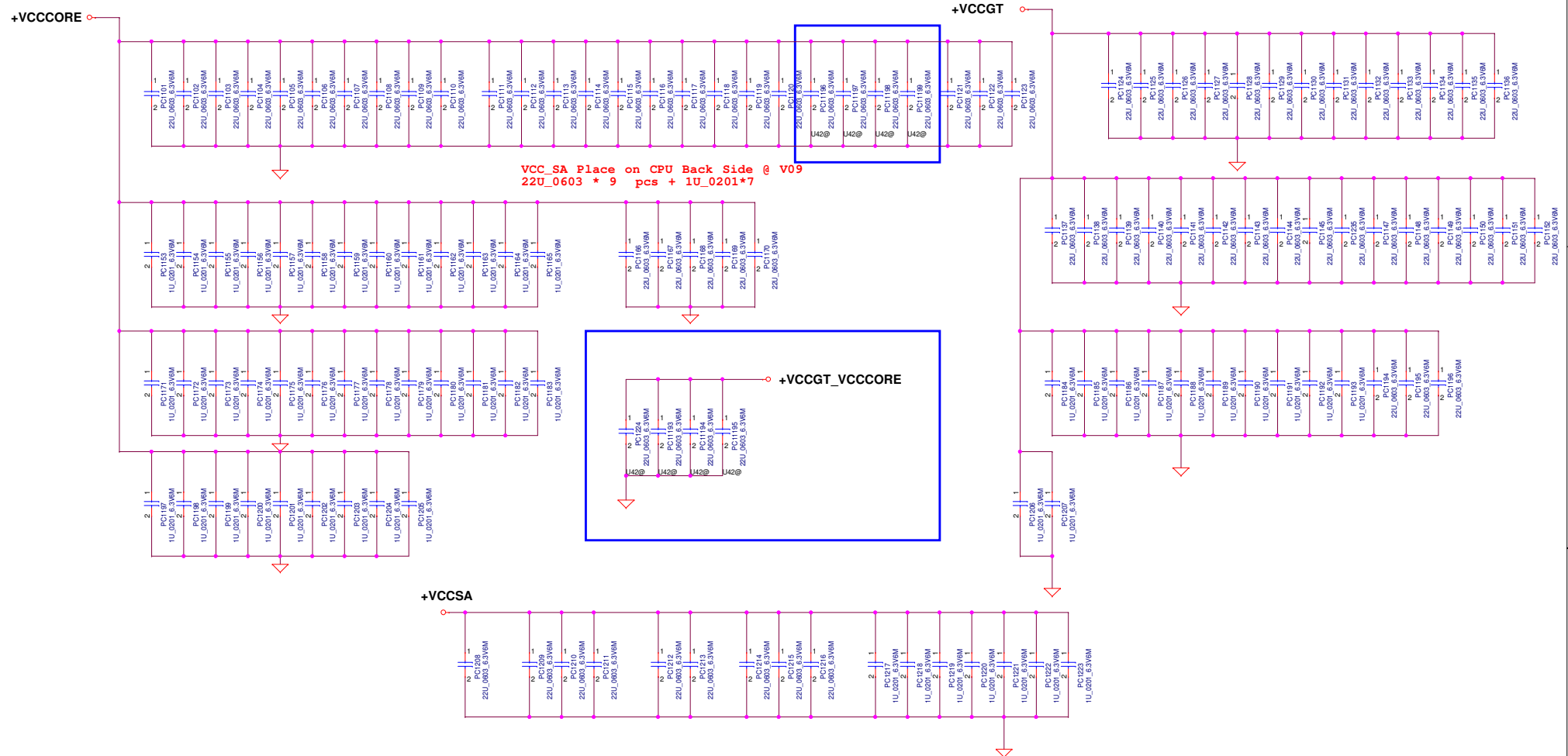
|                                |                 |    |       |
|--------------------------------|-----------------|----|-------|
|                                |                 |    |       |
| Title<br>NCP81218              |                 |    |       |
| Size                           | Document Number |    |       |
| Date: Wednesday, June 21, 2017 | Sheet           | 46 | of 51 |

| CPU | POWER | STAGES |
|-----|-------|--------|
|-----|-------|--------|



VCC\_CORE Place on CPU Back Side @ V09  
22U\_0603 \* 36pcs +1U\_0201\*35 pcs

VCC\_GT Place on CPU Back Side @ V09  
22U\_0603 \* 32 pcs +1U\_0201\*12 pcs



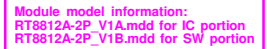
| PWM-VID Spec       | Config A | Config B | Config C |
|--------------------|----------|----------|----------|
| Vmin               | 0.6V     | 0.6V     | 0.65V    |
| Vmax               | 1.2V     | 1.2V     | 1.15V    |
| Vboot              | 0.875V   | 0.9V     | 0.9V     |
| Voltage step       | 6.25mV   | 6.25mV   | 25mV     |
| N of Voltage steps | 96       | 96       | 20       |
| Prf8               | 39K      | 20K      | 39K      |
| Prf7               | 39K      | 20K      | 30K      |
| Prf10              | 1.5K     | 2K       | 3K       |
| Prf20              | 30K      | 18K      | 24K      |
| Prf21              | 30K      | 0        | 3K       |
| PC9                | 1.5m     | 2.7m     | 1.8m     |

```

Rl=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rl/(Rref1+Rl)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

```

VGA@ PR1468 Pull high on HW side  
1K 0402 5%



+VGA\_CORE  
EDP-Continuous 26.5A  
EDP-Peak 53A  
OCP min 66.4A

**+VGA\_CORE** Under GPU Core **GB4-128 package**

$$V_{out} = 0.6V * (1 + R_1/R_2)$$
$$= 0.6 * (1 + (12.4/10))$$
$$V_{out} = 1.344V$$

|  |                          |                 |                           |          |
|--|--------------------------|-----------------|---------------------------|----------|
| Security Classification  | Compal Secret Data       |                 | Title                     |          |
| Issued Date  | 2017/06/05               | Deciphered Date | 2018/06/05                |          |
| <p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAQ ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT OF COMPAQ ELECTRONICS, INC. NEITHER THE SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAQ ELECTRONICS, INC.</p> |                          |                 | <p><b>PWR-CPU_GFX</b></p> |          |
| Size   | Document                 | Number          | Rev                       |          |
| Quantity   | KBL                      |                 | 2A                        |          |
| Date   | Wednesday, June 21, 2017 |                 | Sheet                     | 48 of 51 |