ZZZ PCB@

PCB 1Q3 LA-D821P REV1 M/B 1

DA80017D010

UC1 KBL_15W_2+2@

S IC A31 FJ8067702739720 QKKS G0 2.4G

SA00009PJ0L

UC1 SKL_15W@

S IC FJ8066201931104 SR2EU D1 2.3G A31!

SA000092N4L

UC1 KBL_15W_I3@

SA0000A382L

KBL_U_SR2VN

S IC FJ8067702739738 SR2VN H0 2.4G A31!

UC1 KBL_15W_I5@

SA0000A372L

KBL_U_SR2VL

S IC FJ8067702739739 SR2VL H0 2.5G A31!

UC1 KBL_15W_I7@

SA0000A342L

KBL_U_SR2VM

S IC FJ8067702739740 SR2VM H0 2.7G A31!

UC1 KBL_15W_2+1@

S IC A31 FJ8067702739920 QKKQ G0 1.7G

SA00009QM0L

UC1 KBL_15W_SUP_ES@

S IC A31 FJ8067702739718 QKJW G0 2.6G

SA00009UR0L

Compal Confidential

BKA50 / BKA40 / BKD50 / BKD40

MB Schematic Document

LA-D821P

Rev: 1.0

2016.05.30

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Title	Cover Page	
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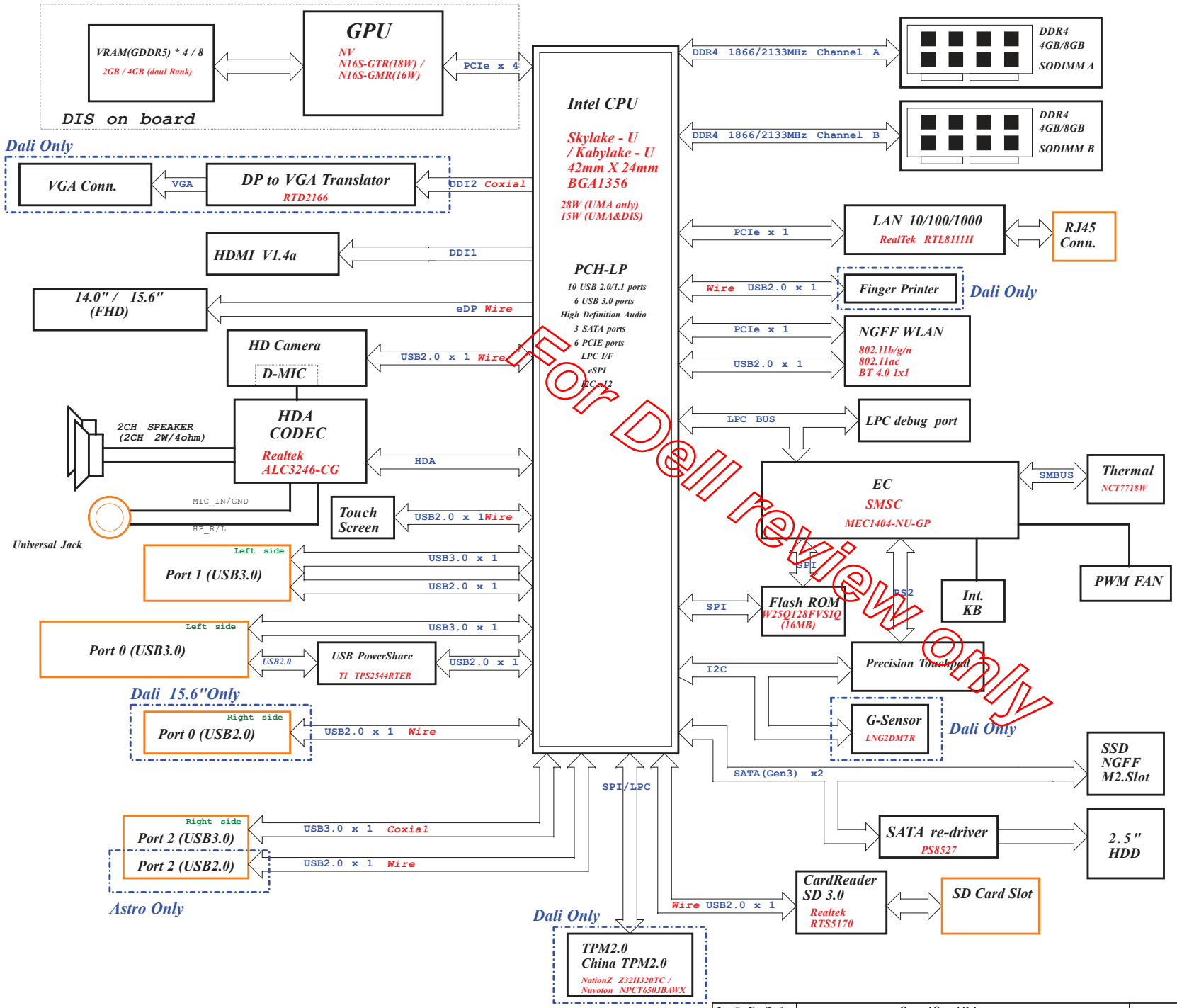

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

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Title: SKL-U 2+2 Block Diagrams

Size	Document Number	Rev
Custom	LA-D821P	0.1

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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB3.0 Port0
2	USB3.0 Port1
3	USB3.0 Port2 (IO Board)
4	USB2.0 Port0
5	HD CAM
6	Card Reader
7	Touch Screen
8	BT
9	Finger Printer
10	N/A

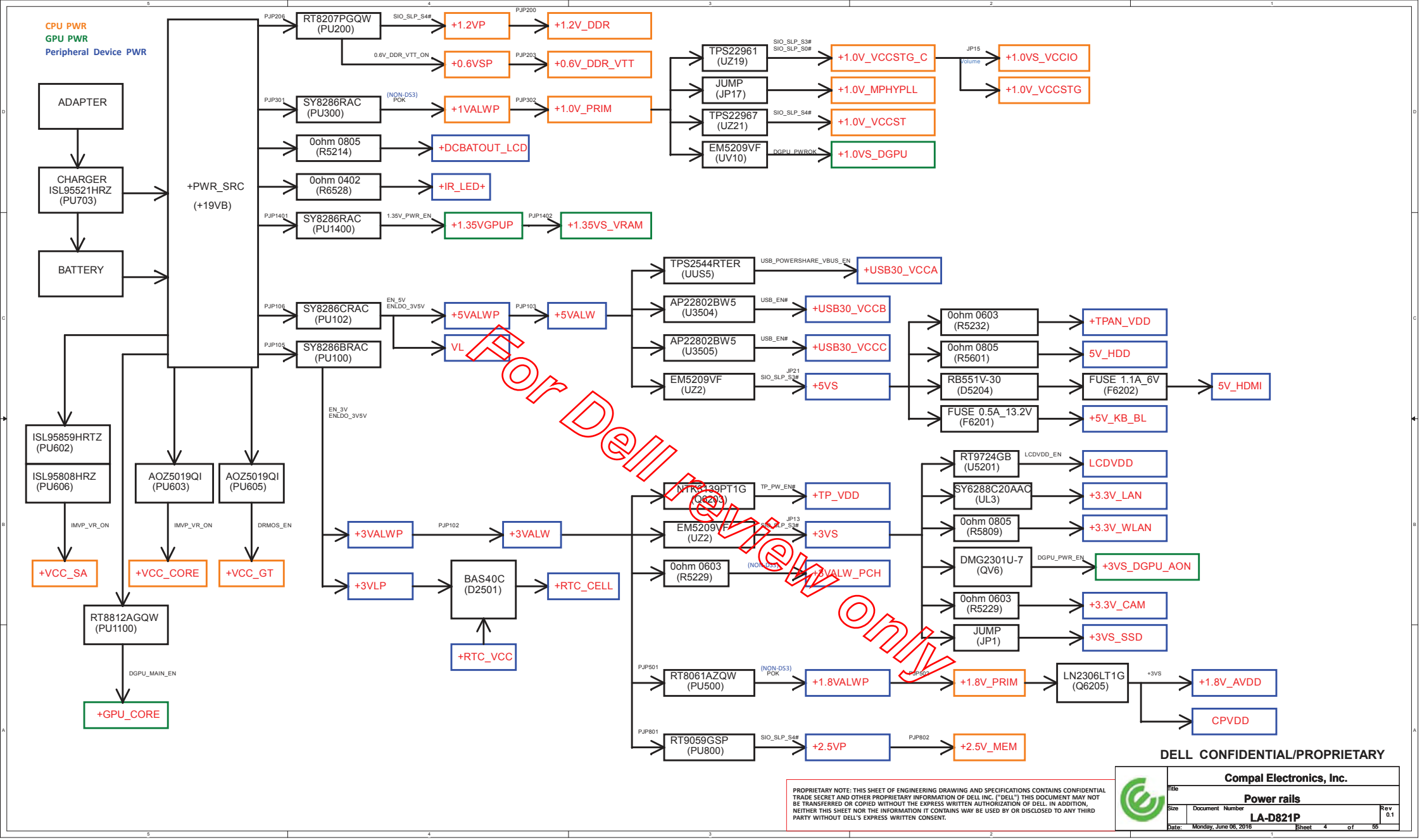
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port0
USB3.0-2	SSIC-1			USB3.0 Port1
USB3.0-3	SSIC-2			USB3.0 Port2 (IO Board)
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		WLAN
		PCIE-6		GLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	N/A
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	SATA SSD

PM TABLE

power plane / State	+RTC_CELL +RTC_VCC +3VLP +19VB	+1.0V_PRIM +1.0V_MPHYPLL +5VALW +3VALW +3.3V_ALW_DSW +1.8V_PRIM	+1.0V_VCCST +1.2V_DDR +2.5V_MEM +3VALW_PCH	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VCC_CORE +GPU_CORE +5VS +3VS +1.8VS +0.6V_DDR_VTT
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	OFF	OFF
S4&S5 / DC	ON	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down(K ohm)	Pull-up (K ohm)	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT(X00)
2	100	13.7	2.902	DVT1(X01)
3	100	17.8	2.801	DVT2(X02)
4	100	22.1	2.703	Pilot(A00)
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	



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Title: Power rails

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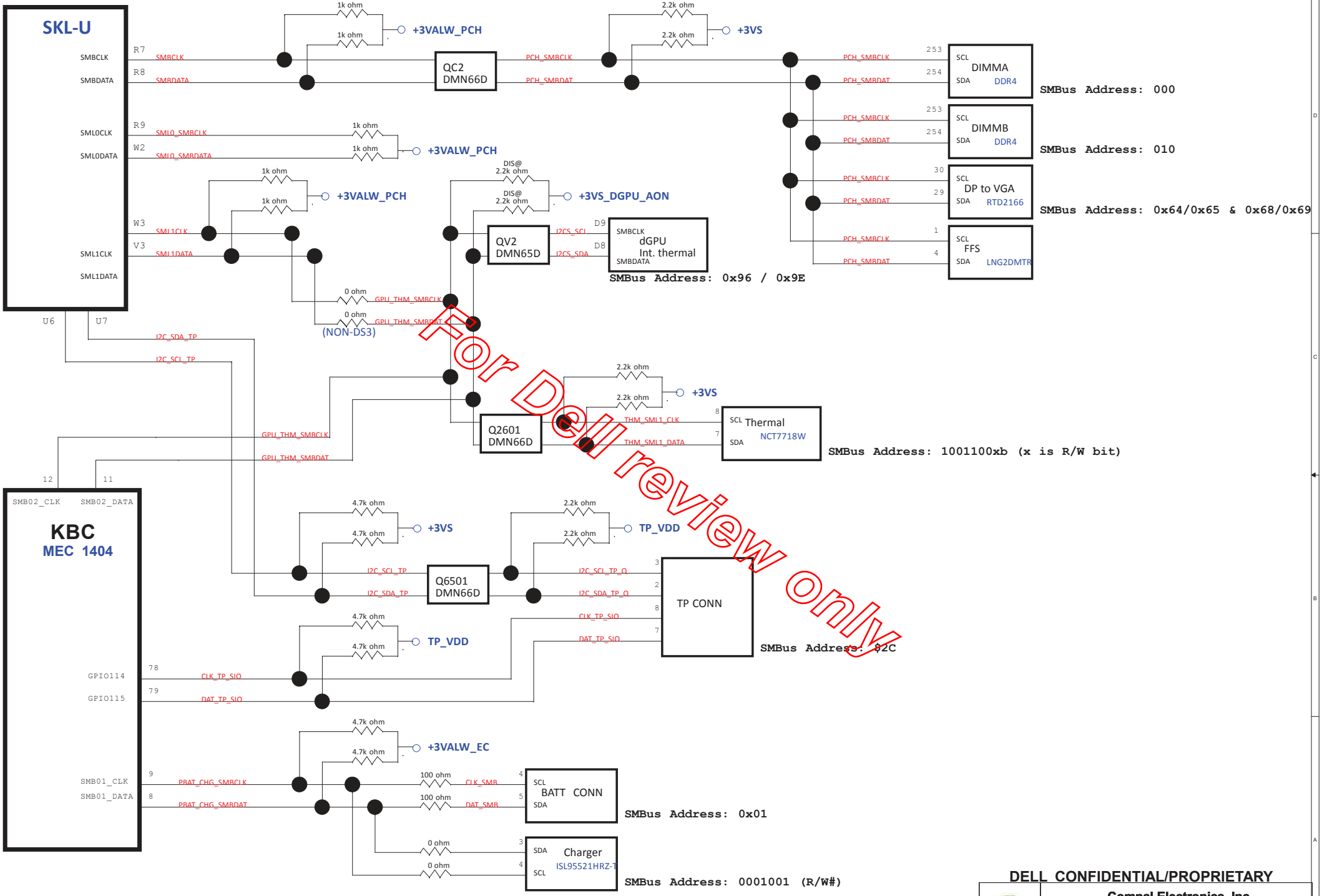

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Title: SMbus Block diagram

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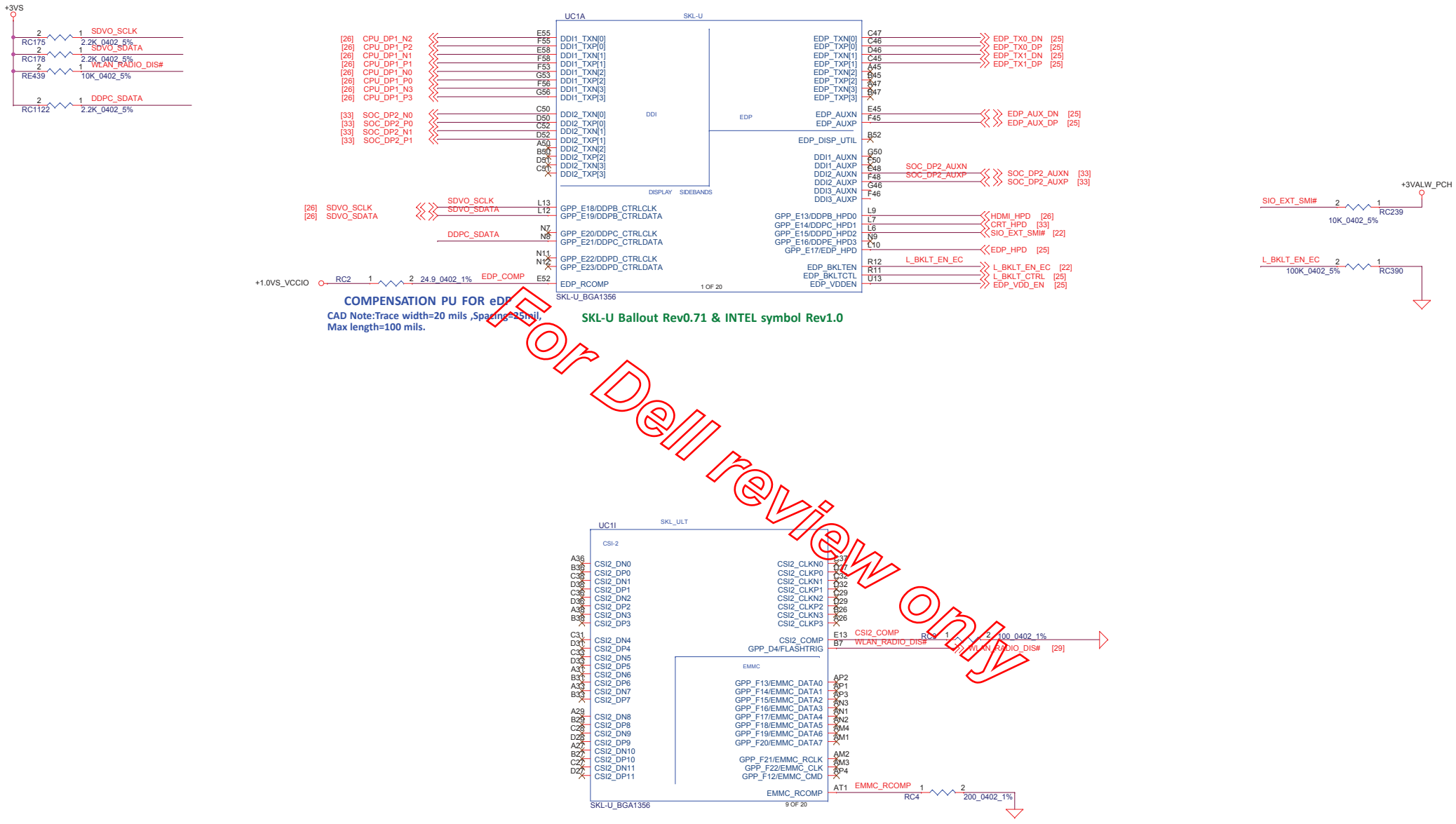

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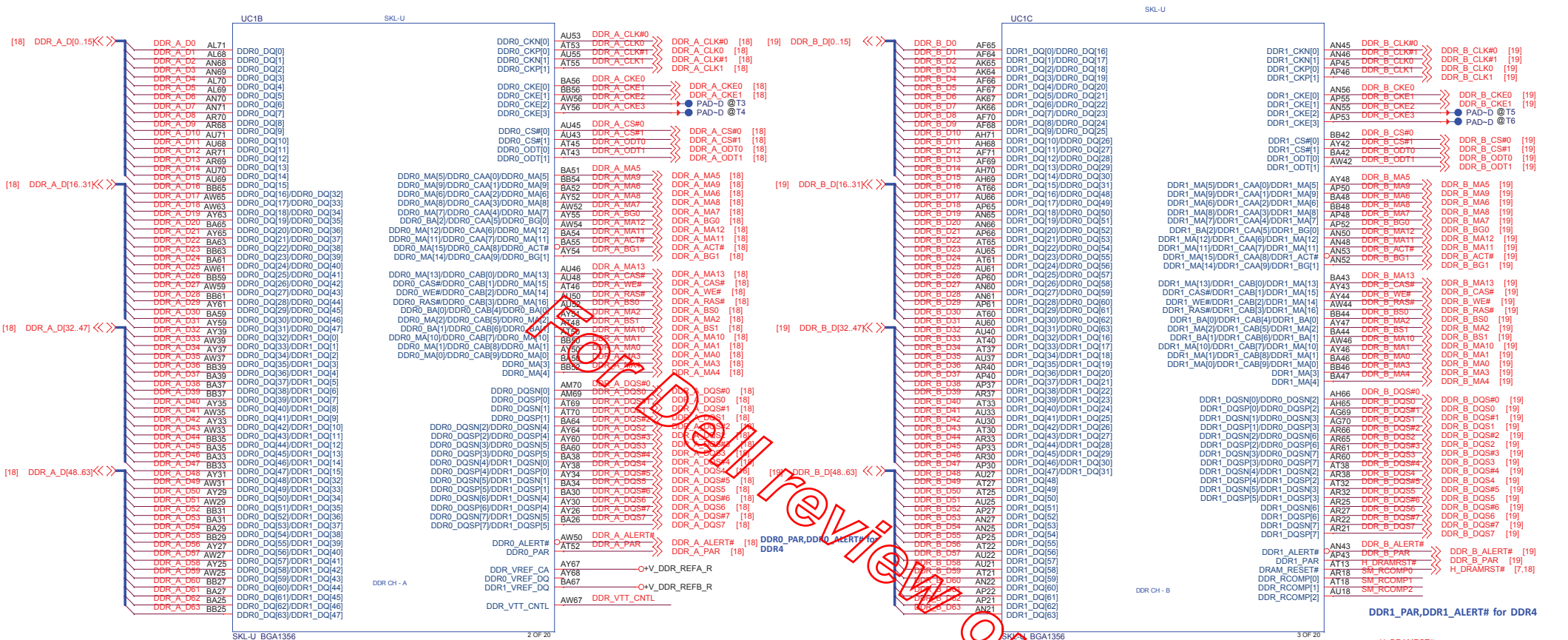
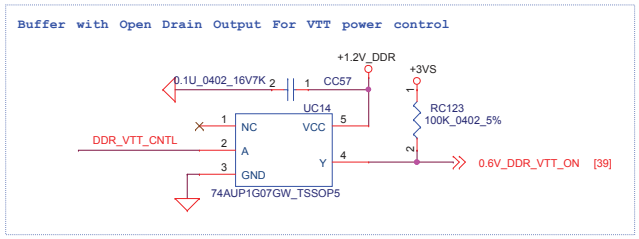
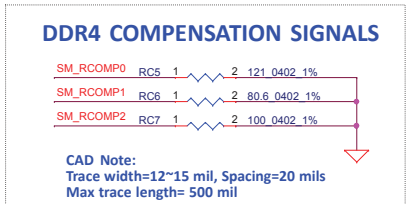
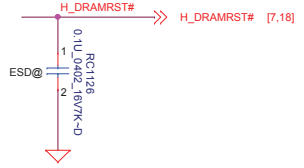
DDR4, Ballot for B2B(Interleave)









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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

SMB -> DDR,CRT,FFS

SML1 -> EC,DGPU,THM

Single SPI ROM_CS0#

16M SPI ROM (Confirmed by BIOS RD)

Layout need meet L1 = L2 = L3

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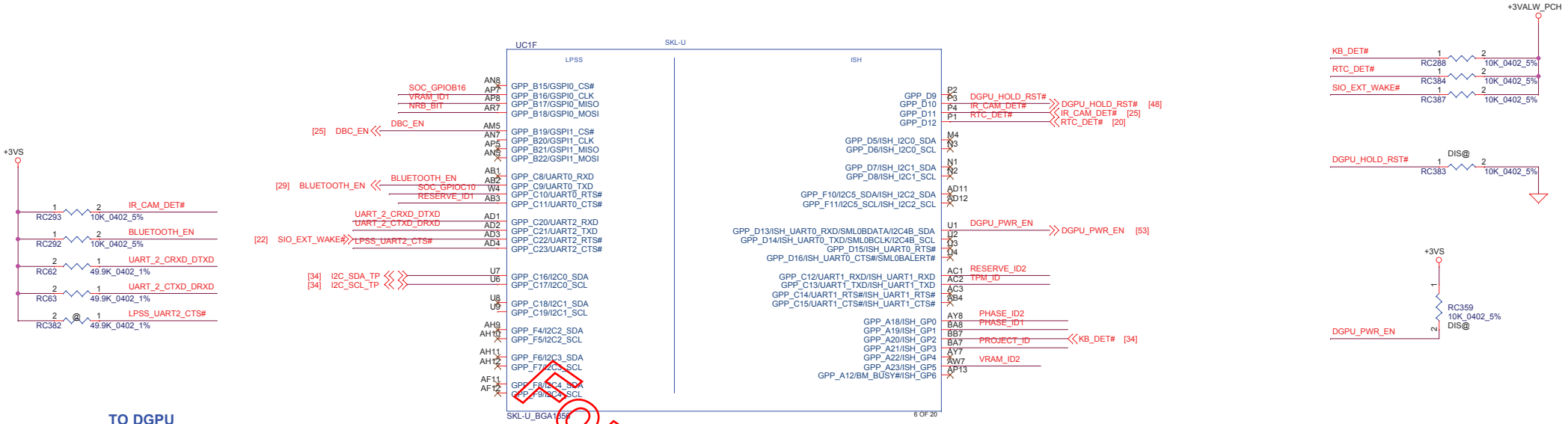
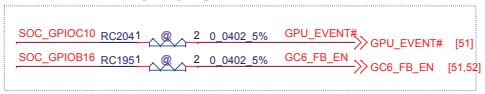
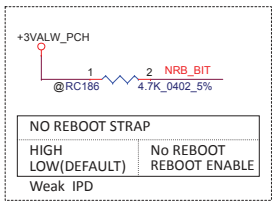


TO DGPU



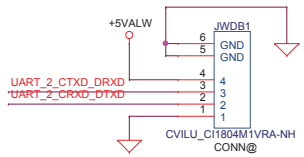


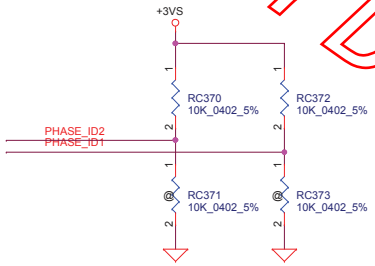
NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Weak IPD

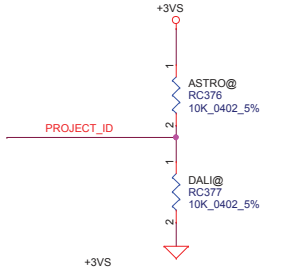
Win7 Debug solution

Option 2 : For Open Chassis Platforms

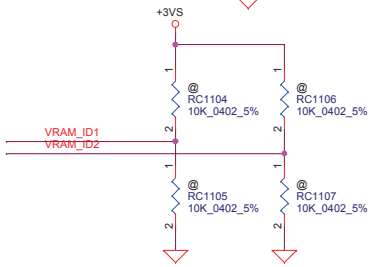




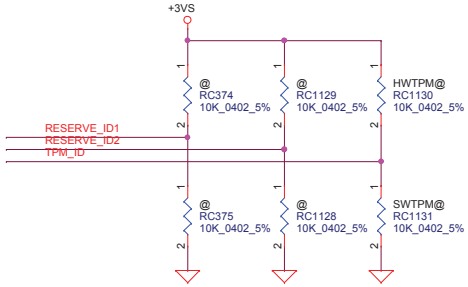
PHASE_ID	PHASE_ID1 (GPP_A19)	PHASE_ID2 (GPP_A18)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1



PROJECT ID	PROJECT_ID (GPP_A21)
Dali	0
Astro	1



VRAM ID (PCBA VRAM Size Config.)	VRAM_ID2 (GPP_A23)	VRAM_ID1 (GPP_B17)
UMA	0	0
2G	0	1
4G	1	0
Reserved	1	1



PROJECT ID	TPM_ID (GPP_C13)
SW_TPM	0
HW_TPM	1

RESERVE ID	RESERVE_ID1 (GPP_C11)	RESERVE_ID2 (GPP_C12)

RC1105 4G@ 10K_0402_5% SD028100280
RC1106 4G@ 10K_0402_5% SD028100280
RC1104 2G@ 10K_0402_5% SD028100280
RC1107 2G@ 10K_0402_5% SD028100280
RC1105 UMA@ 10K_0402_5% SD028100280
RC1107 UMA@ 10K_0402_5% SD028100280

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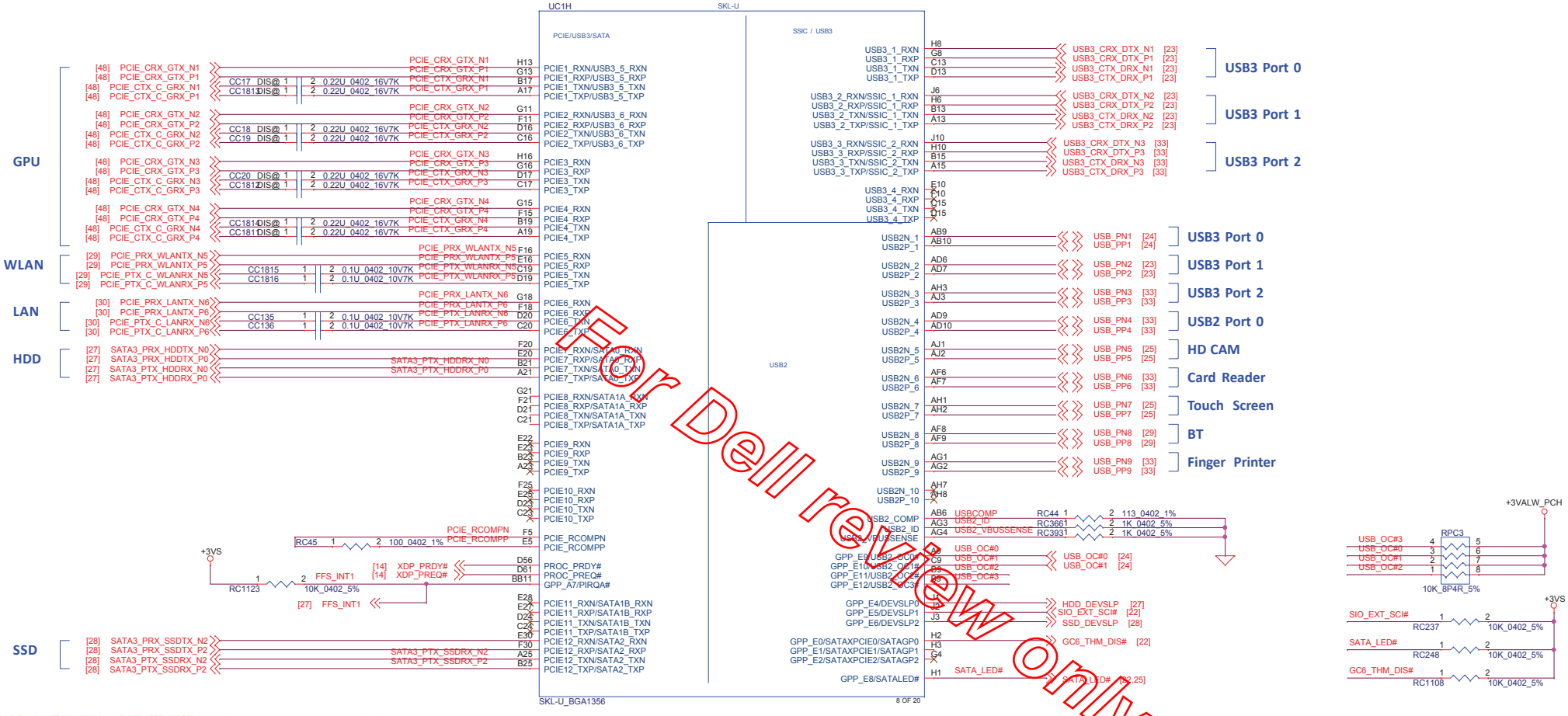
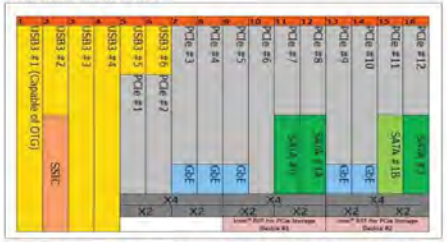


3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



There are 16 HSIO lanes on SKL PCH-LP U Series, supporting the following port configurations:

1. Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
   - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
   - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as 4x1, 2x2, 1x2 + 2x1, or 1x4.
2. Up to 3 SATA ports (multiplexed with PCIe*)
   - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
3. Up to 6 USB 3.0 ports (multiplexed with PCIe*)
   - USB Dual Role (OTG) capability is available on USB 3.0 Port 1
   - One SSIC x1 port is multiplexed with USB 3.0 Port 2
4. One GbE lane
   - GbE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10
   - When GbE is enabled, there can be at most up to 5 PCIe* ports enabled.
5. Up to 2 Intel RST for PCIe* storage devices supported
   - [illegible] x2 or [illegible]
   - [illegible] implementation [illegible] SATA controller

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

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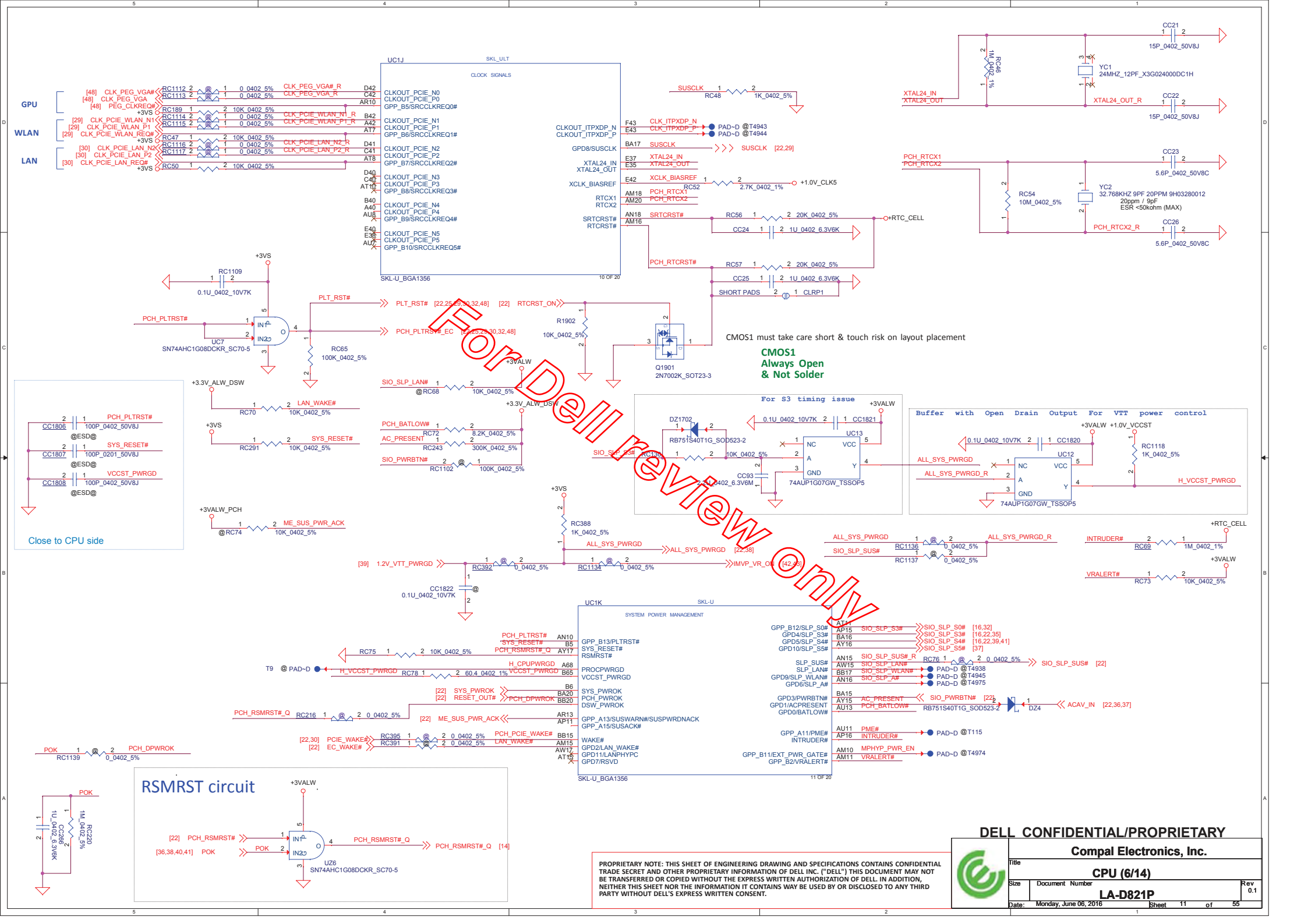
GPU
WLAN
LAN
UC1J
SKL_ULT
CLOCK SIGNALS
SKL-U_BGA1356
10 OF 20
CLK_PEG_VGA#_R
CLK_PEG_VGA_R
CLK_PCIE_WLAN_N1_R
CLK_PCIE_WLAN_P1_R
CLK_PCIE_LAN_N2_R
CLK_PCIE_LAN_P2_R
SUSCLK
XTAL24_IN
XTAL24_OUT
XTAL24_OUT_R
YC1
24MHZ_12PF_X3G024000DC1H
PCH_RTCX1
PCH_RTCX2
PCH_RTCX2_R
YC2
32.768KHZ 9PF 20PPM 9H03280012
20ppm / 9pF
ESR <50kohm (MAX)
SRTCRST#
PCH_RTCRST#
+RTC_CELL
SHORT PADS
CLRP1
PLT_RST#
PCH_PLTRST#
PCH_PLTRST#_EC
RTCRST_ON
Q1901
2N7002K_SOT23-3
CMOS1 must take care short & touch risk on layout placement
CMOS1
Always Open
& Not Solder
For S3 timing issue
Buffer with Open Drain Output For VTT power control
Close to CPU side
SIO_SLP_LAN#
LAN_WAKE#
SYS_RESET#
PCH_BATLOW#
AC_PRESENT
SIO_PWRBTN#
ME_SUS_PWR_ACK
ALL_SYS_PWRGD
ALL_SYS_PWRGD_R
SIO_SLP_SUS#
IMVP_VR_ON
1.2V_VTT_PWRGD
INTRUDER#
VRALERT#
H_VCCST_PWRGD
ACAV_IN
RSMRST circuit
PCH_RSMRST#
PCH_RSMRST#_Q
POK
PCH_DPWROK
PCIE_WAKE#
EC_WAKE#
PCH_PCIE_WAKE#
LAN_WAKE#
SYS_PWROK
RESET_OUT#
ME_SUS_PWR_ACK
UC1K
SKL-U
SYSTEM POWER MANAGEMENT
SKL-U_BGA1356
11 OF 20
SIO_SLP_S0#
SIO_SLP_S3#
SIO_SLP_S4#
SIO_SLP_S5#
SIO_SLP_SUS#_R
SIO_SLP_LAN#
SIO_SLP_WLAN#
SIO_SLP_A#
AC_PRESENT
PCH_BATLOW#
PME#
INTRUDER#
MPHYP_PWR_EN
VRALERT#
ACAV_IN
UC7
SN74AHC1G08DCKR_SC70-5
UC12
UC13
74AUP1G07GW_TSSOP5
DZ1702
DZ4
RB751S40T1G_SOD523-2
UZ6
SN74AHC1G08DCKR_SC70-5
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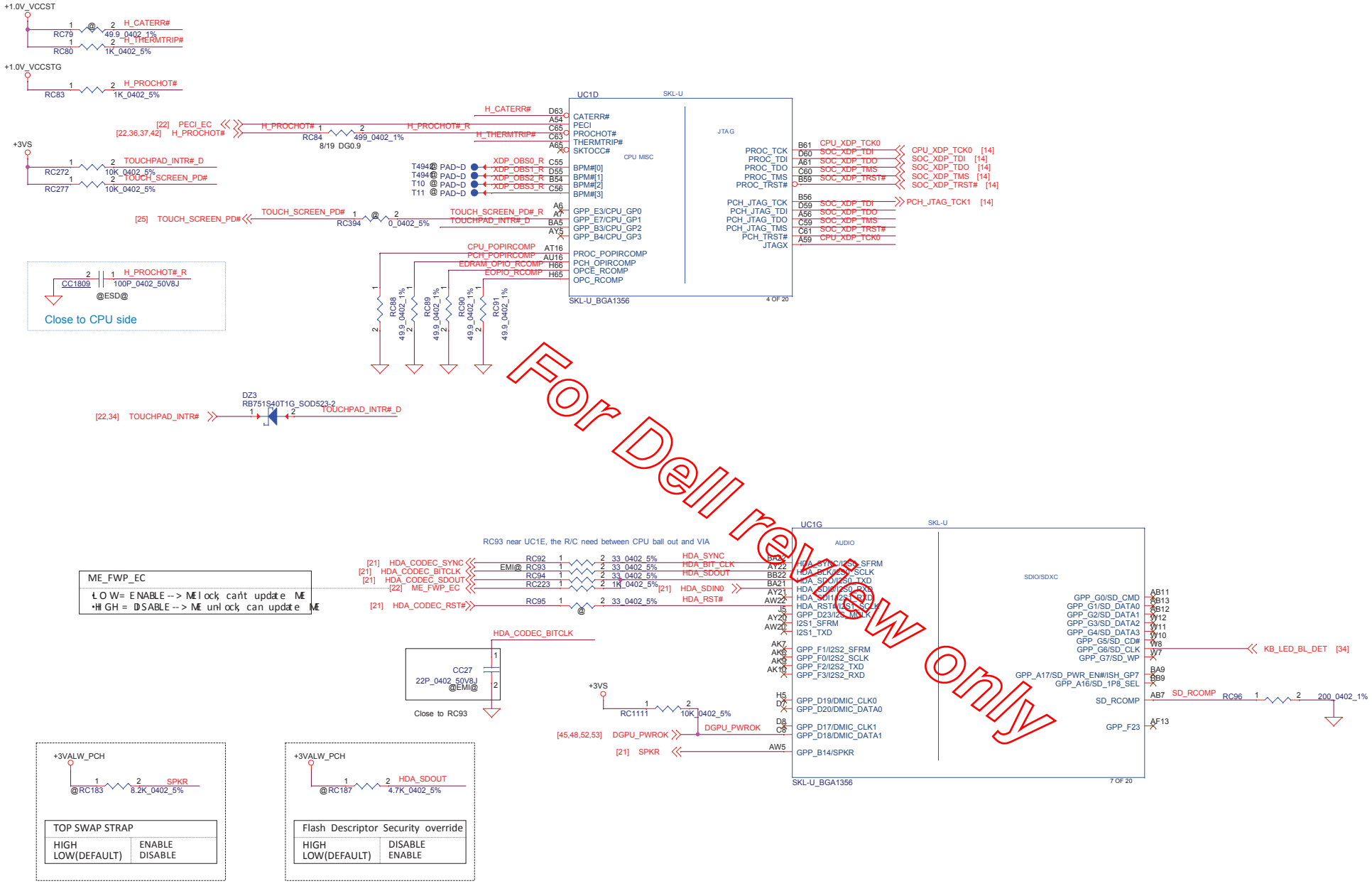

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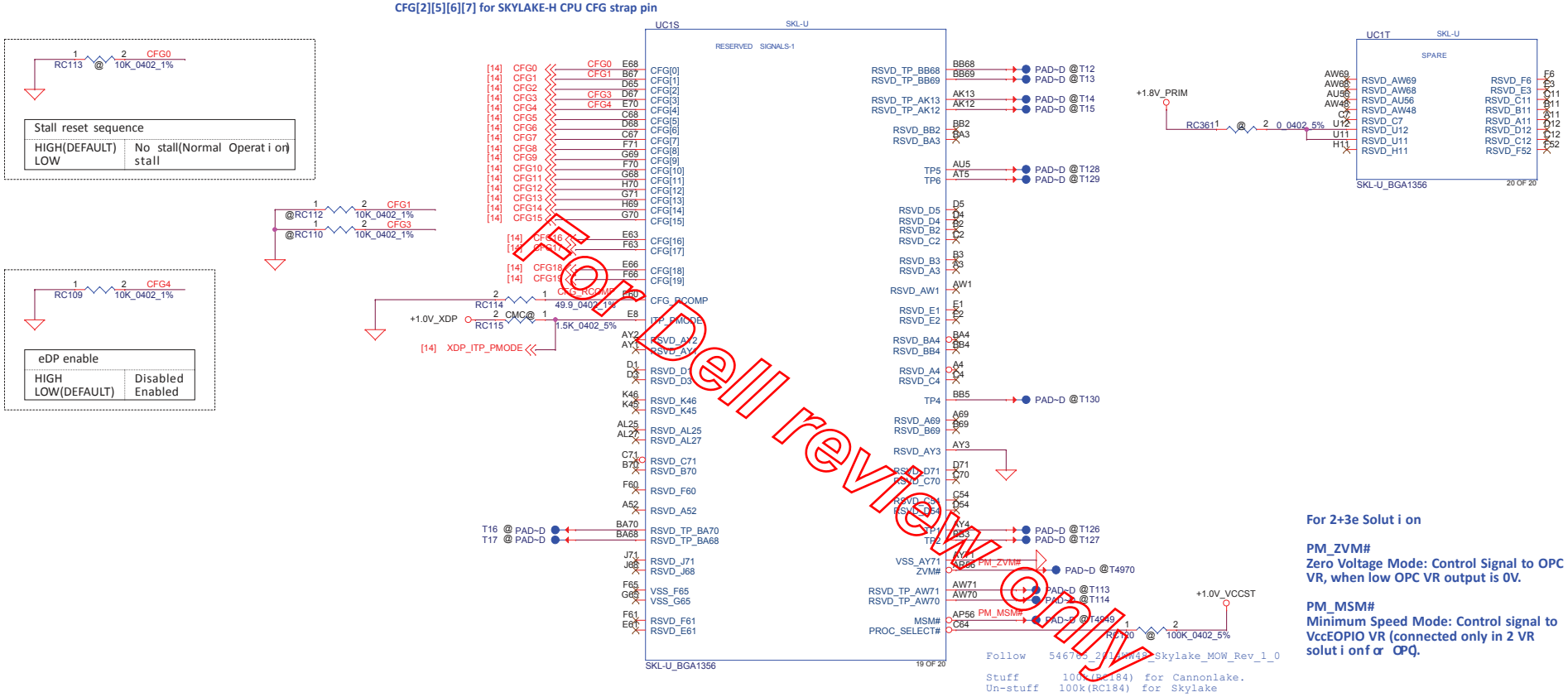

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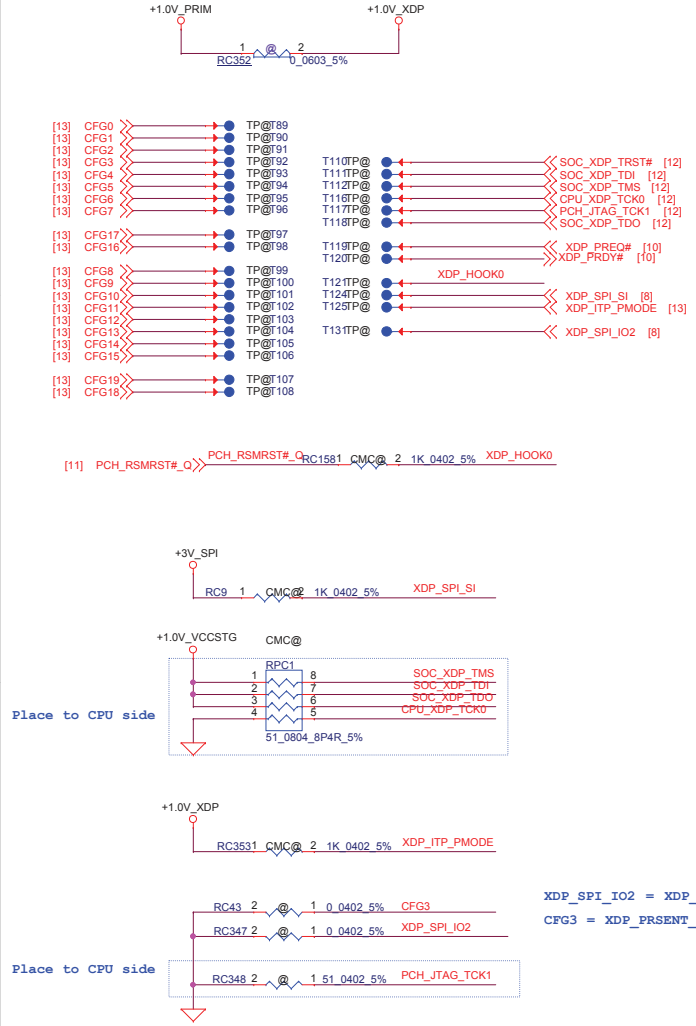
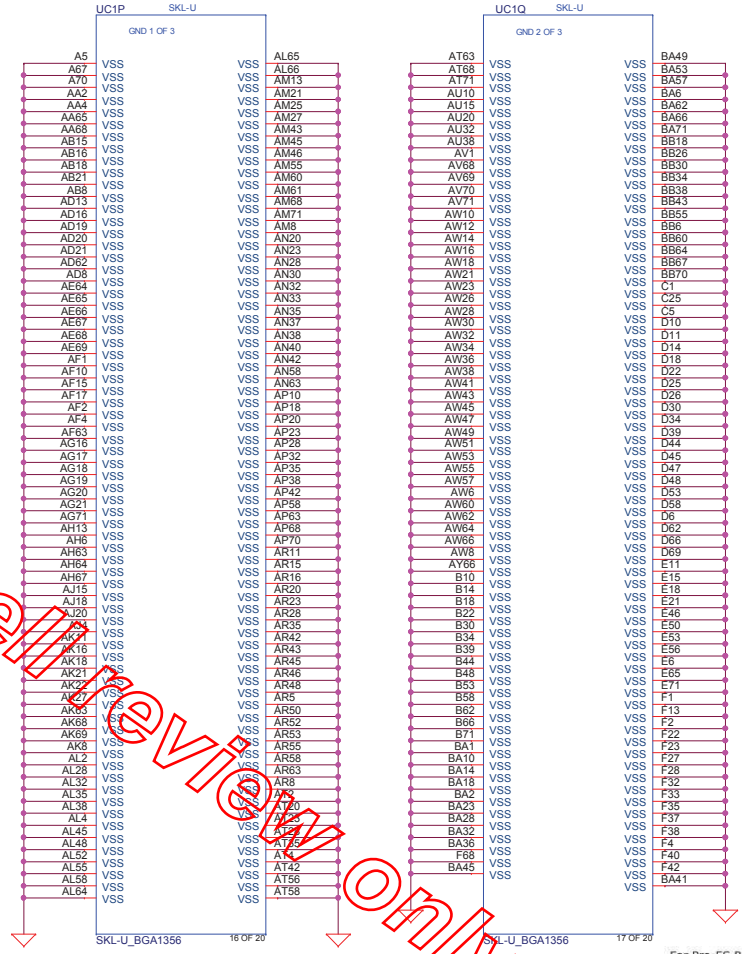
PRIMARY CMC CONN



XDP_SPI_IO2 = XDP_PRSENT_PCH

CFG3 = XDP_PRSENT_CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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Title: CPU (9/14)

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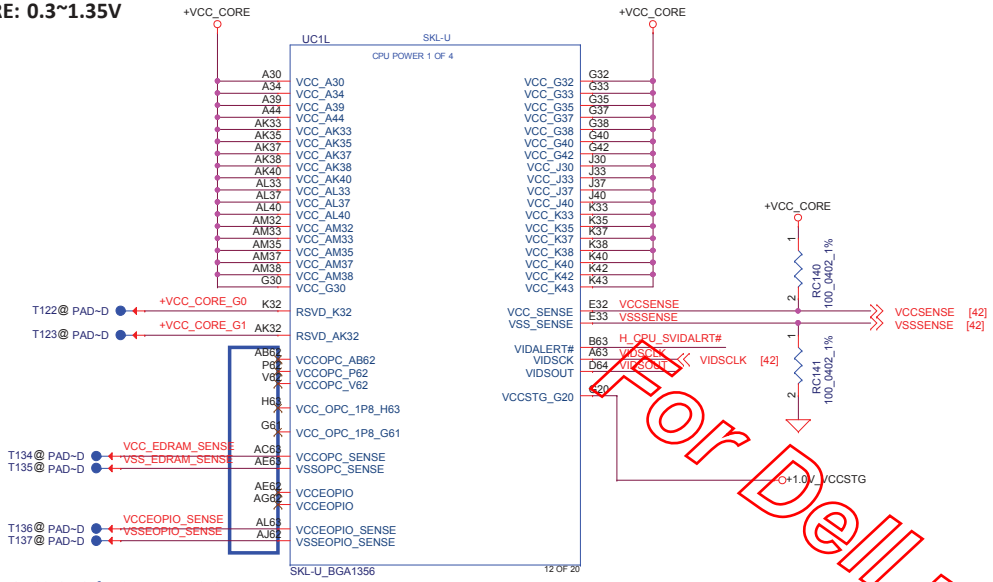
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

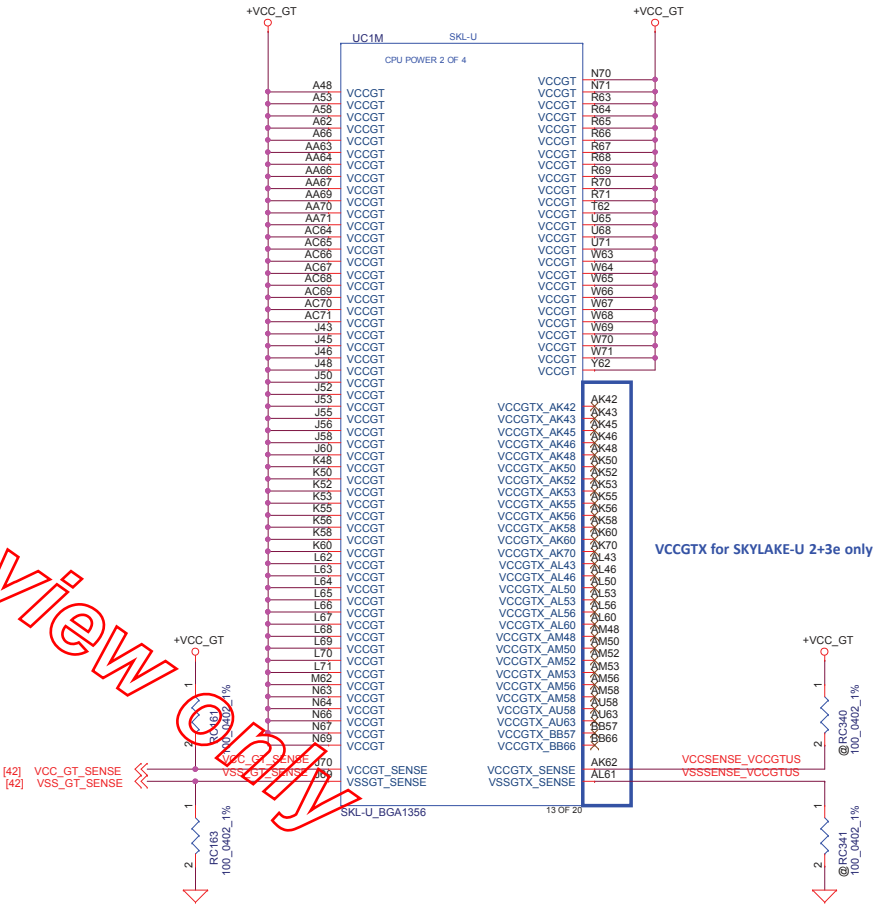
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

+VCC_CORE: 0.3~1.35V

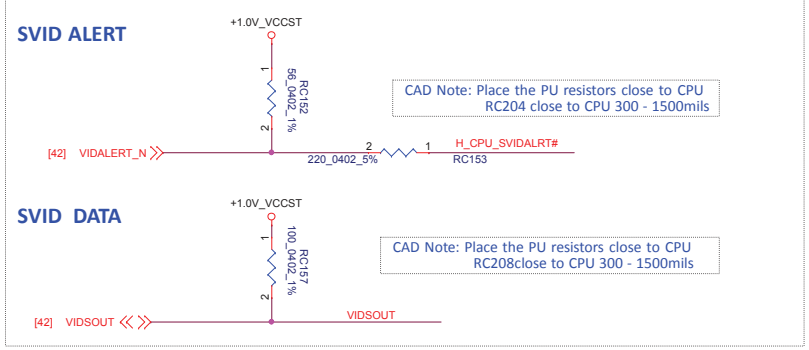


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



VCCGTX for SKYLAKE-U 2+3e only



Compal Electronics, Inc.

Title: CPU (10/14)

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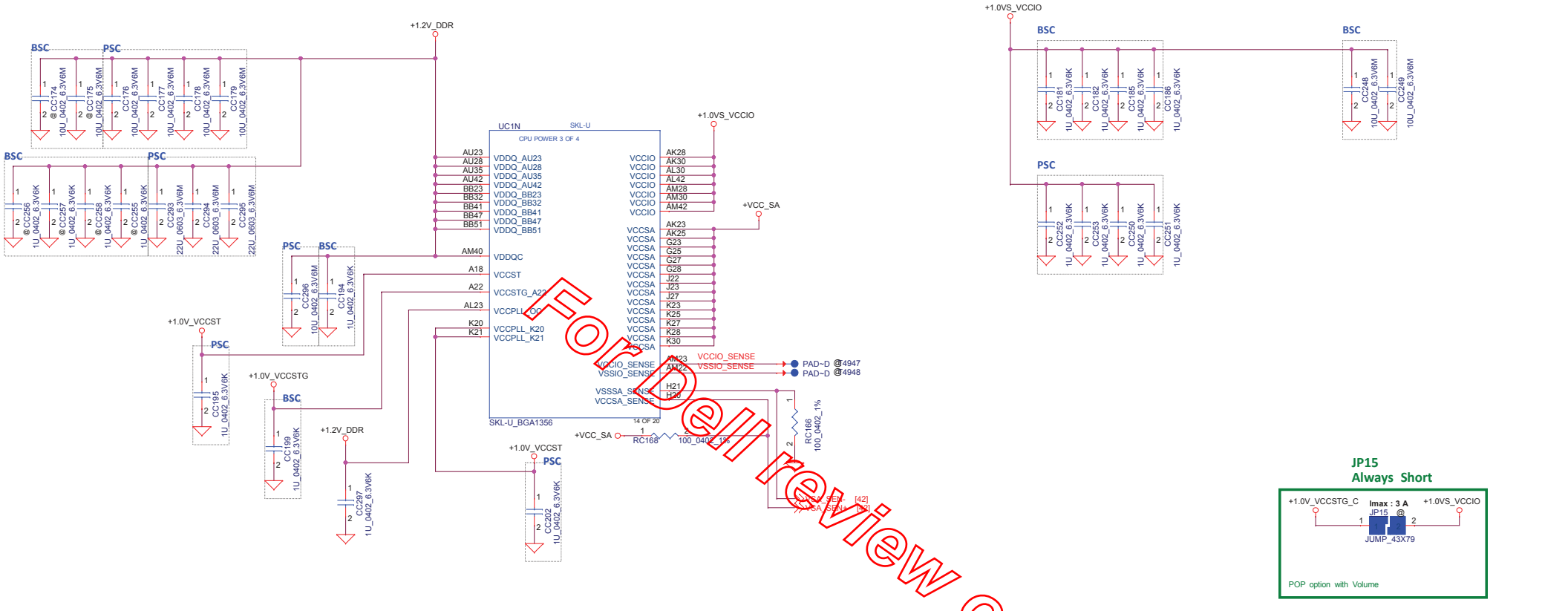
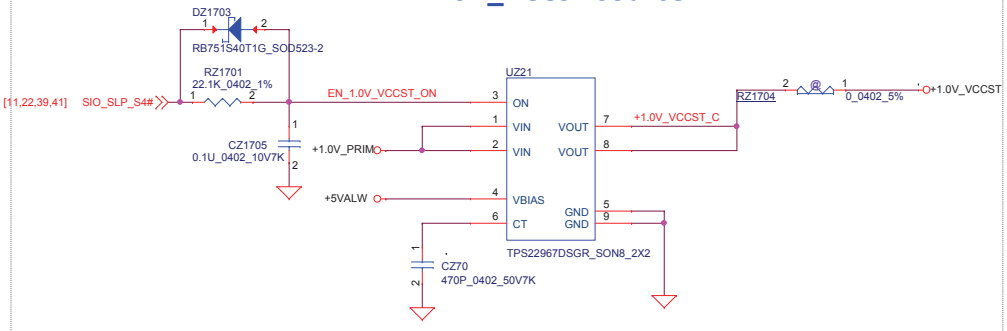
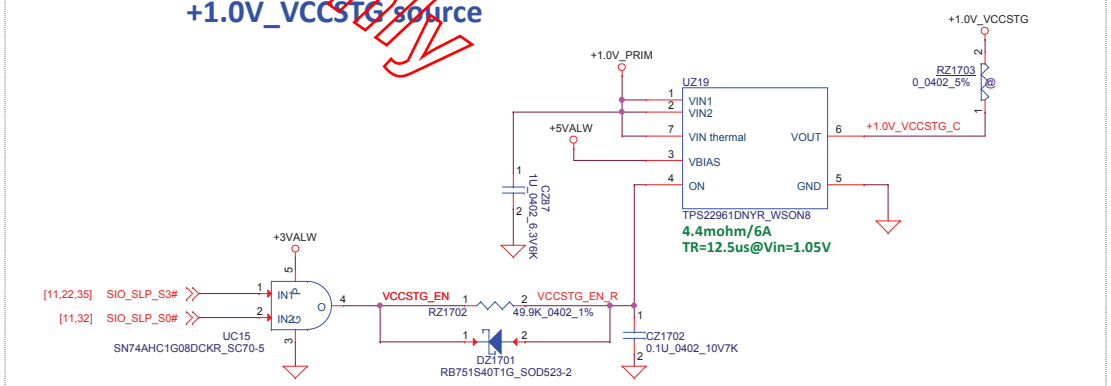


+1.0V_VCCST source



+1.0V_VCCSTG source

VCCSTG Imax: 0.16A



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Compal Electronics, Inc.

Title	CPU (12/14)	
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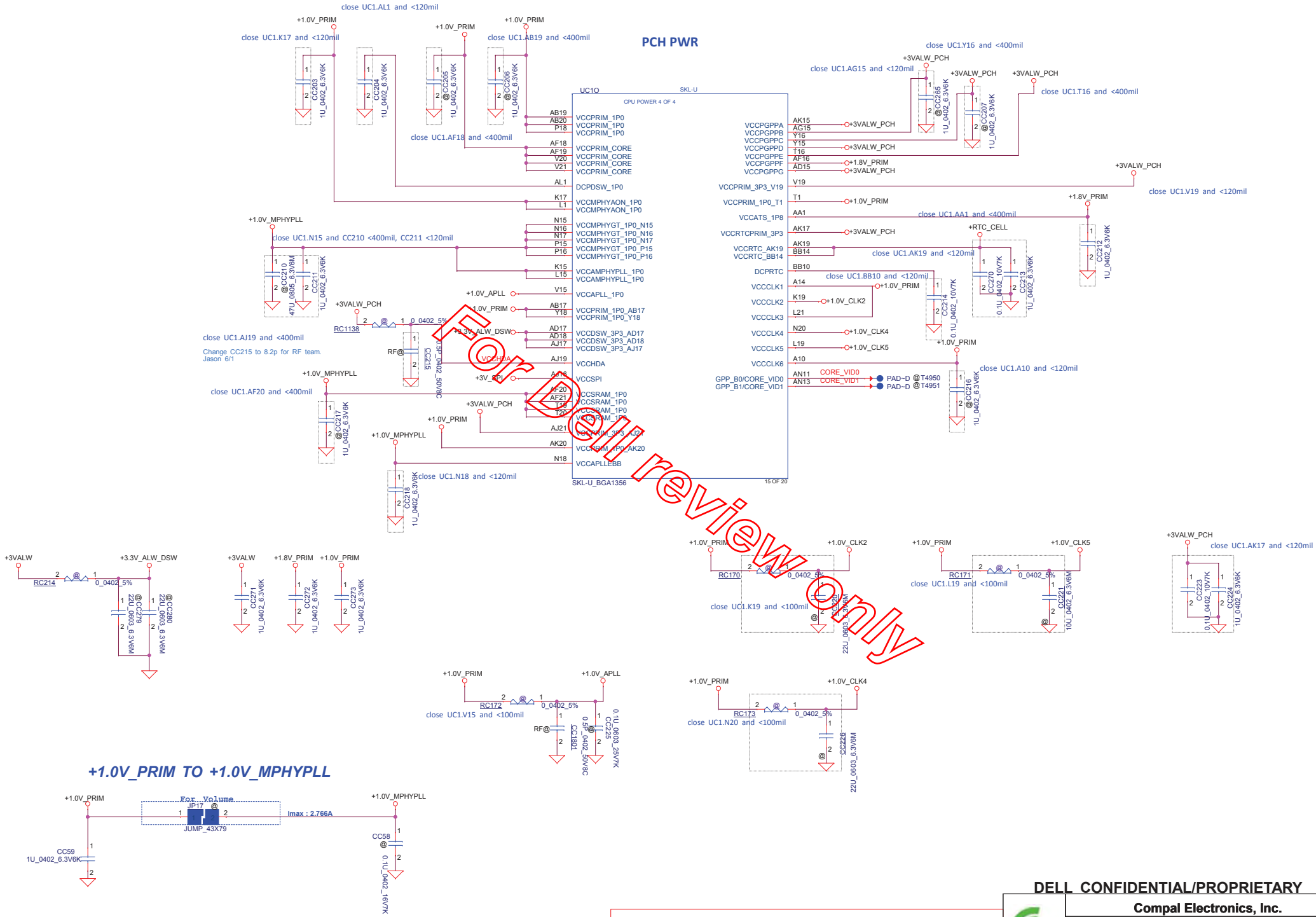
Date: Monday, June 06, 2016	Sheet 16 of 55	


PCH PWR
UC1O
SKL-U
CPU POWER 4 OF 4
SKL-U_BGA1356
15 OF 20
close UC1.AL1 and <120mil
close UC1.K17 and <120mil
close UC1.AB19 and <400mil
close UC1.AF18 and <400mil
close UC1.AG15 and <120mil
close UC1.Y16 and <400mil
close UC1.T16 and <400mil
close UC1.V19 and <120mil
close UC1.AA1 and <400mil
close UC1.AK19 and <120mil
close UC1.BB10 and <120mil
close UC1.A10 and <120mil
close UC1.N15 and CC210 <400mil, CC211 <120mil
close UC1.AJ19 and <400mil
Change CC215 to 8.2p for RF team.
Jason 6/1
close UC1.AF20 and <400mil
close UC1.N18 and <120mil
close UC1.AK17 and <120mil
close UC1.L19 and <100mil
close UC1.K19 and <100mil
close UC1.V15 and <100mil
close UC1.N20 and <100mil
+1.0V_PRIM TO +1.0V_MPHYPLL
Imax : 2.766A
JUMP_43X79
For Volume
For Dell review only
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Compal Electronics, Inc.
Title
CPU (13/14)
Size
Document Number
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0.1
Date: Monday, June 06, 2016
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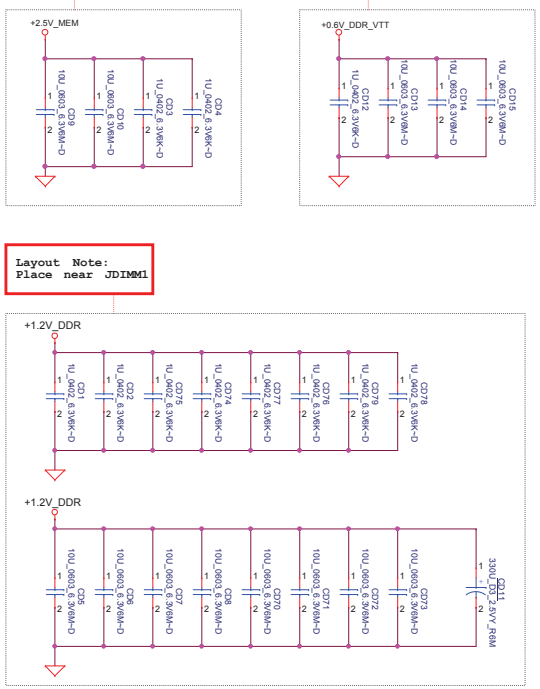
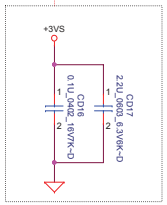
Layout Note:
Place near JDIMM1.257,259

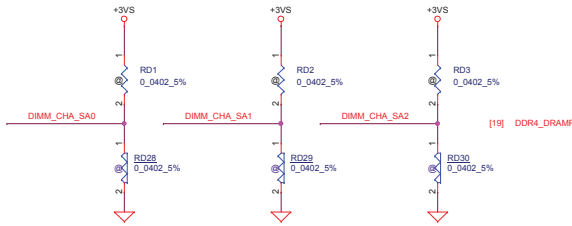
Layout Note:
Place near JDIMM1.258

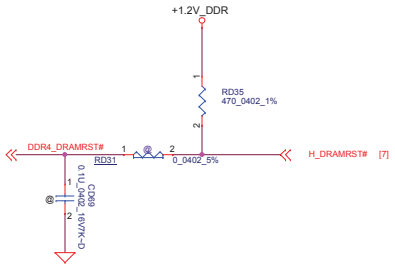
Layout Note:
Place near JDIMM1.255

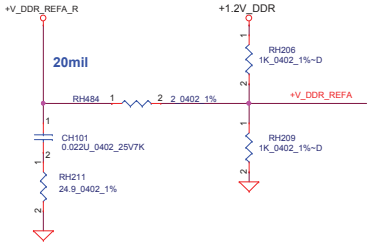
Layout Note:
Place near JDIMM1

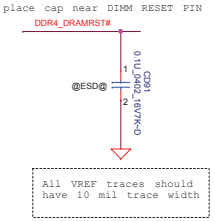












Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size	Document Number	Rev
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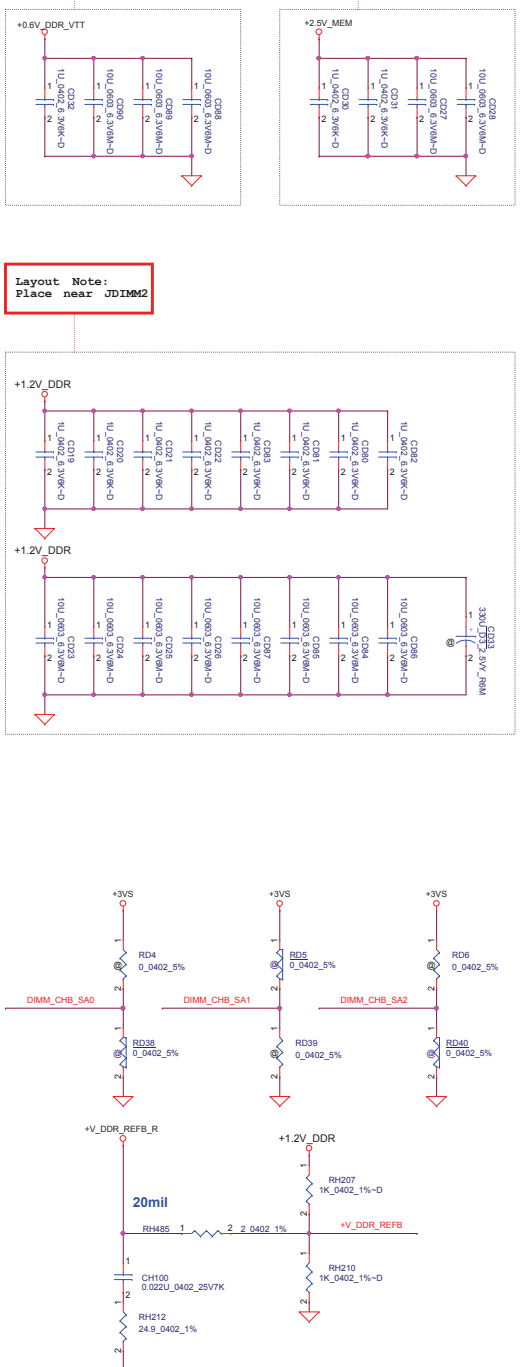
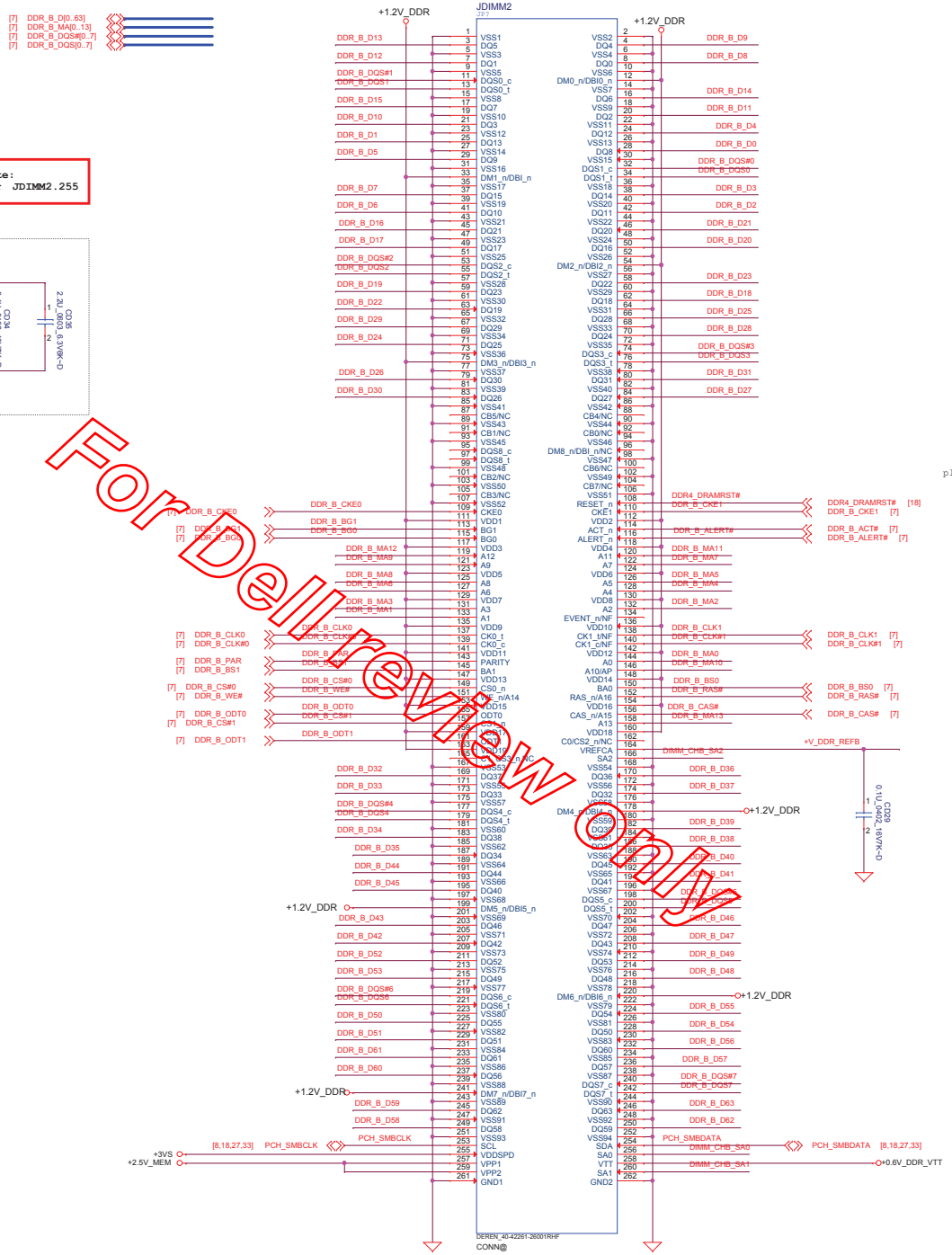
Layout Note:
Place near JDIMM2.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2





Security Classification	Compal Secret Data		
Issued Date	2015/01/30	Deciphered Date	2016/12/31

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size	Document Number	Rev
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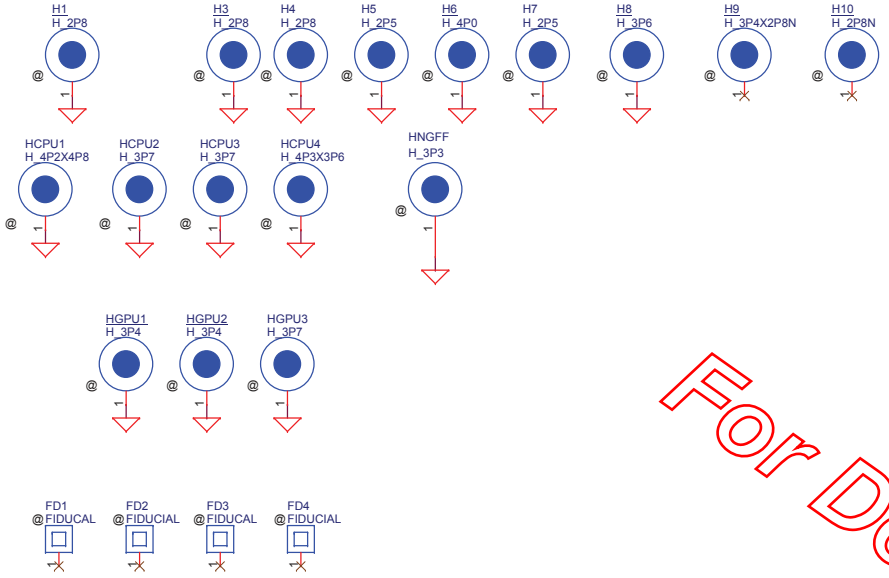
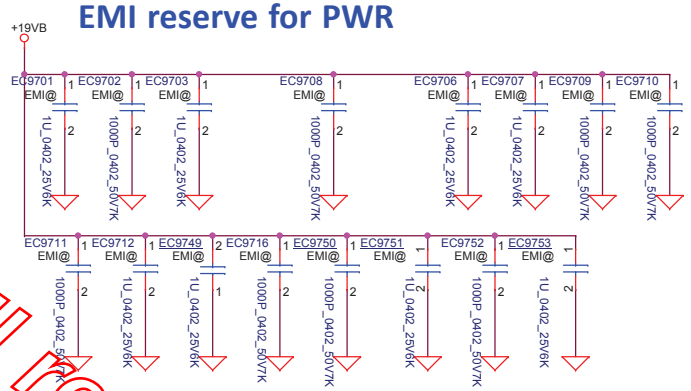
Main Func = Other

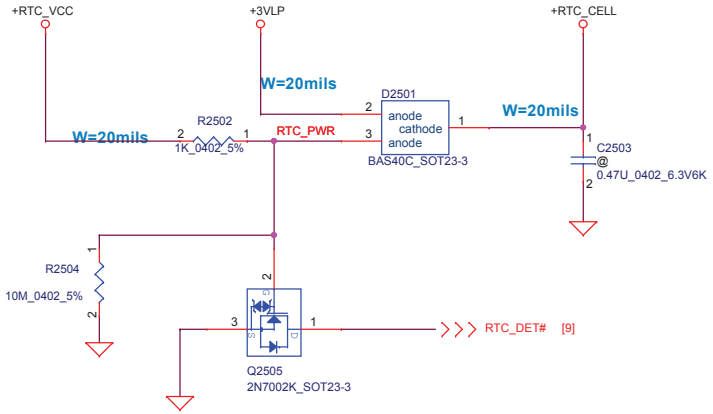
Screw hole/FD/EMI stop



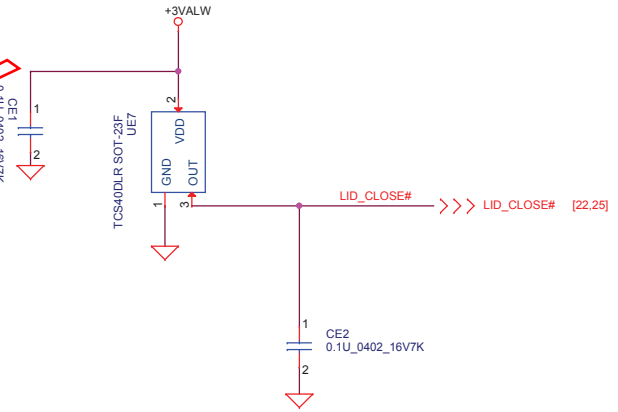
EMI reserve for PWR



Main Func = RTC



Main Func = LID Switch



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: RTC/Screw hole/EMI caps

Size	Document Number	Rev
	LA-D821P	0.1

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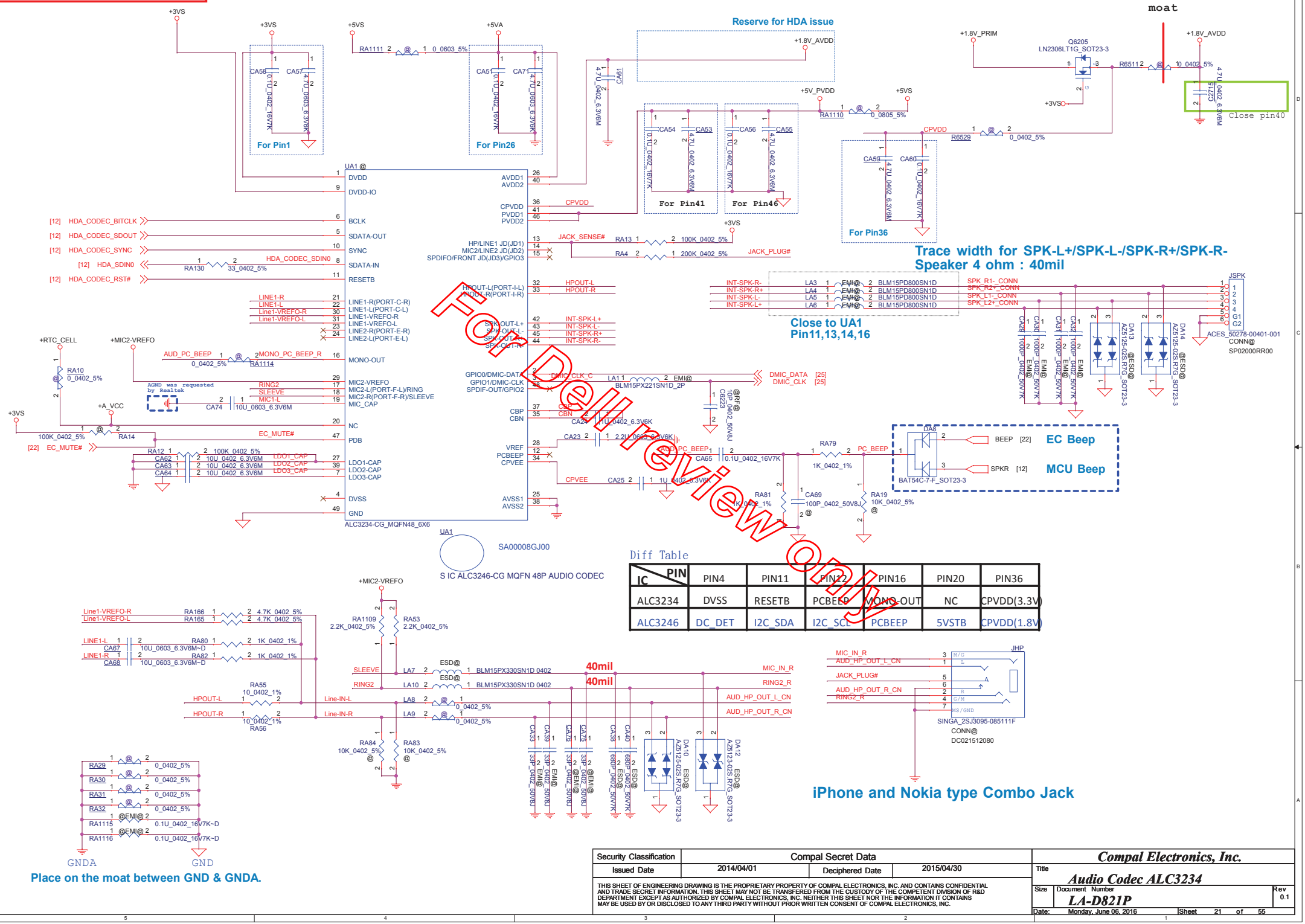
Main Func = Audio



Diff Table

IC \ PIN	PIN4	PIN11	PIN12	PIN16	PIN20	PIN36
ALC3234	DVSS	RESETB	PCBEEP	MONO-OUT	NC	CPVDD(3.3V)
ALC3246	DC_DET	I2C_SDA	I2C_SCL	PCBEEP	5VSTB	CPVDD(1.8V)

Security Classification	Compal Secret Data		
Issued Date	2014/04/01	Deciphered Date	2015/04/30

Compal Electronics, Inc.

Title: Audio Codec ALC3234

Size: | Document Number: LA-D821P | Rev: 0.1

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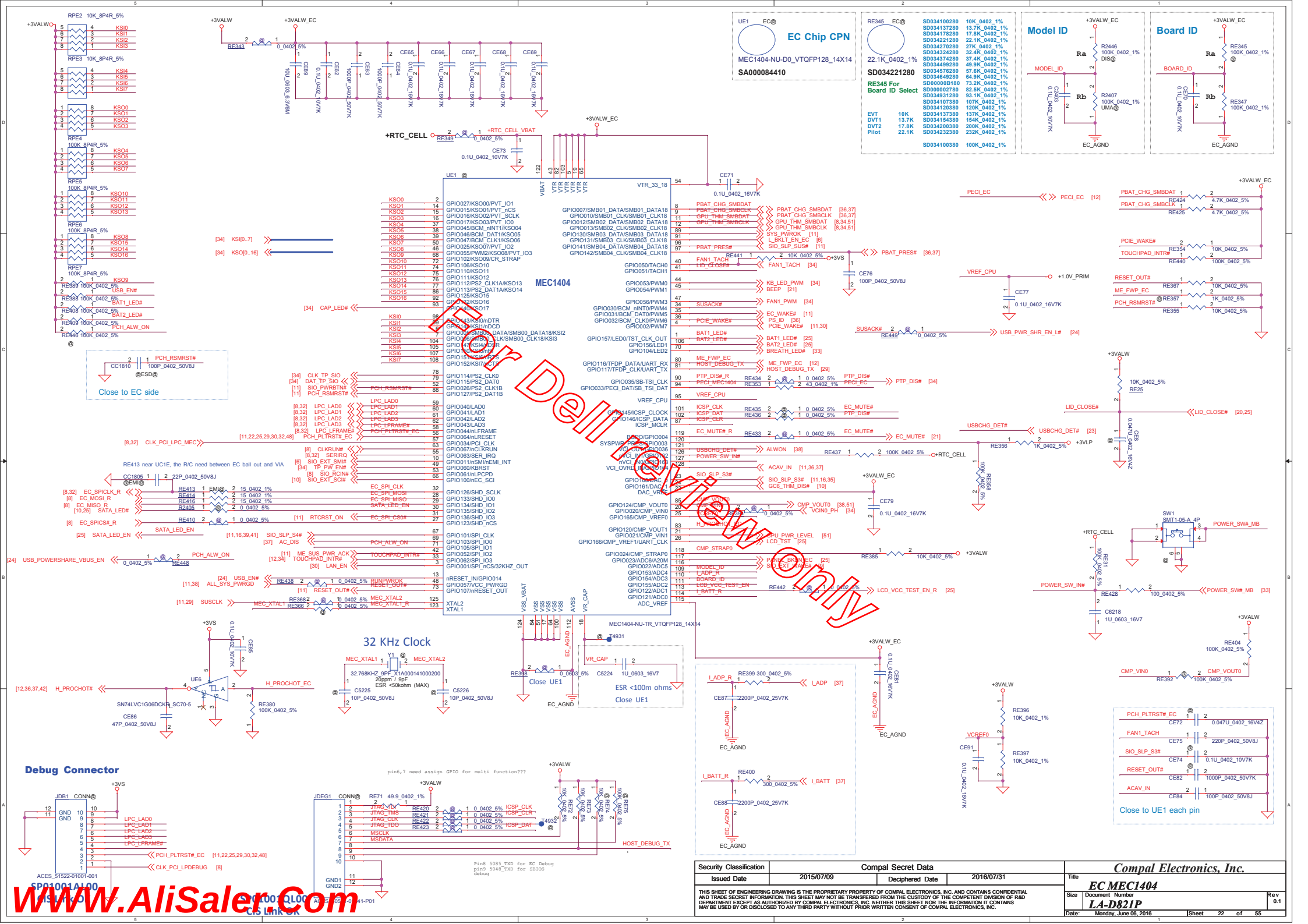

Security Classification	Compal Secret Data
Issued Date	2015/07/09
Deciphered Date	2016/07/31

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Compal Electronics, Inc.

Title: EC MEC1404

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Main Func = USB3.0 Port1/Port2

USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1

USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)

[24] USB_PN1_CHR
[24] USB_PP1_CHR
TR3404
MCM1012B900F06BP_4P
EMI@
USB_PN1_CHR_C
USB_PP1_CHR_C

U3402
L05ESDL5V0NA-4_SLP2510P8-10-9
ESD@
USB3_CRX_DTX_N1_C
USB3_CRX_DTX_P1_C
USB3_CTX_DRX_N1_C
USB3_CTX_DRX_P1_C

JUSB1
TAIWI_USB034-107CRL-TWD
CONN@
+USB30_VCCA
USB_PP1_CHR_C
USB_PN1_CHR_C
USB3_CRX_DTX_P1_C
USB3_CRX_DTX_N1_C
USB3_CTX_DRX_P1_C
USB3_CTX_DRX_N1_C
[22] USBCHG_DET#
R6531 2_@ESD@1 0_0402_5%
C6220 0.1U_0402_16V7K ESD@
ESD@ AZC199-02SPR7G_SOT23-3 EU3403

USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

[10] USB3_CTX_DRX_P1
C3404 0.1U_0402_16V7K
USB3_CTX_DRX_P1_R
R3408 0_0402_5%
USB3_CTX_DRX_P1_C

[10] USB3_CRX_DTX_P1
R3410 0_0402_5%
USB3_CRX_DTX_P1_C

[10] USB3_CTX_DRX_N1
C3403 0.1U_0402_16V7K
USB3_CTX_DRX_N1_R
R3409 0_0402_5%
USB3_CTX_DRX_N1_C

[10] USB3_CRX_DTX_N1
R3411 0_0402_5%
USB3_CRX_DTX_N1_C

USB2.0 90ohm
Main SM070003Z00(S COM FI_ INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FI_ MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FI_ PANASONIC EXC24CQ900U)

[10] USB_PN2
[10] USB_PP2
TR3405
MCM1012B900F06BP_4P
EMI@
USB_PN2_C
USB_PP2_C

U3403
L05ESDL5V0NA-4_SLP2510P8-10-9
ESD@
USB3_CRX_DTX_N2_C
USB3_CRX_DTX_P2_C
USB3_CTX_DRX_N2_C
USB3_CTX_DRX_P2_C

JUSB2
TAITW_PUBAUN-09FLBS1NN4H0
CONN@
+USB30_VCCB
USB_PN2_C
USB_PP2_C
USB3_CRX_DTX_N2_C
USB3_CRX_DTX_P2_C
USB3_CTX_DRX_N2_C
USB3_CTX_DRX_P2_C
ESD@ AZC199-02SPR7G_SOT23-3 EU3404

USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

[10] USB3_CTX_DRX_P2
C3405 0.1U_0402_16V7K
USB3_CTX_DRX_P2_R
R3416 0_0402_5%
USB3_CTX_DRX_P2_C

[10] USB3_CRX_DTX_P2
R3418 0_0402_5%
USB3_CRX_DTX_P2_C

USB3.0 90ohm
Main SM070003V00(S COM FI_ INPAQ HCM1012GH900BP)
2nd SM070004000(S COM FI_ TAIYO MCF12102G900-T)
3rd SM070004300(S COM FI_ PANASONIC EXC24CH900U)

[10] USB3_CTX_DRX_N2
C3406 0.1U_0402_16V7K
USB3_CTX_DRX_N2_R
R3419 0_0402_5%
USB3_CTX_DRX_N2_C

[10] USB3_CRX_DTX_N2
R3417 0_0402_5%
USB3_CRX_DTX_N2_C

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Compal Electronics, Inc.

Title: USB3.0 CONN

Size	Document Number	Rev
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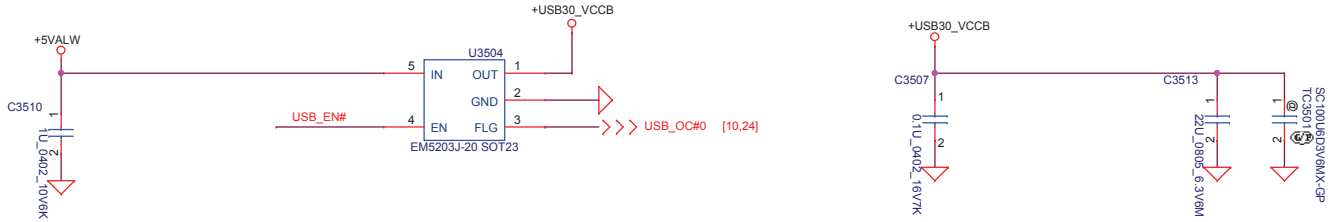
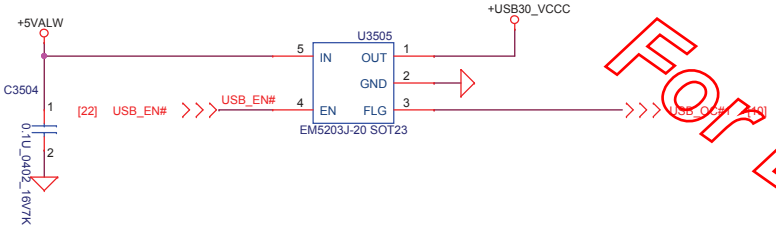
Main Func = USB3.0 Port2

USB3.0 Port2



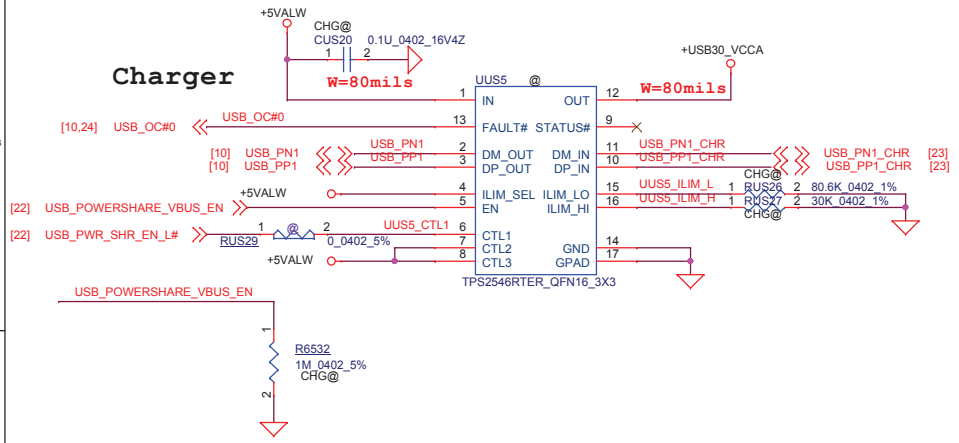
Main Func = USB3.0 Port3

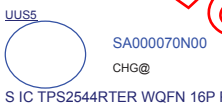
USB3 Port3/USB2 Port1 (IO Board)



Main Func = USB Chager

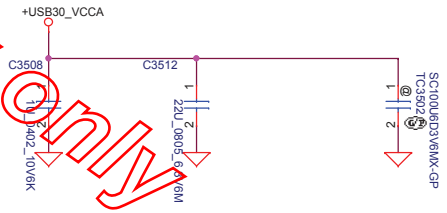
Charger





Diff Table

IC \ PIN	PIN9
TPS2546	STATUS#
TPS2544	NC



Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPXIOA07(pin104)	GPIO22(pin41)	GPXIOA11(pin108)	GPIO21(pin40)
S0/S3(CDP)	1	1	1	1
S4/S5(DCP)	0	1	1	1

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: USB Power SW

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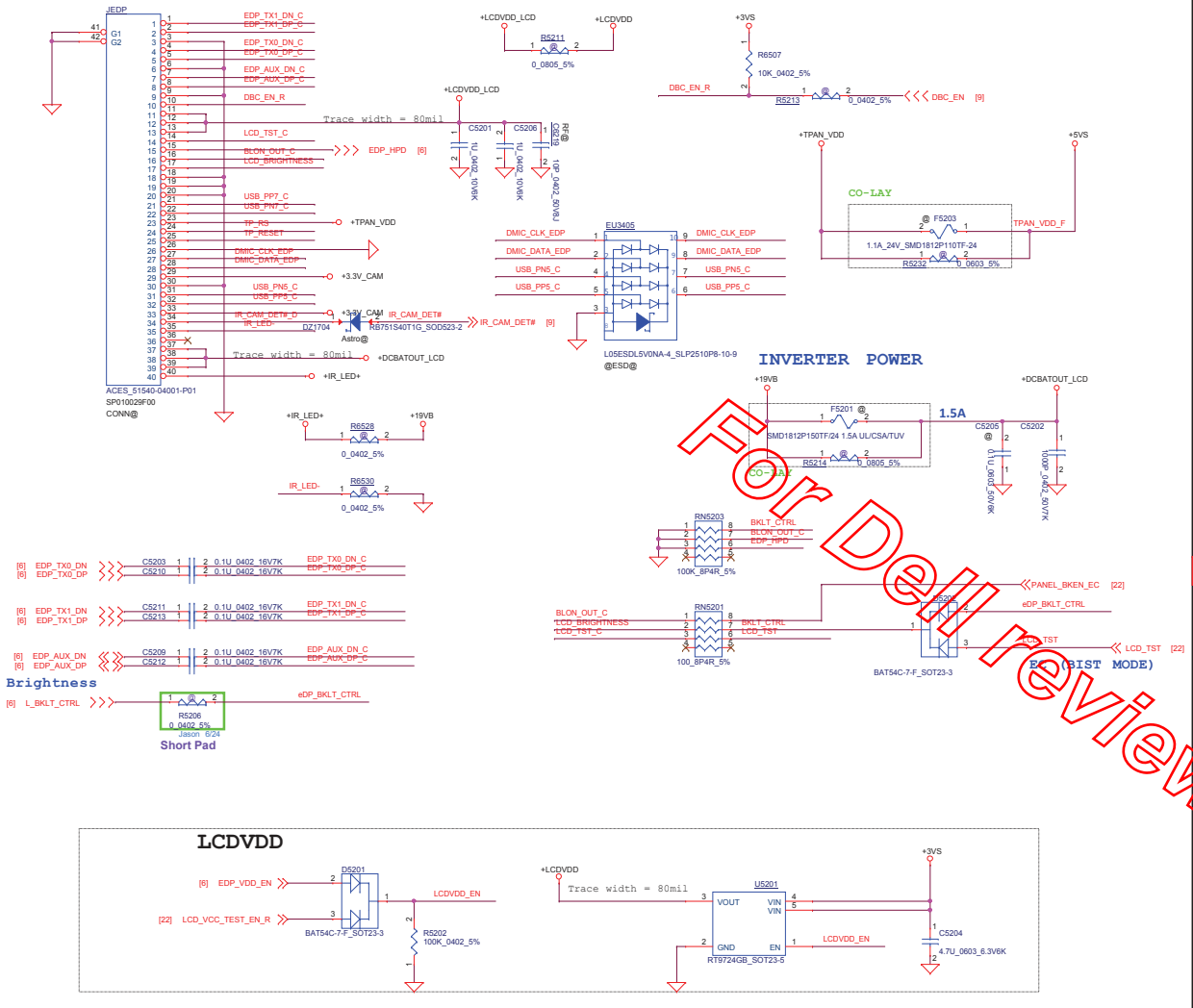
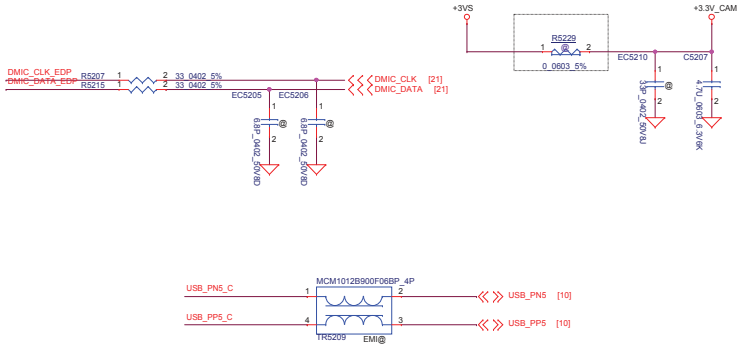
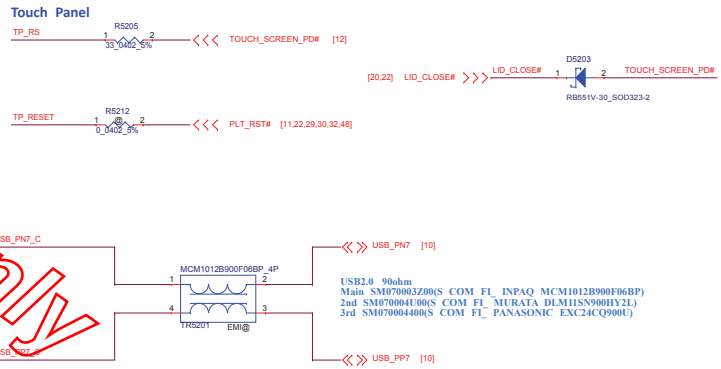
Main Func = LCD



Main Func = CAM

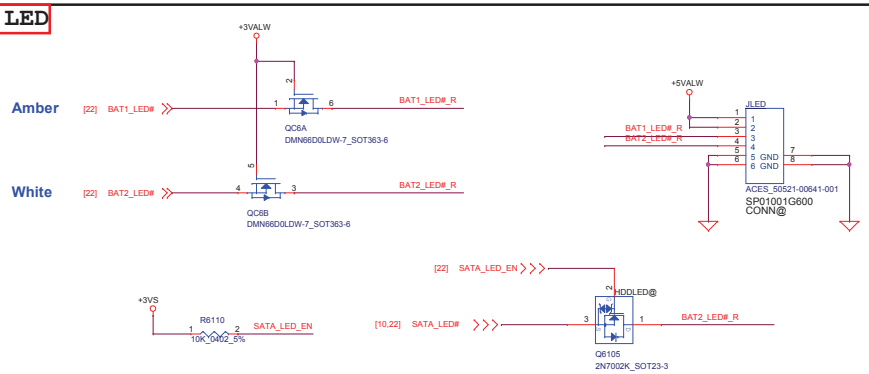


Main Func = TS



LCDVDD

Main Func = LED



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.			
Title: LCD/Inverter CONN			
Size	Document Number: LA-D821P		Rev: 0.1
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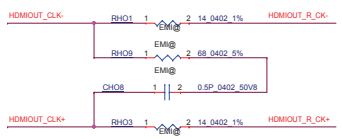
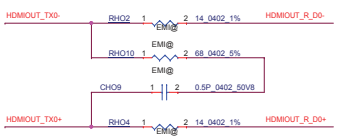
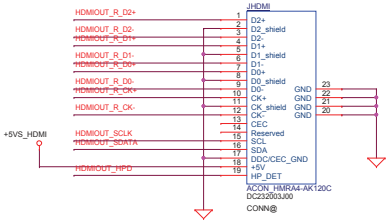
Main Func = HDMI

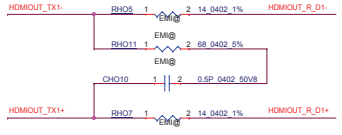
2014.12.25
1. LHO1 4HO2 LH3 · LH O4 chan ge ro ot p in (SI ZE : 050 4) a nd unpp
2. RHO1,RHO3,RHO5,RHO7,RHO2,RHO4,RHO6,RHO8,RHO13,RHO14,RHO15,RHO16, change to pop.

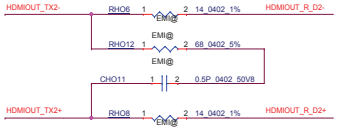
HDMI-OUT Connector

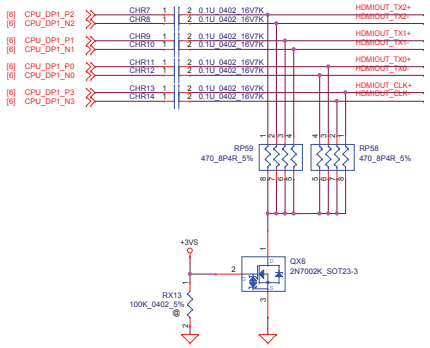


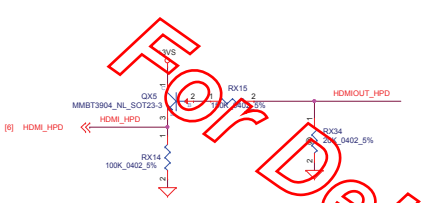


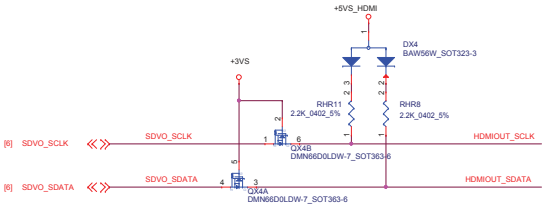












Security Classification	Compal Secret Data		
Issued Date	2014/04/02	Deciphered Date	2015/10/02

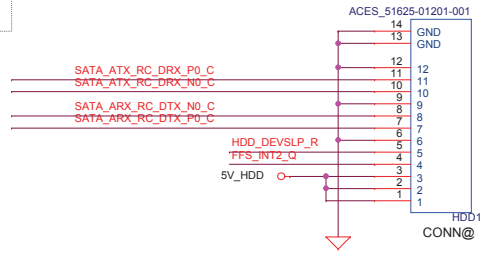
Compal Electronics, Inc.		
Title: P21-HDMI		
Size	Document Number: LA-D821P	Rev: 0.1
Date: Monday, June 06, 2016	Sheet 26 of 55	

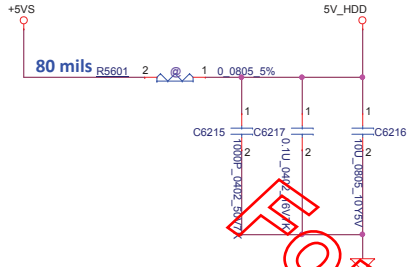
Main Func = HDD

SATA HDD Connector

Reserve, refer to M15 EE Implementation Requirements

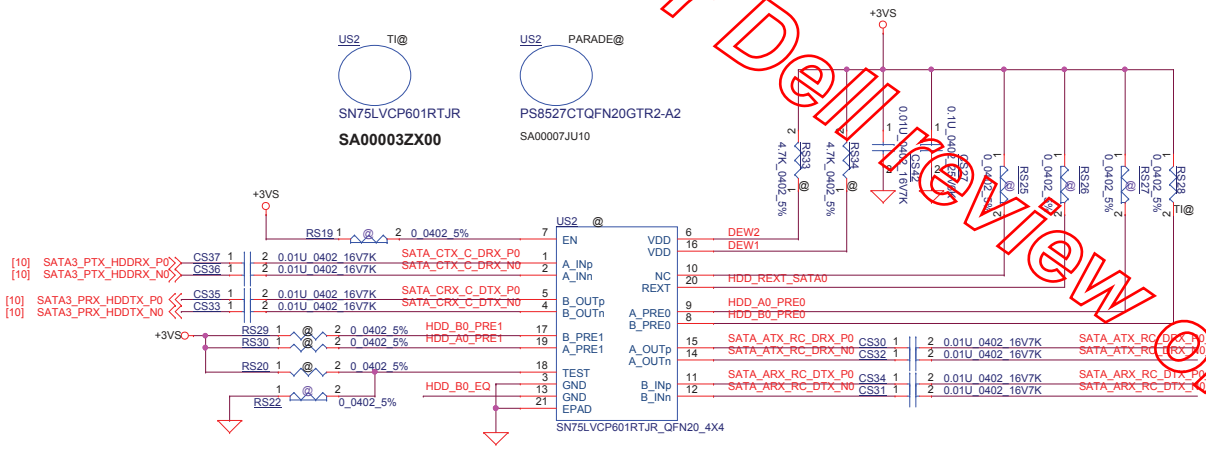
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

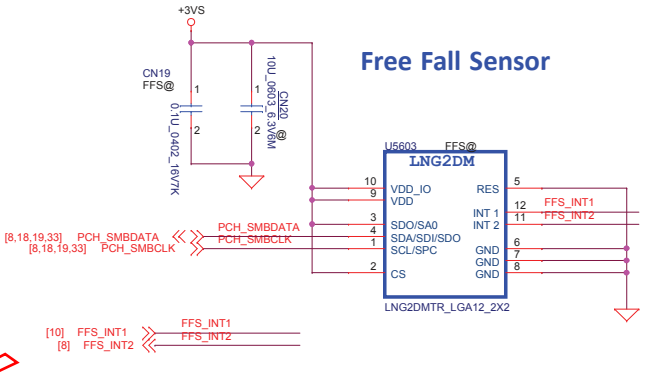




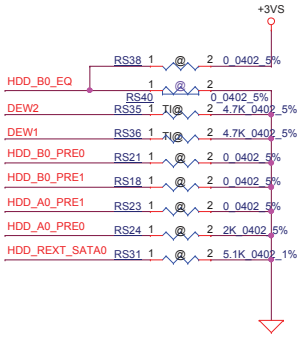
US2 TI@ SN75LVCP601RTJR SA00003ZX00

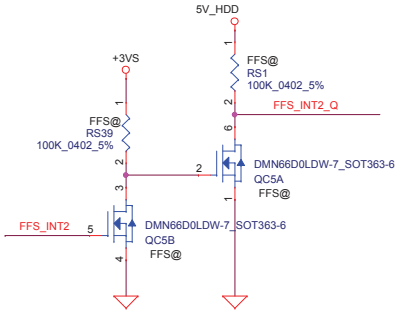
US2 PARADE@ PS8527CTQFN20GTR2-A2 SA00007JU10





	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007JU00	7.5K	NC	V	V	V	NC	NC





Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

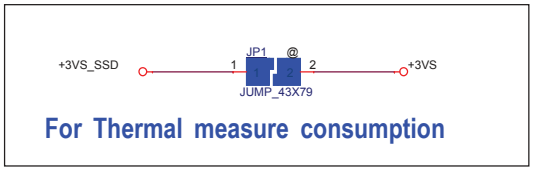
Compal Electronics, Inc.

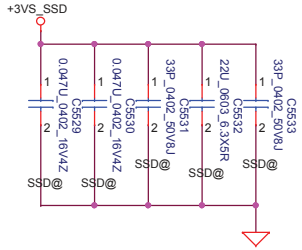
Title: HDD/ODD

Size | Document Number: LA-D821P | Rev: 0.1

Date: Monday, June 06, 2016 | Sheet 27 of 55

Main Func = SSD





2/6 TX Cap change P/N,
Now It's 0402 0ohm resistor.

SSD
NGFF Slot_2 Key M

For Layout change pin define

Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

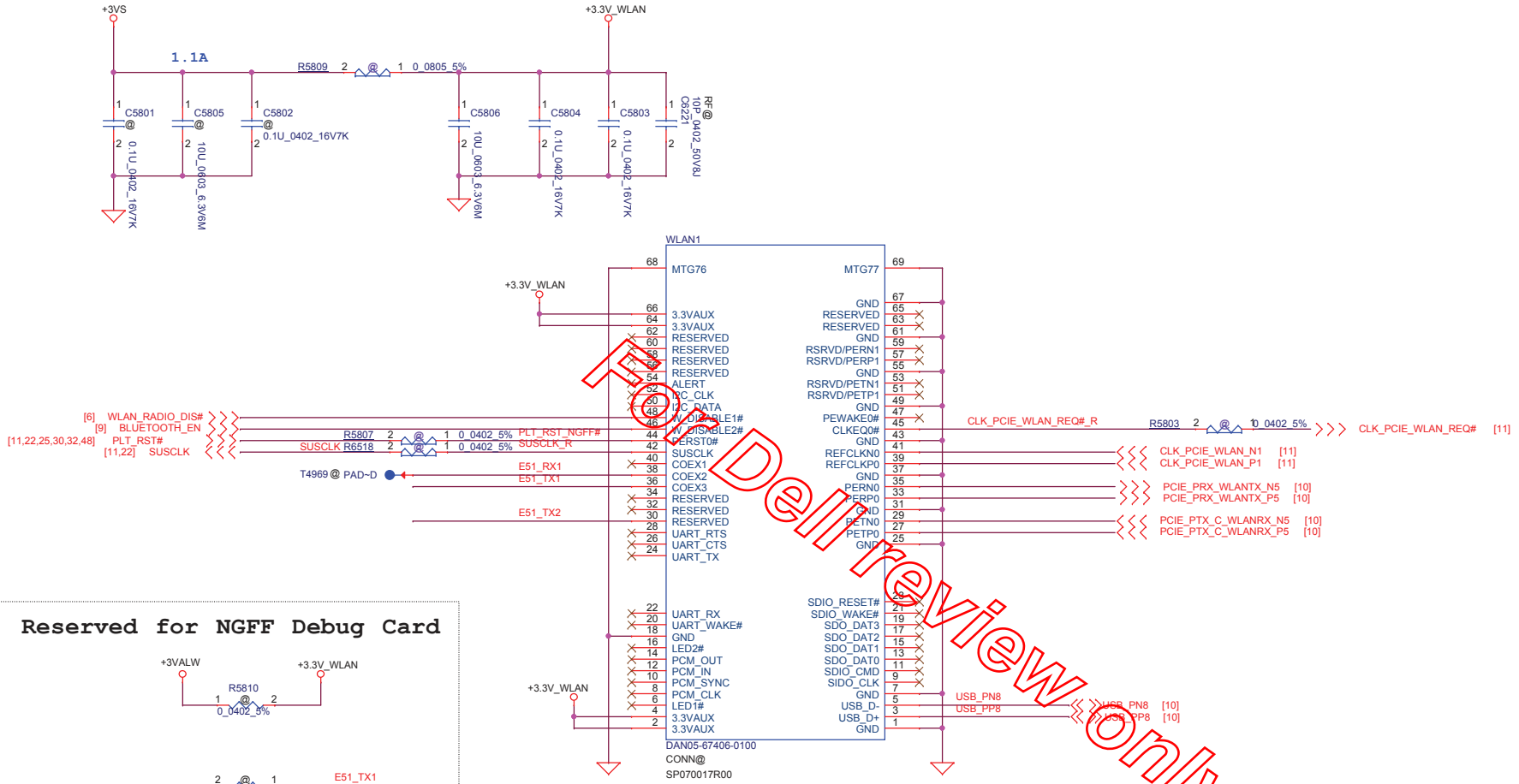
Compal Electronics, Inc.

Title: SSD

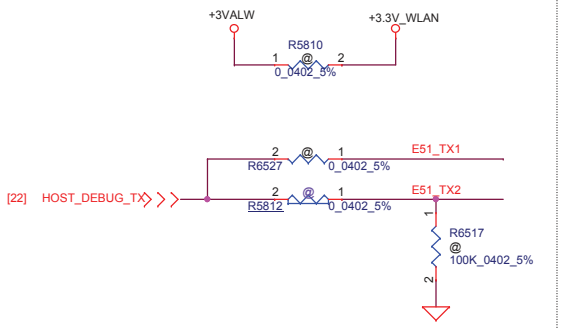
Size	Document Number	Rev
	LA-D821P	0.1

Date: Monday, June 06, 2016 Sheet 28 of 55

Main Func = WLAN



Reserved for NGFF Debug Card



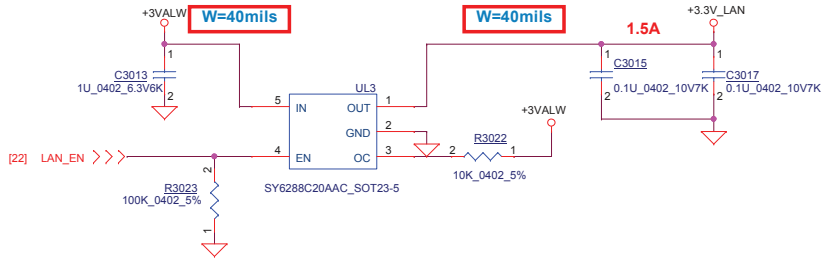
Support: Intel Dual Band Wireless-AC 3160

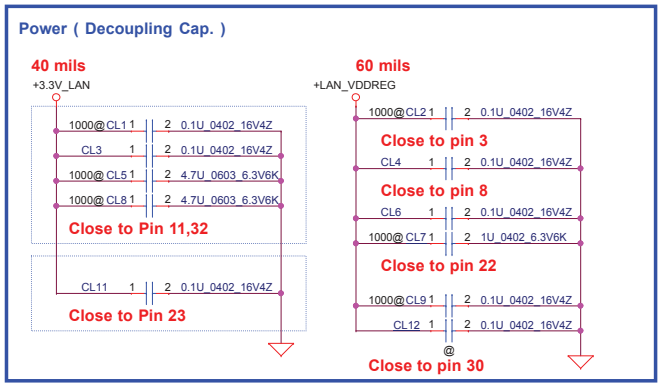
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

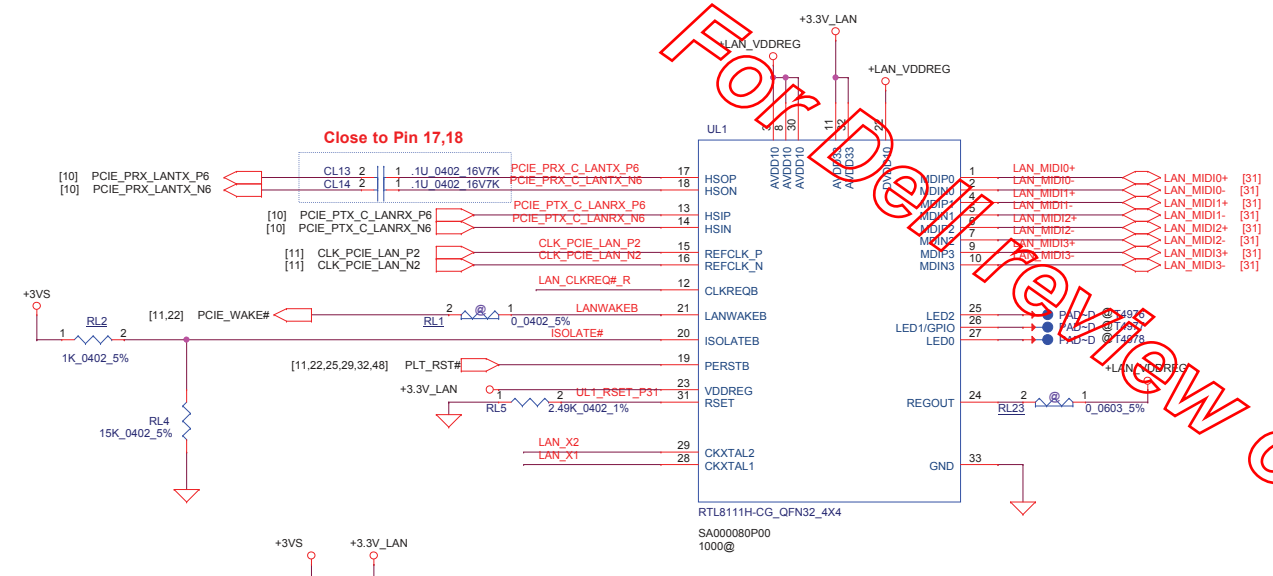
Compal Electronics, Inc.			
Title: NGFF_WLAN CONN			
Size	Document Number: LA-D821P		Rev: 0.1
Date: Monday, June 06, 2016		Sheet 29 of 55	

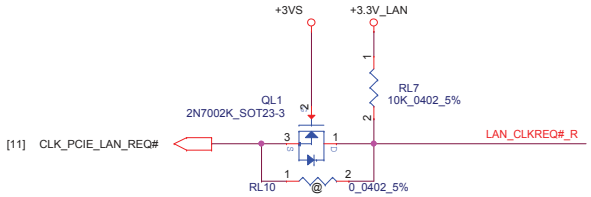
Main Func = LAN

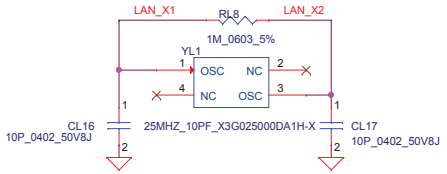
+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.











Security Classification	Compal Secret Data		
Issued Date	2014/12/15	Deciphered Date	2016/12/15

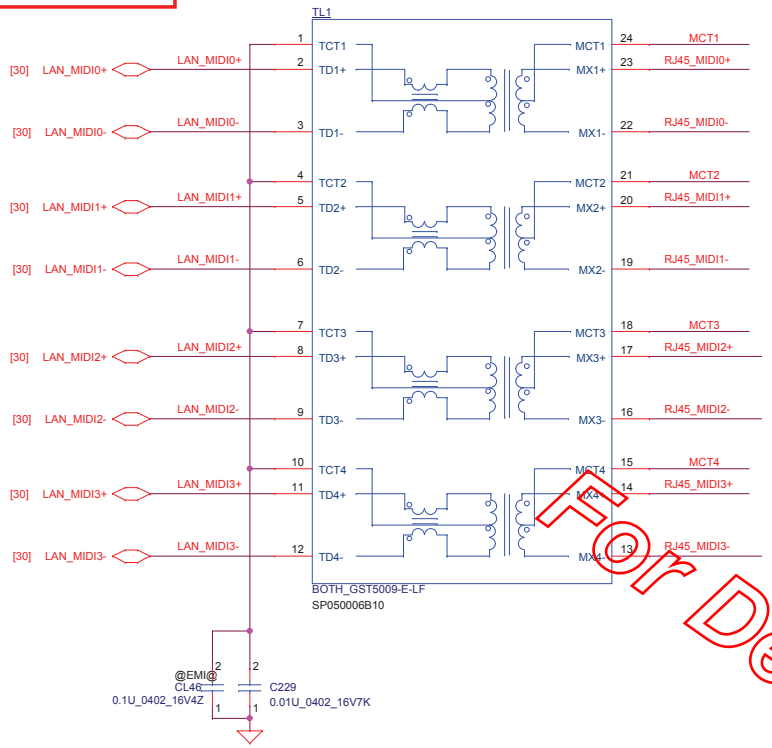
Compal Electronics, Inc.

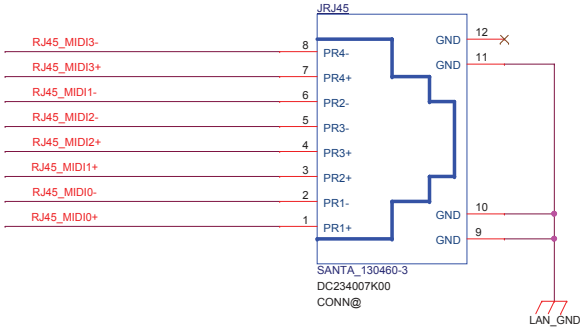
Title: LAN RTL8111H-CG

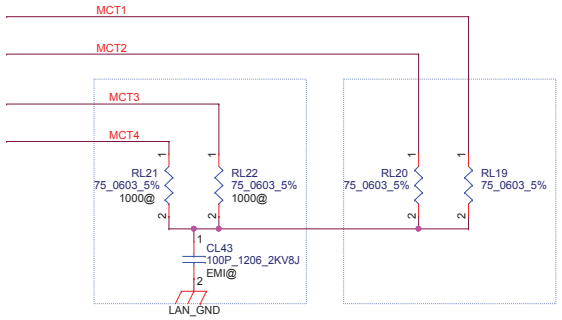
Size	Document Number	Rev
Custom	LA-D821P	0.1

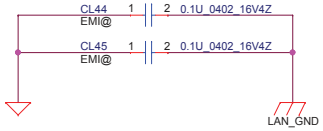
Date: Monday, June 06, 2016 | Sheet 30 of 55

Main Func = LAN









Security Classification	Compal Secret Data		
Issued Date	2012/04/27	Deciphered Date	2013/04/27

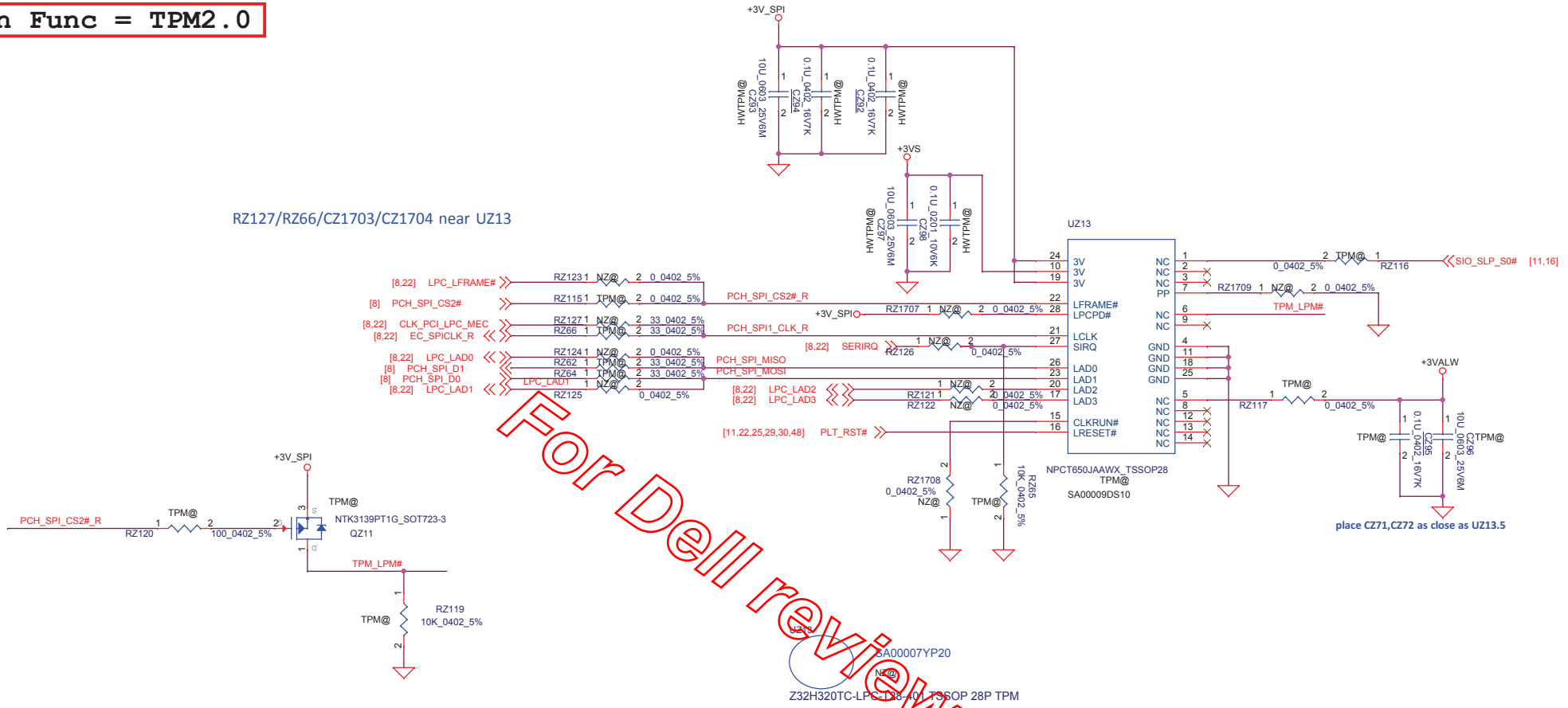
Compal Electronics, Inc.

Title: JMB385 Media Card Controller

Size	Document Number	Rev
Custom	LA-D821P	0.1

Date: Monday, June 06, 2016 Sheet 31 of 55

Main Func = TPM2.0



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2015/07/21

Compal Electronics, Inc.

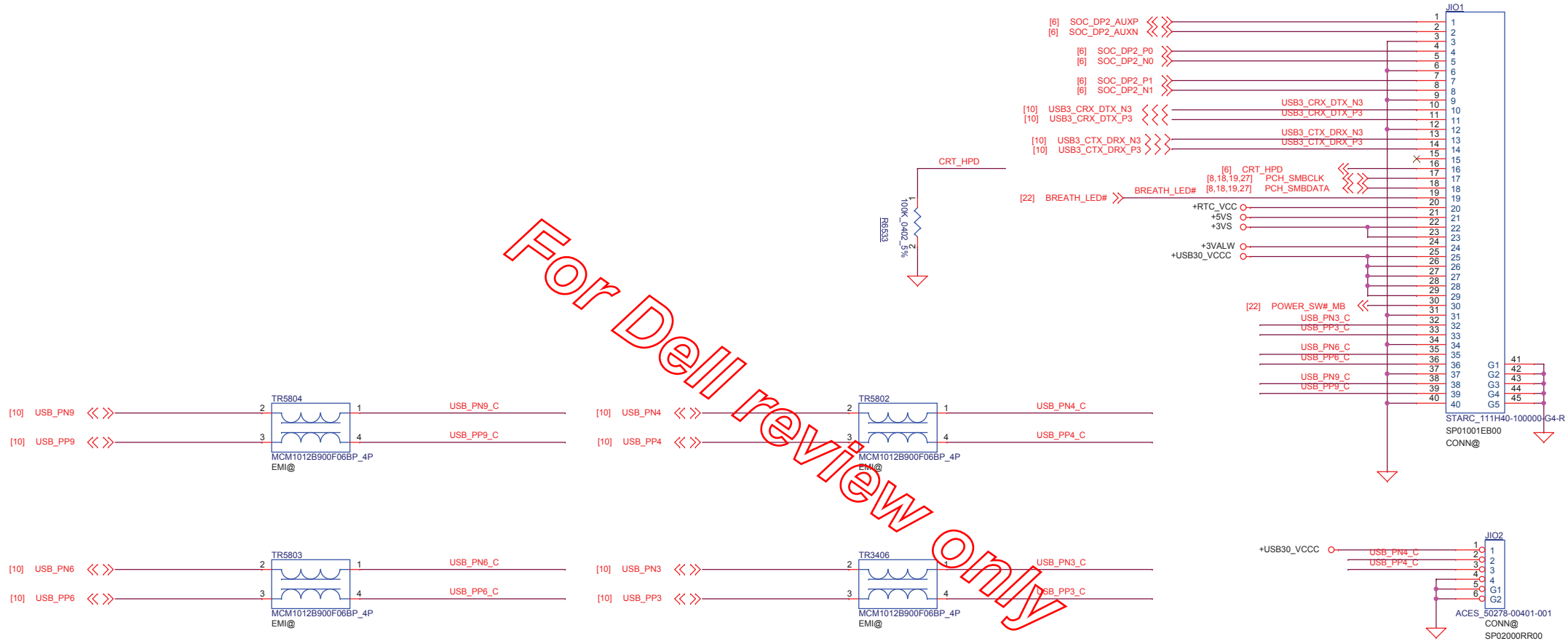
Title: TPM

Size: Custom | Document Number: LA-D821P | Rev: 0.1

Date: | Sheet 32 of 55

Main Func = IO Connector

I/O Board Connector



Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: **IO Board Connector**

Size	Document Number	Rev
	LA-D821P	0.1

Date: Monday, June 06, 2016 Sheet 33 of 55

Main Func = KB

Keyboard Backlight (Reserved)

KB Backlight Power Consumption: 285mA max.

JKB
ACES_50699-03041-P01
SP01001LM00
CONN@

JKBBL
ACES_51575-00401-001

CAP LED Control
LOW actived from KBC GPIO

Main Func = TPAD

EC/PS2
PCH/I2C

TP_VDD Discharge

TPAD1
ACES_51524-0080N-001
CONN@
SP01001A900

Main Func = Thermal

Layout Note: DIMM / CPU

Layout Note: C2607 close THM26

Address: X100_1100(4C), 1001_100X(98)

DXN and DXP routing width and spacing is 10 mil / 10 mil.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Close to Thermal sensor

Close to KBC VD_IN1 for system thermal sensor

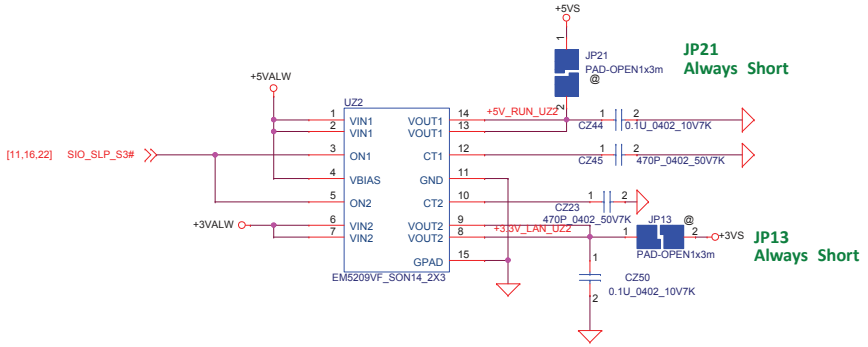
Short Pad

PURE_KBCT8

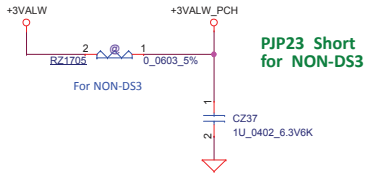
Security Classification	Compal Secret Data		
Issued Date	2015/07/09	Deciphered Date	2016/07/31

Compal Electronics, Inc.	
Title	Keyboard/Touch Pad/Thermal
Size	Document Number: LA-D821P
Rev	0.1
Date:	Monday, June 06, 2016
Sheet	34 of 55

+5V_RUN/+3.3V_RUN for System



+3VALW_PCH for System

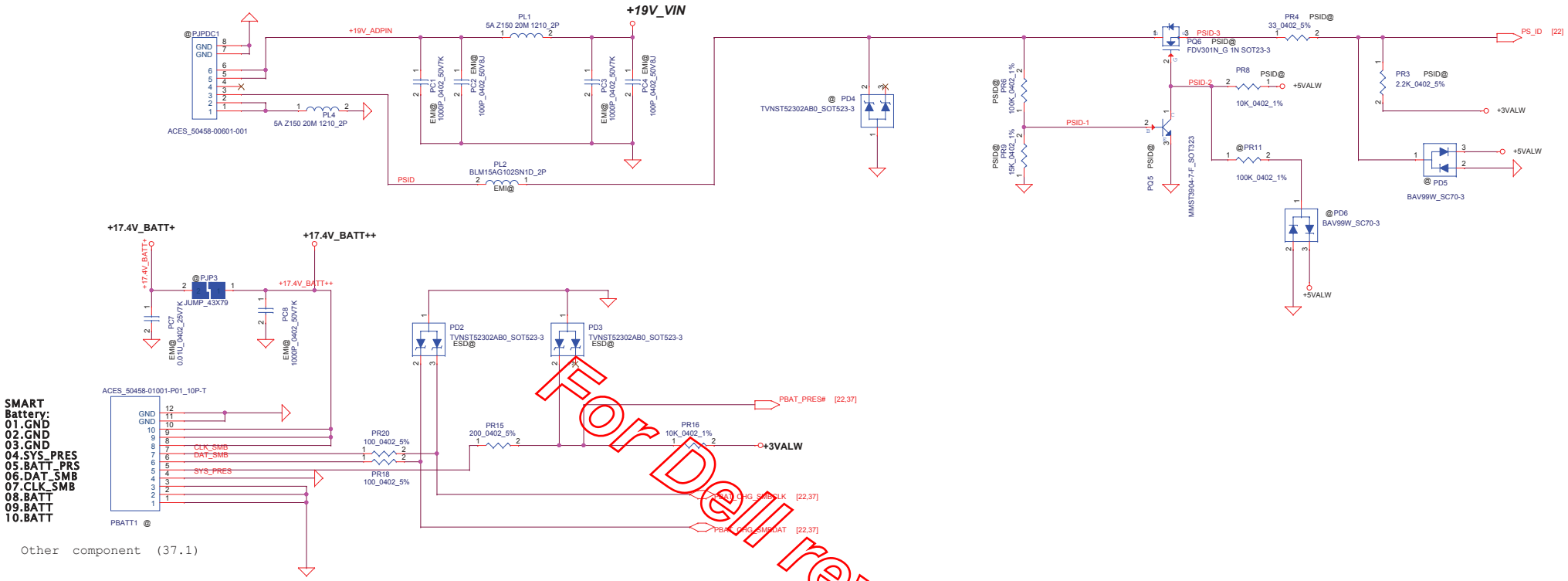


Compal Electronics, Inc.

Title: Power control

Size | Document Number: LA-D821P | Rev: 0.1

Date: Monday, June 06, 2016 | Sheet 35 of 55



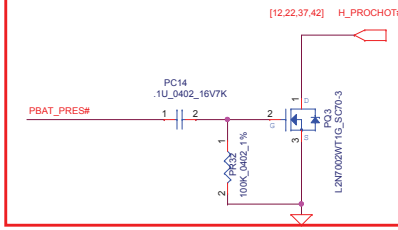
Other component (37.1)

15W_U22+VGA(SKL)
X63:PSID@/U22_SKL@/VGA@
X4P:EMI@/ESD@/VGA@EMI@/RF@VGA@

15W_U22+VGA(KBL)
X63:PSID@/U22_KBL@/VGA@
X4P:EMI@/ESD@/VGA@EMI@/RF@VGA@

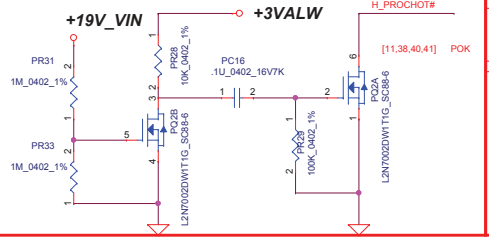
Adapter protection

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

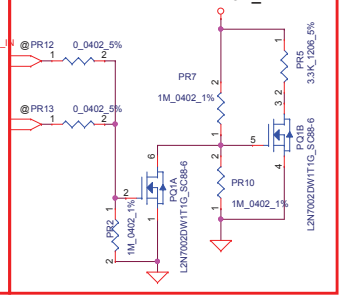


Battery protection

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



Erp lot6 Circuit



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Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

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Compal Electronics, Inc.

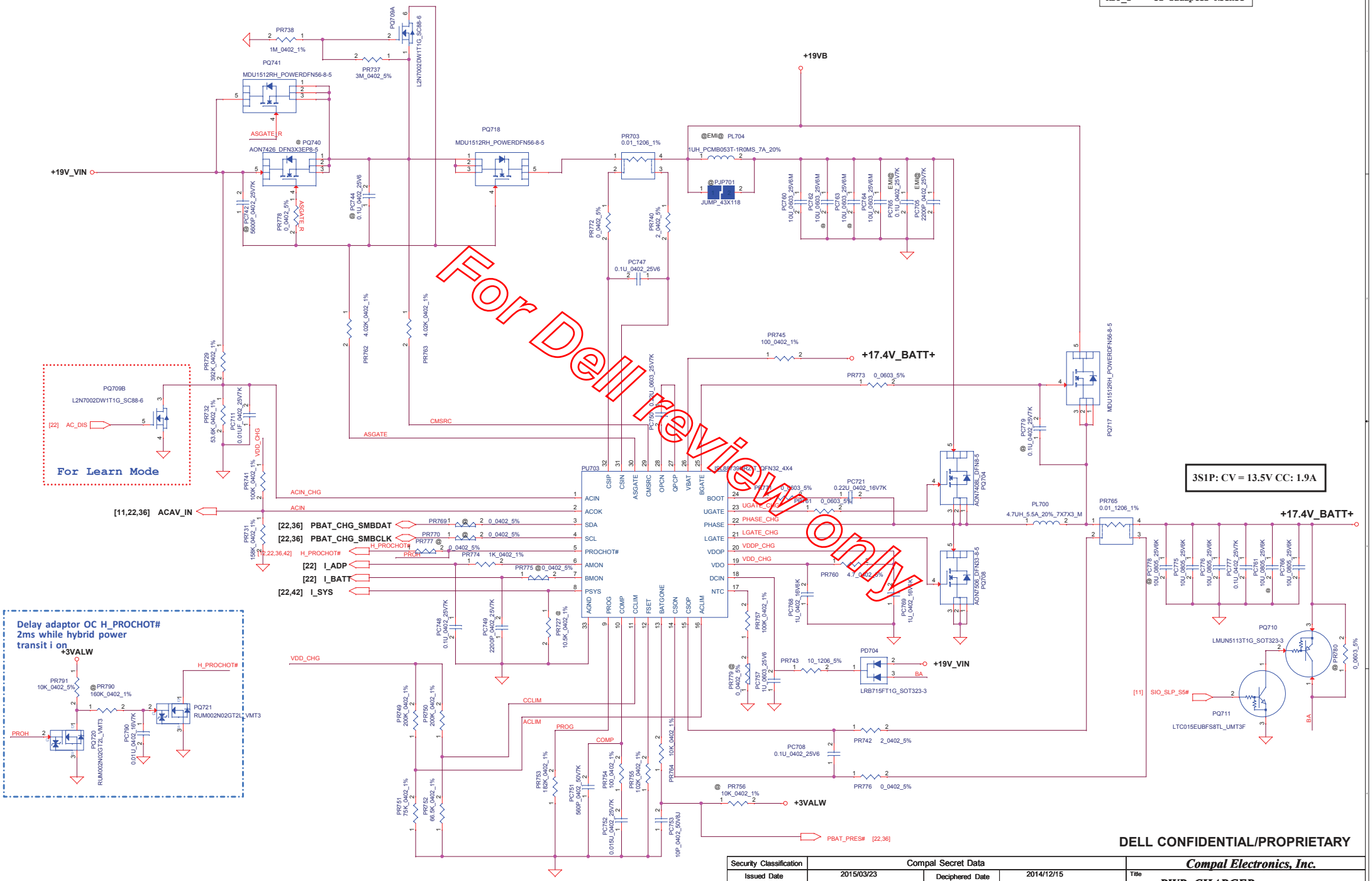
Title: PWR_DCIN/BATT CONN/OTP

Size | Document Number | Rev X01(0.2)

Date: Monday, June 06, 2016 | Sheet 36 of 55

Iada=0~3.33A(65W)
Iada=0~2.30A(45W)

ADP_I = 32*Iadapter*Rsense



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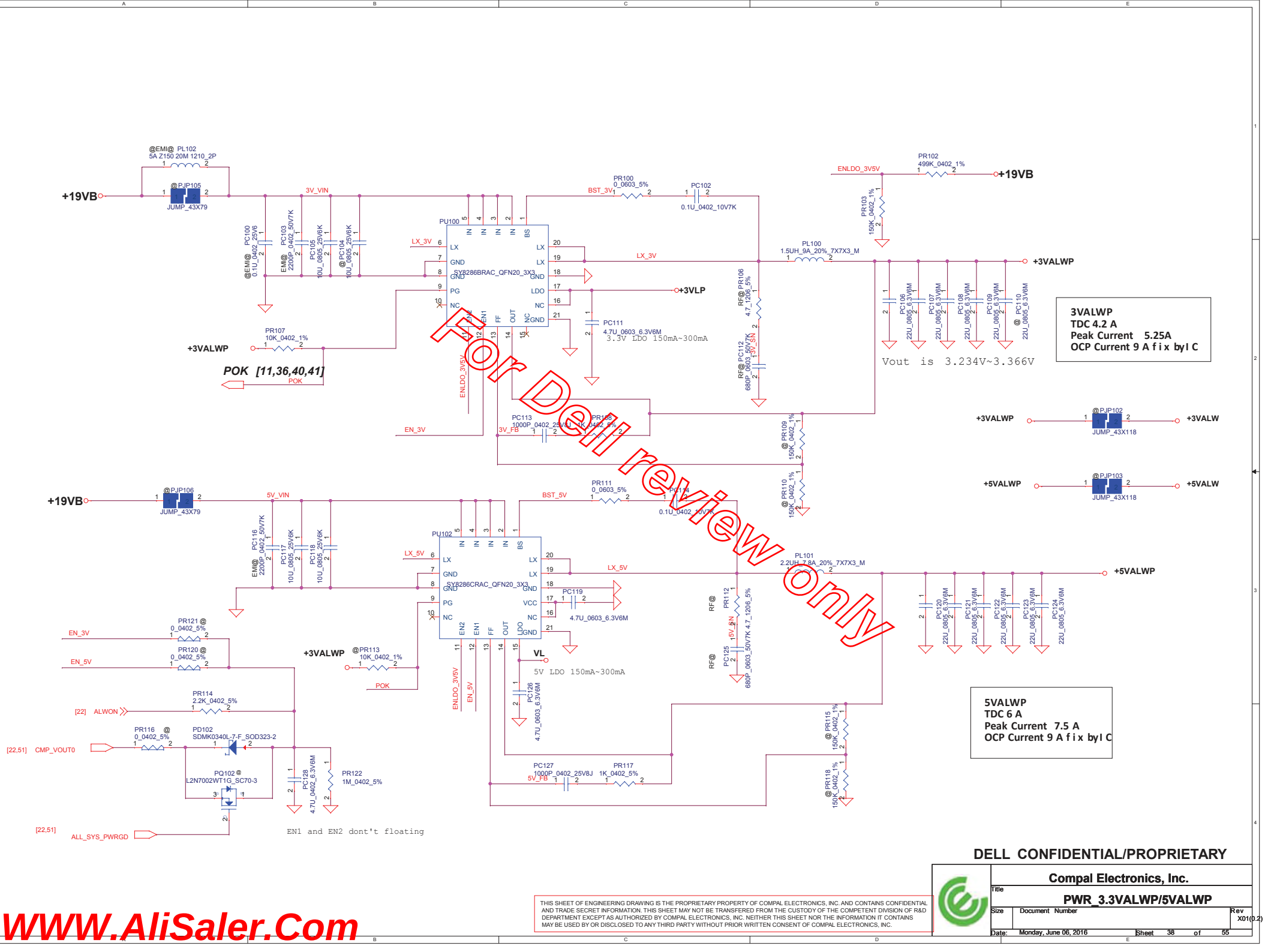
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_CHARGER

Size | Document Number | Rev X01(0.2)

Date: Monday, June 06, 2016 | Sheet 37 of 55

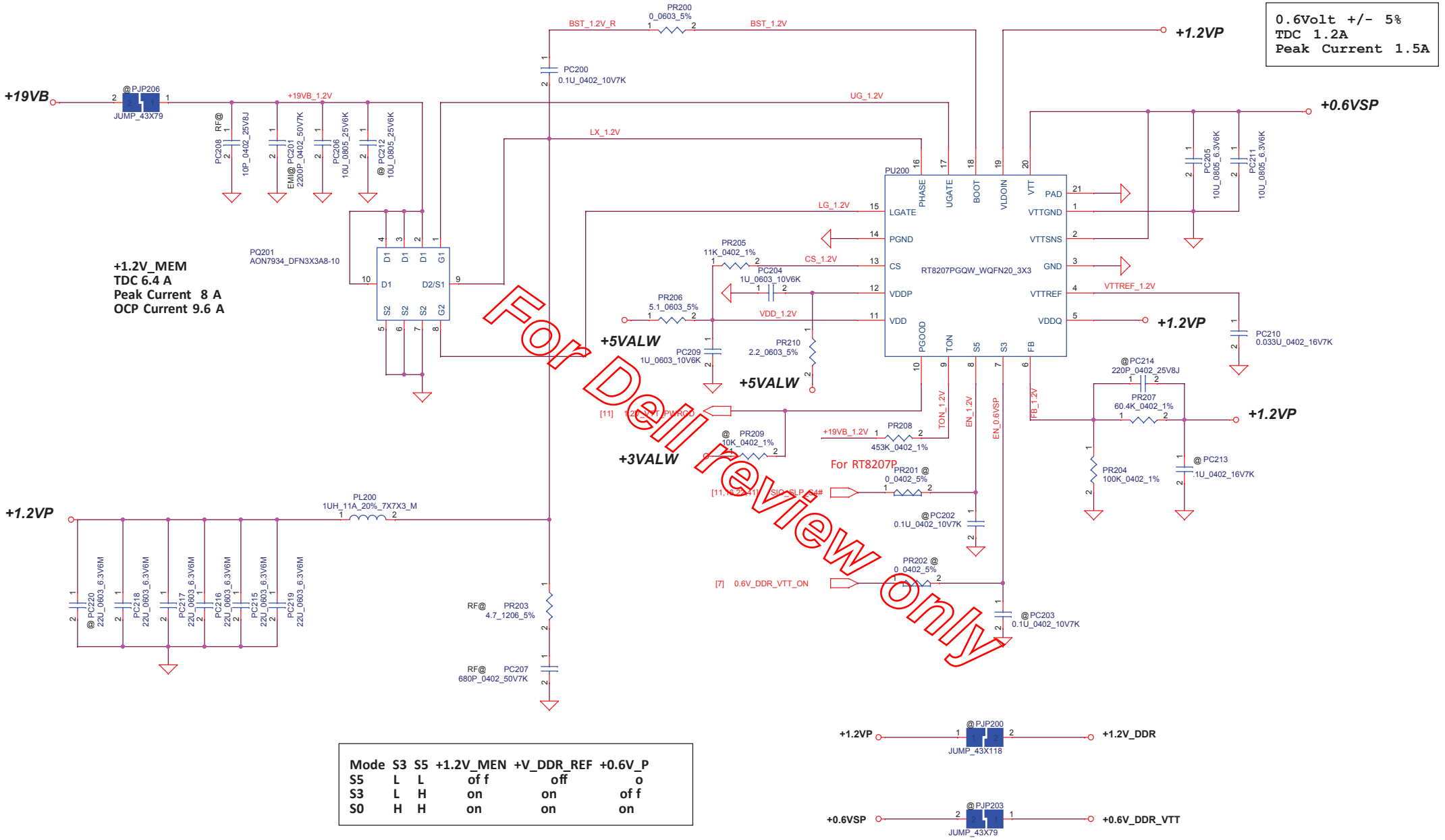


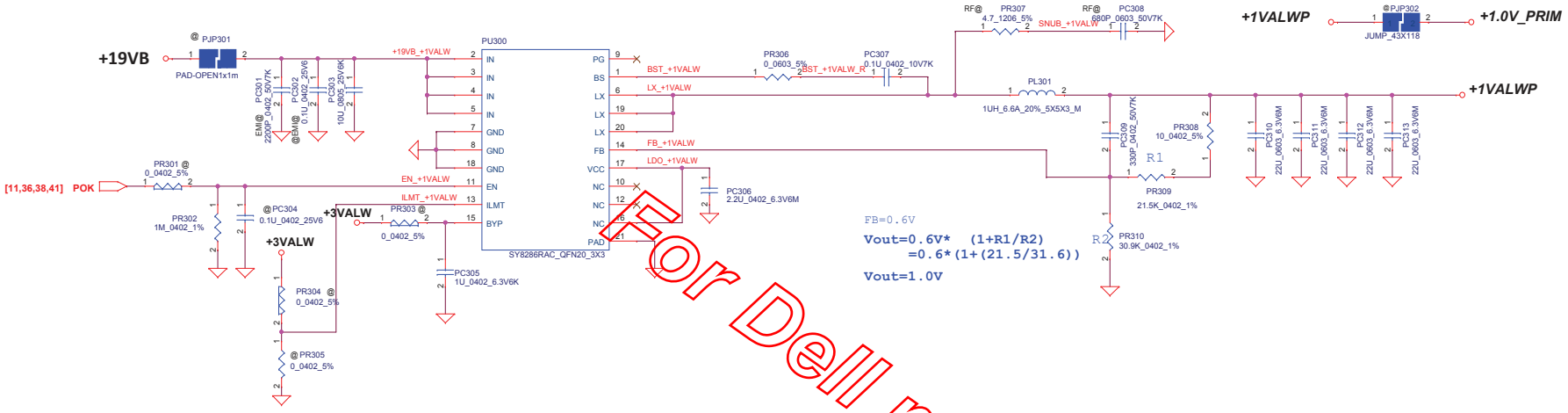
Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

Size | Document Number | Rev: X01(0.2)

Date: Monday, June 06, 2016 | Sheet 38 of 55


0.6Volt +/- 5%
TDC 1.2A
Peak Current 1.5A
+19VB
+1.2VP
+0.6VSP
+1.2V_MEM
TDC 6.4 A
Peak Current 8 A
OCP Current 9.6 A
+5VALW
+3VALW
PU200
RT8207PGQW_WQFN20_3X3
PQ201
AON7934_DFN3X3A8-10
PL200
1UH_11A_20%_7X7X3_M
+1.2V_DDR
+0.6V_DDR_VTT
For RT8207P
For Dell review only
Mode S3 S5 +1.2V_MEN +V_DDR_REF +0.6V_P
S5 L L of f off o
S3 L H on on of f
S0 H H on on on
DELL CONFIDENTIAL/PROPRIETARY
Security Classification Compal Secret Data
Issued Date 2015/03/23 Deciphered Date 2014/12/15
PWR_+1.2V_MEN/+0.6V_DDR_VTT
Size Custom Document Number Rev X01(0.2)
Date: Monday, June 06, 2016 Sheet 39 of 55



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

+1.0V_PRIM
TDC 6 A
Peak Current 8.6 A
OCP Current 12 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm , 12.0mohm	

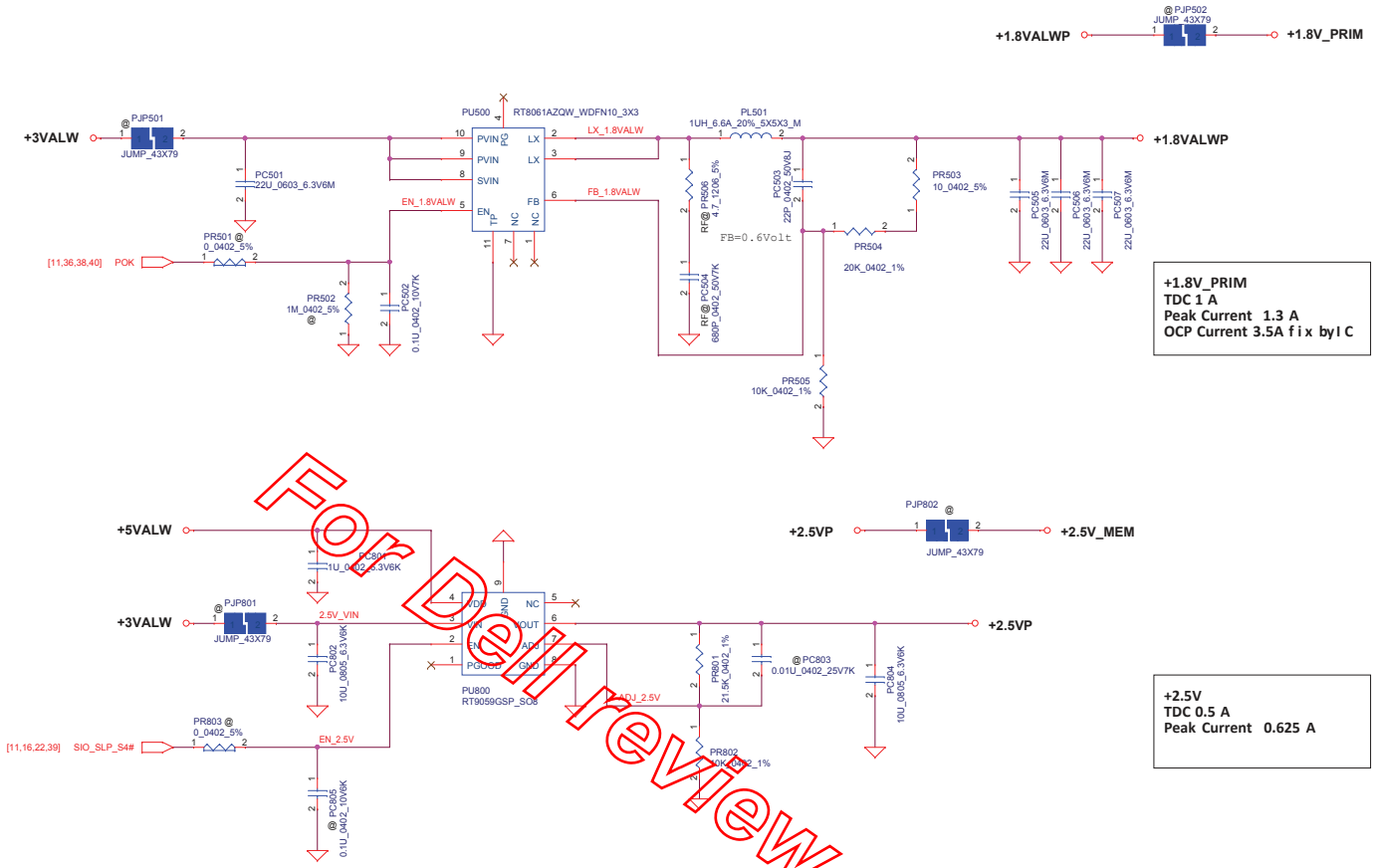
Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: PWR_+1VALWP

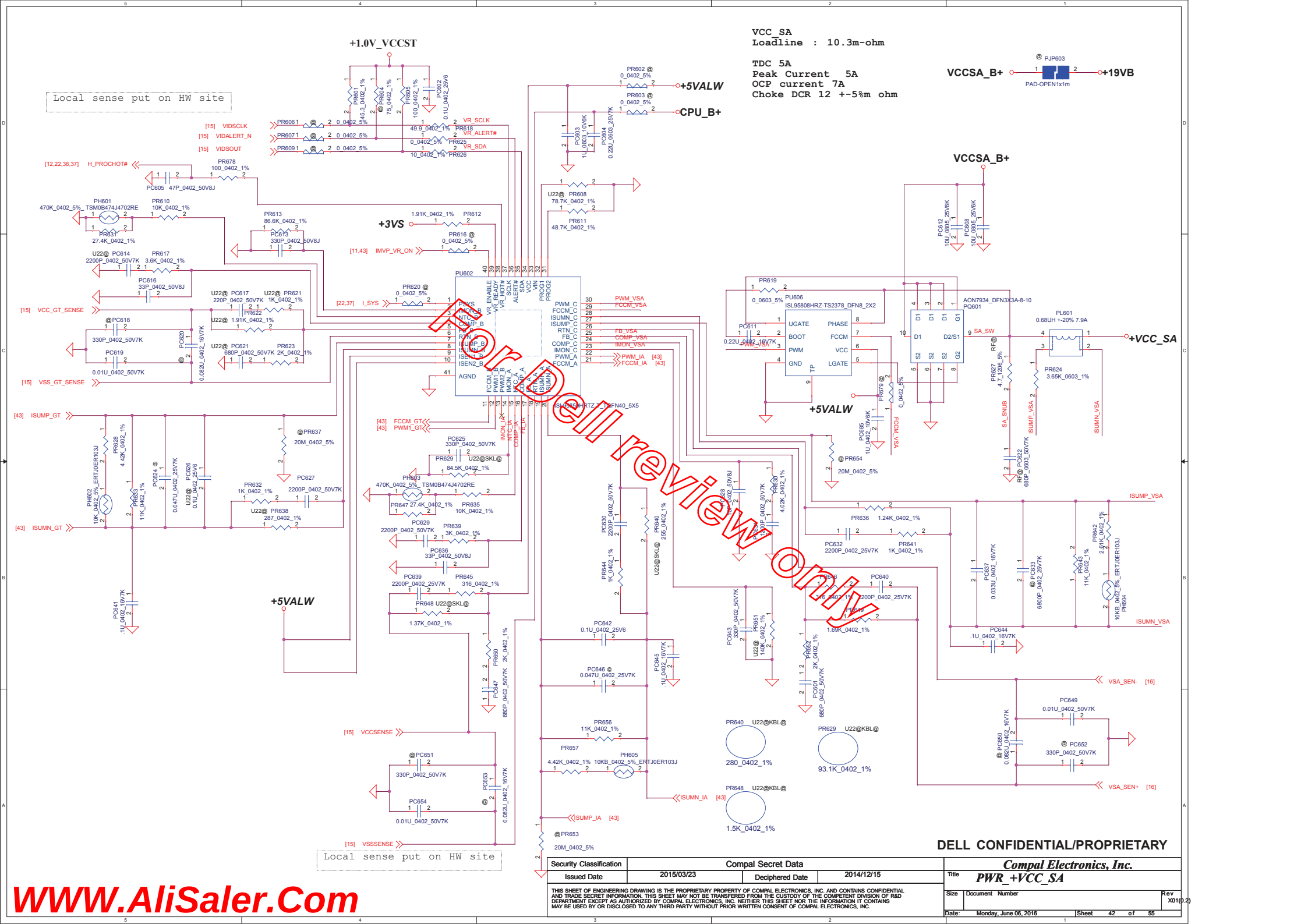
Size	Document Number	Rev
C		X01(0.2)

Date: Monday, June 06, 2016 Sheet 40 of 55



Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title: PWR +1.8V PRIM and +2.5V			
Size: C	Document Number		Rev: X01(02)
Date: Monday, June 06, 2016		Sheet 41 of 55	


VCC_SA
Loadline : 10.3m-ohm
TDC 5A
Peak Current 5A
OCP current 7A
Choke DCR 12 +-5%m ohm
VCCSA_B+
PJP603
PAD-OPEN1x1m
+19VB
+1.0V_VCCST
Local sense put on HW site
+5VALW
CPU_B+
+3VS
VCCSA_B+
PU602
PU606
ISL95808HRZ-TS2378_DFN8_2X2
AON7934_DFN3X3A-8-10
PQ601
PL601
0.68UH +-20% 7.9A
+VCC_SA
+5VALW
ISL95855HRTZ-T_TQFN40_5X5
ISUMP_VSA
ISUMN_VSA
VSA_SEN- [16]
VSA_SEN+ [16]
Local sense put on HW site
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Security Classification
Compal Secret Data
Issued Date
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Compal Electronics, Inc.
Title
PWR_+VCC_SA
Size
Document Number
Rev
X01(0.2)
Date: Monday, June 06, 2016
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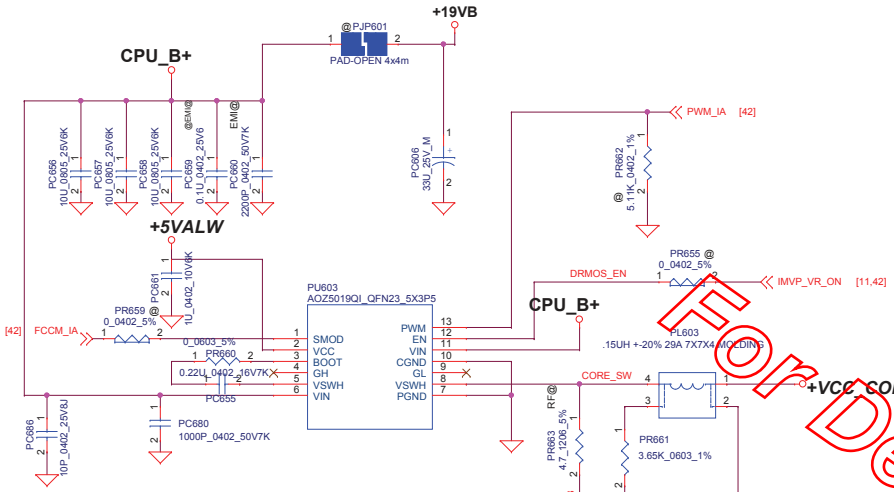
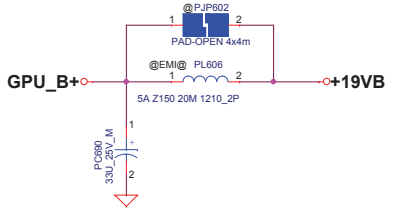
VCC_core
U22 - 15W
Loadline : 2.4m-ohm

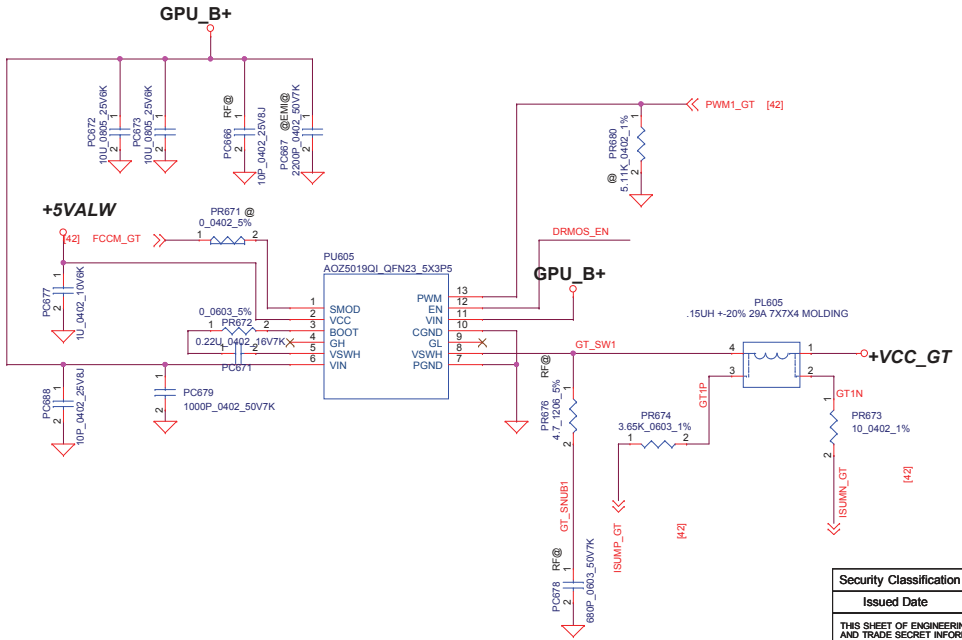
TDC 21A
Peak Current 29A
OCP current 34A
Choke DCR 0.66 +-7%m ohm

VCC_GT
U22 - 15W
Loadline : 3.1m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7%m ohm







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Title: PWR_+VCC_core and +VCC_GT

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VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+220u_D2*2 pcs

+VCC_CORE

VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +330u_D2*1 pcs

+VCC_GT

VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs

+VCC_SA

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Title: PWR_CPU&VGA bulk and MLCC

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		X00(0.1)

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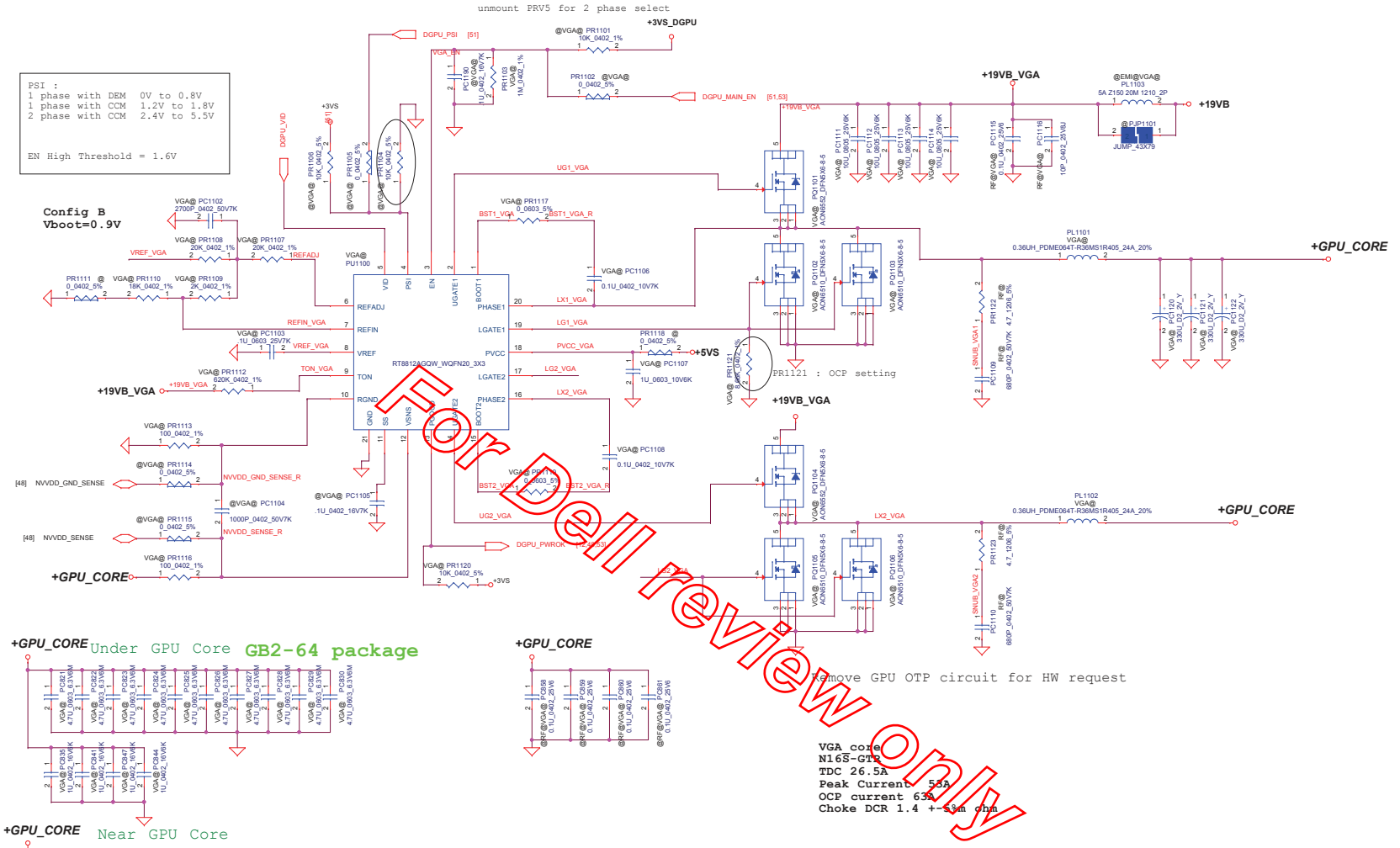

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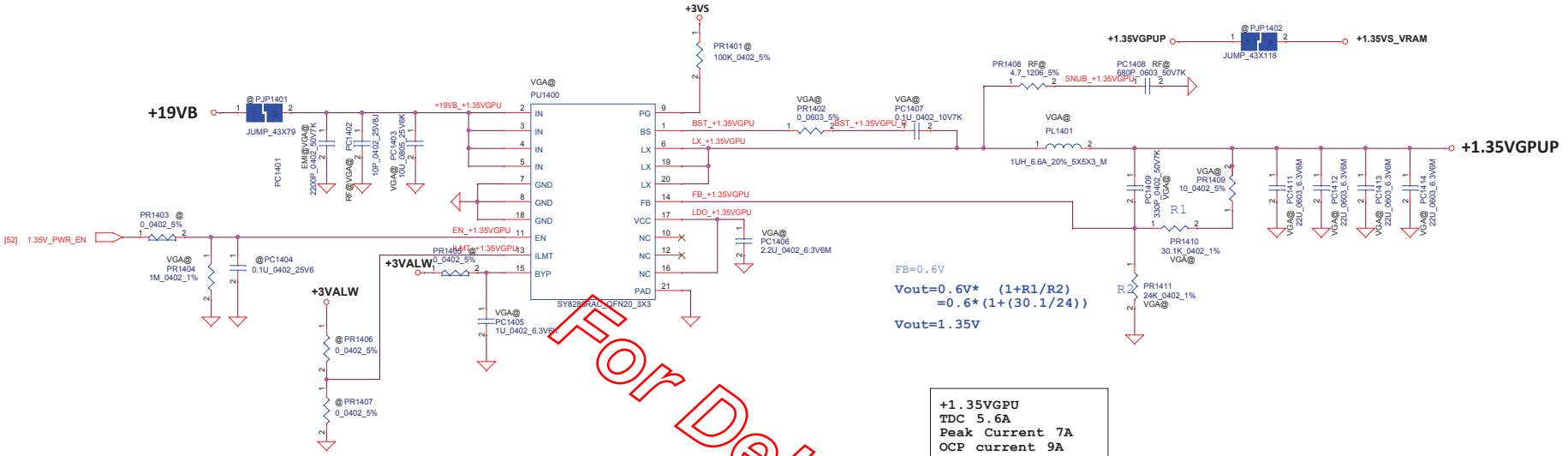

+1.35VGPUP
TDC 5.6A
Peak Current 7A
OCP current 9A

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin13)
6A	Pull low
9A	Floating
12A	Pull high

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Title: PWR +1.35VGPU

Size | Document Number | Rev 0.1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P37	PWR	20160303	COMPAL	to change charger IC	change charger IC(PU703) to ISL88739	0.2(X00)

2	P39
	P43
	P45
	P46
		PWR	20160303	COMPAL	to prevent RF issue	add PC208
						add PC666,PR676,PC678
						add PC1116,PR1122,PC1109,
						add PC1402,PR1408,PC1408	

3	P42	PWR	20160303	COMPAL	to adjust +VCC_CORE and +VCC_GT load line	change PR622 to 1.91K,PR638 to 287 ohm,PC626 to 0.1uF,PC642 to 0.1uF	
4	P36,P42	PWR	20160303	COMPAL	to save layout space	delete PL3,PL602(reserve location)	
5	P36	PWR	20160303	COMPAL	to fix battery connector ME issue	to change battery connector	
6	P37	PWR	20160304	COMPAL	to fix Temp/Voltage 19.5V DC-IN issue	change PR732 to 53.6K	
7	P44	PWR	20160304	COMPAL	to fix DFB solder open problem	change PC1127,PC1062,PC1128 footprint	
8	P38	PWR	20160308	COMPAL	to prevent OTP functions abnormal issue	to reserve PQ102 and connect to ALL_SYS_PWRGD	
9	P37	PWR	20160316	COMPAL	to save layout space by EMI request	change PC760,PC762,PC763,PC764 to 0603 size and delete PR766,PC767	
10	P43	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's load line	to unmount PC624 and PC646	
11	P44	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's output MLCC's location(only change BOM) and bulk cap	unmount:PC1021,PC1135,PC1133,PC1131,PC1022,PC1025,PC1027, PC1028,PC1063, PC1008,PC1003,PC1011,PC1072,PC1076,PC1071,PC1081,PC1082,PC1004, PC1007,PC1012 to mount:PC1176,PC1175,PC1177,PC1179,PC1178,PC1180,PC1183,PC1184, PC1170,PC1173,PC1174 to change PC1127,PC1062 to 220uF/9m ohm	
12	P36	PWR	20160429	COMPAL	To improve EMI and reduce inrush current to mount π filter' s bead and change cap	unmount:PL1,PL4 change PC2,PC4 to 100pF	
13	P37	PWR	20160429	COMPAL	ISL88739 doesn't support PSYS function	unmount PR727 change PR774 to 1K ohm change PC748 0.1uF	0.3(X02)
14	P39	PWR	20160429	COMPAL	to adjust 1.2V OCP to 10.2A	change PR205 to 11K	
15	P37	PWR	20160429	COMPAL	to aviod inrush to damage MOS	to reserve PQ741	

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Title: PWR Change list

Size | Document Number | Rev

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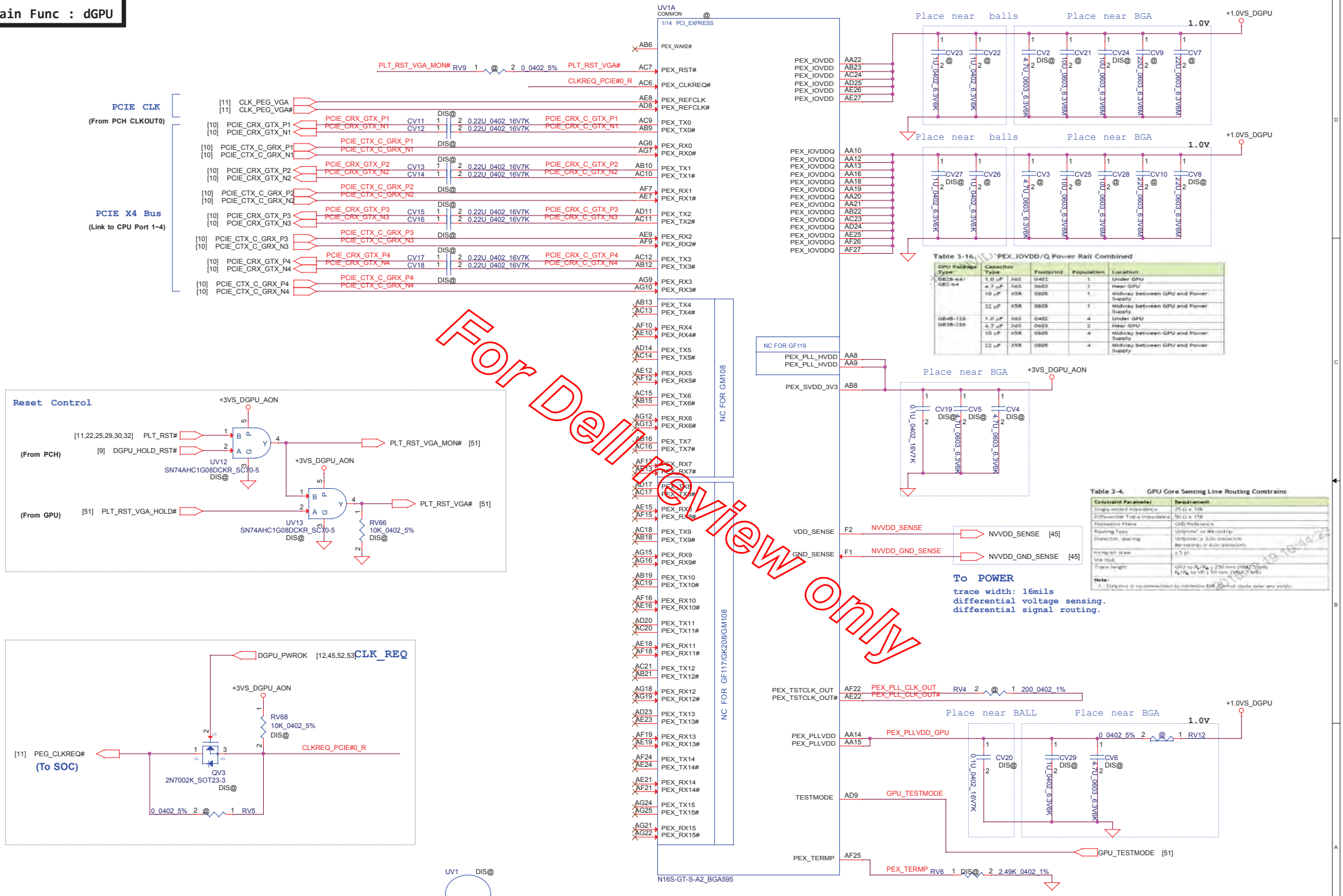
Main Func : dGPU



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Size: Custom | Document Number: LA-C071P | Rev: 0.2

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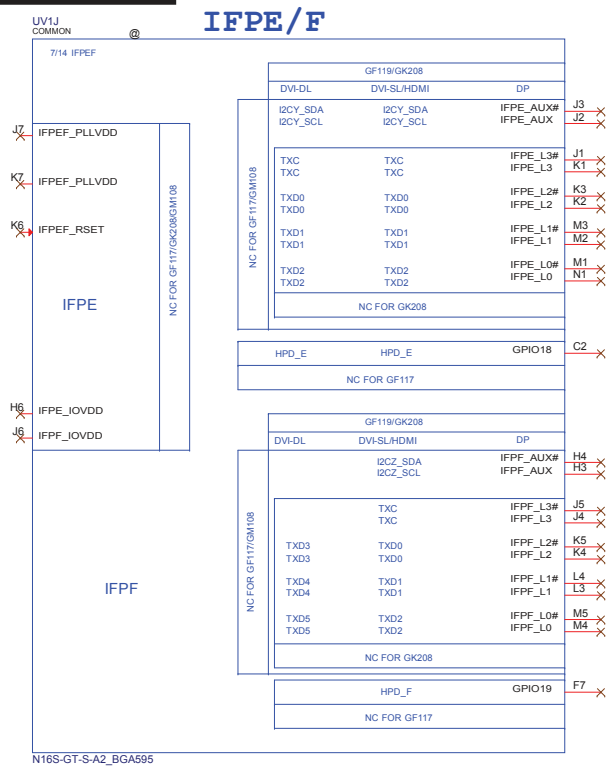
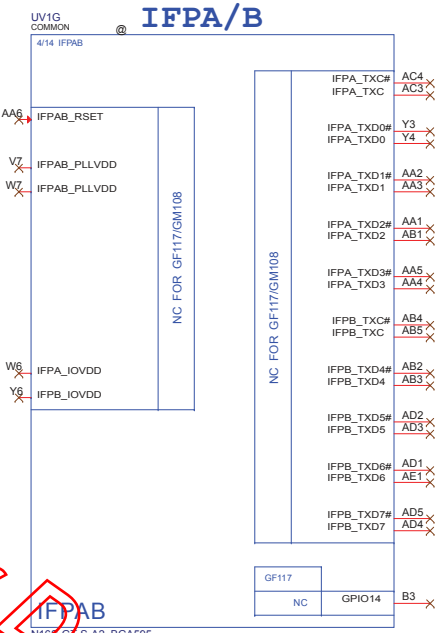
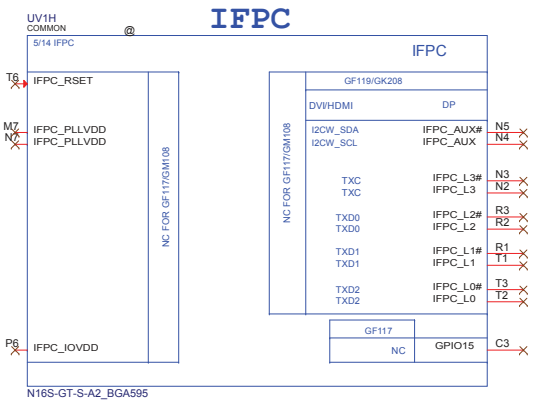
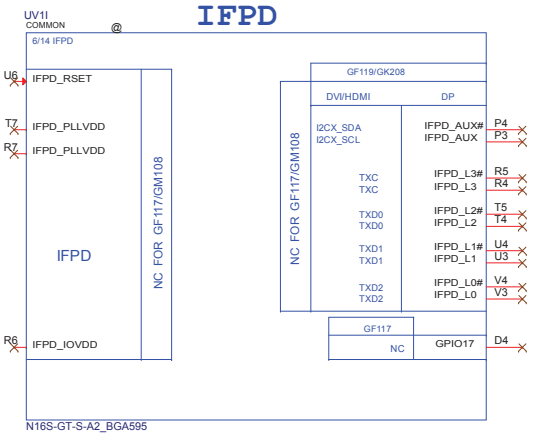
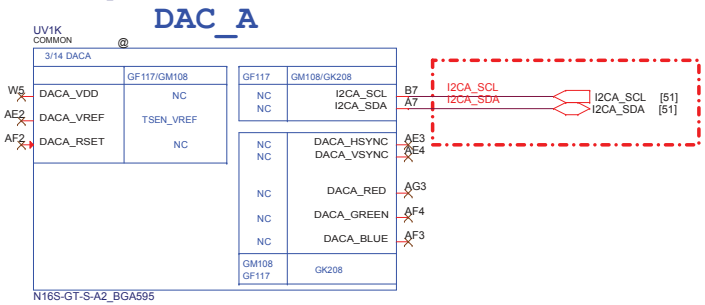
Main Func : dGPU

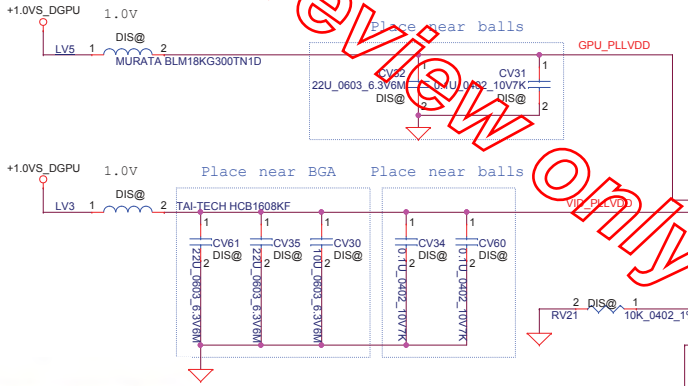












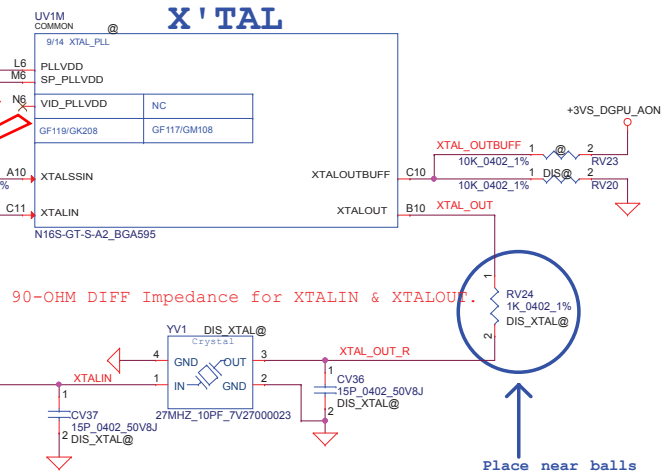


Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:

1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

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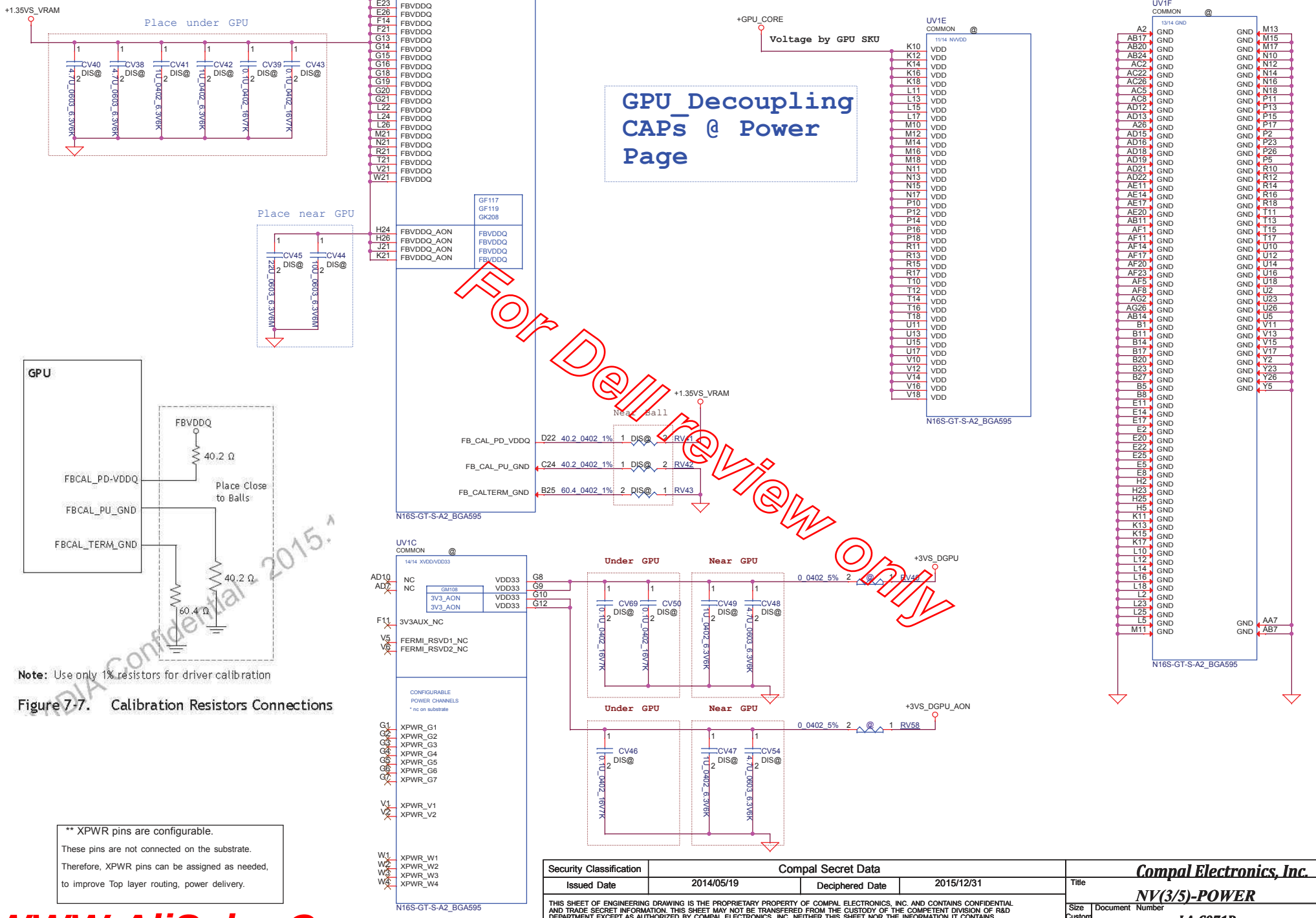
Main Func : dGPU



Note: Use only 1% resistors for driver calibration

Figure 7-7. Calibration Resistors Connections

** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed, to improve Top layer routing, power delivery.

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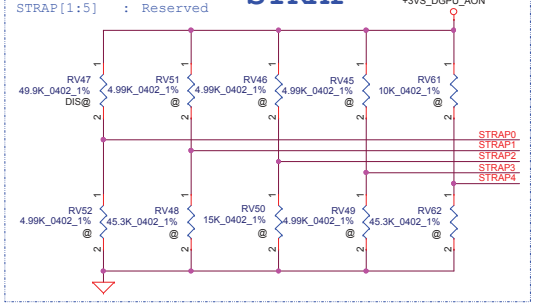
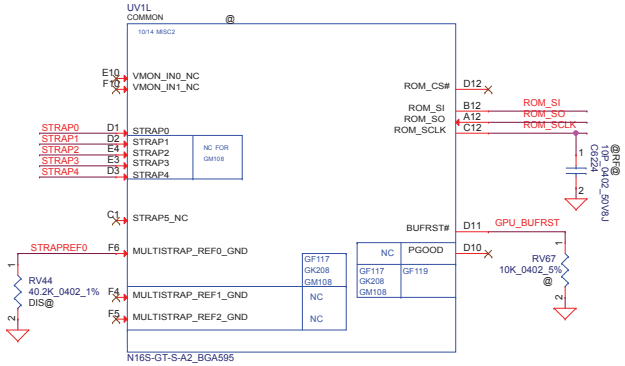
Title: NV(3/5)-POWER			
Size: Custom	Document Number: LA-C071P		Rev: 0.2
Date: Monday, June 06, 2016	Sheet 50 of 55		

Main Func : dGPU

STRAP

STRAP0 : PU 49.9K (50K)
STRAP[1:5] : Reserved

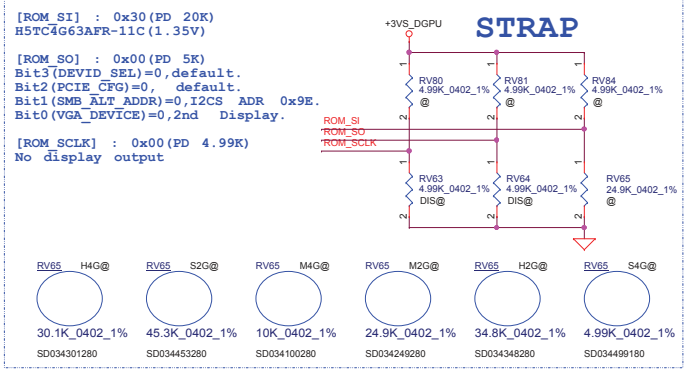




[ROM_SI] : 0x30(PD 20K)
H5TC4G63AFR-11C(1.35V)

[ROM_SO] : 0x00(PD 5K)
Bit3(DEVID_SEL)=0,default.
Bit2(PCIE_CFG)=0, default.
Bit1(SMB_ALT_ADDR)=0,I2CS ADR 0x9E.
Bit0(VGA_DEVICE)=0,2nd Display.

[ROM_SCLK] : 0x00(PD 4.99K)
No display output



Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Type		RAM_CFG[3:0] (ROM_SI)	BKD40 /BKA40
K4G80325FB-HC28	S4G@	0x0(PD 4.99K)	
MT51J256M32HF-70:A	M4G@	0x1(PD 10K)	
EDW4032BABG-70-F	M2G@	0x4(PD 24.9K)	V (SSI)
H5GC4H24AJR-R0C	H2G@	0x6(PD 34.8K)	
K4G41325FE-HC28	S2G@	0x7(PD 45.3K)	
H5GC8H24MJR-R0C	H4G@	0x5(PD 30.1K)	

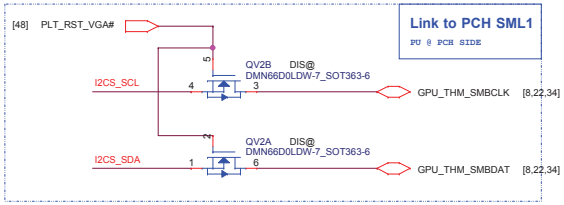
Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

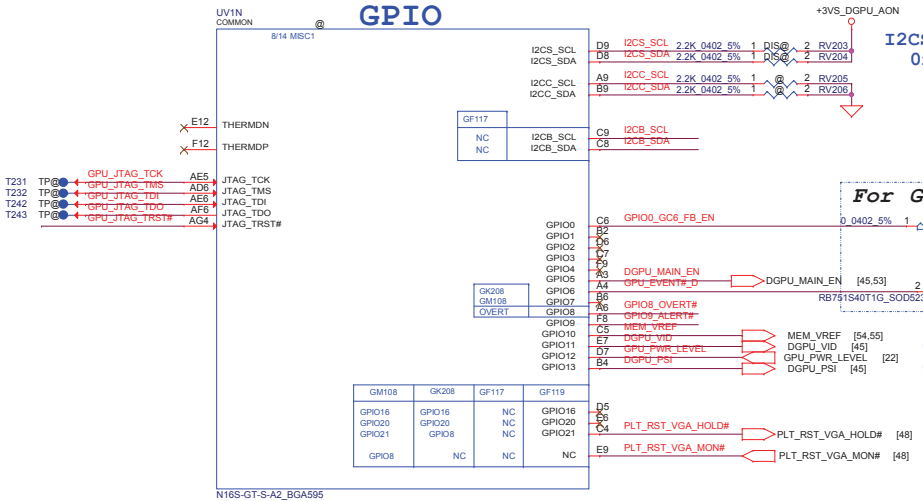
10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful I²CS Slave addresses can be used with SMB_ALT_ADDR strapping.

Internal Thermal Sensor

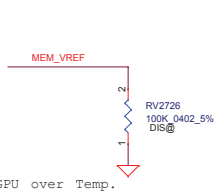


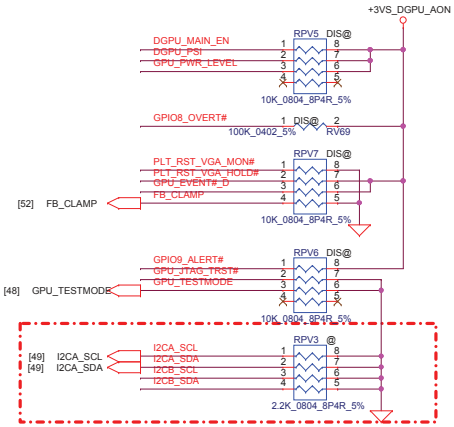
GPIO



I2CS SMBUS:
0x96 and 0x9E(Default)

For GC6 2.0





VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

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Title: NV(4/5)-GPIO/Strap

Size: Custom | Document Number: LA-C071P | Rev: 0.2

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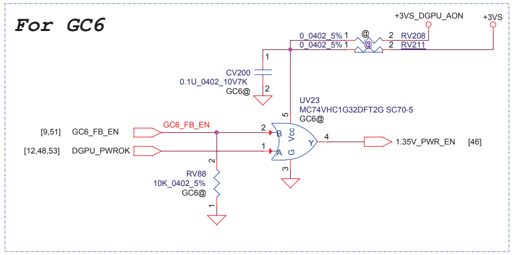
Main Func : dGPU

For GC6



From DG-07158-001_v05_secured(NVDIA Spec)

Table 7-3. Supported GDDR5 Command Mappings by GPU and Package

Package	Supported CMD Mapping	Benefits
GB2-64	H	4-signal layers fan-out
GB2B-64	H	4-signal layers fan-out
GB4B-128	H	4-signal layers fan-out
GB3B-256	F	4-signal layers fan-out

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	**Channel 0 & 1**		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.

Note:
- GB2-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel 0 data bits [31:0] can be left unconnected.
- For 32-bit implementation on GB2-64, please inform account AE for VBIOS support.

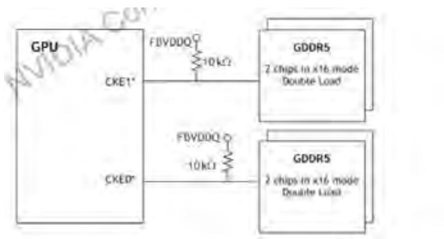


Figure 7-5. Clock Enable (CKE*) Signal Connection, ×16 Mode

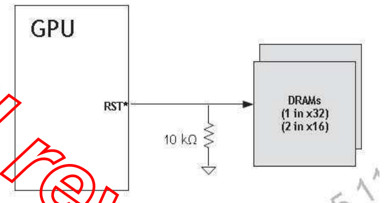


Figure 7-3. Reset Signal Connection

7.1.13 FBx_Debug0/1

The FBx_Debug0/1 signals are used for debug purposes only. These debug signals are on CMD34 and CMD35. Reserve a footprint for a 0402 package size pull-up resistor to FBVDDQ on each FBx_Debug0/1 signal. The resistor should be no-stuffed for normal operation.

7.1.14 DBI/EDC

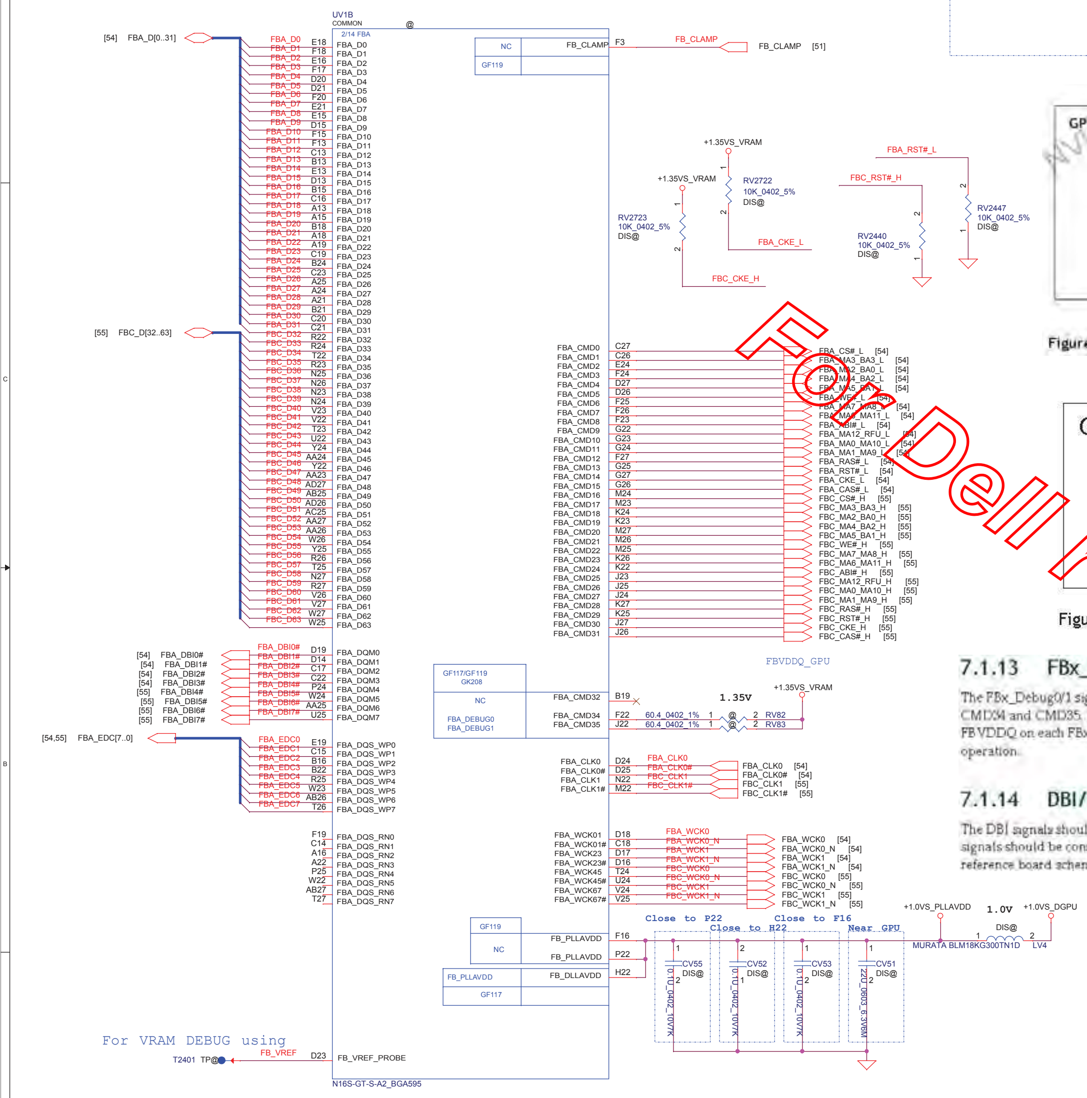
The DBI signals should be connected to the GPU balls named FBx_DQMx. The EDC signals should be connected to the GPU balls named FBx_DQS_WPx. Refer to the reference board schematics for detailed connections.

Table 7-6. Memory-Side Termination

Signal	Termination	Notes
DQ, DBI, CMD, ADDR	ODT	ODT impedance set using an external resistor (ZQ). Digitally adjustable to ZQ or ZQ/2 based on loading consideration
WCK	ODT	Single-ended (60 Ω to FBDDQ) ODT is supported by DRAM.
CK	External, termination on the board is required.	ODT is NOT supported by DRAMs.

Table 7-7. GPU-Side Termination

Signal	Termination	Notes
DQ, DBI	ODT	40 Ω pull-up, fixed. Disabled during low performance states.



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: NV(5/5)-MEMORY FBA

Size: Custom | Document Number: LA-C071P | Rev: 0.2

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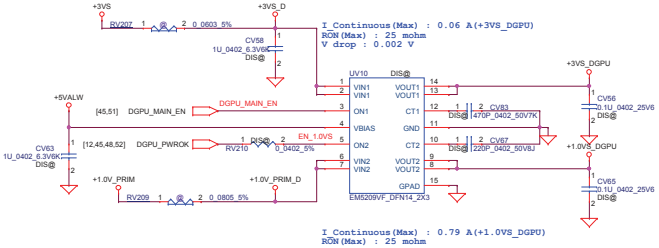
Main Func : dGPU

+3VS to +3VS_DGPU



+1.0V_PRIM to +1.0VS_DGPU

+3VS to +3VS_DGPU_AON

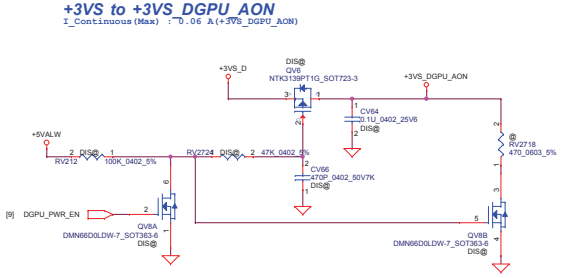


Table 5. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]	3.3V Total
		–	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5	26.5	–	2.0	–	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 3-8. Power Rail Specification for GDDR5 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDD/FBVDDQ	1.35, 1.50V, or 1.50 V memory with DVS[1] support at 1.35V
FBVDD/FBVDDQ switching time	<=64 µs
DC Tolerance	± 3%
AC Tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW
GPU FBVREF [2]	Internal VREF
Memory FBVREF	0.7 x FBVDDQ when termination is enabled 0.5 x FBVDDQ when termination is disabled

Note:
1. DVS = Dynamic Voltage Switching.
2. Since the GPU internal VREF is used, the FBVREF pin on the GPU can be left unconnected.

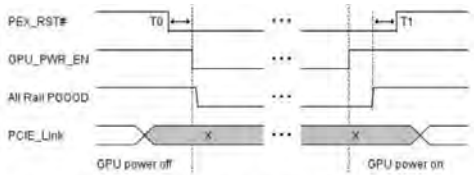


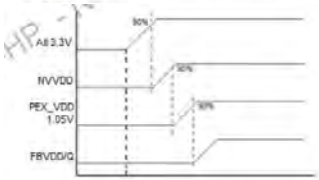
Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Chapter 3

- Added 1.0V support to PEX_VDD and all 1.05V Power Rails



Notes: All 3.3V includes all rails powered at 3.3V
PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.

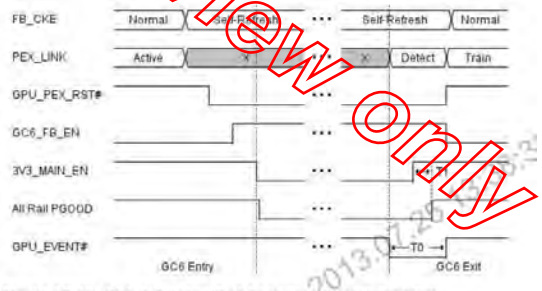


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title	DGPU_DC/DC Interface		
Size	Document Number		Rev 0.2
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Memory Partition A- Lower 32 bit

MF=0

MF=1

ZQ = 121 Ω, 1%, 0402

W=16mils

Table 7-12. CK External Termination

Component	Value
R1	80 Ω, 1%, 0402

Table 7-14. VREF Configuration

Configuration	Requirement	Notes
×32	Share one Vref-C circuit for two memory parts.	GDDR5 DRAMs have internal VREF for DQ, DBI, EDC (VREF-D).
×16	Share one VREF-C circuit for four memory parts.	Command, Address VREF (VREF-C) needs to be externally supplied since DRAMs do NOT internally generate VREF for these signals.

7.1.12.1 VREF-D

VREF-D pins can be left floating.

7.1.12.2 VREF-C

VREF-C connections for the ×16 mode are shown in Figure 7-8.

Figure 7-8. VREF-C Connections for ×16 Mode

Security Classification	Compal Secret Data	
Issued Date	2015/01/06	Deciphered Date 2016/01/06

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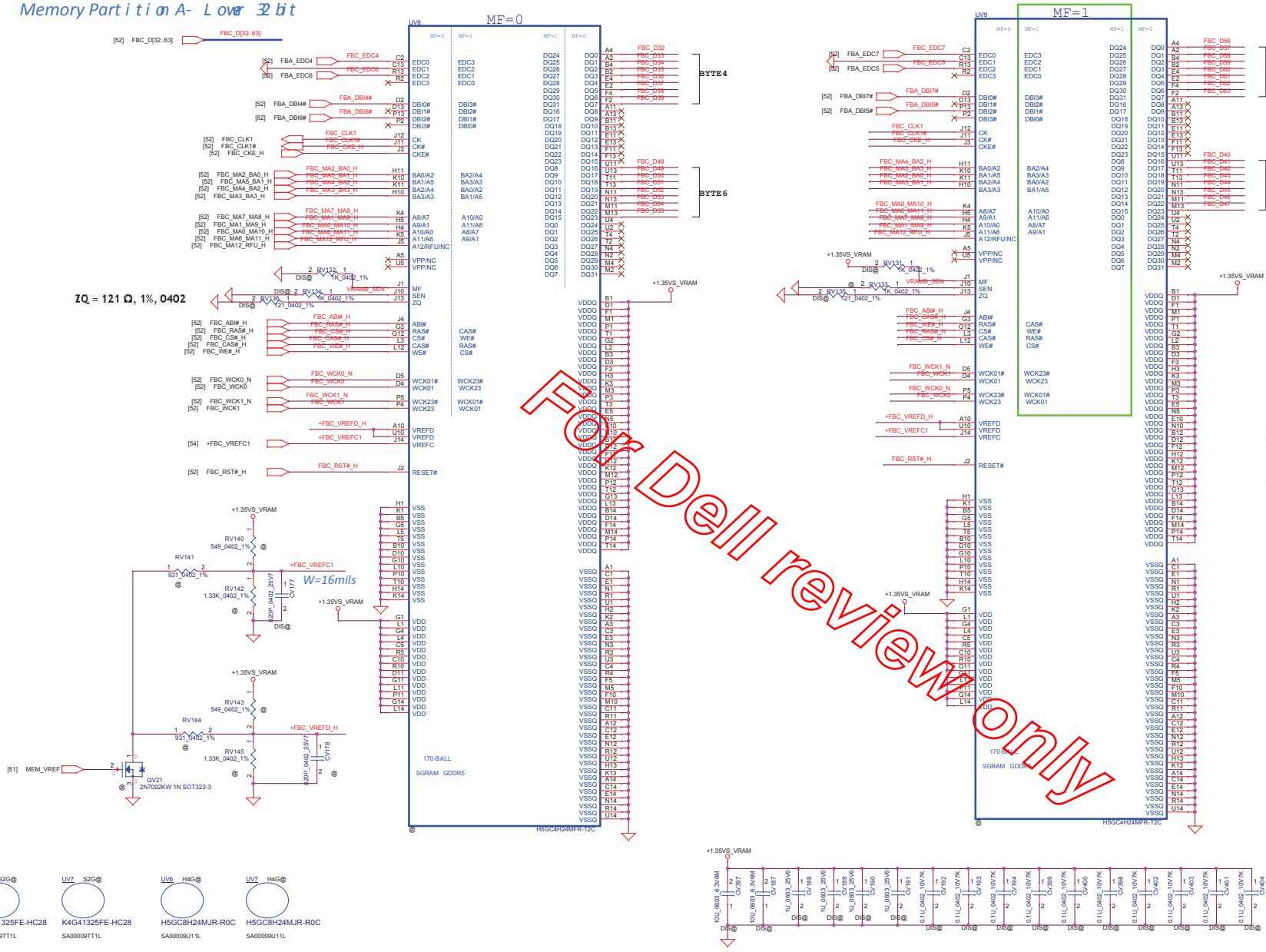
Title: N16P_GDDR5_A

Size: | Document Number: Thor | Rev: 0.1

Date: Monday, June 06, 2016 | Sheet 54 of 55

Memory Partition A- Lower 32 bit



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7.1.12.2 VREF-C

VREF-C connections for the ×16 mode are shown in Figure 7-8.

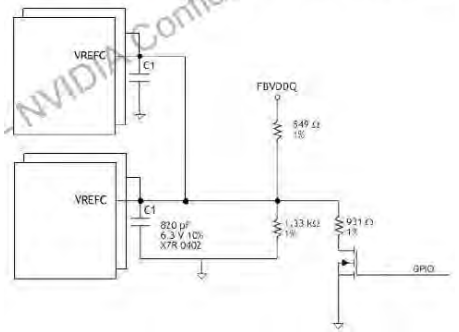

Figure 7-8. VREF-C Connections for ×16 Mode

UV6 S2G@	UV7 S2G@	UV6 H4G@	UV7 H4G@
K4G41325FE-HC28	K4G41325FE-HC28	H5GC8H24MJR-R0C	H5GC8H24MJR-R0C
SA00009TT1L	SA00009TT1L	SA00009U11L	SA00009U11L
UV8 S2G@	UV9 S2G@	UV8 H4G@	UV9 H4G@
K4G41325FE-HC28	K4G41325FE-HC28	H5GC8H24MJR-R0C	H5GC8H24MJR-R0C
SA00009TT1L	SA00009TT1L	SA00009U11L	SA00009U11L

Security Classification	Compal Secret Data		
Issued Date	2015/01/06	Deciphered Date	2016/01/06

Compal Electronics, Inc.	
Title	N16P_GDDR5_B
Size	Document Number: LA-C901P
Rev	0.1
Date:	Monday, June 06, 2016
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