COMPAL CONFIDENTIAL

MODEL NAME : DAZ40
PCB NO : LA-F322P
BOM P/N : 431A8U31L0X

Steamboat MLK 14" NonAR

Kabylake-U U22 & Kabylake-R U42

2017-12-29

REV : 2.0 (A01)

@ : Nopop Component

EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CXDP@ : XDP Component
CONN@ : Connector Component
ESPI@ : ESPI interface Component
LPC@ : External ESPI Component (SHD)
INFI@ : Infinity SKU Component
U42@ : KBL-R U42 Component
U22@ : KBL-R U22 Component
DS3@ : Deep sleep Component
NDS3@ : Non Deep sleep Component
546@ : TI TUSB546 Component
8743@ : PARADE PS8743 Component

MB PCB

Part Number	Description
DA8001CH010	PCB 265 LA-F322P REV0 MB NAR 1

Layout Dell logo

REV:A01
PWB: YWCKR

Power CKT : 0920
GPIO map : 0821

Compal Electronics, Inc.

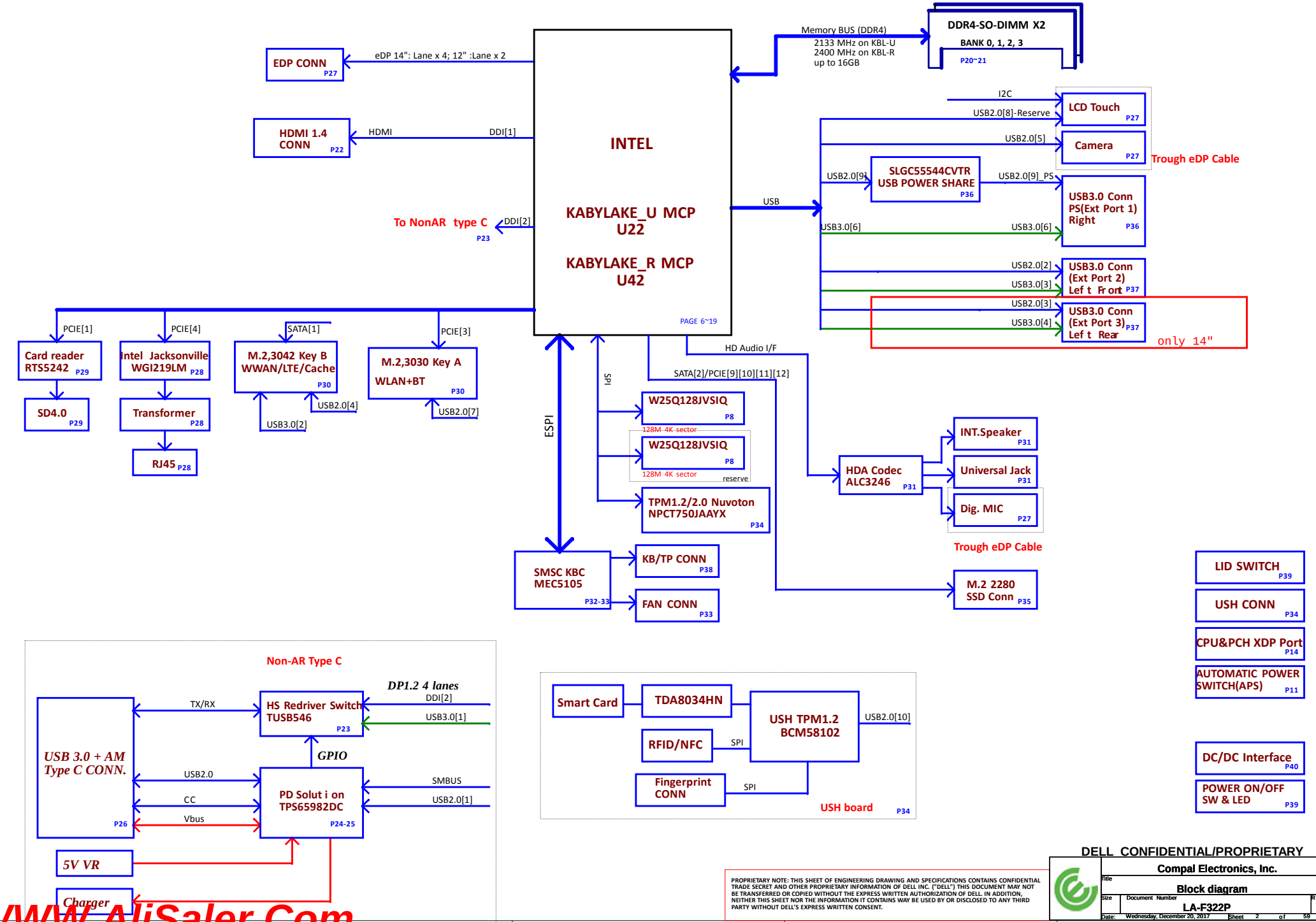
Title: Cover Sheet

Size: | Document Number: LA-F322P | Rev: 2.0

Date: Friday, December 29, 2017 | Sheet 1 of 59

Steamboat MLK 14 w/o AR Block Diagram

Steamboat MLK 12&13 only support one DIMM
Reverse Type



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Title	Block diagram
Size	Document Number: LA-F322P
Rev	2.0
Date:	Wednesday, December 20, 2017
Sheet	2 of 59

NonAR config

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.0mm ± 10%)			39.4		41.40000
					1.05156

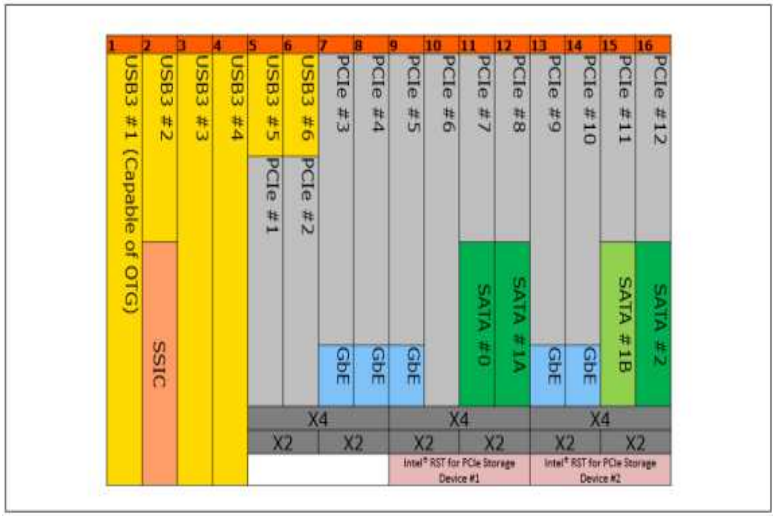
AR use 1086PP (10L)
Non AR use 1080PP (8L)

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				Typce-C(Non AR)
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left Front
USB3.0-4				JUSB3-->Left Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader (PCIE)
USB3.0-6		PCIE-2		JUSB1-->Right
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	NA
		PCIE-8	SATA-1	M.2 3042(SATA Cache)
		PCIE-9		M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-1*	
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	Typce-C(Non AR)
2	JUSB2-->Left Front
3	JUSB3-->Left Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	JUSB1-->Right
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U

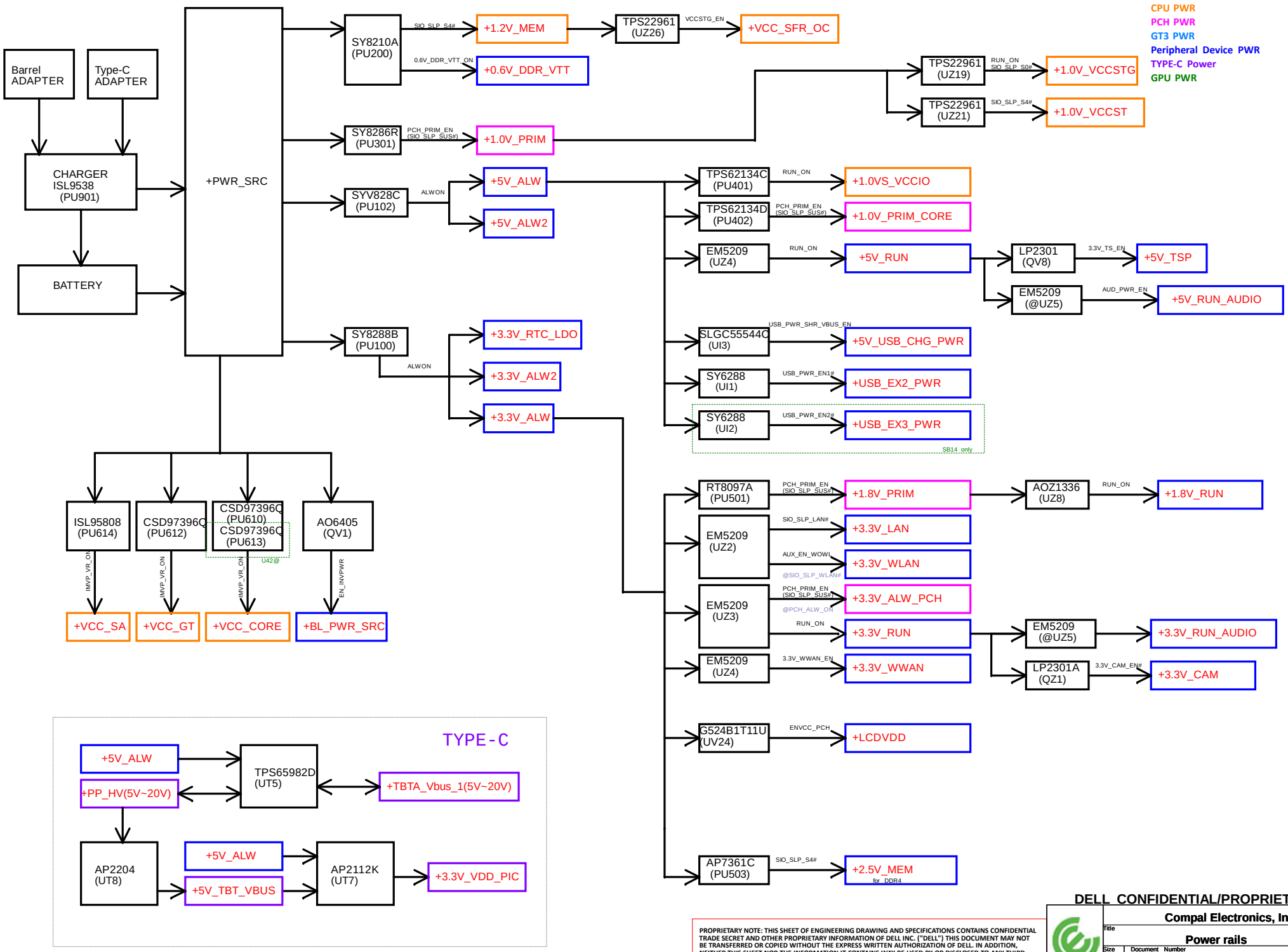


Compal Electronics, Inc.

Title: Port assignment

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 3 of 59



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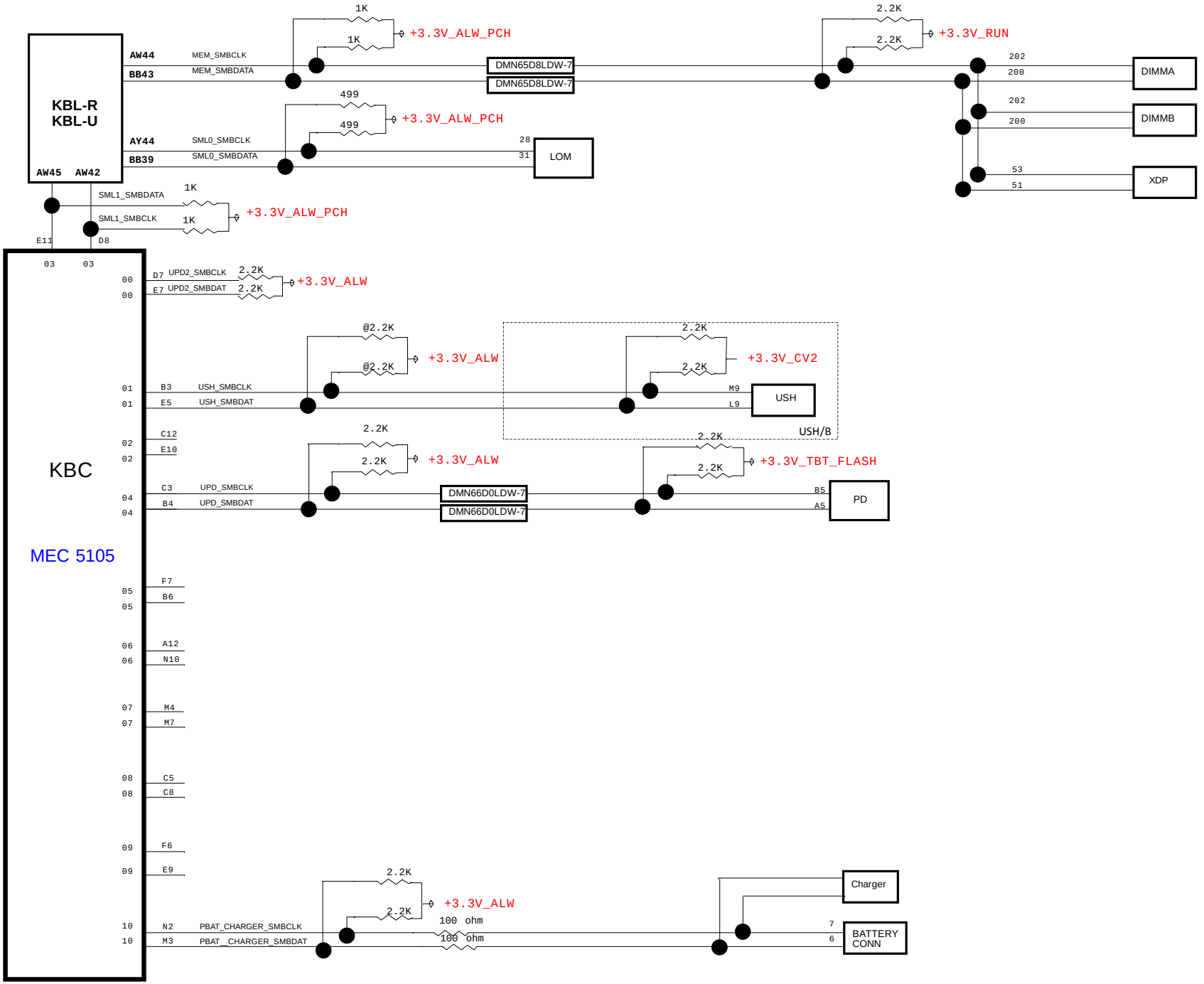
Title: Power rails

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 4 of 59

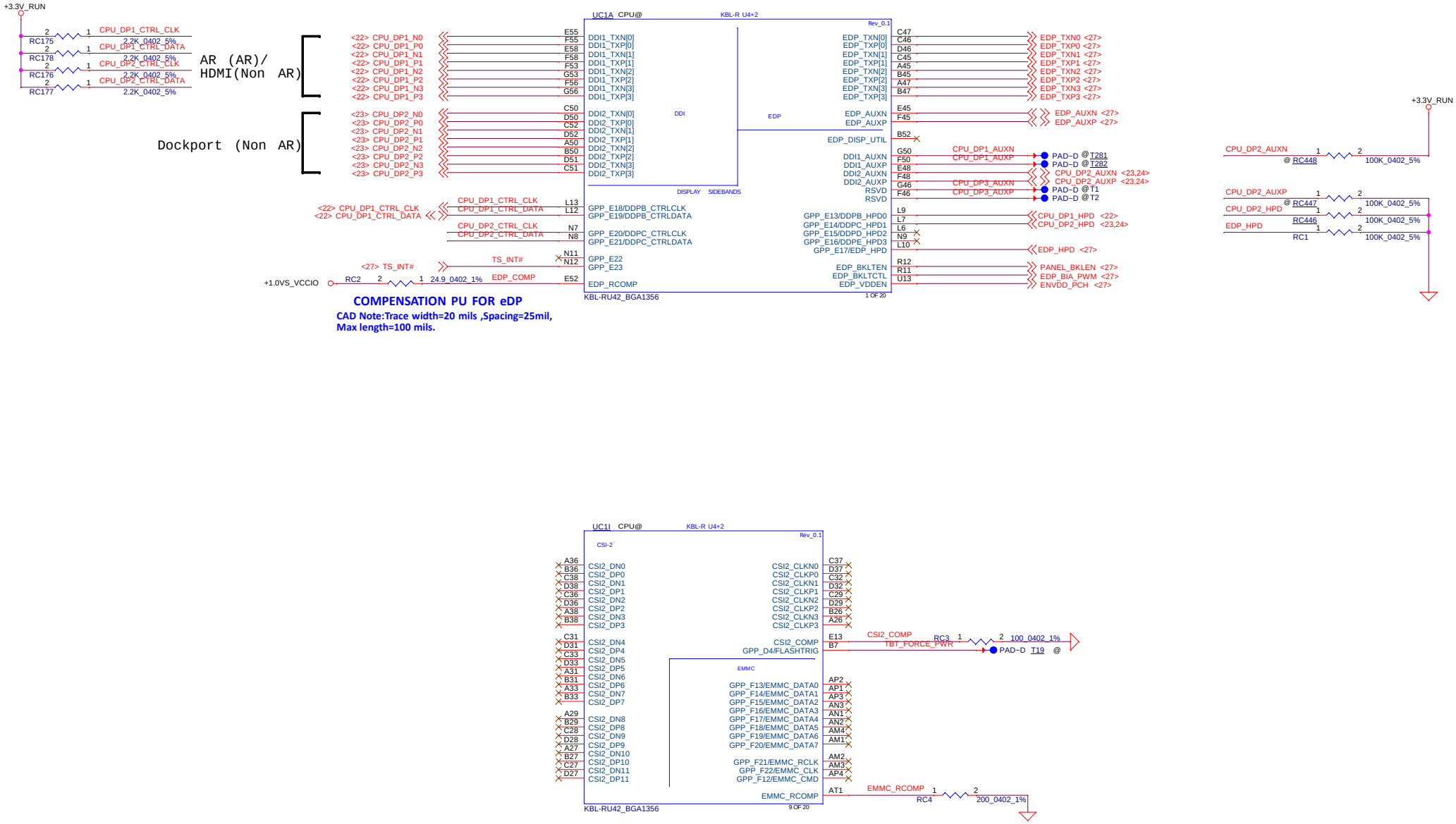


Compal Electronics, Inc.

Title: Port assignment

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 5 of 59



Compal Electronics, Inc.

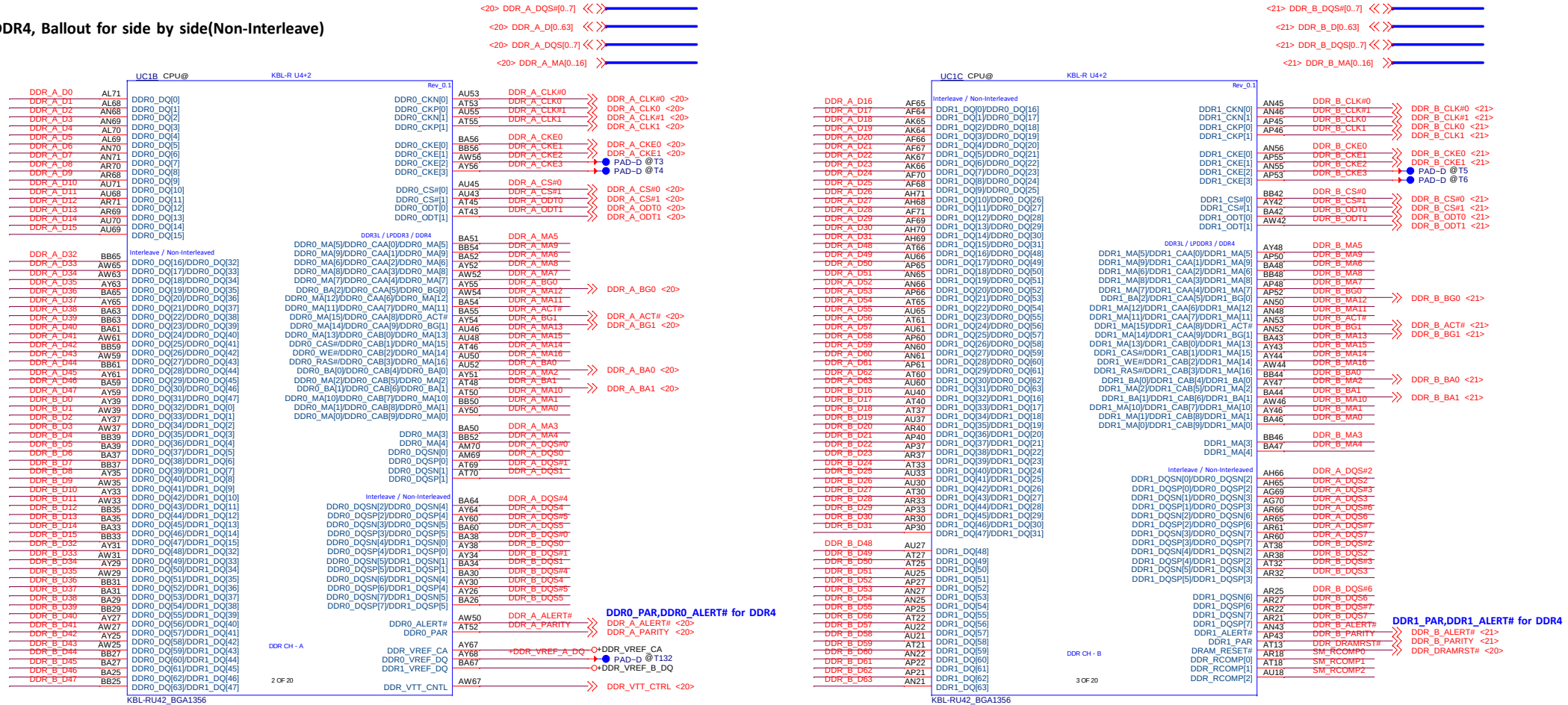
Title: CPU (1/14)

Size | Document Number: LA-F322P | Rev: 2.0

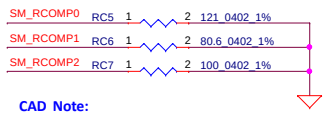
Date: Wednesday, December 20, 2017 | Sheet 6 of 59

For DDR4

DDR4, Ballot for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Title: CPU (2/14)

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 7 of 59

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

UC1E CPU@ KBL-R U4+2

SPI - FLASH

PCH_SPI_CLK AV2 SPI0_CLK
PCH_SPI_D1 AW3 SPI0_MISO
PCH_SPI_D0 AV3 SPI0_MOSI
PCH_SPI_D2 AW2 SPI0_IO2
PCH_SPI_D3 AU4 SPI0_IO3
PCH_SPI_CS#0 AU3 SPI0_CS0#
PCH_SPI_CS#1 AU2 SPI0_CS1#
PCH_SPI_CS#2 AU1 SPI0_CS2#

<14> PCH_SPI_DO_XDP
<14> PCH_SPI_DO2_XDP
CXDP@RC10 1 2 1K_0402_1%
CXDP@RC11 1 2 1K_0402_1%
<34> PCH_SPI_CS#2

SPI - TOUCH

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C LINK

G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

<30> PCH_CL_CLK1
<30> PCH_CL_DATA1
<30> PCH_CL_RST1#

AW13 GPP_A0/RCIN#
AY11 GPP_A6/SERIRQ

<32> ESPI_ALERT#
+3.3V_1.8V_ESPI RC21 2 1 8.2K_0402_1%

KBL-RU42_BGA1356 5 OF 20

SMBUS, SMLINK

R7 GPP_C0/SMBCLK MEM_SMBCLK
R8 GPP_C1/SMBDATA MEM_SMBDATA
R10 GPP_C2/SMBALERT# PCH_SMB_ALERT#

R9 GPP_C3/SML0CLK SML0_SMBCLK
W2 GPP_C4/SML0DATA SML0_SMBDATA
W1 GPP_C5/SML0ALERT# GPP_C5

SML0_SMBCLK <28>
SML0_SMBDATA <28>

W3 GPP_C6/SML1CLK SML1_SMBCLK
V3 GPP_C7/SML1DATA SML1_SMBDATA
AM7 GPP_B23/SML1ALERT#/PCHHOT# GPP_B23

SML1_SMBCLK <32>
SML1_SMBDATA <32>

LPC

AY13 GPP_A1/LAD0/ESPI_IO0 ESPI_IO0_R
BA13 GPP_A2/LAD1/ESPI_IO1 ESPI_IO1_R
BB13 GPP_A3/LAD2/ESPI_IO2 ESPI_IO2_R
AY12 GPP_A4/LAD3/ESPI_IO3 ESPI_IO3_R
BA12 GPP_A5/LFRAME#/ESPI_CS#
BA11 GPP_A14/SUS_STAT#/ESPI_RESET#

RC3661 2 15_0402_5% ESPI_IO0 <32,33>
RC3671 2 15_0402_5% ESPI_IO1 <32,33>
RC3681 2 15_0402_5% ESPI_IO2 <32,33>
RC3691 2 15_0402_5% ESPI_IO3 <32,33>
ESPI_CS# <32,33>
ESPI_RESET# <32,33>

AW9 GPP_A9/CLKOUT_LPC0/ESPI_CLK ESPI_CLK
AY9 GPP_A10/CLKOUT_LPC1 PCI_CLK_LPC1
AW11 GPP_A8/CLKRUN# CLKRUN#

EMI@ RC16 1 2 15_0402_5%
@RC22 1 2 22_0402_5%
ESPI_CLK_5105 <32,33>

CHECK LPC_CLK FOR DEBUG CARD?

+3.3V_RUN
MEM_SMBCLK 6 1 DDR_XDP_WAN_SMBCLK <14,20,21>
QC2A DMN65D8LDW-7_SOT363-6
MEM_SMBDATA 3 4 DDR_XDP_WAN_SMBDAT <14,20,21>
QC2B DMN65D8LDW-7_SOT363-6

+3.3V_RUN
DDR_XDP_WAN_SMBDAT RC318 2.2K_0402_5%
DDR_XDP_WAN_SMBCLK RC319 2.2K_0402_5%
+3.3V_ALW_PCH
MEM_SMBCLK RC12 1K_0402_5%
MEM_SMBDATA RC14 1K_0402_5%
SML1_SMBCLK RC15 1K_0402_5%
SML1_SMBDATA RC17 1K_0402_5%
SML0_SMBCLK RC347 499_0402_1%
SML0_SMBDATA RC348 499_0402_1%

Reserve

+3.3V_LAN
SML0_SMBCLK @RC19 499_0402_1%
SML0_SMBDATA @RC20 499_0402_1%

CLKRUN# LPC@ RC27 8.2K_0402_5%

SOFTWARE TAA

PCH_SPI_CLK_1_R
PCH_SPI_CLK_0_R
33_0402_5% @EMI@ RC28
33P_0402_50V8J @EMI@ CC7
33_0402_5% @EMI@ RC29
33P_0402_50V8J @EMI@ CC8

+3.3V_SPI
@RC30 PCH_SPI_D2_R1 1K_0402_5%
@RC31 PCH_SPI_D3_R1 1K_0402_5%
@RC316 PCH_SPI_D3_R1 1K_0402_5%
03/02:follow Intel MOW_2015WW06

RPC1
<34> PCH_SPI_D1_R1
<34> PCH_SPI_D0_R1
<34> PCH_SPI_CLK_R1
PCH_SPI_D3_R1
PCH_SPI_D1_0_R
PCH_SPI_D0_0_R
PCH_SPI_CLK_0_R
PCH_SPI_D3_0_R
33_0804_8P4R_5%

PCH_SPI_D3_R1 @RC407 33_0402_5% PCH_SPI_D3_1_R
PCH_SPI_CLK_R1 @RC408 33_0402_5% PCH_SPI_CLK_1_R
PCH_SPI_D0_R1 @RC409 33_0402_5% PCH_SPI_D0_1_R
PCH_SPI_D1_R1 @RC410 33_0402_5% PCH_SPI_D1_1_R

RF Request
ESPI_CLK_5105 @RF@ CC316 33P_0402_50V8J
SML0_SMBCLK @RF@ CC318 33P_0402_50V8J
SML1_SMBCLK @RF@ CC319 33P_0402_50V8J
MEM_SMBCLK @RF@ CC320 33P_0402_50V8J
Place close CPU side

+3.3V_ALW_PCH
PCH_SMB_ALERT# RC23 2.2K_0402_5%

TLS CONFIDENTIALITY
HIGH ENABLE
LOW(DEFAULT) DISABLE
WEAK INTERNAL 20K PD

+3.3V_ALW_PCH
GPP_C5 ESPI@RC25 4.7K_0402_5%

EC interface
HIGH ESPI
LOW(DEFAULT) LPC
WEAK INTERNAL 20k PD

+3.3V_ALW_PCH
GPP_B23 RC317 150K_0402_5%

EXI BOOT STALL BYPASS
HIGH ENABLED
LOW(DEFAULT) DIABLED
WEAK INTERNAL PD

128Mb Flash ROM
UC5
+3.3V_SPI
CC9 0.1U_0201_10V6K
PCH_SPI_CS#0_R1 @RC37 0_0402_5%
PCH_SPI_D2_R1 RC39 33_0402_5%
PCH_SPI_CS#0_R2
PCH_SPI_D1_0_R
PCH_SPI_D2_0_R
/CS VCC
IO1 IO3
IO2 CLK
GND IO0
PCH_SPI_D3_0_R
PCH_SPI_CLK_0_R
PCH_SPI_D0_0_R
W25Q128JVSIQ_SO8

128Mb Flash ROM
@UC6
+3.3V_SPI
@CC10 0.1U_0201_10V6K
PCH_SPI_CS#1_R1 @RC42 0_0402_5%
PCH_SPI_D2_R1 @RC43 33_0402_5%
PCH_SPI_CS#1_R2
PCH_SPI_D1_1_R
PCH_SPI_D2_1_R
/CS VCC
IO1 IO3
IO2 CLK
GND IO0
PCH_SPI_D3_1_R
PCH_SPI_CLK_1_R
PCH_SPI_D0_1_R
W25Q128JVSIQ_SO8

JSPI1 CONN@
PCH_SPI_CS#1_R1 @RC32 0_0402_5% PCH_SPI_CS#1
PCH_SPI_D0_R1 @RC33 0_0402_5% PCH_SPI_D0
PCH_SPI_D1_R1 @RC34 0_0402_5% PCH_SPI_D1
PCH_SPI_CLK_R1 @RC35 0_0402_5% PCH_SPI_CLK
PCH_SPI_CS#0_R1 @RC36 0_0402_5% PCH_SPI_CS#0
PCH_SPI_D2_R1 @RC38 0_0402_5% PCH_SPI_D2
PCH_SPI_D3_R1 @RC40 0_0402_5% PCH_SPI_D3
+3.3V_SPI
+3.3V_ALW_PCH @RC41 0_0402_5%
GND1 GND2
CVILU_CF5020FD0R0-05-NH

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Title: CPU (3/14)
Size: Document Number: LA-F322P
Rev: 2.0
Date: Wednesday, December 20, 2017 Sheet 8 of 59

For BR/SB

UC1F CPU@ — KBL-R U4+2 — KBL-RU42_BGA1356 — 6 OF 20

LPSS: GPP_B15/GSPI0_CS# AN8; GPP_B16/GSPI0_CLK AP7; GPP_B17/GSPI0_MISO AP8; GPP_B18/GSPI0_MOSI AR7; GPP_B19/GSPI1_CS# AM5; GPP_B20/GSPI1_CLK AN7; GPP_B21/GSPI1_MISO AP5; GPP_B22/GSPI1_MOSI AN5; GPP_C8 AB1; GPP_C9/UART0_TXD AB2; GPP_C10/UART0_RTS# W4; GPP_C11/UART0_CTS# AB3; GPP_C20/UART2_RXD AD1; GPP_C21/UART2_TXD AD2; GPP_C22/UART2_RTS# AD3; GPP_C23/UART2_CTS# AD4; GPP_C16/I2C0_SDA U7; GPP_C17/I2C0_SCL U6; GPP_C18/I2C1_SDA U8; GPP_C19/I2C1_SCL U9; GPP_F4/I2C2_SDA AH9; GPP_F5/I2C2_SCL AH10; GPP_F6/I2C3_SDA AH11; GPP_F7/I2C3_SCL AH12; GPP_F8/I2C4_SDA AF11; GPP_F9/I2C4_SCL AF12

ISH: GPP_D9 P2; GPP_D10 P3; GPP_D11 P4; GPP_D12 P1; GPP_D5/ISH_I2C0_SDA M4; GPP_D6/ISH_I2C0_SCL N3; GPP_D7/ISH_I2C1_SDA N1; GPP_D8/ISH_I2C1_SCL N2; GPP_F10/I2C5_SDA/ISH_I2C2_SDA AD11; GPP_F11/I2C5_SCL/ISH_I2C2_SCL AD12; GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA U1; GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL U2; GPP_D15/ISH_UART0_RTS# U3; GPP_D16/ISH_UART0_CTS#/SML0BALERT# U4; GPP_C12/UART1_RXD/ISH_UART1_RXD AC1; GPP_C13/UART1_TXD/ISH_UART1_TXD AC2; GPP_C14/UART1_RTS#/ISH_UART1_RTS# AC3; GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB4; GPP_A18/ISH_GP0 AY8; GPP_A19/ISH_GP1 BA8; GPP_A20/ISH_GP2 BB7; GPP_A21/ISH_GP3 BA7; GPP_A22/ISH_GP4 AY7; GPP_A23/ISH_GP5 AW7; Sx_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY# / ISH_GP6 AP13

+3.3V_RUN
PCH_3.3V_TS_EN <34> TPM_PIRQ# — RC5601 0_0402_5% — TPM_PIRQ#_R — NRB_BIT
@RC282 100K_0402_5%
RC237 10K_0402_5%
@RC402 49.9K_0402_1%
@RC403 49.9K_0402_1%
SIO_EXT_SCI#
LPSS_UART2_RXD
LPSS_UART2_TXD
<29> MEDIACARD_IRQ# — ONE_DIMM#
@RC5611 0_0402_5% — SIO_EXT_SCI#
<27> PCH_3.3V_TS_EN — BBS_BIT6
@RC4052 100K_0402_5% — GPP_C8
<33> SBIOS_TX — TYPEC_CON_SEL1 — TYPEC_CON_SEL2
LPSS_UART2_RXD
LPSS_UART2_TXD
<27> TS_I2C_SDA
<27> TS_I2C_SCL
<38> I2C1_SDA_TP
<38> I2C1_SCK_TP
I2C3_ANT_SDA
I2C3_ANT_SCL

+3.3V_ALW_PCH
RC283 SIO_EXT_WAKE# 10K_0402_5%
@RC330 LPSS_UART2_RXD 49.9K_0402_1%
@RC331 LPSS_UART2_TXD 49.9K_0402_1%

MEM_INTERLEAVED
AR_DET#
ISH_I2C2_SDA — ISH_I2C2_SDA <30>
ISH_I2C2_SCL — ISH_I2C2_SCL <30>
WWAN
9/24: Reserve for embedded location,refer to PDG09
WLAN
ISH_UART0_RXD <30>
ISH_UART0_TXD <30>
ISH_UART0_RTS# <30>
ISH_UART0_CTS# <30>
RTD3_CIO_PWR_EN — SIO_EXT_WAKE# <30>
LCD_CBL_DET# <27>
CLKDET# — PAD-D @T258
TPM_TYPE
LID_CL#_PCH — PAD-D @ T268
GPP_A GROUP is +1.8V

+1.8V_RUN
ISH_I2C2_SDA — RC363 1K_0402_5%
ISH_I2C2_SCL — RC362 1K_0402_5%
+3.3V_RUN
LCD_CBL_DET# — RC287 100K_0402_5%
Reserved TPM_TYPE — @RC349 100_0402_1%

+3.3V_RUN
@RC186 NRB_BIT 4.7K_0402_5%

NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Weak IPD

+3.3V_ALW_PCH
@RC184 BBS_BIT6 8.2K_0402_5%

BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI

Internal 20k PD

+3.3V_RUN
@RC2267 10K_0402_5%
ONE_DIMM#
RC2268 10K_0402_5%

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

I2C3_ANT_SCL_Q — @RC5491 0_0402_5%
I2C3_ANT_SDA_Q — @RC5481 0_0402_5%
LPSS_UART2_RXD — @RC5471 0_0402_5% — UART2_RX_I2C3_SDA
LPSS_UART2_TXD — @RC5461 0_0402_5% — UART2_TX_I2C3_SCL
+3.3V_RUN — @RC4351 0_0402_5% — +3.3V_+5V_UART
+5V_ALW — @RC4341 0_0402_5%
CONN@ JUART1 — CVILU_CI1804M1HRG-NH

+3.3V_ALW_PCH
@RC371 10K_0402_5%
MEM_INTERLEAVED
10K_0402_5% RC372

DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

+3.3V_ALW_PCH
RC400 10K_0402_5%
AR_DET#
@10K_0402_5% RC401

AR_DET#	
HIGH	NON AR
LOW	AR

+3.3V_ALW_PCH
@RC555 10K_0402_5%
@RC553 10K_0402_5%
TYPEC_CON_SEL1
TYPEC_CON_SEL2
@RC556 10K_0402_5%
@RC554 10K_0402_5%

Vendor	JAE	FOXCON	TBD	TBD
TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

+3.3V_RUN
RC512 2.2K_0402_5%
+1.8V_RUN
RC510 2.2K_0402_5%
I2C3_ANT_SDA_Q — I2C3_ANT_SDA
QC4A DMN63D8LDW-7_SOT363-6
+3.3V_RUN
RC513 2.2K_0402_5%
+1.8V_RUN
RC511 2.2K_0402_5%
I2C3_ANT_SCL_Q — I2C3_ANT_SCL
QC4B DMN63D8LDW-7_SOT363-6

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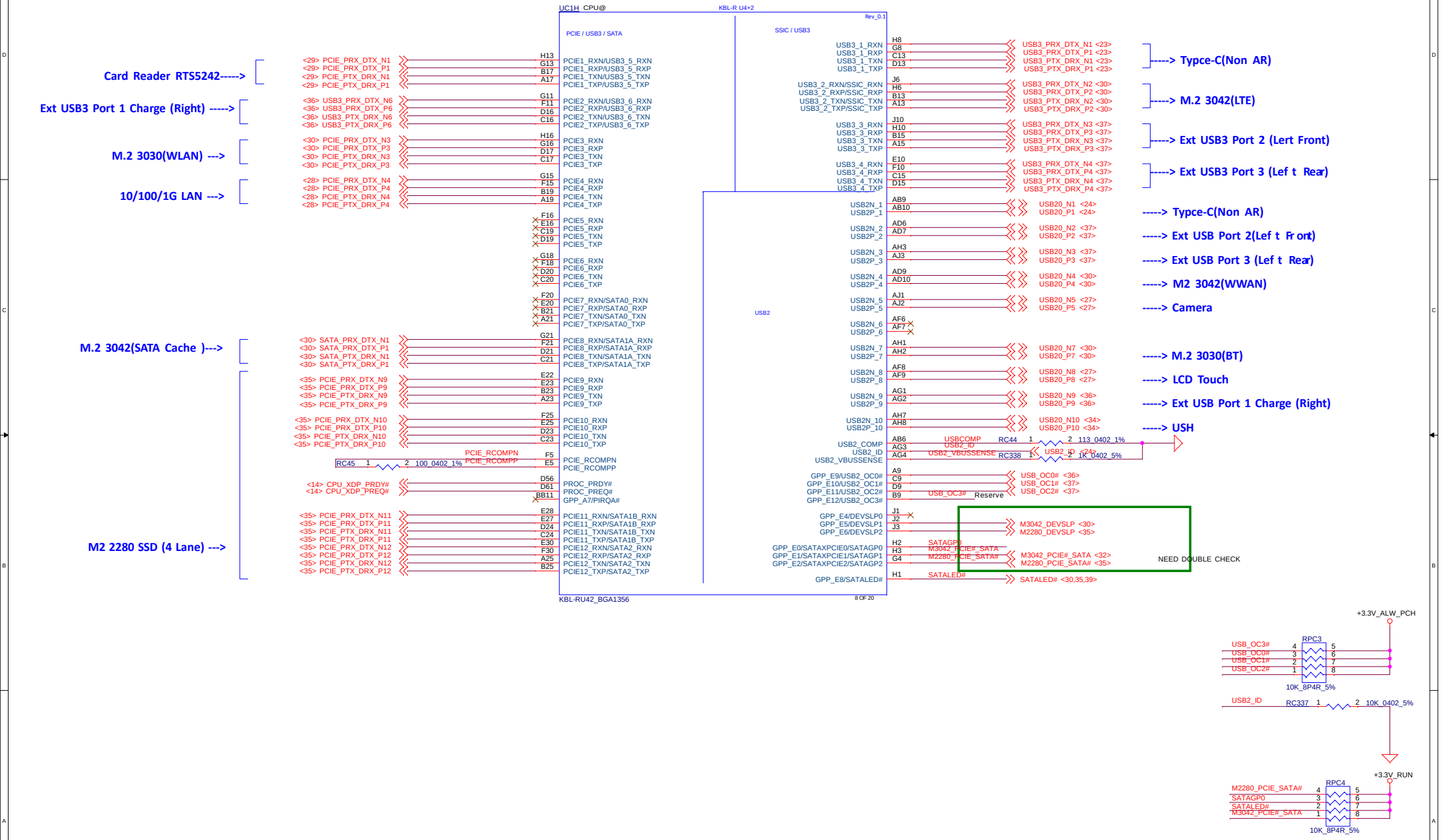
Compal Electronics, Inc.

Title: CPU (4/14)

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 9 of 59

Steamboat MLK 14 nonAR



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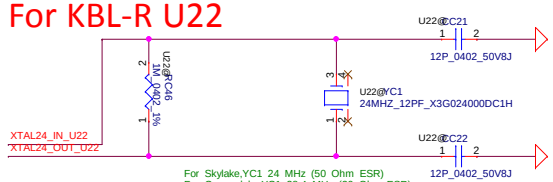
Title: CPU (5/14)

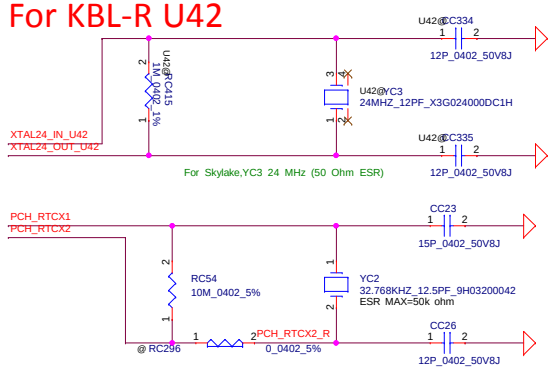
Size | Document Number: LA-F322P | Rev: 2.0

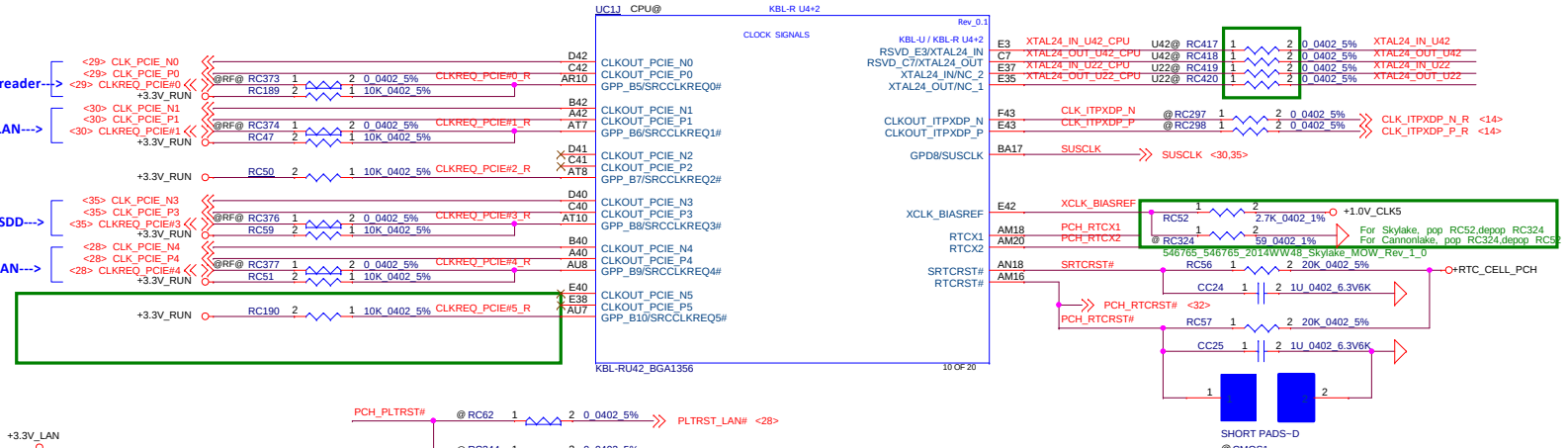
Date: Wednesday, December 20, 2017 | Sheet 10 of 59

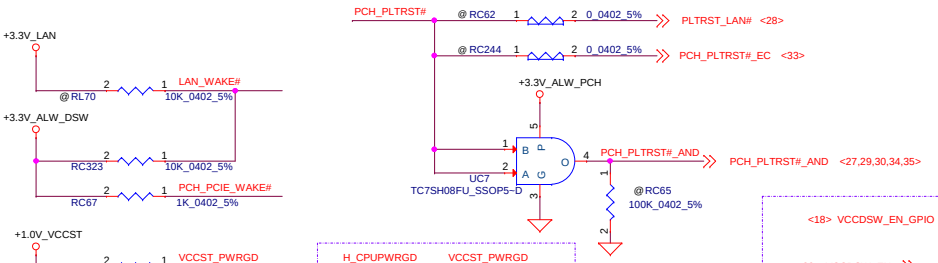
For KBL-R U22

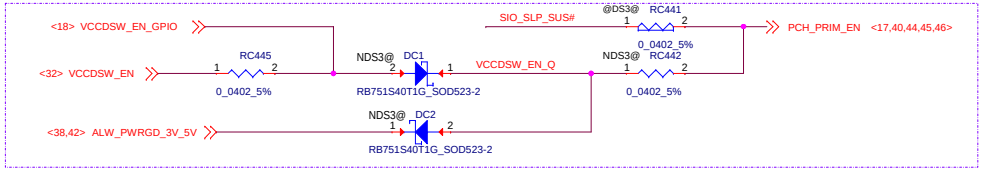


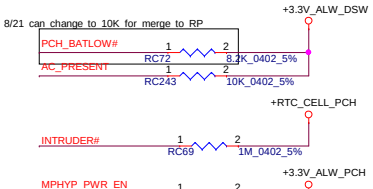
For KBL-R U42

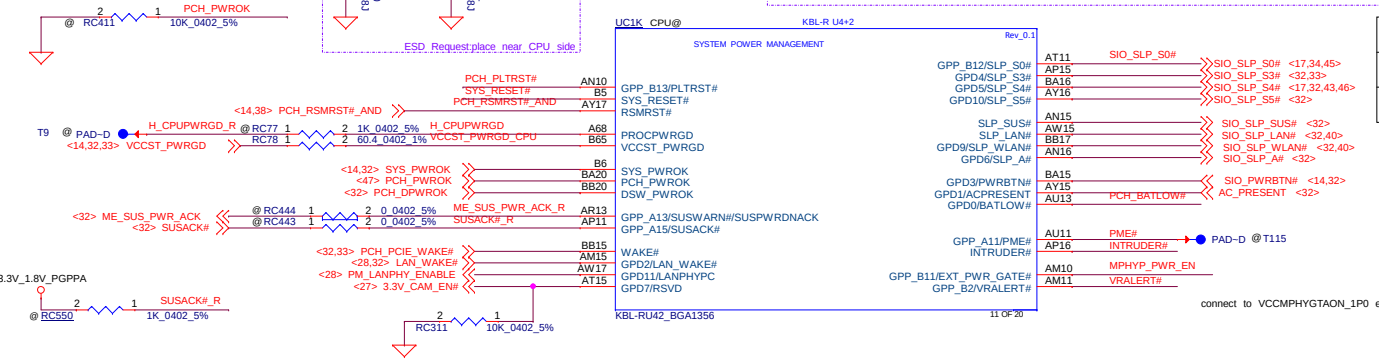






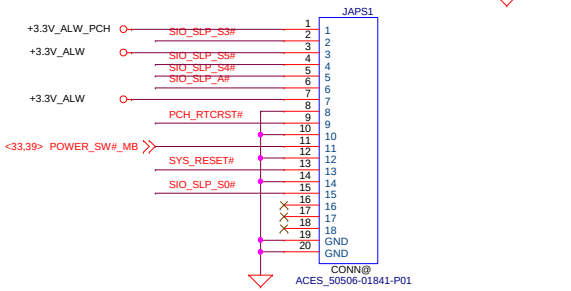


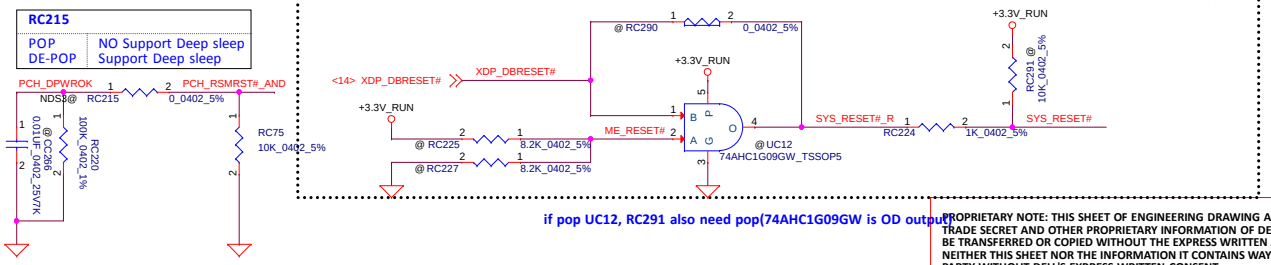




	RC439	RC440	RE536	RC215	RC441	RC442
Support DS3	V	X	V	X	V	X
No Support DS3	X	V	X	V	X	V

'V' mean POP, 'X' mean DE-POP





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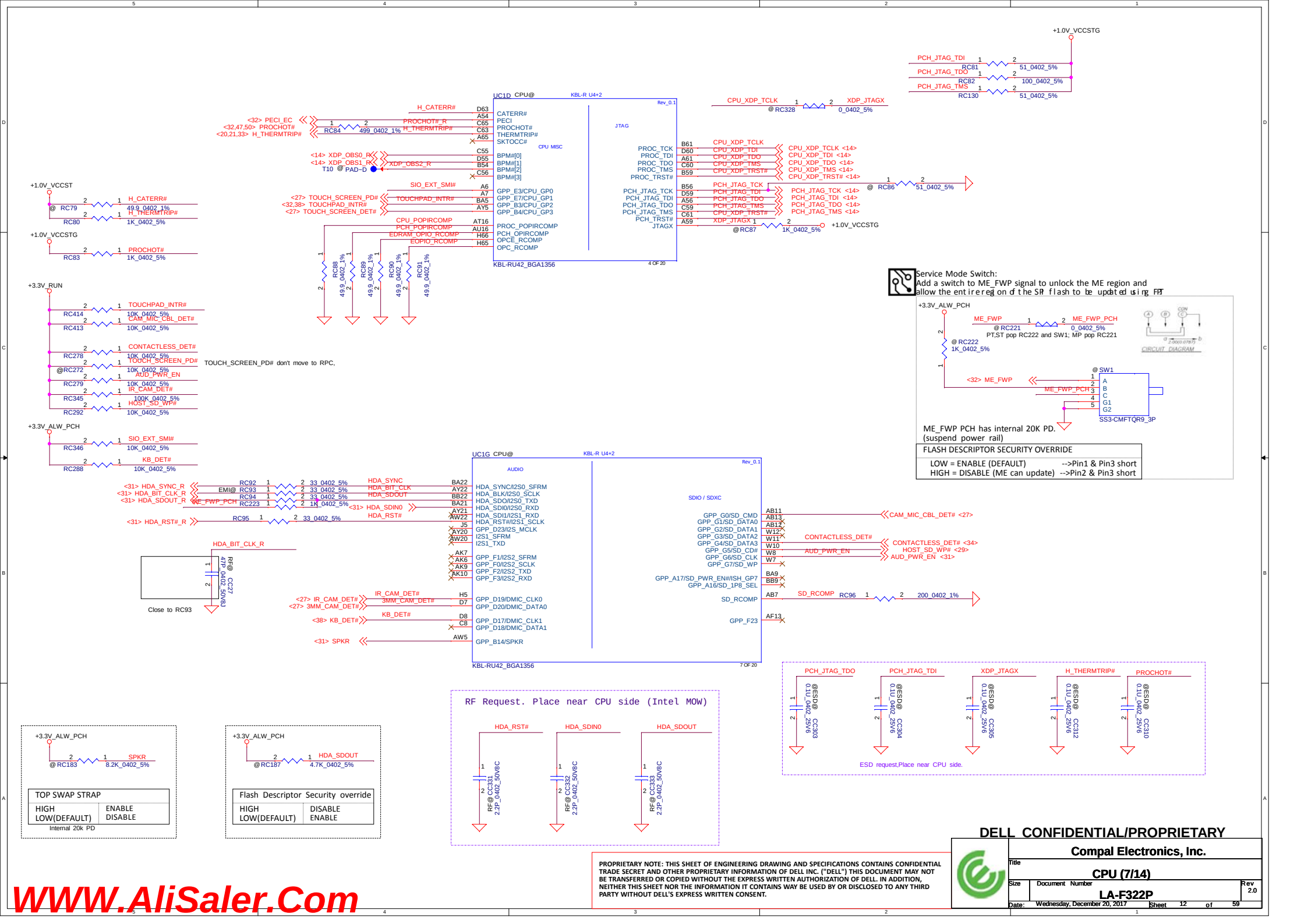
Title: CPU (6/14)

Size: | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 11 of 59



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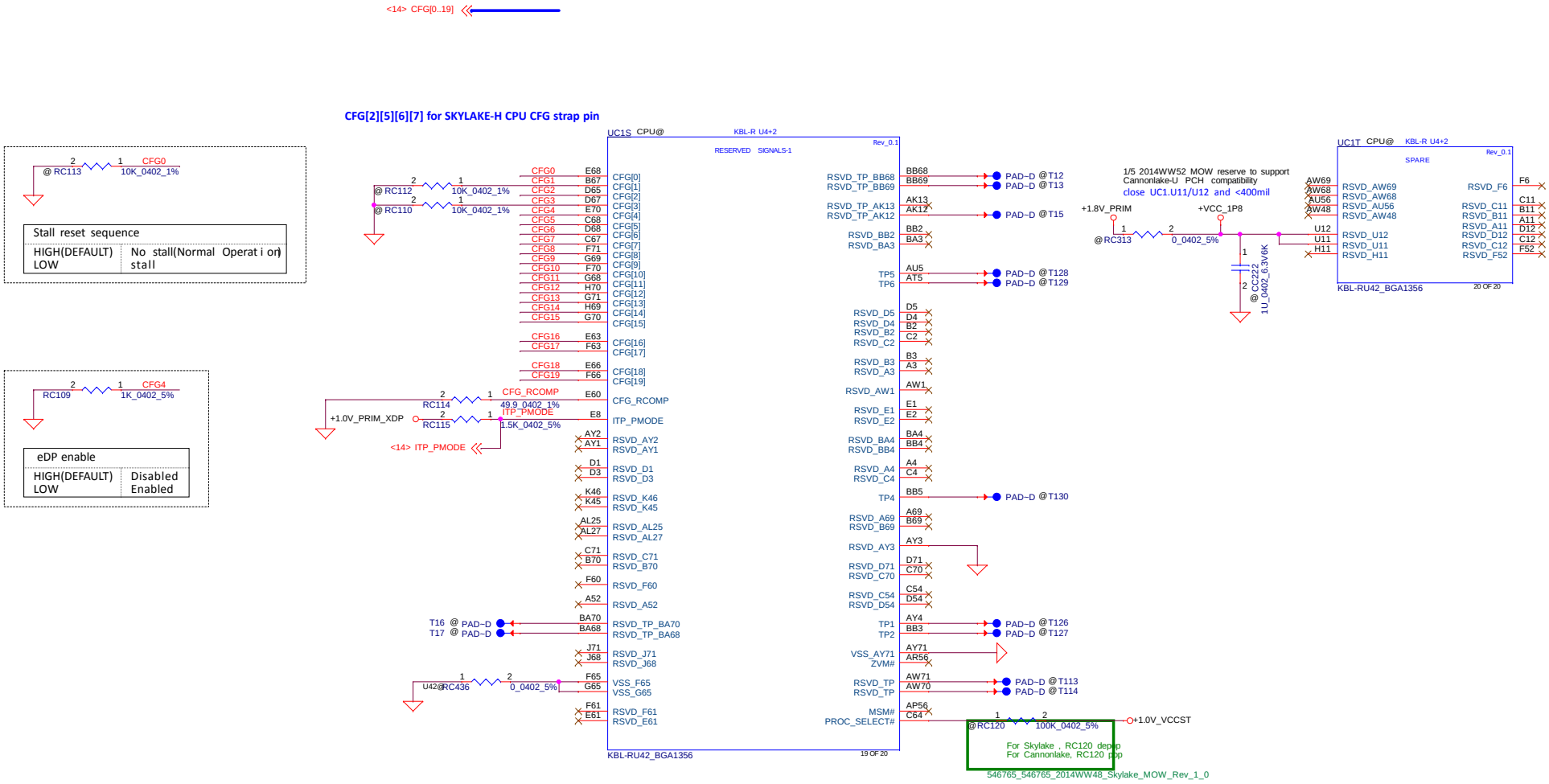
Title: CPU (7/14)

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 12 of 59



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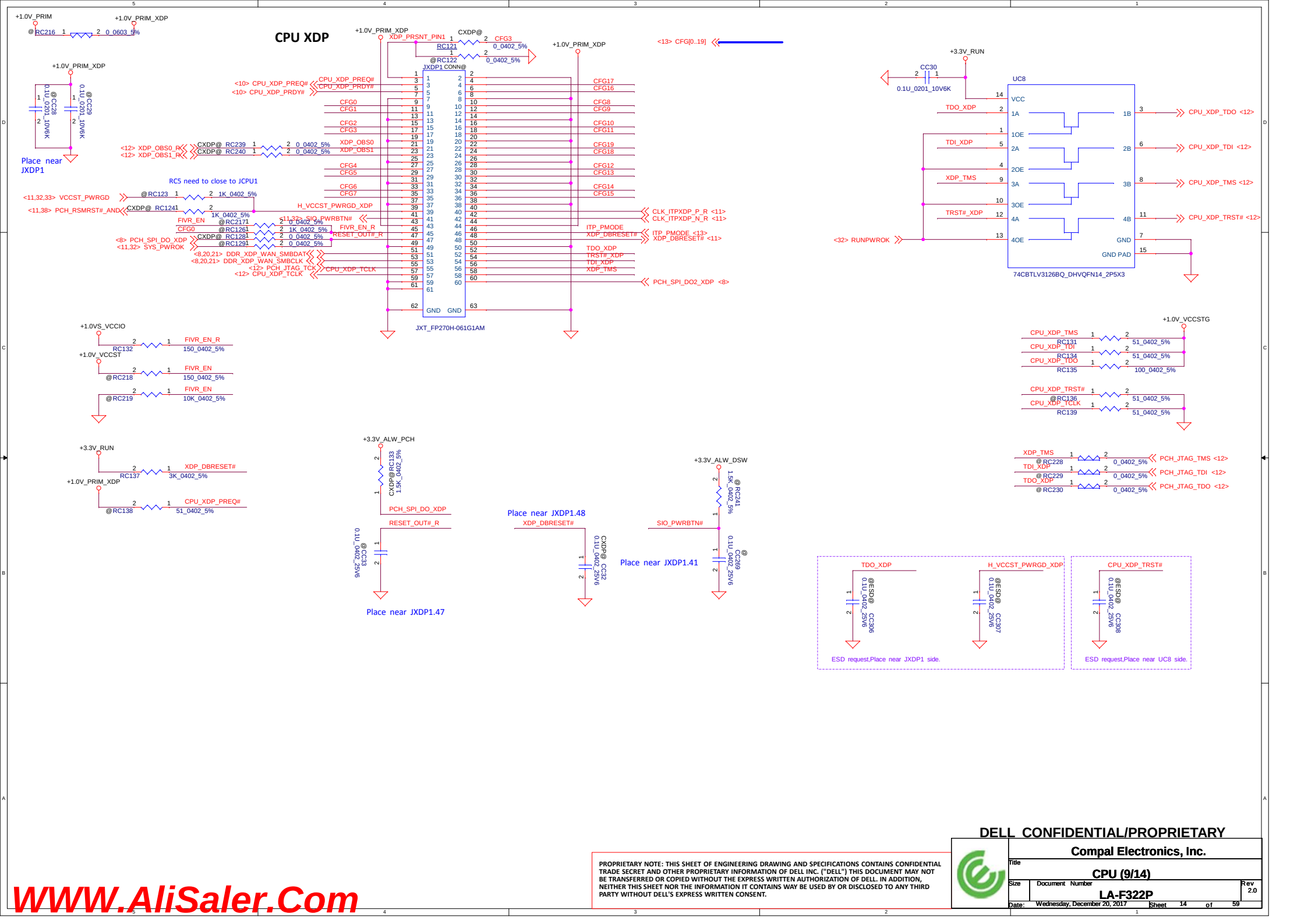
Title	CPU (8/14)	
Size	Document Number LA-F322P	Rev 2.0
Date: Wednesday, December 20, 2017	Sheet 13 of 59	



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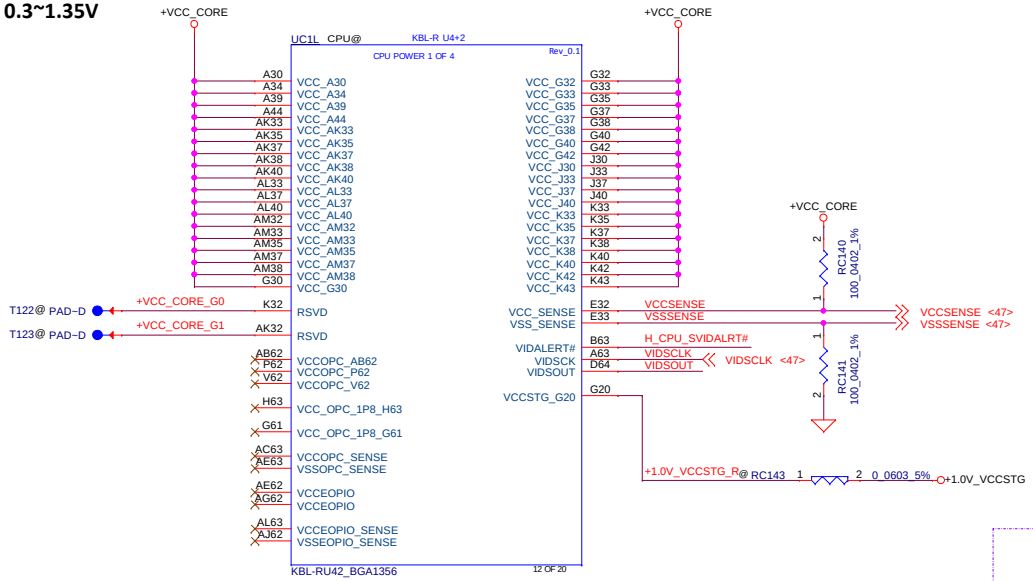
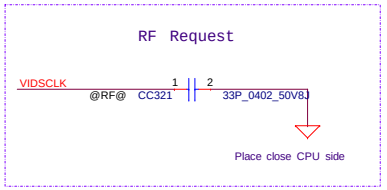
Compal Electronics, Inc.		
Title: CPU (9/14)		
Size	Document Number: LA-F322P	Rev: 2.0
Date: Wednesday, December 20, 2017	Sheet 14 of 59	

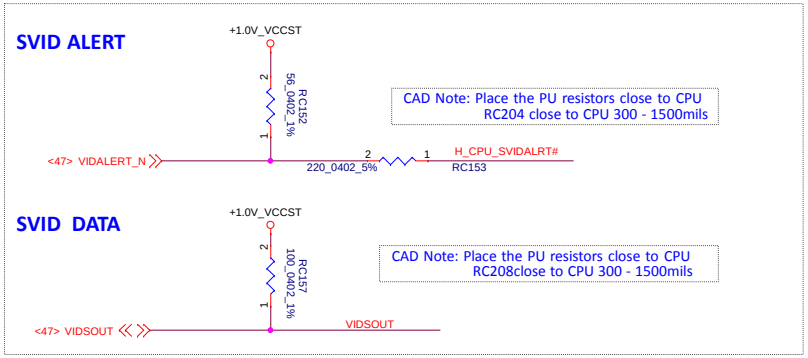
+VCC_CORE: 0.3~1.35V



PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source





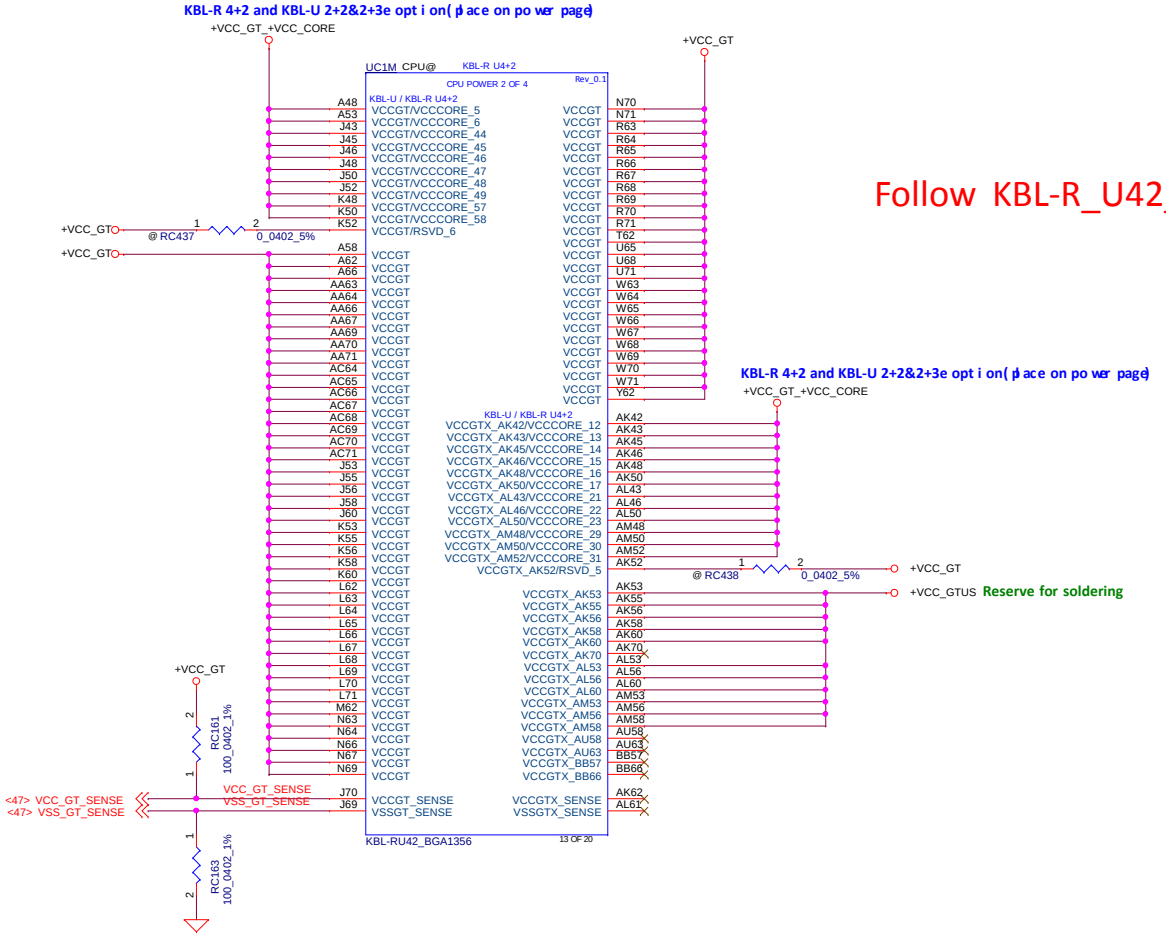
Compal Electronics, Inc.

Title: CPU (10/14)

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 15 of 59

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



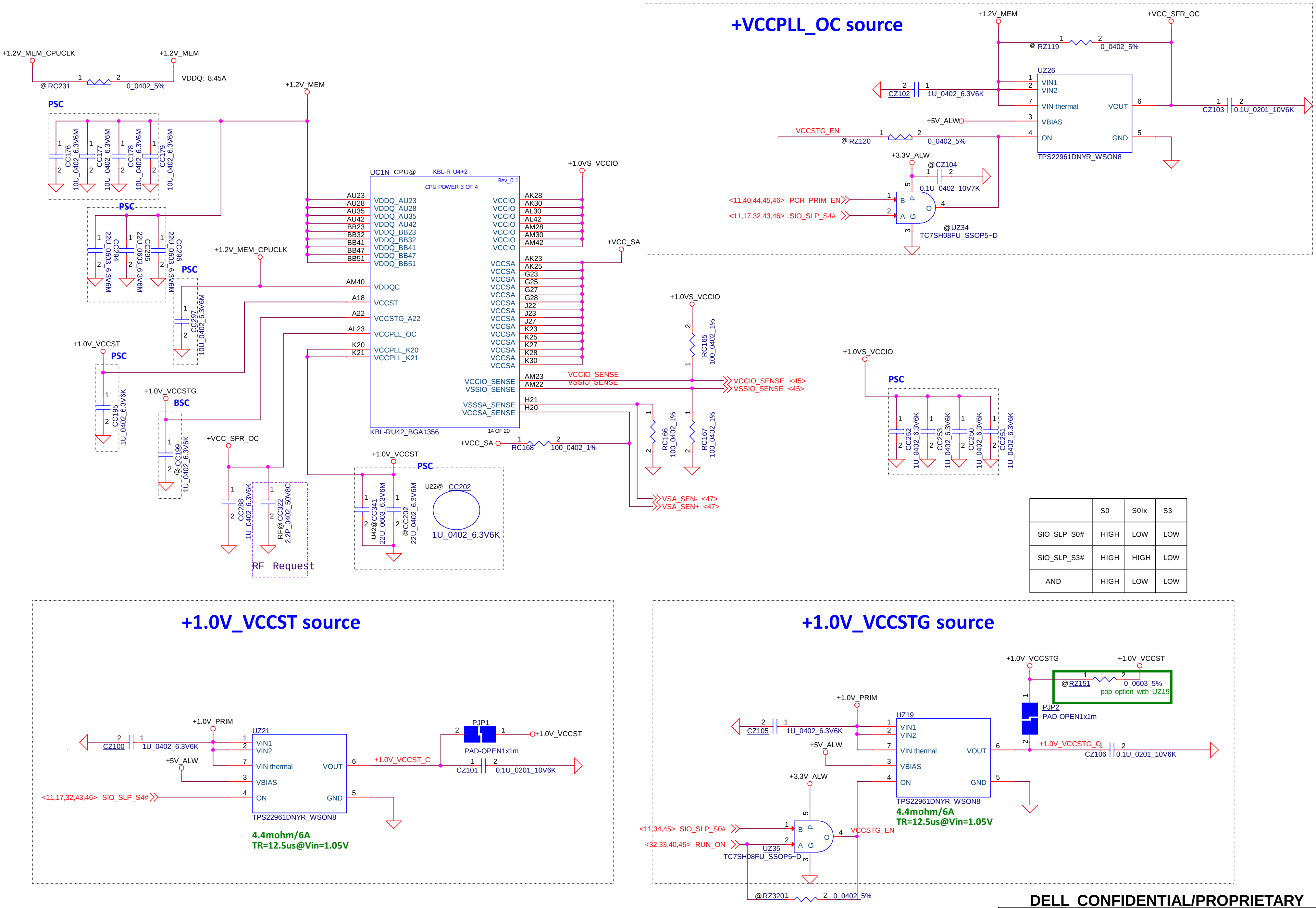
Follow KBL-R_U42_Processor_Line_BGA1356_Ballout_Rev1p0

Compal Electronics, Inc.

Title: CPU (11/14)

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 16 of 59


+VCCPLL_OC source
+1.0V_VCCST source
+1.0V_VCCSTG source
UC1N CPU@
KBL-R U4+2
CPU POWER 3 OF 4
KBL-RU42_BGA1356
VDDQ_AU23
VDDQ_AU28
VDDQ_AU35
VDDQ_AU42
VDDQ_BB23
VDDQ_BB32
VDDQ_BB41
VDDQ_BB47
VDDQ_BB51
VDDQC
VCCST
VCCSTG_A22
VCCPLL_OC
VCCPLL_K20
VCCPLL_K21
VCCIO
VCCSA
VCCIO_SENSE
VSSIO_SENSE
VSSSA_SENSE
VCCSA_SENSE
+1.2V_MEM_CPUCLK
+1.2V_MEM
VDDQ: 8.45A
@RC231 0_0402_5%
PSC
BSC
+1.0VS_VCCIO
+VCC_SA
+1.0V_VCCST
+1.0V_VCCSTG
+VCC_SFR_OC
RC165 100_0402_1%
RC166 100_0402_1%
RC167 100_0402_1%
RC168 100_0402_1%
VCCIO_SENSE <45>
VSSIO_SENSE <45>
VSA_SEN- <47>
VSA_SEN+ <47>
RF Request
U22@ CC202 1U_0402_6.3V6K
UZ26 TPS22961DNYR_WSON8
@RZ119 0_0402_5%
CZ102 1U_0402_6.3V6K
CZ103 0.1U_0201_10V6K
VCCSTG_EN
@RZ120 0_0402_5%
+5V_ALW
+3.3V_ALW
@CZ104 0.1U_0402_10V7K
<11,40,44,45,46> PCH_PRIM_EN
<11,17,32,43,46> SIO_SLP_S4#
@UZ34 TC7SH08FU_SSOP5~D
UZ21 TPS22961DNYR_WSON8
+1.0V_PRIM
CZ100 1U_0402_6.3V6K
+1.0V_VCCST_C
PJP1 PAD-OPEN1x1m
CZ101 0.1U_0201_10V6K
4.4mohm/6A
TR=12.5us@Vin=1.05V
UZ19 TPS22961DNYR_WSON8
CZ105 1U_0402_6.3V6K
@RZ151 0_0603_5%
pop option with UZ19
PJP2 PAD-OPEN1x1m
+1.0V_VCCSTG_C
CZ106 0.1U_0201_10V6K
<11,34,45> SIO_SLP_S0#
<32,33,40,45> RUN_ON
UZ35 TC7SH08FU_SSOP5~D
@RZ3201 0_0402_5%

	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

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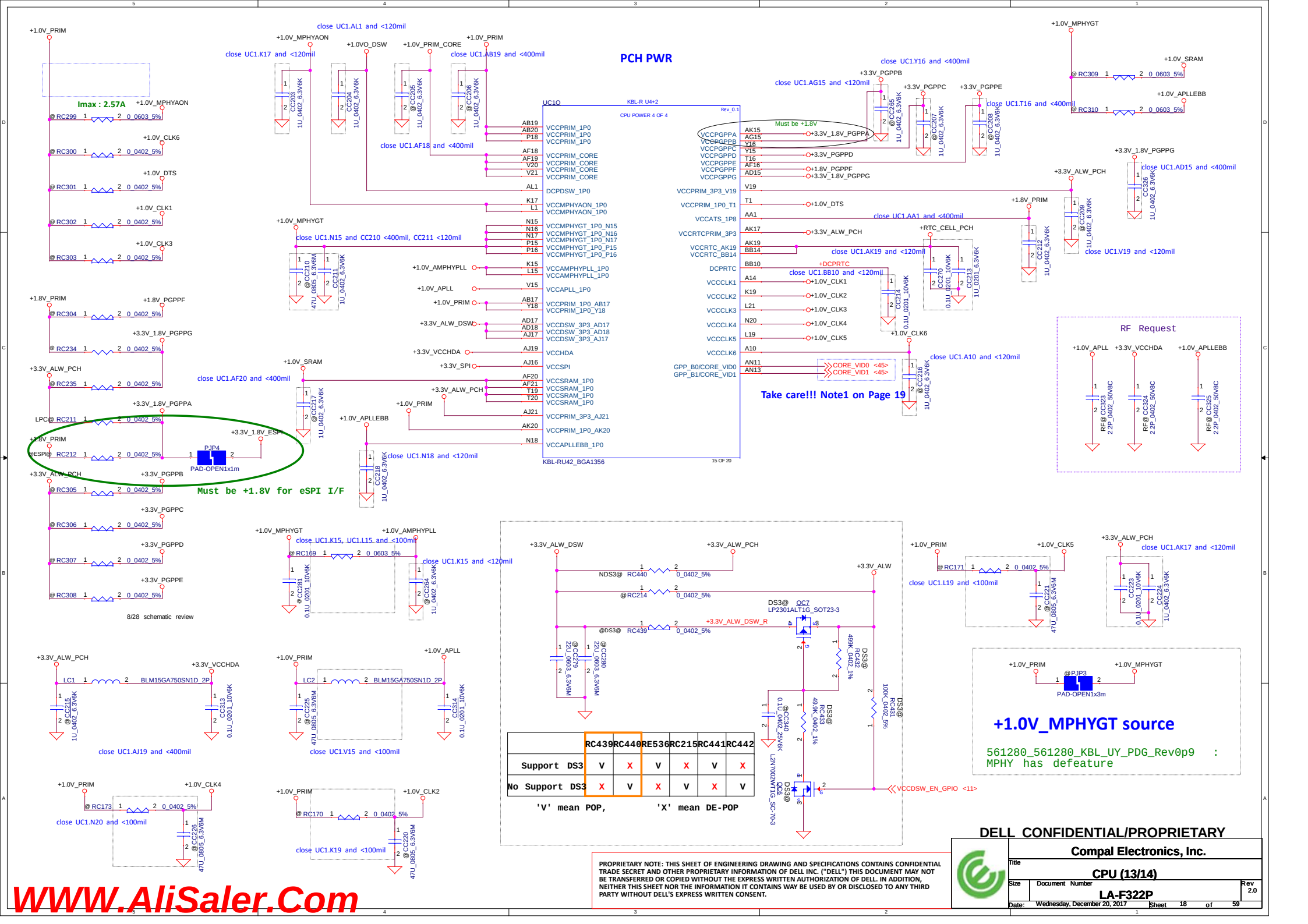
Title: CPU (12/14)

Size | Document Number: LA-F322P | Rev 2.0



	RC439	RC440	RE536	RC215	RC441	RC442
Support DS3	V	X	V	X	V	X
No Support DS3	X	V	X	V	X	V

CPU@
UC1P KBL-R U4+2
Rev_0.1
GND 1 OF 3

A5	VSS	VSS	AL65
A67	VSS	VSS	AL66
A70	VSS	VSS	AM13
AA2	VSS	VSS	AM21
AA4	VSS	VSS	AM25
AA65	VSS	VSS	AM27
AA68	VSS	VSS	AM43
AB15	VSS	VSS	AM45
AB16	VSS	VSS	AM46
AB18	VSS	VSS	AM55
AB21	VSS	VSS	AM60
AB8	VSS	VSS	AM61
AD13	VSS	VSS	AM68
AD16	VSS	VSS	AM71
AD19	VSS	VSS	AM8
AD20	VSS	VSS	AN20
AD21	VSS	VSS	AN23
AD62	VSS	VSS	AN28
AD8	VSS	VSS	AN30
AE64	VSS	VSS	AN32
AE65	VSS	VSS	AN33
AE66	VSS	VSS	AN35
AE67	VSS	VSS	AN37
AE68	VSS	VSS	AN38
AE69	VSS	VSS	AN40
AF1	VSS	VSS	AN42
AF10	VSS	VSS	AN58
AF15	VSS	VSS	AN63
AF17	VSS	VSS	AP10
AF2	VSS	VSS	AP18
AF4	VSS	VSS	AP20
AF63	VSS	VSS	AP23
AG16	VSS	VSS	AP28
AG17	VSS	VSS	AP32
AG18	VSS	VSS	AP35
AG19	VSS	VSS	AP38
AG20	VSS	VSS	AP42
AG21	VSS	VSS	AP58
AG71	VSS	VSS	AP63
AH13	VSS	VSS	AP68
AH6	VSS	VSS	AP70
AH63	VSS	VSS	AR11
AH64	VSS	VSS	AR15
AH67	VSS	VSS	AR16
AJ15	VSS	VSS	AR20
AJ18	VSS	VSS	AR23
AJ20	VSS	VSS	AR28
AJ4	VSS	VSS	AR35
AK11	VSS	VSS	AR42
AK16	VSS	VSS	AR43
AK18	VSS	VSS	AR45
AK21	VSS	VSS	AR46
AK22	VSS	VSS	AR48
AK27	VSS	VSS	AR5
AK63	VSS	VSS	AR50
AK68	VSS	VSS	AR52
AK69	VSS	VSS	AR53
AK8	VSS	VSS	AR55
AL2	VSS	VSS	AR58
AL28	VSS	VSS	AR63
AL32	VSS	VSS	AR8
AL35	VSS	VSS	AT2
AL38	VSS	VSS	AT20
AL4	VSS	VSS	AT23
AL45	VSS	VSS	AT28
AL48	VSS	VSS	AT35
AL52	VSS	VSS	AT4
AL55	VSS	VSS	AT42
AL58	VSS	VSS	AT56
AL64	VSS	VSS	AT58
	VSS	VSS	

KBL-RU42_BGA1356 16 OF 20

CPU@
UC1O KBL-R U4+2
Rev_0.1
GND 2 OF 3

AT63	VSS	VSS	BA49
AT68	VSS	VSS	BA53
AT71	VSS	VSS	BA57
AU10	VSS	VSS	BA6
AU15	VSS	VSS	BA62
AU20	VSS	VSS	BA66
AU32	VSS	VSS	BA71
AU38	VSS	VSS	BB18
AV1	VSS	VSS	BB26
AV68	VSS	VSS	BB30
AV69	VSS	VSS	BB34
AV70	VSS	VSS	BB38
AV71	VSS	VSS	BB43
AW10	VSS	VSS	BB55
AW12	VSS	VSS	BB6
AW14	VSS	VSS	BB60
AW16	VSS	VSS	BB64
AW18	VSS	VSS	BB67
AW21	VSS	VSS	BB70
AW23	VSS	VSS	C1
AW26	VSS	VSS	C25
AW28	VSS	VSS	C5
AW30	VSS	VSS	D10
AW32	VSS	VSS	D11
AW34	VSS	VSS	D14
AW36	VSS	VSS	D18
AW38	VSS	VSS	D22
AW41	VSS	VSS	D25
AW43	VSS	VSS	D26
AW45	VSS	VSS	D30
AW47	VSS	VSS	D34
AW49	VSS	VSS	D39
AW51	VSS	VSS	D44
AW53	VSS	VSS	D45
AW55	VSS	VSS	D47
AW57	VSS	VSS	D48
AW6	VSS	VSS	D53
AW60	VSS	VSS	D58
AW62	VSS	VSS	D6
AW64	VSS	VSS	D62
AW66	VSS	VSS	D66
AW8	VSS	VSS	D69
AY66	VSS	VSS	E11
B10	VSS	VSS	E15
B14	VSS	VSS	E18
B18	VSS	VSS	E21
B22	VSS	VSS	E46
B30	VSS	VSS	E50
B34	VSS	VSS	E53
B39	VSS	VSS	E56
B44	VSS	VSS	E6
B48	VSS	VSS	E65
B53	VSS	VSS	E71
B58	VSS	VSS	F1
B62	VSS	VSS	F13
B66	VSS	VSS	F2
B71	VSS	VSS	F22
BA1	VSS	VSS	F23
BA10	VSS	VSS	F27
BA14	VSS	VSS	F28
BA18	VSS	VSS	F32
BA2	VSS	VSS	F33
BA23	VSS	VSS	F35
BA28	VSS	VSS	F37
BA32	VSS	VSS	F38
BA36	VSS	VSS	F4
F68	VSS	VSS	F40
BA45	VSS	VSS	F42
	VSS	VSS	BA41

KBL-RU42_BGA1356 17 OF 20

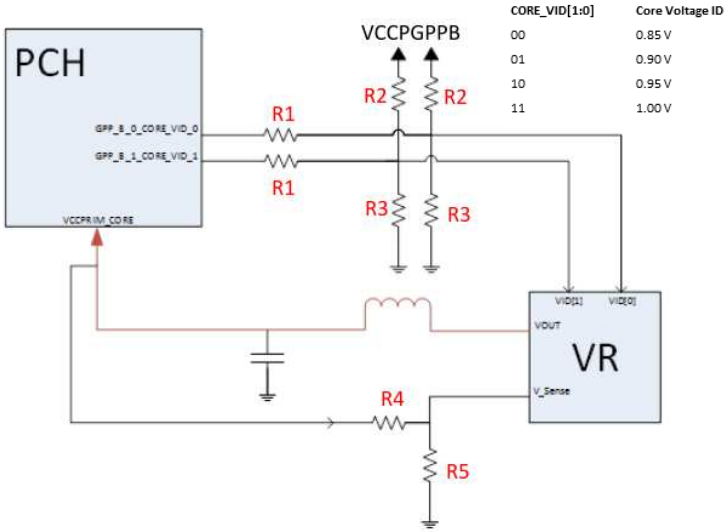
CPU@
UC1R KBL-R U4+2
Rev_0.1
GND 3 OF 3

F8	VSS	VSS	L18
G10	VSS	VSS	L2
G22	VSS	VSS	L20
G43	VSS	VSS	L4
G45	VSS	VSS	L8
G48	VSS	VSS	N10
G5	VSS	VSS	N13
G52	VSS	VSS	N19
G55	VSS	VSS	N21
G58	VSS	VSS	N6
G6	VSS	VSS	N65
G60	VSS	VSS	N68
G63	VSS	VSS	P17
G66	VSS	VSS	P19
H15	VSS	VSS	P20
H18	VSS	VSS	P21
H71	VSS	VSS	R13
J11	VSS	VSS	R6
J13	VSS	VSS	T15
J25	VSS	VSS	T17
J28	VSS	VSS	T18
J32	VSS	VSS	T2
J35	VSS	VSS	T21
J38	VSS	VSS	T4
J42	VSS	VSS	U10
J8	VSS	VSS	U63
K16	VSS	VSS	U64
K18	VSS	VSS	U66
K22	VSS	VSS	U67
K61	VSS	VSS	U69
K63	VSS	VSS	U70
K64	VSS	VSS	V16
K65	VSS	VSS	V17
K66	VSS	VSS	V18
K67	VSS	VSS	W13
K68	VSS	VSS	W6
K70	VSS	VSS	W9
K71	VSS	VSS	Y17
L11	VSS	VSS	Y19
L16	VSS	VSS	Y20
L17	VSS	VSS	Y21
	VSS	VSS	

KBL-RU42_BGA1356 18 OF 20

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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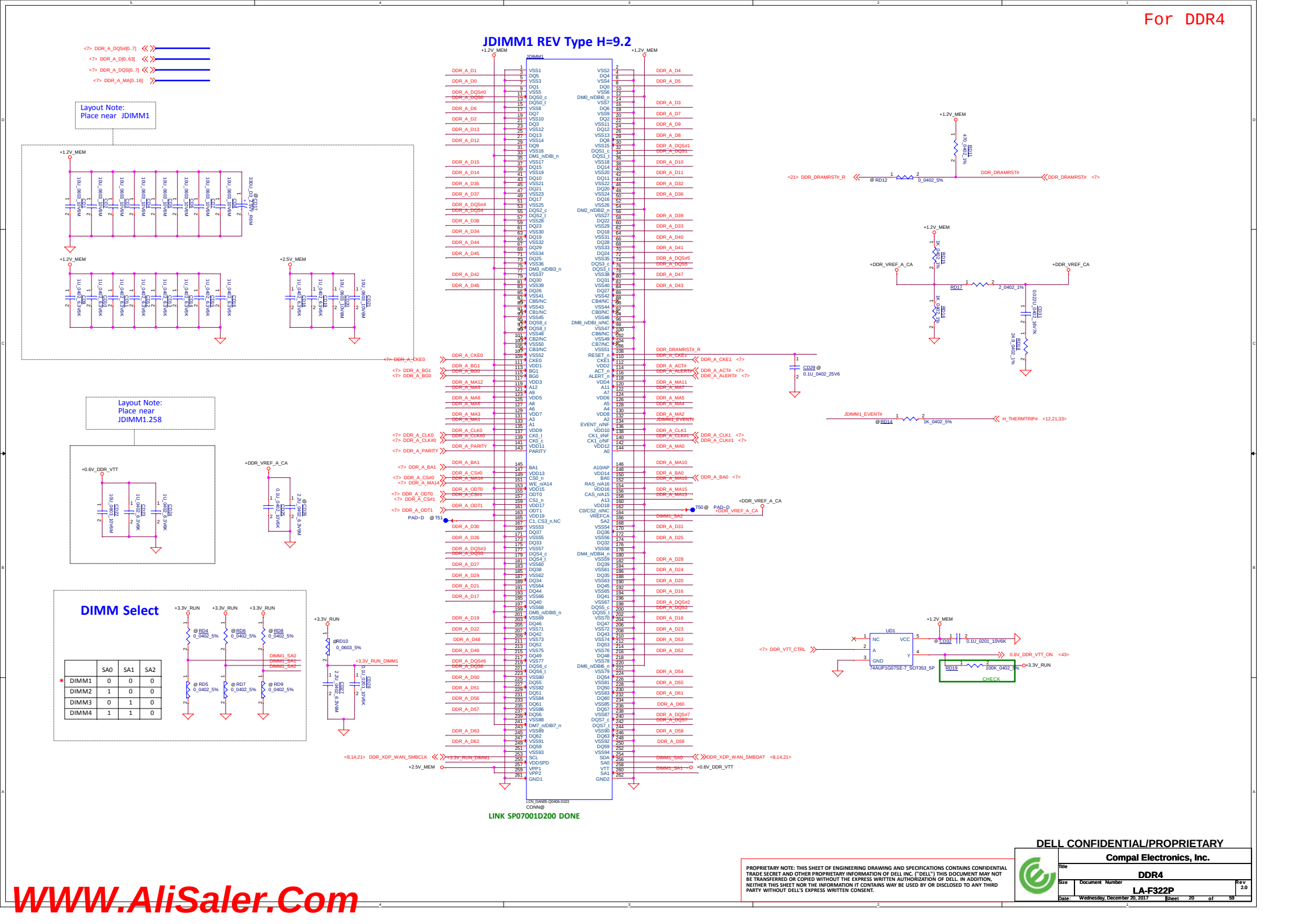
Title: CPU (14/14)

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 19 of 59

For DDR4

JDIMM1 REV Type H=9.2



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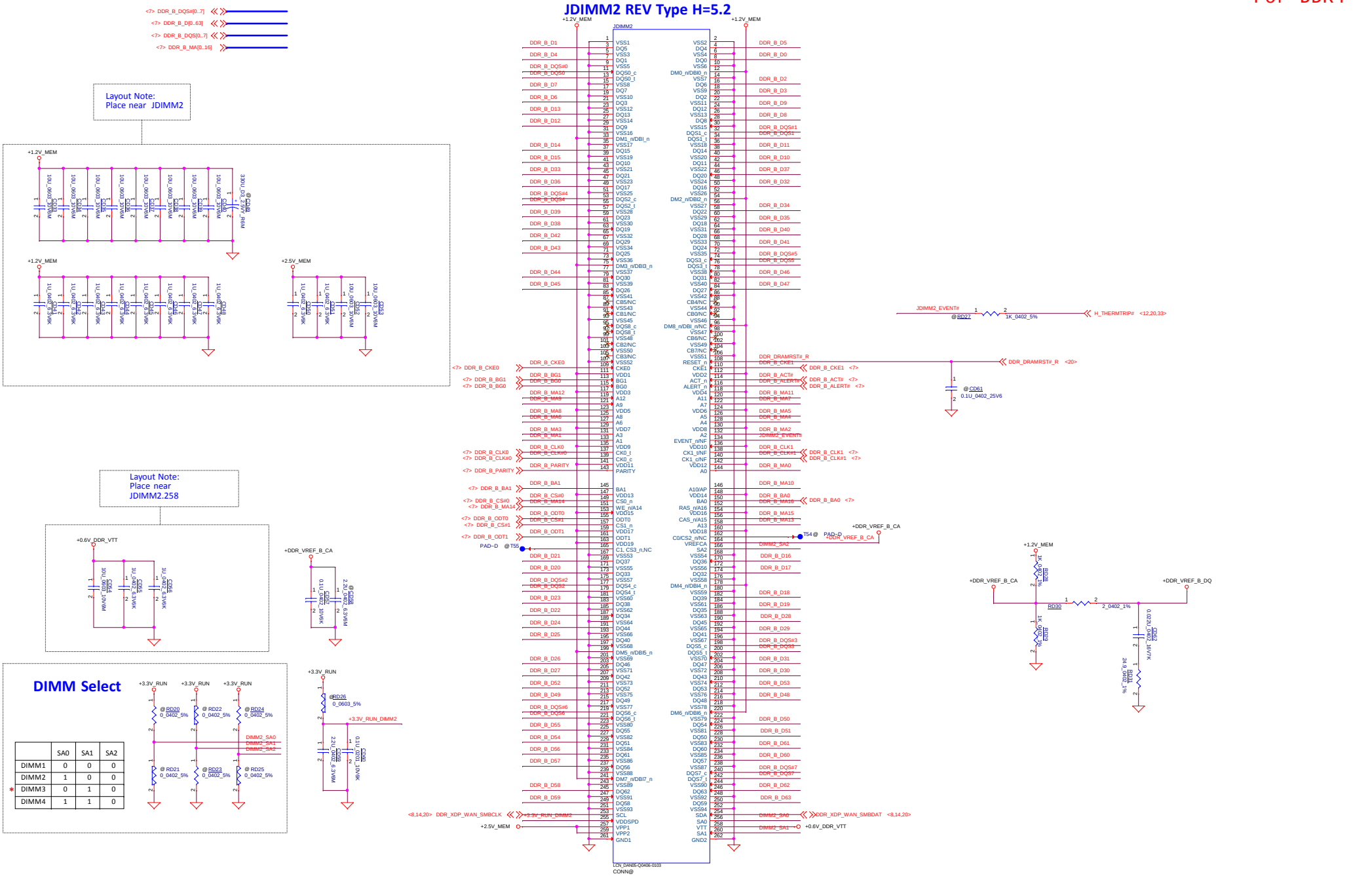
Title: DDR4

Size: Document Number: LA-F322P Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 20 of 59

For DDR4

JDIMM2 REV Type H=5.2



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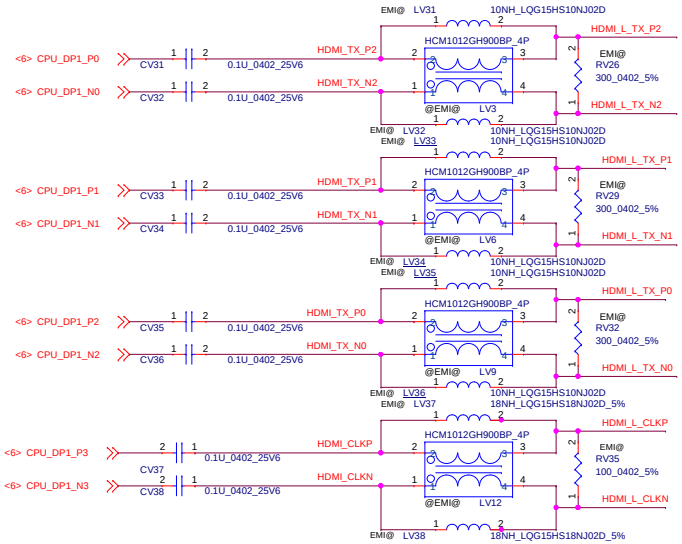
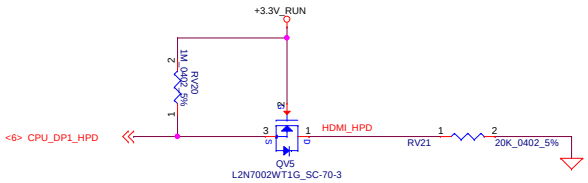
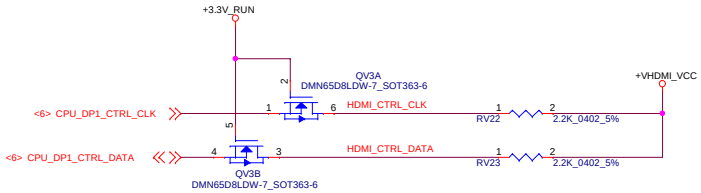
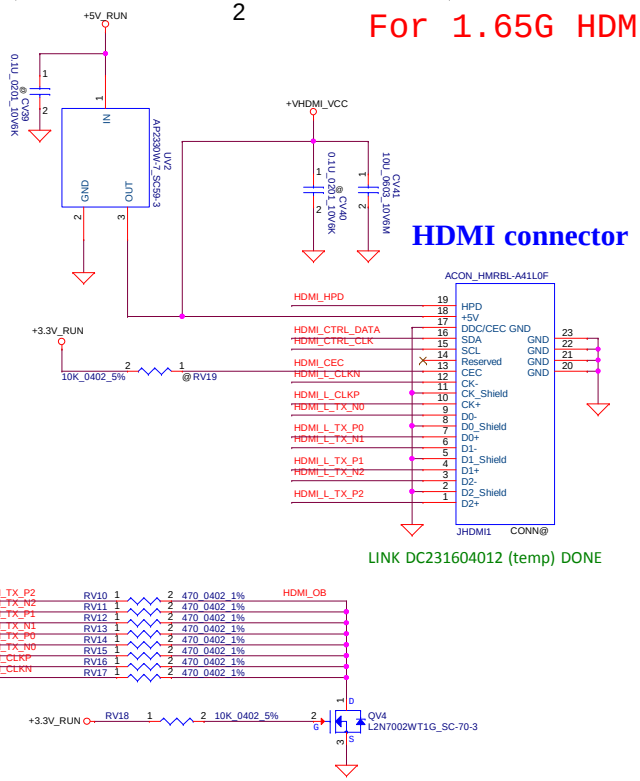
Compal Electronics, Inc.	
Title	DDR4
Size	Document Number: LA-F322P
Rev	2.0
Date:	Wednesday, December 20, 2017
Sheet	21 of 59

For 1.65G HDMI from CPU









LINK DC231604012 (temp) DONE

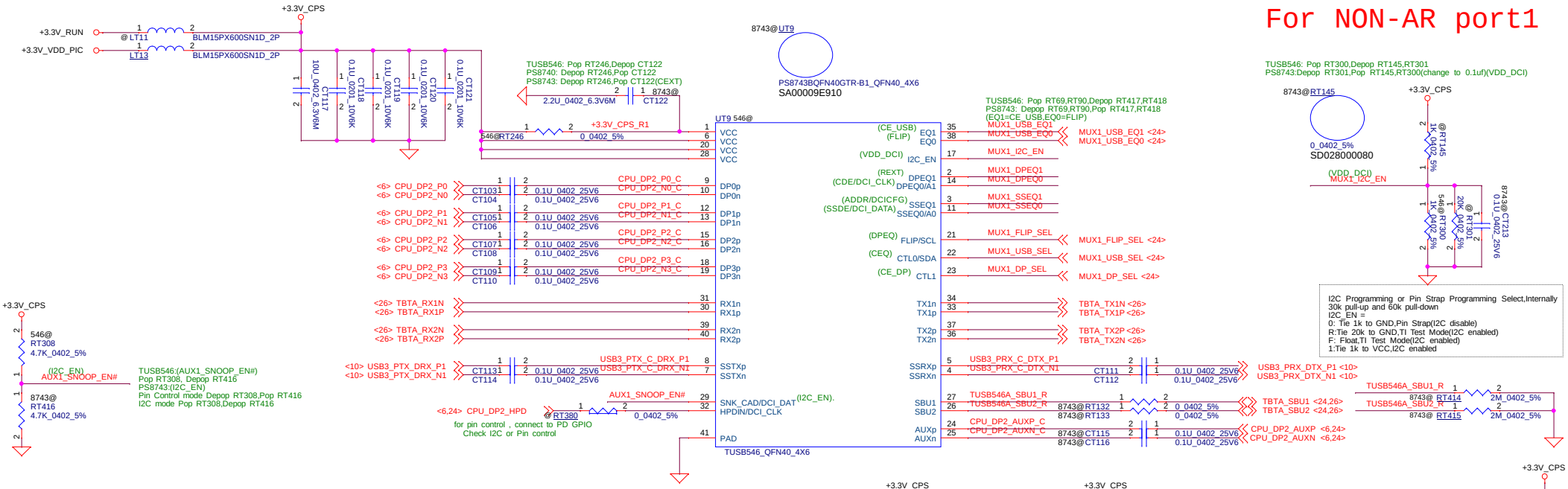
Compal Electronics, Inc.

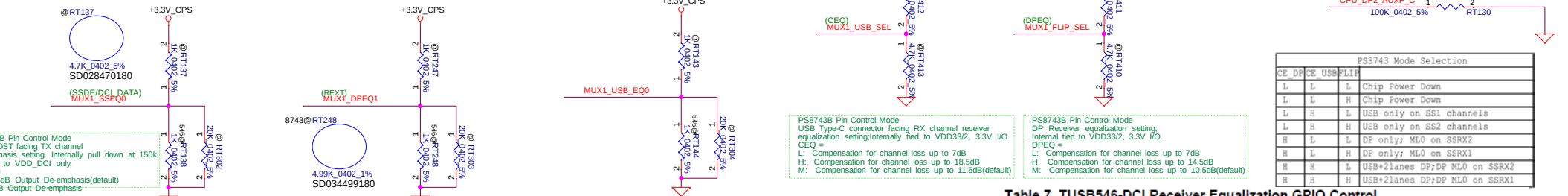
Title: HDMI CONN

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 22 of 59

For NON-AR port1

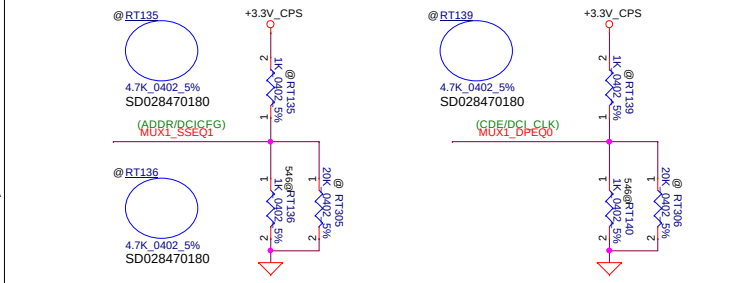




PS8743 Mode Selection			
CE_DP	CE_USB	FLIP	
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	USB only on SS1 channels
L	H	H	USB only on SS2 channels
H	L	L	DP only; MLO on SSRX2
H	L	H	DP only; MLO on SSRX1
H	H	L	USB+2lanes DP;DP MLO on SSRX2
H	H	H	USB+2lanes DP;DP MLO on SSRX1

Table 7. TUSB546-DCI Receiver Equalization GPIO Control

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN LEVEL	EQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ GAIN at 2.5 GHz (dB)	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ GAIN at 4.05 GHz (dB)
0	0	0	0.2	0	0	-1.6	0	0	1.0
1	0	R	1.2	0	R	-0.5	0	R	3.3
2	0	F	2.2	0	F	0.5	0	F	4.9
3	0	1	3.3	0	1	1.6	0	1	6.5
4	R	0	4.2	R	0	2.4	R	0	7.5
5	R	R	5.1	R	R	3.4	R	R	8.6
6	R	F	5.9	R	F	4.1	R	F	9.5
7	R	1	6.7	R	1	4.9	R	1	10.4
8	F	0	7.4	F	0	5.7	F	0	11.1
9	F	R	8.1	F	R	6.4	F	R	11.7
10	F	F	8.7	F	F	6.9	F	F	12.3
11	F	1	9.3	F	1	7.5	F	1	12.8
12	1	0	9.7	1	0	8.0	1	0	13.2
13	1	R	10.2	1	R	8.5	1	R	13.6
14	1	F	10.6	1	F	8.9	1	F	14.0
15	1	1	11.1	1	1	9.4	1	1	14.4



Compal Electronics, Inc.

Title: DP/USB3 Repeater SW TUSB546

Size: Document Number: LA-F322P Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 23 of 59

For NON-AR port1

DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.5A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Check AUX connect to PD or PS8743B

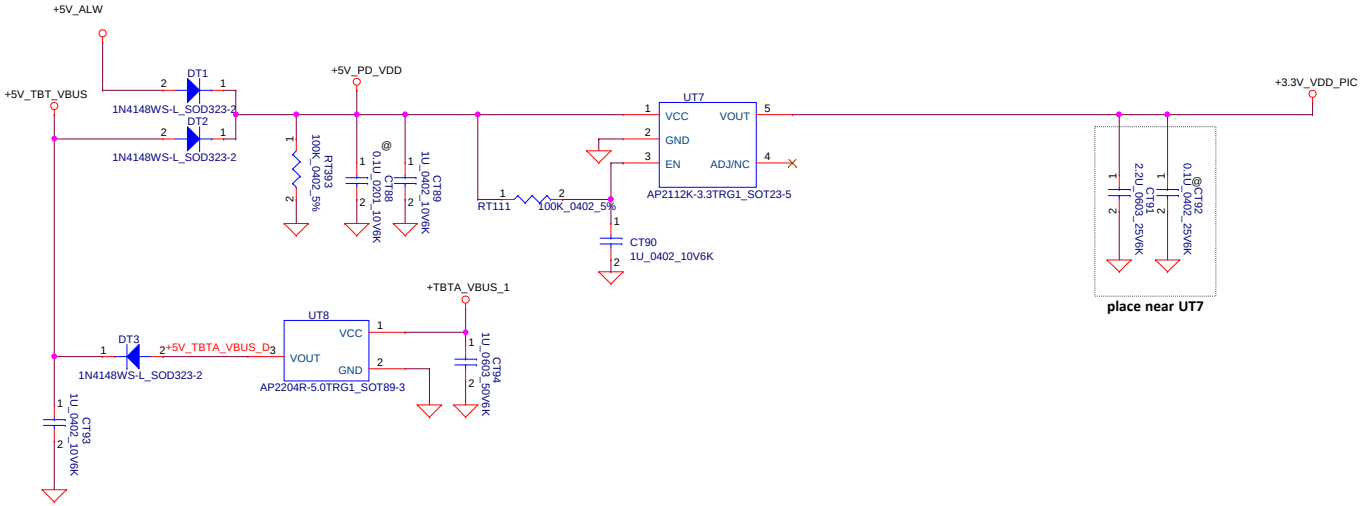
Need Link TPS65982D

Compal Electronics, Inc.

Title: [Type C]PD Controller TI

Size: | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 24 of 59



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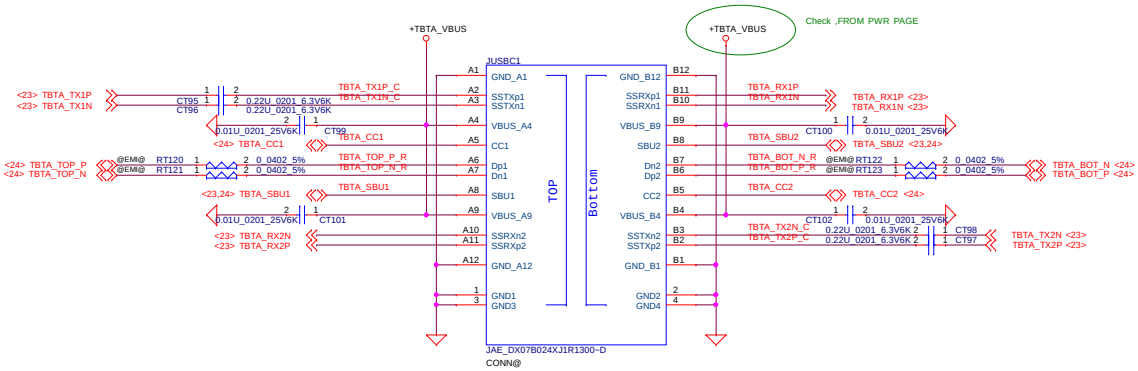
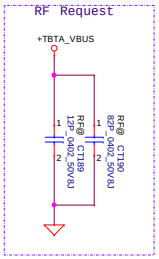
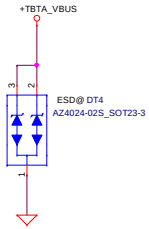
Compal Electronics, Inc.		
Title: [Type C]PD Power		
Size	Document Number: LA-F322P	Rev: 2.0
Date: Wednesday, December 20, 2017	Sheet 25 of 59	

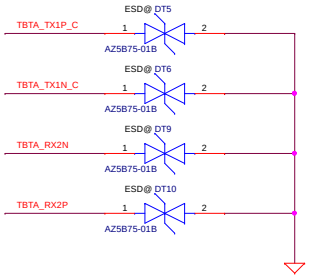
For NON AR Config

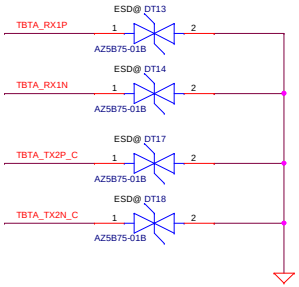


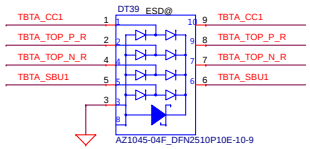


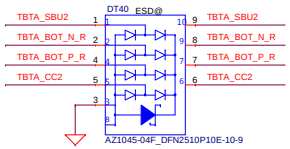


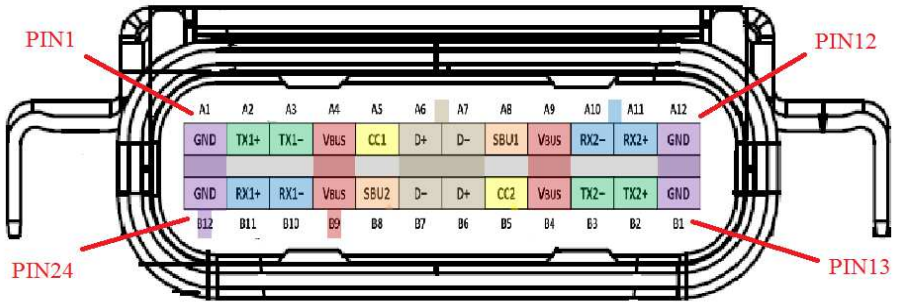
Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done











Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 26 of 59

LINK 50398-04041-001 DONE

For 4LANE EDP &5V_TSP,Steamboat14

JEDP1

ACES_50398-04041-001
CONN@

+3.3V_RUN
+3.3V_CAM
USB20_N5_R
USB20_P5_R
CAM_MIC_CBL_DET# <12>
+BL_PWR_SRC
Pin10: LOOP_BACK
EMI@ LV1
DISP_ON
BIA_PWM
BLM15PX221SN1D_2P
DMIC0 <31>
DMIC_CLK0 <31>
@EMI@ 100P_0402_50V8J
EMI Request
EDP_HPD <6>
LCD_TST <32>
+LCDVDD
3MM_CAM_DET# <12>
EDP_AUXN_C
EDP_AUXP_C
EDP_TXP0_C
EDP_TXN0_C
EDP_TXP1_C
EDP_TXN1_C
EDP_TXP2_C
EDP_TXN2_C
EDP_TXP3_C
EDP_TXN3_C
CV1 CV2 CV3 CV4 CV5 CV6 CV7 CV8 CV9 CV10
0.1U_0402_25V6
EDP_AUXN <6>
EDP_AUXP <6>
EDP_TXP0 <6>
EDP_TXN0 <6>
EDP_TXP1 <6>
EDP_TXN1 <6>
EDP_TXP2 <6>
EDP_TXN2 <6>
EDP_TXP3 <6>
EDP_TXN3 <6>
LCD_CBL_DET# <9>

EDP_HPD
@ RV7
100K_0402_5%
+LCDVDD
Reserve for EA

+3.3V_CAM
10K_0402_5%
RV235
3MM_CAM_DET#

Due to SBMLK14 WLAN antenna locati onis d ifferent bet ween 3mm CAM and 3.5mm CAM, so add 3mm_CAM_DET# pin to identify.

Due to SB12/14 Mic. receive path is diff erent bet ween Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for diff erent verb table

CONN@ JTS1
ACES_50208-01001-P03
+5V_TSP
PCH_PLTRST#_AND <11,29,30,34,35>
TOUCH_SCREEN_PD# <12>
TS_I2C_SDA <9>
TS_I2C_SCL <9>
TS_INT# <6>
TOUCH_SCREEN_DET# <12>
GND GND

TOUCH_PANEL_PD#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events

USB20_N8_R
USB20_P8_R
EXC24CQ900U_4P
LV27 @EMI@
USB20_N8 <10>
USB20_P8 <10>
@ESD@ AZC199-02SPR7G_SOT23-3
DV4
ESD depop locat i on

+3.3V_RUN
TS_I2C_SDA RV98 2.2K_0402_5%
TS_I2C_SCL RV99 2.2K_0402_5%
TS_INT# RV311 100K_0402_5%
TS_INT# @ RV319 1K_0402_5%

RF Request
+PWR_SRC
RF@ 100P_0402_50V8J CZ23

RF Request
TS_I2C_SDA @RF@ CV54 33P_0402_50V8J
TS_I2C_SCL @RF@ CV55 33P_0402_50V8J

+3.3V_RUN
10K_0402_5%
RV8
TOUCH_SCREEN_DET#
CONN@ JIR1
IR_CAM_DET# <12>
+PWR_SRC
GND GND
E-T_4251K-F06N-40L

RF Request
+5V_TSP
RF@ 12P_0402_50V8J CV18
RF@ 82P_0402_50V8J CV19

+BL_PWR_SRC
+LCDVDD
+3.3V_CAM
+5V_TSP
+3.3V_RUN
0.1U_0201_10V6K
@CV11 @CV12 @CZ1 @CZ2 @CA7
Close to JEDP1.17~19
Close to JEDP1.30~31
Close to JEDP1.11
Close to JEDP1.1
Close to JEDP1.10

DV1
BAT54CW_SOT323-3
BIA_PWM
EDP_BIA_PWM
BIA_PWM_EC
EDP_BIA_PWM <6>
BIA_PWM_EC <32>
RV1 4.7K_0402_5%

DV2
BAT54CW_SOT323-3
DISP_ON
PANEL_BKLEN <6>
PANEL_BKEN_EC <32>
RV2 4.7K_0402_5%

RF Request
+LCDVDD
+3.3V_CAM
+BL_PWR_SRC
RF@ 12P_0402_50V8J CV20
RF@ 82P_0402_50V8J CV21
RF@ 12P_0402_50V8J CV22
RF@ 82P_0402_50V8J CV23
RF@ 12P_0402_50V8J CV24
RF@ 82P_0402_50V8J CV25

For Touchscreen

+5V_RUN
+5V_TSP
+5V_RUN
+3.3V_RUN
47K_0402_5%
RV6
QV8 LP2301ALT1G_SOT23-3
100K_0402_5%
RV326
RV400 0_0402_5%
<32> 3.3V_TS_EN
<9> PCH_3.3V_TS_EN
@ RV323 0_0402_5%
@ RV324 0_0402_5%
3.3V_TS_EN_R
QV7 L2N7002WT1G_SC-70-3
@CV635 0.1U_0402_25V6K

LCDVDD POWER

+LCDVDD
+EDP_VDD
+3.3V_ALW
@CV16 10U_0603_10V6M
@PJP12 PAD-OPEN1x1m
UV24 G524B1T11U_SOT23-5
VOUT VIN GND EN /OC
@CV17 0.01UF_0402_25V7K
DV3 BAT54CW_SOT323-3
<32> LCD_VCC_TEST_EN
<6> ENVDD_PCH
EN_LCDPWR
RV3 100K_0402_5%

WebCAM

+3.3V_CAM
+3.3V_RUN
QZ1 LP2301ALT1G_SOT23-3
<11> 3.3V_CAM_EN#
RZ380 0_0402_5%
@CZ2200 0.1U_0402_25V6K
LZ1 EMI@
<10> USB20_P5
<10> USB20_N5
USB20_P5_R
USB20_N5_R
EXC24CQ900U_4P

Backlight POWER

+PWR_SRC
+BL_PWR_SRC
QV1 AO6405_TSOP6
CV13 1000P_0402_50V7K
RV4 270K_0402_5%
BL_PWR_SRC_ON
CV15 0.1U_0603_50V7K
QV2 L2N7002WT1G_SC-70-3
RV5 47K_0402_5%
CV14 0.01U_0402_50V7K
<32> EN_INVPWR

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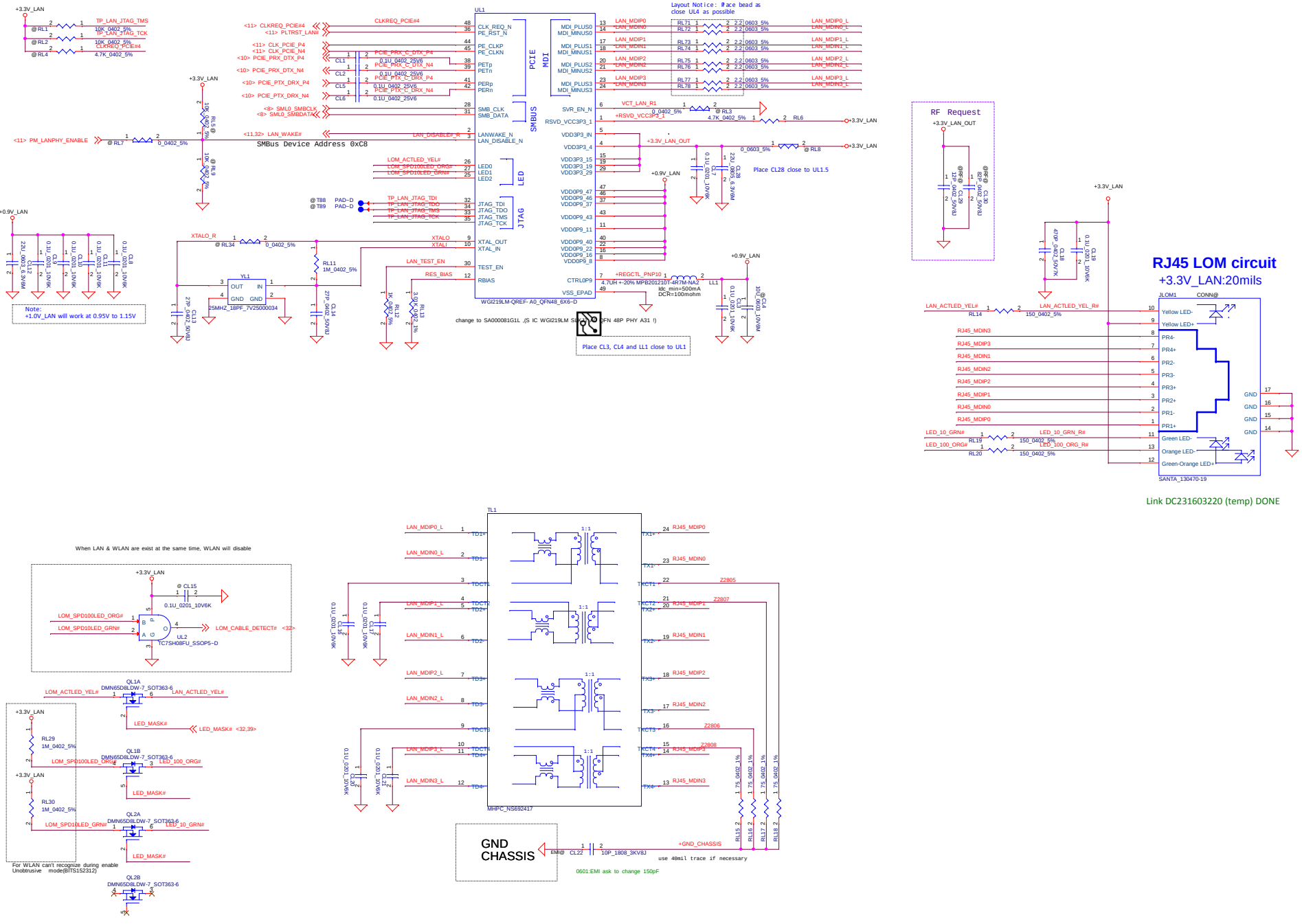
Title: eDP CONN & Touch screen

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 27 of 59



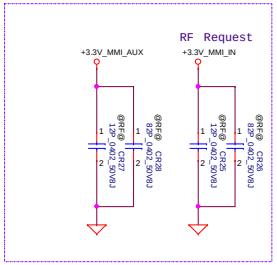
Compal Electronics, Inc.

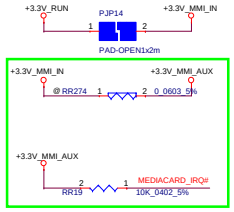
Title: LAN Clarkville & RJ45

Size | Document Number: LA-F322P | Rev: 2.0

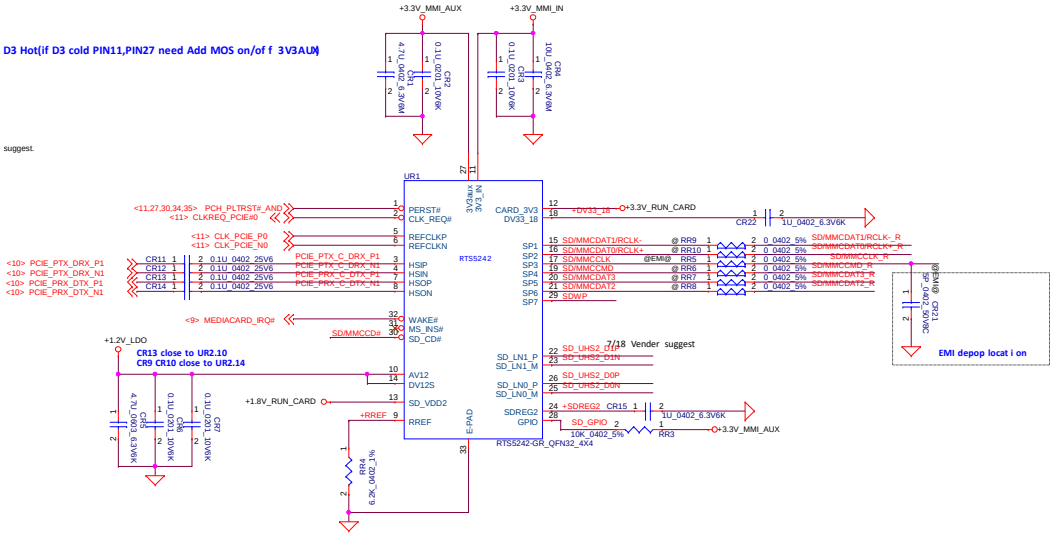
Date: Wednesday, December 20, 2017 | Sheet 28 of 59

For PCIE Interface

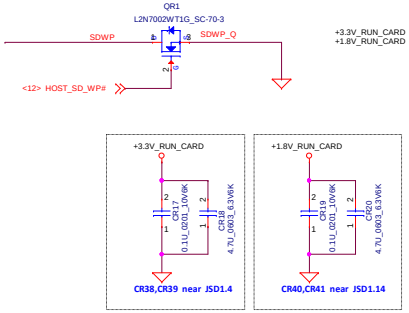


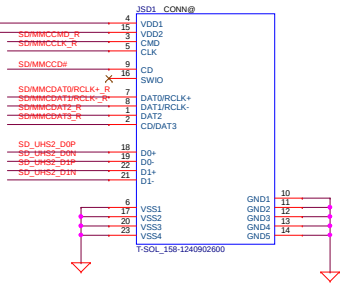


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX)



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	Low	Low	Write Enable
Low	Low	High	Write Protect(FW LOCK)





LINK SP071603151 (temp) DONE

Compal Electronics, Inc.

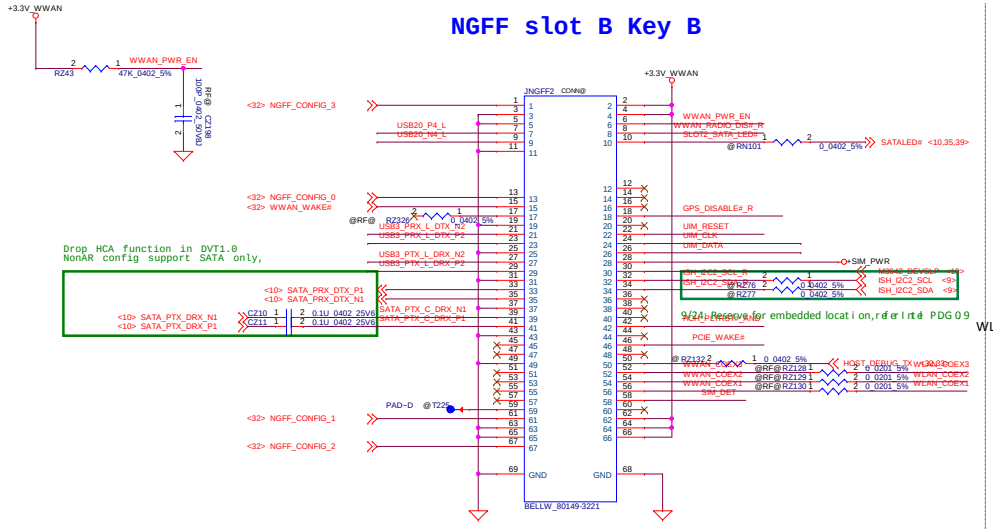
Title: Card Reader RTS5242

Size: Document Number: LA-F322P Rev: 2.0

Date: Wednesday, December 20, 2017 Sheet 29 of 59

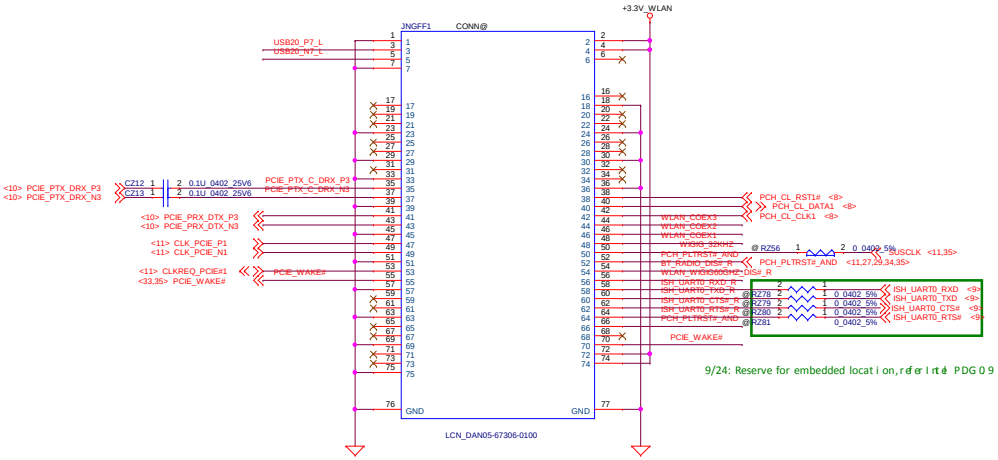
for no AR,Brekenridge 12/14/15 UMA/Steamboat

NGFF slot B Key B

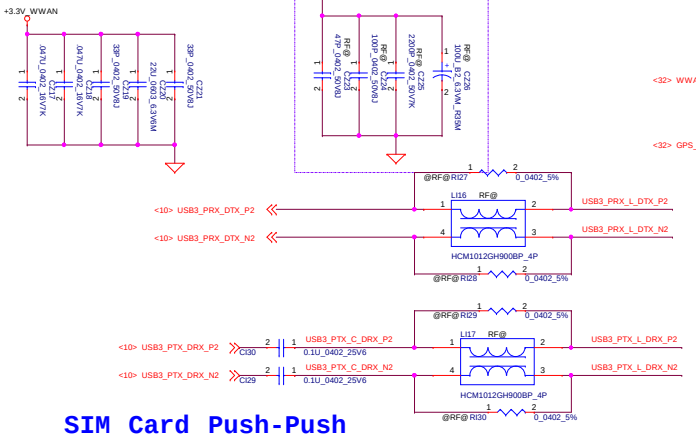


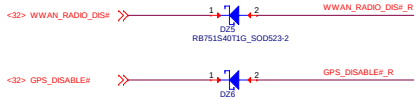
80149-3221 LINK DONE

NGFF slot A Key A

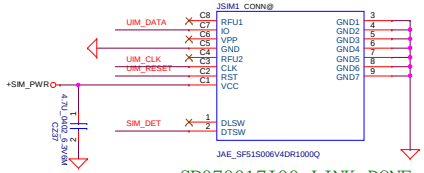


SP070019F00 LINK DONE

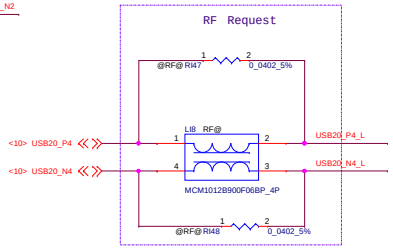


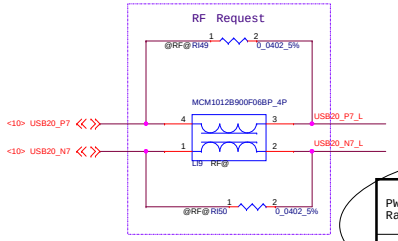


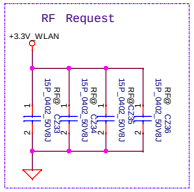
SIM Card Push-Push

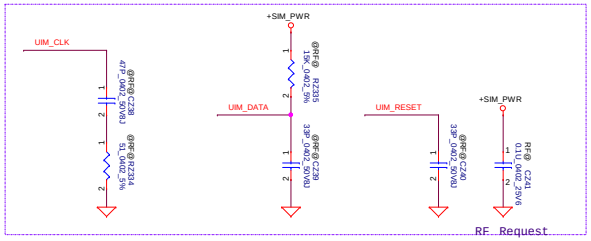


SP070017I00 LINK DONE









STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

Compal Electronics, Inc.

Title: NGFF Card

Size: | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 30 of 59

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

ACES_50271-0040N-001

Link SP02000TS00 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 13.

Add for solve pop noise and detect issue

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

RF Request

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

Normal Open

Only BR15U UMA use LA2,LA3,because 6L

Link DC23000DG10 DONE

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Compal Electronics, Inc.

Codec ALC3246

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Size	Document Number	Rev
C	LA-F322P	2.0

Date: Wednesday, December 20, 2017 Sheet 31 of 59

For SB

For EVT/DVT1.0 Only,SA00009GL10, S IC MEC5105K-TMP2-TN WFBGA 169P EC
After DVT1.1,SA00009GL00, S IC MEC5105K-D1-TN WFBGA 169P EC

	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

Deep Sleep support	
non Deep Sleep	1
Deep Sleep	0

	VGA_IDENTIFY
Discrete	0
UMA	1

RF Request

Close to pin H1

close to pin G8/M9

Close to pin N5

32 KHz Clock

For EMI request

Compal Electronics, Inc.
Title: EC MEC5105
Size: Document Number: LA-F322P
Rev: 2.0
Date: Wednesday, December 20, 2017
Sheet 32 of 59

For SB

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

*	RE343	CE62	REV
	240K	4700p	Single Port ACE w/o AR
	130K	4700p	Single Port ACE w/AR
	62K	4700p	Dual Port ACE w/o AR
	33K	4700p	Dual Port ACE w/AR
	8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
	4.3K	4700p	.
	2K	4700p	
	1K	4700p	

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
* 2K	4700p	A01
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
* 33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	15P
1K	4700p	

PD_ACE_DET# rise ti me is measuredfro m 5 %~68 %

BOARD_ID rise ti me is measuredfro m 5 %~68 %

SYSTEM_ID rise ti me is measuredfro m 5 %~68 %

Rest=1.58K , Tp=96 degree
Rest=1.33K , Tp=93 degree

Link 50271-0040N-001 DONE

Thermal diode mapping

5105 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

CHECK

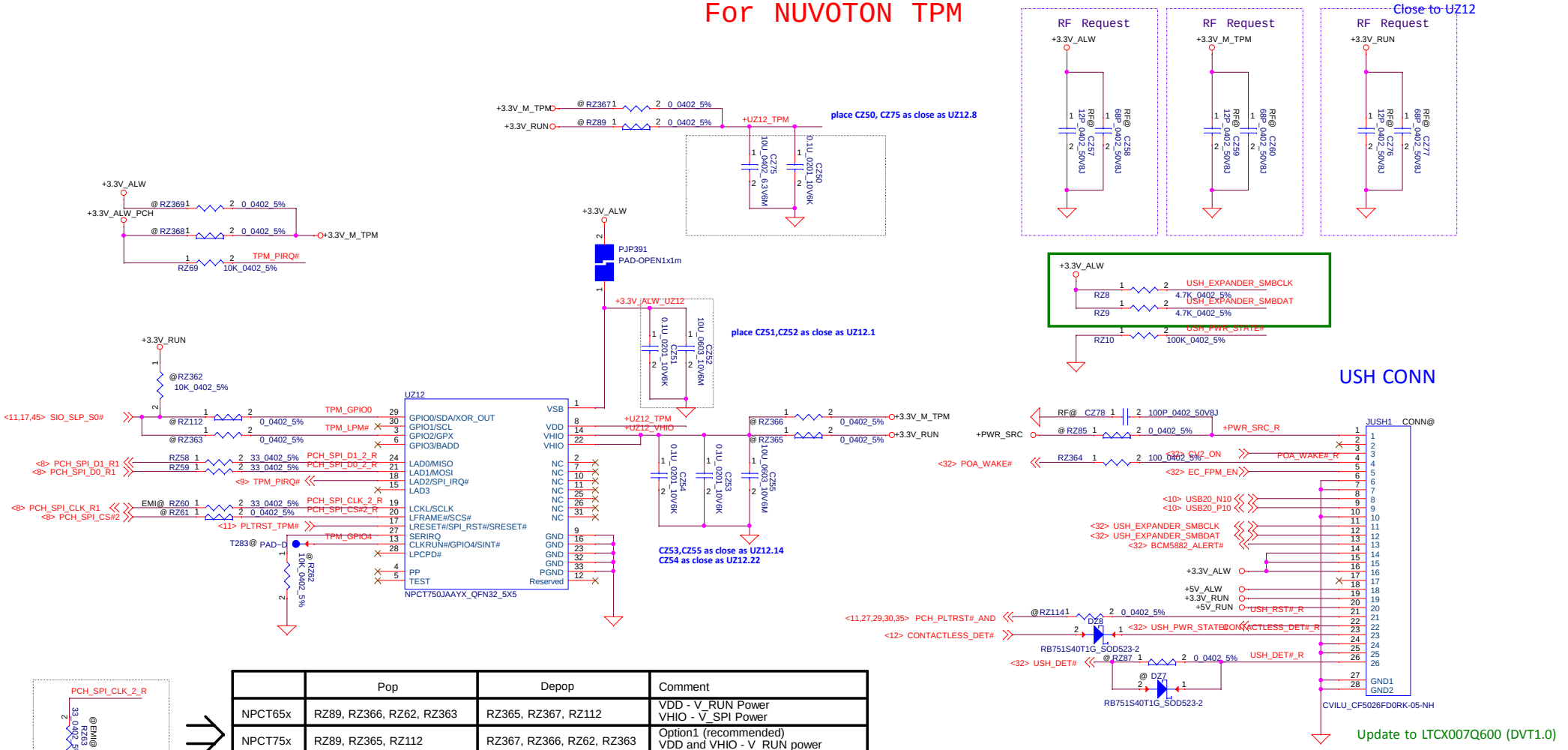
Stuff RE275 and no stuff RE274 keep ES design
Stuff RE274 and no stuff RE275 to save two GPIOs on EC(PCH_PCIE_WAKE# should be output with OD)

RF Request

DELL CONFIDENTIAL/PROPRIETARY

Title: MEC5105 support
Size: Document Number: LA-F322P
Rev: 2.0
Date: Friday, December 29, 2017 Sheet 33 of 59

For NUVOTON TPM



	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V_RUN Power VHIO - V_SPI Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V_RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V_SPI power

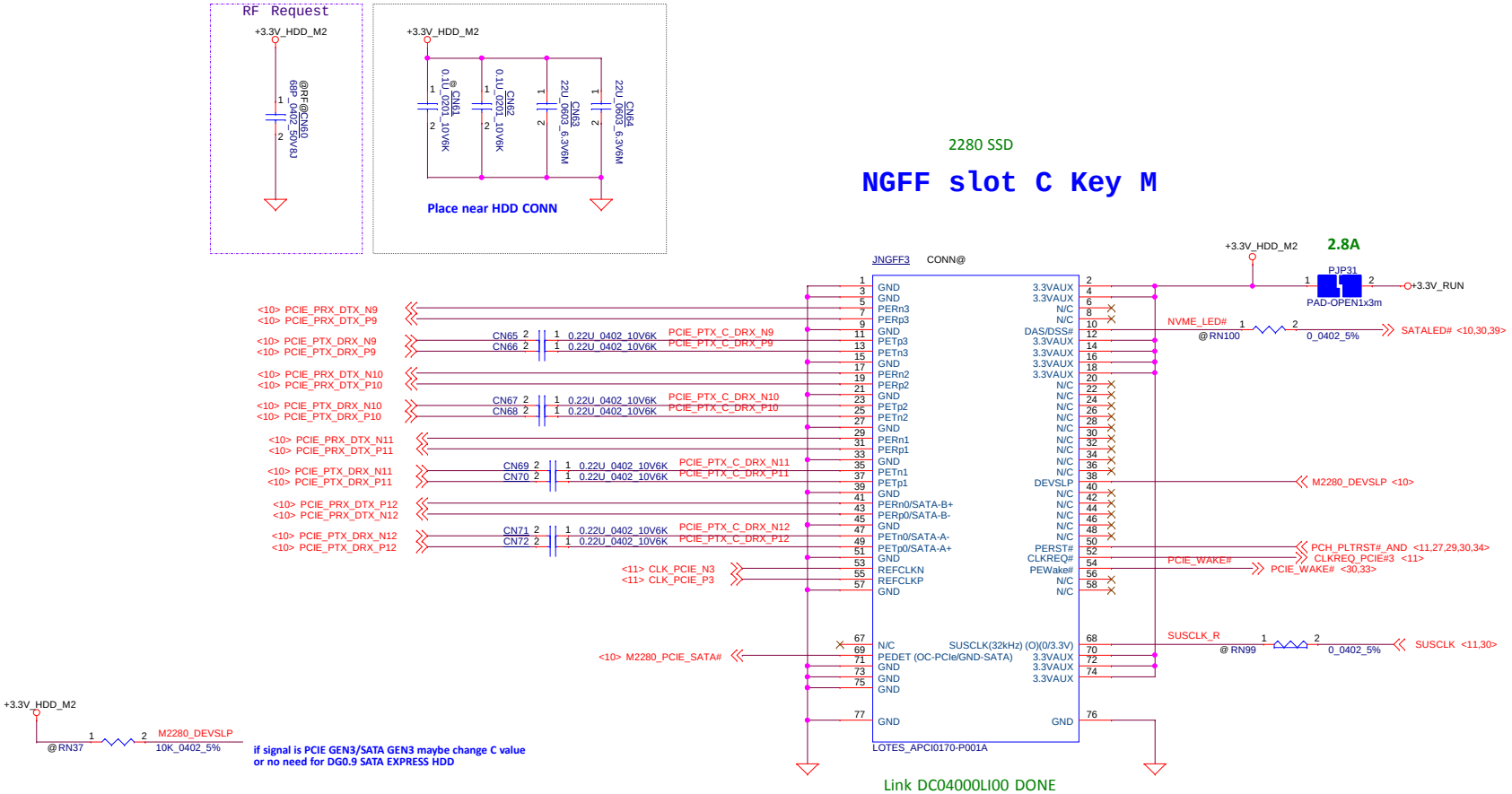
Compal Electronics, Inc.

Title: USH & TPM

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 34 of 59

For Brekenridge 12/14/15 UMA/Steamboat

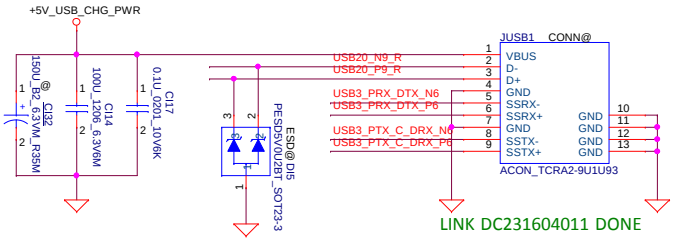


Compal Electronics, Inc.

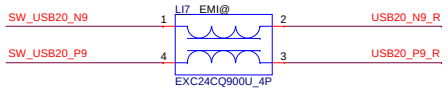
Title: M2 2280 Socket

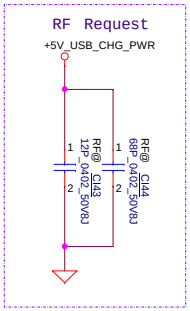
Size | Document Number: LA-F322P | Rev: 2.0

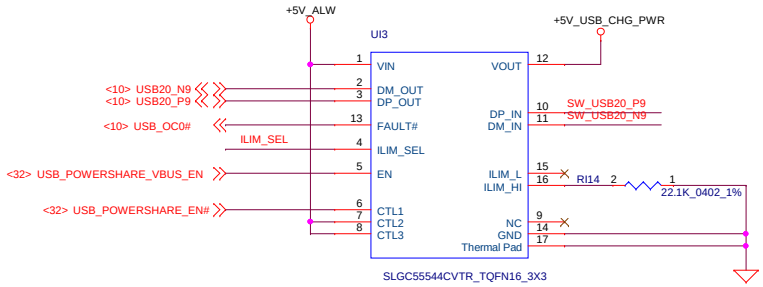
Date: Wednesday, December 20, 2017 | Sheet 35 of 59



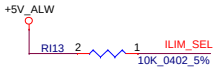
LINK DC231604011 DONE

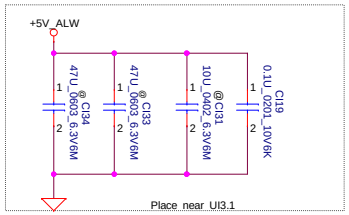






SA000097E10 Link Done





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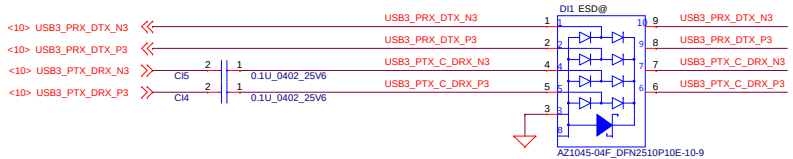
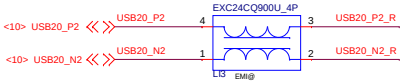
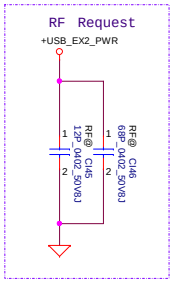
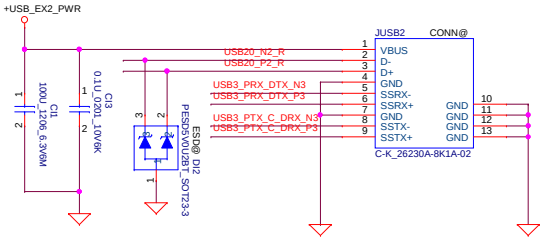
Compal Electronics, Inc.	
Title	JUSB1+PS
Size	Document Number: LA-F322P
Rev	2.0
Date:	Wednesday, December 20, 2017
Sheet	36 of 59

For Breckenridge 14&15/Steamboat 14



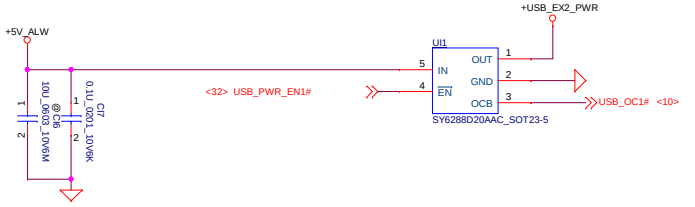


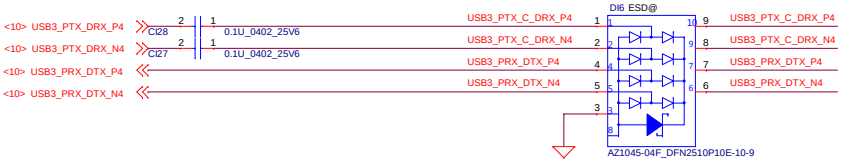


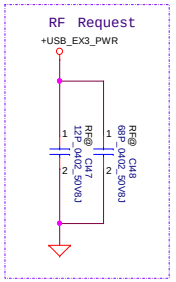


Link DC231604112(Temp) DONE

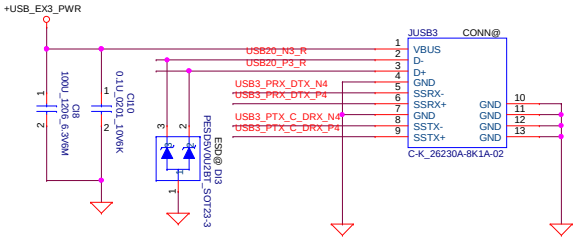
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



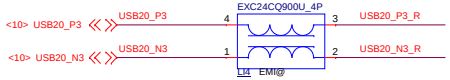


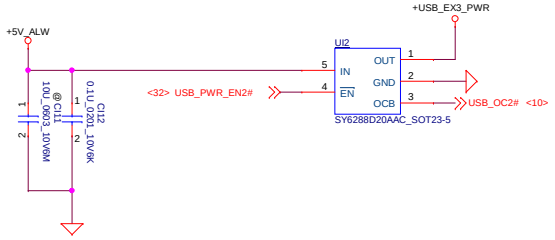


12" not support



Link DC231604112(Temp) DONE





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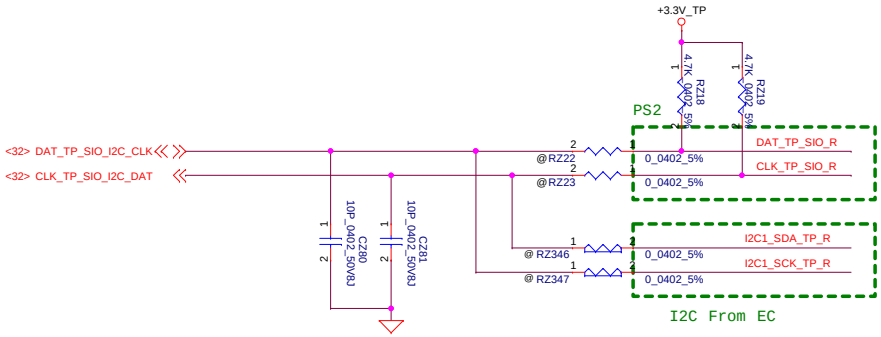
Compal Electronics, Inc.

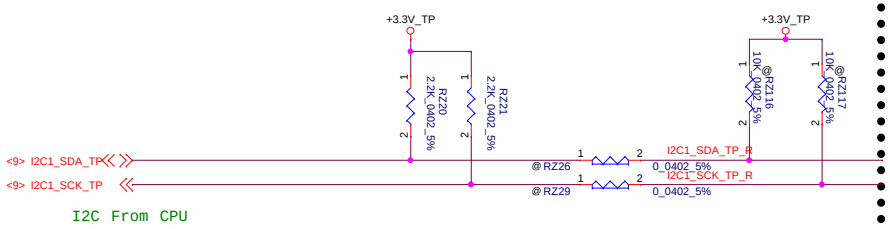
Title: JUSB2&JUSB3

Size | Document Number: LA-F322P | Rev: 2.0

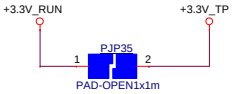
Date: Wednesday, December 20, 2017 | Sheet 37 of 59

Touch Pad

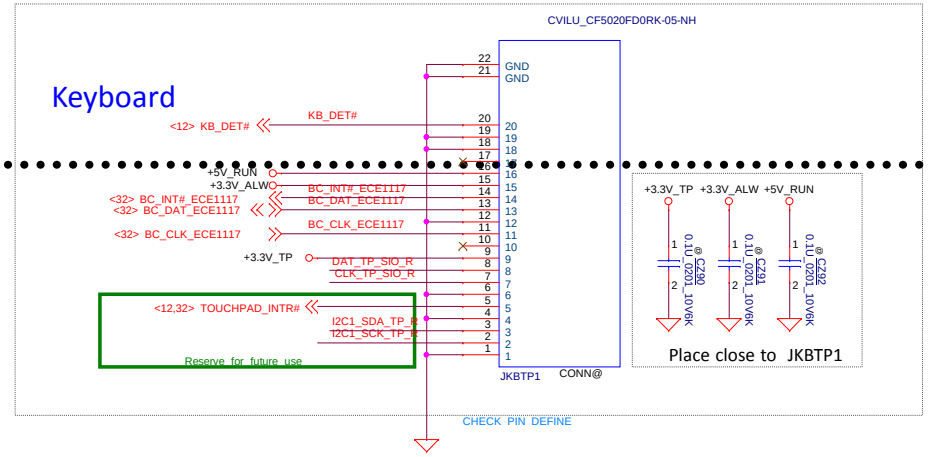




Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

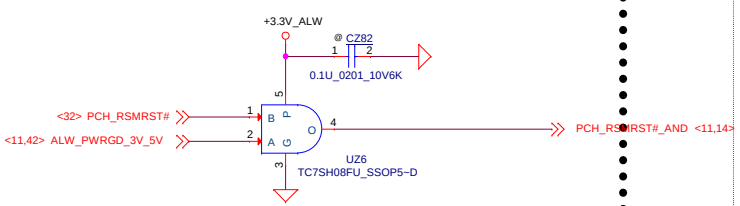


Keyboard



Update to LTCX007Q500 (DVT1.0)

RSMRST circuit



Compal Electronics, Inc.

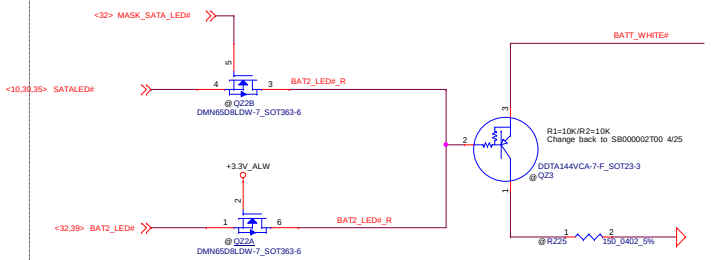
Title: Keyboard

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 38 of 59

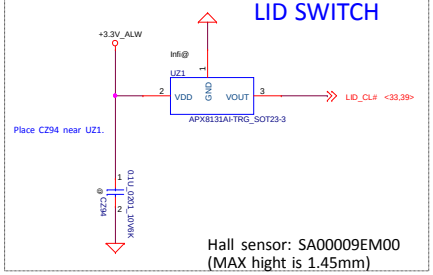
HDD LED MUX

means EC can switch battery white led and HDD LED by hot key " Fn+R

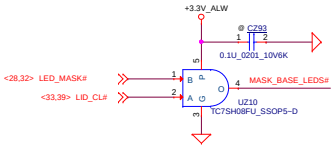


Bat tery LED

LID SWITCH

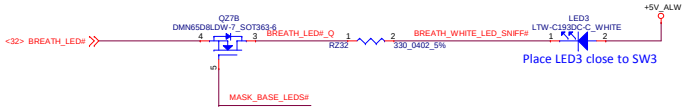


Hall sensor: SA00009EM00
(MAX hight is 1.45mm)

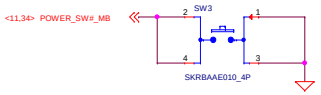


Breath LED

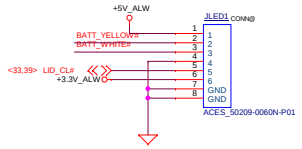
LED P/N change to SC50000FL00 from SC50000BA00



POWER & INSTANT ON SWITCH



LED board CONN

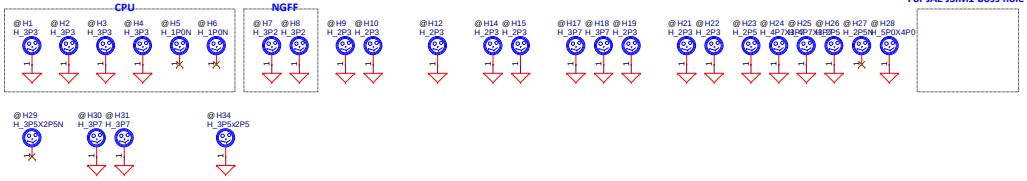


Fiducial Mark

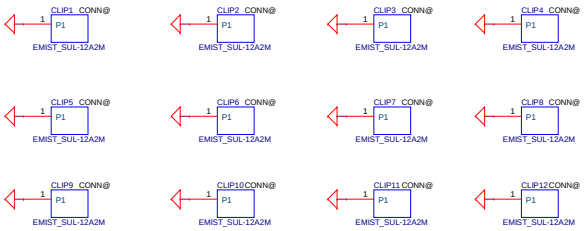
@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



For JAE JSIM1 boss hole



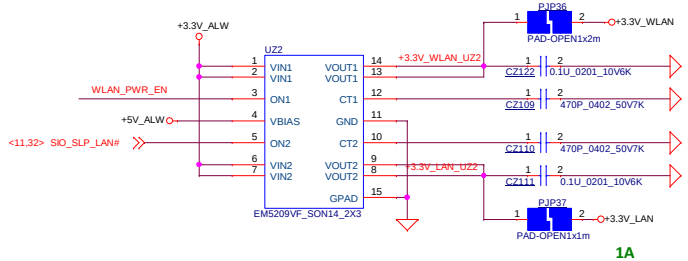
Compal Electronics, Inc.

Title: PAD, LED

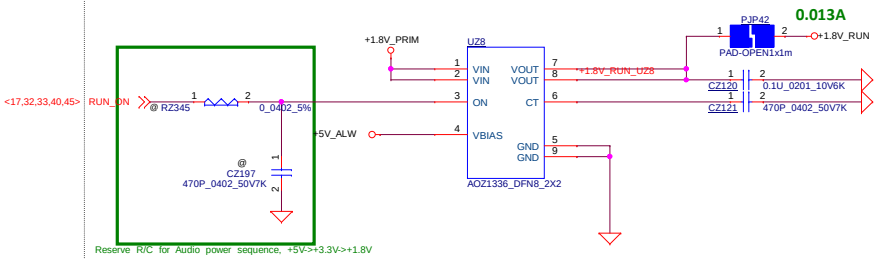
Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 39 of 59

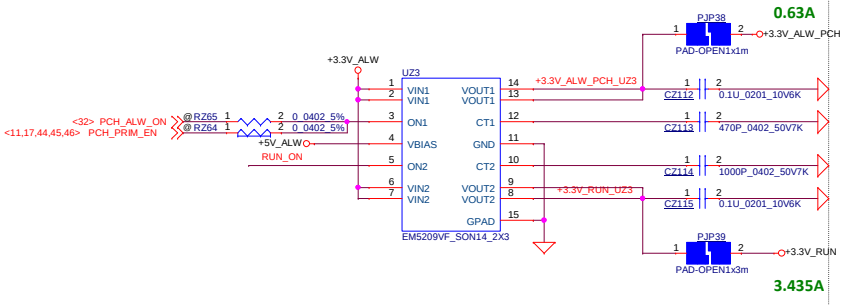
+3.3V_WLAN/+3.3V_LAN source

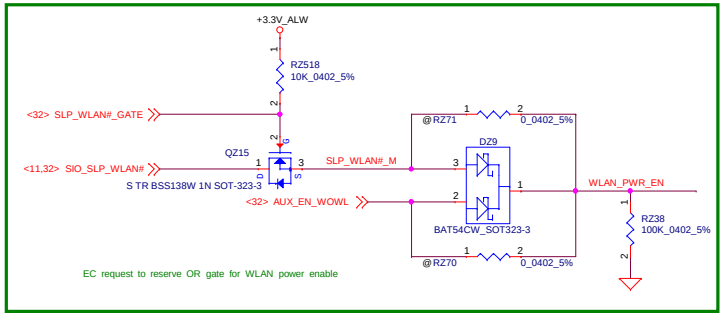


+1.8V_RUN source

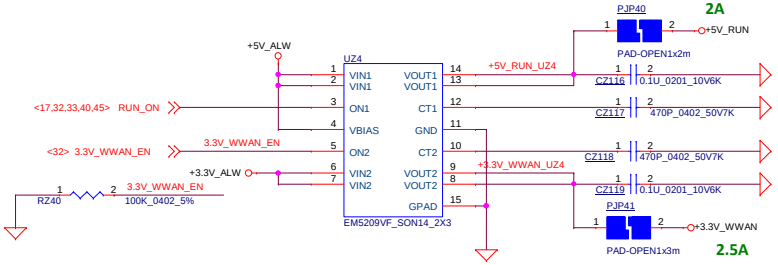


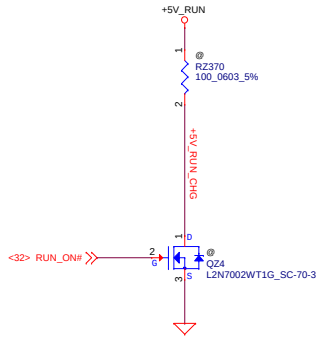
+3.3V_ALW_PCH/+3.3V_RUN source



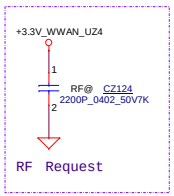


+5V_RUN/+3.3V_WWAN source





Reserve for S3 no power issue (+5V_RUN discharge circuit)

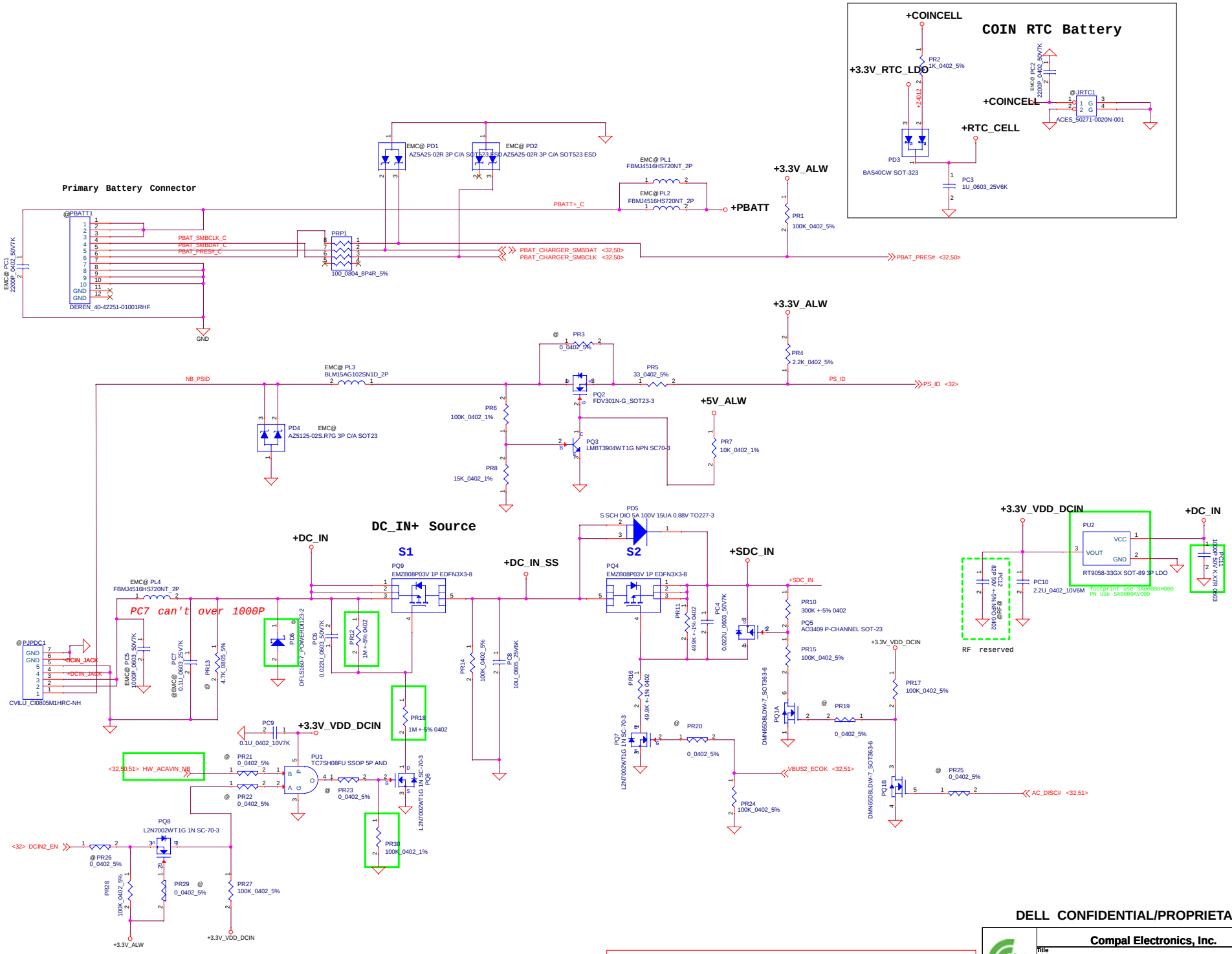


Compal Electronics, Inc.

Title: Power control

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 40 of 59



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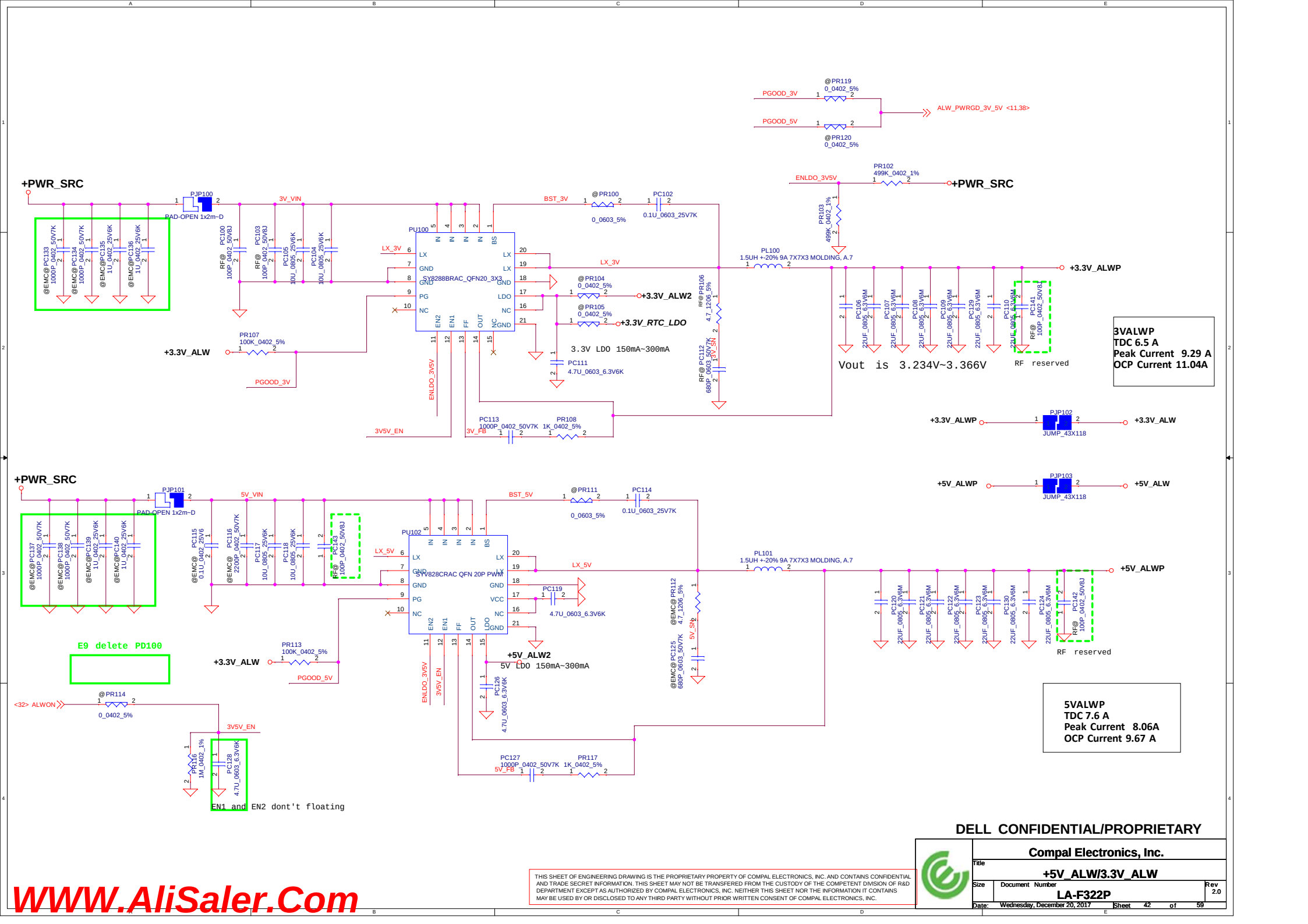
Compal Electronics, Inc.			
Title: +DCIN			
Size	Document Number: LA-F322P		Rev: 2.0
Date: Wednesday, December 20, 2017	Sheet 41 of 59		



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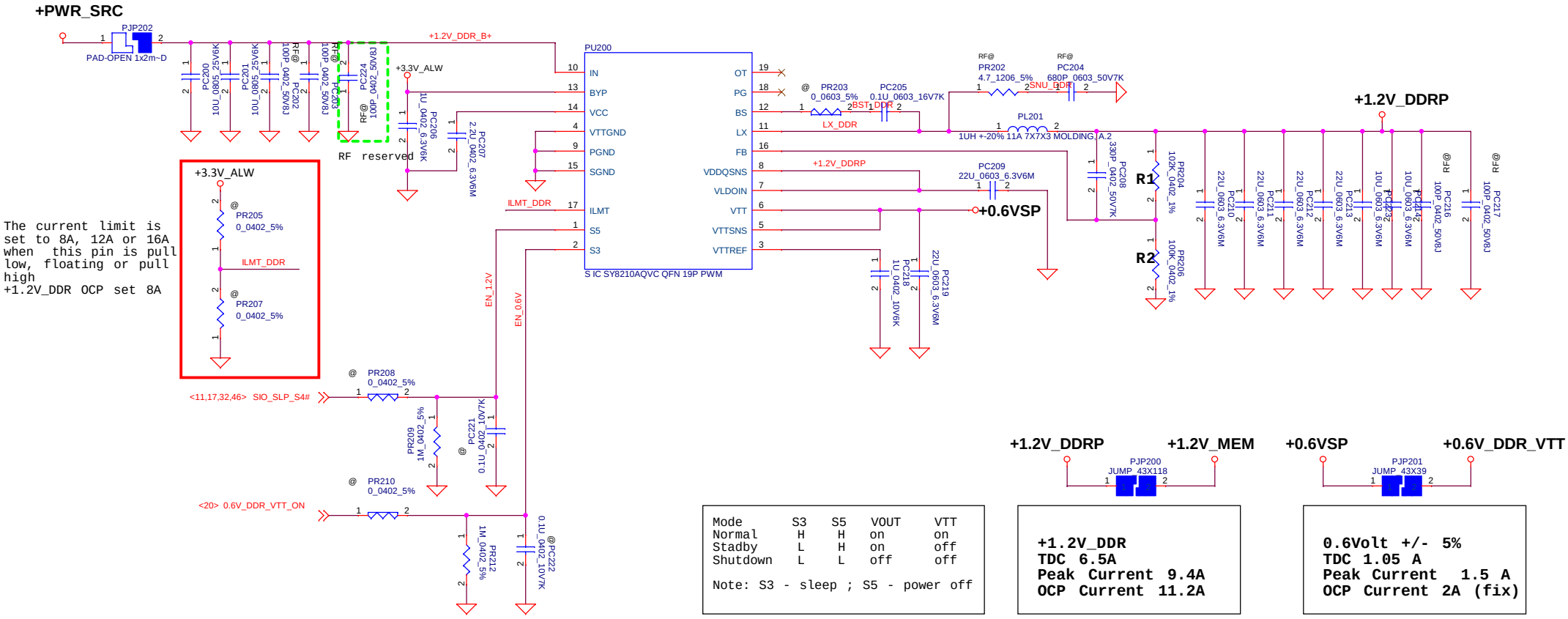
Compal Electronics, Inc.	
Title	+5V_ALW/3.3V_ALW
Size	Document Number: LA-F322P
Rev	2.0
Date:	Wednesday, December 20, 2017
Sheet	42 of 59



Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 6.5A
Peak Current 9.4A
OCP Current 11.2A

0.6Volt +/- 5%
TDC 1.05 A
Peak Current 1.5 A
OCP Current 2A (fix)

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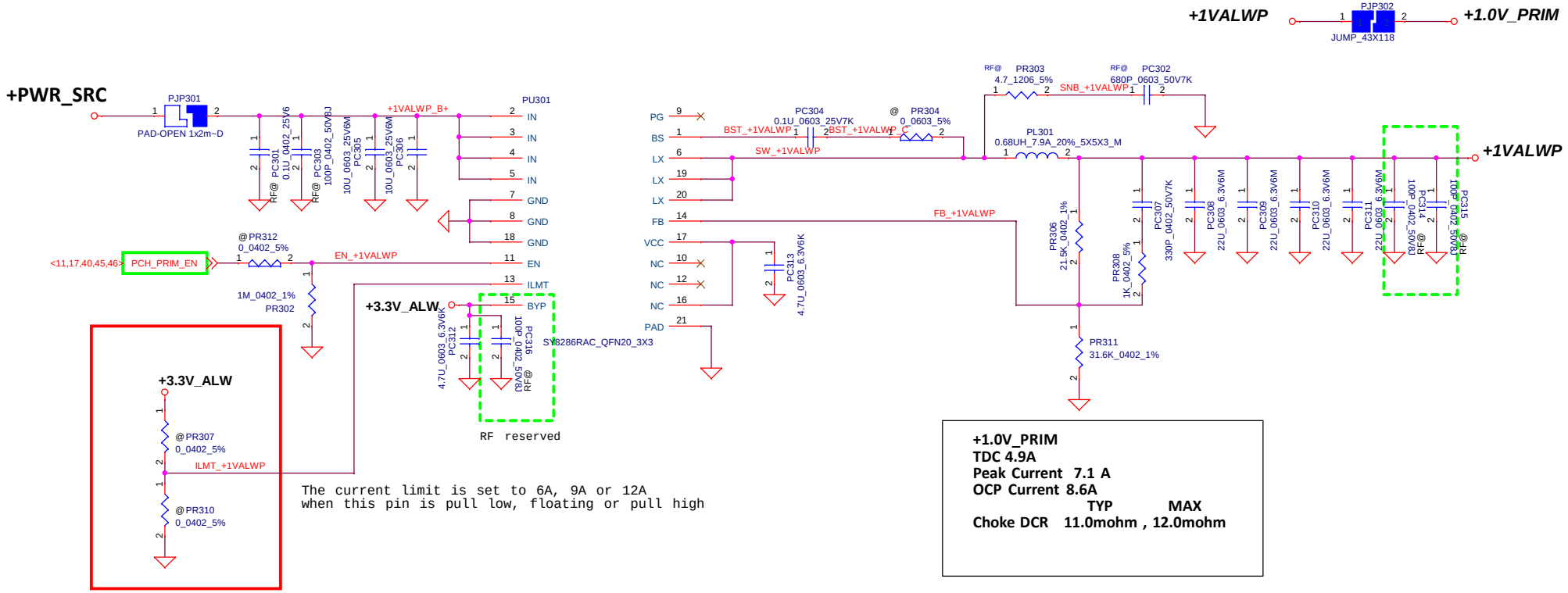
Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 43 of 59

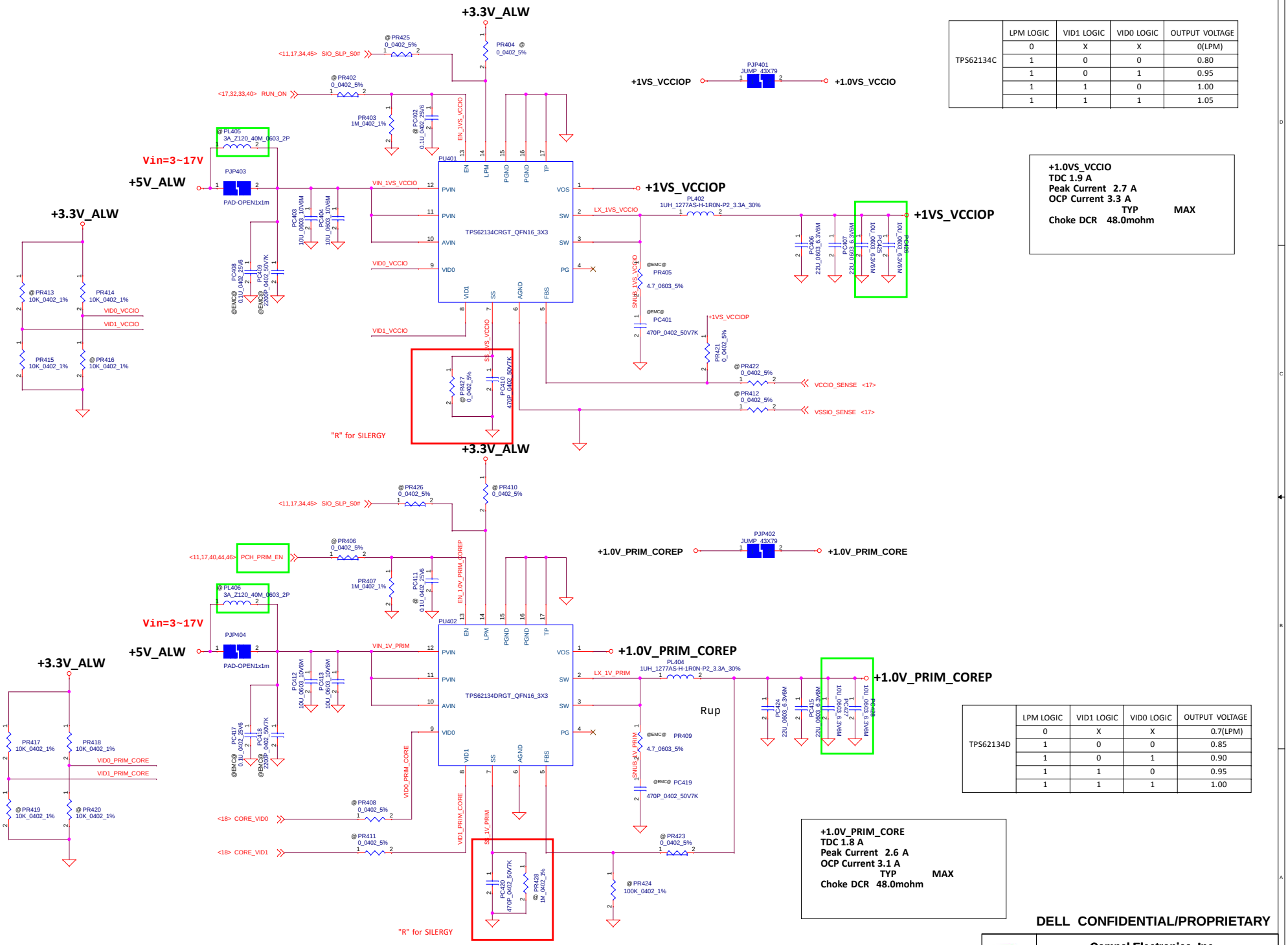


Compal Electronics, Inc.

Title: +1VALWP

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 44 of 59



TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A

	TYP	MAX
Choke DCR	48.0mohm	

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A

	TYP	MAX
Choke DCR	48.0mohm	

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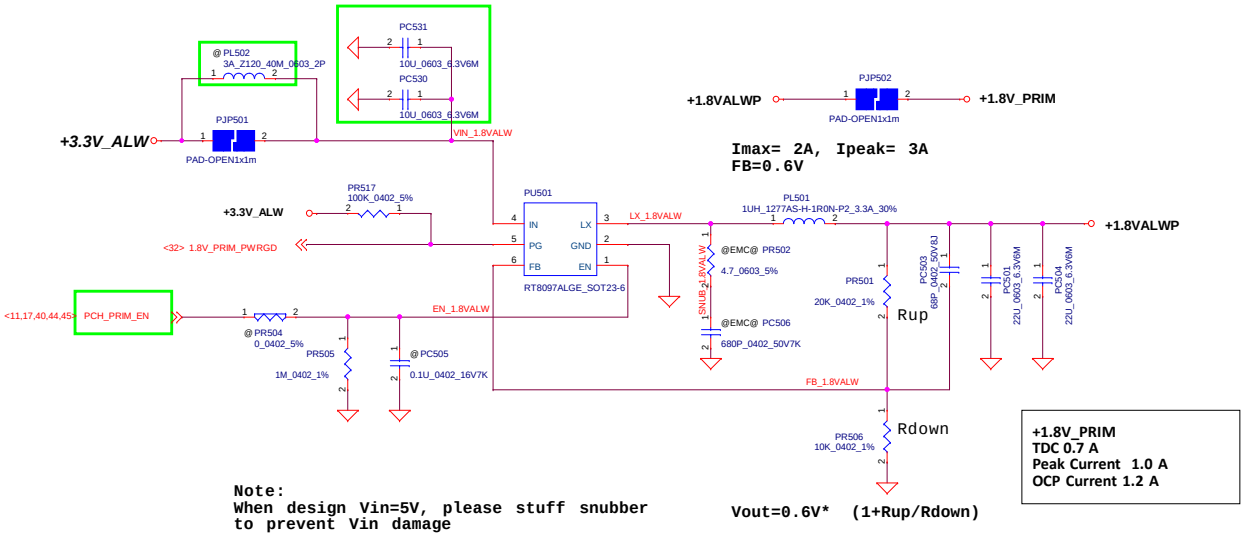
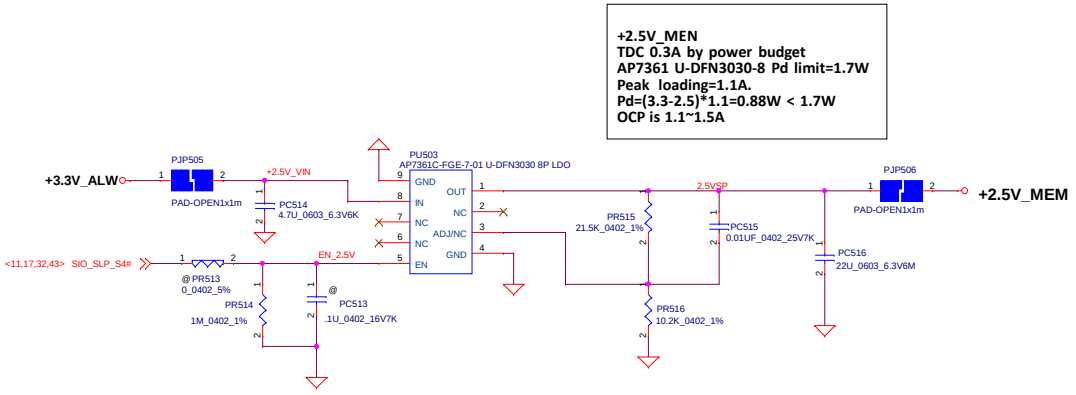
Compal Electronics, Inc.

Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

Size: | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 45 of 59



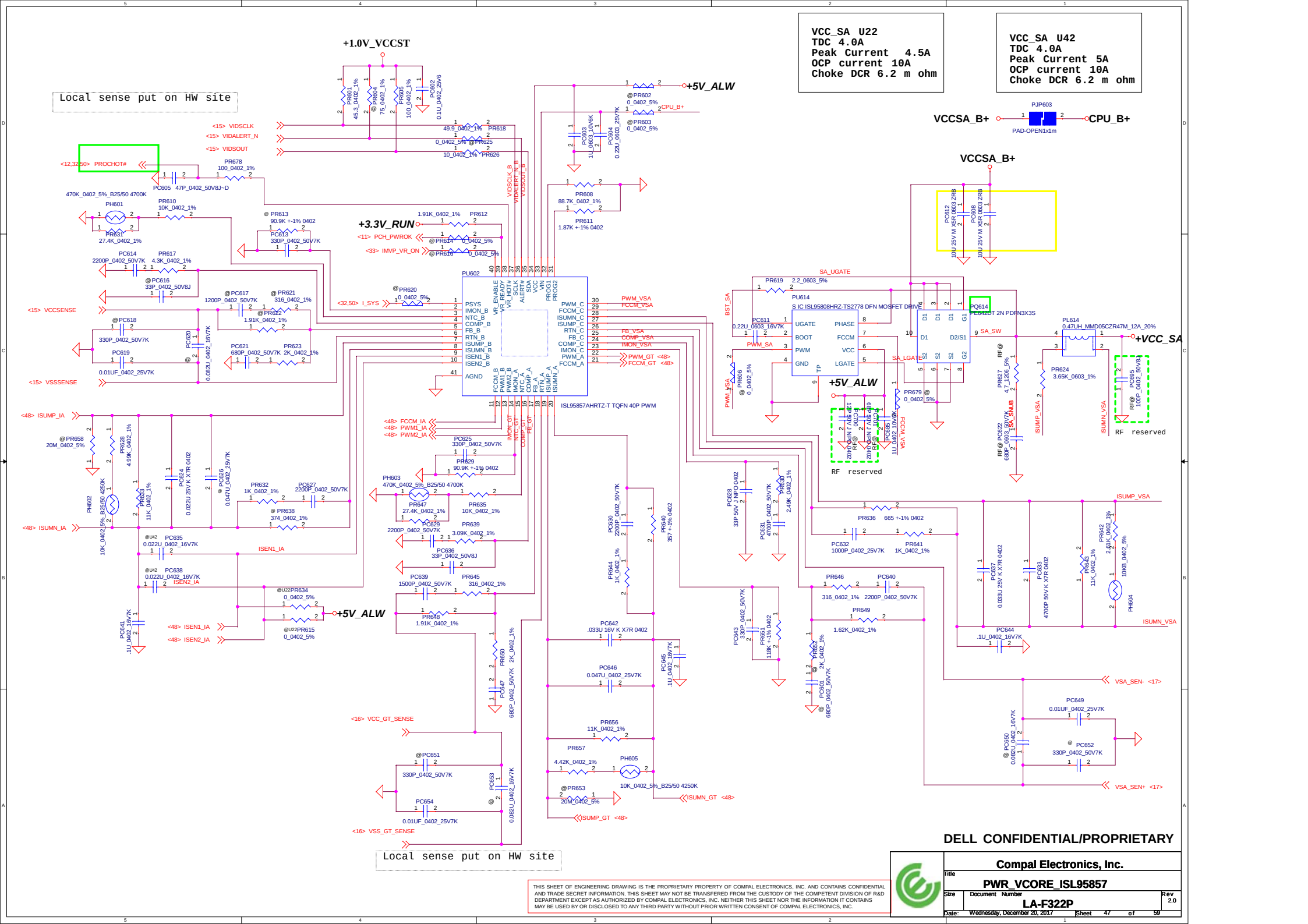


Compal Electronics, Inc.

Title: +1.8VALWP/+1.5VSP

Size | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 46 of 59


VCC_SA U22
TDC 4.0A
Peak Current 4.5A
OCP current 10A
Choke DCR 6.2 m ohm
VCC_SA U42
TDC 4.0A
Peak Current 5A
OCP current 10A
Choke DCR 6.2 m ohm
Local sense put on HW site
+1.0V_VCCST
+5V_ALW
+3.3V_RUN
VCCSA_B+
CPU_B+
PJP603
PAD-OPEN1x1m
PU602
ISL95857AHRTZ-T TQFN 40P PWM
PU614
S IC ISL95808HRZ-TS2778 DFN MOSFET DRIVE
PQ614
PE642DT 2N PDFN3X3S
+VCC_SA
RF reserved
Local sense put on HW site
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Title
PWR_VCORE_ISL95857
Size
Document Number
LA-F322P
Rev
2.0
Date: Wednesday, December 20, 2017
Sheet 47 of 59

VCC_core (U22)
TDC 21A
Peak Current 32A
OCP current 38.4A
Choke DCR 0.9 +-5%m ohm

VCC_core (U42)
TDC 42A
Peak Current 64A
OCP current 76.8A
Choke DCR 0.9 +-5%m ohm

For KBL U42 : Pop PR682 and PR684
For KBL U22 : Pop PR683 and PR685

U42

PC626 @U42 0.1U 25V 0402
PR613 @U42 93.1K +-1% 0402
PR621 @U42 1K +-1% 0402
PR638 @U42 464 +-1% 0402
PR622 @U42 3.09K_0402_1%
PC616 @U42 68P 50V J 0402
PC617 @U42 220P 50V 0402

U22

PC626 @U22 0.047U_0402_25V7K
PR613 @U22 90.9K +-1% 0402
PR621 @U22 316 +-1% 0402
PC617 @U22 1200P 50V 0402
PR638 @U22 365 +-1% 0402
PR622 @U22 1.5K +-1% 0402
PC616 @U22 33P 50V J 0402

VCC_GT (U22)
TDC 18A
Peak Current 31A
OCP current 37.2A
Choke DCR 0.9 +-5%m ohm

VCC_GT (U42)
TDC 12A
Peak Current 28A
OCP current 33.6A
Choke DCR 0.9 +-5%m ohm

RF demand

RF reserved

Compal Electronics, Inc.

Title: PWR_VCORE_ISL95857

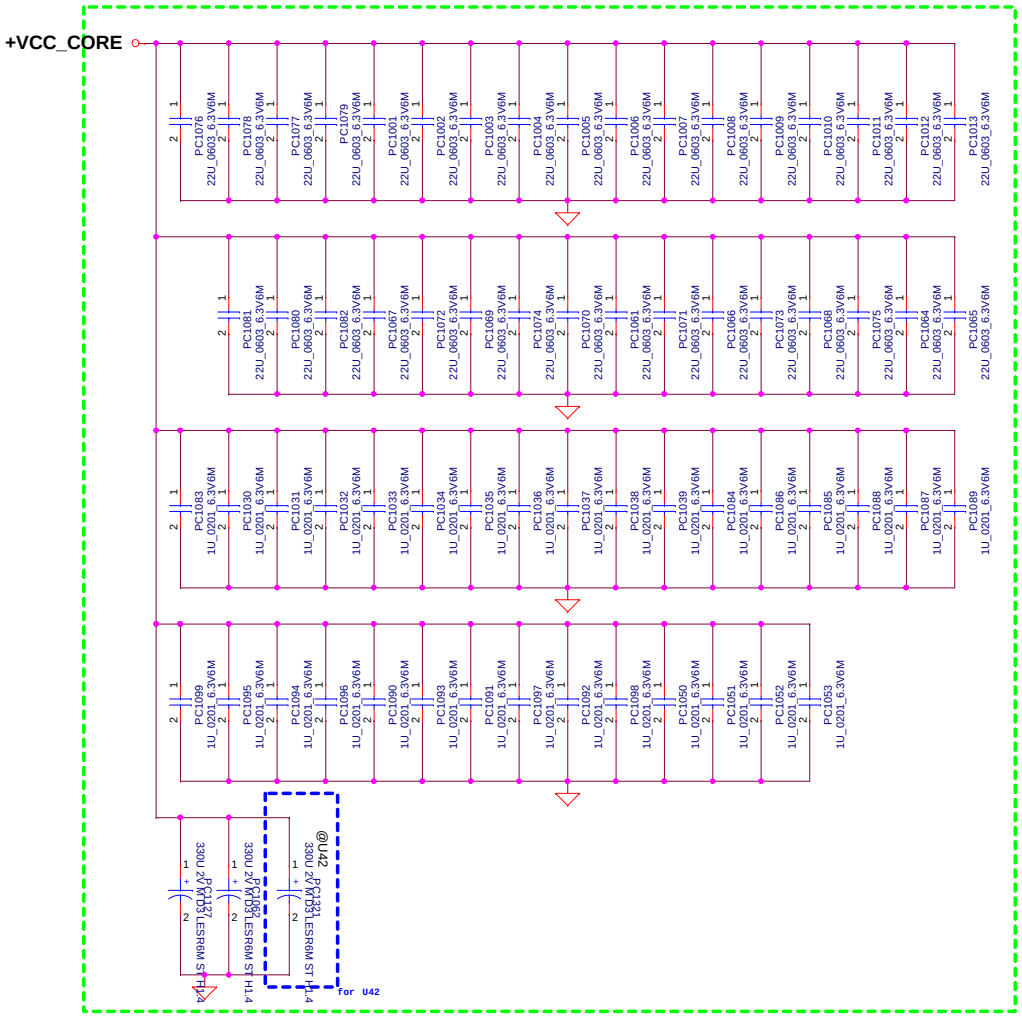
Size: | Document Number: LA-F322P | Rev: 2.0

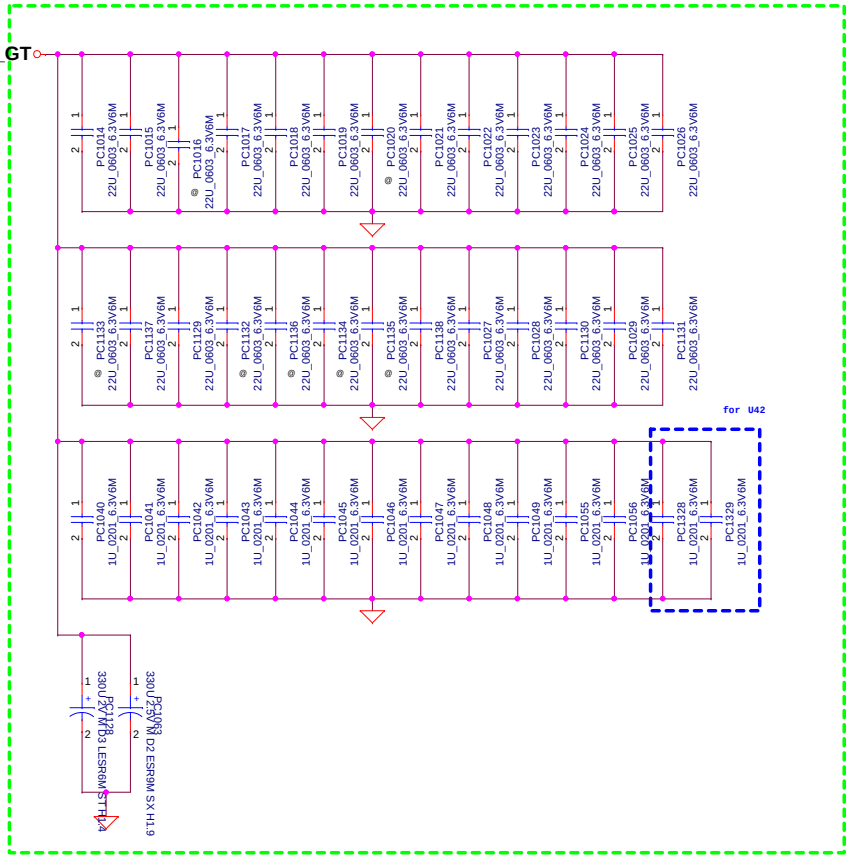
Date: Wednesday, December 20, 2017 | Sheet 48 of 59

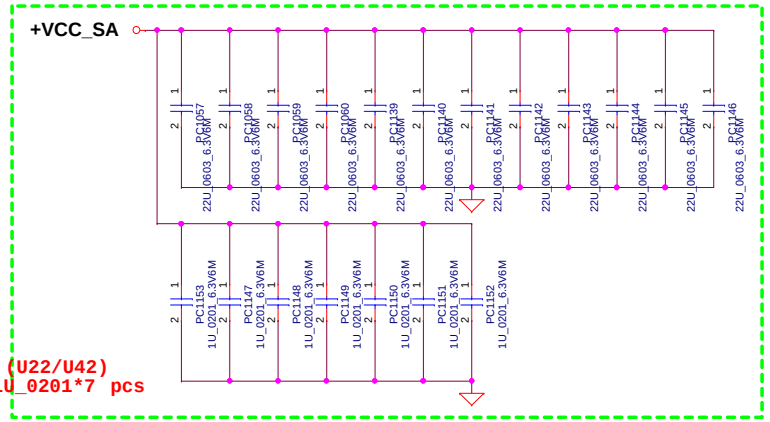
VCC_CORE Place on CPU (U22)
22U_0603 * 33 pcs +1U_0201*31 pcs
+330u_D3*2 pcs

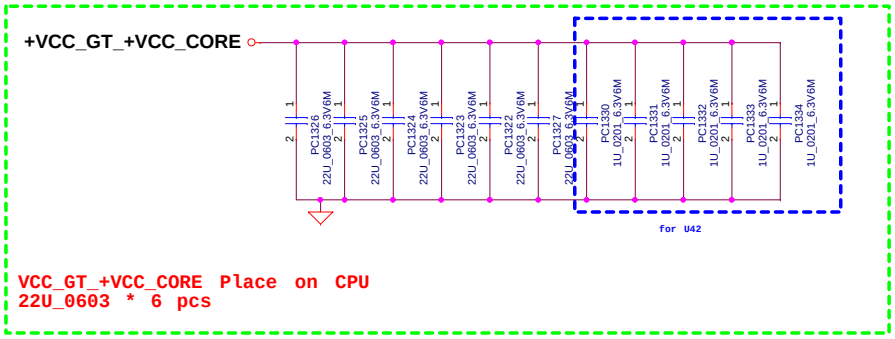
VCC_CORE Place on CPU (U42)
22U_0603 * 33 pcs +1U_0201*31 pcs
+330u_D3*3 pcs

VCC_GT Place on CPU (U22/U42)
22U_0603 * 19 pcs +1U_0201*14 pcs
+330u_D3*2 pcs









VCC_SA Place on CPU (U22/U42)
22U_0603 * 12 pcs + 1U_0201*7 pcs

VCC_GT_+VCC_CORE Place on CPU
22U_0603 * 6 pcs

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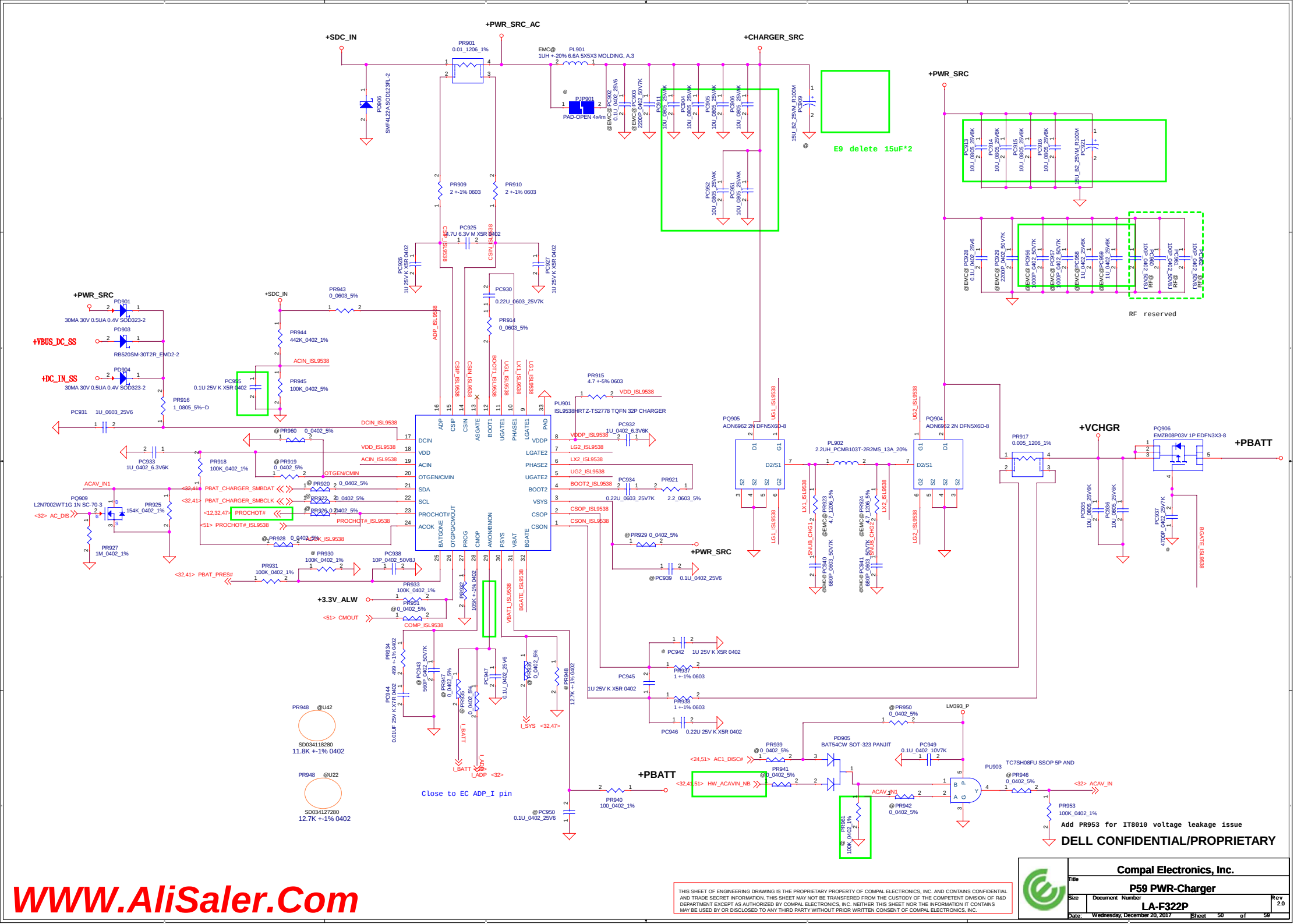
Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size: | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 49 of 59

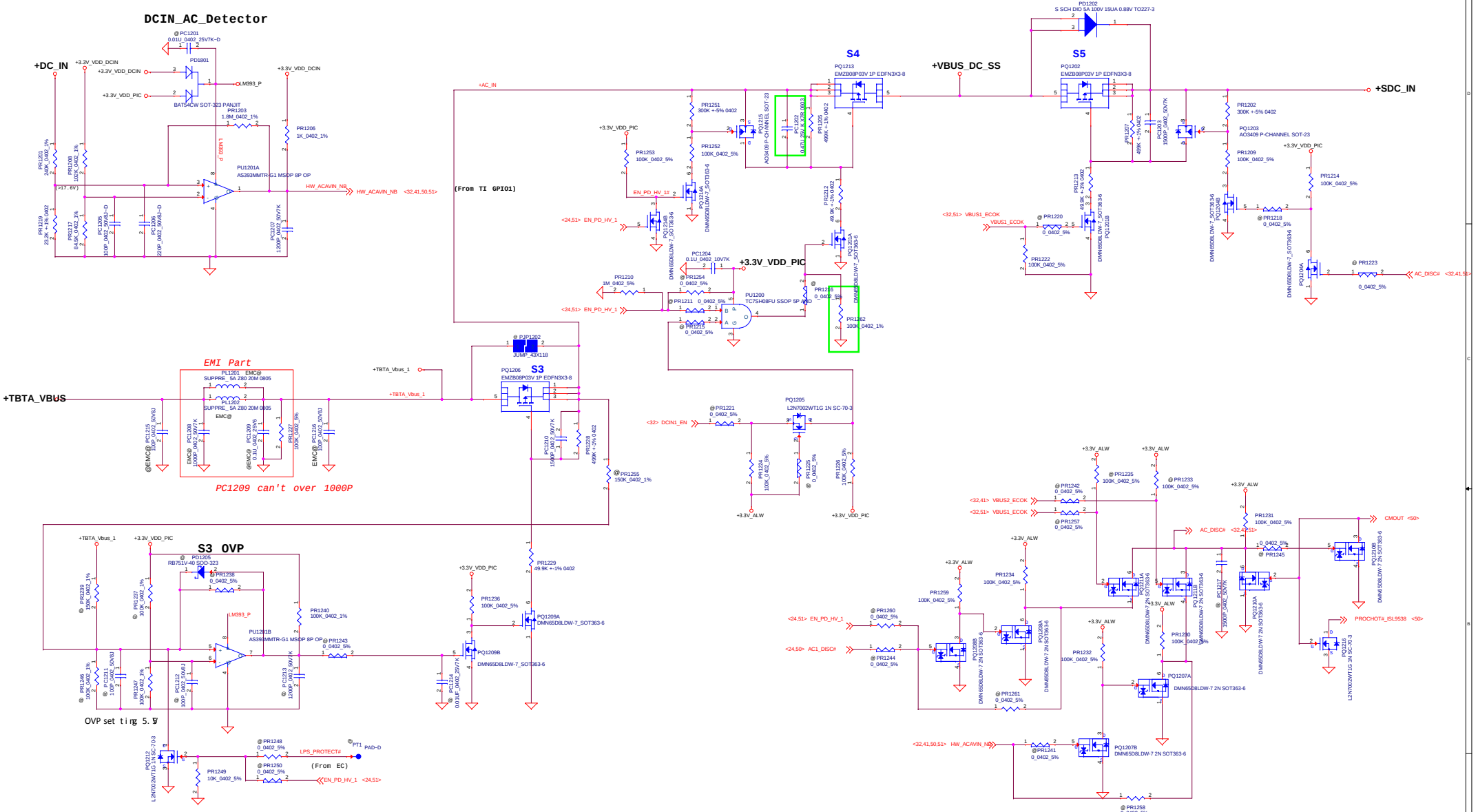


Compal Electronics, Inc.

Title: P59 PWR-Charger

Size: | Document Number: LA-F322P | Rev: 2.0

Date: Wednesday, December 20, 2017 | Sheet 50 of 59



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Compal Electronics, Inc.	
Title	TypeC_PD
Size	Document Number: LA-F322P
Rev	2.0
Date: Wednesday, December 20, 2017	Sheet 51 of 59

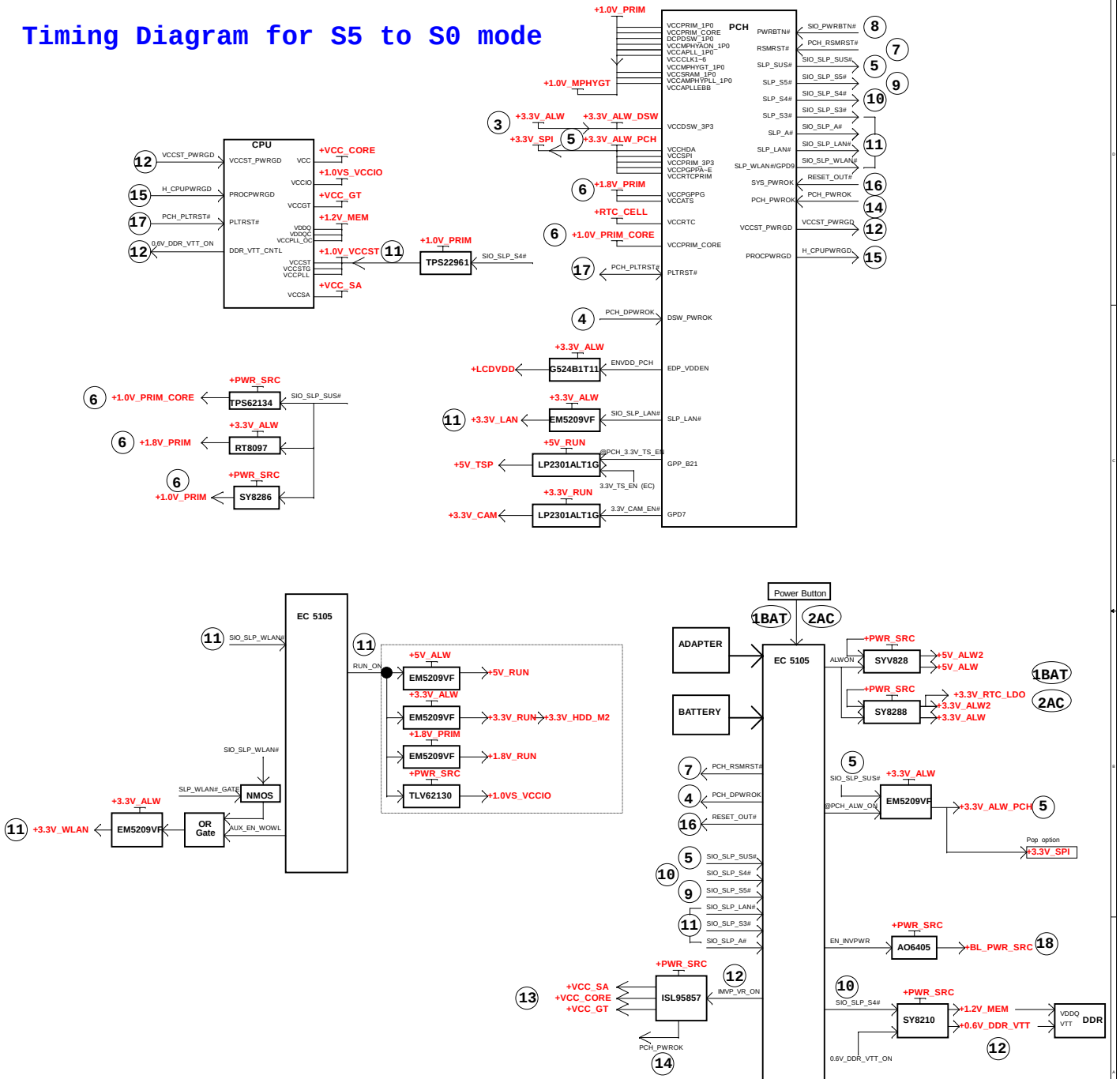
Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	57	VCC_CORE VCORE_VGT,VSA	2017 06/08	Compal	TI DrMOS (CSD97396) material shortage	PU610/ PU612/ PU613 change to FDMF3035 (SA0000AHX00)	X01
2	57	VCC_CORE VCORE_VGT,VSA	2017 06/08	Compal	Acoustic solution	Pop 2pcs 100uf (PC606 ,PC607)	X01
3	57	VCC_CORE VCORE_VGT,VSA	2017 06/08	Compal	Acoustic solution	VCORE input change to low noise MLCC (SE00000X210)	X01
4	59	Charger	2017 06/08	Compal	Acoustic solution	charger output emove 10uf*4 (PC916,PC917,PC918,PC919,PC920) and replace 1pcs 15uf_POSCAP(PC921)	X01
5	51,56 57,59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Compal	EMI request	Remove PC133,PC134,PC135,PC136,PC137,PC138,PC139,PC140 Remove PC689,PC690,PC691,PC692 Pop PL901 ,depop PJP901 Remove PC956,PC957,PC958,PC959	X01
6	51,56 57,59	+3.3V_ALW, +5V_ALW VCC_CORE VCORE_VGT,VSA Charger	2017 06/12	Compal	RF request	reservePC12,PC141,PC142,CP143,PC224,PC314,PC315,PC316,PC693, PC694,PC695,PC696,PC697,PC706,PC960,PC961,PC962	X01
7	59	charger	2017 08/04	Compal	for PU901 burn out issue	New add TVS Diode PD906 before PL901	X02
8	59	charger	2017 08/04	Compal	intersil FAE suggest	Change PR915,PR909,PR910,PR937,PR938 from 0402 to 0603.	X02
9	60	Type-C PD selector	2017 08/04	Compal	EMC request Type C bead change to 80 ohm	Tpye-C PD Bead EOL ,so change PL1201/PL1202 Bead to 80 ohm bead, CPN:SM01000P200=>SM01000U300(2nd) CPN:SM01000P200=>SM01000U400(main)	X02
10	510	charger	2017 08/04	Compal	intersil FAE suggest	For ISL9538 Psys resistance change value 1.UMA R-U42 UMA change to 11.8K 2.UMA U22 UMA keep use 12.7K	X02
11				Compal			
12				Compal			
13				Compal			
14				Compal			
15				Compal			
16				Compal			
17				Compal			
18				Compal			
19							
20							
21							
22							
23							

Compal Electronics, Inc.

Title			
PWR P.I.R			
Size	Document Number		Rev
	LA-F322P		2.0
Date: Wednesday, December 20, 2017	Sheet 52 of 58		

Timing Diagram for S5 to S0 mode



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Power Sequence

LA-F322P

Rev 2.0

Wednesday, December 20, 2017

Sheet 53 of 58

Version Change List (P. I. R. List)

LA-F322P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	8	CPU (3/14)	2017/03/21	EE	Winbond 16MB SPI ROM EOL (change to J-die)	Change UC5, UC6 to SA00005VV20	0.1(X00)
2	8	CPU (3/14)	2017/03/21	ME	JSPI1 connector change vendor	Change JSPI1 to SP010022Q00	0.1(X00)
3	11	CPU (6/14)	2017/03/21	EE	KBL-R U42 X'tal	Add RC415~RC420,CC334,CC335,YC3	0.1(X00)
4	13	CPU (8/14)	2017/03/21	EE	KBL-R CRB schematic	Add RC436 0ohm to GND	0.1(X00)
5	14	CPU (9/14)	2017/03/21	ME	JXDP1 connector change vendor	Change JXDP1 to SP01001VB00	0.1(X00)
6	16	CPU (11/14)	2017/03/21	EE	Follow KBL-R_U42_Processor_Line_BGA1356_ Ballout_Rev1p0	Reserve RC437, RC438	0.1(X00)
7	18	CPU (13/14)	2017/03/21	EE	RTC Power Gate Circuit for +3.3V_DSW	Add RC431~RC433, RC439, RC440, QC6, QC7	0.1(X00)
8	33	EC MEC5105	2017/03/21	EE	RTC Power Gate Circuit for RTCRST	Add QE14~QE17, RE540~RE546, RE551, CE63, RC441, RC442, DC1, DC2, RC445	0.1(X00)
9	34	EC MEC5105 Support	2017/03/21	EE	Remove IO expander	Remove UE2 relating circuit	0.1(X00)
10	28	eDP CONN & Touch screen	2017/03/21	ESD	ESD request	Remove DV7, DV8	0.1(X00)
11	35	USH & TPM	2017/03/21	EE	TPM NPCT65X and NPCT75X schematic colay	UZ12 relating circuit and change UZ12 to SA0000AQ200	0.1(X00)
12	31	NGFF Card	2017/03/21	RF	RF request to align w/ BR MLK	LI8, LI9 change to SM070003Z00, LI16, LI17 change to SM070003V00	0.1(X00)
13	33	EC MEC5105	2017/03/21	EE	RTCRST_ON glitch	Reserve CE64	0.1(X00)
14	All	All	2017/03/21	EE	Port map change	JUSB1 change to USB30_port6 and USB20_port9 USB20_port1 BOM option to Type-C(PD UT5) Delete PS8338 and WIGIG circuit and connect DDI2 to UT1 (Add RC446~RC448 for CPU_DP2_HPD/CPU_DP2_AUXP/CPU_DP2_AUXN)	0.1(X00)
15	27	eDP CONN & Touch screen	2017/03/21	EE	I2C touch screen for SB14 only	Change JTS1 to 10pin and add TS_I2C_SDA,TS_I2C_SCL,TS_INT#	0.1(X00)
16	24	[Type C]PD Controller TI	2017/03/28	EE	Change PD to PD3.0	Change UT5 to SA0000AP500	0.1(X00)
17	33	EC MEC5105 Support	2017/03/28	EE	Panel ID define change	RE300 change to 33K ohm	0.1(X00)
18	34	USH & TPM	2017/03/28	EE	Prevent POA_WAKE# ESD	Add RZ364 100 ohm to POA_WAKE#	0.1(X00)
19	34	USH & TPM	2017/03/28	EE	Prevent Contactless_det# backdrive	Add DZ8	0.1(X00)
20	26	[Type C]USB3.0 CONN	2017/03/28	ESD	ESD request	Change DT7, DT8, DT11, DT12 to DT39 Change DT15, DT16, DT19, DT20 to DT40	0.1(X00)
21	11	CPU (6/14)	2017/03/28	EE	RTC Power Gate Circuit option	Add RC441, RC442, DC1, DC2, RC445	0.1(X00)

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Title: EE P.I.R (1/6)
Size: Document Number: LA-F322P
Rev: 2.0
Date: Wednesday, December 20, 2017
Sheet 54 of 59

Version Change List (P. I. R. List)
LA-F322P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	All	All	2017/03/28	EE	GPIO map change	PCH_RSMRST#_GPIO204 -> USH_PWR_STATE# (delete RE363) PORT80_DET# -> DCIN1_EN (delete RE512,RE513,RZ131) SHD_IO3 -> VBUS1_ECOK SHD_IO1 -> SATA_LED_EN ENVDD_PCH -> DCIN2_EN SIO_RCIN#_EC -> VBUS2_ECOK and delete RE339/RC13 USH_SMBCLK -> USH_EXPANDER_SMBCLK USH_SMBDAT -> USH_EXPANDER_SMBCLK Delete RTCRST_ON_GPIO141 PRIM_PWRGD_GPIO024 -> RESET_IN# 3.3V_TS_EN rename to PCH_3.3_TS_EN SHD_IO0 change to 3.3V_TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V_TS_EN/PCH_3.3V_TS_EN option	0.1(X00)
23	27	eDP CONN & Touch screen	2017/03/30	EE	3MM_CAM detection	Add 3MM_CAM_DET# GPIO and add PU RV325	0.1(X00)
24	All	All	2017/03/30	EE	GPIO map change	PANEL_ID -> SYSTEM_ID SHD_IO1 -> SATA_LED_EN -> MASK_SATA_LED# EXPANDER_GPU_SMDAT -> VCCDSW_EN_GPIO and delete RE524 EXPANDER_GPU_SMCLK -> free and delete RE525 THERMATRIP1# -> THERMTRIP1# THERMATRIP2# -> THERMTRIP2# SIO_EXT_SCI#_EC -> free and delete RE341 FAN1_TACH -> TACH_FAN1 LCD_TST -> free WWAN_RADIO_DIS# -> LCD_TST EC GPIO123 (UE1.F12) -> WWAN_RADIO_DIS# DCIN3_EN -> EC GPIO202 (UE1.J6) (SBMLK 12/13 only) FAN1_PWM -> PWM_FAN1 PS_ID -> free SHD_CLK -> PS_ID and delete RE374 AUD_NB_MUTE# -> NB_MUTE#	0.1(X00)
25	All	All	2017/03/30	EE	GPIO map change	UE1.B1 -> add net name 3.3V_ALW2 and depop RE57 (Microchip suggest) RESET_IN# -> Remove RE361 (Microchip suggest) SLOT2_CONFIG_3 -> NGFF_CONFIG_3 ME_FWP -> ME_FWP_PCH ME_FW_EC -> ME_FWP HW_GPS_DISABLE# -> GPS_DISABLE# VGA_ID -> BEEP H_PROCHOT# -> PROCHOT# USB_PWR_SHR_VBUS_EN -> USB_POWERSHARE_VBUS_EN USB_PWR_SHR_LFT_EN# -> USB_POWERSHARE_EN# SIO_EXT_SMI#_EC -> free and delete RE338 CLKRUN#_EC -> ENABLE_DS# and delete RE337 and add RE549, RE550 SHD_IO2 -> 1.8V_PRIM_PWRGD and delete RE360 BEEP -> VGA_IDENTIFY (rename from VGA_ID) SHD_CS# -> PCH_RSMRST# and delete RE364 SLOT2_CONFIG_0 -> NGFF_CONFIG_0 SLOT2_CONFIG_1 -> NGFF_CONFIG_1 SLOT2_CONFIG_2 -> NGFF_CONFIG_2 ACAV_IN_NB -> HW_ACAVIN_NB LID_CL#_NB -> LID_CL_SIO# SYS_PWROK->reserved 0ohm RE548 and add netname to RESET_OUT	0.1(X00)
							0.1(X00)

Version Change List (P. I. R. List)
LA-F322P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
26	All	All	2017/03/30	EE	Port map change	NGFF3 (SSD 4 Lane) add PCIE port 9 and port 10 LOM change to PCIE port 4	0.1(X00)
27	11 32	CPU (6/14) EC MEC5105	2017/04/05	EE	Intel PDG for DSx and NonDSx	Add RC443, RC444 for SUSACK#, ME_SUS_PWR_ACK Add BOM structure DS3@ for RE349 and RE536	0.1(X00)
28	17 40	CPU (12/14) Power control	2017/04/05	EE	PCH_PRIM_EN net name change	Change net name from SIO_SLP_SUS# to PCH_PRIM_EN	0.1(X00)
29	33	EC MEC5105 Support	2017/04/05	EE	Microchip suggest	Change RE71 to 10 ohm	0.1(X00)
30	40	Power control	2017/04/05	EE	+5V_RUN discharge circuit for S3 no power issue	Add QZ4 and RZ370	0.1(X00)
31	9	CPU (4/14)	2017/04/06	EE	RF need to validate Active Steering Antenna for SB14 only	Change JUART1 to SP01002LL00 and add RC434, RC435 for power option	0.1(X00)
32	33	EC MEC5105 Support	2017/04/11	EE	+5V_RUN for FAN	Change DE1 to SC400002J00	0.1(X00)
33	40	Power control	2017/04/14	EE	EC request to reseve OR gate for WLAN power EN	Reserve DZ9	0.1(X00)
34	33	EC MEC5105 Support	2017/04/14	EE	EC request to reseve ESPI_RESET# for JESPI	Reserve RE560	0.1(X00)
35	32	EC MEC5105	2017/04/14	EE	Schmatic align	Add GPU_SMCLK/GPU_SMDAT PU to RPE12	0.1(X00)
36	11	CPU (6/14)	2017/04/14	EE	WIGIG feature remove	Add back RC50 and depop	0.1(X00)
37	31	CodeC ALC3246	2017/04/14	EE	Realtek request	CA54 change back to 10pf and depop	0.1(X00)
38	32 11	EC MEC5105 CPU (6/14)	2017/04/14	EE	RTC power Gate circuit rev.2 (0411)	Delete RE540, RE542, RE544, RE545, QE14, QE16 Change RE543 to 1M ohm and RE546 to 10K ohm Add DE2, CE65, Reserve CE66 for VCCDSW_EN	0.1(X00)
39	11	CPU (6/14)	2017/04/14	EE	RTC Power Gate Circuit option (0411)	RC445 change to connect to VCCDSW_EN and pop	0.1(X00)
40	9	CPU (4/14)	2017/04/14	RF	I2C interface for Active Steering Antenna (SB14 only)	Add RC510~RC513, QC4 (1.8v level shift), RC546~RC549	0.1(X00)
41	10 24	CPU (5/14) [Type C]PD Controller TI	2017/04/14	EE	OTG support	Pop RT74, Depop RC337	0.1(X00)
42	13	CPU (8/14)	2017/04/19	EE	KBL-R CRB schematic	Add BOM structure for RC436 U42@	0.1(X00)
43	All	All	2017/04/19	EE	GPIO map change	RC443 BOM structure change to @ GPIO126->GPU_PWR_LEVEL Add RTCRST_ON_R net neme for QE17.2 Add SIO_SLP_SUS#_R net name and PU RE561 SYS_LED_MASK#->LED_MASK# RC27.2->NC for CLKRUN# HDD_DET#->SATAGP0 Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN	0.1(X00)
44	34	USH & TPM	2017/04/19	EE	TPM change to NPCT650x	Change UZ12 to SA00008EL80 and related resistors	0.1(X00)
45	9	CPU (4/14)	2017/04/19	RF	I2C interface for Active Steering Antenna (SB14 only)	Swap I2C3_SDA and I2C3_SCL	0.1(X00)

Version Change List (P. I. R. List)
LA-F322P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
46	32	EC MEC5105	2017/04/19	EE	Dell request to add test point for EC free pins	Add test point T141 for UE1.D1->GPIO051 Add test point T142 for UE1.L11->GPIO054 Add test point T264 for UE1.F13->VBUS3_ECOK Add test point T143 for UE1.K7->GPIO011 Add test point T144 for UE1.M1->GPIO100 Add test point T262 for UE1.J6->DCIN3_EN Add test point T147 for UE1.M4->GPIO013	0.1(X00)
47	All	All	2017/04/20	EE	GPIO map change	GPIO013 net name change to DGPU_PWROK UPD1_ALERT#->UPD1_SMBINT# UPD1_SMBUS_ALERT#->UPD1_SMBINT#_R	0.1(X00)
48	11	CPU (6/14)	2017/04/20	EE	Schematic align	INTRUDER# PU change to +RTC_CELL_PCH	0.1(X00)
49	32	EC MEC5105	2017/04/26	EE	GPIO map change	UPD2_ALERT#->UPD2_SMBINT#	0.1(X00)
50	11	CPU (6/14)	2017/05/03	EE	CLKREQ align	Pop RC50 and RC190	0.1(X00)
51	10	CPU (5/14)	2017/05/03	EE	OTG support	RC337 pop and change to 10K ohm	0.1(X00)
52	40	Power control	2017/06/02	EE	EC request to reseve OR gate for WLAN power EN	Add QZ15 and RZ518 Add SLP_WLAN#_GATE net and RE552 to UE1.K10	0.2(X01)
53	24	[Type C]PD Controller TI	2017/06/02	EE	PD ROM main source change	UT6 change to SA000095R10 (GD)	0.2(X01)
54	11	CPU (6/14)	2017/06/02	EE	Schematic align	Reserve RC551 for SUSACK#_R	0.2(X01)
55	34	USH & TPM	2017/06/02	EE	Nuvoton request to change TPM_PIRQ# power rail TPM change to NPCT750	TPM_PIRQ# power rail change to +3.3V_ALW_PCH Change UZ12 to SA0000AQ200 and related resistors and CZ75 change to 10U	0.2(X01)
56	All	All	2017/06/02	ESD	Main source change	DI1,DI4,DT39,DT40,DI6 change to SC300001Y00 DI2,DI3,DI5 change to SCA00000T00 DA2 change to SCA00001A00 DT4 change to SCA00002Q00	0.2(X01)
57	All	All	2017/06/02	EE	DFX request	DA8, DC1, DC2, DE2, DZ1, DZ2, DZ5-DZ8 footprint change to AZ5125-01HPR7G_SOD523-2	0.2(X01)
58	All	All	2017/06/02	EE	Dell request to change cap to L-end P/N	L-end P/N for all cap	0.2(X01)
59	31	CodeC ALC3246	2017/06/12	EE	DFX request	LA13 footprint change to TAI-T_HCB2012KF-121T50_2P	0.2(X01)
60	34	USH & TPM	2017/06/12	RF	RF request	Add CZ76/CZ77 (12pf/68pf) for +3.3V_RUN of UZ12 Add CZ78 (100pf) for +PWR_SRC of JUSH1	0.2(X01)
61	33	EC MEC5105 Support	2017/06/12	EE	Board ID	Change RE79 to 130Kohm (rev. X01)	0.2(X01)
62	9	CPU (4/14)	2017/06/12	RF	ASA for I2C interface	Pop RC549, RC548 and depop RC546, RC547 (14" only)	0.2(X01)
63	9	CPU (4/14)	2017/06/14	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553-RC556 for connector selection	0.2(X01)
64	40	Power control	2017/06/14	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2(X01)
65	23	TUSB546	2017/06/14	EE	PS8743-B1 colay (SA00009E910)	Add RT410, RT411, RT412,RT413, RT414, RT415, RT416,CT213	0.2(X01)
66	24	[Type C]PD Controller TI	2017/06/14	EE	PS8743-B1 colay (SA00009E910)	Add RT405, RT406, RT407, RT417, RT418	0.2(X01)

Version Change List (P. I. R. List)

LA-F322P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
67	31	CodeC ALC3246	2017/06/15	RF	RF request	Reserve CA78 for +5V_RUN_AUDIO	0.2(X01)
68	24	[Type C]PD Controller TI	2017/06/21	EE	PD change to rer.C	UT5 change to SA0000AX700	0.2(X01)
69	6	CPU (1/14)	2017/06/21	EE	AUX voltage level shift	Depop RC448, RC447	0.2(X01)
70	23	TUSB546	2017/06/21	EE	TUSB546 DPEQ set to level 5	Depop RT248, RT140 and pop RT303 and RT306	0.2(X01)
71	24	[Type C]PD Controller TI	2017/08/02	EE	PS8743-B1 colay (SA00009E910)	Change RT405-RT407 to 10K	0.3(X02)
72	26	[Type C]USB3.0 CONN	2017/08/02	EE	Schematic align	CT99-CT102 change to 0.01uf (SE00000YH00)	0.3(X02)
73	23	TUSB546	2017/08/02	EE	TUSB546 new version IC	UT9 change to SA00009R720	0.3(X02)
74	27 32 18	eDP CONN EC MEC5105 CPU (13/14)	2017/08/04	EE	Reserve soft start solution	Reserve RV400, CV635 for QV8 Reserve CZ200, RZ380 for QZ1 Reserve CC340 for QC7 Reserve RE565 for QE15	0.3(X02)
75	31	CodeC ALC3246	2017/08/04	RF	RF request to pop CA54 for 2MHz/4MHz noise	Change CA54 to 82pf and pop	0.3(X02)
76	22	HDMI Conn	2017/08/04	EMI/EE	HDMI EA for NonAR only	Change RV35 to 100ohn Change LV37, LV38 to SHI0000M500 Change LV31-LV36 to SHI00003F0L	0.3(X02)
77	27	eDP CONN	2017/08/04	EE	Touch screen support I2C interface	Depop LV27	0.3(X02)
78	33	EC MEC5105 Support	2017/08/07	EE	Board ID	Change RE79 to 62Kohm (rev. X02)	0.3(X02)
79	9	CPU (4/14)	2017/08/09	EE	TPM_PIRQ# GPIO map change	Add RC560 and reserve RC561 to TPM_PIRQ#	0.3(X02)
80	33	EC MEC5105 Support	2017/09/15	EE	Board ID	Change RE79 to 4.2Kohm (rev. A00)	1.0(A00)
81	12	CPU (7/14)	2017/09/15	EE	ME SW depop	Depop RC222, SW1, RC221 change to 0 ohm short pad	1.0(A00)
82	34	USH & TPM	2017/09/15	EE	TPM change to MP version	UZ12 change to SA0000AQ220	1.0(A00)
83	9	CPU (4/14)	2017/09/15	EE	GPIO map change	Depop RC330, RC331	1.0(A00)
84	8	CPU (3/14)	2017/09/15	EE	Add solder mask	Add UC6 -NPM	1.0(A00)
85	All	All	2017/09/15	EE	0 ohm change to short pad	0 ohm change to short pad	1.0(A00)
86	All	All	2017/09/15	EE	Only support DS3 (0 ohm change to short pad)	Only support DS3 (0 ohm change to short pad)	1.0(A00)
87	23	TUSB546	2017/09/15	EE	TUSB546 DPEQ set to default	Depop RT303, RT306, Pop RT140, RT248	1.0(A00)
88	22 31	HDMI CONN NGFF card	2017/09/18	EE	DFX request	Add LV3,LV6,LV9,LV12 RI27,RI28,RI29,RI30,RI47,RI48,RI49,RI50 -NPM	1.0(A00)

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Title: EE P.I.R (5/6)
Size: Document Number: LA-F322P
Rev: 2.0
Date: Wednesday, December 20, 2017
Sheet 58 of 59

Version Change List (P. I. R. List)

LA-F322P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
89	25	[Type C]PD Power	2017/10/03	EE	X1 Code	DT1,DT2,DT3 Change from SC1N4148180 to SC100005500	1.0(A00)
90	24	[Type C] PD Controller TI	2017/11/10	EE	Main vendor EOL	CT74,CT83 Change from SE00000OU00 to SE00000QL10	1.0(A00)
91	24	[Type C] PD Controller TI	2017/11/10	EE	PD just change part number	UT5 Change from SA0000AX700 to SA0000BIJ00	1.0(A00)
92	17	CPU (12/14)	2017/12/08	EE	WHEA BSOD Intel request	CC202 change to 22uf for 4+2 CPU, but keep 1uf for 2+2 CPU	1.0(A00)
93	17	CPU (12/14)	2017/12/20	EE	WHEA BSOD	Add CC341 22uf 0603,Depop CC202 22uf 0402	2.0(A01)
94	33	MEC5105 support	2017/12/29	EE	Board ID	Change RE79 to 2Kohm (rev. A01)	2.0(A01)