COMPAL CONFIDENTIAL

MODEL NAME :CDM70

PCB NO : LA-E082P

BOM P/N :

BR14 KBL-U DSC

Kabylake U

2016-11-07

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

CXDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DAA000CR000	PCB 1SD LA-E082P REV0 MB DSC 1

Layout Dell logo

REV:X00
PWB: DKJP1

Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-E082P | Rev: 1.0

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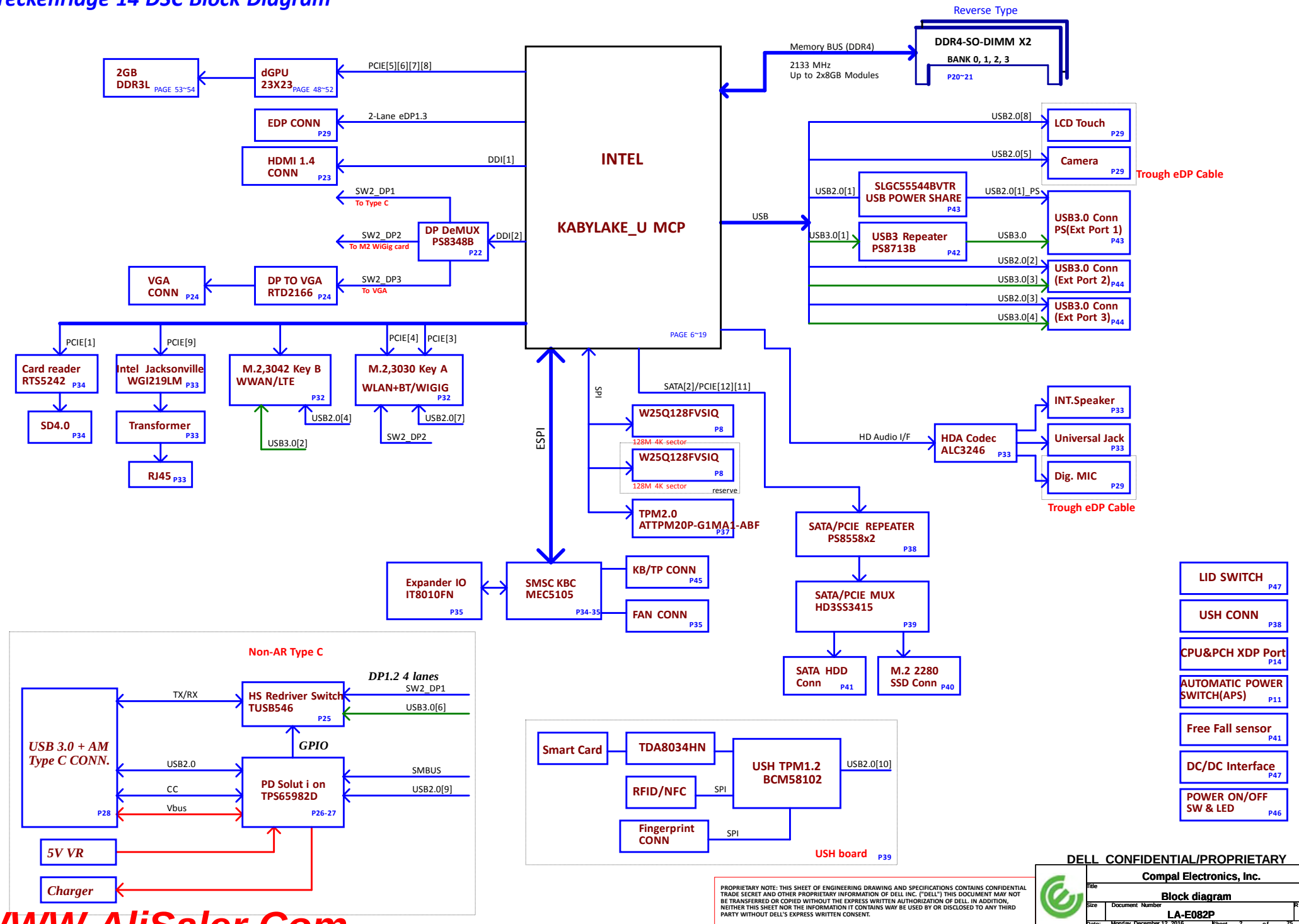
Breckenridge 14 DSC Block Diagram



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Title	Block diagram
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

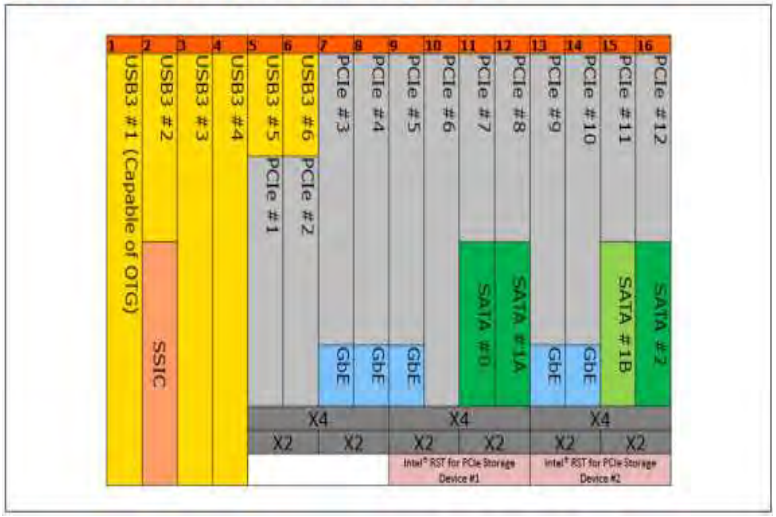
power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.6
		3.8	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
3	IN 1		Copper foil	1oz	1.25
		3.7	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
5	IN 2		Copper foil	1oz	1.25
		3.6	Prepreg	1080H x2 orPP2116HRC	4.2
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
9	GND		Copper foil	1oz	1.25
		3.8	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.6
			Add Plating		
			SolderMask	IT-158	0.5
Overall Thickness (1.2mm ± 10%)					47.68000 1.211072

USB3.0	SSIC	PCIE	SATA	DESTINATION	
USB3.0-1				JUSB1-->Right	
USB3.0-2	SSIC			M.2 3042(LTE)	
USB3.0-3				JUSB2-->Lef t	
USB3.0-4				JUSB3-->Rear Lef t	
USB3.0-5		PCIE-1		Card Reader	
USB3.0-6		PCIE-2		Type-C Port	
		PCIE-3		M.2 3030(WLAN)	
		PCIE-4		M.2 3030(WIGIG)	
		PCIE-5		Discrete Graphics x4	
		PCIE-6			
		PCIE-7	SATA-0		
		PCIE-8	SATA-1		
		PCIE-9		LOM	
		PCIE-10		NA	
		PCIE-11	SATA-1*	NA	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	SATA HDD	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Lef t
3	JUSB3-->Rear Lef t
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	Type-C Port
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



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Title: Port assignment

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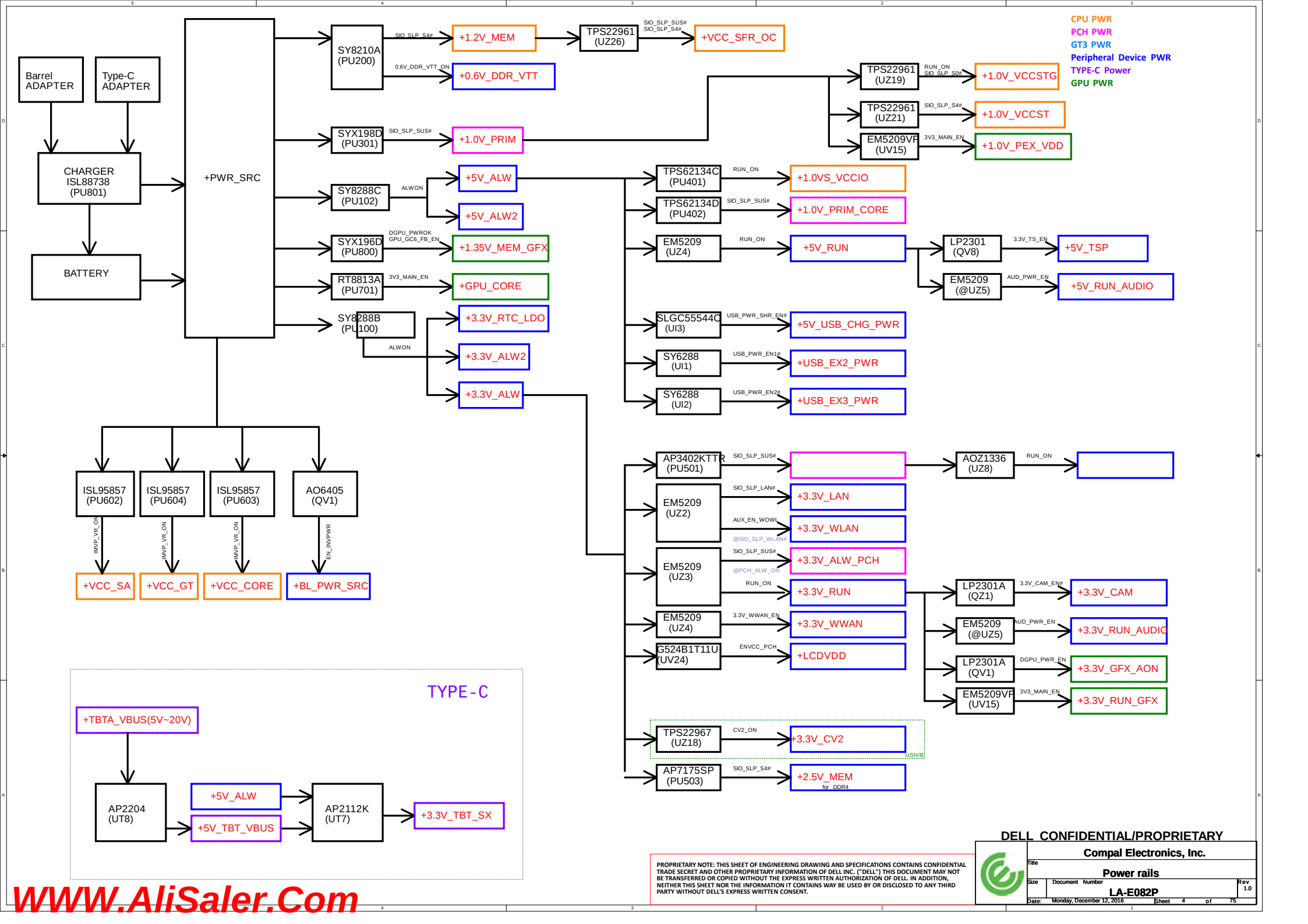

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Title: Power rails

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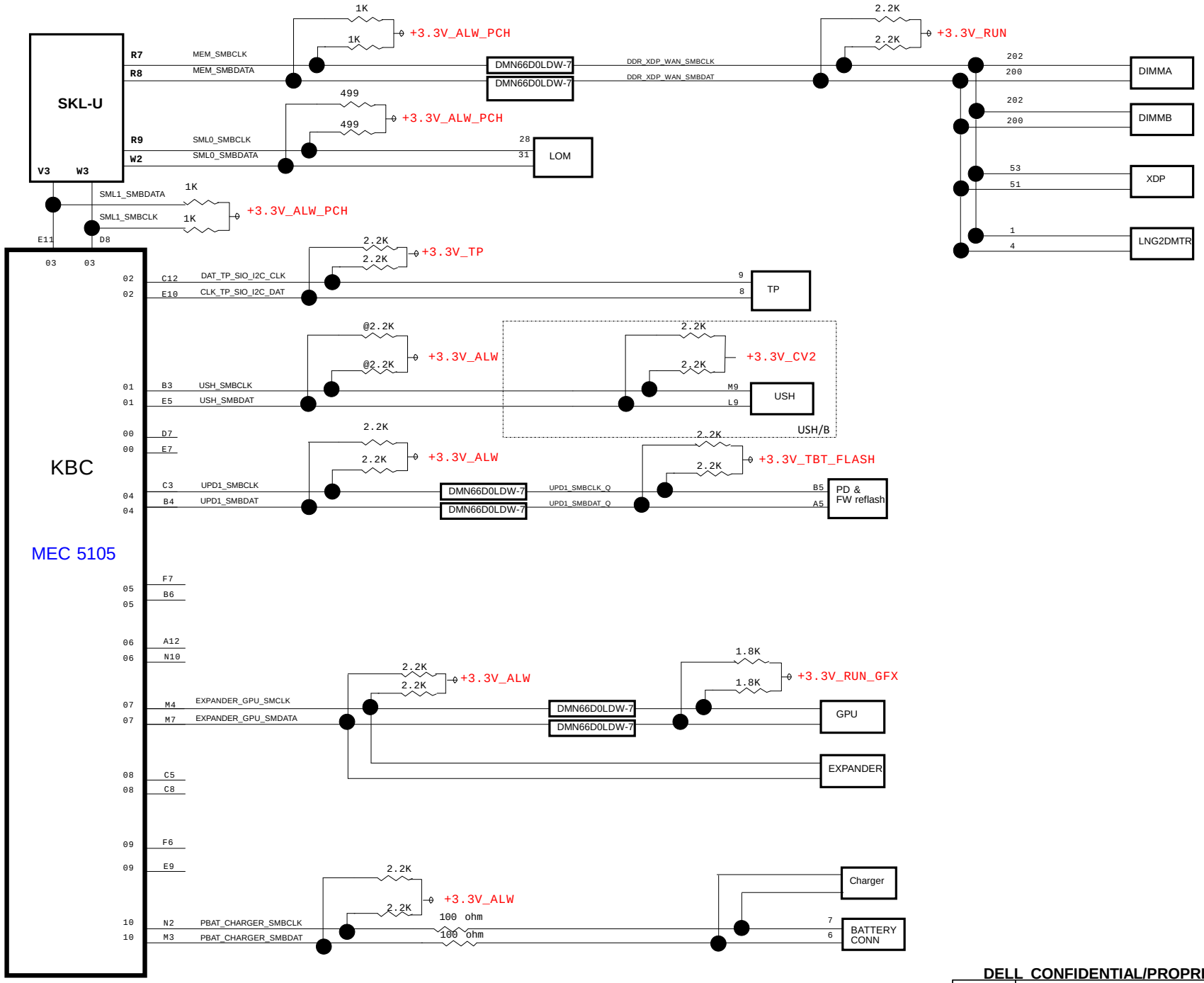

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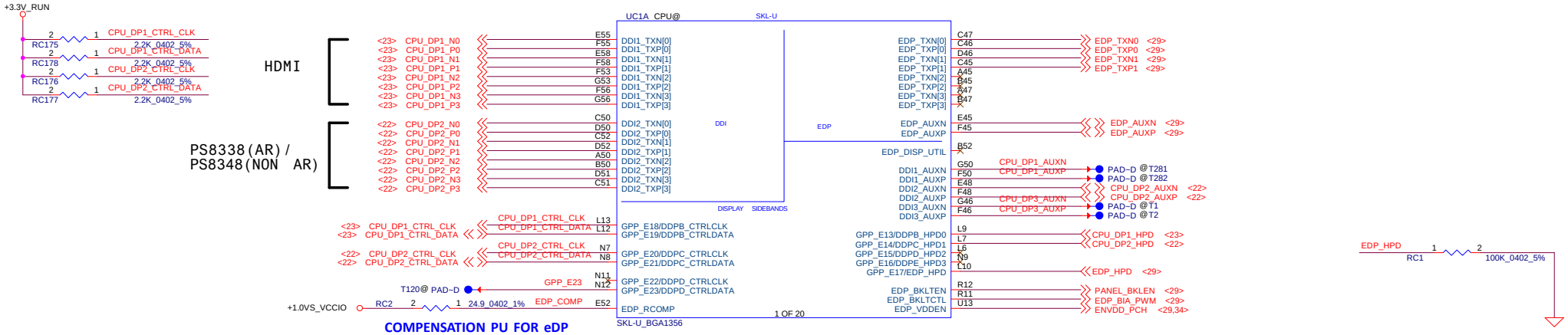
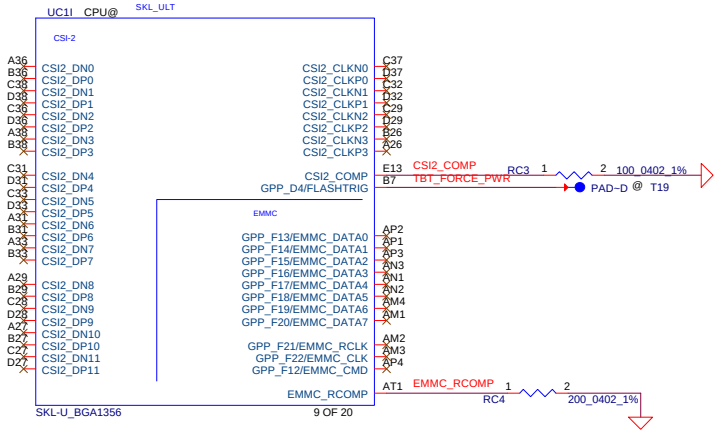
For 2LANE EDP,BR/SB12



COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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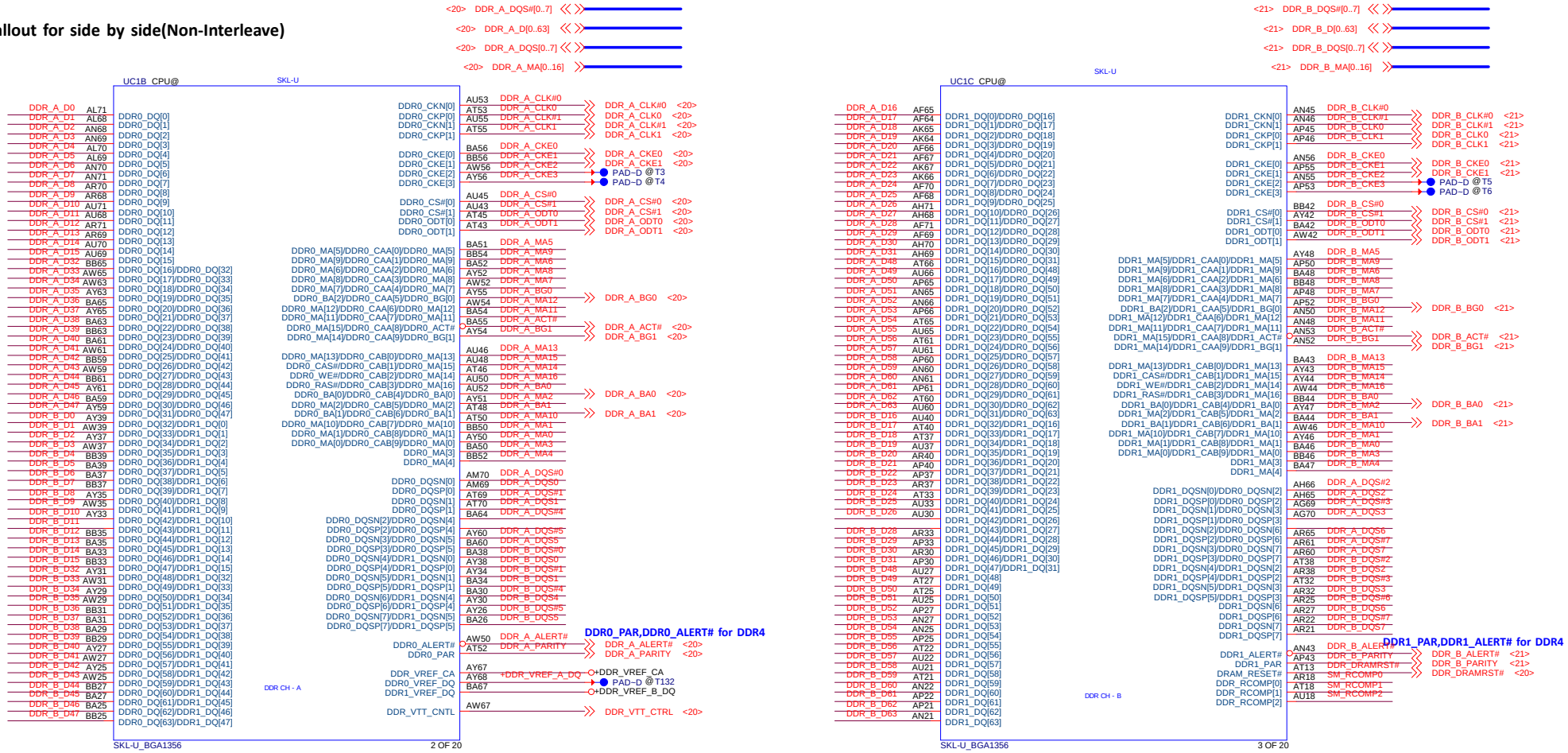
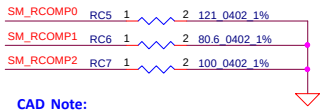
For DDR4

DDR4, Ballout for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Title: CPU (2/14)

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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

UC1E CPU@ SKL-U

SPI - FLASH

SPI - TOUCH

C LINK

SMBUS, SMLINK

LPC

SKL-U_BGA1356

5 OF 20

For BR/SB

SOFTWARE TAA

RF Request

Place close CPU side

128Mb Flash ROM

W25Q128FVSIQ_SO8

JSPI1

E-T_6705K-Y20N-00L

CONN@

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

WEAK INTERNAL 20K PD

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

WEAK INTERNAL 20k PD

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

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Title: CPU (3/14)

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For BR DSC

+3.3V_RUN

HDD_FALL_INT — RC370 10K_0402_5%
3.3V_TS_EN — RC282 100K_0402_5%
SIO_EXT_SCI# — RC237 10K_0402_5%
LPSS_UART2_RXD — @RC402 49.9K_0402_1%
LPSS_UART2_TXD — @RC403 49.9K_0402_1%

+3.3V_ALW_PCH

SIO_EXT_WAKE# — RC283 10K_0402_5%
LPSS_UART2_RXD — RC330 49.9K_0402_1%
LPSS_UART2_TXD — RC331 49.9K_0402_1%

UC1F CPU@ SKL-U

LPSS

<31> MEDIACARD_IRQ# — ONE_DIMM# — AN8 GPP_B15/GSPI0_CS#
<36> TPM_PIRQ# — NRB_BIT — AP7 GPP_B16/GSPI0_CLK; AP8 GPP_B17/GSPI0_MISO; AR7 GPP_B18/GSPI0_MOSI
<41> HDD_FALL_INT — HDD_FALL_INT — AM5 GPP_B19/GSPI1_CS#
<34> SIO_EXT_SCI# — AN7 GPP_B20/GSPI1_CLK
<29> 3.3V_TS_EN — BBS_BIT6 — AP5 GPP_B21/GSPI1_MISO; AN5 GPP_B22/GSPI1_MOSI
Reserve — @RC405 — GPP_C8 — AB1 GPP_C8/UART0_RXD; 100K_0402_5% — AB2 GPP_C9/UART0_TXD
<35> SBBS_TX — W4 GPP_C10/UART0_RTS#; AB3 GPP_C11/UART0_CTS#
LPSS_UART2_RXD — AD1 GPP_C20/UART2_RXD
LPSS_UART2_TXD — AD2 GPP_C21/UART2_TXD; AD3 GPP_C22/UART2_RTS#; AD4 GPP_C23/UART2_CTS#
U7 GPP_C16/I2C0_SDA; U6 GPP_C17/I2C0_SCL
<45> I2C1_SDA_TP — U8 GPP_C18/I2C1_SDA
<45> I2C1_SCK_TP — U9 GPP_C19/I2C1_SCL
AH9 GPP_F4/I2C2_SDA; AH10 GPP_F5/I2C2_SCL
AH11 GPP_F6/I2C3_SDA; AH12 GPP_F7/I2C3_SCL
AF11 GPP_F8/I2C4_SDA; AF12 GPP_F9/I2C4_SCL

ISH

GPP_D9 — P2 — MEM_INTERLEAVED
GPP_D10 — P3
GPP_D11 — P4 — AR_DET# — DGPU_HOLD_RST# <48>
GPP_D12 — P1 — DGPU_PWR_EN <52>
GPP_D5/ISH_I2C0_SDA — M4
GPP_D6/ISH_I2C0_SCL — N3
GPP_D7/ISH_I2C1_SDA — N1
GPP_D8/ISH_I2C1_SCL — N2
GPP_F10/I2C5_SDA/ISH_I2C2_SDA — AD11 — ISH_I2C2_SDA — ISH_I2C2_SDA <32>
GPP_F11/I2C5_SCL/ISH_I2C2_SCL — AD12 — ISH_I2C2_SCL — ISH_I2C2_SCL <32>
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA — U1 — ISH_UART0_RXD <32>
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL — U2 — ISH_UART0_TXD <32>
GPP_D15/ISH_UART0_RTS# — U3 — ISH_UART0_RTS# <32>
GPP_D16/ISH_UART0_CTS#/SML0BALERT# — U4 — ISH_UART0_CTS# <32>
GPP_C12/UART1_RXD/ISH_UART1_RXD — AC1
GPP_C13/UART1_TXD/ISH_UART1_TXD — AC2 — RTD3_CIO_PWR_EN — PAD-D @ T18
GPP_C14/UART1_RTS#/ISH_UART1_RTS# — AC3
GPP_C15/UART1_CTS#/ISH_UART1_CTS# — AB4 — HDD_EN — LCD_CBL_DET# <29>
GPP_A18/ISH_GP0 — AY8 — CLKDET# — PAD-D @T258
GPP_A19/ISH_GP1 — BA8
GPP_A20/ISH_GP2 — BB7
GPP_A21/ISH_GP3 — BA7
GPP_A22/ISH_GP4 — AY7 — TPM_TYPE
GPP_A23/ISH_GP5 — AW7 — LID_CL#_PCH — PAD-D @ T268
GPP_A12/BM_BUSY#/ISH_GP6 — AP13

SKL-U_BGA1356 — 6 OF 20

WWAN
WLAN
9/24: Reserve for embedded location,refer to PDG 0.9
GPP_A GROUP is +1.8V

+1.8V_RUN
ISH_I2C2_SDA — RC363 1K_0402_5%
ISH_I2C2_SCL — RC362 1K_0402_5%

+3.3V_RUN
LCD_CBL_DET# — RC287 100K_0402_5%
DGPU_PWR_EN — RC386 10K_0402_5%

DGPU_PWR_EN — @RC385 10K_0402_5%
Reserved — TPM_TYPE — @RC349 100_0402_1%

+3.3V_RUN
NRB_BIT — @ RC186 4.7K_0402_5%

NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Internal 20k PD

+3.3V_ALW_PCH
BBS_BIT6 — @ RC184 8.2K_0402_5%

BOOT BIOS Destination(Bit 6)	
HIGH	LPC
LOW(DEFAULT)	SPI

Internal 20k PD

+3.3V_RUN
@ RC267 10K_0402_5% — ONE_DIMM# — RC268 10K_0402_5%

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

CONN@ JUART1
LPSS_UART2_TXD — 2
LPSS_UART2_RXD — 3
4
5 GND
6 GND
CVILU_CI1804M1VRA-NH

CI1804M1VRA-NH LINK DONE

+3.3V_ALW_PCH
@ RC371 10K_0402_5%
MEM_INTERLEAVED
10K_0402_5% RC372

DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

+3.3V_ALW_PCH
RC400 10K_0402_5%
AR_DET#
10K_0402_5% @RC401

AR_DET#	
HIGH	NON AR
LOW	AR

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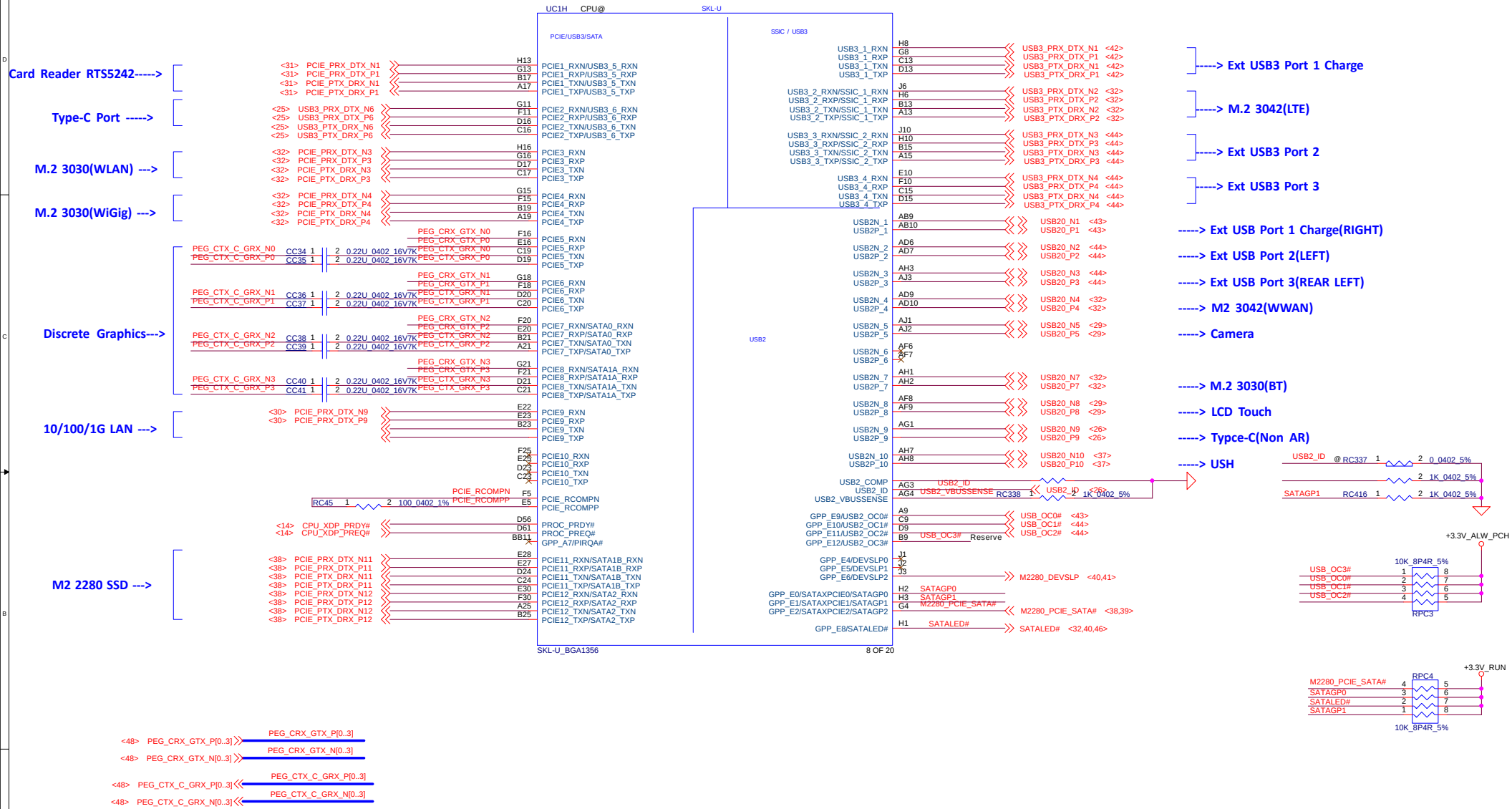
For Non AR,Breckenridge 14/15 DSC



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For BR DSC

GPU--->
WLAN--->
WIGIG--->
M.2 SDD--->
LAN--->
Card Reader --->

UC1J CPU@ SKL_ULT
CLOCK SIGNALS
SKL-U_BGA1356
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XTAL24_IN_R 33_0402_5% 15P_0402_50V8J
YC1 24MHZ_12PF_X3G024000DC1H
XTAL24_OUT_R 33_0402_5% 15P_0402_50V8J
For Skylake,YC1 24 MHz (50 Ohm ESR)
For Cannonlake,YC1 38.4 MHz (30 Ohm ESR)
546765_546765_2014WW48_Skylake_MOW_Rev_1_0

YC2 32.768KHZ_12.5PF_9H03200042 ESR MAX=50k ohm
RC54 10M_0402_5%
PCH_RTCRST# 0_0402_5%
12P_0402_50V8J

SHORT PADS~D @CMOS1
CMOS1 must take care short & touch risk on layout placement

8/21 can change to 10K for merge to RP
PCH_BATLOW# RC72 8.2K_0402_5%
AC_PRESENT RC243 10K_0402_5%

LAN_WAKE# 10K_0402_5%
RC323 10K_0402_5%
PCH_PCIE_WAKE# 1K_0402_5%
VCCST_PWRGD 1K_0402_5%
ME_SUS_PWR_ACK 10K_0402_5%
10/6 depop, prevent singal step.
RC411 10K_0402_5%

PCH_PLTRST# RC62 0_0402_5% PLTRST_LAN# <30>
RC244 0_0402_5% PCH_PLTRST#_EC <35>
RC406 0_0402_5% PLTRST_GPU# <48>
UC7 TC7SH08FU_SSOP5-D
PCH_PLTRST#_AND <31,32,37,40>
RC65 100K_0402_5%

PCH_PLTRST# RC60 0_0402_5% PLTRST_TPM# <36>
PCH_PLTRST#_AND RC325 0_0402_5%

INTRUDER# RC69 1M_0402_5%
MPHYP_PWR_EN RC387 10K_0402_5%
VRALERT# RC73 10K_0402_5%
RC344 10K_0402_5%
SIO_SLP_LAN# RC68 10K_0402_5%
SUSCLK RC48 1K_0402_5%

UC1K CPU@ SKL-U
SYSTEM POWER MANAGEMENT
SKL-U_BGA1356
11 OF 20
connect to VCCMPHYGTAON_1P0 enable pin

T9 PAD~D <14,34,35> VCCST_PWRGD
H_CPUPWRGD RC77 1K_0402_5% H_CPUPWRGD
RC78 60.4_0402_1% VCCST_PWRGD
<14,45> PCH_RSMRST#_AND
H_CPUPWRGD VCCST_PWRGD
ESD@ CC300 100P_0402_25V8J
ESD@ CC301 100P_0402_25V8J
ESD Request:place near CPU side

<14,34> SYS_PWROK
<63> PCH_PWROK
<35> PCH_DPWROK
<34> ME_SUS_PWR_ACK
<34> SUSACK#
<34,35> PCH_PCIE_WAKE#
<30,34> LAN_WAKE#
<30> PM_LANPHY_ENABLE
<29> 3.V_CAM_EN#
RC311 10K_0402_5%

SIO_SLP_S0# <17,36,61>
SIO_SLP_S3# <34,35>
SIO_SLP_S4# <17,34,59,62>
SIO_SLP_S5# <34>
SIO_SLP_SUS# <17,34,47,60,61,62>
SIO_SLP_LAN# <34,47>
SIO_SLP_WLAN# <34,47>
SIO_SLP_A# <34>
SIO_PWRBTN# <14,34>
AC_PRESENT <34>
PCH_BATLOW#
PME#
PAD~D @T115
INTRUDER#
MPHYP_PWR_EN
VRALERT#

JAPS1
CONN@ ACES_50506-01841-P01
<35,46> POWER_SW#_MB
SYS_RESET#
SIO_SLP_S0#

SYS_RESET# @ESD@ CC282 0.01U_0402_25V6
ESD Request:place near CPU side

RC215
POP NO Support Deep sleep
DE-POP Support Deep sleep
PCH_DPWROK RC215 0_0402_5% PCH_RSMRST#_AND
CC286 0.01UF_0402_25V7K
RC220 100K_0402_1%
RC75 10K_0402_5%

<14> XDP_DBRESET# XDP_DBRESET#
RC290 0_0402_5%
RC291 10K_0402_5%
RC225 8.2K_0402_5%
RC227 8.2K_0402_5%
ME_RESET#
UC12 74AHC1G09GW_TSSOP5
SYS_RESET#_R RC224 1K_0402_5%
SYS_RESET#

if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)

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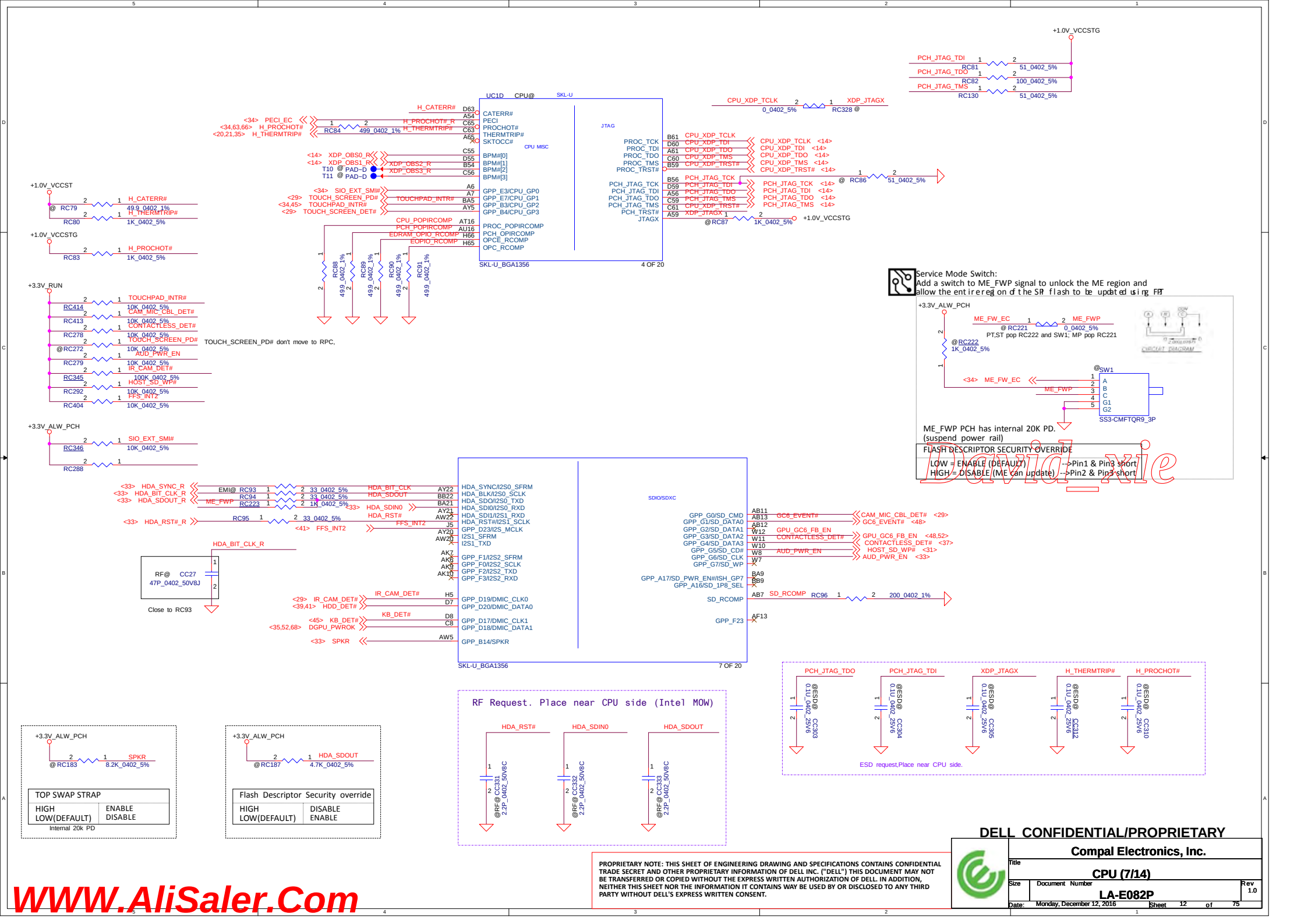

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Title: CPU (7/14)		
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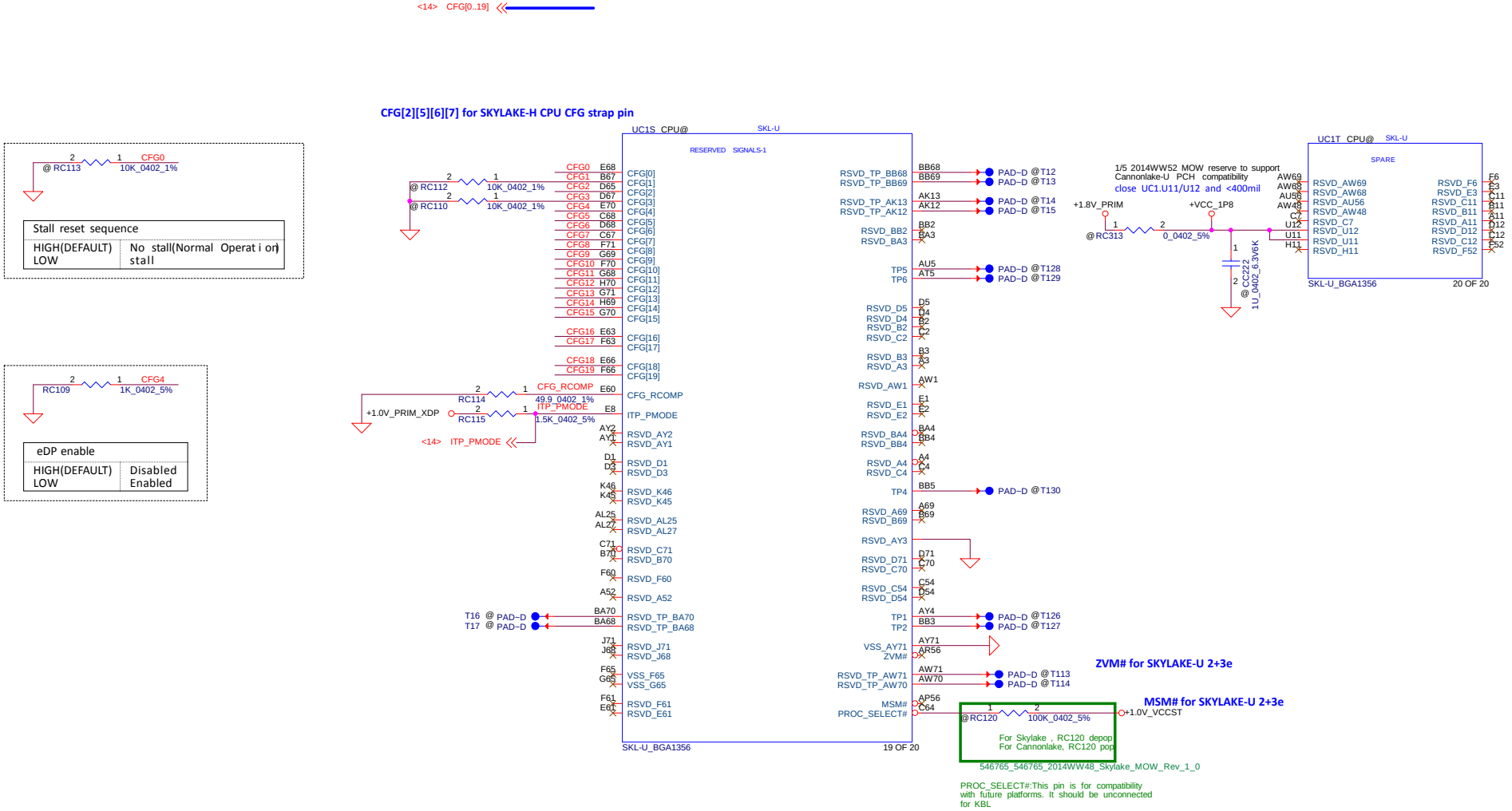
Date: Monday, December 12, 2016	Sheet 12 of 75	



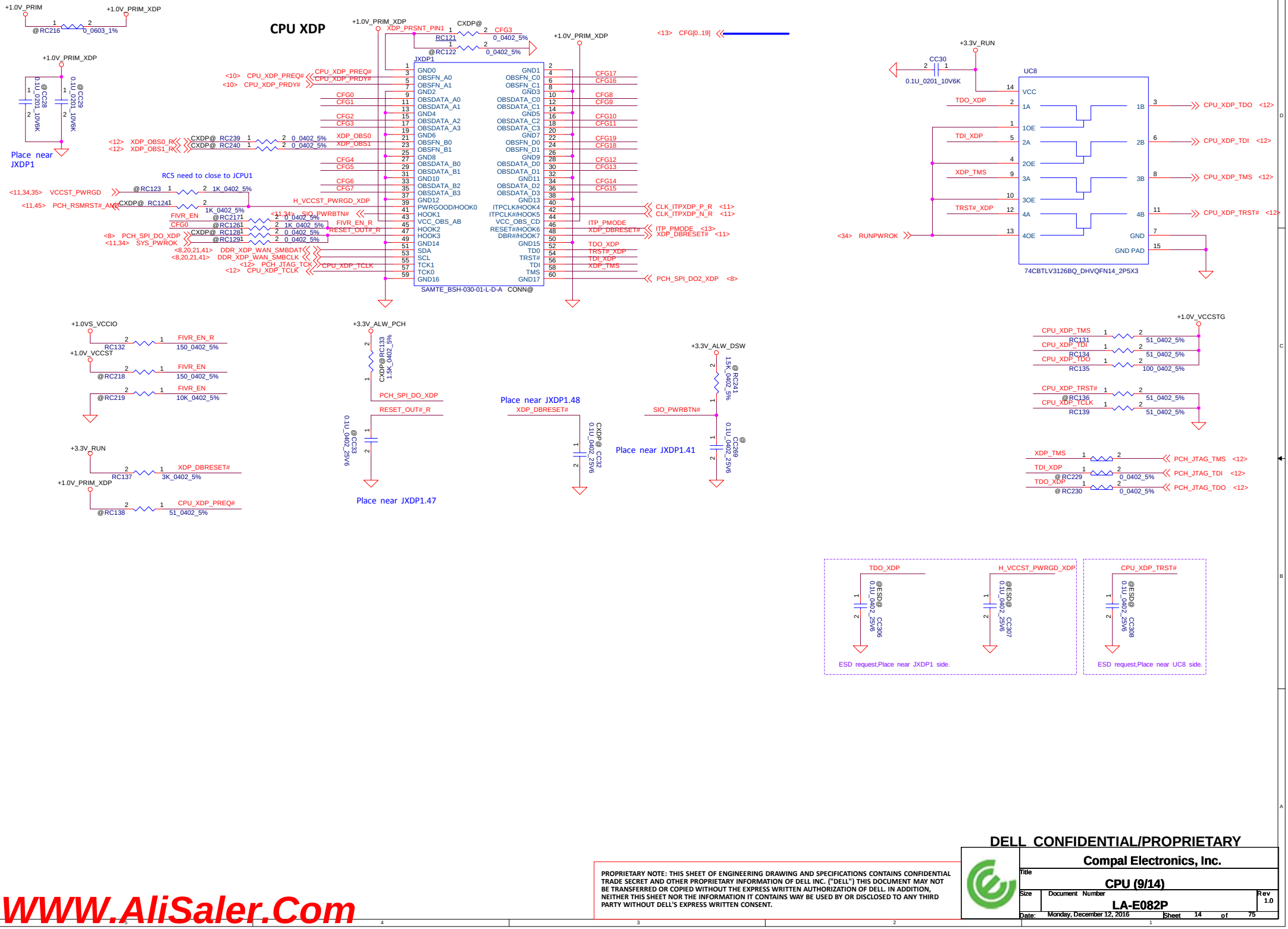
Compal Electronics, Inc.

Title: CPU (8/14)

Size | Document Number: LA-E082P | Rev: 1.0

Date: Monday, December 12, 2016 | Sheet 13 of 75

CPU XDP



Compal Electronics, Inc.

Title: CPU (9/14)

Size | Document Number: LA-E082P | Rev: 1.0

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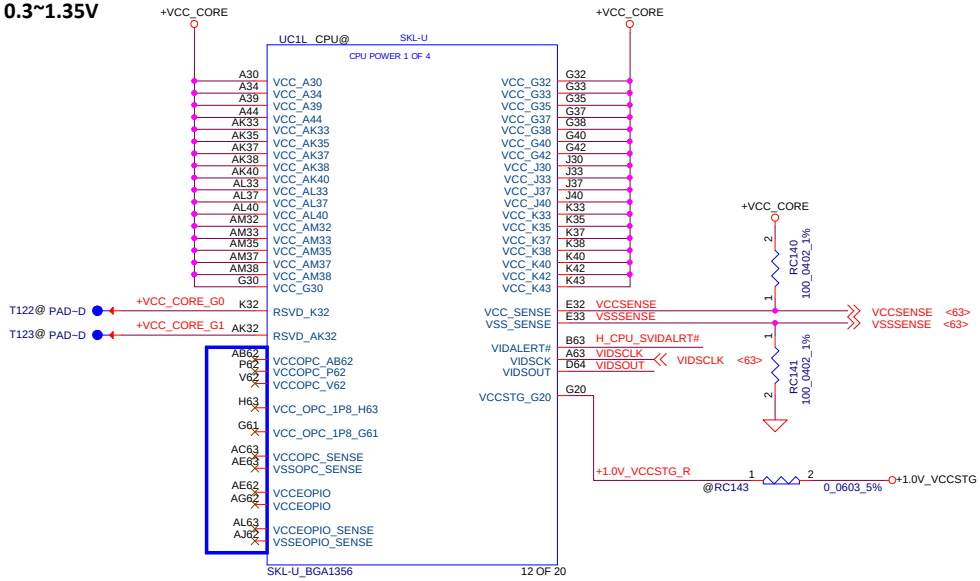
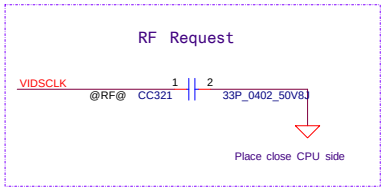
+VCC_CORE: 0.3~1.35V

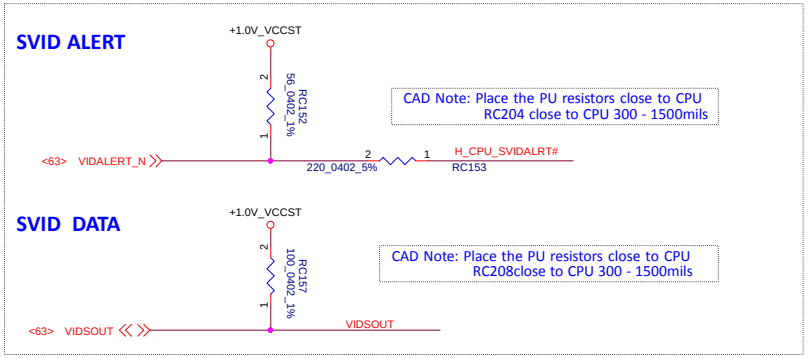


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)





Compal Electronics, Inc.

Title: CPU (10/14)

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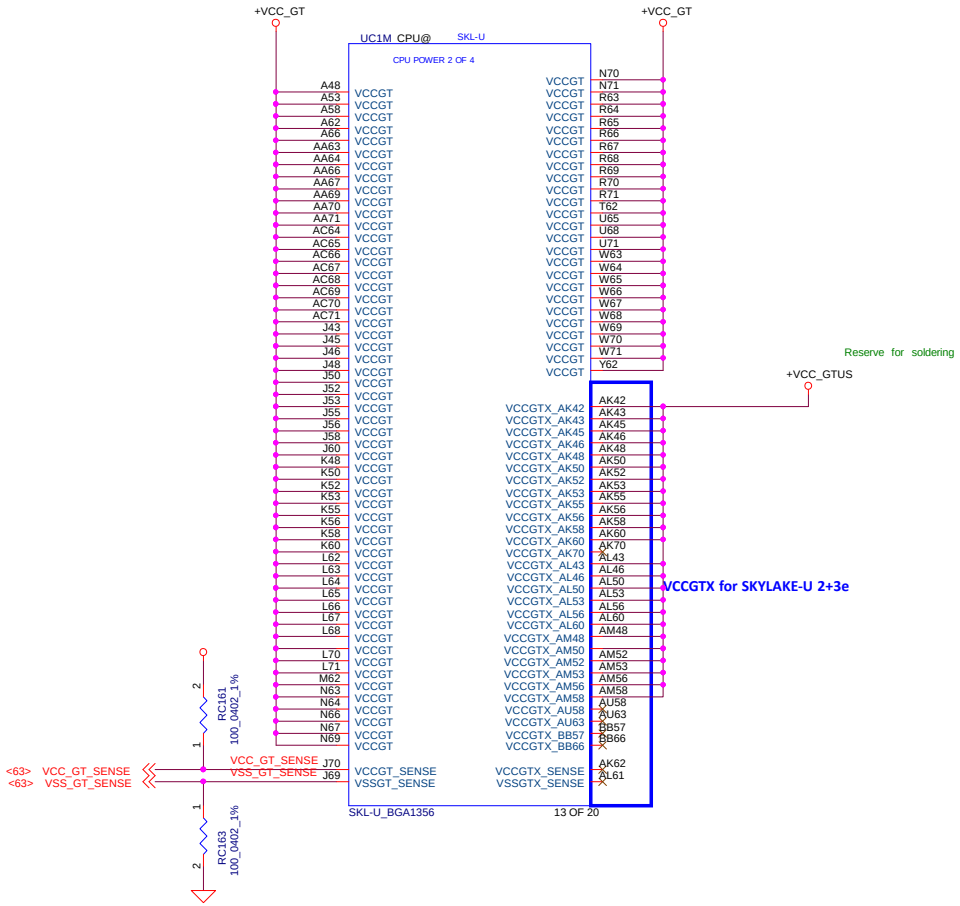
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

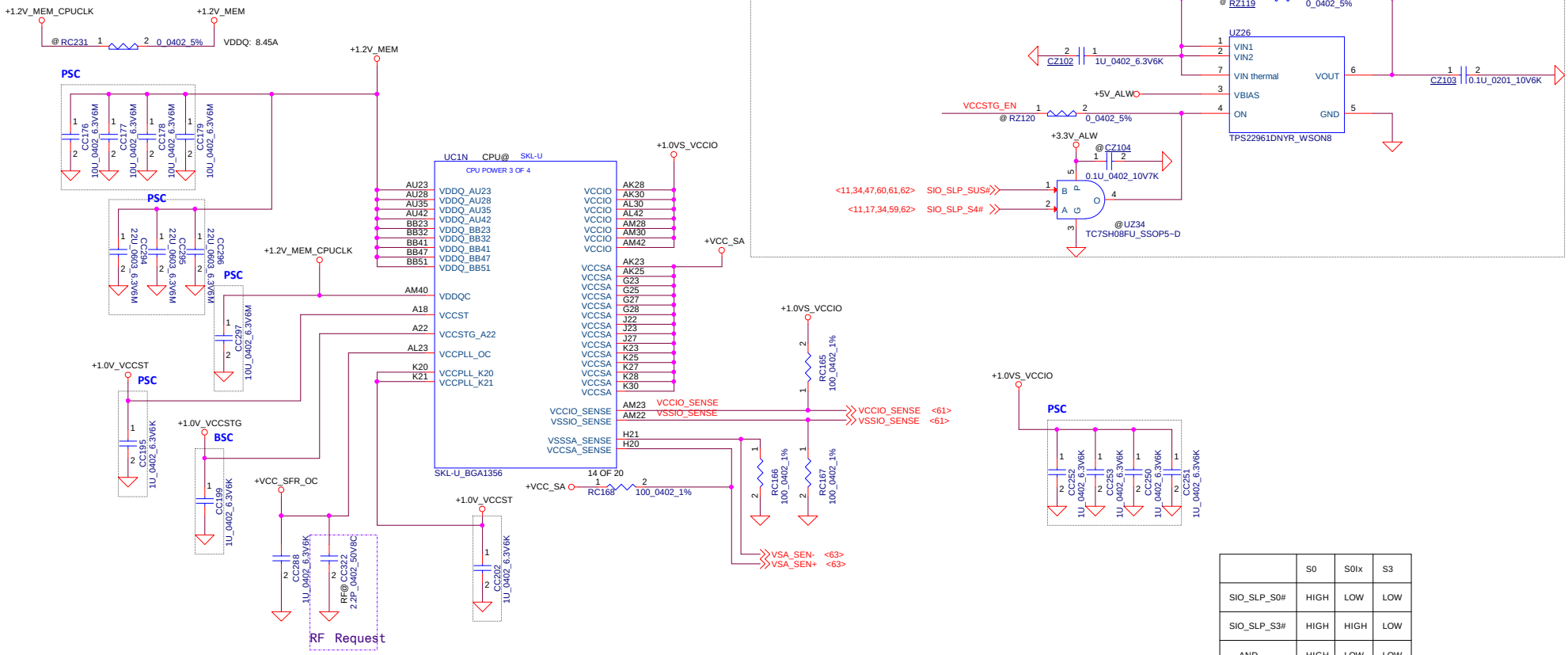


Compal Electronics, Inc.

Title: CPU (11/14)

Size | Document Number: LA-E082P | Rev: 1.0

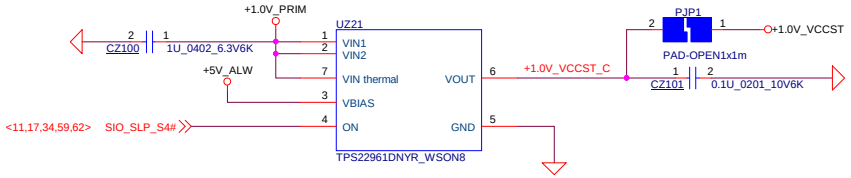
Date: Monday, December 12, 2016 | Sheet 16 of 75



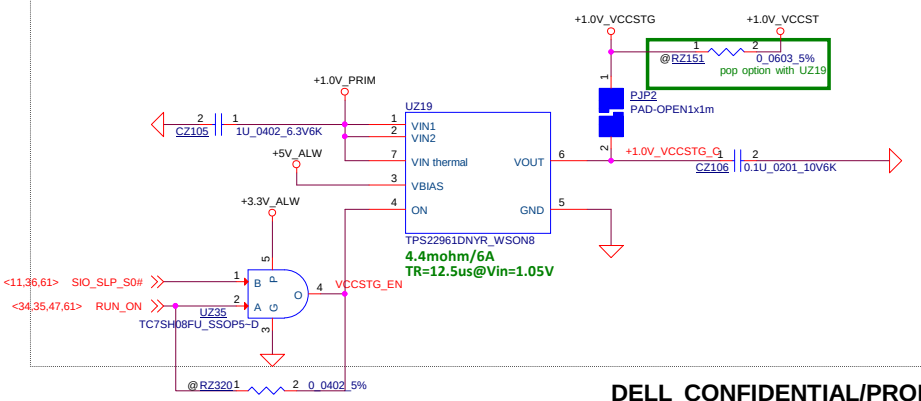
+VCCPLL_OC source

	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

+1.0V_VCCST source



+1.0V_VCCSTG source



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Title: CPU (12/14)

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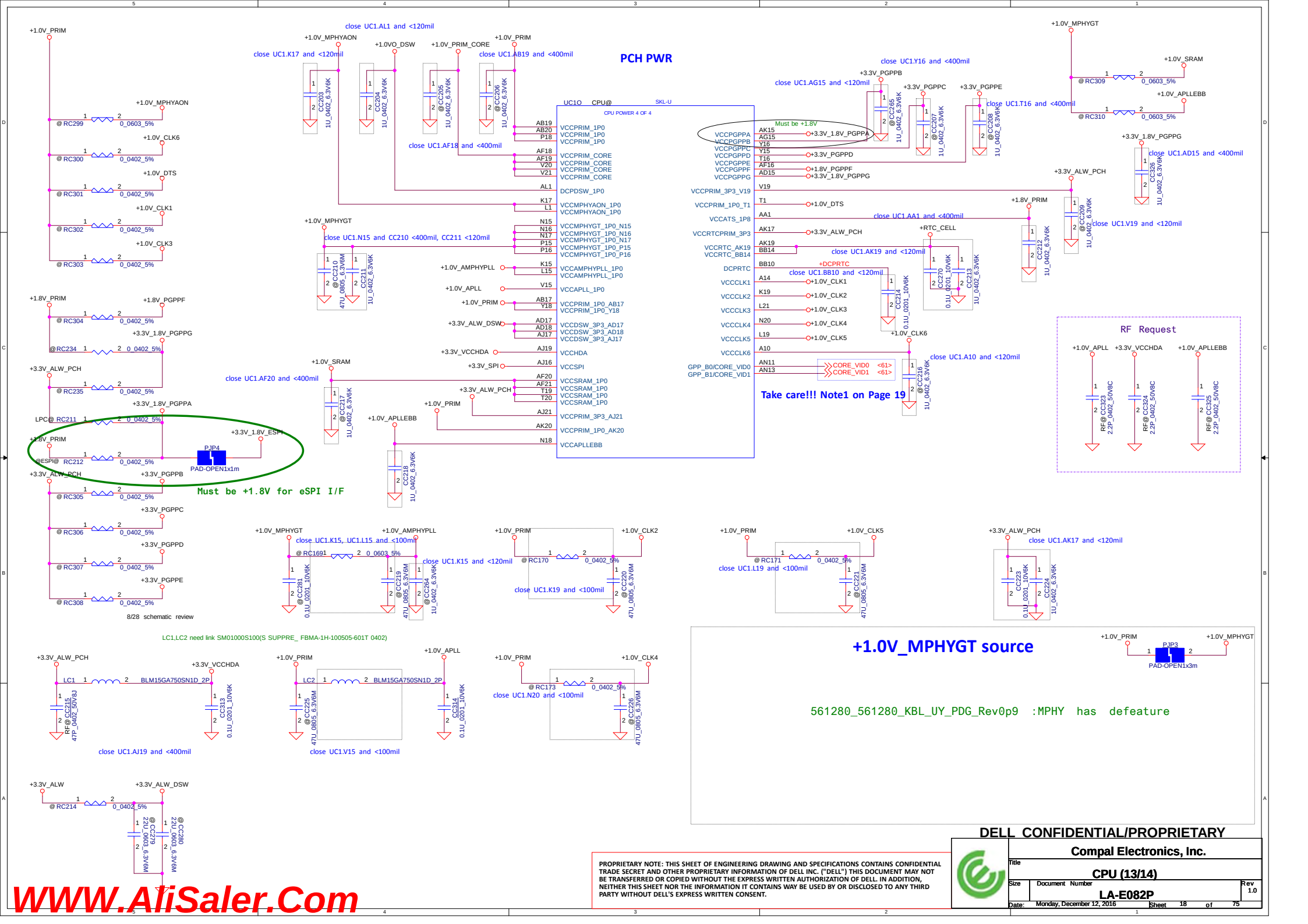
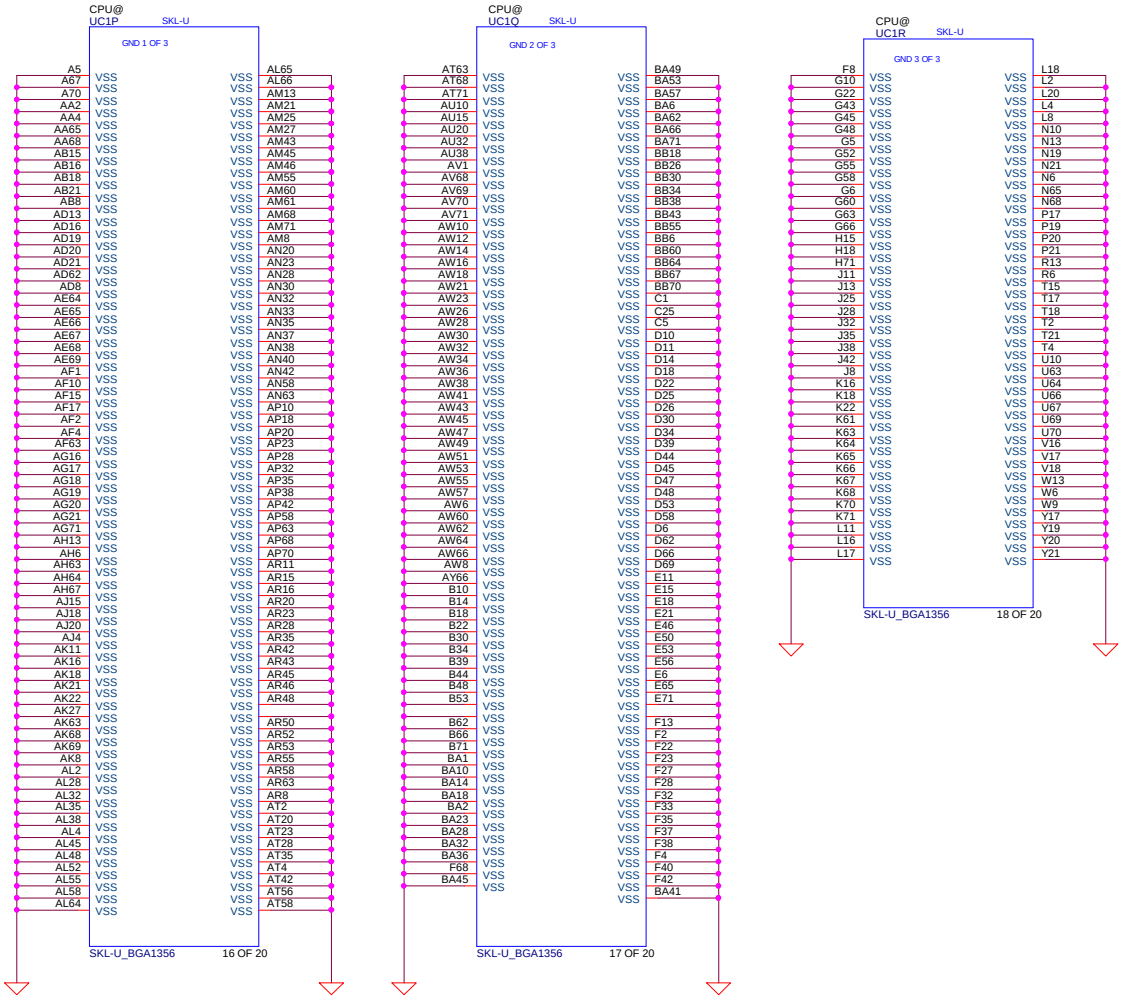
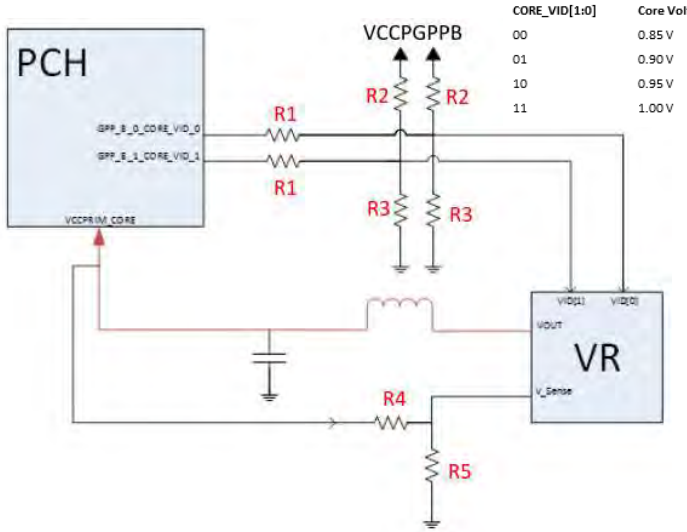




Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

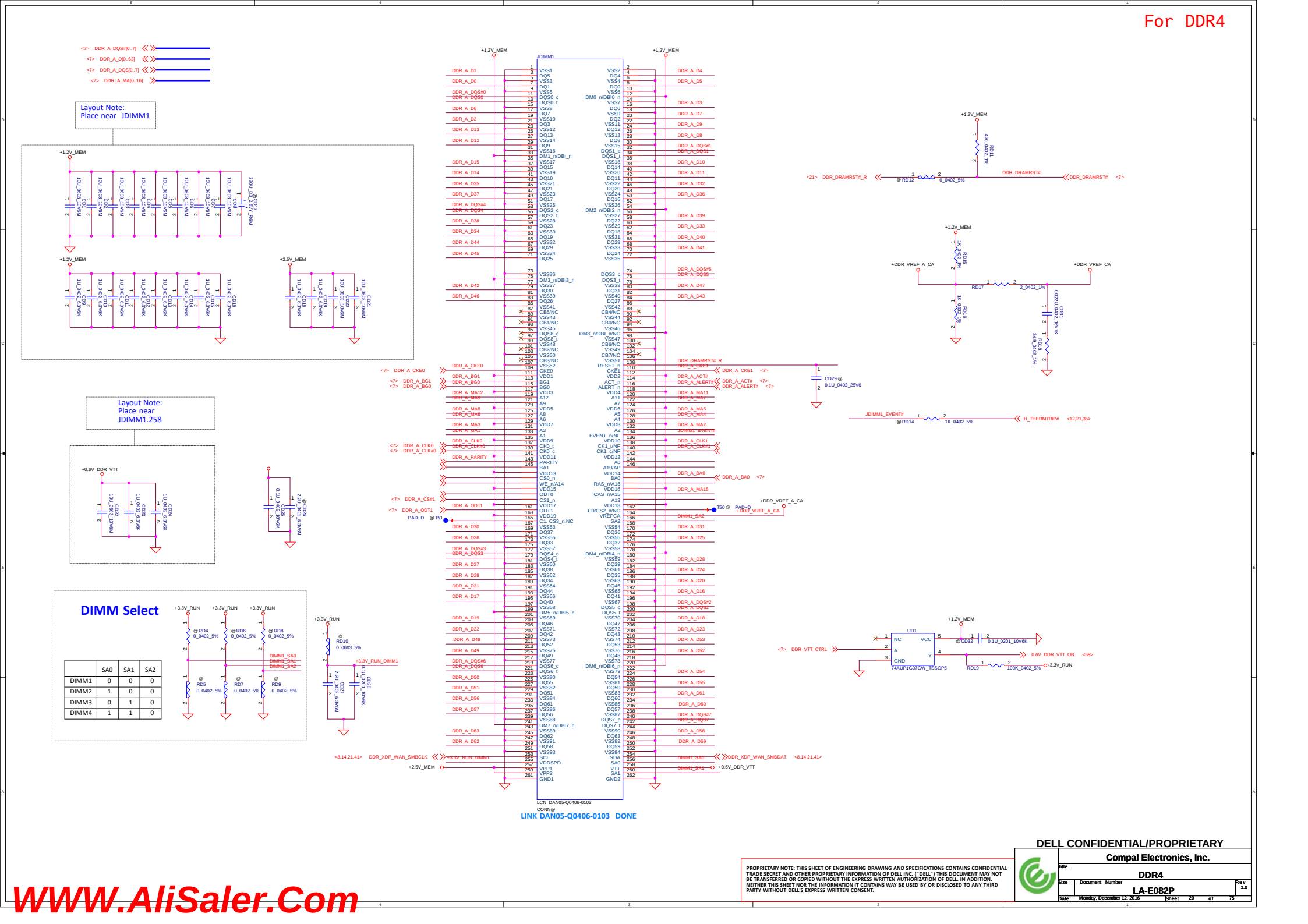
- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

For DDR4



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Title: DDR4

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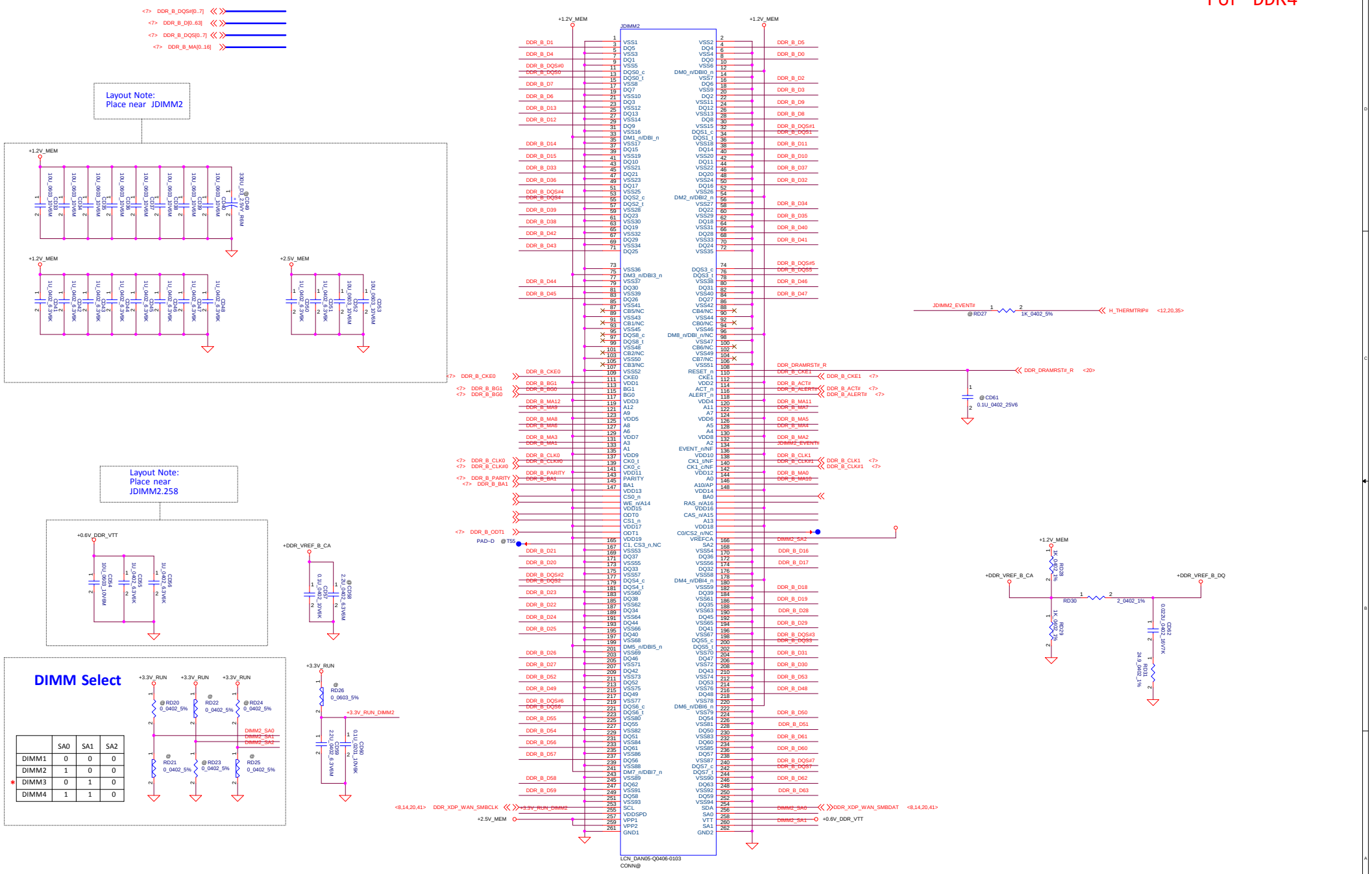
For DDR4



	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0

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Title: DDR4

Size: Document Number: LA-E082P

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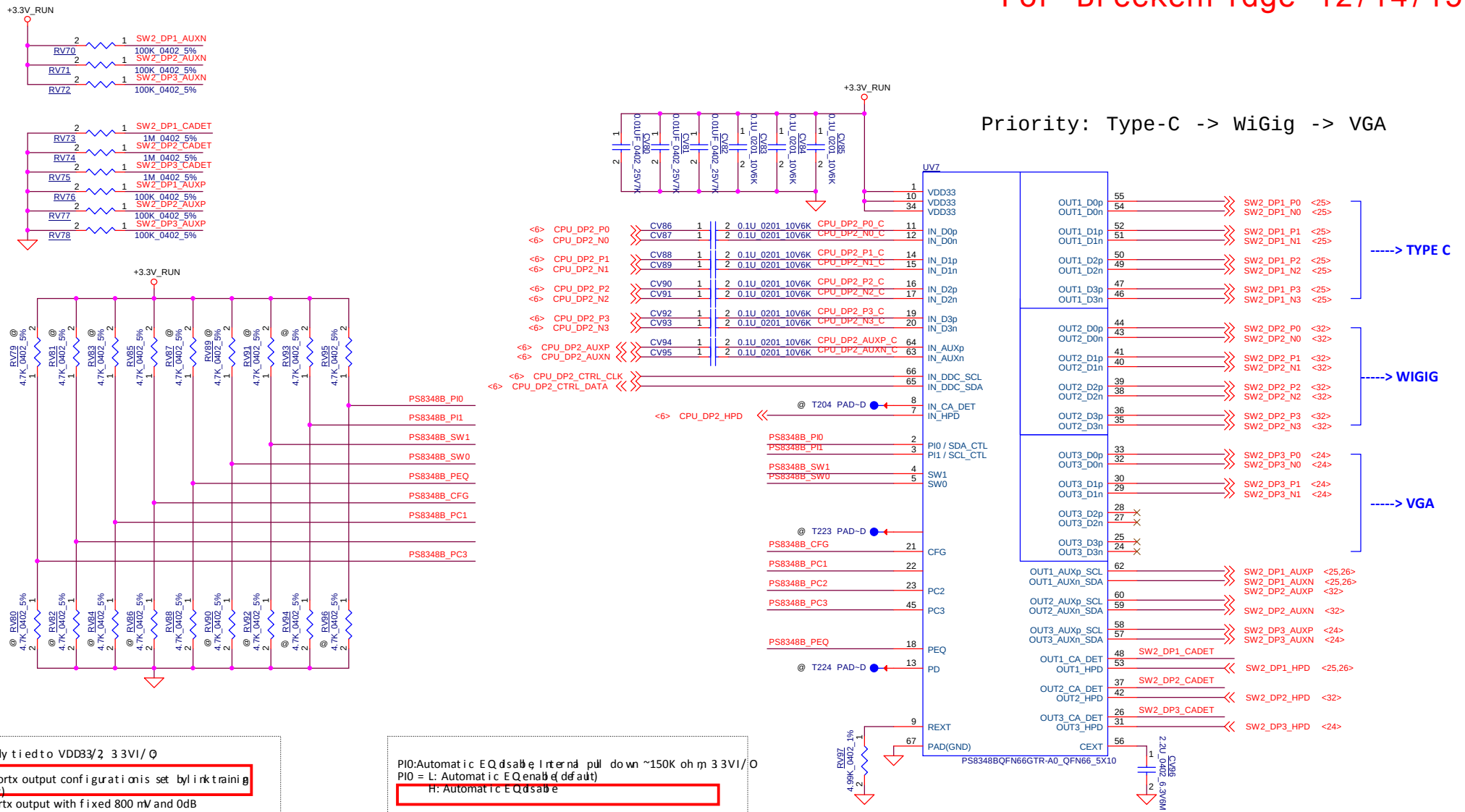
For Breckenridge 12/14/15



Priority: Type-C -> WiGig -> VGA

Internally tied to VDD33/2, 3.3V I/O
PCx =
M:Portx output configuration is set by link training (default)
H:Portx output with fixed 800 mV and 0dB
L:Portx output with fixed 400 mV and 0dB
x=1, 2, 3

PI0:Automatic EQ disable, Internal pull down ~150K ohm 3.3V I/O
PI0 = L: Automatic EQ enable (default)
H: Automatic EQ disable

Internally pull down ~150K.3.3V I/O
For Control Switching Mode (CFG = L):
[SW1,SW0]= [L,L], Port1 is selected (default)
[SW1,SW0]= [L,H], Port2 is selected
[SW1,SW0]= [H,L], Port3 is selected
[SW1,SW0]= [H,H], Port3 is selected
For Automatic Switching Mode (CFG0= H):
[SW1,SW0]= [L,L], Port1 >Port2 >Port3 (default)
[SW1,SW0]= [L,H], Port1 >Port3 >Port2
[SW1,SW0]= [H,L], Port3 >Port2 >Port1
[SW1,SW0]= [H,H], Port3 >Port1 >Port2
[SW1,SW0]= [L,M], Port2 >Port1 >Port3
[SW1,SW0]= [M,M], Port2 >Port3 >Port1

Internally tied to VDD33/2, 3.3V I/O
PEQ =
M:default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H:HEQ, compensate channel loss up to 14.5dB @ HBR2
L:LLEQ, compensate channel loss up to 8.5dB @ HBR2

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Title: DP SW2 PS8348B

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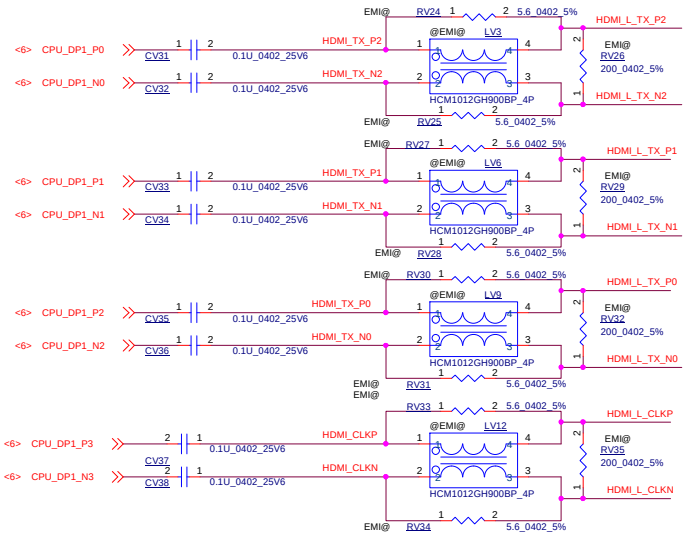
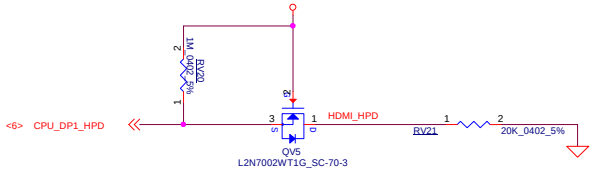
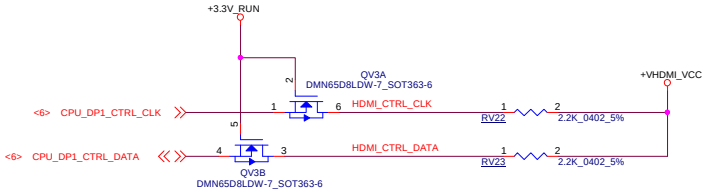
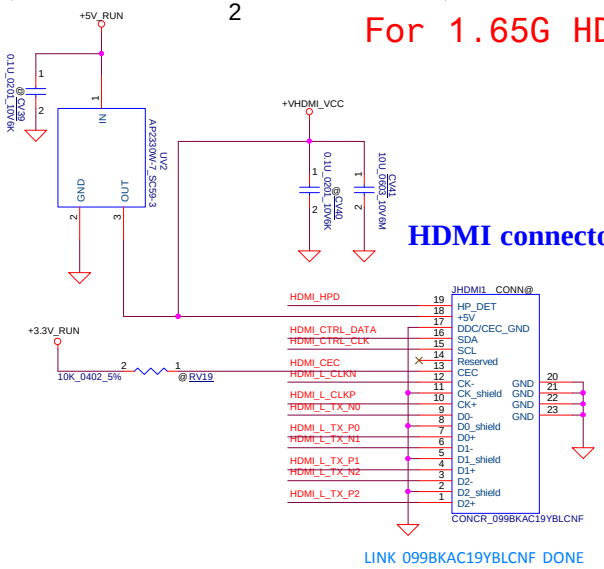
For 1.65G HDMI from CPU

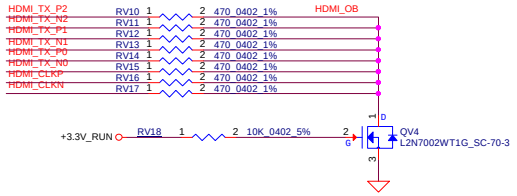








LINK 099BKAC19YBLCNF DONE



Compal Electronics, Inc.

Title: HDMI CONN

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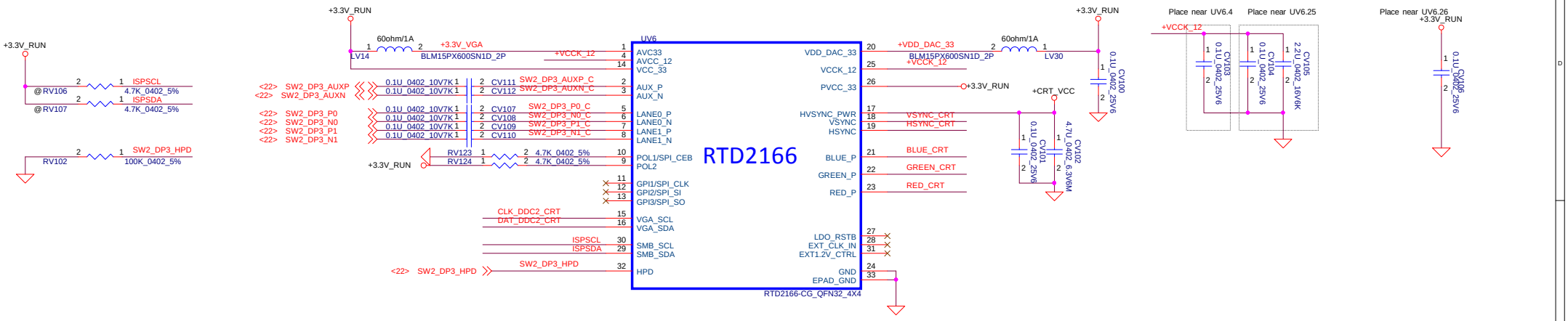
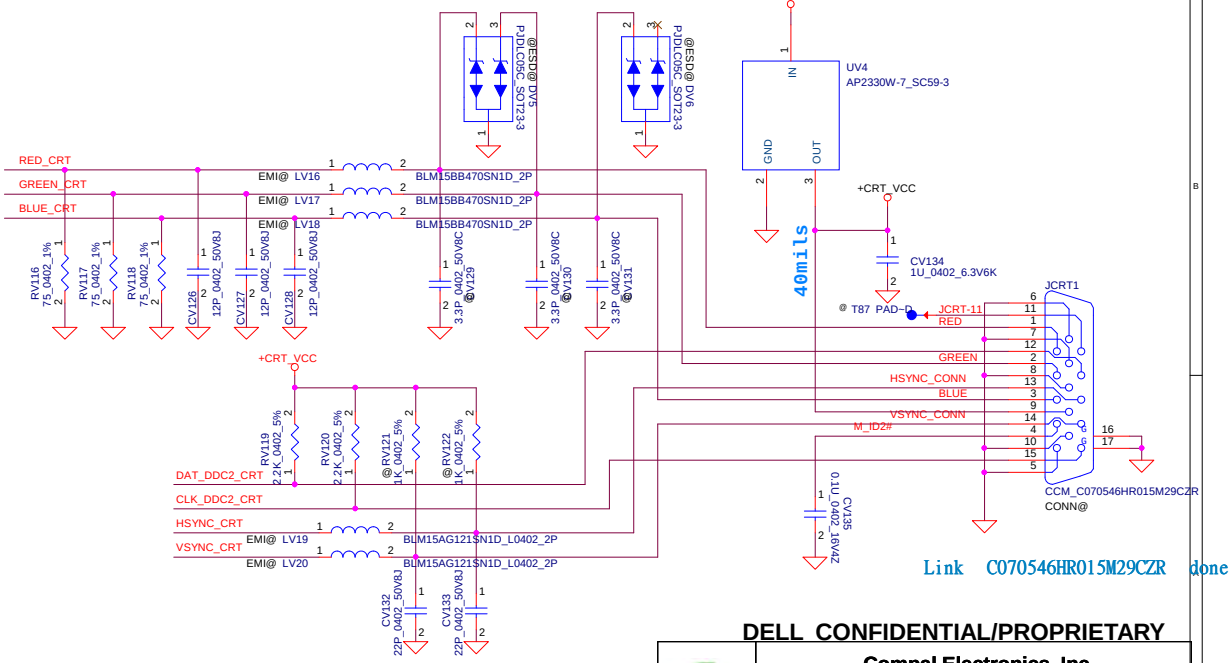
For Breckenridge 12/14/15
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



Link C070546HR015M29CZR done

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Title: DP to VGA & VGA Conn

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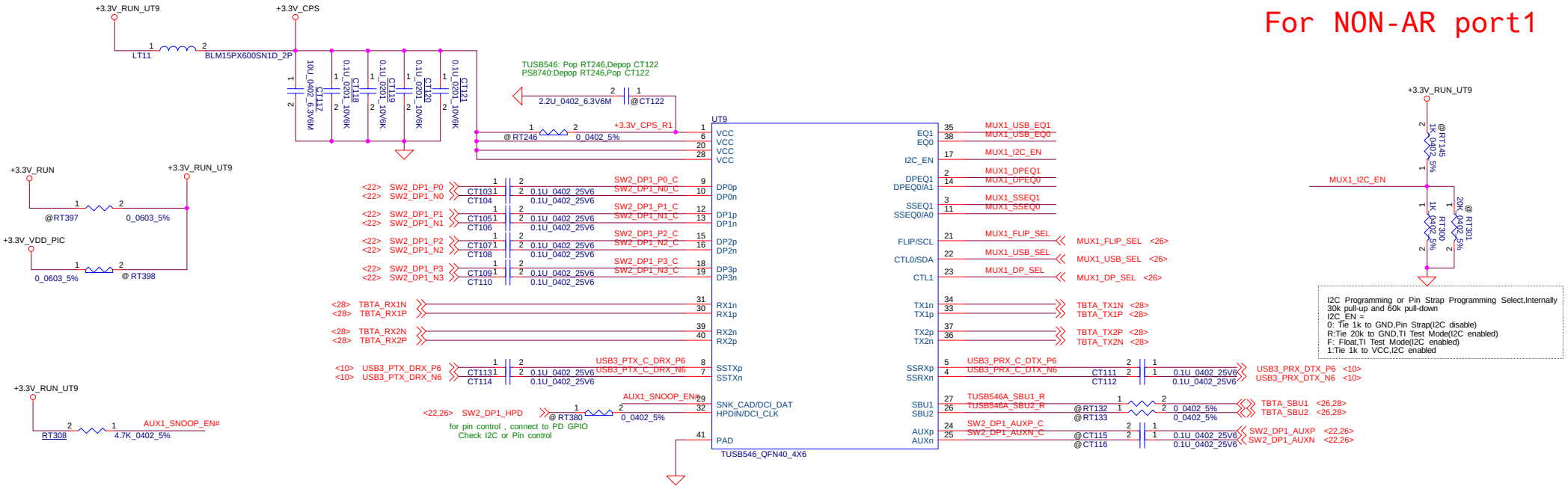
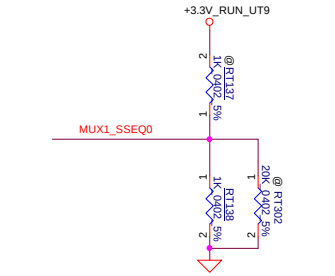
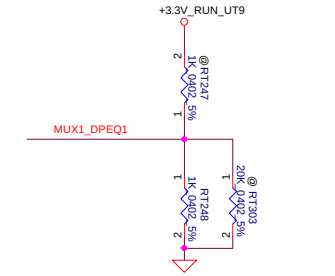
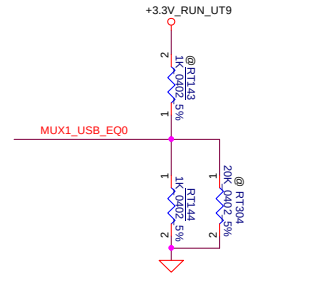
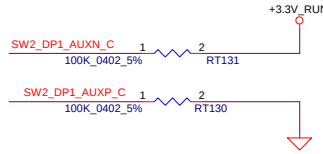
For NON-AR port1

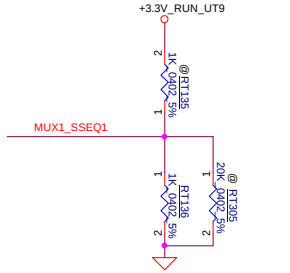


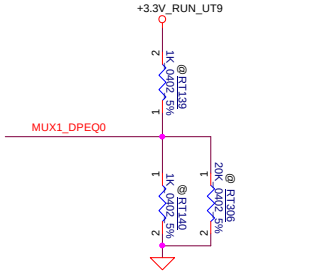












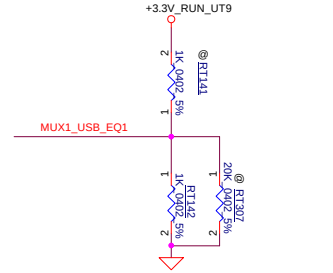


Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Compal Electronics, Inc.

Title: DP/USB3 Repeater SW TUSB546

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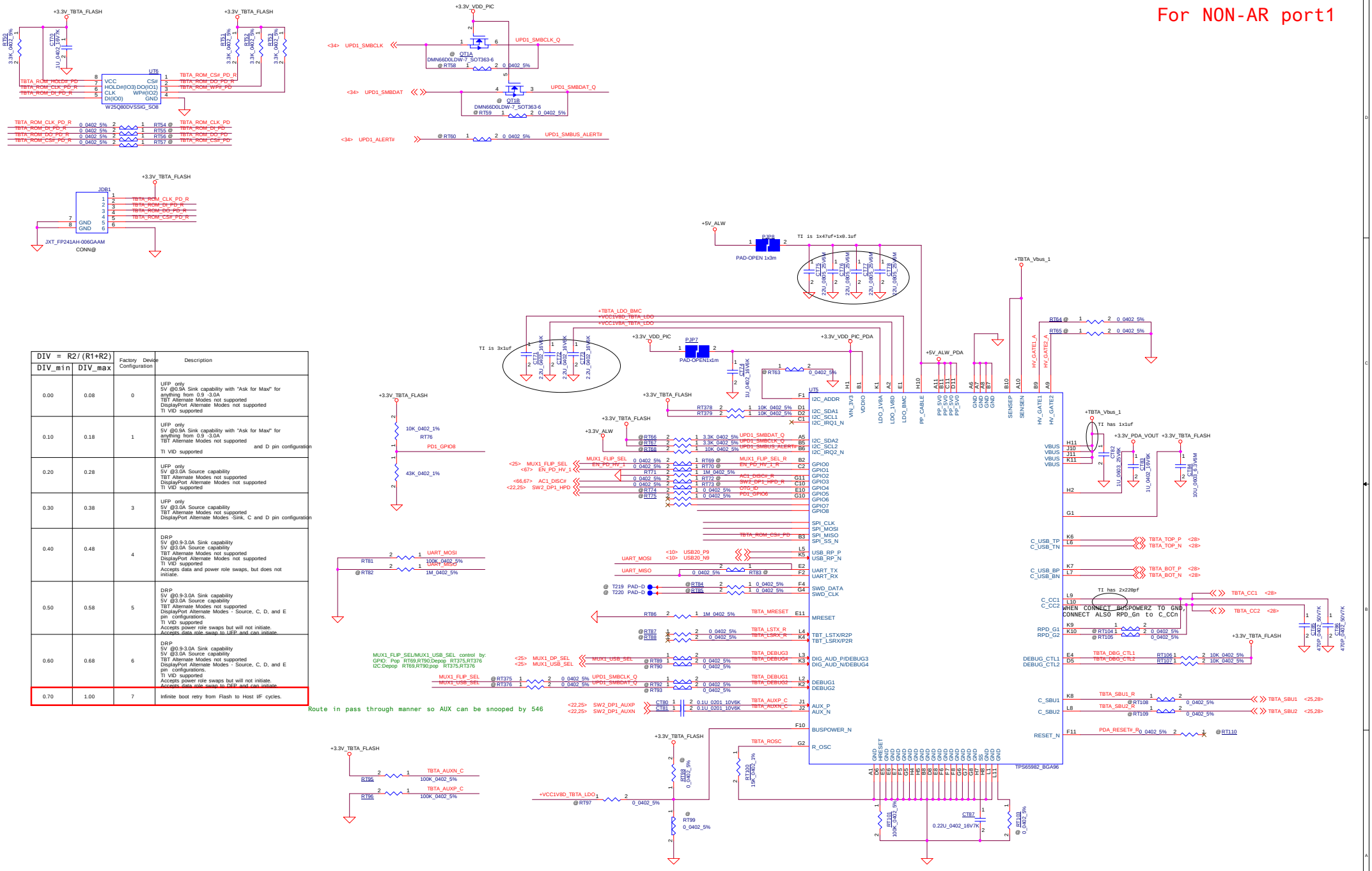
For NON-AR port1



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported and D pin configuration TI VID supported
0.20	0.28		UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

Compal Electronics, Inc.

Title: [Type C]PD Controller TI

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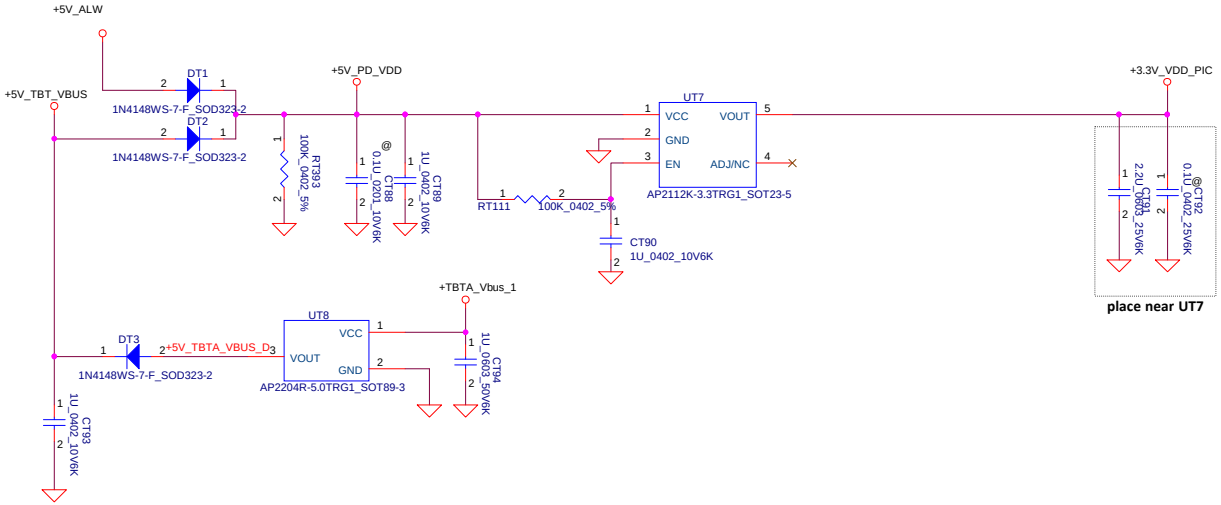

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Title: [Type C]PD Power

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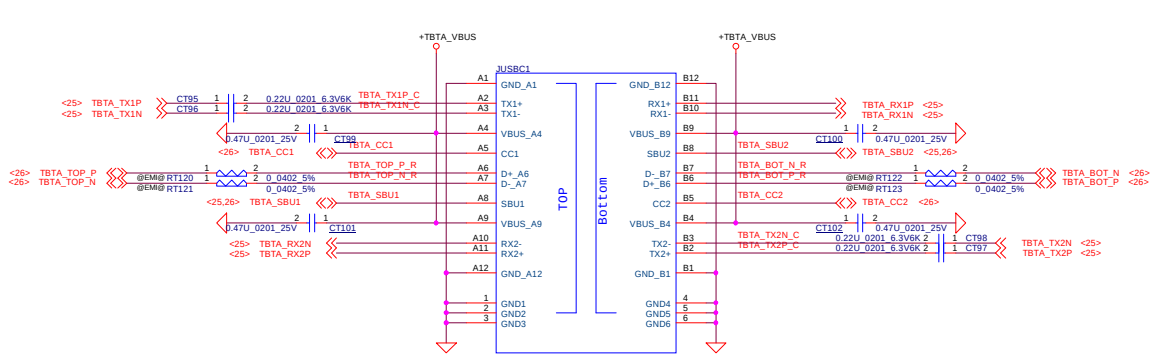
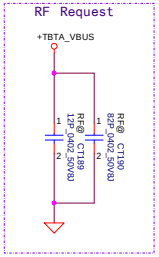
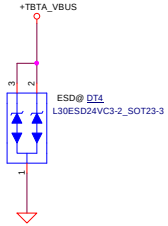
For NON AR Config

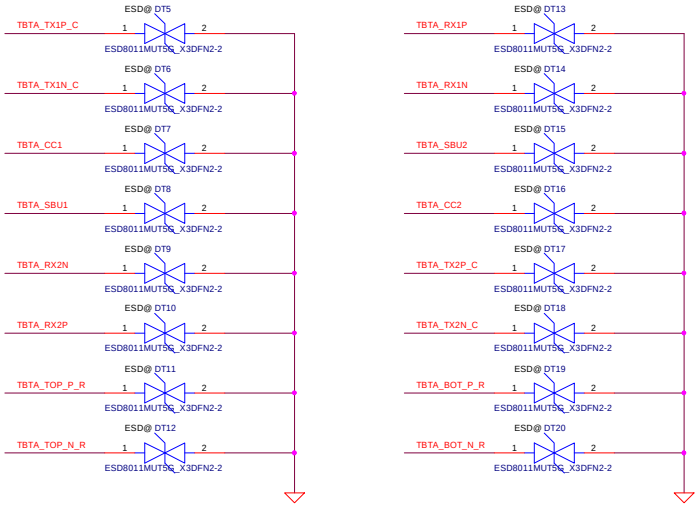


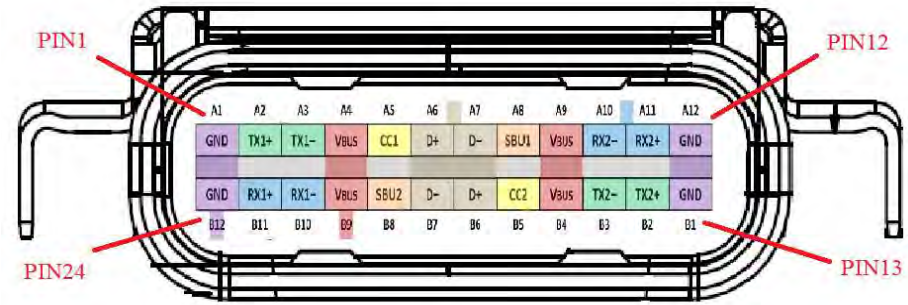




DX07BD24JJ2 LINK DONE

Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B





Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-E082P | Rev: 1.0

Date: Monday, December 12, 2016 | Sheet 28 of 75

For 2LANE EDP &5V_TSP

For Breckenridge 14/15

LINK 50398-04041-001 DONE

JEDP1

ACES_50398-04041-001
CONN@

TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events

EXC24CQ900U_4P
LV27 EMI@

ESD depop locat i on

EMI Request

RF Request

If touch panel, GPIO Low-> Touch Mic. EQ ; others the GPIO is High -> Non-Touch Mic. EQ

JIR1
ACES_50208-0060N-P01
CONN@

Link ACES_50208-0060N-P01 done

RF Request

DV1

DV2

RF Request

WebCAM

EXC24CQ900U_4P
LZ1 EMI@

Backlight POWER

QV1 AO6405_TSOP6

QV2 L2N7002WT1G_SC-70-3

LCDVDD POWER

PJP12 PAD-OPEN1x1m

UV24 G524B1T11U_SOT23-5

DV3 BAT54CW_SOT323-3

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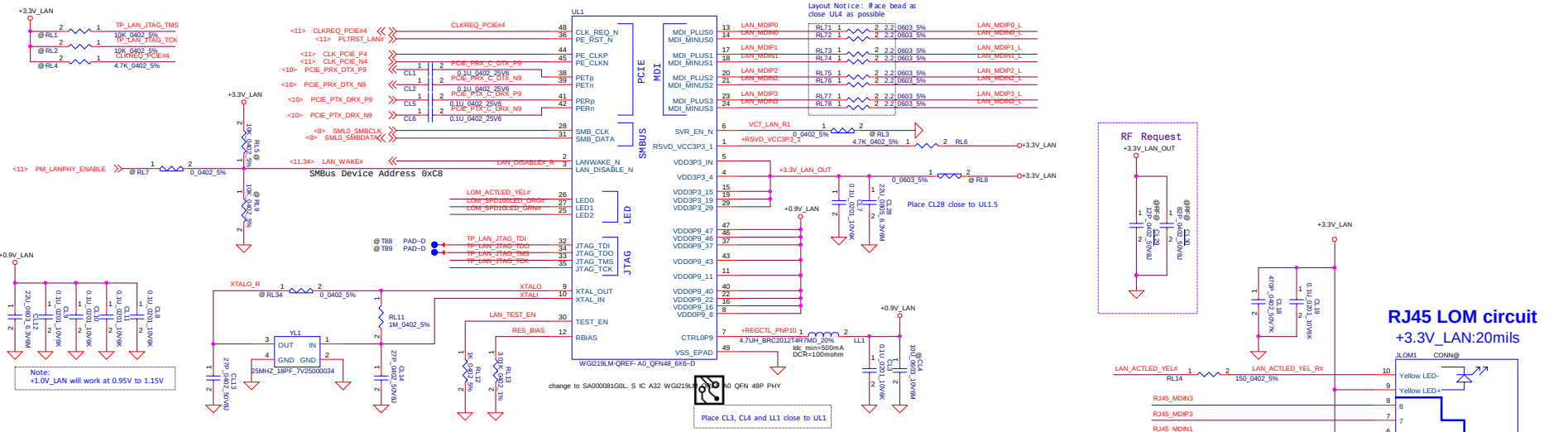
Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size | Document Number: LA-E082P | Rev: 1.0

Date: Monday, December 12, 2016 | Sheet 29 of 75



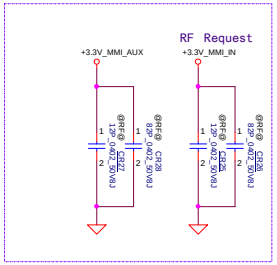
Compal Electronics, Inc.

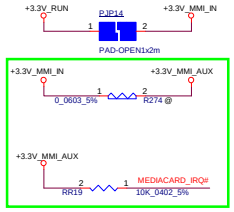
Title: LAN Clarkville & RJ45

Size | Document Number | Rev: LA-E082P | 1.0

Date: Monday, December 12, 2016 | Sheet 30 of 75

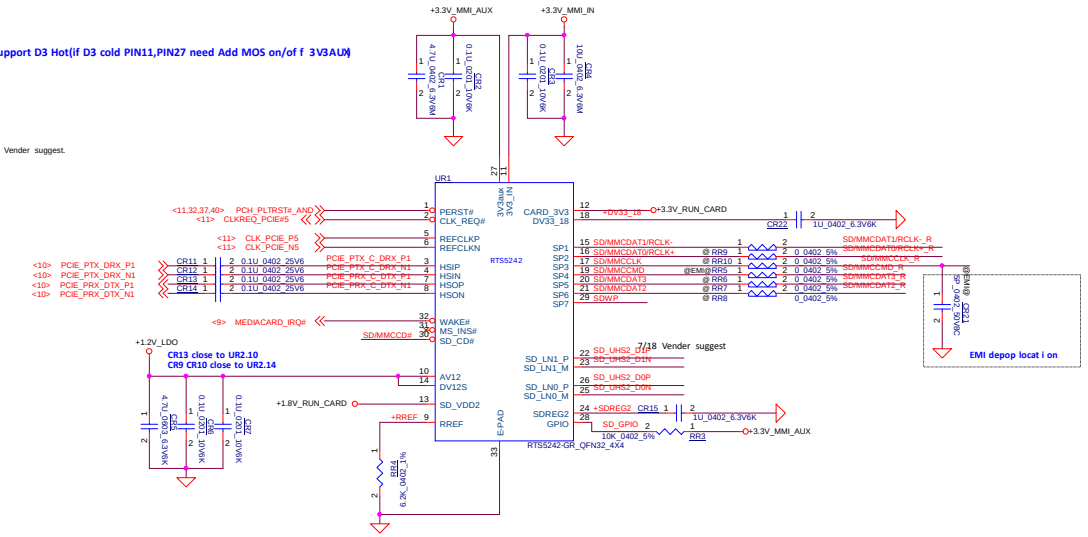
For PCIE Interface



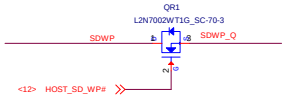


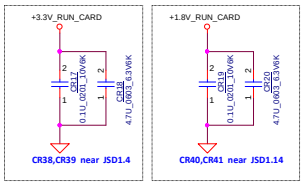
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX)

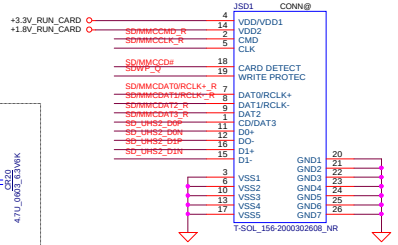
7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)







LINK SP070011U00 DONE

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Compal Electronics, Inc.

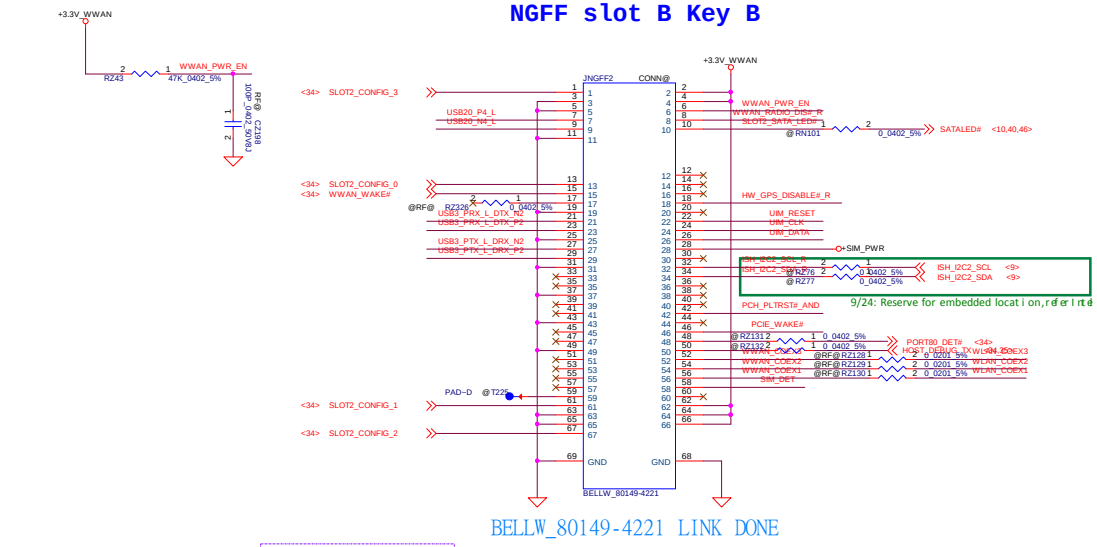
Title: Card Reader RTS5242

Size: Document Number: LA-E082P

Rev: 1.0

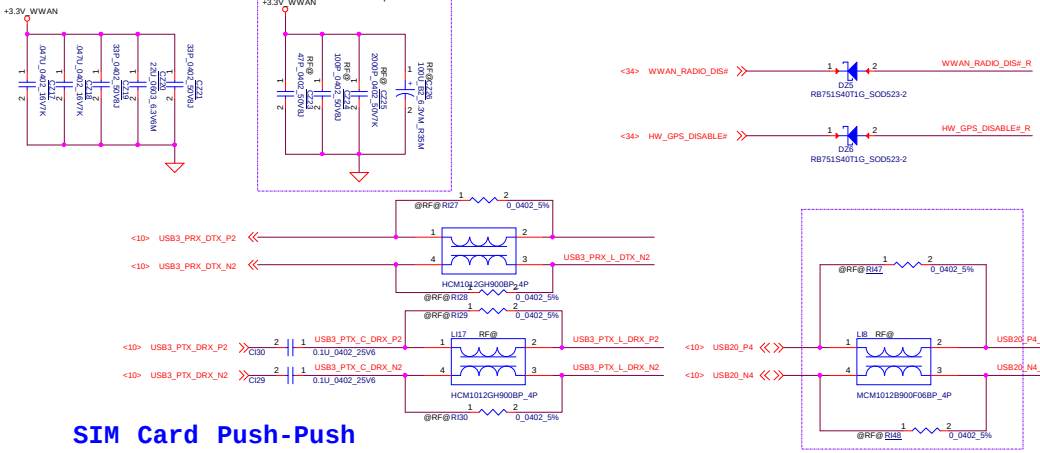
Date: Monday, December 12, 2016 Sheet 31 of 75

NGFF slot B Key B

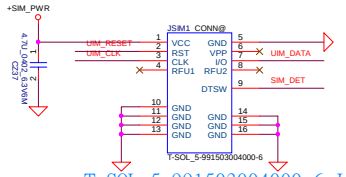


9/24: Reserve for embedded location, refer to PDG 0.9

BELLW_80149-4221 LINK DONE

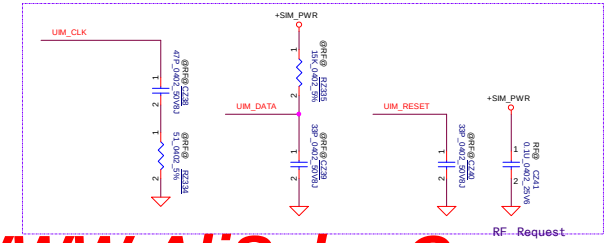


SIM Card Push-Push



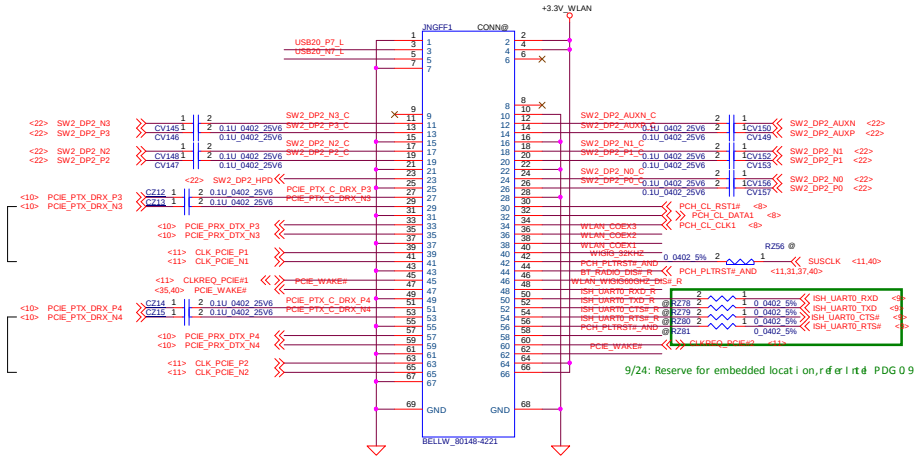
T-SOL_5-991503004000-6 LINK DONE

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low



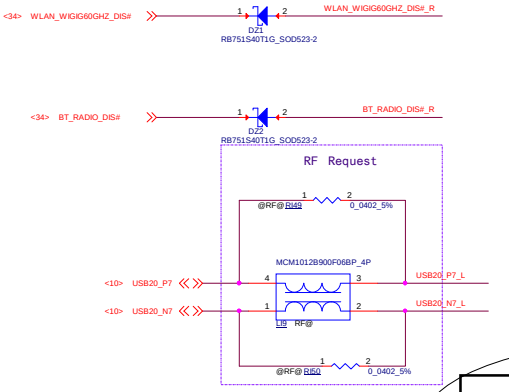
for Brekenridge 14/15 DSC

NGFF slot A Key A



9/24: Reserve for embedded location, refer to PDG 0.9

BELLW_80148-4221 LINK DONE



Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

Compal Electronics, Inc.

Title: NGFF Card

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1

ACES_50278-00401-001

Link 50278-00401-001 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 14.

Add for solve pop noise and detect issue

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

EM5209VF_SON14_2X3

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

RF Request

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

Normal Open

Only BR15U UMA use LA2,LA3,because 6L

JHP1

SINGA_2SJ3095-136111F

CONN@

Link 2SJ3095-136111F DONE

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Codec ALC3246

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	<Deciphered_Date>

Size	Document Number	Rev
C	LA-E082P	1.0

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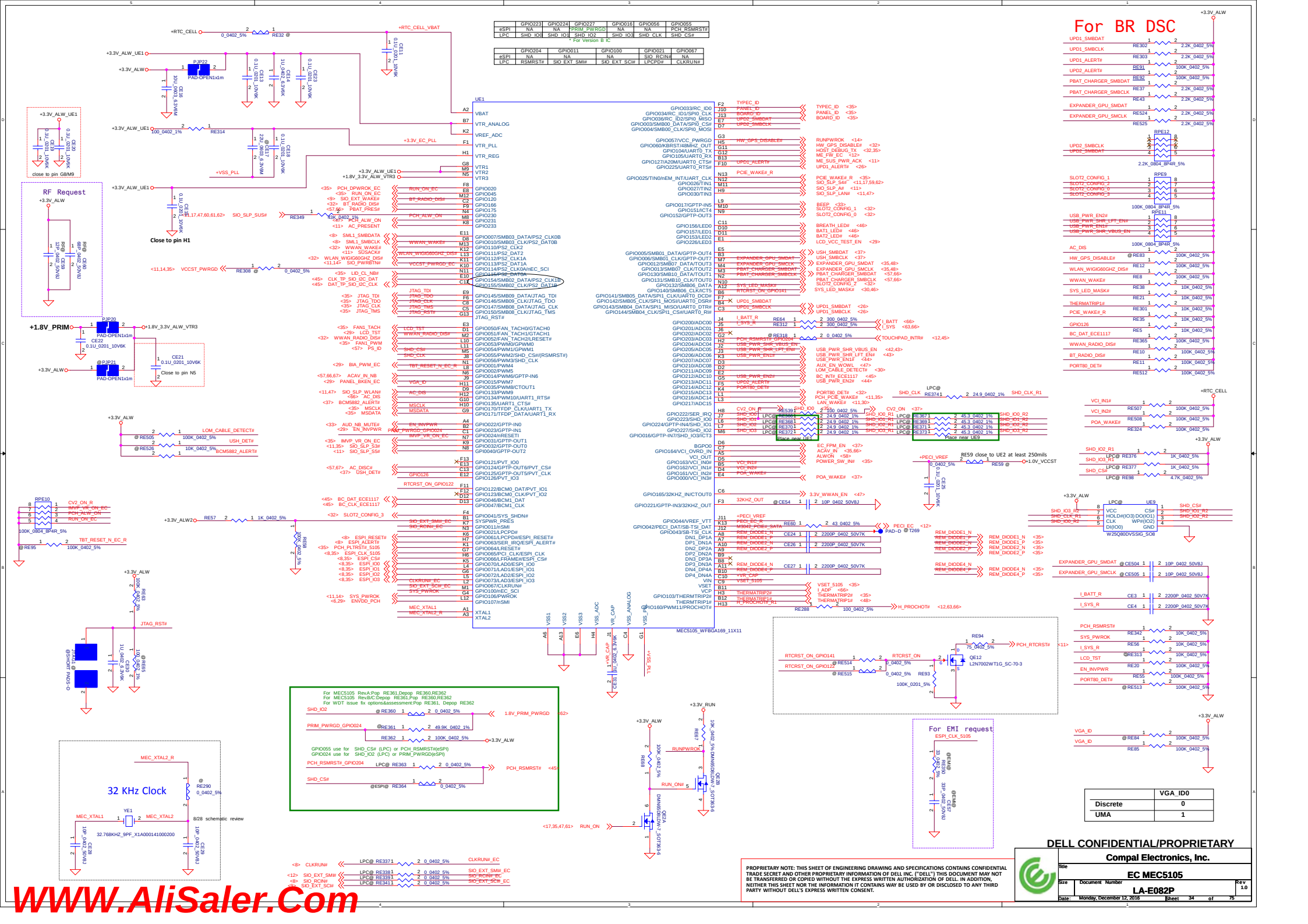
For BR DSC
RF Request
Close to pin H1
Close to pin N5
close to pin G8/M9
32 KHz Clock
For EMI request
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Compal Electronics, Inc.
EC MEC5105
LA-E082P
Rev 1.0
Monday, December 12, 2016
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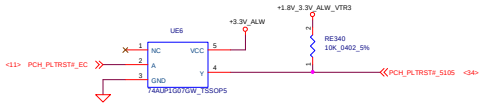
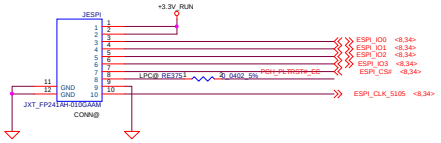
For BR DSC



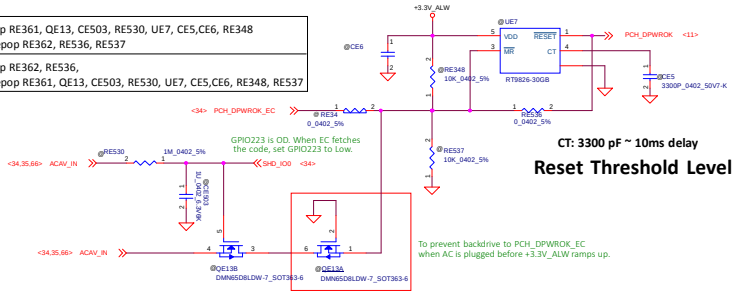


JXT_FP241AH-010GAAM LINK DONE

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

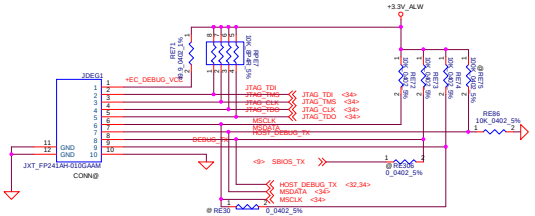
PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

WDT option
MEC5105 rev.B: Pop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348 Depop RE362, RE536, RE537
MEC5105 rev.C: Pop RE362, RE536, Depop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348, RE537



CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V



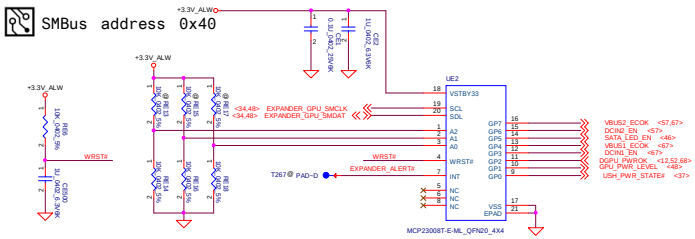
JXT_FP241AH-010GAAM LINK DONE

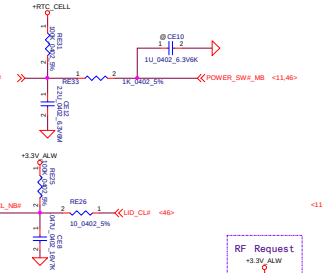
Control Byte

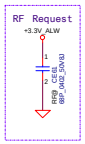
0	1	0	0	A2	A1	A0	R/W

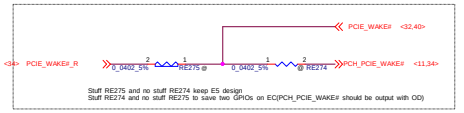
R/W = 0 = Write
R/W = 1 = Read

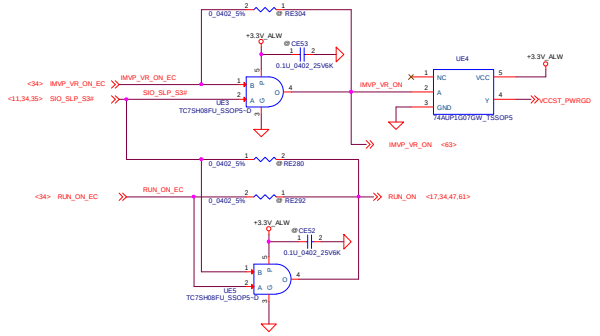
SMBus address 0x40

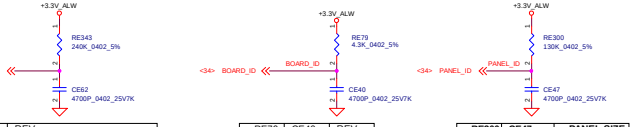












RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
	4700p	
	4700p	
1K	4700p	

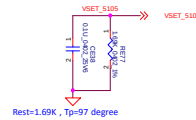
PD_ACE_DET# rise time measured from 5%~68%

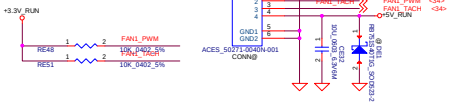
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
* 4.3K	4700p	A00
1K	4700p	

BOARD_ID rise time measured from 5%~68%

RE300	CE47	PANEL SIZE
240K	4700p	12"
* 130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

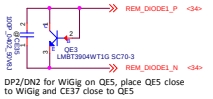
PANEL_ID rise time measured from 5%~68%



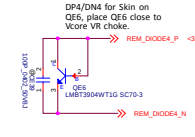


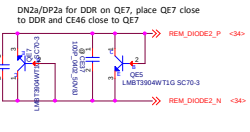
Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5





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Title: MEC5105 Support

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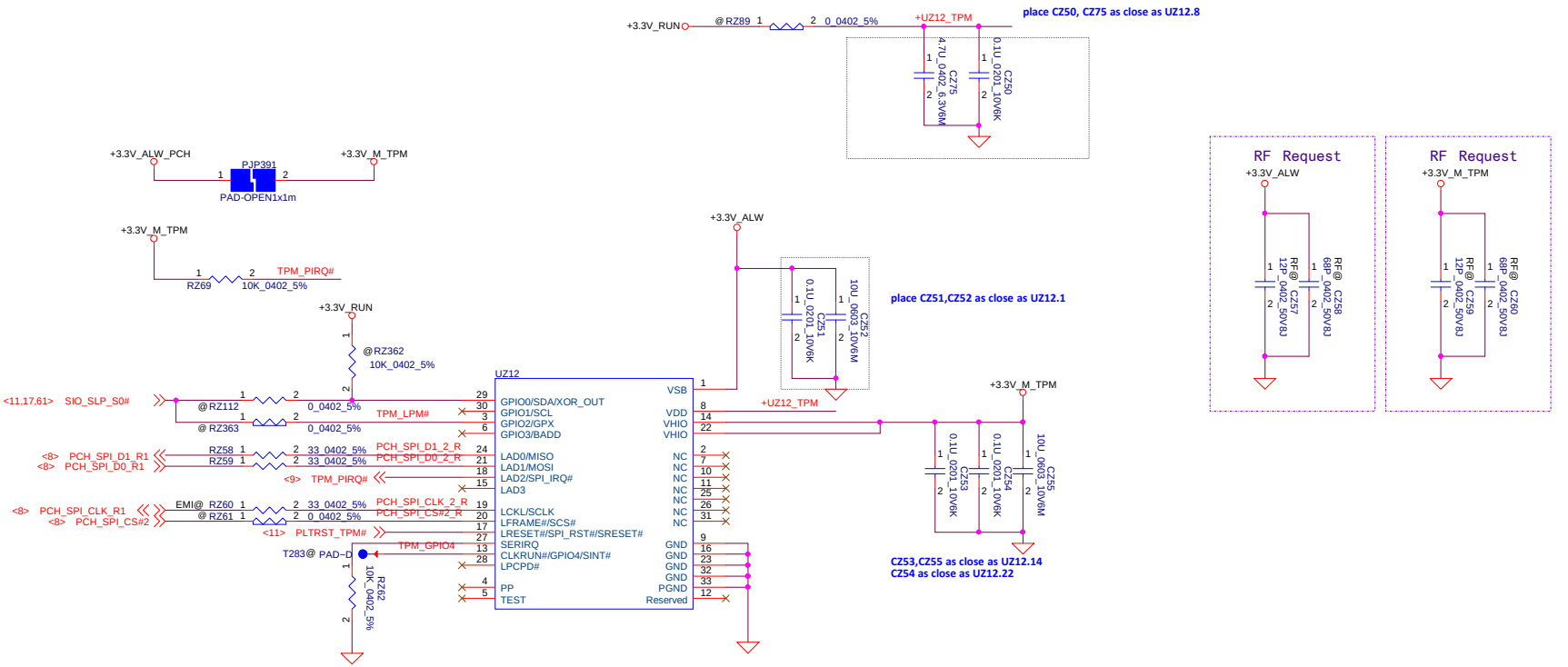
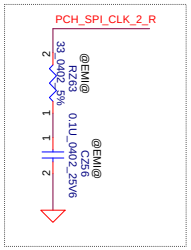
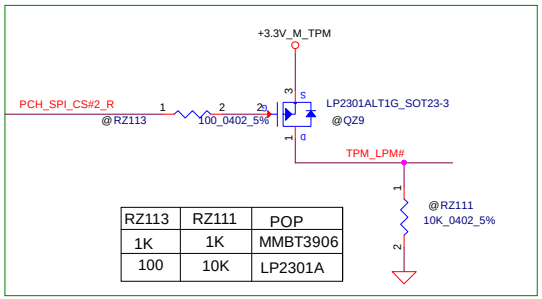
Date: Monday, December 12, 2016 | Sheet 35 of 75

For NUVOTON TPM



JB2YX change to VB2YX 09/08





RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A

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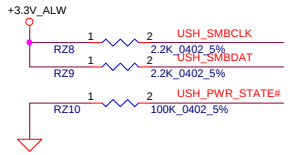
Title: USH & TPM

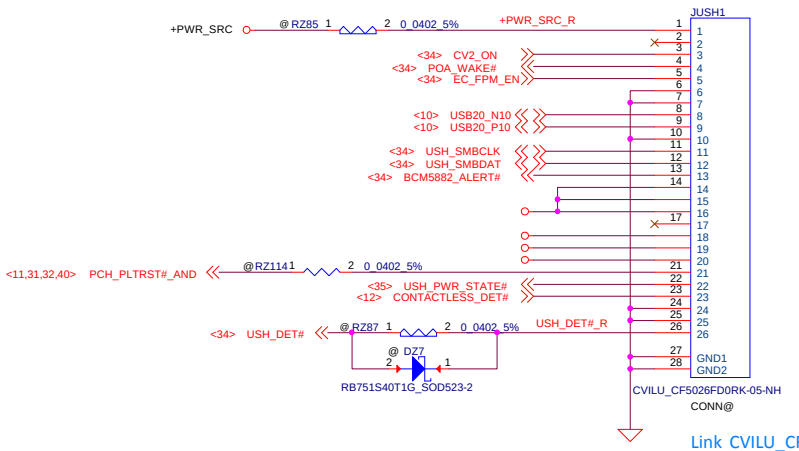
Size | Document Number: LA-E082P | Rev: 1.0

Date: Monday, December 12, 2016 | Sheet 36 of 75

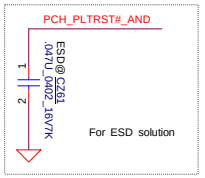
For ATMEL TPM



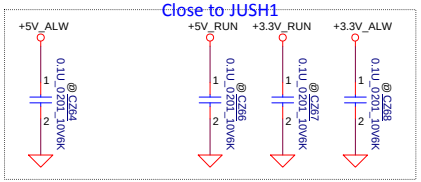
USH CONN

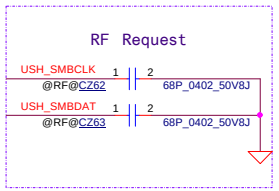


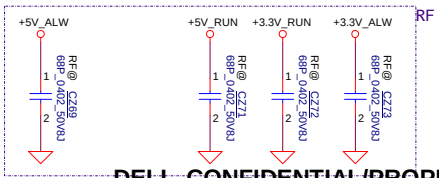
Link CVILU_CF5026FD0RK-05-NH



Close to JUSH1







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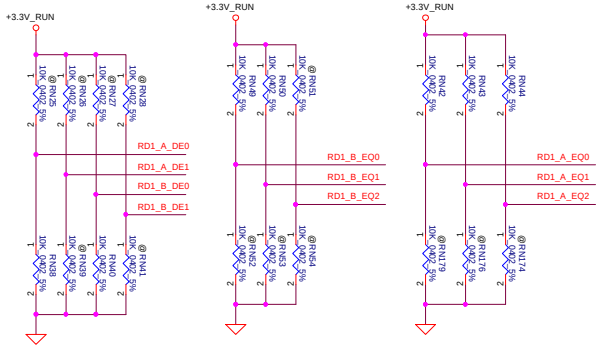
Compal Electronics, Inc.	
Title	USH & TPM
Size	Document Number: LA-E082P
Rev	1.0
Date:	Monday, December 12, 2016
Sheet	37 of 75

For Parade 2 Lane solution

	PCIE/SATA Redriver for 2280
Brekenridge12	Need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	No need
Steamboat14	Need
Kirkwood12&13	Check



Programmable output de-emphasis level setting for channel A
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
LL: -2dB
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

Programmable output de-emphasis level setting for channel B
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

[B_DE1,B_DE0] ==
LL: -2dB
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

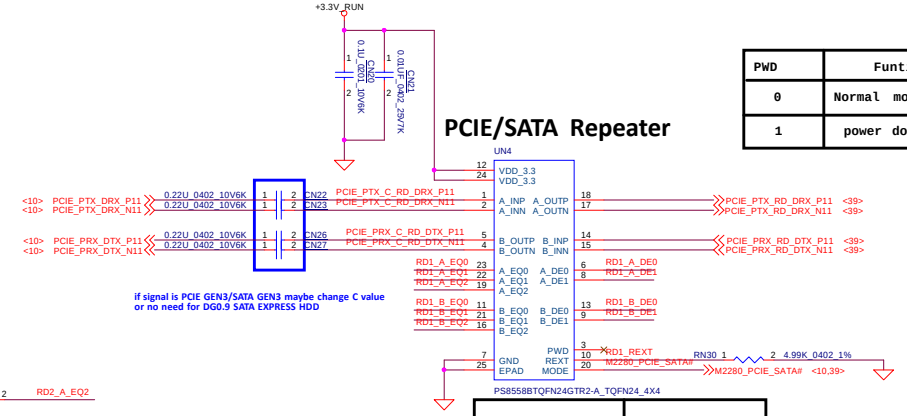
[A_EQ2,A_EQ1,A_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LLH: For channel loss up to 18dB
LHH: For channel loss up to 10dB
HLH: For channel loss up to 16dB
HHH: For channel loss up to 20dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

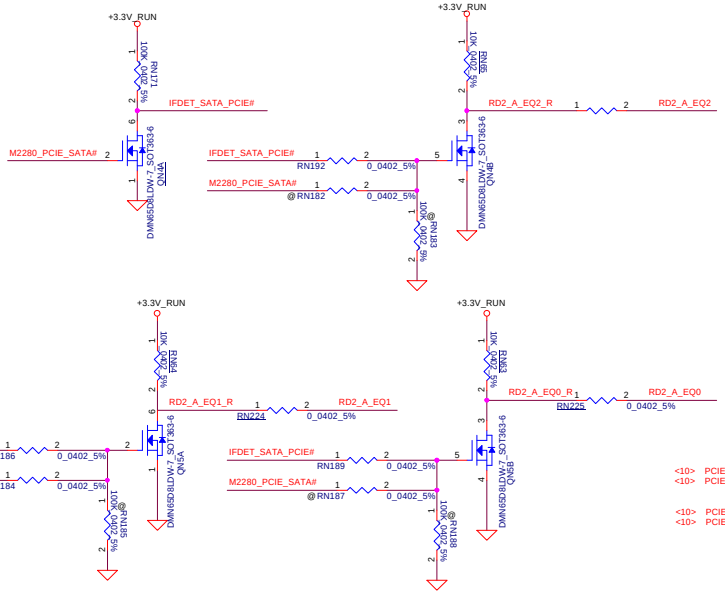
[B_EQ2,B_EQ1,B_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LLH: For channel loss up to 18dB
LHH: For channel loss up to 10dB
HLH: For channel loss up to 16dB
HHH: For channel loss up to 20dB

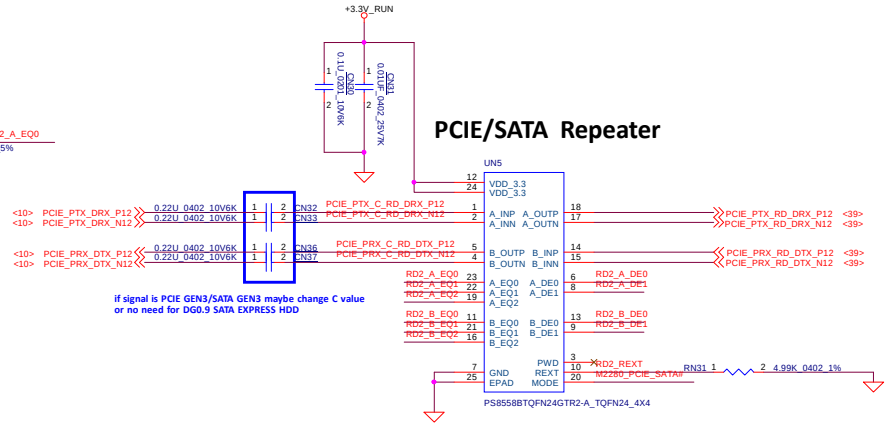
PCIE/SATA Repeater

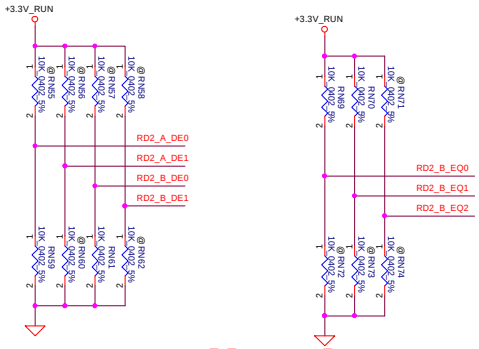
PWD	Funtion
0	Normal mode(default)
1	power down mode



0	SATA
1	PCIE







SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Compal Electronics, Inc.

Title: SATA/PCIE REPEATER for M.2 2280

Size: | Document Number: LA-E082P | Rev: 1.0

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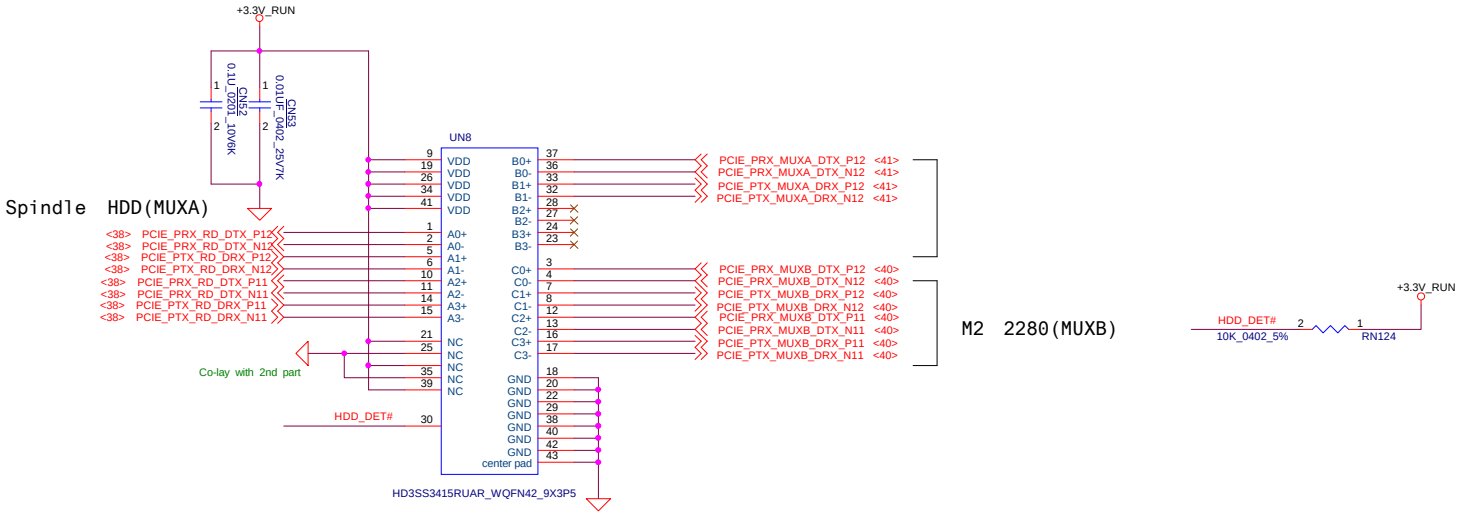
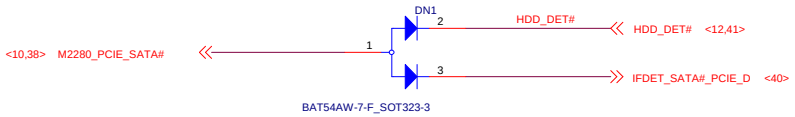
For Breckenridge 14/15 DSC

NEED LINK TI hd3ss3415 as main



IFDET_SATA#_PCIE	
L	SATA
H	PCIE

HDD_SEL(HDD_DET#)	
L	Spindle HDD(MUXA)
H	M.2 2280(MUXB)



Compal Electronics, Inc.

Title: SATA/PCIE DEMUX

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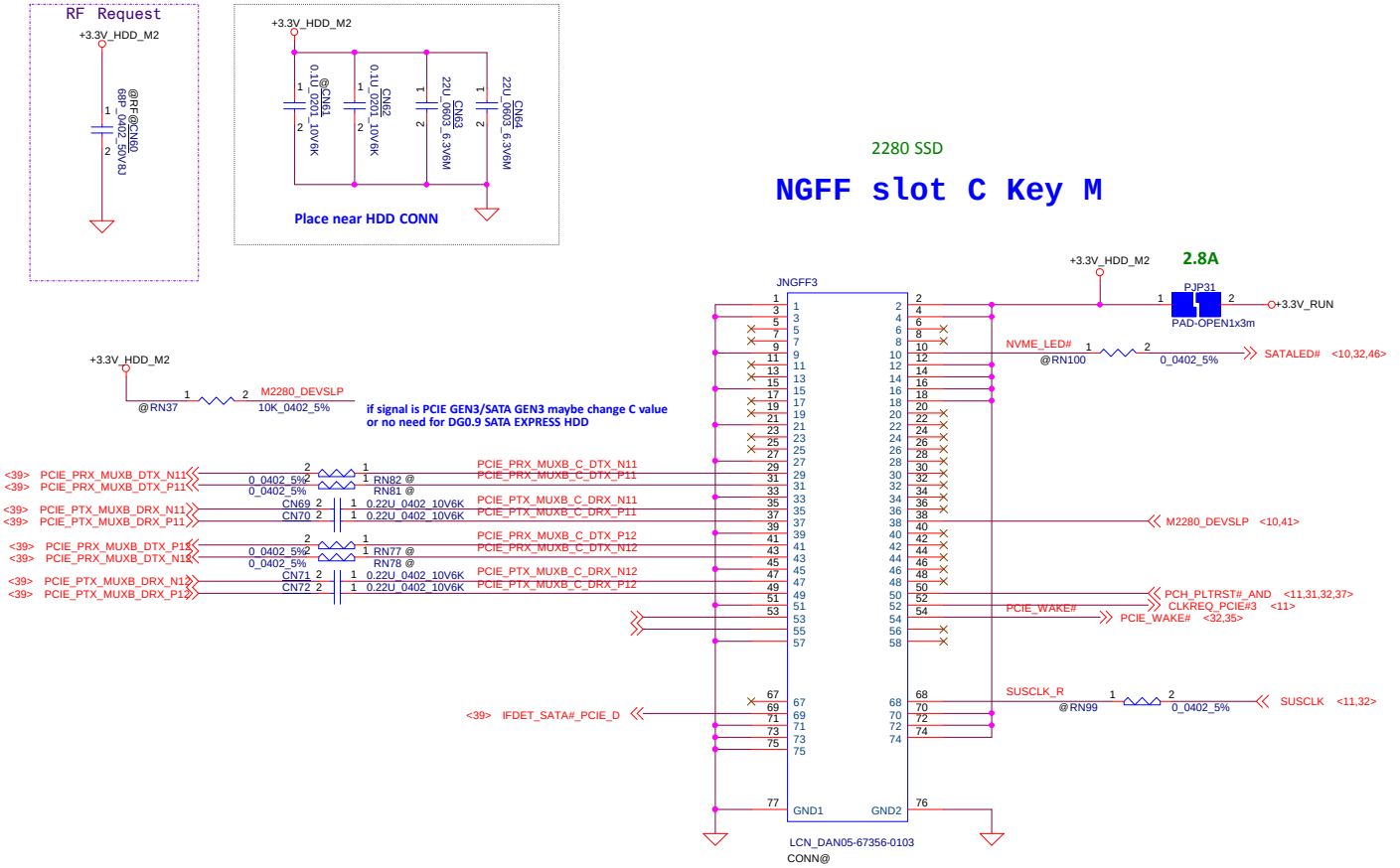

Compal Electronics, Inc.

Title: M2 2280 Socket

Size | Document Number: LA-E082P | Rev: 1.0

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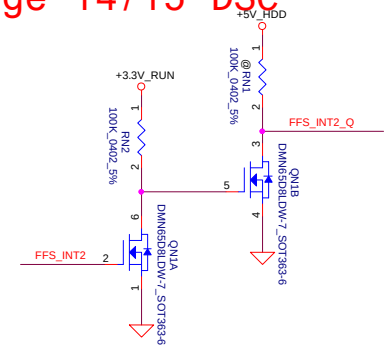
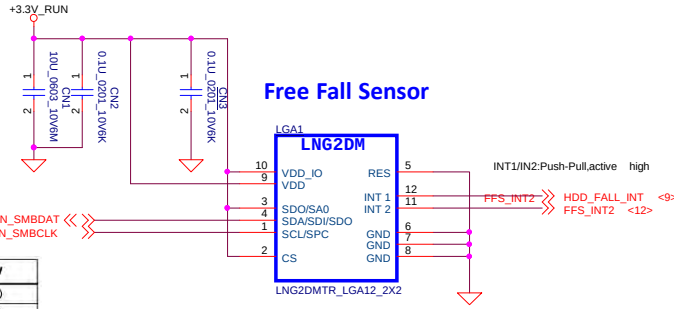
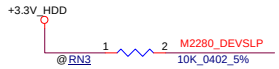
For Breckenridge 14/15 DSC

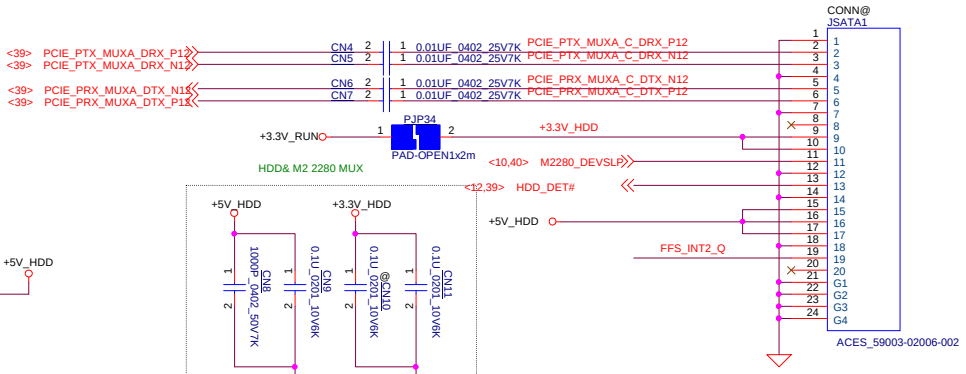


Free Fall Sensor



Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

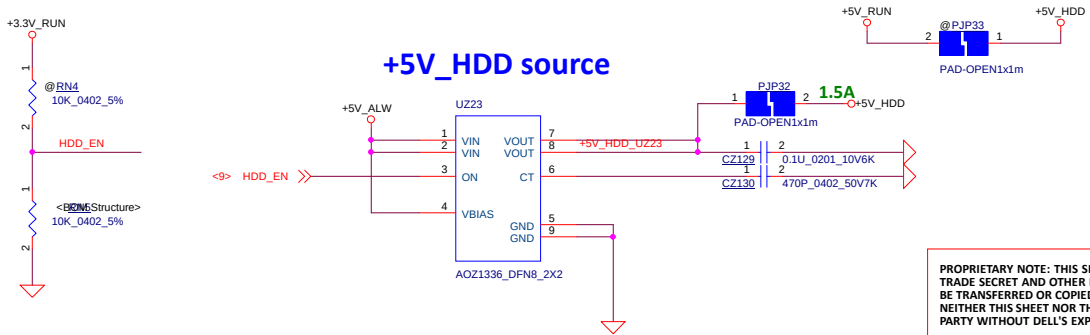




Place near HDD CONN

Link 59003-02006-002 DONE

+5V_HDD source



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: HDD CONN

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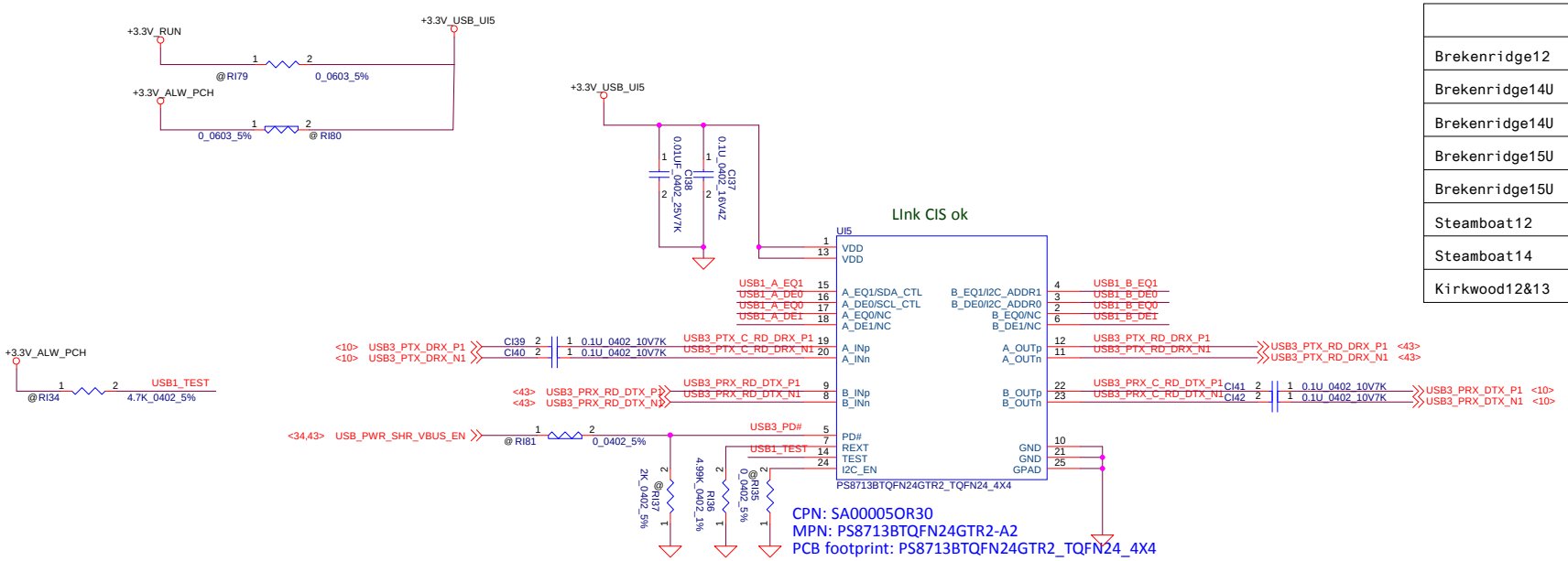
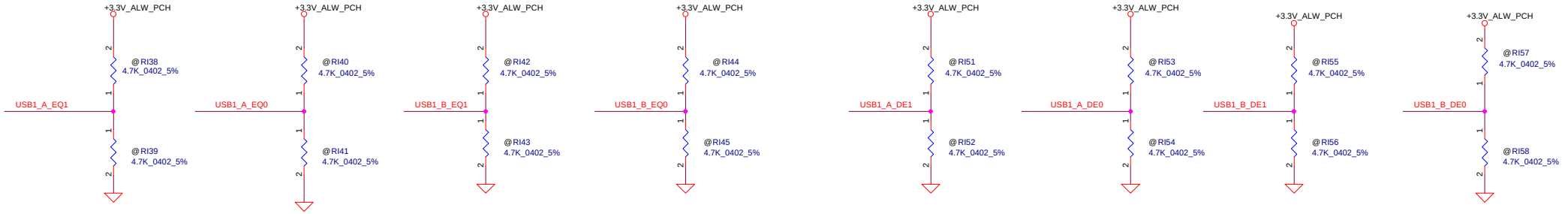


	USB3 Redriver for charge
Brekenridge12	No need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	Need
Steamboat14	Need
Kirkwood12&13	Check



Parade_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150k

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A_DE&B_DE have internal pull-down 150k

Compal Electronics, Inc.

Title: USB3.0 Repeater

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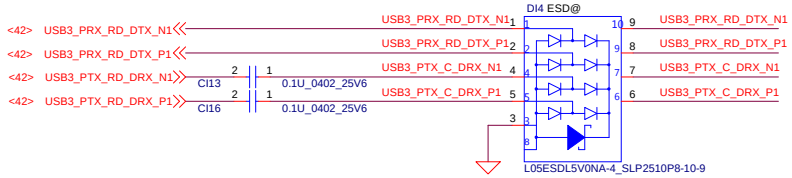
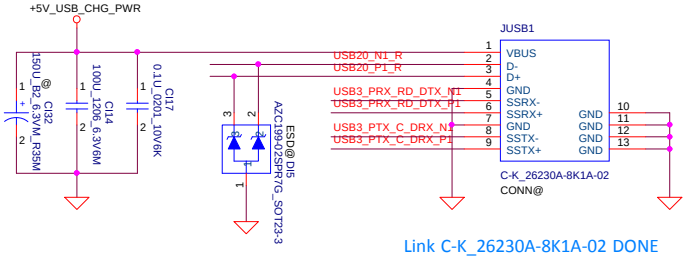
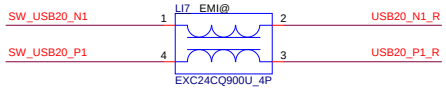
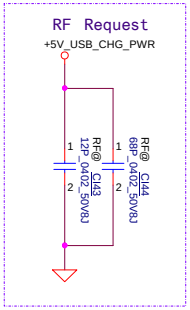
For w/ Repeater

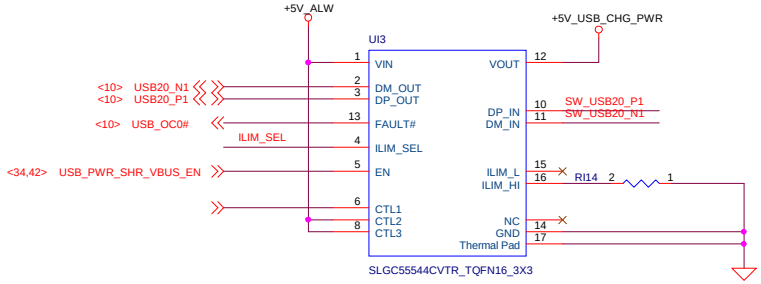




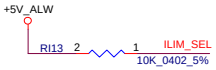
Link C-K_26230A-8K1A-02 DONE

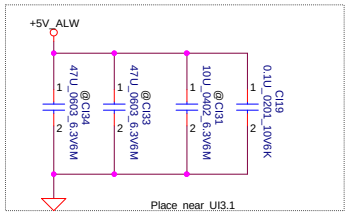






Link Seligro SA000097E10 Done
MAIN:SLGC55544CVTR





Compal Electronics, Inc.

Title: JUSB1+PS

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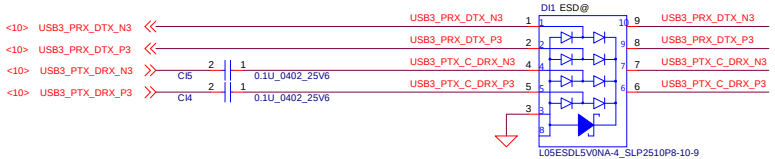
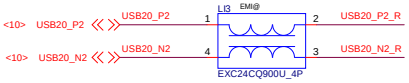
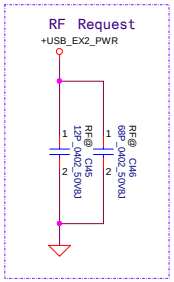
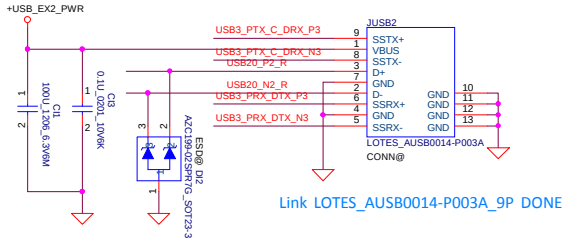
For Breckenridge 14&15/Steamboat 14



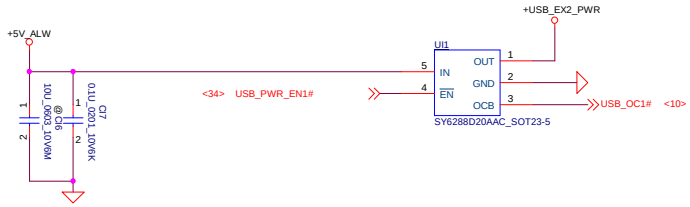




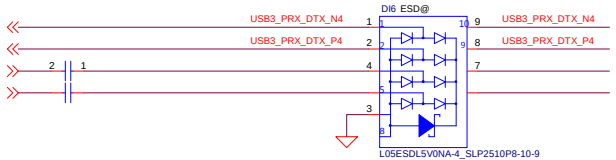


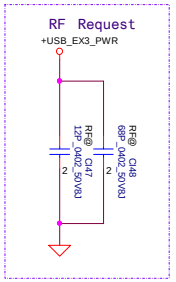
Link LOTES_AUSB0014-P003A_9P DONE

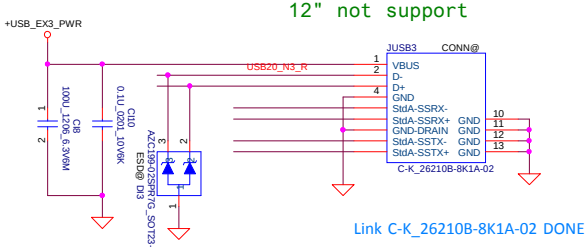
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



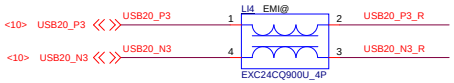
12" not support

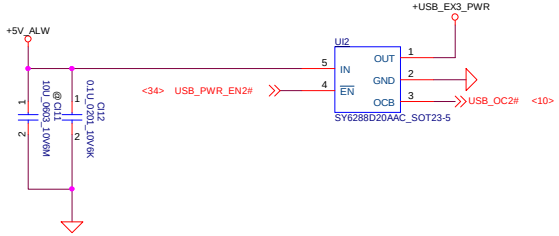






Link C-K_26210B-8K1A-02 DONE





Compal Electronics, Inc.

Title: JUSB2&JUSB3

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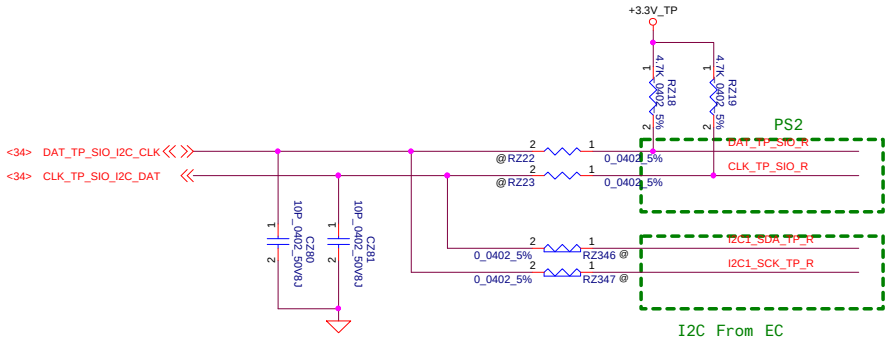
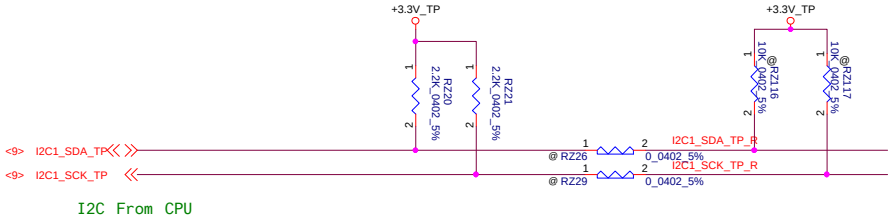
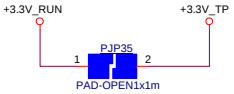
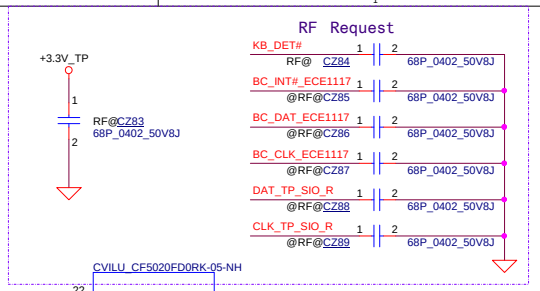
Touch Pad

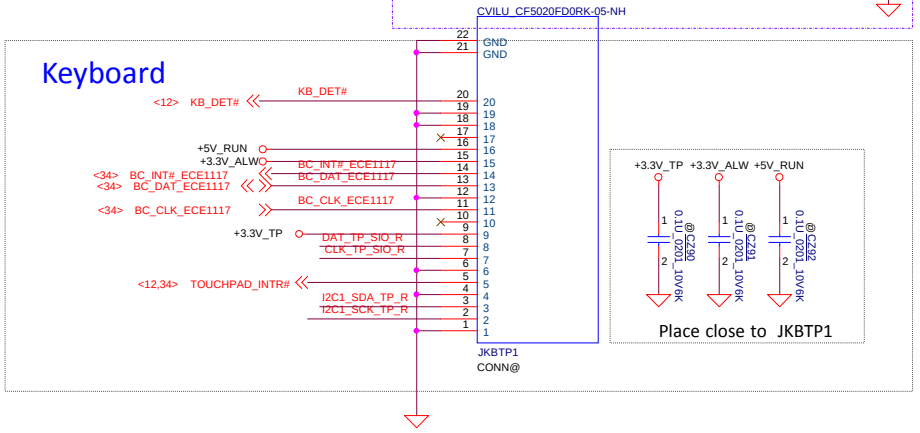




Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

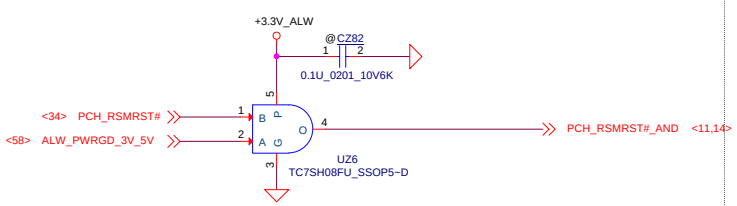






Link HRS_TF49-20S-0P5SH done

RSMRST circuit



Compal Electronics, Inc.

Title: Keyboard

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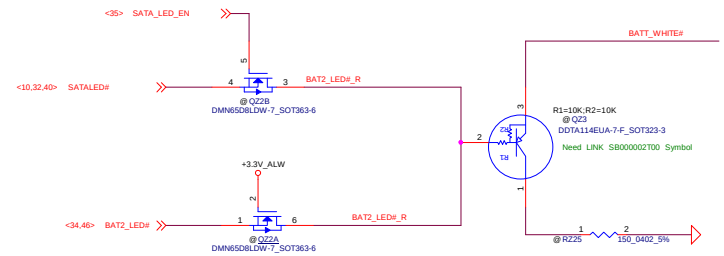
Bat t ery LE D

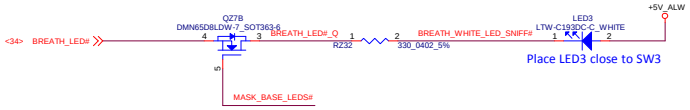
HDD LED MUX

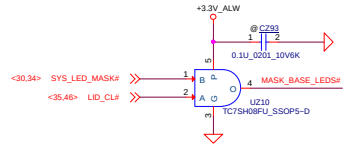
means EC can switch battery white led and HDD LED by hot key " Fn+H



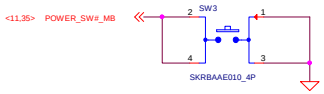
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

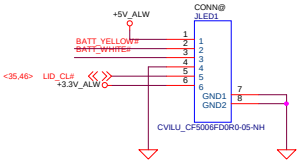




POWER & INSTANT ON SWITCH



LED board CONN

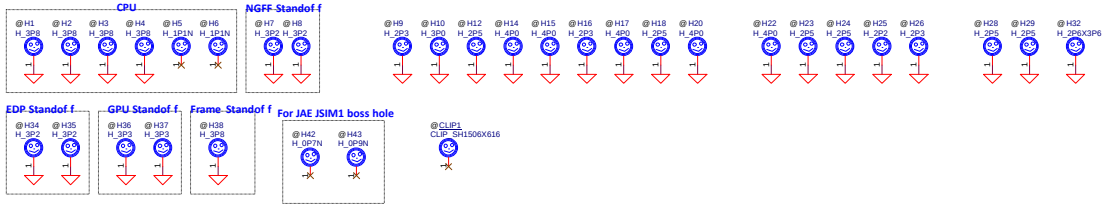


Link CF5006FD0R0-05-NH DONE

Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



Compal Electronics, Inc.

Title: PAD, LED

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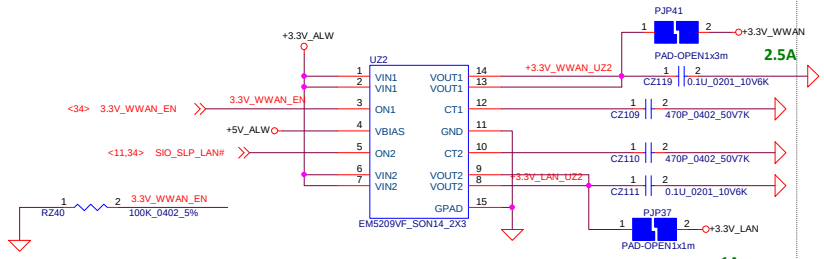
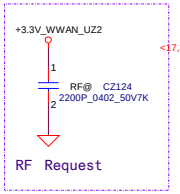
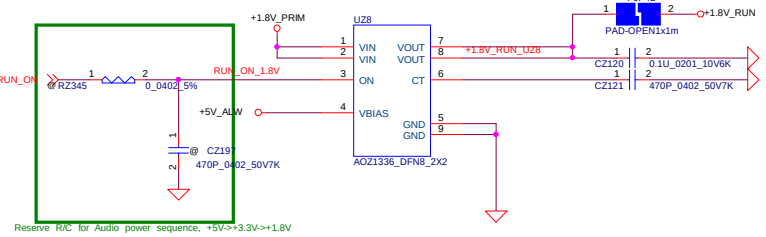
+3.3V_WWAN/+3.3V_LAN source

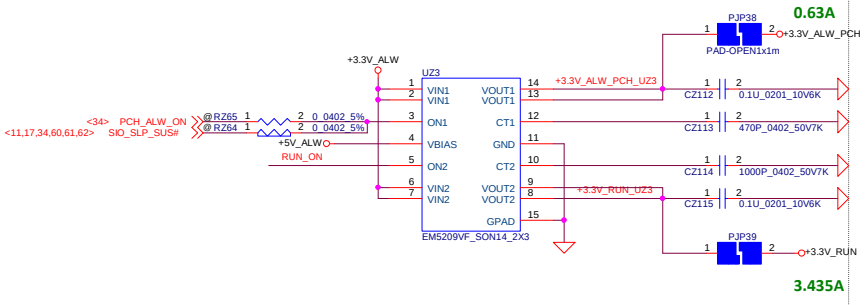




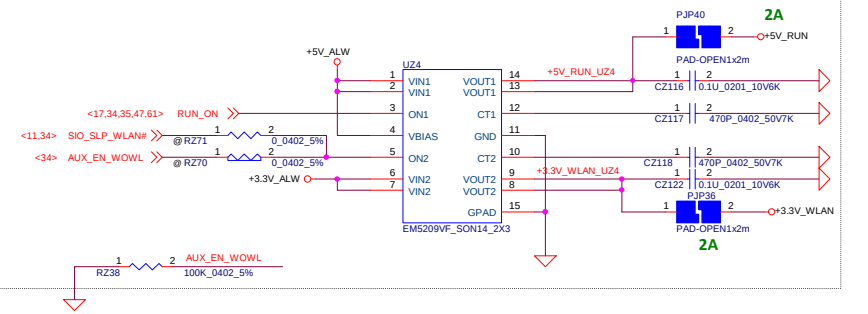
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WLAN source



Compal Electronics, Inc.			
Title: Power control			
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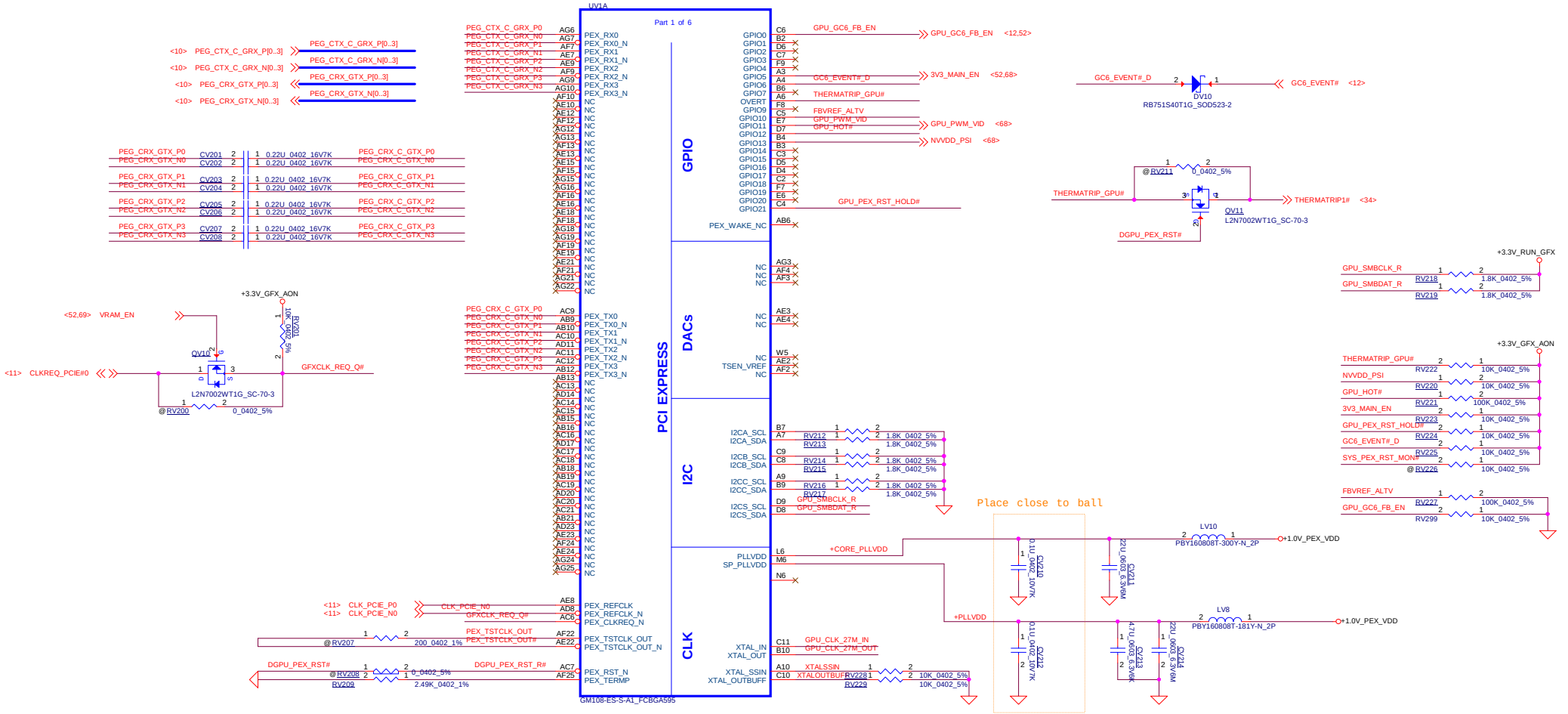

SP_PLLVDD and VID_PLLVDD Power rail Filtering Combined	
Capacitor Type	Population
0.1uF 0402	1 per ball
4.7uF 0603	1
22uF 0805	1
Bead 180 ohm (ESR=0.2 ohm) 0603	1

PLLVDD Filtering	
Capacitor Type	Population
0.1uF 0402	1
22uF 0805	1
Bead 30 ohm (ESR=0.05 ohm) 0402	1

GPU_PWR_LEVEL	
LOW	Low Performace
HIGH	High Performace

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Compal Electronics, Inc.

Title: N15S PCIE,I2C,DAC,GPIO

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I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi-GPU usage)

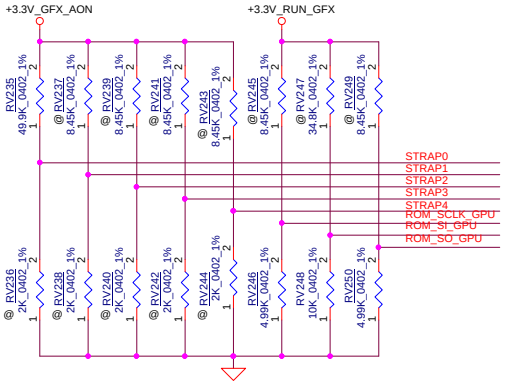
VGA_DEVICE Setting

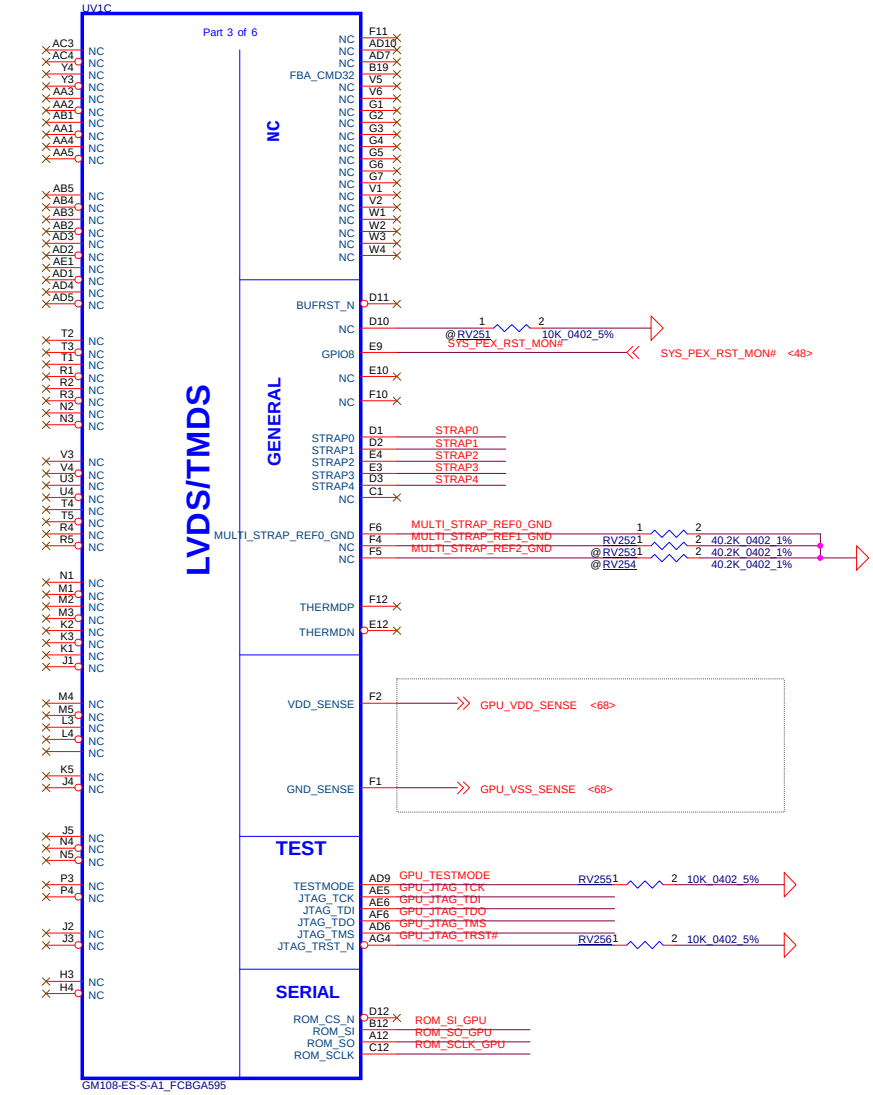
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 302h)
1	Primary Display or VGA Device(Class Code 300h)

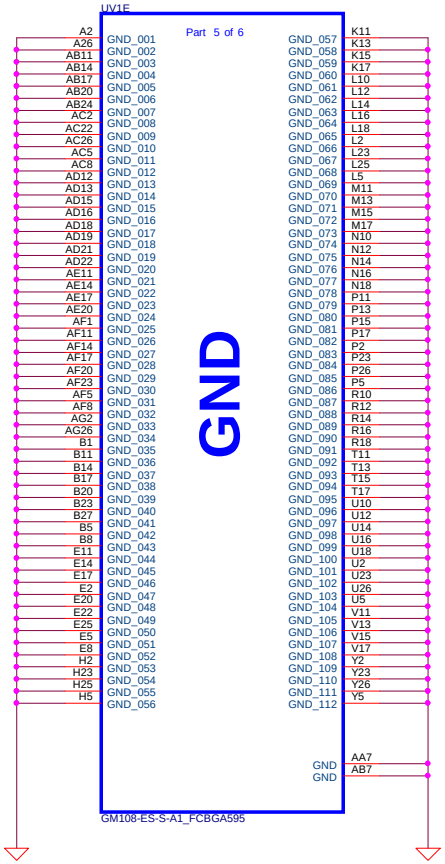
Resistance Mapping to Hex Values

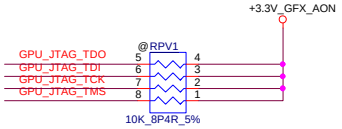
Resistor Value	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Decive ID change to 0x1056









Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down RV246 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down RV248 24.9k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(defual)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down RV250 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up RV235 50k to +3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID_SEL/PCIE_CFG defaul set 0, need refer Platform Update Notification for the latest configuration

VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x7	H5TC4G63CFR-N0C	RV248 45.3k PD
Micron	0x6	MT41J256M16LY-091G:N	RV248 34.8k PD
Samsung	0x1	K4W4G1646E-BC1A	RV248 10k PD

Compal Electronics, Inc.

Title: N15S DP, STRAP, GND

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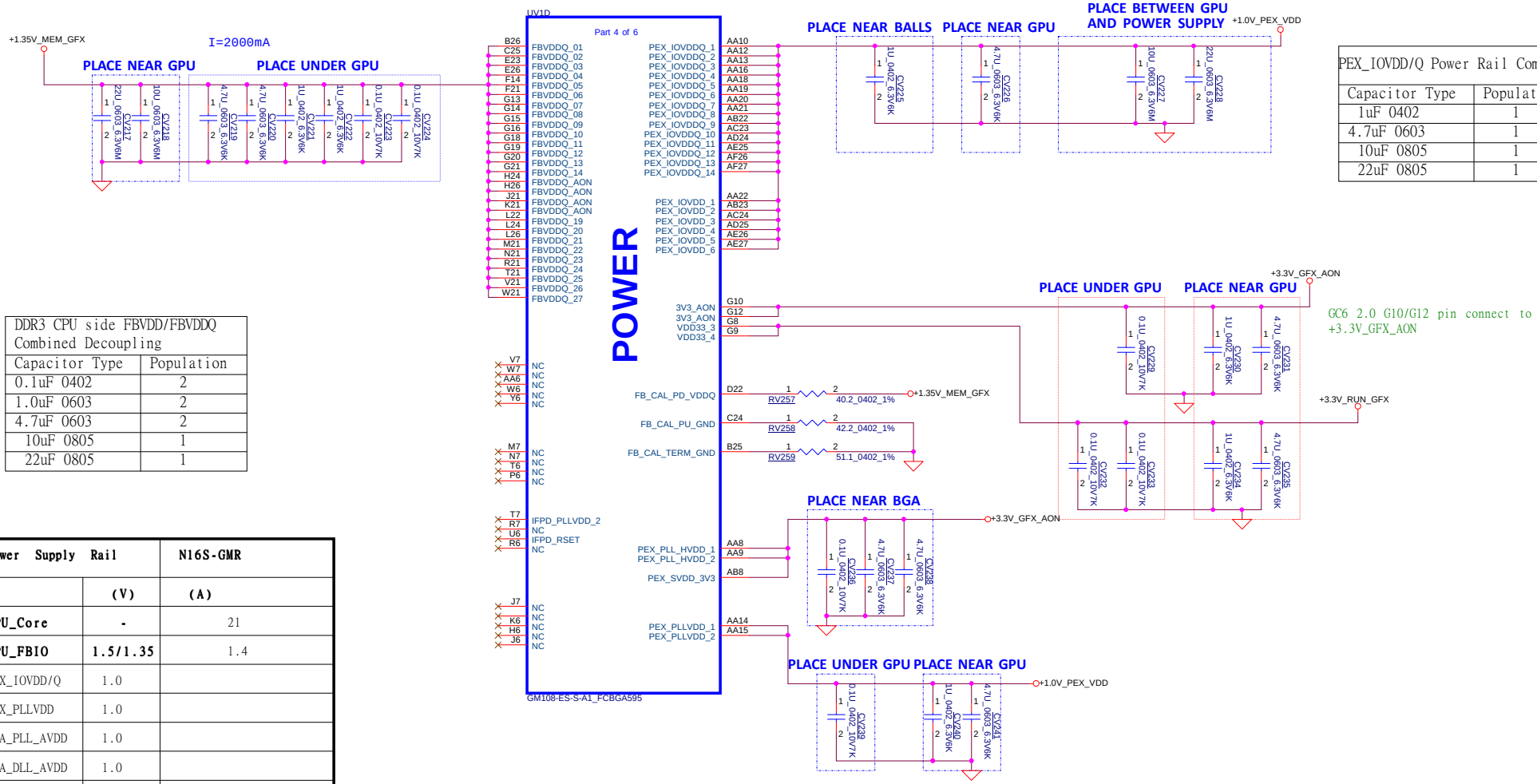

PEX_IOVDD/Q Power Rail Combined	
Capacitor Type	Population
1uF 0402	1
4.7uF 0603	1
10uF 0805	1
22uF 0805	1

DDR3 CPU side FBVDD/FBVDDQ Combined Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	2
4.7uF 0603	2
10uF 0805	1
22uF 0805	1

Power Supply Rail		N16S-GMR
	(V)	(A)
GPU_Core	-	21
GPU_FBIO	**1.5/1.35**	1.4
PEX_IOVDD/Q	1.0	
PEX_PLLVDD	1.0	
FBA_PLL_AVDD	1.0	
FBA_DLL_AVDD	1.0	
PLL_VDD	1.0	
SP_PLLVDD	1.0	
1.1V Total	1.0	0.8
VDD33+3V3AON	3.3	
PEX_SVDD_3V3	3.3	
PEX_PLL_HVDD	3.3	
3.3V Total	**3.3**	0.06

PEX_PLLVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0805	1

PEX_SVDD/PEX_PLL_HVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
4.7uF 0603	2

3V3_MAIN Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1uF 0603	1
4.7uF 0603	1

3V3_AON Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0603	1

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Title: N15S Power

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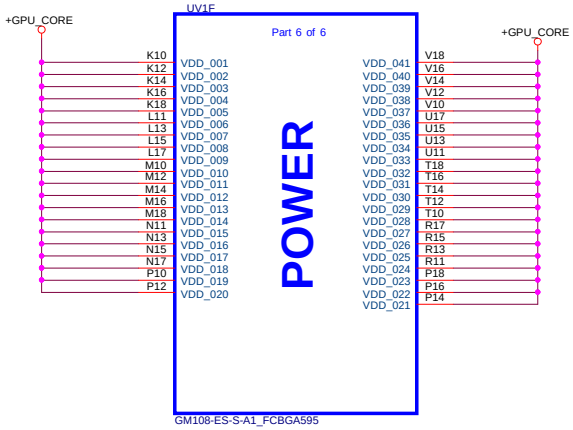
Caps on Power Side
1UX4 4.7UX10 under GPU
4.7UX5 22UX1 47UX2 330UX2 near GPU



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Title: N15S Power GFX Core

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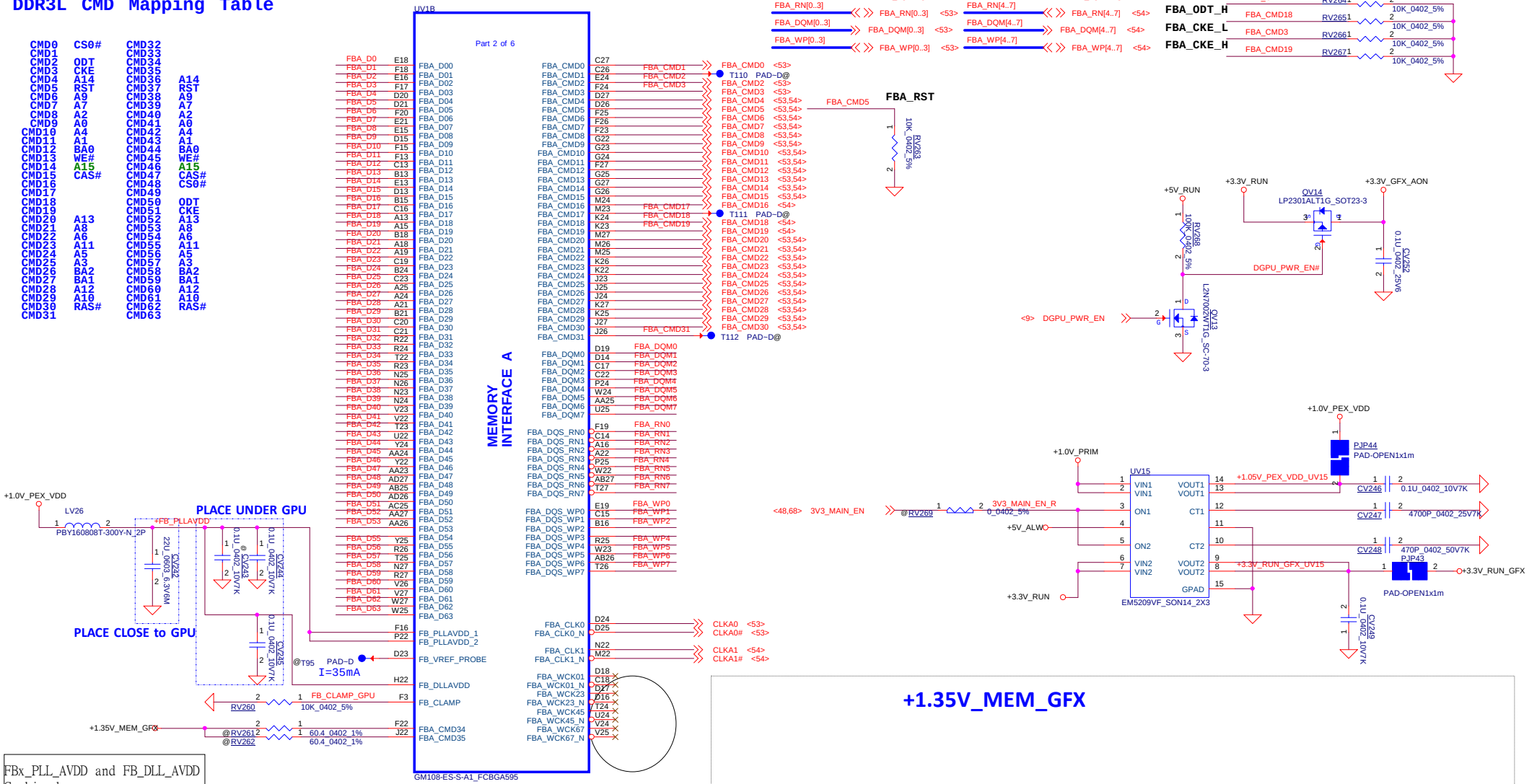
DDR3L CMD Mapping Table

CMD0	CS0#	CMD32
CMD1		CMD33
CMD2	ODT	CMD34
CMD3	CKE	CMD35
CMD4	A14	CMD36 A14
CMD5	RST	CMD37 RST
CMD6	A9	CMD38 A9
CMD7	A7	CMD39 A7
CMD8	A2	CMD40 A2
CMD9	A0	CMD41 A0
CMD10	A4	CMD42 A4
CMD11	A1	CMD43 A1
CMD12	BA0	CMD44 BA0
CMD13	WE#	CMD45 WE#
CMD14	A15	CMD46 A15
CMD15	CAS#	CMD47 CAS#
CMD16		CMD48 CS0#
CMD17		CMD49
CMD18		CMD50 ODT
CMD19		CMD51 CKE
CMD20	A13	CMD52 A13
CMD21	A8	CMD53 A8
CMD22	A6	CMD54 A6
CMD23	A11	CMD55 A11
CMD24	A5	CMD56 A5
CMD25	A3	CMD57 A3
CMD26	BA2	CMD58 BA2
CMD27	BA1	CMD59 BA1
CMD28	A12	CMD60 A12
CMD29	A10	CMD61 A10
CMD30	RAS#	CMD62 RAS#
CMD31		CMD63



FBx_PLL_AVDD and FB_DLL_AVDD Combined	
Capacitor Type	Population
0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1

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Title: N15S Memory

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Memory Partition A - Upper 16 bits

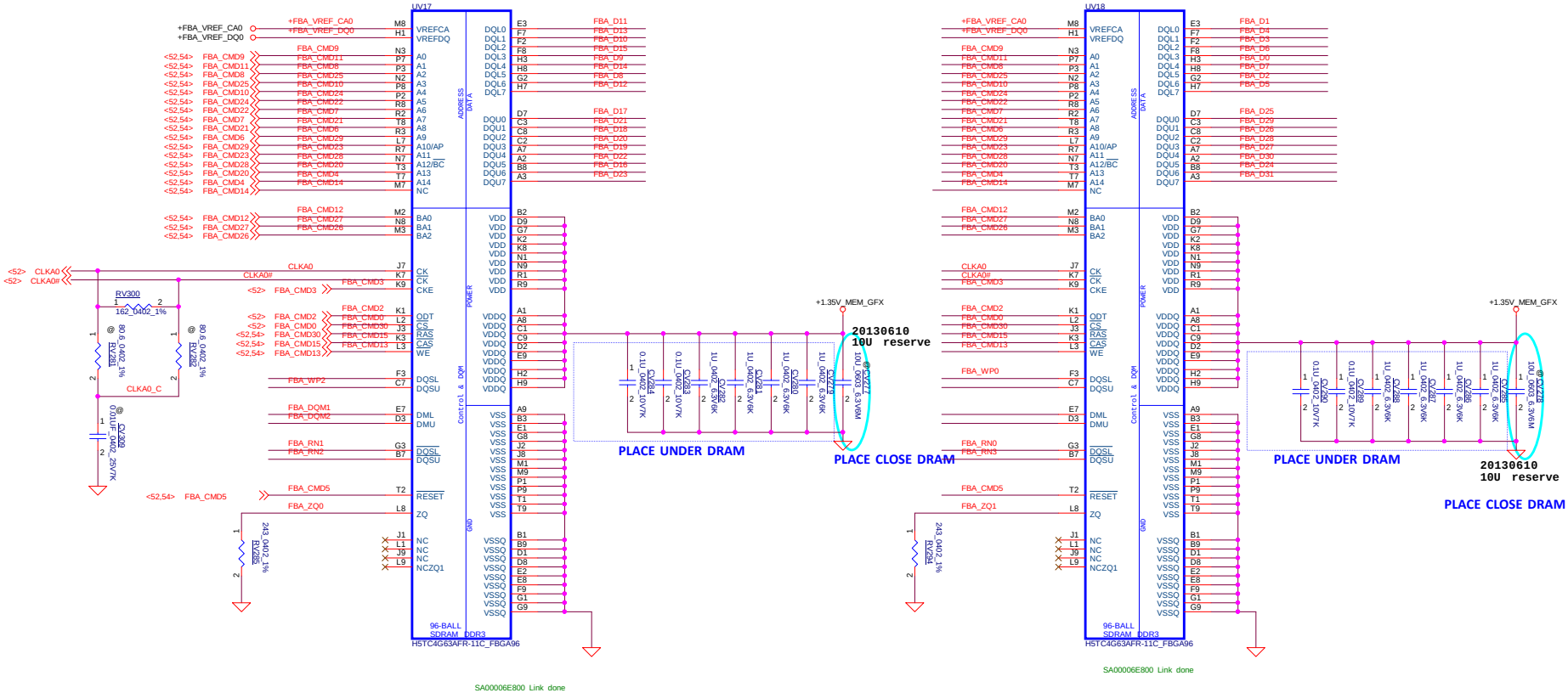
256x16 DDR3L

FBA_D[0..31] — FBA_D[0..31] <52>

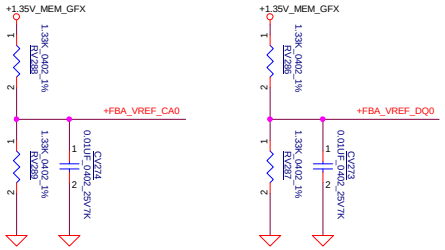
FBA_WP[0..3] — FBA_WP[0..3] <52>

FBA_DQM[0..3] — FBA_DQM[0..3] <52>

FBA_RN[0..3] — FBA_RN[0..3] <52>



DDR3 per Memory FBVDD/Q Decoupling	
FBVDD/Q Combined	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	4
10uF 0805	0



Compal Electronics, Inc.

Title: MARX-VRAM_A Lower

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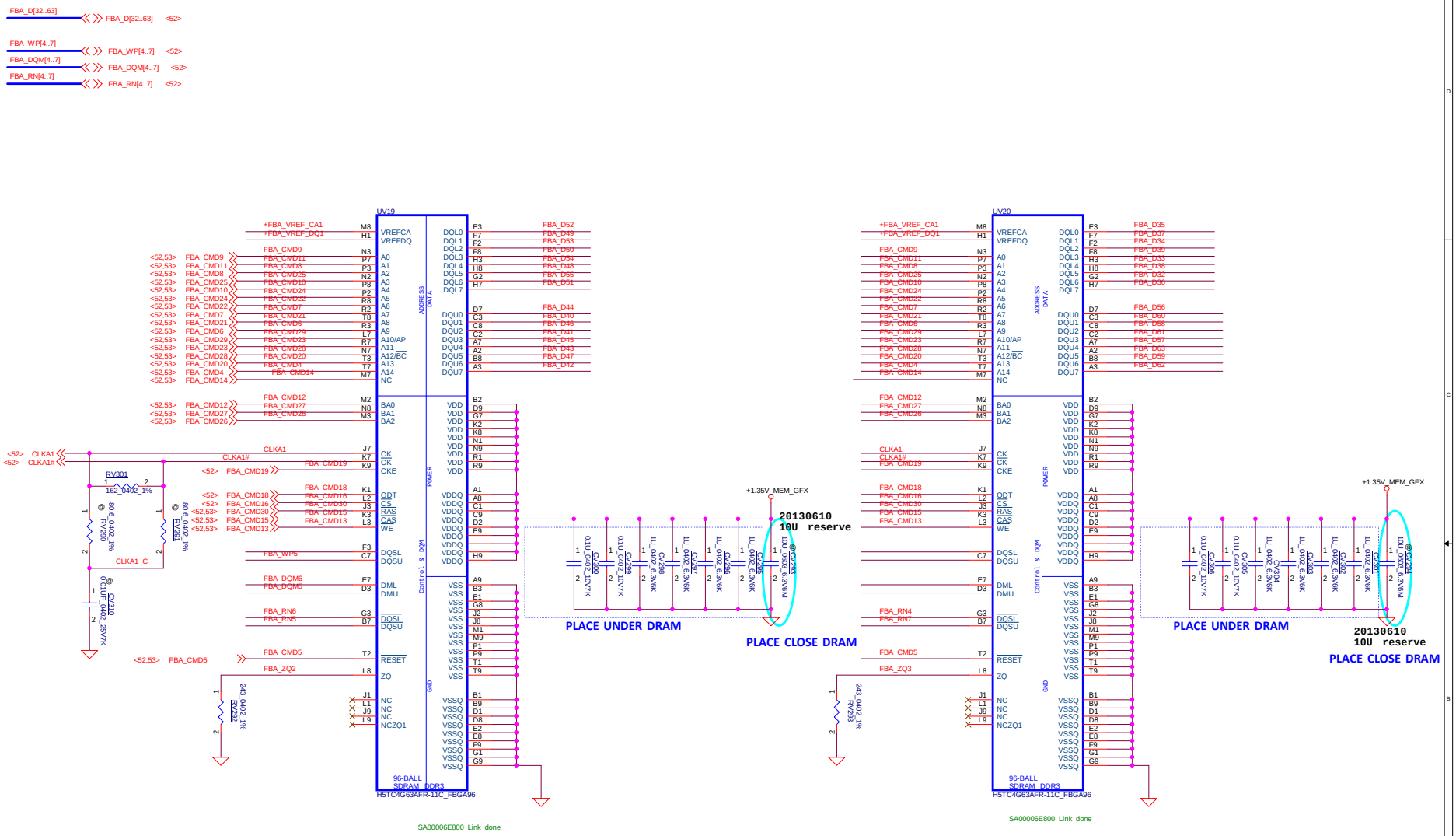
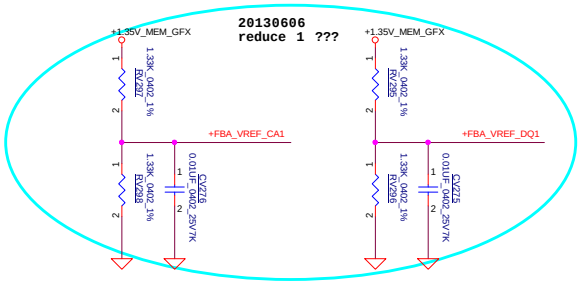
Memory Partition A - Lower 16 bits

256x16 DDR3L





Compal Electronics, Inc.

Title: MARX-VRAM_A Lower

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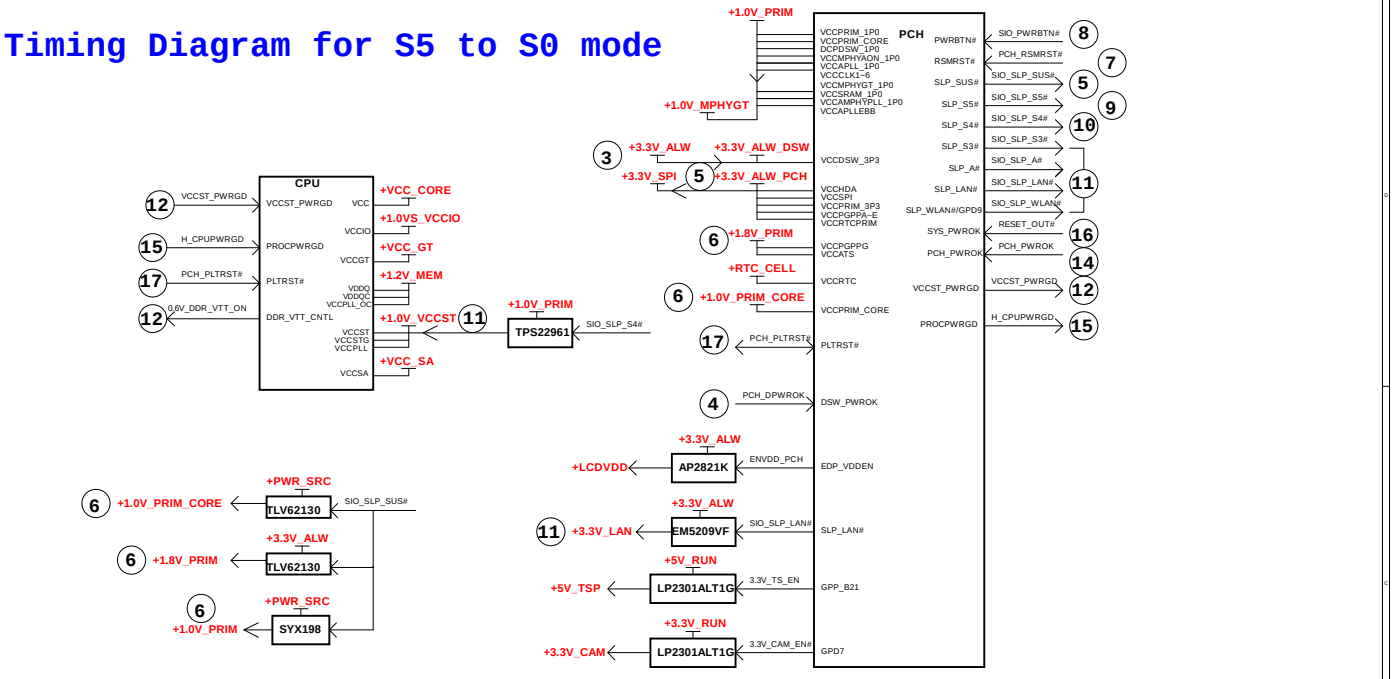
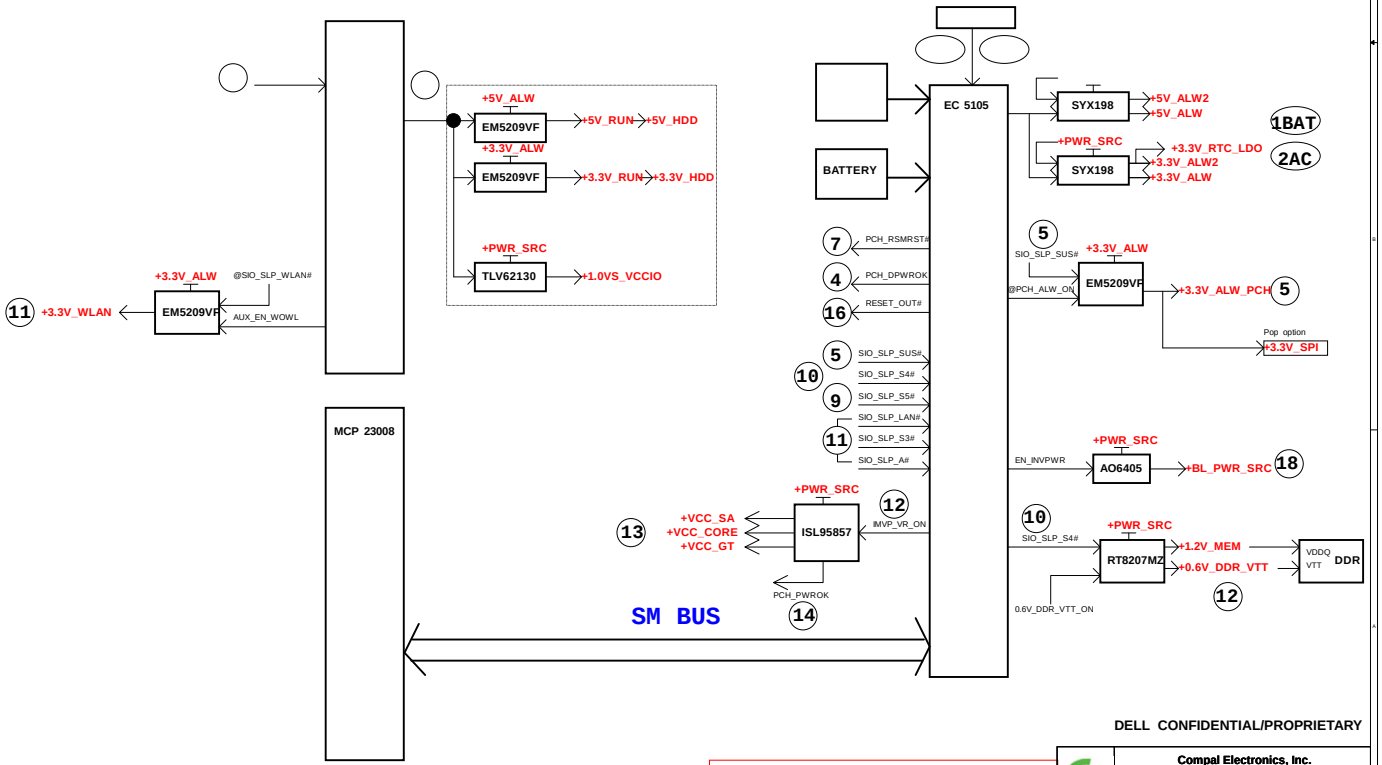
Timing Diagram for S5 to S0 mode





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Power Sequence

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1

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay time(ps/inch)	25 ± 2.5 ohm single-end	35 ± 3.5 ohm single-end	39 ± 3.9 ohm single-end	43 ± 4.3 ohm Single-end	45 ± 4.5 ohm Single-end	48 ± 4.8 ohm single-end	50 ± 5 ohm Single-end	52 ± 5.2 ohm Single-end	50 ± 5 ohm Diff.	70 ± 7 ohm Diff.	75 ± 7.5 ohm Diff.	80 ± 8 ohm Diff.	83 ± 83 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	88 ± 8.8 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	100 ± 10 ohm Diff.	Ref	100 ± 10 ohm Diff.	Ref	90 ± 9 ohm Diff.	Ref
			SolderMask	IT-158	0.5		trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)		trace Width (±12%)		trace Width (±12%)	
			Add Plating												SE 25	SE 40	SE 43	SE 46		SE 50	SE 52				SE 50	SE 50	SE 52								
1	Top		Copper foil	0.5oz+plating	1.6	149.18	13.4	8	6.8	5.5	5	4.3	4	3.7	13.5/X	6.8/5.2	5.5/4.5	4.4/3.7	3.9/3.5	4/4.1	3.7/3.6				4/5	4/5.7	3.7/4.7	3/3.3	3.5/4.5	3.5/5.3	L2	9/8.5	no Ref	7/6	L3
		3.8	Prepreg	1080	3.5		24.98	34.95	39.05	43.06	45.2	48.08	50.23	52	無法做對	69.98	75	79.85	82.85	84.88	85.11				88.12	90.04	89.99	89.92	89.96	100.02		99.28		89.49	
2	GND		Copper foil	1oz	1.25																													
		3.7	Core	4mil	3.67										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48							
3	IN 1		Copper foil	1oz	1.28	161.77	11.4	8.8	8.6	8.7	8.8	8.7	8.5	8.3	11.4/X	5.6/3.9	5.6/3.8	4.9/4.1	4.6/3.9	3.9/3.6	3.8/3.3	3.7/4.1	4.3/4.2		3.5/4.3	3.5/4.8	3.3/4.8	3.7/5.7		3/6.5	L2/L4	9.5/6	no Ref		
		3.7	Prepreg	2116H	4.3		24.92	34.99	39.12	42.94	44.9	48.22	49.45	51.84	無法做對	69.94	74.93	79.85	83.31	84.76	85.01	85.13	85.05		87.86	89.98	89.97	89.99		99.94		99.81			
4	GND/PWR		Copper foil	1oz	1.25																													
		3.7	Core	4mil	3.67										SE 25	SE 40	SE 43	SE 48		SE 50	SE 52	SE 48			SE 50	SE 50	SE 52								
5	IN 2		Copper foil	1oz	1.28	160.76	15.5	9.3	7.3	6.5	5.9	5.2	5.8	4.4	15.5/15	7.7/5	6.6/4.8	5.2/3.7	4.8/3.8	4.8/4.3	4.6/4.6	5.2/5.2			4.8/5.3	4.8/5.9	4.4/4.7			4.7/7.0	L4/L7	8.5/6	no Ref		
		3.6	Prepreg	1086H x2 or PP2116HRC	4.2		24.88	34.96	39.08	42.88	45.09	48.01	49.87	51.68	49.1	70.2	75.38	80.01	83.17	85.27	85.09	85.35			86.35	90.32	89.95			100.28		100.68			
6	IN 3		Copper foil	1oz	1.25		15.8	9.2	7.7	6.5	5.9	5.2	4.8	4.4	15.5/12	7.7/5	6.6/4.6	5.2/3.7	4.8/3.8	4.9/4.3	4.4/3.8	5.2/5.2			4.8/5.2	4.8/5.9	4.4/4.7			4.7/6.9	L4/L7	8.5/6	no Ref		
		3.7	Core	4mil	3.67																													
7	GND/PWR		Copper foil	1oz	1.25																													
		3.8	Prepreg	2116H	4.3										SE 25	SE 40	SE 43	SE 46		SE 50	SE 52	SE 48	SE 46		SE 50	SE 50	SE 52	SE 48							
8	IN 4		Copper foil	1oz	1.23		11.4	8.8	8.6	8.7	8.8	8.7	8.5	8.3	11.4/X	5.6/3.9	4.8/3.8	4.9/4.1	4.6/3.9	3.9/3.6	3.8/3.3	3.7/4.1	4.3/4.2		3.5/4.3	3.5/4.8	3.3/4.8	3.7/5.7		3/6.5	L7/L9	9.5/6	no Ref		
		3.7	Core	4mil	3.67		24.92	34.99	39.12	42.94	44.9	48.22	49.45	51.84	無法做對	69.94	74.93	79.85	83.31	84.76	85.01	85.13	85.05		87.88	89.98	89.97	89.99		99.94		99.94			
9	GND		Copper foil	1oz	1.25																													
		3.8	Prepreg	1080	3.5																													
10	Bottom		Copper foil	0.5oz+plating	1.6		13.4	8	6.8	5.5	5	4.3	4	3.7	13.5/X	6.8/5.2	5.5/4.5	4.4/3.7	3.9/3.5	4/4.1	3.7/3.6				4/5	4/5.7	3.7/4.7	3/3.3	3.5/4.5	3.5/5.3	L9	9/8.5	no Ref		
			Add Plating				24.98	34.95	39.05	43.06	45.2	48.08	50.23	52	無法做對	69.98	75	79.85	82.85	84.88	85.11				88.12	90.04	89.99	89.92	89.96	100.02		99.75			
			SolderMask	IT-158	0.5																													
Overall Thickness (1.2mm ± 10%)					47.68900																													
					1.211072																													

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Title: Stack-up

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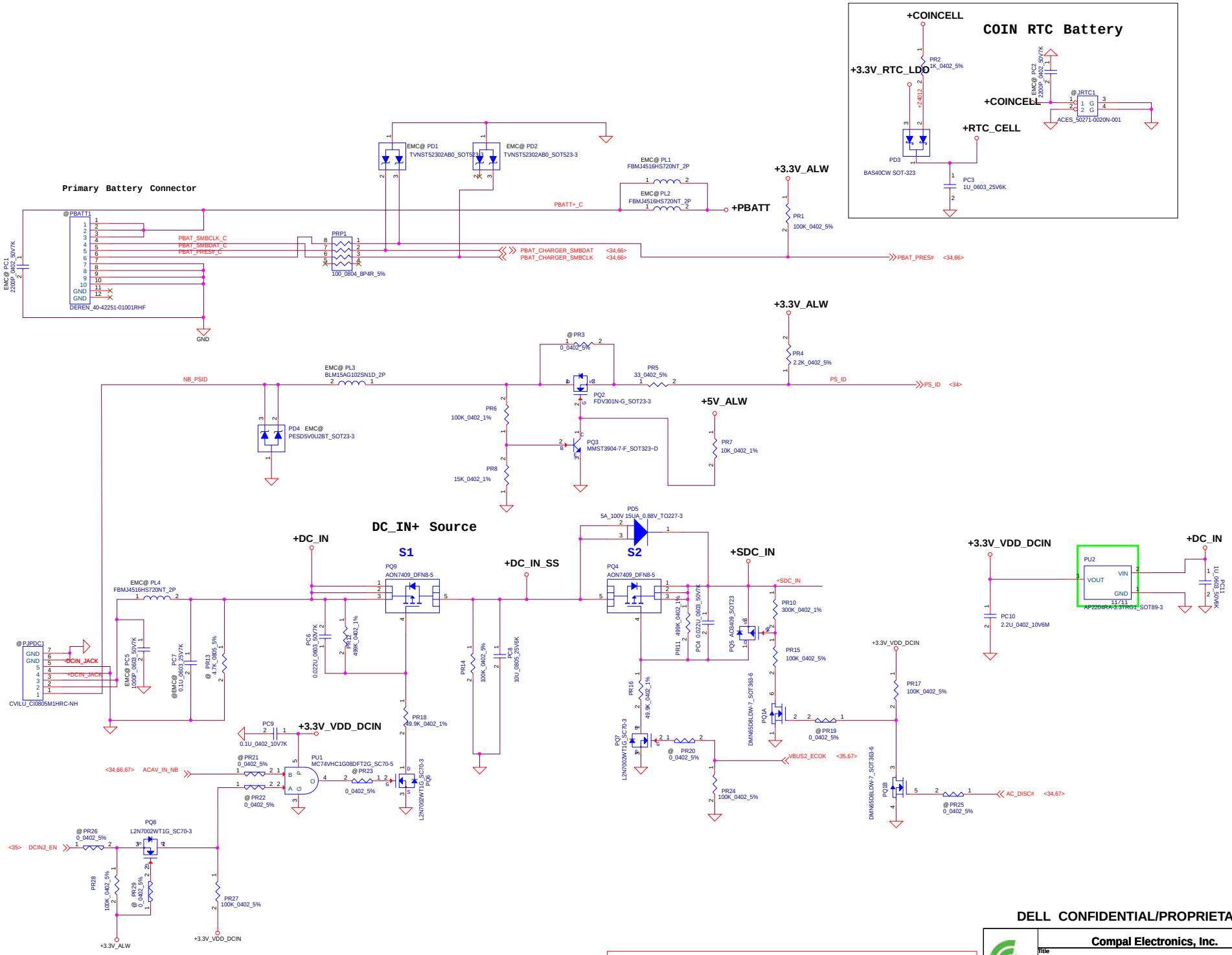

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Title: +DCIN		
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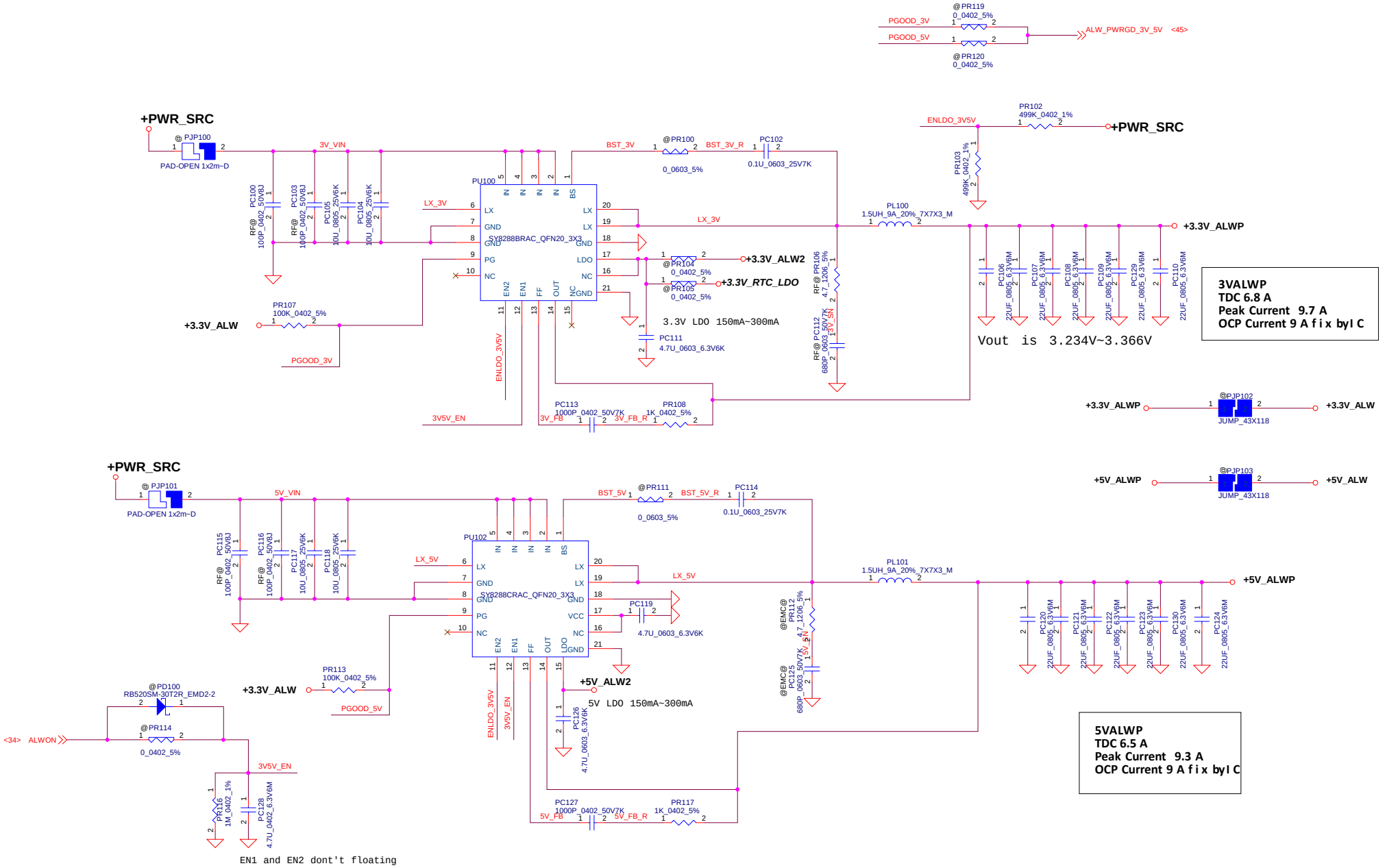

Compal Electronics, Inc.
Title: +5V_ALW/3.3V_ALW
Size: Document Number: LA-E082P
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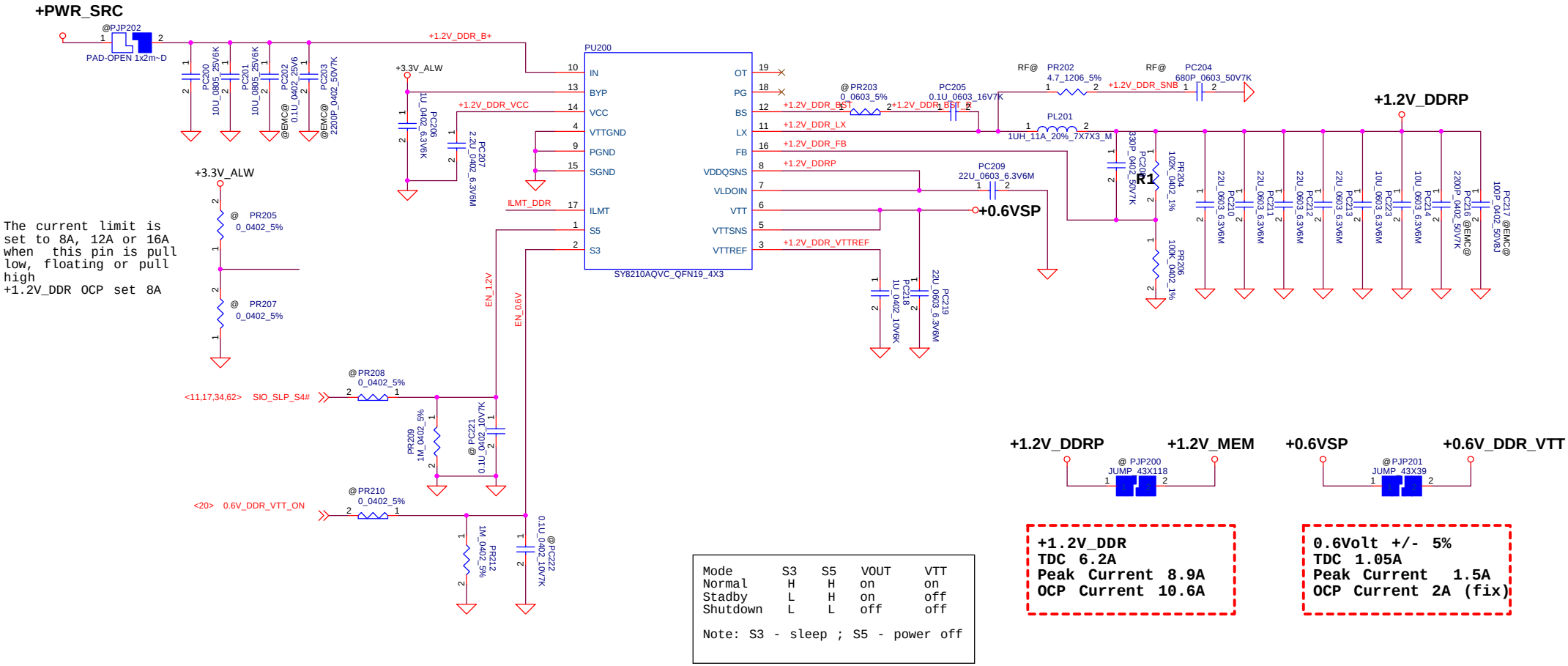

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 8A

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 6.2A
Peak Current 8.9A
OCP Current 10.6A

0.6Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 2A (fix)

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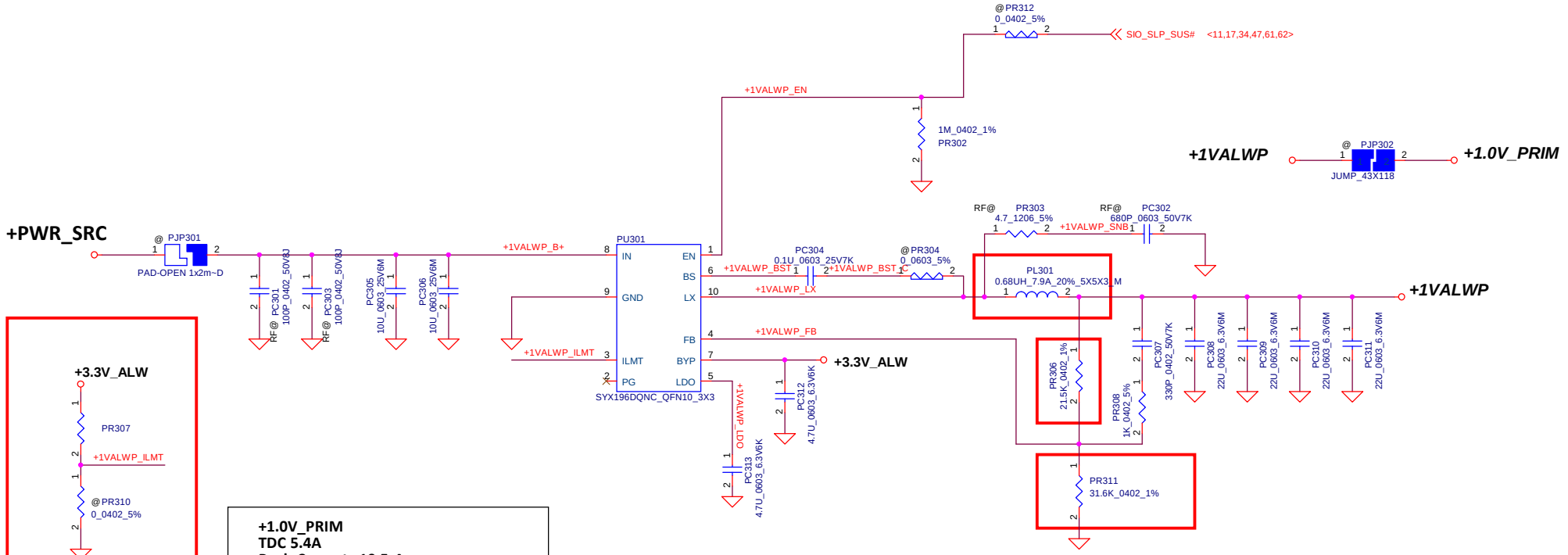
Title: +1.2V_MEN/+0.6V_DDR_VTT

Size | Document Number: LA-E082P | Rev: 0.1

Date: Monday, December 12, 2016 | Sheet 59 of 71



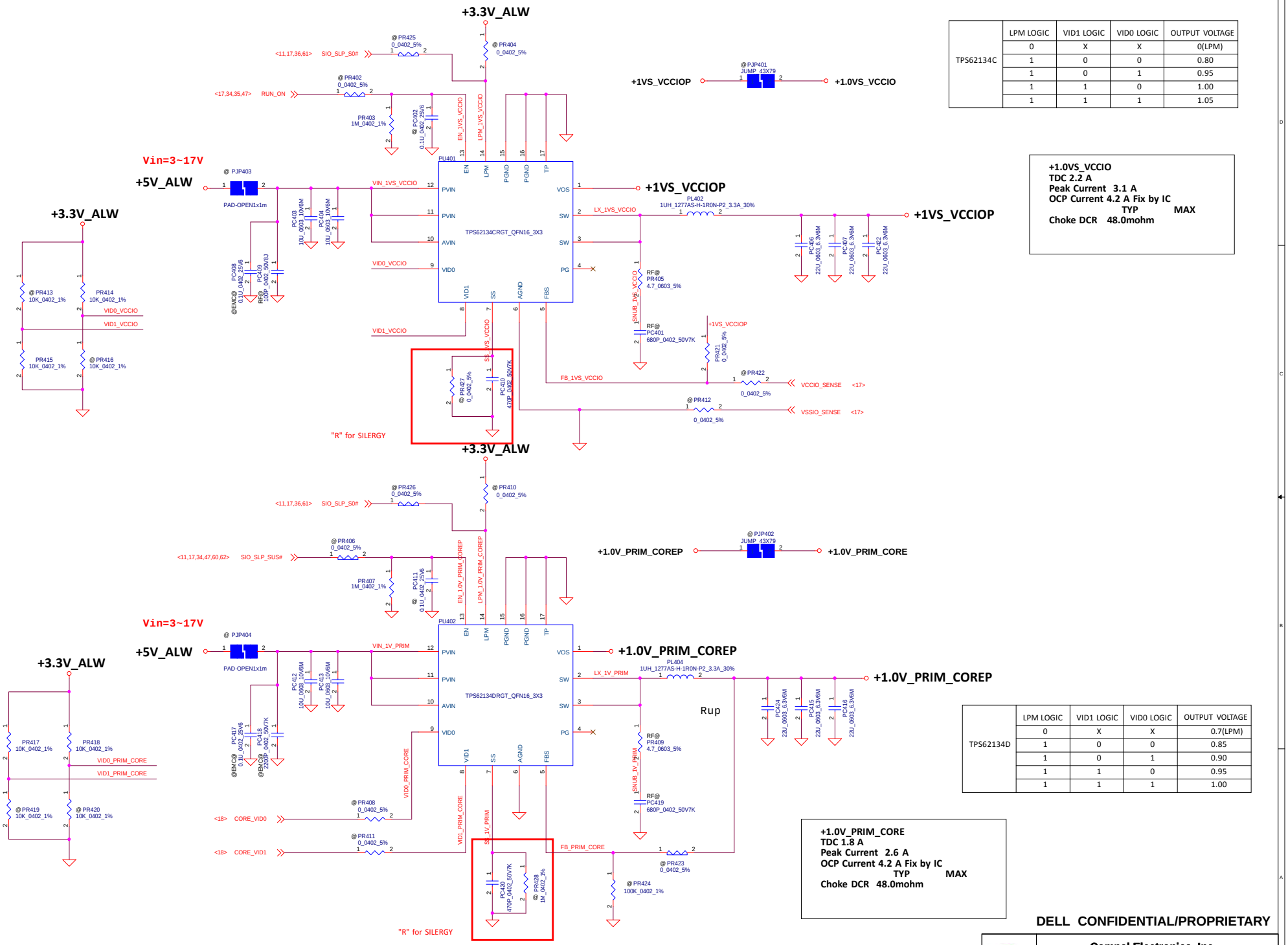
+1.0V_PRIM
TDC 5.4A
Peak Current 10.5 A
OCP 12.6A
OCP Current 9 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

Compal Electronics, Inc.

Title	+1VALWP	
Size	Document Number LA-E082P	Rev 0.1
Date: Monday, December 12, 2016	Sheet 60 of 71	



TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 2.2 A
Peak Current 3.1 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

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Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

Size: | Document Number: LA-E082P | Rev: 0.1

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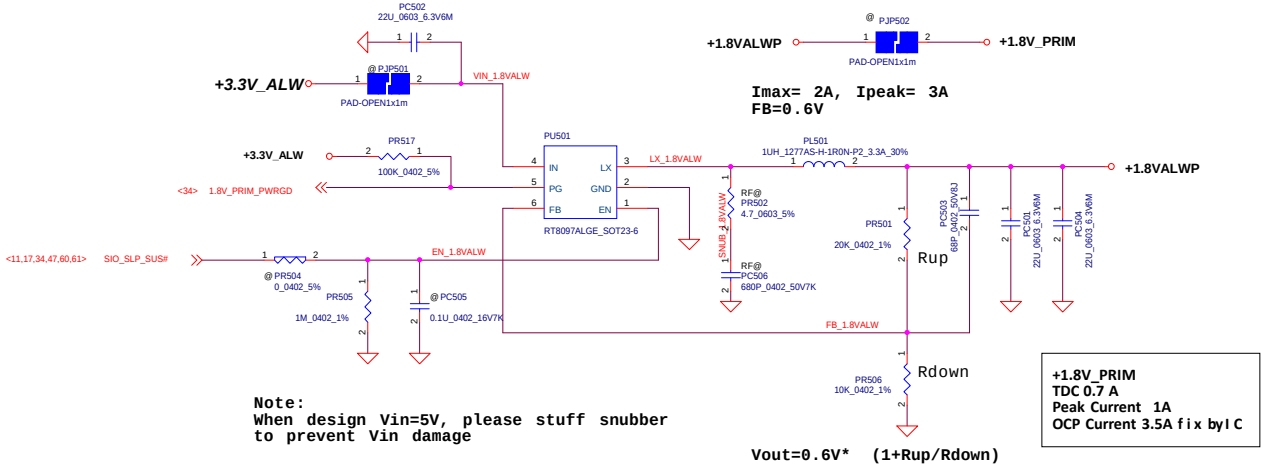
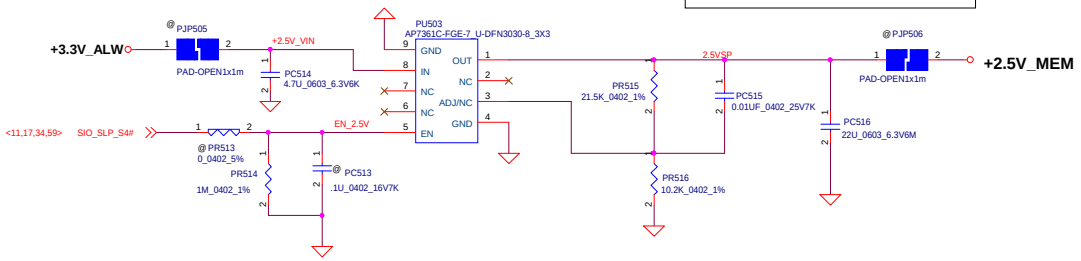


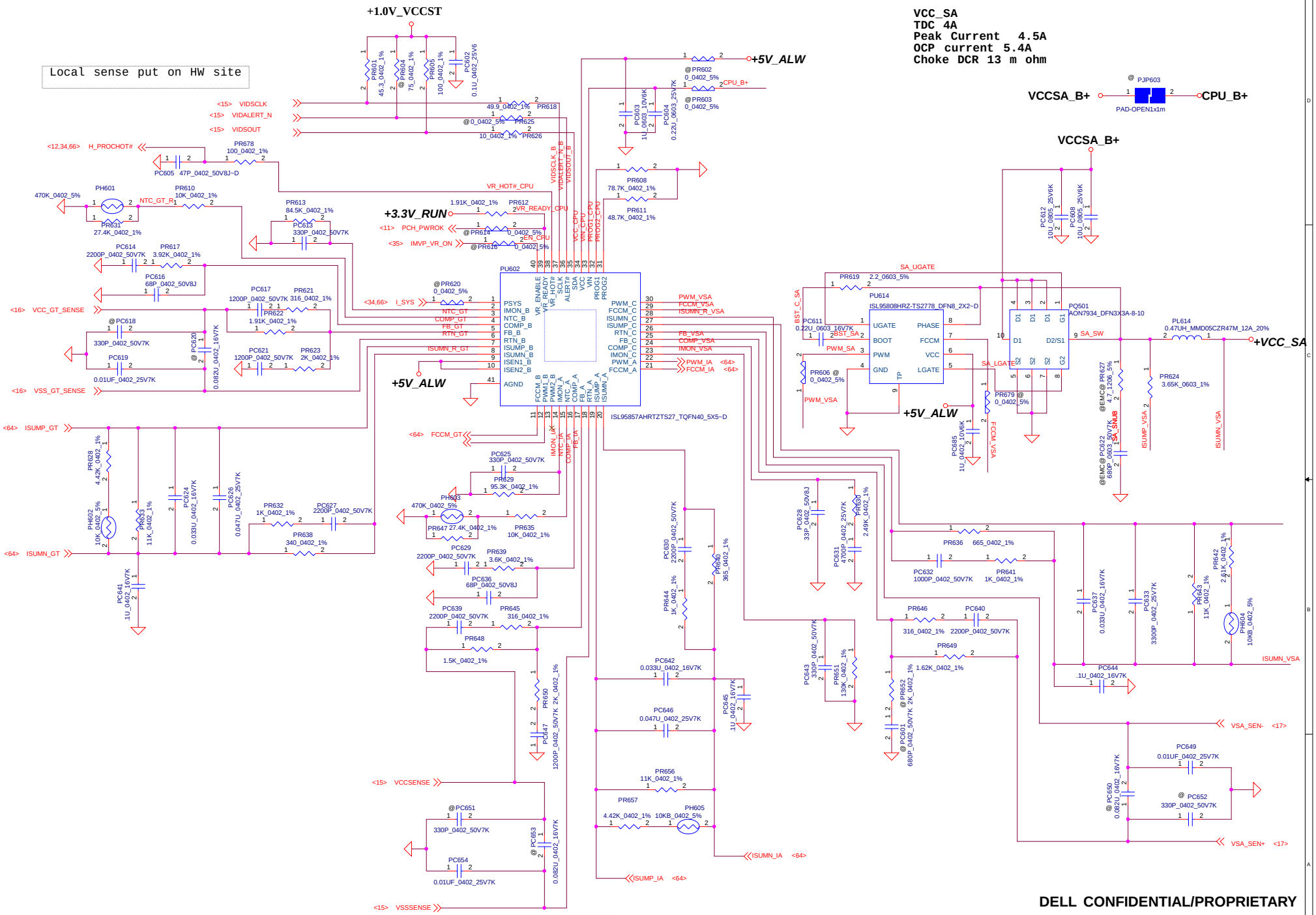


Compal Electronics, Inc.

Title: +1.8VALWP/+2.5VSP

Size | Document Number: LA-E082P | Rev: 0.1

Date: Monday, December 12, 2016 | Sheet 62 of 71


+1.0V_VCCST
Local sense put on HW site
VCC_SA
TDC 4A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm
VCCSA_B+
CPU_B+
PJP603
PAD-OPEN1x1m
+5V_ALW
+3.3V_RUN
+VCC_SA
PU602
ISL95857AHRTZTS27_TQFN40_5X5~D
PU614
ISL95808HRZ-TS2778_DFN8_2X2~D
PQ501
AON7934_DFN3X3A-8-10
PL614
0.47UH_MMD05CZR47M_12A_20%
PH601
PH602
PH603
PH604
PH605
Local sense put on HW site
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Compal Electronics, Inc.
VCCSA_ISL95857
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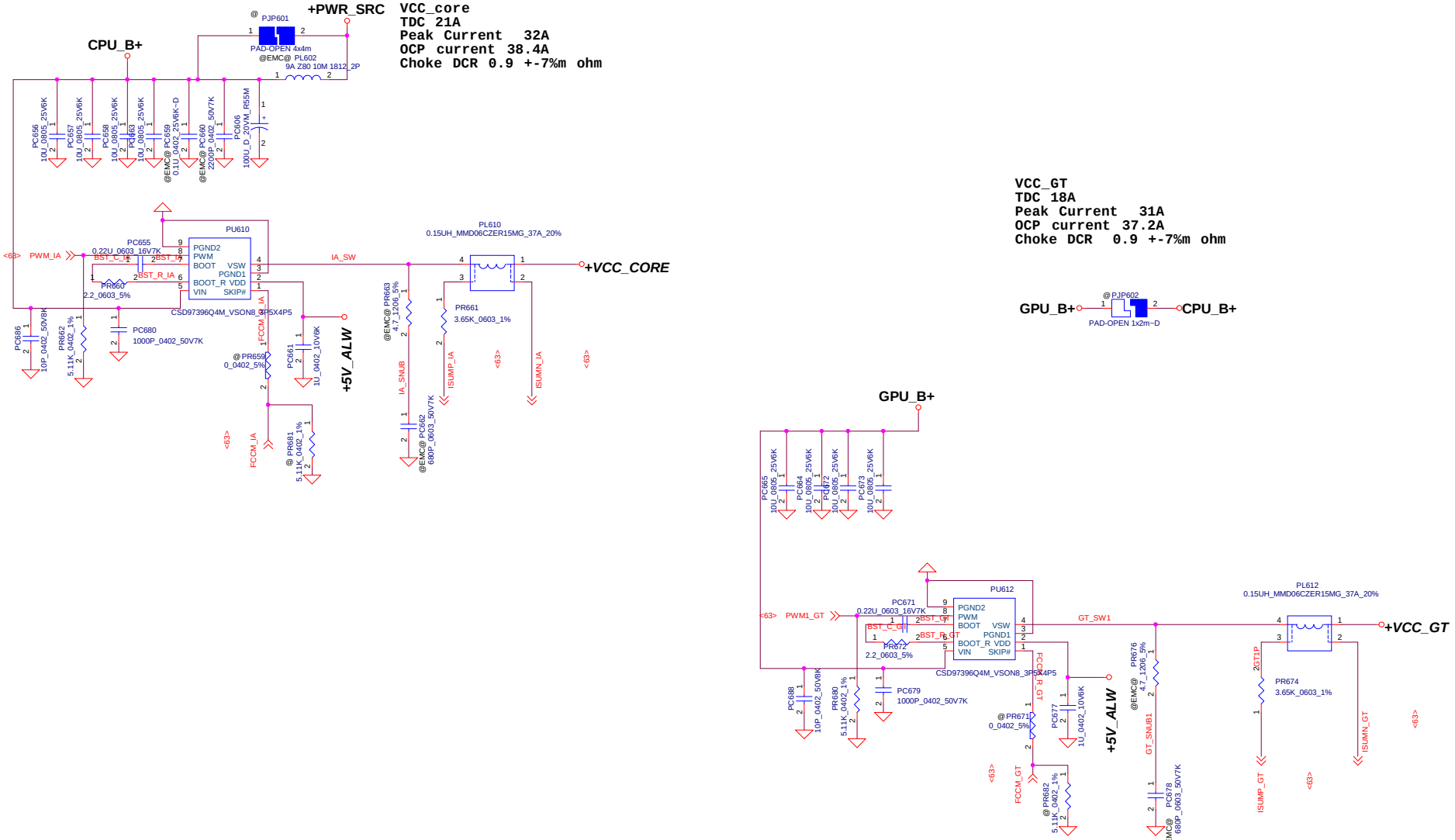

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Compal Electronics, Inc.

Title: VCC_CORE/GT_ISL95857

Size | Document Number: LA-E082P | Rev: 0.1

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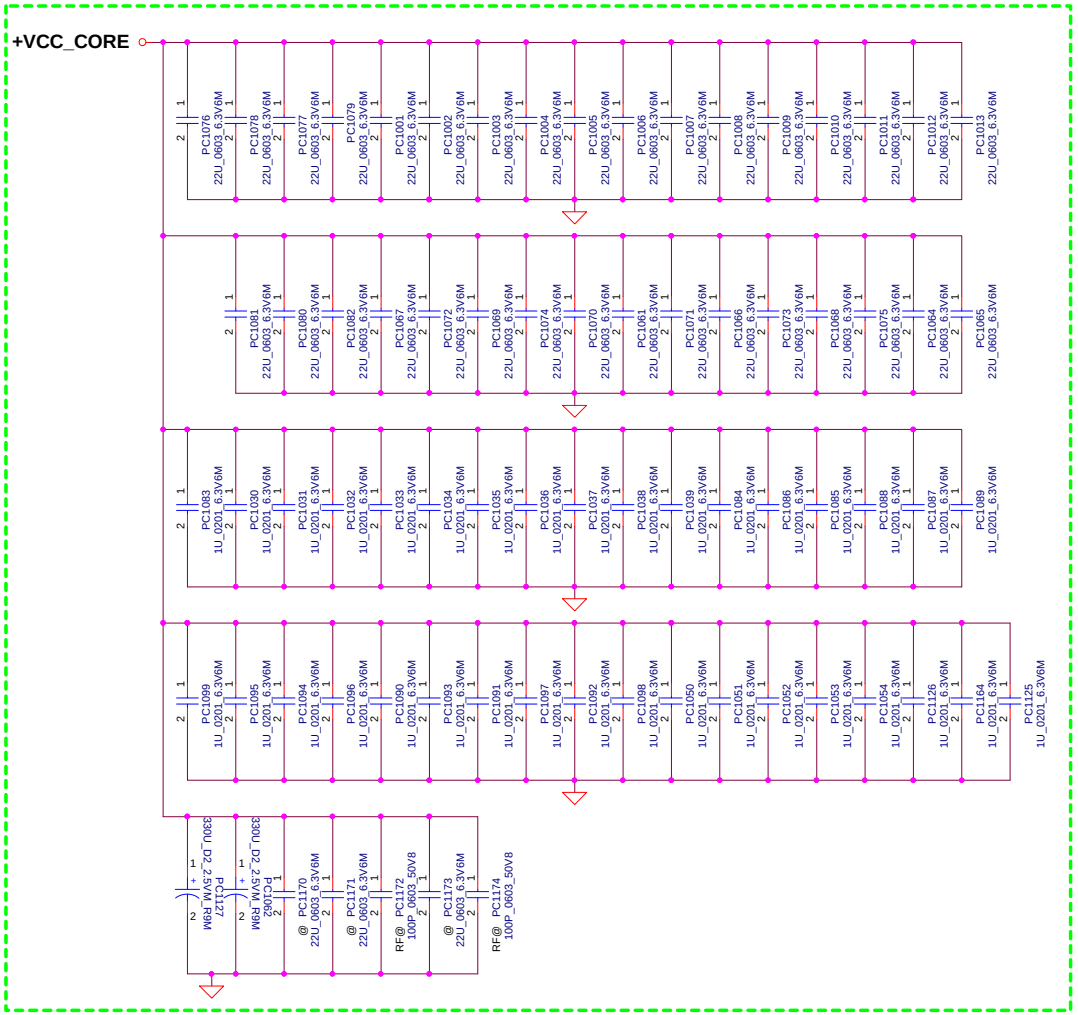
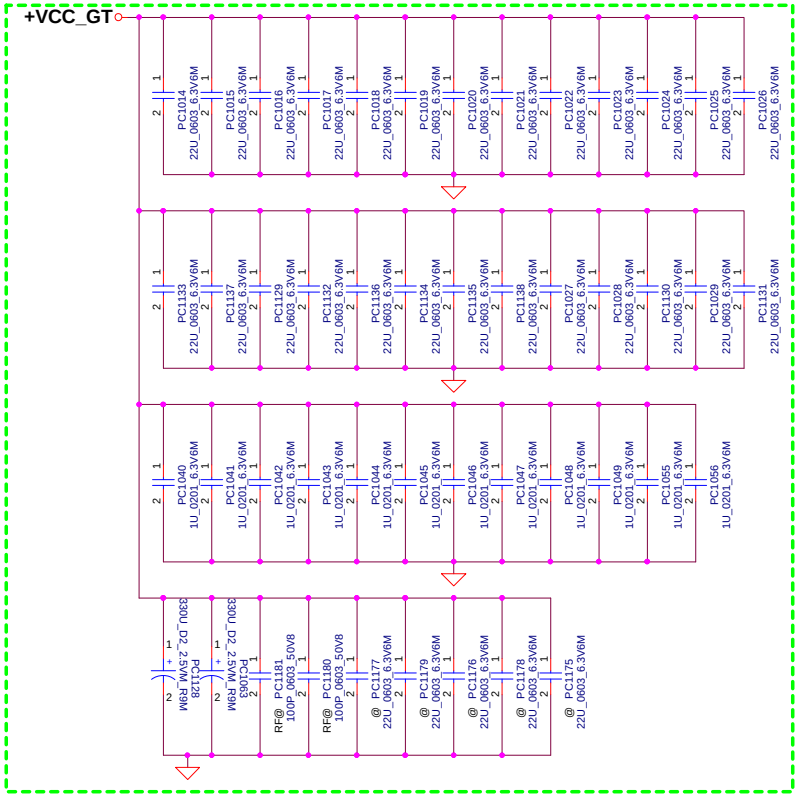
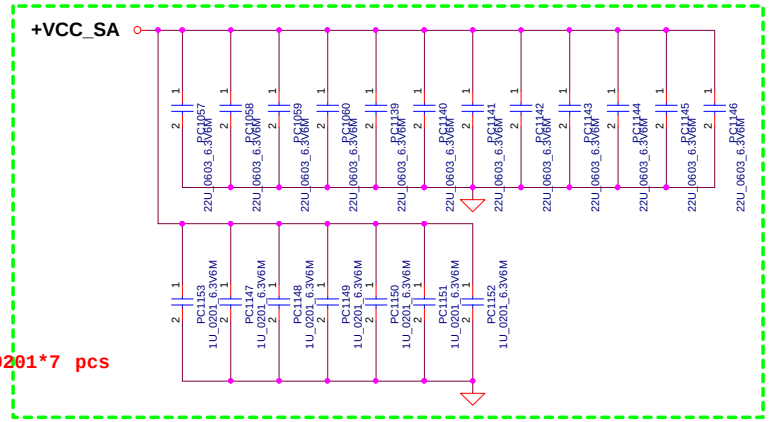
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs



VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs





VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs

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Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

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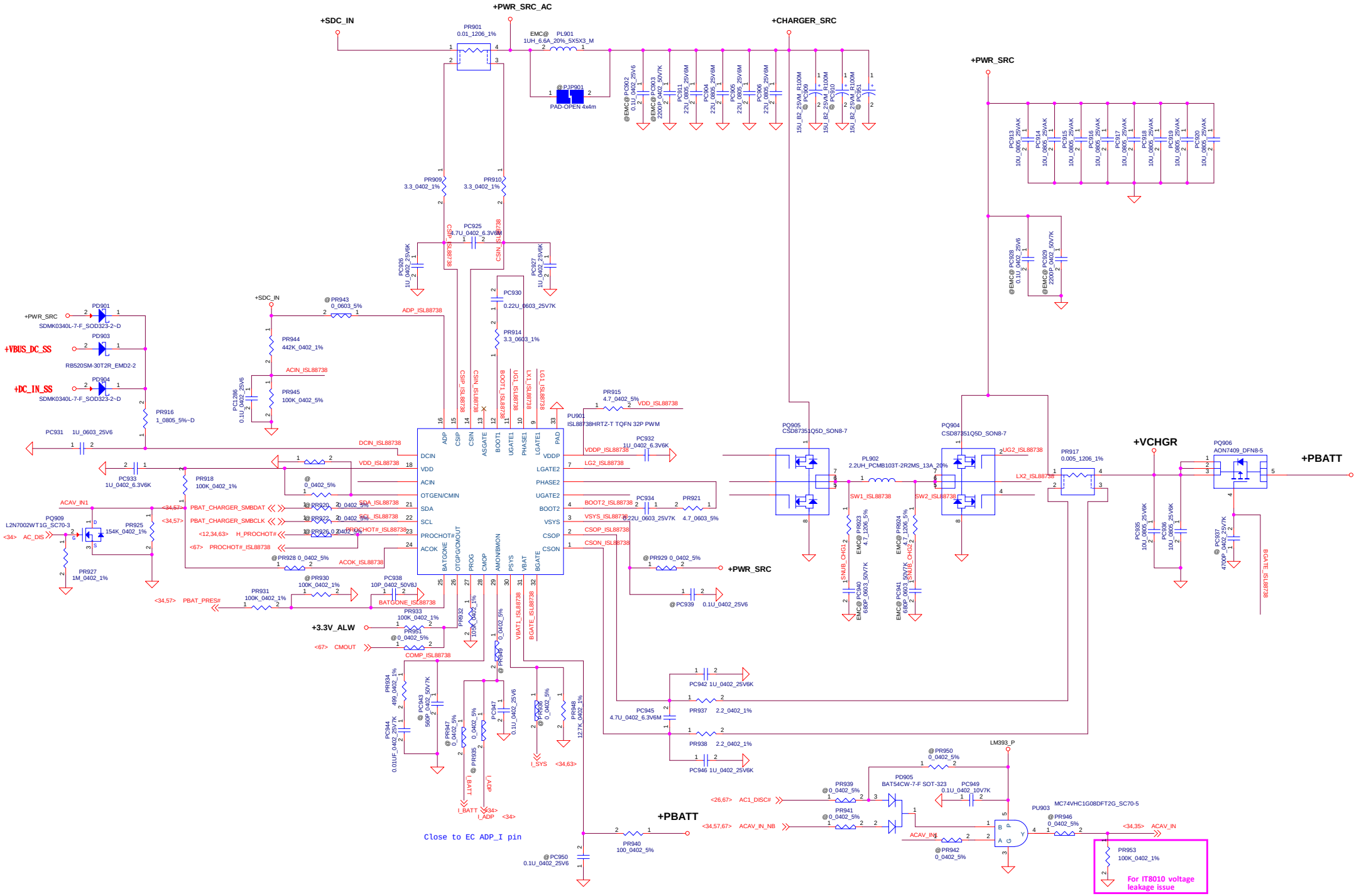


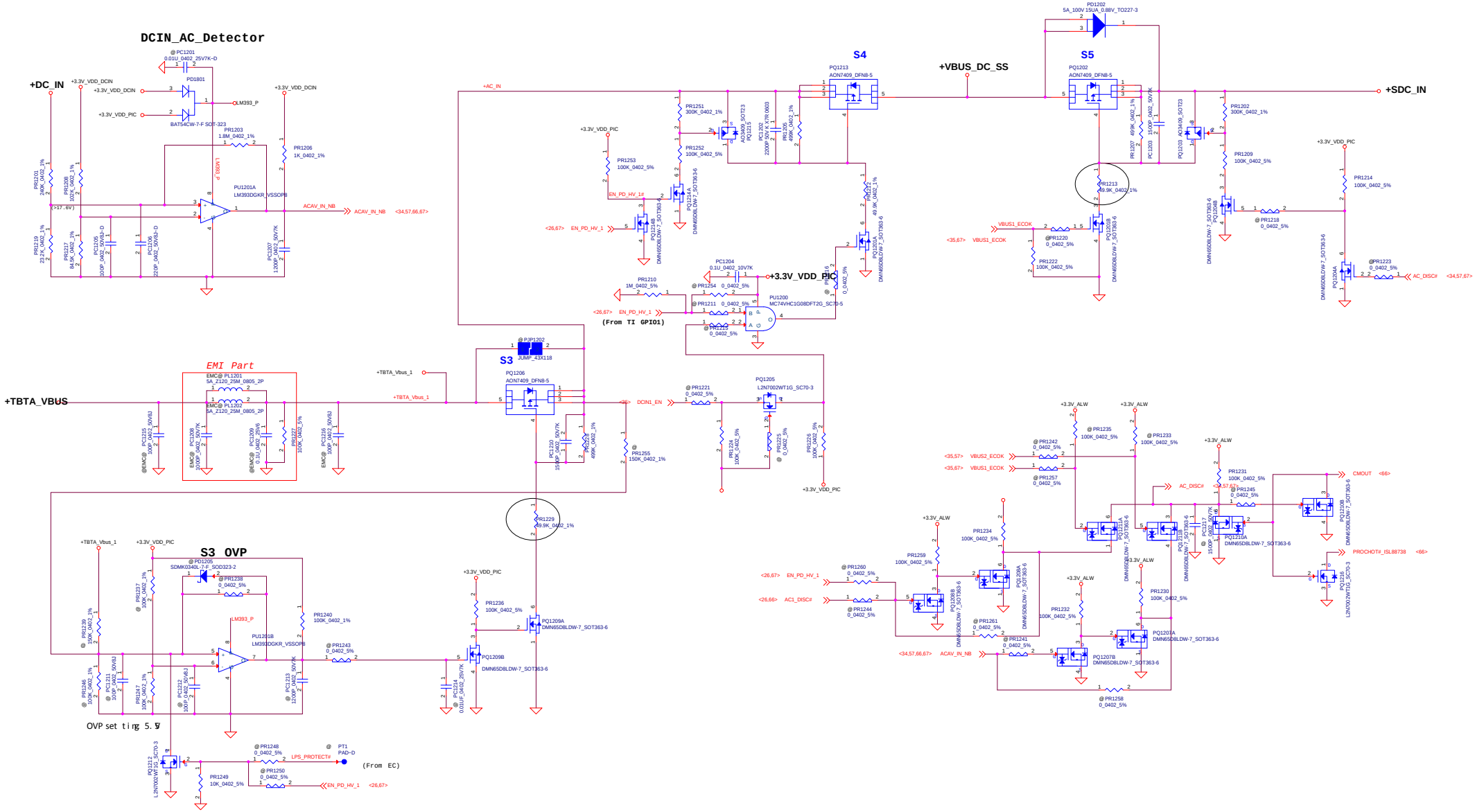
Security Classification	Compal Secret Data		
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.

Title: CHARGE

Size	Document Number	Rev
	LA-E082P	0.1

Date: Monday, December 12, 2016 | Sheet 66 of 71



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Compal Electronics, Inc.	
Title	ParkCity_TypeC_PD
Size / Document Number	LA-E082P
Rev	0.1
Date: Monday, December 12, 2016	Sheet 67 of 71

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(6-0.9)*0.9/
(287Khz*0.22u*6)=12.12A

OCP=47.4A/2=23.7A per_phase
Ivalley=23.7A-12.12A/2=17.64A

H-side MOS:CSD87351 Rds(on):
8.8m ohm(max)@Vgs=4.5V

L-side MOS:CSD87351 Rds(on):
3.1m ohm(max)@Vgs=4.5V

Choke: 0.22uH (Size:7*7*3)
Rdc=0.98mohm +-5%
Heat Rating Current=28A
Saturation Current=28A

C=1*330uF (6mohm)=330uF
Vripple=Iripple*ESR(min)=12.79A*6mohm=76.74mV

VGA Chip	N16S-GMR-S
OpenVReg Configurations	Config B
Rated TDP Power at Tj=102C	18W
Boosted GPU Total at Tj=102C	23W
EDP-Continuous at Tj=102C	21A
EDP-Peak at Tj=102C	39.5A
Istep max (Evaluation)	28A
OCP Setting Current	47.4A
Rocset	9.76K
Recommendation	2phase
Polymer Cap (330uF)	6mohm * 1

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of Voltage level		96	96	20
Rrefadj	PR1307	39K	20K	39K
Rref1	PR1308	39K	20K	30K
Rboot	PR1305	1.5K	2K	3K
Rref2=PR10+PR12	PR1309	30K	18K	24K
	PR1310	1.5K	0	3K
C	PC1308	1.5nf	2.7nf	1.8nf

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

PSI Pull high on HW side

Pull high on HW side

Reserve Location

+VGA_CORE
EDP-Continuous 21 A
EDP-Peak 39.5 A
OCP 47.4A

1. VSNS Soft-Start time (Internal) is 0.7ms (PC1315 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms (PC1315 pop)

2. Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)
=301.5Khz(Vin=13.5V)

3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PR620=VTSNS/Rth

	T_min	T_typical	T_max
PR1318=18.7K	86.73C	100C	103.1C
PR1318=13K	106.38C	110C	113.4C

Compal Electronics, Inc.
Title: +GPU_CORE
Size: Document Number: LA-E082P
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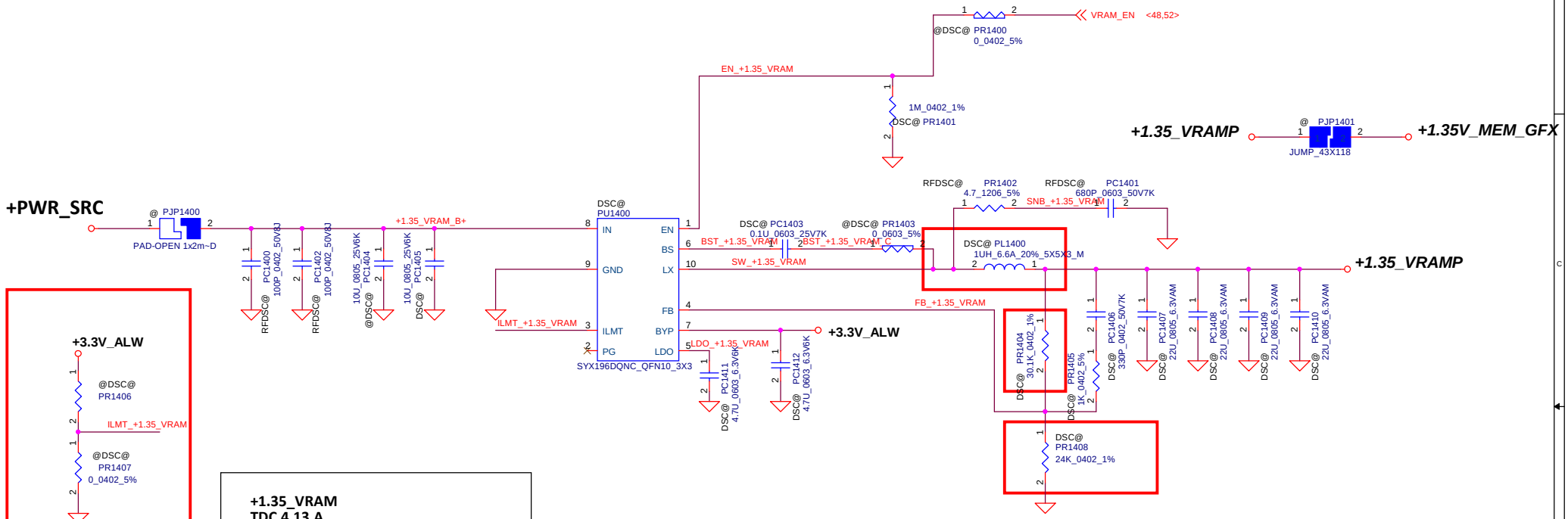

+1.35_VRAM
TDC 4.13 A
Peak Current 5.9 A
OCP Current 9 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

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Title	GPU_VRAM(SYX198D)	
Size	Document Number LA-E082P	Rev 0.1
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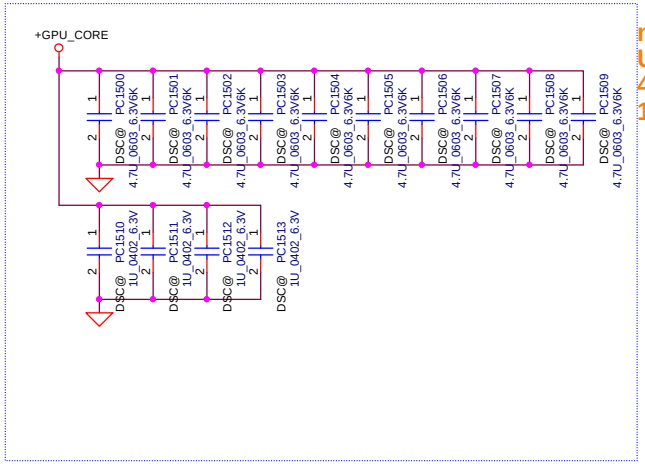
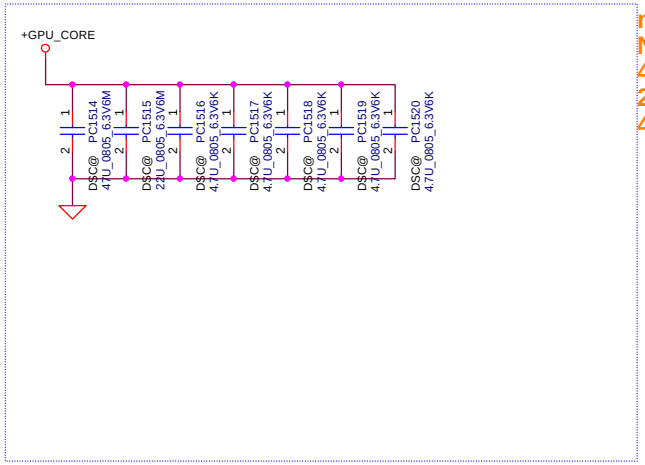


nVidia GB4-64 package
Under GPU
4.7uF 0603 * 10
1uF 0402 * 4



nVidia GB4-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

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Compal Electronics, Inc.

Title	PROCESSOR DECOUPLING	
Size	Document Number LA-E082P	Rev 0.1
Date: Monday, December 12, 2016	Sheet 70 of 71	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	67	1Type-C PD Selector	2016 05/20	Compal	Change the S4 fast turn off circuit to avoid the leakage.	Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN.	X01
2	66	CHARGER	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Add PR960 0_0402_5%(SD028000080) and depop PR919 0_0402_5%(SD028000080) let the PU901.20 CMIN connect to GND. PU901.23 add cross page net PROCHOT#_ISL88738	X01
3	67	1Type-C PD Selector	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Add PQ1216 DMN65D8LW-7_SOT323-3(SB00000UO00) to drive the PROCHOT# Reserve PC1217 1500P_0402_50V7K(SE074152K80)	X01
4	67	1Type-C PD Selector	2016 06/13	Compal	For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V	PR1219 change from 22.6K to 23.2K(SD034232280)	X01
5	63~64	VCCSA_ISL95857 VCC_CORE/ GT_ISL95857	2016 06/13	Compal	location alignment	IA_CORE change location PU603 to PU610, PL603 to PL610 GT_CORE change location PU604 to PU612, PL604 to PL612 SA_CORE change location PU606 to PU614, PL601 to PL614	X01
6	66	CHARGER	2016 06/13	Compal	To decrease the charger input leakage voltage for TypeC AC.	PD903 change from SDMK0340L-7-F_SOD323-2~D(SCS0340L010) to RB520SM-30T2R_EMD2-2(SCS00006C00)	X01
7	57 67	+DCIN 1Type-C PD Selector	2016 06/20	Compal	To solve the MOS leakage problem to avoid the error active.	PR12, PR11, PR1205, PR1207, PR1228 change from 1M_0402_5%(SD028100480) to 499K_0402_1%(SD034499380) PR16, PR18, PR1212, PR1213, PR1229 change from 1M_0402_5%(SD028100480) to 49.9K_0402_1%(SD034499280) PR10, PR1251 and PR1202 change from 100K_0402_5%(SD028100380) to 300K_0402_1%(SD034300380)	X01
8	63	VCCSA_ISL95857	2016 06/22	Compal	IA/GT/SA CORE static LL optimization	PC621, PC647 change from 680P(SE074681K80) to 1200P(SE074122K80) PR640 change from 383_0402_1%(SD034383080) to 365_0402_1%(SD034365080) PR638 change from 374_0402_1%(SD034374080) to 340_0402_1%(SD00000KT80) PR629 change from 93.1K_0402_1%(SD034931280) to 95.3K_0402_1% (SD034953280)	X01
9	66	CHARGER	2016 06/27	Compal	EMI request	PR921 change from 2.2_0603_5%(SD013220B80) to 4.7_0603_5%(SD013470B80) PR914 change from 0_0603_5%(SD013000080) to 3.3_0603_1%(SD014330B80) pop PR923, PR924 4.7_1206_5%(SD001470B80) pop PC940, PC941 680P_0603_50V7K(SE025681K80)	X01
10	58~61 68~69	+5V/+3.3V +1.2V_MEN +0.6V_DDR 1VALWP/VCCIO_PRIM GPU_COREP/GPU_VRAM	2016 06/28	Compal	RF request	pop PC100, PC103, PC115, PC116, PC301, PC303, PC409, PC1400, PC1402 100P_0402_50V8J(SE071101J80) pop PC1320, PC1312, PC204, PC302, PC112 680P_0603_50V7K(SE025681K80) pop PR1319, PR1311, PR202, PR303, PR106 4.7_1206_5%(SD000010280)	X01
11	66	CHARGER	2016 07/01	Compal	Reserve the OVP function to protect the typeC device.	Depop PJP1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212 , PD1205, PC1213, PC1214, PR1248 Change PR1247 from 200K_0402_1%(SD034200380) to 100K_0402_1%(SD034100380) Re-modify the S11 OVP description to S3 OVP.	X01
12	66	CHARGER	2016 07/01	Compal	Change the charger version from A version to B version.	Change PU901 from ISL88738HRTZ REV.A-T TQFN 32P PWM(SA00009VW10) to ISL88738HRTZ REV.B-T TQFN 32P PWM(SA00009VW20)	X01
13	66	CHARGER	2016 09/02	Compal	For IT8010 voltage leakage issue	Add PR953 100K_0402_1%(SD034100380)	X03
14	63	+VCCSA_ISL95857	2016 09/21	Compal	Change CPU core version to MP version.	Change PU602 from SA0000A4A00 to SA0000A4A0L	X03
15	61	VCCIO/PRIM	2016 09/29	Compal	PCH LPM function	Unpop PR410 0_0402_5%(SD028000080) Pop PR426 0_0402_5%(SD028000080)	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	HW	2016/05/24	COMPAL	For Schematic align	Remove RA2	0.2(X01)
2	35	HW	2016/05/24	COMPAL	Symbol pin name change	UE1.C1 pin name change to GPIO024/nRESETI	0.2(X01)
3	9	HW	2016/05/24	COMPAL	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)
4	25	HW	2016/05/24	COMPAL	Symbol pin name change	UT9.20 pin name change to SNK_CAD/DCI_DAT, UT9.32 pin name change to HPDIN/DCI_CLK	0.2(X01)
5	6	HW	2016/05/24	COMPAL	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
6	25	HW	2016/05/24	COMPAL	Disable AUX snoop feature	Pop RT308	0.2(X01)
7	33,40	HW	2016/05/24	COMPAL	Remove HDD LED MUX feature	Depop RN100/RN101	0.2(X01)
8	35	HW	2016/05/24	COMPAL	PORT80_DET#	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
9	6	HW	2016/05/24	COMPAL	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182 Add test point T281/T282 for CPU_DP1_AUXN and CPU_DP1_AUXP	0.2(X01)
10	17	HW	2016/05/24	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
11	46						0.2(X01)
12	43,46					1.add CLIP1	0.2(X01)
13	25	HW	2016/05/27	COMPAL	For Schematic align	SW2_DP1_HPD Add RT380 place near TUSB546	0.2(X01)
14	30	HW	2016/06/01	INTEL	Intel reviwe result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
15	37,38	HW	2016/06/07	DELL	change to Nuvoton TPM form ATMEL TPM	Delete ATMEL TPM circuit, Add Nuvoton TPM circuit	0.2(X01)
16	12	HW	2016/06/07	INTEL	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
17	33	HW	2016/06/07	INTEL	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
18	33	HW	2016/06/07	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
19	35	HW	2016/06/07	COMPAL	For MEC5105K-D1-TN sample	1.UE1 change to SA00009GL00(S IC MEC5105K-D1-TN WFBGA 169P EC) 2.Depop RE361,Pop RE360,RE362	0.2(X01)
20	46	HW	2016/06/17	COMPAL	Base on ME drawing	H10 change from H_4P0 to H_3P0	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	42	HW	2016/06/17	COMPAL	Base on USB3 EA result,B_EQ change to13dB	Depop RI42,pop RI44	0.2(X01)
22	11	HW	2016/06/17	COMPAL	Base on Crystal EA result	CC23 change form 15pF to 12pF	0.2(X01)
23	41	HW	2016/06/17	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	Depop RN5	0.2(X01)
24	38,45	HW	2016/06/20	COMPAL	ME request	1.JKBTP1 change from HRS_TF49-20S-0P5SH_20P-T to CVILU_CF5020FD0RK-05-NH_20P-T 2.JUSH1 change from HRS_TF49-26S-0P5SH_26P-T to CVILU_CF5026FD0RK-05-NH_26P-T	0.2(X01)
25	34	HW	2016/06/20	COMPAL	Base on Audio EA result	RA7,RA8 change from 24.9 to 16.2 ohm(SD00001U900)	0.2(X01)
26	30	HW	2016/06/22	COMPAL	EMI request	CL22 change from 1500pF to 10pF (SE167100J80 S CER CAP 10P 3KV J NPO 1808 AC250V X2Y3)	0.2(X01)
27	29	HW	2016/06/22	COMPAL	EMI request	Change LV1 from SM01000BV00 to SM01000NY00	0.2(X01)
28	29	HW	2016/06/22	COMPAL	ME request	JIR1 change from SP010023D00 to SP010013W20	0.2(X01)
29	35	HW	2016/06/22	DELL	The posibility of GPIO map update,RTCRST_ON change from GPIO141 to GPIO122	Add RE514(@),RE515 for RTCRST_ON	0.2(X01)
30	36						0.2(X01)
31	29	HW	2016/06/22	COMPAL	RF request	CA7、CZ1 change to 100pF(0201)SE174101J80	0.2(X01)
32	12	HW	2016/06/22	COMPAL	BIOS need detect Storage type and dynamic change the name	UE1.D7 add HDD_DET#	0.2(X01)
33	24	HW	2016/06/28	COMPAL	For VGA test result	Pop RV121/RV122/CV132/CV133	0.2(X01)
34	46	HW	2016/06/28	COMPAL	For DFX request	CLIP1.1 change from GND to NC	0.2(X01)
35	38	HW	2016/06/29	COMPAL	X8 have no difference JUSH1 pin define concern	Depop DZ7,Pop RZ87	0.2(X01)
36	38	HW	2016/06/29	COMPAL	Let USH_PWR_STATE# keep low at S5	RZ10 change from 1M to 100k ohm	0.2(X01)
37	36	HW	2016/06/29	COMPAL	Foe X01 Board ID	RE79 change from 240k to 130k ohm	0.2(X01)
38	41	HW	2016/06/29	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)
39	29	HW	2016/08/04	COMPAL	RF request	POP CC27 & change value from 22p to 47p	0.3(X02)
39	18	HW	2016/08/04	COMPAL	DSC BOM change	Pop RC385, Depop RC386	0.3(X02)

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40	34, 35	HW	2016/08/04	COMPAL	Vendor schematic review	1. Add net WRST# to UE2.4 and CE500 1uf (SE000000K80) 2. Add RE523 0 ohm for UE2 power pin soft start 3. Change RE14,RE15,RE18 from 100k ohm to 10k ohm 4. Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT 5. Change RPE12.2 to RE525 (10Kohm) for EXPANDER_GPU_SMCLK 6. Reserve CE504~CE505 for EXPANDER_GPU_SMDAT/CLK to GND.	0.3(X02)
41	14	HW	2016/08/04	COMPAL	Intel suggestion	RC137 change from 1K to 3K	0.3(X02)
42	27	HW	2016/08/04	COMPAL	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)
43	45	HW	2016/08/04	COMPAL	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
44	26	HW	2016/08/04	COMPAL	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
45	42	HW	2016/08/05	COMPAL	BITS290368-System can't be waked from S3 when connect to right USB port via USB3.0 to LAN Dongle.	USB3 repeater power rail Add RI79 0ohm to +3.3V_RUN and De-pop it. Add RI80 0ohm to +3.3V_ALW_PCH and pop it.	0.3(X02)
46	11	HW	2016/08/08	COMPAL	EMI request	add RC417 (0 ohm) for Xtak24_IN	0.3(X02)
47	42	HW	2016/08/08	COMPAL	schematic modify	1. pop RI37 2. RI79, RI80 footprint change form 0402 to 0603 3. add QI1 controlling USB3 repeater PD#	0.3(X02)
48	32, 37	HW	2016/08/09	COMPAL	DFB request	SMT concern DZ1, DZ2, DZ5, DZ6 PCB pad is too small, suggest use the symbol "RB520SM-30T2R_EMD2-2" follow PD903	0.3(X02)
49	18						0.3(X02)
50	48						0.3(X02)
51	33, 35, 48	HW	2016/08/10	COMPAL	Footprint align	DA8,DE1,DV10 follow symbol "RB520SM-30T2R_EMD2-2"	0.3(X02)
52	42	HW	2016/08/11	COMPAL	schematic modify	change USB repeater PD# enable pin to "USB_PWR_SHR_VBUS_EN"	0.3(X02)
53	35	HW	2016/08/11	COMPAL	schematic align	add power rail +3.3V_ALW_UE2 for UE2	0.3(X02)
54	42	HW	2016/08/12	COMPAL	schematic modify	delete QI1, depop RI37, add RI81 connecting "USB_PWR_SHR_VBUS_EN" & "USB3_PD#'	0.3(X02)
55	42	HW	2016/08/16	COMPAL	EA request	depop RI38, RI44, RI53, RI57 for USB3 repeater	0.3(X02)
56	9	HW	2016/09/08	COMPAL	DGPU_PWR_EN need to use BIOS solution	depop RC385,pop RC386	0.4(X03)
57	38	HW	2016/09/08	COMPAL	TPM change to NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.4(X03)
58	35	HW	2016/09/08	COMPAL	Expander I/O change from ITE8010 to MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.4(X03)
59	34	HW	2016/09/08	COMPAL	Board ID	Change RE79 to 33kohm (SD028330280)	
60	34	HW	2016/09/08	COMPAL	schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.4(X03)
61	34	HW	2016/09/08	COMPAL	EC request for power consumption	Add RE505 PU to +3.3V_ALW for LOM_CABLE_DETECT# (Reserve) Add RE532 PU to +3.3V_ALW for BCM5882_ALERT#	0.4(X03)
62	37	HW	2016/09/08	COMPAL	USH/B de-pop, pop on MB side	POP RZ8,RZ9 for USH SMBus	0.4(X03)
63	35	HW	2016/09/20	COMPAL	DELL request	Add RE536/RE537 for resistors for PCH_DPWROK circuit	0.4(X03)
64	34	HW	2016/09/20	COMPAL	WDT schematic option 2	use Option2: pop RE361 / depop RE362	0.4(X03)
65	33	HW	2016/09/20	COMPAL	EMI request	1. L6~L9 change to 80ohm bead (BLM15PD800SN1D, SM01000N000) for BR14/15 2. depop CA2, CA3 3. RA55,RA56 change location toLA15, LA16 with 33ohm bead (BLM15PX330SN1D,SM01000NA00)	0.4(X03)
66	39	HW	2016/09/20	COMPAL	NV GPU seqest	CV247 change from 3900pf t0 4700pf (SE075472K80) CV248 change form 220pf to 470pf (SE074471K80)	0.4(X03)
67	35	HW	2016/09/20	COMPAL	EMI request	RC295/RC417 change from 0 to 33 ohm	

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68	35	HW	2016/10/04	COMPAL	BITS294007 - Sometimes need to press power button twice to power on system.	CE12 change to 2.2u (SE000008880) RE33 change to 1K (SD028100180)	0.4(X03)
69	24	HW	2016/10/04	COMPAL	U-line VGA EA PASS	depop RV121/RV122	0.4(X03)
70	26	HW	2016/10/04	COMPAL	TI CC pin for ESD request	CT85,CT86 change to 470p.(SE074471k80)	0.4(X03)
71	25	HW	2016/10/04	COMPAL	BR14 OTP issue	RE77 change to 1.69K_1% (SD00000JB80)	0.4(X03)
72	35	HW	2016/10/04	COMPAL	EC watchdog reserve	add QE13,RE530,CE503	0.5(X04)
73	34	HW	2016/10/06	COMPAL	UE1.H8 to prevent EOS issue on MEC5105	Add RE539(100ohm) to CV2_ON	0.5(X04)
74	36	HW	2016/10/06	COMPAL	BOARD ID	Change RE79 to 8.2k ohm(SD028820180)	0.5(X04)
75	36	HW	2016/10/31	COMPAL	BOARD ID	Change RE79 to 4.3k ohm(SD028430180)	1.0(A00)
76	36	HW	2016/10/31	COMPAL	Change R1 to R3 for MP part	Change UL1 CP/N to SA000081G1L Change UE1 CP/N to SA00009GL30 change UV1 CP/N to SA00009S01L	1.0(A00)
77	36	HW	2016/10/31	COMPAL	For DFB request.	Close solder mask CMOS1 (-NPM) and other co-lay part	1.0(A00)
78	36	HW	2016/10/31	COMPAL	Service Mode Switch remove	Depop SW1 and RC222 and RC221 change to short pad	1.0(A00)
79	36	HW	2016/10/31	COMPAL	RE374 change BS to LPC@	RE374 change BS to LPC@	1.0(A00)
80	36	HW	2016/10/31	COMPAL	For MEC5105 rev. C	Pop RE362,RE536; Depop RE361,QE13,CE503,RE530,UE7,CE5,CE6,RE348,RE537	1.0(A00)
81	36						1.0(A00)

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