

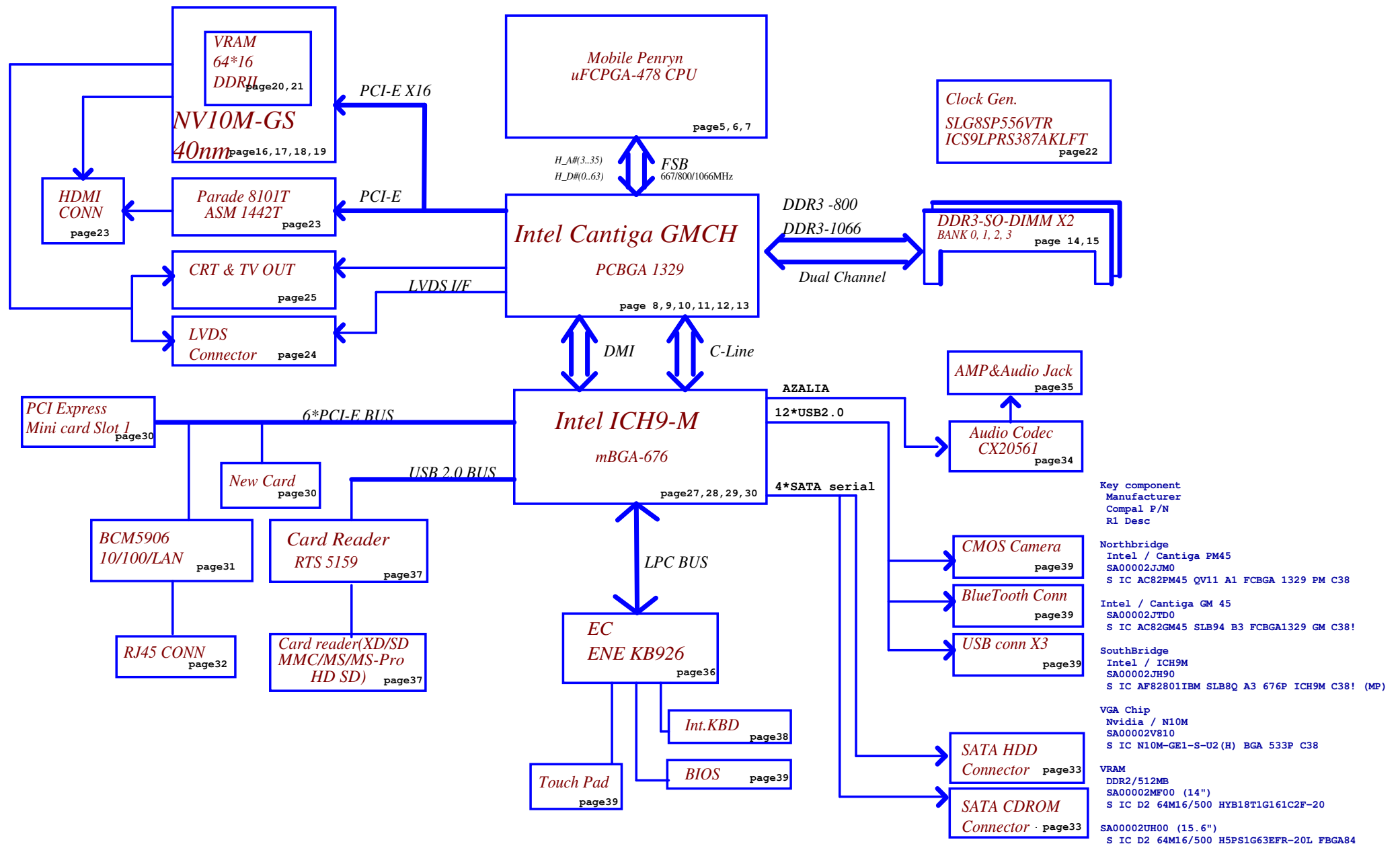
# KIWA5/A6

## Schematics Document

Mobile Penryn uFCPGA with Intel  
Cantiga\_GM/PM+ICH9-M core logic

REV:1.0

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## DDR3 Voltage Rails

power plane State	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS <b>+0.75VS</b> +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	N10M	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	N10M	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT (55nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	N10M	X	X	X	V	X	X	X	X	X	X	X	X	X
IFPC_AUX IFPC_AUX_N (40nm)	N10M	V	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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VGA and DDR2 Voltage Rails (N10M)

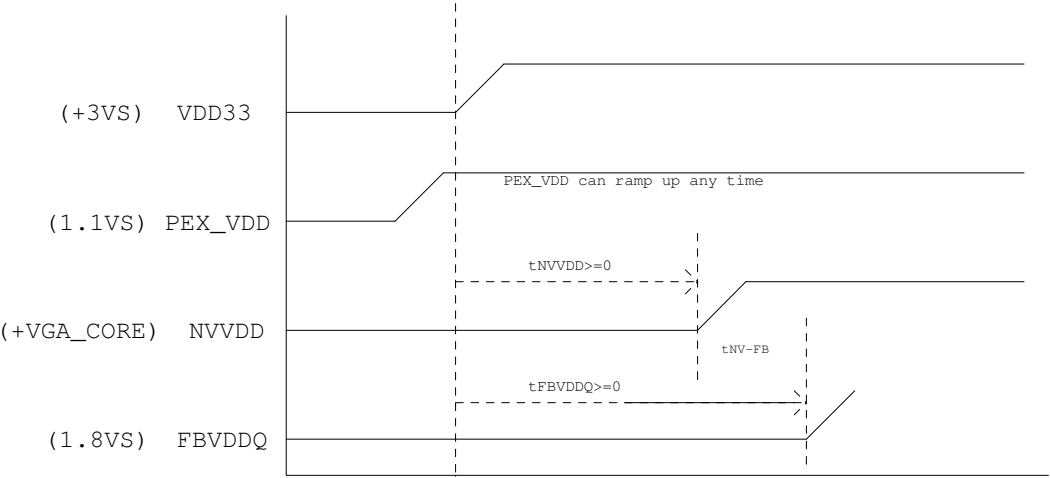
State \ power plane	+3VS +VGA_CORE +1.1VS <b>+1.8VS</b>
S0	○
S1	○
S3	✗
S5 S4/AC	✗
S5 S4/ Battery only	✗
S5 S4/AC & Battery don't exist	✗

EDP at Tj = 97C\*

Power Supply Rail		NB10M-GS		N10M-GE1-S	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

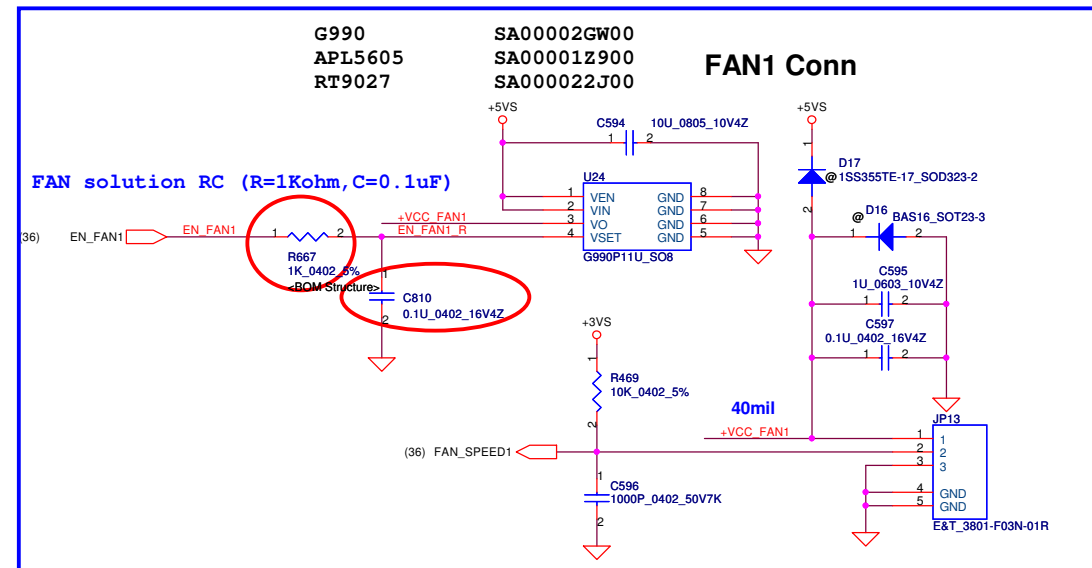
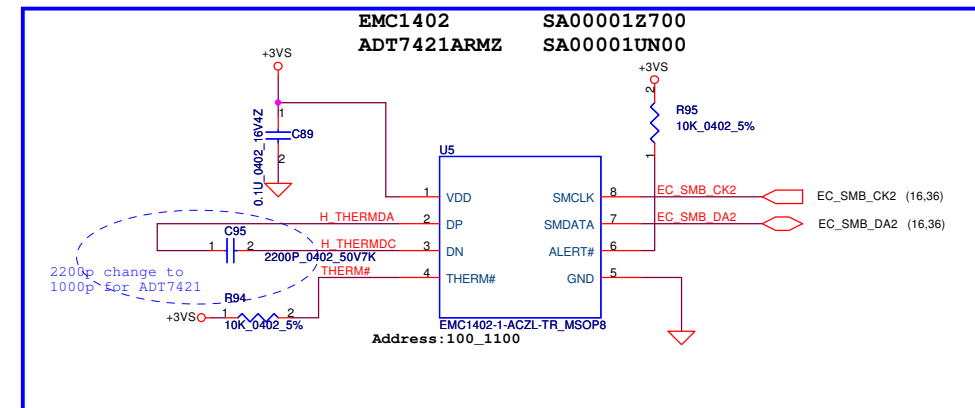
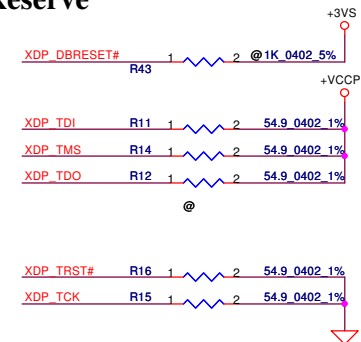
POWER SEQUENCE

The ramp time for any rail must be more than 40us



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## XDP Reserve



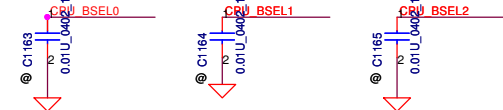
H\_THERMDA, H\_THERMDC routing together,  
Trace width / Spacing = 10 / 10 mil

RSVD pins on the CPU  
should be left as NO  
CONNECT

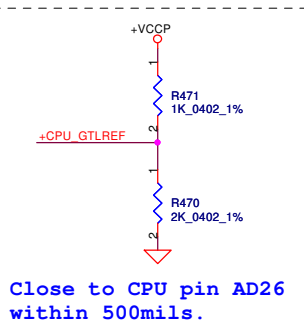
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Width=4 mil,  
Spacing: 15mil  
(55Ohms)

Trace Close CPU < 0.5"



Layout note: Z0=55 ohm  
0.5" max for GTLREF.

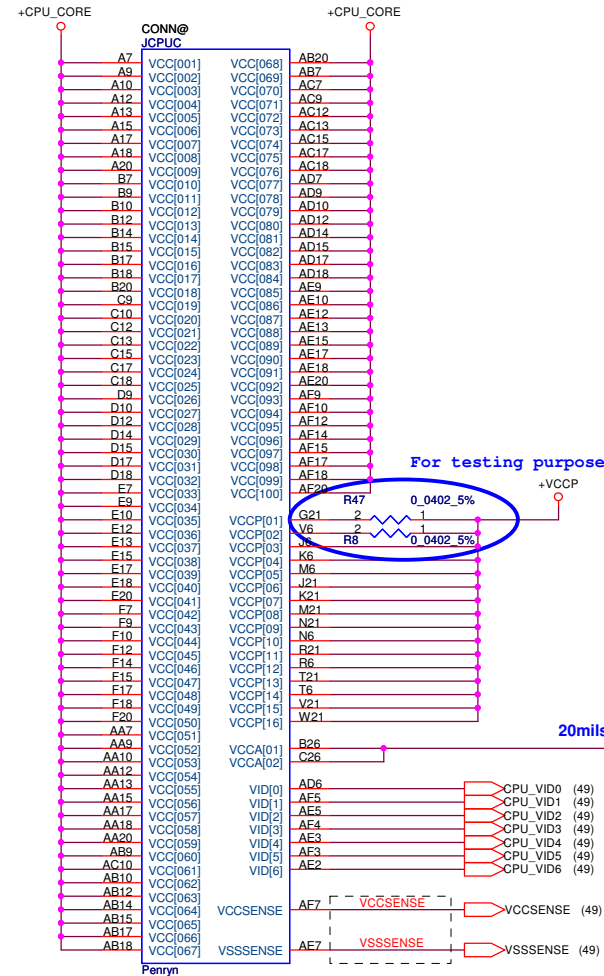


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

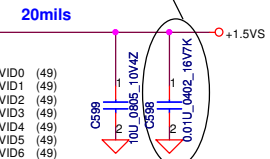
TRACE CLOSELY CPU < 0.5"  
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)  
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

3/17 change to 68P



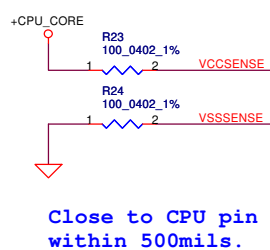
For testing purpose only

Near pin B26

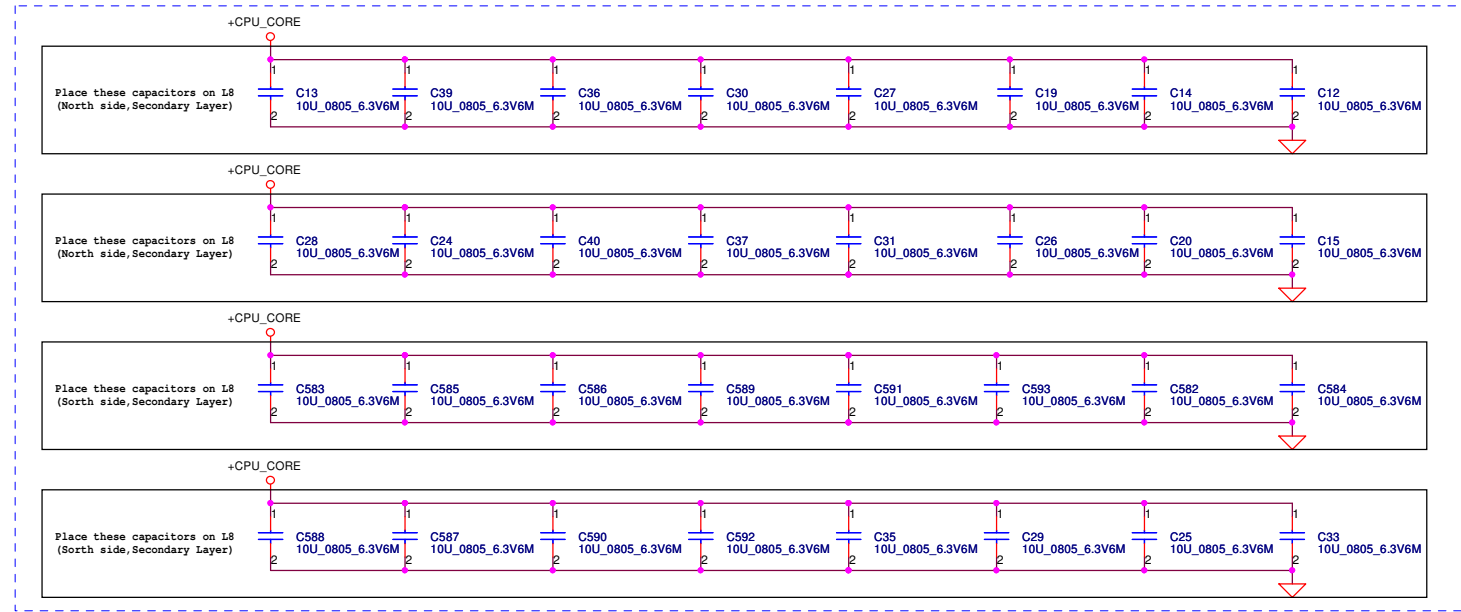


Length match within 25 mils.  
The trace width/space/other is  
16/7/25.

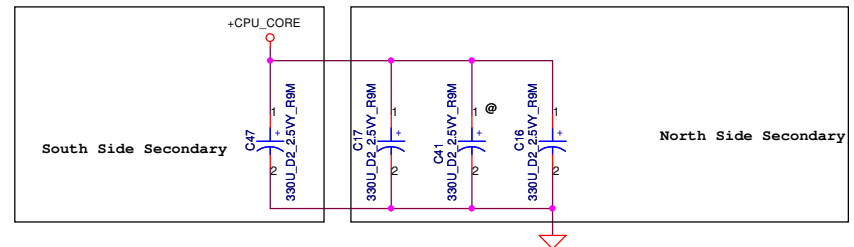
Layout Note:  
Route VCCSENSE and VSSSENSE traces at  
27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.



CONN@ JCPUD		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	V2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D16	VSS[031]	AA11
D19	VSS[032]	AA14
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB16
E24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	AF6
M22	VSS[075]	AF8
M25	VSS[076]	AF11
N1	VSS[077]	AF13
N4	VSS[078]	AF16
N23	VSS[079]	AF19
N26	VSS[080]	AF21
P3	VSS[081]	A25
		AF25

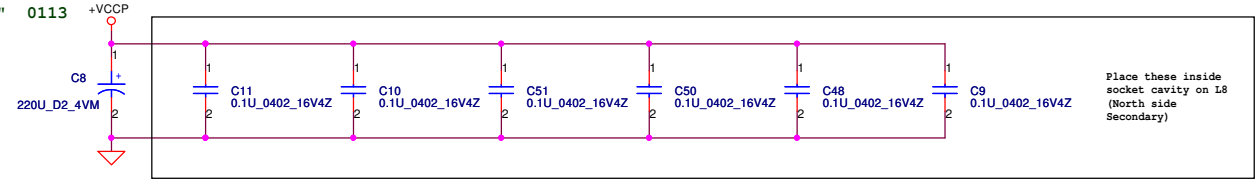


Mid Frequency Decoupling



ESR <= 1.5m ohm  
Capacitor > 1980uF

Delete "REMOVE?" 0113



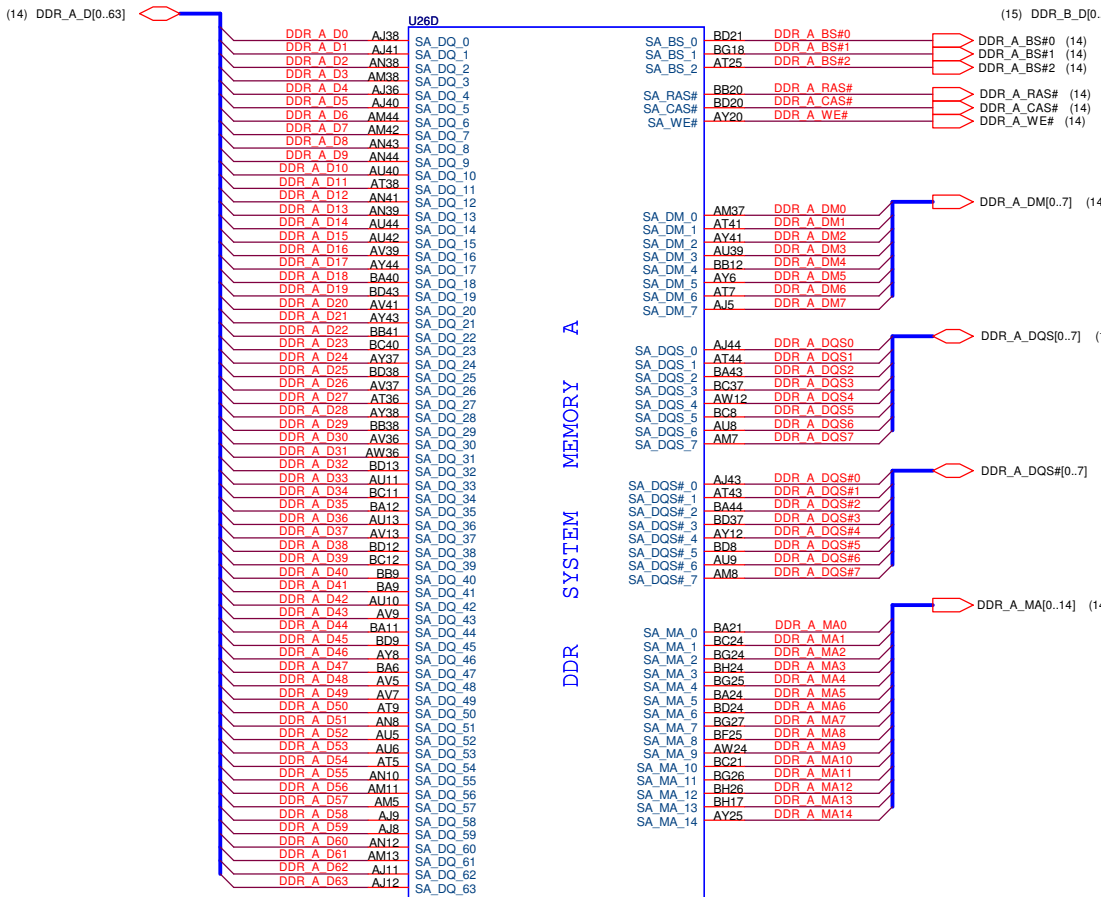
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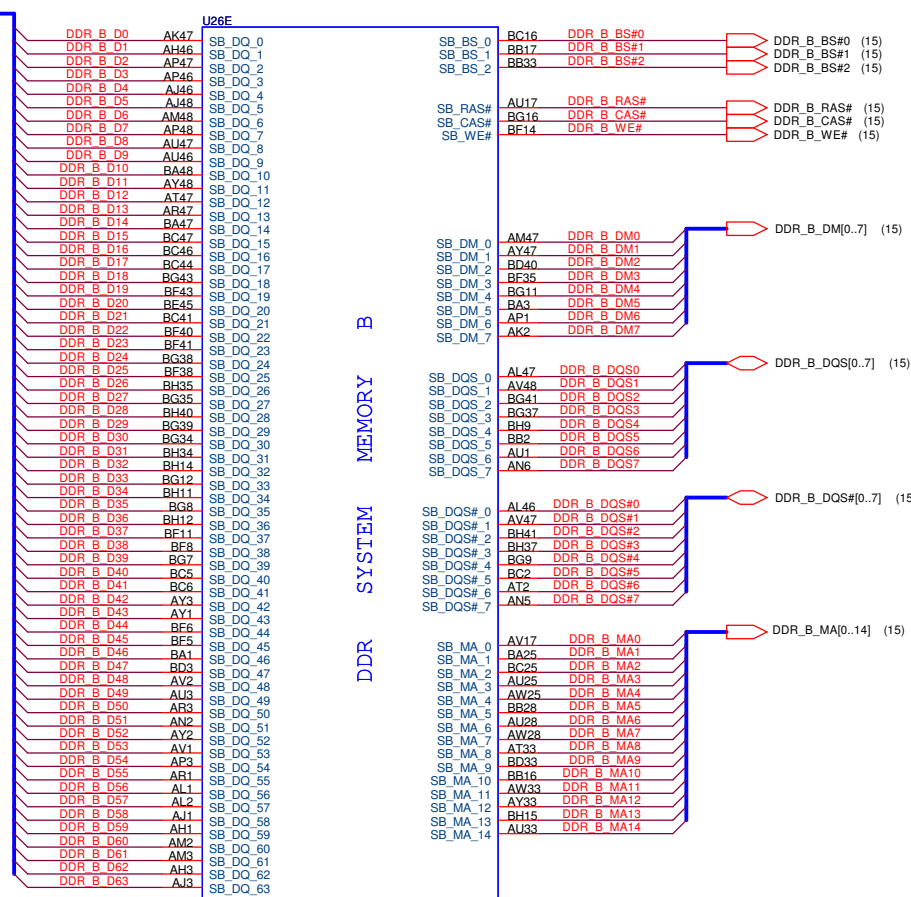
(14) DDR\_A\_D[0..63]



GM45@

CANTIGA ES\_FCBGA1329

(15) DDR\_B\_D[0..63]

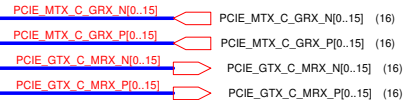
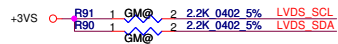


GM45@

CANTIGA ES\_FCBGA1329

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Place the resistor within 500mils (1.27mm) of the GMCH

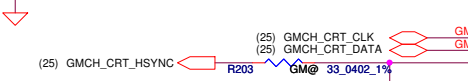
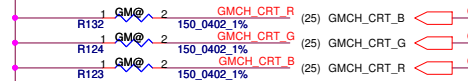
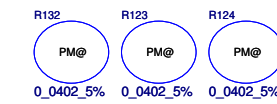
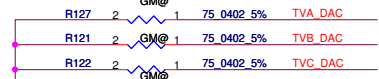
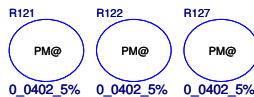
PEGCOMP trace width and spacing is 20/25 mils.

Please check Power source if want support IAMT

For Cantiga: 2.37kohm  
For Crestline: 2.4kohm  
For Calero: 1.5kohm

Note: All LVDS data signals/and it's compliments should be routed Differentially

Layout Note: Place 150 Ohm termination resistors close to GMCH



For Cantiga: 1.02kohm  
For Crestline: 1.3kohm  
For Calero: 255ohm

U26C

LVDS

GRAPHICS

PCI-EXPRESS

TV

VGA

CANTIGA ES\_FCBGA1329

GM45@

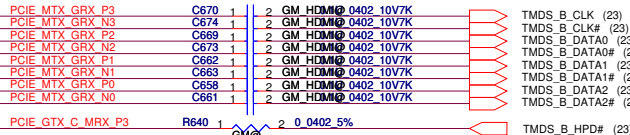
1.02K 0402 1%

GM@

R138

PM@

0.0402 5%



## Strap Pin Table

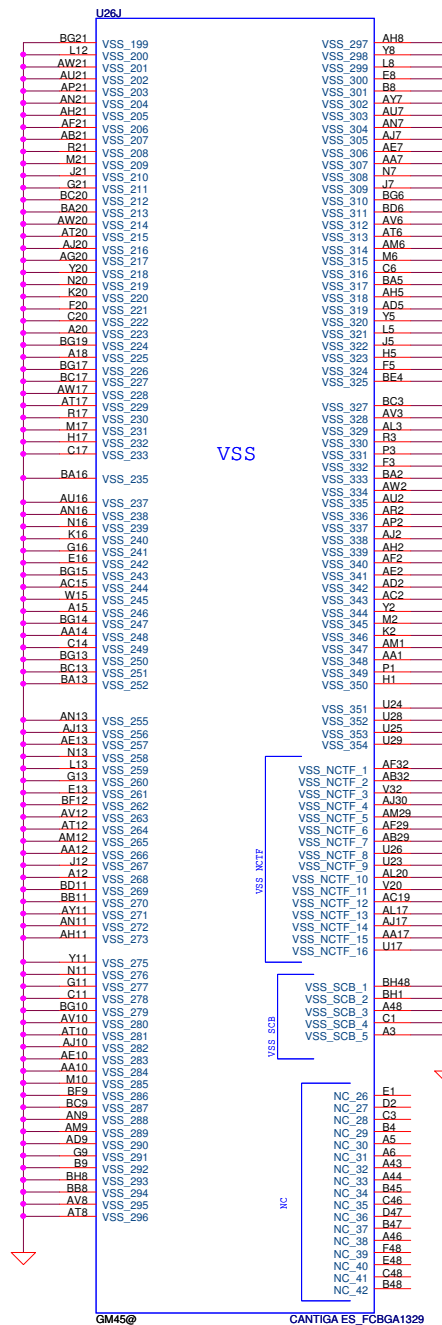
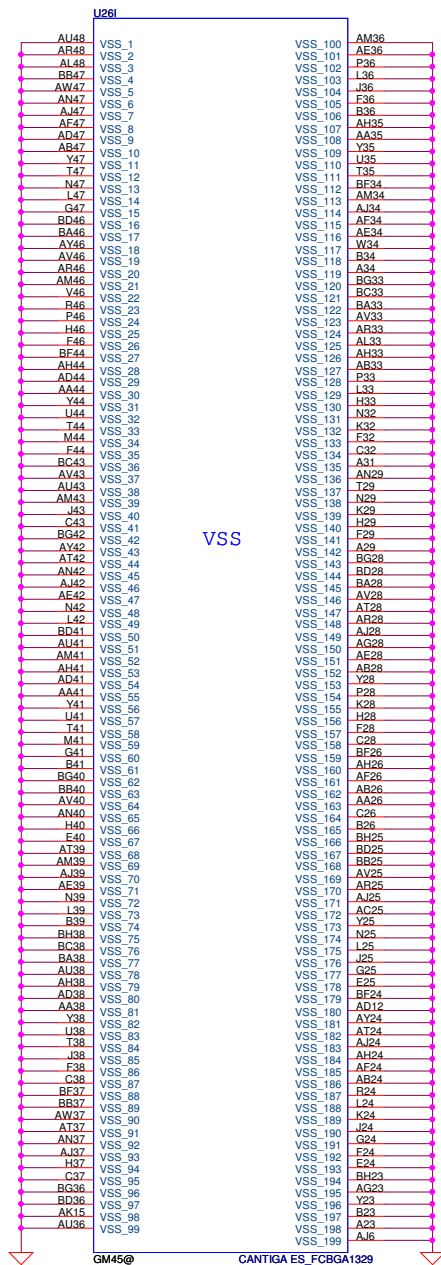
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chipset suite with no confidentiality 1=(TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation 1 = Reverse Lane *
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *

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Cantiga GMCH (3/6)-VGA/LVDS/TV	
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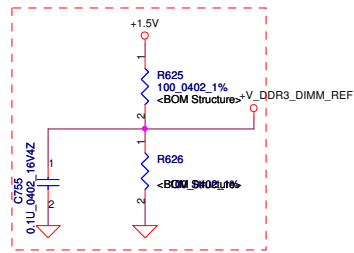




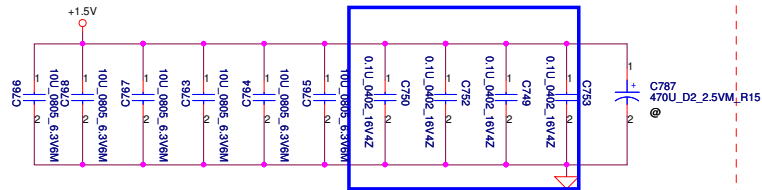


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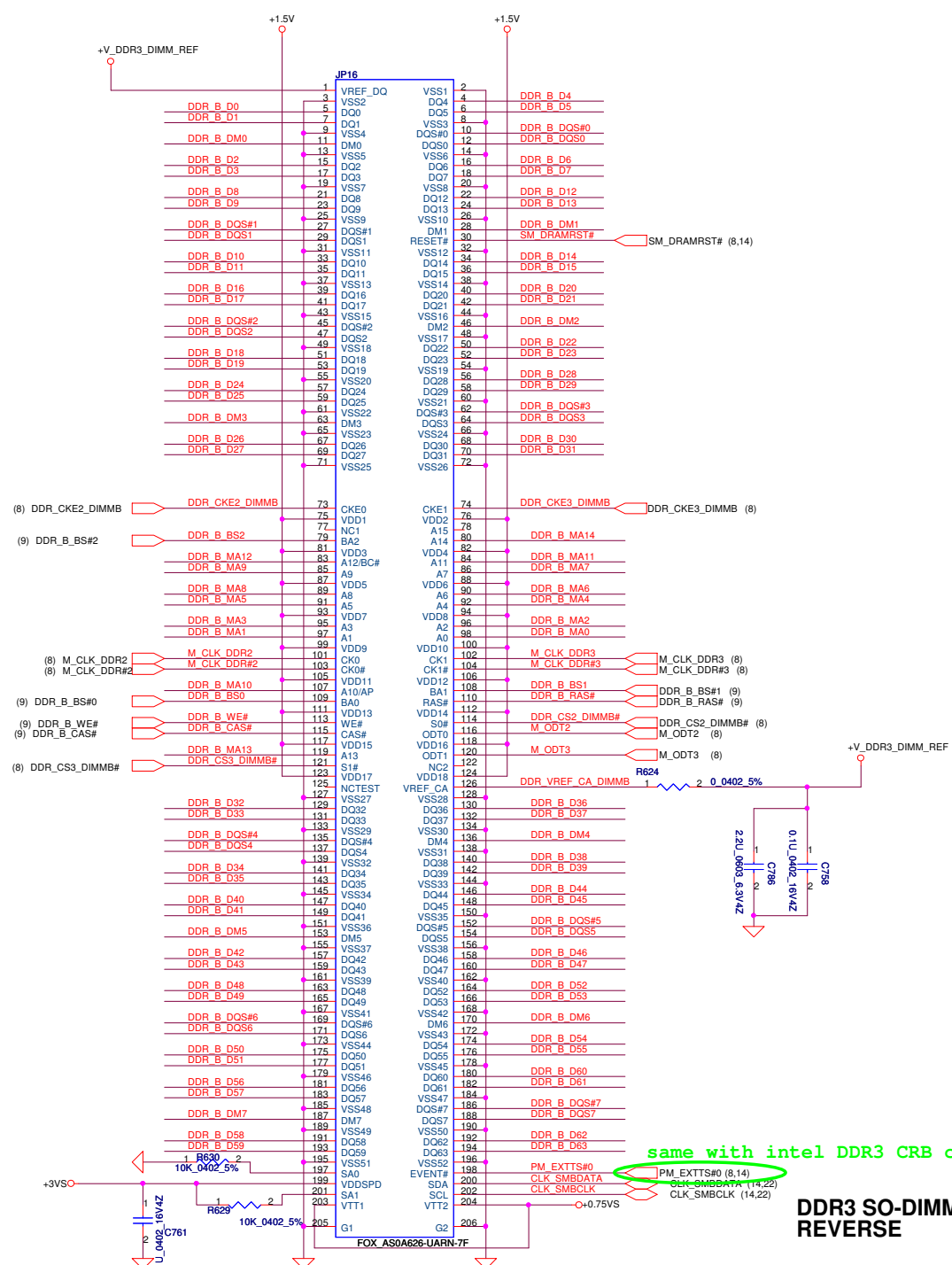
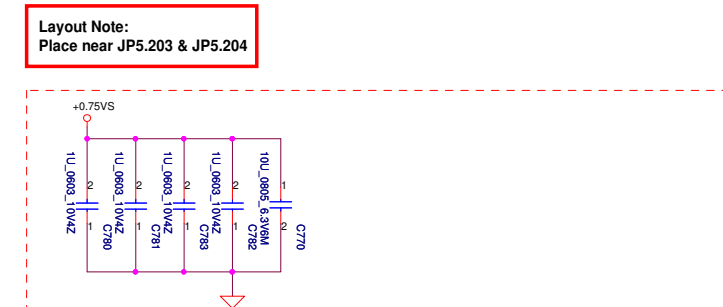
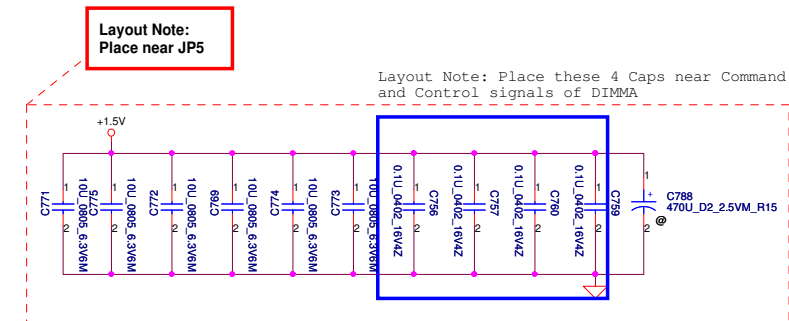
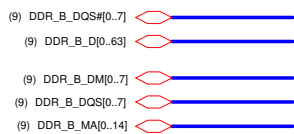


Layout Note: Place these 4 Caps near Command  
and Control signals of DIMMA



***Compal Electronics, Inc.***  
***DDRIII-SODIMM SLOT1***

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				<b>DDRIII-SODIMM SLOT!</b>			
				Size Custmr	Document Number		Rev
				<b>KIWX_LA-5081P</b>		1.0	
Date:				Tuesday, April 28, 2009		Sheet 14 of 51	



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GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10, 12
1	1	1.20V	0
0	1	1.09V	8

VGA CRT\_R R933 1 PM@ 2 150\_0402 1%  
VGA CRT\_G R934 1 PM@ 2 150\_0402 1%  
VGA CRT\_B R935 1 PM@ 2 150\_0402 1%

(10) PCIE\_MTX\_C\_GRX\_N[0..15] PCIE\_MTX\_C\_GRX\_N[0..15]  
(10) PCIE\_MTX\_C\_GRX\_P[0..15] PCIE\_MTX\_C\_GRX\_P[0..15]  
(10) PCIE\_GTX\_C\_MRX\_N[0..15] PCIE\_GTX\_C\_MRX\_N[0..15]  
(10) PCIE\_GTX\_C\_MRX\_P[0..15] PCIE\_GTX\_C\_MRX\_P[0..15]

Part of 5

GPIO  
DACA  
DACC  
DACC  
I2C  
TEST  
CLK

PCIE\_MTX\_C\_GRX\_P0 AE12  
PCIE\_MTX\_C\_GRX\_N0 AE12  
PCIE\_MTX\_C\_GRX\_P1 AE12  
PCIE\_MTX\_C\_GRX\_N1 AE12  
PCIE\_MTX\_C\_GRX\_P2 AE13  
PCIE\_MTX\_C\_GRX\_N2 AE13  
PCIE\_MTX\_C\_GRX\_P3 AE13  
PCIE\_MTX\_C\_GRX\_N3 AE13  
PCIE\_MTX\_C\_GRX\_P4 AE13  
PCIE\_MTX\_C\_GRX\_N4 AE13  
PCIE\_MTX\_C\_GRX\_P5 AE16  
PCIE\_MTX\_C\_GRX\_N5 AE16  
PCIE\_MTX\_C\_GRX\_P6 AE16  
PCIE\_MTX\_C\_GRX\_N6 AE16  
PCIE\_MTX\_C\_GRX\_P7 AE18  
PCIE\_MTX\_C\_GRX\_N7 AE18  
PCIE\_MTX\_C\_GRX\_P8 AE18  
PCIE\_MTX\_C\_GRX\_N8 AE18  
PCIE\_MTX\_C\_GRX\_P9 AE21  
PCIE\_MTX\_C\_GRX\_N9 AE21  
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PCIE\_MTX\_C\_GRX\_N10 AE21  
PCIE\_MTX\_C\_GRX\_P11 AE22  
PCIE\_MTX\_C\_GRX\_N11 AE22  
PCIE\_MTX\_C\_GRX\_P12 AE24  
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PCIE\_MTX\_C\_GRX\_P13 AE24  
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PCIE\_MTX\_C\_GRX\_P14 AE25  
PCIE\_MTX\_C\_GRX\_N14 AE25  
PCIE\_MTX\_C\_GRX\_P15 AE27  
PCIE\_MTX\_C\_GRX\_N15 AE27

PCIE\_GTX\_C\_MRX\_P0 C930 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_N0 C931 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_P1 C932 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_N1 C933 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_P2 C934 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_N2 C935 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_P3 C936 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_N3 C937 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_P4 C938 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_N4 C939 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_P5 C940 PM@ 1 2 0.1U\_0402\_10V7K  
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PCIE\_GTX\_C\_MRX\_P6 C942 PM@ 1 2 0.1U\_0402\_10V7K  
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PCIE\_GTX\_C\_MRX\_N14 C959 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_P15 C960 PM@ 1 2 0.1U\_0402\_10V7K  
PCIE\_GTX\_C\_MRX\_N15 C961 PM@ 1 2 0.1U\_0402\_10V7K

GPIO  
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I2C  
TEST  
CLK

GPIO  
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OSC\_SPREAD  
OSC\_OUT

R963 22\_0402\_5%  
R964 10K\_0402\_5% PM@  
R965 10K\_0402\_5% PM@  
R966 10K\_0402\_5% PM@

If External Spread Spectrum not stuff then stuff resistor

27MHZ\_16PF\_X75027000B1H-U PM@  
C967 20P\_0402\_50V8 PM@  
C968 20P\_0402\_50V8 PM@

GPIO  
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GPIO  
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TEST  
CLK

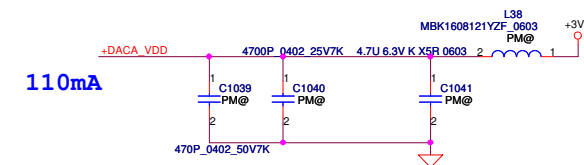
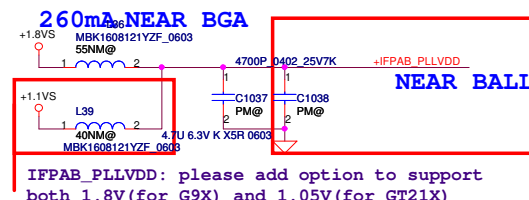
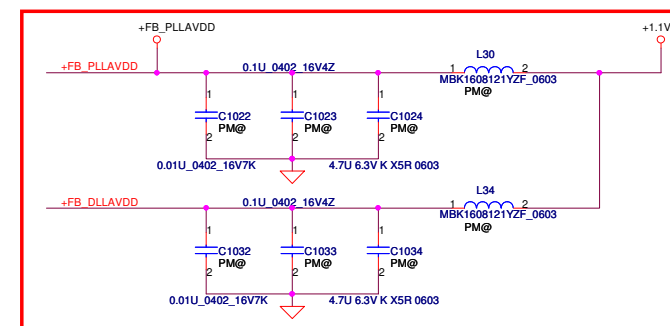
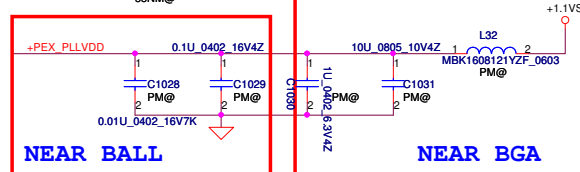
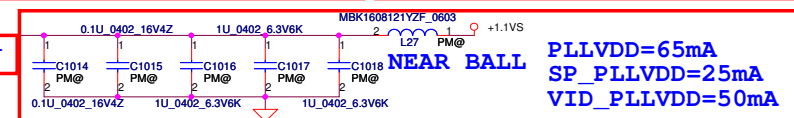
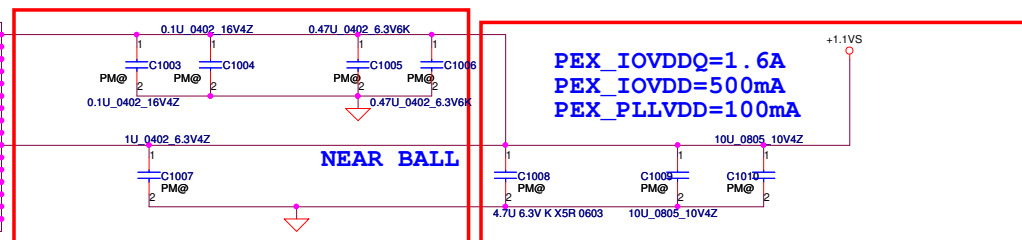
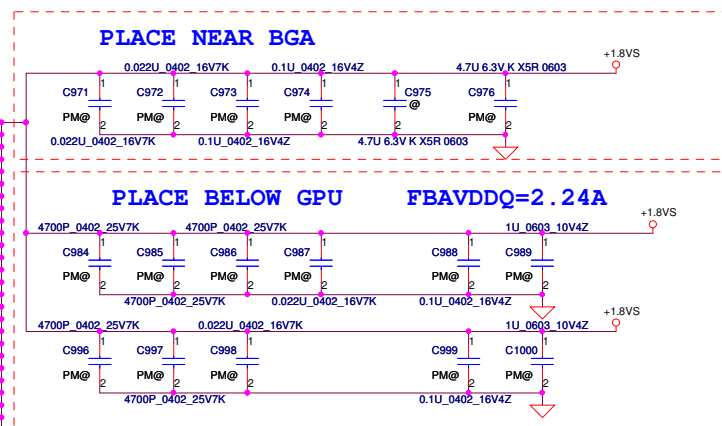
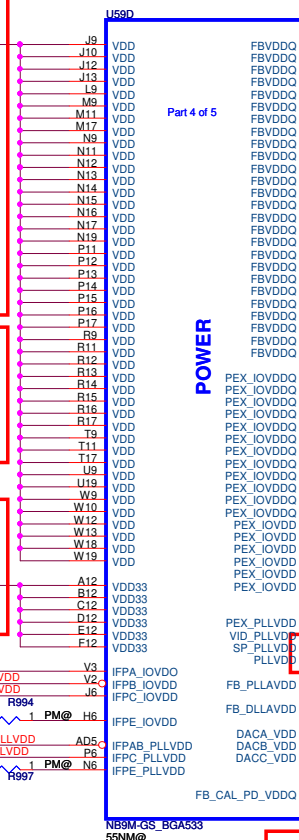
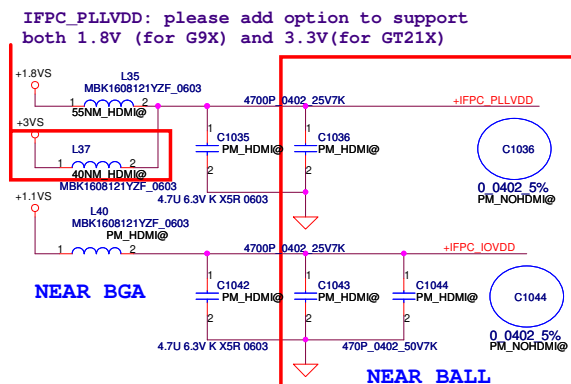
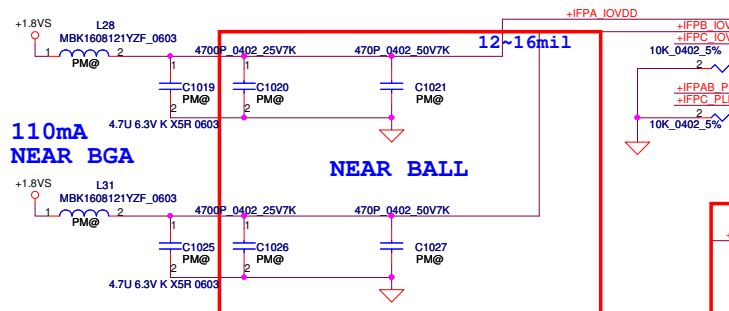
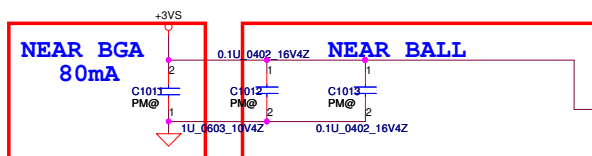
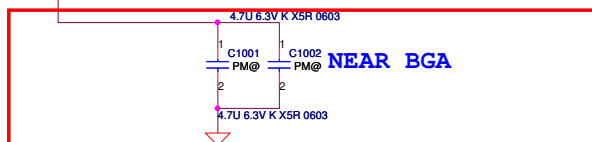
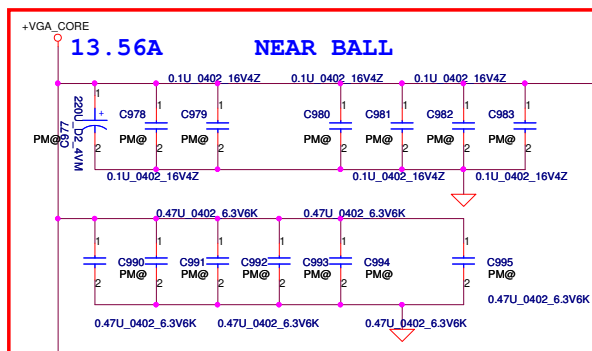
GPIO  
DACA  
DACC  
DACC  
I2C  
TEST  
CLK

GPIO  
DACA  
DACC  
DACC  
I2C  
TEST  
CLK

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Issued Date	2009/04/23	Deciphered Date	2010/05
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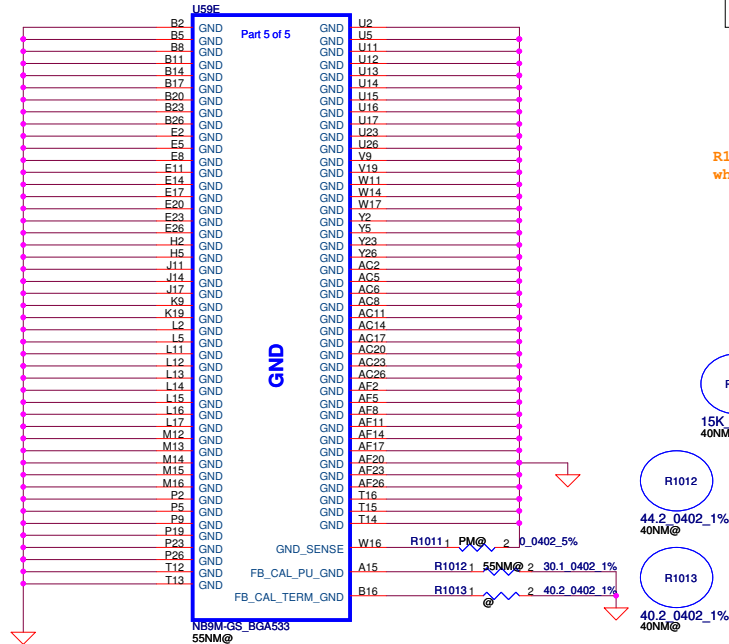


FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS



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Issued Date	2009/04/23	Deciphered Date	2010/05	Title		
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				Date:	Tuesday, April 28, 2009	Sheet 18 of 51

A total of 8 signals are required for GB1 strapping this includes  
 2 reference signals  
 6 physical strapping pins  
 4 logical strapping bits  
 A total of 24 logical strapping bits are available



R148 pop 25K ohm  
 when use N10M-GE1-S (55nm)

(17) STRAP2  
 (17) STRAP1  
 (17) STRAP0  
 (17) ROM\_SCLK  
 (17) ROM\_SI  
 (17) ROM\_SO

R1002  
 15K 0402\_1%  
 40NM@

R1005  
 24.9K 0402\_1%  
 40NM@

R1012  
 44.2 0402\_1%  
 40NM@

R1013  
 40.2 0402\_1%  
 40NM@

### GB1 Family GPU Strap Options

X76

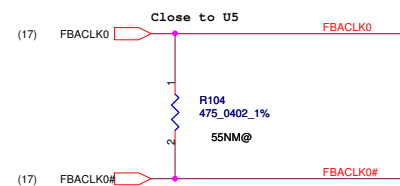
GPU	FB Memory (DDR2)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung	64Mx16	PU 5K	PD 15K	PD 20K	PU 25K	PD 10K PU 45K
	Hynix	64Mx16	PU 5K	PD 15K	PD 5K	PU 25K	PD 10K PU 45K
	Qimonda	64Mx16	PU 5K	PD 15K	PD 15K	PU 25K	PD 10K PU 45K
N10M-GS (0x6EC) 40nm	Samsung	64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 35K PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 35K PU 45K
	Qimonda	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 35K PU 45K

4/23 update strap1 10K to 35K  
 according to N10M latest PUN

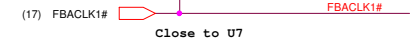
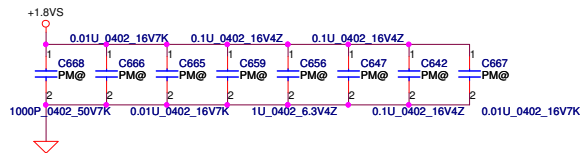
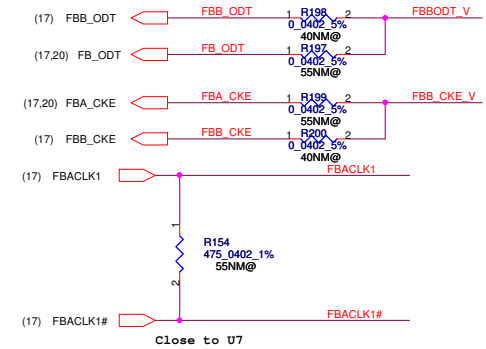
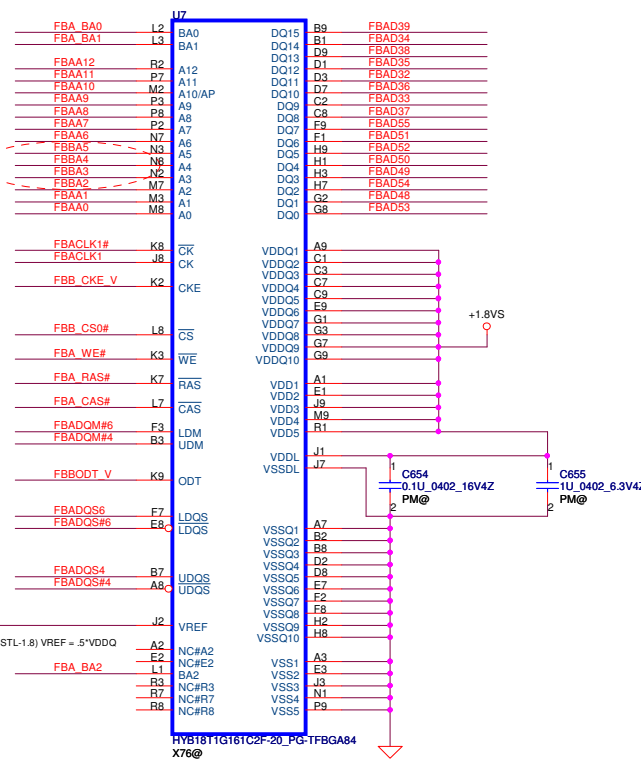
Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001\_V06 (2008/4/01)

U59  
 NB10M-GS-S  
 40NM@



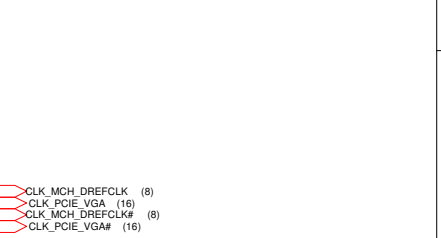
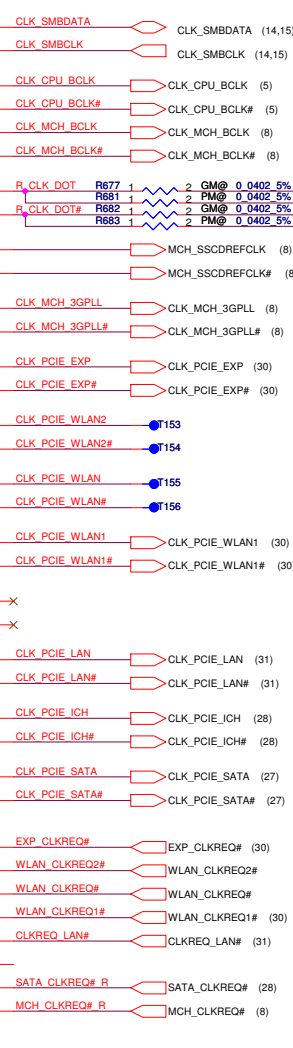
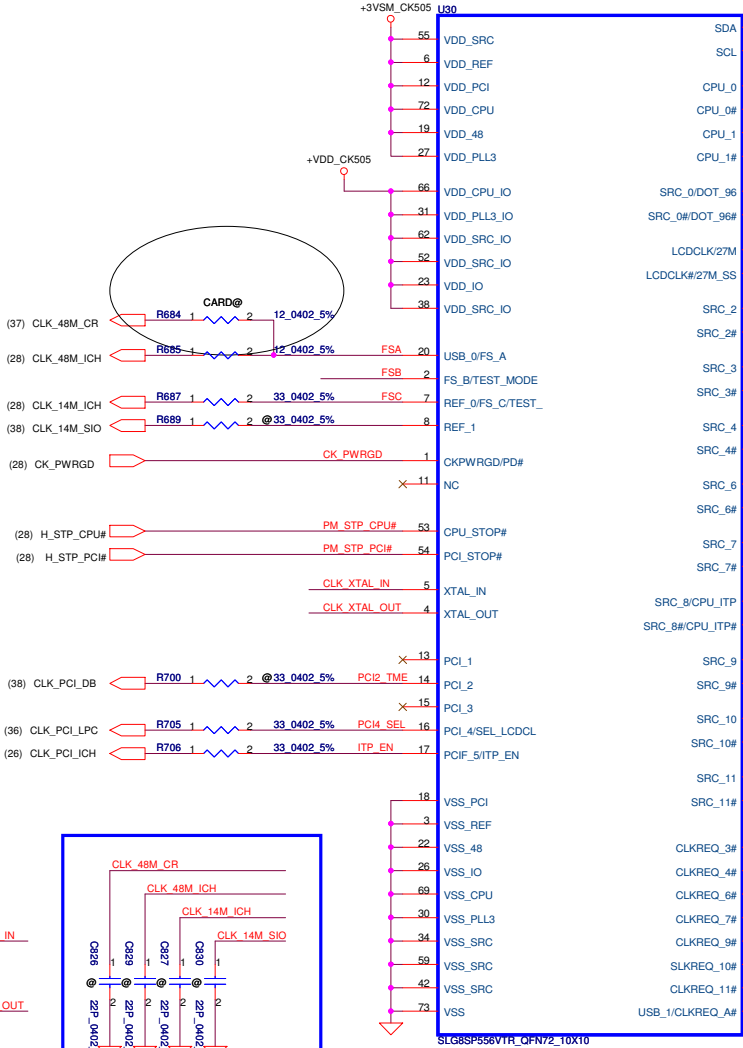
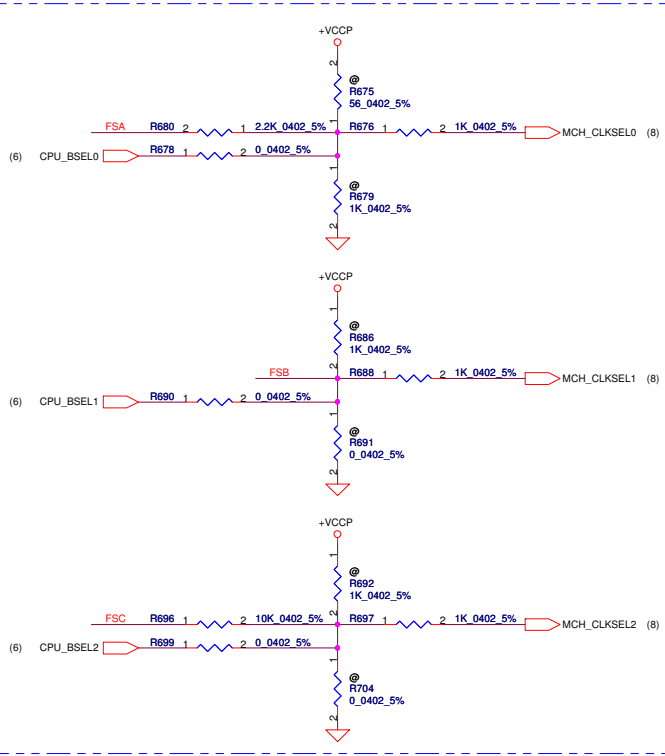
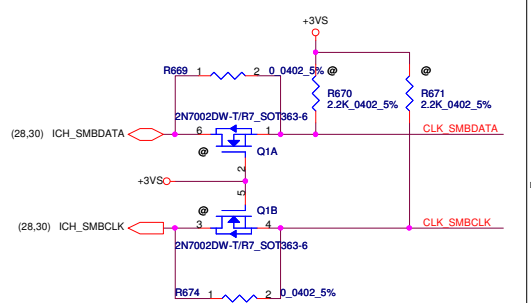
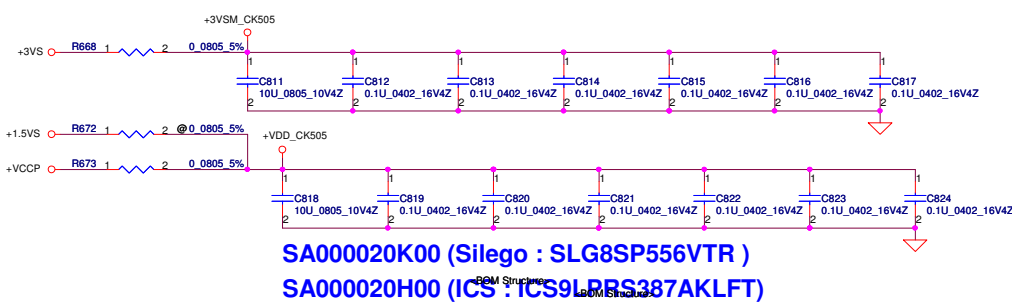
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2009/04/23	Deciphered Date	2010/05	Title <b>VRAM DDRA</b>		
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				Date: Tuesday, April 28, 2009	Sheet 20	of 51



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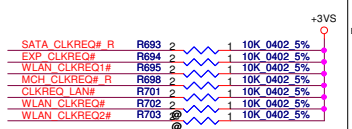


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



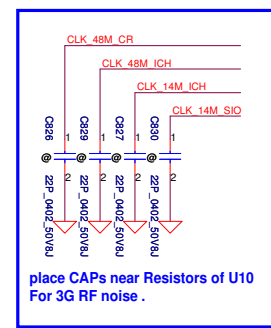
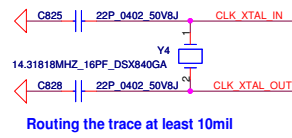
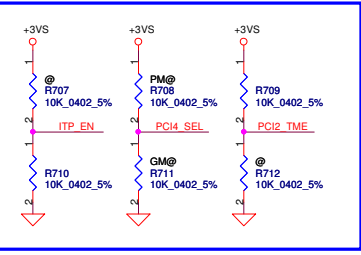
# SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN
SRC6	PCIE_WLAN1
SRC8	PCIE_WLAN1
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



# REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	PCIE_SATA
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL



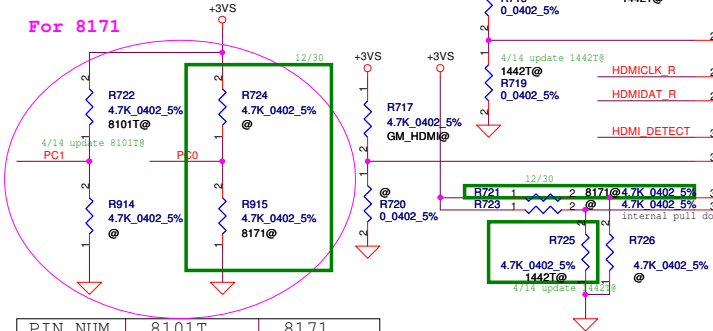
For ITP\_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#  
For PCI4\_SEL, 0 = Pin24/25 : DOT96 / DOT96#  
Pin28/29 : LCDCLK / LCDCLK#  
1 = Pin24/25 : SRC\_0 / SRC\_0#  
Pin28/29 : 27M/27M\_SS

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Size				Document Number				KIWA5/6 LA-5081P			
Date: Tuesday, April 28, 2009				1				Sheet 22 of 51			



10/30 update PS8171 co-lay circuit  
4/14 update 1442T co-lay circuit

For 8171

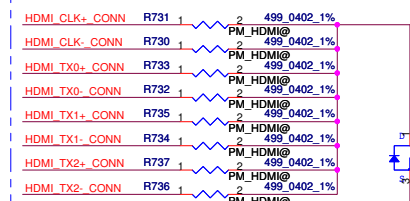


PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PIO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	APD
PIN12	GND	ASQ1
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

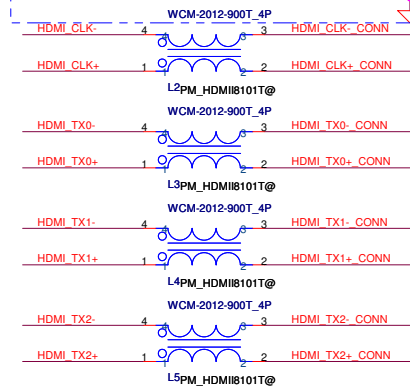
(10) TMD5\_B\_CLK#  
(10) TMD5\_B\_CLK#  
(10) TMD5\_B\_DATA0#  
(10) TMD5\_B\_DATA0#  
(10) TMD5\_B\_DATA1#  
(10) TMD5\_B\_DATA1#  
(10) TMD5\_B\_DATA2#  
(10) TMD5\_B\_DATA2#  
(10) TMD5\_B\_DATA2#  
(10) TMD5\_B\_DATA2#

For 8171 net name:  
EMI0, EMI1  
ASQ0, ASQ1  
APD

TMD5 pull down (500ohm) resistors for ATI M92-S2 XT



NEAR CONNECTOR



HDMI_CLK+	R751	1442T@	2	0.0402_5%	HDMI_CLK+ CONN
HDMI_CLK-	R752	1442T@	2	0.0402_5%	HDMI_CLK- CONN
HDMI_TX0+	R753	1442T@	2	0.0402_5%	HDMI_TX0+ CONN
HDMI_TX0-	R754	1442T@	2	0.0402_5%	HDMI_TX0- CONN
HDMI_TX1+	R755	1442T@	2	0.0402_5%	HDMI_TX1+ CONN
HDMI_TX1-	R756	1442T@	2	0.0402_5%	HDMI_TX1- CONN
HDMI_TX2+	R757	1442T@	2	0.0402_5%	HDMI_TX2+ CONN
HDMI_TX2-	R758	1442T@	2	0.0402_5%	HDMI_TX2- CONN

P/N:SA00002D700 (8101T)  
P/N:SA00001U920 (CH7318C)

U31

SIC ASM1442T

1442T@

OE#

SCL\_SINK

SDA\_SINK

HPD\_SINK

DDC\_EN

CFG0

CFG1

IN\_D4+

IN\_D4-

IN\_D3+

IN\_D3-

IN\_D2+

IN\_D2-

IN\_D1+

IN\_D1-

OUT\_D4+

OUT\_D4-

OUT\_D3+

OUT\_D3-

OUT\_D2+

OUT\_D2-

OUT\_D1+

OUT\_D1-

OUT\_D1+

OUT\_D1-

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OUT\_D1+

OUT\_D1-

OUT\_D1+

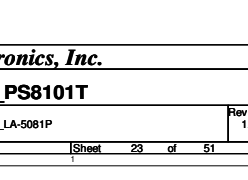
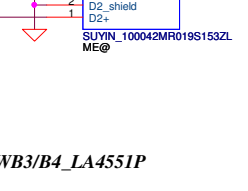
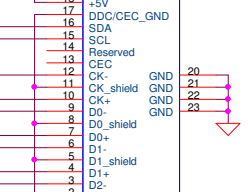
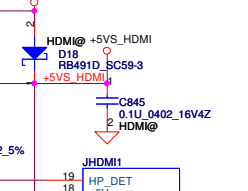
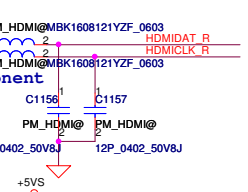
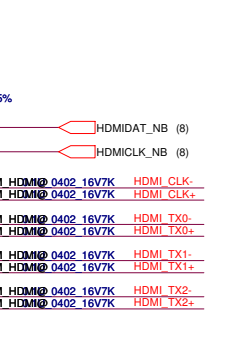
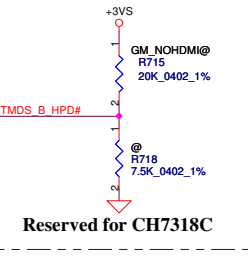
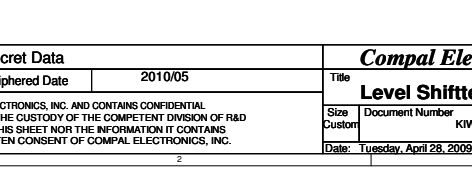
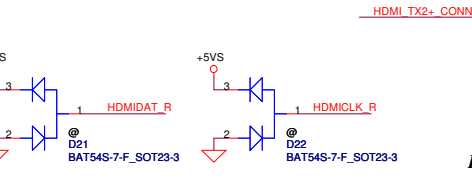
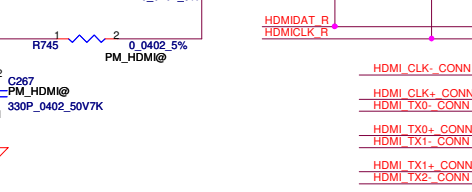
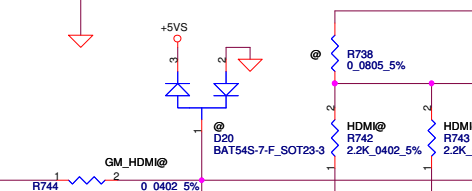
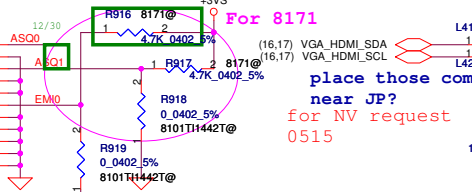
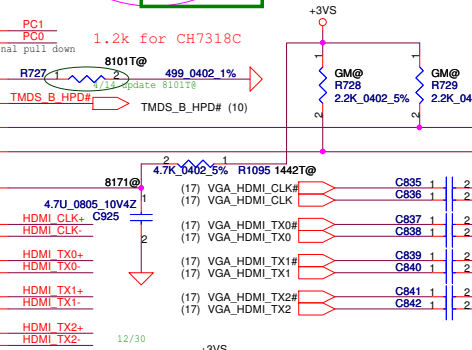
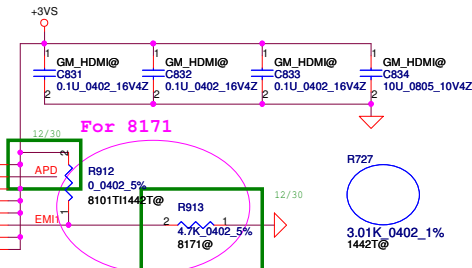
OUT\_D1-

OUT\_D1+

OUT\_D1-

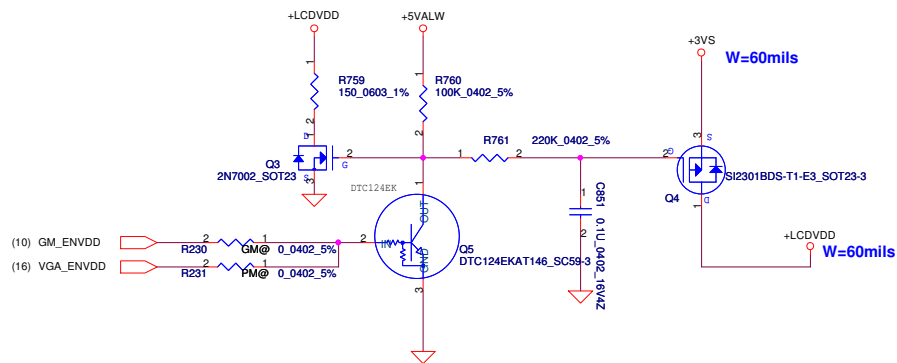
OUT\_D1+

OUT\_D1-

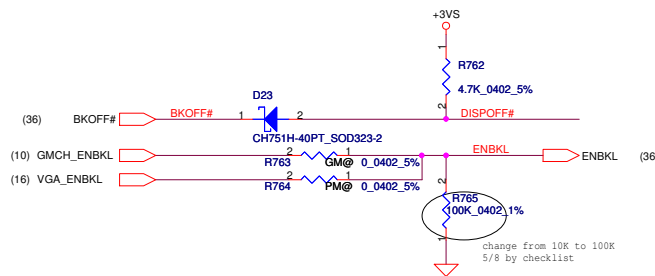


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2010/05		
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Title		
Level Shifter_PS8101T		
Size	Document Number	Rev
Custom	KIWA_XA-5081P	1.0
Date	Tuesday, April 28, 2009	Sheet 23 of 51

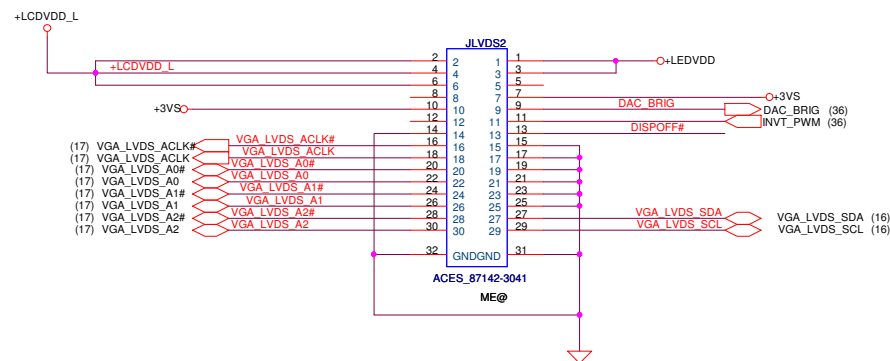
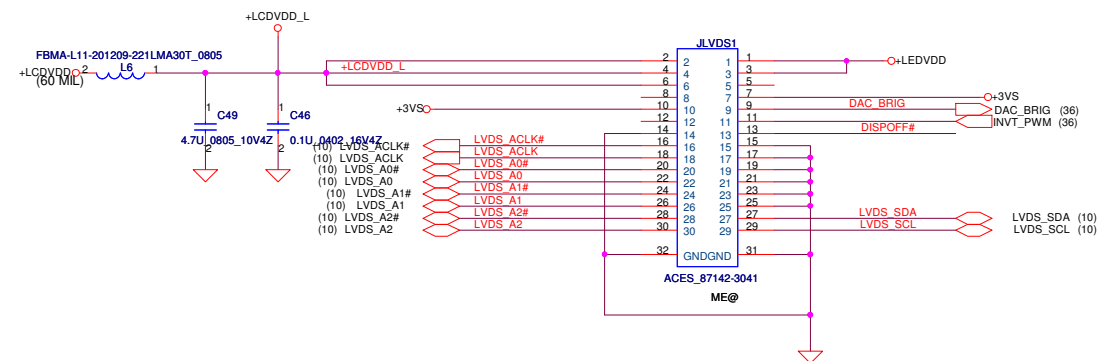
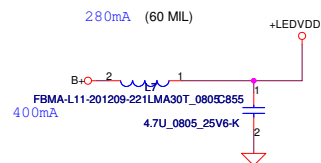
# LCD POWER CIRCUIT



LCD/PANEL BD. Conn.  
FOR UMA



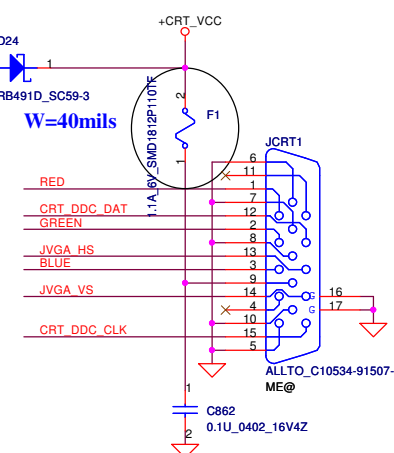
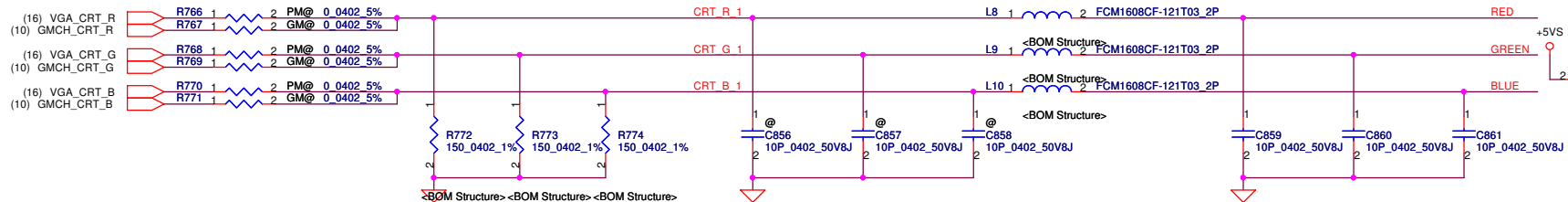
LCD/PANEL BD. Conn.  
FOR DIS



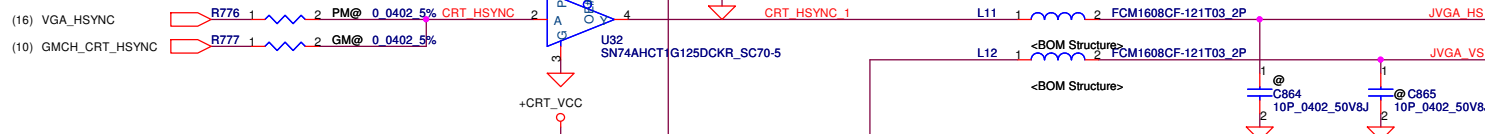
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/04/23				Title			
				Deciphered Date				LVDS & DVI Connector			
				2010/05				KIWA5/6 LA-5081P			
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				Size				Rev			
				B				1.0			
				Sheet				24 of 51			

# CRT Connector

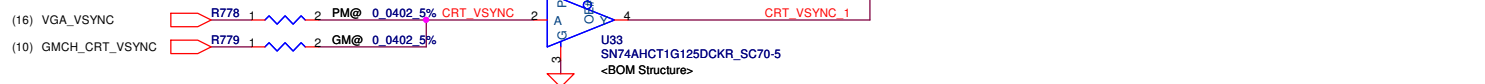
## CLOSE TO CONN



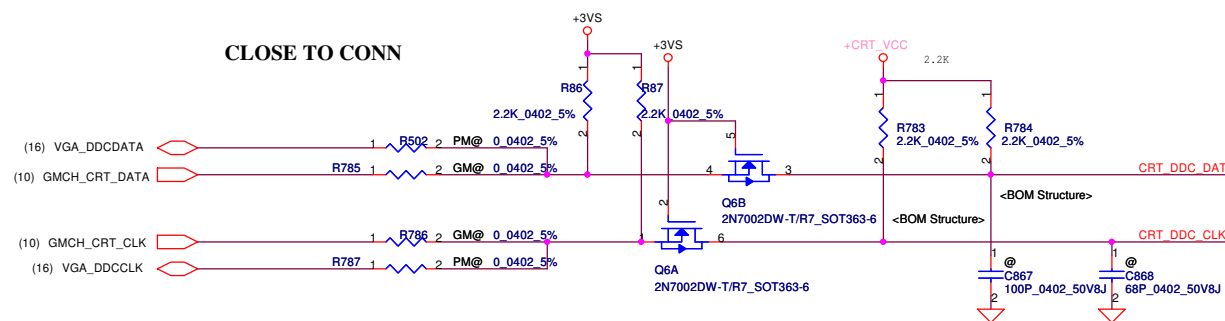
## CLOSE TO CONN



## CLOSE TO CONN



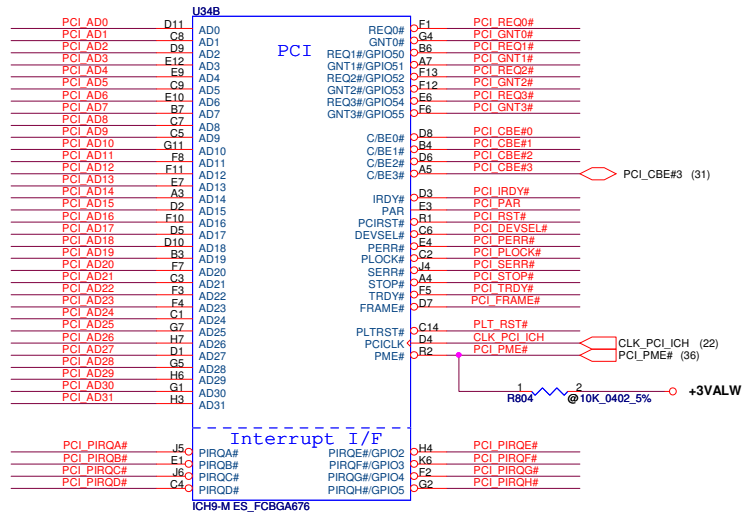
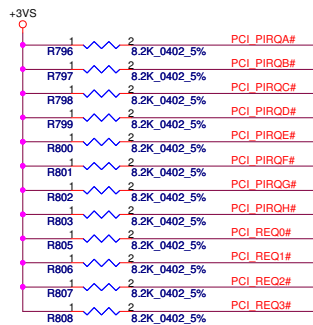
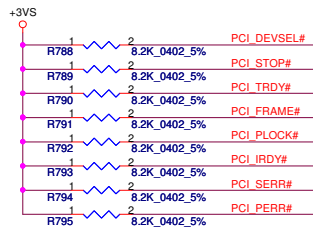
## CLOSE TO CONN



## PIN ASSIGMENT

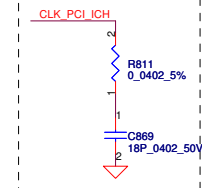
D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Custom	Document Number	KIWA5/6 LA-5081P	Rev	1.0
Date:	Tuesday, April 28, 2009	Sheet	25	of	51



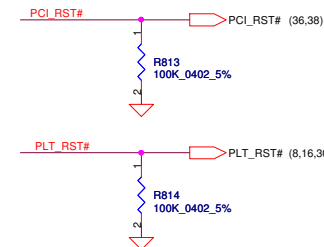
Pull high?

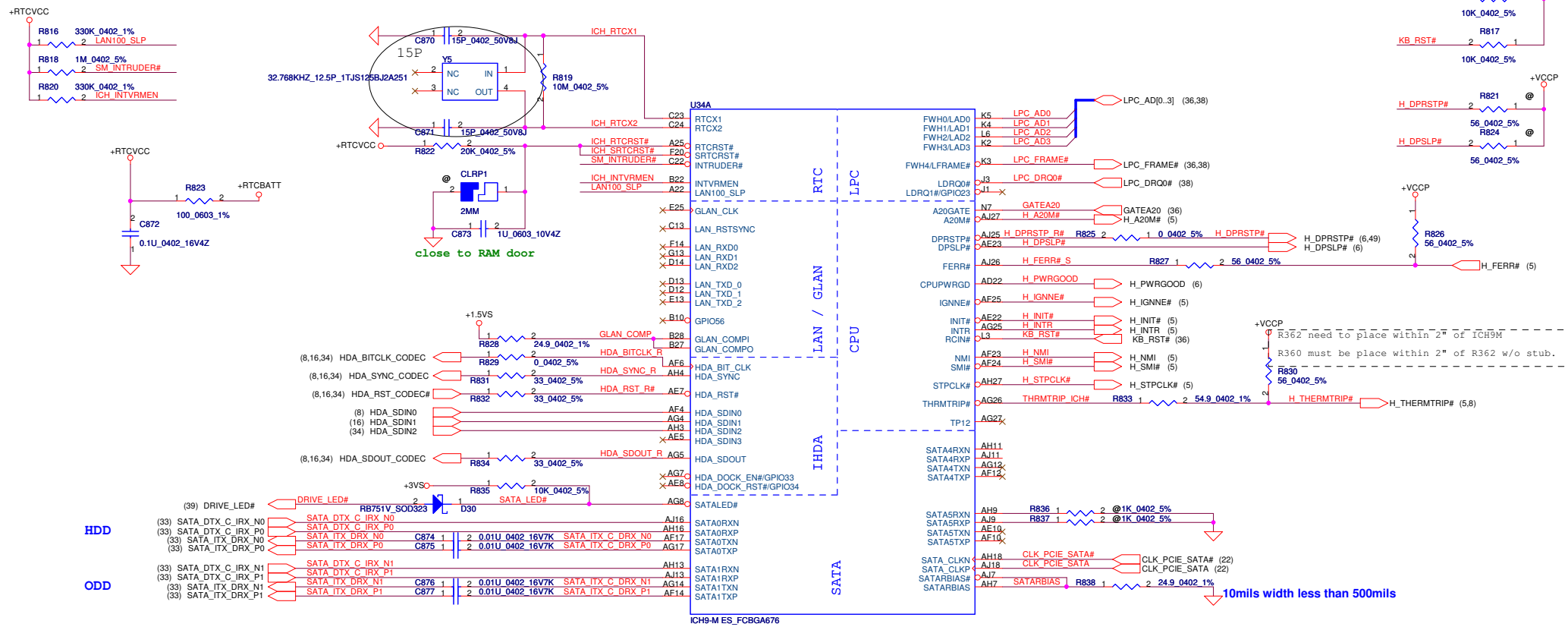
Place closely pin D4



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

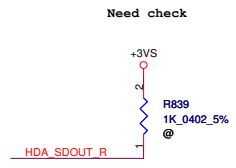
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*





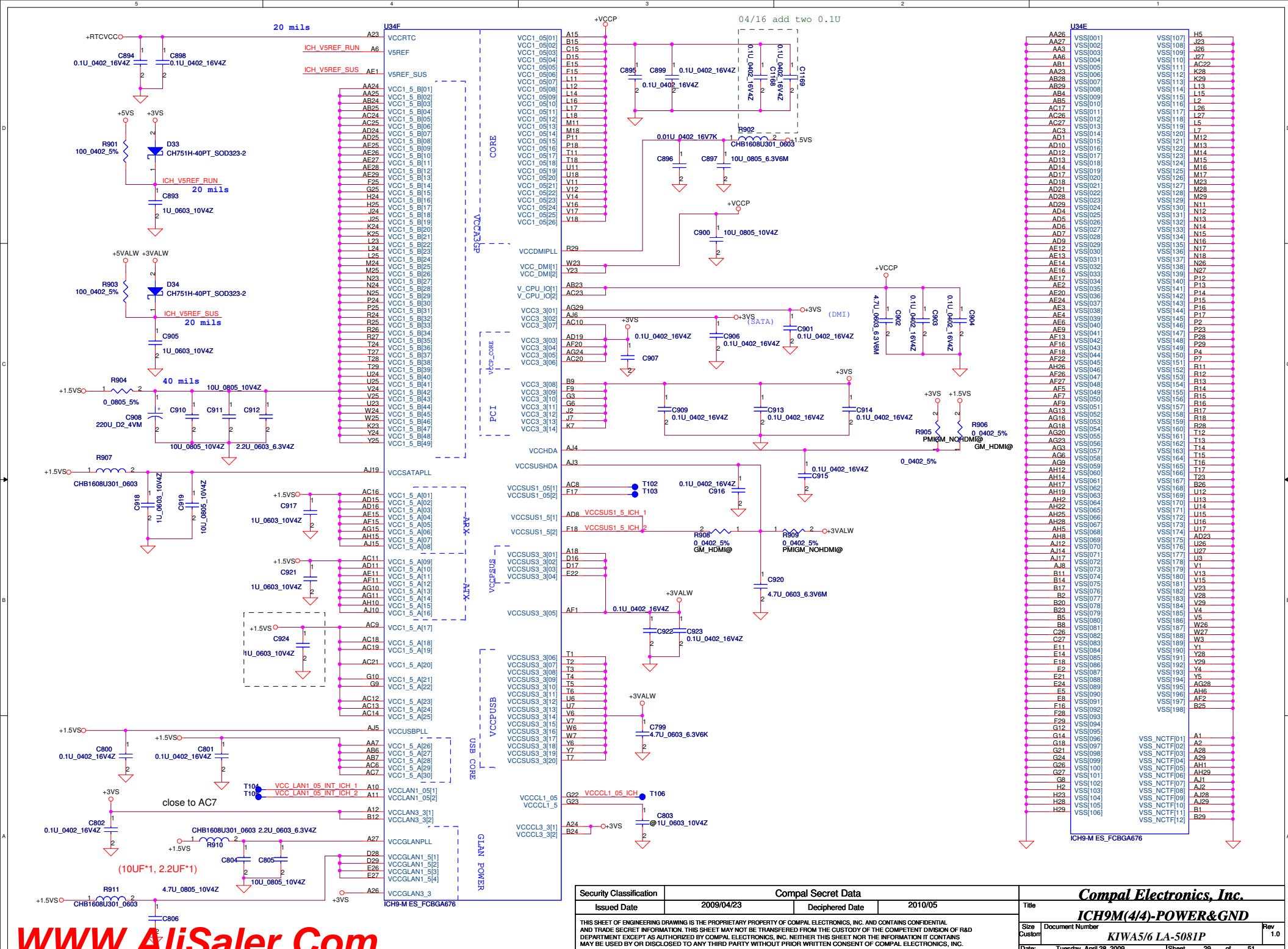
SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1







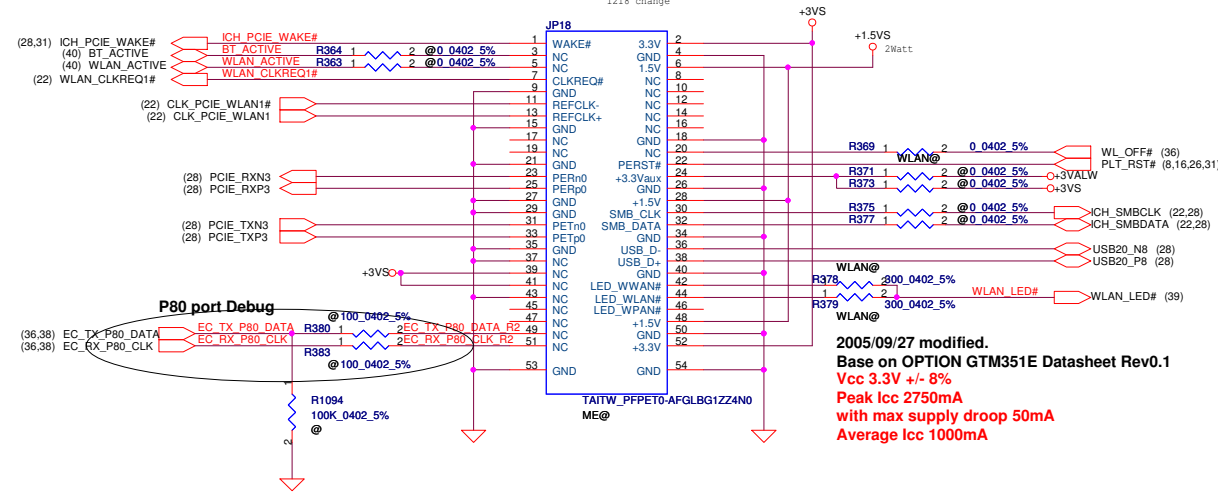


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Title		KIWA5/6 LA-5081P	
Size	Document Number	Rev 1.0	
Custom	Tuesday, April 28, 2009	Sheet 29 of 51	

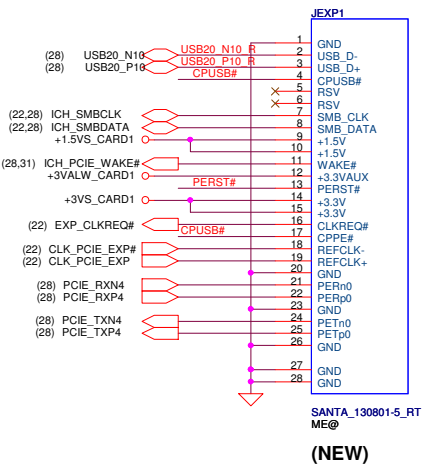
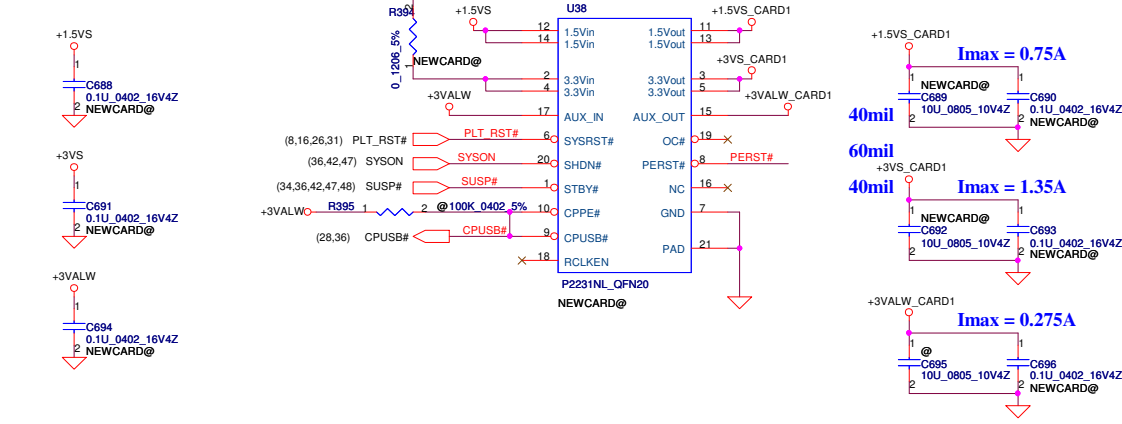


Mini-Express Card(Slot 2-WIRELESS) 5.2mm high

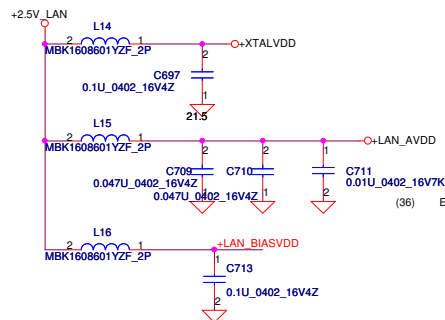


2005/09/27 modified.  
Base on OPTION GTM351E Datasheet Rev0.1  
Vcc 3.3V +/- 8%  
Peak Icc 2750mA  
with max supply droop 50mA  
Average Icc 1000mA

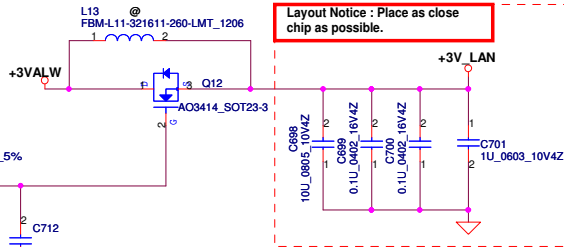
Express Card Power Switch



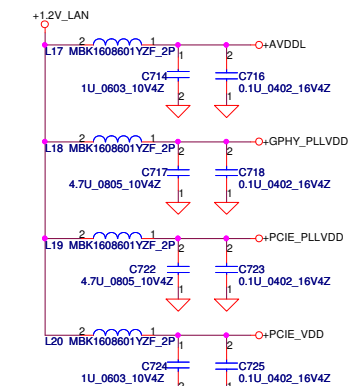
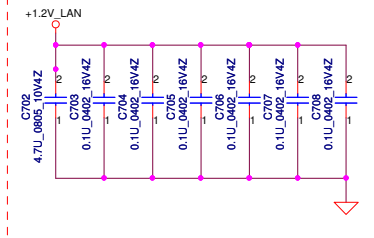
Layout Notice : Filter place as close chip as possible.



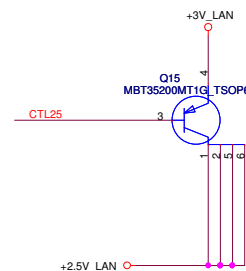
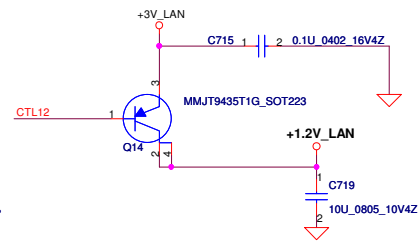
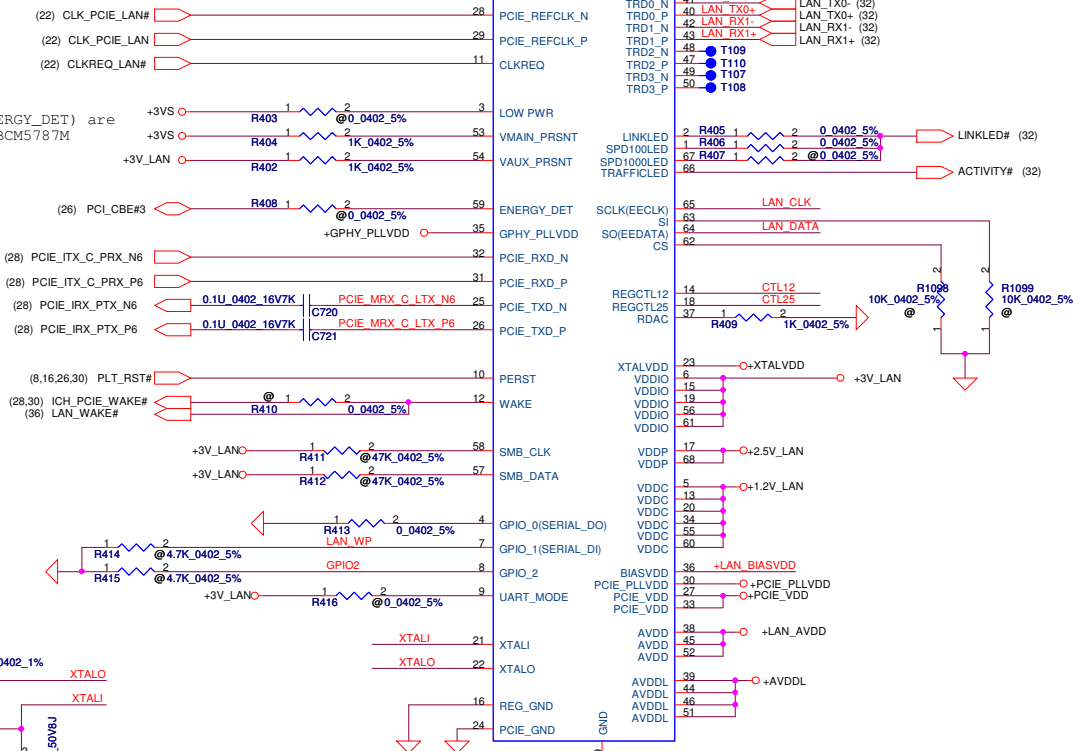
Layout Notice : Place as close chip as possible.



Layout Notice : 1.2V filter. Place as close chip as possible.



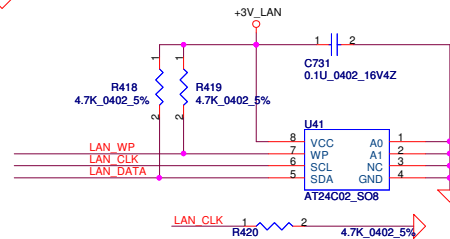
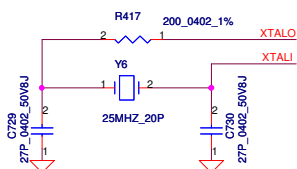
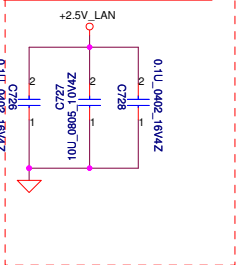
(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M



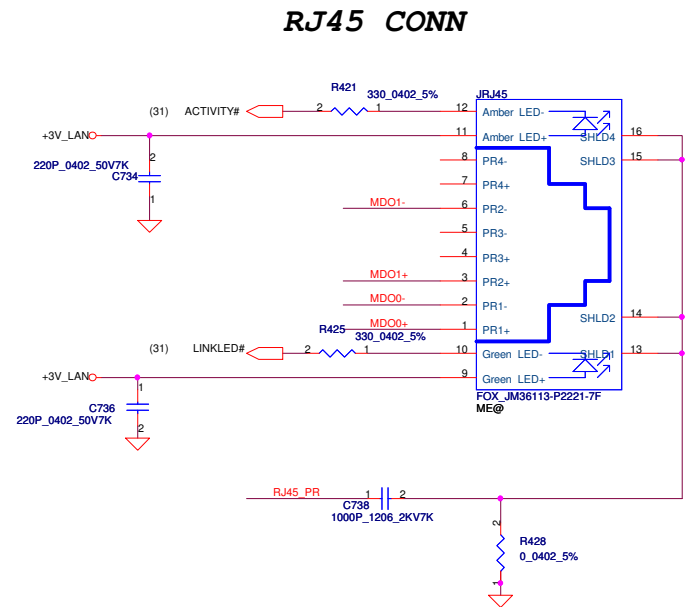
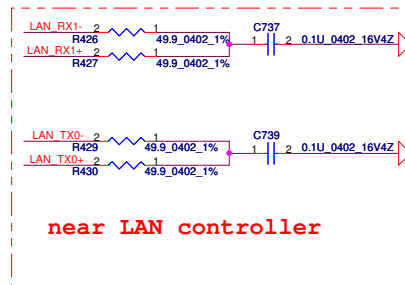
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

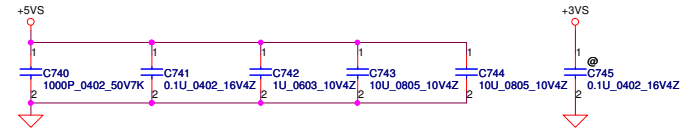
Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

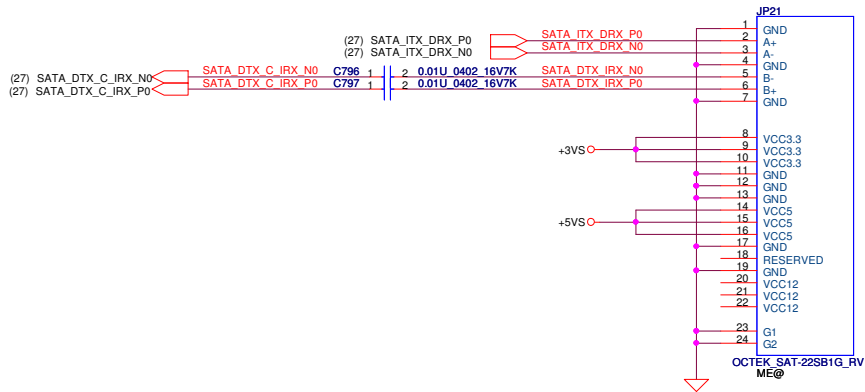


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								Compal Electronics, Inc.			
								BCM5906			
Size				Document Number				KIWA5/6 LA-5081P			
Date:				Tuesday, April 28, 2009				Rev 1.0			
								Sheet 31 of 51			

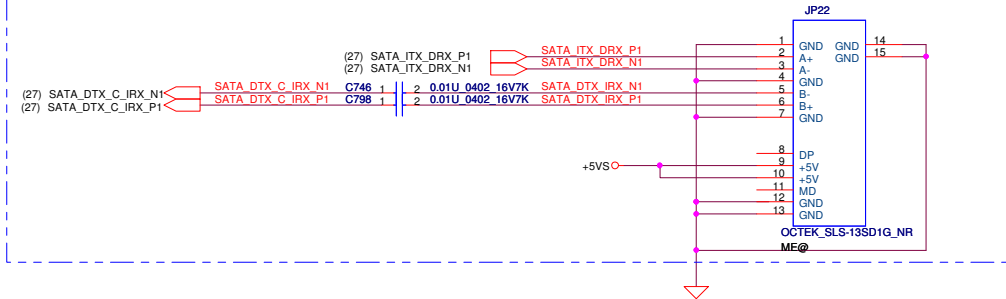




### SATA HDD Conn.



### SATA ODD Conn.



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				Size B	Document Number	Rev
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				Date:	Tuesday, April 28, 2009	Sheet 33 of 51

0308\_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

**For Layout:**  
Place decoupling caps near the power pins of SmartAMC device.



**B control**

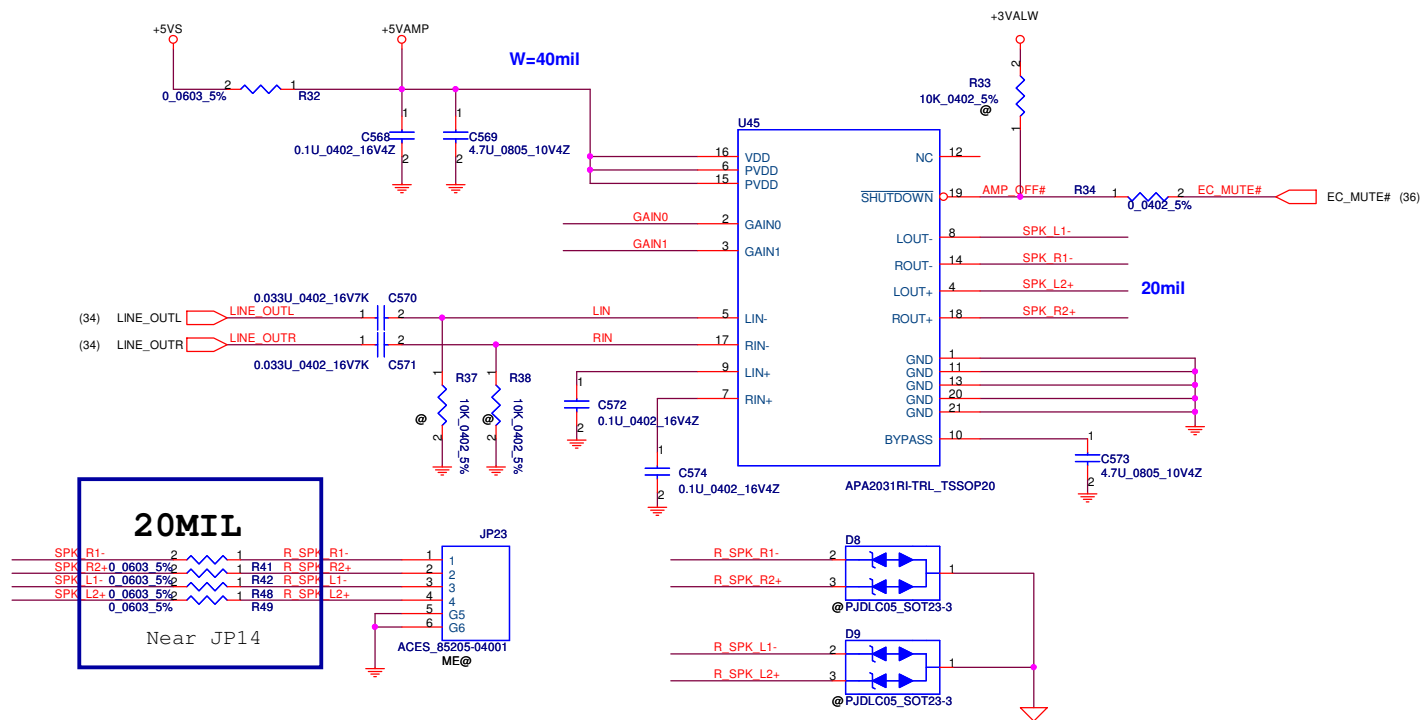
R1056

0216\_Change value.

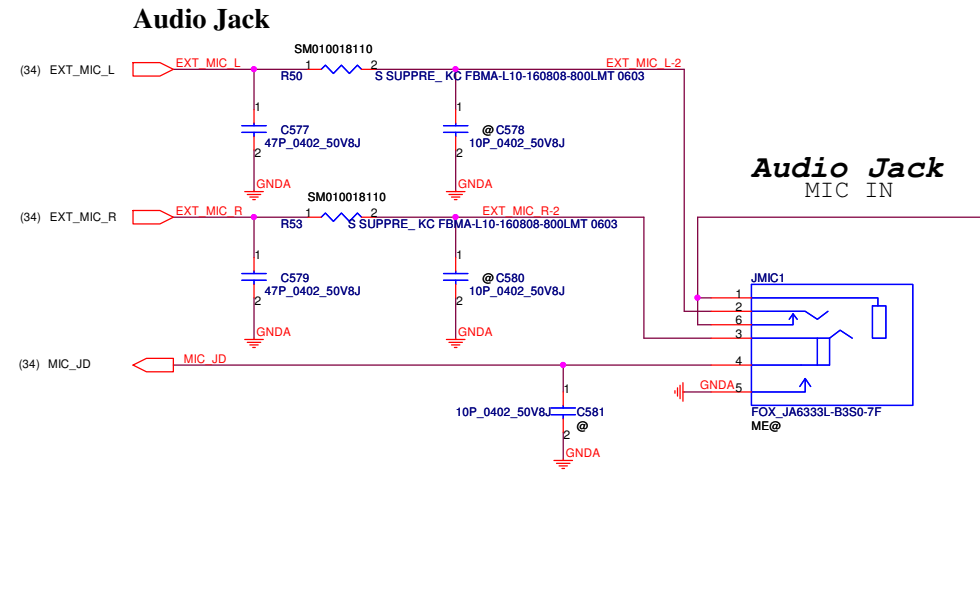
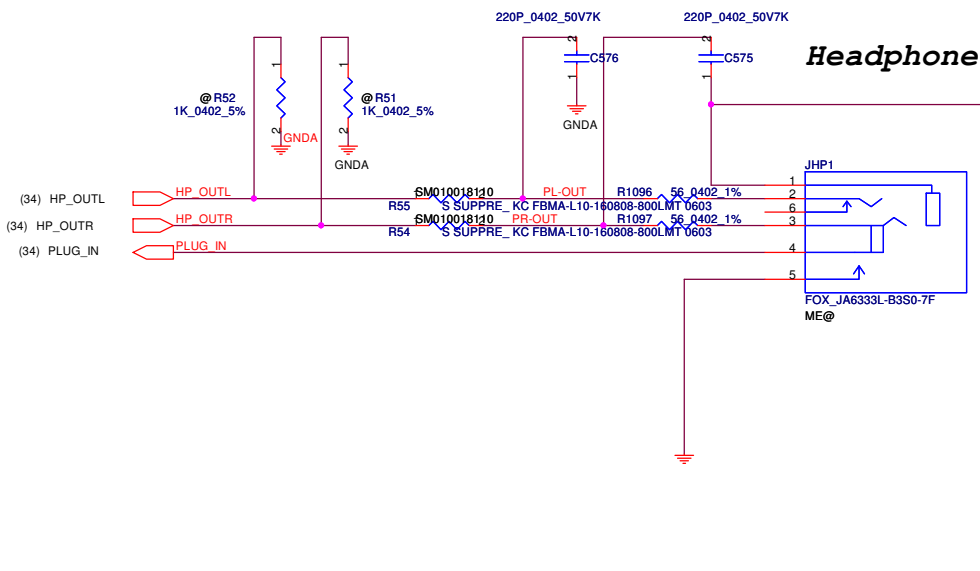
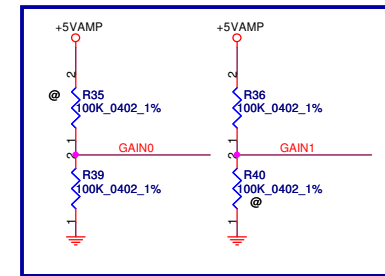
Place these C and R around AGND and DGND,  
then choose the one which is close to Codec  
to mutate

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Size		Document Number				Rev 1.0
Custom		KJWA/6 LA-5081P				
Date:		Tuesday, April 28, 2009		Sheet 34 of 51		

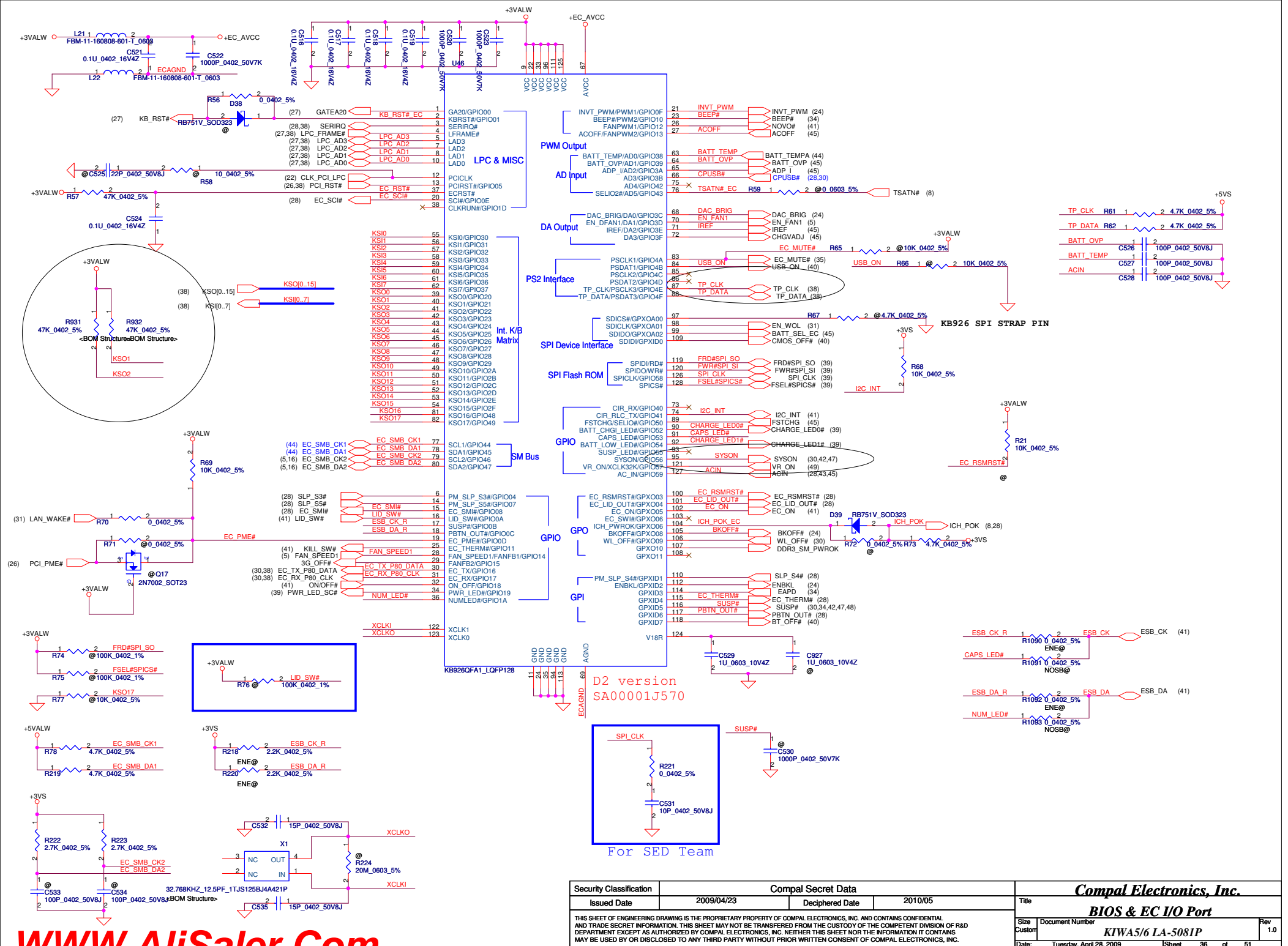
# Speaker Connector



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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				Custom	KIWA5/6 LA-5081P
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				Rev	1.0



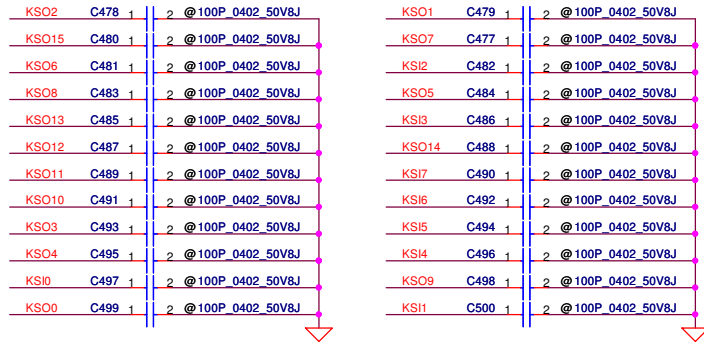




Source:SP010001E00  
2nd source:SP010001F00  
30 pin

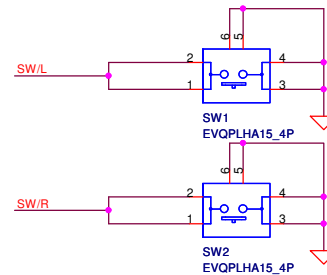
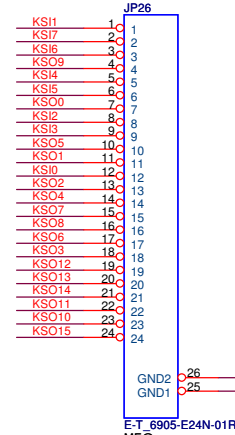
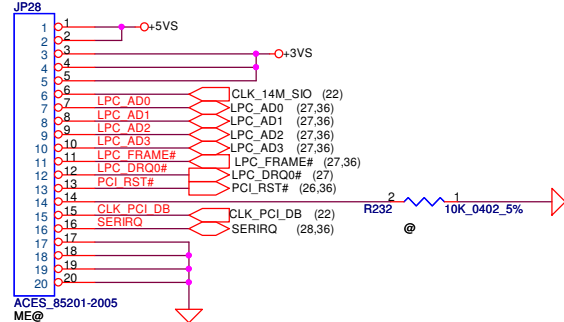
## INT\_KBD Conn.

KS[0..7] (36)  
KSO[0..15] (36)

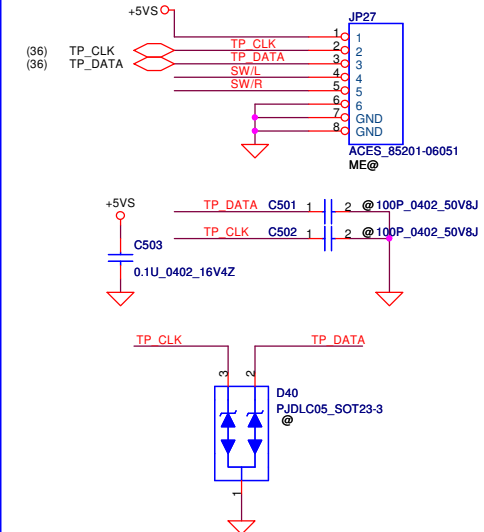
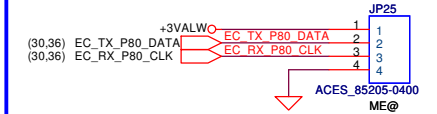


CONN PIN define need double check

## FOR LPC SIO DEBUG PORT

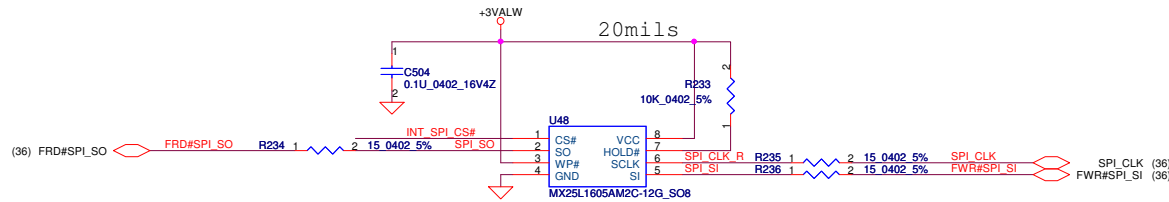


## EC DEBUG PORT

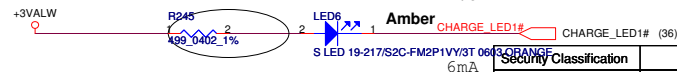
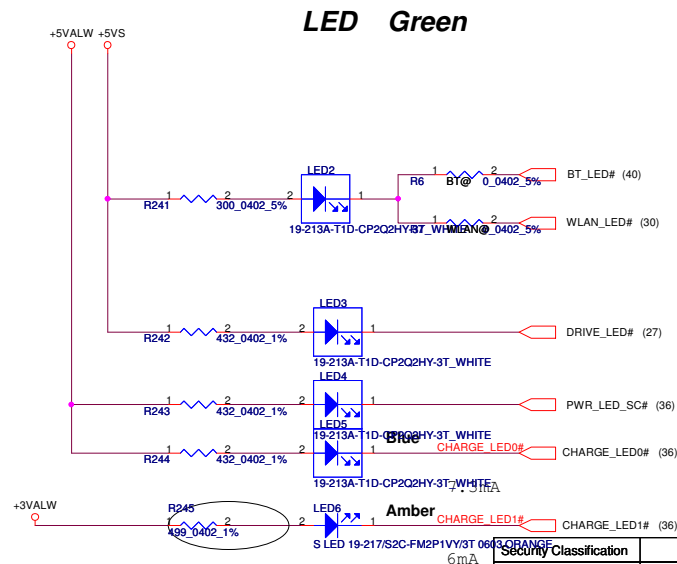
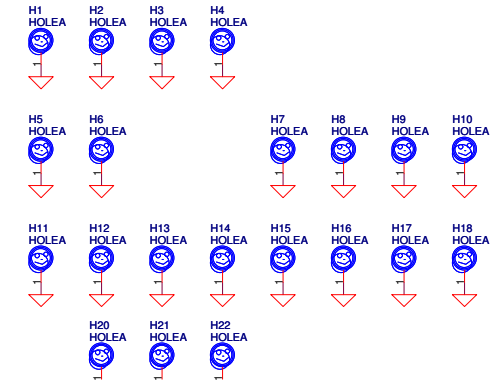
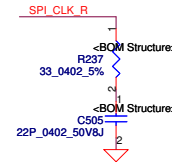
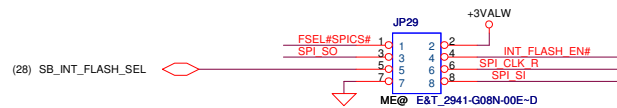
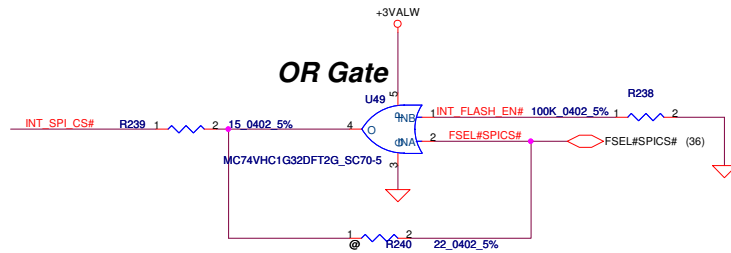


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				Date: Tuesday, April 28, 2009	Rev 1.0
				Sheet 38	of 51

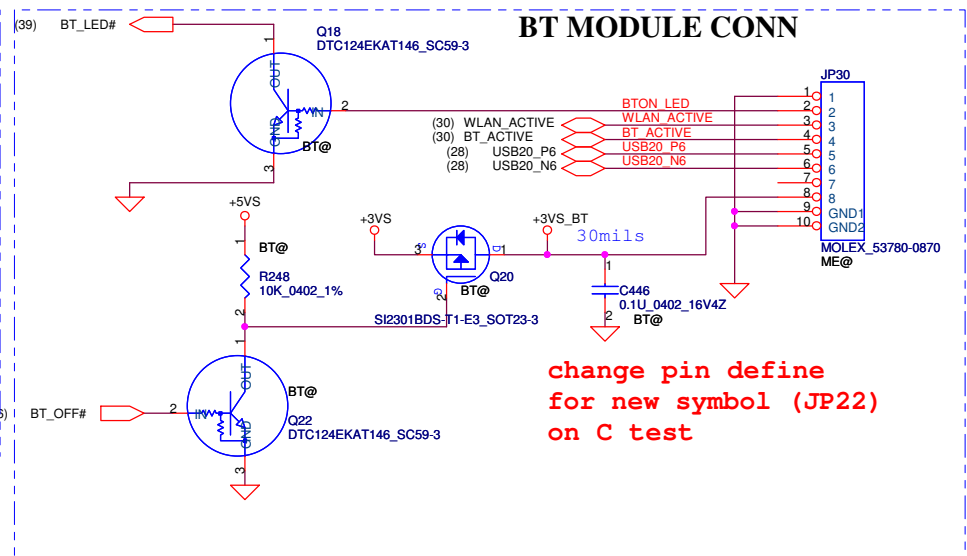
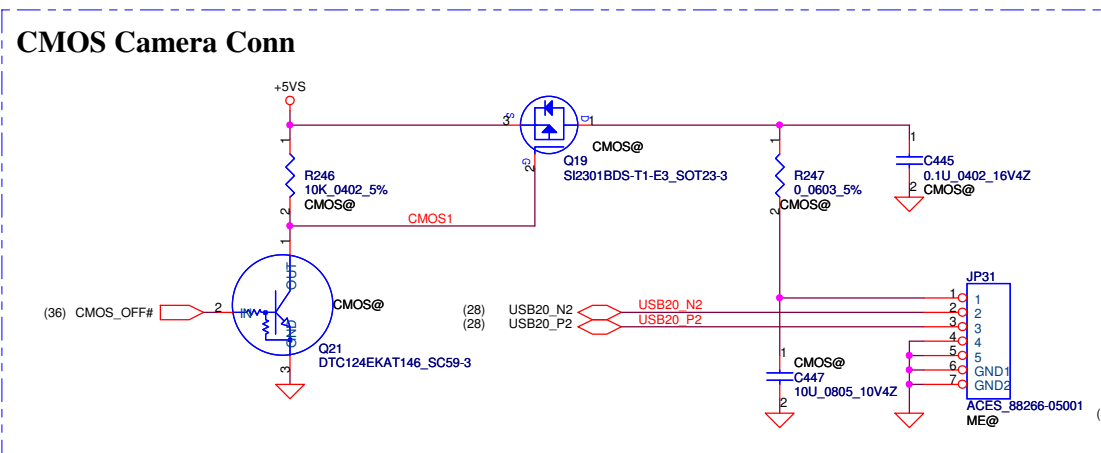
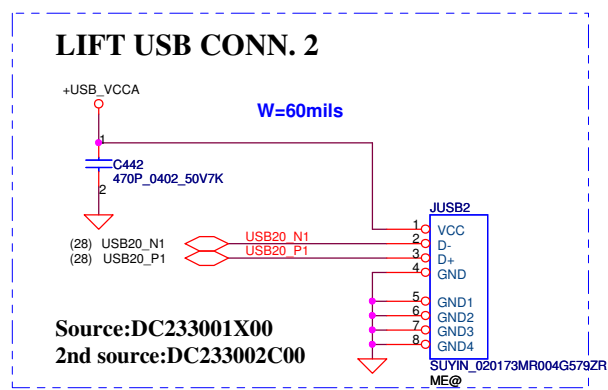
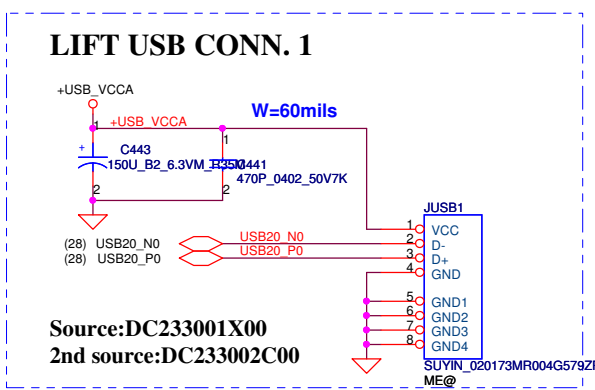
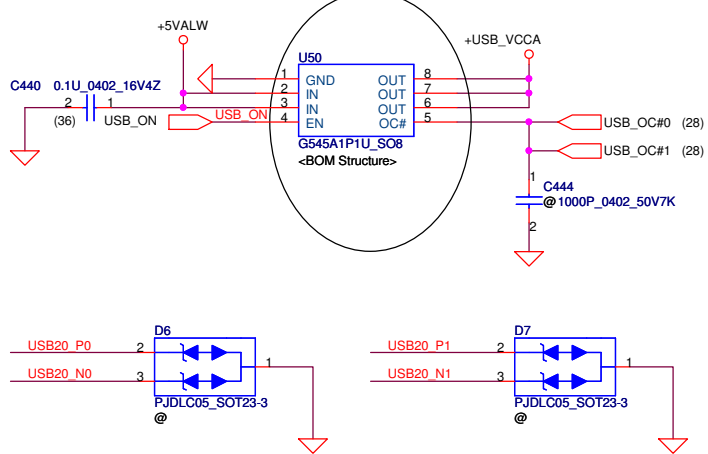
# FOR EC 16M SPI ROM



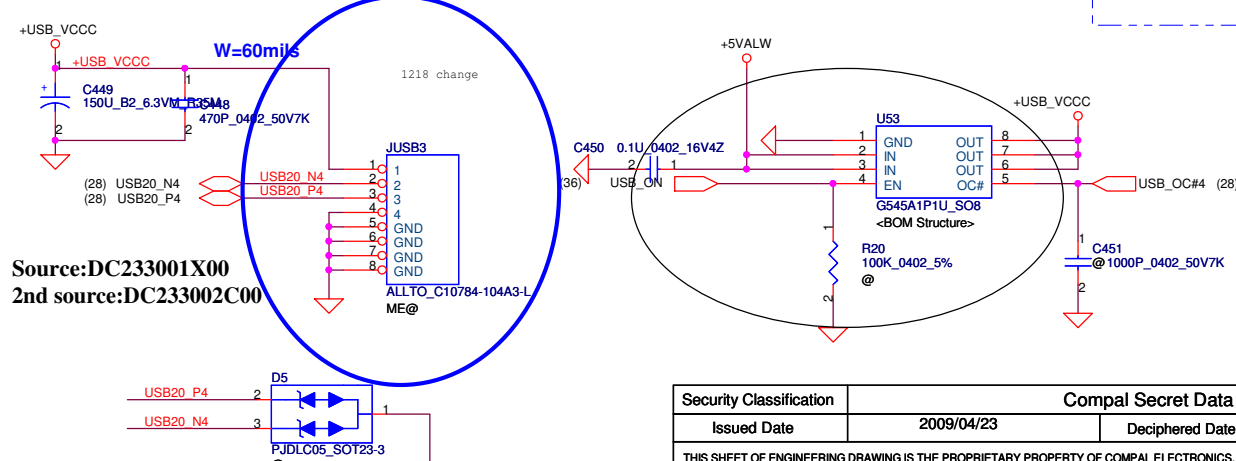
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H



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				Size B	Document Number	Rev
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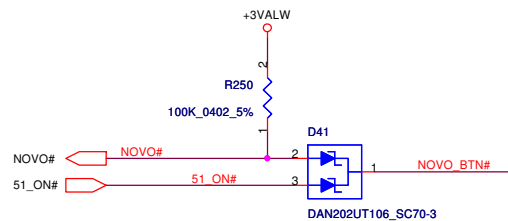


### LIFT USB CONN. 1



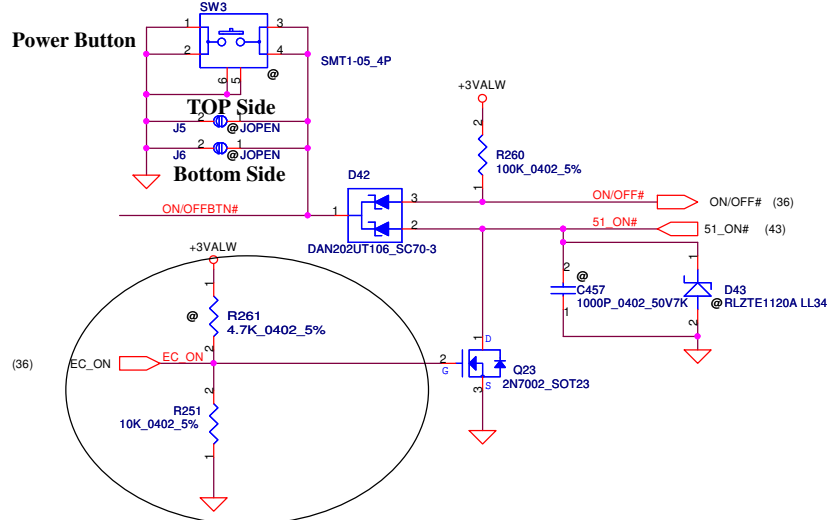
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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(36)  
(43)

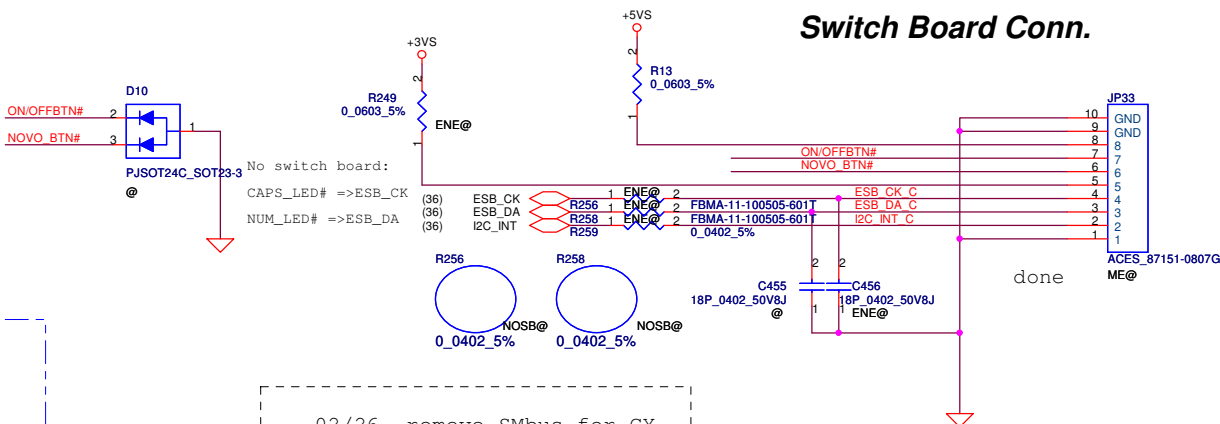
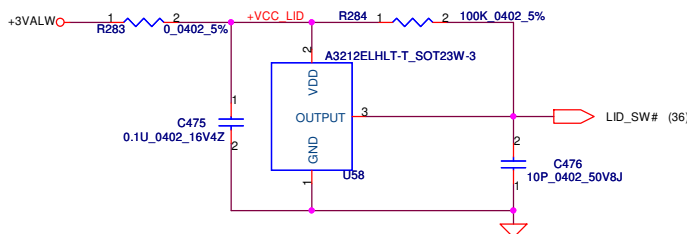


## ON/OFF switch

### Power Button

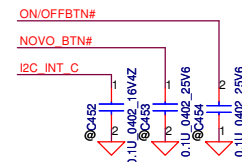
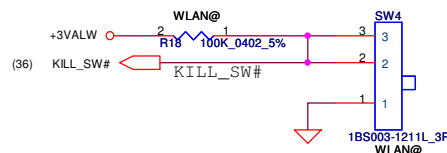


## Lid Switch



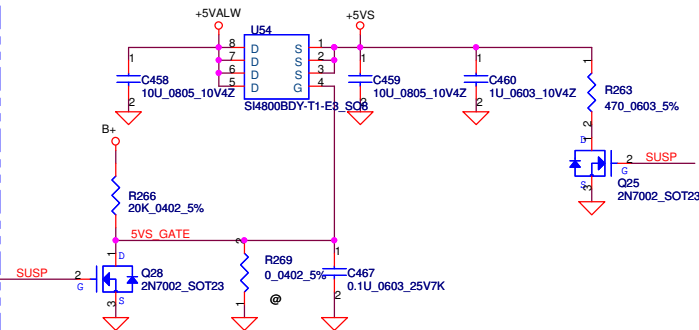
02/26 remove SMBus for CY

## Kill Switch

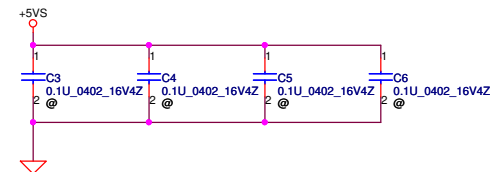
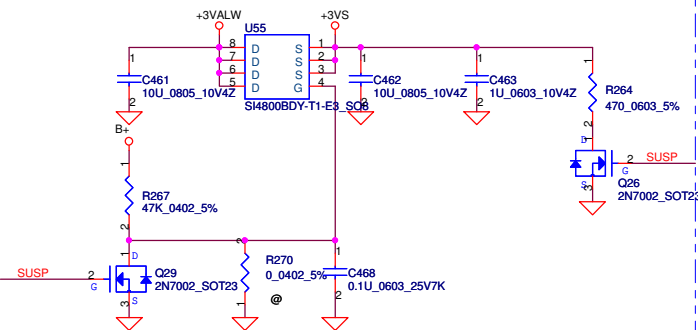


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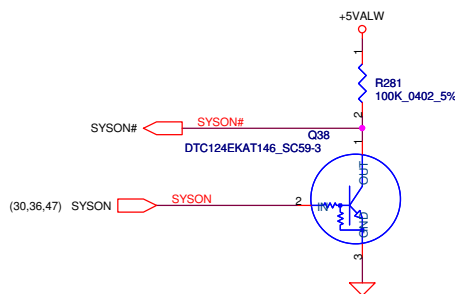
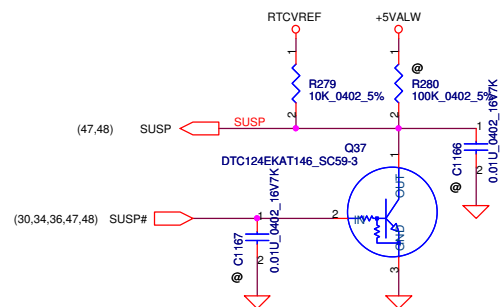
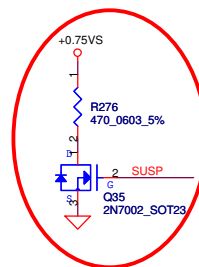
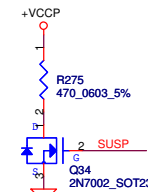
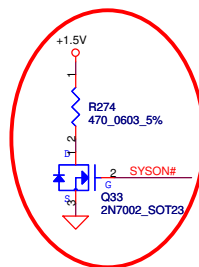
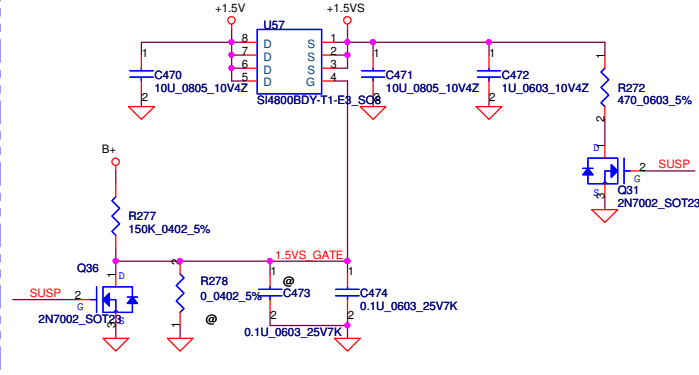
# +5VALW TO +5VS



# +3VALW TO +3VS

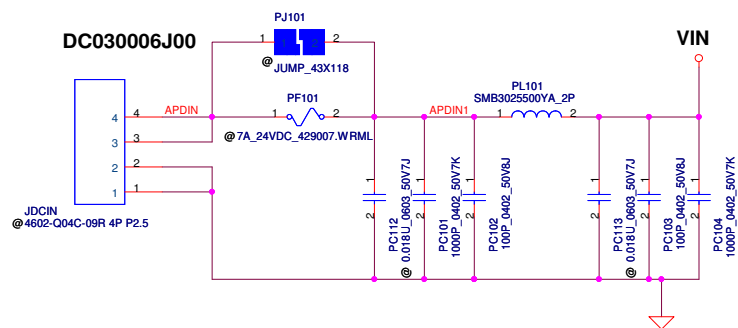


# +1.5V to +1.5VS



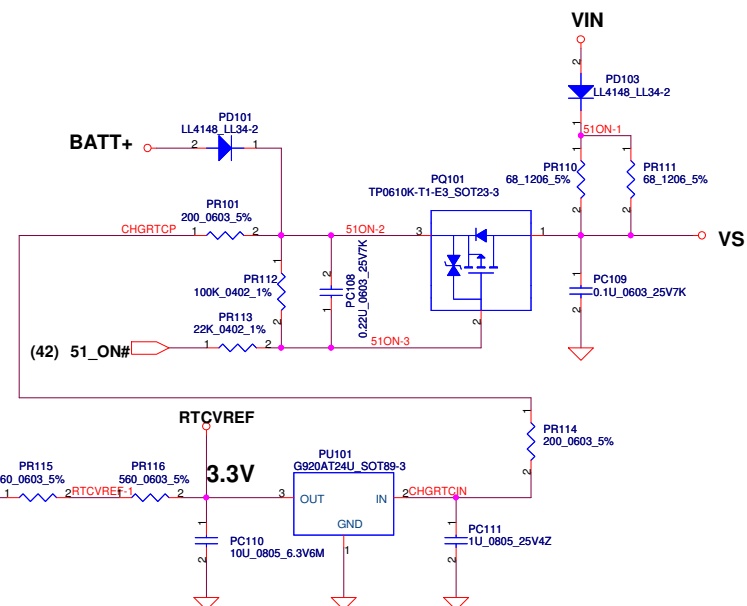
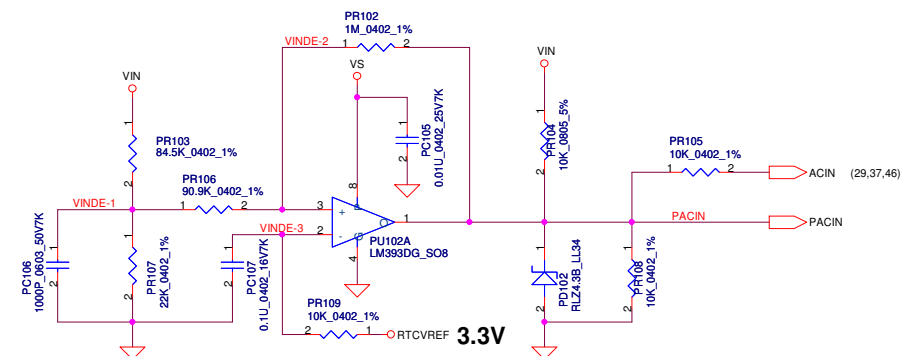
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Customer						1.0
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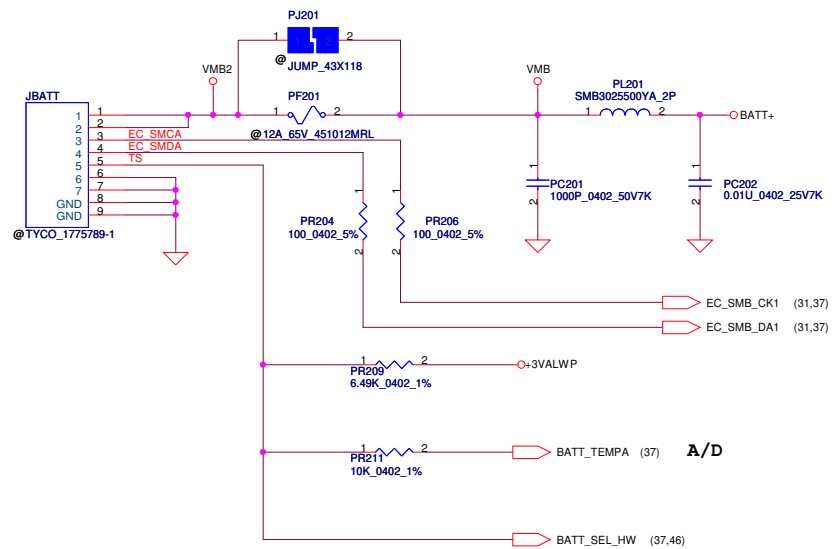


### Vin Detector

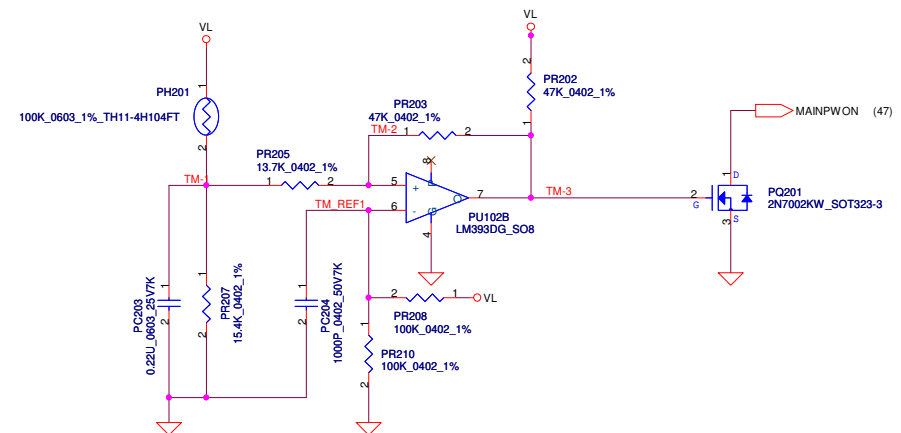
High	17.944	17.706	17.470
Low	16.242	16.027	15.808



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Size	Document Number	Custom	Rev	Date: Tuesday, April 28, 2009	
			0.1	Sheet 44 of 53	

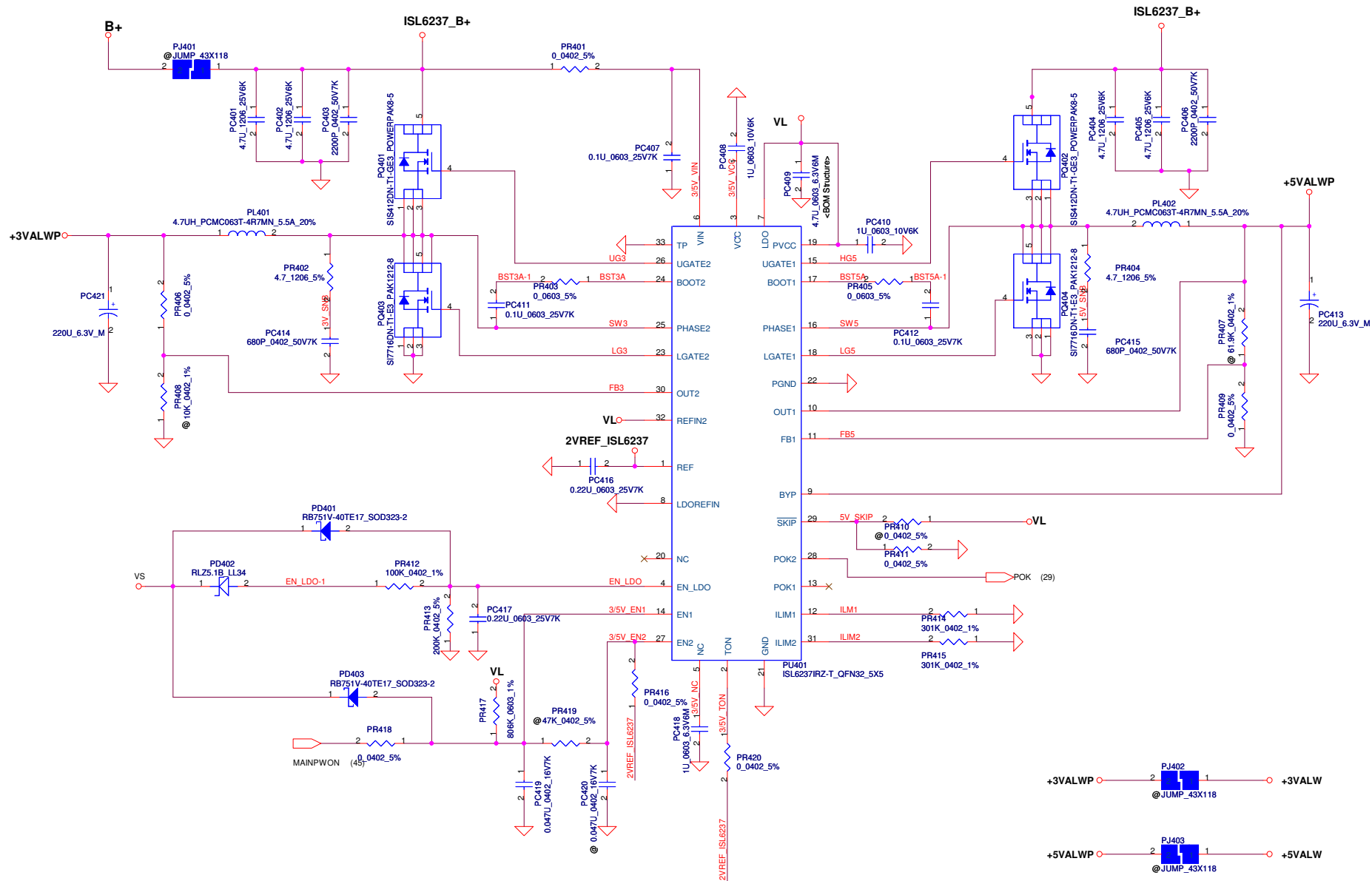


PH1 under CPU bottom side :  
CPU thermal protection at 92 degree C  
Recovery at 56 degree C



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		0.1		Sheet 45 of 53	



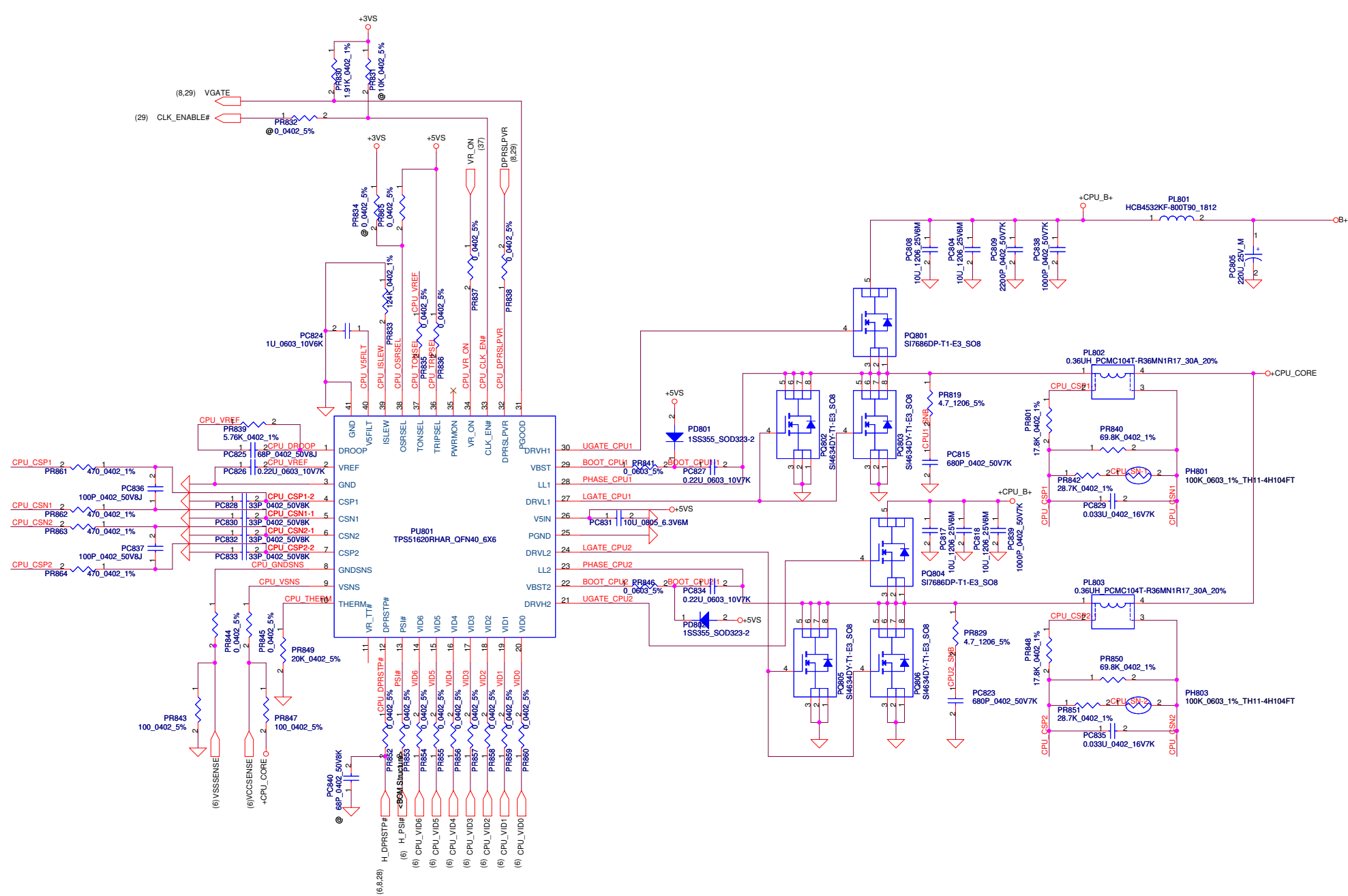


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## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)	2009.01.14	
3							
4							
5							
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20							
21							

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