LZ2 Block Diagram

Project code: 91.4K101.001 ZY LZ2
91.4J301.001 XR LX2
PCB P/N : 07260-SB
Revision : SA

CLK GEN. 3

Mobile CPU
Penryn SV 35W
4, 5

EMC2102 07

HOST BUS 800/1066MHz@1.05V

DDR3 socket 15 — 800/1066MHz

DDR3 socket 16 — 800/1066MHz

Cantiga 8,9,10,11,12,13,14
- AGTL+ CPU I/F
- DDR Memory I/F
- INTEGRATED GRAHPICS
- LVDS, CRT I/F

R.G.B → CRT 18

LVDS → 12"W LCD 17

X4 DMI 400MHz

C-Link0

ICH9M 19,20,21,22,23
- 6 PCIe ports
- PCI/PCI BRIDGE
- ACPI 1.1
- 4 SATA
- 12 USB
- High Definition Audio
- LPC I/F
- Serial Peripheral I/F

INT MIC

SPR x2

Codec ALC269 (include AMP) 25 — AZALIA

MIC In

HP

RJ11 — MODEM MDC Card 24

USB → Realtek RTS5158E Cardreader 28 → SD/MMC/MS 3 in 1 28

PCIe → LAN Boardcom 5906M 26 → RJ45 27

PCIe/ USB → Mini Card a/b/g/n 31

LPC BUS

New card 31 — PCI Express / USB

Power switch 31

SATA → SATA-HDD 24

SATA → SATA-ODD 24

USB → USB 3 Port 32

Finger Print 32

BlueTooth 24

CAMERA 17

KBC Winbond WPC776 29 — SPI I/F
- G-sensor 30
- Touch Pad 34
- INT. KB 34
- BIOS 2M byte 34

LPC DEBUG CONN. 24

PCB 8-LAYER STACKUP

TOP
GND
S
S
PWR
S
GND
BOTTOM

SYSTEM DC/DC TPS51120 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S3

TPS51100 38

1D5V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
1D5V_S3	33 1D5V_S0

CHARGER BQ24740 39

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V UP+5V 5V 100mA

CPU DC/DC ADP3208 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size: A3 | Document Number: LZ2 | Rev: SB

Date: Friday, April 11, 2008 | Sheet 1 of 41

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved Rising Edge of PWROK.	This signal has a weak internal pull-down. Note:This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap(Server Only) Rising edge of PWROK	Tying this strap low configures DMI for SIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server latforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG11 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1= The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE1	BroadCom LAN
LANE2	MiniCard WLAN
LANE4	NewCard

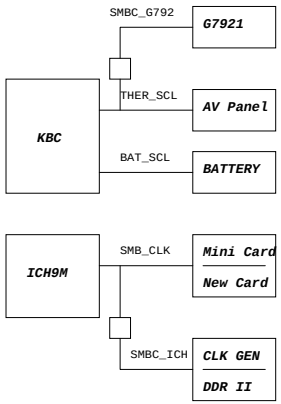
History:

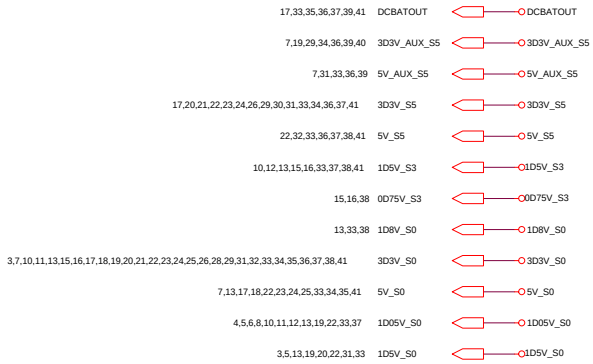
LAB: 2008/01/02

USB Table

USB	
Pair	Device
0	JACK0
1	NC
2	JACK2
3	NC
4	BLUETOOTH
5	JACK1
6	Fringer Print
7	Mini Card
8	CAMERA
9	NEW CARD
10	CARDREADER
11	NC

SMBus





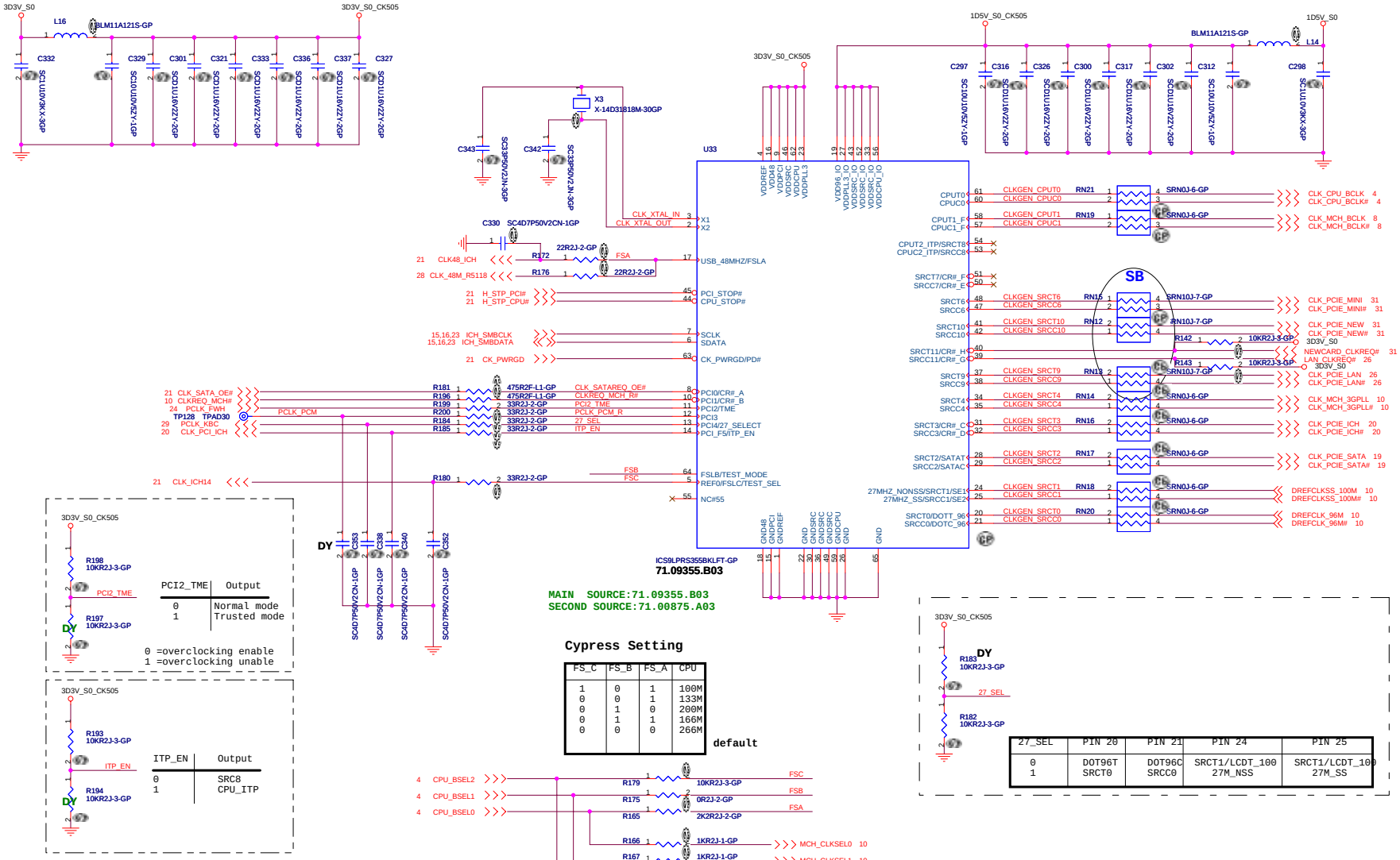
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 2 of 41



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

Wistron Corporation
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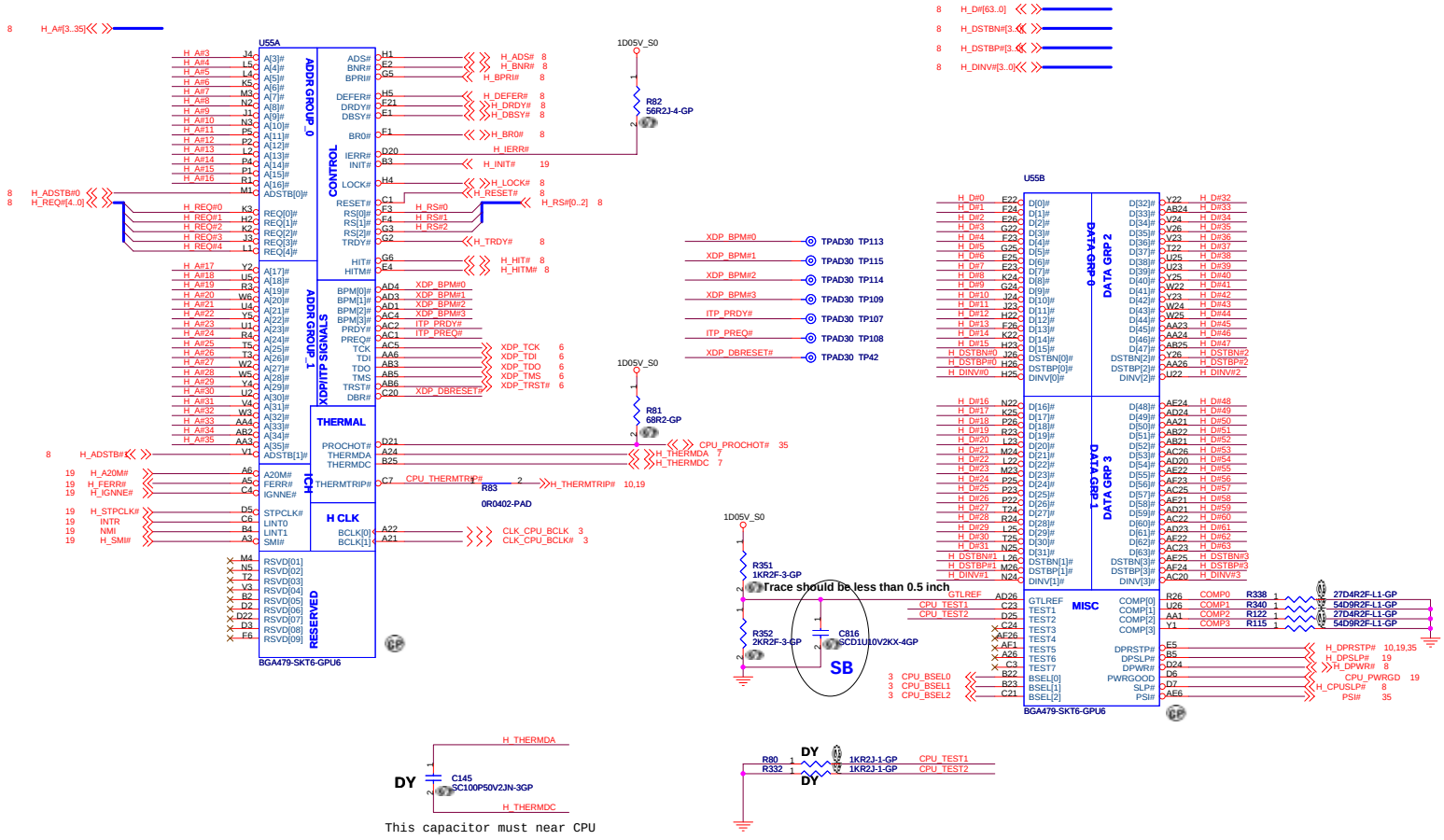
Title: Clock Generator

Size	Document Number	Rev
	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 3 of 41



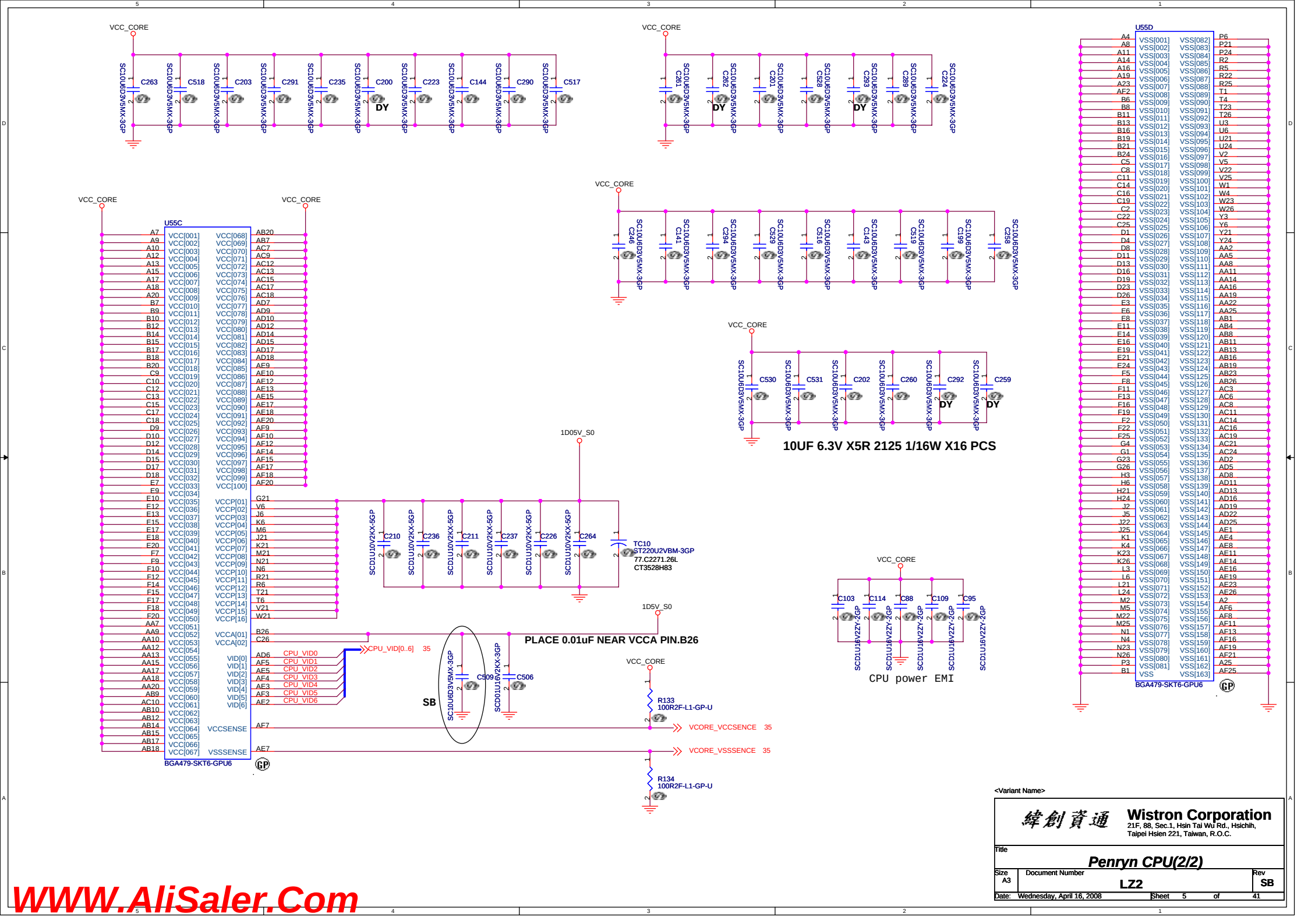
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Penryn CPU(1/2)

Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 4 of 41



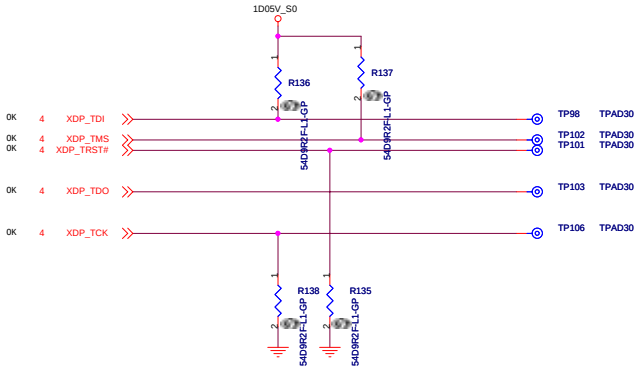
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Penryn CPU(2/2)

Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 5 of 41



<Variant Name>

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP CONN

Size: C | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 | Sheet 6 of 41

Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing

Layout notice :
Both H_THERMDA_1 and THERMDC_1 routing
10 mil trace width and 10 mil spacing

Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing

Layout notice :
C809, C811, C812
close to chip side;

CPU0

SYSTEM

This cap should close to thermal diode.

Layout 15 mil

EMC2102

SC

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)

220ms delay time after Power-on

Dummy when G792 enhanced T8 function

HW thermal shut down tempature
setting 95 degree . Put Near CPU .

Rset=0.0012*T^2-0.9308*T+96.147

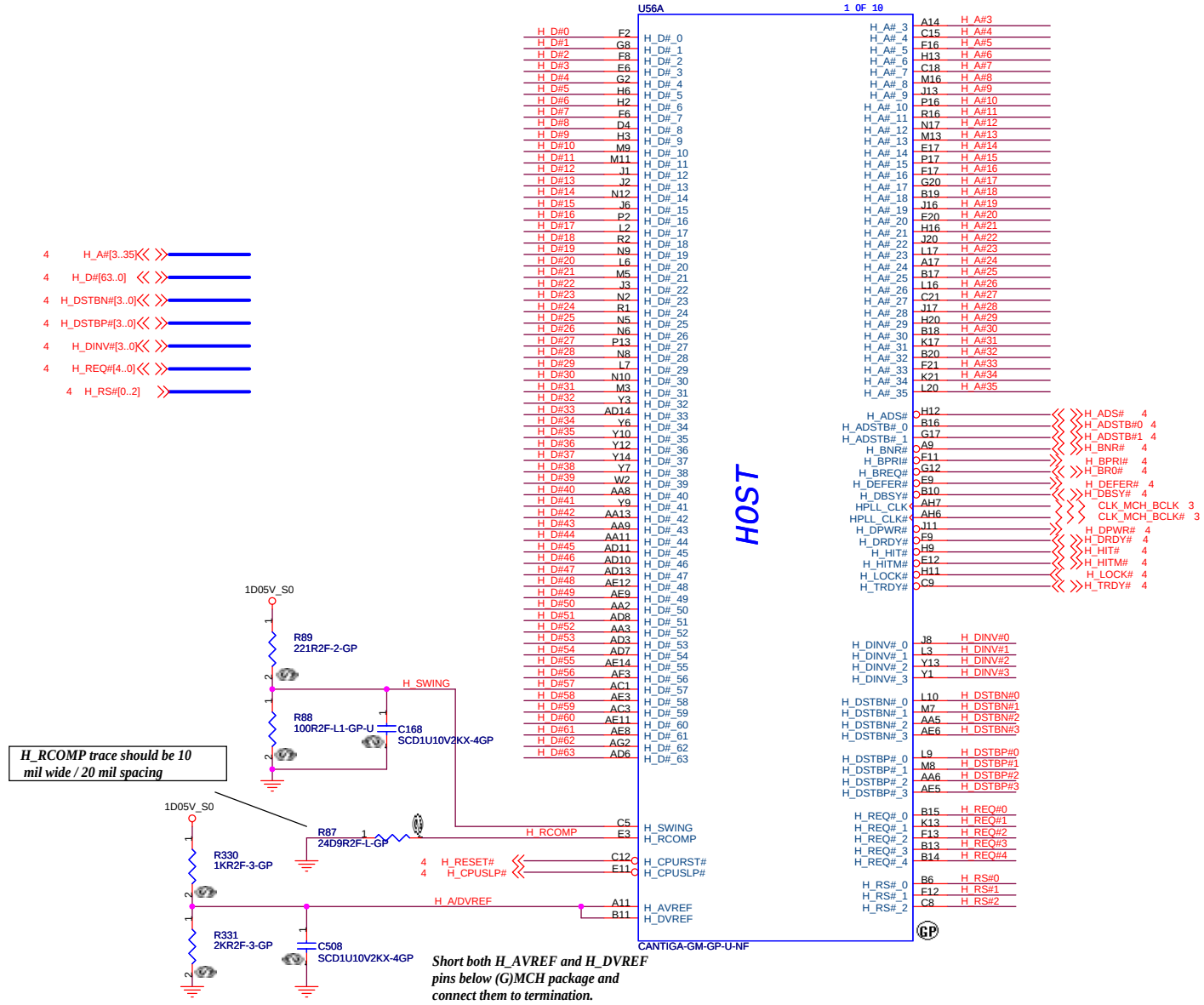
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 | Sheet 7 of 41



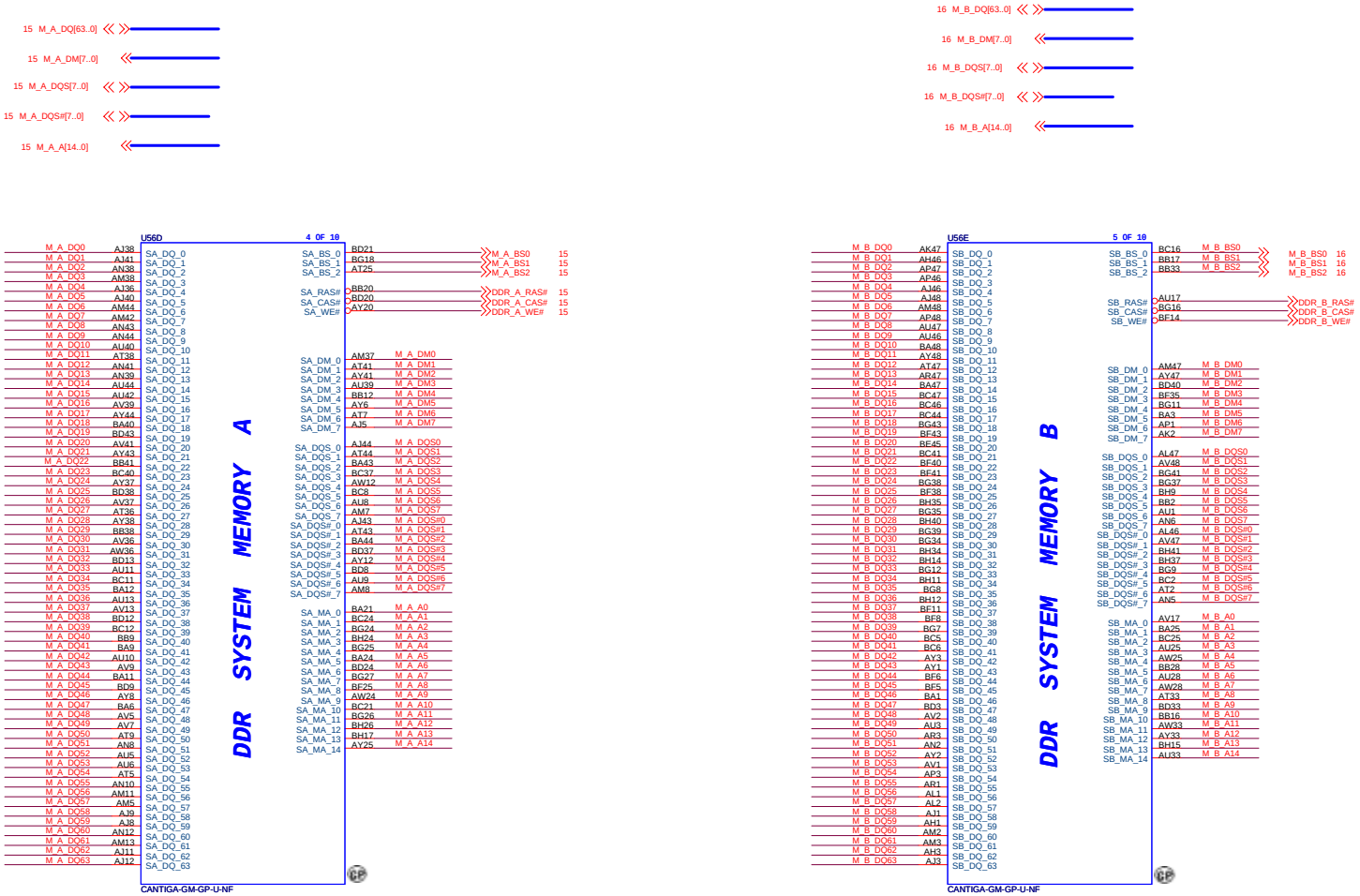
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(1/7):HOST I/F

Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 8 of 41



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蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Cantiga(2/7):DDR3		
Size C	Document Number LZ2		Rev SB
Date: Wednesday, April 16, 2008	Sheet 9	of	41

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown

U56B — 2 OF 10

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC
HDA

CANTIGA-GM-GP-U-NF

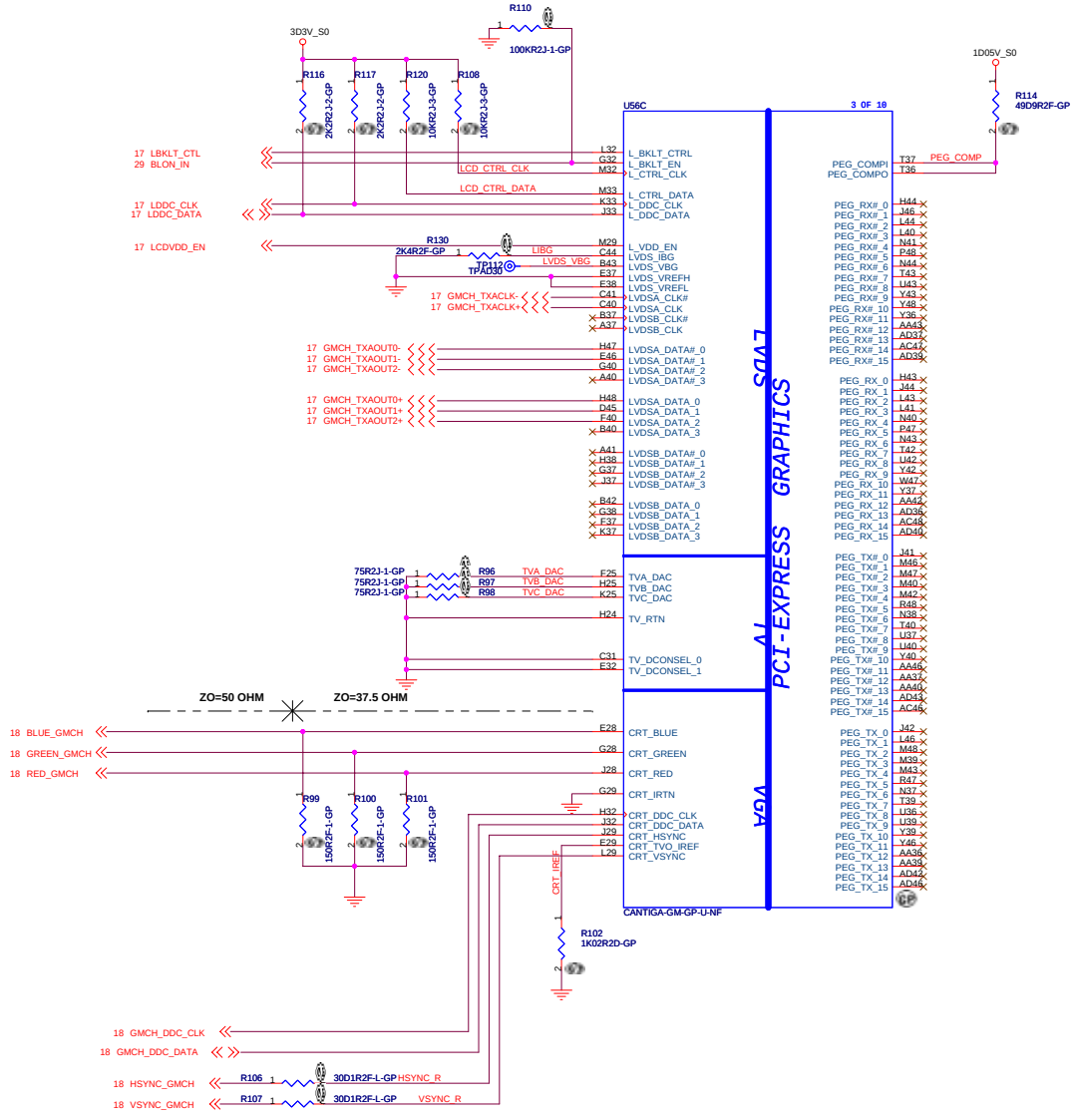
SM_REXT:Constant circuit reference for clocks.

INTEL Suggest use 511

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(3/7):DMI/PM/CFG/GF
Size: C | Document Number: LZ2 | Rev: SB
Date: Wednesday, April 16, 2008 | Sheet 10 of 41



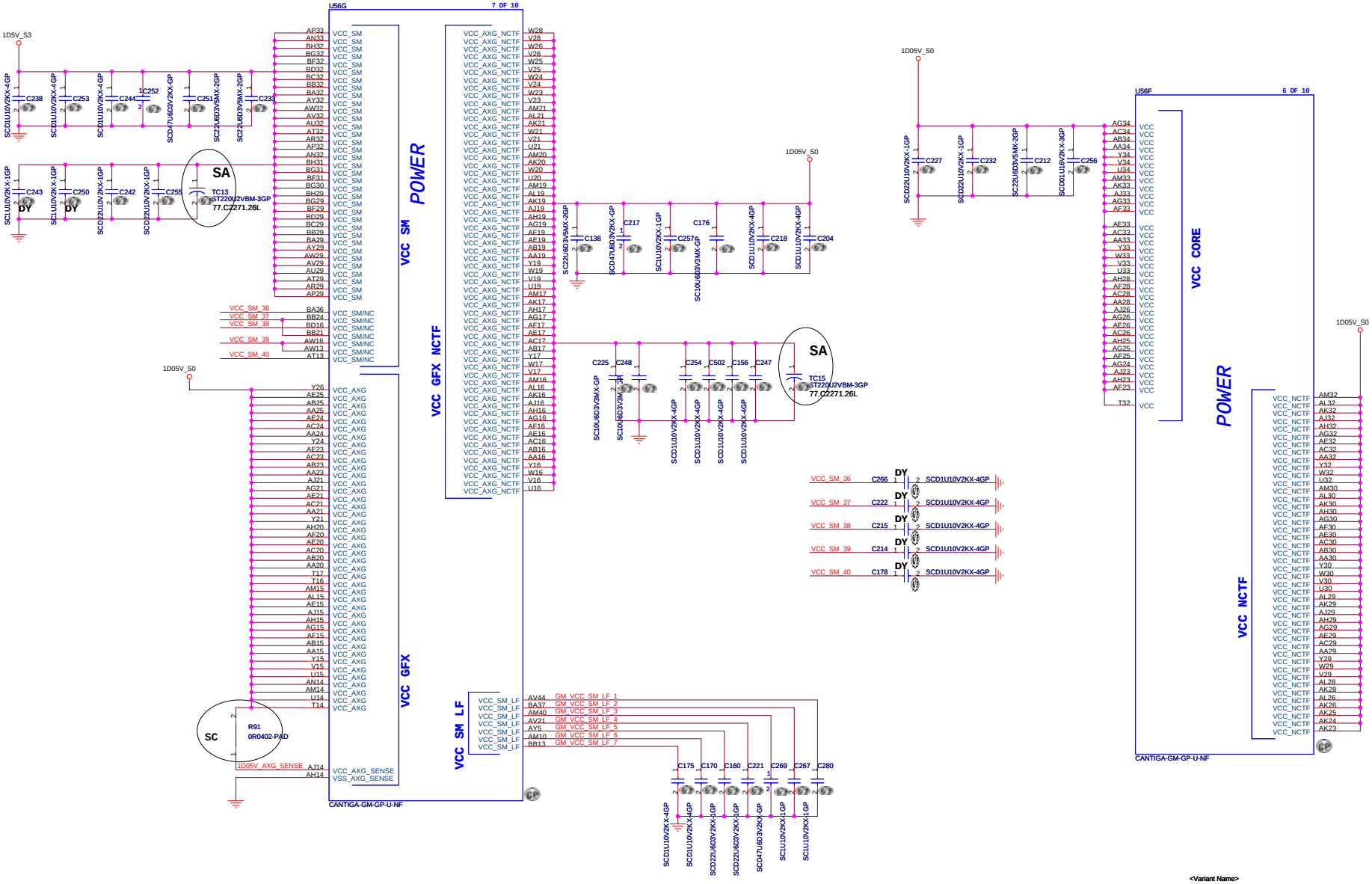
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CANTIGA(5/7)-VGA/LVDS

Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 16, 2008 Sheet 11 of 41



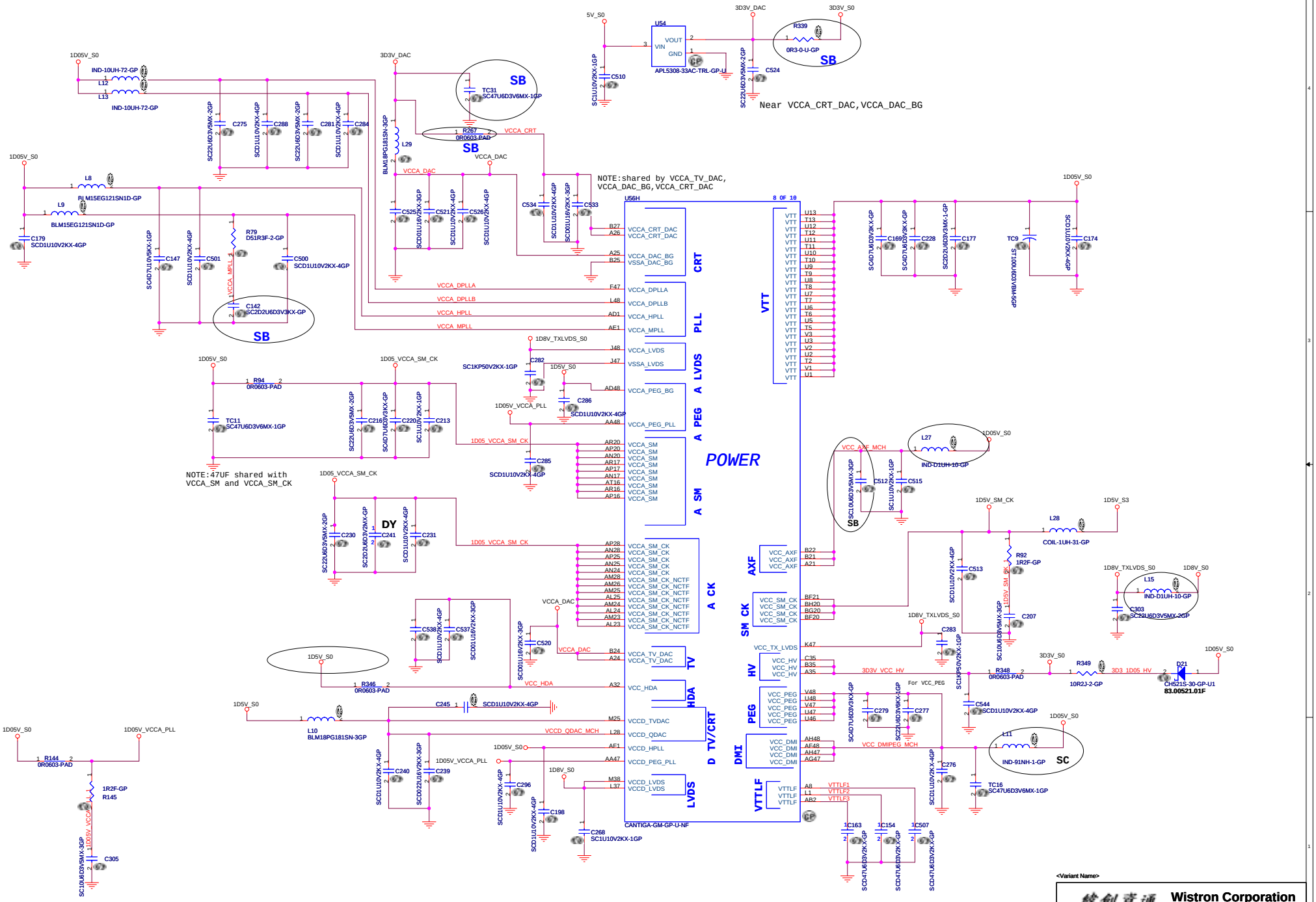
<Variant Name>

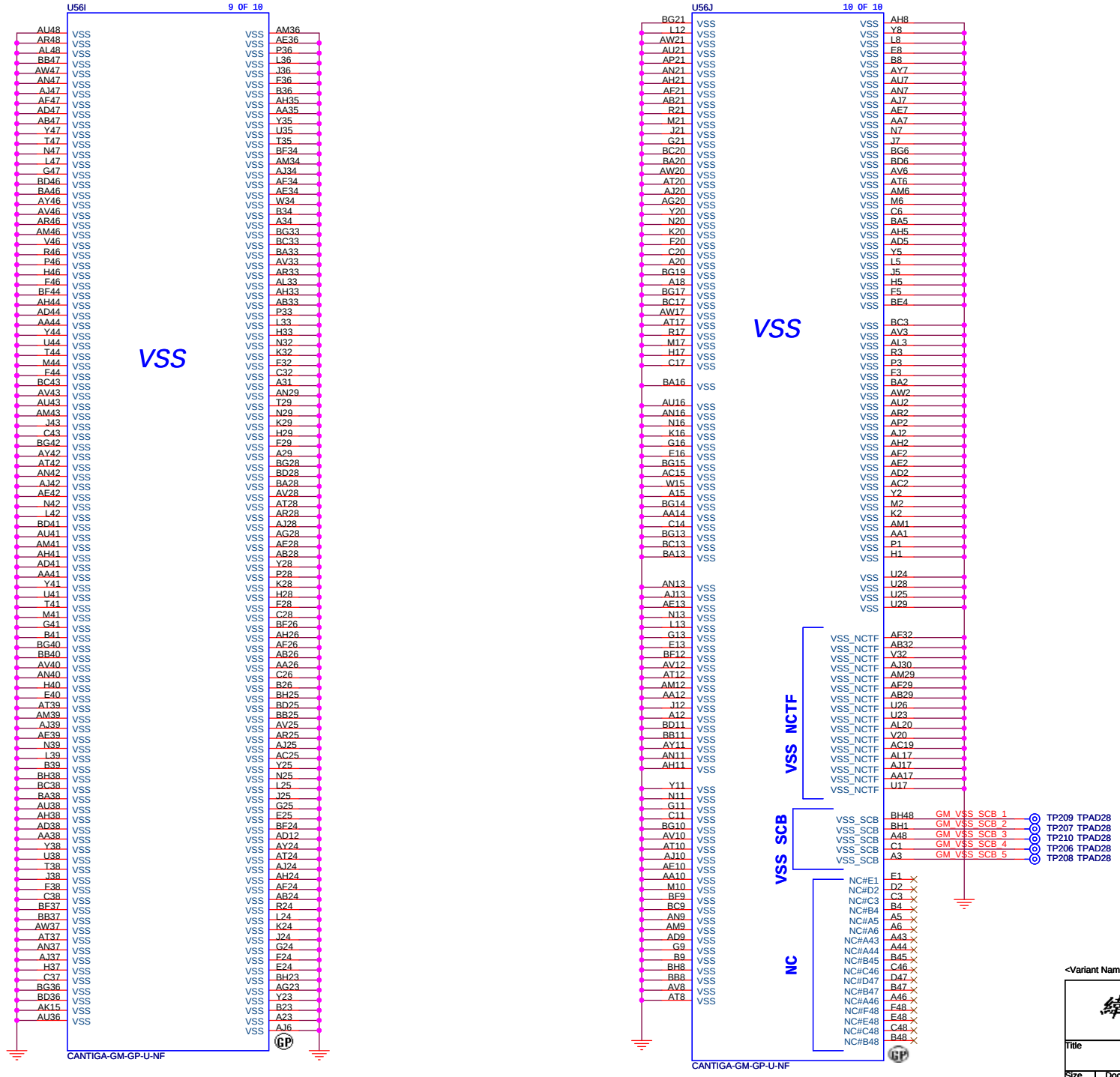
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(5/7):VCC

Size	Document Number	Rev
C	LZ2	SB

Date: Friday, April 11, 2008 Sheet 12 of 41





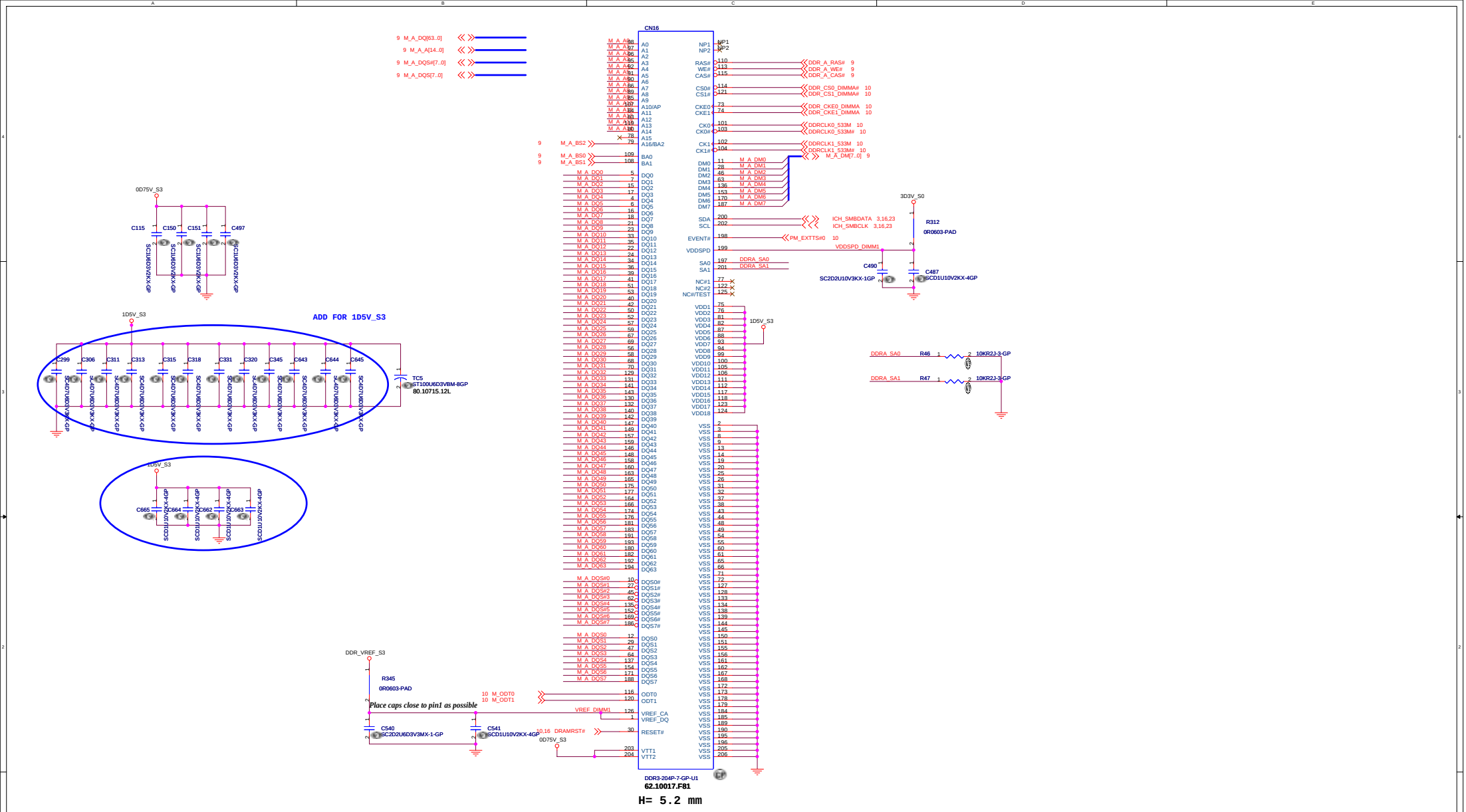
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(8/7):GND

Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 09, 2008 Sheet 14 of 41



<Variant Name>

Wistron Corporation
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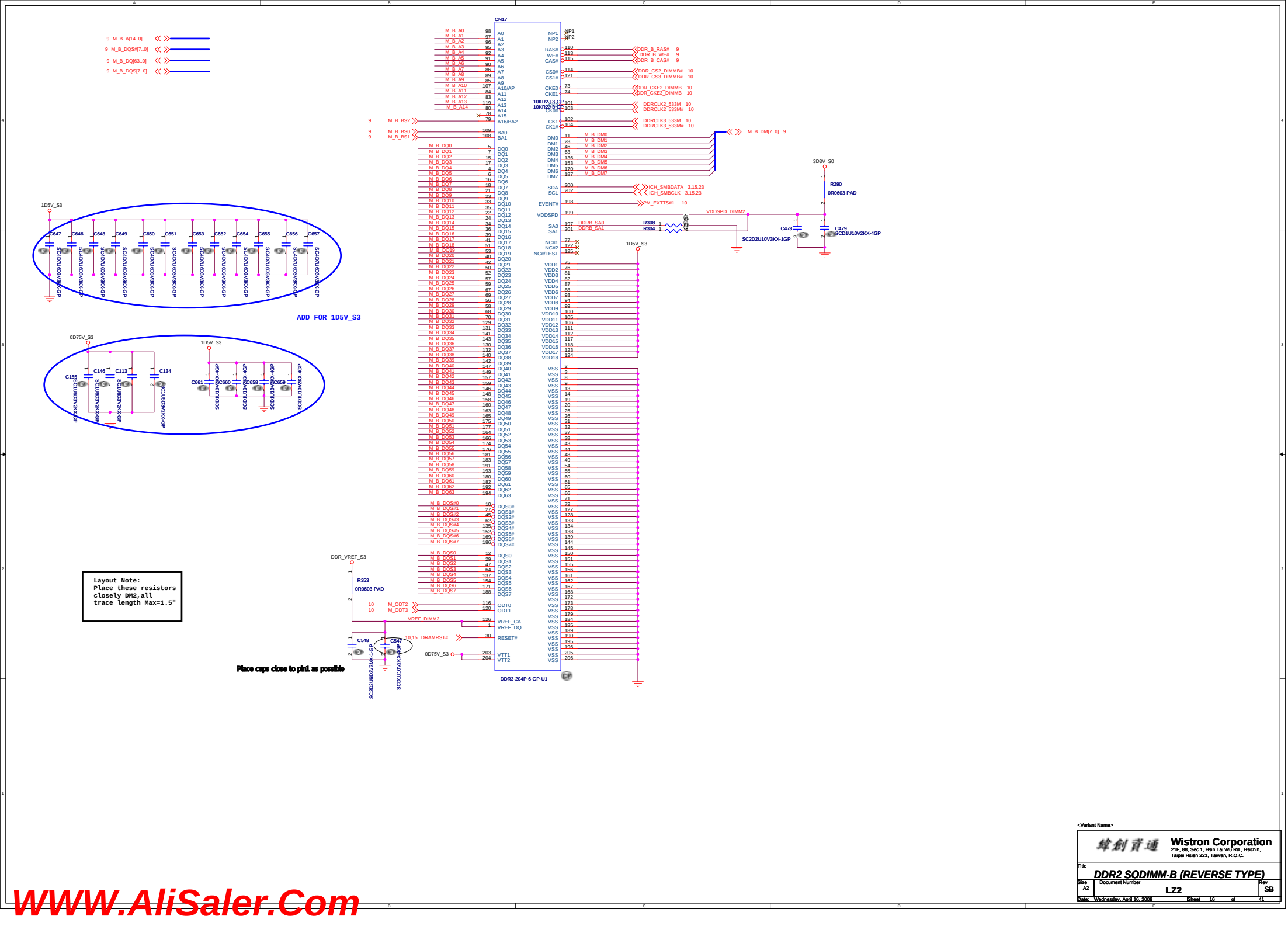
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SODIMM-A (NORMAL TYPE)

Size: A2 | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 | Sheet 15 of 41



<Variant Name>

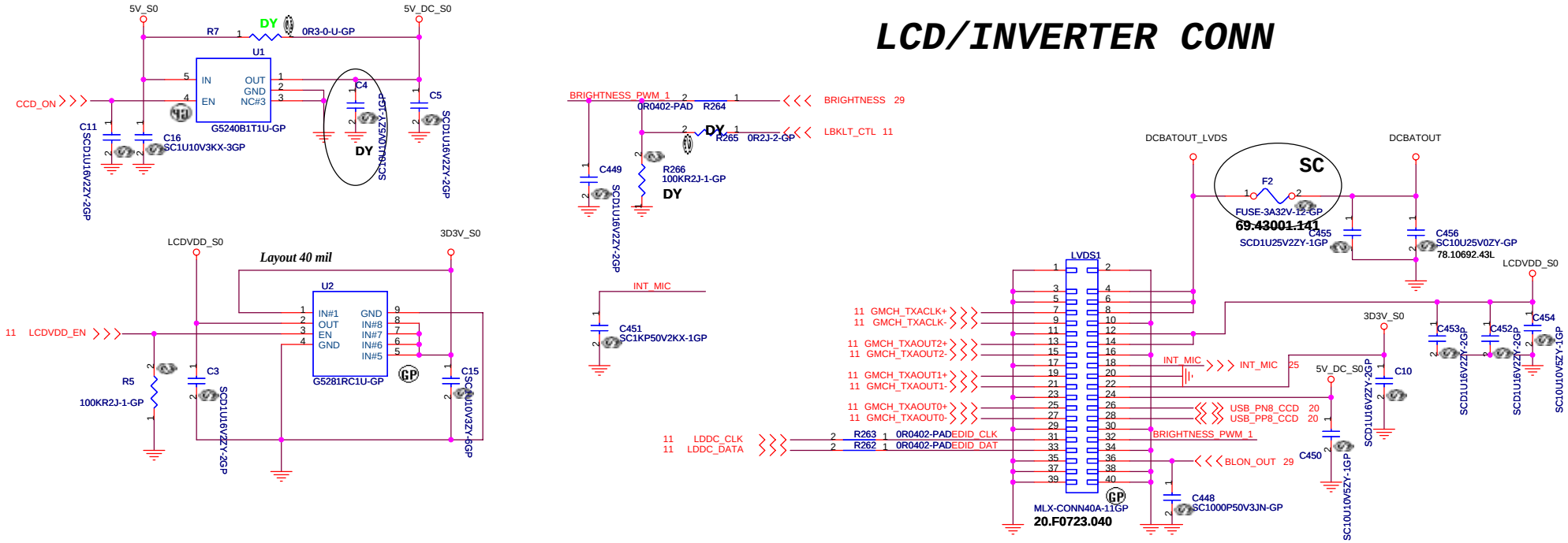
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SODIMM-B (REVERSE TYPE)

Size: A2 | Document Number: LZ2 | Rev: SB

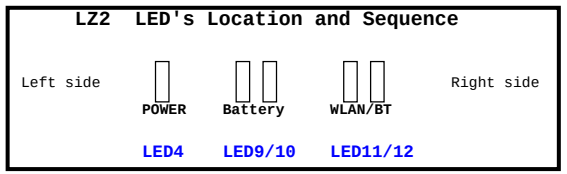
Date: Wednesday, April 16, 2008 | Sheet 16 of 41

LCD/INVERTER CONN

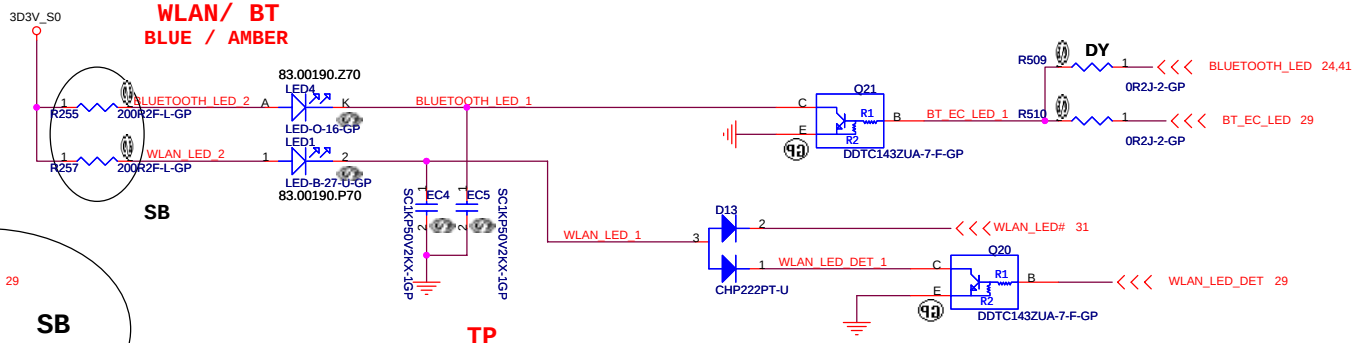


M/B LED

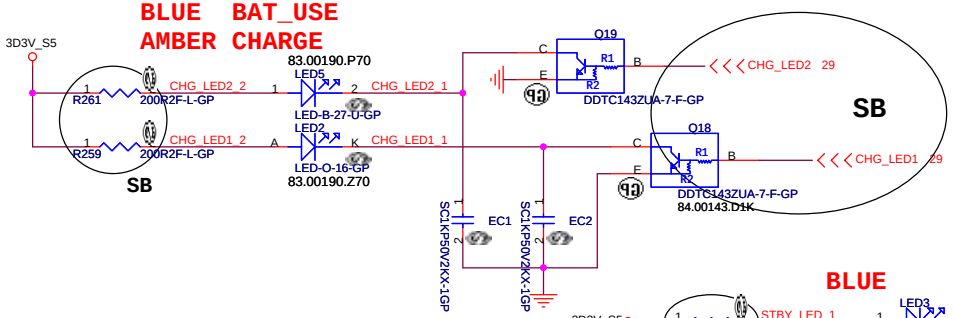
LZ2 LED's Location and Sequence



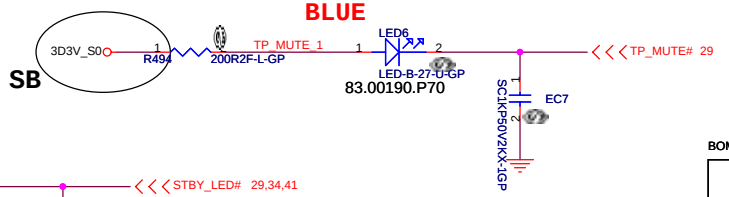
WLAN/ BT
BLUE / AMBER



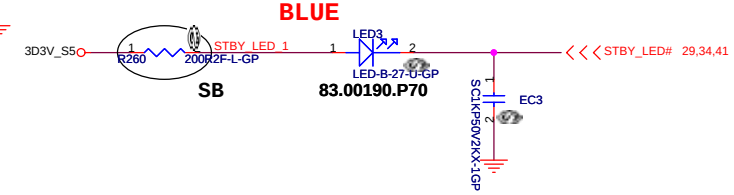
BLUE BAT_USE
AMBER CHARGE



TP
BLUE



BLUE



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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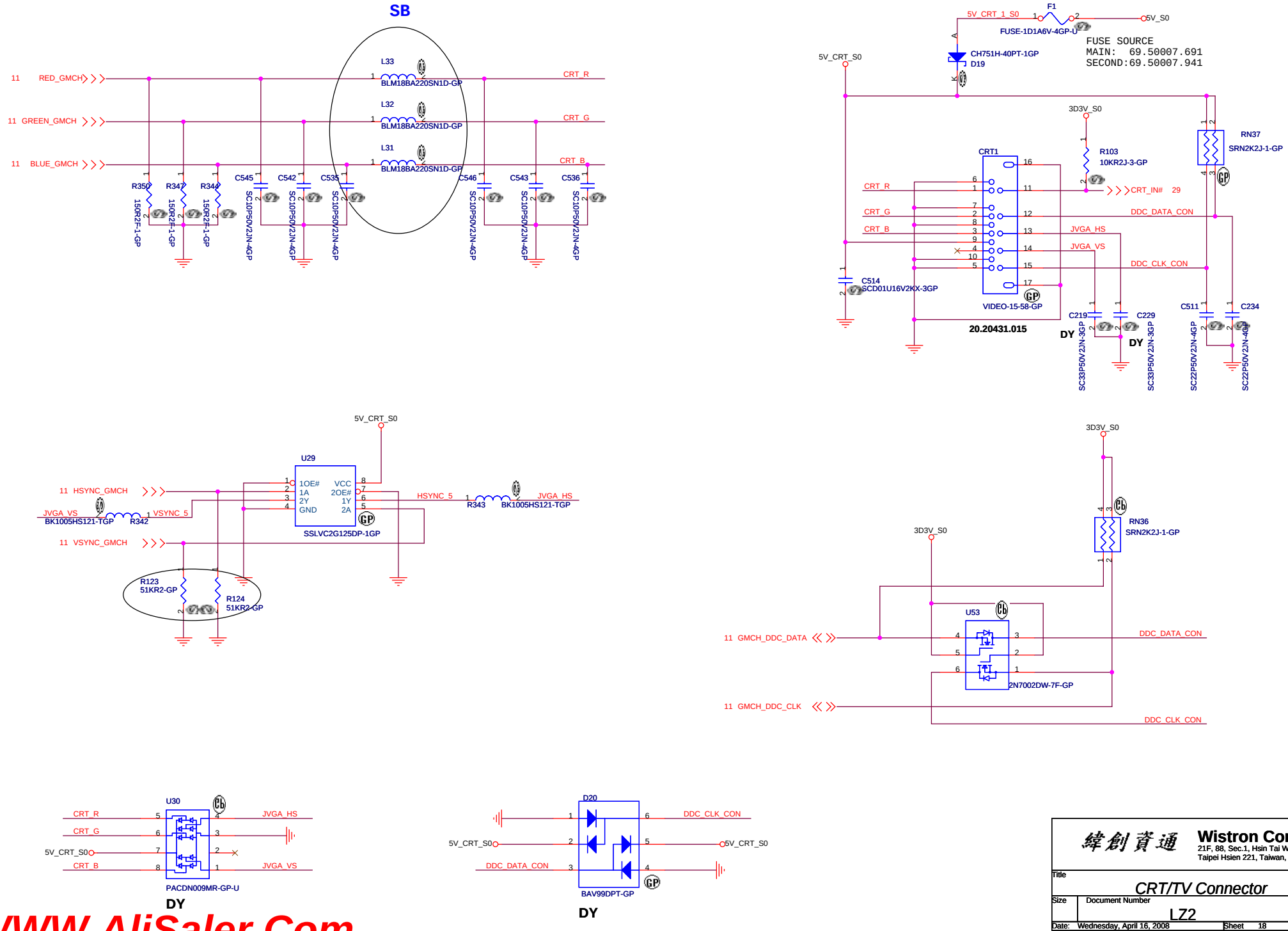
Title	LCD CONN & CAMERA & DIG-MIC		
Size	Document Number		Rev
	LZ2		SB
Date: Wednesday, April 16, 2008	Sheet 17	of	41


SB
11 RED_GMCH
11 GREEN_GMCH
11 BLUE_GMCH
L33
L32
L31
BLM18BA220SN1D-GP
CRT_R
CRT_G
CRT_B
R350
R347
R348
150R2F-1-GP
C545
C542
C535
C546
C543
C536
SC10P50V2JN-4GP
5V_CRT_S0
F1
5V_CRT_1_S0
5V_S0
FUSE-1D1A6V-4GP-U
FUSE SOURCE
MAIN: 69.50007.691
SECOND:69.50007.941
CH751H-40PT-1GP
D19
3D3V_S0
R103
10KR2J-3-GP
RN37
SRN2K2J-1-GP
CRT1
CRT_IN# 29
DDC_DATA_CON
JVGA_HS
JVGA_VS
DDC_CLK_CON
C514
SCD01U16V2KX-3GP
VIDEO-15-58-GP
20.20431.015
C219
C229
DY
SC33P50V2JN-3GP
C511
C234
SC22P50V2JN-4GP
U29
1OE#
1A
2Y
GND
VCC
2OE#
1Y
2A
SSLVC2G125DP-1GP
11 HSYNC_GMCH
11 VSYNC_GMCH
HSYNC_5
VSYNC_5
R343
R342
BK1005HS121-TGP
R123
51KR2-GP
R124
51KR2-GP
U53
2N7002DW-7F-GP
11 GMCH_DDC_DATA
11 GMCH_DDC_CLK
RN36
U30
CRT_R
CRT_G
CRT_B
JVGA_HS
JVGA_VS
PACDN009MR-GP-U
D20
BAV99DPT-GP
DY
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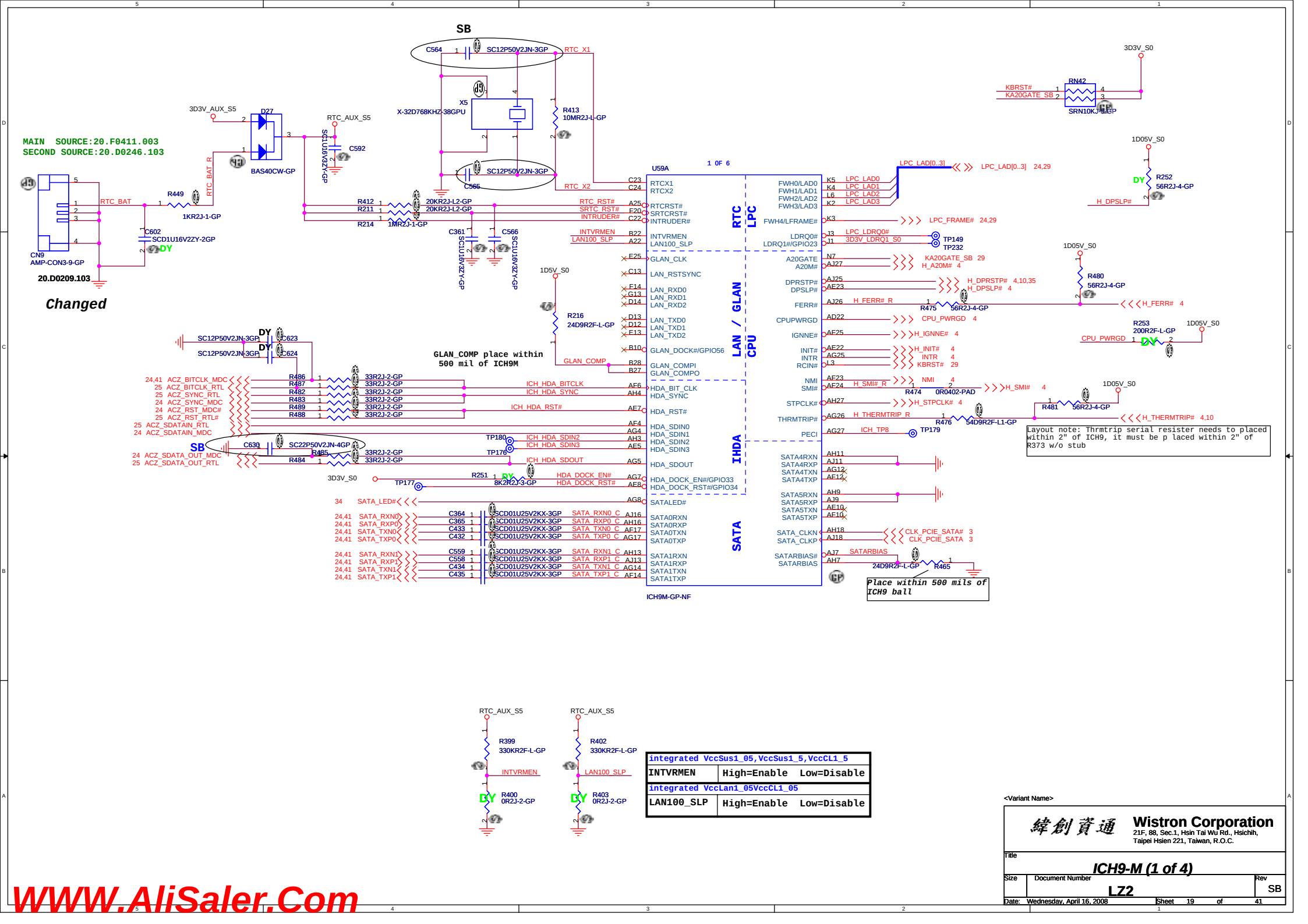
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT/TV Connector
Size
Document Number
LZ2
Rev
SB
Date: Wednesday, April 16, 2008
Sheet 18 of 41


SB
MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103
20.D0209.103
Changed
U59A
1 OF 6
ICH9M-GP-NF
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
Layout note: Thrmtrip serial resister needs to placed within 2" of ICH9, it must be p laced within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
LZ2
SB
Wednesday, April 16, 2008
19 of 41
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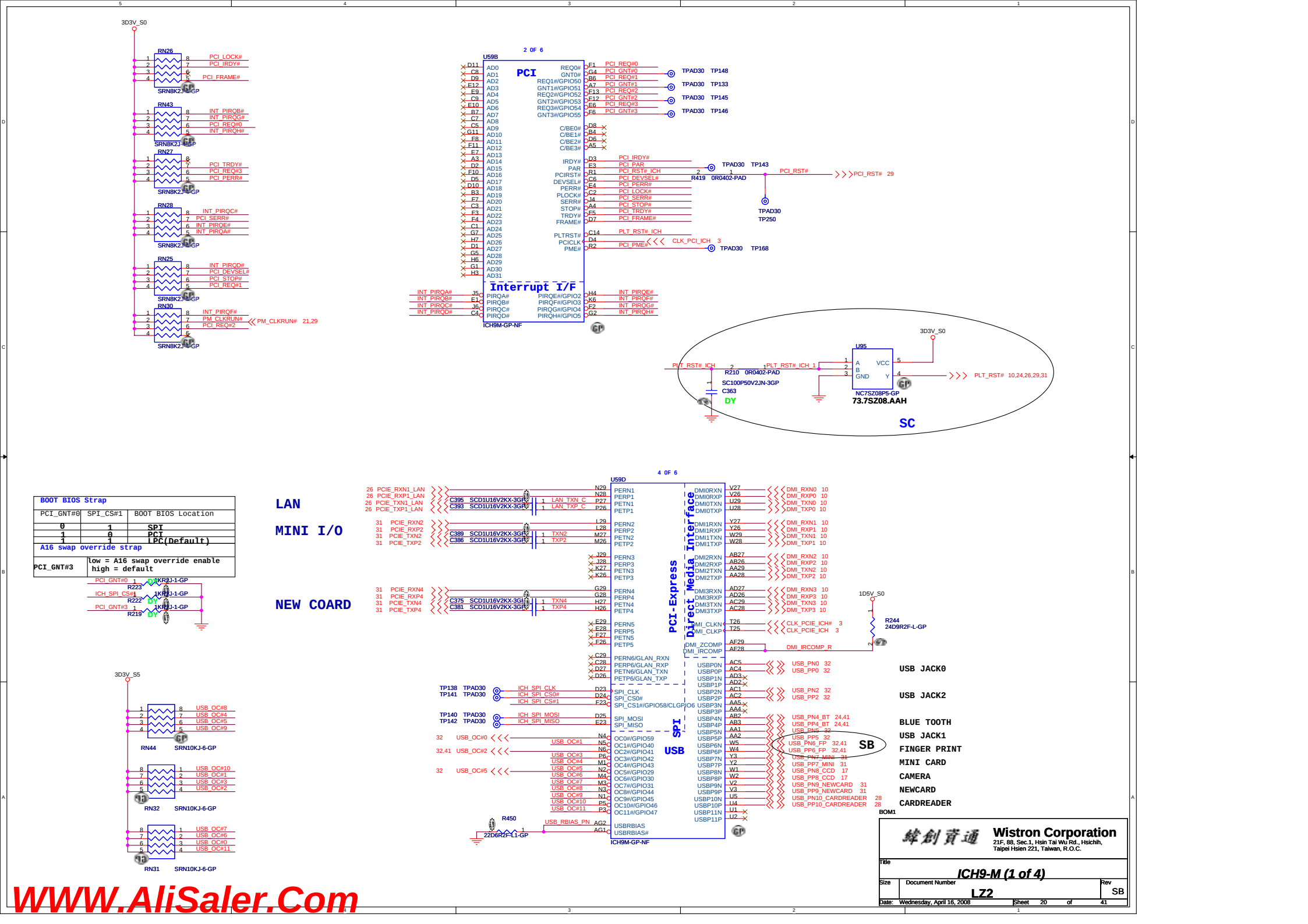

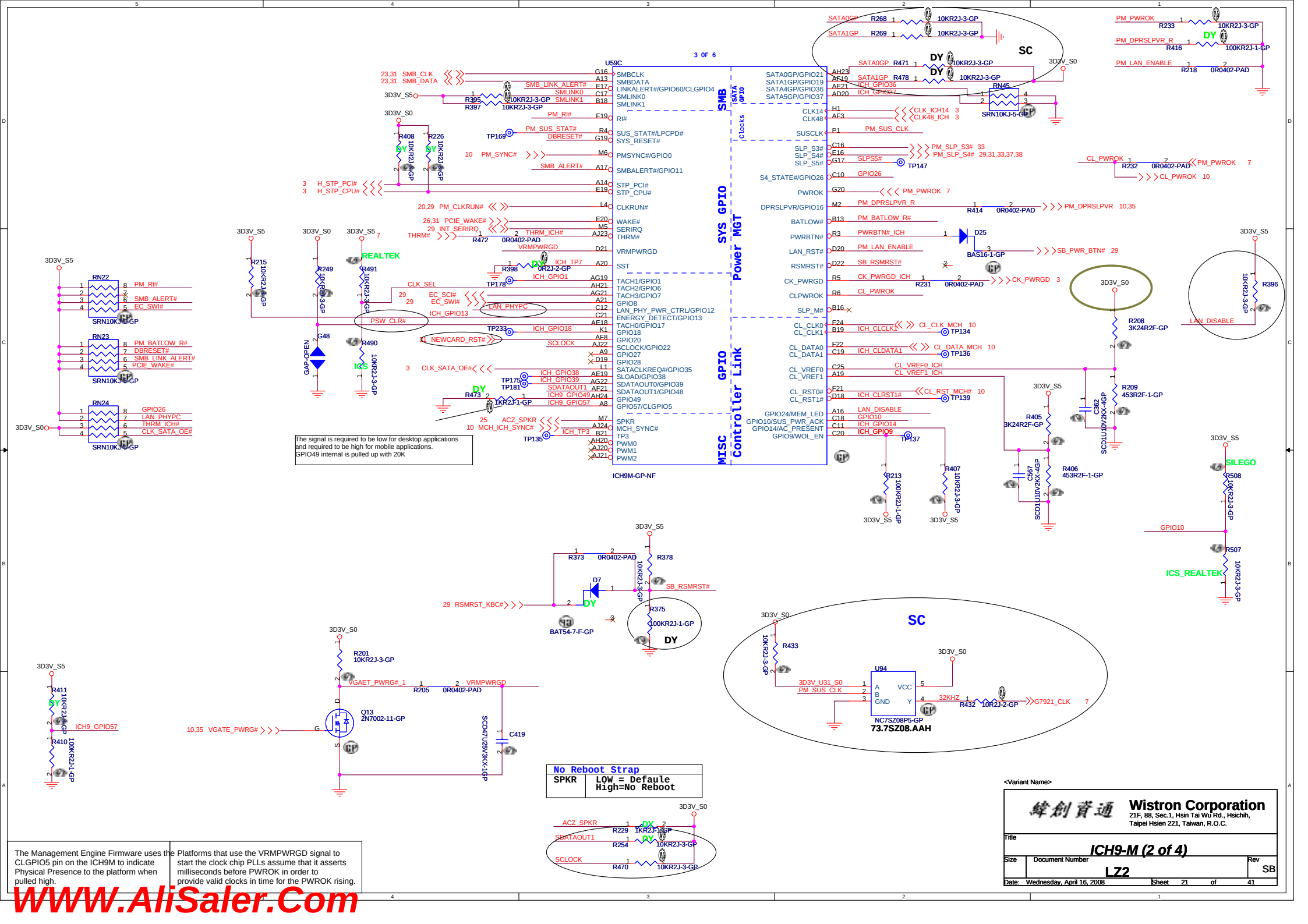
U59C
3 OF 6
ICH9M-GP-NF
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SC
REALTEK
ICS
SILEGO
DY
GAP-OPEN
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
The signal is required to be low for desktop applications and required to be high for mobile applications. GPIO49 internal is pulled up with 20K
The Management Engine Firmware uses the CLGPIO5 pin on the ICH9M to indicate Physical Presence to the platform when pulled high.
Platforms that use the VRMPWRGD signal to start the clock chip PLLs assume that it asserts milliseconds before PWROK in order to provide valid clocks in time for the PWROK rising.
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<Variant Name>
Title
ICH9-M (2 of 4)
Size
Document Number
LZ2
Rev
SB
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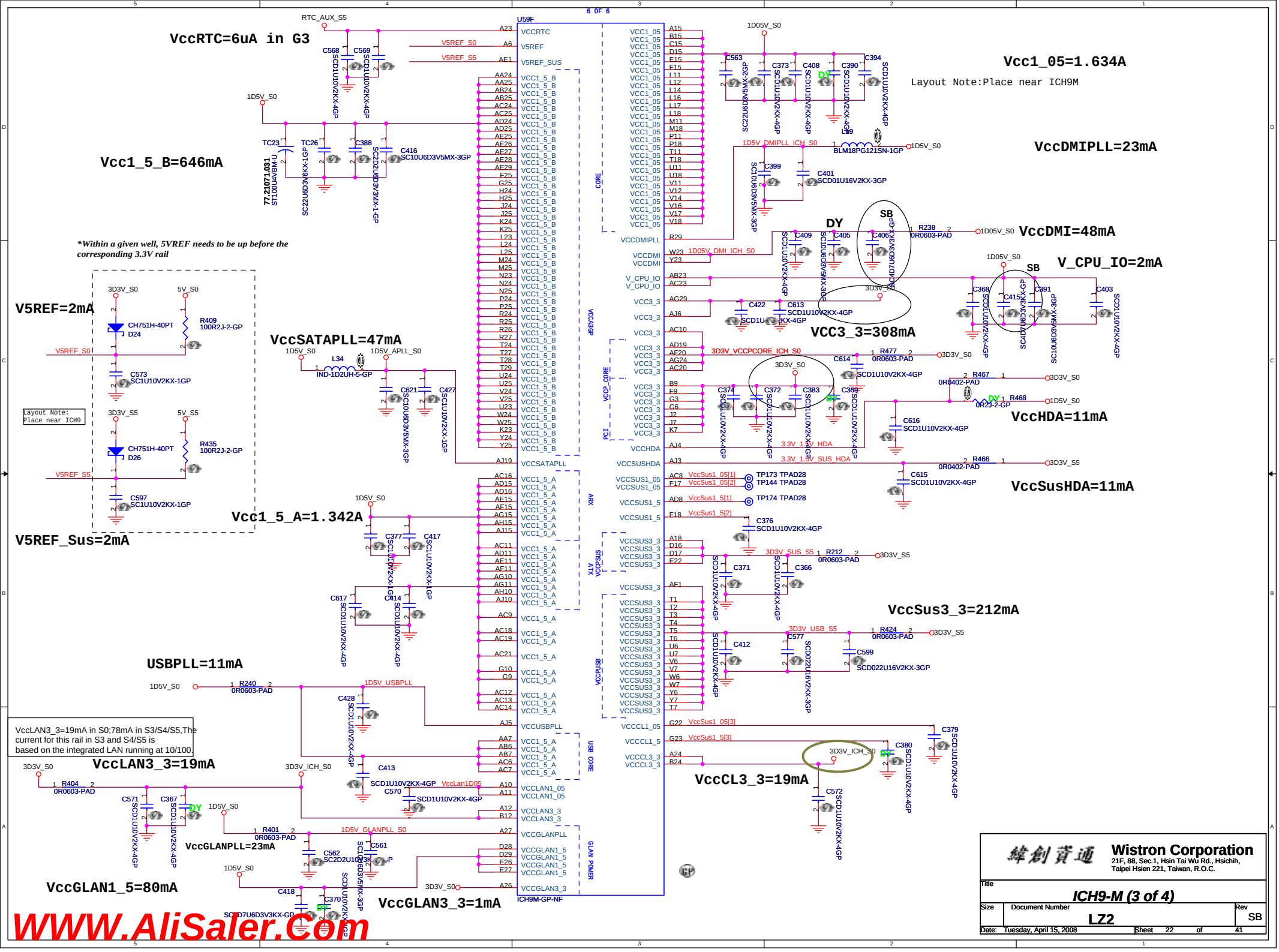
VccRTC=6uA in G3
Vcc1_5_B=646mA
Vcc1_05=1.634A
Layout Note:Place near ICH9M
VccDMIPLL=23mA
VccDMI=48mA
V_CPU_IO=2mA
VccHDA=11mA
VccSusHDA=11mA
VccSus3_3=212mA
VccCL3_3=19mA
VccGLANPLL=23mA
VccGLAN1_5=80mA
VccGLAN3_3=1mA
USBPLL=11mA
VccLAN3_3=19mA
VccLAN3_3=19mA in S0;78mA in S3/S4/S5,The current for this rail in S3 and S4/S5 is based on the integrated LAN running at 10/100.
V5REF=2mA
V5REF_Sus=2mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
VccSATAPLL=47mA
Vcc1_5_A=1.342A
VCC3_3=308mA
U59F
6 OF 6
ICH9M-GP-NF
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
LZ2
SB
Tuesday, April 15, 2008
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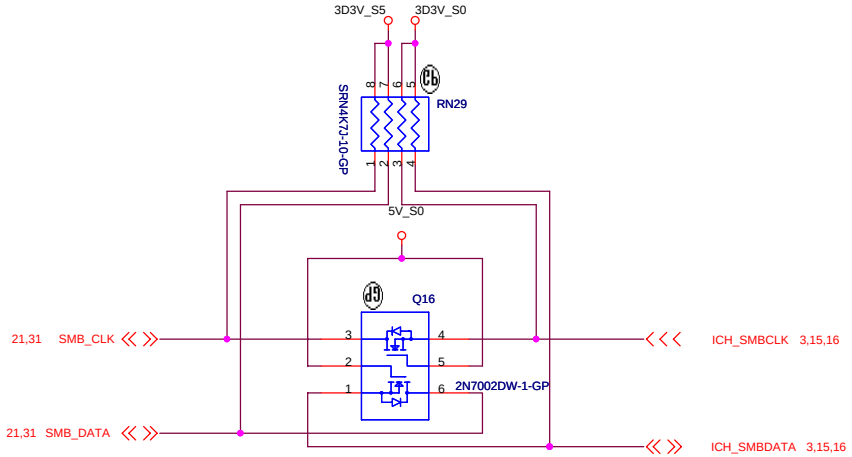
U59E

AA26	VSS	VSS	H5	VSS	A1
AA27	VSS	VSS	J23	VSS	A2
AA3	VSS	VSS	J26	VSS	A28
AA6	VSS	VSS	J27	VSS	A29
AB1	VSS	VSS	AC22	VSS	AH1
AA23	VSS	VSS	K28	VSS	AH29
AB28	VSS	VSS	K29	VSS	AJ1
AB29	VSS	VSS	L13	VSS	AJ2
AB4	VSS	VSS	L15	VSS	AJ28
AB5	VSS	VSS	L2	VSS	AJ29
AC17	VSS	VSS	L26	VSS	B1
AC26	VSS	VSS	L27	VSS	B29
AC27	VSS	VSS	L5		
AC3	VSS	VSS	L7		
AD1	VSS	VSS	M12		
AD10	VSS	VSS	M13		
AD12	VSS	VSS	M14		
AD13	VSS	VSS	M15		
AD14	VSS	VSS	M16		
AD17	VSS	VSS	M17		
AD18	VSS	VSS	M23		
AD21	VSS	VSS	M28		
AD28	VSS	VSS	M29		
AD29	VSS	VSS	N11		
AD4	VSS	VSS	N12		
AD5	VSS	VSS	N13		
AD6	VSS	VSS	N14		
AD7	VSS	VSS	N15		
AD9	VSS	VSS	N16		
AE12	VSS	VSS	N17		
AE13	VSS	VSS	N18		
AE14	VSS	VSS	N26		
AE16	VSS	VSS	N27		
AE17	VSS	VSS	P12		
AE2	VSS	VSS	P13		
AE20	VSS	VSS	P14		
AE24	VSS	VSS	P15		
AE3	VSS	VSS	P16		
AE4	VSS	VSS	P17		
AE6	VSS	VSS	P2		
AE9	VSS	VSS	P23		
AF13	VSS	VSS	P28		
AF16	VSS	VSS	P29		
AF18	VSS	VSS	P4		
AF22	VSS	VSS	P7		
AH26	VSS	VSS	R11		
AF26	VSS	VSS	R12		
AF27	VSS	VSS	R13		
AF5	VSS	VSS	R14		
AF7	VSS	VSS	R15		
AF9	VSS	VSS	R16		
AG13	VSS	VSS	R17		
AG16	VSS	VSS	R18		
AG18	VSS	VSS	R28		
AG20	VSS	VSS	T12		
AG23	VSS	VSS	T13		
AG3	VSS	VSS	T14		
AG6	VSS	VSS	T15		
AG9	VSS	VSS	T16		
AH12	VSS	VSS	T17		
AH14	VSS	VSS	T23		
AH17	VSS	VSS	B26		
AH19	VSS	VSS	U12		
AH2	VSS	VSS	U13		
AH22	VSS	VSS	U14		
AH25	VSS	VSS	U15		
AH28	VSS	VSS	U16		
AH5	VSS	VSS	U17		
AH8	VSS	VSS	AD23		
AJ12	VSS	VSS	U26		
AJ14	VSS	VSS	U27		
AJ17	VSS	VSS	U3		
AJ8	VSS	VSS	V1		
B11	VSS	VSS	V13		
B14	VSS	VSS	V15		
B17	VSS	VSS	V23		
B2	VSS	VSS	V28		
B20	VSS	VSS	V29		
B23	VSS	VSS	V4		
B5	VSS	VSS	V5		
B8	VSS	VSS	W26		
C26	VSS	VSS	W27		
C27	VSS	VSS	W3		
E11	VSS	VSS	Y1		
E14	VSS	VSS	Y28		
E18	VSS	VSS	Y29		
E2	VSS	VSS	Y4		
E21	VSS	VSS	Y5		
E24	VSS	VSS	AG28		
E5	VSS	VSS	AH6		
E8	VSS	VSS	AF2		
F16	VSS	VSS	B25		
F28	VSS				
F29	VSS				
G12	VSS				
G14	VSS				
G18	VSS				
G21	VSS				
G24	VSS				
G26	VSS				
G27	VSS				
G8	VSS				
H2	VSS				
H23	VSS				
H28	VSS				
H29	VSS				

ICH9M-GP-NF

ICH_VSS_TP_1	TP223	TPAD28
ICH_VSS_TP_2	TP220	TPAD28
ICH_VSS_TP_3	TP222	TPAD28
ICH_VSS_TP_4	TP225	TPAD28
ICH_VSS_TP_5	TP254	TPAD28
ICH_VSS_TP_6	TP253	TPAD28
ICH_VSS_TP_7	TP256	TPAD28
ICH_VSS_TP_8	TP257	TPAD28
ICH_VSS_TP_9	TP258	TPAD28
ICH_VSS_TP_10	TP255	TPAD28
ICH_VSS_TP_11	TP227	TPAD28
ICH_VSS_TP_12	TP228	TPAD28



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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Title: ICH9-M (4 of 4)

Size | Document Number: LZ2 | Rev: SB

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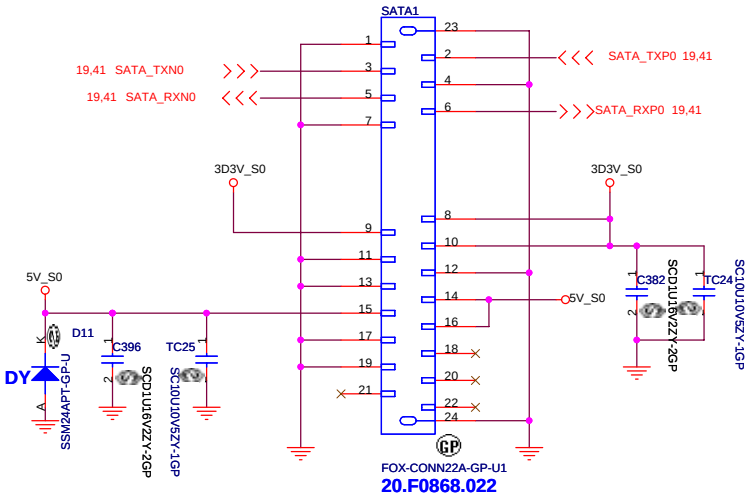
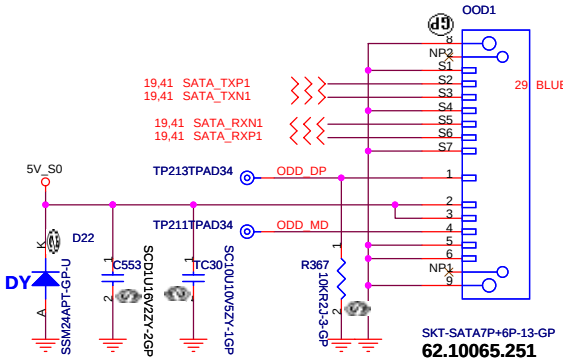
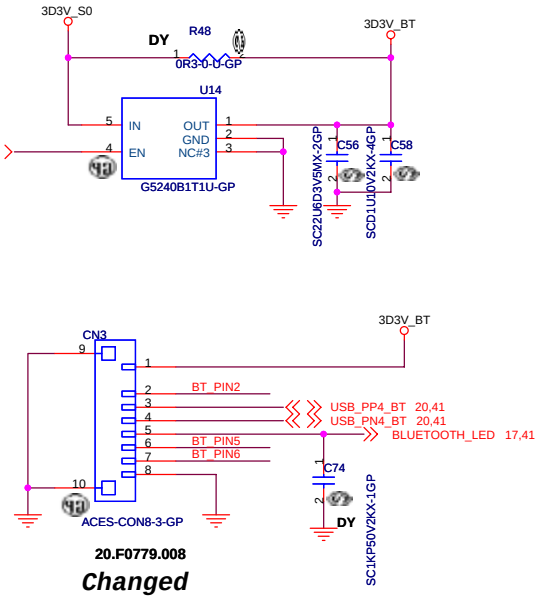
SATA HD Connector



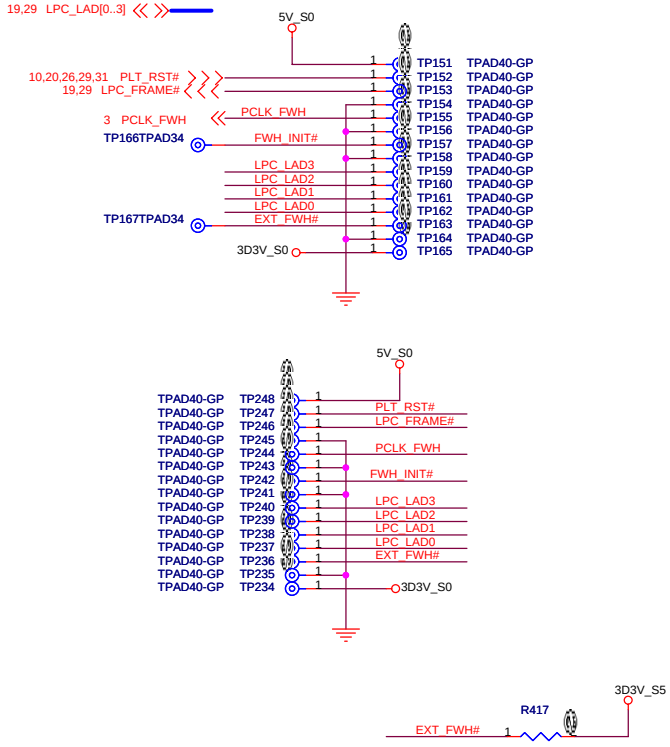
ODD Connector



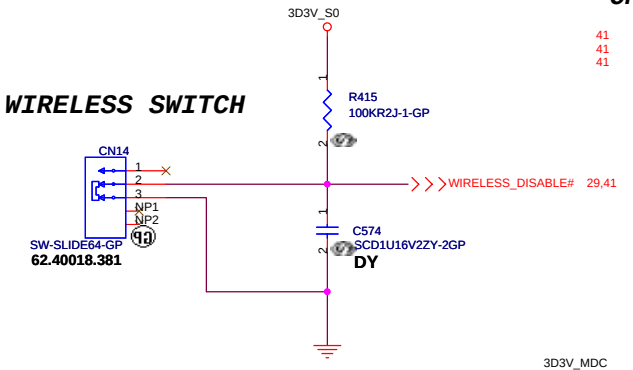
BT CONNECTOR



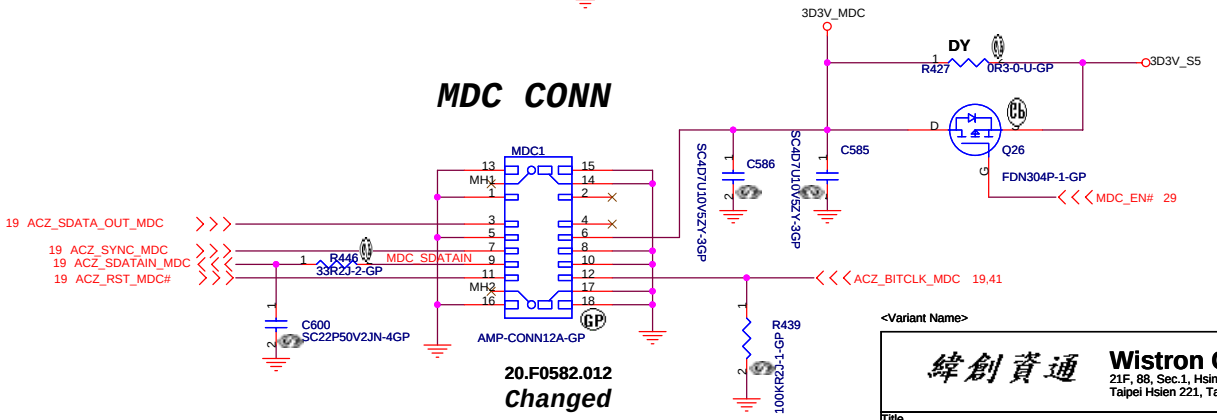
GOLDEN FINGER FOR DEBUG BOARD



WIRELESS SWITCH



MDC CONN



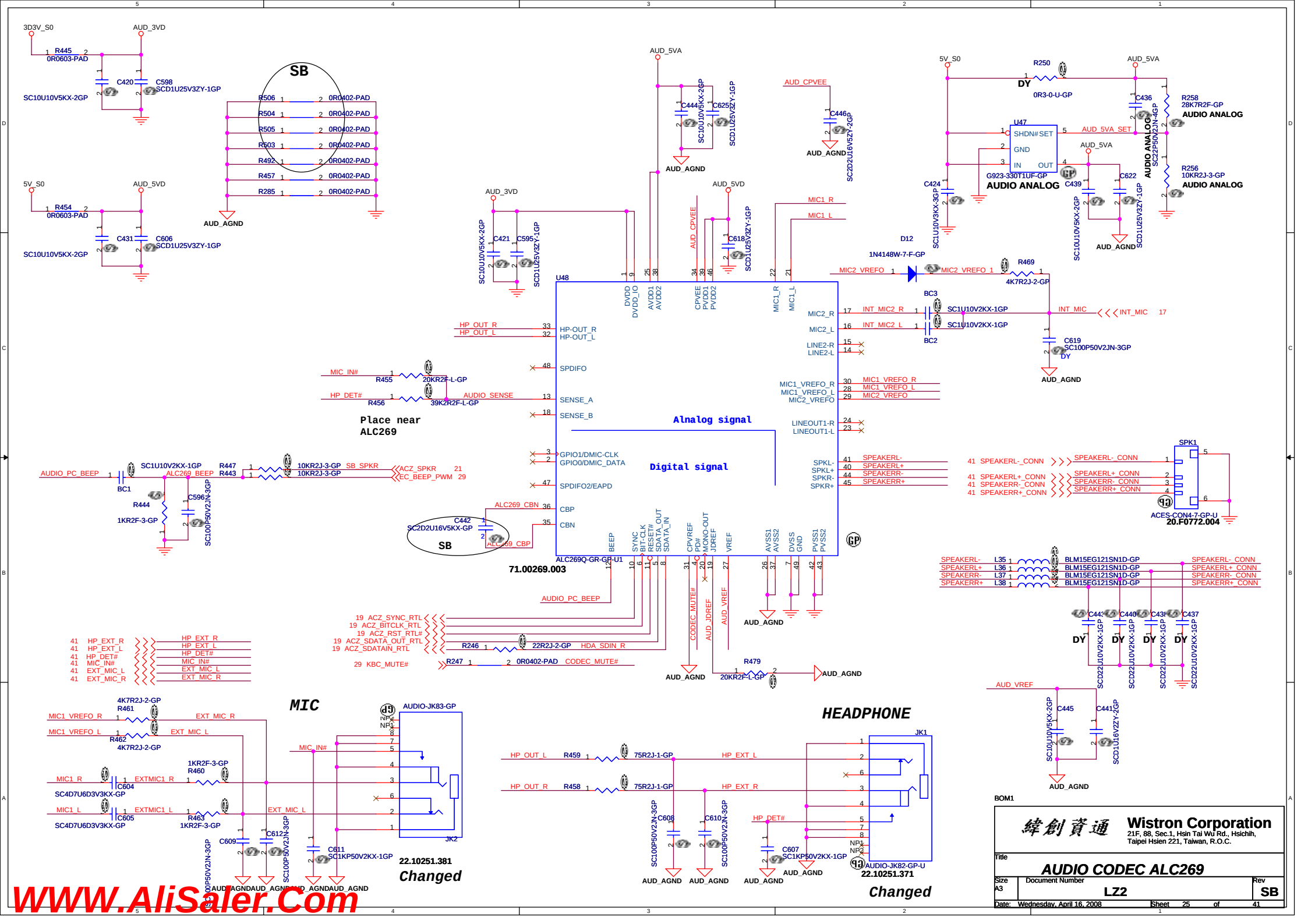
<Variant Name>

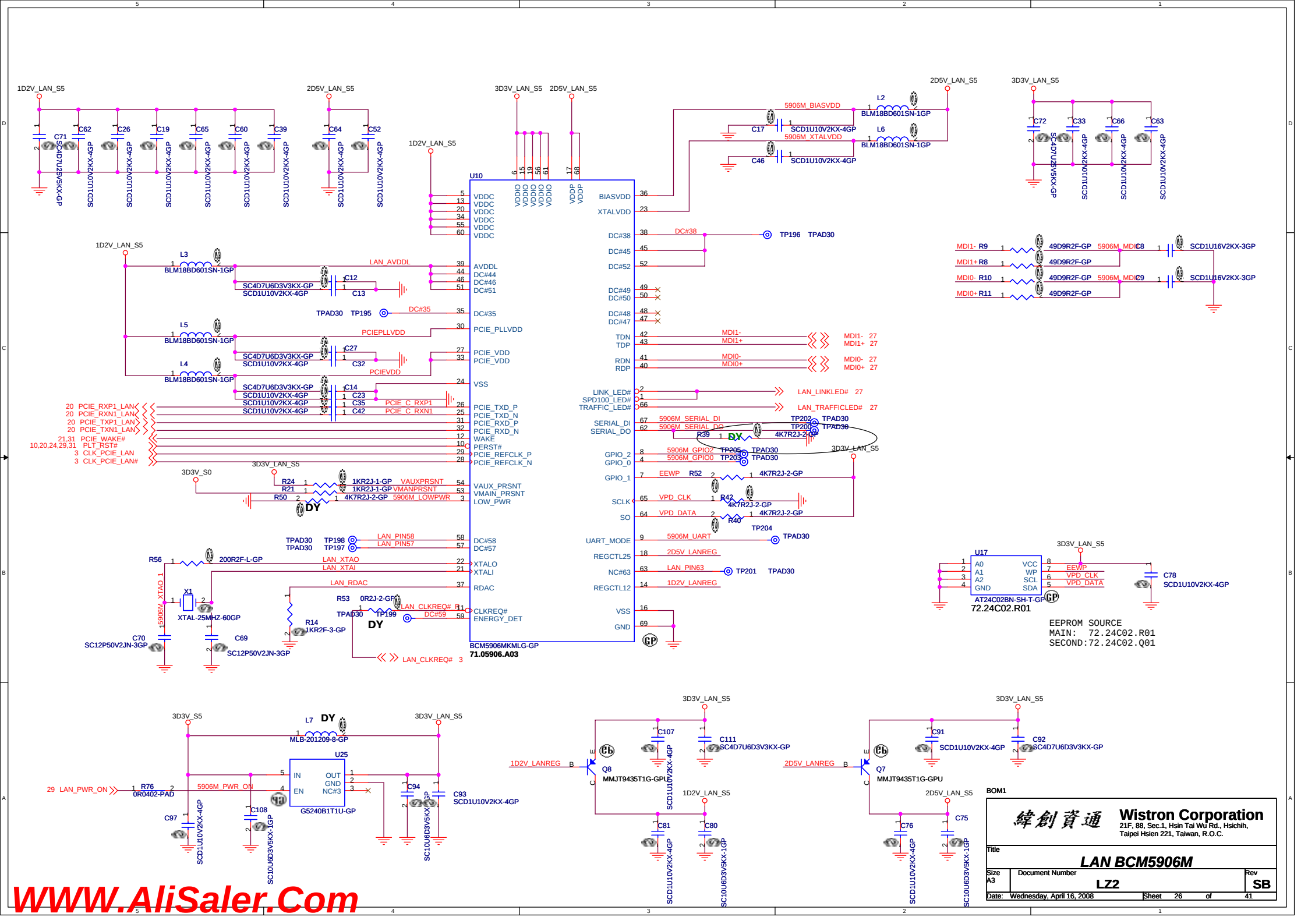
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/CDROM/DEBUG /MODEM/WIRELESS SW/BT**

Size	Document Number	Rev
	LZ2	SB

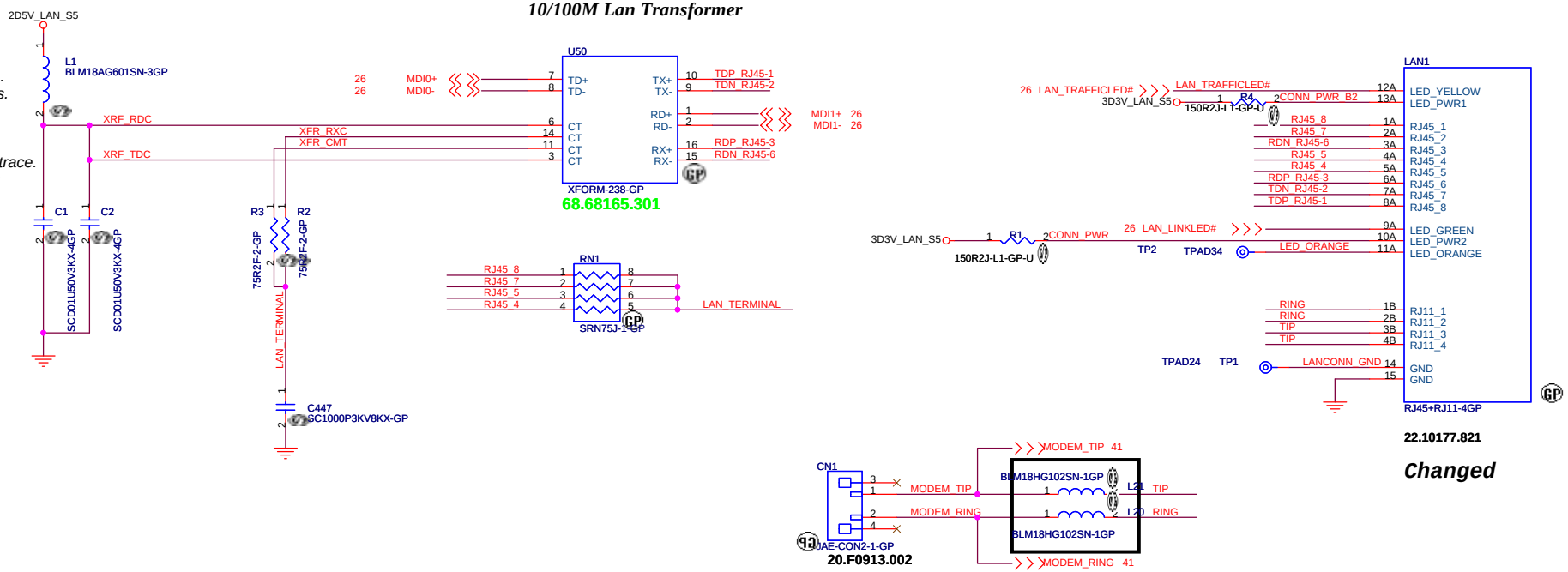
Date: Wednesday, April 16, 2008 Sheet 24 of 41





10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

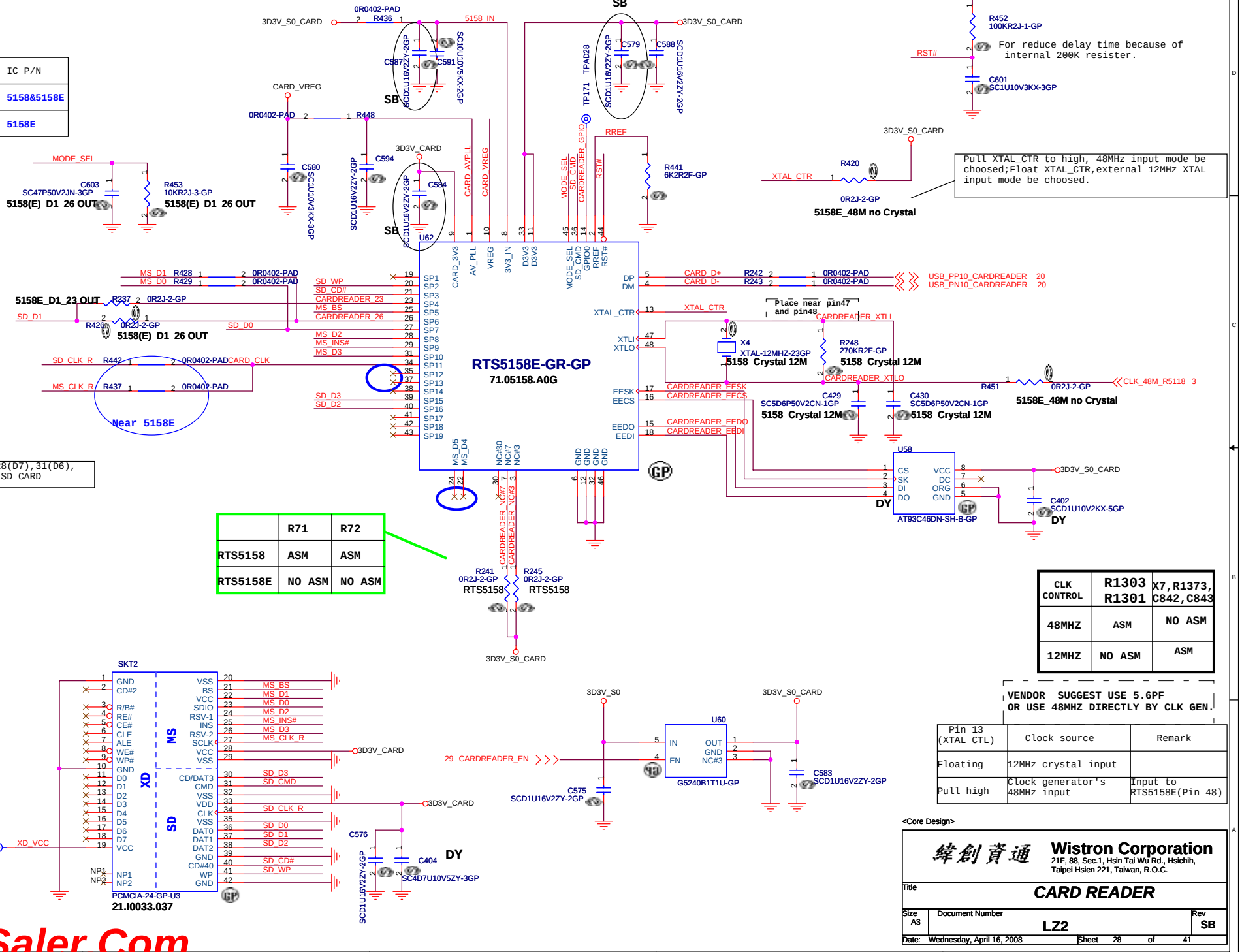


<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN connector/NEW CARD/SIM		
Size: A3	Document Number: LZ2	Rev: SB
Date: Wednesday, April 16, 2008	Sheet 27 of 41	

For 3in1 SD/MMC/MS CARD

R1302	C38	SD_D1 OUT FROM	IC P/N
10K	47 PF	PIN 26(MS_D1)	5158&5158E
NC	NC	PIN 23	5158E



	R71	R72
RTS5158	ASM	ASM
RTS5158E	NO ASM	NO ASM

CLK CONTROL	R1303 R1301	X7,R1373, C842,C843
48MHZ	ASM	NO ASM
12MHZ	NO ASM	ASM

Pin 13 (XTAL CTL)	Clock source	Remark
Floating	12MHz crystal input	
Pull high	Clock generator's 48MHz input	Input to RTS5158E(Pin 48)

<Core Design>

Wistron Corporation
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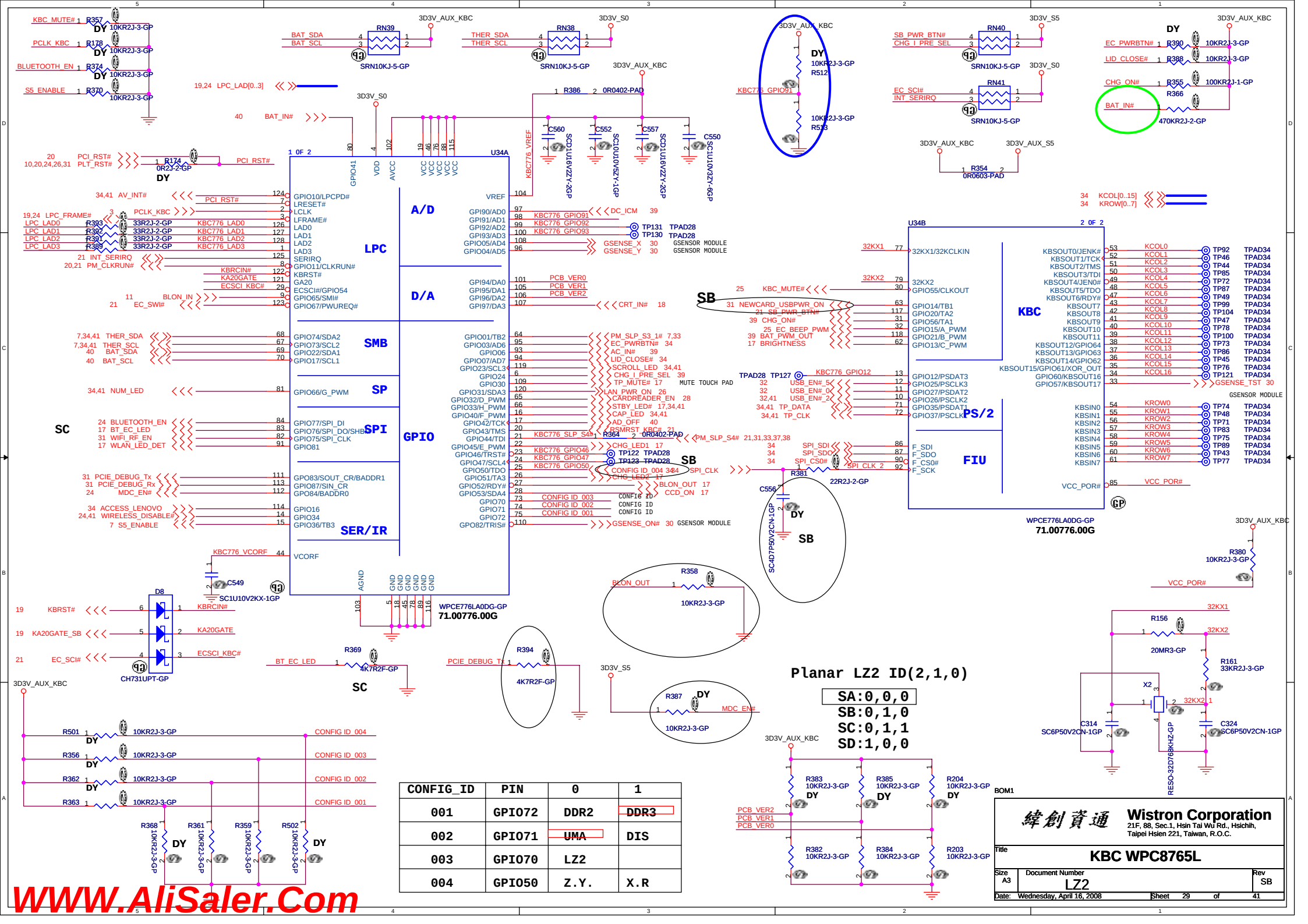
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER

Size: A3 | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 16, 2008 | Sheet 28 of 41


U34A
1 0F 2
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
SC
SB
U34B
2 0F 2
KBC
PS/2
FIU
WPCE776LA0DG-GP
71.00776.00G
WPCE776LA0DG-GP
71.00776.00G
CH731UPT-GP
Planar LZ2 ID(2,1,0)
SA:0,0,0
SB:0,1,0
SC:0,1,1
SD:1,0,0
CONFIG_ID | PIN | 0 | 1
001 | GPIO72 | DDR2 | DDR3
002 | GPIO71 | UMA | DIS
003 | GPIO70 | LZ2 |
004 | GPIO50 | Z.Y. | X.R
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8765L
Size A3
Document Number LZ2
Rev SB
Date: Wednesday, April 16, 2008
Sheet 29 of 41
BOM1
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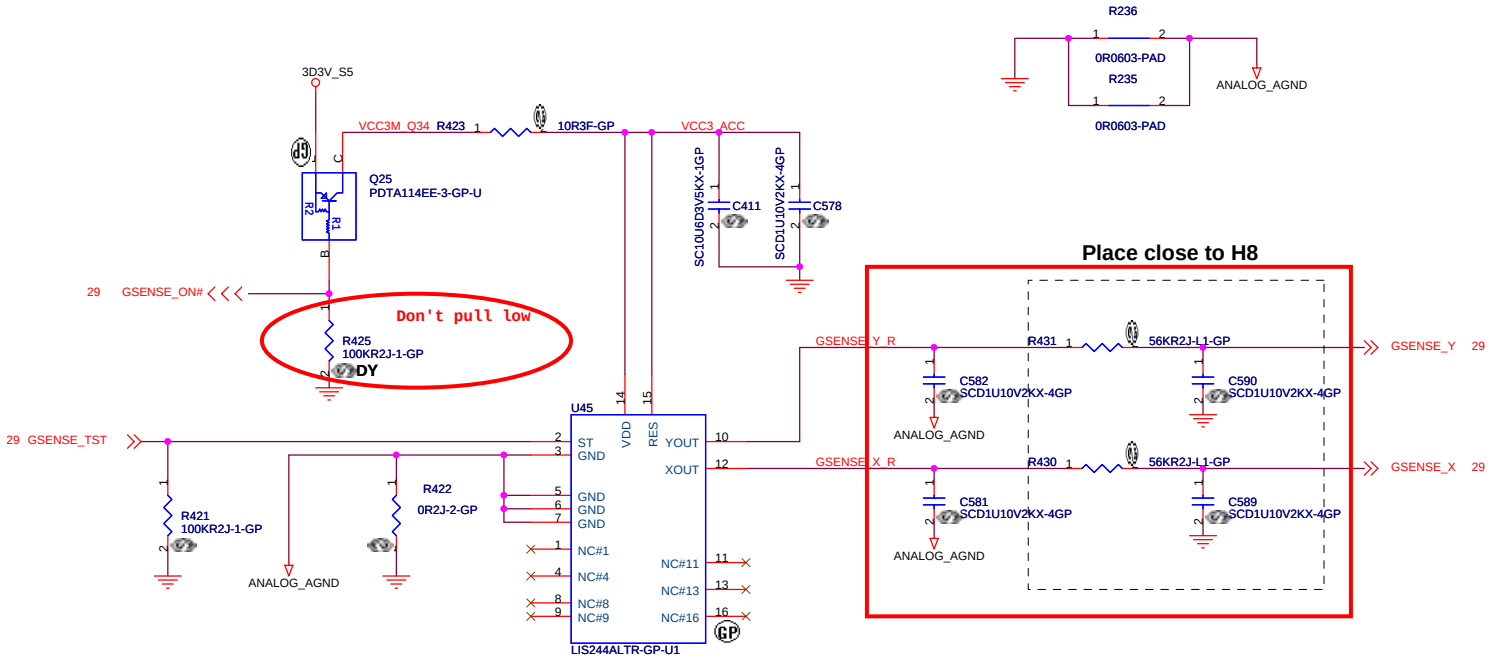

Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GSENSOR**

Size	Document Number	Rev
	LZ2	SB

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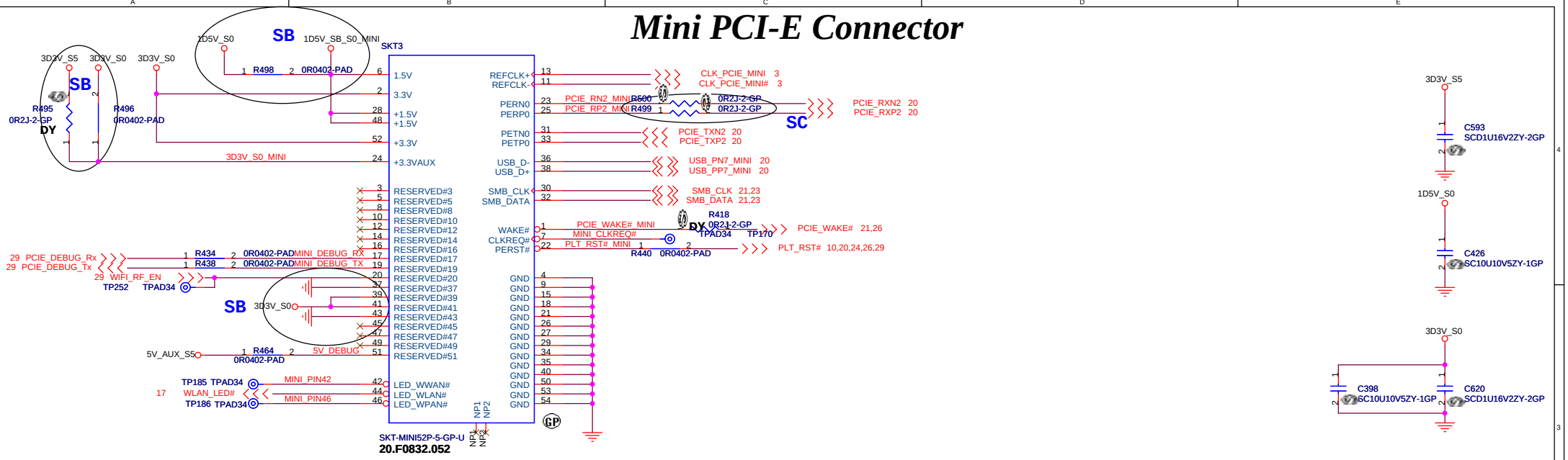
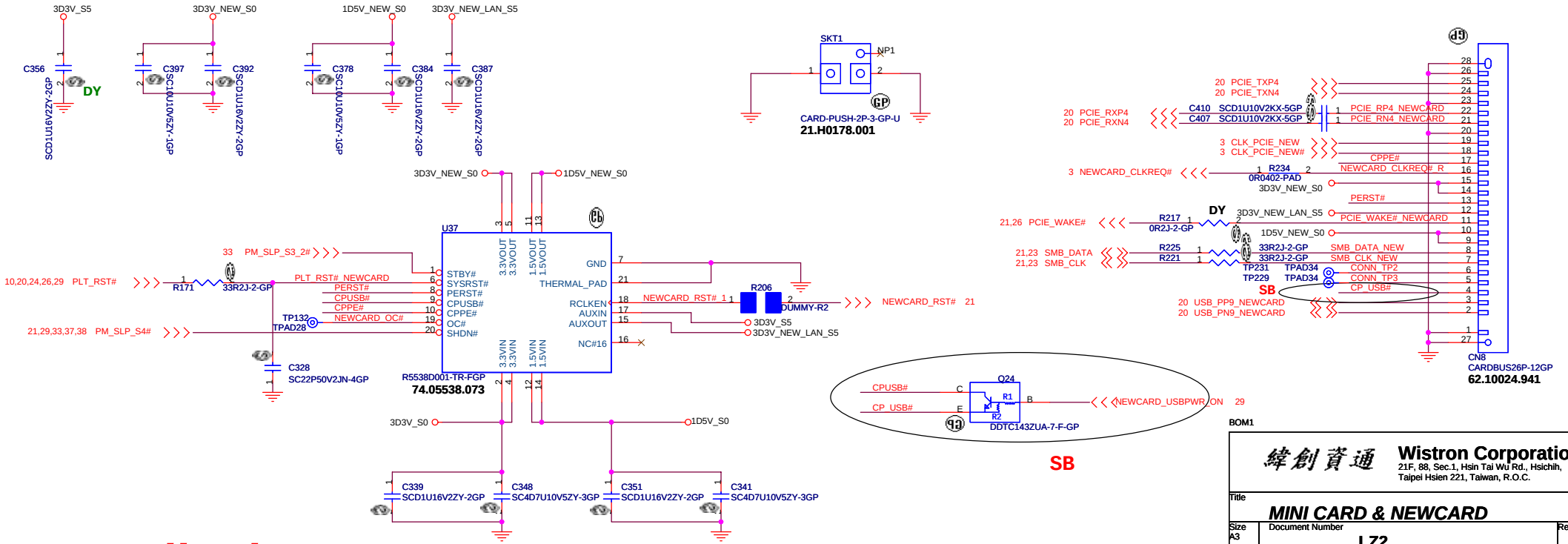
Mini PCI-E Connector



Place them Near to Chip

Place them Near to Connector

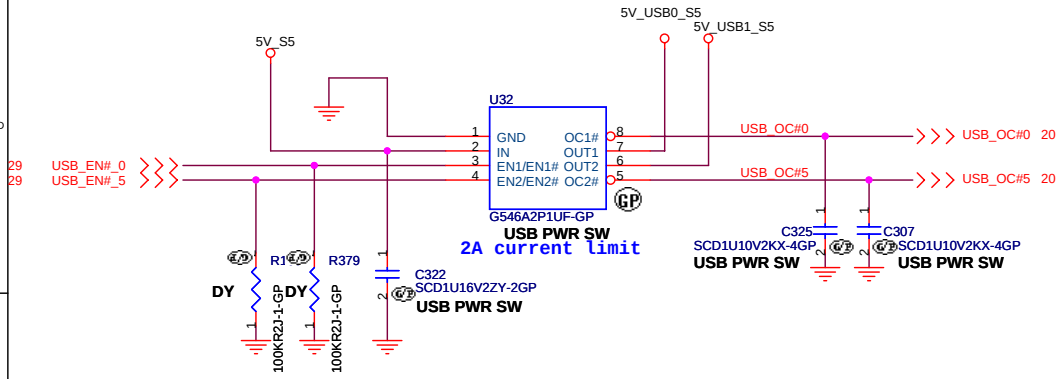
.N.E.W.C.A.R.D. C.O.N.N.

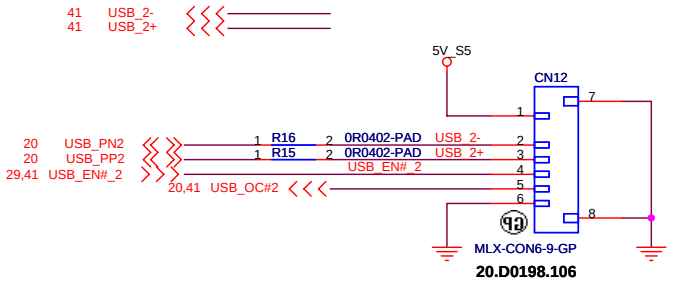


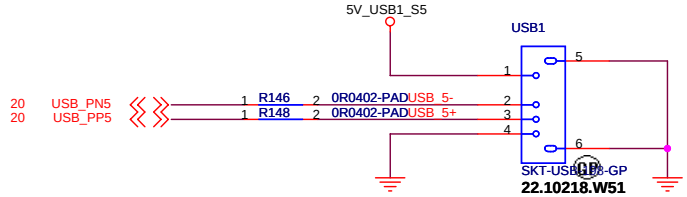
BOM1

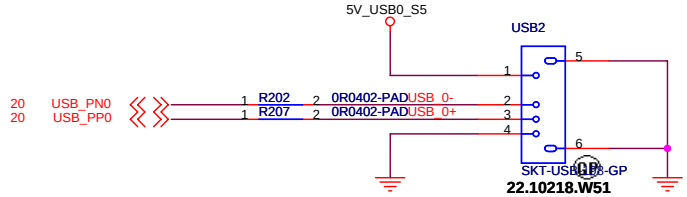
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD & NEWCARD	
Size A3	Document Number LZ2	Rev SB
Date: Wednesday, April 16, 2008	Sheet 31 of 41	

USB * 3 PORT

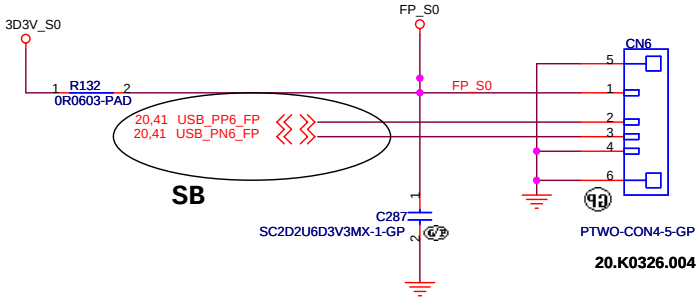


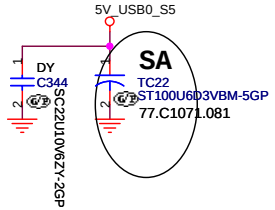


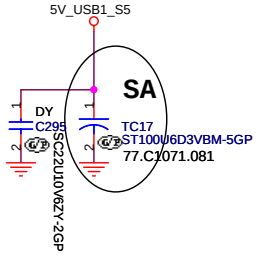


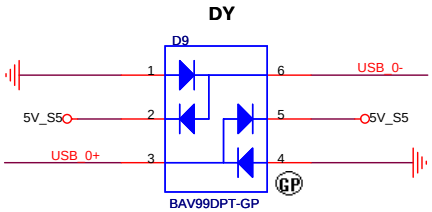


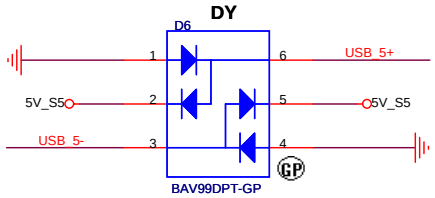
Finger Print











BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB CONN/FINGER PRINT**

Size	Document Number	Rev
B	LZ2	SB

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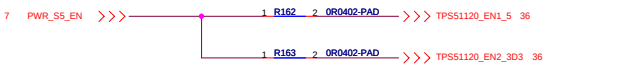
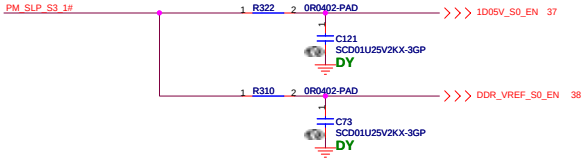
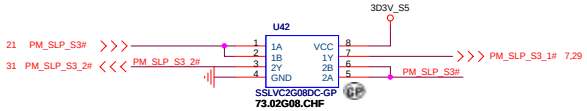
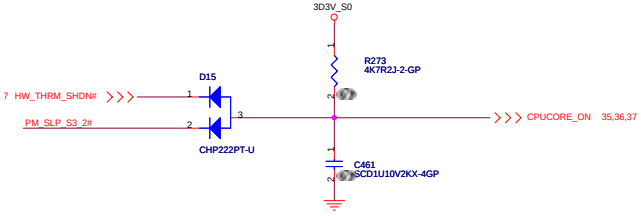
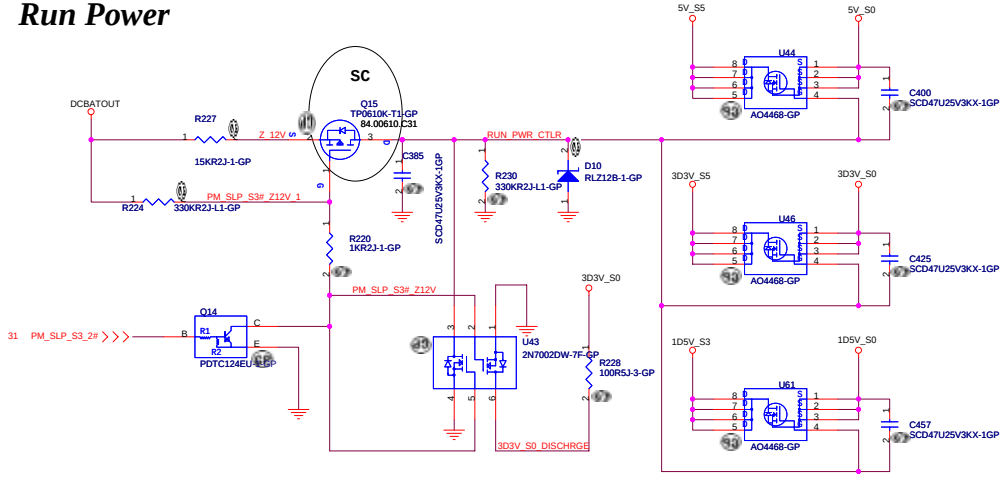


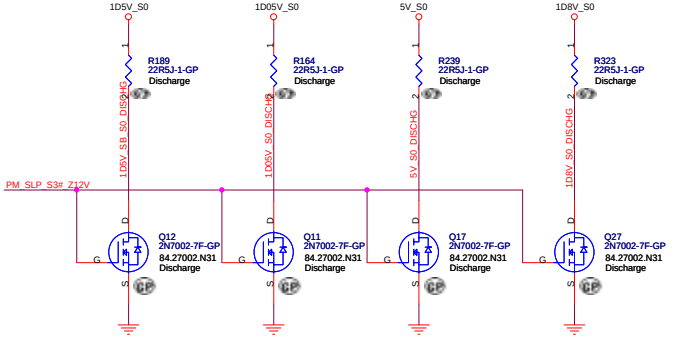


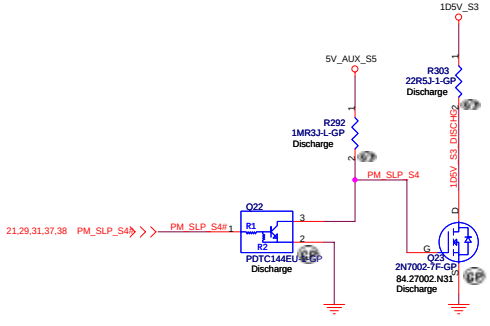




Run Power







BOM1

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PWRPLANE&RESET LOGIC***

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	LZ2	SB

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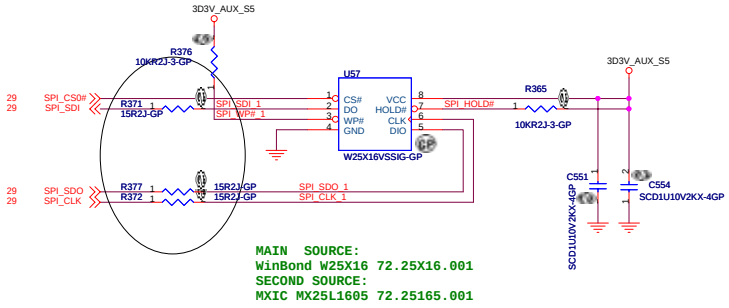
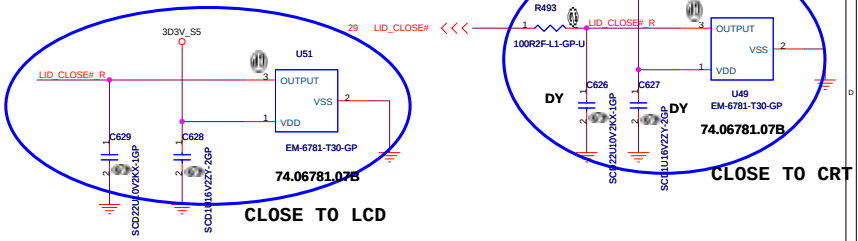
SPI Flash

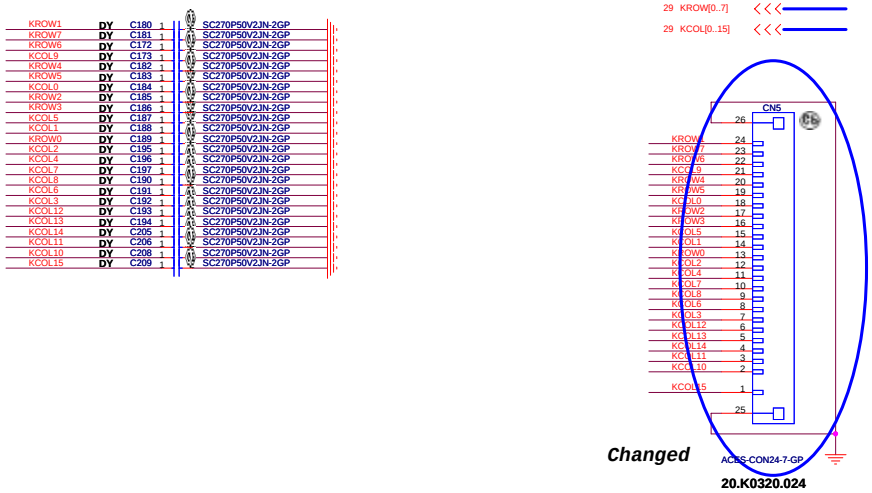


MAIN SOURCE:
WinBond W25X16 72.25X16.001
SECOND SOURCE:
MXIC MX25L1605 72.25165.001

Lid Switch



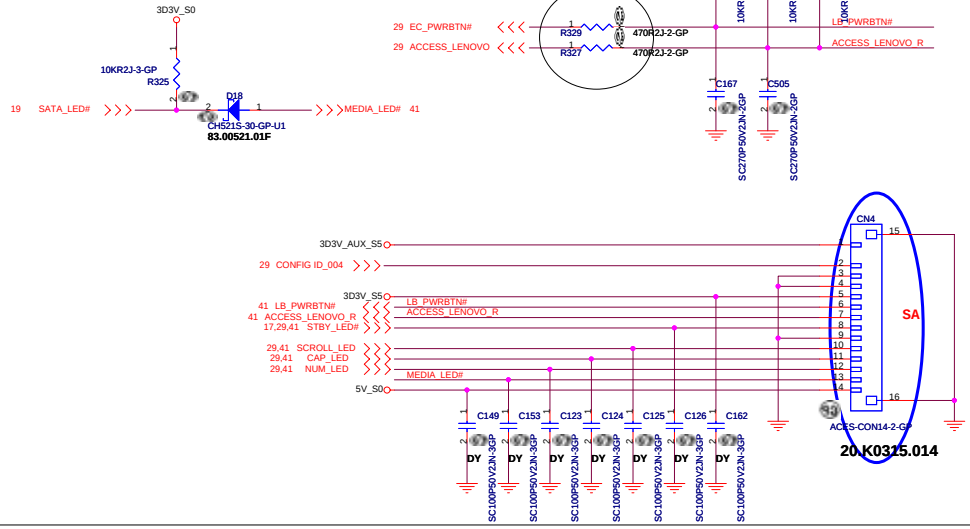
Keyboard Connector



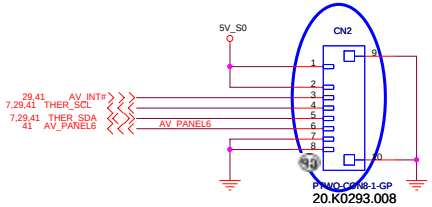
Changed

20.K0320.024

Launch Board

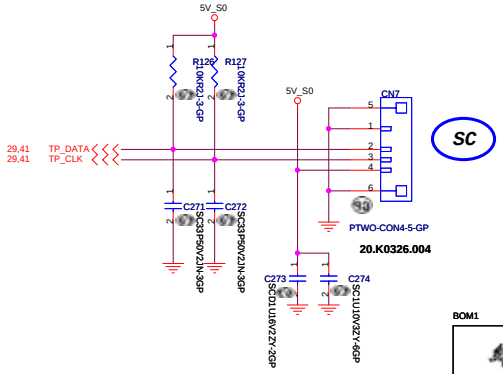


AV Panel



20.K0293.008

TouchPad Connector



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TP/SPI/AV/Charger

Size	Document Number	Rev
	LZ2	SB

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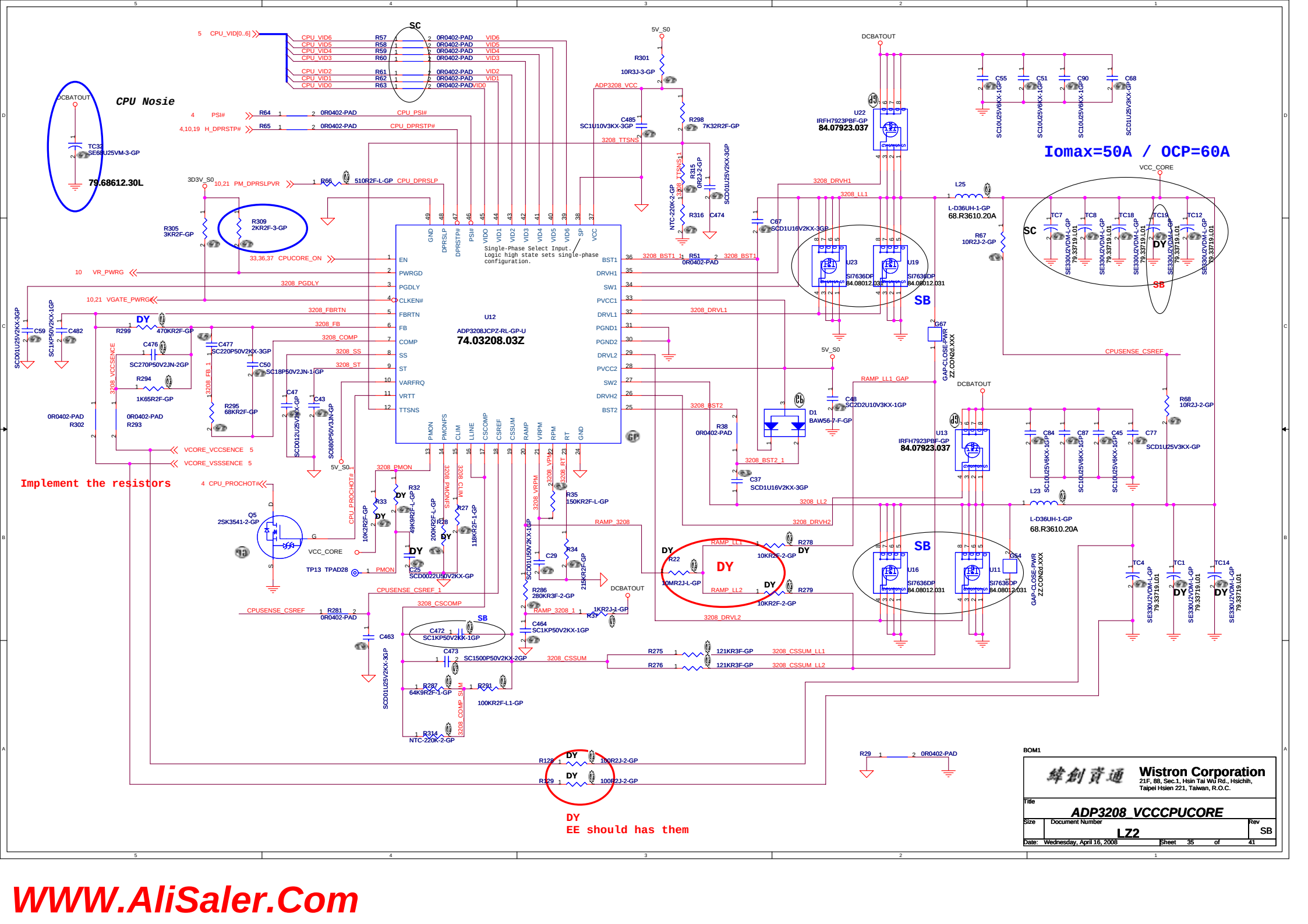

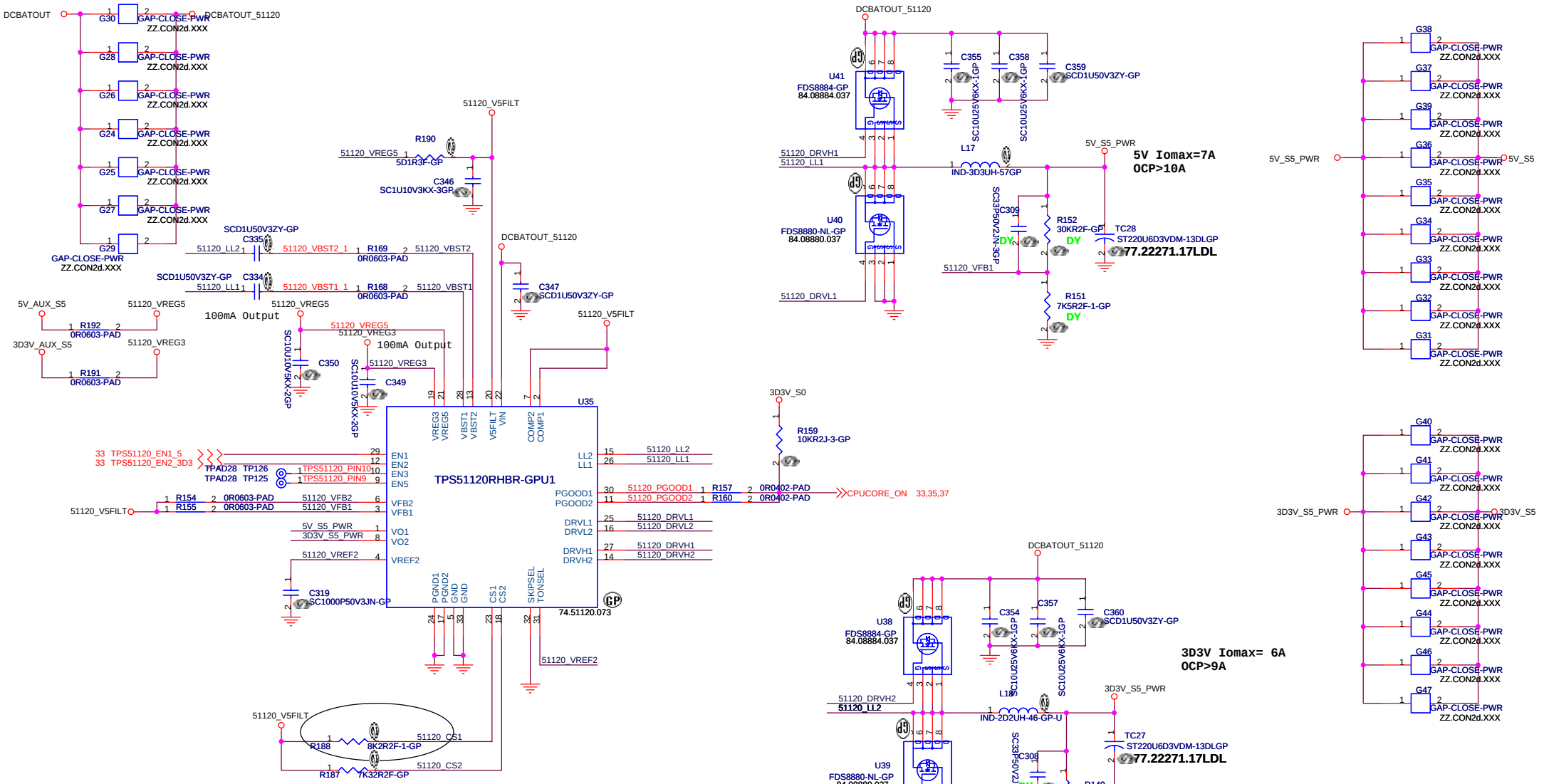

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
	N/A	N/A	CURRENT MODE	D-Cap MODE
	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
	N/A	not use	ADJ.	5V Fixed Output
	N/A	not use	ADJ.	3.3V Fixed Output
	Switcher OFF	not use	Swithchr ON	Switcher ON
	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V / 3D3V

Size	Document Number	Rev
A3	LZ2	SB

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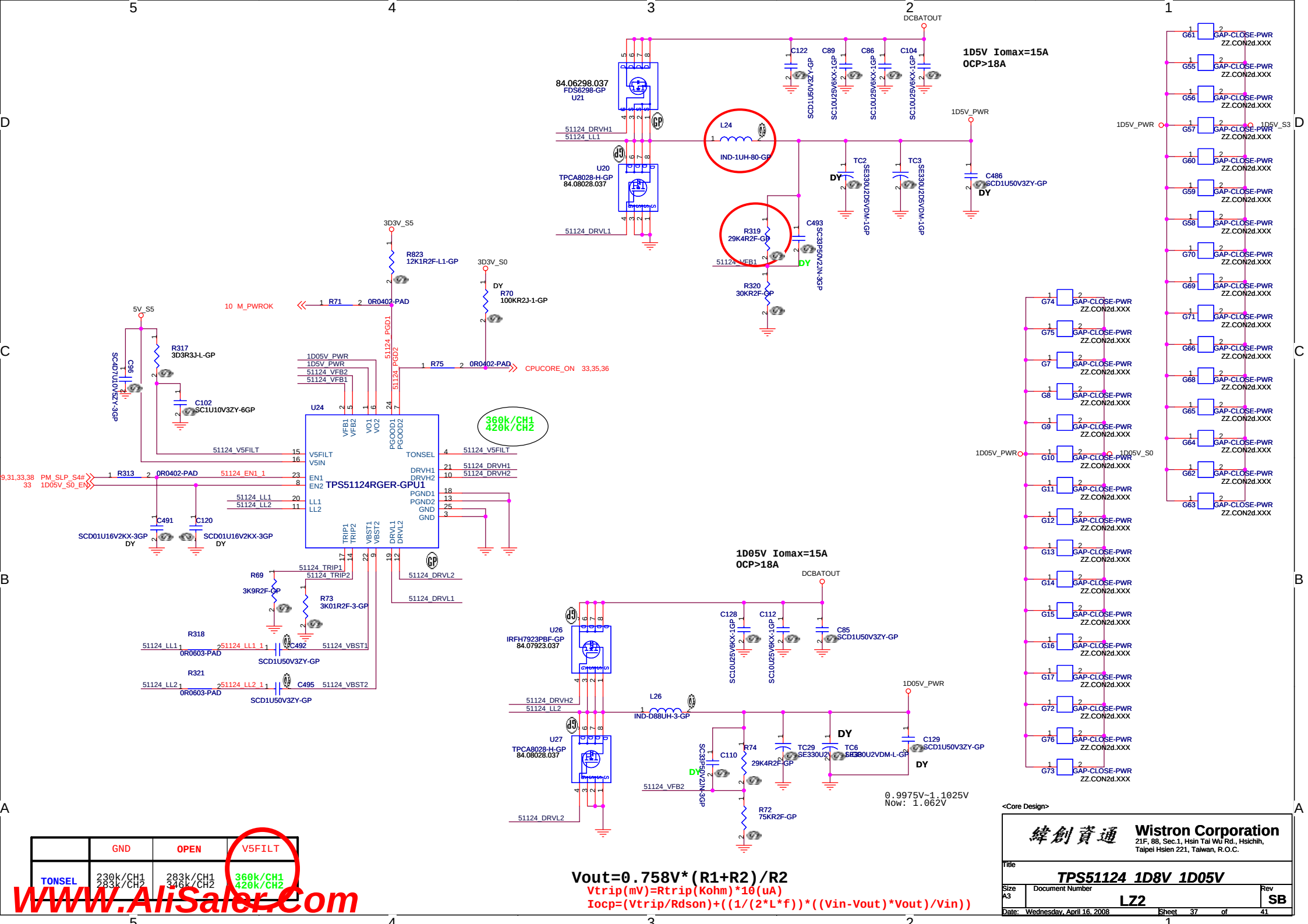

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360k/CH1 420k/CH2

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D05V

Size: A3 | Document Number: LZ2 | Rev: SB

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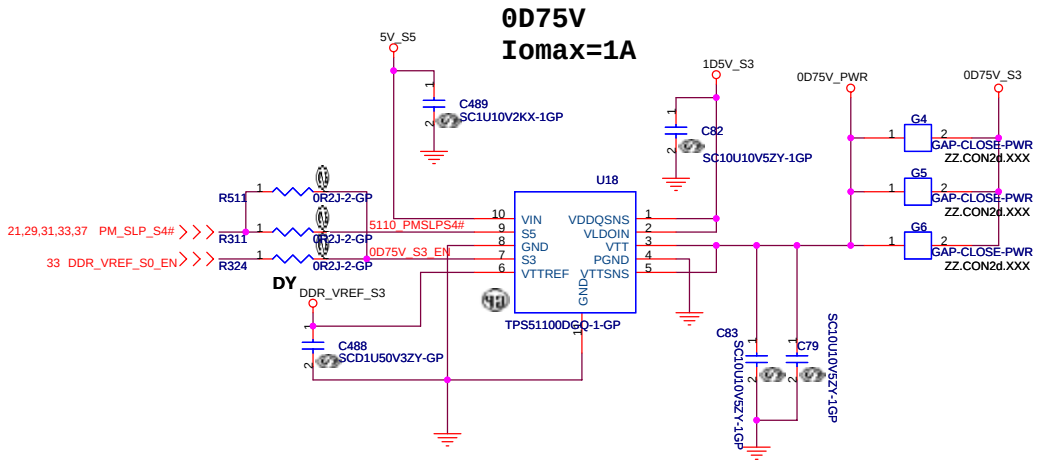

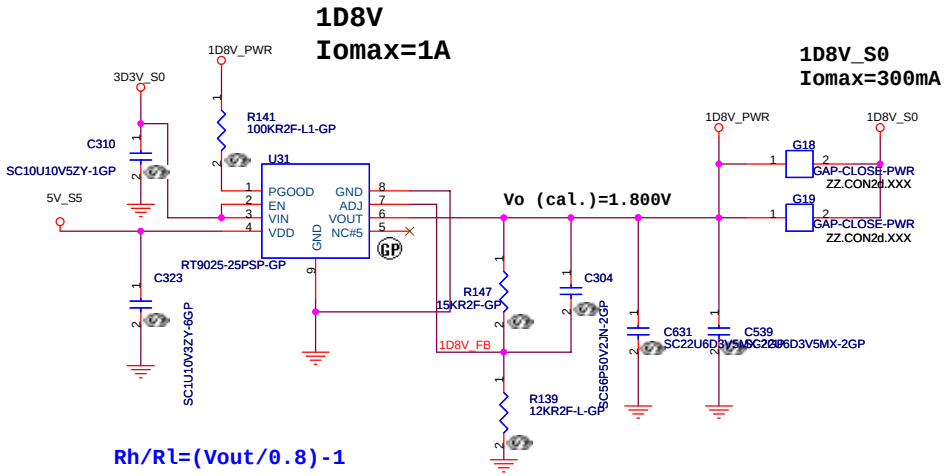

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 0D9V / 1D5V_S0

Size	Document Number	Rev
A3	LZ2	SB

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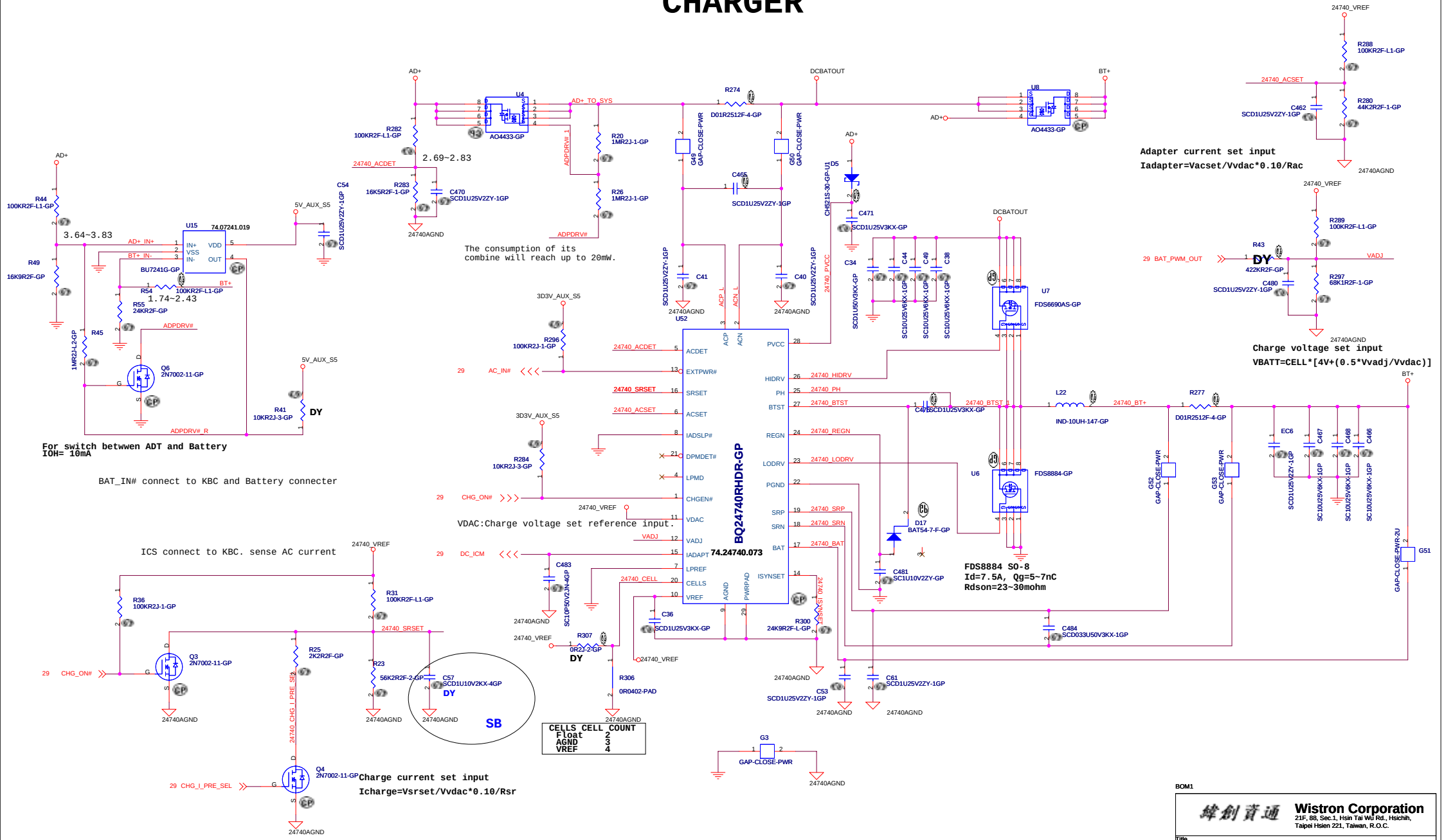
CHARGER



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger BQ24740

Size	Document Number	Rev
	LZ2	SB

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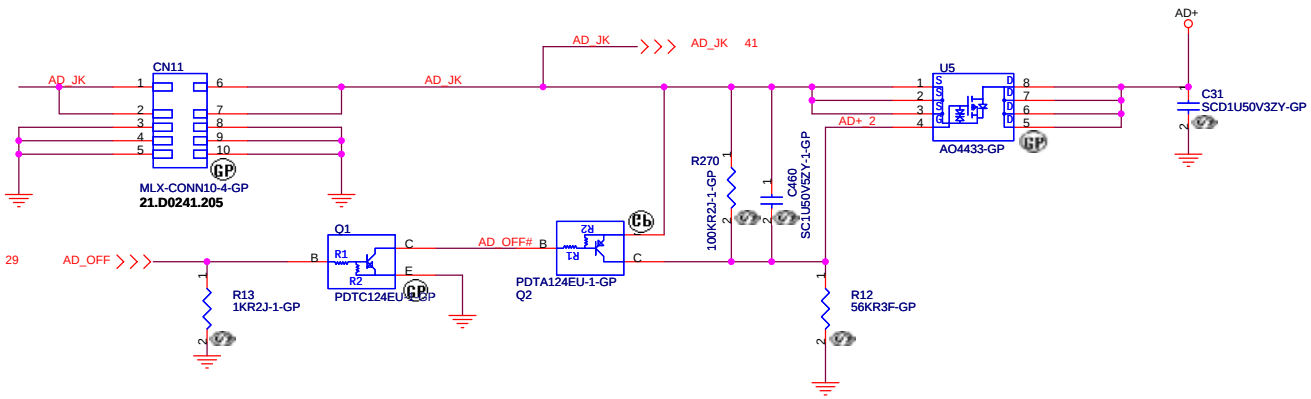
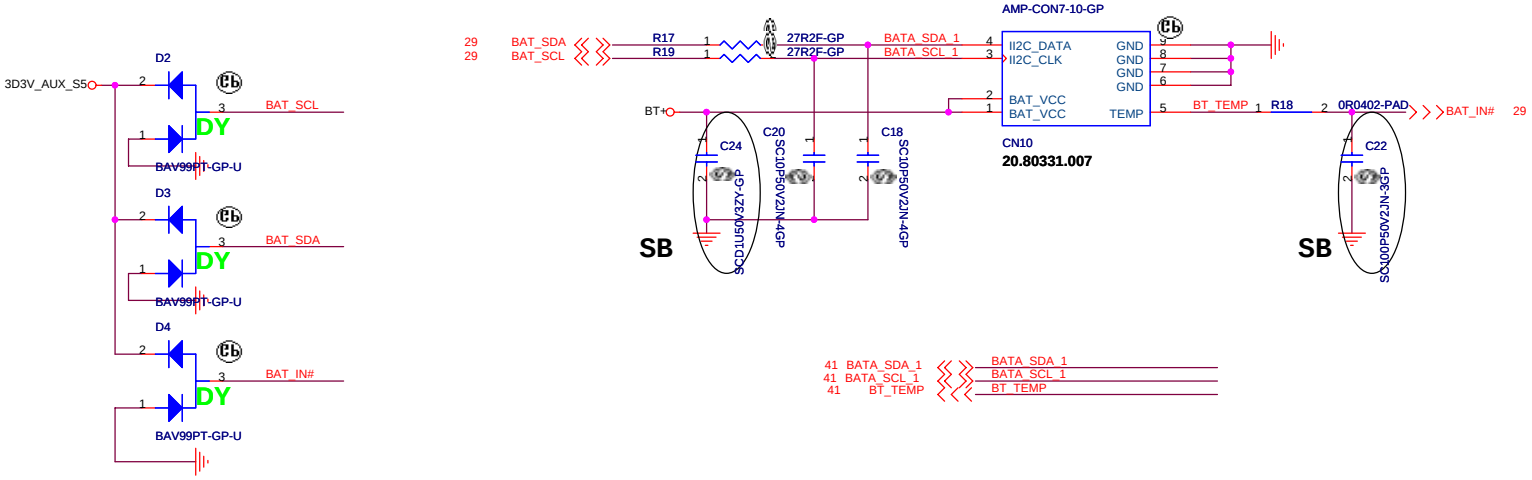
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PTH FOR SCREW HOLES

Size: A3 | Document Number: LZ2 | Rev: SB

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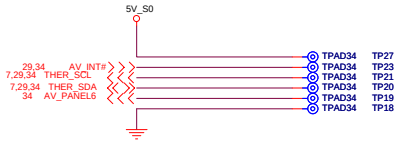
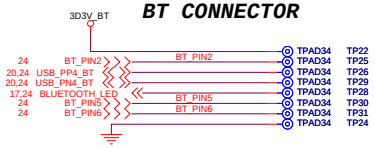
AV Panel

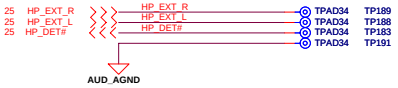


BT CONNECTOR



SATA CONN

HEADPHONE CONN



TouchPad Connector

WIRELESS SWITCH

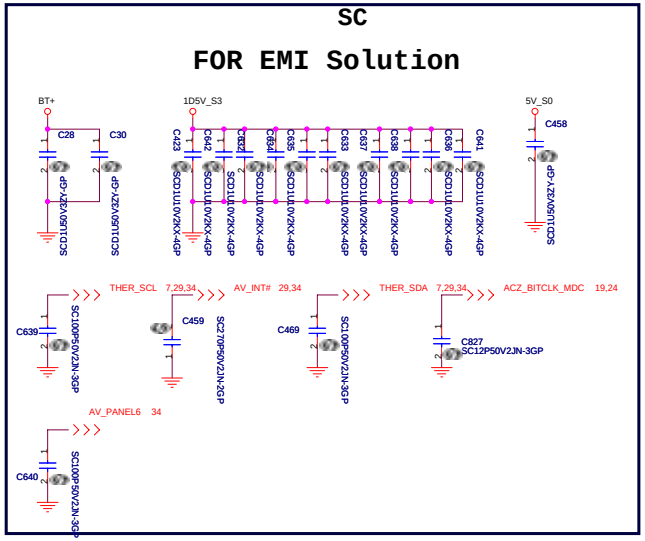
FAN CONN

ODD CONN

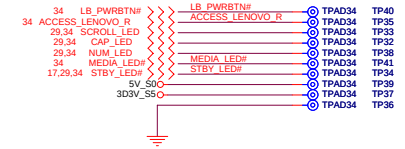
MIC CONN

SC

FOR EMI Solution

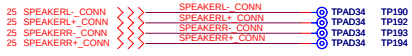


Launch Board

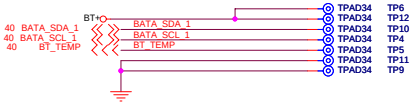


ADT BOARD CONN

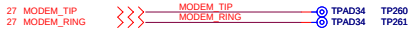
SPEAKER CONN



BATTERY CONN

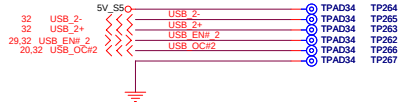


MODEM CABLE CONN

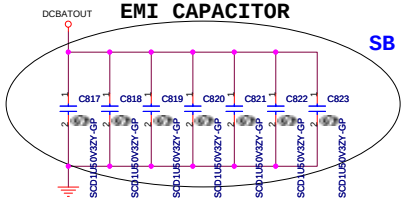


Finger Print CONN

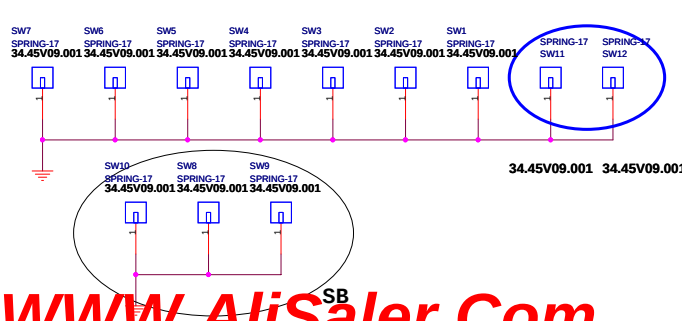
USB BOARD CONN

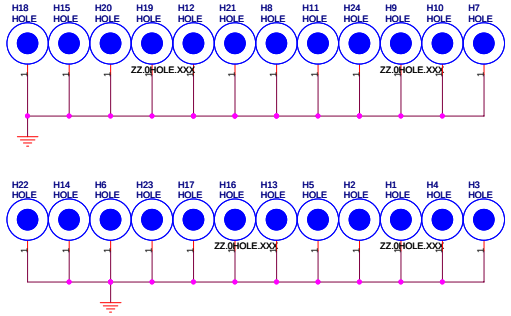


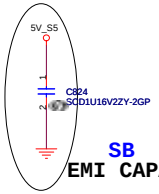
EMI CAPACITOR



FOR EMI Solution







BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TTEST_PAD

Size: C | Document Number: LZ2 | Rev: SB

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