LZ2 Block Diagram

Project code: 91.4K101.001 ZY LZ2
91.4J301.001 XR LX2
PCB P/N : 07260-2
Revision : -2

CLK GEN. 3

Mobile CPU
Penryn SV 35W
4, 5

EMC2102 07

HOST BUS 667/800/1066MHz@1.05V

DDR2 socket 15 — 667/800MHz

DDR2 socket 16 — 667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8,9,10,11,12,13,14

R.G.B → CRT 18

LVDS → 12"W LCD 17

X4 DMI 400MHz

C-Link0

INT MIC

SPR x2

Codec
ALC269
(include AMP)
25

AZALIA

MIC In

HP

RJ11

MODEM
MDC Card
24

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
4 SATA
12 USB
High Definition Audio
LPC I/F
Serial Peripheral I/F
19,20,21,22,23

USB → Realtek RTS5158E Cardreader 28 → SD/MMC/MS 3 in 1 28

PCIe → LAN Boardcom 5906M 26 → RJ45 27

PCIe/ USB → Mini Card a/b/g/n 31

LPC BUS → KBC Winbond WPC776 29 → SPI I/F → BIOS 2M byte 34

LPC DEBUG CONN. 24

KBC → G-sensor 30

KBC → Touch Pad 34

KBC → INT. KB 34

New card 31 — PCI Express / USB

Power switch 31

SATA → SATA-HDD 24

SATA → SATA-ODD 24

USB → Finger Print 32

USB → BlueTooth 24

USB → CAMERA 17

USB → USB 3 Port 32

PCB 8-LAYER STACKUP

TOP
GND
S
S
PWR
S
GND
BOTTOM

SYSTEM DC/DC TPS51120 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 38

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5912 38

1D8V_S3	1D5V_NB_S0

APL5912 38

1D8V_S3	1D5V_SB_S0

CHARGER BQ24740 39

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V UP+5V 5V 100mA

CPU DC/DC ADP3208 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: LZ2 | Rev: SB
Date: Tuesday, June 24, 2008 | Sheet 1 of 41

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved Rising Edge of PWROK.	This signal has a weak internal pull-down. Note:This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap(Server Only) Rising edge of PWROK	Tying this strap low configures DMI for SIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server latforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG11 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1= The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

17,33,35,36,37,39,41	DCBATOUT	DCBATOUT
7,19,29,34,36,39,40	3D3V_AUX_S5	3D3V_AUX_S5
7,31,33,36,39	5V_AUX_S5	5V_AUX_S5
17,20,21,22,23,24,26,29,30,31,33,34,36	3D3V_S5	3D3V_S5
17,22,32,33,34,36,37,38,41	5V_S5	5V_S5
10,12,13,15,16,33,37,38,41	1D8V_S3	1D8V_S3
3,7,10,11,13,15,16,17,18,19,20,21,22,23,24,25,26,28,29,31,32,33,34,35,36,37,41	3D3V_S0	3D3V_S0
7,13,17,18,22,23,24,25,33,34,35,41	5V_S0	5V_S0
4,5,6,8,10,11,12,13,19,22,33,37	1D05V_S0	1D05V_S0
19,20,22,31,33,38	1D5V_SB_S0	1D5V_SB_S0
3,5,13,31,33,38	1D5V_NB_S0	1D5V_NB_S0

PCIE Routing

LANE1	BroadCom LAN
LANE2	MiniCard WLAN
LANE4	NewCard

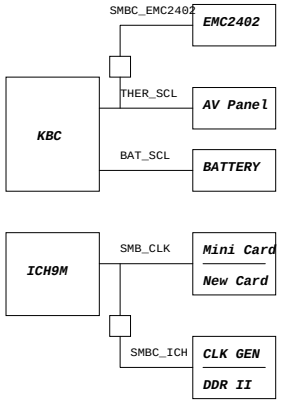
History:

LAB: 2008/01/02

USB Table

USB	
Pair	Device
0	JACK0
1	NC
2	JACK2
3	NC
4	BLUETOOTH
5	JACK1
6	Fringer Print
7	Mini Card
8	CAMERA
9	NEW CARD
10	CARDREADER
11	NC

SMBus



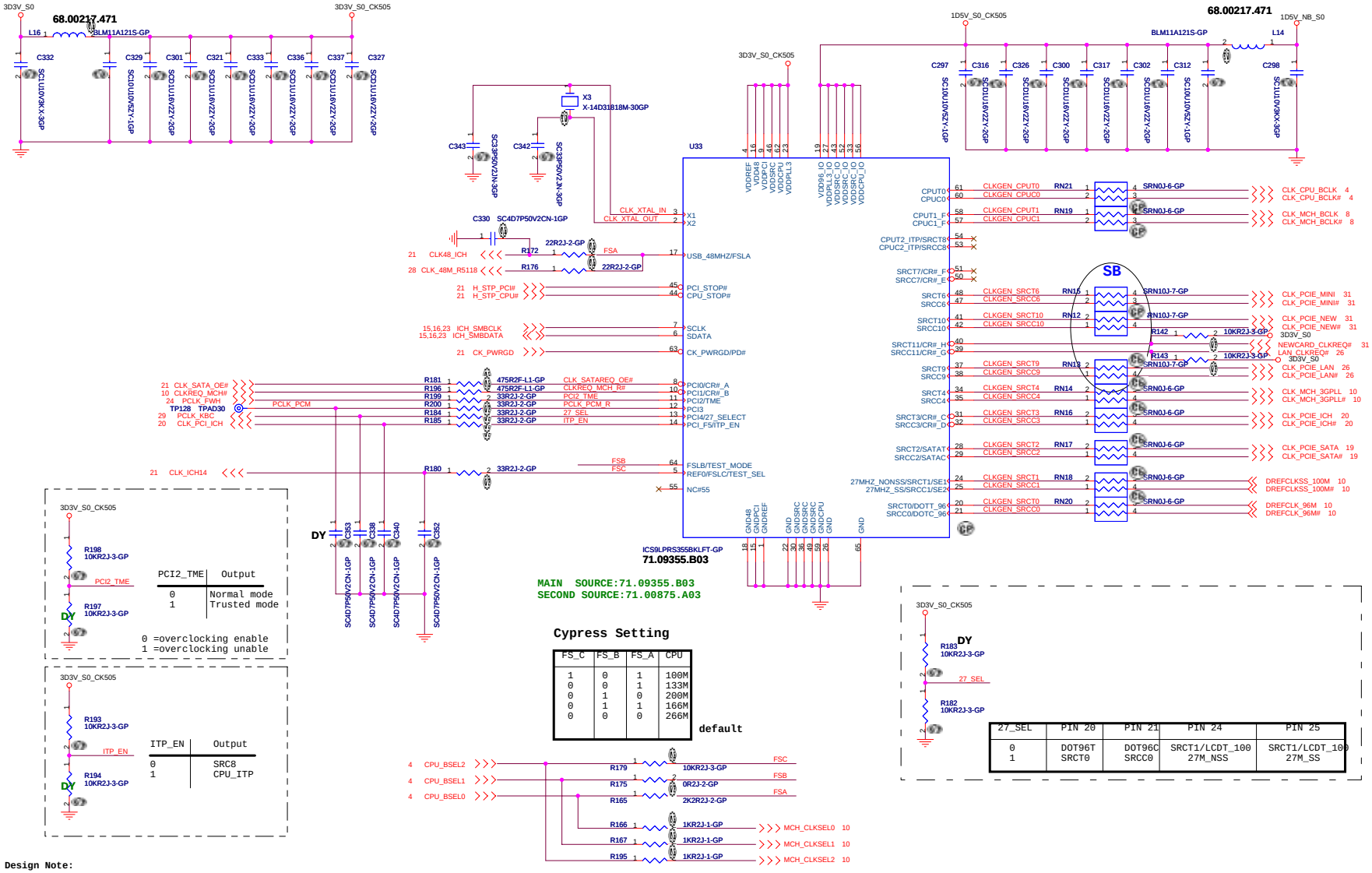
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 2 of 41



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

Wistron Corporation
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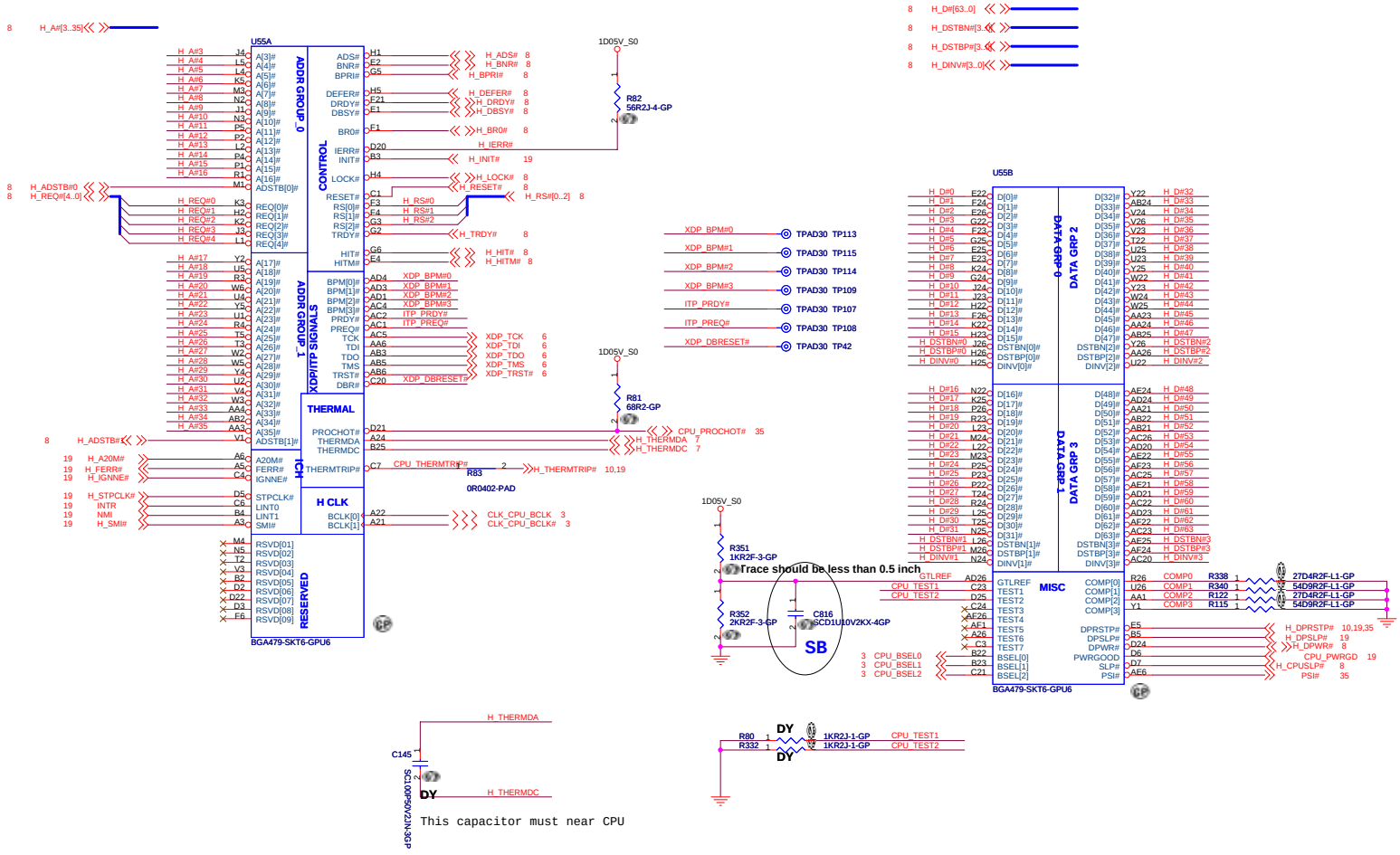
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size	Document Number	Rev
	LZ2	SB

Date: Monday, June 23, 2008 Sheet 3 of 41



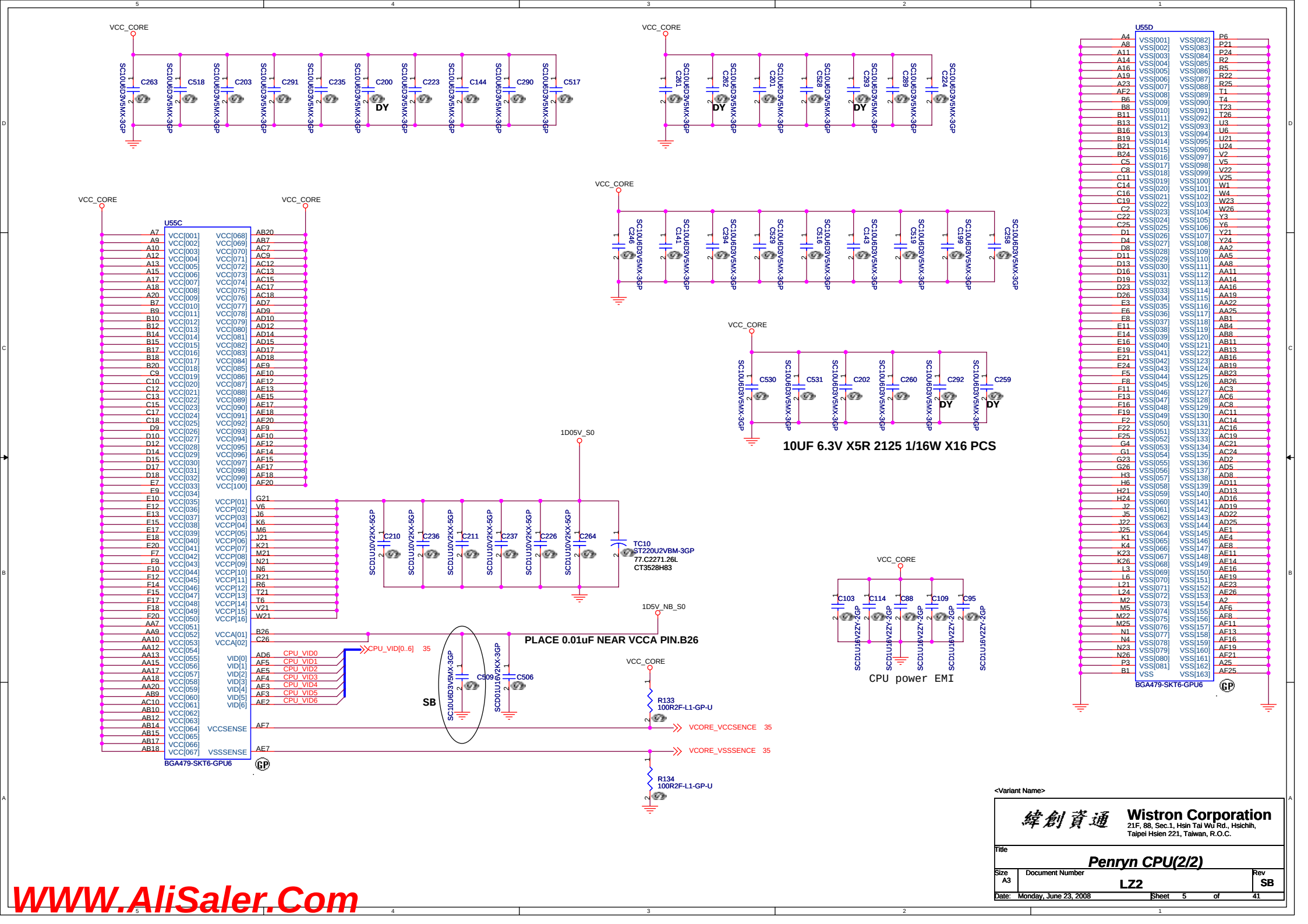
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Penryn CPU(1/2)

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 4 of 41



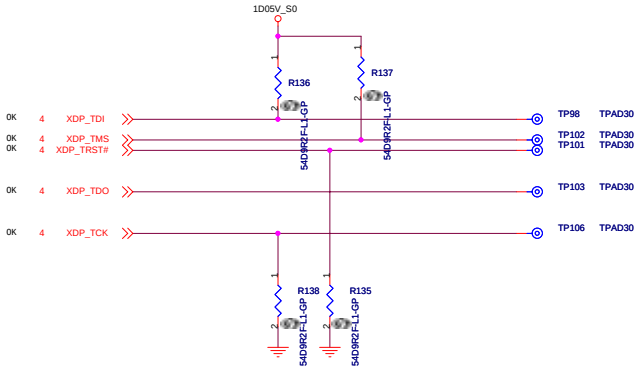
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Penryn CPU(2/2)

Size	Document Number	Rev
A3	LZ2	SB

Date: Monday, June 23, 2008 Sheet 5 of 41



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP CONN

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 6 of 41

Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing

Layout notice :
Both H_THERMDA_1 and THERMDC_1 routing
10 mil trace width and 10 mil spacing

Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing

Layout 15 mil

20.F0714.003

Layout notice :
C809, C811, C812
close to chip side;

CPU0

SYSTEM

This cap should close to thermal diode.

EMC2102

EMC2102-DZK-GP
74.02102.A73

SC

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

SC
73.7SZ08.AAH
220ms delay time after Power-on

Dummy when G792 enhanced T8 function

HW thermal shut down tempature
setting 95 degree . Put Near CPU .

Rset=0.0012*T^2-0.9308*T+96.147

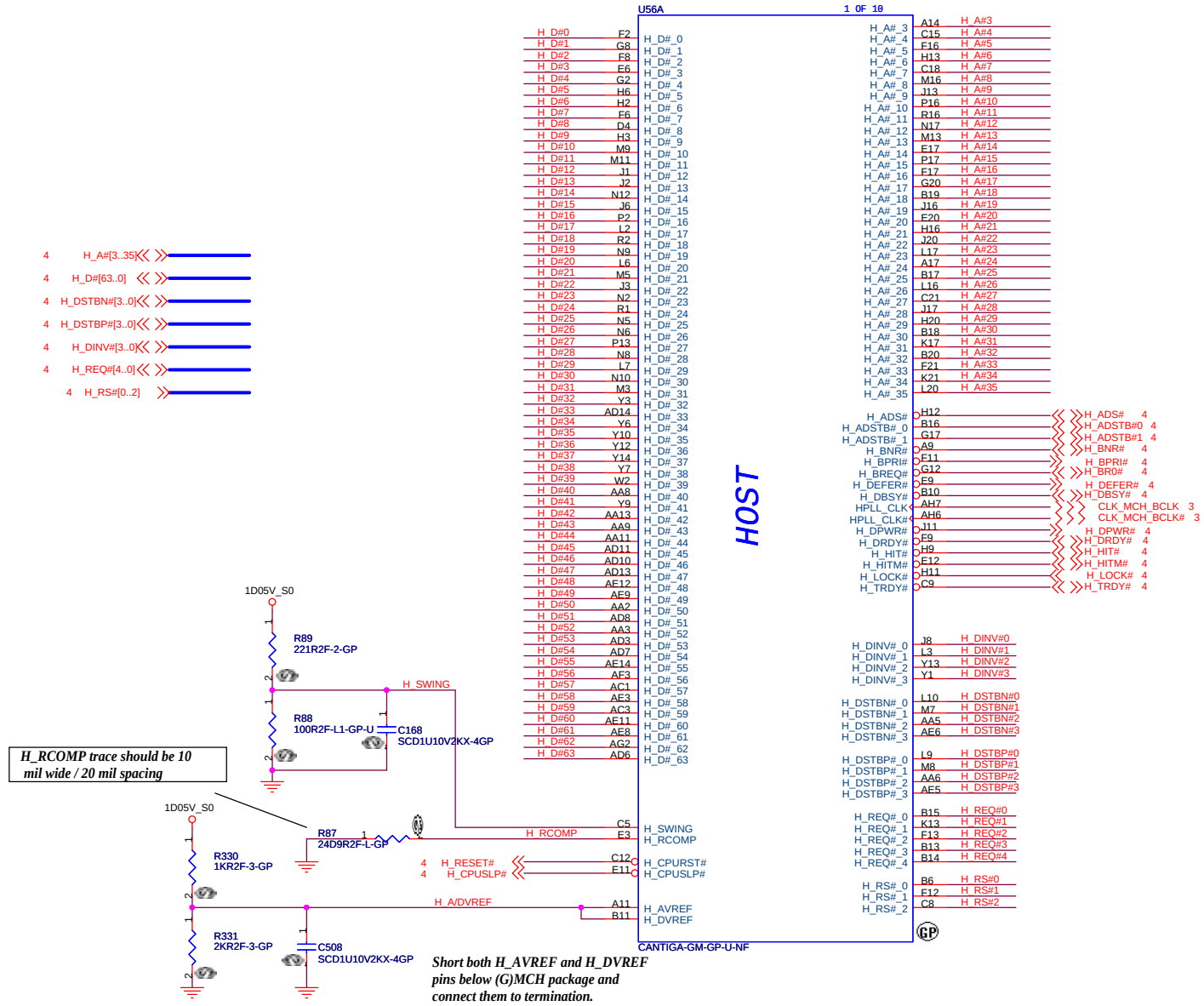
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 7 of 41



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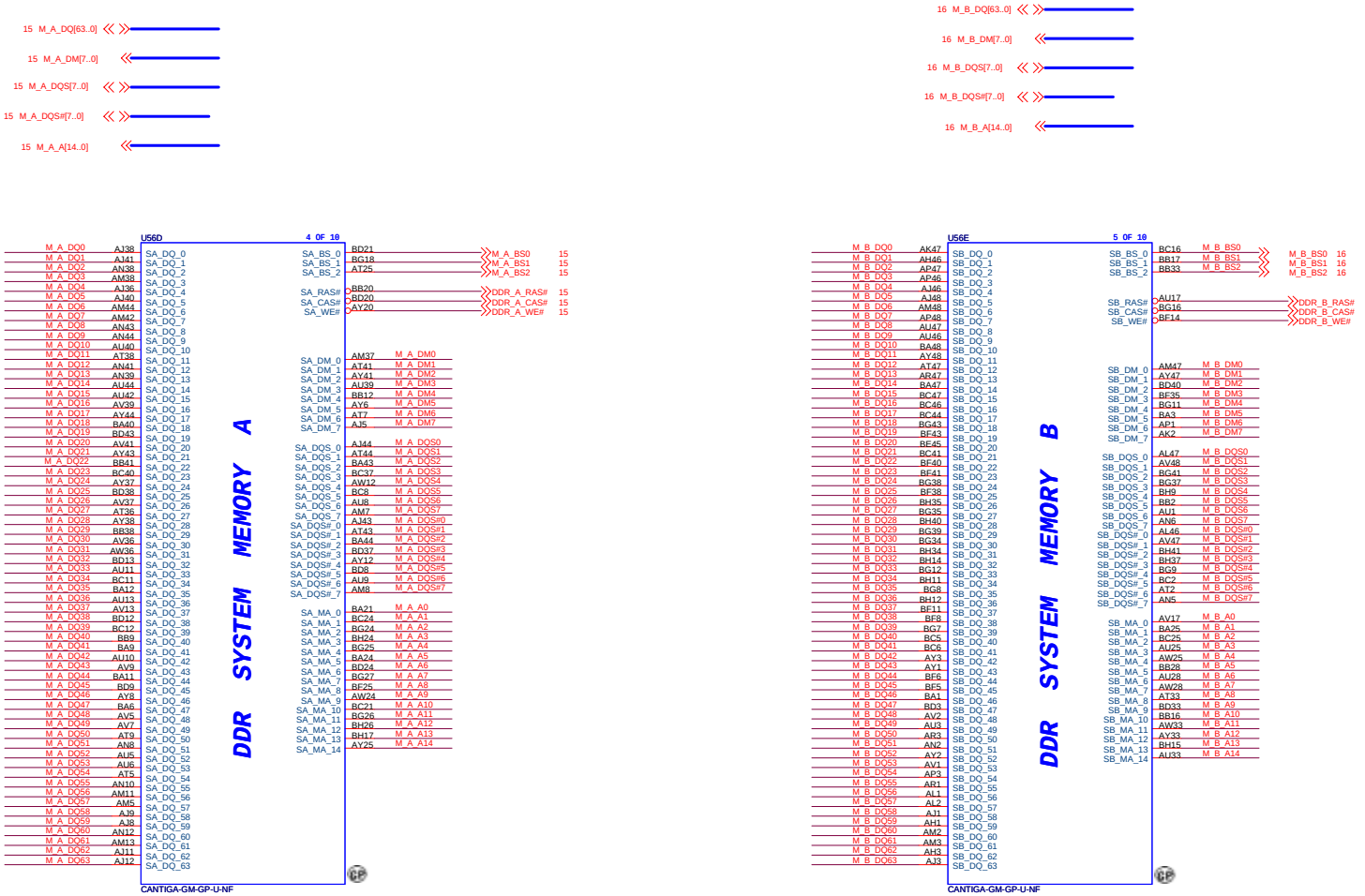
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Cantiga(1/7):HOST I/F		
Size: A3	Document Number: LZ2	Rev: SB
Date: Monday, June 23, 2008	Sheet 8 of 41	



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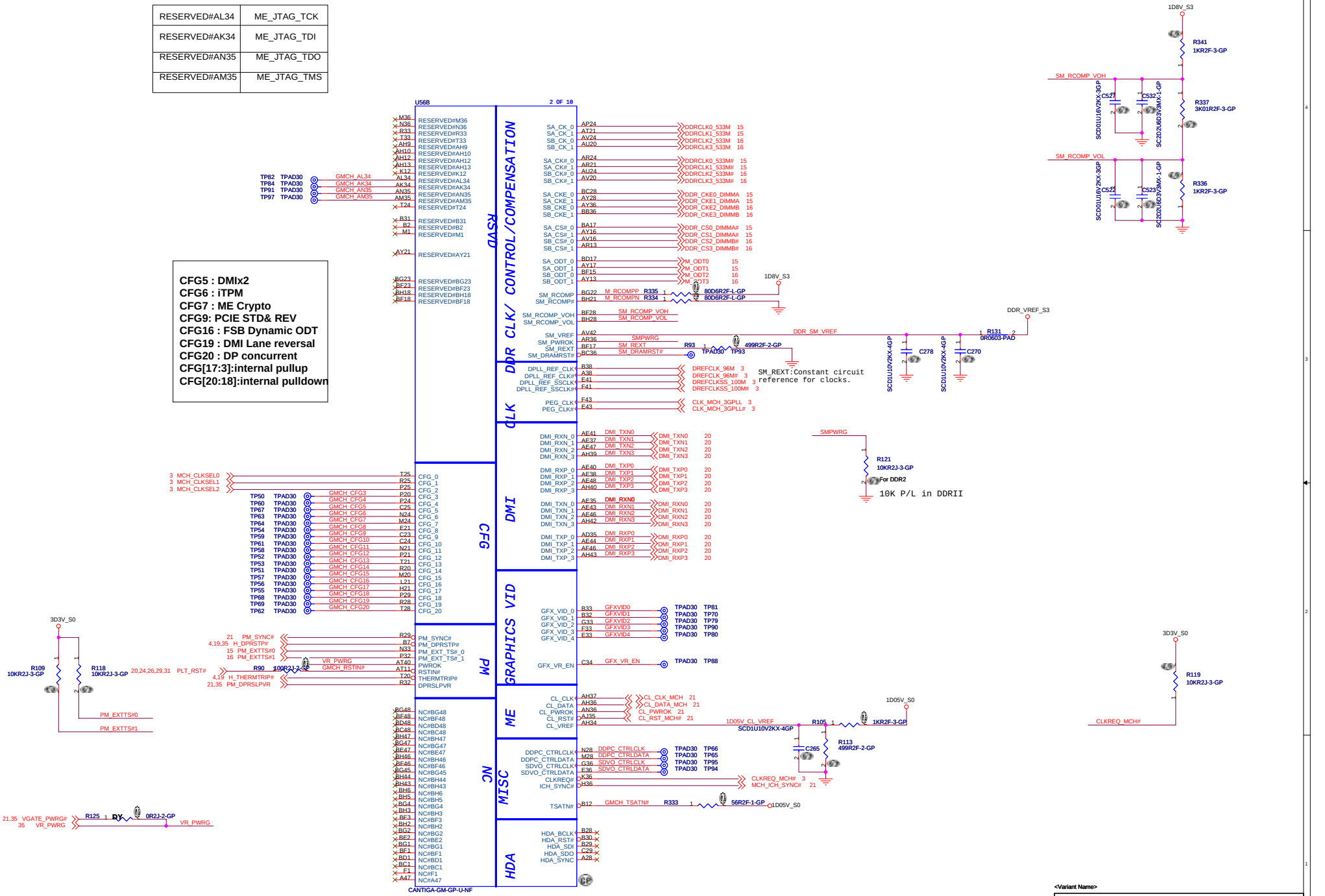
蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Cantiga(2/7):DDR3		
Size C	Document Number LZ2		Rev SB
Date: Monday, June 23, 2008	Sheet 9	of	41

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown

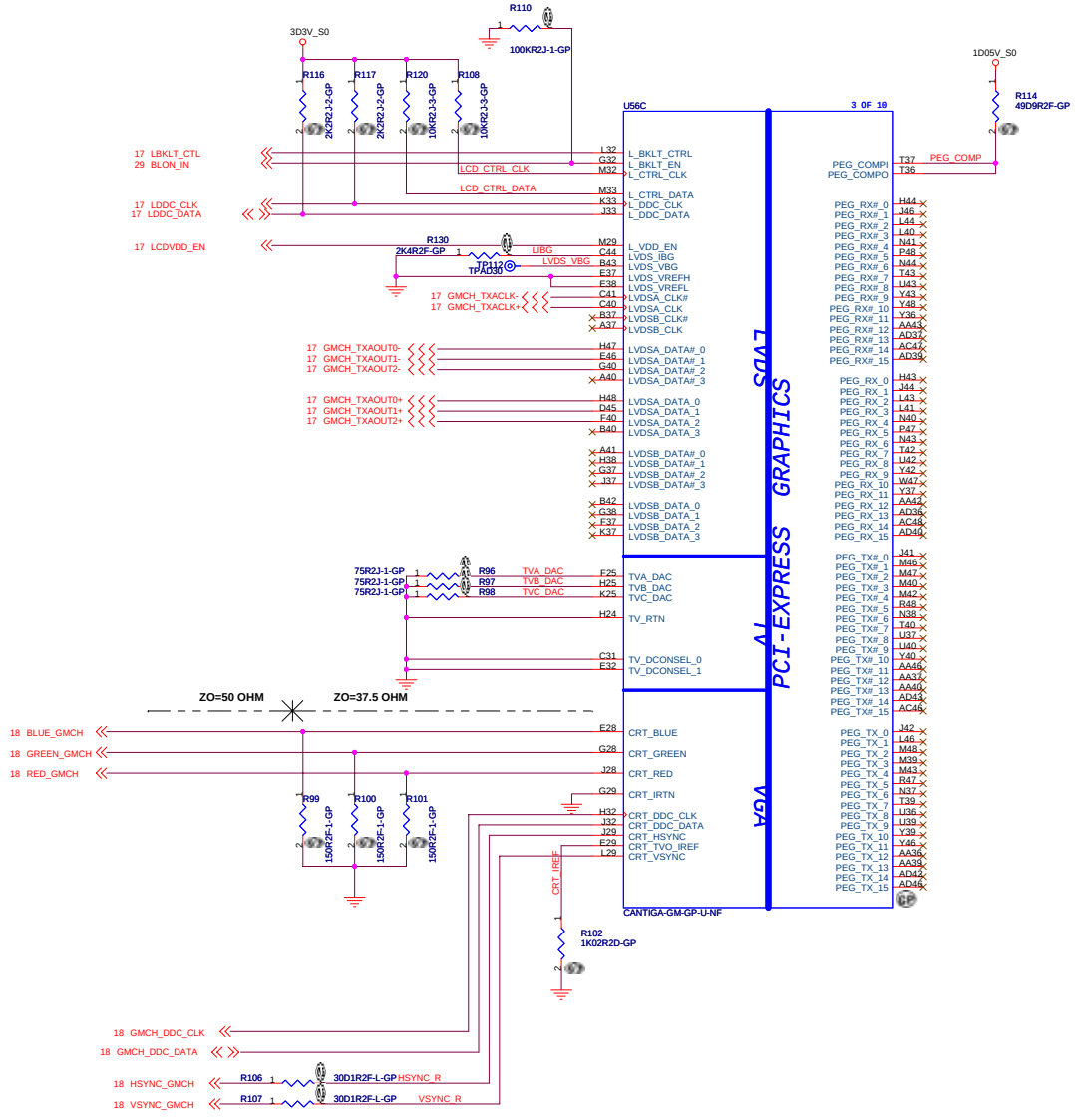


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(3/7):DMI/PM/CFG/GF

Size: C | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 10 of 41



<Variant Name>

Wistron Corporation
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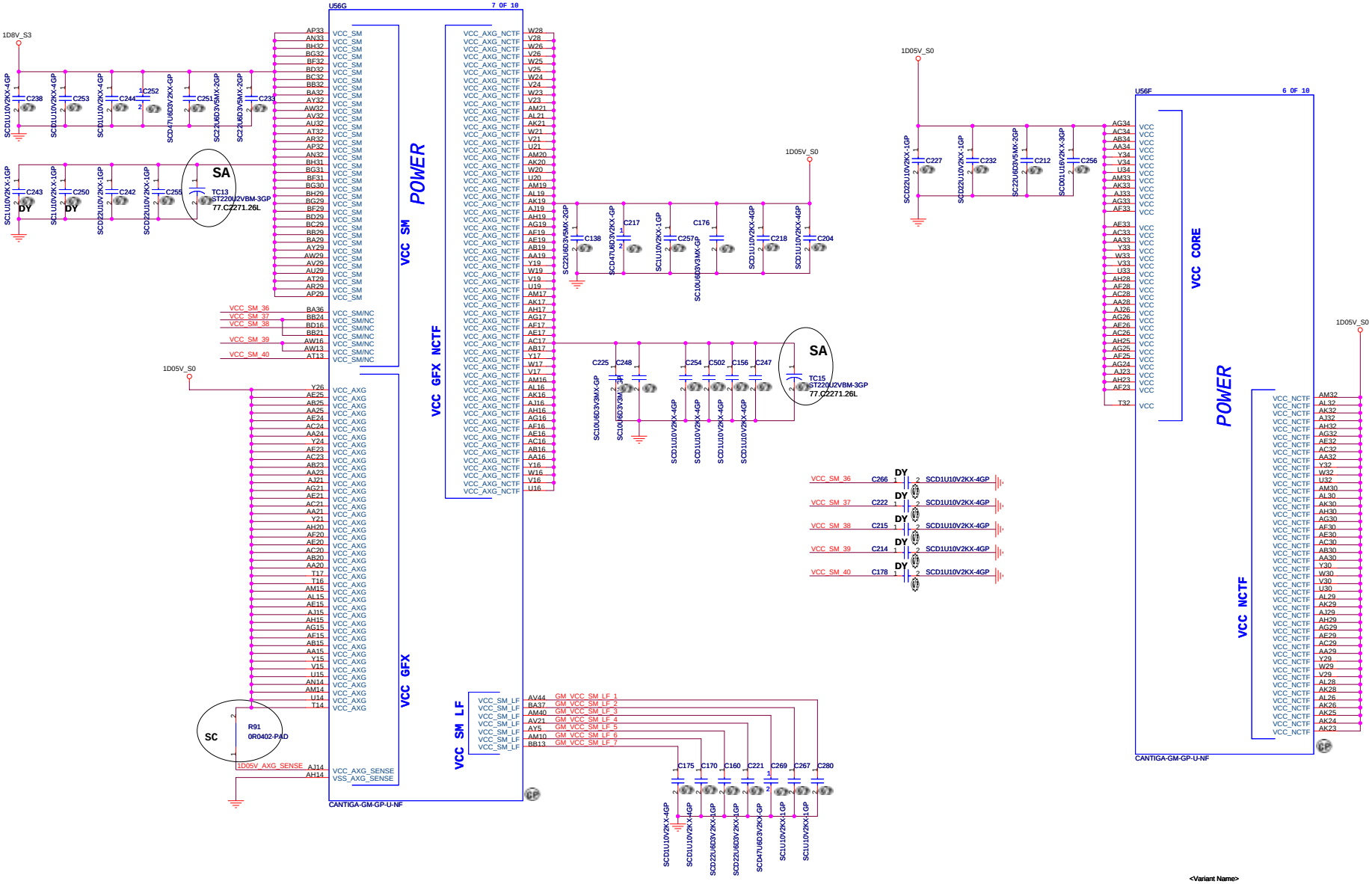
Taipei Hsien 221, Taiwan, R.O.C.

Title: CANTIGA(5/7)-VGA/LVDS

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 11 of 41



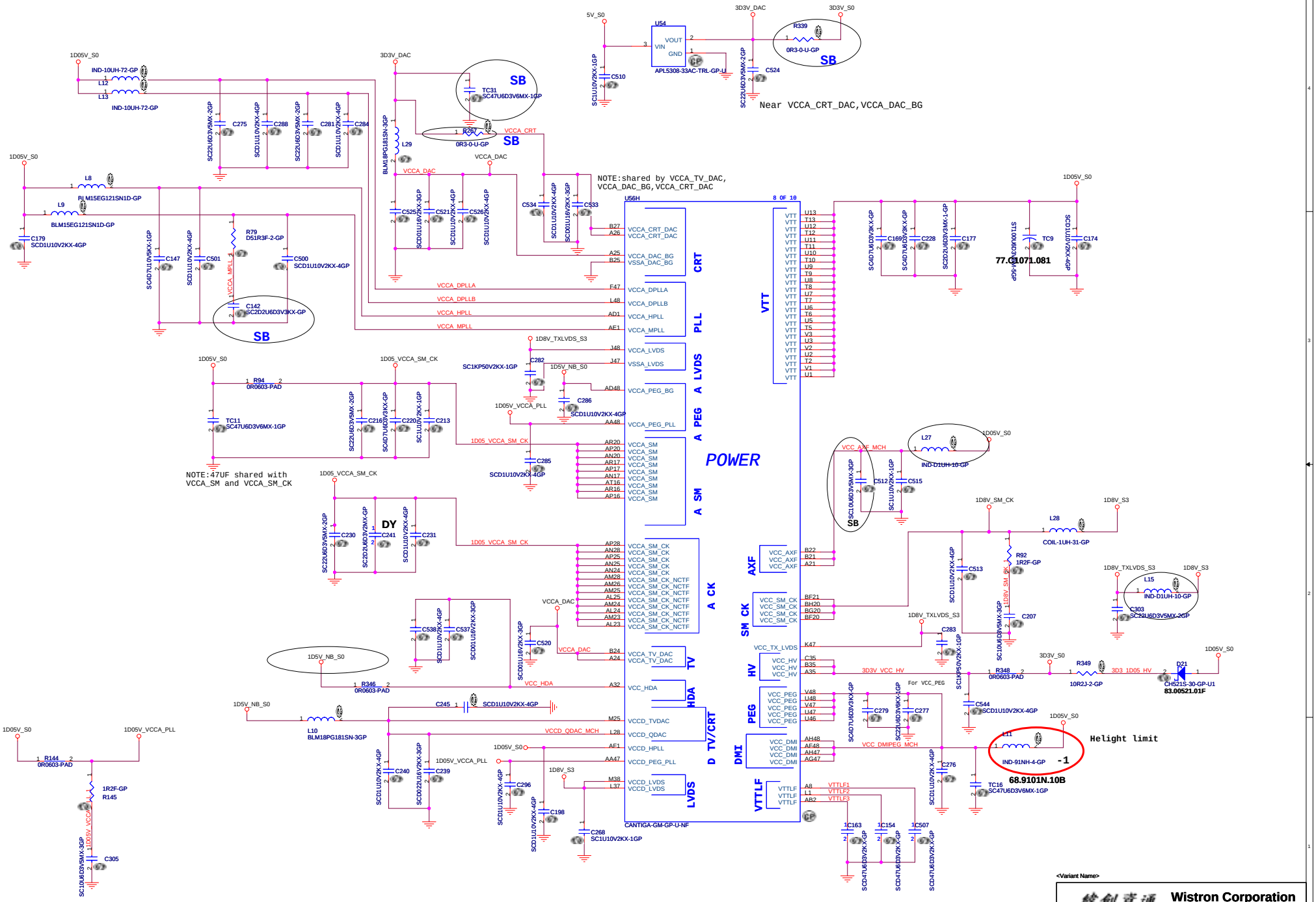
<Variant Name>

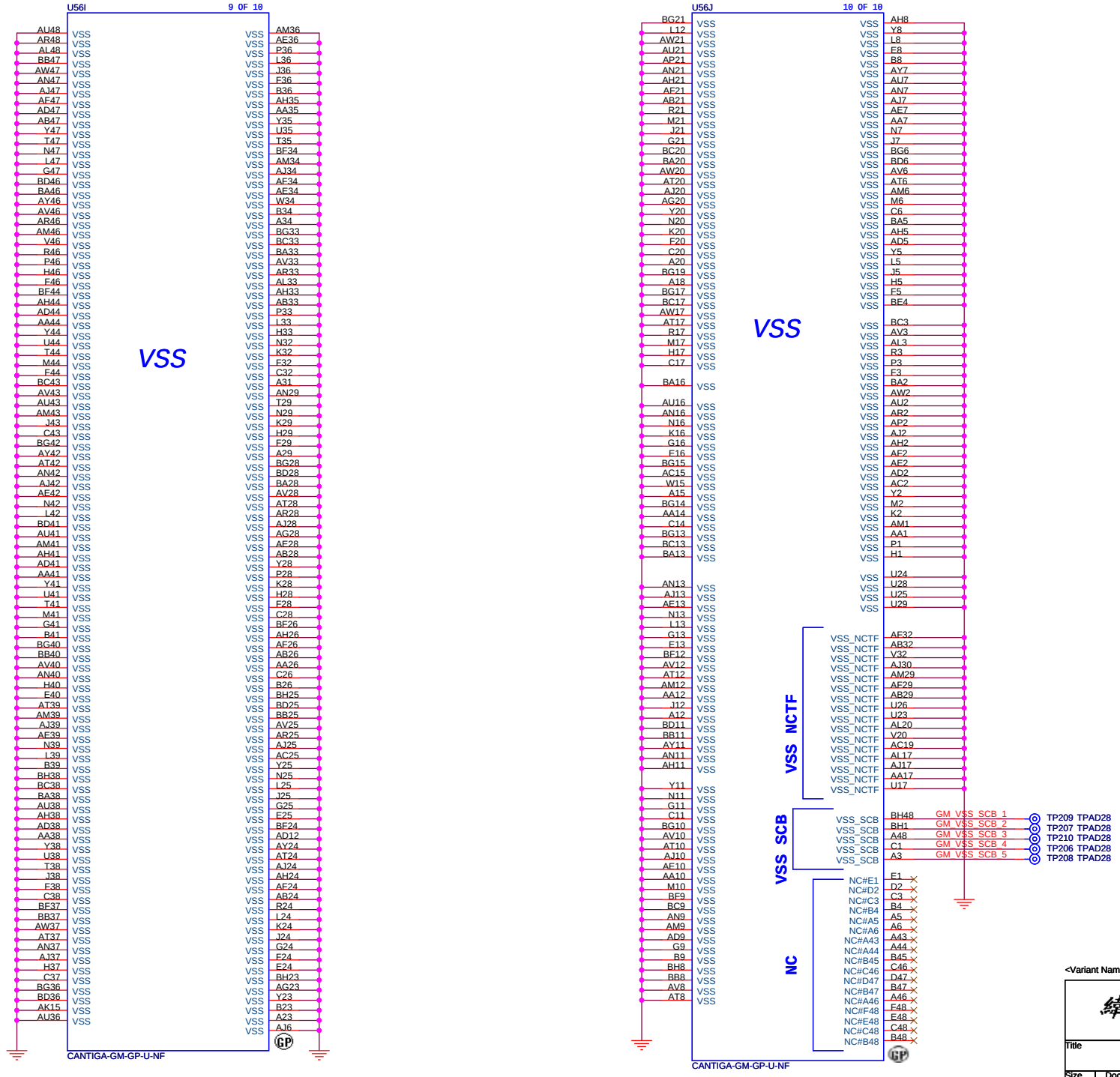
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(5/7):VCC

Size: C | Document Number: LZ2 | Rev: SB

Date: Wednesday, April 09, 2008 | Sheet 12 of 41





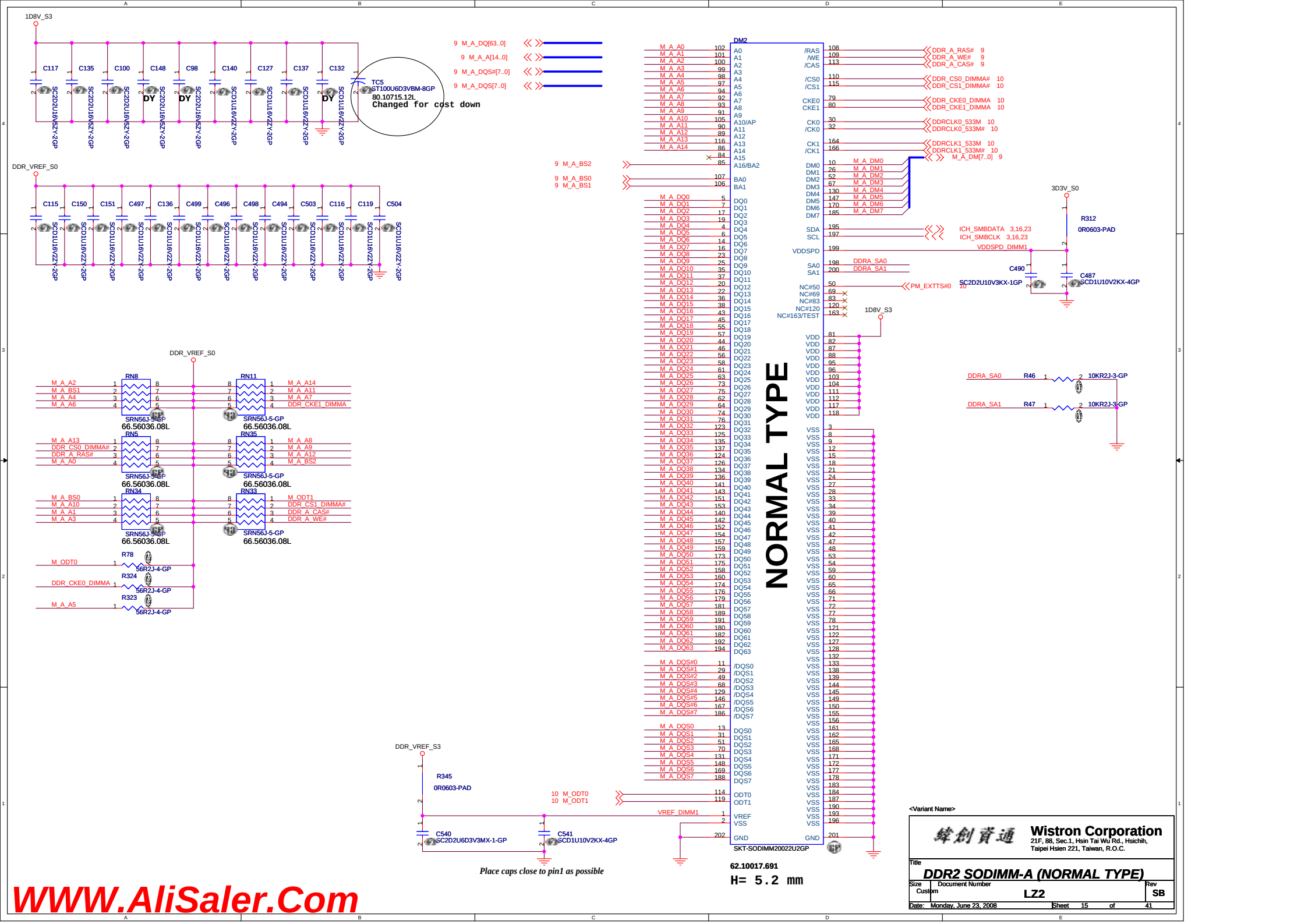
<Variant Name>

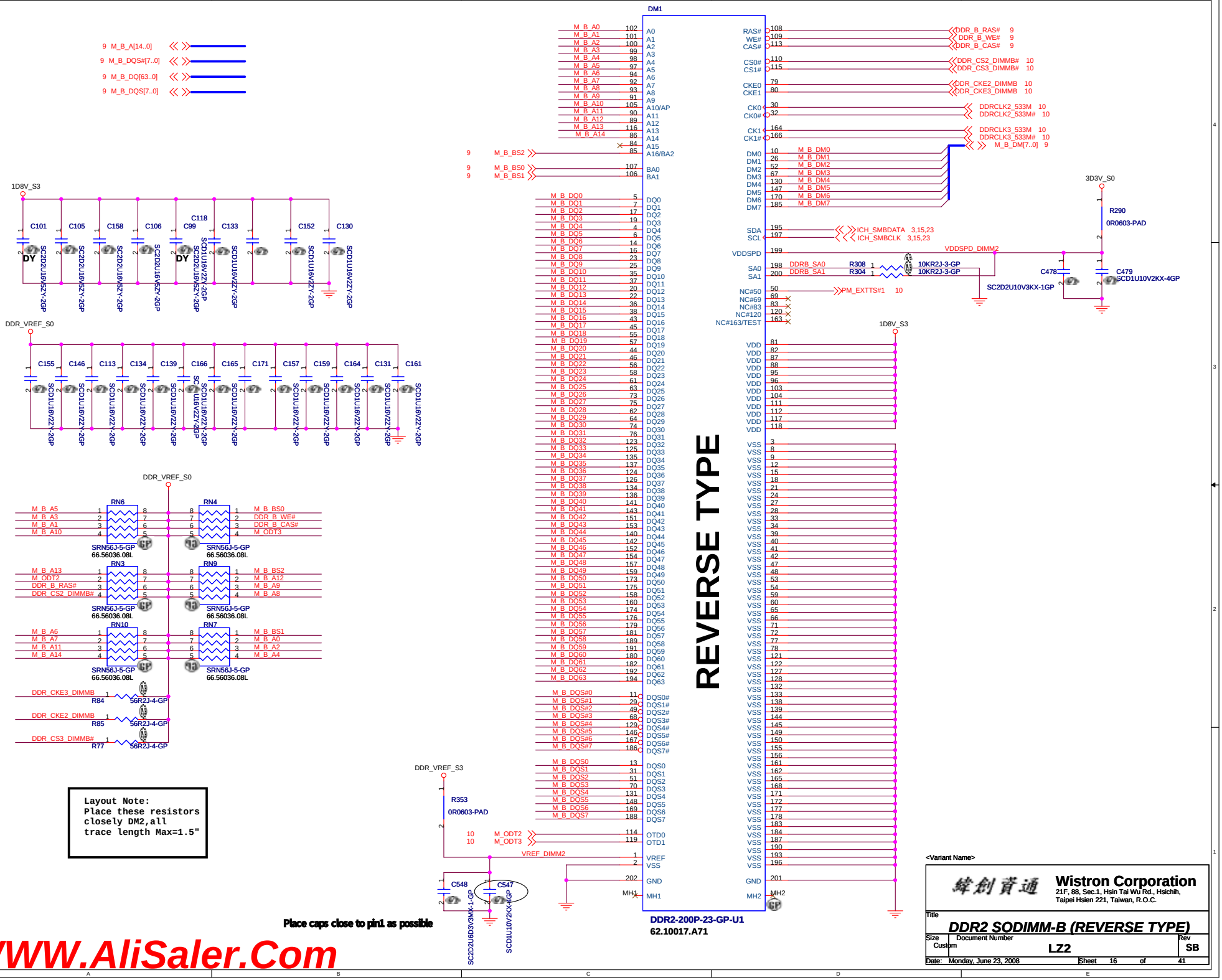
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(8/7):GND

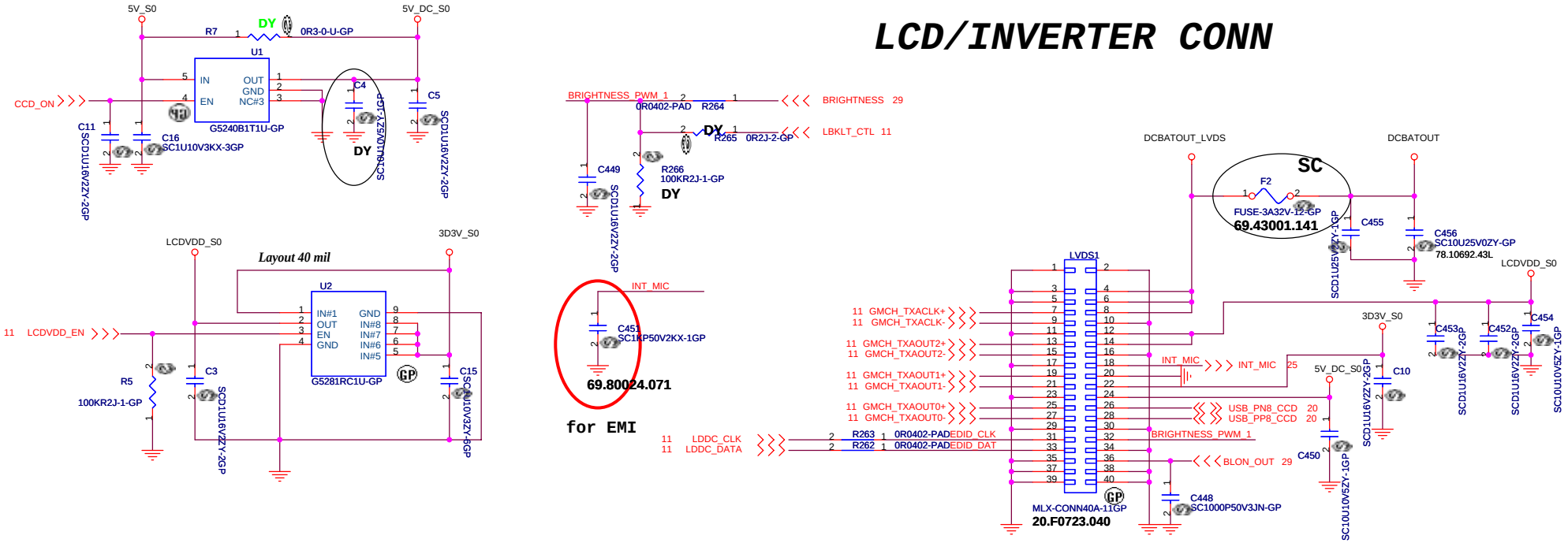
Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 09, 2008 Sheet 14 of 41




9 M_B_A[14..0]
9 M_B_DQS#[7..0]
9 M_B_DQ[63..0]
9 M_B_DQS[7..0]
DM1
REVERSE TYPE
DDR2-200P-23-GP-U1
62.10017.A71
1D8V_S3
3D3V_S0
DDR_VREF_S0
DDR_VREF_S3
C101
C105
C158
C106
C118
C99
C133
C152
C130
C155
C146
C113
C134
C139
C166
C165
C171
C157
C159
C164
C131
C161
RN6
RN4
RN3
RN9
RN10
RN7
SRN56J-5-GP
66.56036.08L
R84
R85
R77
56R2J-4-GP
R308
R304
10KR2J-3-GP
R290
0R0603-PAD
R353
C548
C547
C478
C479
SCD1U10V2KX-4GP
SC2D2U10V3KX-1GP
VDDSPD_DIMM2
VREF_DIMM2
Layout Note:
Place these resistors
closesly DM2,all
trace length Max=1.5"
Place caps close to pin1 as possible
WWW.AliSaler.Com
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 SODIMM-B (REVERSE TYPE)
Size
Custom
Document Number
LZ2
Rev
SB
Date: Monday, June 23, 2008
Sheet 16 of 41

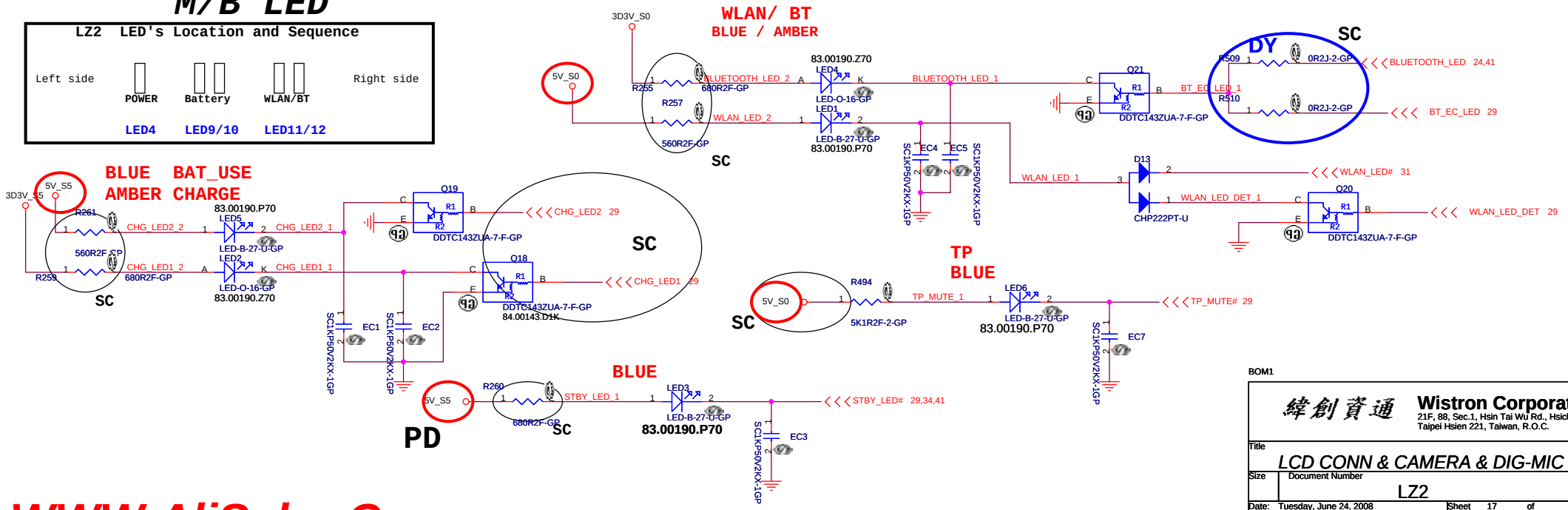
LCD/INVERTER CONN



M/B LED

LZ2 LED's Location and Sequence

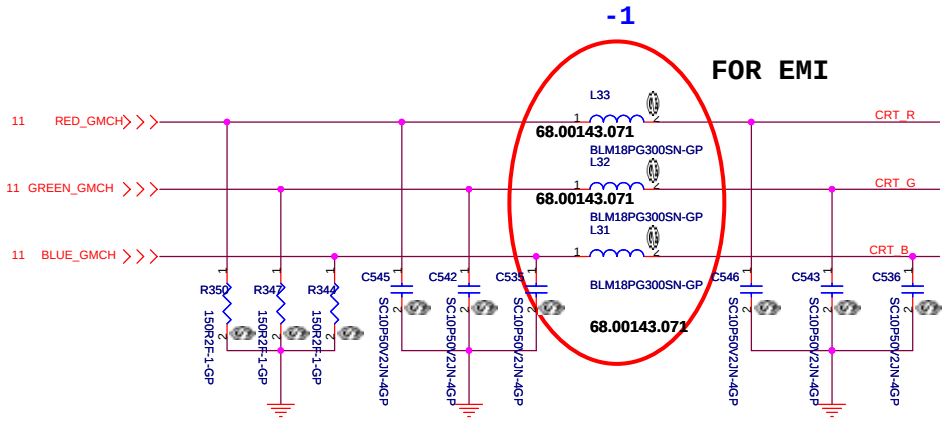
Left side	POWER	Battery	WLAN/BT	Right side
	LED4	LED9/10	LED11/12	

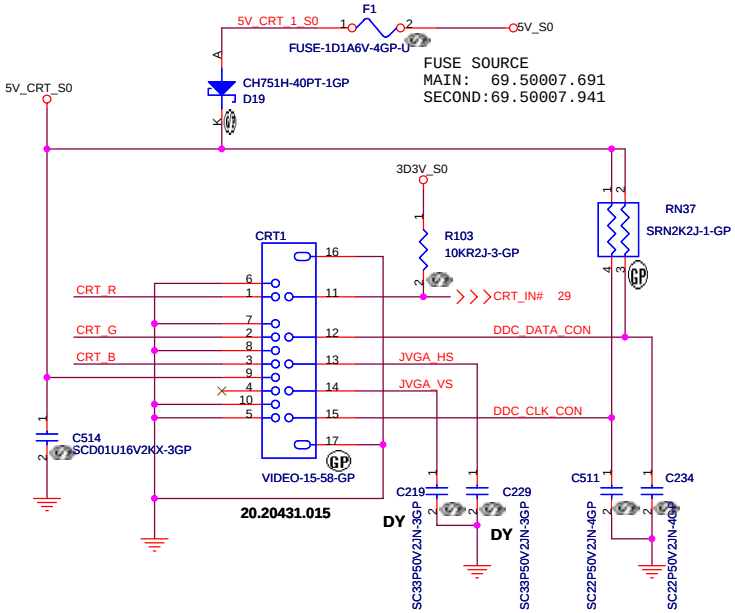


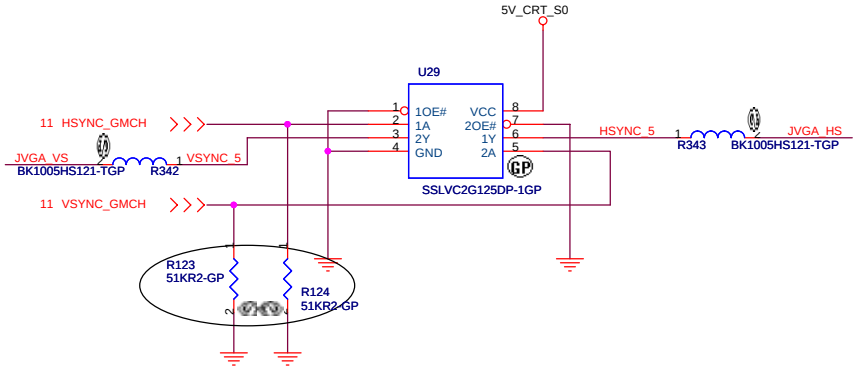
BOM1

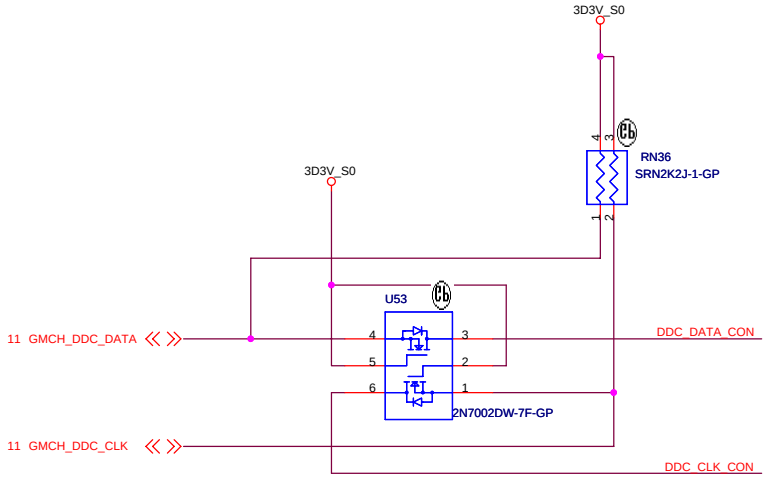
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

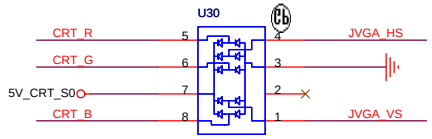
Title	LCD CONN & CAMERA & DIG-MIC	
Size	Document Number	Rev
	LZ2	SB
Date: Tuesday, June 24, 2008	Sheet 17 of 41	

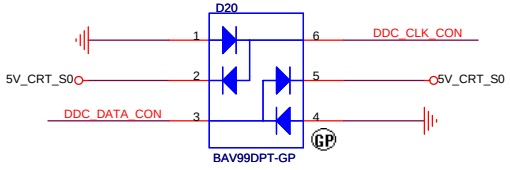












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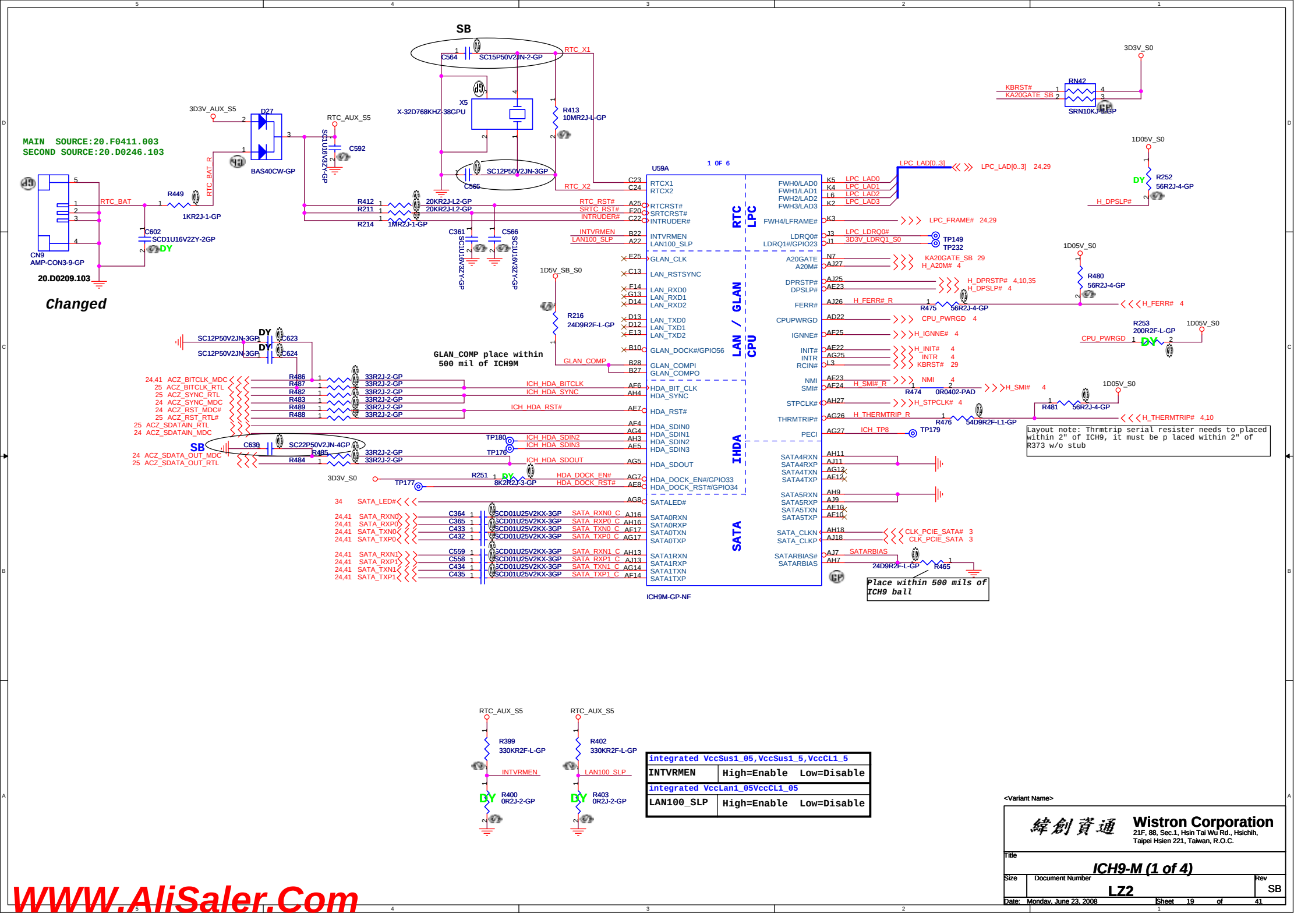
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector

Size | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 18 of 41


SB
MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103
20.D0209.103
Changed
U59A
1 OF 6
ICH9M-GP-NF
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
Layout note: Thrmtrip serial resister needs to placed within 2" of ICH9, it must be p laced within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
LZ2
SB
Monday, June 23, 2008
19 of 41
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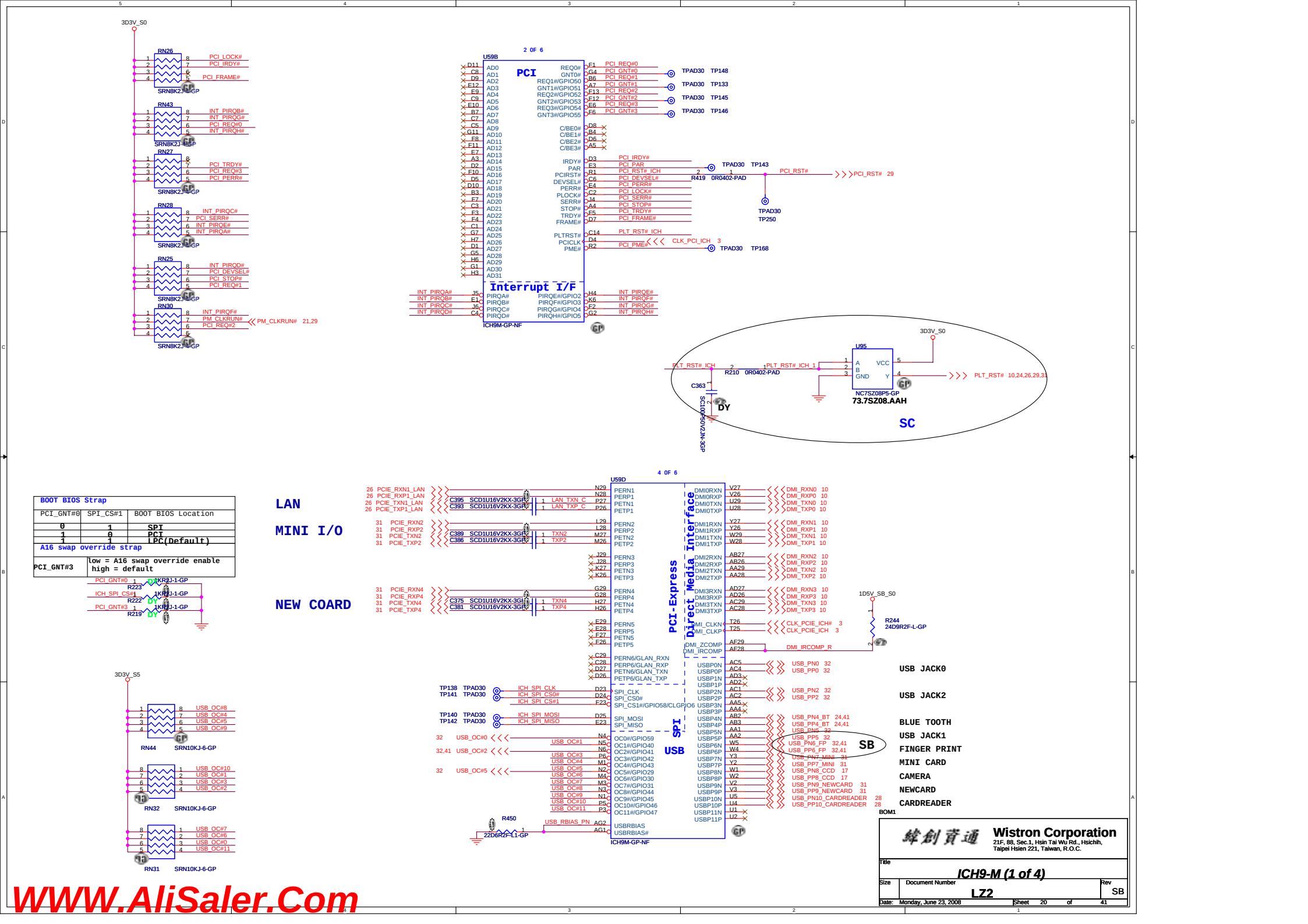

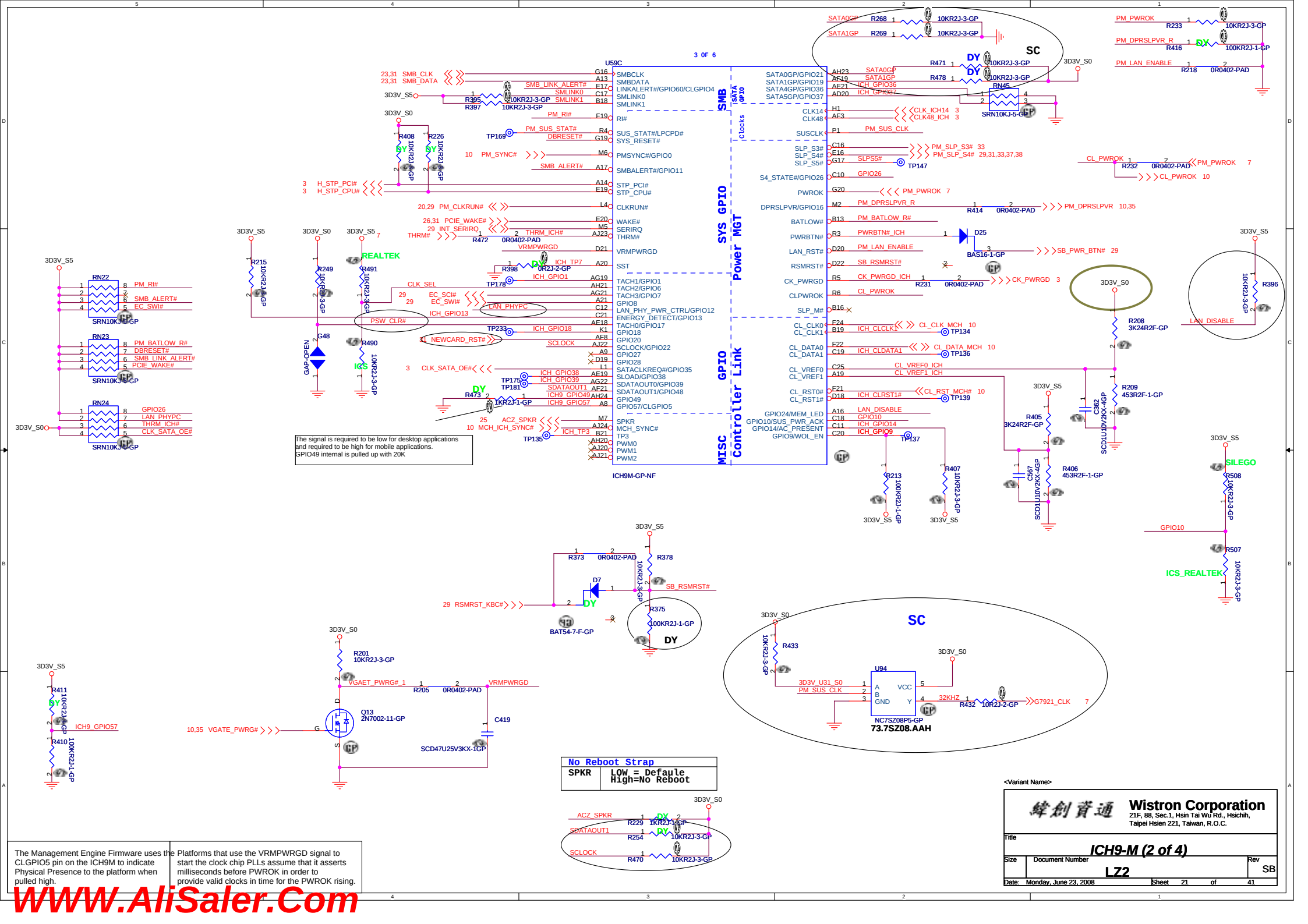
U59C
3 OF 6
ICH9M-GP-NF
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SC
REALTEK
ICS
SILEGO
GAP-OPEN
DY
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
3D3V_S5
3D3V_S0
SMB_CLK
SMB_DATA
SMB_LINK_ALERT#
PM_RI#
PM_SUS_STAT#
DBRESET#
PM_SYNC#
SMB_ALERT#
H_STP_PCI#
H_STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
THRM#
VRMPWRGD
ICH_TP7
ICH_GPIO1
CLK_SEL
EC_SCI#
EC_SWI#
LAN_PHYPC
PSW_CLR#
ICH_GPIO13
ICH_GPIO18
NEWCARD_RST#
SCLOCK
CLK_SATA_OE#
ICH_GPIO38
ICH_GPIO39
SDATAOUT1
ICH9_GPIO49
ICH9_GPIO57
ACZ_SPKR
MCH_ICH_SYNC#
ICH_TP3
SATA0GP
SATA1GP
ICH_GPIO36
ICH_GPIO37
CLK_ICH14
CLK48_ICH
PM_SUS_CLK
SLP_S3#
SLP_S4#
SLPS5#
GPIO26
PM_PWROK
PM_DPRSLPVR_R
PM_BATLOW_R#
PWRBTN#_ICH
LAN_ENABLE
SB_RSMRST#
CK_PWRGD_ICH
CL_PWROK
ICH_CLCLK1
ICH_CLDATA1
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST_MCH#
ICH_CLRST1#
LAN_DISABLE
GPIO10
ICH_GPIO14
ICH_GPIO9
SB_PWR_BTN#
CL_CLK_MCH
CL_DATA_MCH
R268 10KR2J-3-GP
R269 10KR2J-3-GP
R471 10KR2J-3-GP
R478 10KR2J-3-GP
RN45 SRN10KJ-5-GP
R233 10KR2J-3-GP
R416 100KR2J-1-GP
R218 0R0402-PAD
R232 0R0402-PAD
R414 0R0402-PAD
R231 0R0402-PAD
D25 BAS16-1-GP
R208 3K24R2F-GP
R209 453R2F-1-GP
R405 3K24R2F-GP
R406 453R2F-1-GP
C362 SCD1U10V2KX-4GP
C567 SCD1U10V2KX-4GP
R396 10KR2J-3-GP
R508 10KR2J-3-GP
R507 10KR2J-3-GP
R213 100KR2J-1-GP
R407 10KR2J-3-GP
TP134
TP136
TP139
TP137
TP147
TP169
TP233
TP175
TP181
TP135
R395 10KR2J-3-GP
R397 10KR2J-3-GP
R408 10KR2J-3-GP
R226 10KR2J-3-GP
R472 0R0402-PAD
R398 0R2J-2-GP
R178 10KR2J-3-GP
R215 10KR2J-3-GP
R249 10KR2J-3-GP
R491 10KR2J-3-GP
R490 10KR2J-3-GP
R473 1KR2J-1-GP
RN22 SRN10KJ-5-GP
RN23 SRN10KJ-5-GP
RN24 SRN10KJ-5-GP
R373 0R0402-PAD
R378 10KR2J-3-GP
R375 100KR2J-1-GP
D7 BAT54-7-F-GP
R433 10KR2J-3-GP
U94 NC7SZ08P5-GP
73.7SZ08.AAH
32KHZ
R432 10KR2J-2-GP
G7921_CLK
R201 10KR2J-3-GP
R205 0R0402-PAD
Q13 2N7002-11-GP
C419 SCD47U25V3KX-1GP
VGATE_PWRG#_1
VRMPWRGD
10,35 VGATE_PWRG#
R411 10KR2J-3-GP
R410 100KR2J-1-GP
ICH9_GPIO57
R229 1KR2J-1-GP
R254 10KR2J-3-GP
R470 10KR2J-3-GP
SDATAOUT1
SCLOCK
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
The signal is required to be low for desktop applications and required to be high for mobile applications. GPIO49 internal is pulled up with 20K
The Management Engine Firmware uses the CLGPIO5 pin on the ICH9M to indicate Physical Presence to the platform when pulled high.
Platforms that use the VRMPWRGD signal to start the clock chip PLLs assume that it asserts milliseconds before PWROK in order to provide valid clocks in time for the PWROK rising.
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
LZ2
Rev
SB
Date: Monday, June 23, 2008
Sheet 21 of 41
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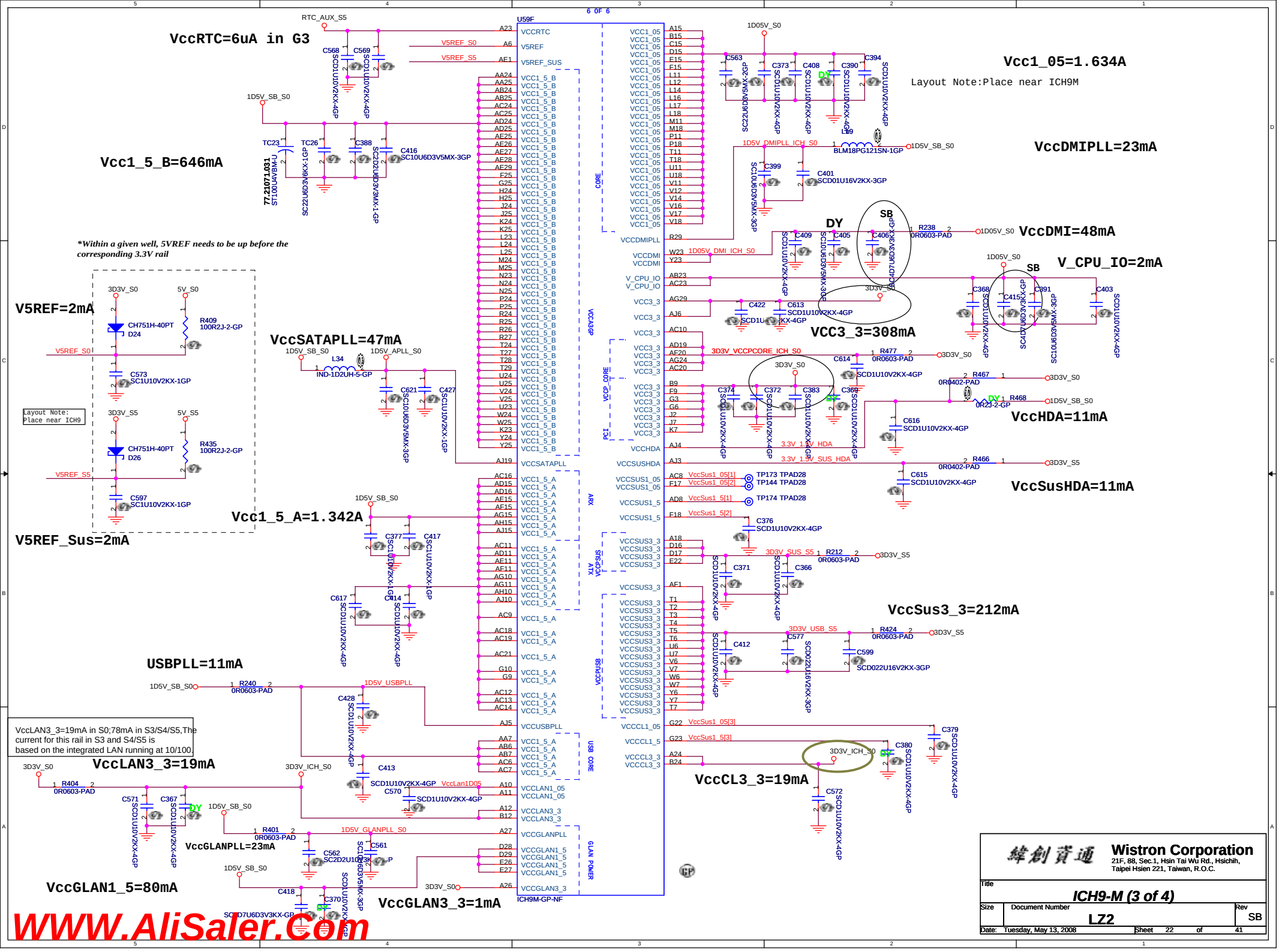
VccRTC=6uA in G3
Vcc1_5_B=646mA
Vcc1_05=1.634A
Layout Note:Place near ICH9M
VccDMIPLL=23mA
VccDMI=48mA
V_CPU_IO=2mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
V5REF=2mA
VccSATAPLL=47mA
VCC3_3=308mA
VccHDA=11mA
Layout Note: Place near ICH9
V5REF_Sus=2mA
Vcc1_5_A=1.342A
VccSusHDA=11mA
VccSus3_3=212mA
USBPLL=11mA
VccLAN3_3=19mA
VccLAN3_3=19mA in S0;78mA in S3/S4/S5,The current for this rail in S3 and S4/S5 is based on the integrated LAN running at 10/100.
VccCL3_3=19mA
VccGLANPLL=23mA
VccGLAN1_5=80mA
VccGLAN3_3=1mA
U59F
6 OF 6
ICH9M-GP-NF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
LZ2
SB
Tuesday, May 13, 2008
Sheet 22 of 41
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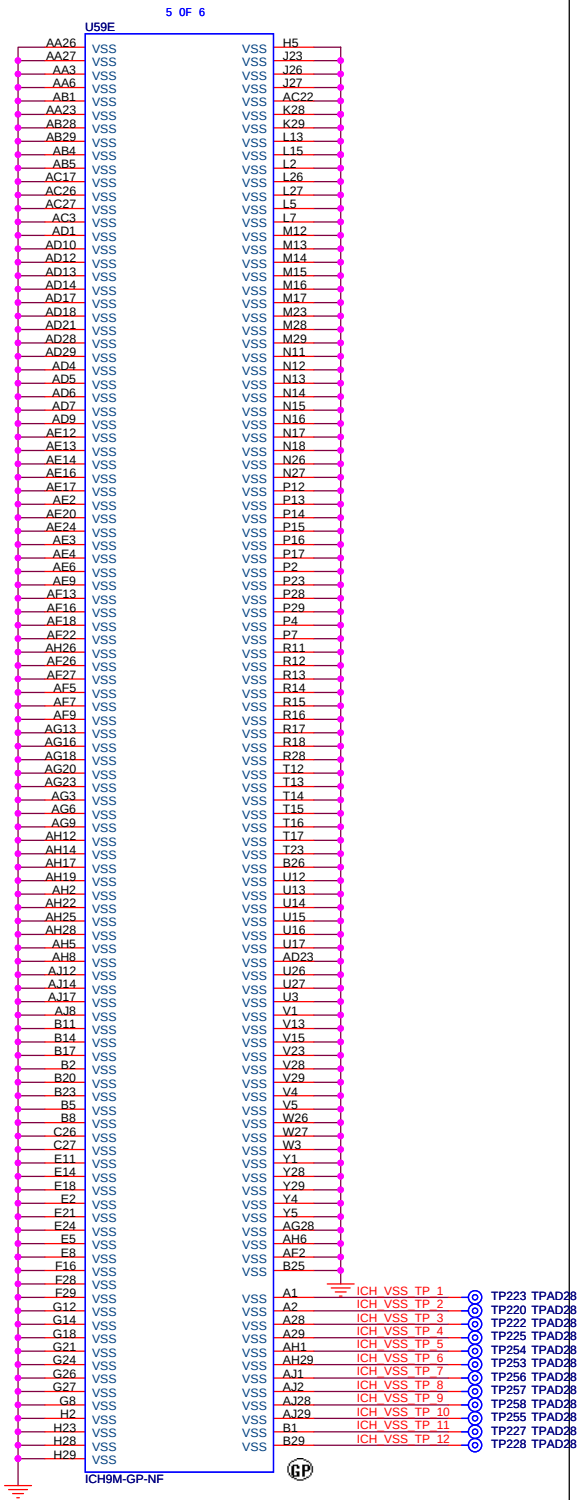

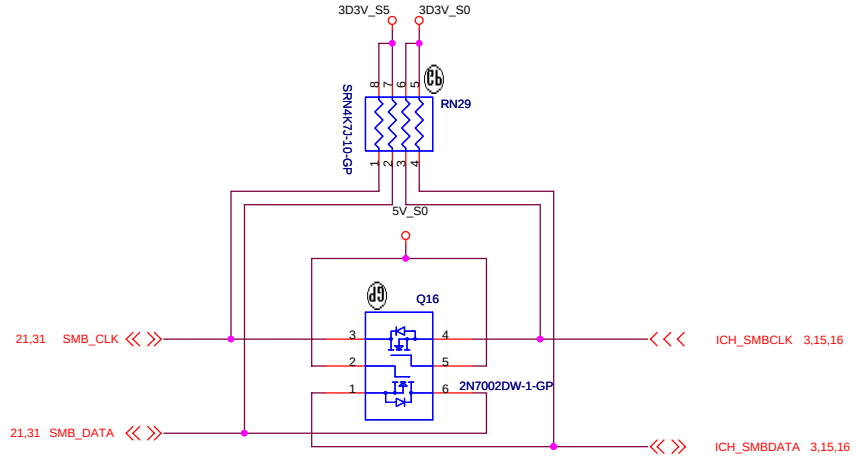

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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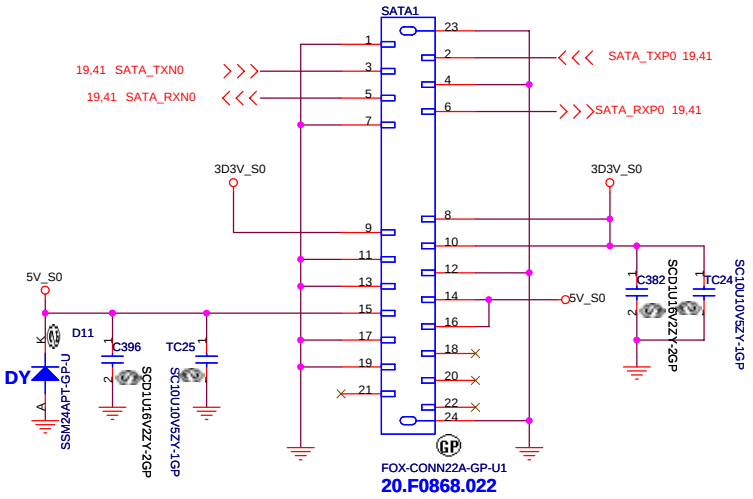
Title: ICH9-M (4 of 4)

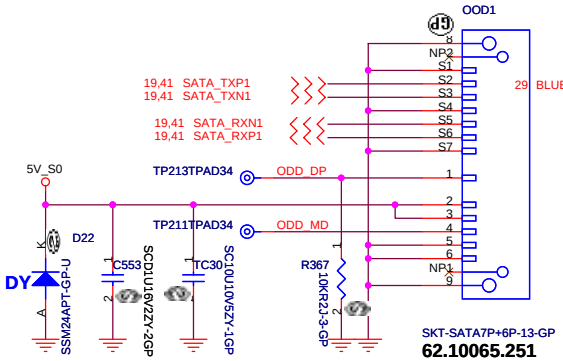
Size | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 23 of 41

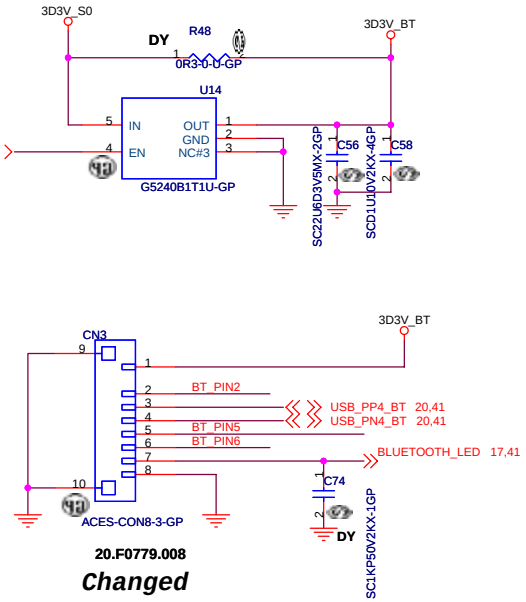
SATA HD Connector



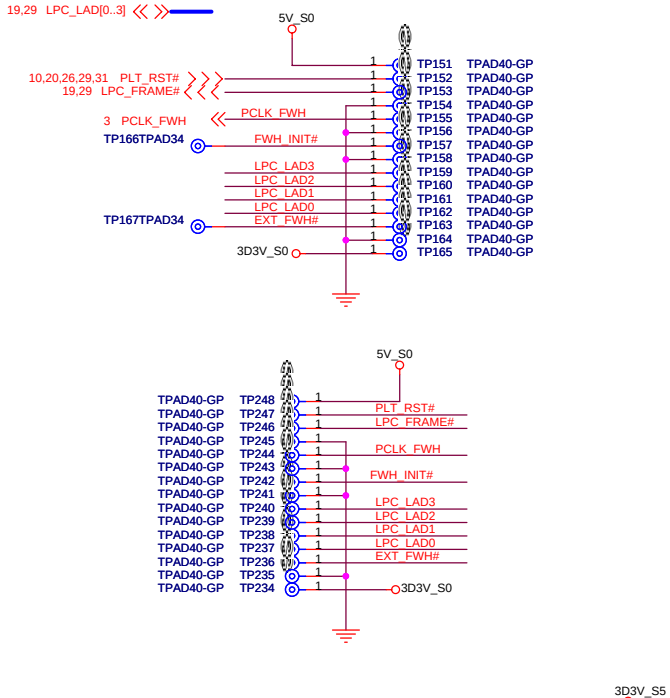
ODD Connector



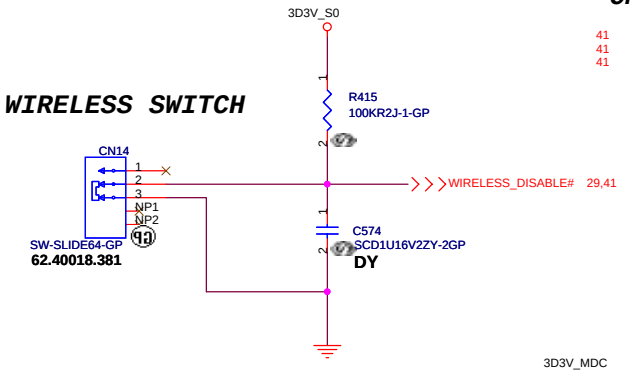
BT CONNECTOR



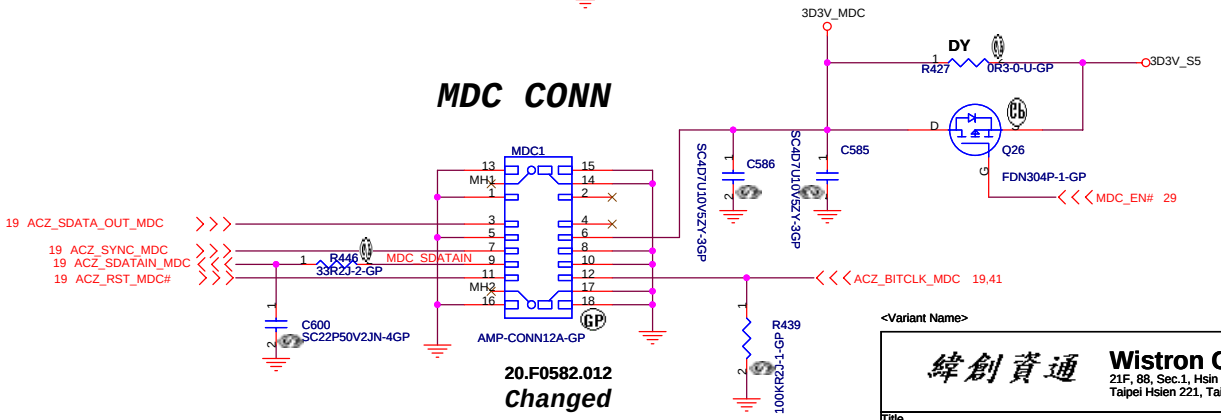
GOLDEN FINGER FOR DEBUG BOARD



WIRELESS SWITCH



MDC CONN



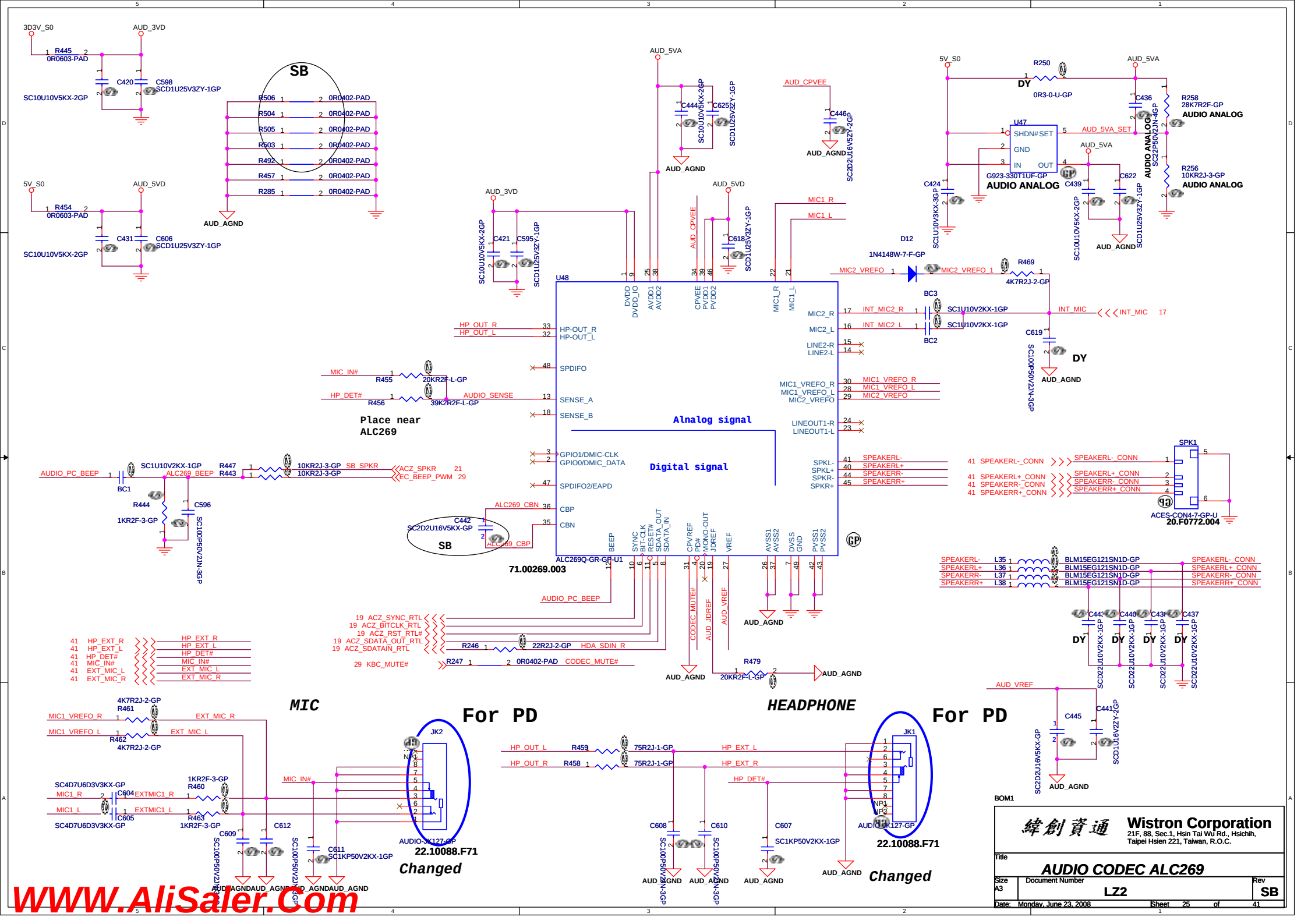
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/CDROM/DEBUG /MODEM/WIRELESS SW/BT

Size	Document Number	Rev
	LZ2	SB

Date: Monday, June 23, 2008 Sheet 24 of 41


3D3V_S0
AUD_3VD
R445
0R0603-PAD
C420
SC10U10V5KX-2GP
C598
SCD1U25V3ZY-1GP
SB
R506
R504
R505
R503
R492
R457
R285
0R0402-PAD
AUD_AGND
5V_S0
AUD_5VD
R454
C431
C606
AUD_5VA
C444
C625
C446
SC2D2U16V5ZY-2GP
AUD_CPVEE
AUD_3VD
C421
C595
C618
MIC1_R
MIC1_L
D12
1N4148W-7-F-GP
MIC2_VREFO
MIC2_VREFO_1
R469
4K7R2J-2-GP
U48
DVDD
DVDD_IO
AVDD1
AVDD2
CPVEE
PVDD1
PVDD2
HP_OUT_R
HP_OUT_L
MIC2_R
MIC2_L
LINE2-R
LINE2-L
SPDIFO
SENSE_A
SENSE_B
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
LINEOUT1-R
LINEOUT1-L
GPIO1/DMIC-CLK
GPIO0/DMIC_DATA
SPDIFO2/EAPD
CBP
CBN
SPKL-
SPKL+
SPKR-
SPKR+
BEEP
SYNC
BIT-CLK
RESET#
SDATA_OUT
SDATA_IN
CPVREF
PD#
MONO-OUT
JDREF
VREF
AVSS1
AVSS2
DVSS
GND
PVSS1
PVSS2
ALC269Q-GR-GP-U1
71.00269.003
Alnalog signal
Digital signal
MIC_IN#
R455
20KR2F-L-GP
HP_DET#
R456
39K2R2F-L-GP
AUDIO_SENSE
Place near
ALC269
INT_MIC2_R
INT_MIC2_L
BC3
BC2
SC1U10V2KX-1GP
INT_MIC
C619
DY
SC100P50V2JN-3GP
5V_S0
R250
0R3-0-U-GP
U47
SHDN#
SET
GND
IN
OUT
G923-330T1UF-GP
AUDIO ANALOG
AUD_5VA_SET
C436
C424
C439
C622
R258
28K7R2F-GP
R256
10KR2J-3-GP
SC22P50V2JN-4GP
SC1U10V3KX-3GP
SC10U10V5KX-2GP
SCD1U25V3ZY-1GP
AUDIO_PC_BEEP
ALC269_BEEP
R447
R443
10KR2J-3-GP
SB_SPKR
ACZ_SPKR
EC_BEEP_PWM
BC1
R444
1KR2F-3-GP
C596
ALC269_CBN
C442
SC2D2U16V5KX-GP
ALC269_CBP
SPK1
ACES-CON4-7-GP-U
20.F0772.004
SPEAKERL-
SPEAKERL+
SPEAKERR-
SPEAKERR+
SPEAKERL-_CONN
SPEAKERL+_CONN
SPEAKERR-_CONN
SPEAKERR+_CONN
L35
L36
L37
L38
BLM15EG121SN1D-GP
C441
C440
C438
C437
DY
SCD22U10V2KX-1GP
AUD_VREF
C445
C443
SC2D2U16V5KX-GP
SCD1U16V2ZY-2GP
19 ACZ_SYNC_RTL
19 ACZ_BITCLK_RTL
19 ACZ_RST_RTL#
19 ACZ_SDATA_OUT_RTL
19 ACZ_SDATAIN_RTL
R246
22R2J-2-GP
HDA_SDIN_R
29 KBC_MUTE#
R247
0R0402-PAD
CODEC_MUTE#
CODEC_MUTE#
AUD_JDREF
AUD_VREF
R479
20KR2F-L-GP
41 HP_EXT_R
41 HP_EXT_L
41 HP_DET#
41 MIC_IN#
41 EXT_MIC_L
41 EXT_MIC_R
MIC
For PD
HEADPHONE
For PD
4K7R2J-2-GP
R461
R462
MIC1_VREFO_R
MIC1_VREFO_L
EXT_MIC_R
EXT_MIC_L
SC4D7U6D3V3KX-GP
C604
C605
EXTMIC1_R
EXTMIC1_L
1KR2F-3-GP
R460
R463
C609
C612
C611
SC1KP50V2KX-1GP
JK2
AUDIO-JK127-GP
22.10088.F71
Changed
HP_OUT_L
HP_OUT_R
R459
R458
75R2J-1-GP
HP_EXT_L
HP_EXT_R
HP_DET#
C608
C610
C607
JK1
AUDIO-JK127-GP
22.10088.F71
Changed
AUD_AGNDAUD_AGNDAUD_AGNDAUD_AGND
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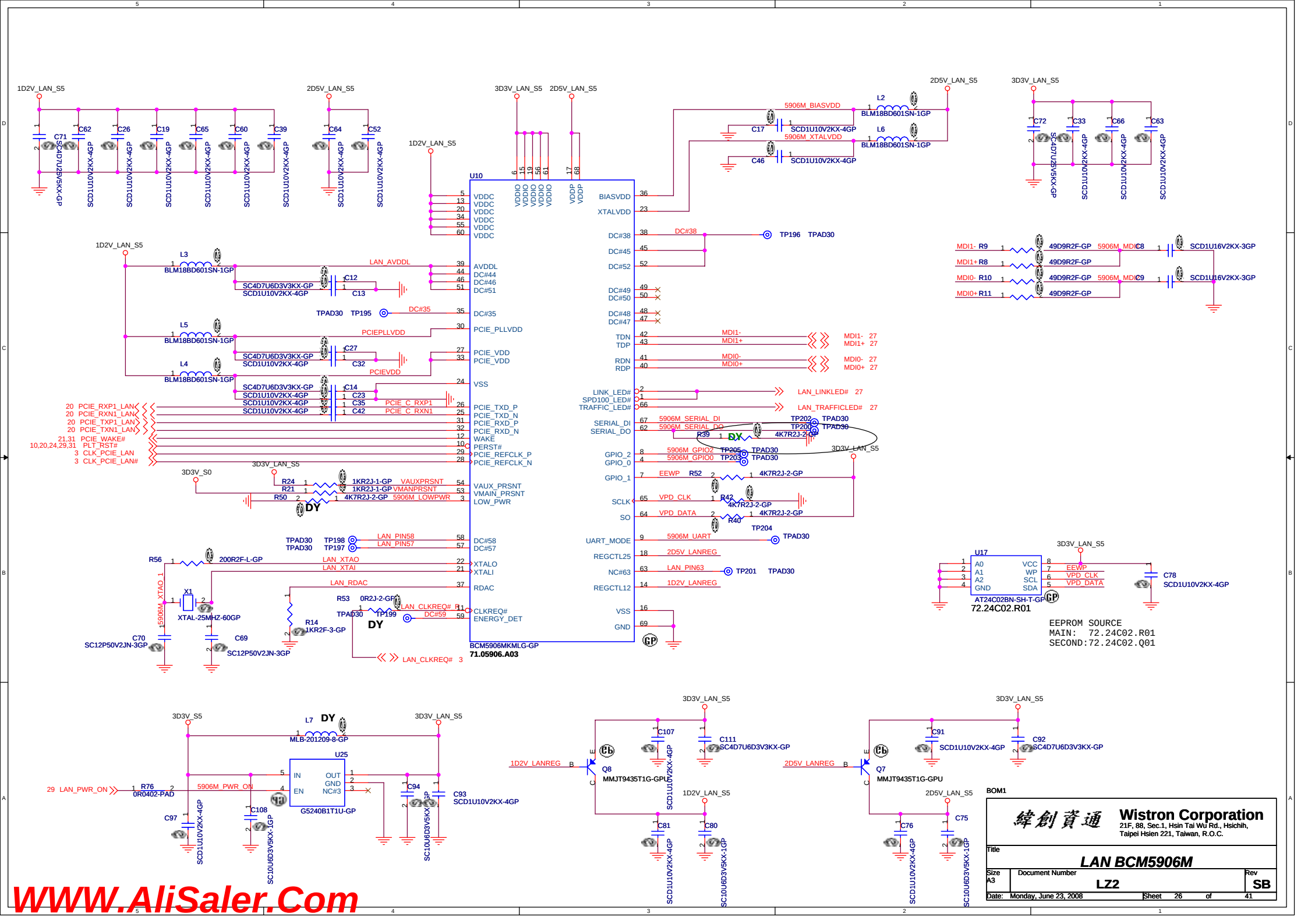
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC ALC269
Size
A3
Document Number
LZ2
Rev
SB
Date: Monday, June 23, 2008
Sheet 25 of 41


1D2V_LAN_S5
2D5V_LAN_S5
3D3V_LAN_S5
U10
BCM5906MKMLG-GP
71.05906.A03
5906M_BIASVDD
5906M_XTALVDD
LAN_AVDDL
PCIEPLLVDD
PCIEVDD
PCIE_RXP1_LAN
PCIE_RXN1_LAN
PCIE_TXP1_LAN
PCIE_TXN1_LAN
PCIE_WAKE#
PLT_RST#
CLK_PCIE_LAN
CLK_PCIE_LAN#
PCIE_C_RXP1
PCIE_C_RXN1
VAUXPRSNT
VMANPRSNT
5906M_LOWPWR
LAN_PIN58
LAN_PIN57
LAN_XTAO
LAN_XTAI
LAN_RDAC
LAN_CLKREQ#
MDI1-
MDI1+
MDI0-
MDI0+
LAN_LINKLED#
LAN_TRAFFICLED#
5906M_SERIAL_DI
5906M_SERIAL_DO
5906M_GPIO2
5906M_GPIO0
EEWP
VPD_CLK
VPD_DATA
5906M_UART
2D5V_LANREG
LAN_PIN63
1D2V_LANREG
XTAL-25MHZ-60GP
MLB-201209-8-GP
G5240B1T1U-GP
LAN_PWR_ON
5906M_PWR_ON
MMJT9435T1G-GPU
AT24C02BN-SH-T-GP
72.24C02.R01
EEPROM SOURCE
MAIN: 72.24C02.R01
SECOND:72.24C02.Q01
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN BCM5906M
LZ2
SB
Monday, June 23, 2008
Sheet 26 of 41
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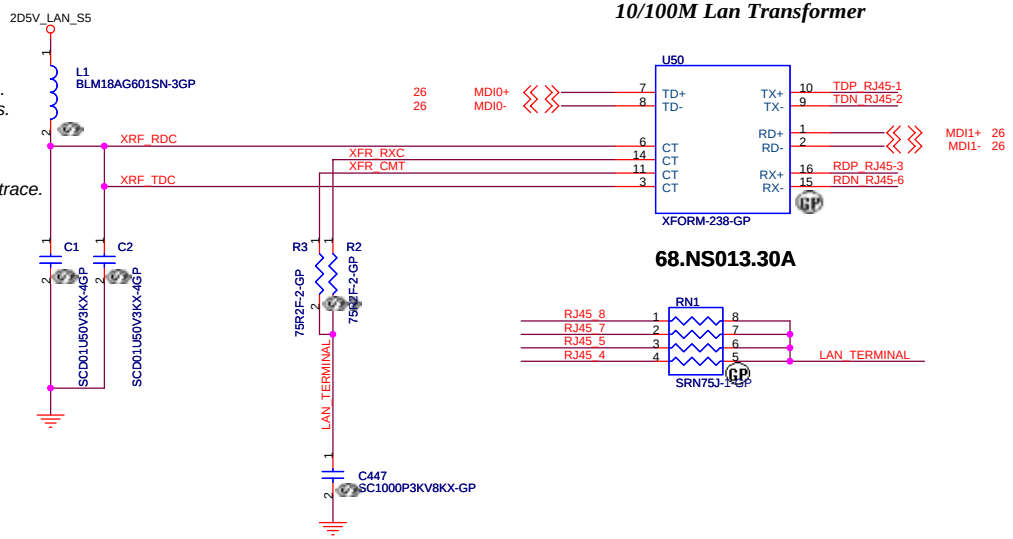
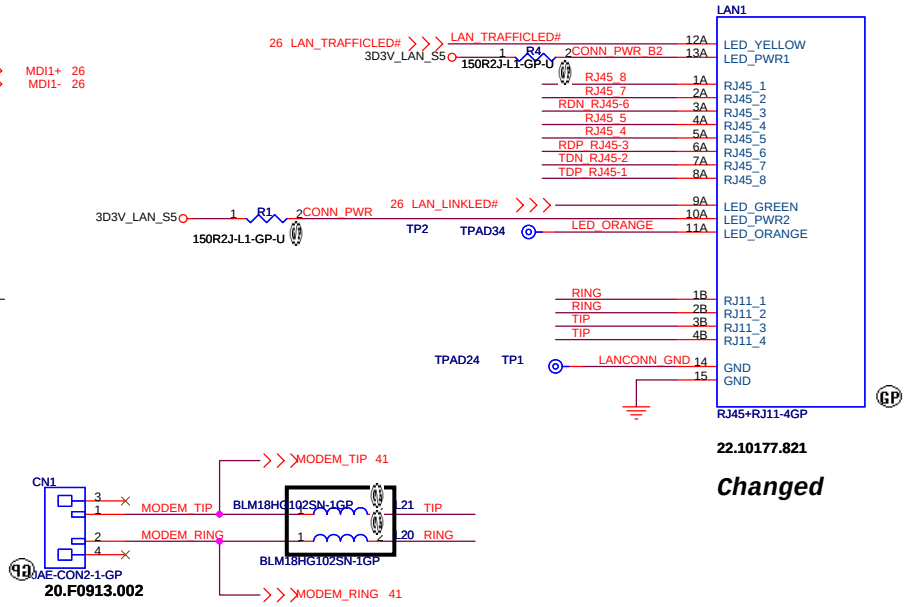
10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



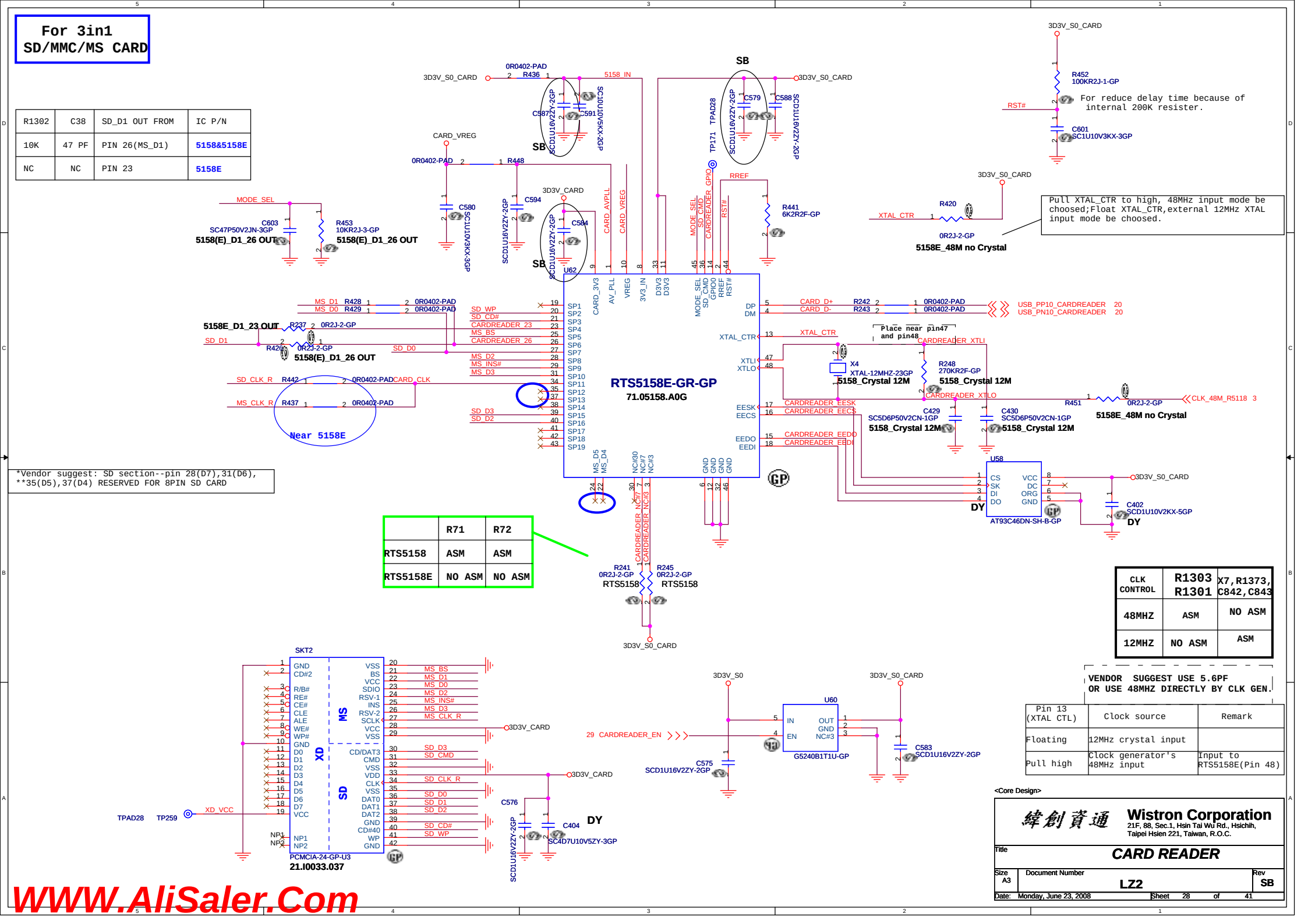


<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN connector/NEW CARD/SIM		
Size: A3	Document Number: LZ2	Rev: SB
Date: Monday, June 23, 2008	Sheet 27 of 41	

For 3in1 SD/MMC/MS CARD

R1302	C38	SD_D1 OUT FROM	IC P/N
10K	47 PF	PIN 26(MS_D1)	5158&5158E
NC	NC	PIN 23	5158E



	R71	R72
RTS5158	ASM	ASM
RTS5158E	NO ASM	NO ASM

CLK CONTROL	R1303 R1301	X7,R1373, C842,C843
48MHZ	ASM	NO ASM
12MHZ	NO ASM	ASM

Pin 13 (XTAL CTL)	Clock source	Remark
Floating	12MHz crystal input	
Pull high	Clock generator's 48MHz input	Input to RTS5158E(Pin 48)

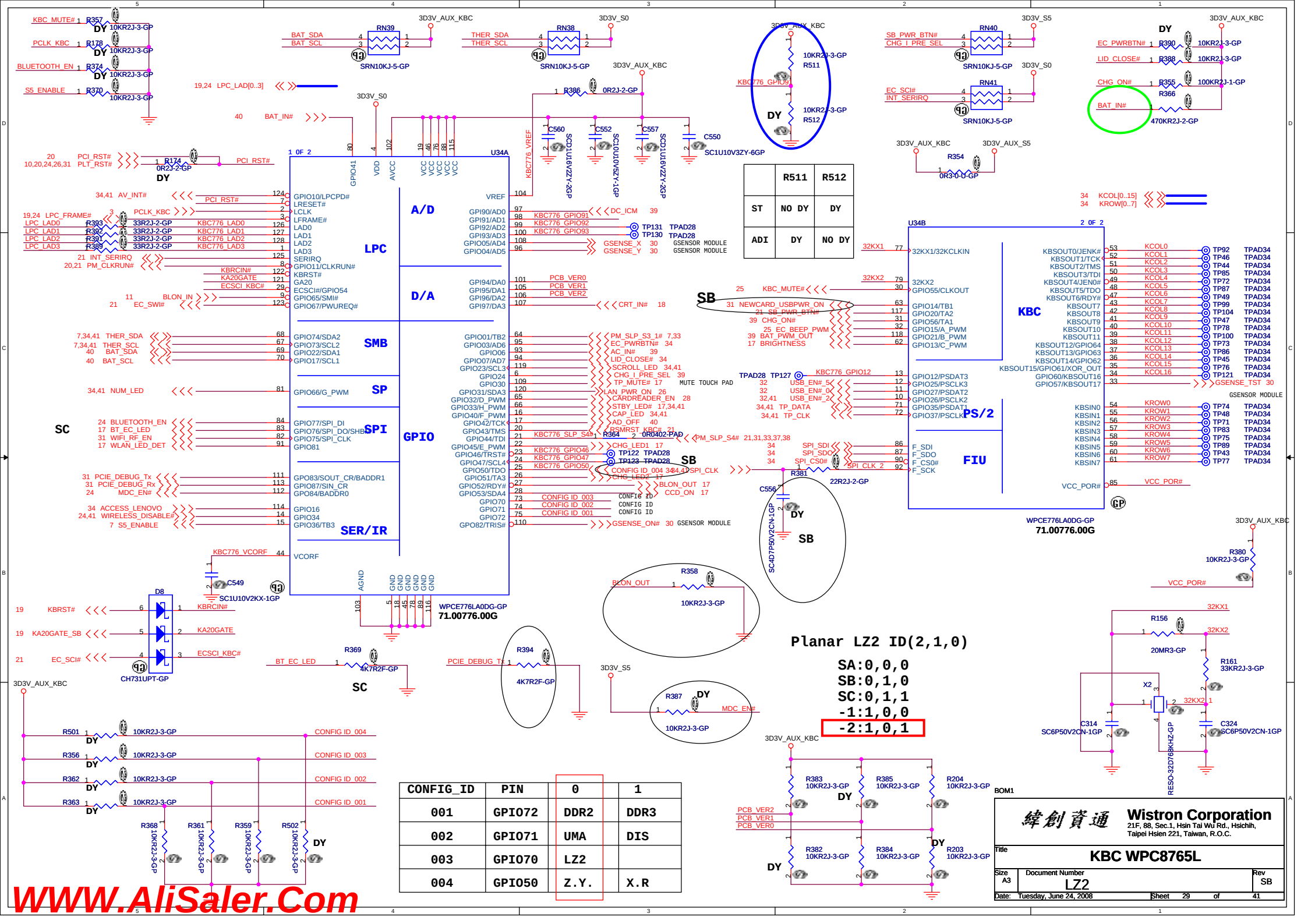
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER

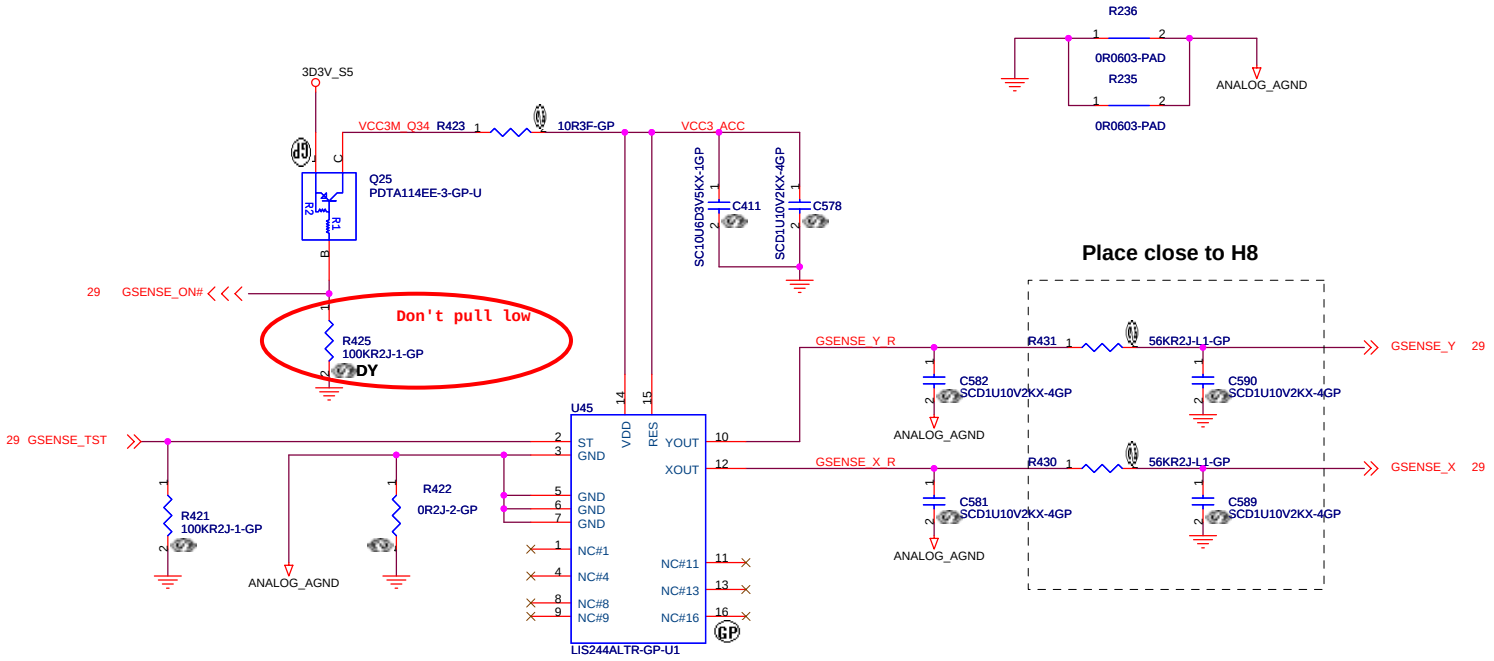
Size: A3 | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 28 of 41



	R511	R512
ST	NO DY	DY
ADI	DY	NO DY

CONFIG_ID	PIN	0	1
001	GPIO72	DDR2	DDR3
002	GPIO71	UMA	DIS
003	GPIO70	LZ2	
004	GPIO50	Z.Y.	X.R



Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

BOM1

緯創資通 **Wistron Corporation**
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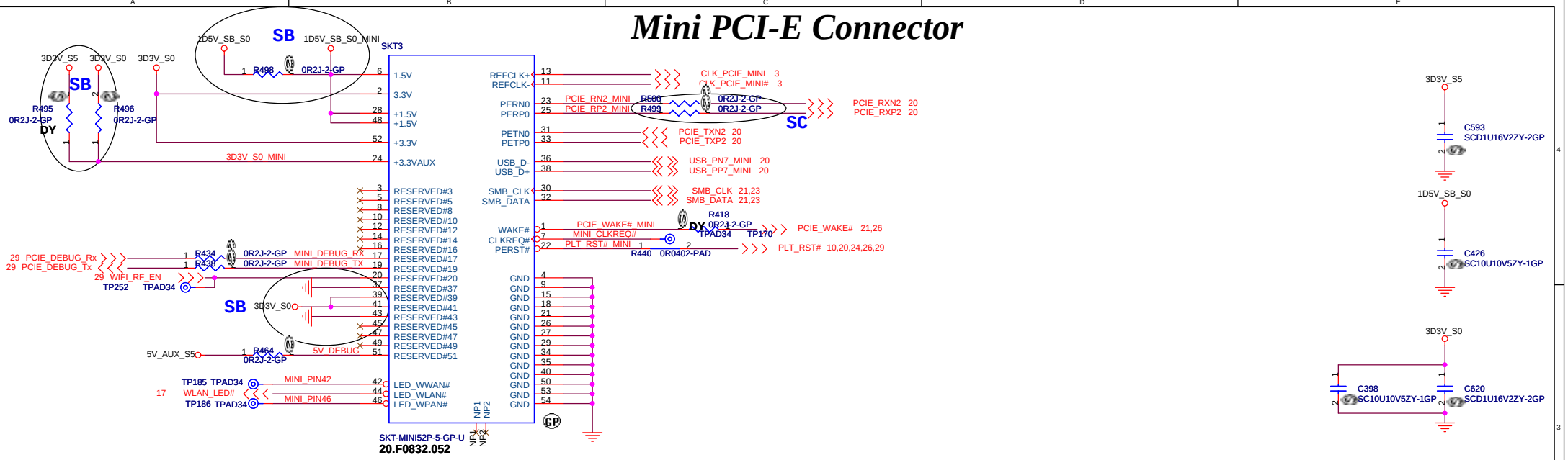
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GSENSOR**

Size	Document Number	Rev
	LZ2	SB

Date: Monday, June 23, 2008 Sheet 30 of 41

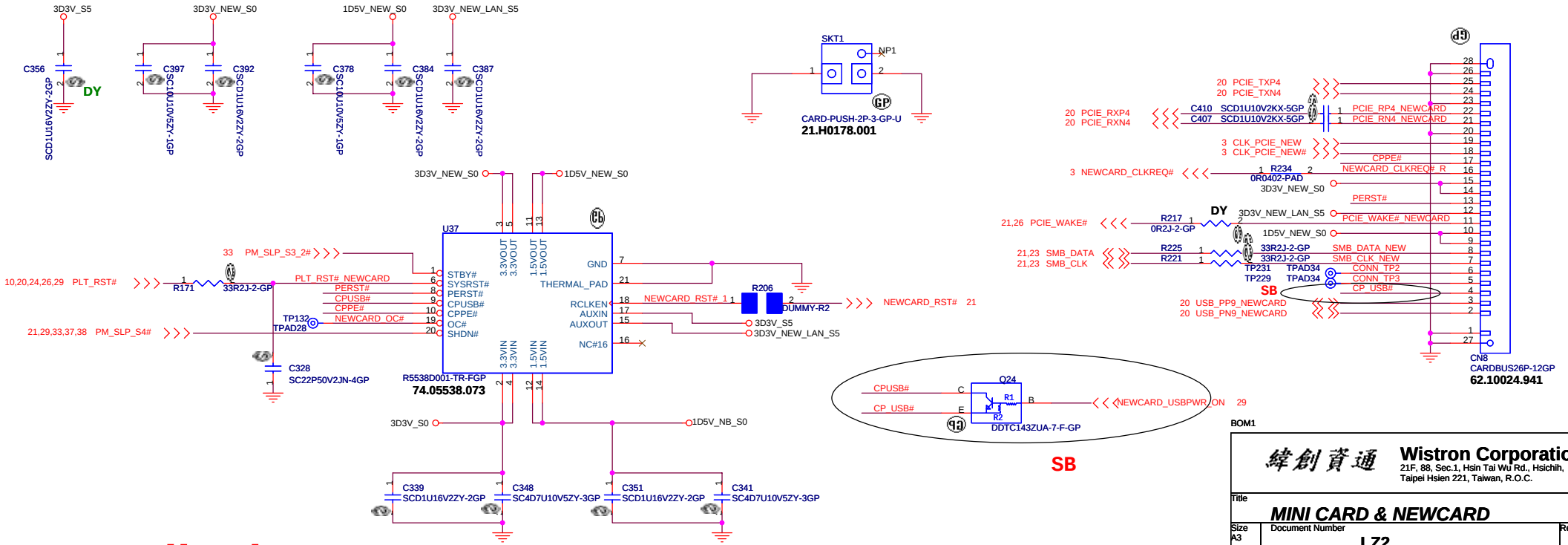
Mini PCI-E Connector



Place them Near to Chip

Place them Near to Connector

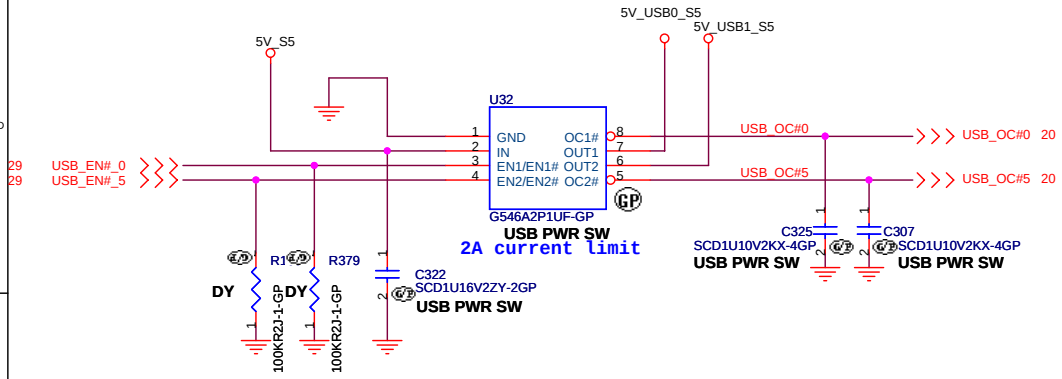
.N.E.W.C.A.R.D. C.O.N.N.

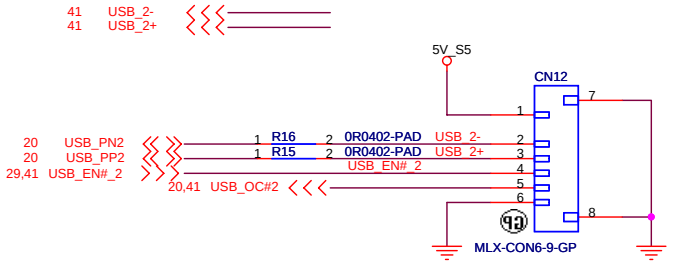


BOM1

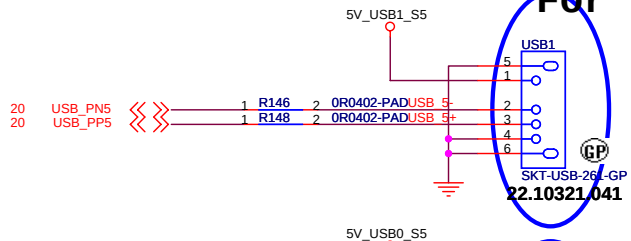
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD & NEWCARD	
Size A3	Document Number LZ2	Rev SB
Date: Monday, June 23, 2008	Sheet 31 of 41	

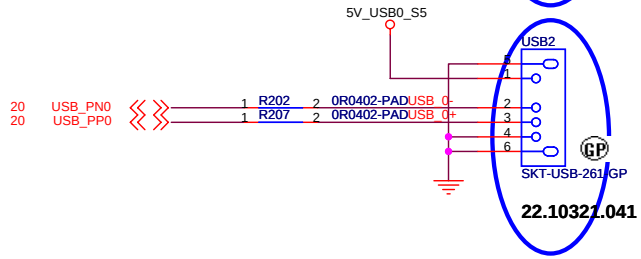
USB * 3 PORT



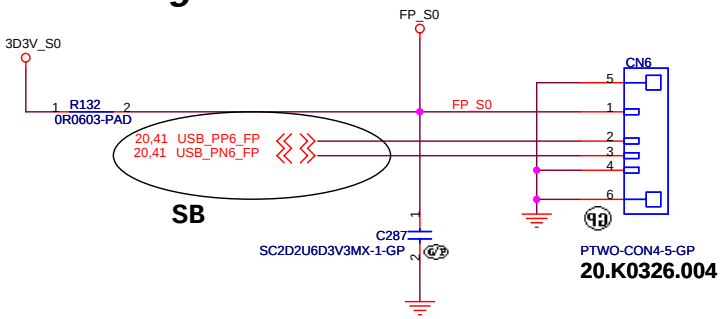


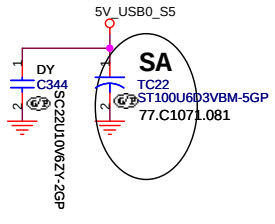
For PD

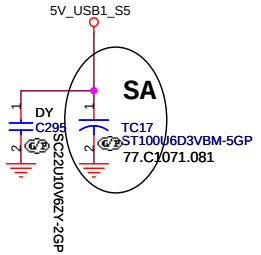


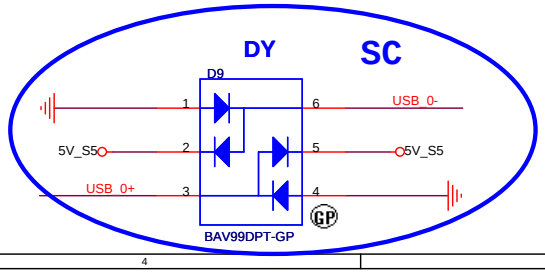


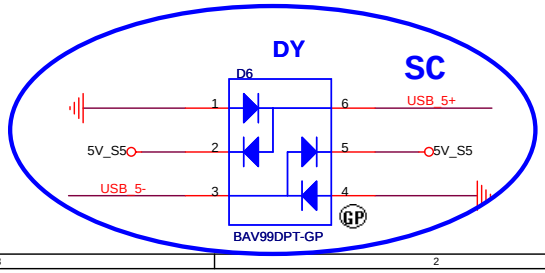
Finger Print











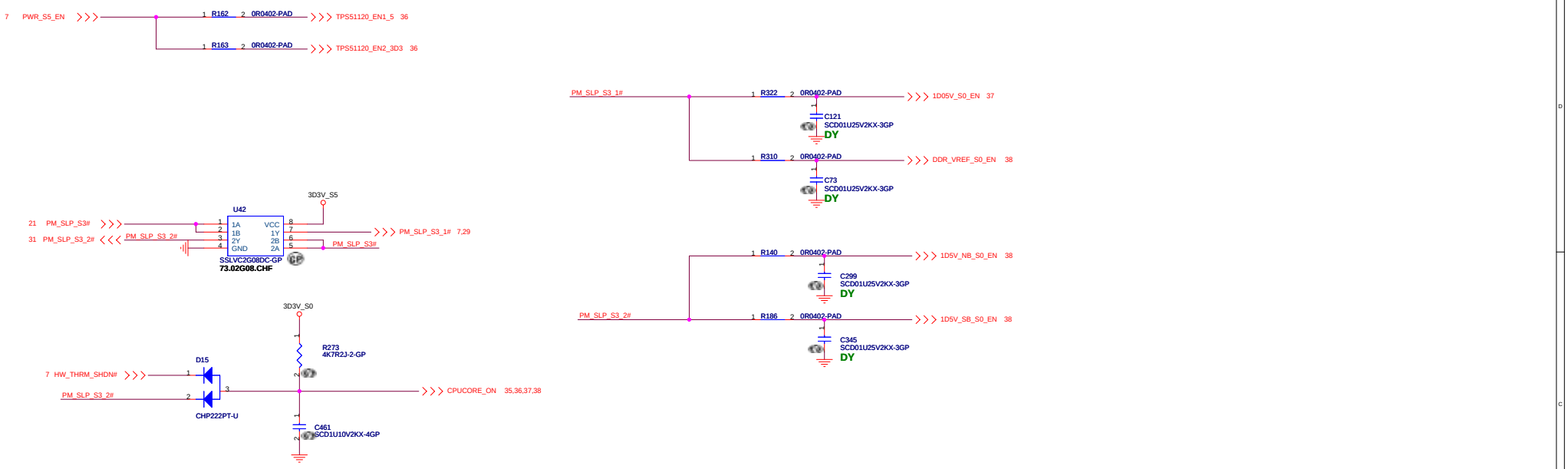
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

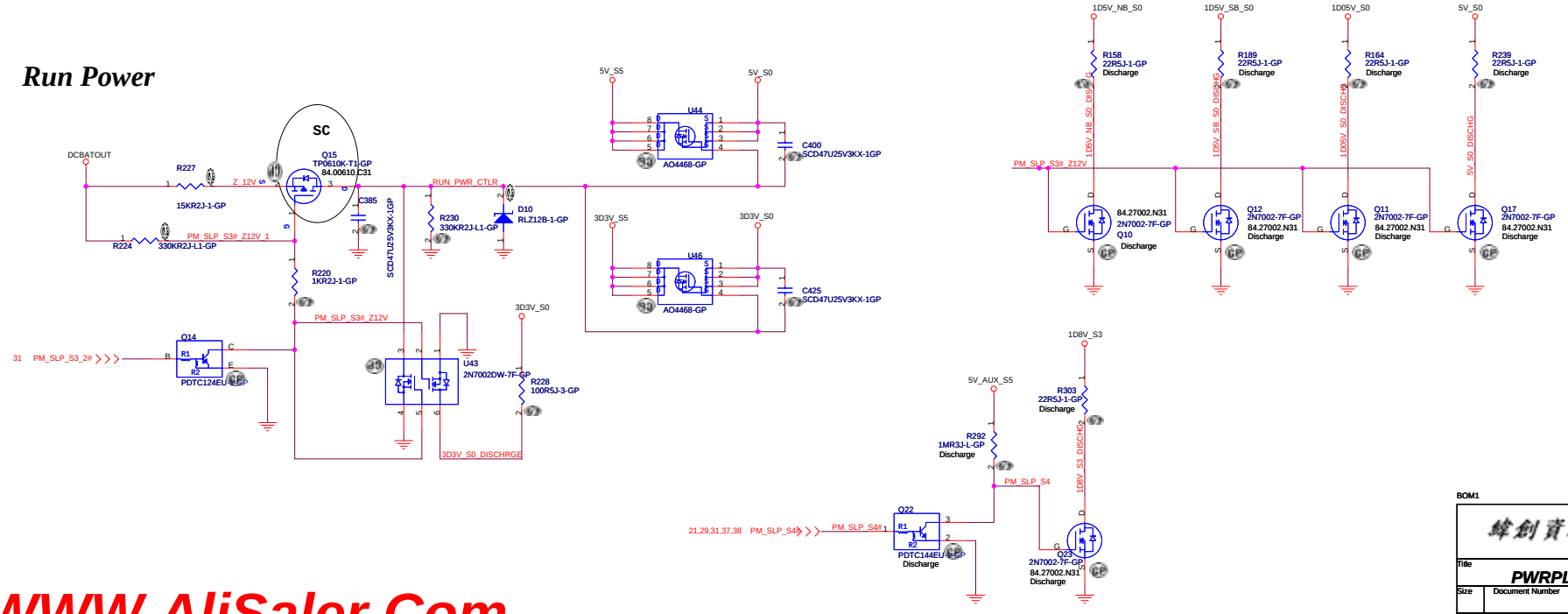
Title: **USB CONN/FINGER PRINT**

Size	Document Number	Rev
B	LZ2	SB

Date: Monday, June 23, 2008 Sheet 32 of 41



Run Power



BOM1

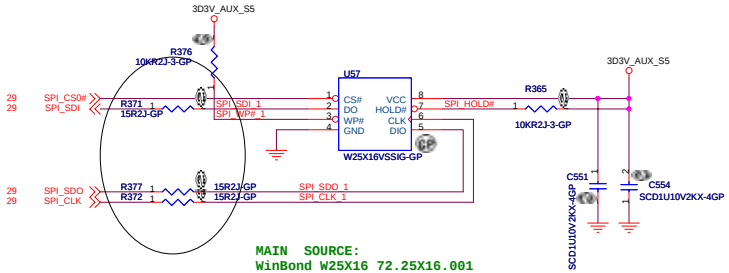
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWRPLANE&RESET LOGIC

Size	Document Number	Rev
	LZ2	SB

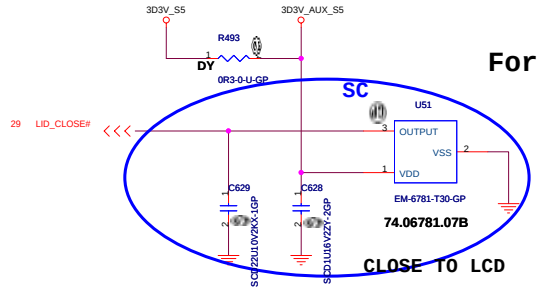
Date: Monday, June 23, 2008 Sheet 33 of 41

SPI Flash



MAIN SOURCE:
WinBond W25X16 72.25X16.001
SECOND SOURCE:
MXIC MX25L1605 72.25165.001

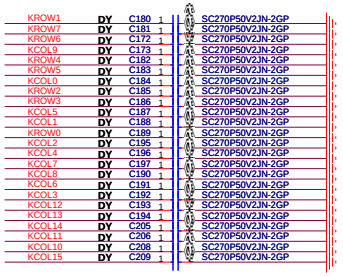
Lid Switch

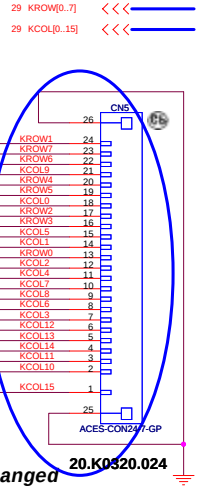


For PD

CLOSE TO LCD

Keyboard Connector

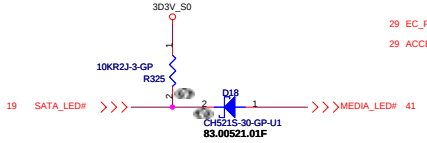


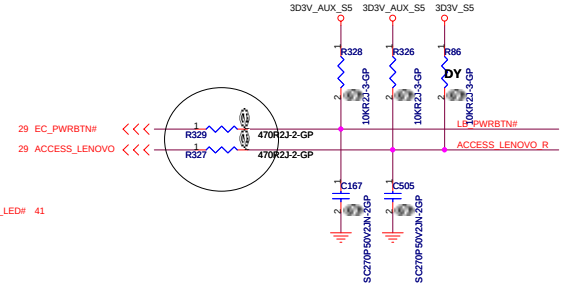


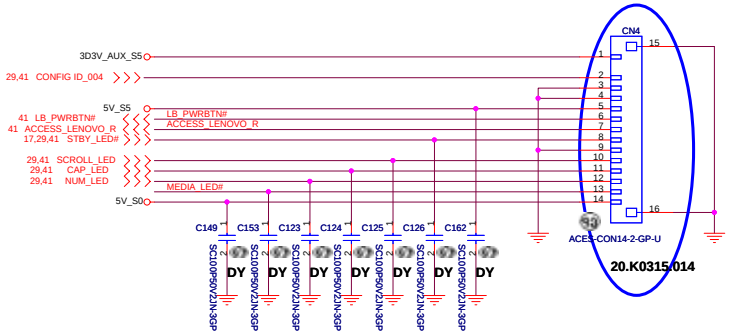
Changed

20.K0320.024

Launch Board

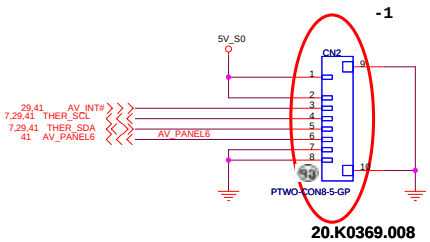






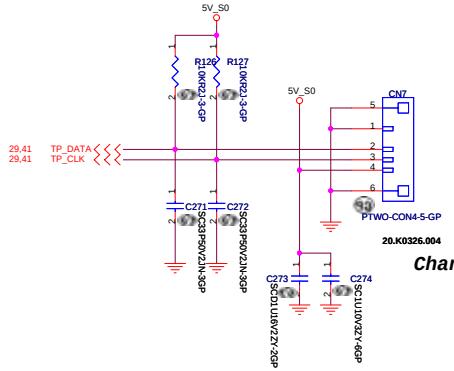
20.K0315.014

AV Panel



20.K0369.008

TouchPad Connector



20.K0326.004

Changed

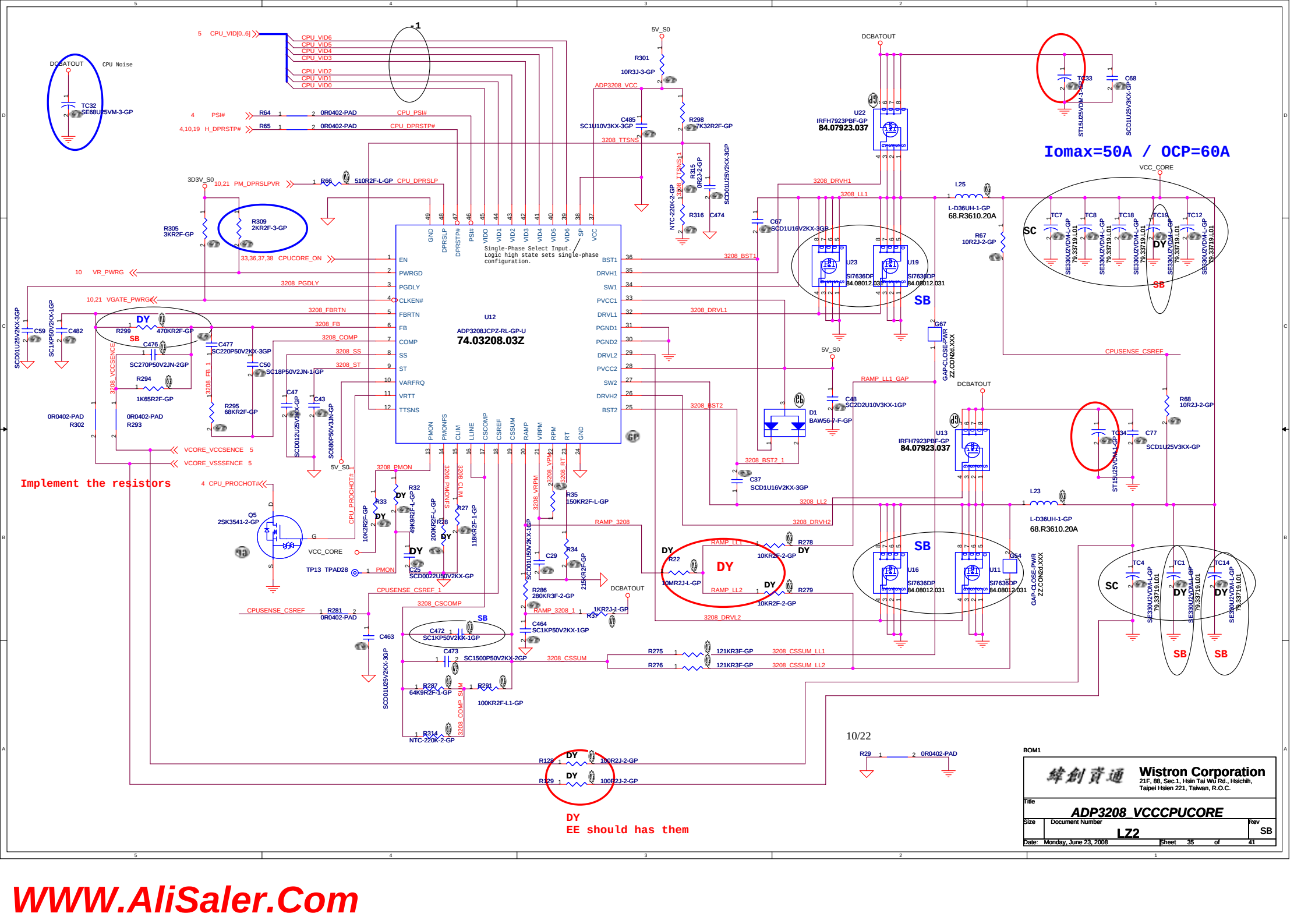
BOM1

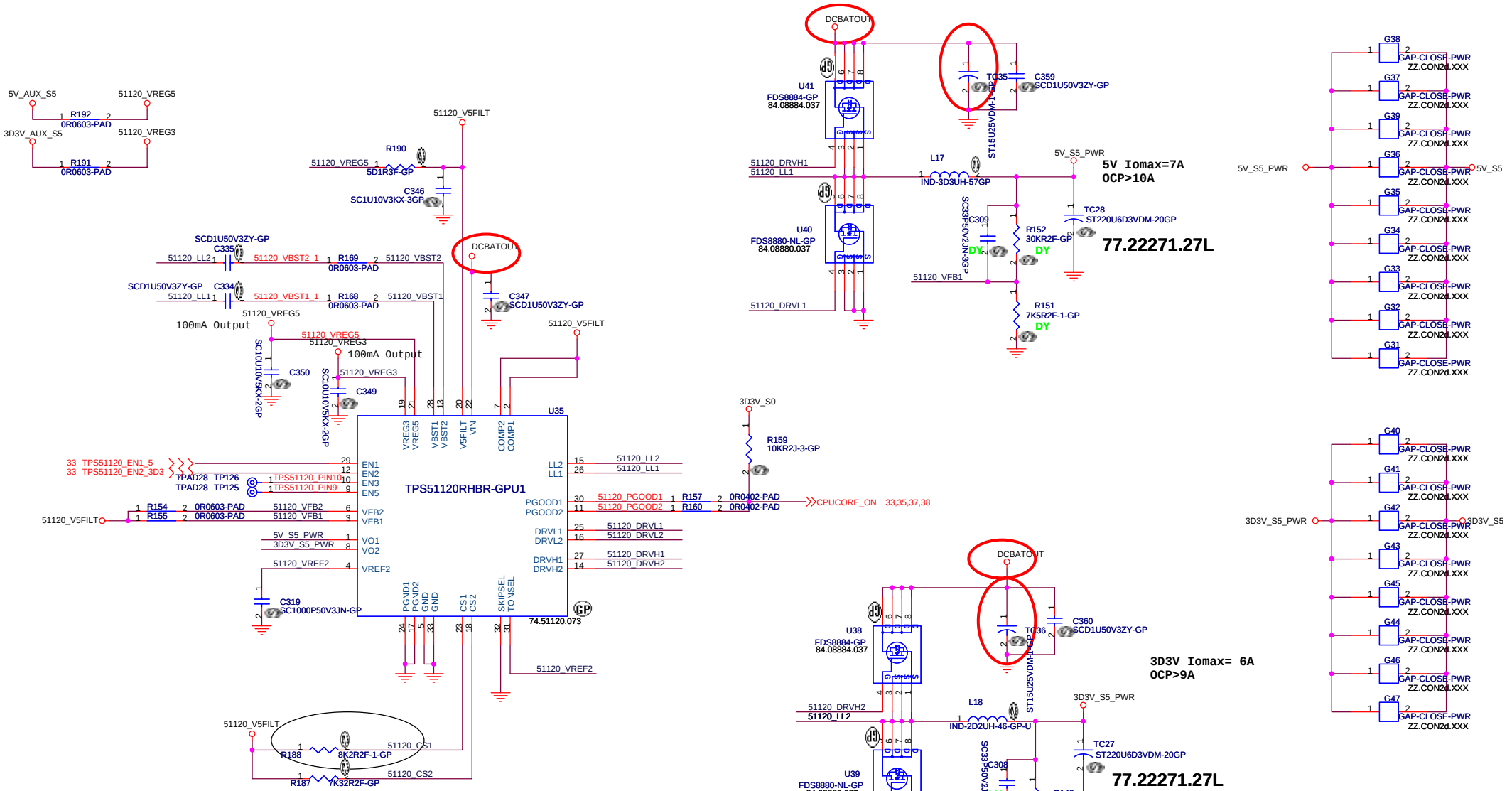
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TP/SPI/AV/Charger

Size	Document Number	Rev
	LZ2	SB

Date: Monday, June 23, 2008 Sheet 34 of 41





	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
	N/A	N/A	CURRENT MODE	D-Cap MODE
	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
	N/A	not use	ADJ.	5V Fixed Output
	N/A	not use	ADJ.	3.3V Fixed Output
	Switcher OFF	not use	Swithchr ON	Switcher ON
	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

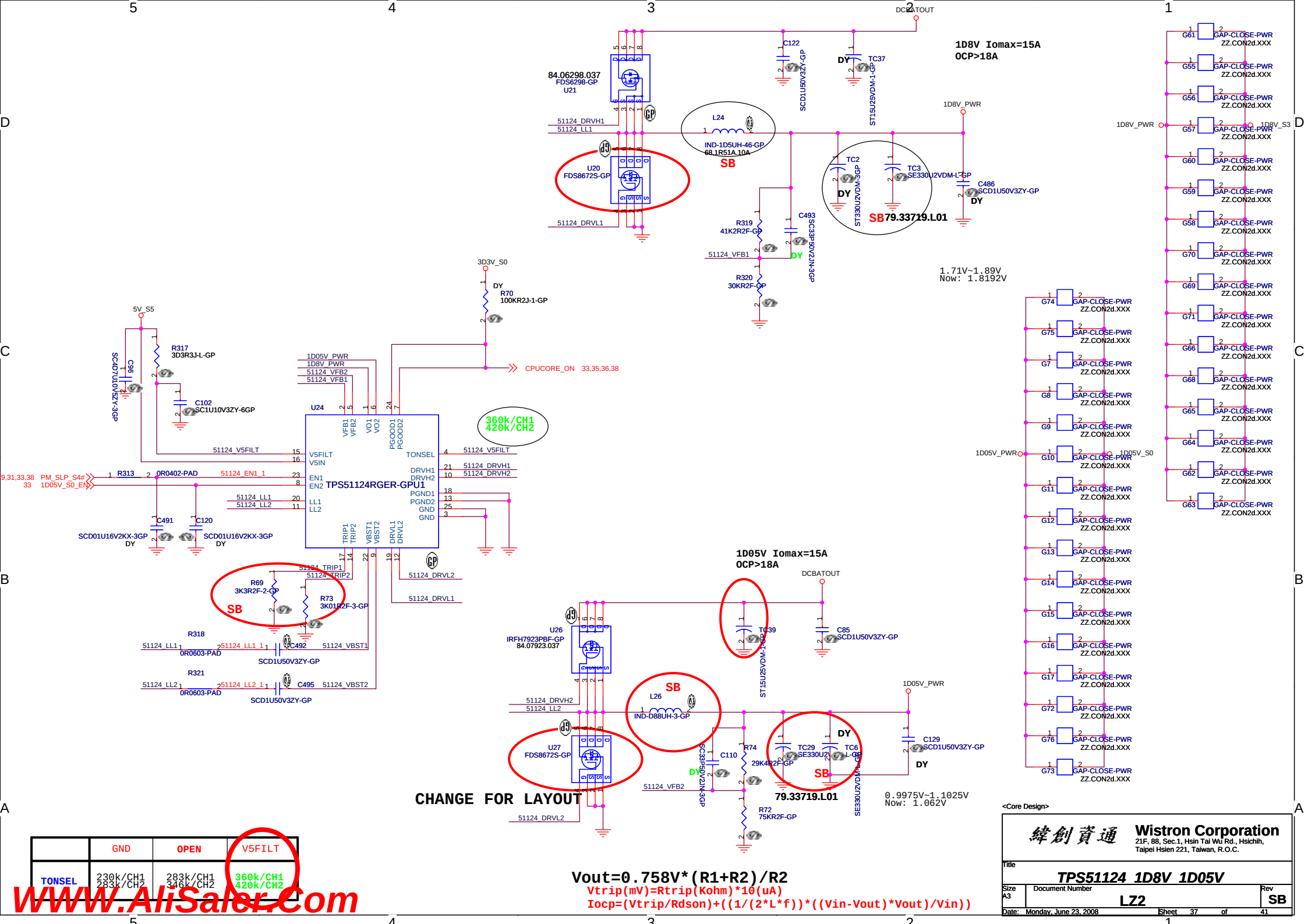
<Core Design>

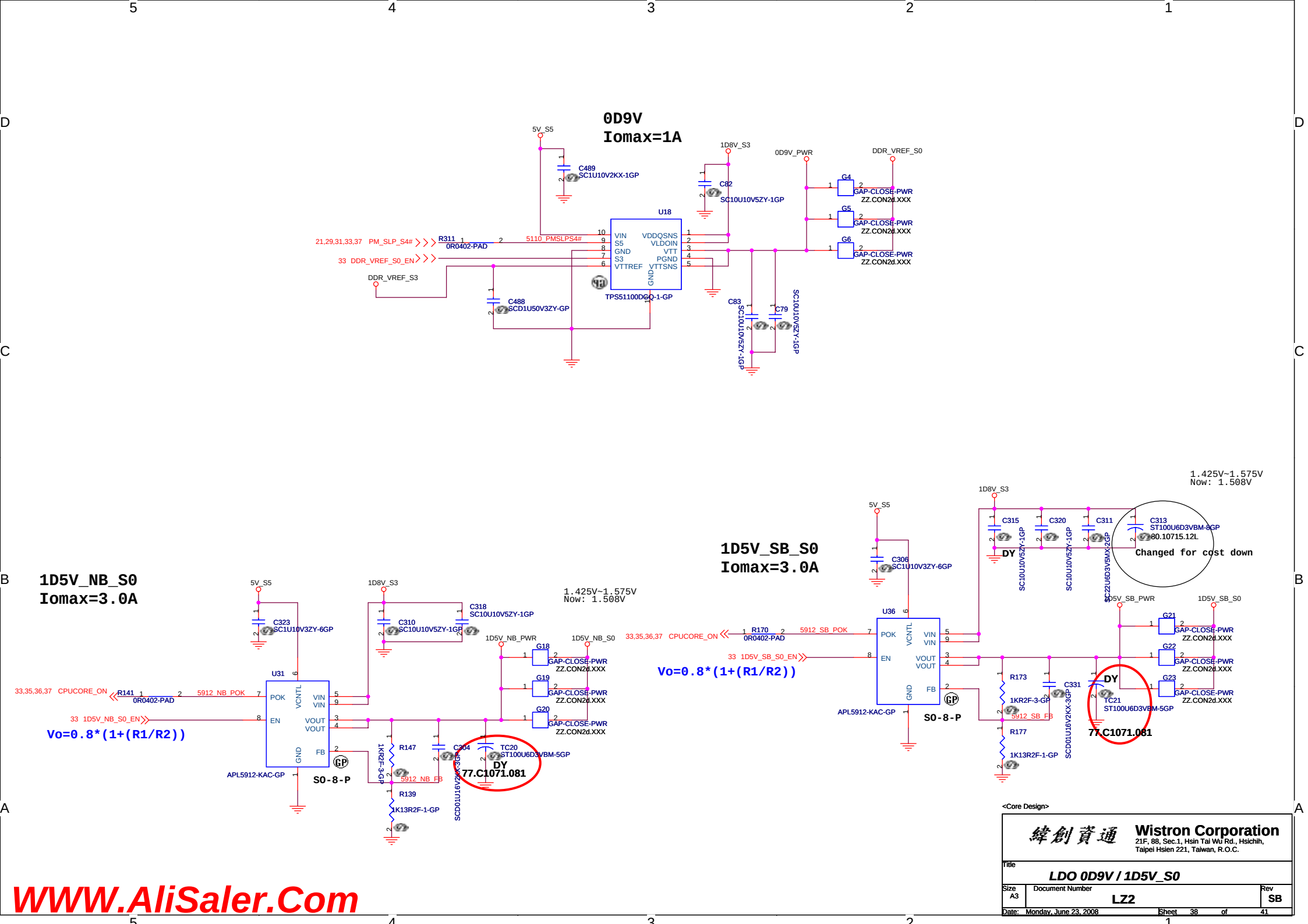
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V / 3D3V

Size	Document Number	Rev
A3	LZ2	SB

Date: Monday, June 23, 2008 Sheet 36 of 41


1D8V Iomax=15A
OCP>18A
84.06298.037
FDS6298-GP
U21
DCBATOUT
C122
SCD1U50V3ZY-GP
DY
TC37
ST15U25VDM-1-GP
1D8V_PWR
51124_DRVH1
51124_LL1
L24
IND-1D5UH-46-GP
68.1R51A.10A
SB
U20
FDS8672S-GP
51124_DRVL1
TC2
ST330U2VDM-3GP
TC3
SE330U2VDM-L-GP
C486
SCD1U50V3ZY-GP
SB79.33719.L01
R319
41K2R2F-GP
C493
SC33P50V2JN-3GP
51124_VFB1
R320
30KR2F-GP
1.71V~1.89V
Now: 1.8192V
3D3V_S0
R70
100KR2J-1-GP
CPUCORE_ON 33,35,36,38
5V_S5
R317
3D3R3J-L-GP
C96
SC47U10V5ZY-3GP
C102
SC1U10V3ZY-6GP
1D05V_PWR
1D8V_PWR
51124_VFB2
51124_VFB1
U24
360k/CH1
420k/CH2
51124_V5FILT
V5FILT
V5IN
TONSEL
R313
0R0402-PAD
51124_EN1_1
EN1
EN2
TPS51124RGER-GPU1
51124_DRVH1
51124_DRVH2
51124_LL1
51124_LL2
LL1
LL2
PGND1
PGND2
GND
C491
C120
SCD01U16V2KX-3GP
DY
51124_TRIP1
51124_TRIP2
R69
3K3R2F-2-GP
R73
3K01R2F-3-GP
SB
51124_DRVL2
51124_DRVL1
R318
R321
0R0603-PAD
C492
C495
SCD1U50V3ZY-GP
51124_VBST1
51124_VBST2
1D05V Iomax=15A
OCP>18A
DCBATOUT
U26
IRFH7923PBF-GP
84.07923.037
TC39
ST15U25VDM-1-GP
C85
SCD1U50V3ZY-GP
1D05V_PWR
SB
L26
IND-D88UH-3-GP
51124_DRVH2
51124_LL2
U27
FDS8672S-GP
51124_DRVL2
C110
SC33P50V2JN-3GP
R74
29K4R2F-GP
TC29
SE330U2
TC6
L-GP
C129
SCD1U50V3ZY-GP
51124_VFB2
R72
75KR2F-GP
79.33719.L01
SE330U2VDM-L-GP
0.9975V~1.025V
Now: 1.062V
CHANGE FOR LAYOUT
Vout=0.758V*(R1+R2)/R2
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
GAP-CLOSE-PWR
ZZ.CON2d.XXX
G61
G55
G56
G57
G60
G59
G58
G70
G69
G71
G66
G68
G65
G64
G62
G63
G74
G75
G7
G8
G9
G10
G11
G12
G13
G14
G15
G16
G17
G72
G76
G73
1D8V_S3
1D05V_S0
1D05V_PWR
9,31,33,38 PM_SLP_S4#
33 1D05V_S0_EN
TONSEL
GND
OPEN
V5FILT
230k/CH1
283k/CH2
283k/CH1
346k/CH2
360k/CH1
420k/CH2
WWW.AliSaler.Com
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51124 1D8V 1D05V
Size A3
Document Number
LZ2
Rev
SB
Date: Monday, June 23, 2008
Sheet 37 of 41



<Core Design>

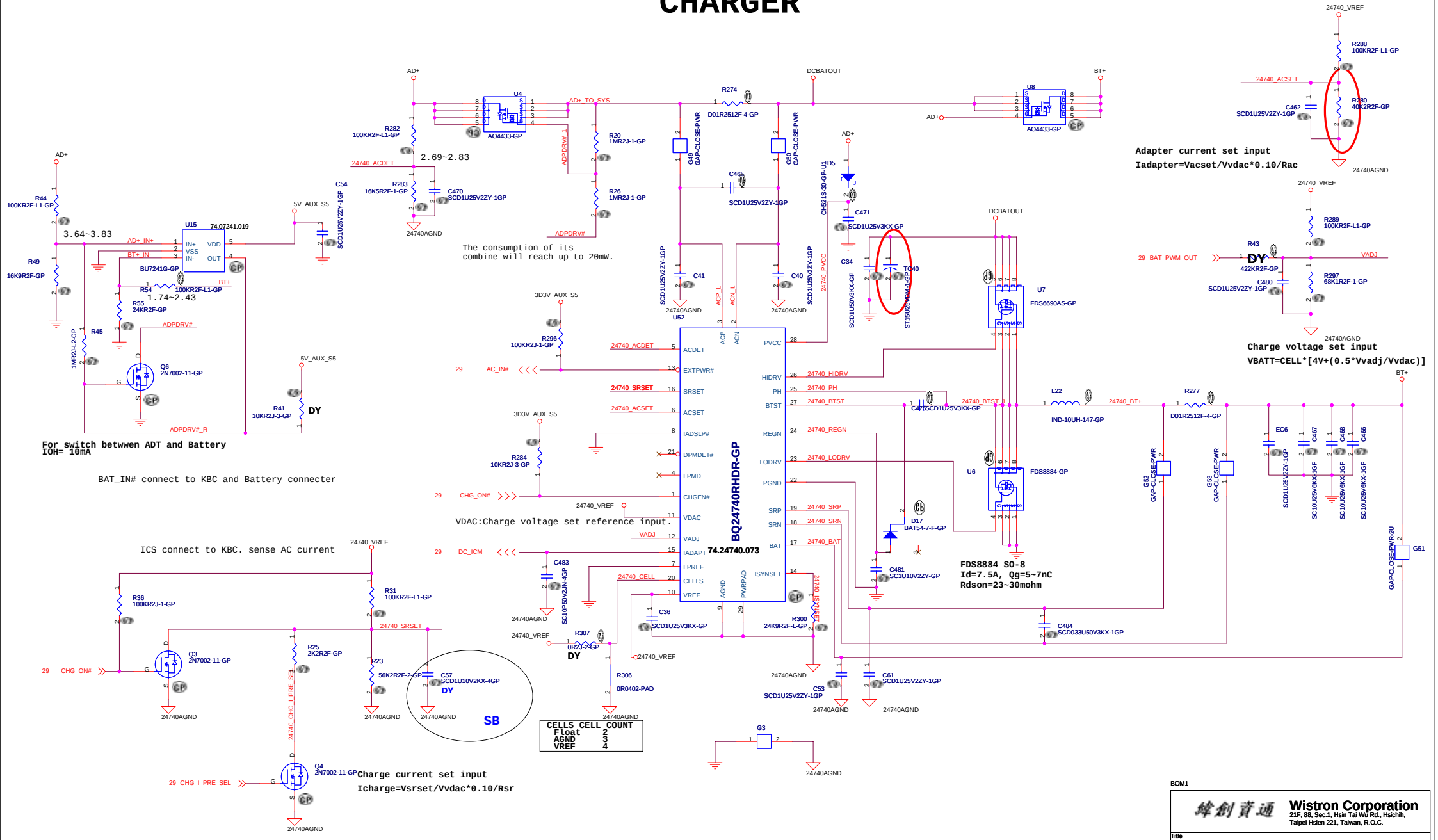
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 0D9V / 1D5V_S0

Size	Document Number	Rev
A3	LZ2	SB

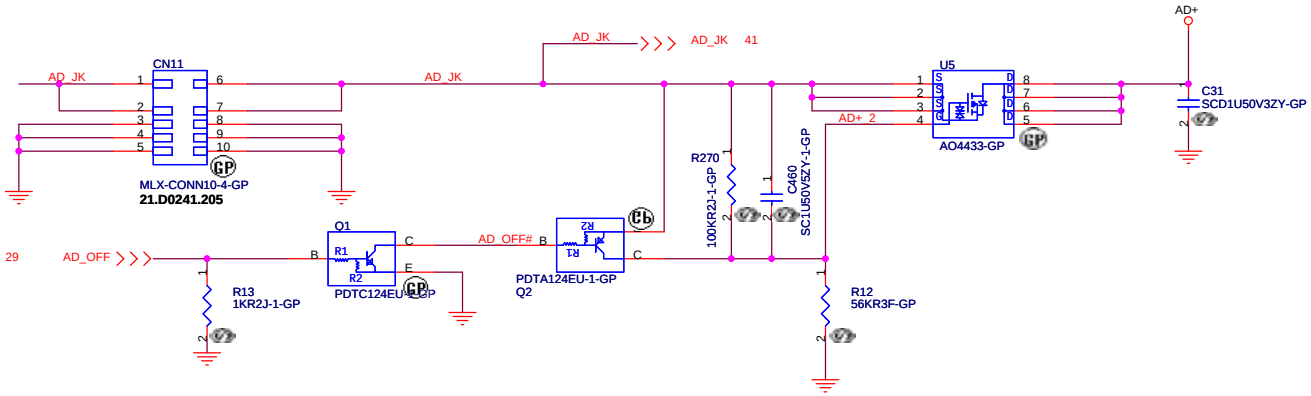
Date: Monday, June 23, 2008 Sheet 38 of 41

CHARGER

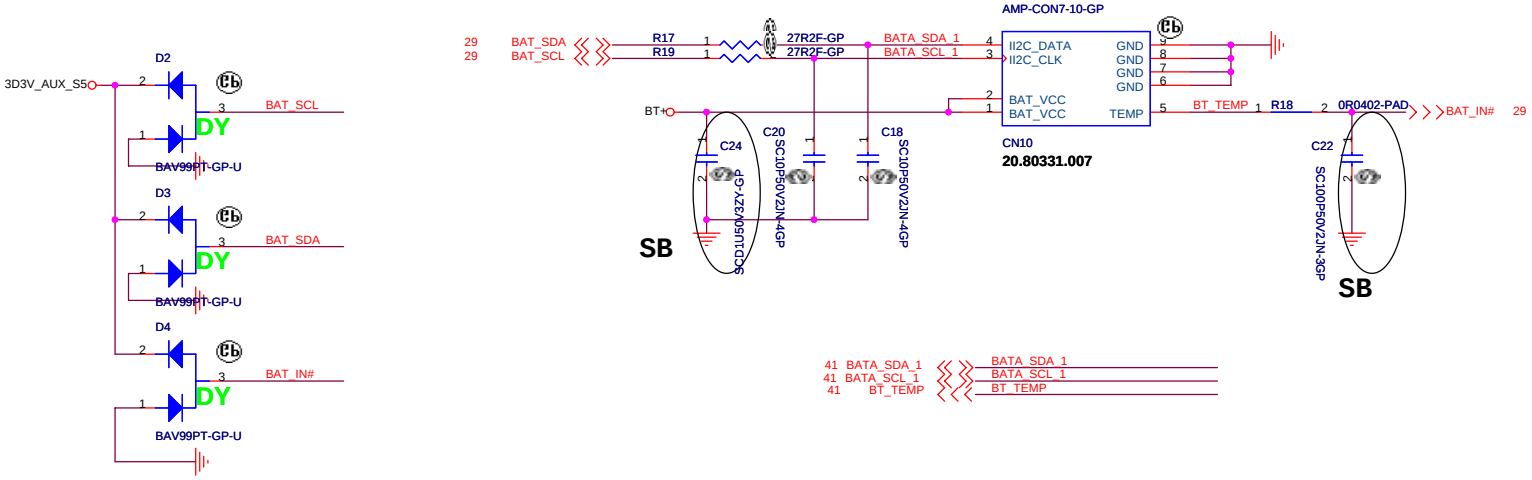


BOM1	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Charger BQ24740
Size	Document Number: LZ2 — Rev: SB
Date: Monday, June 23, 2008	Sheet 39 of 41

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

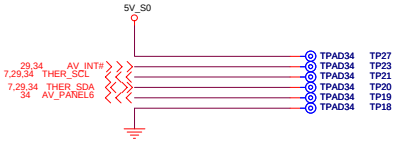
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PTH FOR SCREW HOLES

Size: A3 | Document Number: LZ2 | Rev: SB

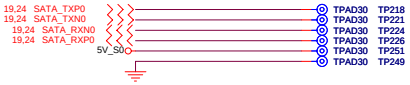
Date: Monday, June 23, 2008 | Sheet 40 of 41

AV Panel

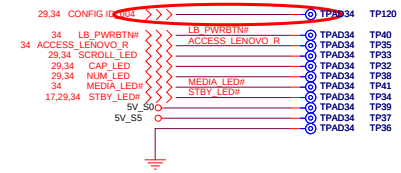


TouchPad Connector

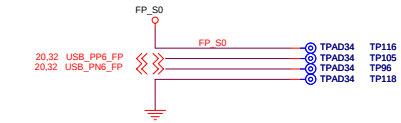
ODD CONN



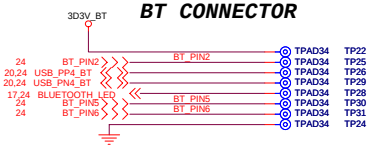
Launch Board



Finger Print CONN



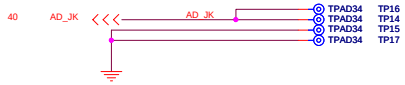
BT CONNECTOR



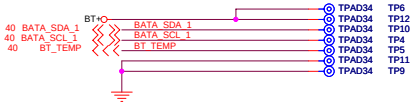
WIRELESS SWITCH

MIC CONN

ADT BOARD CONN

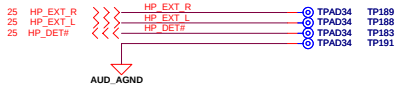


BATTERY CONN



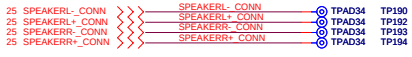
SATA CONN

HEADPHONE CONN

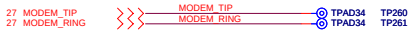


FAN CONN

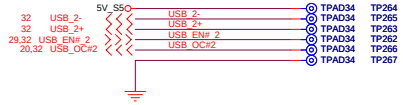
SPEAKER CONN



MODEM CABLE CONN

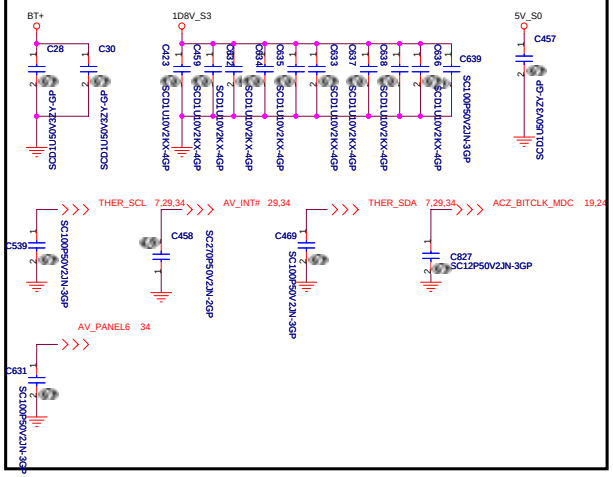


USB BOARD CONN

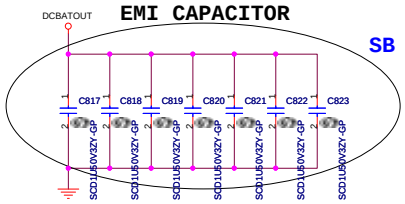


SC

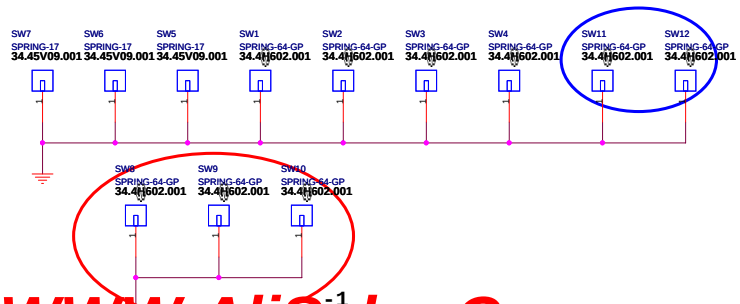
FOR EMI Solution

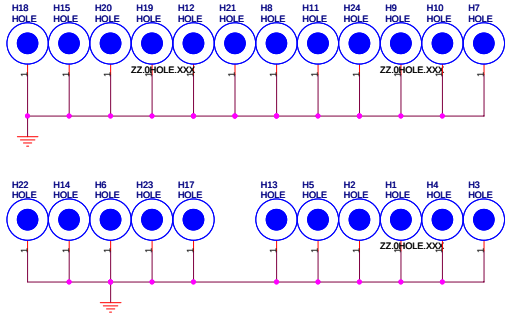


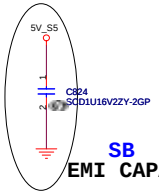
EMI CAPACITOR



FOR EMI Solution







SB
EMI CAPACITOR

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TTEST_PAD

Size: C | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 41 of 41