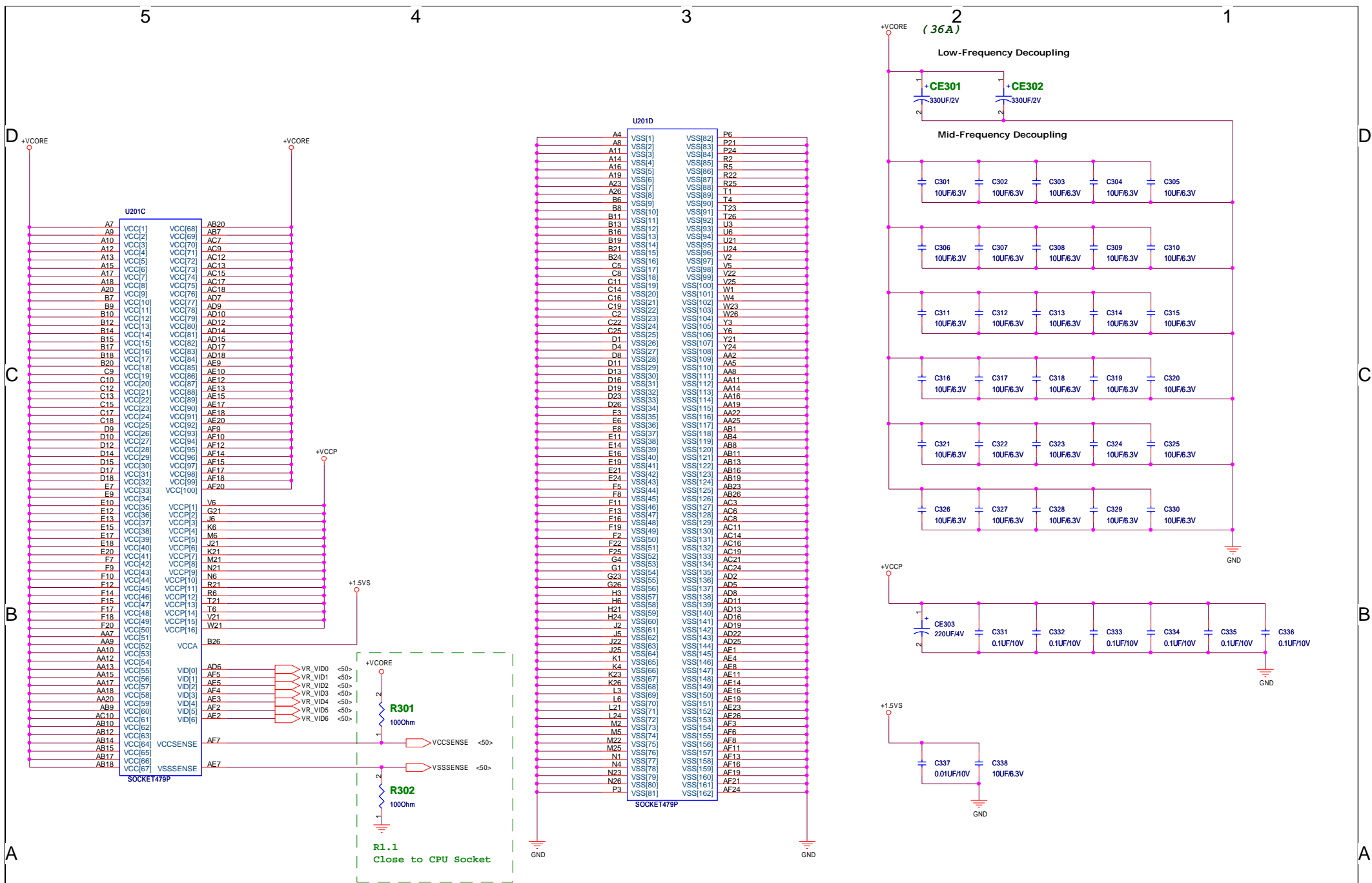
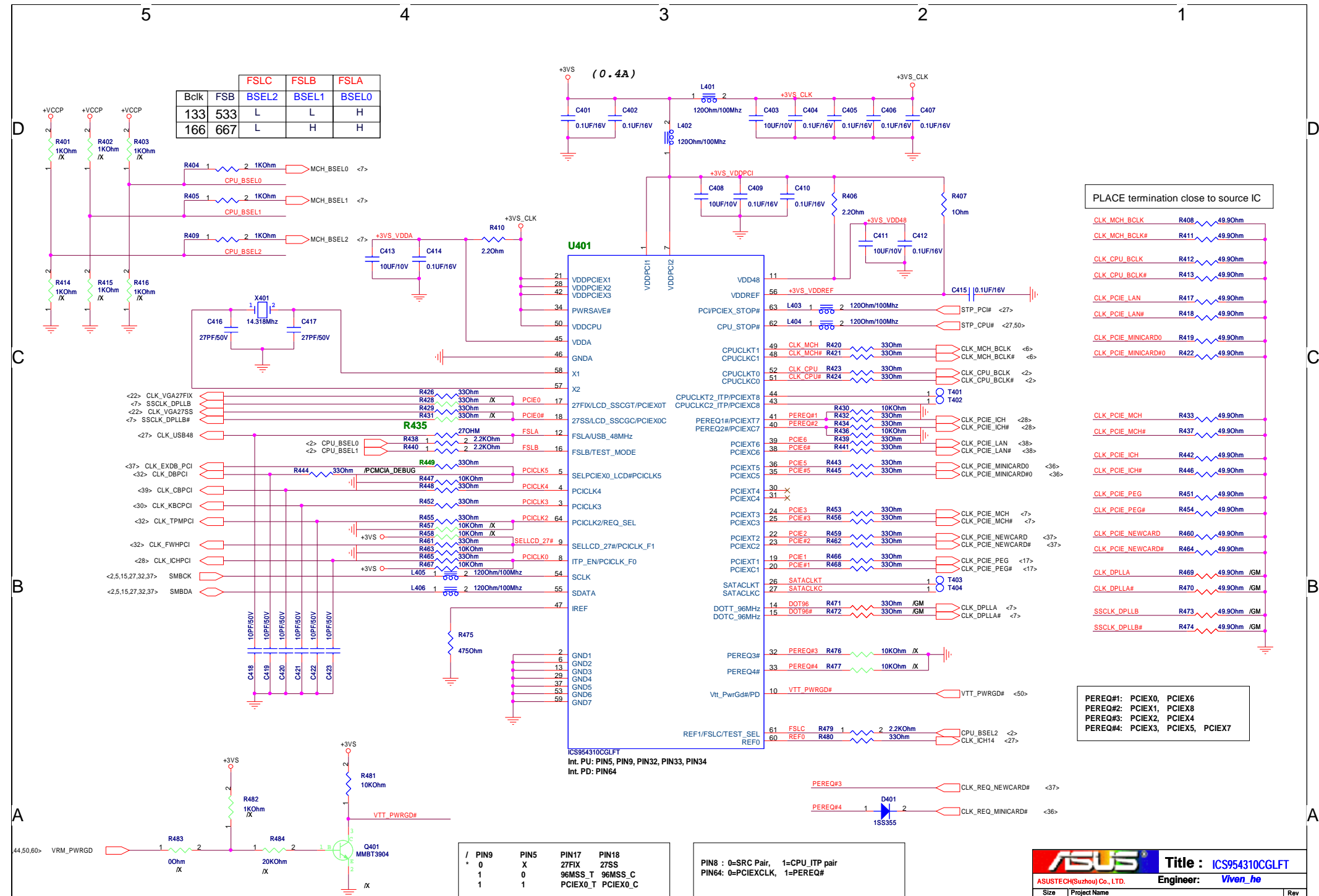


Content





Bclk	FSB	FSLC	FSLB	FSLA
133	533	BSEL2	BSEL1	BSEL0
166	667	L	L	H
		L	H	H



PLACE termination close to source IC

PEREQ#1: PCIE#0, PCIE#6
PEREQ#2: PCIE#1, PCIE#8
PEREQ#3: PCIE#2, PCIE#4
PEREQ#4: PCIE#3, PCIE#5, PCIE#7

Pin	Signal
1	VDDPCIE1
2	VDDPCIE2
3	VDDPCIE3
4	VDDPCIE4
5	VDDPCIE5
6	VDDPCIE6
7	VDDPCIE7
8	VDDPCIE8
9	VDDPCIE9
10	VDDPCIE10
11	VDDPCIE11
12	VDDPCIE12
13	VDDPCIE13
14	VDDPCIE14
15	VDDPCIE15
16	VDDPCIE16
17	VDDPCIE17
18	VDDPCIE18
19	VDDPCIE19
20	VDDPCIE20
21	VDDPCIE21
22	VDDPCIE22
23	VDDPCIE23
24	VDDPCIE24
25	VDDPCIE25
26	VDDPCIE26
27	VDDPCIE27
28	VDDPCIE28
29	VDDPCIE29
30	VDDPCIE30
31	VDDPCIE31
32	VDDPCIE32
33	VDDPCIE33
34	VDDPCIE34
35	VDDPCIE35
36	VDDPCIE36
37	VDDPCIE37
38	VDDPCIE38
39	VDDPCIE39
40	VDDPCIE40
41	VDDPCIE41
42	VDDPCIE42
43	VDDPCIE43
44	VDDPCIE44
45	VDDPCIE45
46	VDDPCIE46
47	VDDPCIE47
48	VDDPCIE48
49	VDDPCIE49
50	VDDPCIE50
51	VDDPCIE51
52	VDDPCIE52
53	VDDPCIE53
54	VDDPCIE54
55	VDDPCIE55
56	VDDPCIE56
57	VDDPCIE57
58	VDDPCIE58
59	VDDPCIE59

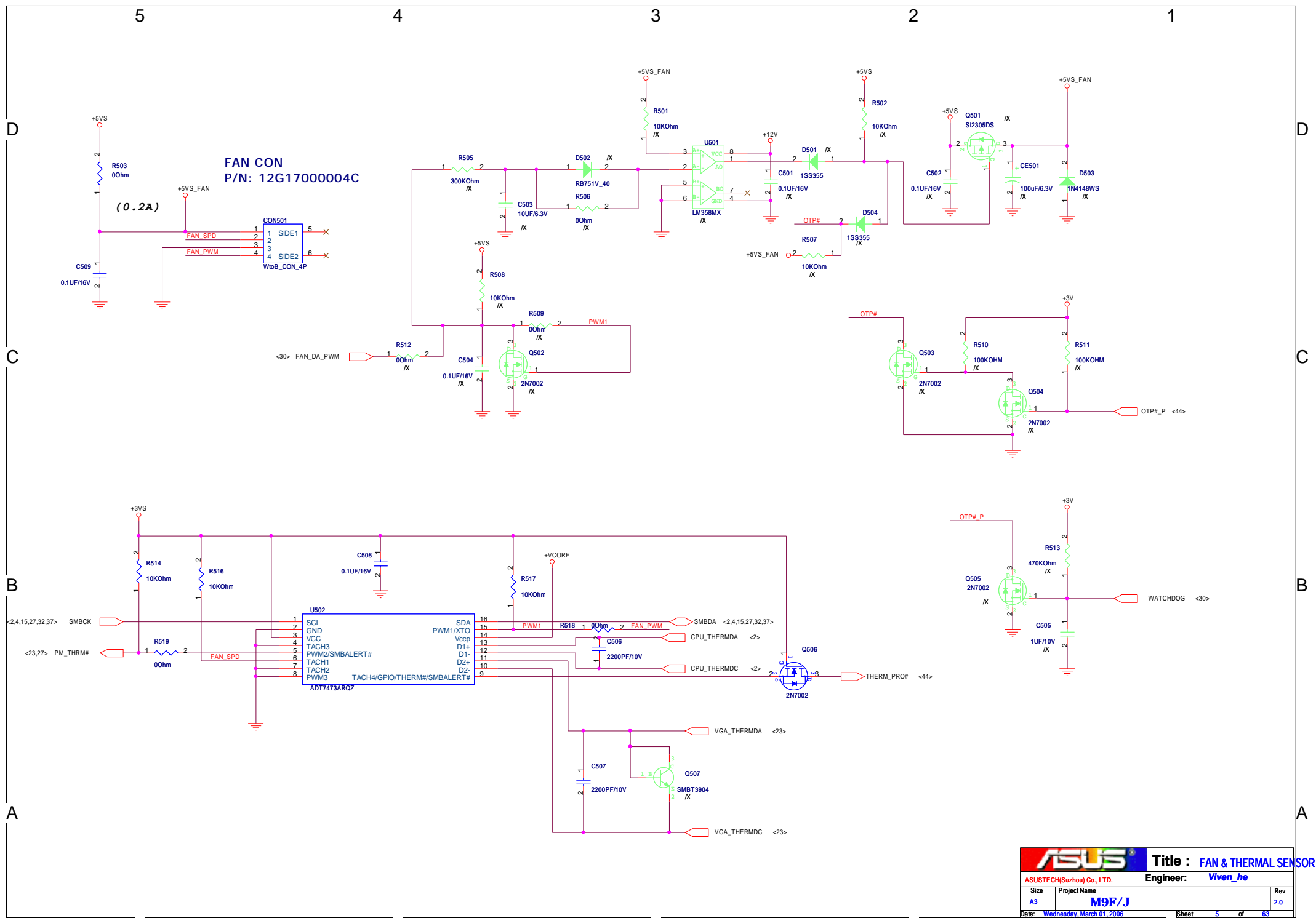
PIN8 : 0=SRC Pair, 1=CPU_ITP pair
PIN64 : 0=PCIECLK, 1=PEREQ#

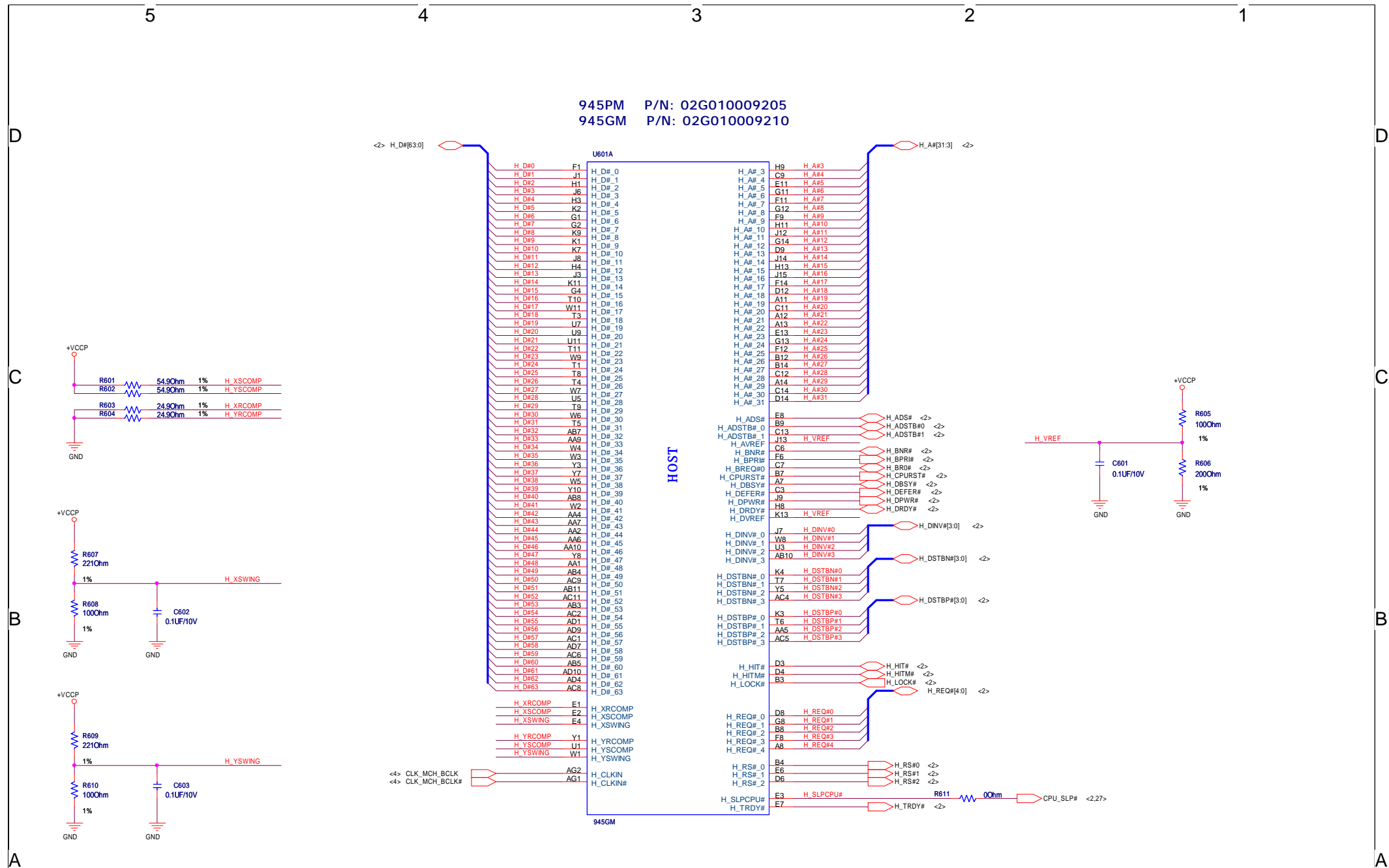
Title : ICS954310CGLFT

ASUSTECH(Suzhou) Co., LTD.
 Engineer: Viven_hu

Size A3
 Project Name M9F/J
 Rev 2.0

Date: Wednesday, March 01, 2006
 Sheet 4 of 63





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STRAPPING CONFIGURATION

CFG[17:3] - Internal pull-up
CFG[20:18] - Internal pull-down

R705 2.2KOhm /X DMI_SEL

CFG5 - DMI x2 Select
0 = DMI x2
1 = DMI x4 (default)

R710 2.2KOhm /X CPU_STRAP

CFG7 - CPU Strap
0 = Reserved
1 = Mobile CPU (default)

R711 2.2KOhm PCIE_RVS

CFG9 - PCI-E Lane Reversal
0 = Reverse Lanes
1 = Normal (default)

R714 2.2KOhm /X TEST_MD0

R715 2.2KOhm /X TEST_MD1

CFG[13:12] - XOR/ALLZ
00 = Partial Clock Gating Disable
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal (default)

R718 2.2KOhm /X DYN_ODT

CFG16 - FSB Dynamic ODT
0 = Disabled
1 = Enabled (default)

R723 1KOhm /X VCC_SEL

CFG18 - GMCH VCC Select
0 = 1.05V (default)
1 = 1.5V

R725 1KOhm /X DMI_RVS

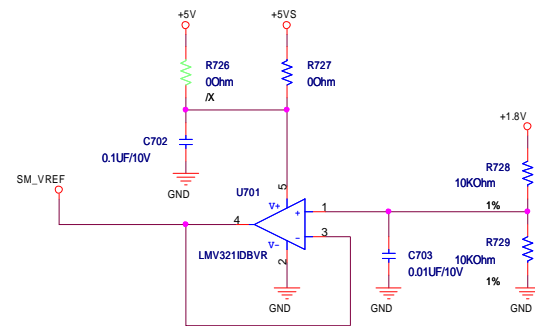
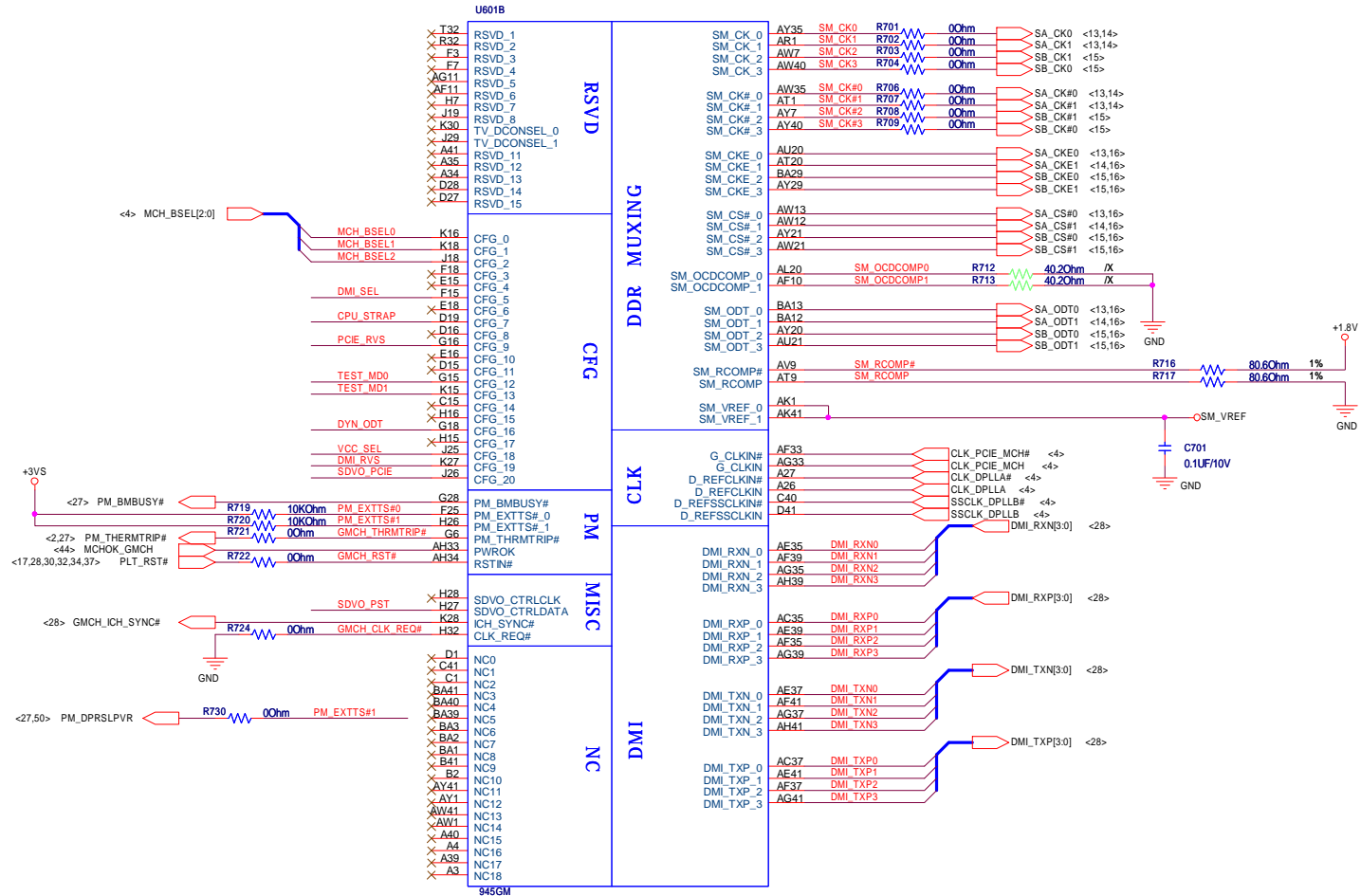
CFG19 - DMI Lane Reversal
0 = Normal (default)
1 = Reverse Lanes

T701 1 TPC28T SDVO_PCIE

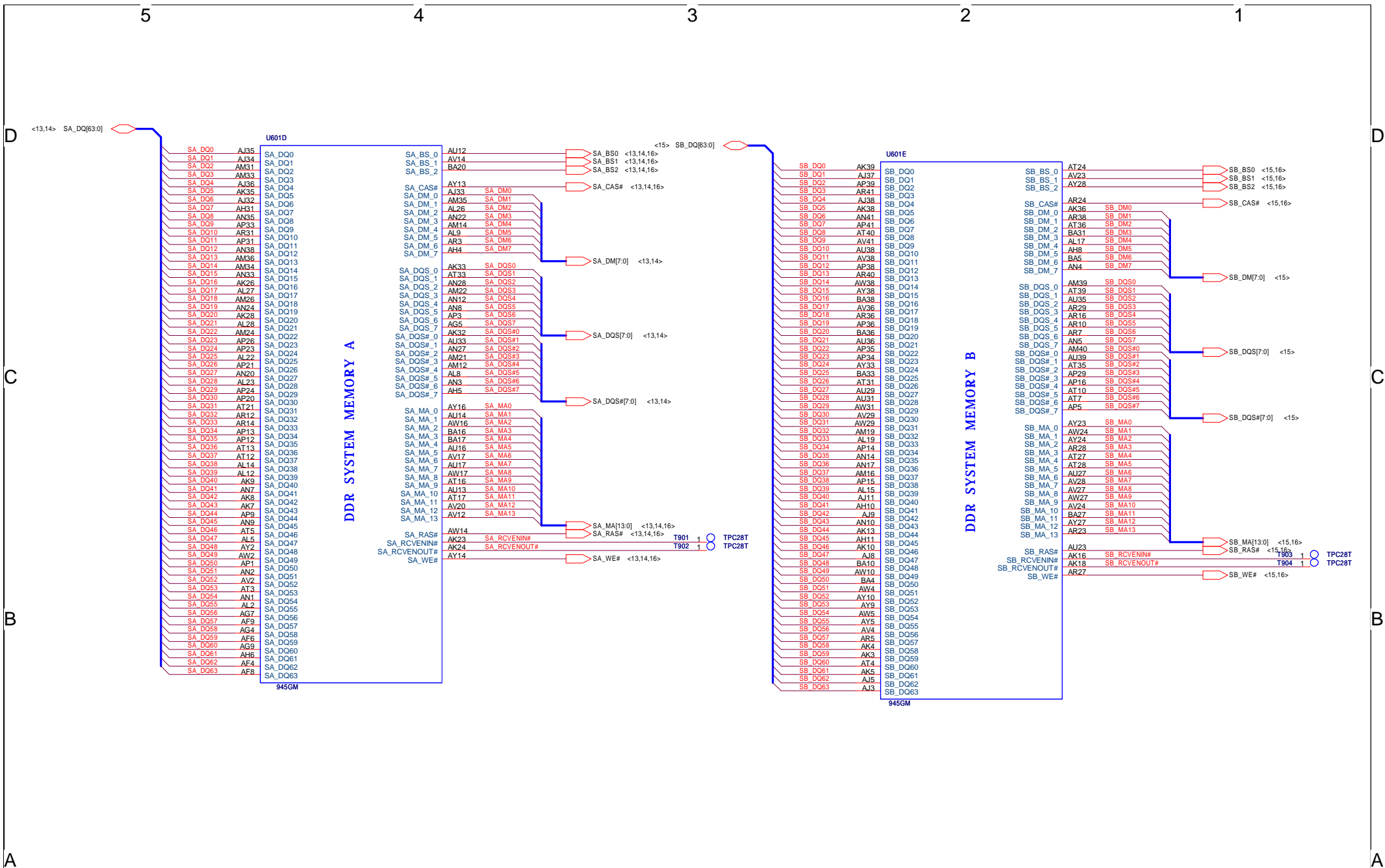
CFG20 - SDVO/PCIE Concurrent
0 = Only SDVO or PCIE x1 is operational (default)
1 = SDVO and PCIE x1 are operating simultaneously via PEG port

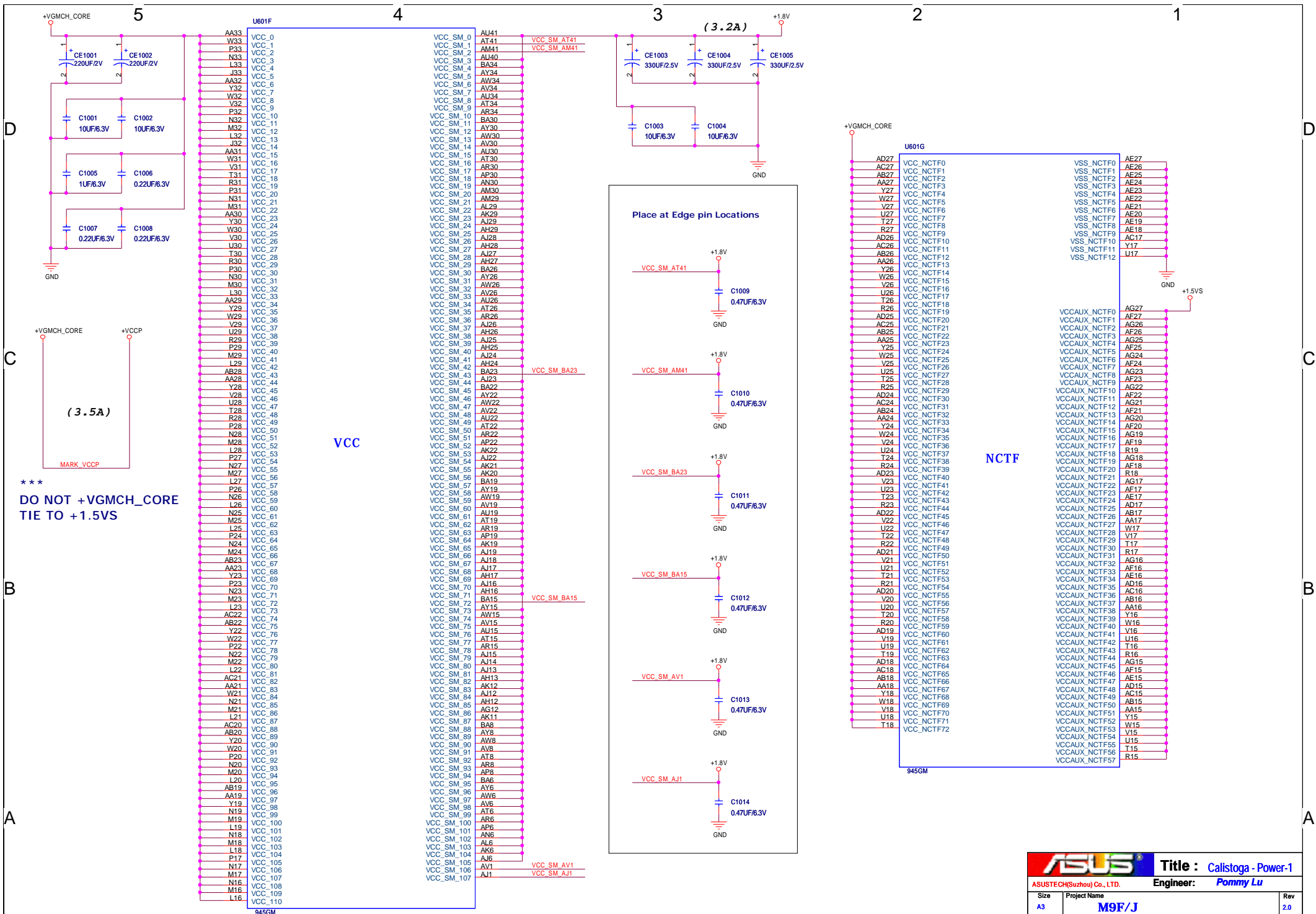
T702 1 TPC28T SDVO_PST

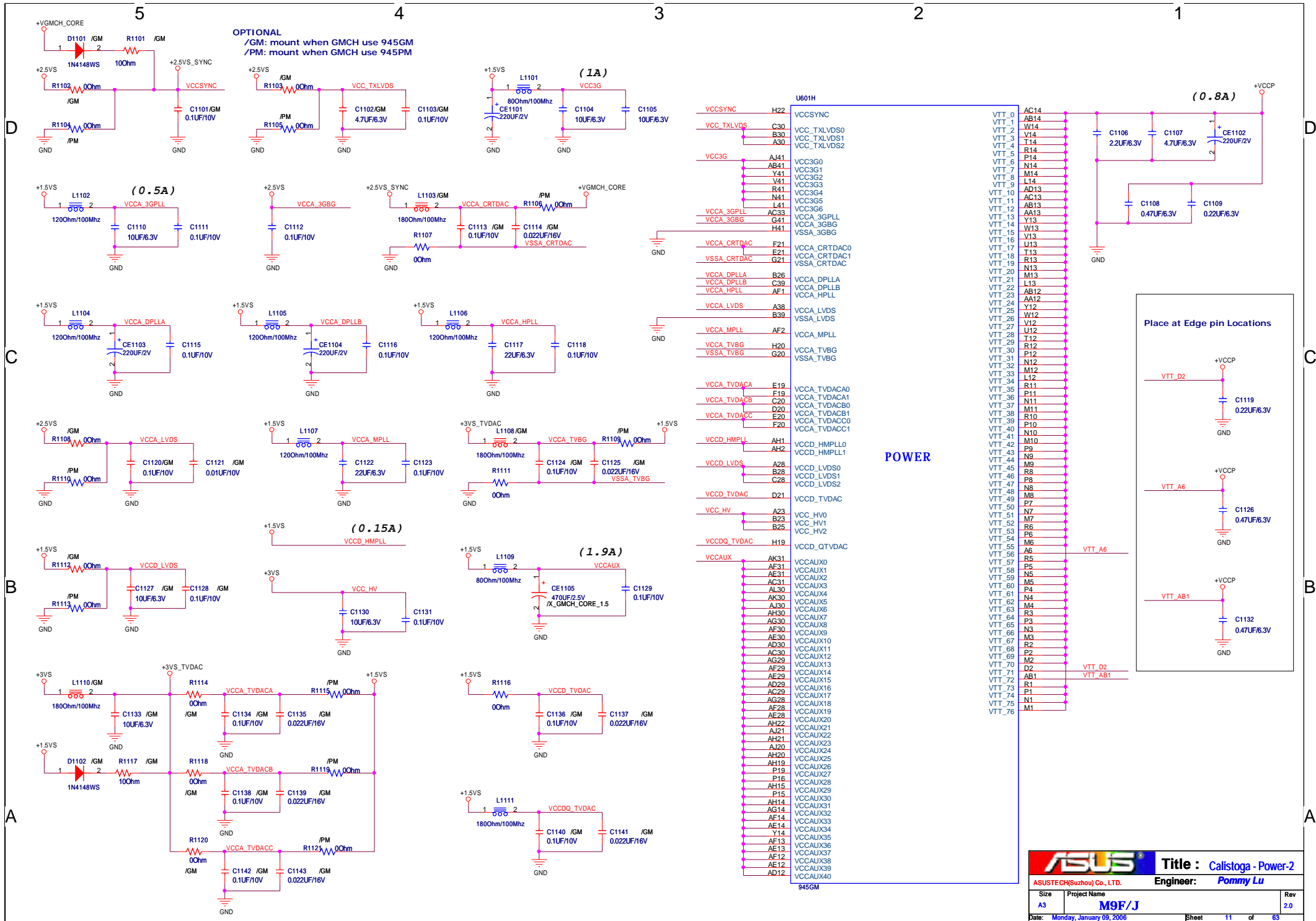
SDVO_CTRLCLK - SDVO Present
0 = No SDVO Card Present (default)
1 = SDVO Card Present











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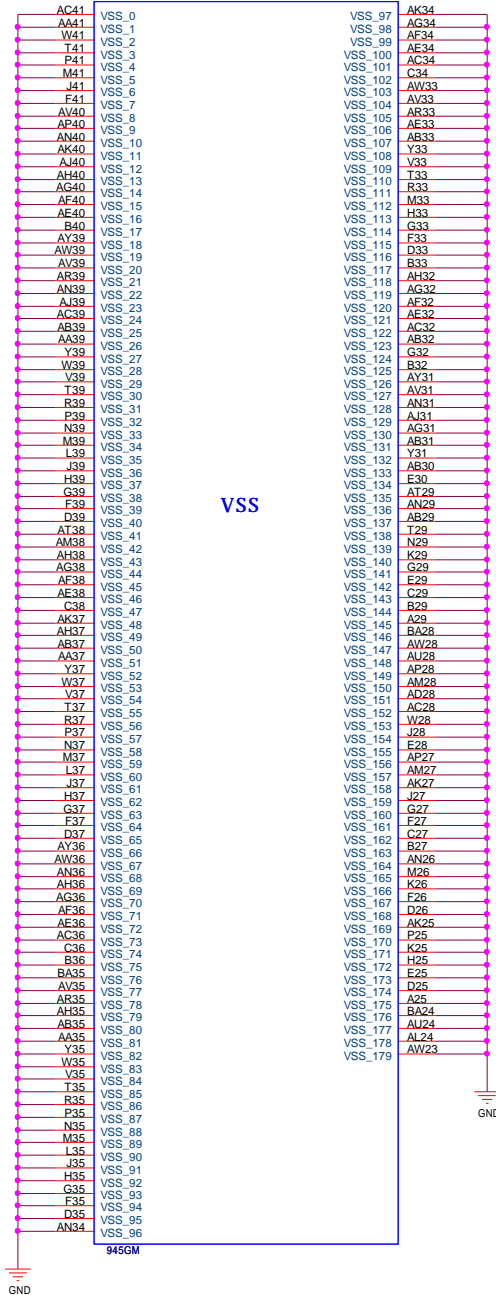
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U601I



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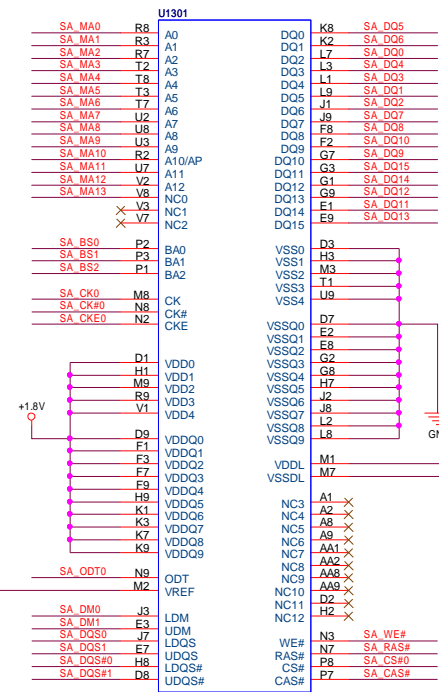
A

On Board 256MB
DDR2 533 32Mx16-3.7
P/N: 03G15073B010 (1st)
03G15133E110 (2nd)

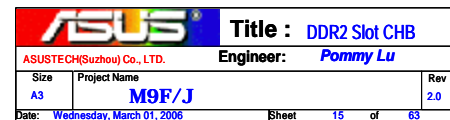
On Board 512MB
DDR2 533 32Mx16-3.7
P/N: 03G15073B010 (1st)
03G15133E110 (2nd)

On Board 512MB
DDR2 667 32Mx16-3
P/N: (null)

On Board 1GB
DDR2 533 64Mx16-3.7
P/N: 03G15163E010







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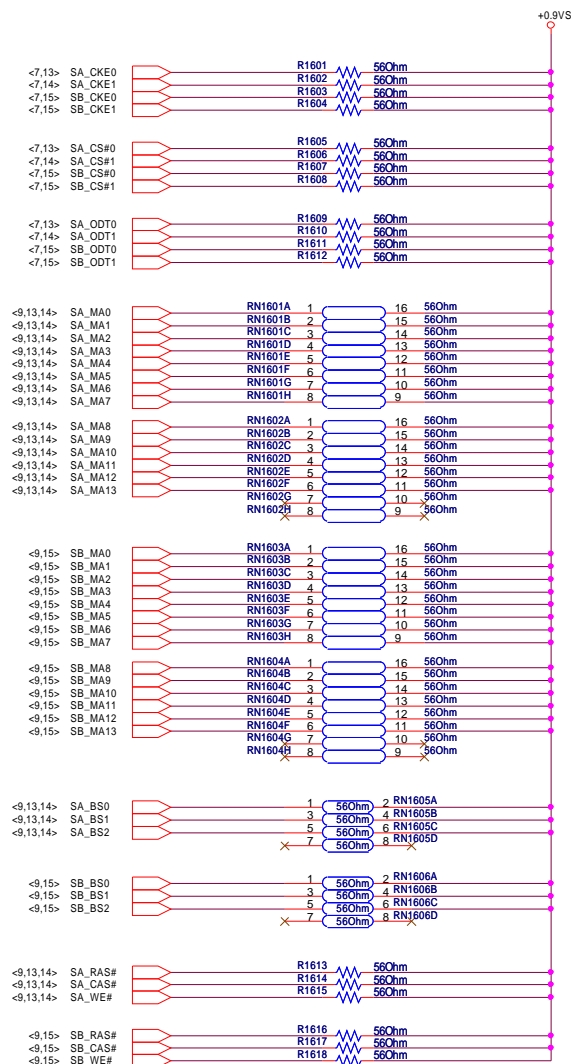
C

B

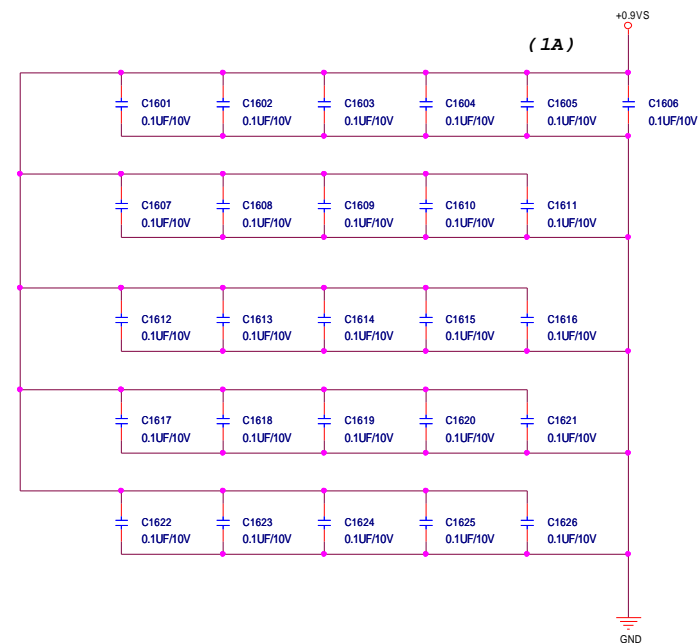
B

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Place one cap close to every 2 pull-up resistors terminated to +0.9VS



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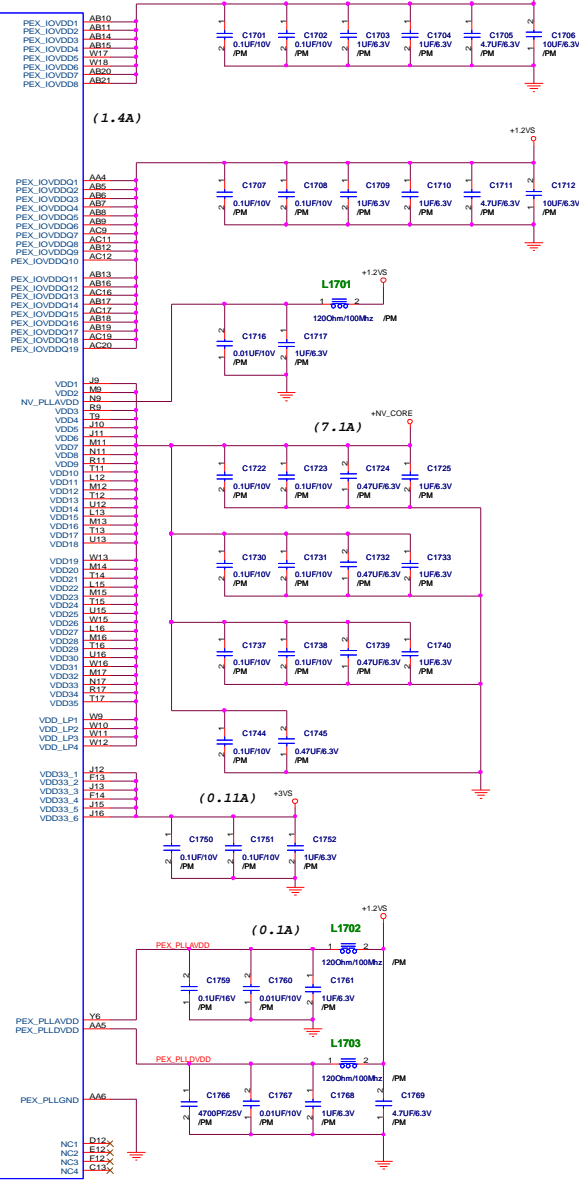
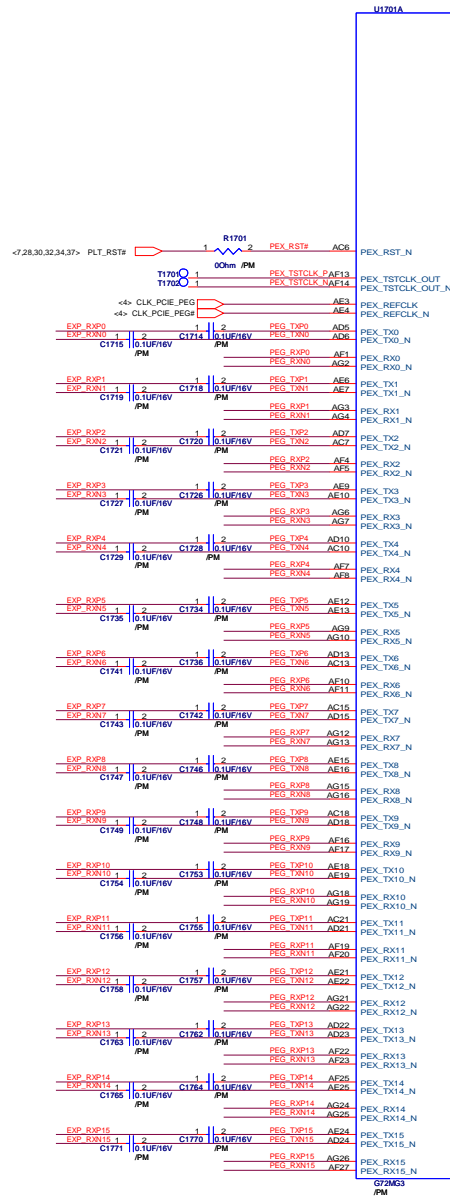
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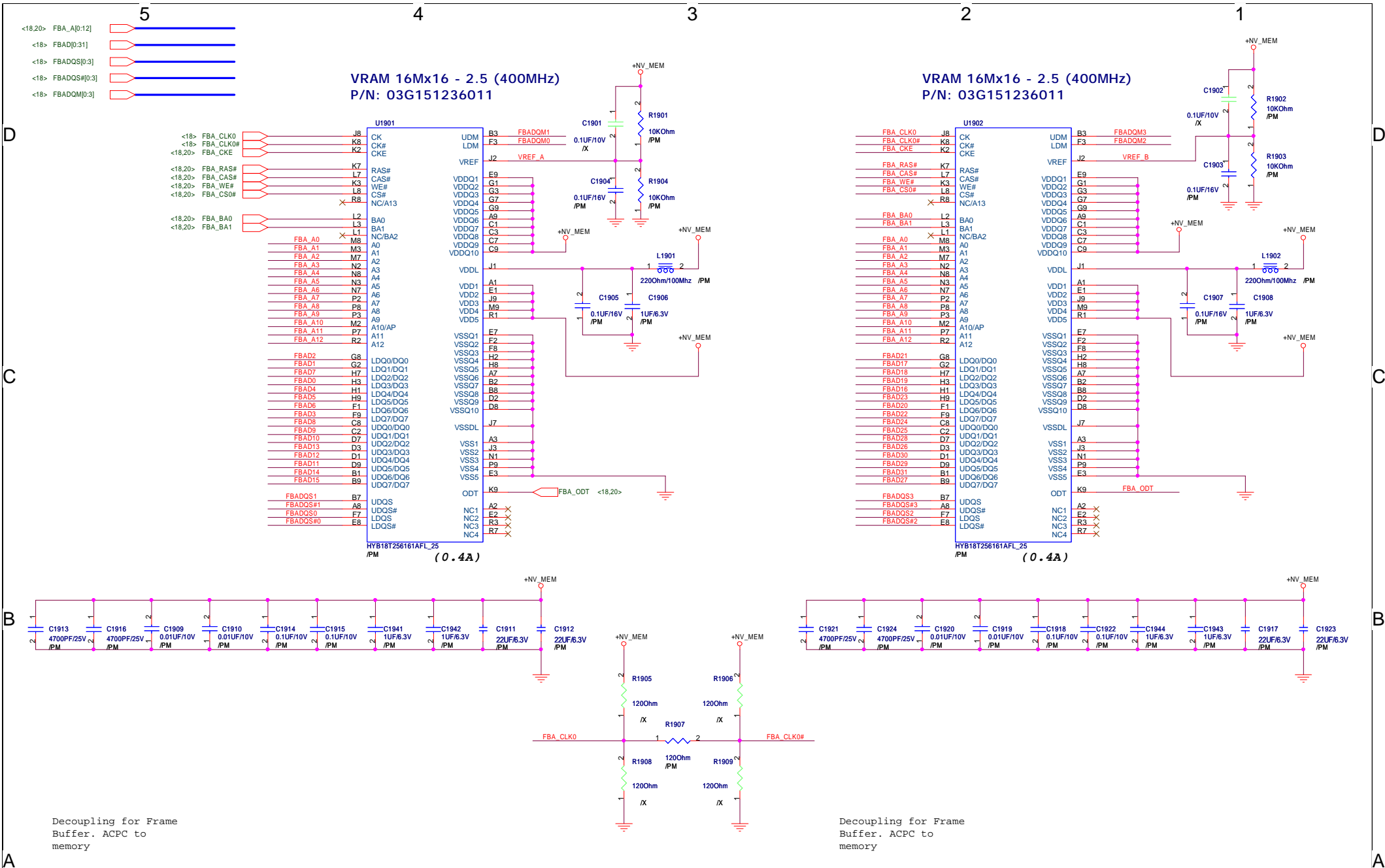
3

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1

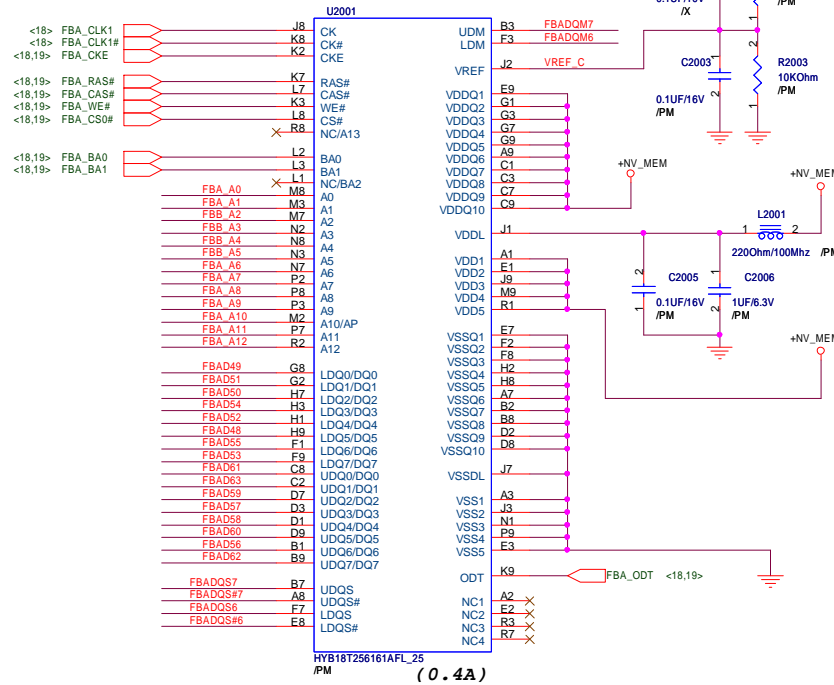
G72M-V P/N: 02G190009311



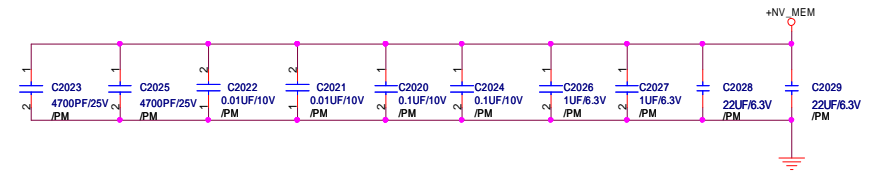
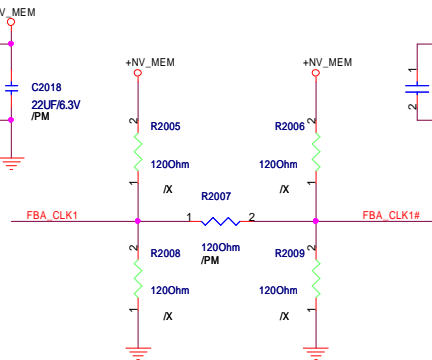
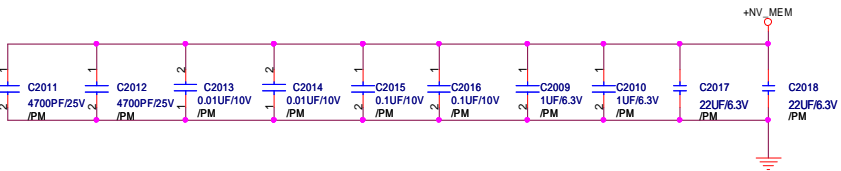
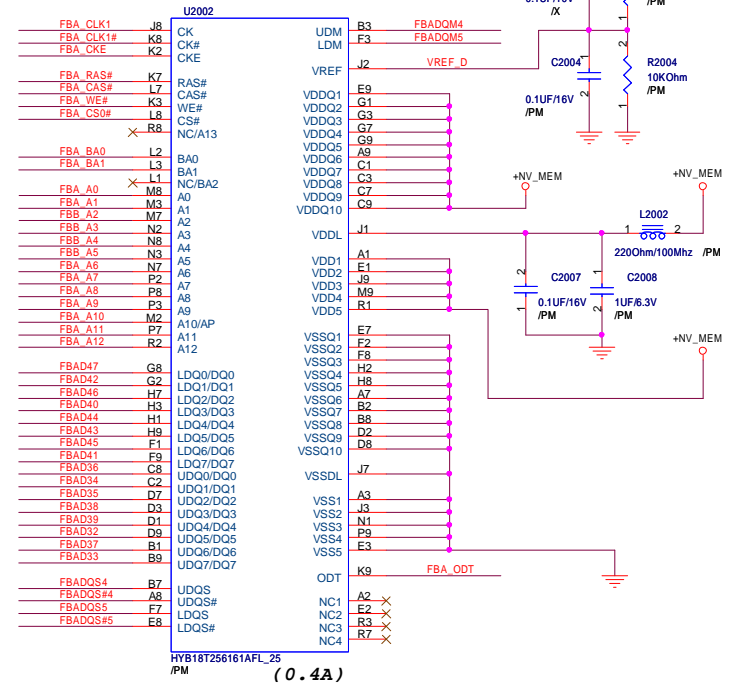


<18,19> FBA_A[0:12]
 <18> FBAD[32:63]
 <18> FBADQS[4:7]
 <18> FBB_A[2:5]
 <18> FBADQS[4:7]
 <18> FBADQM[4:7]

VRAM 16Mx16 - 2.5 (400MHz)
 P/N: 03G151236011



VRAM 16Mx16 - 2.5 (400MHz)
 P/N: 03G151236011

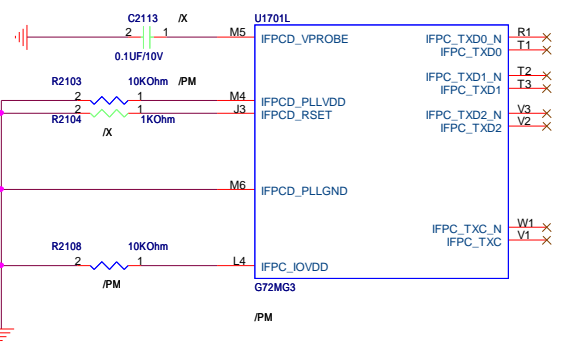
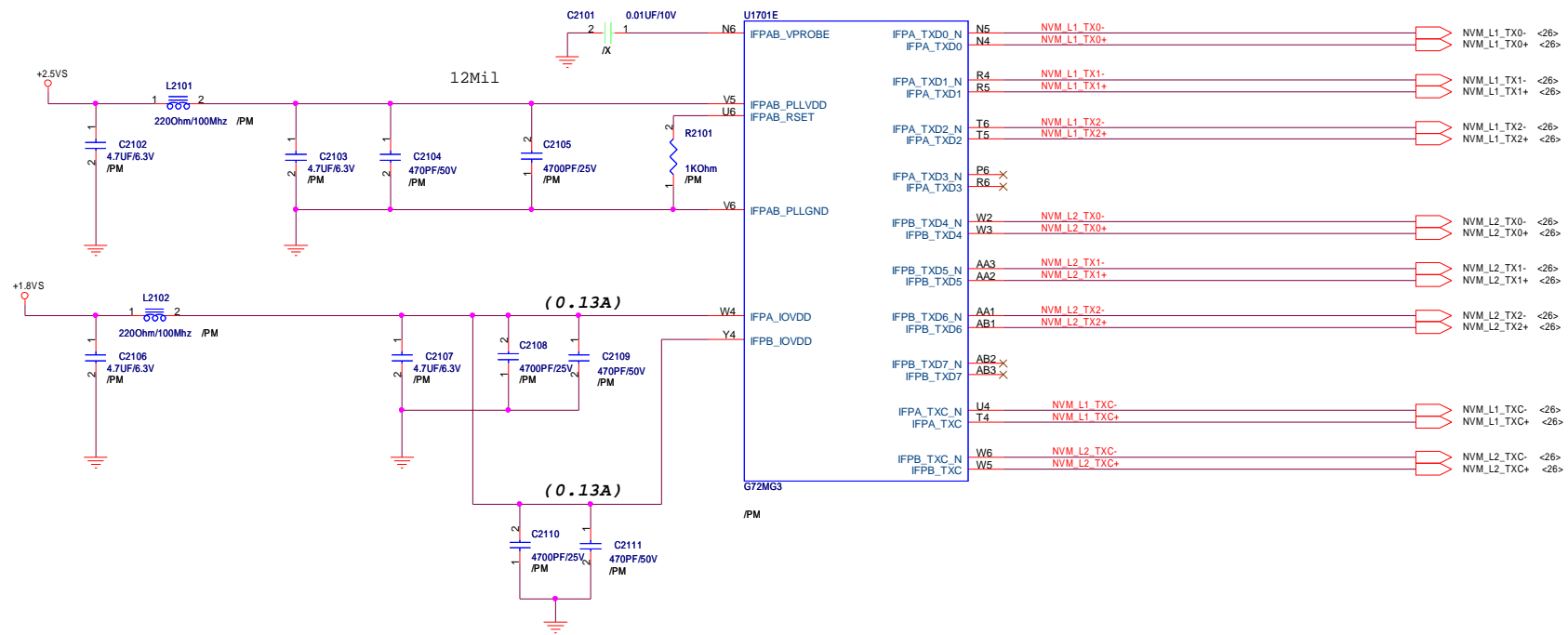


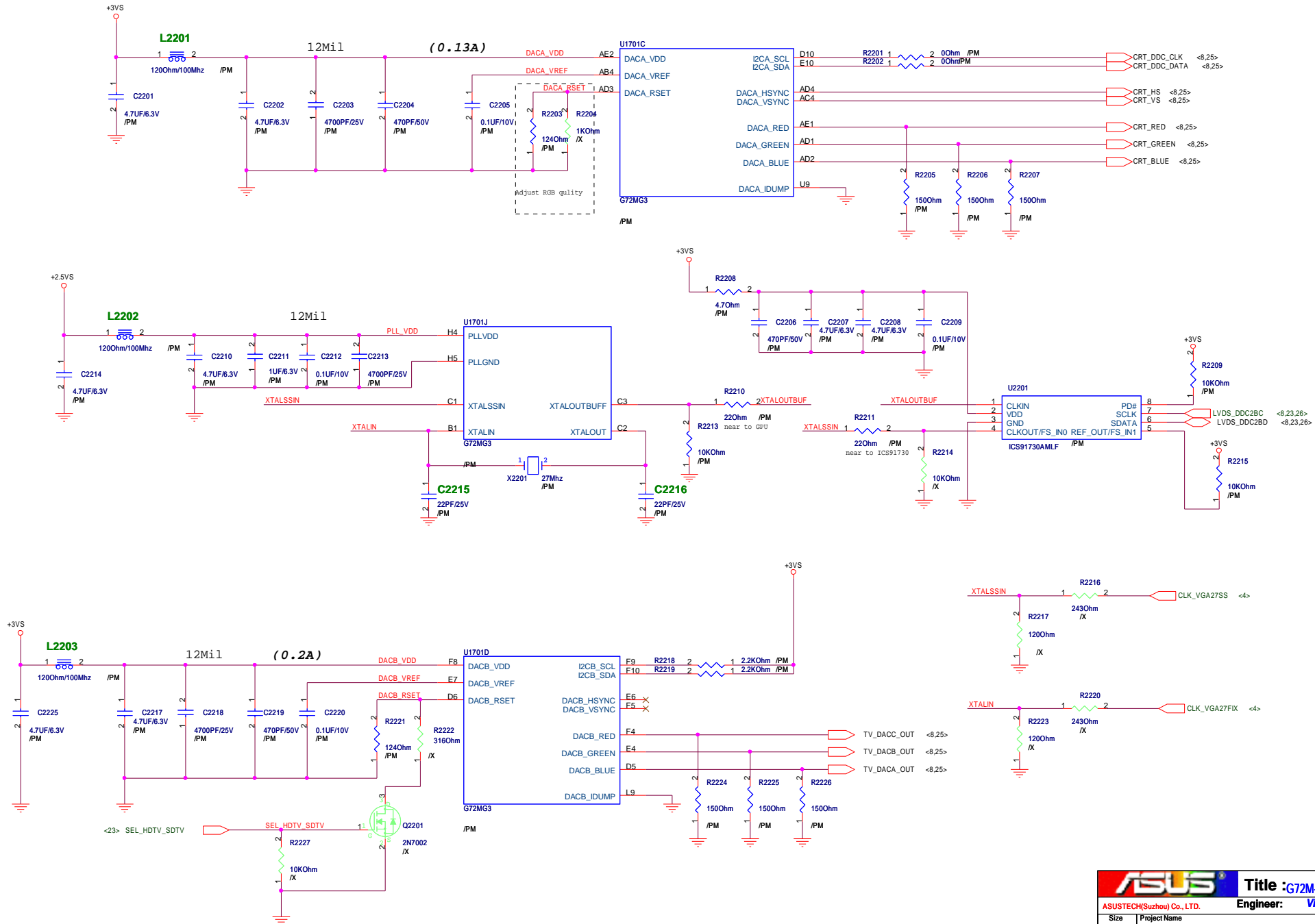
Decoupling for Frame
 Buffer. ACPC to
 memory

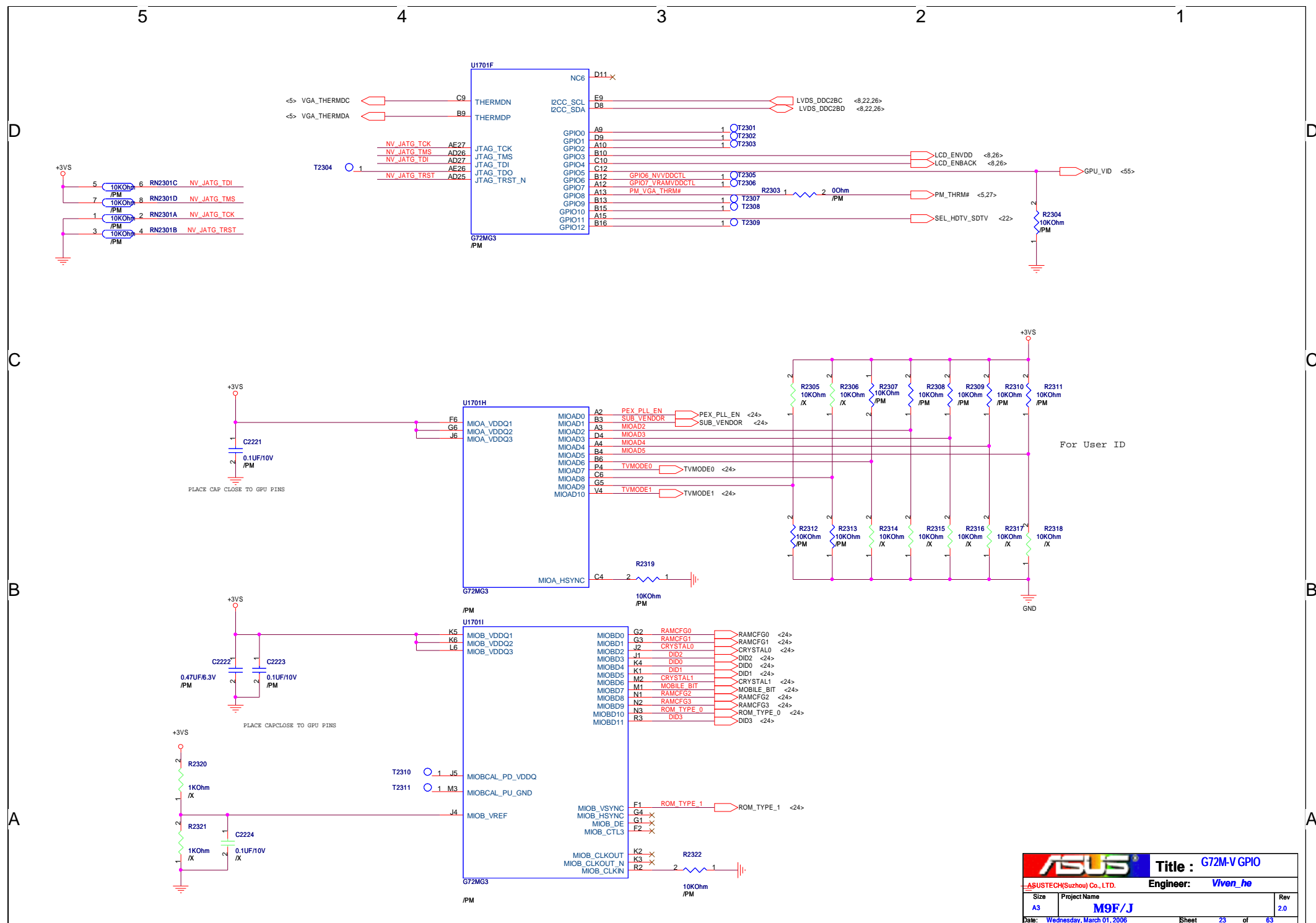
Decoupling for Frame
 Buffer. ACPC to
 memory

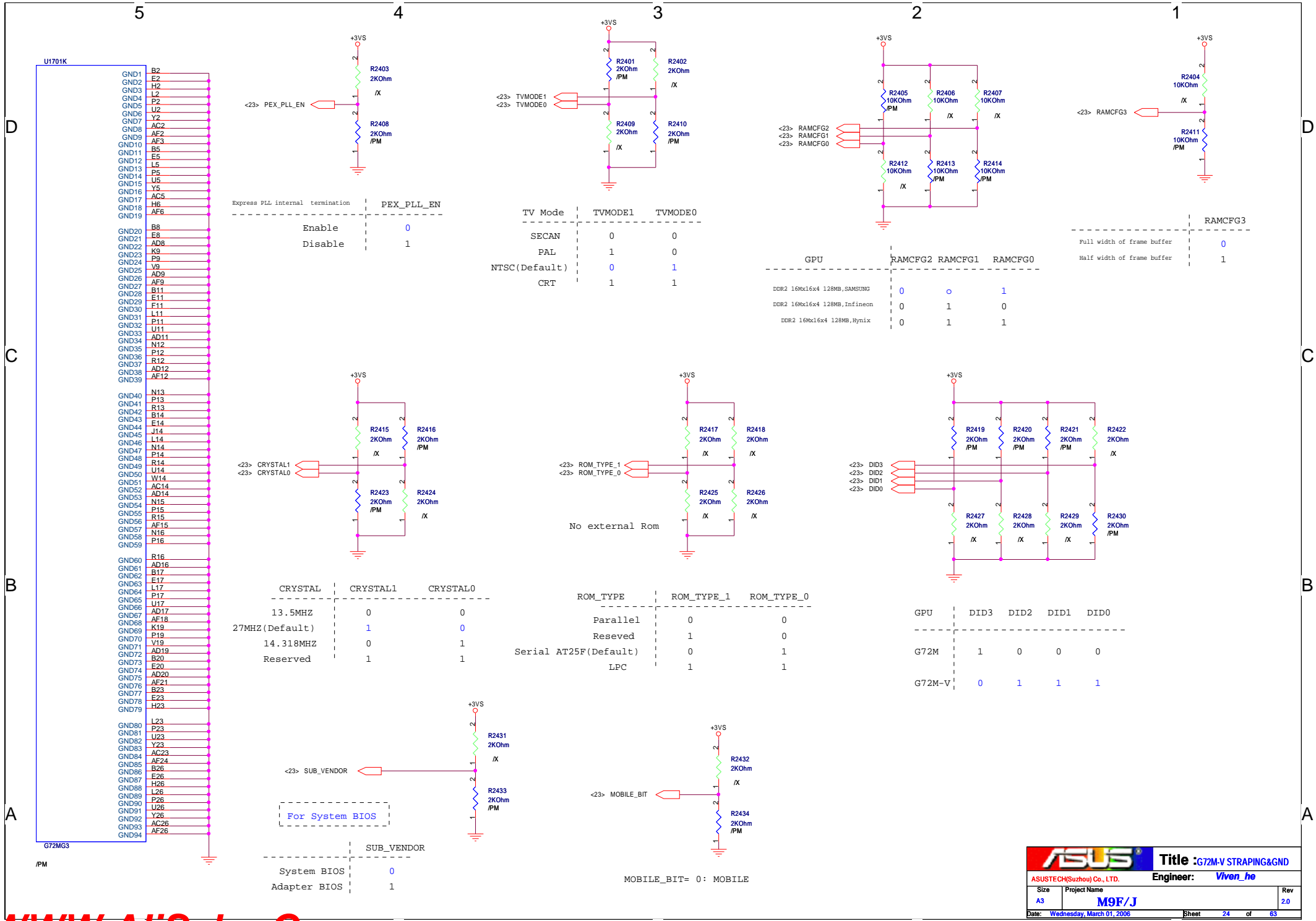
ASUS		Title : G72M-V VRAM2	
ASUSTECH(Suzhou) Co., LTD.		Engineer: Viven_he	
Size A3	Project Name M9F/J	Rev 2.0	
Date: Wednesday, March 01, 2006		Sheet 20 of 63	

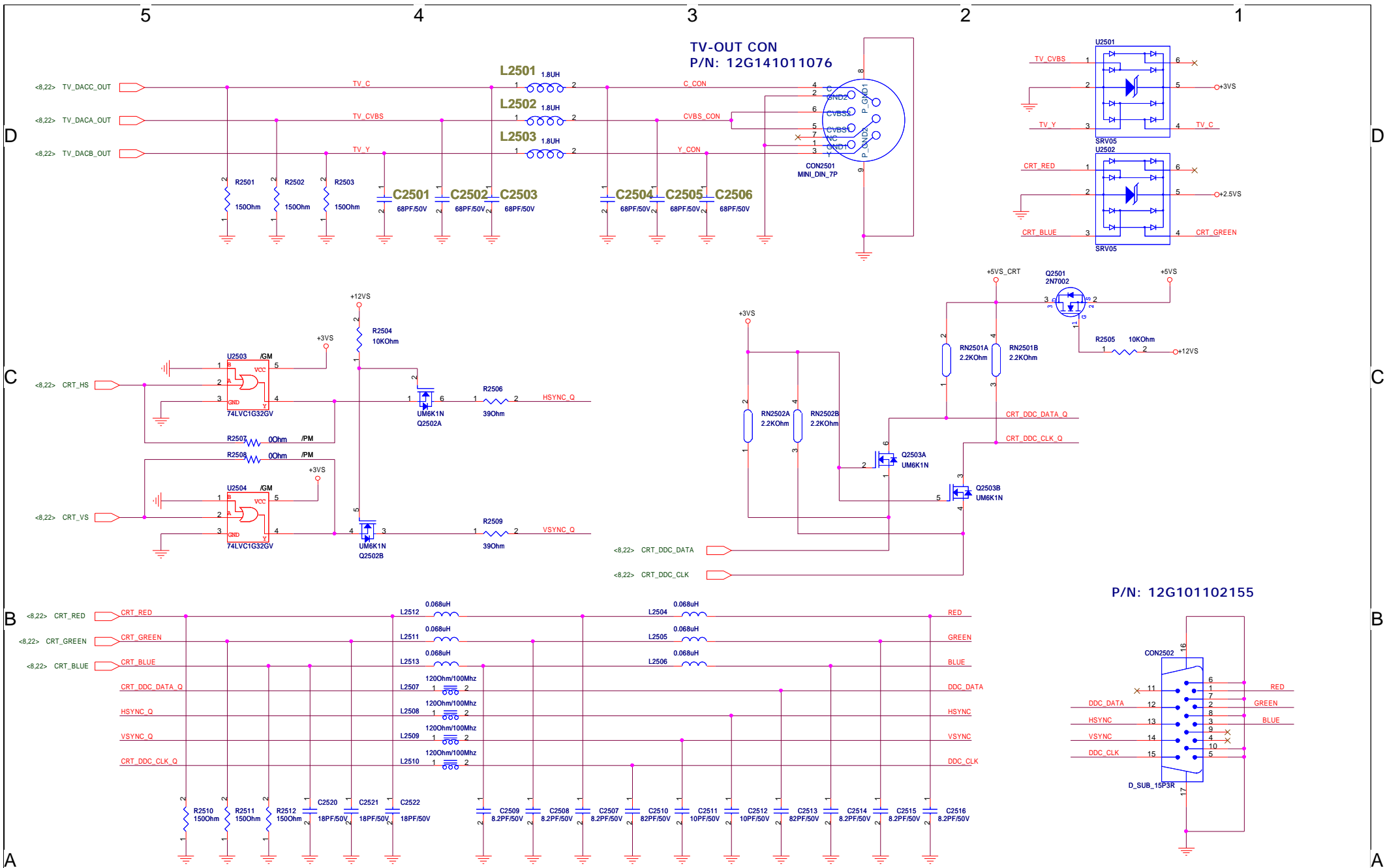
5 4 3 2 1



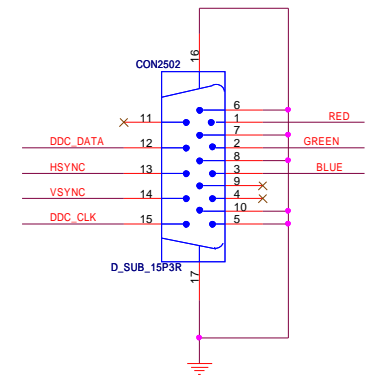


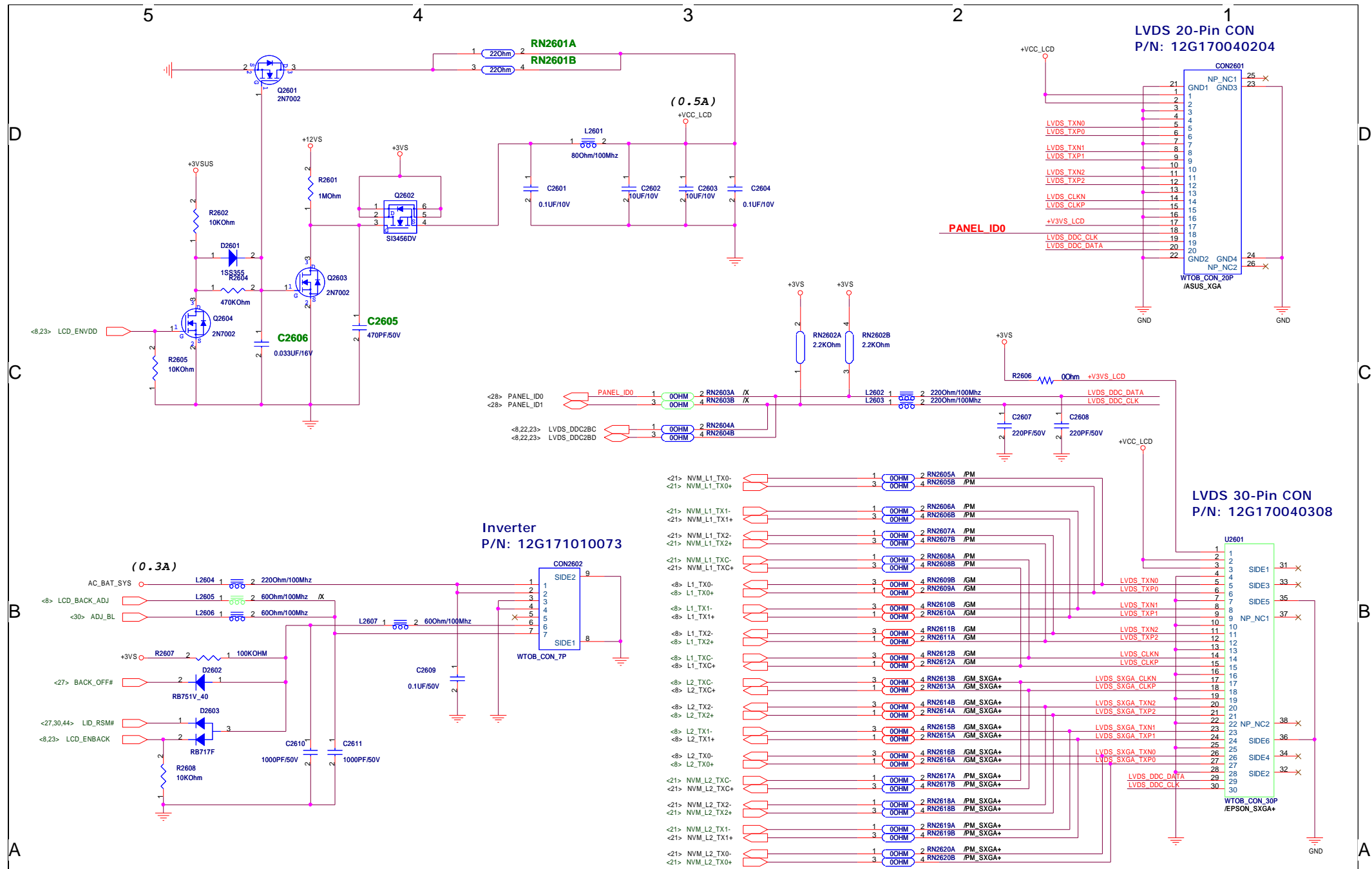


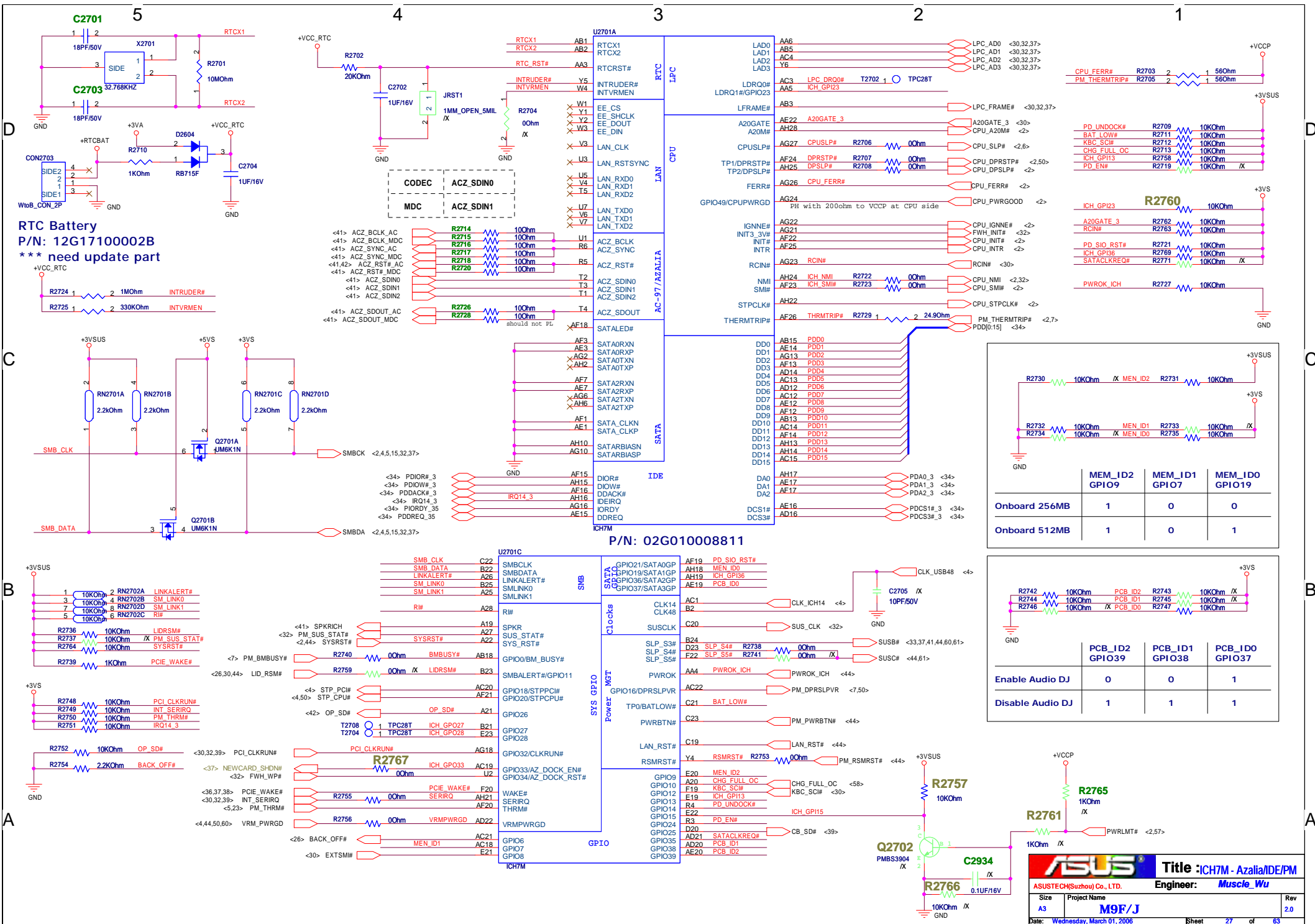




P/N: 12G101102155

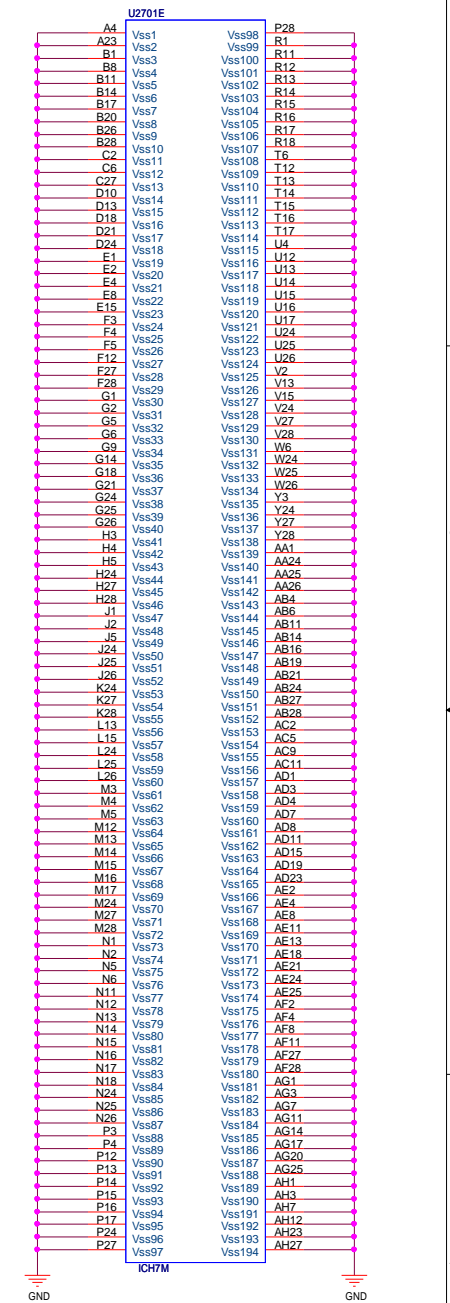
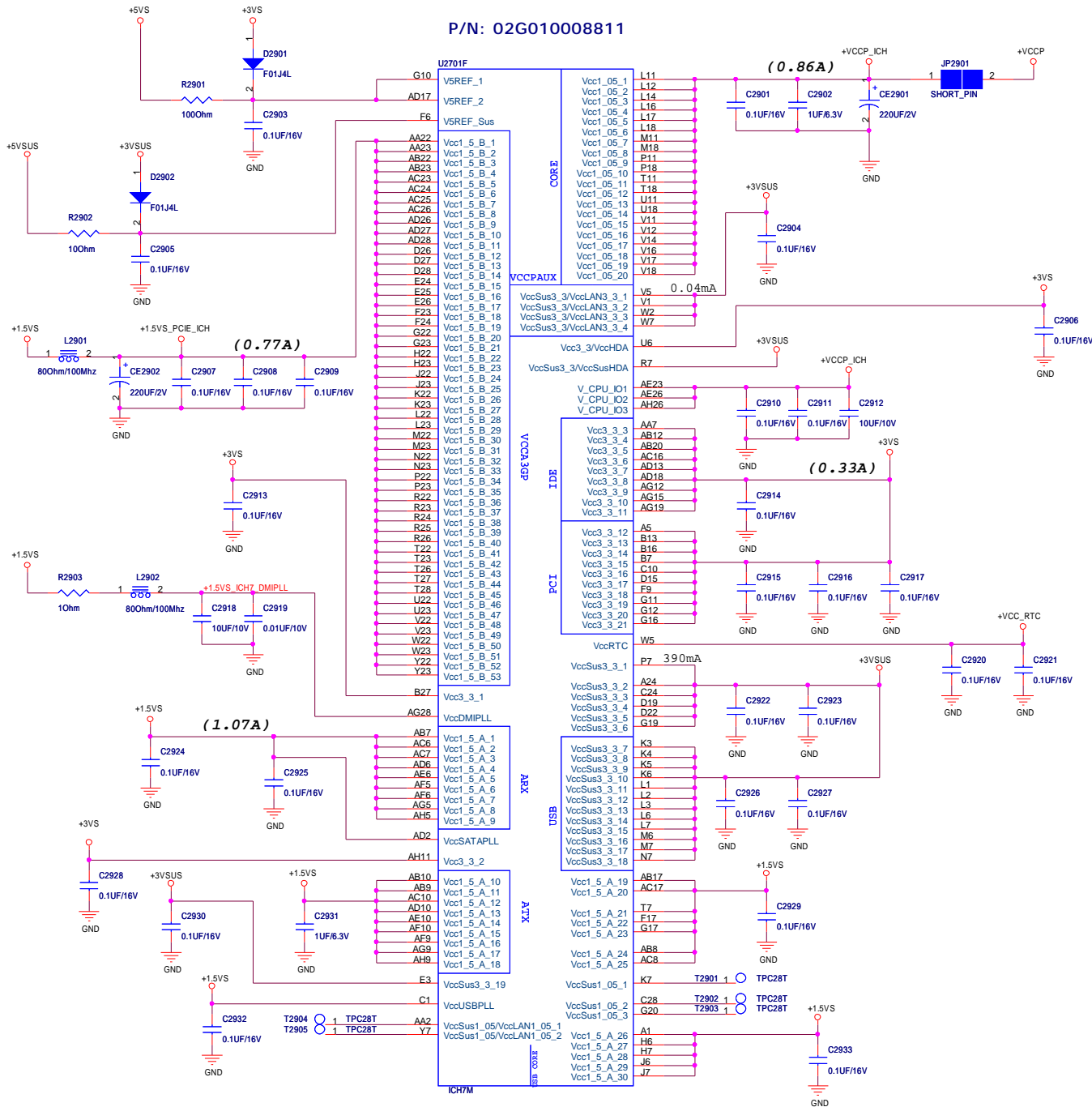


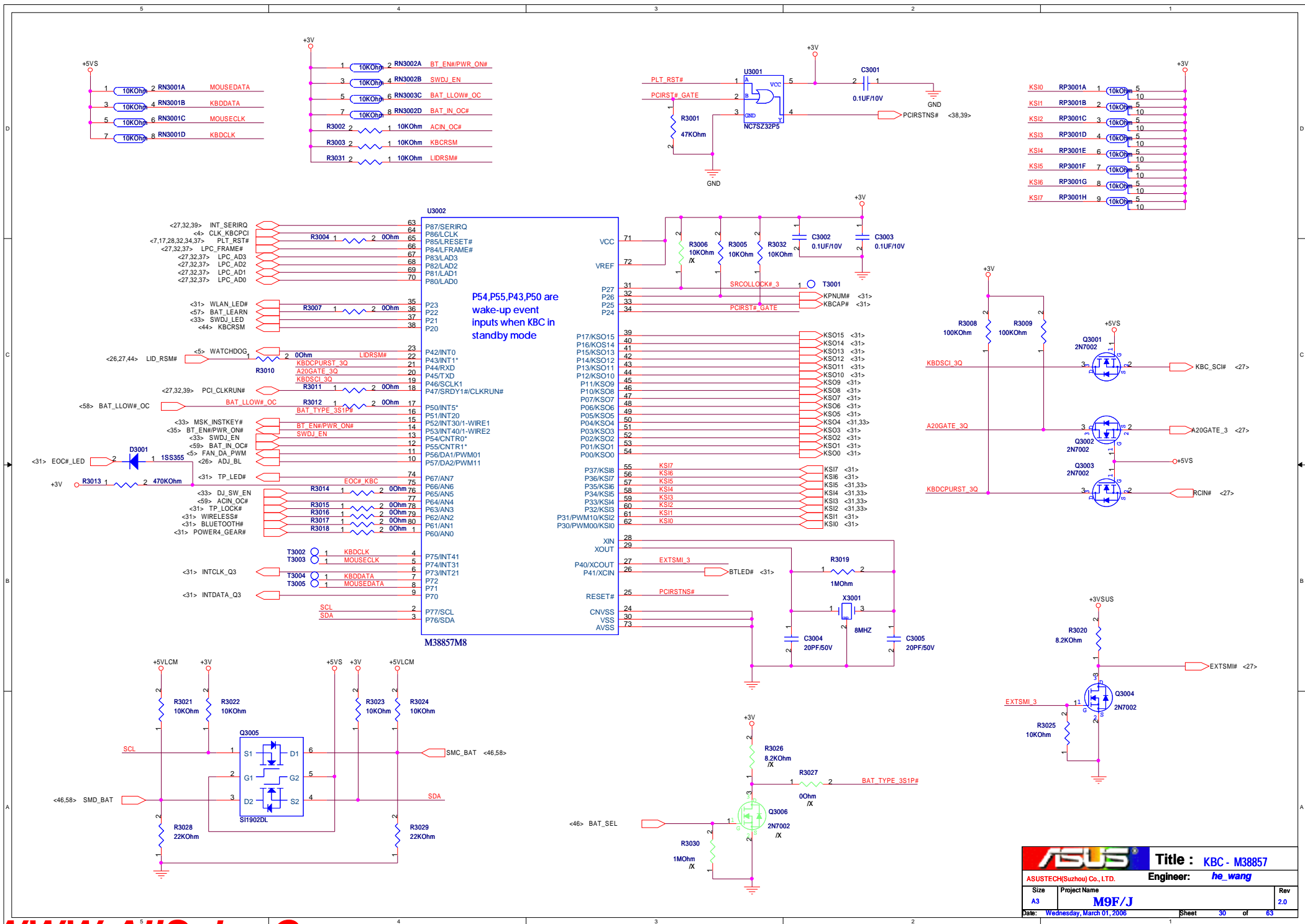


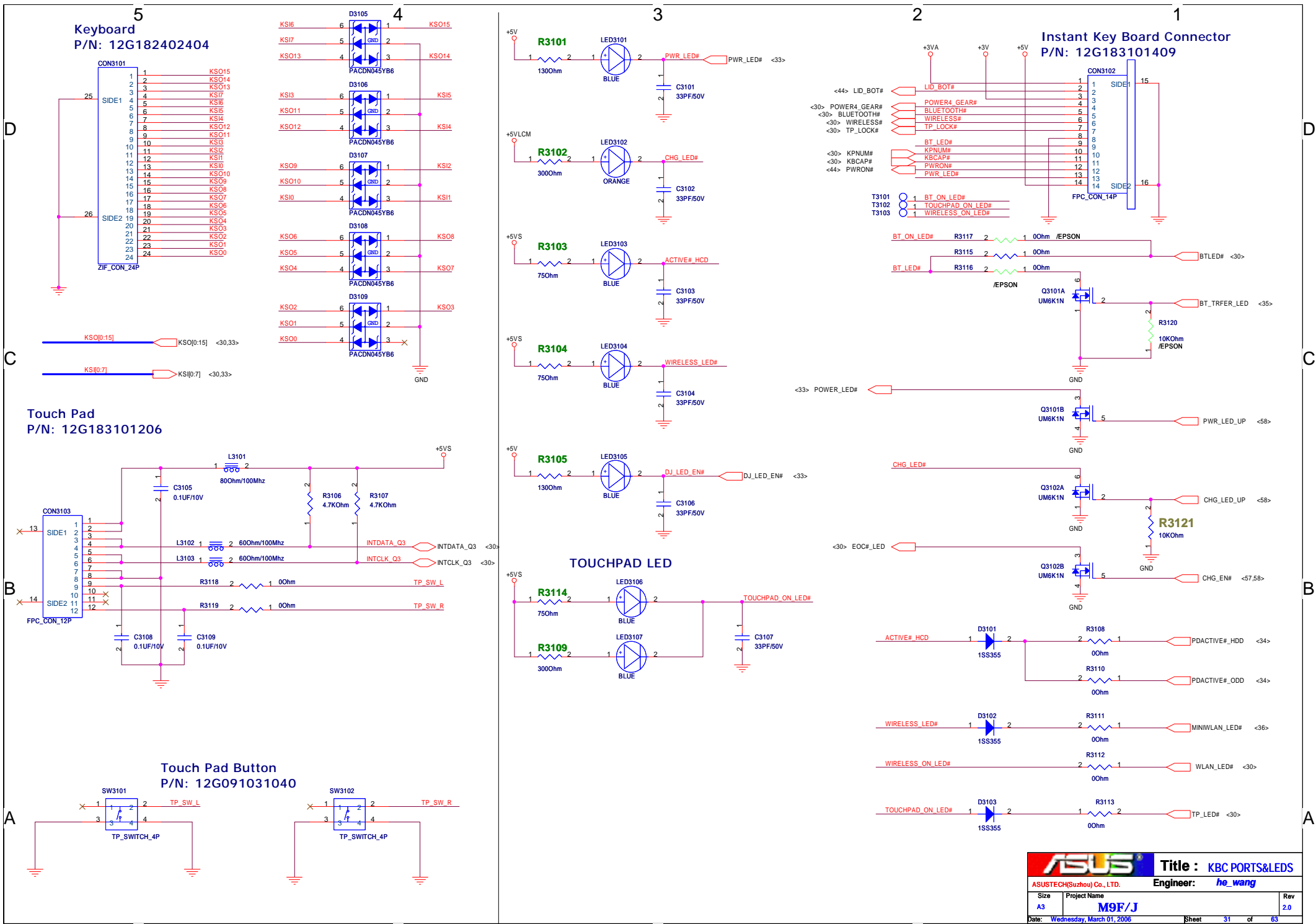




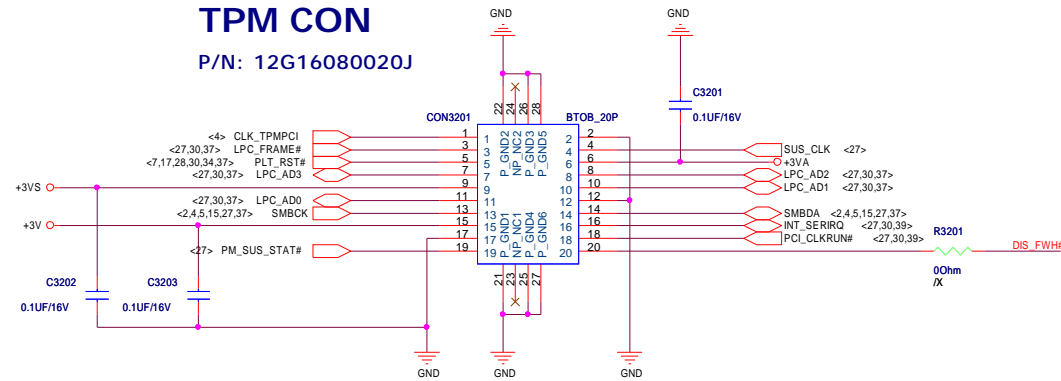
P/N: 02G010008811



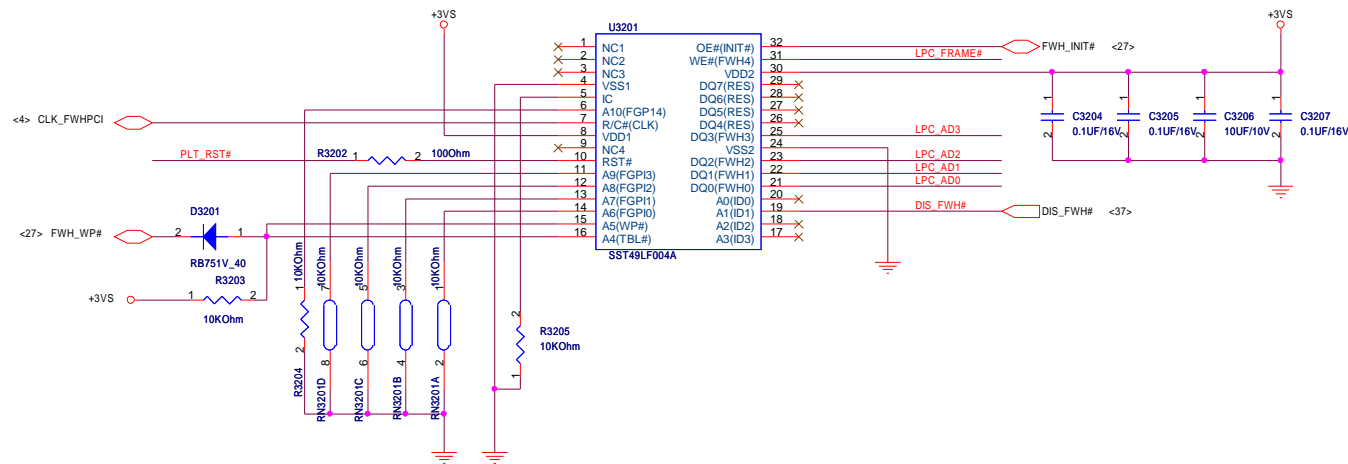




P/N: 12G16080020J

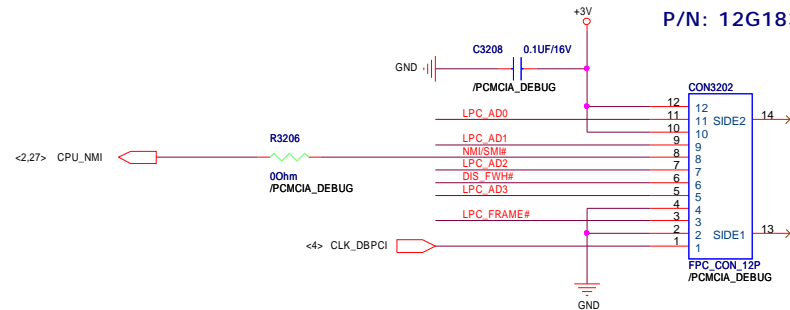


FWH



DEBUG PORT (CONNECT WITH FFC)

P/N: 12G183101206



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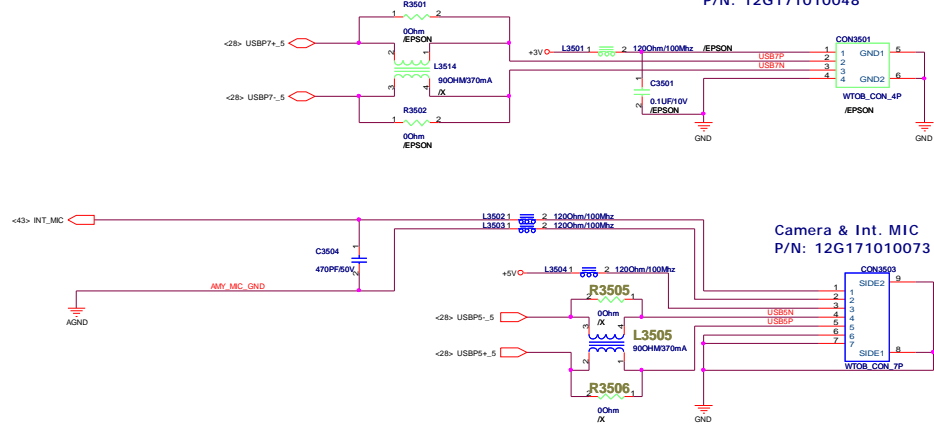
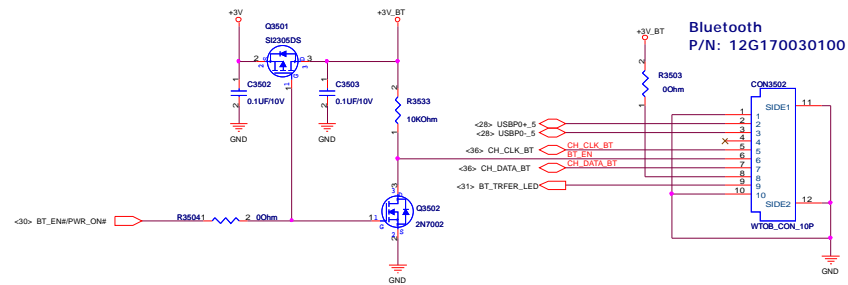
3

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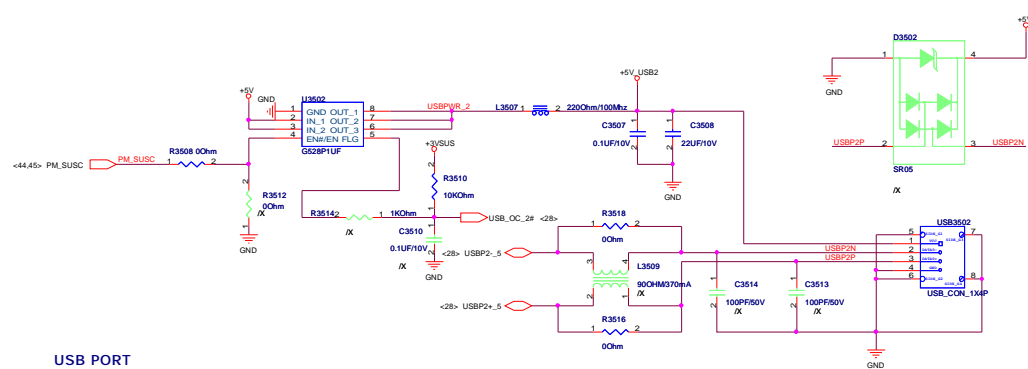
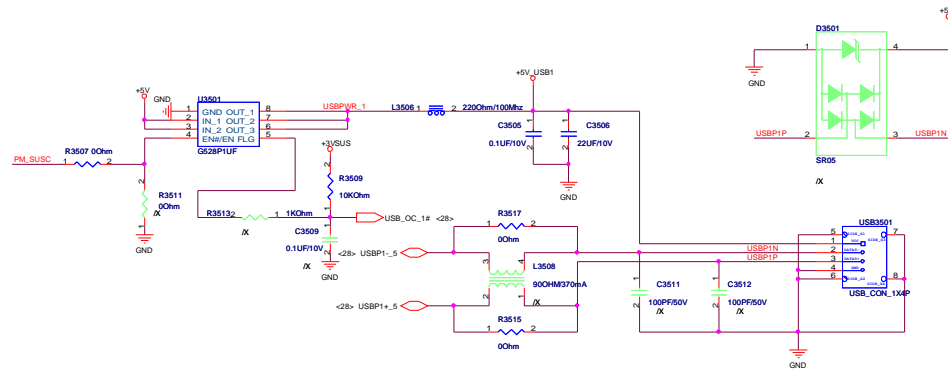
D

D



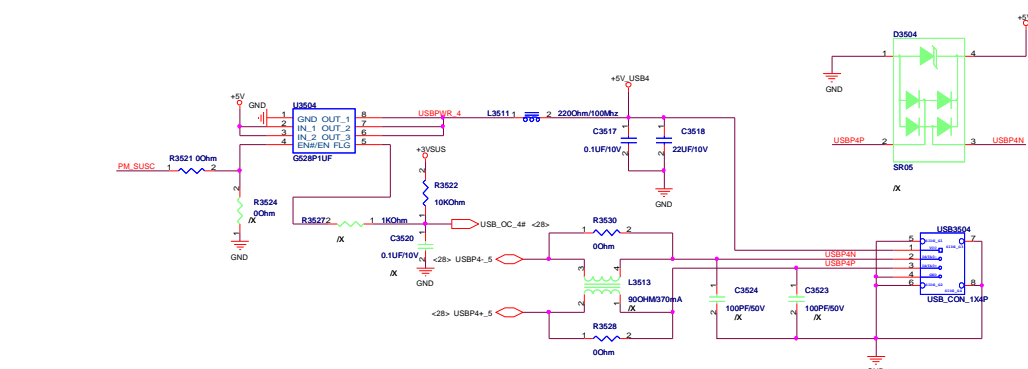
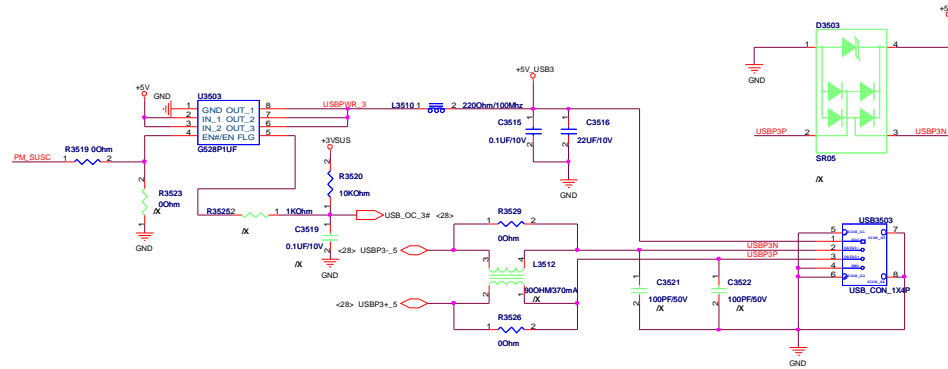
C

C



B

B



A

A

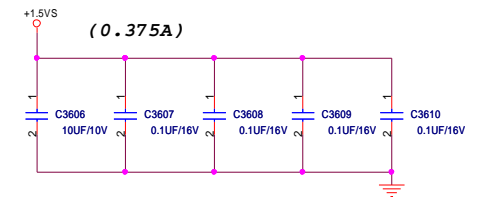
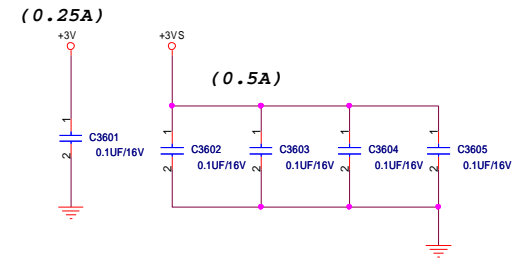
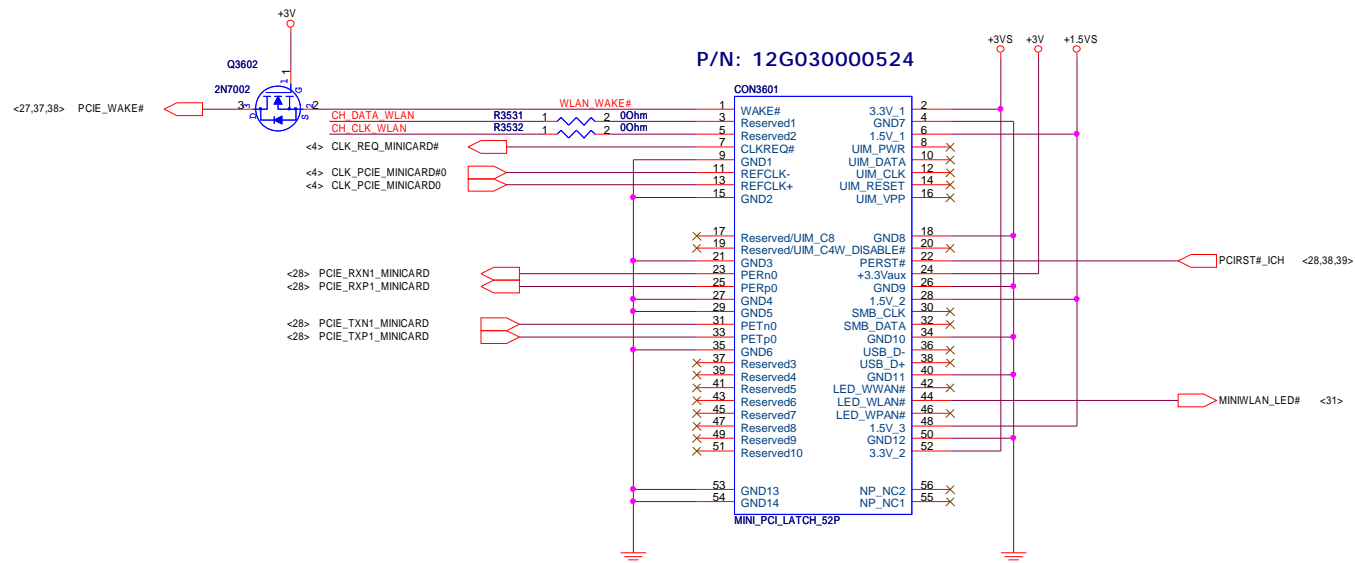
5

4

3

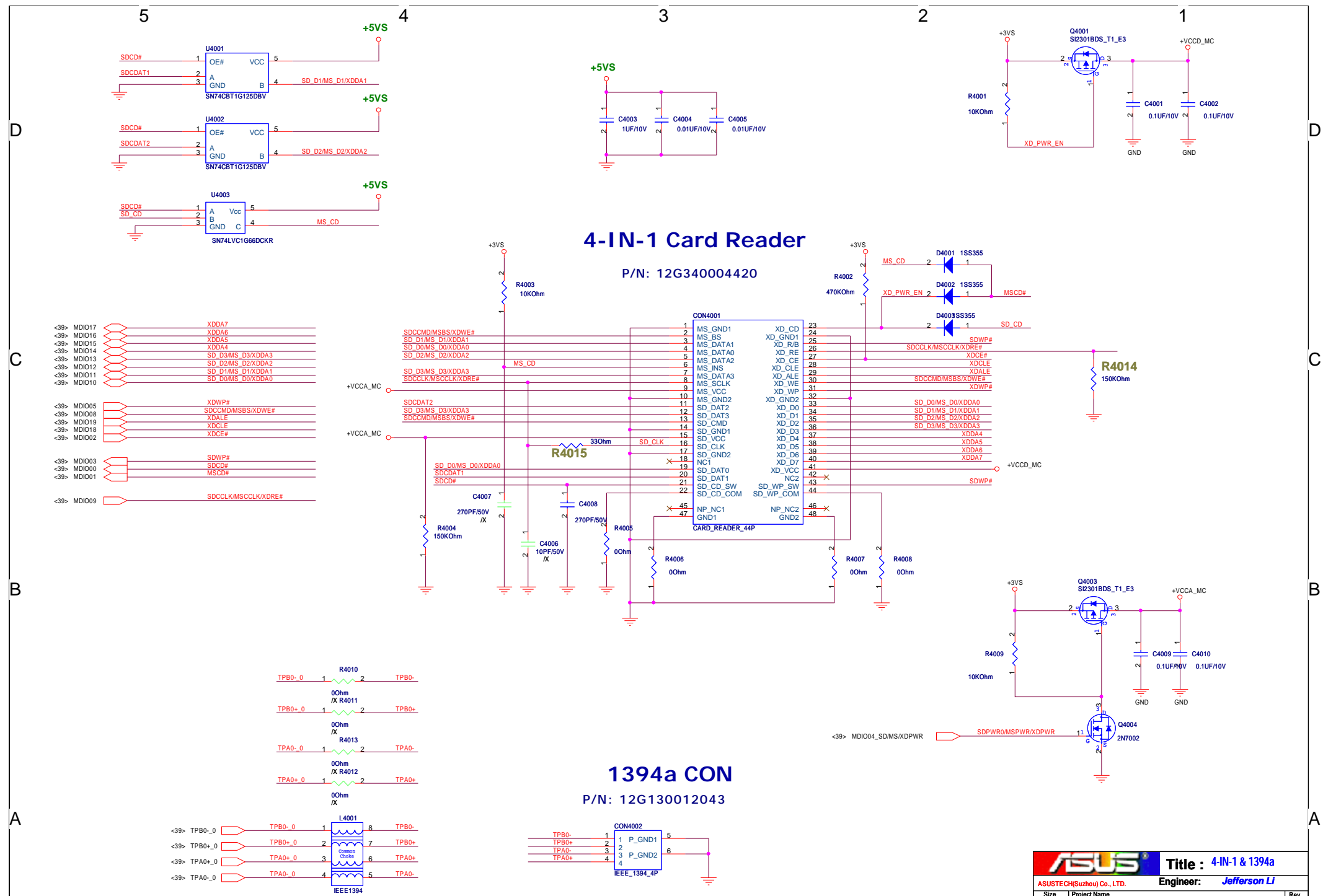
2

1



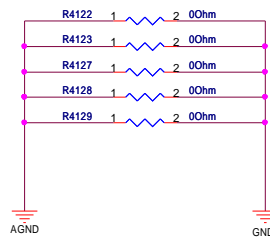
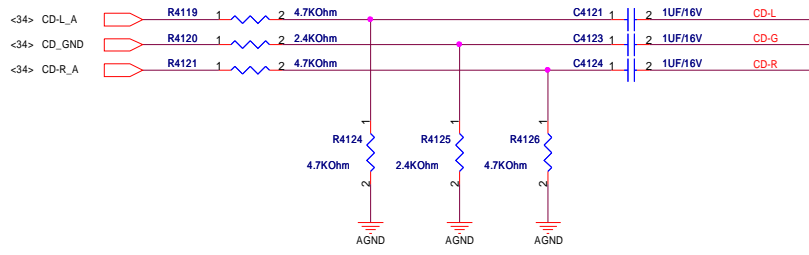
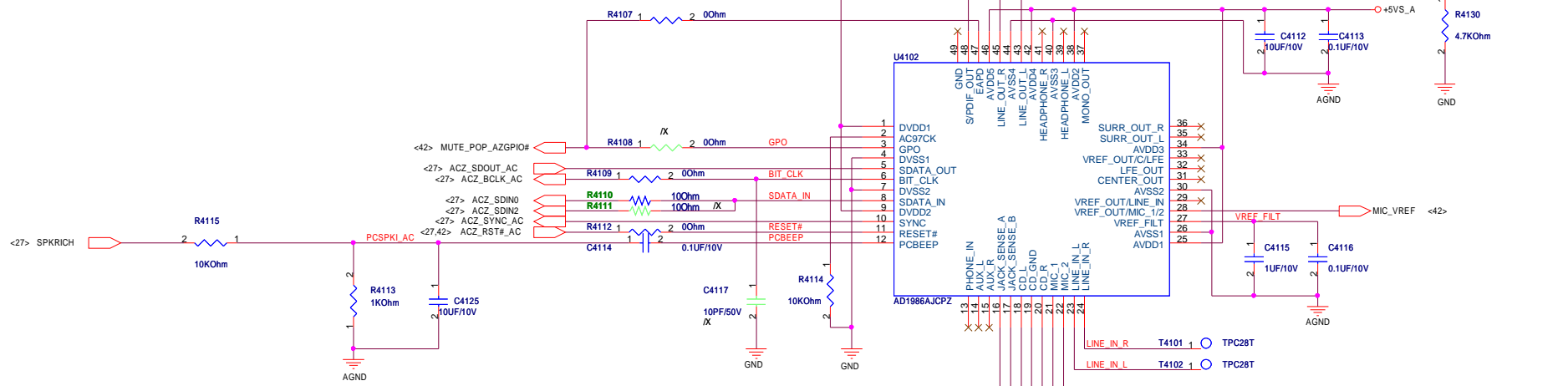
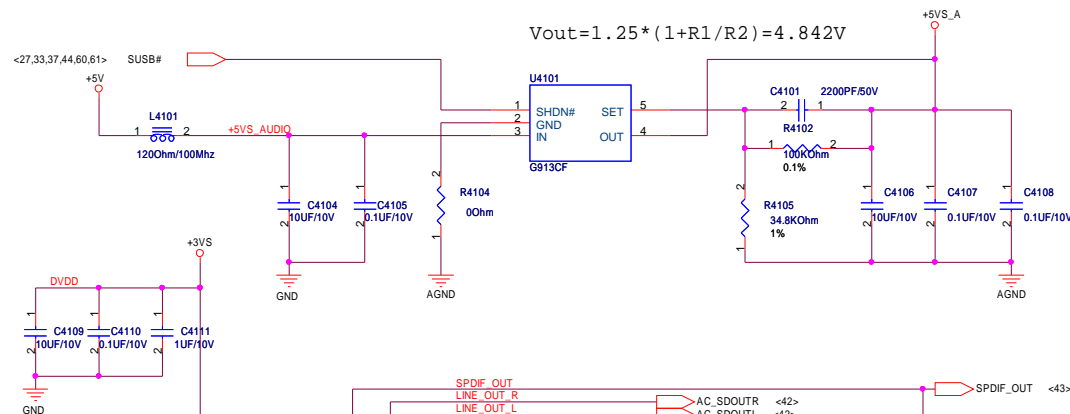
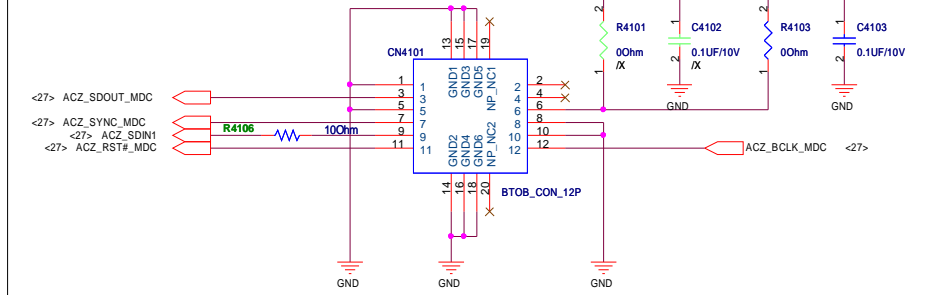


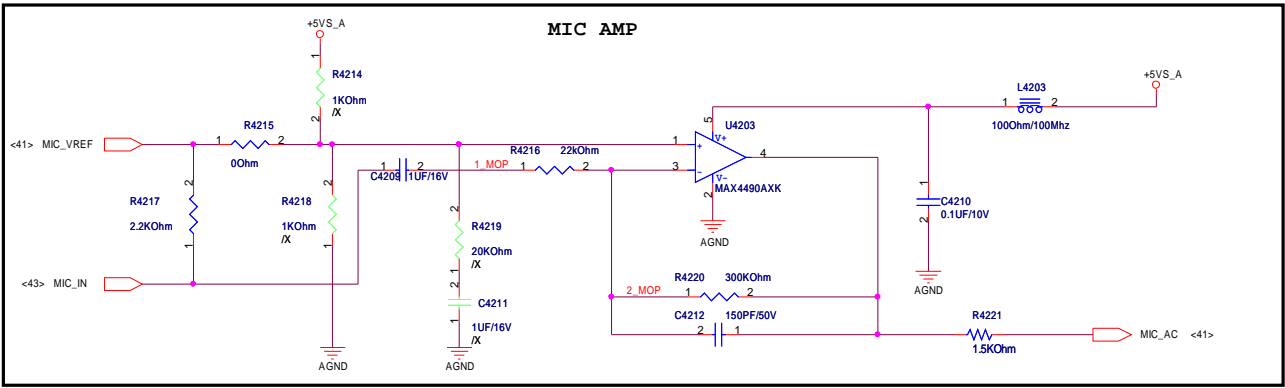
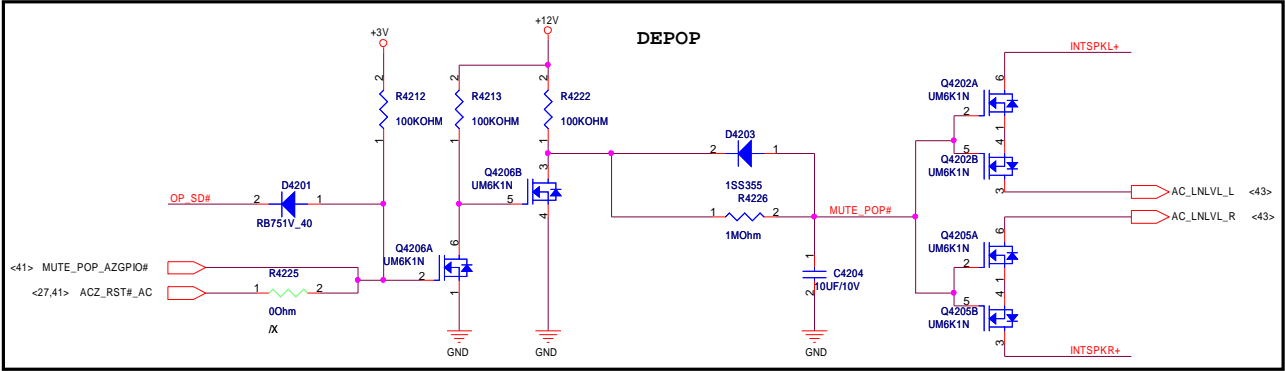
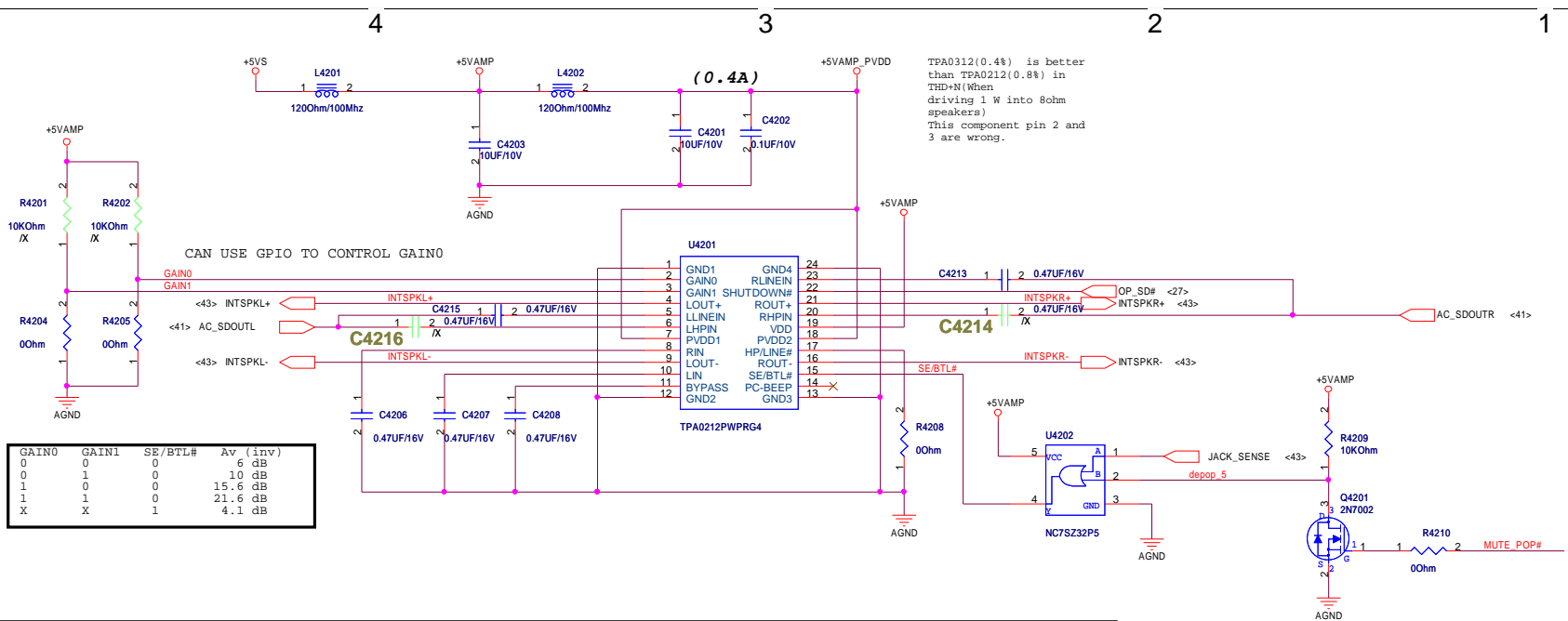


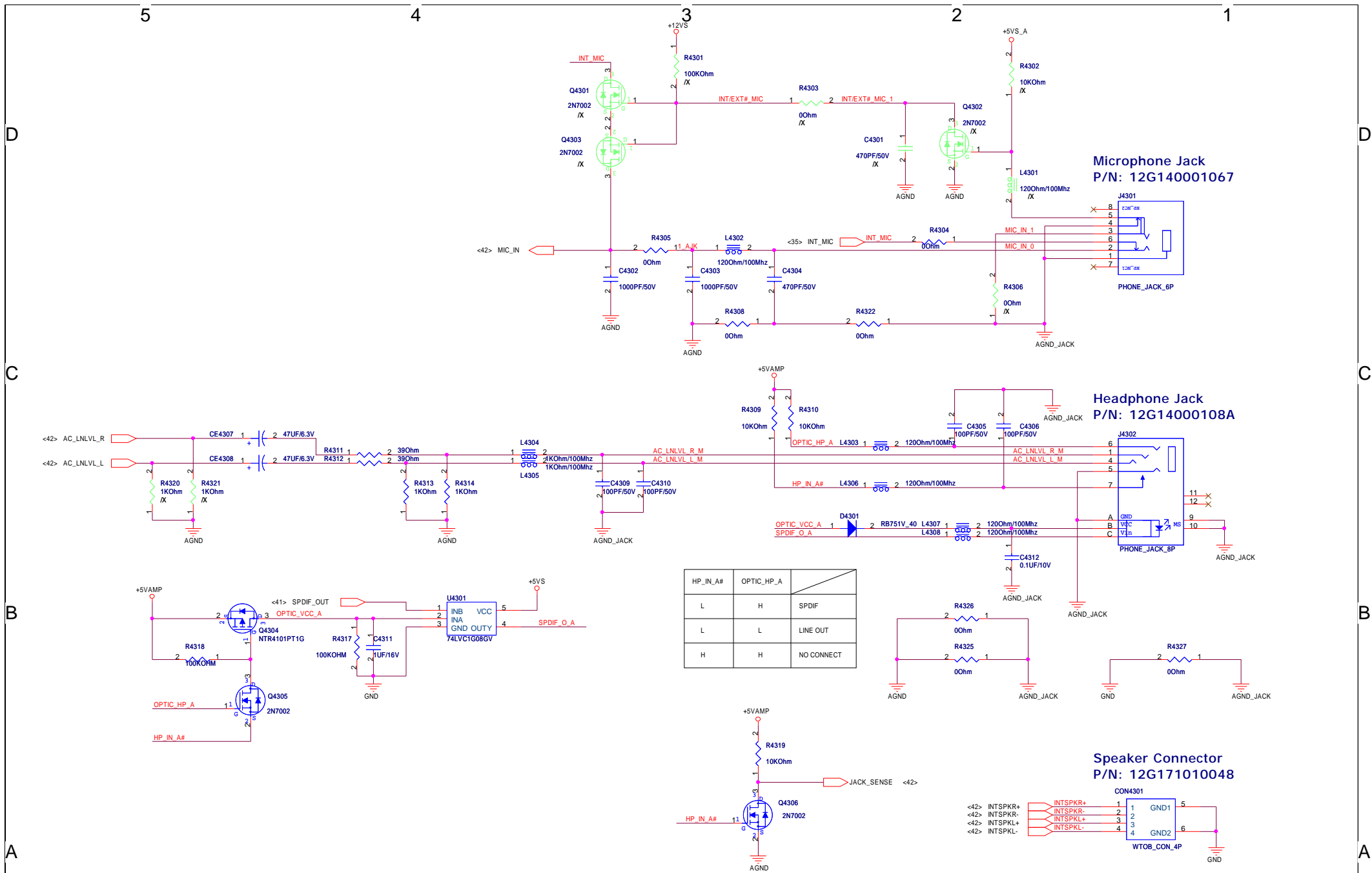


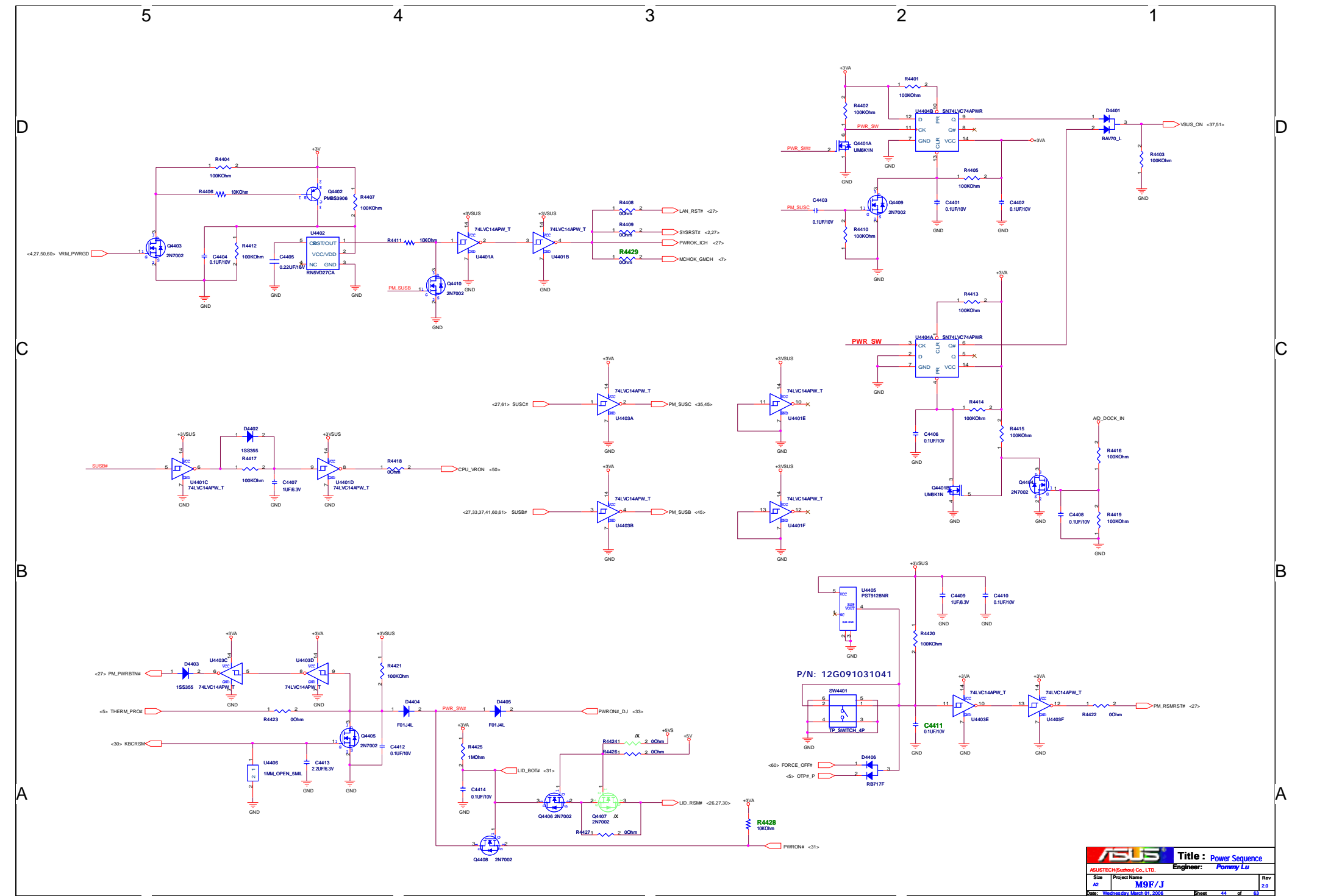
Modem CON

P/N: 12G161200120









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D

C

B

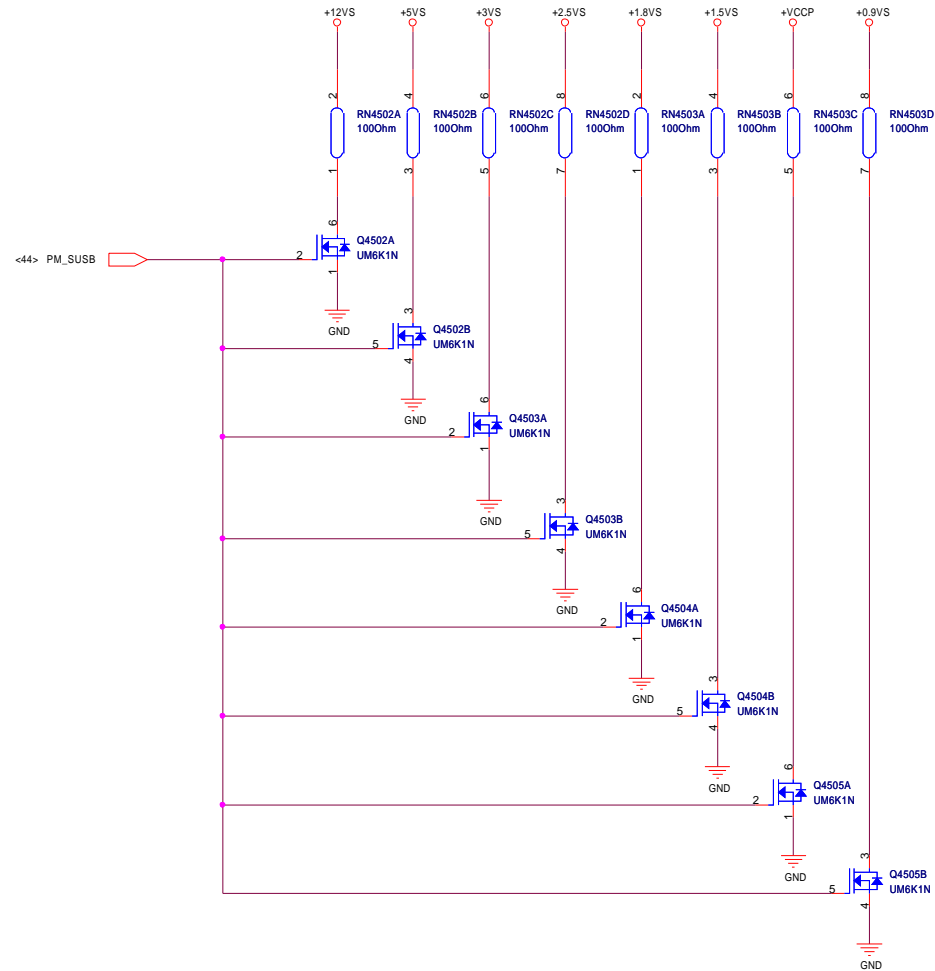
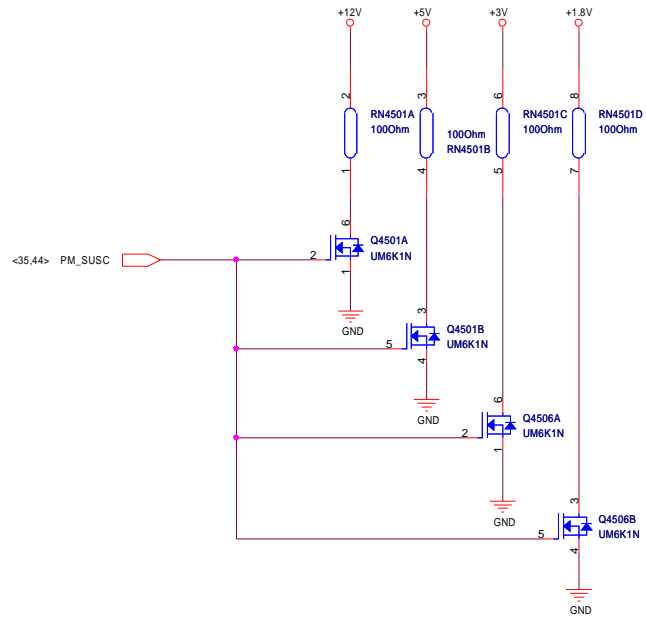
A

D

C

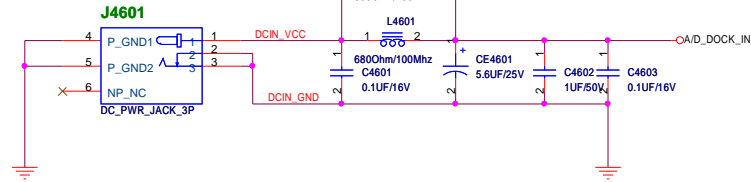
B

A



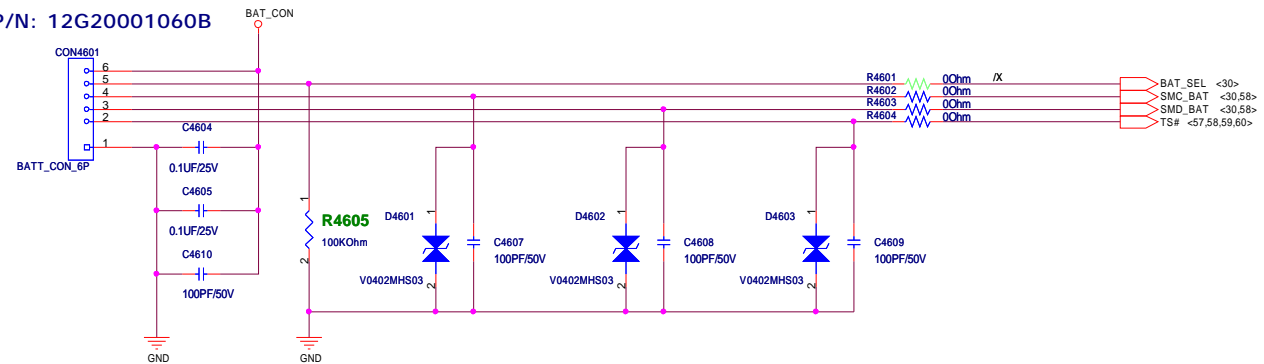
DC-IN

P/N: 12G14530103E



Battery-IN

P/N: 12G20001060B



		Title : DC-IN & BAT-IN	
ASUSTECH(Suzhou) Co., LTD.		Engineer: Pommy Lu	
Size	Project Name	Rev	
A3	M9F/J	2.0	
Date: Wednesday, March 01, 2006		Sheet	46 of 63

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E

F

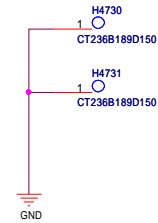
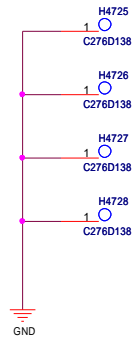
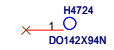
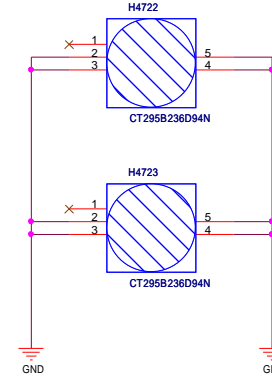
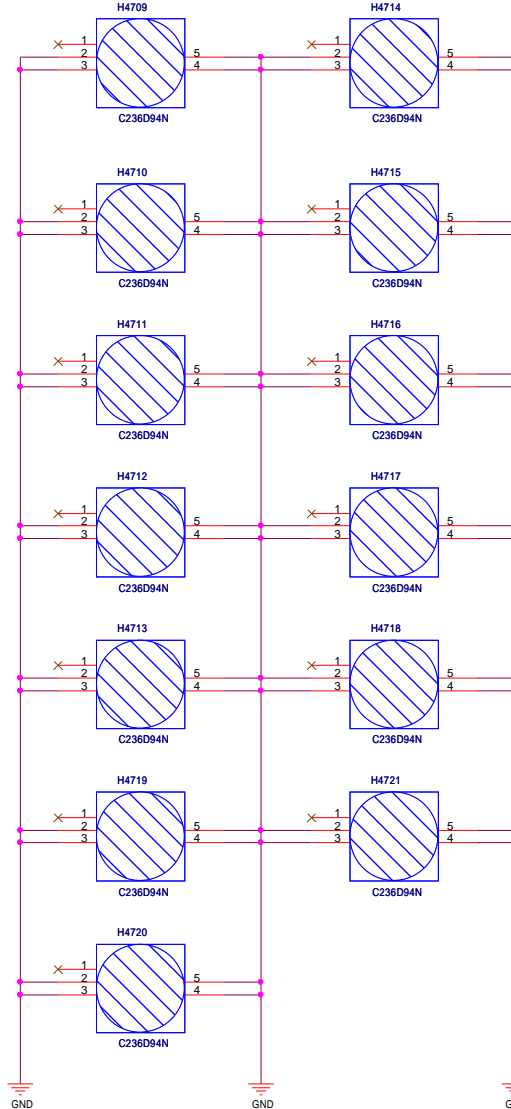
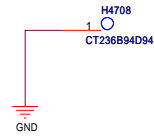
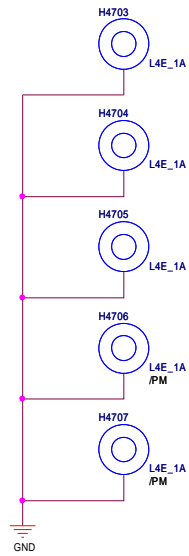
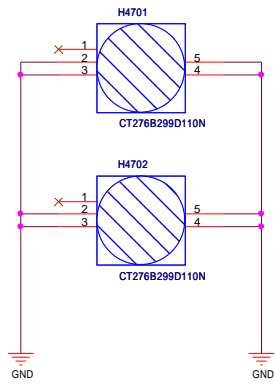
J

L

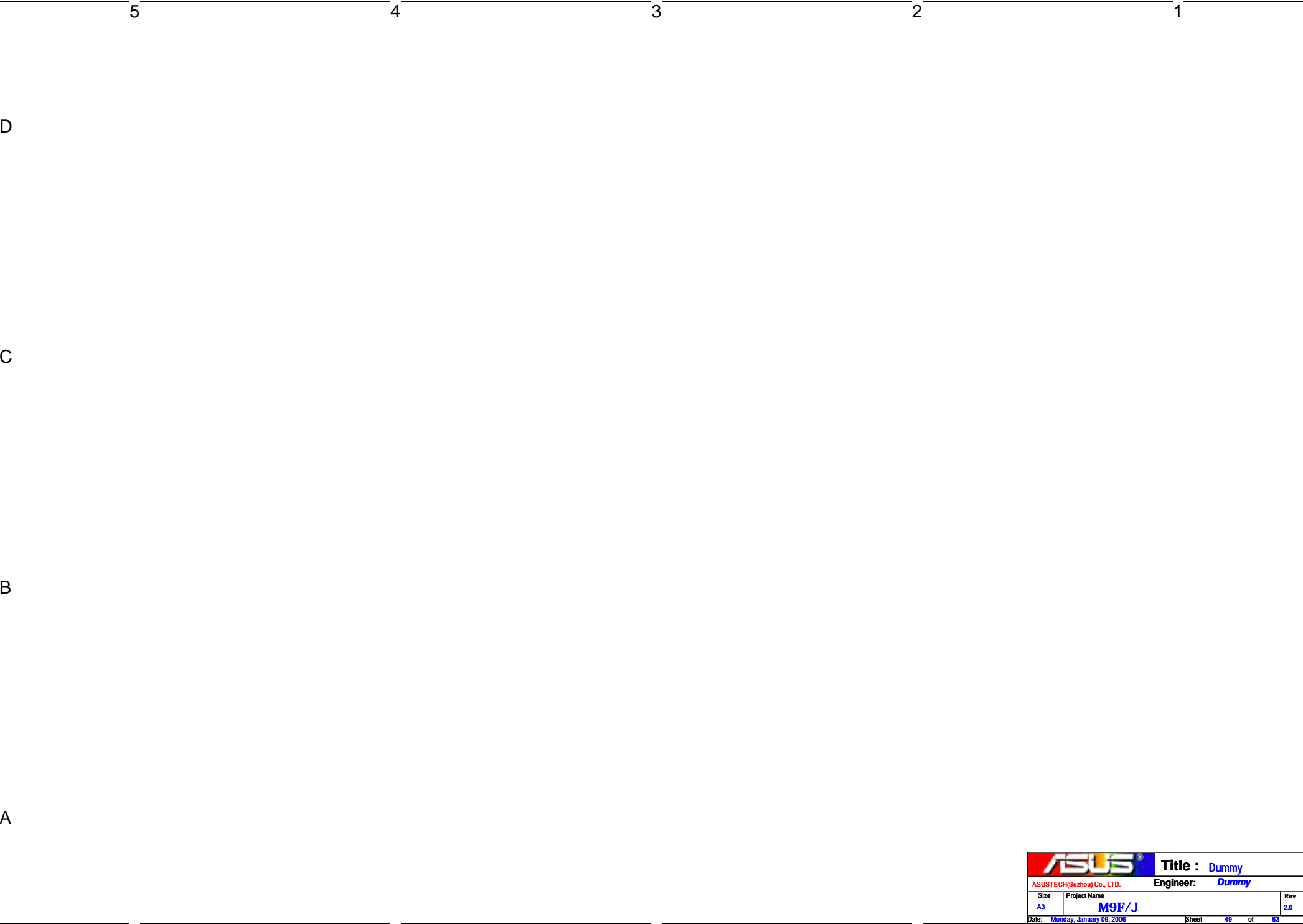
O

CPU Heat Sink Bracket Holes

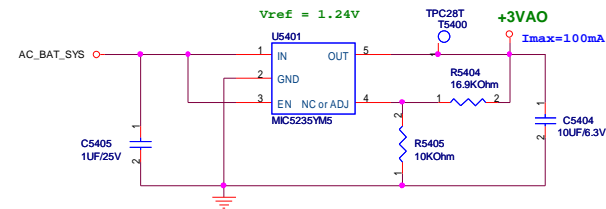
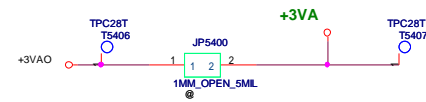
Mini Card Latch Nuts



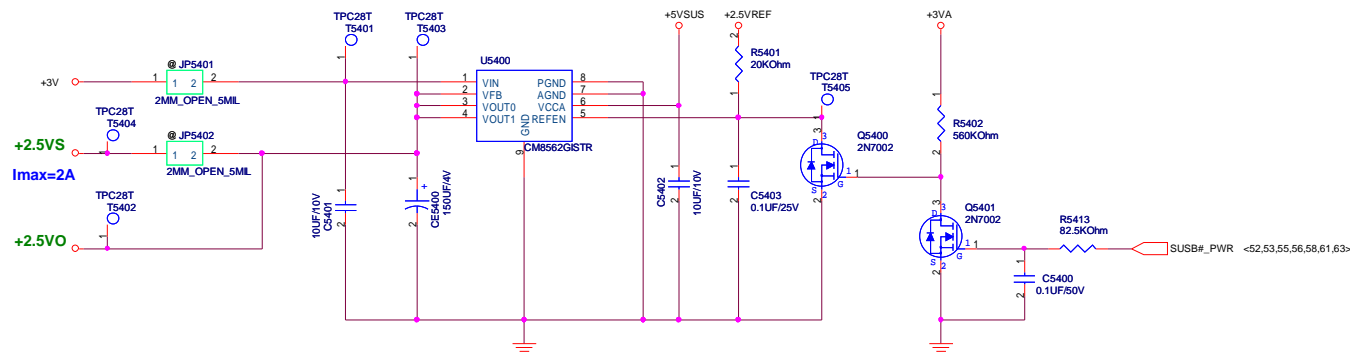
		Title : <i>Dummy</i>	
ASUSTECH(Suzhou) Co., LTD.		Engineer: <i>Dummy</i>	
Size	Project Name		Rev
A3	M9F/J		2.0
Date: <i>Monday, January 09, 2006</i>		Sheet	48 of 63

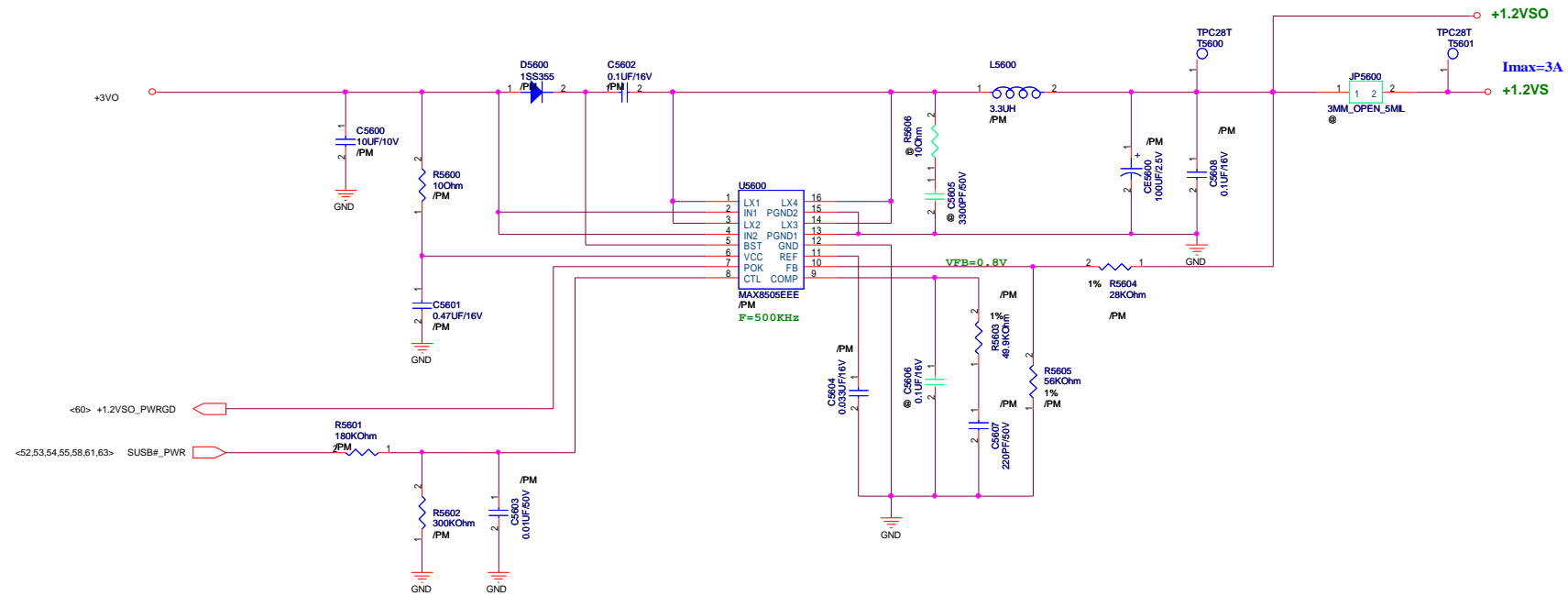


+3VAO

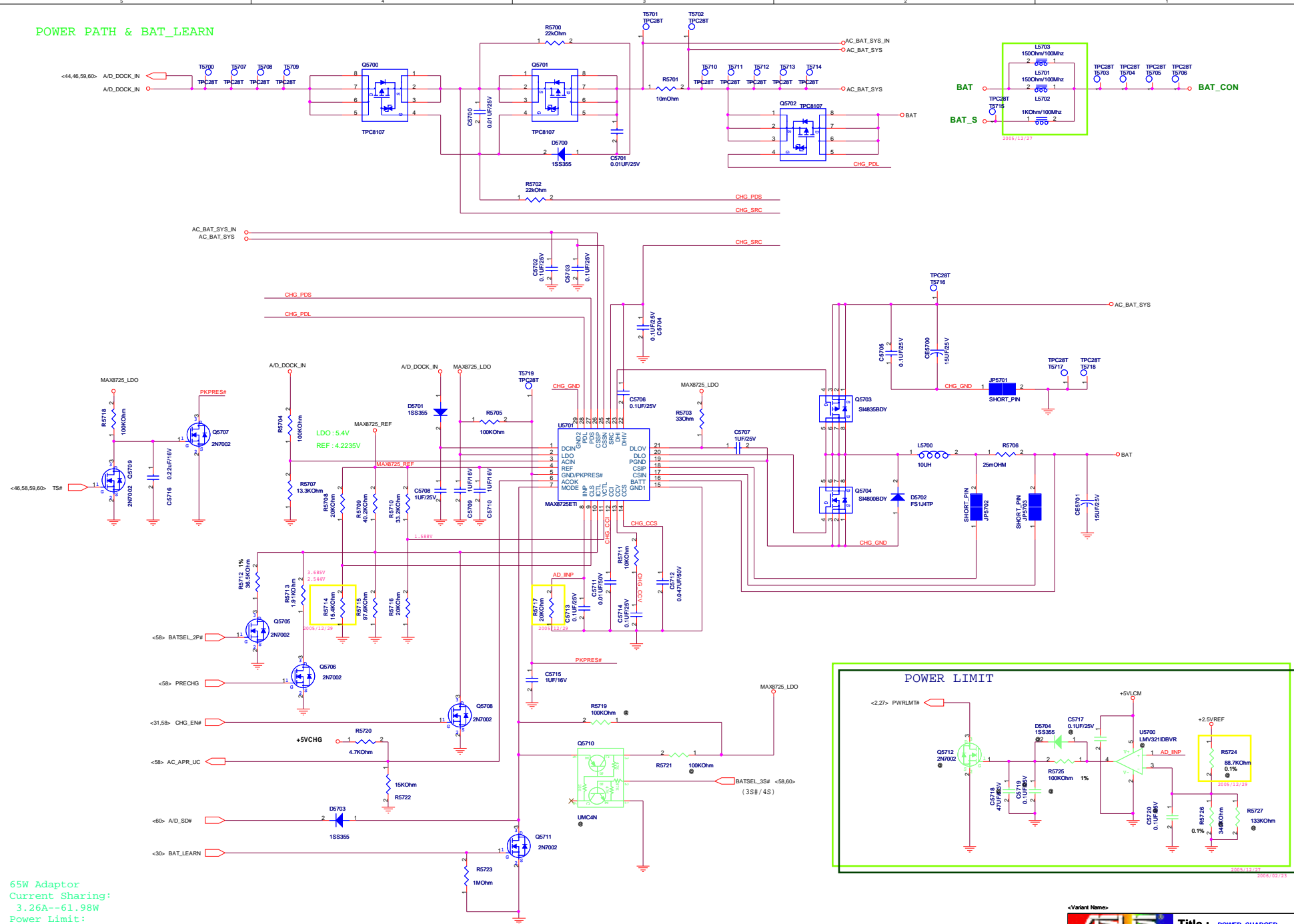


+2.5VS





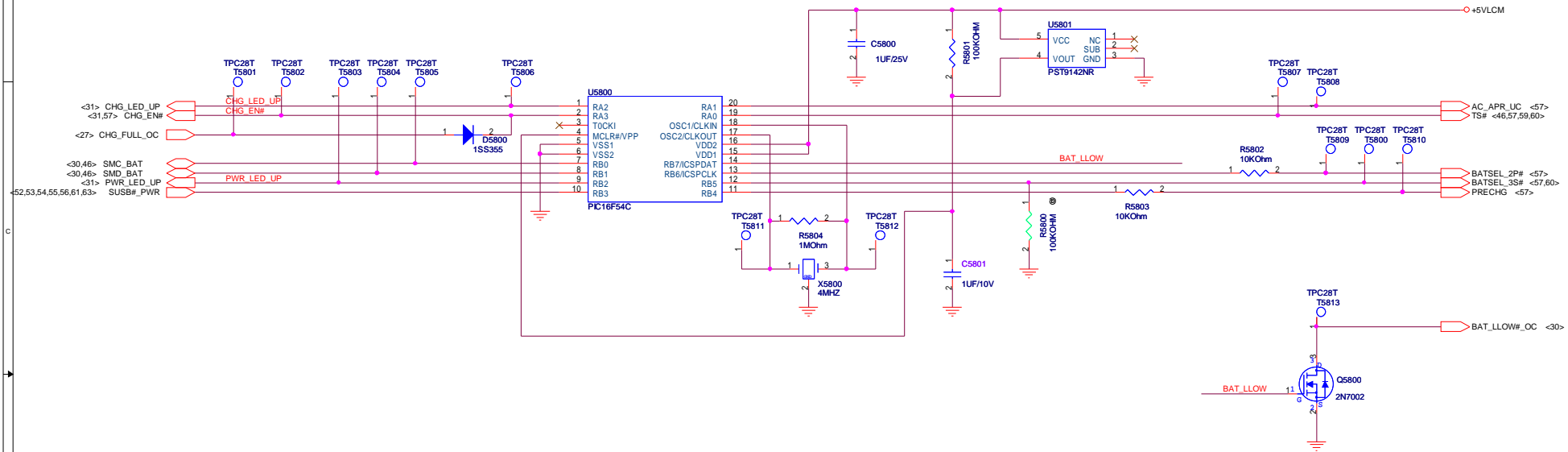
POWER PATH & BAT_LEARN



<Variant Name>

ASUS		Title : POWER_CHARGER	
<OrigName>		Engineer: Johnson	
Size	Project Name	Rev	
C	M0J	2.0	
Date: Wednesday, March 01, 2008		Sheet	67 of 63

PIC16F54C

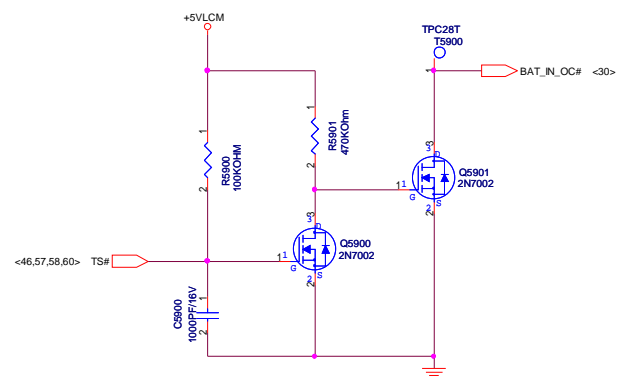


When BAT_LLOW#_OC is active, system entry 54

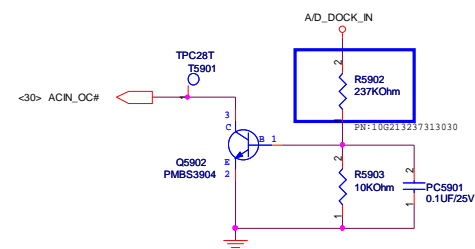
<Variant Name>

ASUS		Title : POWER_PIC	
<OrgName>		Engineer: Johnson	
Size	Project Name	Rev	
Custom	M9J	2.0	
Date: Wednesday, March 01, 2006	Sheet	58	of 63

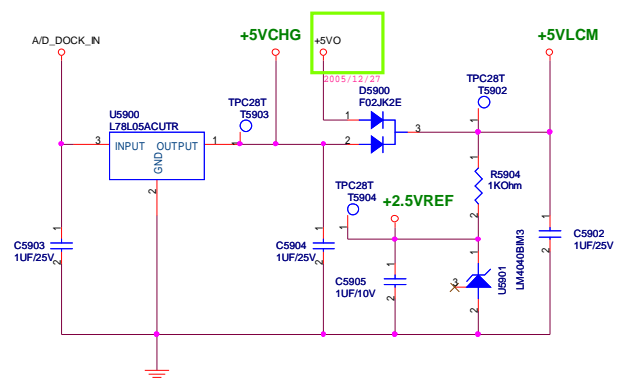
BATTERY IN DETECT



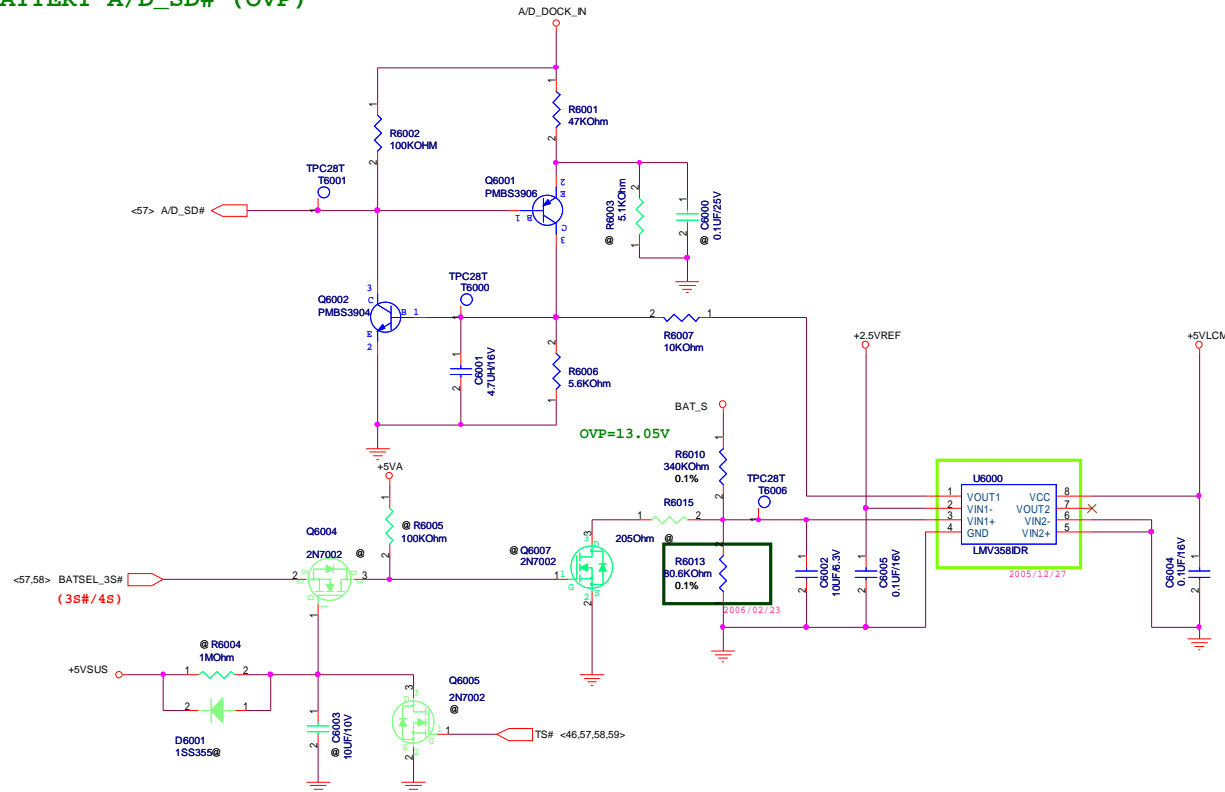
ADAPTER IN DETECT



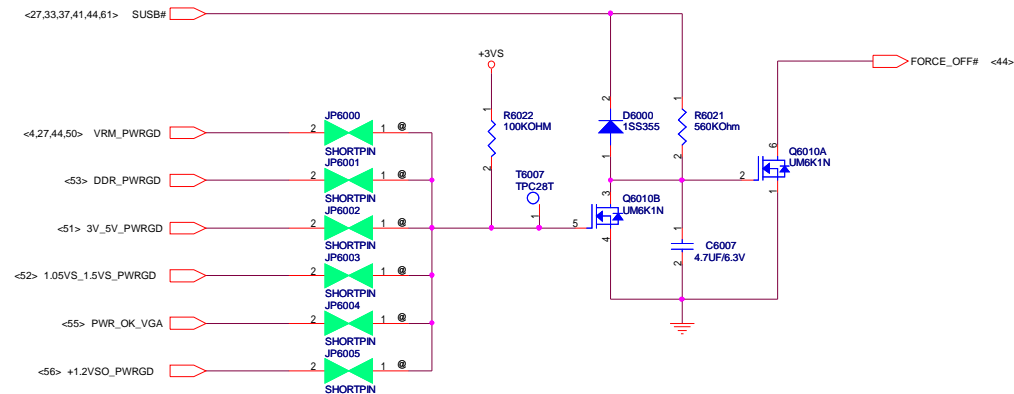
+5VLCM, +5VCHG & +2.5VREF



BATTERY A/D_SD# (OVP)



POWER GOOD DETECTOR

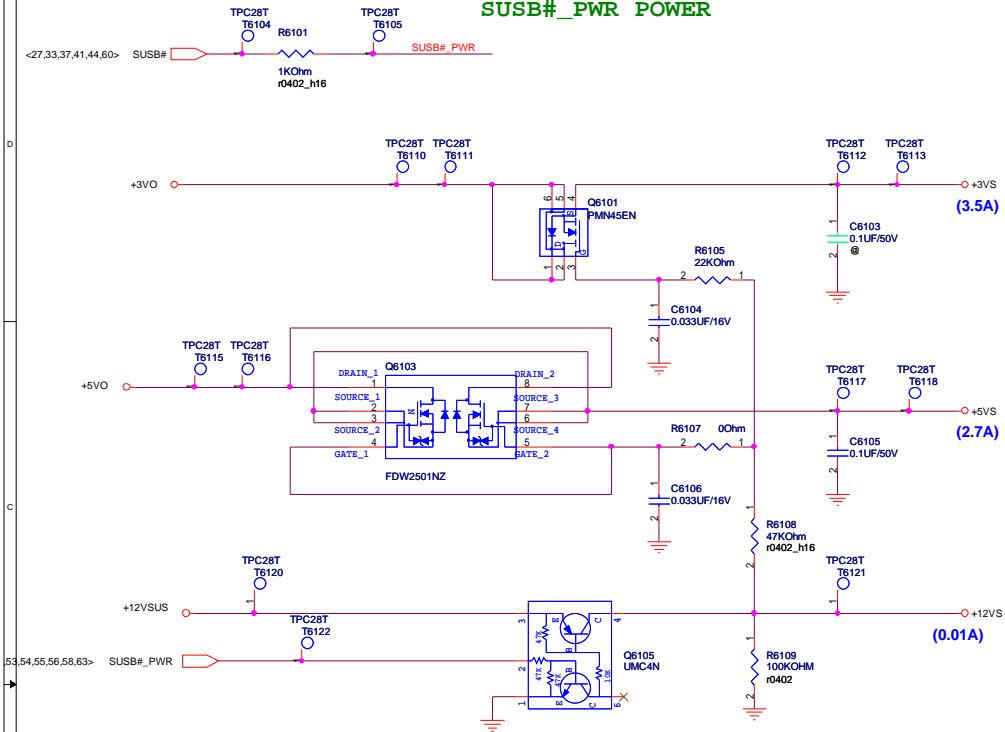


TPC28T T6002	1	VRM_PWRGD
TPC28T T6003	1	DDR_PWRGD
TPC28T T6004	1	3V_5V_PWRGD
TPC28T T6005	1	1.05VS_1.5VS_PWRGD

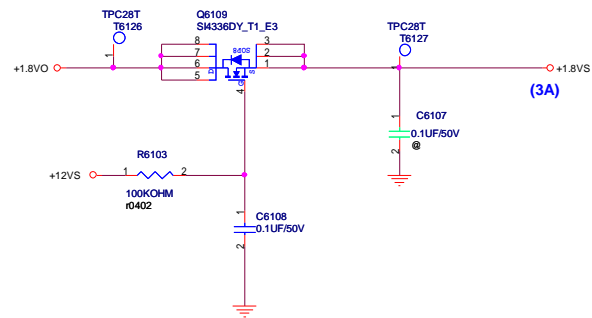
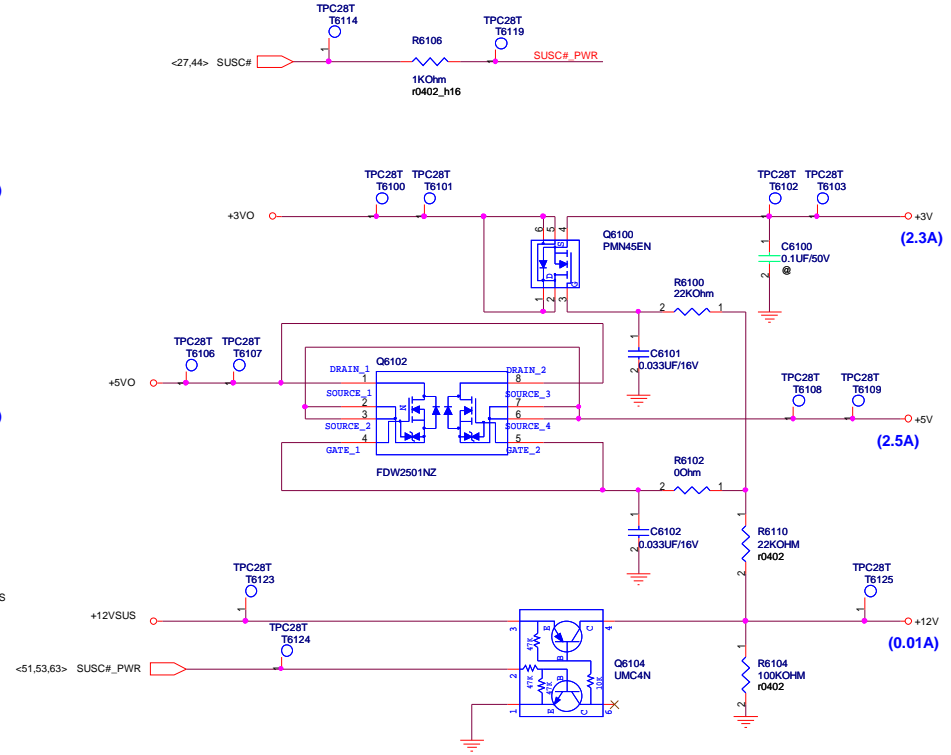
<Variant Name>

ASUS		Title : POWER_PROTECT	
<OrgName>		Engineer: <i>Johnson</i>	
Size	Project Name		Rev
Custom	M9J		2.0
Date: Wednesday, March 01, 2006		Sheet	60 of 63

SUSB#_PWR POWER



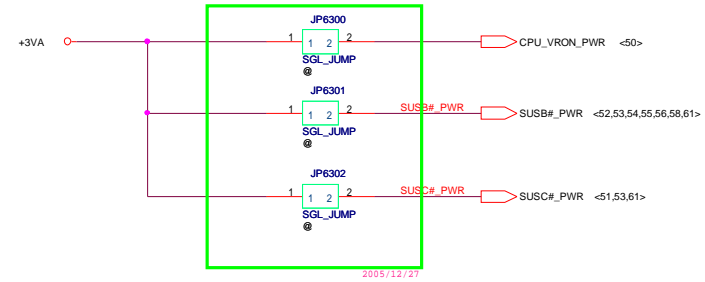
SUSC#_PWR POWER



<Variant Name>

ASUS		Title : POWER_LOAD SWITCH	
<OrgName>		Engineer: <i>Johnson</i>	
Size Custom	Project Name M9J	Rev 2.0	
Date: Wednesday, March 01, 2006		Sheet	61 of 63

FOR POWER TEST



MODIFY LIST

2000/02/23
1.Unmount Power Limit Circuit
2.Modify OVP Circuit
3.Change R6013 to 0.1% resistor

<Variant Name>

		Title : POWER_SIGNAL	
<OrgName>		Engineer: Johnson	
Size	Project Name		Rev
Custom	M9J		2.0
Date: Wednesday, March 01, 2006		Sheet	63 of 63