DJ1 Montevina UMA Schematics Document

uFCPGA Mobile Penryn

Intel GM45+ICH9M

2010-02-10

REV : A00

DY : Nopop Component

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: *DJ1 Montevina UMA*	Rev: *A00*
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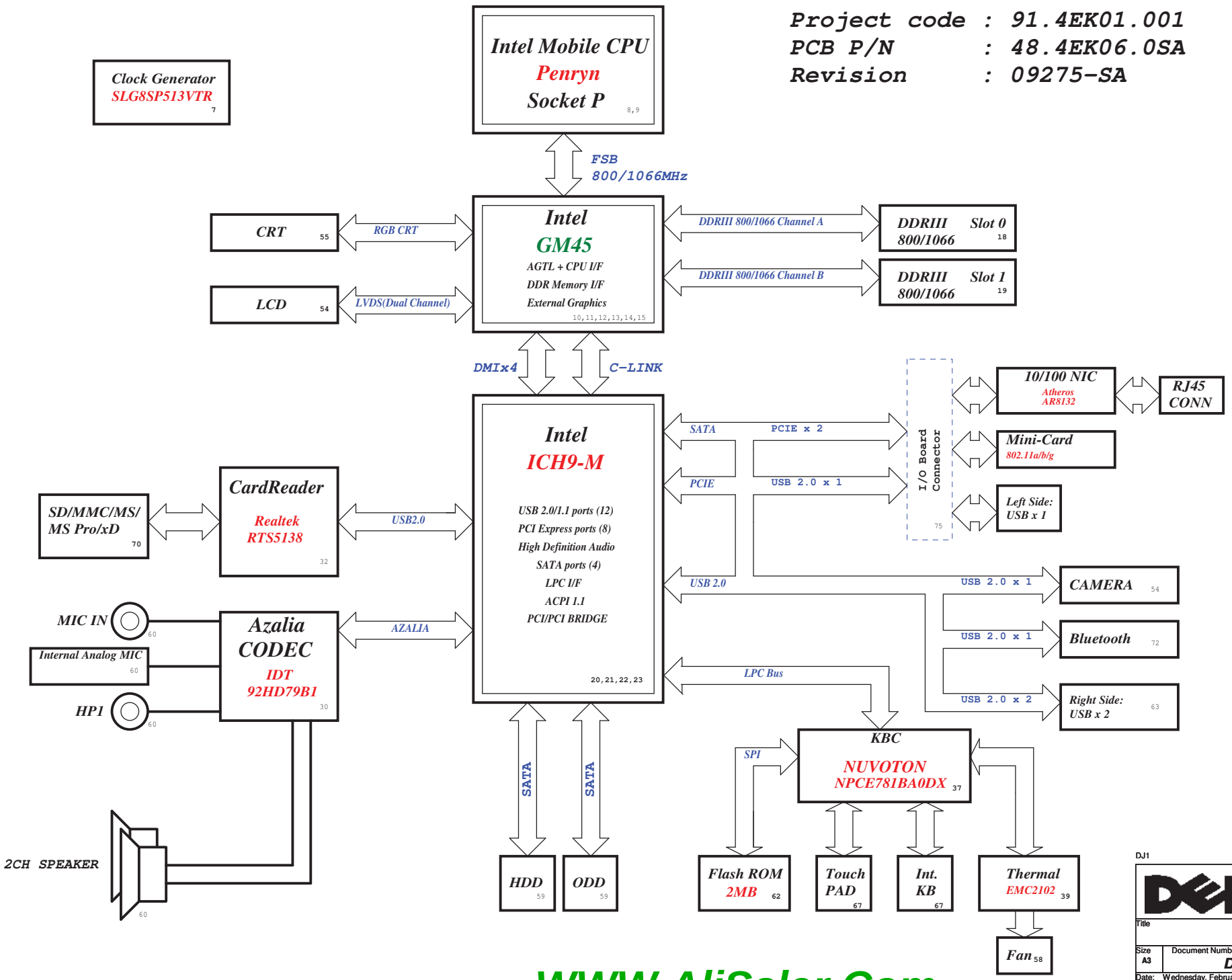
DJ1 Montevina UMA Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK06.0SA
Revision : 09275-SA



CPU DC/DC TPS51620 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC TPS51125 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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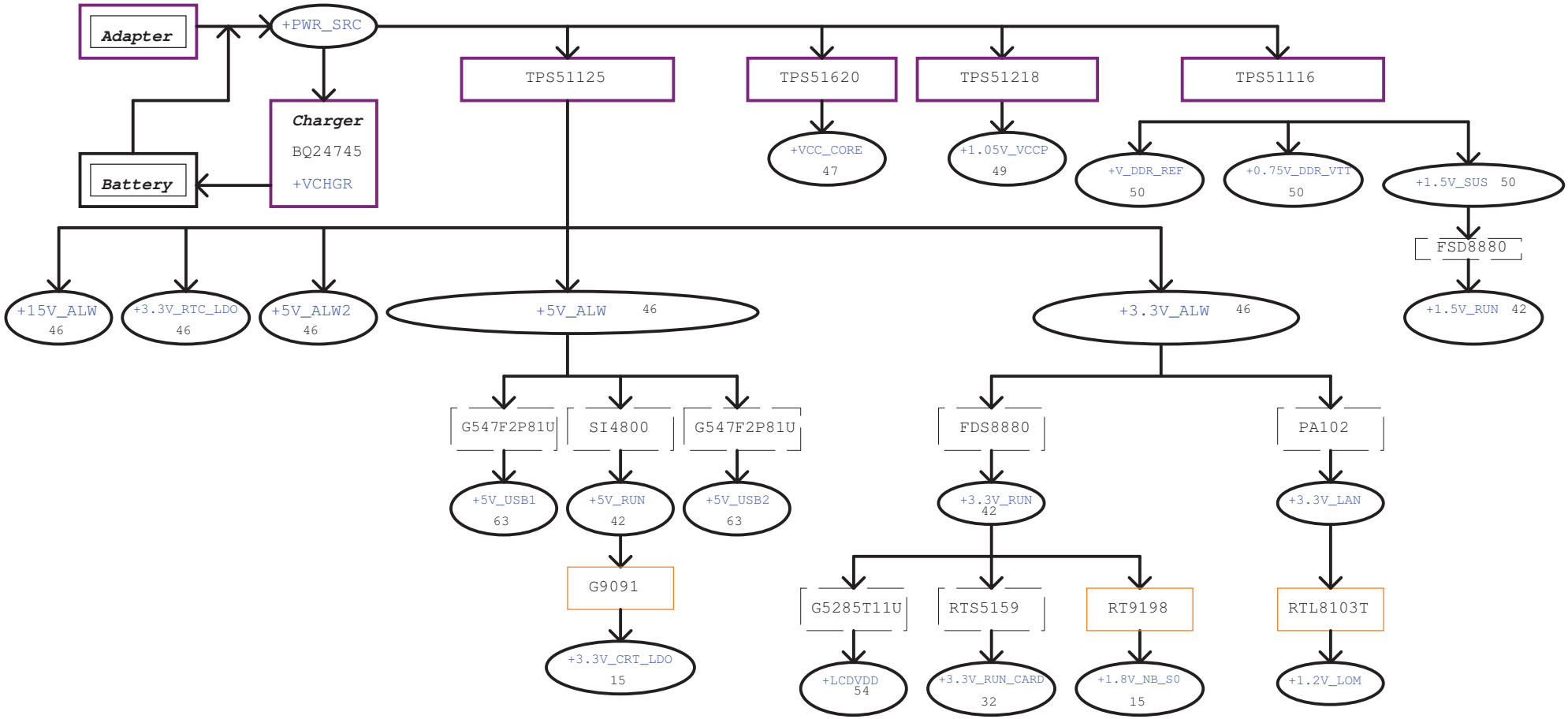
Title: Block Diagram

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 2 of 88

DJ1 Montevina UMA Power Block Diagram



Power Shape

Regulator | LDO | Switch

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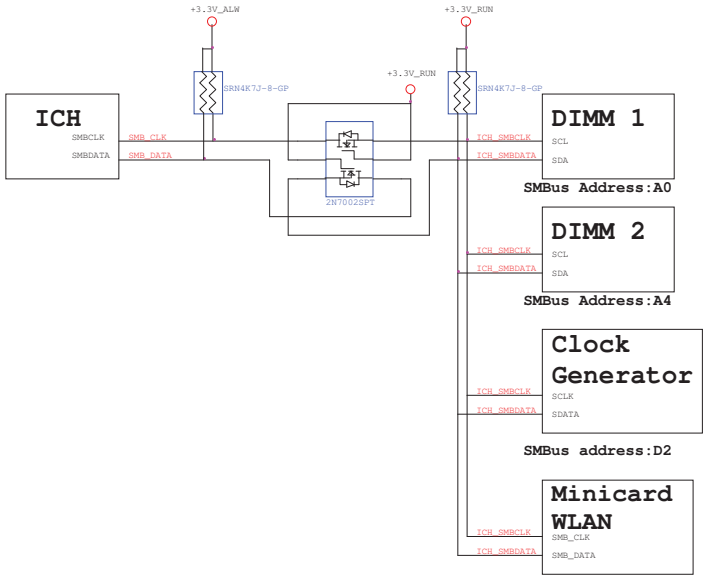
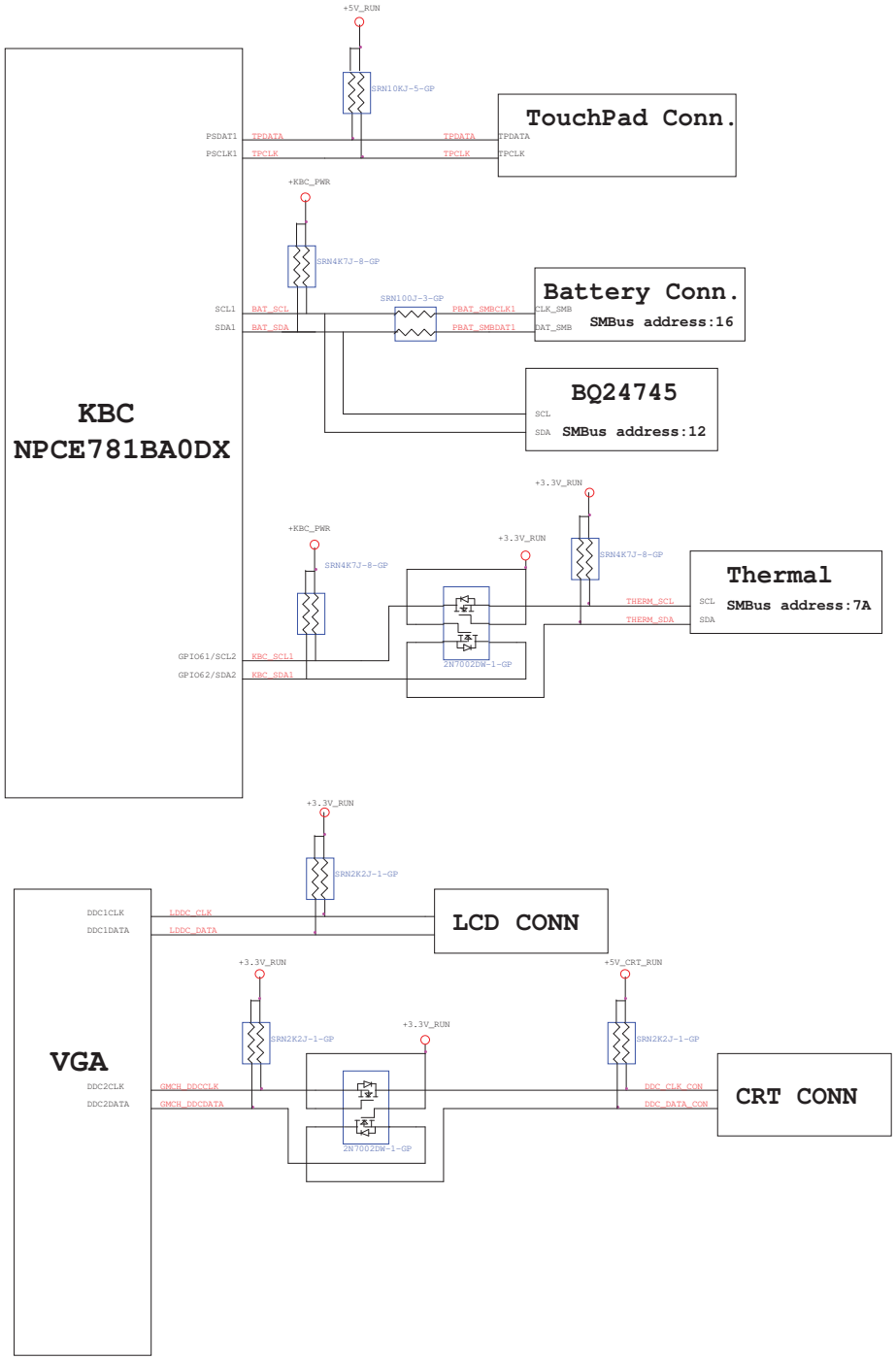
ICH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
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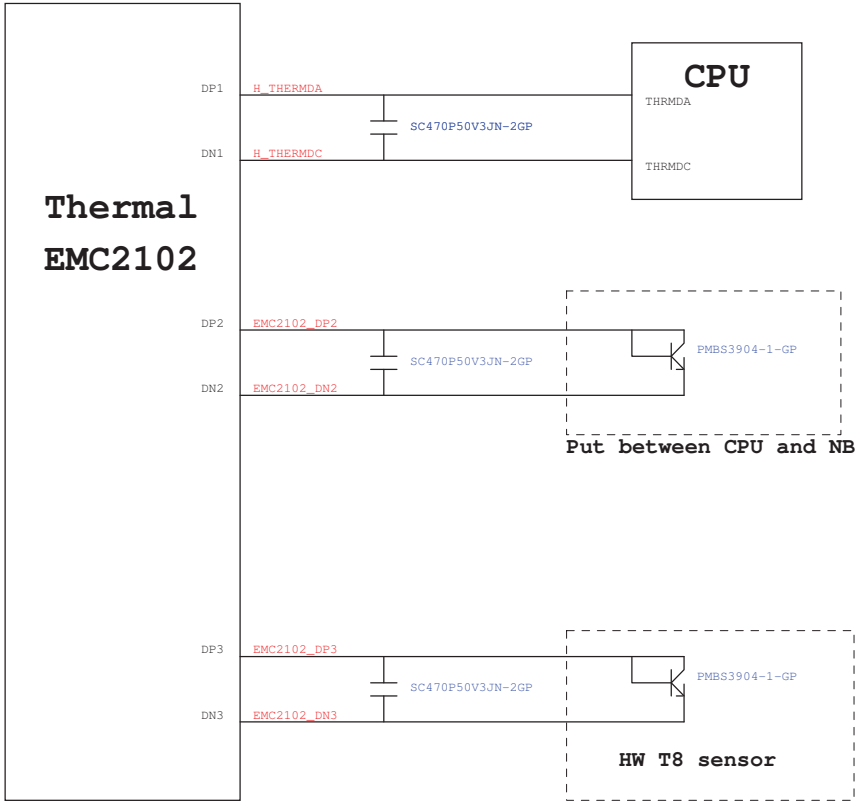
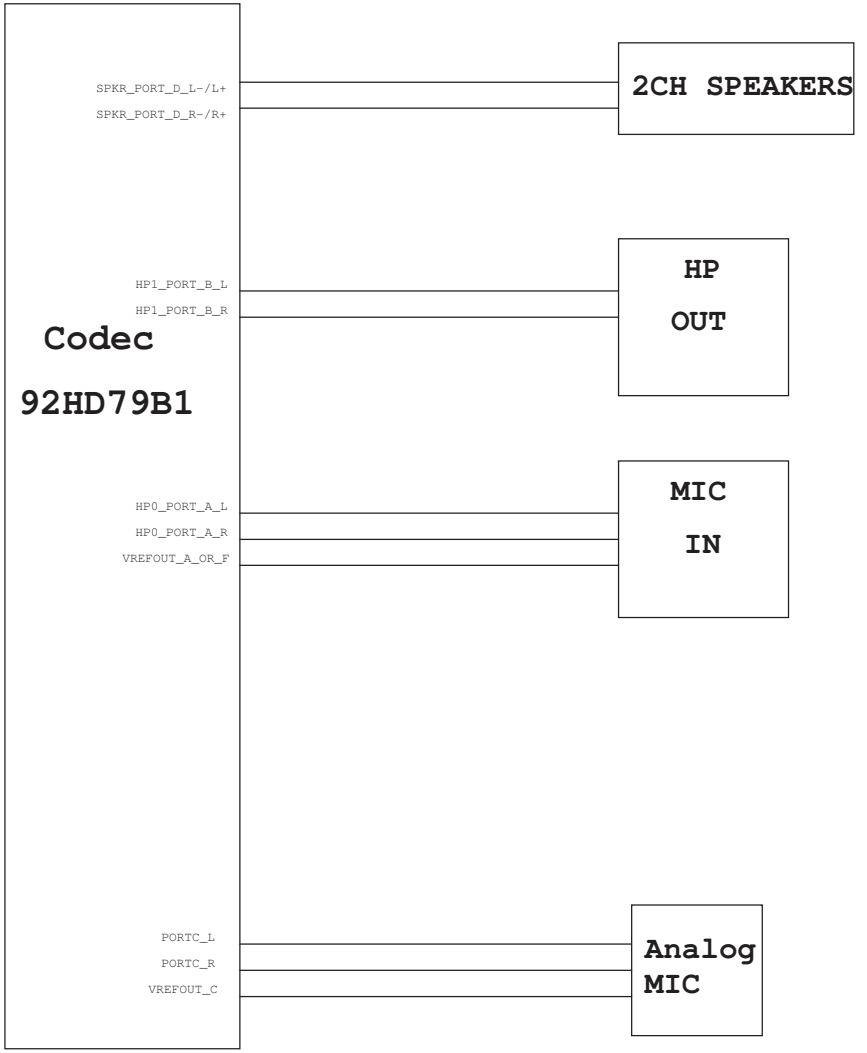
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.2.3

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance / PCI Express* Port Config 1 bit 1 (Port 1-4), Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset 224h).This signal has a weak internal pull-down.
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4), Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h)
GNT2#/ GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6), Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers:Offset 0224h) when sampled low.
GPIO20	Reserved, Rising Edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1#/ GPIO51	ESI Strap (Server Only), Rising Edge of PWROK.	Tying this strap low configures DMI for ESIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h: bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#	Boot BIOS Destination Selection 1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved
SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0, Rising Edge of CLPWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved
SATALED#	PCI Express Lane Reversal (Lanes 1-4). Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot, Rising Edge of PWROK.	Sampled high: this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN# (Mobile Only)	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. Sampled high: the security measures will be in effect. This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be high for mobile applications.
SPI_MOSI (Moble Only)	Integrated TPM Enable. Rising Edge of CLPWROK.	Sampled low: the Integrated TPM will be disabled. Sampled high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. NOTE: This signal is required to be floating or pulled low for desktop applications.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.2.3

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT0#, GNT[3:1]#/ GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LAD[3:0]# / FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ0	PULL-UP 20K
LDRQ1 / GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1# / GPIO58 (Desktop Only) / CLGPIO6 (Digital Office Only)	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP3	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

PCIE Routing

LANE1	
LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB Pair	Device
0	USB0 (I/O Board)
1	USB1 (I/O Board 17")
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 355648 Rev.2.3

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	ITPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	**0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality** **1 = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	**0 = Reverse Lanes, 15->0, 14->1 etc.** **1 = Normal operation (default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG12	ALLZ	0 =ALLZ mode enabled (Note 3) **1 = Disable (Default)**
CFG13	XOR	0 = XOR mode enabled (Note 3) **1 = Disable (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe	**0 = Only digital DisplayPort (SDVO/DP/HDMI) or PCIe is operational (default)** **1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port**
SDVO _CTRLDATA (Note4)	SDVO Present	0 = No SDVO/HDMI/DP interface disabled (default) 1 = SDVO/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled
DDPC _CTRLDATA (Note4)	Digital Display Present	**0 = Digital display (HDMI/DP) device absent (default)** **1 = Digital display (HDMI/DP) Device Present**
CFG4:3 CFG8 CFG11 CFG14 CFG15 CFG17 CFG18	Reserved	

NOTE:

1. All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
3. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
4. DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

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Title: Table of Content

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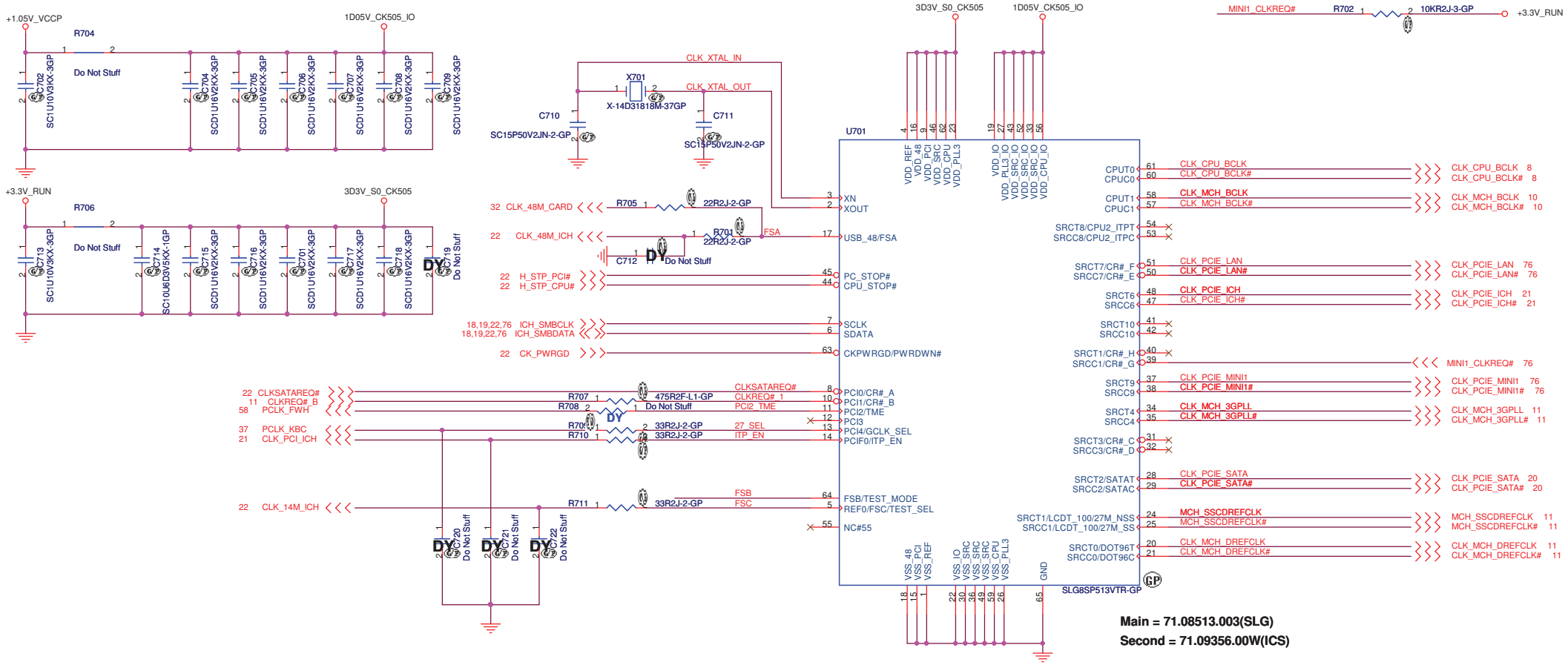
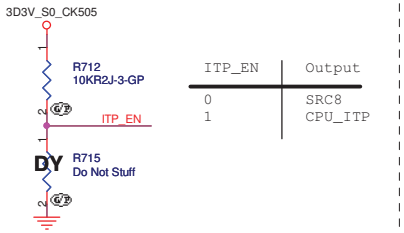
SSID = CLOCK

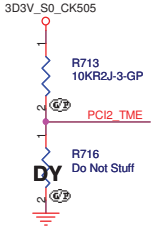


Main = 71.08513.003(SLG)

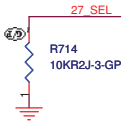
Second = 71.09356.00W(ICS)



ITP_EN	Output
0	SRC8
1	CPU_ITP

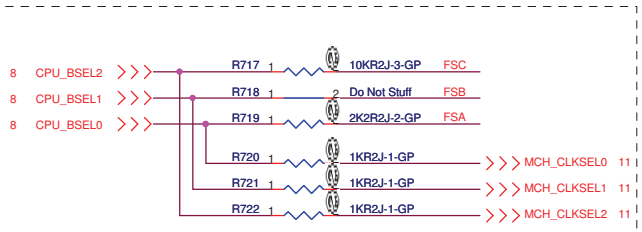


PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed



27_SEL	PIN20/21	PIN24/25
0	96M	100M
1	100M	27M

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



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Title: Clock Generator SLG8SP513VTR

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SSID = CPU

CPU1A 1 OF 4

TP801

H_A#[35..3] ← 10 H_A#[35..3]

ADDR GROUP 0: A3#, A4#, A5#, A6#, A7#, A8#, A9#, A10#, A11#, A12#, A13#, A14#, A15#, A16#, ADSTB0#

REQ0#, REQ1#, REQ2#, REQ3#, REQ4#

10 H_ADSTB#0

10 H_REQ#[4..0]

ADDR GROUP 1: A17#, A18#, A19#, A20#, A21#, A22#, A23#, A24#, A25#, A26#, A27#, A28#, A29#, A30#, A31#, A32#, A33#, A34#, A35#, ADSTB1#

10 H_ADSTB#1

ICH: A20M#, FERR#, IGNNE#, STPCLK#, LINT0, LINT1, SMI#

20 H_A20M#
20 H_FERR#
20 H_IGNNE#
20 H_STPCLK#
20 H_INTR
20 H_NMI
20 H_SMI#

RESERVED: RSVD#M4, RSVD#N5, RSVD#T2, RSVD#V3, RSVD#B2, TEST7, RSVD#D2, RSVD#D22, RSVD#D3, RSVD#F6, KEY_NC

TP802 RSVD_CPU_1 M4
TP803 RSVD_CPU_2 N5
TP804 RSVD_CPU_3 T2
TP805 RSVD_CPU_4 V3
TP806 RSVD_CPU_5 B2
TP807 RSVD_CPU_6 C3
TP808 RSVD_CPU_7 D2
TP809 RSVD_CPU_8 D22
TP810 RSVD_CPU_9 D3
TP811 RSVD_CPU_10 F6
TP812 RSVD_CPU_11 B1

BGA479-SKT6-GPU7
62.10079.001

CONTROL: ADS#, BNR#, BPRI#, DEFER#, DRDY#, DBSY#, BR0#, IERR#, INIT#, LOCK#, RESET#, RS0#, RS1#, RS2#, TRDY#, HIT#, HITM#

H_ADS# 10
H_BNR# 10
H_BPRI# 10
H_DEFER# 10
H_DRDY# 10
H_DBSY# 10
H_BREQ#0 10
CPU_IERR# R802 1 56R2J-4-GP +1.05V_VCCP
H_INIT# 20
H_LOCK# 10
H_CPURST# 10
H_RS#[2..0] 10
H_TRDY# 10
H_HIT# 10
H_HITM# 10

XDP/ITP SIGNALS: BPM0#, BPM1#, BPM2#, BPM3#, PRDY#, PREQ#, TCK, TDI, TDO, TMS, TRST#, DBR#

ITP_BPM#5
ITP_TCK
ITP_TDI
ITP_TDO
ITP_TMS
ITP_TRST#
ITP_DBRESET#

THERMAL: PROCHOT#, THRMDA, THRMDC, THERMTRIP#

R803 1 DY Do Not Stuff CPU_PROCHOT# 47
R804 1 56R2J-4-GP +1.05V_VCCP
H_THERMDA 39
H_THERMDC 39
R805 1 DY Do Not Stuff +1.05V_VCCP
H_THRMTRIP# 11,20,37,42

HCLK: BCLK0, BCLK1

CLK_CPU_BCLK 7
CLK_CPU_BCLK# 7

H_THERMDA
DY C849 Do Not Stuff
H_THERMDC

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

H_THRMTRIP# should connect to
ICH9 and MCH without T-ing.

+1.05V_VCCP
R806 1KR2F-3-GP
CPU_GTLREF0
R812 2KR2F-3-GP
C801 SC1KP50V2KX-1GP

Layout notes
Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

ITP_TMS R816 1 51R2F-2-GP +1.05V_VCCP
ITP_TDI R817 1 51R2F-2-GP
ITP_BPM#5 R818 1 51R2F-2-GP
ITP_TDO R801 1 DY Do Not Stuff
ITP_DBRESET# R825 1 DY 2 Do Not Stuff +3.3V_RUN
ITP_TCK R819 1 51R2F-2-GP
ITP_TRST# R820 1 51R2F-2-GP
All place within 2" to CPU

H_DINV#[3..0] H_DINV#[3..0] 10
H_DSTBN#[3..0] H_DSTBN#[3..0] 10
H_DSTBP#[3..0] H_DSTBP#[3..0] 10
H_D#[63..0] H_D#[63..0] 10

CPU1B 2 OF 4

DATA GRP2: D0#, D1#, D2#, D3#, D4#, D5#, D6#, D7#, D8#, D9#, D10#, D11#, D12#, D13#, D14#, D15#, DSTBN0#, DSTBP0#, DINV0#

H_D#0 F22
H_D#1 F24
H_D#2 F26
H_D#3 G22
H_D#4 F23
H_D#5 G25
H_D#6 E25
H_D#7 E23
H_D#8 K24
H_D#9 G24
H_D#10 J24
H_D#11 J23
H_D#12 H22
H_D#13 F26
H_D#14 K22
H_D#15 H23
10 H_DSTBN#0 J26
10 H_DSTBP#0 H26
10 H_DINV#0 H25

DATA GRP3: D16#, D17#, D18#, D19#, D20#, D21#, D22#, D23#, D24#, D25#, D26#, D27#, D28#, D29#, D30#, D31#, DSTBN1#, DSTBP1#, DINV1#

H_D#16 N22
H_D#17 K25
H_D#18 P26
H_D#19 R23
H_D#20 L23
H_D#21 M24
H_D#22 L22
H_D#23 M23
H_D#24 P25
H_D#25 P23
H_D#26 P22
H_D#27 T24
H_D#28 R24
H_D#29 L25
H_D#30 T25
H_D#31 N25
10 H_DSTBN#1 L26
10 H_DSTBP#1 M26
10 H_DINV#1 N24

DATA GRP0: D32#, D33#, D34#, D35#, D36#, D37#, D38#, D39#, D40#, D41#, D42#, D43#, D44#, D45#, D46#, D47#, DSTBN2#, DSTBP2#, DINV2#

H_D#32 Y22
H_D#33 AB24
H_D#34 V24
H_D#35 V26
H_D#36 V23
H_D#37 T22
H_D#38 U25
H_D#39 U23
H_D#40 Y25
H_D#41 W22
H_D#42 Y23
H_D#43 W24
H_D#44 W25
H_D#45 AA23
H_D#46 AA24
H_D#47 AB25
Y26 H_DSTBN#2 10
AA26 H_DSTBP#2 10
U22 H_DINV#2 10

DATA GRP1: D48#, D49#, D50#, D51#, D52#, D53#, D54#, D55#, D56#, D57#, D58#, D59#, D60#, D61#, D62#, D63#, DSTBN3#, DSTBP3#, DINV3#

H_D#48 AE24
H_D#49 AD24
H_D#50 AA21
H_D#51 AB22
H_D#52 AB21
H_D#53 AC26
H_D#54 AD20
H_D#55 AE22
H_D#56 AF23
H_D#57 AC25
H_D#58 AE21
H_D#59 AD21
H_D#60 AC22
H_D#61 AD23
H_D#62 AF22
H_D#63 AC23
AE25 H_DSTBN#3 10
AF24 H_DSTBP#3 10
AC20 H_DINV#3 10

MISC: GTLREF, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, BSEL0, BSEL1, BSEL2, COMP0, COMP1, COMP2, COMP3, DPRSTP#, DPSLP#, DPWR#, PWRGOOD, SLP#, PSI#

R808 1 DY Do Not Stuff TEST1 AD26
R810 1 DY Do Not Stuff TEST2 C23
R813 1 DY Do Not Stuff CPU_TEST3 D25
C24
AE26
R815 1 DY Do Not Stuff CPU_TEST5 AF1
A26
7 CPU_BSEL0 B22
7 CPU_BSEL1 B23
7 CPU_BSEL2 C21

R26 COMP0 R807 1 27D4R2F-L1-GP
U26 COMP1 R809 1 54D9R2F-L1-GP
AA1 COMP2 R811 1 27D4R2F-L1-GP
Y1 COMP3 R814 1 54D9R2F-L1-GP
E5
B5
D24
D6
D7
AE6
H_DPRSTP# 11,20,47
H_DPSLP# 20
H_DPWR# 10
H_PWRGOOD 20,42
H_CPUSLP# 10
PSI# 47

BGA479-SKT6-GPU7
62.10079.001

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

TP813 1 H_CPURST#

DJ1

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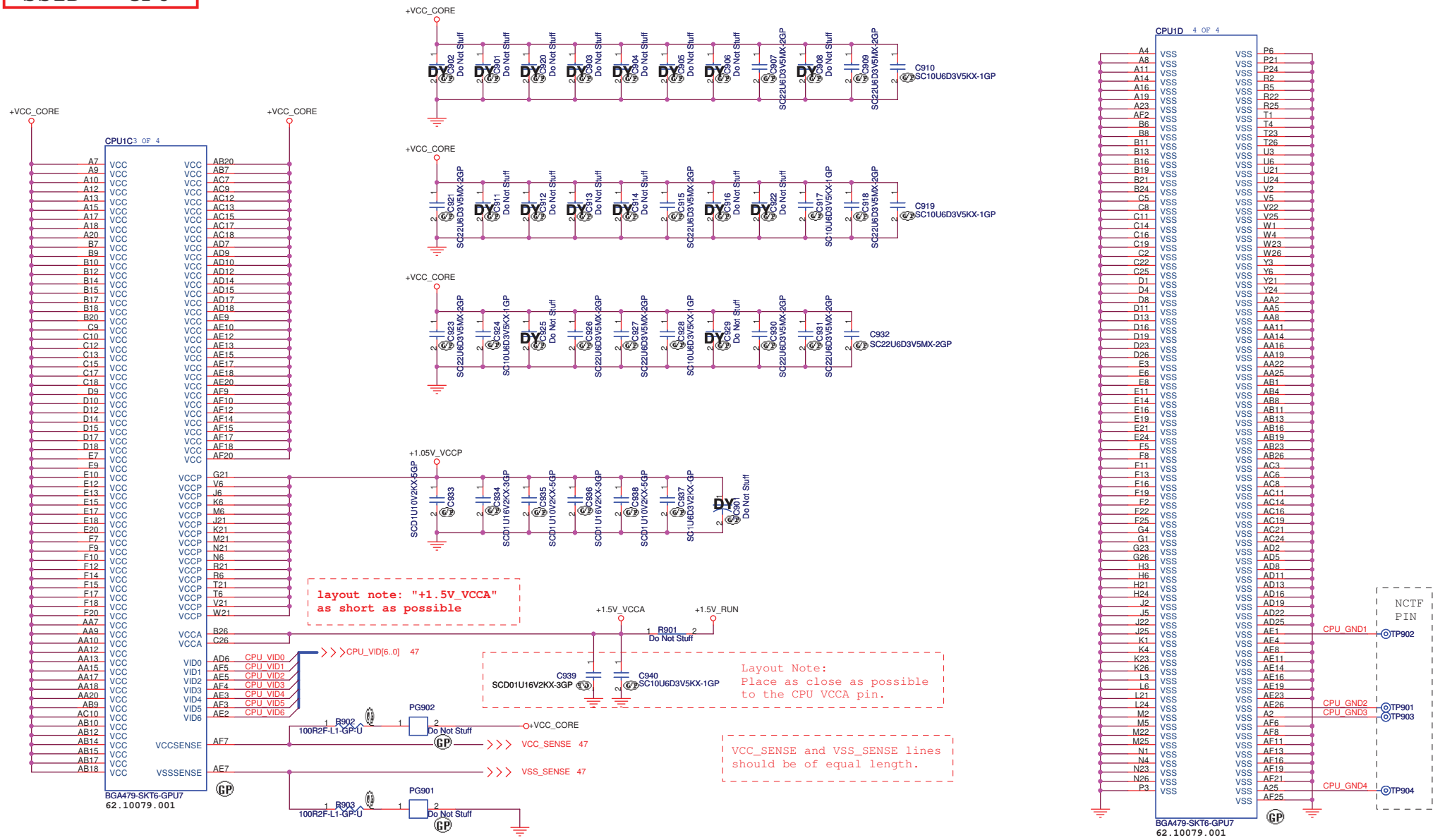
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-FSB(1/2)
Size: Custom
Document Number: DJ1 Montevina UMA
Rev: A00
Date: Friday, February 26, 2010 Sheet 8 of 88

SSID = CPU



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-Power(2/2)

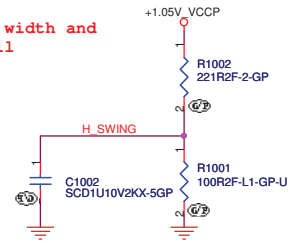
Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 9 of 88

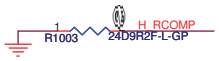
SSID = MCH

H_SWING routing Trace width and Spacing use 10 / 20 mil

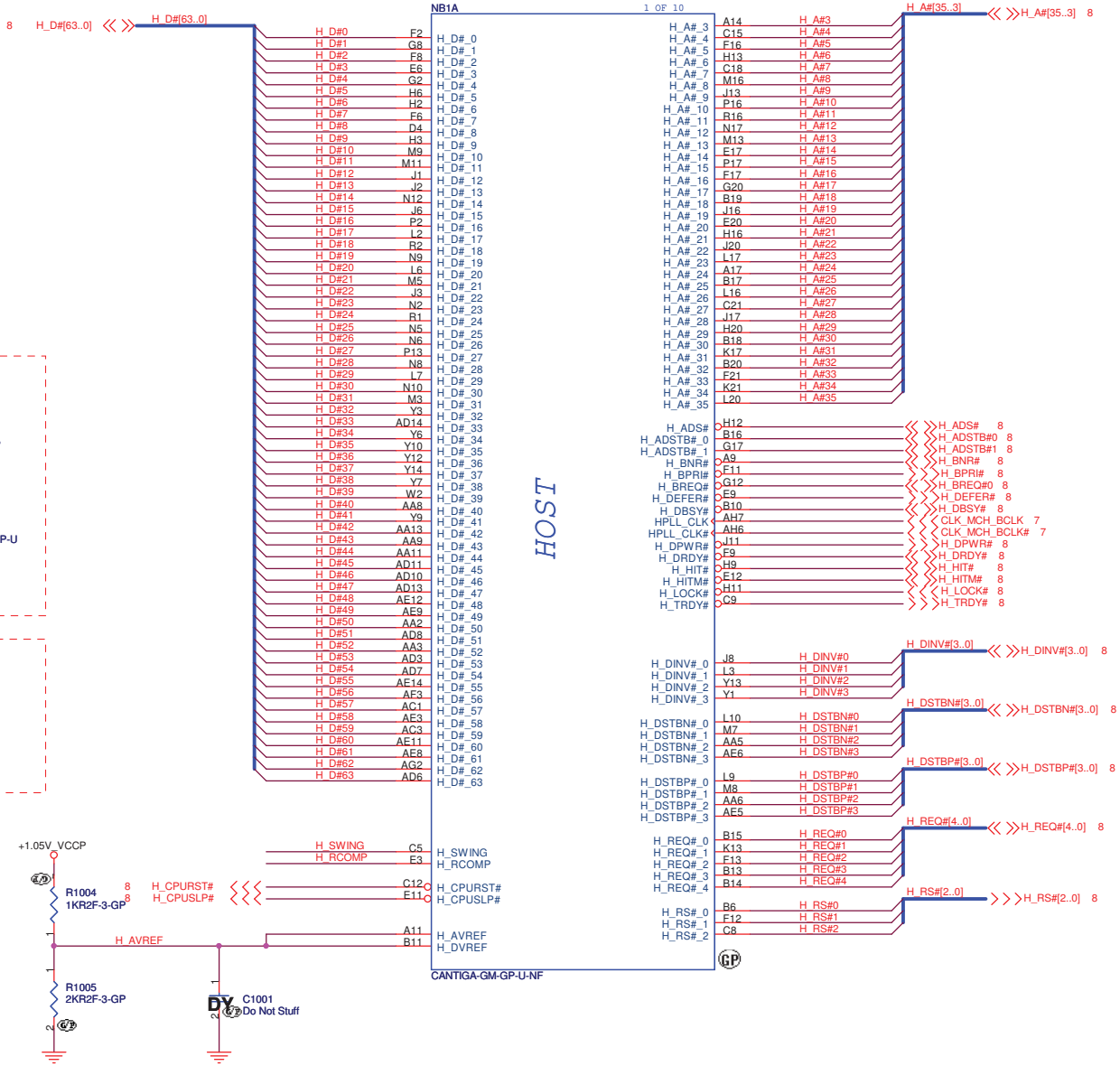
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place R1001 near to the chip (< 0.5")



DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-Host(1/6)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 10 of 88

SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled

NB1B — 2 OF 10 — CANTIGA-GM-GP-U-NF

RSVD: RESERVED#M36, RESERVED#N36, RESERVED#R33, RESERVED#T33, RESERVED#AH9, RESERVED#AH10, RESERVED#AH12, RESERVED#AH13, RESERVED#K12, RESERVED#AL34, RESERVED#AK34, RESERVED#AN35, RESERVED#AM35, RESERVED#T24, RESERVED#B31, RESERVED#B2, RESERVED#M1, RESERVED#AY21, RESERVED#BG23, RESERVED#BF23, RESERVED#BH18, RESERVED#BF18

DDR CLK / CONTROL/COMPENSATION: SA_CK_0..1, SB_CK_0..1 → M_CLK_DDR0..3; SA_CK#_0..1, SB_CK#_0..1 → M_CLK_DDR#0..3; SA_CKE_0..1, SB_CKE_0..1 → M_CKE0..3; SA_CS#_0..1, SB_CS#_0..1 → M_CS#0..3; SA_ODT_0..1, SB_ODT_0..1 → M_ODT0..3; SM_RCOMP, SM_RCOMP# → M_RCOMPP/M_RCOMPN; SM_RCOMP_VOH → SM_RCOMP_VOH; SM_RCOMP_VOL → SM_RCOMP_VOL; SM_VREF → CANTIGA_SM_VREF; SM_PWROK → SM_PWROK; SM_REXT → SM_REXT; SM_DRAMRST# → DDR3_DRAMRST#

CLK: DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK# → CLK_MCH_DREFCLK, CLK_MCH_DREFCLK#, MCH_SSCDREFCLK, MCH_SSCDREFCLK#; PEG_CLK, PEG_CLK# → CLK_MCH_3GPLL, CLK_MCH_3GPLL#

DMI: DMI_RXN_0..3 → DMI_ITXN0..3_MRXN0..3; DMI_RXP_0..3 → DMI_ITXP0..3_MRXP0..3; DMI_TXN_0..3 → DMI_IRXN0..3_MTXN0..3; DMI_TXP_0..3 → DMI_IRXP0..3_MTXP0..3

GRAPHICS VID: GFX_VID_0..4, GFX_VR_EN

ME: CL_CLK, CL_DATA, CL_PWROK, CL_RST#, CL_VREF → CL_CLK0, CL_DATA0, M_PWROK, CL_RST#0, MCH_CLVREF

MISC: DDPC_CTRLCLK, DDPC_CTRLDATA, SDVO_CTRLCLK, SDVO_CTRLDATA, CLKREQ#, ICH_SYNC#, TSATN#; GMCH_HDMI_DATA → TP1106; CLKREQ#_B, MCH_ICH_SYNC#

HDA: HDA_BCLK, HDA_RST#, HDA_SDI, HDA_SDO, HDA_SYNC

CFG: CFG_0..20 — FSB setting: MCH_CLKSEL0..2; CFG3, CFG4, CFG9, CFG10, CFG14..17, CFG19, CFG20; TP1102, TP1103, TP1104, TP1105, TP1101

PM: PM_SYNC#, PM_DPRSTP#, PM_EXT_TS#_0, PM_EXT_TS#_1, PWROK, RSTIN#, THERMTRIP#, DPRSLPVR; PWROK_R, R1125, R1127, C1107

NC: NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

+1.5V_SUS: R1103 80D6R2F-L-GP, R1105 80D6R2F-L-GP, R1102 1KR2F-3-GP, R1104 3K01R2F-3-GP, R1106 1KR2F-3-GP, C1102 SC2D2U6D3V3KX-GP, C1103 SCD01U16V2KX-3GP, C1104 SC2D2U6D3V3KX-GP, C1101 SCD01U16V2KX-3GP, SM_RCOMP_VOH, SM_RCOMP_VOL

+V_DDR_REF: R1108 Do Not Stuff; R1109 499R2F-2-GP; C1105 Do Not Stuff; C1106 Do Not Stuff

+3.3V_RUN: R1112 DY Do Not Stuff CFG19; R1113 DY Do Not Stuff CFG20; RN1102 PM_EXTTS#0, PM_EXTTS#1 SRN10KJ-5-GP; R1118 DY Do Not Stuff CFG9; R1119 DY Do Not Stuff CFG10; R1124 DY Do Not Stuff CFG16

+1.05V_VCCP: R1122 56R2J-4-GP; R1123 DY Do Not Stuff; Q1101 DY Do Not Stuff; TSATN#_KBC → TSATN#_KBC 37; TSATN#

+1.05V_VCCP: R1126 1KR2F-3-GP; R1128 499R2F-2-GP; C1108 SCD01U10V2KX-5GP

+3.3V_RUN: R1129 10KR2J-3-GP; CLKREQ#_B

MCH_CLVREF ~= 0.35V

DDR3_DRAMRST# 18,19; SM_PWROK 41

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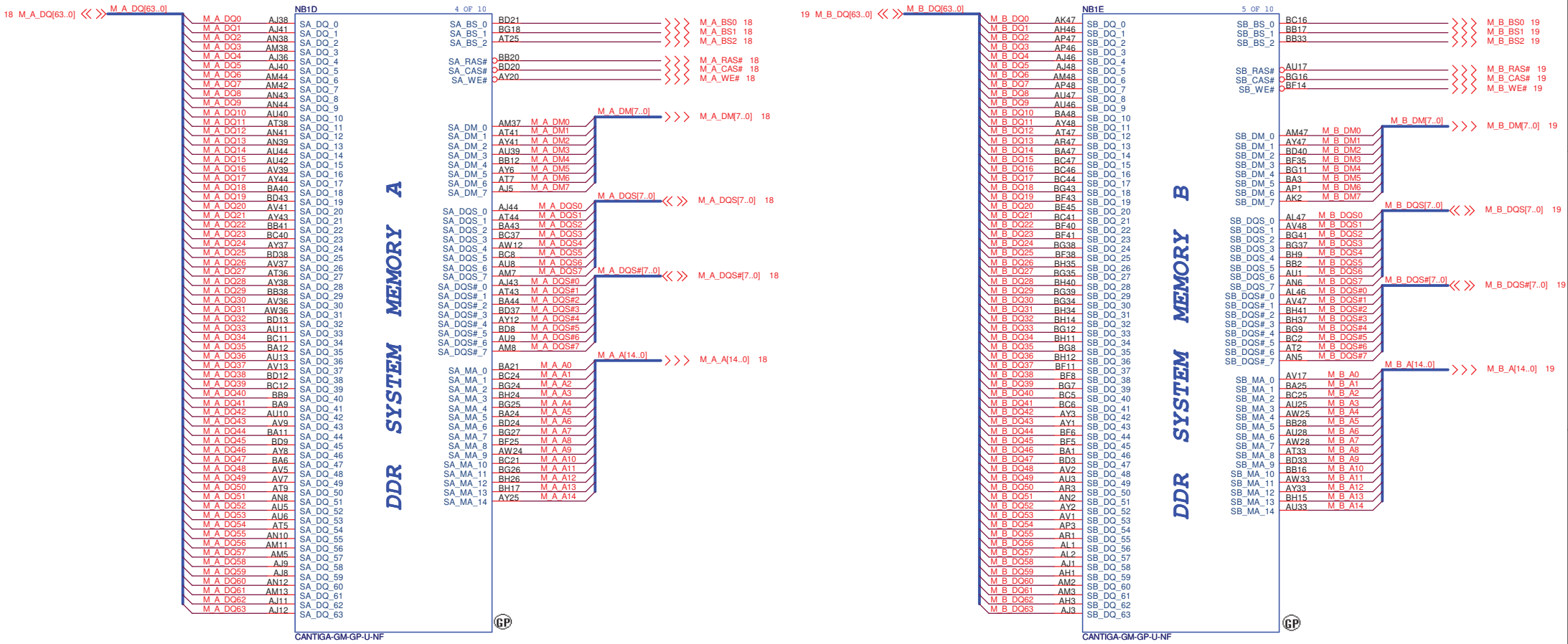
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-DMI/CFG(2/6)
Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00
Date: Friday, February 26, 2010 | Sheet 11 of 88

SSID = MCH



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cantiga-DDR(3/6)*

Size: Custom | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

Date: Friday, February 26, 2010 | Sheet 12 of 88

SSID = MCH

NB1I 9 OF 10

NB1J 10 OF 10

CANTIGA-GM-GP-U-NF

NCTF PIN

CRT_IREF routing Trace width use 20 mil.

NB1C 3 OF 10

LVDS

PCI-EXPRESS GRAPHICS

TV

VGA

CANTIGA-GM-GP-U-NF

Place R1303 close to MCH within 500 mils.

+1.05V_VCCP

R1303 49D9R2F-GP

RN1301 SRN2K2J-1-GP

RN1302 SRN10KJ-5-GP

R1302 2K37R2F-GPTP1302 Do Not Stuff

R1301 R1305 R1306 75R2F-2-GP

R1307 R1308 R1309 150R2F-1-GP

R1310 R1311 R1312 33R2J-2-GP

RN1303 SRN2K2J-1-GP

U1301 2N7002EDW-GP

DJ1

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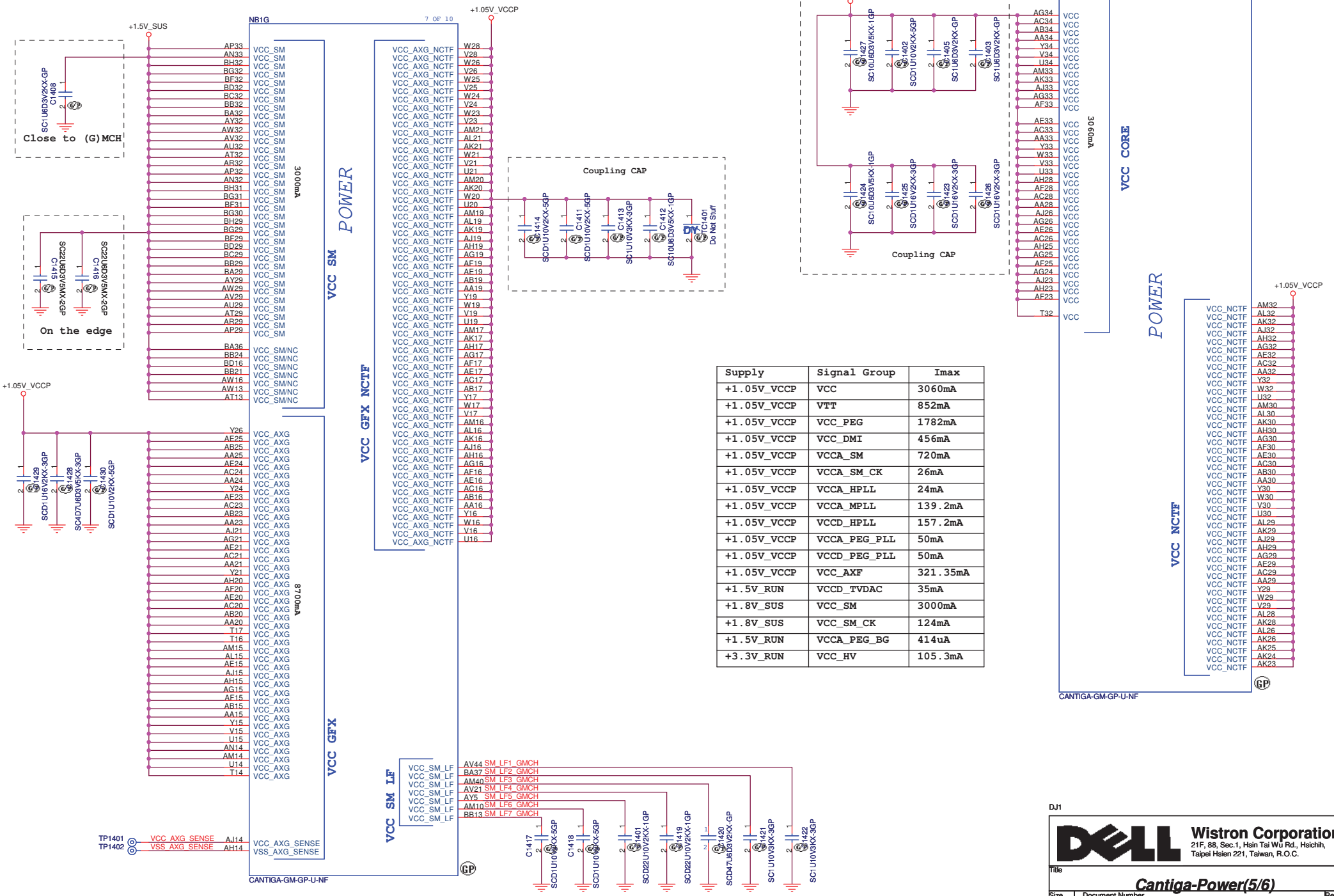
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-GND/LVDS/VGA(4/6)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 13 of 88

SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

DJ1

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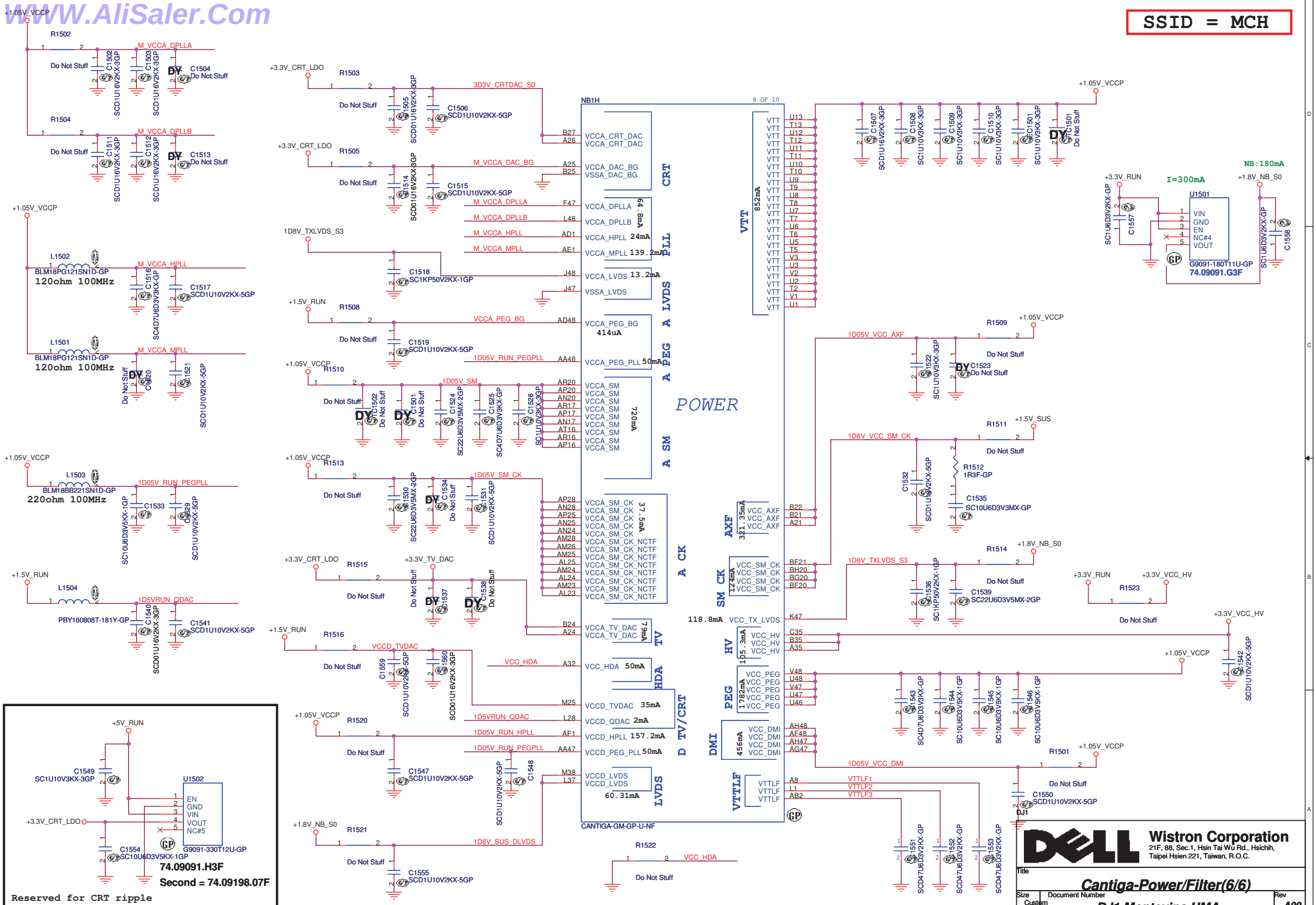
Title: Cantiga-Power(5/6)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 14 of 88

SSID = MCH



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Title	Cantiga-Power/Filter(6/6)
Size: Custom	Document Number: DJ1 Montevina UMA
Rev	A00
Date: Wednesday, February 24, 2010	Sheet 15 of 88

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DJ1

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Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 16 of 88

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Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 17 of 88

M_A_DM[7..0] 12
M_A_DQS#[7..0] 12
M_A_DQS[7..0] 12
M_A_A[14..0] 12

DM1

M_A_A0 98
M_A_A1 97
M_A_A2 96
M_A_A3 95
M_A_A4 92
M_A_A5 91
M_A_A6 90
M_A_A7 86
M_A_A8 89
M_A_A9 85
M_A_A10 107
M_A_A11 84
M_A_A12 83
M_A_A13 119
M_A_A14 80
M_A_A15 78
79

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2

TP1801

12 M_A_BS2
12 M_A_BS0
12 M_A_BS1
12 M_A_DQ[63..0]

109 BA0
108 BA1

M_A_DQ0 5
M_A_DQ1 7
M_A_DQ2 15
M_A_DQ3 17
M_A_DQ4 4
M_A_DQ5 6
M_A_DQ6 16
M_A_DQ7 18
M_A_DQ8 21
M_A_DQ9 23
M_A_DQ10 33
M_A_DQ11 35
M_A_DQ12 22
M_A_DQ13 24
M_A_DQ14 34
M_A_DQ15 36
M_A_DQ16 39
M_A_DQ17 41
M_A_DQ18 51
M_A_DQ19 53
M_A_DQ20 40
M_A_DQ21 42
M_A_DQ22 50
M_A_DQ23 52
M_A_DQ24 57
M_A_DQ25 59
M_A_DQ26 67
M_A_DQ27 69
M_A_DQ28 56
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M_A_DQ30 68
M_A_DQ31 70
M_A_DQ32 129
M_A_DQ33 131
M_A_DQ34 141
M_A_DQ35 143
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M_A_DQ56 181
M_A_DQ57 183
M_A_DQ58 191
M_A_DQ59 193
M_A_DQ60 180
M_A_DQ61 182
M_A_DQ62 192
M_A_DQ63 194

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

M_A_DQS#0 10
M_A_DQS#1 27
M_A_DQS#2 45
M_A_DQS#3 62
M_A_DQS#4 135
M_A_DQS#5 152
M_A_DQS#6 169
M_A_DQS#7 186

M_A_DQS0 12
M_A_DQS1 29
M_A_DQS2 47
M_A_DQS3 64
M_A_DQS4 137
M_A_DQS5 154
M_A_DQS6 171
M_A_DQS7 188

DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

11 M_ODT0
11 M_ODT1

ODT0 ODT1

M_VREF_CA_DIMM0 126
M_VREF_DQ_DIMM0 1

VREF_CA VREF_DQ

11,19 DDR3_DRAMRST# 30

RESET#

+0.75V_DDR_VTT 203 204

VTT1 VTT2

NP1 NP2

RAS# 110
WE# 113
CAS# 115

M_A_RAS# 12
M_A_WE# 12
M_A_CAS# 12

CS0# 114
CS1# 121

M_CS#0 11
M_CS#1 11

CKE0 73
CKE1 74

M_CKE0 11
M_CKE1 11

CK0 101
CK0# 103

M_CLK_DDR0 11
M_CLK_DDR#0 11

CK1 102
CK1# 104

M_CLK_DDR1 11
M_CLK_DDR#1 11

DM0 11 M_A_DM0
DM1 28 M_A_DM1
DM2 46 M_A_DM2
DM3 63 M_A_DM3
DM4 136 M_A_DM4
DM5 153 M_A_DM5
DM6 170 M_A_DM6
DM7 187 M_A_DM7

SDA 200
SCL 202

ICH_SMBDATA 7,19,22,76
ICH_SMBCLK 7,19,22,76

EVENT# 198

PM_EXTTS#0 11

VDDSPD 199

SA0 197 SA0_DIM0
SA1 201 SA1_DIM0

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2 3 8 9 13 14 19 20 25 26 31 32 37 38 43 44 48 49 54 55 60 61 65 66 71 72 127 128 133 134 138 139 144 145 150 151 155 156 161 162 167 168 172 173 178 179 184 185 189 190 195 196 205 206

DDR3-204P-41-GP-U
62.10017.N41

H =5.2mm

SA0_DIM0
SA1_DIM0

R1802 10KR2J-3-GP
R1803 10KR2J-3-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

+3.3V_RUN

C1801 SCD1U10V2KX-5GP
DY C1802 Do Not Stuff

+1.5V_SUS

SODIMM A DECOUPLING

+1.5V_SUS

TC1801 Do Not Stuff
C1803 SC10U10V5ZY-1GP
C1804 SC10U10V5ZY-1GP
C1805 SC10U10V5ZY-1GP
C1806 SC10U10V5ZY-1GP
C1807 SC10U10V5ZY-1GP
C1808 SC10U10V5ZY-1GP

C1813 SCD1U16V2KX-3GP
C1814 SCD1U16V2KX-3GP
C1815 SCD1U16V2KX-3GP
C1816 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

+V_DDR_REF
R1806
M_VREF_CA_DIMM0
Do Not Stuff
C1811 SCD1U10V2KX-5GP
C1812 SC2D2U6D3V3KX-GP

+V_DDR_REF
R1807
M_VREF_DQ_DIMM0
Do Not Stuff
C1817 SCD1U10V2KX-5GP
C1818 SC2D2U6D3V3KX-GP

Place between DM1 and DM2.

+0.75V_DDR_VTT
C1819 SC10U10V5ZY-1GP
DY C1824 Do Not Stuff

+0.75V_DDR_VTT
Place these caps close to VTT1 and VTT2.

C1820 C1821 C1822 C1823 SC1U16V2KX-GP

DJ1

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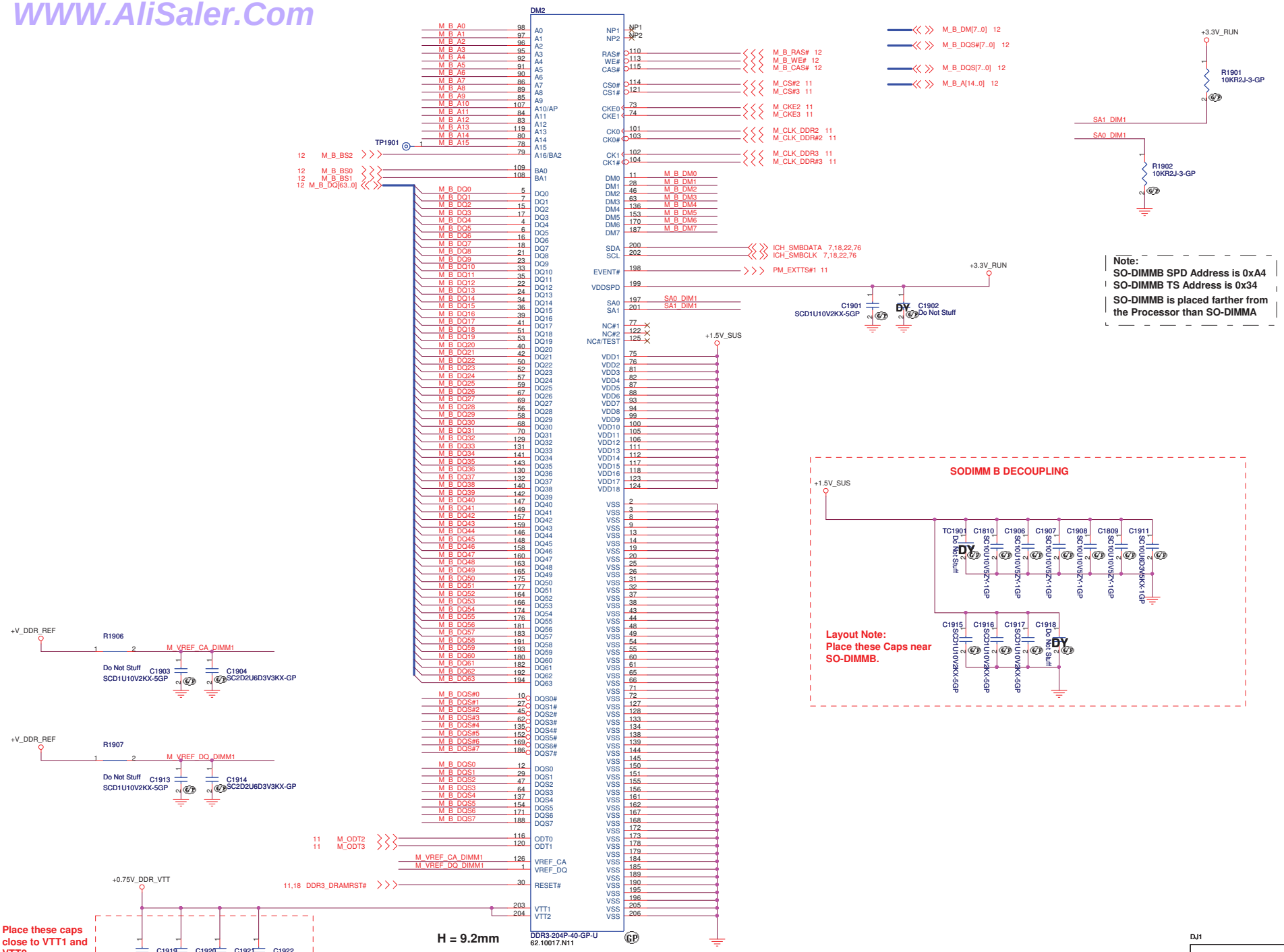
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1
Size: Document Number: DJ1 Montevina UMA
Rev: A00
Date: Friday, February 26, 2010 Sheet 18 of 88

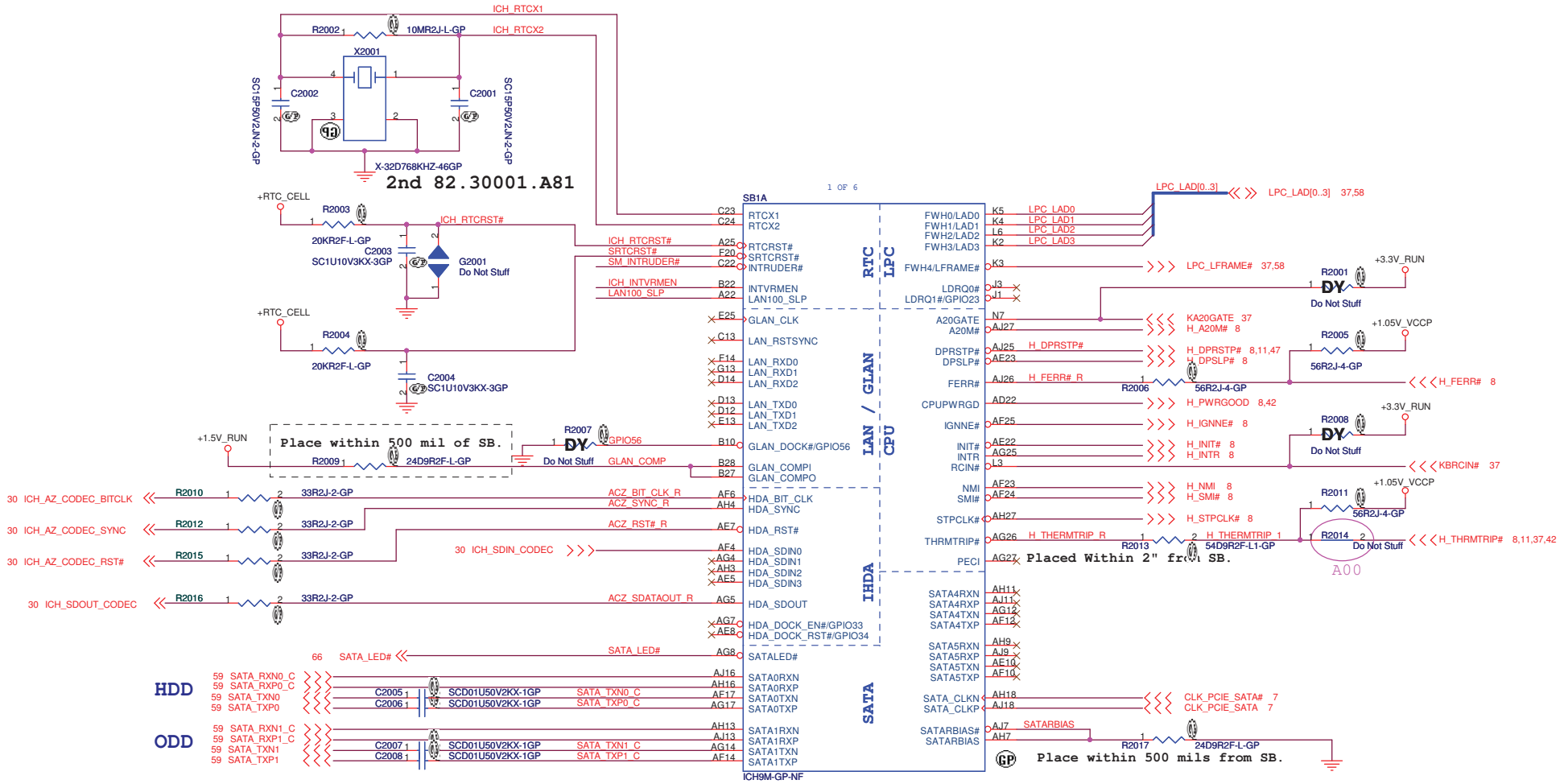


DJ1

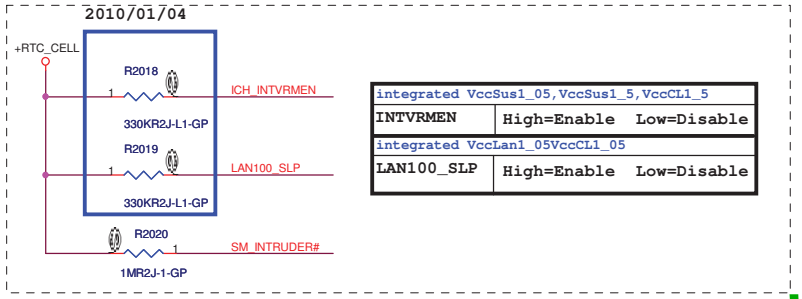
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR3-SODIMM2	
Size	Document Number: DJ1 Montevina UMA	Rev: A00
Date: Friday, February 26, 2010	Sheet 19 of 88	

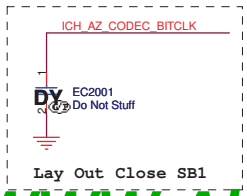
SSID = ICH



2010/01/04



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(1/4)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 20 of 88

SSID = ICH

SB1E — 5 OF 6 — ICH9M-GP-NF

SB1B — 2 OF 6 — ICH9M-GP-NF

SB1D — 4 OF 6 — ICH9M-GP-NF

+3.3V_RUN

PLT_RST# → R2102 Do Not Stuff → PCI_PLTRST#

Layout Note:
Place as close as possible to the ICH Pin

RP2101 SRN10KJ-L3-GP

RN2106 SRN8K2J-4-GP

RN2102 RN2101 RN2103 RN2104 RN2105 SRN8K2J-4-GP

R2103 DY Do Not Stuff — PCI_GNT0#
R2104 DY Do Not Stuff — SPI_CS#1
R2105 DY Do Not Stuff — PCI_GNT3#

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

WLAN — SCD1U10V2KX-5GP — PCIE_RXN2 PCIE_RXP2 PCIE_TXN2 PCIE_TXP2 — C2101 C2104

LAN — SCD1U10V2KX-5GP — PCIE_RXN3 PCIE_RXP3 PCIE_TXN3 PCIE_TXP3 — C2105 C2106

PCI-Express / Direct Media Interface

SPI: SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6 SPI_MOSI SPI_MISO — TP2106 TP2107 TP2110 TP2111

USB: USB_OC#0_1 USB_OC#1 USB_OC#2_3 USB_OC#3 USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9 USB_OC#10 USB_OC#11

USB_RBIAS_PN → R2101 22D6R2F-L1-GP

+1.5V_RUN → R2106 24D9R2F-L-GP → DMI_IRCOMP_R

USB Pair	Device
0	USB0 (I/O Board)
1	RESERVED
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

USB0 — USB_PN0 USB_PP0 — TP2102 TP2103

USB2 USB3 — USB_PN2 USB_PP2 USB_PN3 USB_PP3 USB_PN4 USB_PP4

WLAN — USB_PN6 USB_PP6 USB_PN7 USB_PP7 USB_PN8 USB_PP8 USB_PN9 USB_PP9 — TP2115 TP2116 TP2118 TP2119 TP2112 TP2114

Card Reader CAMERA — USB_PN10 USB_PP10 USB_PN11 USB_PP11

NCTF PIN — ICH_GND1 TP2113, ICH_GND2 TP2117, ICH_GND3 TP2120, ICH_GND4 TP2101

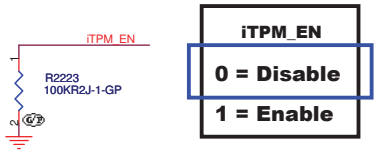
DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

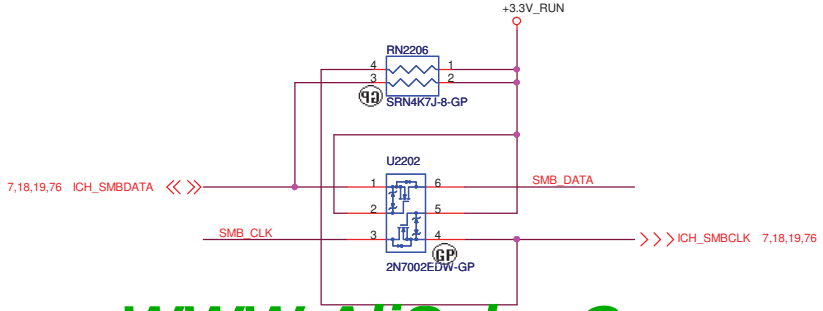
Title: **ICH9-PCI/PCIE/DMI/USB/GND(2/4)**
Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00
Date: Friday, February 26, 2010 | Sheet 21 of 88

SSID = ICH

iTPM Select(Not Strap Pin)



iTPM_EN
0 = Disable
1 = Enable



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

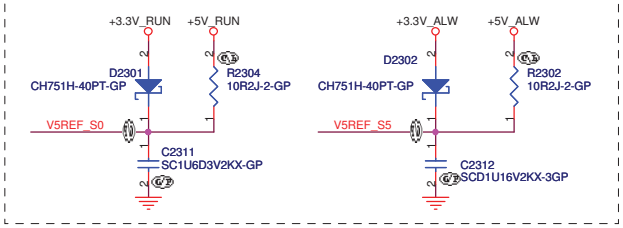
Title: ICH9-GPIO/PM/CL(3/4)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 22 of 88

SSID = ICH

**Within a given well, 5VREF needs to be up before the corresponding 3.3V rail*



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ICH9-Power(4/4)
Size: Custom	Document Number: DJ1 Montevina UMA
Rev	A00
Date: Wednesday, February 24, 2010	Sheet 23 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 24 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 25 of 88

(Blanking)

DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 26 of 88

(Blanking)

DJ1

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Title: Reserved

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 27 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: Custom | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

Date: Wednesday, February 24, 2010 | Sheet 28 of 88

(Blanking)

DJ1

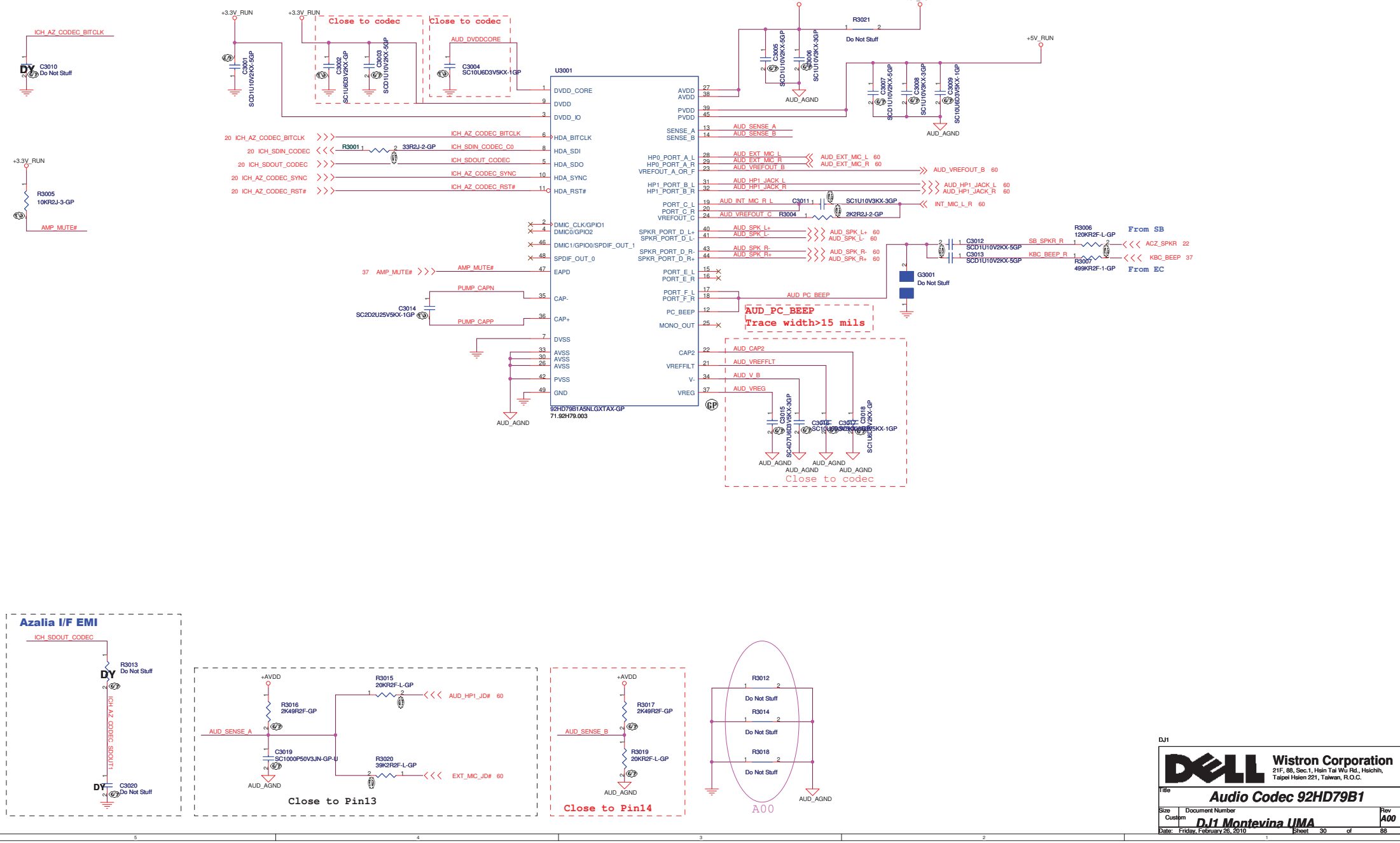
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 29 of 88

SSID = AUDIO



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD79B1

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 30 of 88

(Blanking)

DJ1

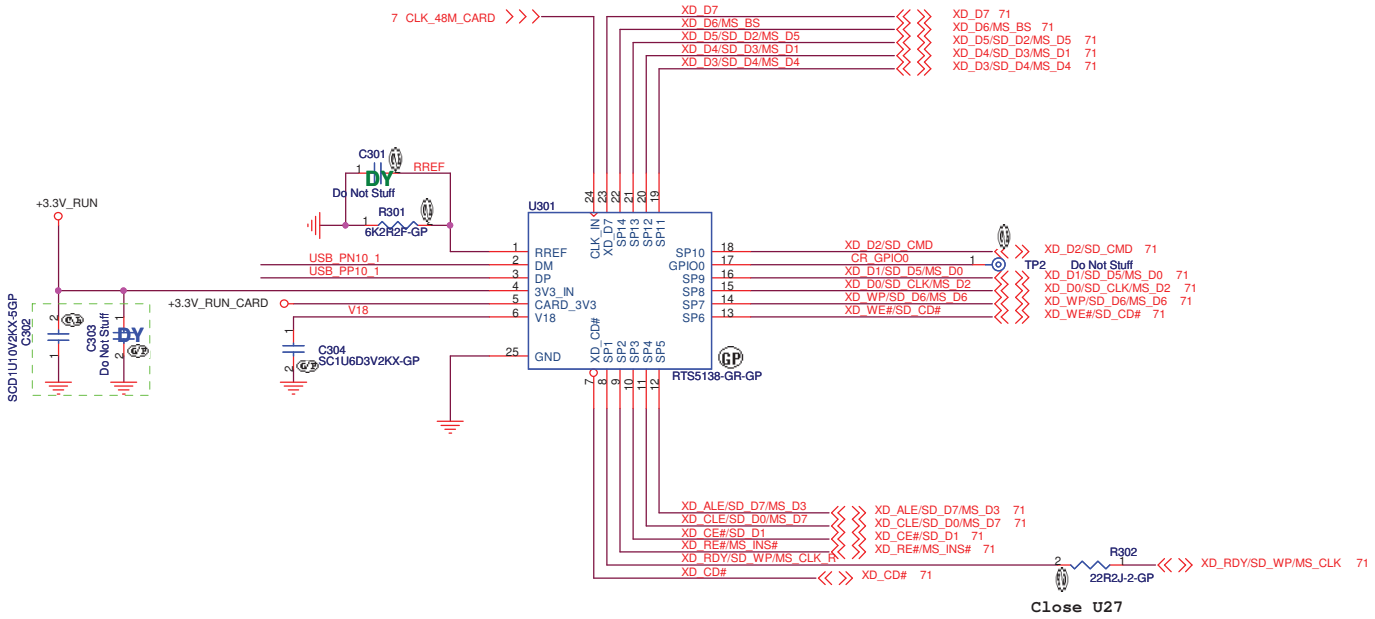
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

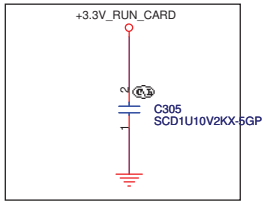
Date: Wednesday, February 24, 2010 Sheet 31 of 88

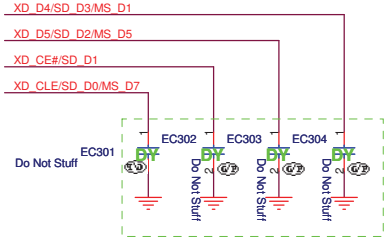
SSID = SDIO

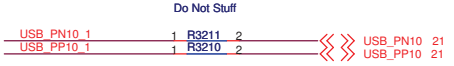


Close U27

Close to U301







2010/01/05

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 32 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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(Blanking)

DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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DJ1

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Title: (Reserved)

Size | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 35 of 88

(Blanking)

DJ1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 36 of 88

CAP close to VCC-GND pin pair

SSID = KBC

U3701A — NPCE781BA0DX-GP

A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR

Layout note:
1. Connect KBC_AGND and GND at one point
2. R3725 close to Pin 103 (AGND)

A00
For RCID Function

MB VERSION ID

	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
A00	0	1	0
A01	0	1	1

KBC CLK
EMI

U3701B — NPCE781BA0DX-GP

KBC
PS/2
FIU

SSID = KBC

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX
Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00
Date: Friday, February 26, 2010 | Sheet 37 of 88

(Blanking)

DJ1

Wistron Corporation
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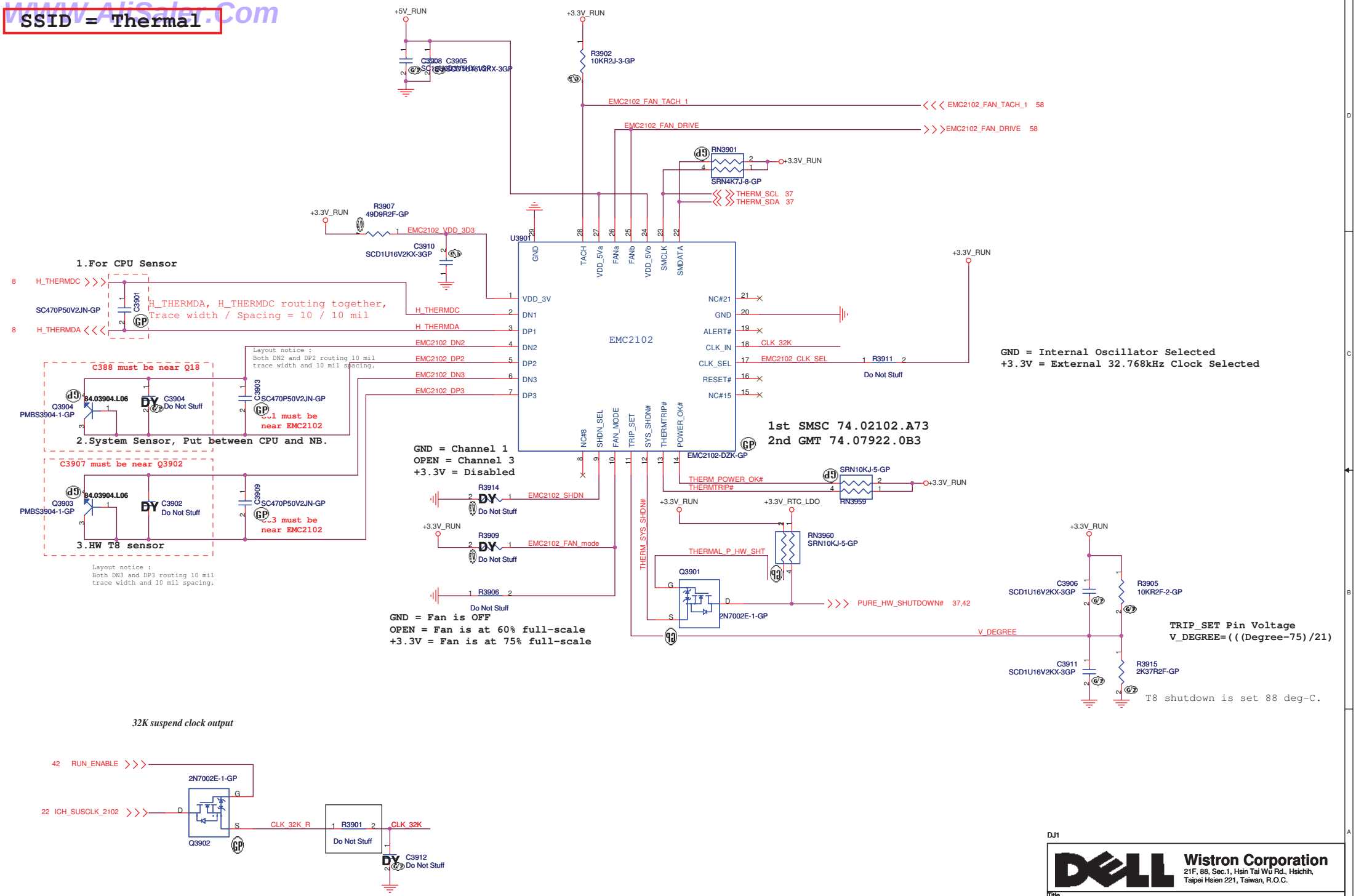
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 38 of 88

SSID = Thermal



32K suspend clock output

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal/Fan Controllor EMC2102*

Size	Document Number	Rev
Custom	*DJ1 Montevina UMA*	*A00*

Date: Friday, February 26, 2010 Sheet 39 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

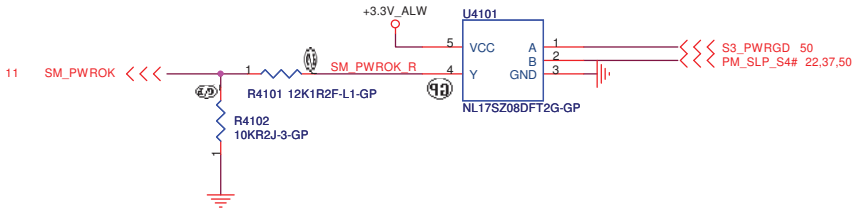
Title

Reserved

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 40 of 88

SSID = Reset.Suspend

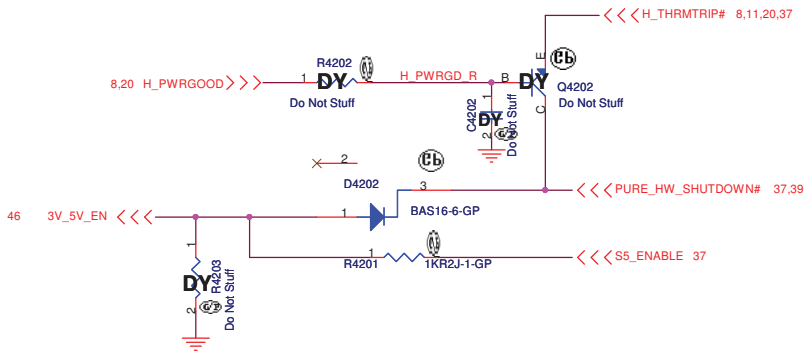


DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

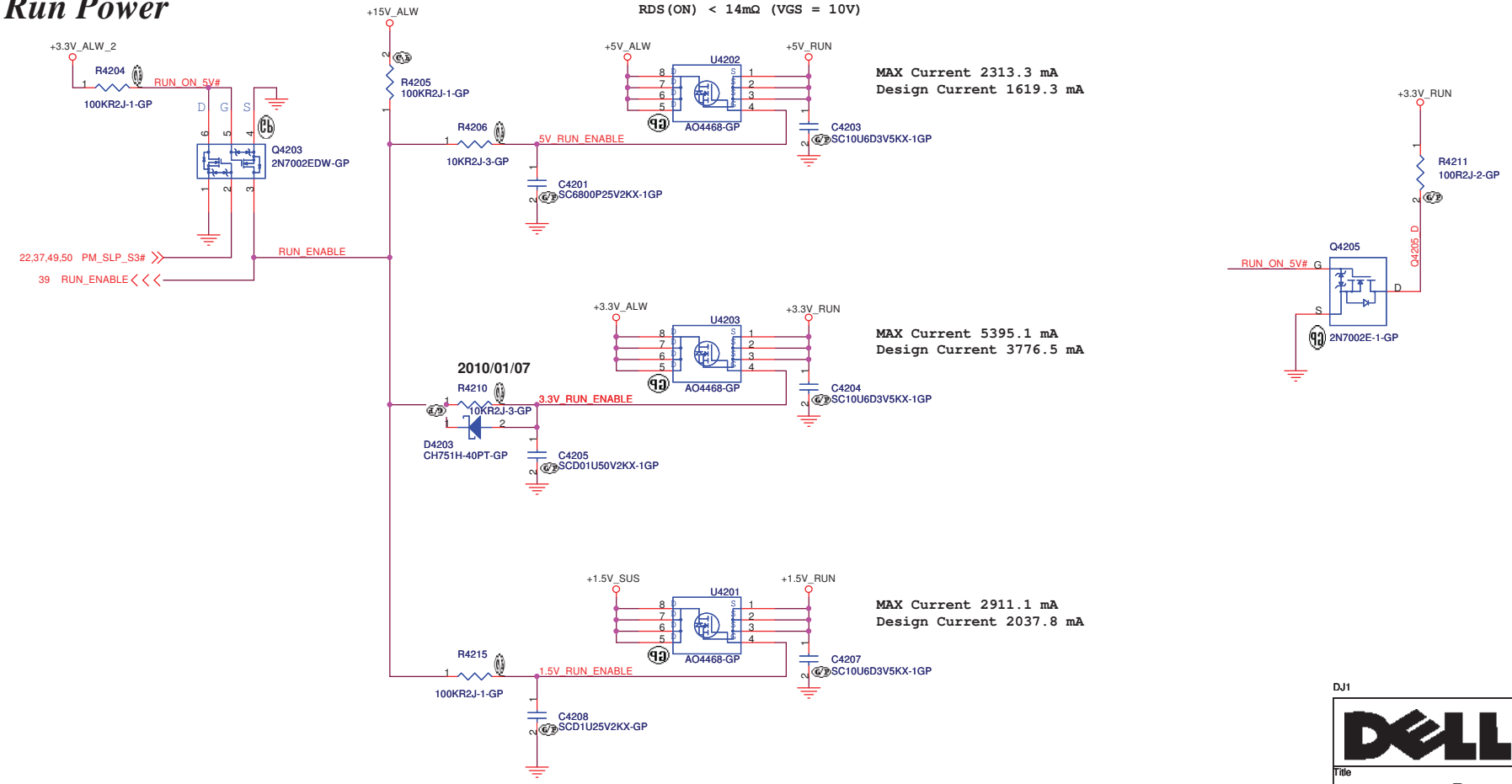
Title	Power On Logic	
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
Date: Friday, February 26, 2010	Sheet 41 of 88	

SSID = Reset.Suspend



Run Power

AO4468 MAX 11.6A
RDS(ON) < 14mΩ (VGS = 10V)



DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 42 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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(Blanking)

DJ1

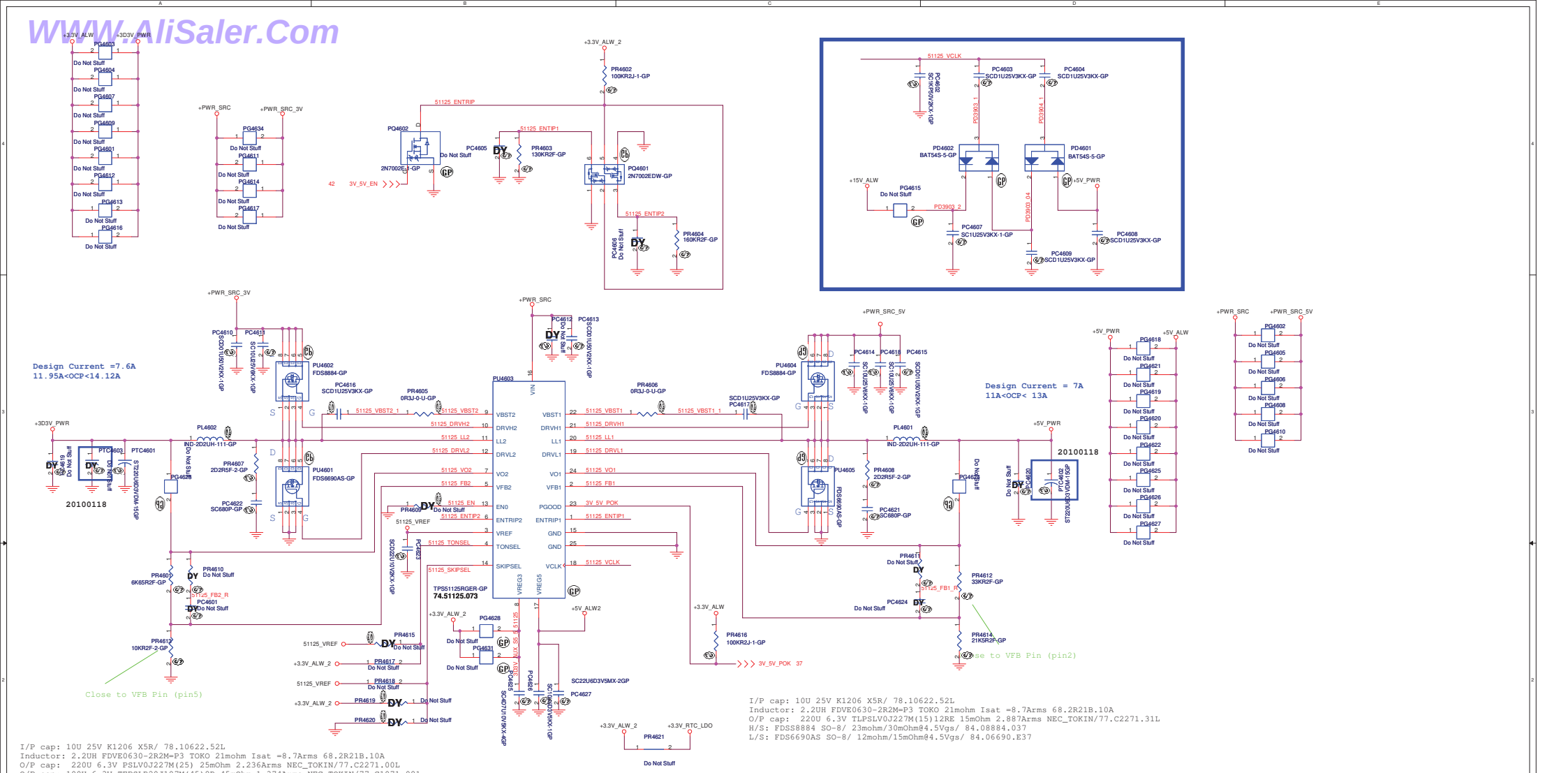
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 45 of 88



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH FDVE0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
O/P cap: 220U 6.3V TLPSLV0J227M(15)12RE 15mOhm 2.887Arms NEC_TOKIN/77.C2271.31L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

DJ1

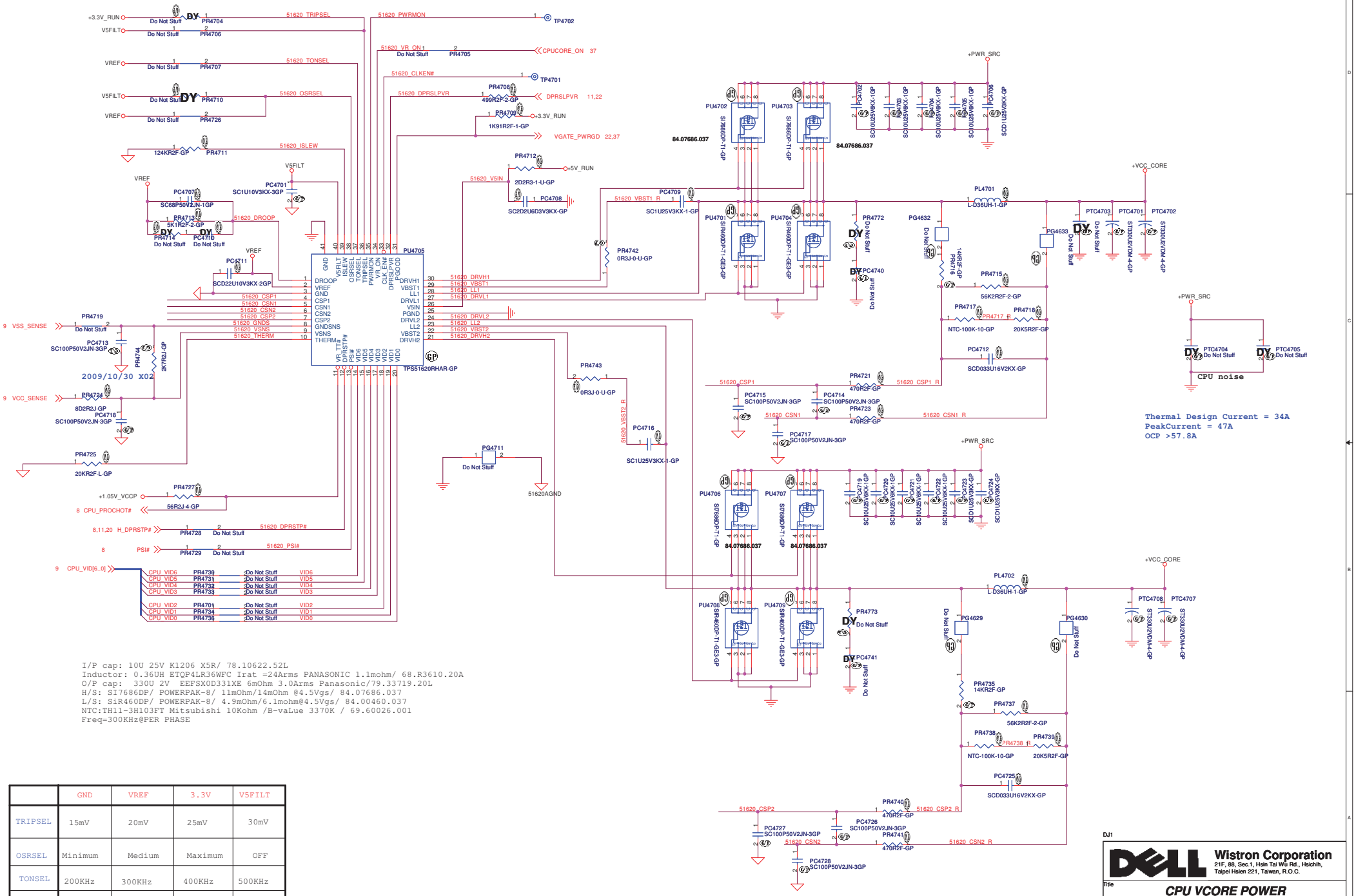
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

Size: A2 | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 46 of 88

SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC Irat =24Arms PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.0Arms Panasonic/79.33719.20L
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/14mOhm @4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
NTC:TH11-3H103FT Mitsubishi 10Kohm /B-vaLue 3370K / 69.60026.001
Freq=300KHz@PER PHASE

	GND	VREF	3.3V	V5FILT
TRIPSEL	15mV	20mV	25mV	30mV
OSRSEL	Minimum	Medium	Maximum	OFF
TONSEL	200KHz	300KHz	400KHz	500KHz
OVPSEL	ENABLE	DISABLE	N/A	N/A

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 47 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

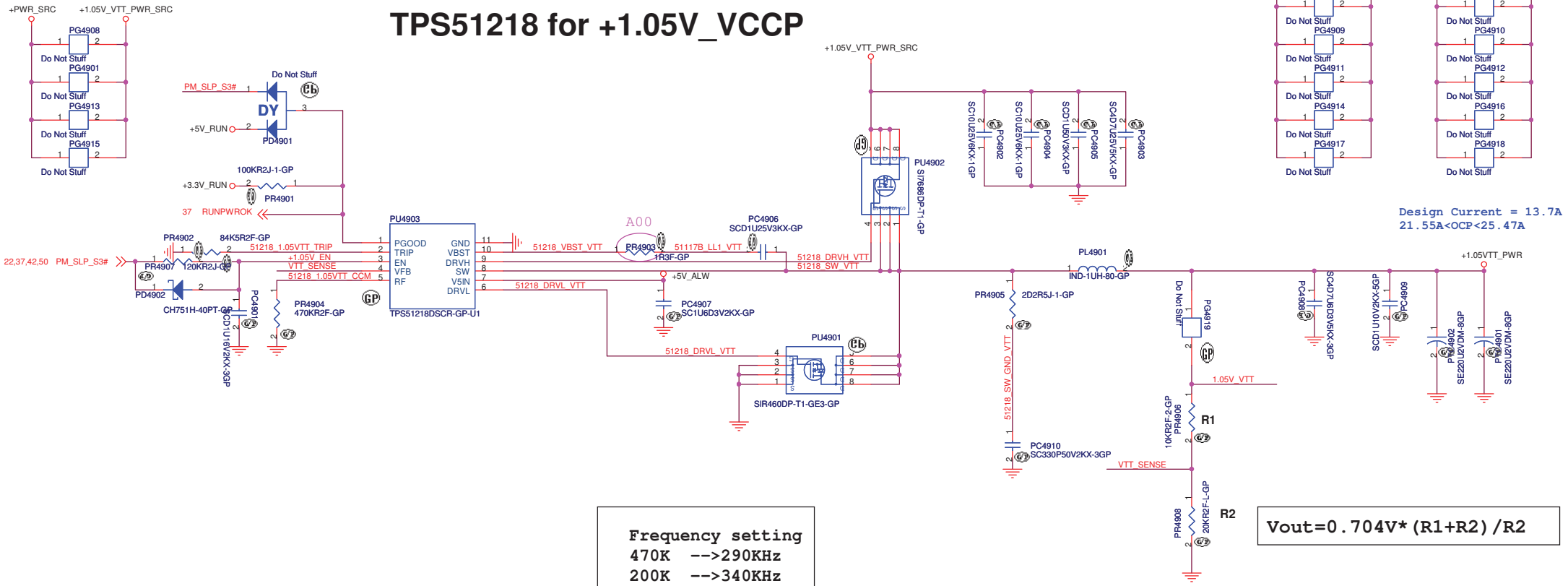
Title: CPU VCORE POWER(2/2)

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 48 of 88

SSID = PWR.Plane.Regulator_1p05v

TPS51218 for +1.05V_VCCP



Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1uH FDUE1040D-1R0M=P3 TOKO DCR:2.35mohm Isat =17.9Arms 68.1R01B.10A
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP-T1-E3/11mohm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SIR460DP-T1-GE3-GP/4.5mOhm/6.1mohm@4.5Vgs/ 84.00460.037

DJ1

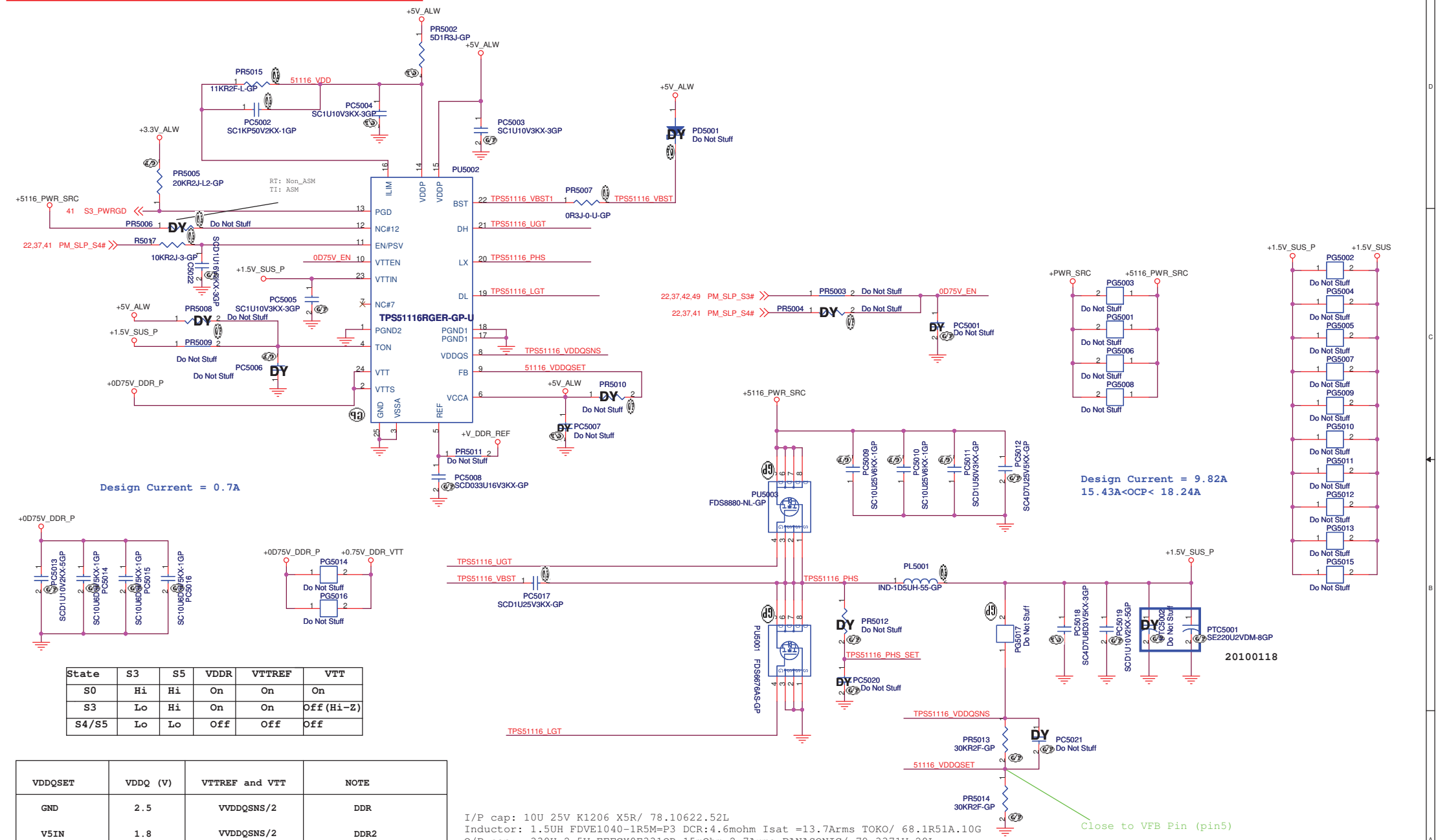
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VCCP

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 49 of 88

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH FDVE1040-1R5M=P3 DCR:4.6mohm Isat =13.7Arms TOKO/ 68.1R51A.10G
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS/ 5.9mOhm/7.25mohm@4.5Vgs/ 84.06676.A37
Switching freq-->400KHz

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116_+1.5V_SUS
Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00
Date: Friday, February 26, 2010 | Sheet 50 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 51 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 52 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

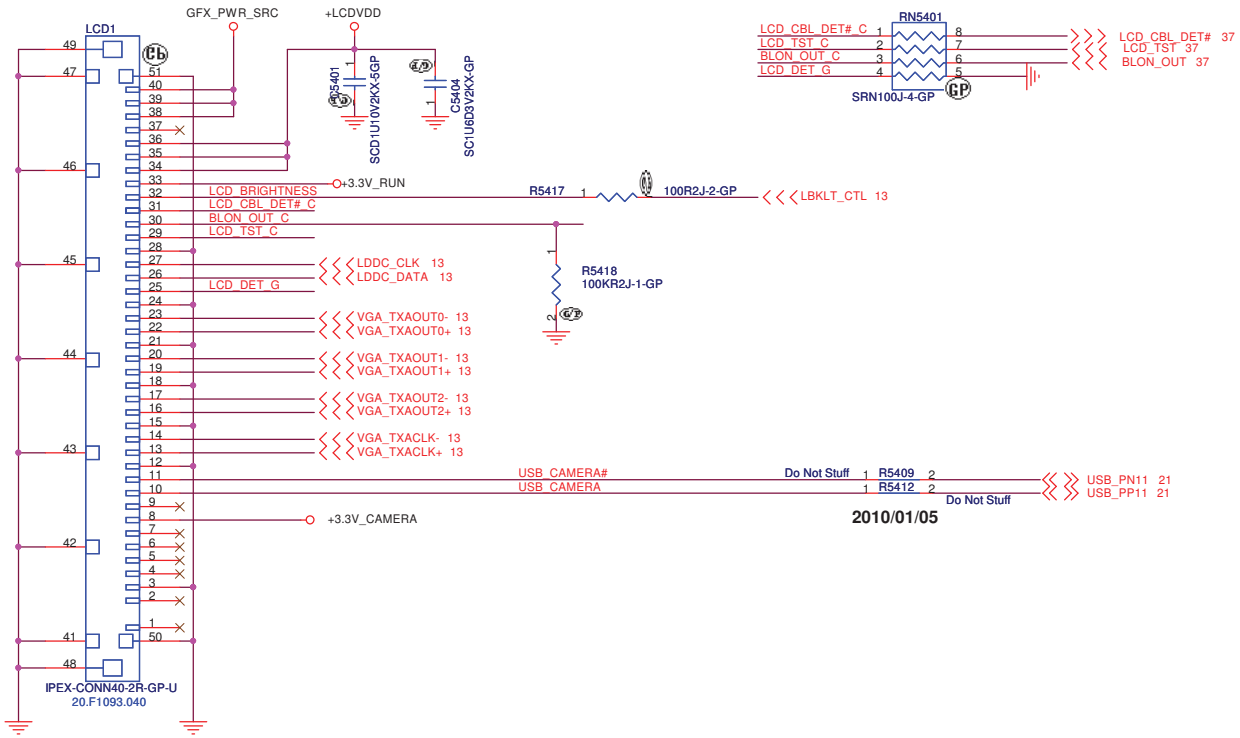
Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 53 of 88

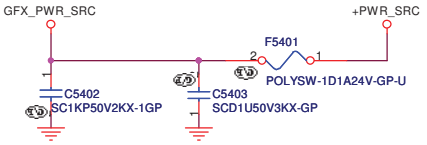
SSID = VIDEO

LVDS CONNECTOR



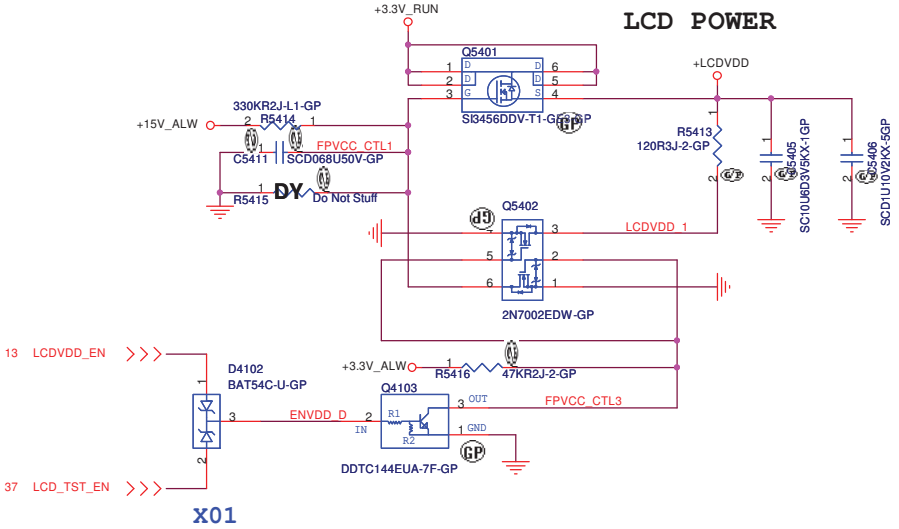
SSID = Inverter

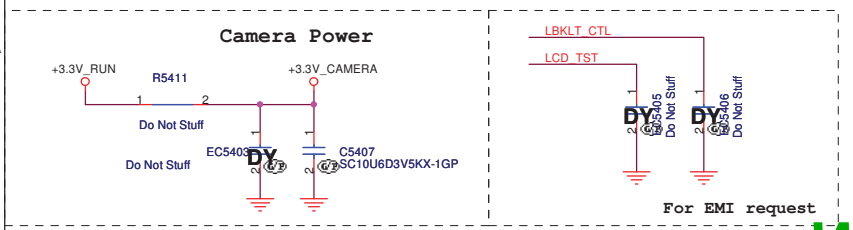
INVERTER POWER



SSID = VIDEO

LCD POWER





DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *LCD/Inverter Connector*

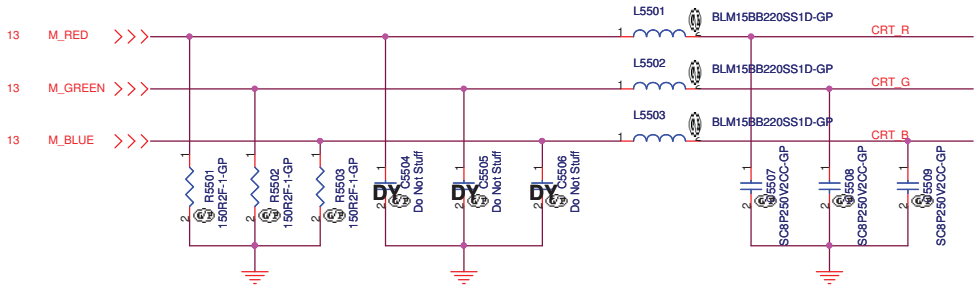
Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

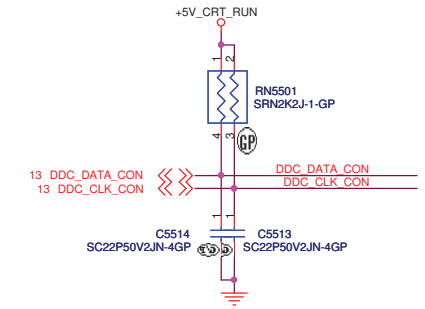
Date: Friday, February 26, 2010 Sheet 54 of 88

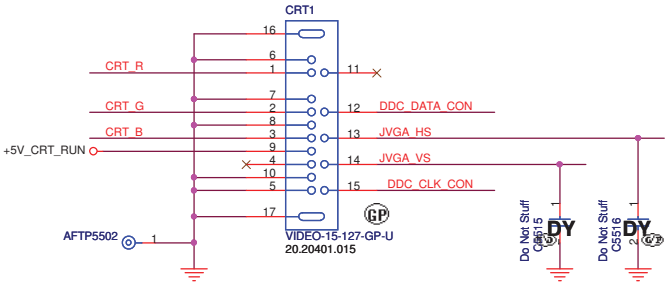
SSID = VIDEO

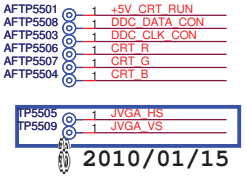
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

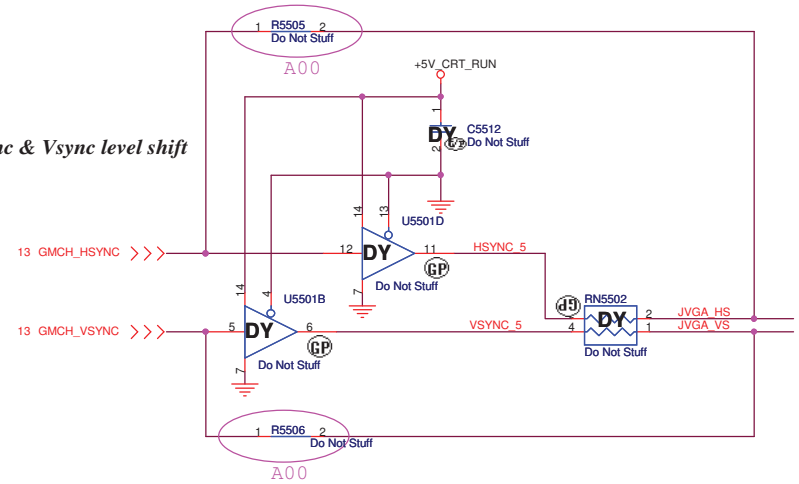


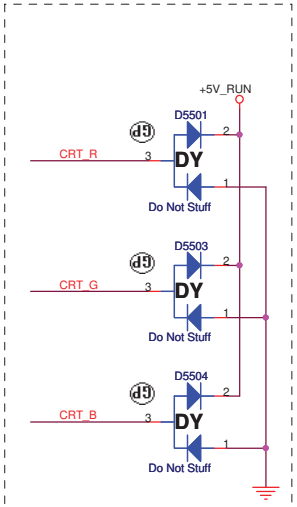


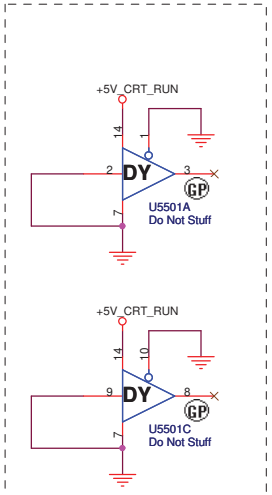


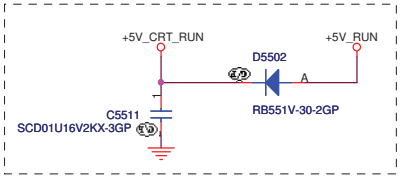


Hsync & Vsync level shift









DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT Connector***

Size | Document Number: ***DJ1 Montevina UMA*** | Rev: ***A00***

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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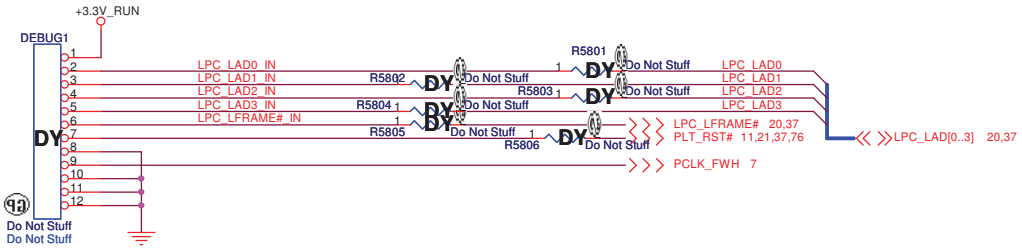
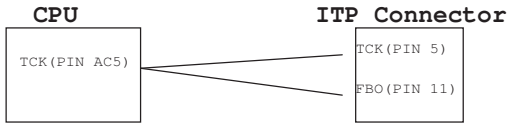
SSID = User.Interface

ITP Connector

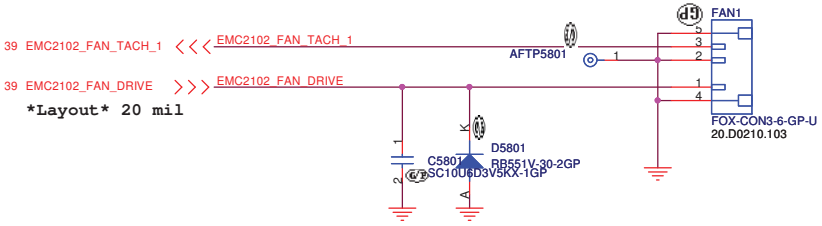
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

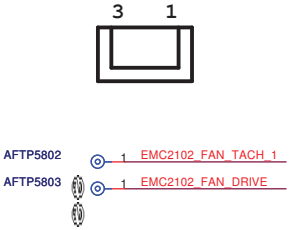




SSID = Thermal

Fan Connector





DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ITP/Fan Connector		
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
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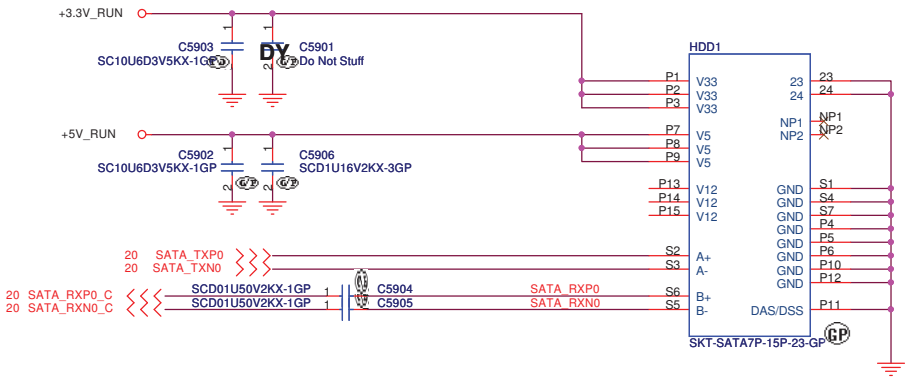
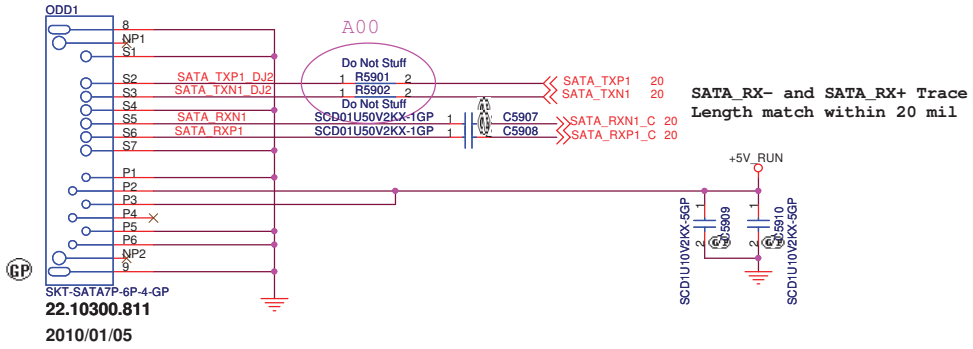
SSID = SATA

SATA HDD Connector



ODD Connector



DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	HDD/ODD	
Size A3	Document Number DJ1 Montevina UMA	Rev A00
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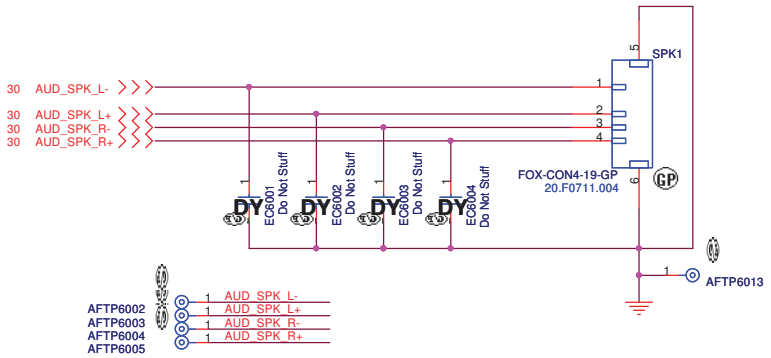
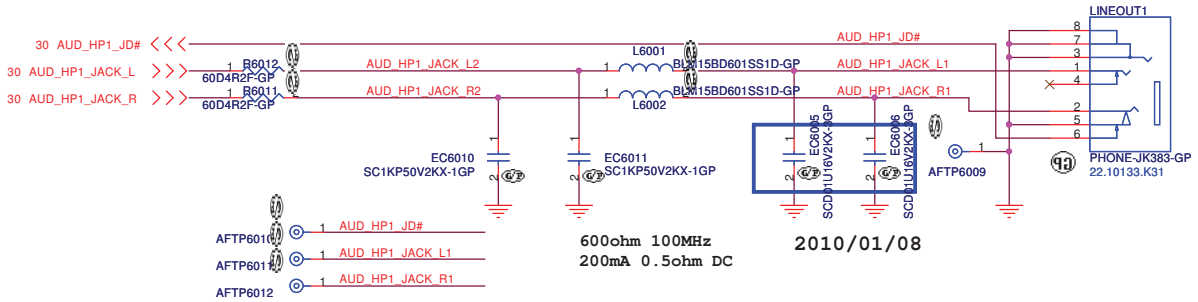
SSID = AUDIO

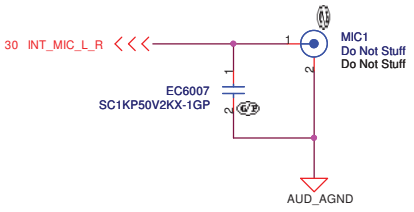
Speaker Connector



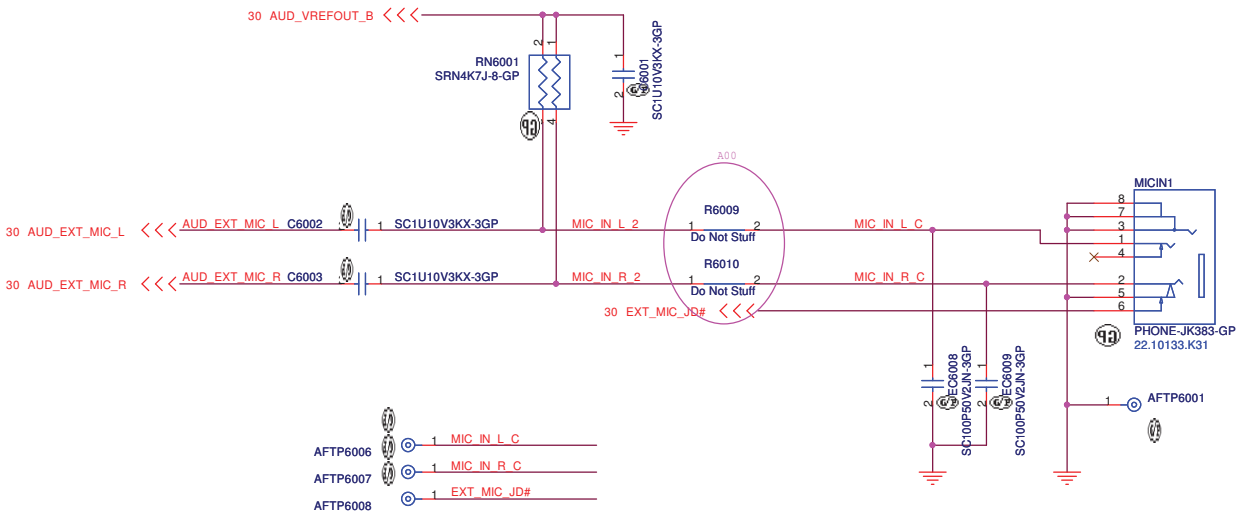
LINE1 OUT



Internal Microphone



MIC IN



DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Jack/Mic/Speaker	
Size A3	Document Number DJ1 Montevina UMA	Rev A00
Date: Friday, February 26, 2010	Sheet 60 of 88	

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DJ1

Wistron Corporation
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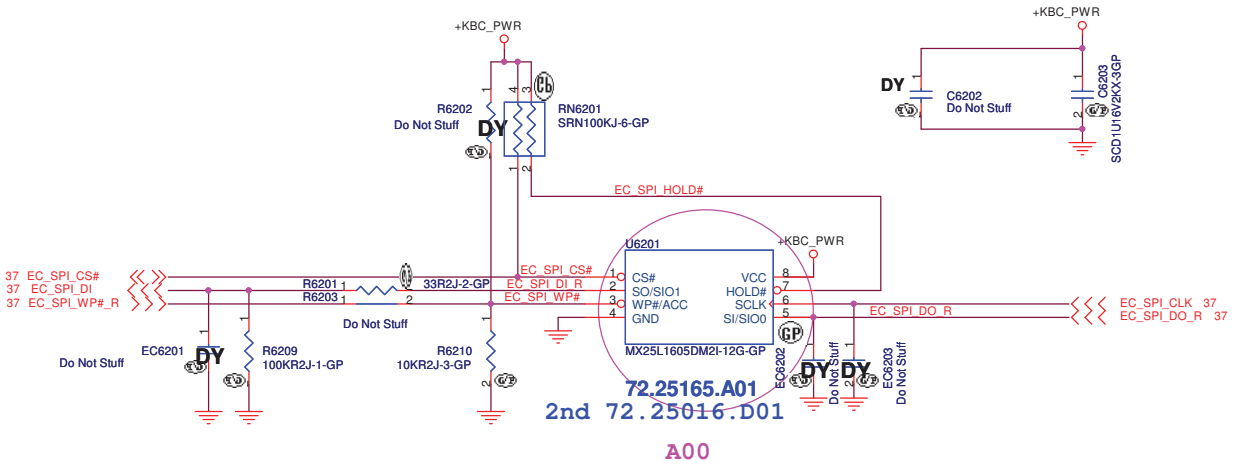
Title: Reserved

Size: A3 | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 61 of 88

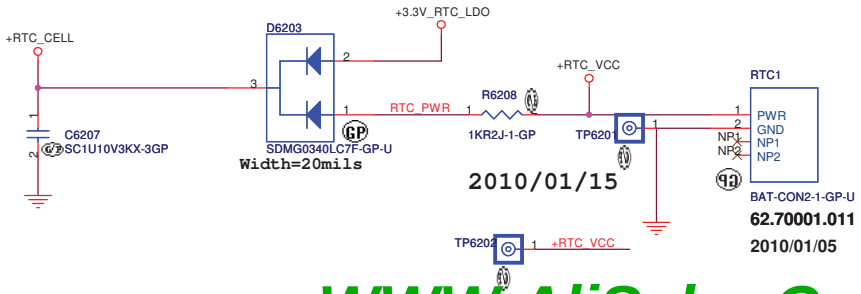
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



DJ1

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Title: Flash/RTC

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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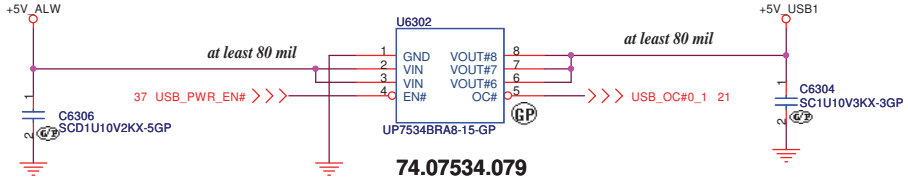
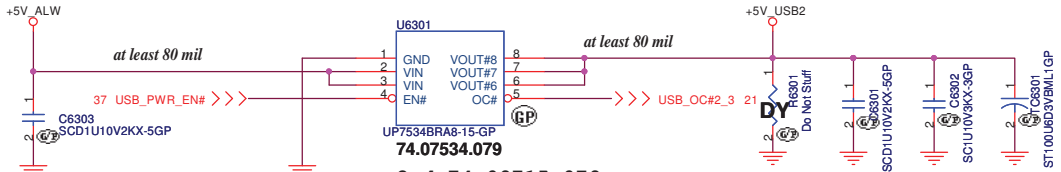
SSID = USB

IO Board USB Power



74.07534.079
2nd 74.09715.079
20100111

Right USB Power

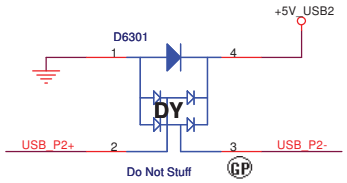


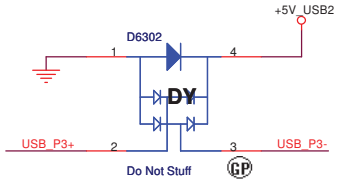
74.07534.079
2nd 74.09715.079
20100111

21 USB_PN2 — USB_PN2 — R6302 (Do Not Stuff) — USB_P2-
21 USB_PP2 — USB_PP2 — R6303 (Do Not Stuff) — USB_P2+

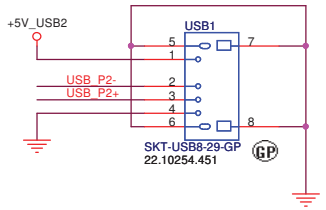
2010/01/05

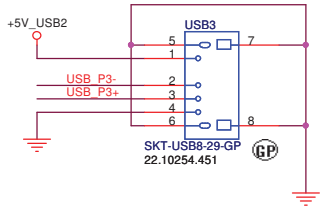
21 USB_PN3 — USB_PN3 — R6304 (Do Not Stuff) — USB_P3-
21 USB_PP3 — USB_PP3 — R6305 (Do Not Stuff) — USB_P3+





USB Socket





AFTP6304 — +5V_USB2
AFTP6302 — USB_P2-
AFTP6301 — USB_P2+
AFTP6306 — USB_P3-
AFTP6305 — USB_P3+

DJ1

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Title		
USB		
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DJ1

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Title: Reserved

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DJ1

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Title: Reserved

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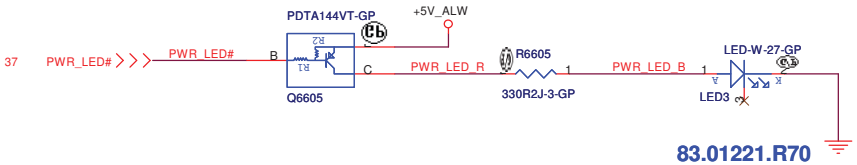
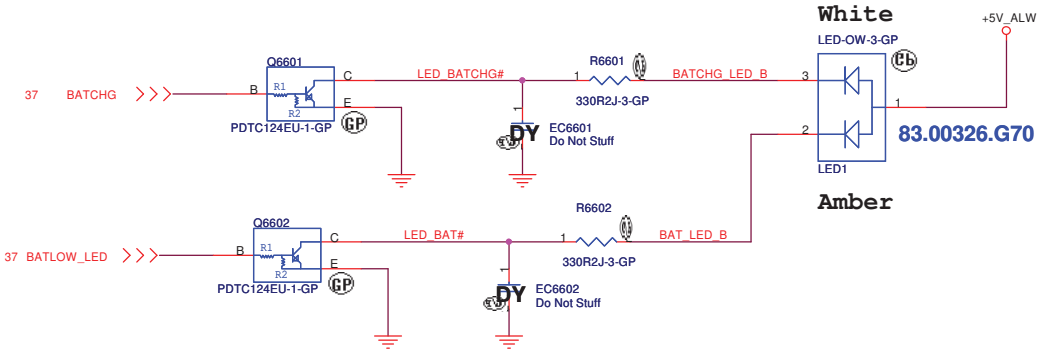
SSID = LED

Power button LED

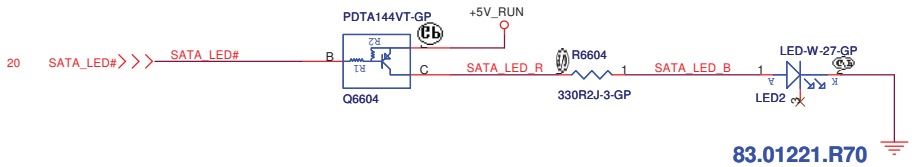
Power LED



Battery LED



HDD LED



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LED		
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
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DJ1

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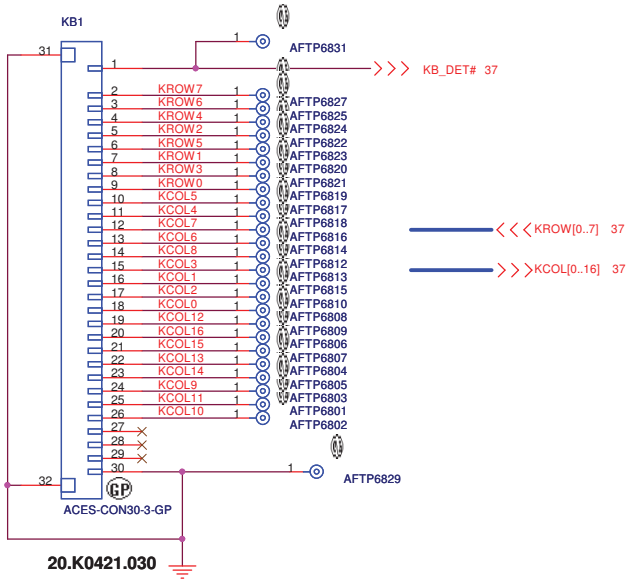
Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 67 of 88

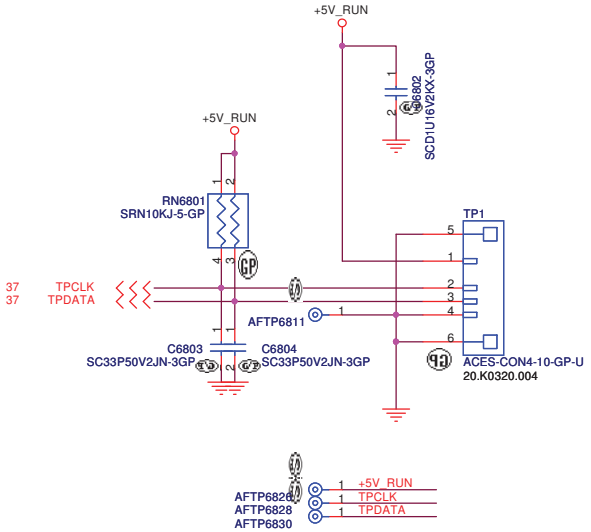
SSID = KBC

Internal KeyBoard Connector



SSID = Touch.Pad

TouchPad Connector



DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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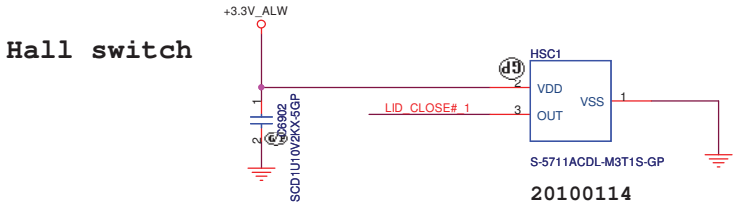
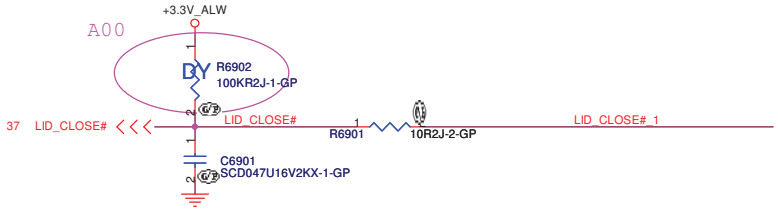
Hall switch





DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

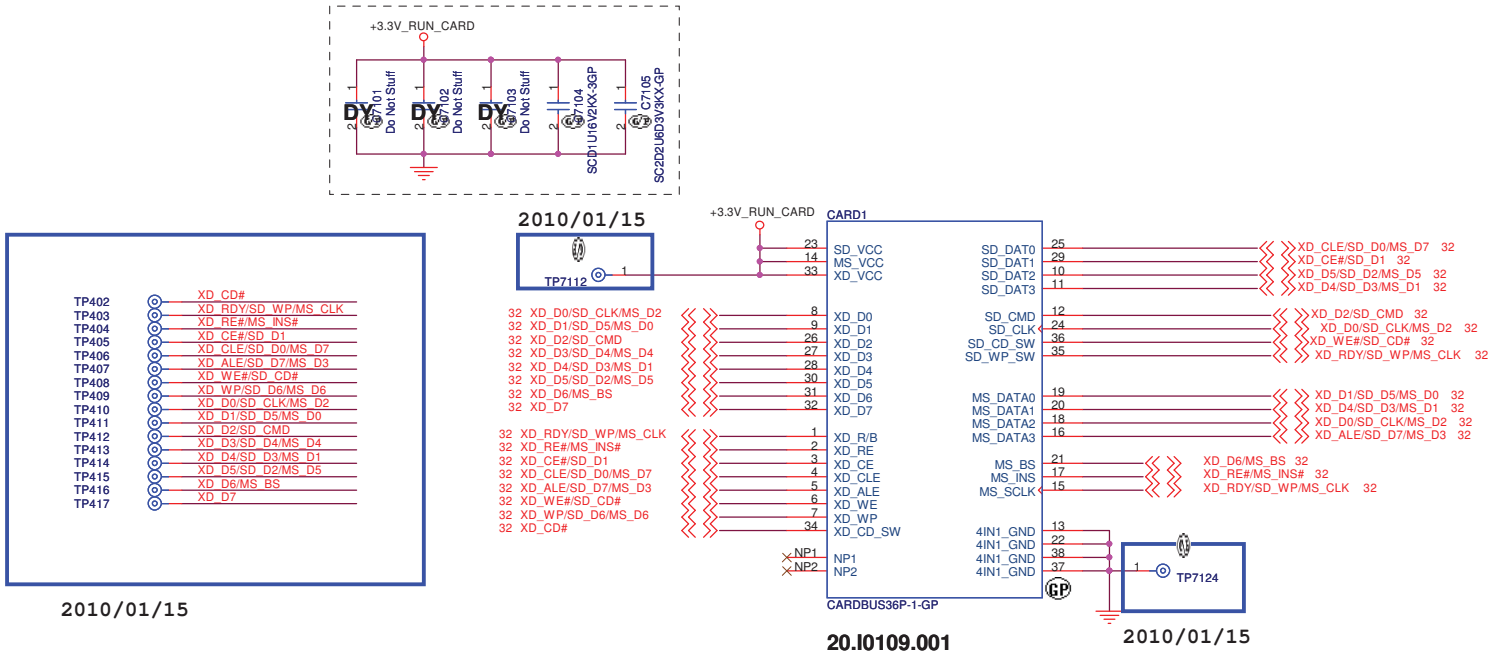
Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 70 of 88

SSID = SDIO

SD/XD/MS Card Reader



20.I0109.001

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader Connector

Size: A3 | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 71 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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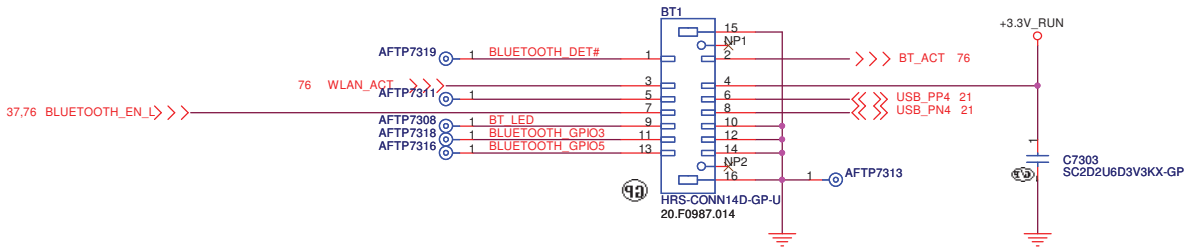
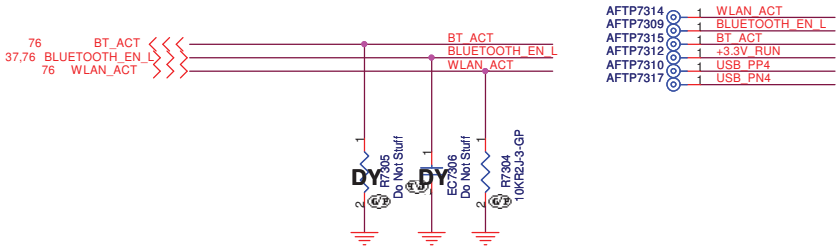
SSID = User.Interface





DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Bluetooth		
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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DJ1

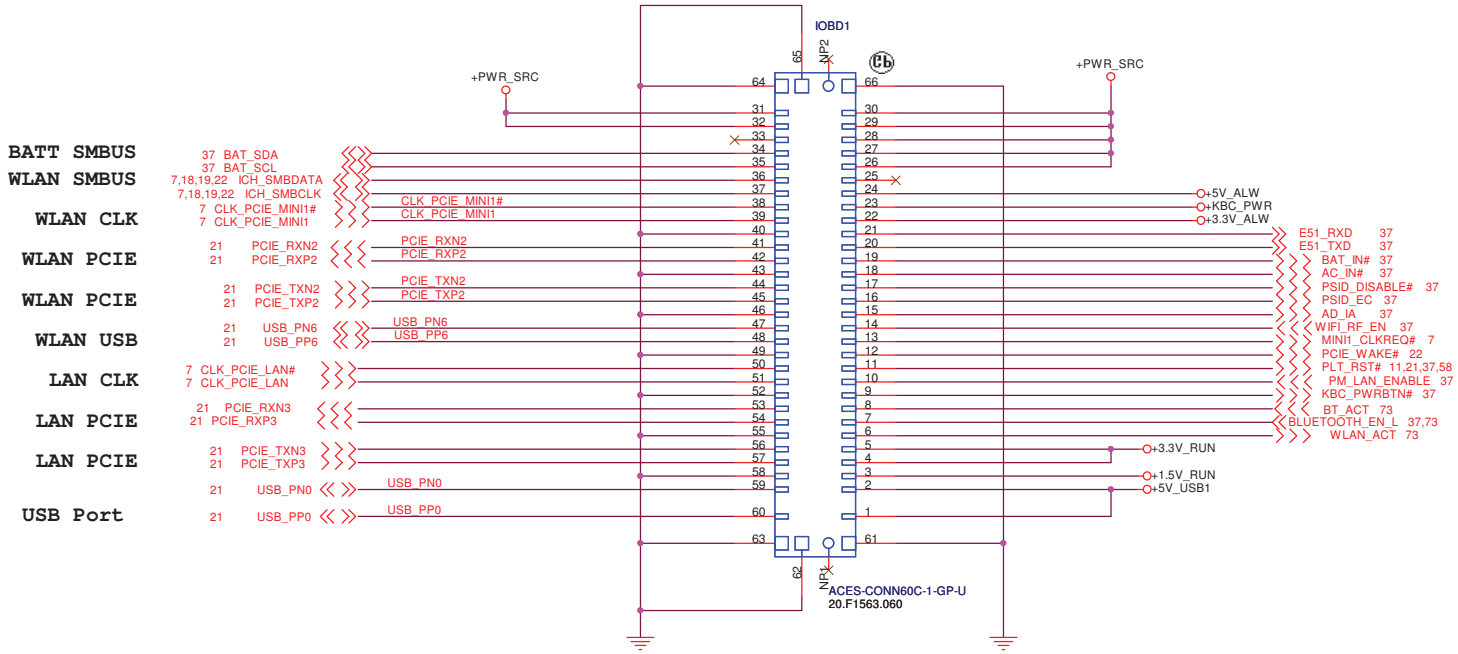
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

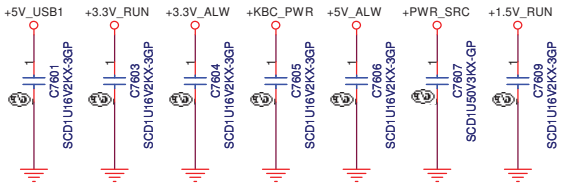
Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 75 of 88

SSID = PWR_Support



Close to IOBD Conn



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

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DJ1

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SSID = Mechanical

H21 Do Not Stuff
H22 Do Not Stuff
H23 Do Not Stuff
SPR1 SPRING-51-GP 34.4F822.002
HBT1 STF237R115H123-GP 34.4A902.001
HMI2 STF217R128H83-GP 34.4Y702.001
2nd 34.4H103.201

H3 Do Not Stuff
H2 Do Not Stuff
H6 Do Not Stuff
H1 Do Not Stuff
H7 Do Not Stuff
H4 Do Not Stuff
H13 Do Not Stuff
H18 Do Not Stuff
H8 Do Not Stuff
H20 Do Not Stuff

+PWR_SRC SCD1U50V3KX-GP EC7901
+PWR_SRC SCD1U50V3KX-GP EC7902
+PWR_SRC SCD1U50V3KX-GP EC7903
+PWR_SRC SCD1U50V3KX-GP EC7904
+PWR_SRC SCD1U50V3KX-GP EC7905
+PWR_SRC SCD1U50V3KX-GP EC7906

+PWR_SRC SCD1U50V3KX-GP EC7907
+PWR_SRC SCD1U50V3KX-GP EC7908
+PWR_SRC SCD1U50V3KX-GP EC7909
+PWR_SRC SCD1U50V3KX-GP EC7910
+PWR_SRC SCD1U50V3KX-GP EC7911
+PWR_SRC SCD1U50V3KX-GP EC7925
+PWR_SRC SCD1U50V3KX-GP EC7926
+PWR_SRC SCD1U50V3KX-GP EC7922
+PWR_SRC Do Not Stuff DY EC7923
+PWR_SRC Do Not Stuff DY EC7924

+PWR_SRC SCD1U50V3KX-GP EC7912
+PWR_SRC SCD1U50V3KX-GP EC7913
+1.5V_SUS_P Do Not Stuff DY EC7914

+1.05V_VCCP Do Not Stuff DY EC7921
+1.05V_VCCP Do Not Stuff DY EC7915
+1.05V_VCCP Do Not Stuff DY EC7916
+1.05V_VCCP Do Not Stuff DY EC7917

+5V_RUN SCD1U50V3KX-GP EC7927
+5V_RUN SCD1U50V3KX-GP EC7928
+5V_RUN SCD1U50V3KX-GP EC7929

+3.3V_RUN SCD1U50V3KX-GP EC7918
+3.3V_RUN SCD1U50V3KX-GP EC7919
+3.3V_RUN SCD1U50V3KX-GP EC7920

+3.3V_RUN SCD1U50V3KX-GP EC7936
+3.3V_RUN SCD1U50V3KX-GP EC7937
+3.3V_RUN SCD1U50V3KX-GP EC7938

+5V_ALW SCD1U50V3KX-GP EC7930
+5V_ALW SCD1U50V3KX-GP EC7931
+5V_ALW SCD1U50V3KX-GP EC7932
+5V_ALW SCD1U50V3KX-GP EC7933
+5V_ALW Do Not Stuff DY EC7934

G6002 Do Not Stuff
G6003 Do Not Stuff
G6004 Do Not Stuff

EMI Request

2010/01/07

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	20	2010/01/04	Wistron	R2018.R2019 to J accurity	Change R2018 R2019 to 63.33434.1DL	X01
2	54	2010/01/04	Wistron	D4102 Change	D4102 change to 83.00054.Q81	X01
3	37	2010/01/04	Wistron	MB version chang to X01	Change R3722 pop,R3727 dummy.	X01
4	59	2009/01/06	Wistron	ME change ODD&RTC Conn	Change ODD Conn to 22.10300.811 Change RTC Conn to 62.70001.011	X01
5	79	2009/01/07	Wistron	EMI Request	Add EC7927 EC7928 EC7929 EC7936 EC7937 EC7938 EC7930 EC7931 EC7932 EC7933 EC7934 POP EC7913 EC7912 EC7925 EC7922 EC7926 PC4610 PC4615	X01
6	54 32 63	2010/01/07	Wistron	USB layout change	Del TR5401 TR3201 TR6301 TR6302 Change R5409 R5412 R3211 R3210 R6302 R6303 R6304 R6305 to 0ohm	X01
7	42	2010/01/07	Wistron	Change R4210 for POP noise	Change R4210 to 10K 63.10334.1DL	X01
8	60	2010/01/08	IDT	IDT Request change EMI CAP to 0.01u	EC6005 EC6006 change to 0.01u 78.10321.2FL	X01
9	63	2010/01/11	Wistron	USB power switch change	Change U6301 U6302 to 74.07534.079	X01
10	37	2010/01/12	Wistron	Prevent BIOS damage	POP U3702 74.00690.I7B	X01
11	37	2010/01/12	DELL	Add one capacitor for IPCC function	Add C3721 close KBC Pin AD_IA	X01
12	69	2010/01/14	Wistron	SMT issue	Change HSC1 layout symbol to Seiko 74.05711.07B	X01
13	47 49 50	2010/01/16	Wistron	Power team request	change PC4740 PC4741 PC4910 PC5020to 78.33124.2FL	X01
14	46	2010/01/18	Wistron	Power team request	DY PTC4603.change PTC5001 PTC4602	X01
15	37	2010/02/10	Wistron	U3702 reset timing is too long	DY U3702	A00
16	37	2010/02/10	Wistron	Change PCB version from X01 to A00	DY R3722 and R3728, stuff R3727 and R3723	A00
17	20 37 55	2010/02/24	Wistron	Change 0ohm to short pad.	Change R2014 R3725 R3748 R5505 R5506 R3012 R3014 R3018 RN5901 R6009 R6010	A00
18	37	2010/02/24	DELL	Add one FET for RCID function	Reserve Q3706	A00
19	69	2010/02/25	Wistron	Do not stuff R6902	Reserve R6902	A00

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