UM7B DISCRETE SYSTEM DIAGRAM

+3V/+5V
(RT8206BGQW)
PG.42

+1.05V
1.05V_PCH(RT8209A)
PG.48

CPU Core
(ADP3212)
PG.45

VGA Core/+1.1V
VGA_ATI park(RT8208A)
PG.49

+1.5V/+0.75V
1.5_DDR/0.75(RT8207A)
PG.43

+1.05VTT/+1.8V
1.05V_VTT(RT8204B)
PG.44

Charger
Charger (ISL88731)
PG.41

14.318MHz
CLOCK GEN
PG.3

SODIMM1
Max. 4GB
PG.13

DDR3
Channel A

SODIMM2
Max. 4GB
PG.14

DDR3
Channel B

INTEL
Arrandale
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.4~7

PCI-E x16

ATI
PARK-S3
23mm X 23mm
TDP 8W
PG.15~19

THERMAL
PG.16

HDMI
HDMI PG.28

CRT
CRT PG.23

LVDS
LVDS PG.22

DDR3 800MHz
VRAM
64Mx16x8,64bit
PG.20,21

DMI

FAN & THERMAL
GMT G990/
EMC1422-1-AIZL-TR PG.37

INTEL PCH
Ibex Peak-m
27mm X 25mm
1071pin FCBGA
TDP 5W
PG.8~12

SATA0
HDD
PG.35

PCI-E x 1
LANE6
LANE2

LAN
Atheros/AR8152
10/100
PG.38

WLAN
PG.32

USB 2.0
PORT4

SATA4

USB+eSATA
Combo port
PG.33

USB 2.0
PORT0

USB2.0 Ports
X2
PG.24, 33

Webcam
PG.22

USB 2.0
PORT1,2
PORT11
PORT12
PORT8

Card Reader
RTS5138
PG.25

BT
BT365
PG.32

Azalia

LPC

KBC
ITE 8502
PG.29

KB
PG.34

TP
PG.34

1M ROM
PG.30

4M ROM
PG.30

AUDIO
CODEC
ALC269-VB2-GR
PG.26

Speaker
PG.26

HP/MIC
PG.27

Analog MIC
PG.26

Stackup
TOP
GND
IN1
IN2
VCC
BOT

Quanta Computer Inc.
PROJECT : UM7 DIS

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	BLOCK DIAGRAM	3A

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Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	23,42,43,44,45,46,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	09,12,30,31	RTC		S0~S5
					S0~S5
+5V_ALW	+5V	37,43,44,47,48	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	30,31,37,42,43,45,47,48	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	12,25,34,37,43,44,45,46,47,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	03,08,09,10,11,12,23,35,37,39,41,46,47,50	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	04,06,14,15,44,47	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	14,15,44	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	08,12,23,24,27,28,29,35,36,3738,47	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,4,8,9,10,11,12,14,15,23,24,26,27,28,29,30 ,31,33,34,36,37,38,39,41,47	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	6,12,45	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	4,6,11,12,45,46	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	12,33,47	PCH/Min Card	RUN_ON	
+1.05V_PCH	+1.05V	3,8,9,10,12,49	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	6,46	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	23	LCD Power	LCDVCC_TST_EN & ENVDD	

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

Quanta Computer Inc.

PROJECT : UM7 DIS

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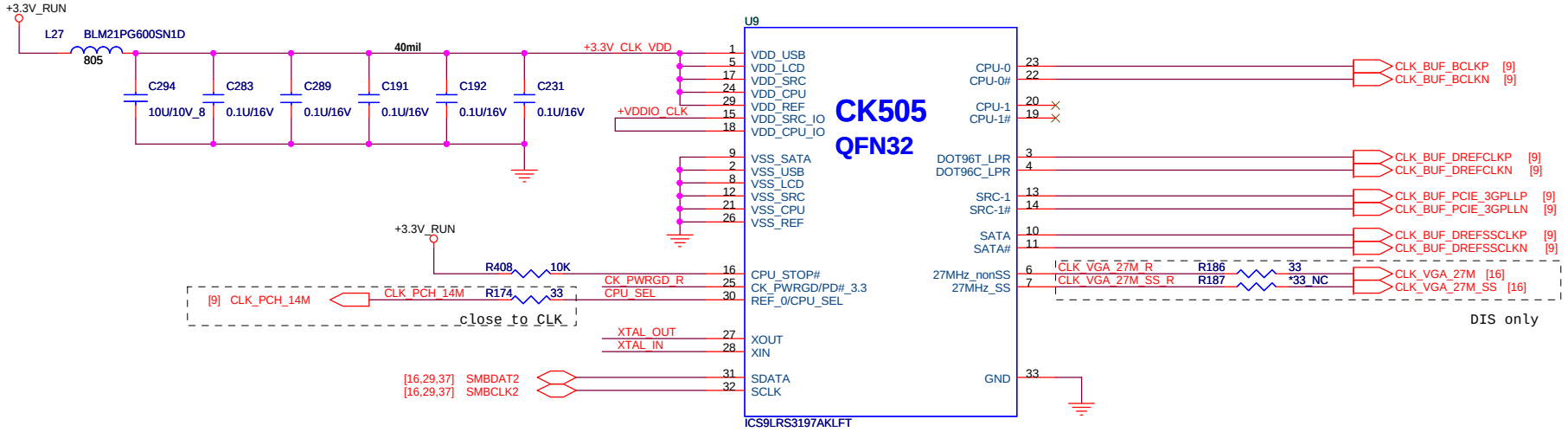
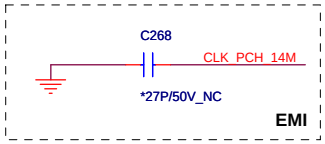
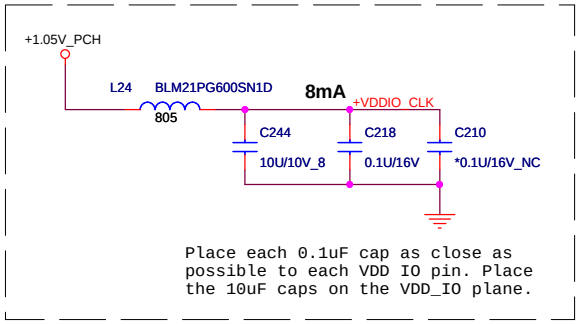
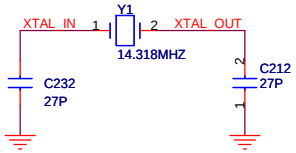
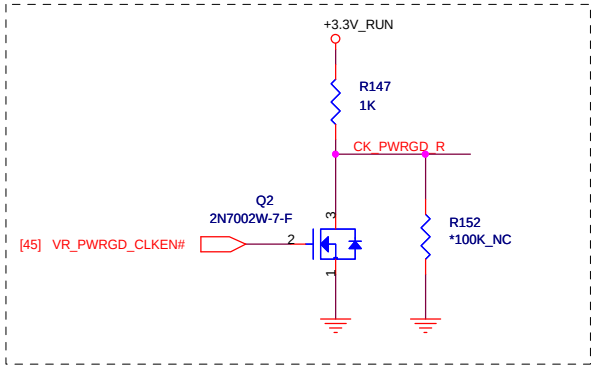


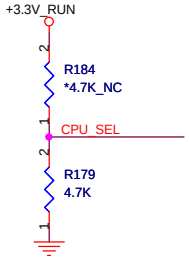
AL003197000IC OTHER(32P)ICS9LRS3197AKLFT(QFN)
~~AL8SP585000IC OTHER(32P)SLG8SP585VTR(QFN)~~
AL8SP590000IC OTHER(32P)SLG8SP590VTR(QFN)











PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Clock Generator	3A
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change PN

U16A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

U16B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

PAD on trace

For ITP CLk

DIS connect GND

PREQ TP not too long

*short0402_NC

R370

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

CPU THERMTRIP

Q24 *2N7002W-7-F_NC

Q23 *MMST3904-7-F_NC

*2.2K/J_4_NC

JTAG

Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins.

R83 *short0402_NC

R52 1.1K/F

R54 3K/F

Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

Quanta Computer Inc.

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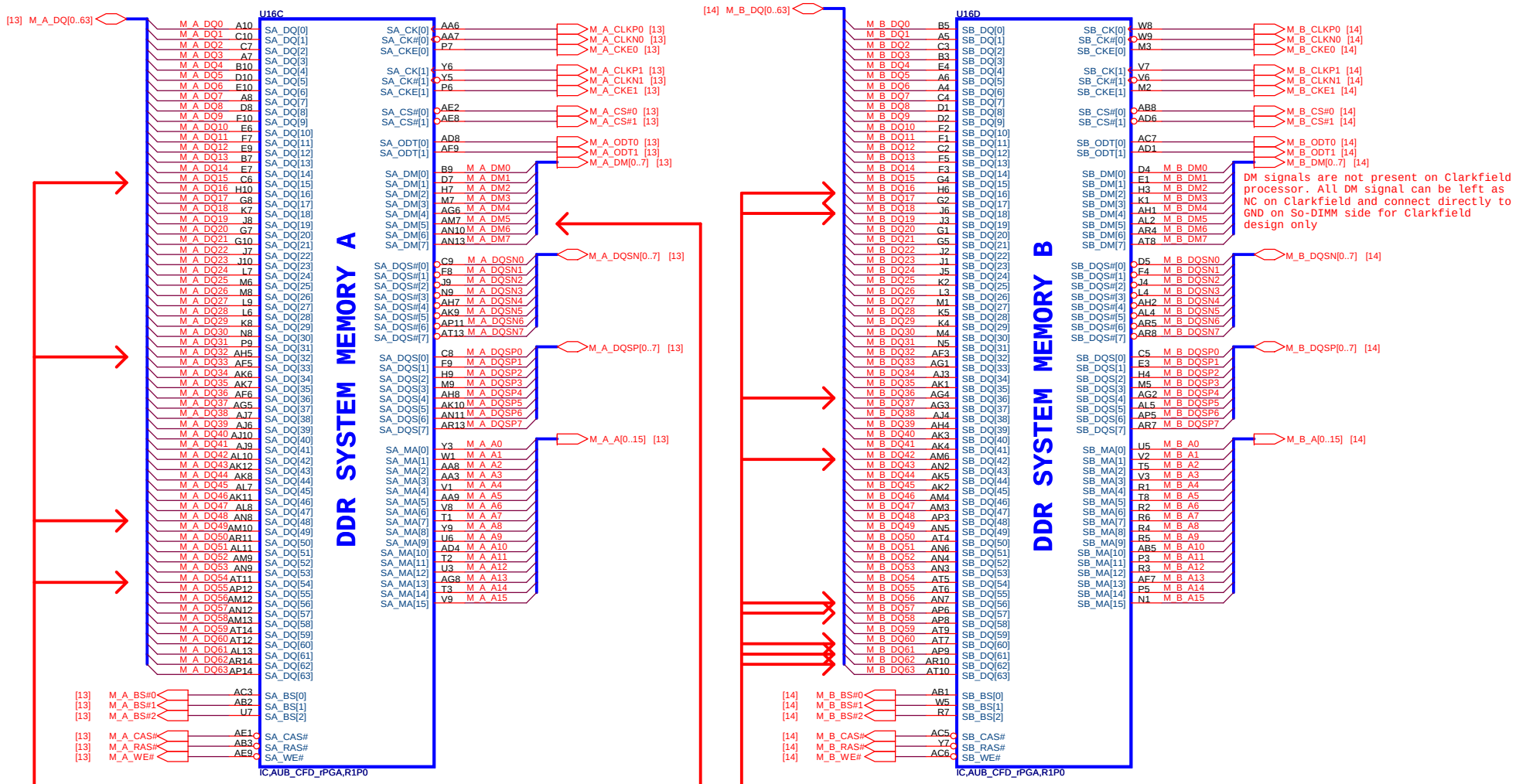
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.

PROJECT : UM7 DIS

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	PROCESSER 2/4(DDR)	3A

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18A

U16F

+VCC_CORE

C506 22U/6.3V_8
C40 22U/6.3V_8
C518 22U/6.3V_8
C23 22U/6.3V_8
C116 22U/6.3V_8
C493 22U/6.3V_8
C507 22U/6.3V_8
C119 22U/6.3V_8
C510 22U/6.3V_8
C90 22U/6.3V_8
C494 *22U/6.3V_8_NC
C111 *22U/6.3V_8_NC
C512 10U/6.3V_8
C509 10U/6.3V_8
C99 10U/6.3V_8
C45 10U/6.3V_8
C81 10U/6.3V_8
C495 10U/6.3V_8
C34 10U/6.3V_8
C120 10U/6.3V_8
C492 10U/6.3V_8
C117 10U/6.3V_8
C118 *10U/6.3V_8_NC
C101 *10U/6.3V_8_NC
C508 *10U/6.3V_8_NC
C104 *10U/6.3V_8_NC
C122 *10U/6.3V_8_NC
C121 *10U/6.3V_8_NC

CPU CORE SUPPLY

POWER

1.1V RAIL POWER

VTT0_1 AH14 → +1.05V_VTT
VTT0_2 AH12
VTT0_3 AH11 C511 10U/6.3V_8
VTT0_4 AH10 C501 10U/6.3V_8
VTT0_5 AJ14 C481 10U/6.3V_8
VTT0_6 J13 C545 10U/6.3V_8
VTT0_7 H14 C147 *10U/6.3V_8_NC
VTT0_8 H12 C484 *10U/6.3V_8_NC
VTT0_9 G14 C146 *10U/6.3V_8_NC
VTT0_10 G13 C82 *10U/6.3V_8_NC
VTT0_11 G12 C78 *10U/6.3V_8_NC
VTT0_12 G11 C515 22U/6.3V_8
VTT0_13 F14 C70 22U/6.3V_8
VTT0_14 F13 C504 *22U/6.3V_8_NC
VTT0_15 F12
VTT0_16 F11
VTT0_17 E14
VTT0_18 E12
VTT0_19 D14
VTT0_20 D13
VTT0_21 D12
VTT0_22 D11
VTT0_23 C14
VTT0_24 C13
VTT0_25 C12
VTT0_26 C11
VTT0_27 B14
VTT0_28 B12
VTT0_29 A14
VTT0_30 A13
VTT0_31 A12
VTT0_32 A11

VTT0_33 AF10 → +1.05V_VTT
VTT0_34 AE10
VTT0_35 AC10 C67 *22U/6.3V_8_NC
VTT0_36 AB10 C68 22U/6.3V_8
VTT0_37 Y10
VTT0_38 W10
VTT0_39 U10
VTT0_40 T10
VTT0_41 J12
VTT0_42 J11
VTT0_43 J16
VTT0_44 J15

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

CPU VIDS

PSI# AN33 H_PSI# → H_PSI# [45]

VID[0] AK35 VID0 → VID0 [45]
VID[1] AK33 VID1 → VID1 [45]
VID[2] AK34 VID2 → VID2 [45]
VID[3] AL35 VID3 → VID3 [45]
VID[4] AL33 VID4 → VID4 [45]
VID[5] AM33 VID5 → VID5 [45]
VID[6] AM35 VID6 → VID6 [45]
PROC_DPRSLPVR AM34 DPRSLPVR → DPRSLPVR [45]

VTT_SELECT G15 TP38

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE AN35 I_MON [45]
VTT_SENSE B15 → VTT_SENSE [44]
VSS_SENSE_VTT A15 TP39

R303 100/F +VCC_CORE
VCC_SENSE AJ34 → VCCSENSE [45]
VSS_SENSE AJ35 → VSSSENSE [45]
R306 100/F

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

IC,AUB_CFD_rPGA,R1P0

U16G

GRAPHICS POWER

SENSE LINES

VAXG_SENSE AR22
VSSAXG_SENSE AT22

GRAPHICS VIDs

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

Pop it when Arrandale Graphics disable.
R80 1K
DIS different UMA

2A

DDR3 - 1.5V RAILS

VDDQ1 AJ1 → +1.5V_SUS
VDDQ2 AF1 C80 1U/6.3V
VDDQ3 AE7 C86 1U/6.3V
VDDQ4 AE4 C88 1U/6.3V
VDDQ5 AC1 C83 1U/6.3V
VDDQ6 AB7 C75 *1U/6.3V_NC
VDDQ7 AB4 C77 22U/6.3V_8
VDDQ8 V1 C60 *22U/6.3V_8_NC
VDDQ9 W7
VDDQ10 W4 C100 *330U_NC
VDDQ11 U1
VDDQ12 T7
VDDQ13 T4
VDDQ14 P1
VDDQ15 N7
VDDQ16 N4
VDDQ17 L1
VDDQ18 H1

FDI

+1.05V_VTT C71 22U/6.3V_8 C478 *22U/6.3V_8_NC
J24 VTT1_45
J23 VTT1_46
H25 VTT1_47

PEG & DMI

+1.05V_VTT C546 22U/6.3V_8 C148 22U/6.3V_8 C149 *22U/6.3V_8_NC C72 *22U/6.3V_8_NC
K26 VTT1_48
J27 VTT1_49
J26 VTT1_50
J25 VTT1_51
H27 VTT1_52
G28 VTT1_53
G27 VTT1_54
G26 VTT1_55
F26 VTT1_56
E26 VTT1_57
E25 VTT1_58

1.1V

P10
N10 C488 10U/6.3V_8 → +1.05V_VTT
L10 C496 *10U/6.3V_8_NC
K10 C479 22U/6.3V_8
J22 C480 *22U/6.3V_8_NC
J20
J18
H21
H20
H19

VTT0_59
VTT0_60
VTT0_61
VTT0_62
VTT1_63
VTT1_64
VTT1_65
VTT1_66
VTT1_67
VTT1_68

1.8V

VCCPLL1 L26 C69 22U/6.3V_8 → +1.8V_RUN
VCCPLL2 L27 C63 4.7U/6.3V_6
VCCPLL3 M26 C73 *2.2U/6.3V_6_NC
C64 1U/6.3V
C482 *1U/6.3V_NC

IC,AUB_CFD_rPGA,R1P0

VID0 R394 1K
R393 *1K_NC
VID1 R381 1K
R380 *1K_NC
VID2 R378 1K
R379 *1K_NC
VID3 R392 *1K_NC
R395 1K
VID4 R371 *1K_NC
R372 1K
VID5 R374 1K
R373 *1K_NC
VID6 R388 *1K_NC
R389 1K
DPRSLPVR R376 1K
R375 *1K_NC
H_PSI# R391 *1K_NC
R390 1K
→ +1.05V_VTT

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
PROJECT : UM7 DIS

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	PROCESSER 3/4(POWER)	3A
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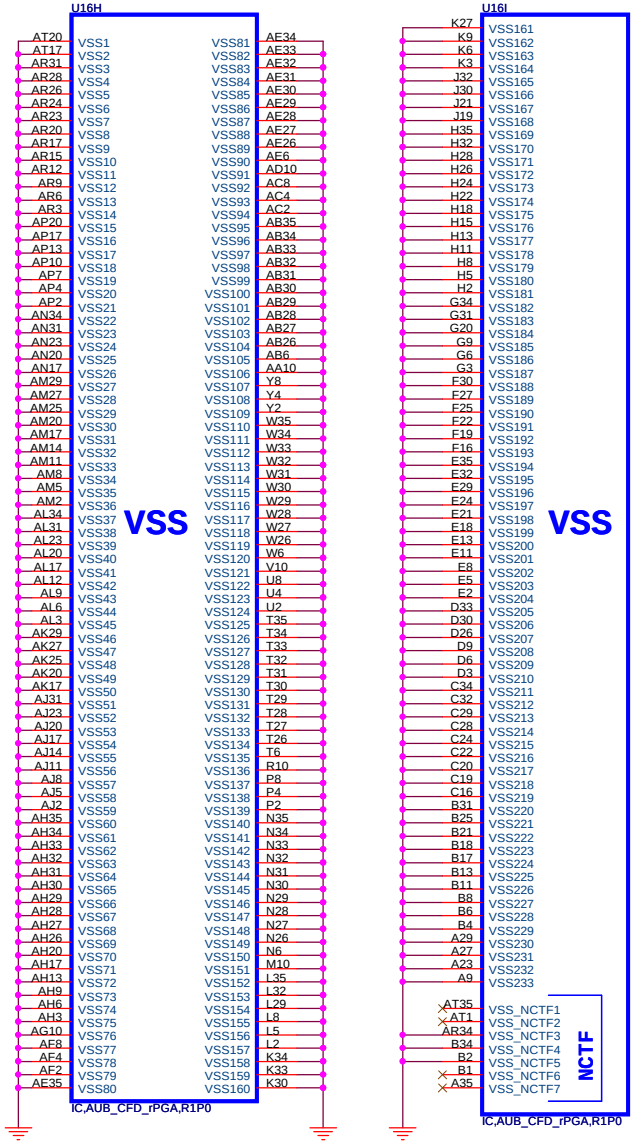
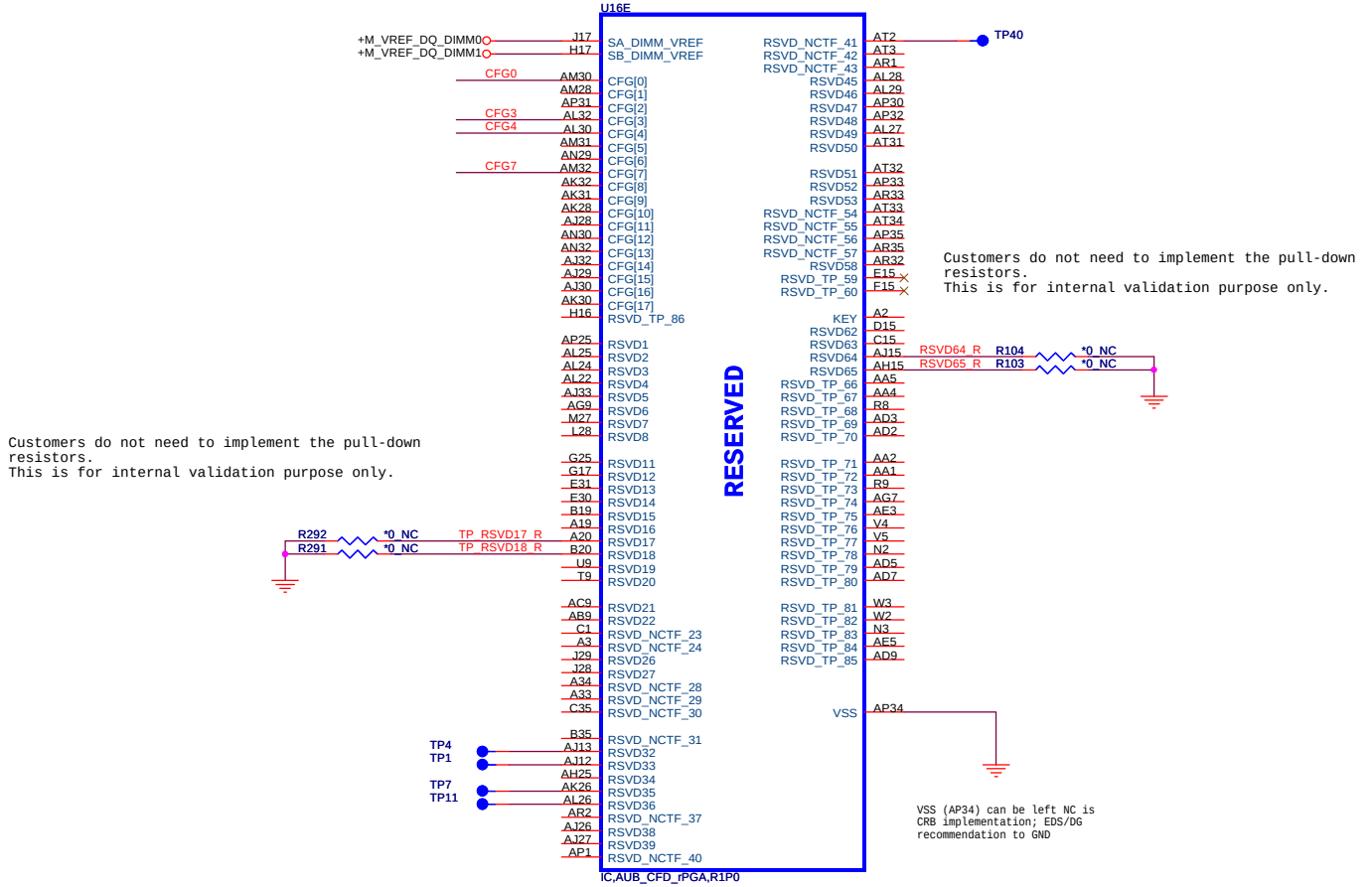
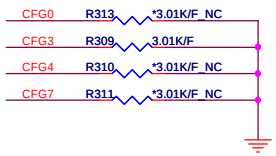
Arrandale PROCESSOR (GND)



Arrandale PROCESSOR(RESERVED, CFG)





The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

Quanta Computer Inc.
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	PROCESSER 4/4 (GND)	3A

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U23A

Ibex-M 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN# / GPIO33 (+3V), HDA_DOCK_RST# / GPIO13 (+3V_S5)
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO
LPC: FWH0 / LAD0, FWH1 / LAD1, FWH2 / LAD2, FWH3 / LAD3, FWH4 / LFRAME#, LDRQ0#, (+3V) LDRQ1# / GPIO23, SERIRQ
SATA: SATA0RXN/RXP, SATA0TXN/TXP, SATA1RXN/RXP, SATA1TXN/TXP, SATA2RXN/RXP, SATA2TXN/TXP, SATA3RXN/RXP, SATA3TXN/TXP, SATA4RXN/RXP, SATA4TXN/TXP, SATA5RXN/RXP, SATA5TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, (+3V) SATA0GP / GPIO21, (+3V_S5) SATA1GP / GPIO19

C572 18P/50V
C570 18P/50V
Y3 32.768KHZ
R428 10M
RTC_X1 B13
RTC_X2 D13
TP49 RTC_RST# C14
TP50 SRTC_RST# D17
SM_INTRUDER# A16
+RTC_CELL R441 330K_6 TP51 A14
ACZ_BITCLK A30
ACZ_SYNC D29
[26] ACZ_SPKR P1
ACZ_RST# C30
[26] ACZ_SDIN0 G30
F30
E32
F32
ACZ_SDOUT B29
[29] PCH_MELOCK H32
J30
TP47 PCH_JTAG_TCK_BUF M3
TP42 PCH_JTAG_TMS K3
TP43 PCH_JTAG_TDI K1
TP41 PCH_JTAG_TDO J2
TP44 PCH_JTAG_RST# J4
[30] SPI_CLK BA2
[30] SPI_CS0# AV3
TP48 AY3
[30] SPI_SI AY1
[30] SPI_SO AV1
SPI_SI

HDD: SATA_RXN0 [35], SATA_RXP0 [35], SATA_TXN0 [35], SATA_TXP0 [35]
SATA_TXN0_C C233 0.01U/16V
SATA_TXP0_C C221 0.01U/16V
ESATA: SATA_RXN4 [33], SATA_RXP4 [33], SATA_TXN4 [33], SATA_TXP4 [33]
SATA_TXN4_C C557 0.01U/16V
SATA_TXP4_C C556 0.01U/16V
SATA_COMP R192 37.4/F +1.05V_PCH
SATA_LED# [36]
10K R386 +3.3V_RUN
10K R159 10K R400 +3.3V_RUN

UMA CRT,LVDS&HDMI signals
IBEX PEAK-M (LVDS,DDI)

U23D

Ibex-M 4 OF 10

LVDS--A: L_BKLTEN, L_VDD_EN, L_BKLTCTL, L_DDC_CLK, L_DDC_DATA, L_CTRL_CLK, L_CTRL_DATA, LVD_IBG, LVD_VBG, LVD_VREFH, LVD_VREFL, LVDSA_CLK#, LVDSA_CLK, LVDSA_DATA#0, LVDSA_DATA#1, LVDSA_DATA#2, LVDSA_DATA#3, LVDSA_DATA0, LVDSA_DATA1, LVDSA_DATA2, LVDSA_DATA3
LVDS--B: LVDSB_CLK#, LVDSB_CLK, LVDSB_DATA#0, LVDSB_DATA#1, LVDSB_DATA#2, LVDSB_DATA#3, LVDSB_DATA0, LVDSB_DATA1, LVDSB_DATA2, LVDSB_DATA3
CRT: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC, DAC_IREF, CRT_IRTN
SDVO: SDVO_TVCLKINN/INP, SDVO_STALLN/STALLP, SDVO_INTN/INTP, SDVO_CTRLCLK, SDVO_CTRLDATA
Digital Display Interface
DISPLAY PORT B: DDPB_AUXN/AUXP, DDPB_HPD, DDPB_0N/0P, DDPB_1N/1P, DDPB_2N/2P, DDPB_3N/3P
DISPLAY PORT C: DDPC_CTRLCLK, DDPC_CTRLDATA, DDPC_AUXN/AUXP, DDPC_HPD, DDPC_0N/0P, DDPC_1N/1P, DDPC_2N/2P, DDPC_3N/3P
DISPLAY PORT D: DDPD_CTRLCLK, DDPD_CTRLDATA, DDPD_AUXN/AUXP, DDPD_HPD, DDPD_0N/0P, DDPD_1N/1P, DDPD_2N/2P, DDPD_3N/3P

TP32 TP33 LVD_IBG LVD_VBG
TP35 TP34 LVD_VREFH LVD_VREFL
R242 1K DAC_IREF

iTPM ENABLE/DISABLE

+3.3V_RUN
R406 *1K_NC SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

R384 51 PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

+3.3V_SUS Res. of TDI near PCH

R130 *200_NC R131 *200_NC R113 *200_NC R111 *20K_NC
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
R123 *100_NC R126 *100_NC R382 *100_NC R100 *10K_NC

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

For AUDIO

[26,29] ACZ_RST#_AUDIO R455 33 ACZ_RST#
[26] ACZ_SDOUT_AUDIO R450 33 ACZ_SDOUT
[26] ACZ_SYNC_AUDIO R452 33 ACZ_SYNC
[26] ACZ_BITCLK_AUDIO R205 33 ACZ_BITCLK
C324 10P/50V

+3.3V_RUN R397 *1K/F_NC ACZ_SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot

RTC 1mA

+RTC_CELL
R433 20K/F C297 1U/6.3V RTC_RST#
R439 20K/F C311 1U/6.3V SRTC_RST#
R434 1M SM_INTRUDER#

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	3A

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IBEX PEAK-M (GND)

U23I

HM57_MP

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U23B

Ibex-M
2 OF 10

PCI-E*

HM57_MP

SMBus

(+3V_S5) SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SML0ALERT# / GPIO60
SML0CLK
SML0DATA
(+3V_S5) SML1ALERT# / GPIO74
(+3V_S5) SML1CLK / GPIO58
(+3V_S5) SML1DATA / GPIO75

+3.3V_SUS

Controller Link

CL_CLK1
CL_DATA1
CL_RST1#

ICH_SMBCLK — ICH_SMBCLK [32]
ICH_SMBDATA — ICH_SMBDATA [32]

PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P

DIS different UMA

CLK_PCIE_VGAN [15]
CLK_PCIE_VGAP [15]
CLK_PCIE_3GPLLN [4]
CLK_PCIE_3GPLLP [4]

CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P

DIS different UMA

From CLK BUFFER

CLKIN_DMI_N — CLK_BUF_PCIE_3GPLLN [3]
CLKIN_DMI_P — CLK_BUF_PCIE_3GPLLP [3]
CLKIN_BCLK_N — CLK_BUF_BCLKN [3]
CLKIN_BCLK_P — CLK_BUF_BCLKP [3]
CLKIN_DOT_96N — CLK_BUF_DREFCLKN [3]
CLKIN_DOT_96P — CLK_BUF_DREFCLKP [3]
CLKIN_SATA_N / CKSSCD_N — CLK_BUF_DREFSSCLKN [3]
CLKIN_SATA_P / CKSSCD_P — CLK_BUF_DREFSSCLKP [3]
REFCLK14IN — CLK_PCH_14M [3]
CLKIN_PCILOOPBACK — CLK_PCI_FB [18]

DIS different UMA
Intel recommendation
short0402_NC

XTAL25_IN
XTAL25_OUT
XCLK_RCOMP — +1.05V_PCH

(+3V) CLKOUTFLEX0 / GPIO64
(+3V) CLKOUTFLEX1 / GPIO65
(+3V) CLKOUTFLEX2 / GPIO66
(+3V) CLKOUTFLEX3 / GPIO67

CLK_FLEX3 — CLK_48M_CARD [25]

Clock Flex

C392 10P/50V

EMI

[WLAN]
[32] PCIE_RXN1
[32] PCIE_RXP1
[32] PCIE_TXN1
[32] PCIE_TXP1
C349 0.1U/10V
C342 0.1U/10V
PCIE_TXN1_C
PCIE_TXP1_C

[LAN]
[38] PCIE_RXN6_LAN
[38] PCIE_RXP6_LAN
[38] PCIE_TXN6_LAN
[38] PCIE_TXP6_LAN
C354 0.1U/10V
C350 0.1U/10V
PCIE_TXN6_LAN_C
PCIE_TXP6_LAN_C

MiniWLAN
[32] CLK_PCIE_WLANN
[32] CLK_PCIE_WLANP
[32] PCIE_CLK_REQ1#

LAN
[38] CLK_PCIE_LANN
[38] CLK_PCIE_LANP
[38] PCIE_CLK_REQB#

PCIE_CLK_REQ0# — PCIECLKRQ0# / GPIO73 (+3V_S5)
PCIE_CLK_REQ1# — PCIECLKRQ1# / GPIO18 (+3V)
PCIE_CLK_REQ2# — PCIECLKRQ2# / GPIO20 (+3V)
PCIE_CLK_REQ3# — PCIECLKRQ3# / GPIO25 (+3V_S5)
PCIE_CLK_REQ4# — PCIECLKRQ4# / GPIO26 (+3V_S5)
PCIE_CLK_REQ5# — PCIECLKRQ5# / GPIO44 (+3V_S5)
PCIE_CLK_REQB# — PEG_B_CLKRQ# / GPIO56 (+3V_S5)

+3.3V_RUN
PCIE_CLK_REQ1# R399 10K
PCIE_CLK_REQ2# R139 10K

+3.3V_SUS
PCIE_CLK_REQ0# R177 10K
PCIE_CLK_REQ3# R164 10K
PCIE_CLK_REQ4# R148 10K
PCIE_CLK_REQB# R202 10K
PCIE_CLK_REQ5# R145 10K

Q25 2N7002W-7-F
SMB_CLK_ME1 — SMBCLK1 [29]
+3.3V_SUS
SMB_DATA_ME1 — SMBDAT1 [29]
Q26 2N7002W-7-F

25M
DIS different UMA

Quanta Computer Inc.			
PROJECT : UM7 DIS			
Size	Document Number		Rev
	PCH 2/5 (PCIE, SMBUS, CK)		3A
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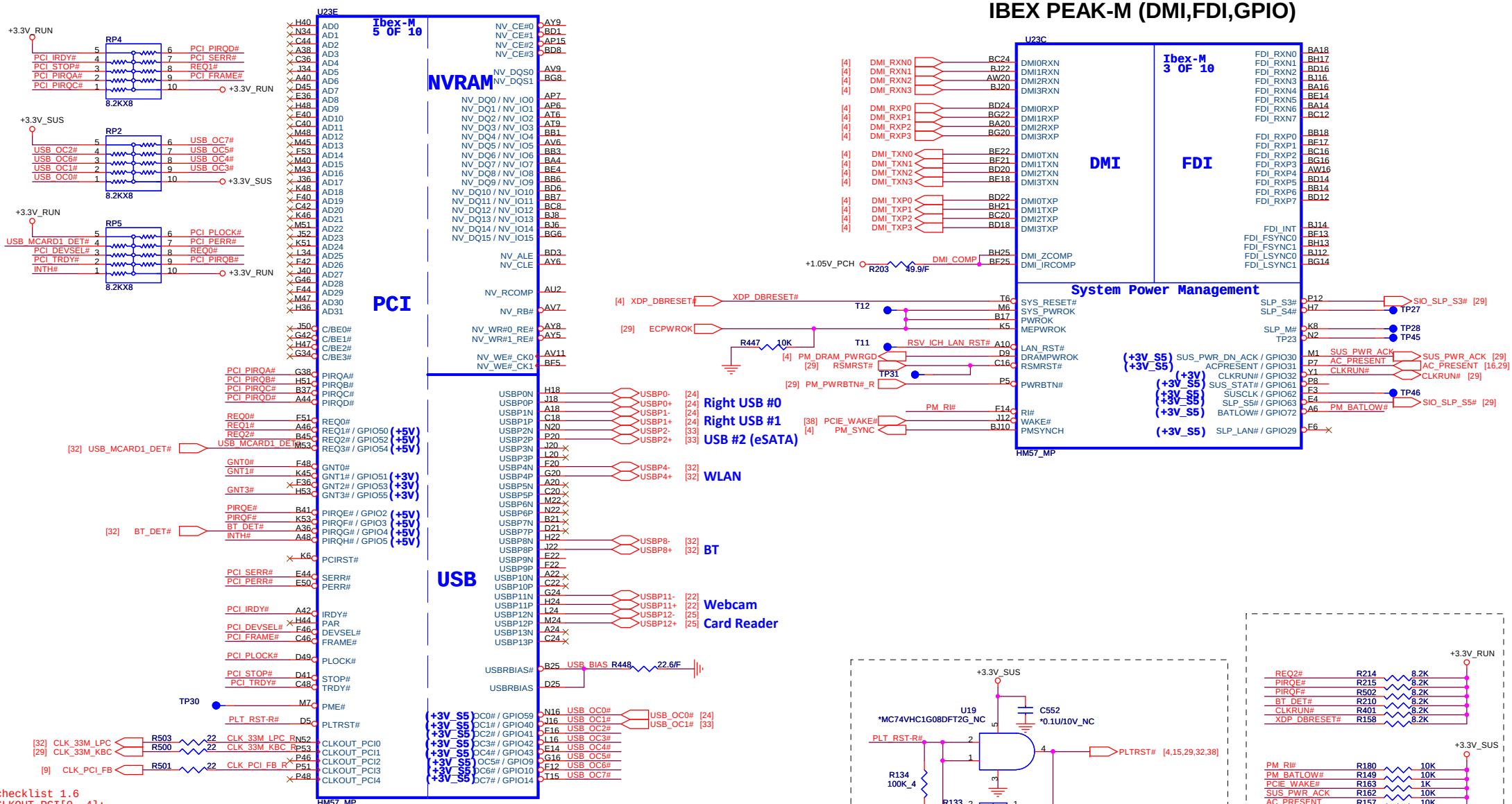
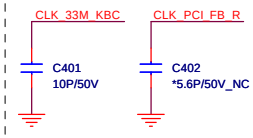
IBEX PEAK-M (PCI,USB,NVRAM)



checklist 1.6
CLKOUT_PCI[0..4]:
47 Ω to 30 Ω
(depends on number of loads)

Reserve capacitor pads for improving WWAN.



GNT0# R231 *1K_NC
GNT1# R499 *1K_NC

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

GNT3# R498 *4.7K_NC

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

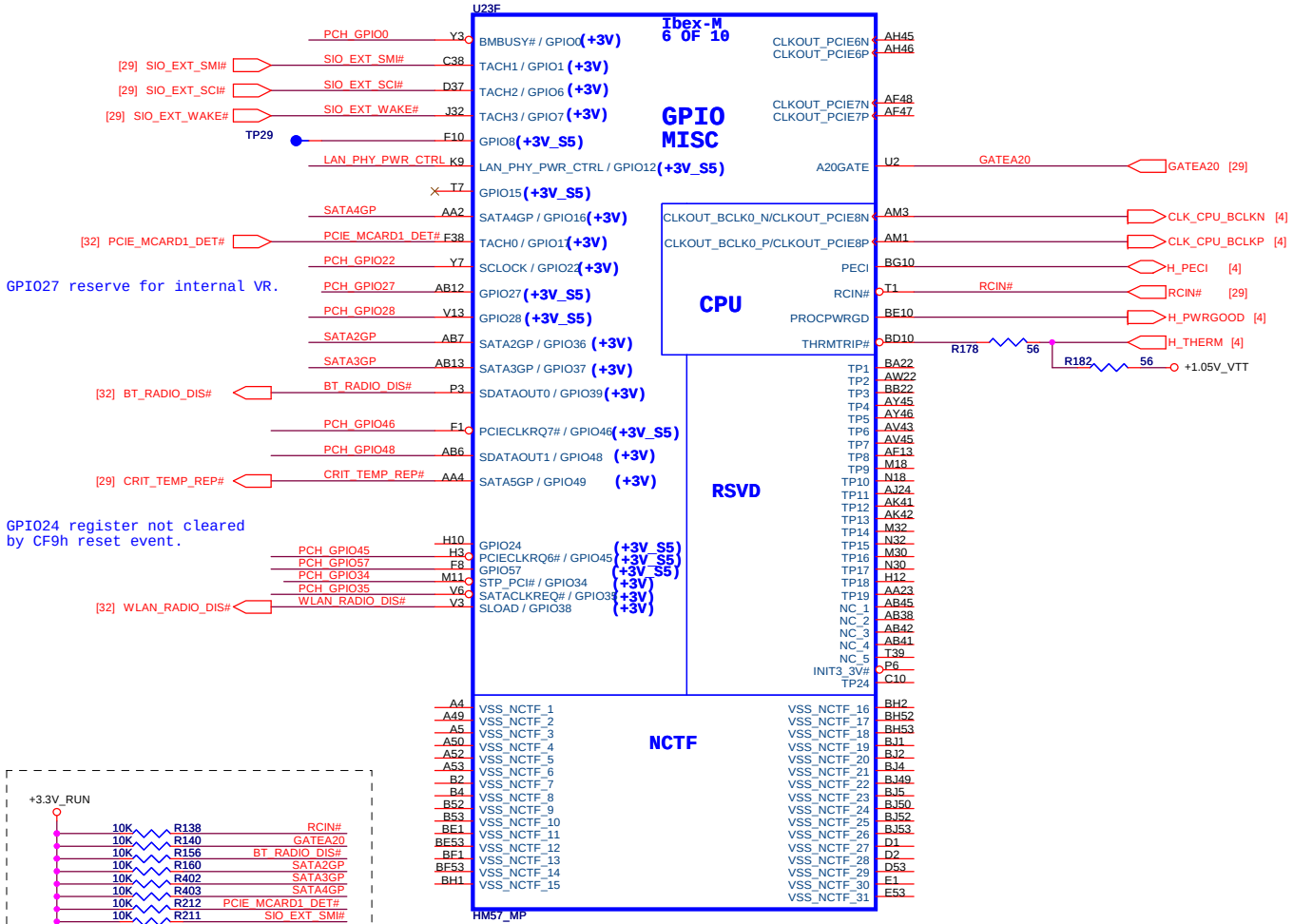
IBEX PEAK-M (DMI,FDI,GPIO)

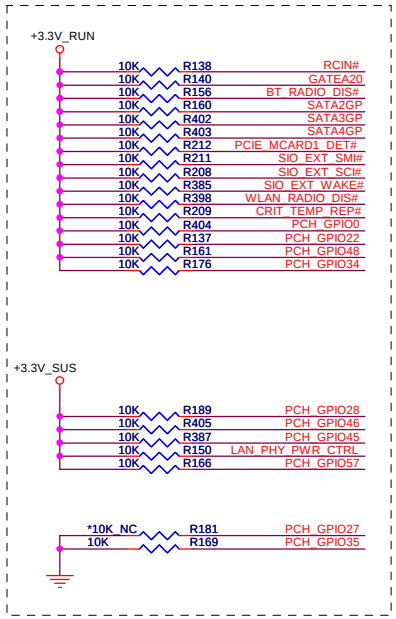
Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 3/5 (PCI,ONFI,USB,DMI)	3A

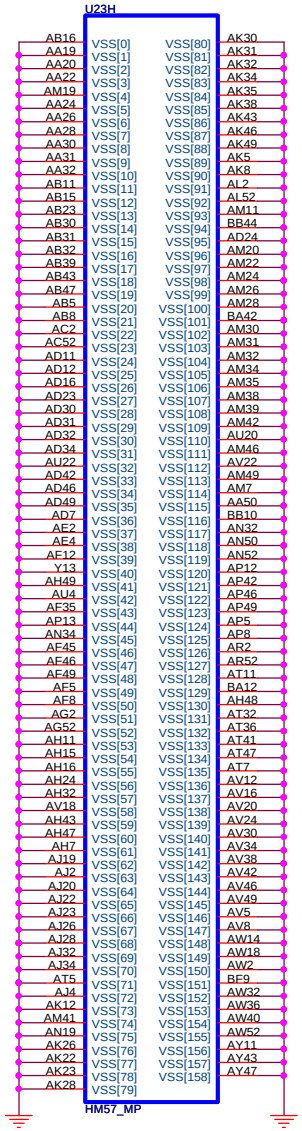
Date: Wednesday, February 03, 2010 Sheet 10 of 52

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)





IBEX PEAK-M (GND)



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	3A
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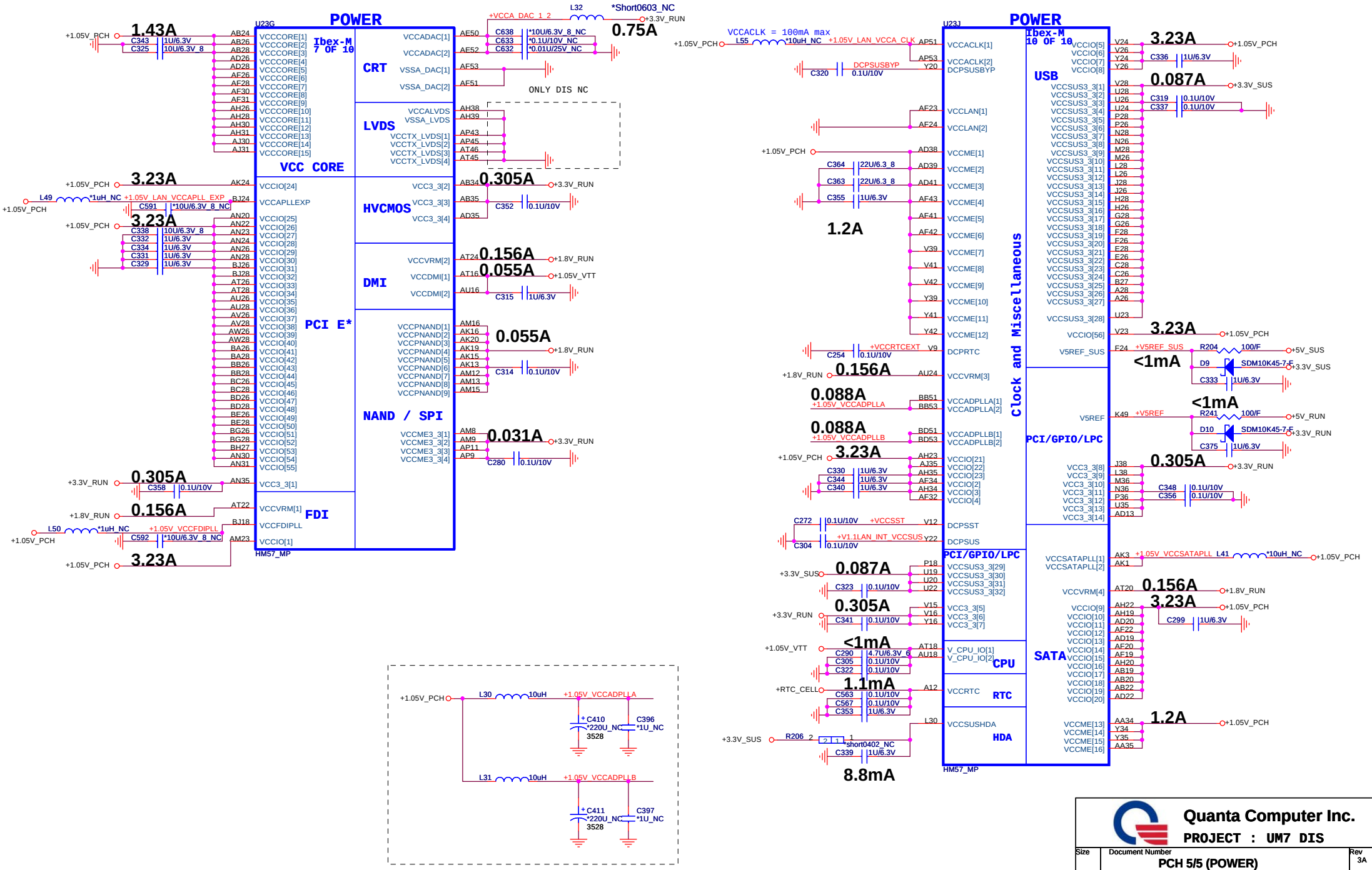
L32 UMA↓
EMI FILTER HCB1608KF-181T15(180,1.5A)
CX000181016

L32 DIS→SHORT



Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: PCH 5/5 (POWER)	Rev: 3A
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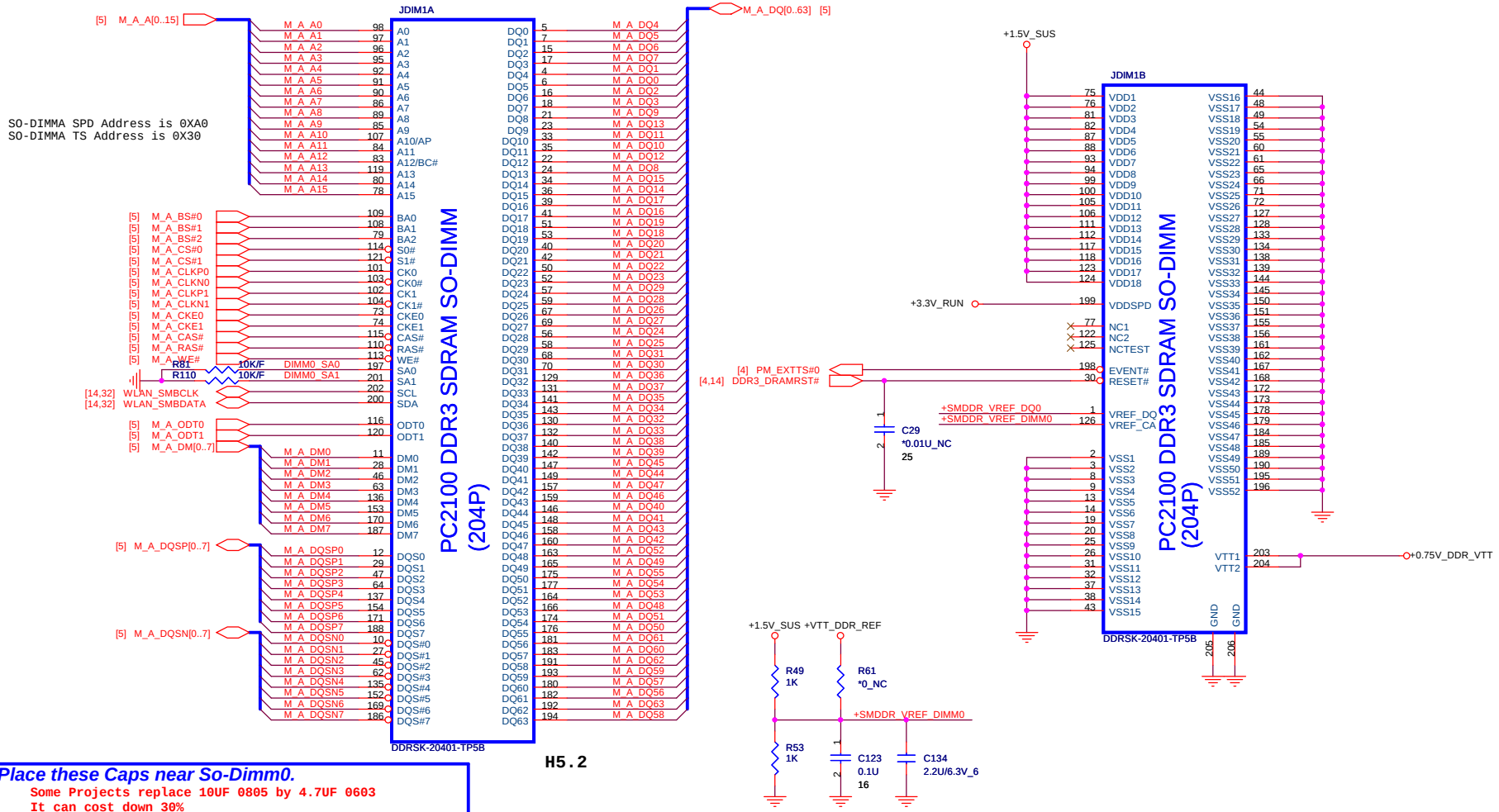
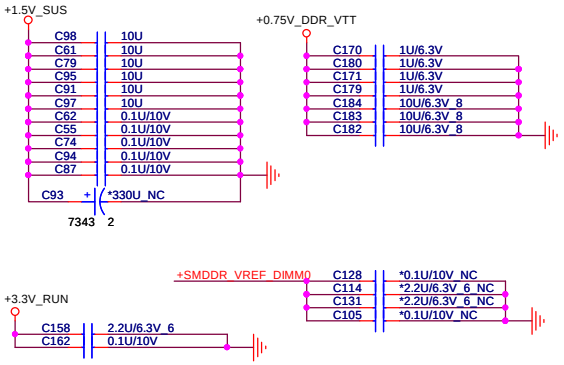


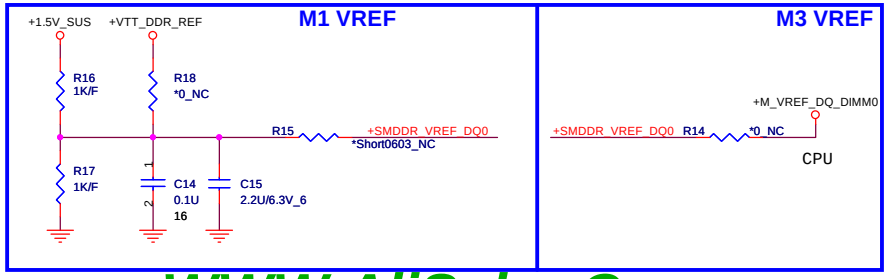
H5.2

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%





Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: DDR3 DIMM-0	Rev: 3A
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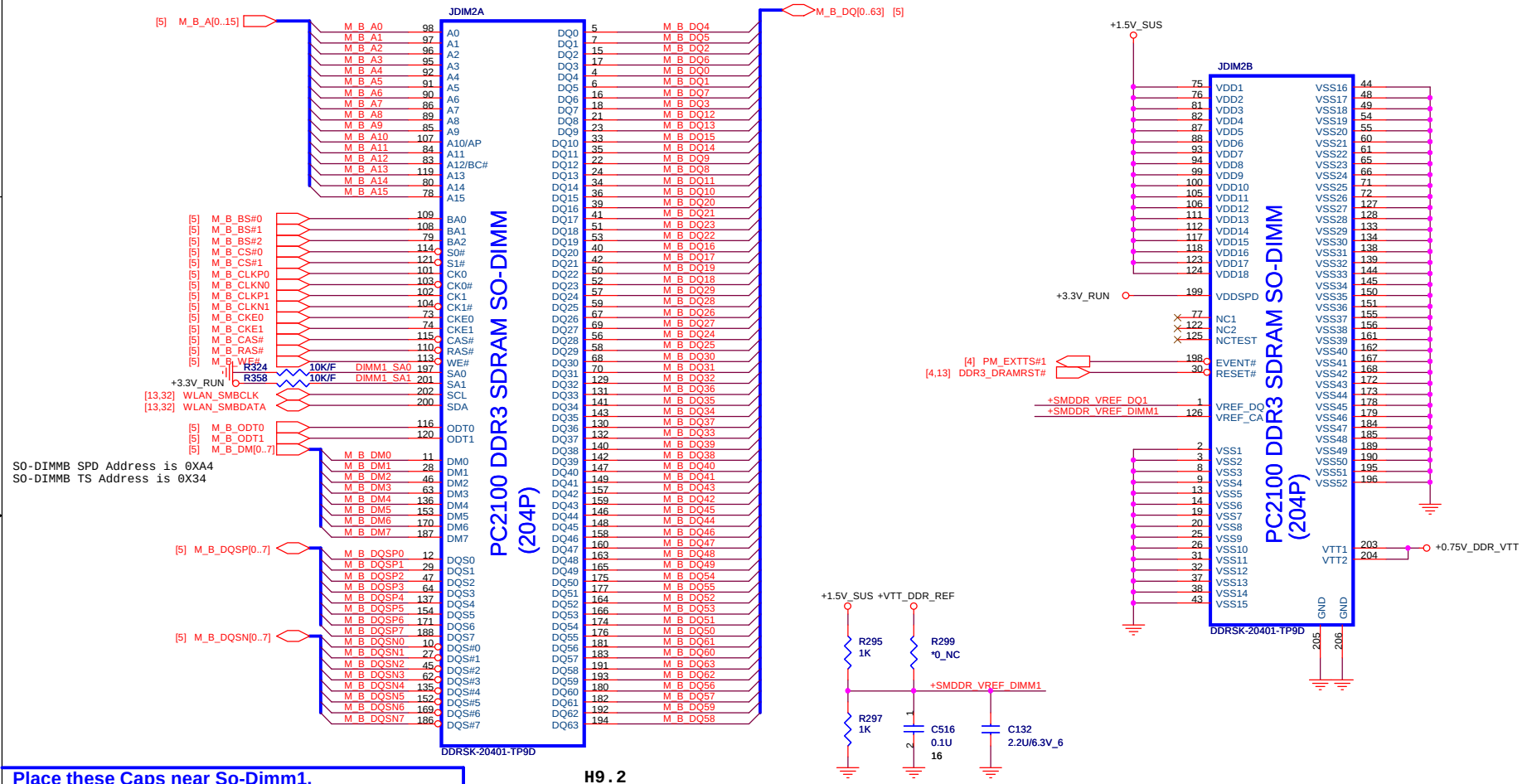
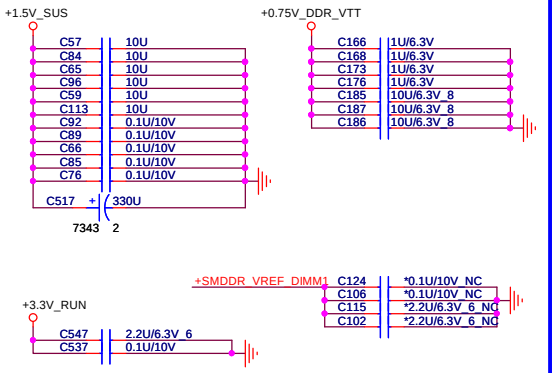


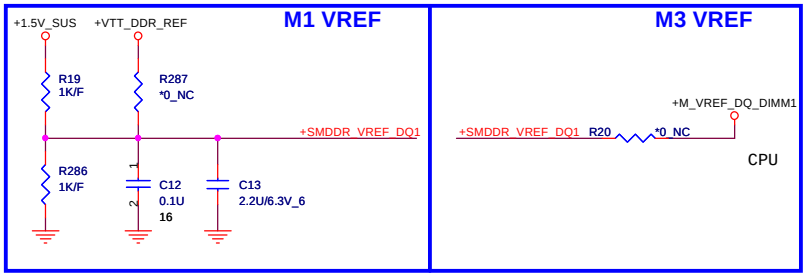
H9.2

Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%





Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number	Rev
	DDR3 DIMM-1	3A
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POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

POWER
for Park-S3
DPx_VDD10=1.0V

U22A

2.5GT/s bit rate

PCI EXPRESS INTERFACE

[4] PEG_TXP15	[4] PEG_TXN15	AF30 AE31	PCIE_RX0P PCIE_RX0N	PCIE_TX0P PCIE_TX0N	AH30 AG31	PEG_RXP15_C PEG_RXN15_C	C240 C241	0.1U/10V 0.1U/10V	PEG_RXP15 [4] PEG_RXN15 [4]
[4] PEG_TXP14	[4] PEG_TXN14	AE29 AD28	PCIE_RX1P PCIE_RX1N	PCIE_TX1P PCIE_TX1N	AG29 AF28	PEG_RXP14_C PEG_RXN14_C	C266 C267	0.1U/10V 0.1U/10V	PEG_RXP14 [4] PEG_RXN14 [4]
[4] PEG_TXP13	[4] PEG_TXN13	AD30 AC31	PCIE_RX2P PCIE_RX2N	PCIE_TX2P PCIE_TX2N	AF27 AF26	PEG_RXP13_C PEG_RXN13_C	C237 C228	0.1U/10V 0.1U/10V	PEG_RXP13 [4] PEG_RXN13 [4]
[4] PEG_TXP12	[4] PEG_TXN12	AC29 AB28	PCIE_RX3P PCIE_RX3N	PCIE_TX3P PCIE_TX3N	AD27 AD26	PEG_RXP12_C PEG_RXN12_C	C318 C312	0.1U/10V 0.1U/10V	PEG_RXP12 [4] PEG_RXN12 [4]
[4] PEG_TXP11	[4] PEG_TXN11	AB30 AA31	PCIE_RX4P PCIE_RX4N	PCIE_TX4P PCIE_TX4N	AC25 AB25	PEG_RXP11_C PEG_RXN11_C	C321 C326	0.1U/10V 0.1U/10V	PEG_RXP11 [4] PEG_RXN11 [4]
[4] PEG_TXP10	[4] PEG_TXN10	AA29 Y28	PCIE_RX5P PCIE_RX5N	PCIE_TX5P PCIE_TX5N	Y23 Y24	PEG_RXP10_C PEG_RXN10_C	C345 C346	0.1U/10V 0.1U/10V	PEG_RXP10 [4] PEG_RXN10 [4]
[4] PEG_TXP9	[4] PEG_TXN9	Y30 W31	PCIE_RX6P PCIE_RX6N	PCIE_TX6P PCIE_TX6N	AB27 AB26	PEG_RXP9_C PEG_RXN9_C	C328 C327	0.1U/10V 0.1U/10V	PEG_RXP9 [4] PEG_RXN9 [4]
[4] PEG_TXP8	[4] PEG_TXN8	W29 V28	PCIE_RX7P PCIE_RX7N	PCIE_TX7P PCIE_TX7N	Y27 Y26	PEG_RXP8_C PEG_RXN8_C	C381 C380	0.1U/10V 0.1U/10V	PEG_RXP8 [4] PEG_RXN8 [4]
[4] PEG_TXP7	[4] PEG_TXN7	V30 U31	PCIE_RX8P PCIE_RX8N	PCIE_TX8P PCIE_TX8N	W24 W23	PEG_RXP7_C PEG_RXN7_C	C360 C359	0.1U/10V 0.1U/10V	PEG_RXP7 [4] PEG_RXN7 [4]
[4] PEG_TXP6	[4] PEG_TXN6	U29 T28	PCIE_RX9P PCIE_RX9N	PCIE_TX9P PCIE_TX9N	V27 U26	PEG_RXP6_C PEG_RXN6_C	C362 C361	0.1U/10V 0.1U/10V	PEG_RXP6 [4] PEG_RXN6 [4]
[4] PEG_TXP5	[4] PEG_TXN5	T30 R31	PCIE_RX10P PCIE_RX10N	PCIE_TX10P PCIE_TX10N	U24 U23	PEG_RXP5_C PEG_RXN5_C	C384 C383	0.1U/10V 0.1U/10V	PEG_RXP5 [4] PEG_RXN5 [4]
[4] PEG_TXP4	[4] PEG_TXN4	R29 P28	PCIE_RX11P PCIE_RX11N	PCIE_TX11P PCIE_TX11N	T26 T27	PEG_RXP4_C PEG_RXN4_C	C371 C370	0.1U/10V 0.1U/10V	PEG_RXP4 [4] PEG_RXN4 [4]
[4] PEG_TXP3	[4] PEG_TXN3	P30 N31	PCIE_RX12P PCIE_RX12N	PCIE_TX12P PCIE_TX12N	T24 T23	PEG_RXP3_C PEG_RXN3_C	C390 C389	0.1U/10V 0.1U/10V	PEG_RXP3 [4] PEG_RXN3 [4]
[4] PEG_TXP2	[4] PEG_TXN2	N29 M28	PCIE_RX13P PCIE_RX13N	PCIE_TX13P PCIE_TX13N	P27 P26	PEG_RXP2_C PEG_RXN2_C	C374 C373	0.1U/10V 0.1U/10V	PEG_RXP2 [4] PEG_RXN2 [4]
[4] PEG_TXP1	[4] PEG_TXN1	M30 L31	PCIE_RX14P PCIE_RX14N	PCIE_TX14P PCIE_TX14N	P24 P23	PEG_RXP1_C PEG_RXN1_C	C368 C367	0.1U/10V 0.1U/10V	PEG_RXP1 [4] PEG_RXN1 [4]
[4] PEG_TXP0	[4] PEG_TXN0	L29 K30	PCIE_RX15P PCIE_RX15N	PCIE_TX15P PCIE_TX15N	M27 N26	PEG_RXP0_C PEG_RXN0_C	C387 C386	0.1U/10V 0.1U/10V	PEG_RXP0 [4] PEG_RXN0 [4]

CLOCK

[9] CLK_PCIE_VGAP — AK30 PCIE_REFCLKP
[9] CLK_PCIE_VGAN — AK32 PCIE_REFCLKN

R316 1 2 10K — N10 PWRGOOD

[4,10,29,32,38] PLTRST# — AL27 PERSTB

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

CALIBRATION

PCIE_CALRP — Y22 — PCIE_CALRP — R188 1.27K/F
PCIE_CALRN — AA22 — PCIE_CALRN — R193 2K/F — +PCIE_VDDC

PARK-XT

U22G

DP E/F POWER

+DPF_VDD18 1.8V(200mA)
AG15 DPE_VDD18#1
AG16 DPE_VDD18#2
Park-S3:TMDS 1.0V@110mA LVDS 1.0V@120mA

+DPF_VDD10
AG20 DPE_VDD10#1
AG21 DPE_VDD10#2

DPE for LVDS

AG14 DPE_VSSR#1
AH14 DPE_VSSR#2
AM14 DPE_VSSR#3
AM16 DPE_VSSR#4
AM18 DPE_VSSR#5

+DPF_VDD18 1.8V(200mA)
AF16 DPF_VDD18#1
AG17 DPF_VDD18#2

+DPF_VDD10
AF22 DPF_VDD10#1
AG22 DPF_VDD10#2
Park-S3:TMDS 1.0V@110mA LVDS 1.0V@120mA

AF23 DPF_VSSR#1
AG23 DPF_VSSR#2
AM20 DPF_VSSR#3
AM22 DPF_VSSR#4
AM24 DPF_VSSR#5

R423 150/F — AF17 DPEF_CALR

+DPF_PVDD 1.8V(20mA)
AG18 DPE_PVDD
AF19 DPE_PVSS

+DPF_PVDD 1.8V(20mA)
AG19 DPF_PVDD
AF20 DPF_PVSS

DP A/B POWER

+DPA_VDD18 1.8V(130mA)
AE11 DPA_VDD18#1
AE11 DPA_VDD18#2
M9x-S3:1.1V@200mA Park-S3:1.0V@110mA

+DPA_VDD10
AF6 DPA_VDD10#1
AF7 DPA_VDD10#2

AE1 DPA_VSSR#1
AE3 DPA_VSSR#2
AG1 DPA_VSSR#3
AG6 DPA_VSSR#4
AH5 DPA_VSSR#5

+DPA_VDD18 1.8V(130mA)
AE13 DPB_VDD18#1
AE13 DPB_VDD18#2
M9x-S3:1.1V@200mA Park-S3:1.0V@110mA

+DPA_VDD10
AF8 DPB_VDD10#1
AF9 DPB_VDD10#2
DPB for HDMI

AE10 DPB_VSSR#1
AG9 DPB_VSSR#2
AH8 DPB_VSSR#3
AM6 DPB_VSSR#4
AM8 DPB_VSSR#5

AE10 R151 150/F — DPAB_CALR

DP PLL POWER

+DPA_PVDD 1.8V(20mA)
AG8 DPA_PVDD
AG7 DPA_PVSS

+DPA_PVDD 1.8V(20mA)
AG10 DPB_PVDD
AG11 DPB_PVSS

PARK-XT

+DPF_VDD18 — C249 0.1U/10V — C560 1U/10V — C561 10U/6.3V_8 — L43 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_RUN_GFX

+DPA_VDD18 — C211 0.1U/10V — C542 1000P/50V — L40 BLM18PG181SN1D(180,1.5A)_6 — C540 10U/6.3V_8 — +1.8V_RUN_GFX

+DPF_VDD10 — C277 0.1U/10V — C583 1000P/50V — L46 BLM18PG181SN1D(180,1.5A)_6 — C586 10U/6.3V_8 — +PCIE_VDDC

+DPA_VDD10 — C178 0.1U/10V — C181 10U/6.3V_8 — C197 1000P/50V — L22 BLM18PG181SN1D(180,1.5A)_6 — +PCIE_VDDC

+DPF_PVDD — C258 0.1U/10V — C573 1000P/50V — L44 BLM18PG181SN1D(180,1.5A)_6 — C574 10U/6.3V_8 — +1.8V_RUN_GFX

+DPA_PVDD — C554 0.1U/10V — C555 1000P/50V — L42 BLM18PG181SN1D(180,1.5A)_6 — C558 10U/6.3V_8 — +1.8V_RUN_GFX

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Park_PCIE_Interface	3A

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MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C	AKD5LZGTW00
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12	AKD5LGGT502
0010	Samsung B-die	128*16-800MHZ	K4W2G1646B-HC12	AKD5N00T501
0011	Reserved			
0100	Reserved			
0101	Reserved			
0110	Reserved			
0111	Reserved			
1000	Reserved			
1001	Reserved			
1010	Reserved			
1011	Reserved			
1100	Reserved			
1101	Reserved			
1110	Reserved			
1111	Reserved			

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

GPU Power-on sequence

Power-Up

- +3.3V_RUN → +VCC_GFX_CORE
- +PCIE_VDDC → +1.8V_RUN_GFX
- CLK_PCIE_VGAP/N → +1.8V_RUN_GFX
- +3.3V_RUN early +VCC_GFX_CORE /+1.8V_RUN_GFX or when +VCC_GFX_CORE /+1.8V_RUN_GFX up then +3.3V_RUN
- +VCC_GFX_CORE reach 90% and +1.8V_RUN_GFX

power-down

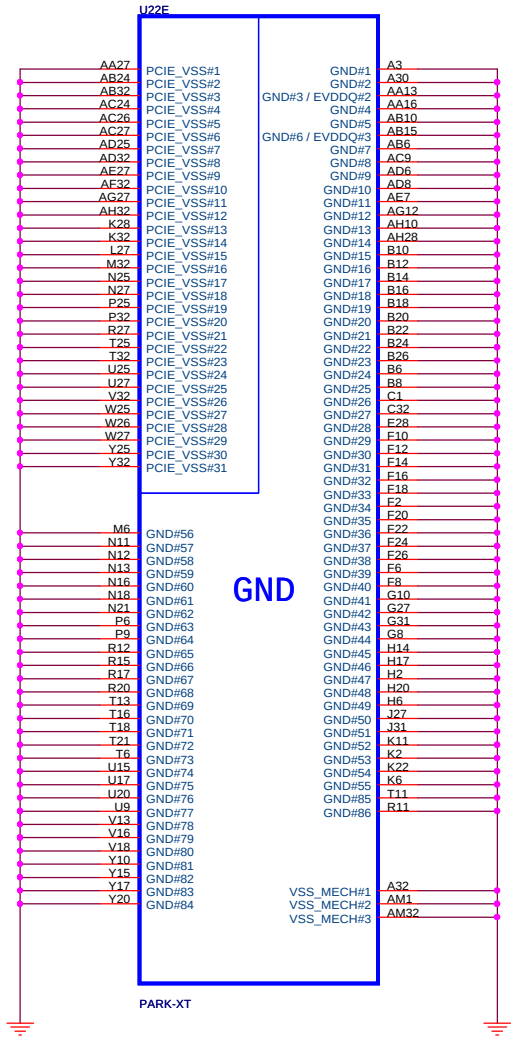
- +1.8V_RUN_GFX → +PCIE_VDDC

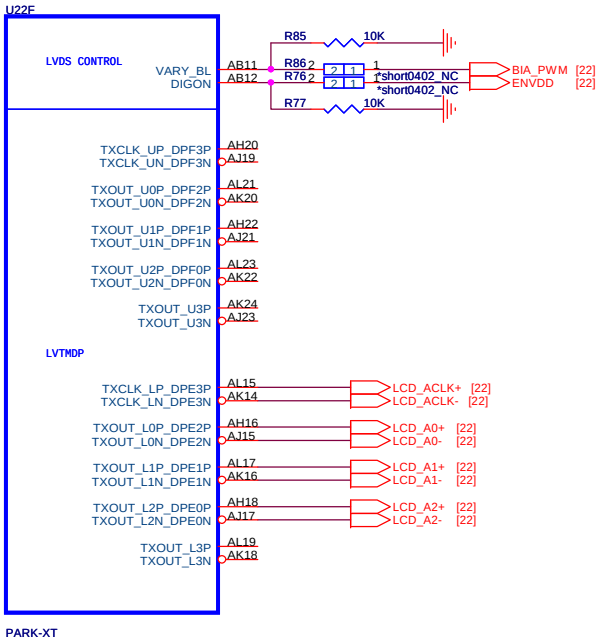
PCIe ref clock(CLK_PCIE_VGAA/B) early +1.8V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

R475 =>
100/F for CLK_VGA_27M CLK Gen
0ohm for Crystal
CS11002FB22
RES CHIP 100 1/16W +-1%(0402)

Quanta Computer Inc.
PROJECT : UM7 DIS
Park_Main
Wednesday, February 03, 2010



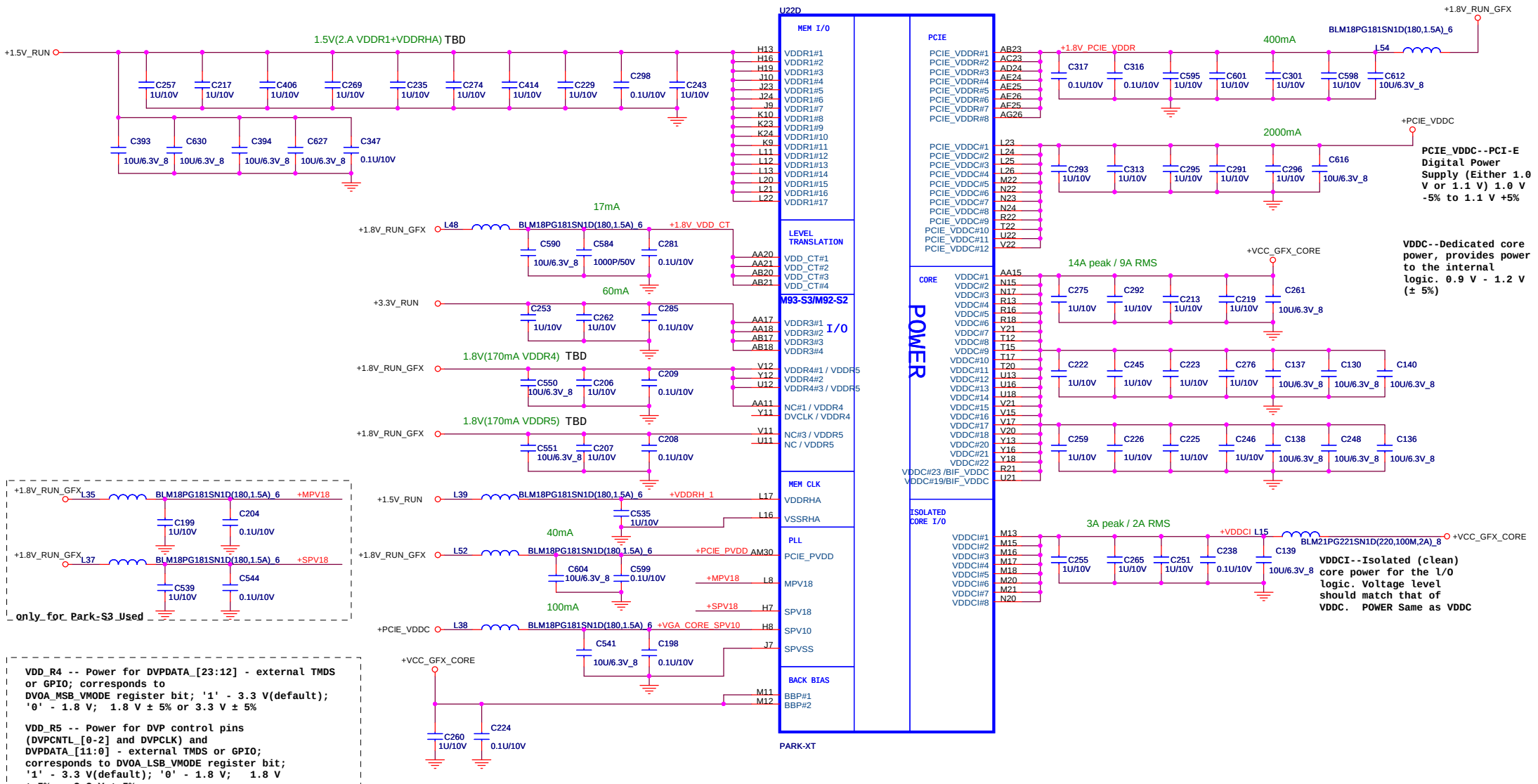


Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**PCI Express Full TX Output Swing** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	**Enable CLKREQ# Power Management** 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYNC HSYNC	**AUD[1] AUD[0]** 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Park_GND / LVDS/ Straps	3A
Date: Wednesday, February 03, 2010	Sheet 17 of 52	

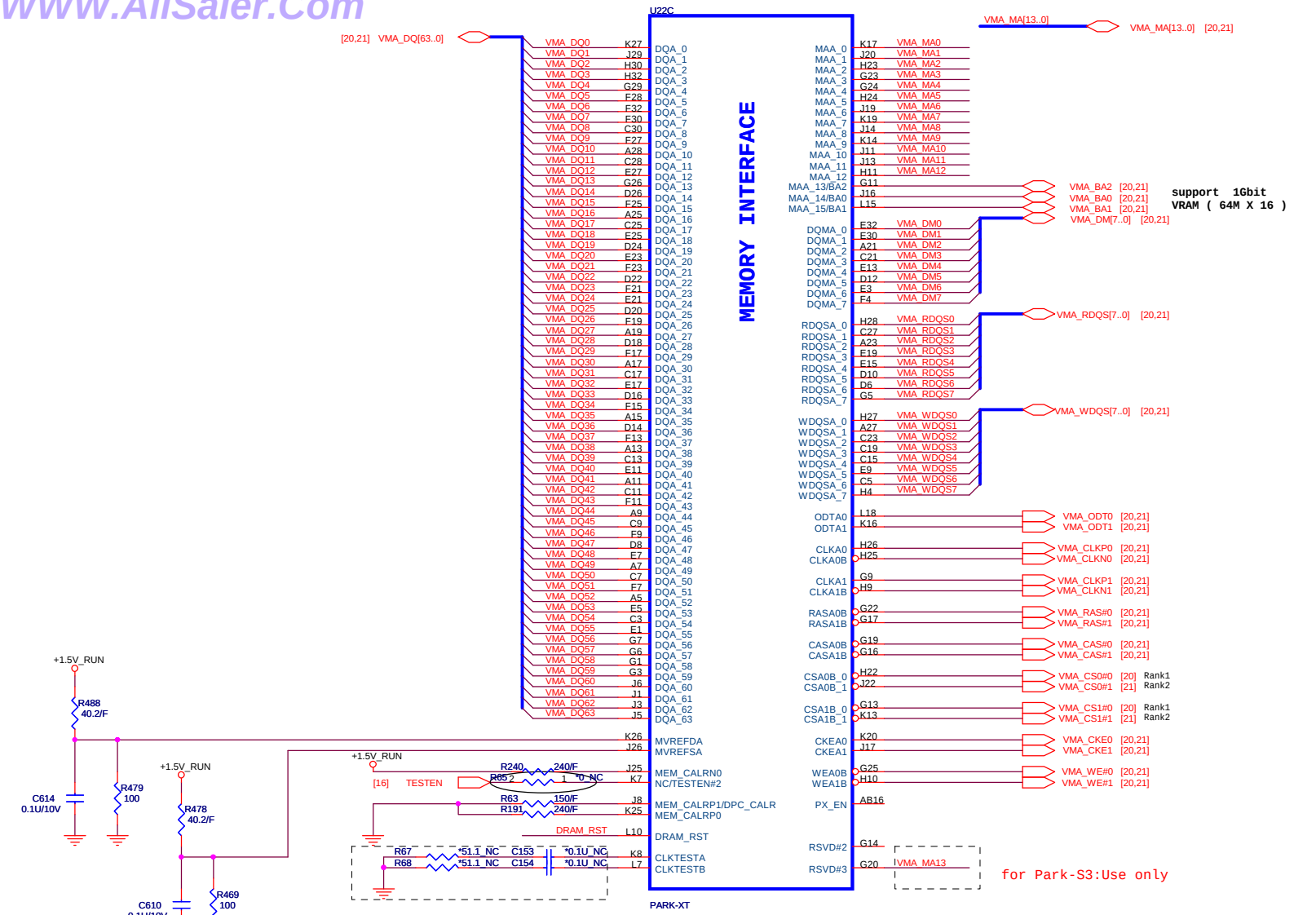
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDD_R4 -- Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDD_R5 -- Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: Park_Power_and_NC	Rev: 3A
Date: Wednesday, February 03, 2010	Sheet 18 of 52	

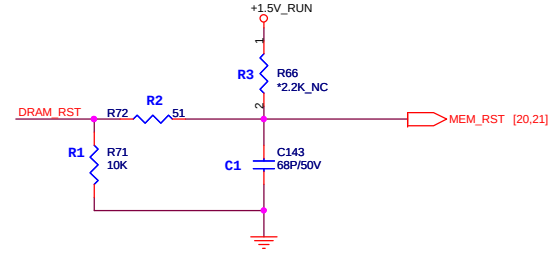


	M9x-S2/S3	Park-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R
MEM_CALRP1(J8)	240R	150R
TESTEN2#2(K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
51R:CS05102JB35

2.2nF:CH22206KB16
68pF:CH06806JB01



Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	Park_MEM_Interface	3A

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DDR3 BGA MEMORY

Hynix
AKD5LZGTW00
IC DDR3(96P) H5TQ1G63BFR-12C (FBGA)

AKD5LZGTW03
IC SDRAM(96P)H5TQ1G63BFR-12C(FBGA)WINBSQ

Samsung
AKD5LGGT502
IC SDRAM(96P) K4W1G1646E-HC12(FBGA)

AKD5LGGT505
IC SDRAM(96P)K4W1G1646E-HC12(FBGA)WINBSQ

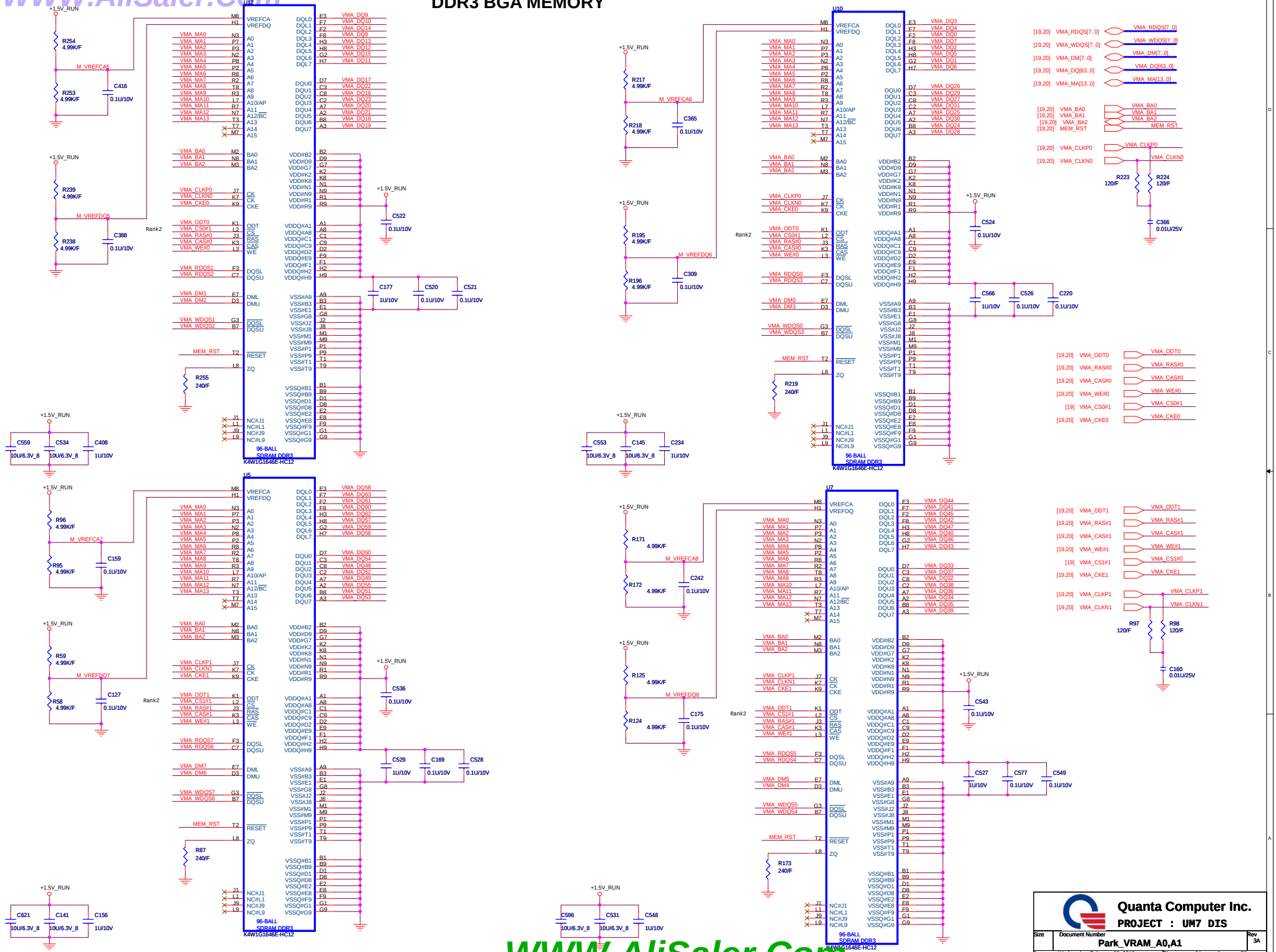
+1.5V_RUN Terminations are required for DUAL RANK Configuration ONLY for better performance (Higher then 700MHz)

U27 U18 U24 U20 — 96-BALL SDRAM DDR3 K4W1G1646E-HC12

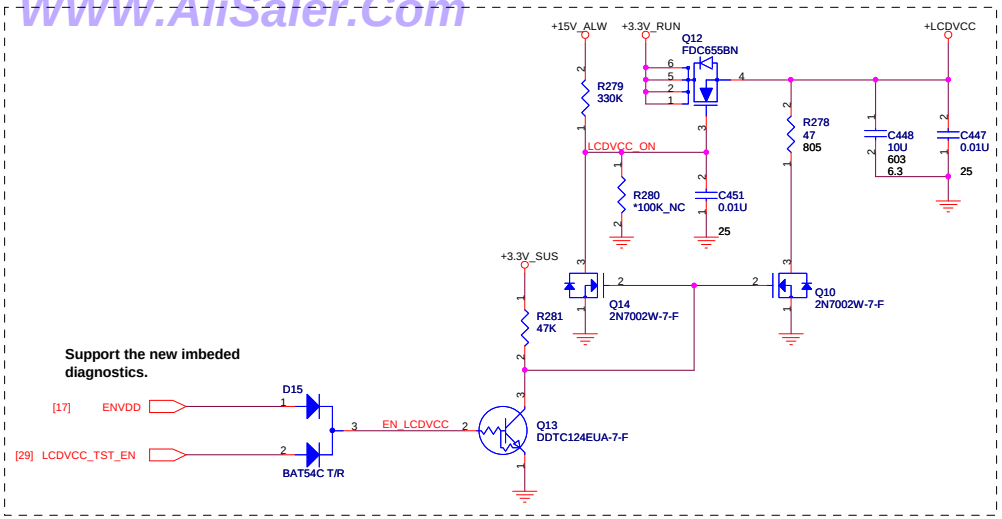
Rank1

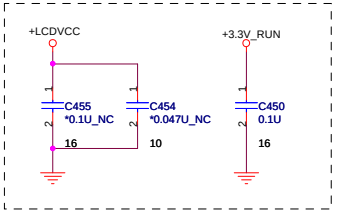
Quanta Computer Inc.
PROJECT : UM7 DIS
Size | Document Number: Park_VRAM_A0,A1 | Rev: 3A
Date: Wednesday, February 03, 2010 | Sheet 20 of 52

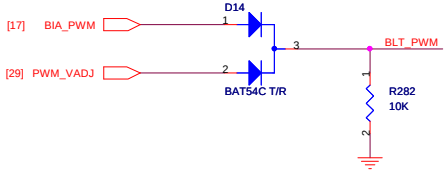
DDR3 BGA MEMORY

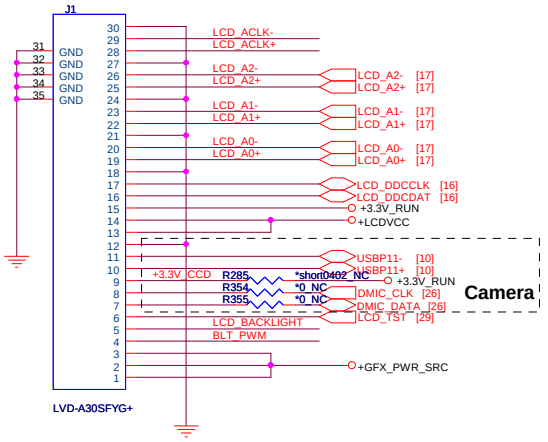


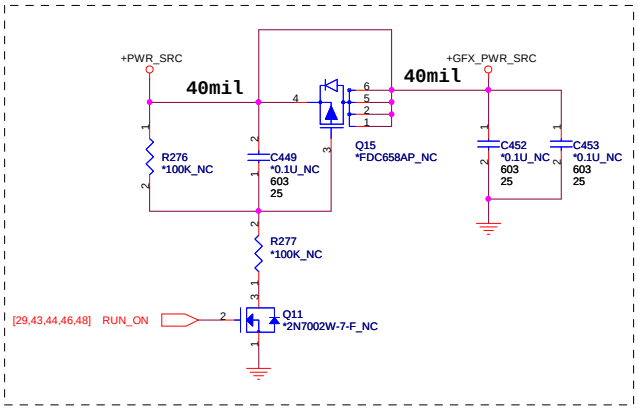
Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: Park_VRAM_A0,A1	Rev: 3A
Date: Wednesday, February 03, 2010	Sheet 21 of 52	

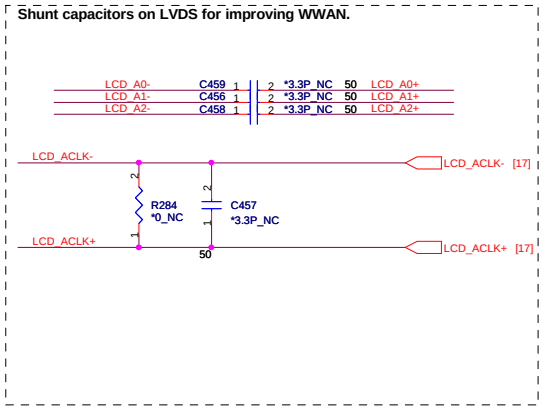


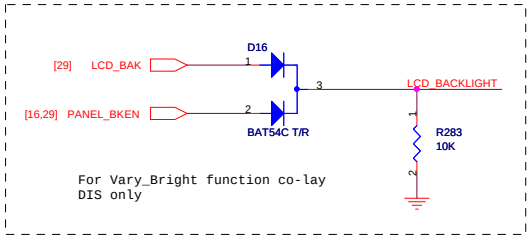












Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	LCD CONN / HDMI CONN	3A
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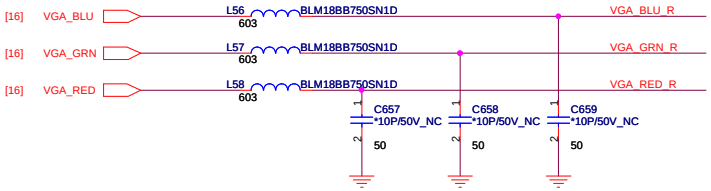

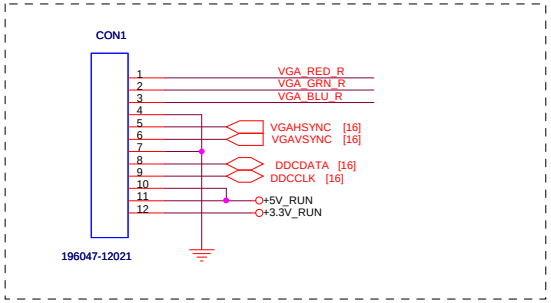

Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	CRT CONN	3A
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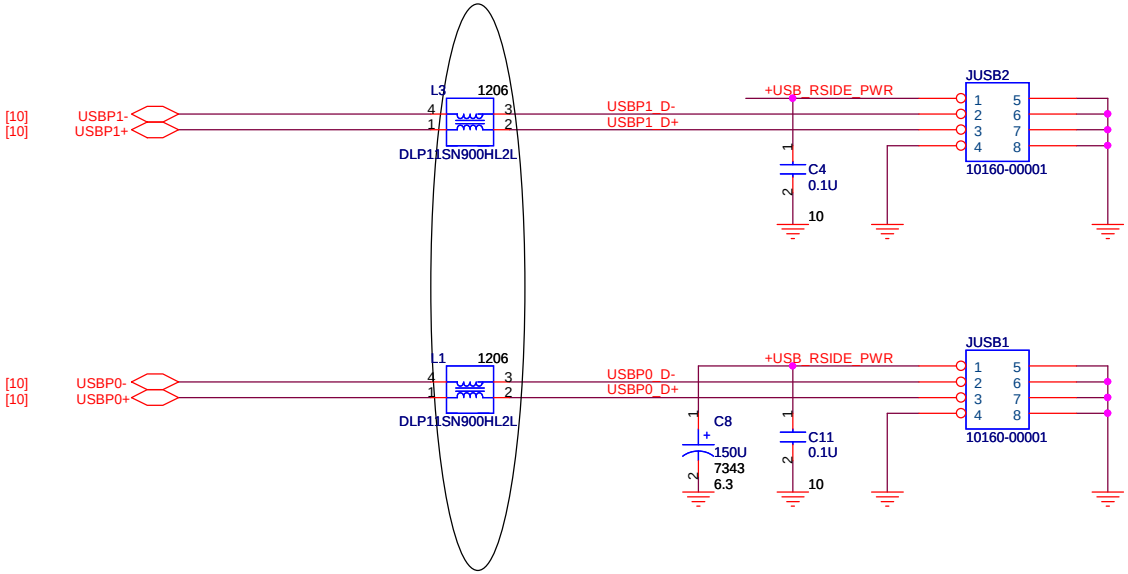
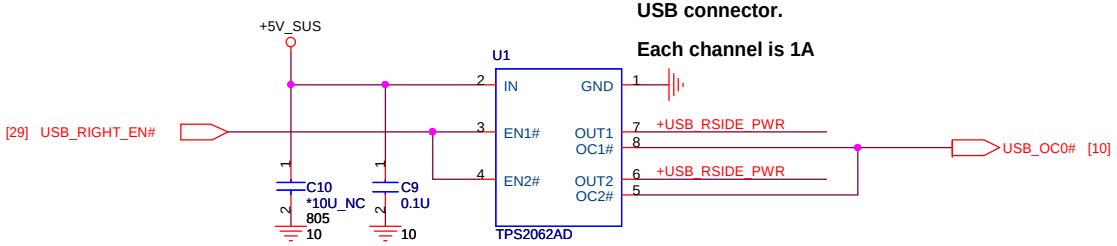
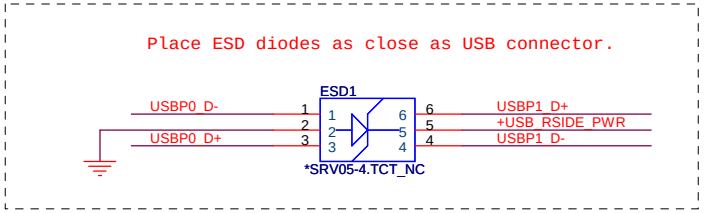


Place one 150uF cap by each USB connector.

Each channel is 1A



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: Right USB	Rev: 3A
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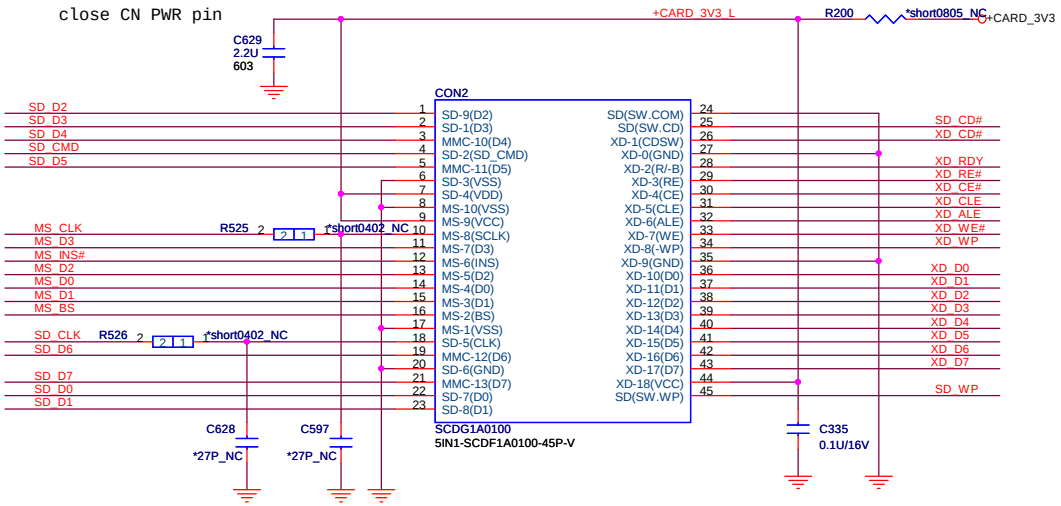
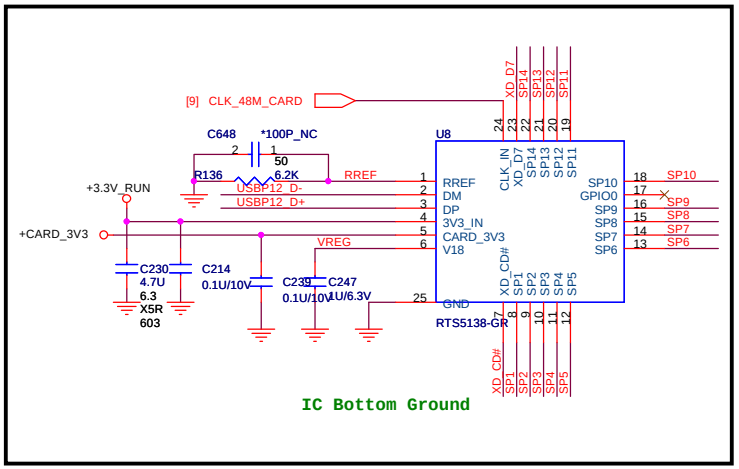
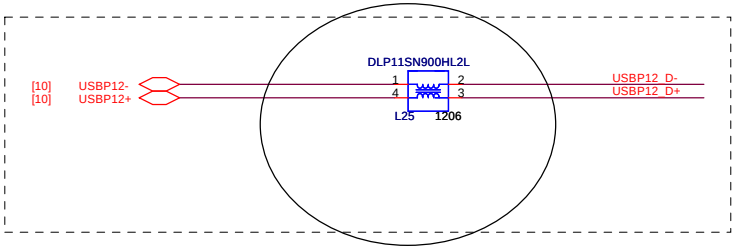


SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

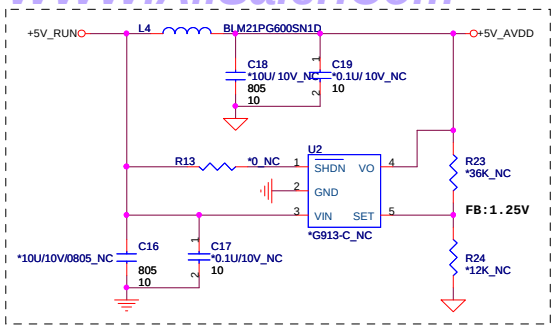
Share Pin



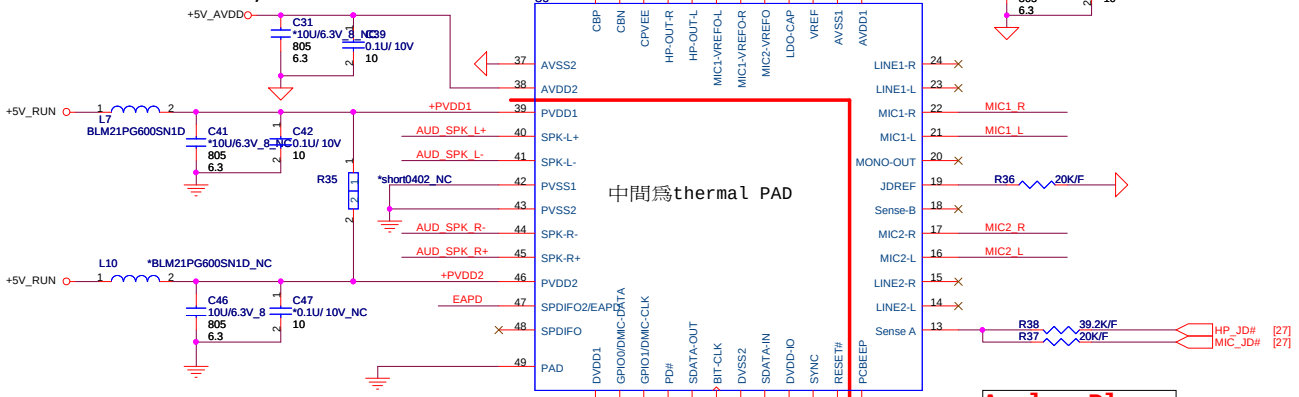
RTS5138-QFN24

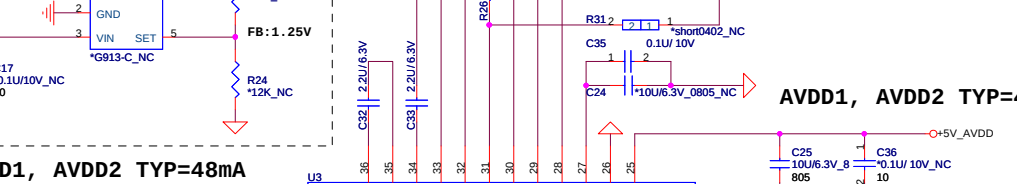


Quanta Computer Inc.			
PROJECT : UM7 DIS			
Size	Document Number		Rev
	Card Reader(RST5138)		3A
Date: Wednesday, February 03, 2010	Sheet 25 of 52		

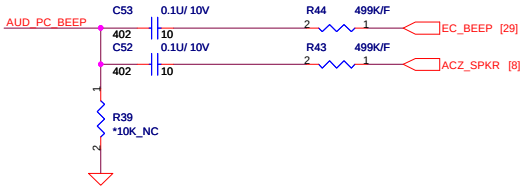


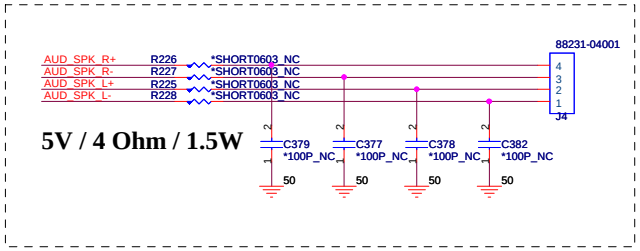
AVDD1, AVDD2 TYP=48mA





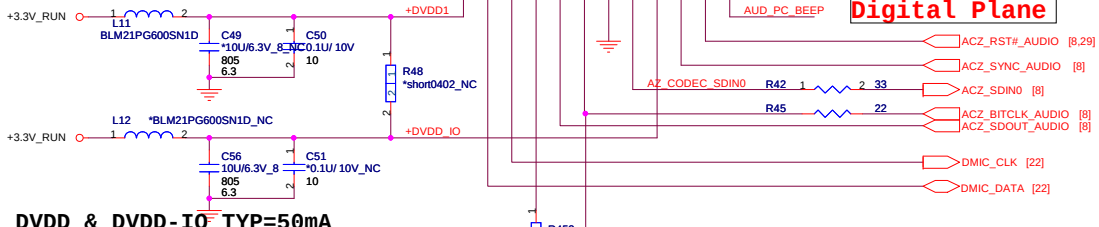
AVDD1, AVDD2 TYP=48mA



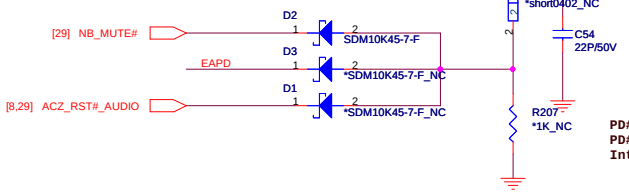


Analog Plane

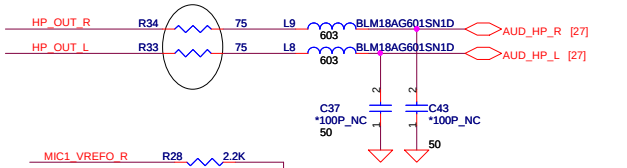
Digital Plane

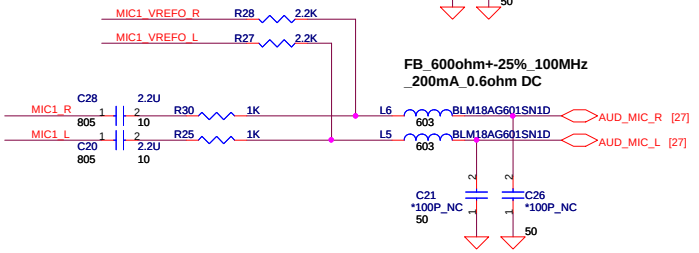


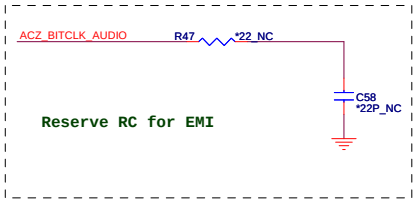
DVDD & DVDD-IO TYP=50mA

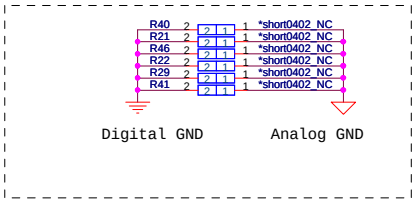


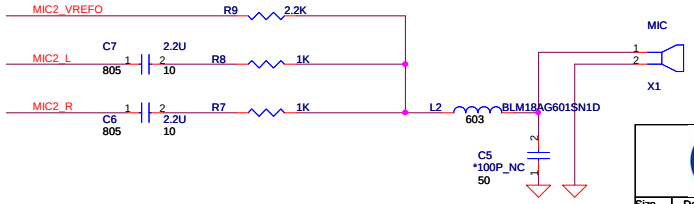
PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.











Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: Azelia CODEC(ALC269)	Rev 3A
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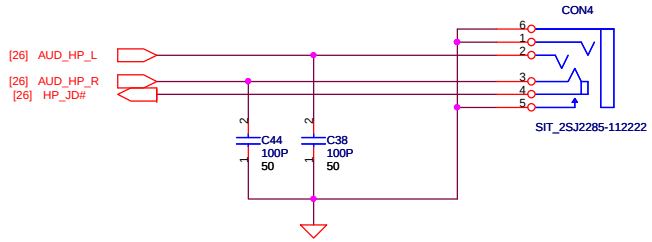
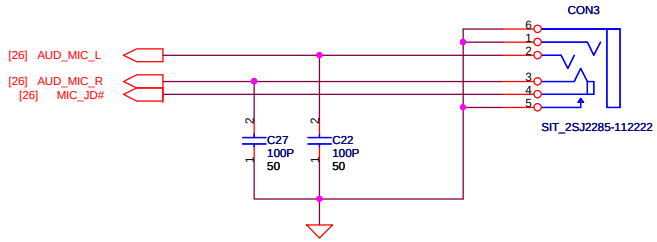
HP JACKN

SUYIN NORMAL OPEN



MIC JACK

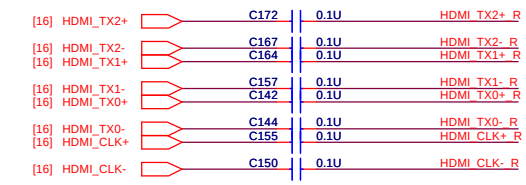
SUYIN NORMAL OPEN

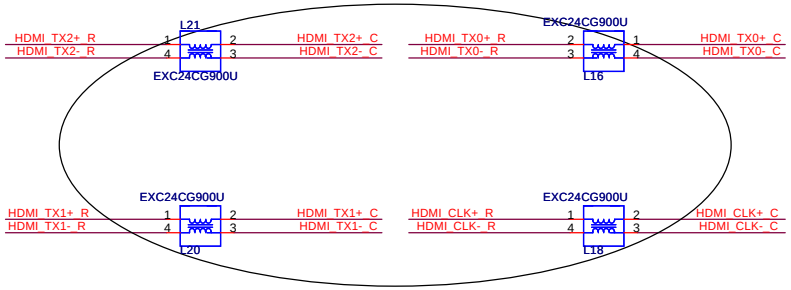


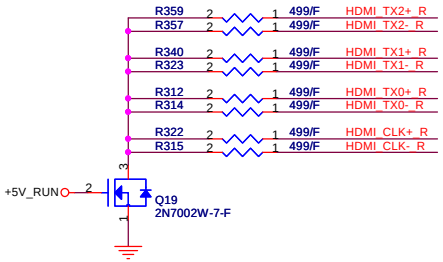
Quanta Computer Inc.

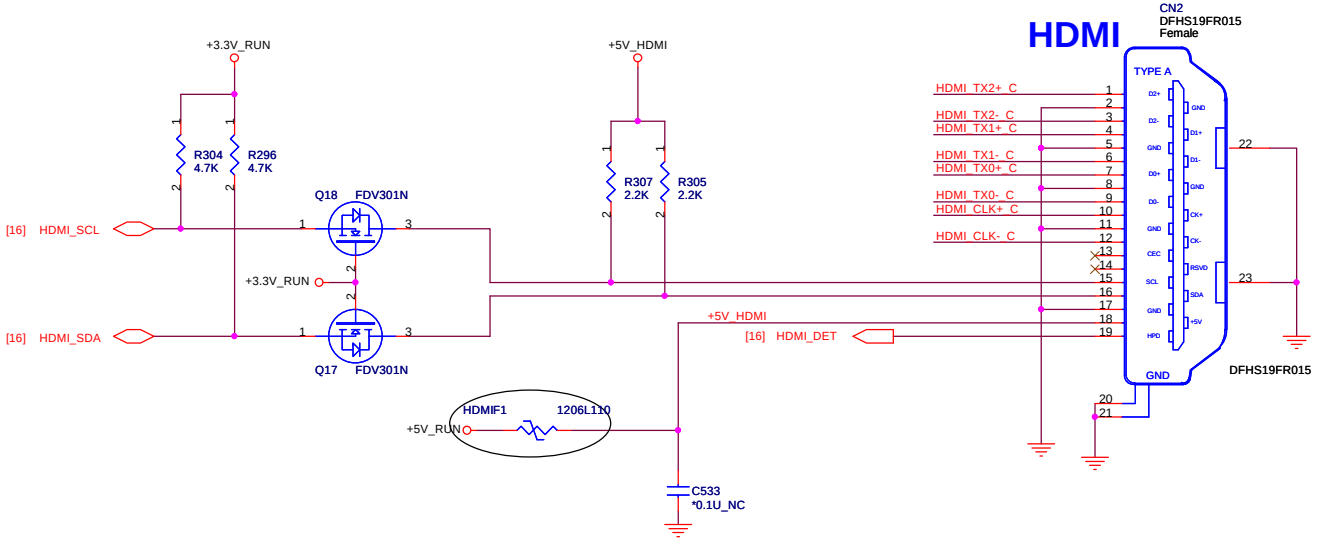
PROJECT : UM7 DIS

Size	Document Number	Rev
	AUDIO CONN	3A
Date: Wednesday, February 03, 2010	Sheet 27 of 52	









Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	Blank	3A

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ITE8502E LQFP-128L

U25

[34] KSO[0..16]
[34] KSI[0..7]

KEYBOARD: KSO17/GPC5, KSO16/GPC3, KSO15, KSO14, KSO13, KSO12/SLCT, KSO11/ERR, KSO10/PE, KSO9/BUSY, KSO8/ACK, KSO7/PD7, KSO6/PD6, KSO5/PD5, KSO4/PD4, KSO3/PD3, KSO2/PD2, KSO1/PD1, KSO0/PD0; KSI7, KSI6, KSI5, KSI4, KSI3/SLIN, KSI2/INT, KSI1/AFD, KSI0/STB

LPC: LPCRST/WUI4/GPD2, LPCCLK, LFRAME, LAD0, LAD1, LAD2, LAD3, CLKRUN/GPH0/ID0, SERIRQ, ECSMI/GPD4, ECSCI/GPD3, GA20/GPB5, LPCPD/WUI6/GPE6

SMBUS: KBRST/GPB6, WRST, PWUREQ/GPC7, L80HLAT/GPE0, L80LLAT/WUI7/GPE7, SMCLK0/GPB3, SMDAT0/GPB4, SMCLK1/GPC1, SMDAT1/GPC2, SMCLK2/GPF6, SMDAT2/GPF7

PS/2: PS2CLK0/GPF0, PS2DAT0/GPF1, PS2CLK1/GPF2, PS2DAT1/GPF3, PS2CLK2/GPF4, PS2DAT2/GPF5

CK32K, CK32KE, VCORE, VSS1, VSS3, VSS4, VSS5, VSS6, VSS7, AVCC, AVSS

VBAT1, VCC, VSTBY1, VSTBY2, VSTBY3, VSTBY4, VSTBY5, VSTBY6

ADC/DAC: ADC0/GPI0, ADC1/GPI1, ADC2/GPI2, ADC3/GPI3, ADC4/GPI4, ADC5/GPI5, ADC6/GPI6, ADC7/GPI7; DAC0/GPJ0, DAC1/GPJ1, DAC2/GPJ2, DAC3/GPJ3, DAC4/GPJ4, DAC5/GPJ5

PWM: PWM0/GPA0, PWM1/GPA1, PWM2/GPA2, PWM3/GPA3, PWM4/GPA4, PWM5/GPA5, PWM6/GPA6, PWM7/GPA7; TACH0/GPD6, TACH1/GPD7; TMRI0/WUI2/GPC4, TMRI1/WUI3/GPC6

IR/UART: RXD/GPB0, TXD/GPB1, GPC0, CTX0/GPB2, CRX1/GPH1/ID1, CTX1/GPH2/ID2

LPC/FWH FLASH: FLFRAME/GPG2/LF, FLRST/GPG0/TM, FLAD3/GPG6, FLAD2/SO, FLAD1/SI, FLAD0/SCE, FLCLK

EGPC: EGAD/GPE1, EGCS/GPE2, EGCLK/GPE3

GPIO: GPH3/ID3, GPH4/ID4, GPH5/ID5, GPH6/ID6, GPG1/ID7; RI1/WUI0/GPD0, RI2/WUI1/GPD1, WUI5/GPE5; RING/PWRFAIL/LPCRST/GPB7; PWRSW/GPE4; GINT/GPD5

IT8502E/KXS-L
lqfp128-16x16-4

+RTC_CELL
+3.3V_RUN
+3.3V_ALW
C631 0.1U/16V

SSI DELETE CAP TO VERIFY
C585 10U/ 6.3V_6 603 6.3
C636 0.1U/16V
C622 0.1U/16V
C593 0.1U/16V
C637 0.1U/16V
Place these caps close to ITE8502.

SMBDAT0 SMBCLK0 RP8 2.2KX2
SMBDAT1 SMBCLK1 RP7 2.2KX2
USB_LEFT_EN# R462 *10K_NC

KB_DET# R511 10K
SERIRQ R495 10K
SMBDAT2 SMBCLK2 RP6 10KX2
ICH_AZ_CODEC_RST0# R524 *10K_NC
LCD_CBL_DET# R520 *10K_NC
PCH_MELOCK R527 *10K_NC
SUS_ON R506 100K
IMVP_VR_ON R493 *100K_NC
V_ID1 R451 10K
V_ID1 for Park

HWPG [37,40,45]
SUS_PWR_ACK [10]
LCD_CBL_DET#
V_ID1
PBAT_PRES# [47]
IINP [41]
SIO_SLP_S5# [10]
CRIT_TEMP_REP# [11]
SIO_EXT_WAKE# [11]
USB_LEFT_EN# [33]
FAN1_DA [37]
RSMRST# [10]
PM_PWRBTN#_R [10]
D23 SDM10K45-7-F

BREATH_LED [36]
FAN1_PWM [37]
PWM_VADJ [22]
EC_BEEP [26]
FAN1_TACH [37]
PANEL_BKEN [16,22]
LID_SW# [34]
SIO_SLP_S3# [10]
[8,26] ACZ_RST#_AUDIO

H_CPUDET# [4]
IMVP_PWRGD [4,45]
RUN_ON [22,43,44,46,48]
BAT1_LED [36]
IMVP_VR_ON [45]
IMVP_VR_ON

SUS_ON [42,43,46]
KB_DET# [34]
SUS_ON
EC_FLASH_SPI_DO [30]
EC_FLASH_SPI_DIN [30]
EC_FLASH_SPI_CS# [30]
EC_FLASH_SPI_CLK [30]

ECPWROK [10]
ALW_ON [36]
GFX_ON [49]

BID2
USB_RIGHT_EN#
BID1
LCD_SIZE_ID0
LCD_SIZE_ID1
USB_RIGHT_EN# [24]

R460 *100K_NC +3.3V_ALW
ACAV_IN [36,41]
BAT2_LED [36]
D21 SDM10K45-7-F
AC_PRESENT [10,16]
SYS_PWR_SW# [36]
LCDVCC_TST_EN [22]

R458 *short0402_NC
[4,10,15,32,38] PLTRST#
[10] CLK_33M_KBC
[8,32] LFRAME#
[8,32] LAD0
[8,32] LAD1
[8,32] LAD2
[8,32] LAD3

[10] CLKRUN#
[8] SERIRQ
[11] SIO_EXT_SMI#
[11] SIO_EXT_SCI#
[11] GATEA20
[22] LCD_TST
SERIRQ
D22 D20 D26 SDM10K45-7-F
SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

[11] RCIN#
D25 SDM10K45-7-F
WRST#
[22] LCD_BAK
[26] NB_MUTE#
ICH_AZ_CODEC_RST0#

R468 *short0402_NC
+3.3V_RUN
R461 *100K_NC
ICH_AZ_CODEC_RST0#
Q29 *2N7002W-7-F_NC
R459 *390K_NC
Q28 *MMST3904-7-F_NC
C615 *0.1U/10V_NC 10

Charge and BAT
PCH
VGA, LAN, Clock Thermal IC

[41,47] SMBCLK0
[41,47] SMBDAT0
[9] SMBCLK1
[9] SMBDAT1
[3,16,37] SMBCLK2
[3,16,37] SMBDAT2

[8] PCH_MELOCK
PCH_MELOCK R521 *short0402_NC
[47] PS_ID
[34] CLK_TP_SIO
[34] DAT_TP_SIO

Discrete
Board ID Straps
R497 10K
R510 10K
R512 *10K_NC
R513 10K
R514 10K
R496 *10K_NC
R505 *10K_NC
R507 10K
R508 *10K_NC
R509 10K_NC
UMA

+3.3V_ALW
R480 100K WRST#
C618 1U/ 10V 603 10
ITE8502_XTAL1
ITE8502_XTAL2
ITE8502IX_JX
+3.3V_ALW
L51 BLM11A05S 603
C606 0.1U/16V

32KHz Clock.
W1
32.768KHZ
C634 18P/50V 50
C635 18P/50V 50

CLK_33M_KBC
R490 *10_NC
C620 *2.2P_NC 50

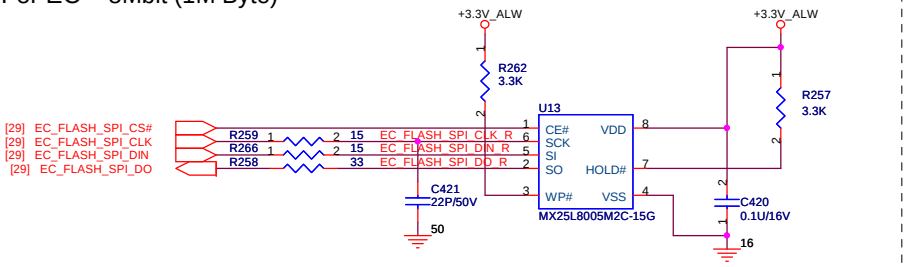
ITE8502IX_JX
C624 0.1U/16V

LCD_SIZE_ID0	LCD_SIZE_ID0	LCD_SIZE	BID1	USB_RIGHT_EN#	Build
0	0	13.3"	0	0	SSI (X00)
0	1	14"	0	1	PT (X01)
1	0	17"	1	0	ST (X02)
			1	1	OT (A00)
			0	0	RAMP(A00)

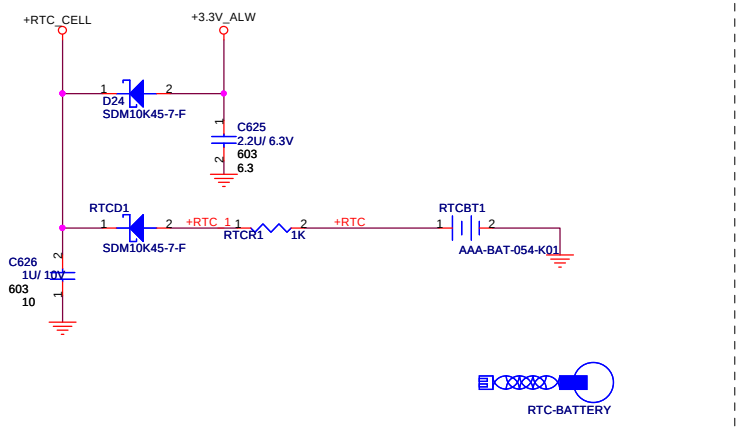
Quanta Computer Inc.
PROJECT : UM7 DIS

Size	Document Number	Rev
	SIO ITE8502	3A
Date: Wednesday, February 03, 2010	Sheet 29 of 52	

For EC 8Mbit (1M Byte)



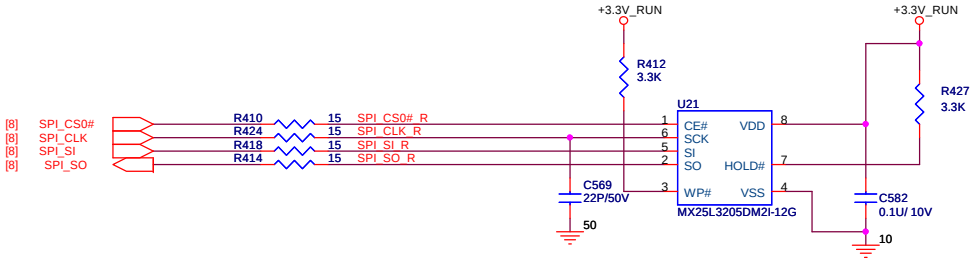
RTC BATTERY



For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	FLASH/RTC	3A

Date: Wednesday, February 03, 2010 Sheet 30 of 52

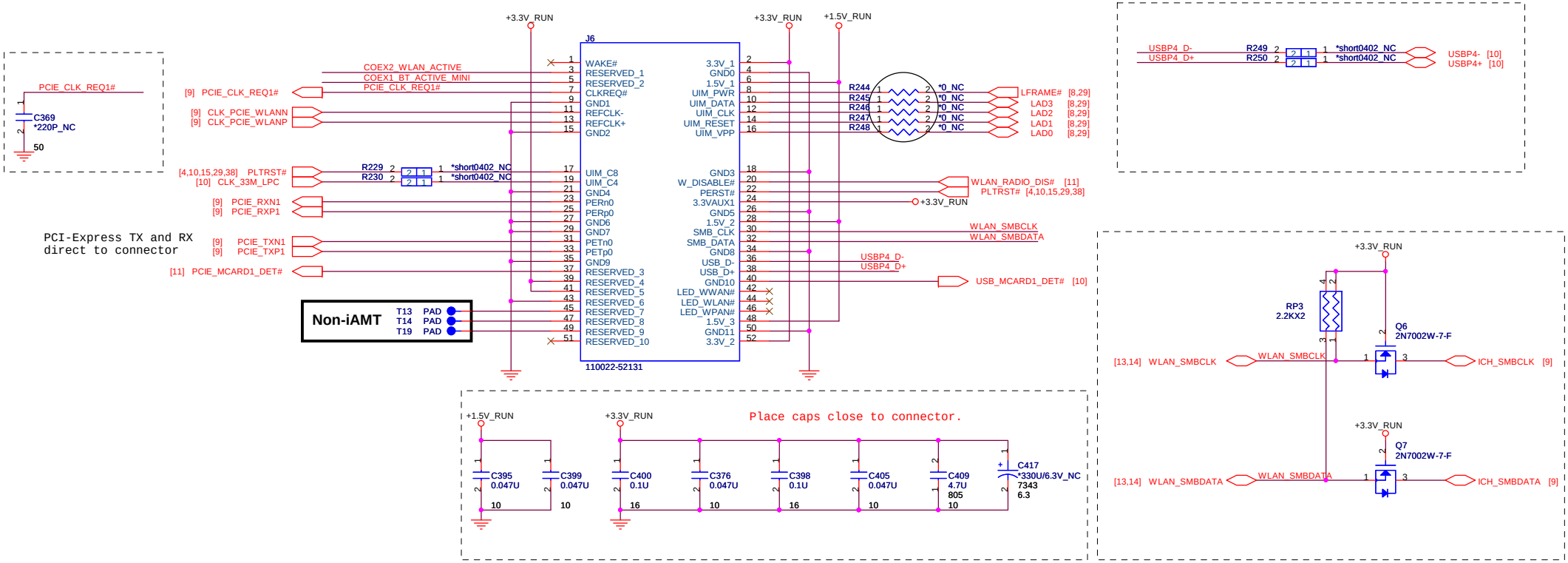
Quanta Computer Inc.

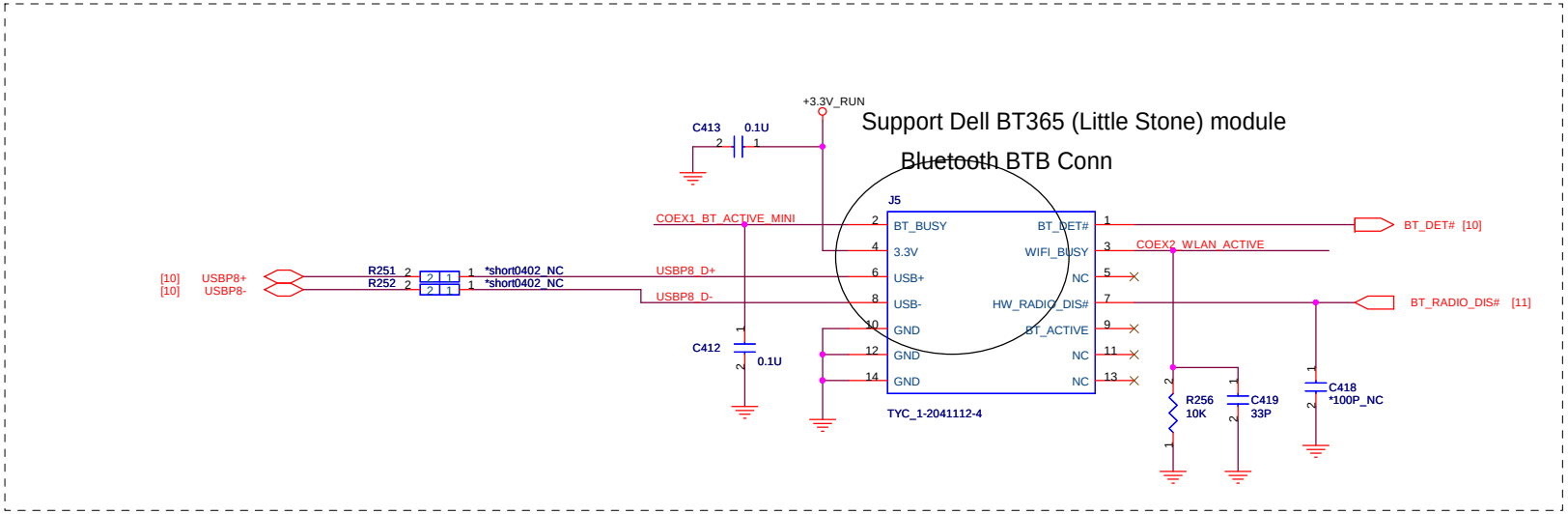
PROJECT : UM7 DIS

Size	Document Number	Rev
	MINI-Card WWAN	3A

Date: Wednesday, February 03, 2010 Sheet 31 of 52

MiniCard WLAN connector



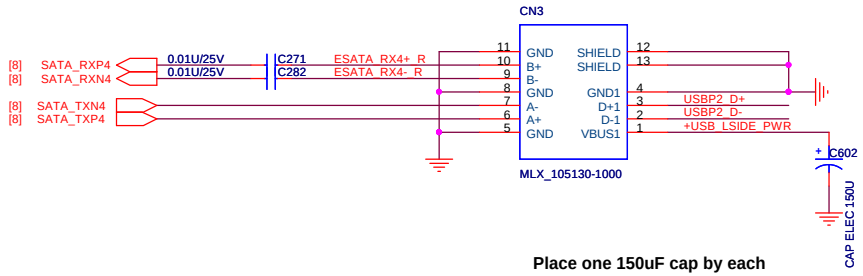


Quanta Computer Inc.

PROJECT : UM7 DIS

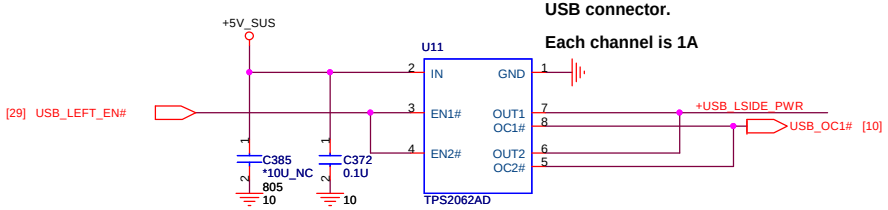
Size	Document Number	Rev
	MINI-Card WLAN / BT	3A
Date: Wednesday, February 03, 2010	Sheet 32 of 52	

USB and eSATA Conn.

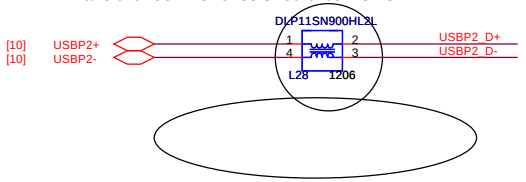


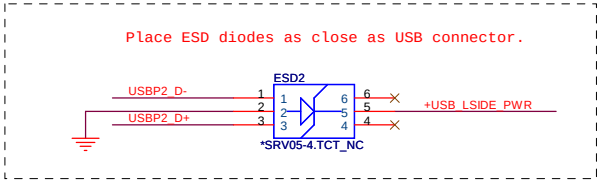
Place one 150uF cap by each USB connector.

Each channel is 1A

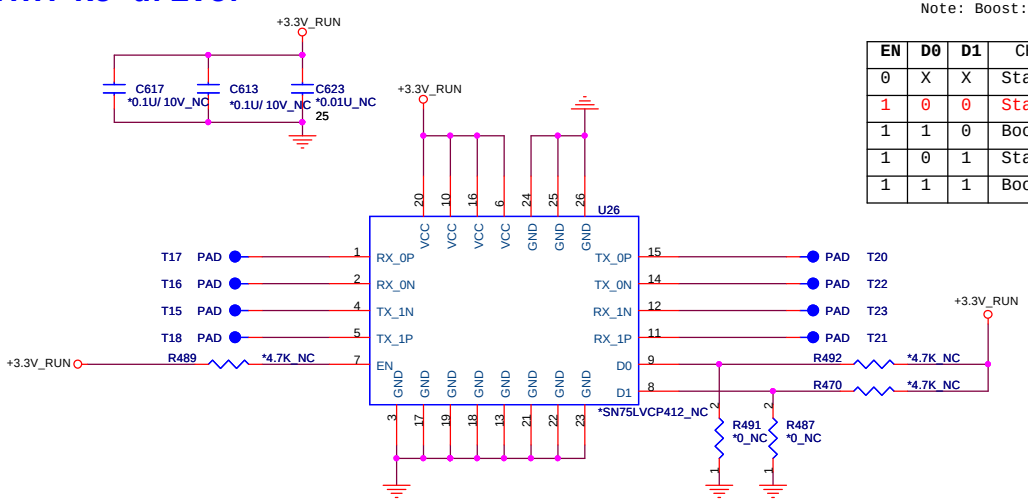


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.





E-SATA Re-driver



Note: Boost:5dB, Standard SATA:0dB

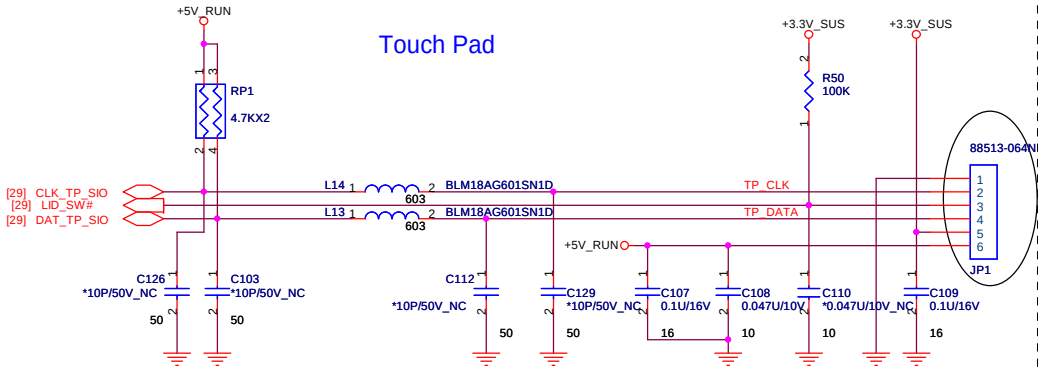
EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Quanta Computer Inc.

PROJECT : UM7 DIS

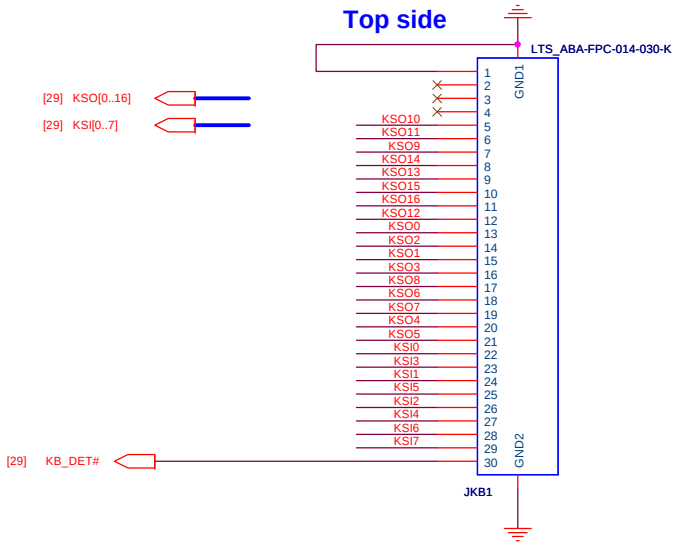
Size	Document Number	Rev
	eSATA & Right USB	3A
Date: Wednesday, February 03, 2010	Sheet 33 of 52	

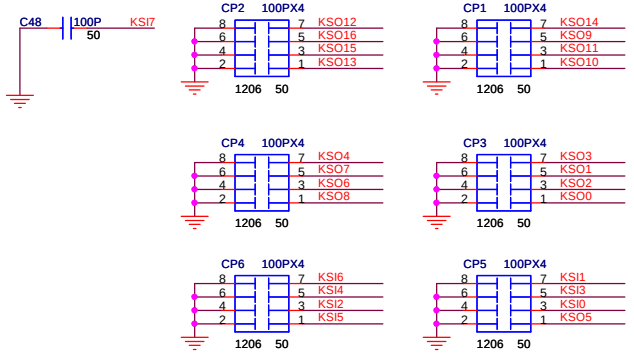
Touch Pad



KEYBOARD CONNECTOR

Top side





100P CAPS CLOSE TO JKB1

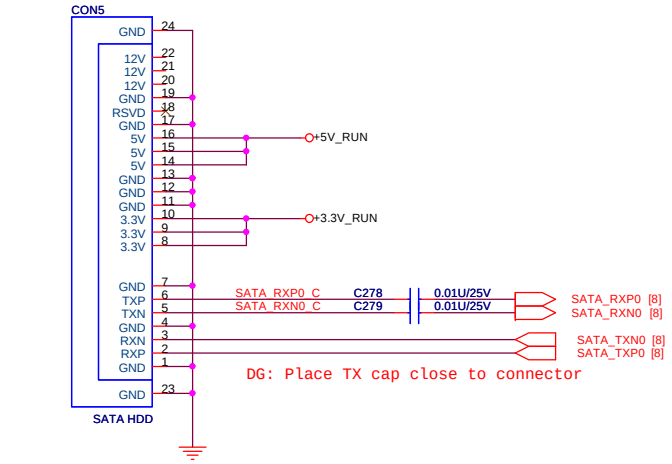
Quanta Computer Inc.

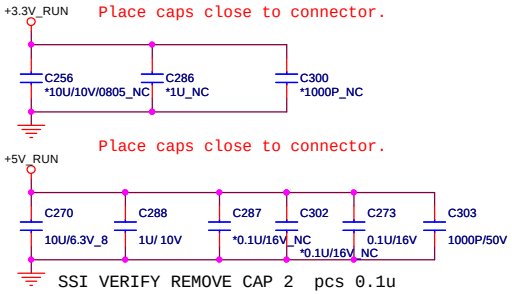
PROJECT : UM7 DIS

Size	Document Number	Rev
	TOUCH PAD, KB	3A

Date: Wednesday, February 03, 2010 Sheet 34 of 52

SATA Connector.





Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	SATA (HDD&CD_ROM)	3A

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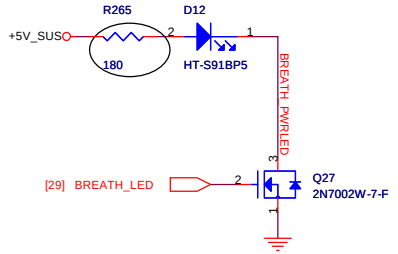
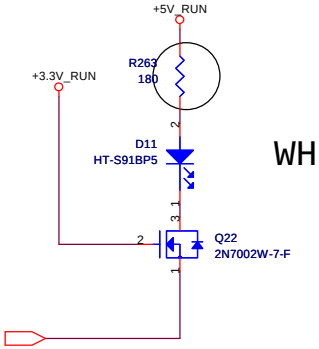
Power

WHITE

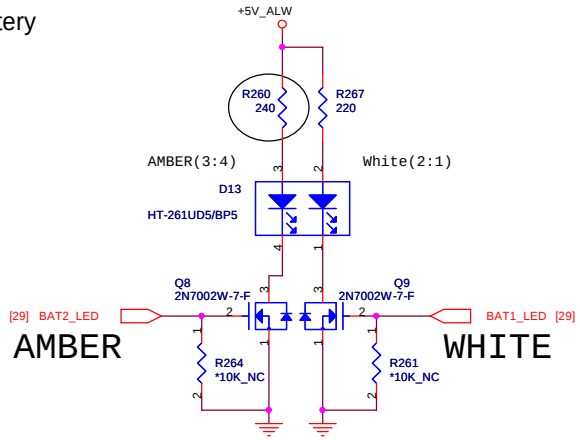


HDD activity LED.



WHITE

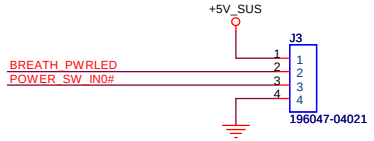
Battery



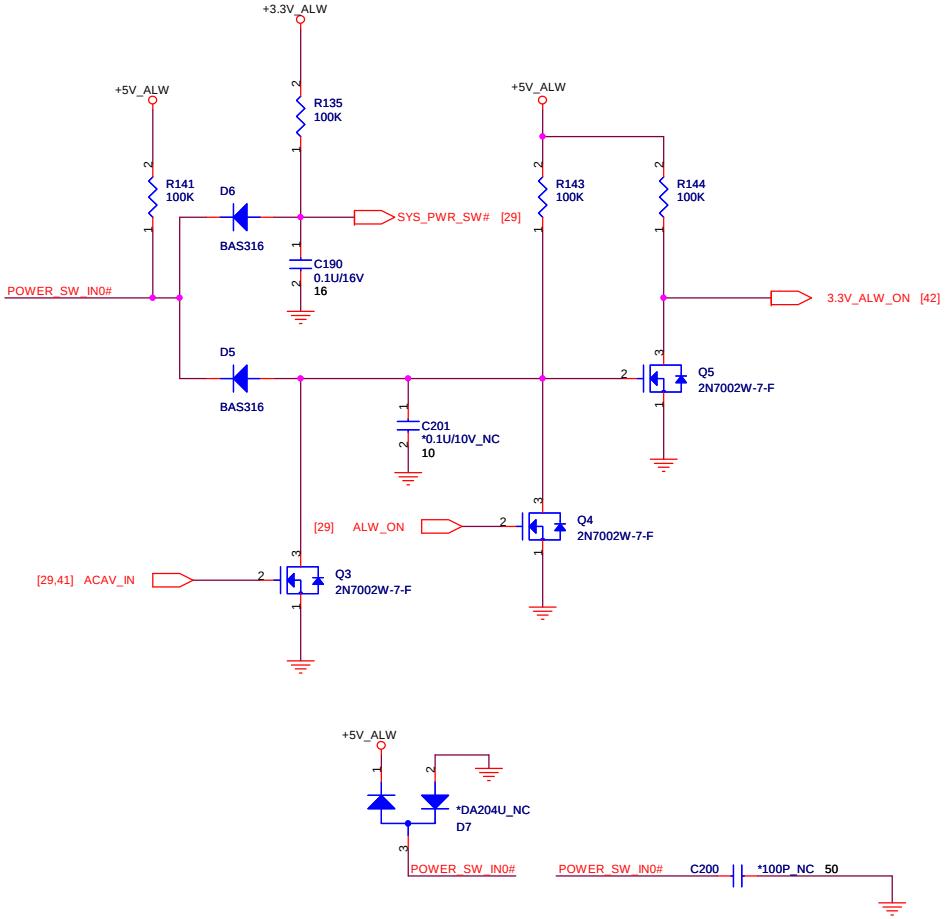
AMBER

WHITE

Power button Cable

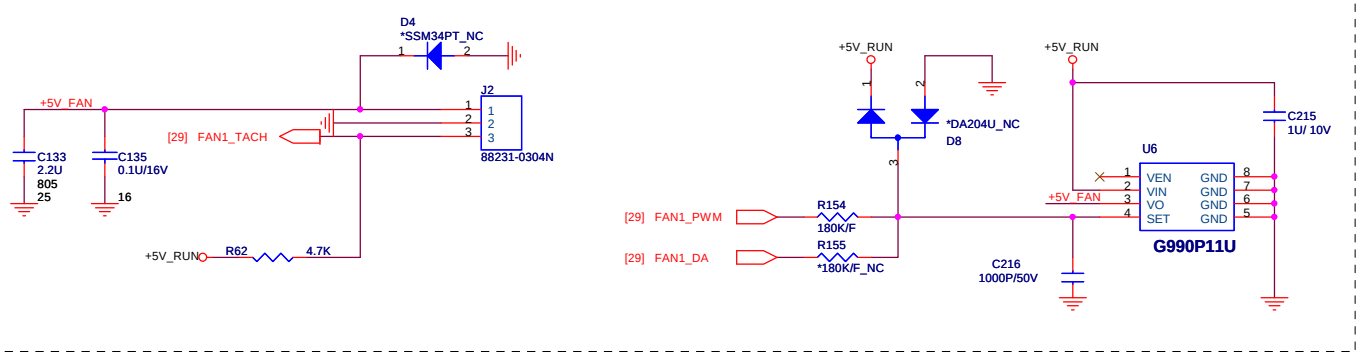


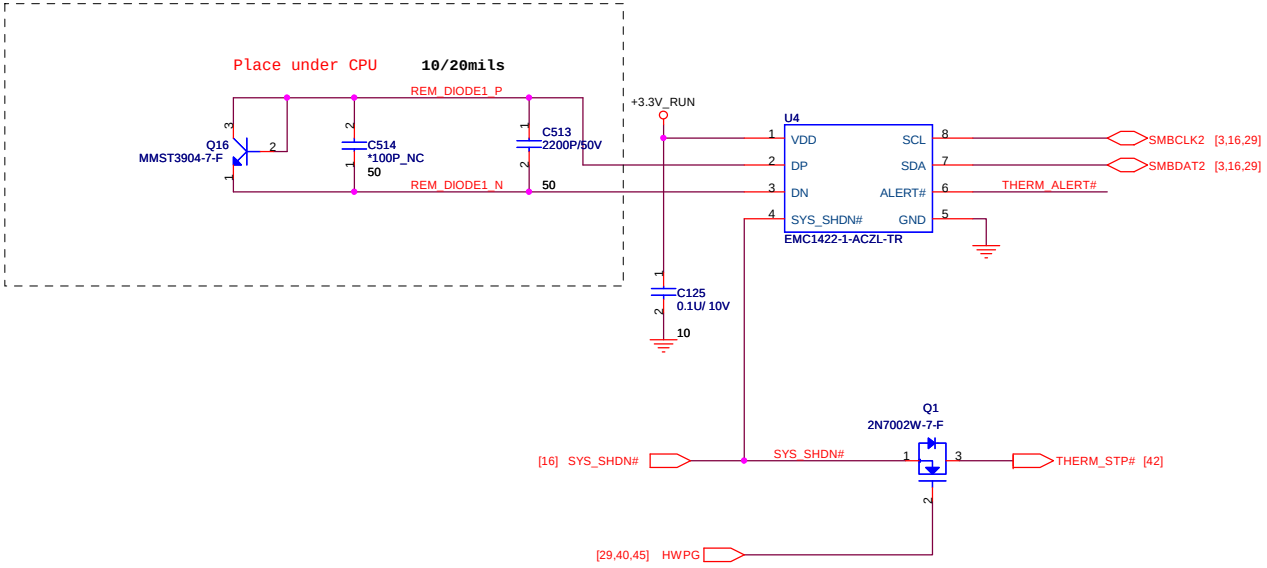
3VALW ON POWER LOGIC

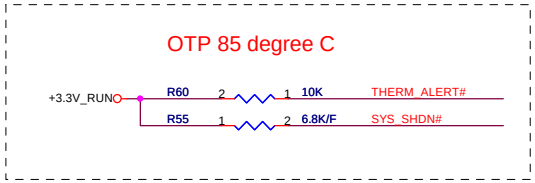


Quanta Computer Inc.		
PROJECT : UM7 DIS		
Size	Document Number: SWITCH, LED	Rev: 3A
Date: Wednesday, February 03, 2010	Sheet 36 of 52	

FAN CONTROL







Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	FAN & THERMAL	3A

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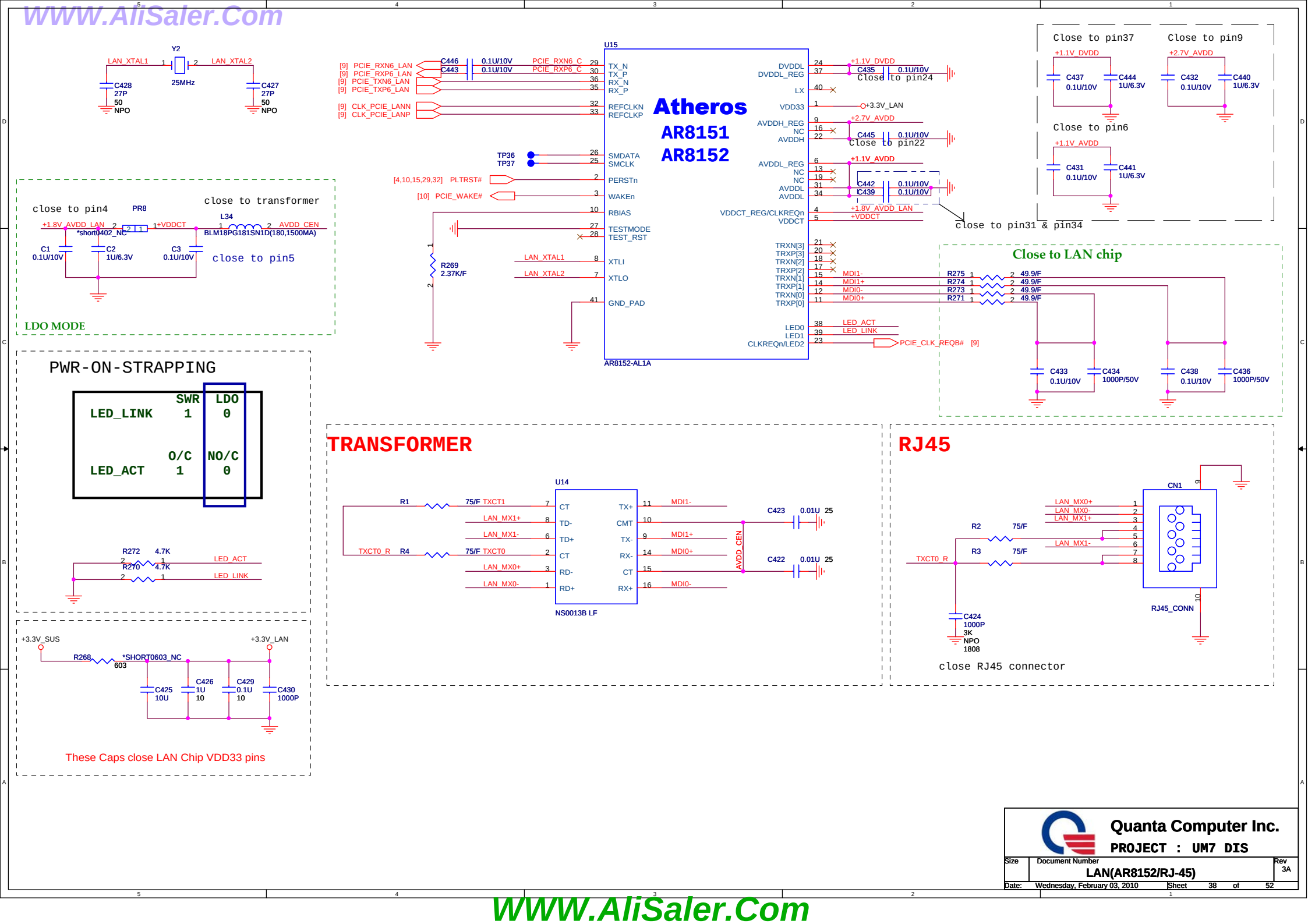


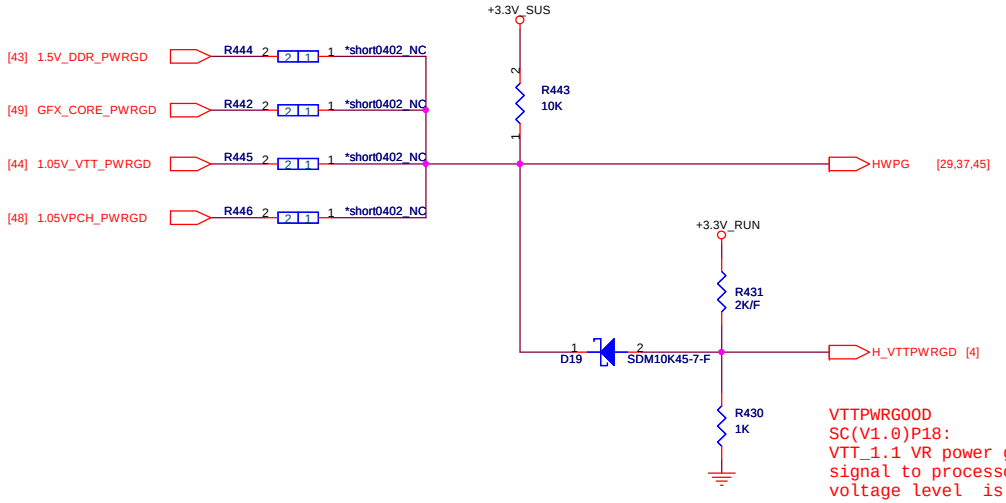
Quanta Computer Inc.	PROJECT : UM7 DIS	
Size	Document Number: LAN(AR8152/RJ-45)	Rev 3A
Date: Wednesday, February 03, 2010	Sheet 38 of 52	

Quanta Computer Inc.

PROJECT : UM7 DIS

Size	Document Number	Rev
	BTB CONN	3A

Date: Wednesday, February 03, 2010 Sheet 39 of 52

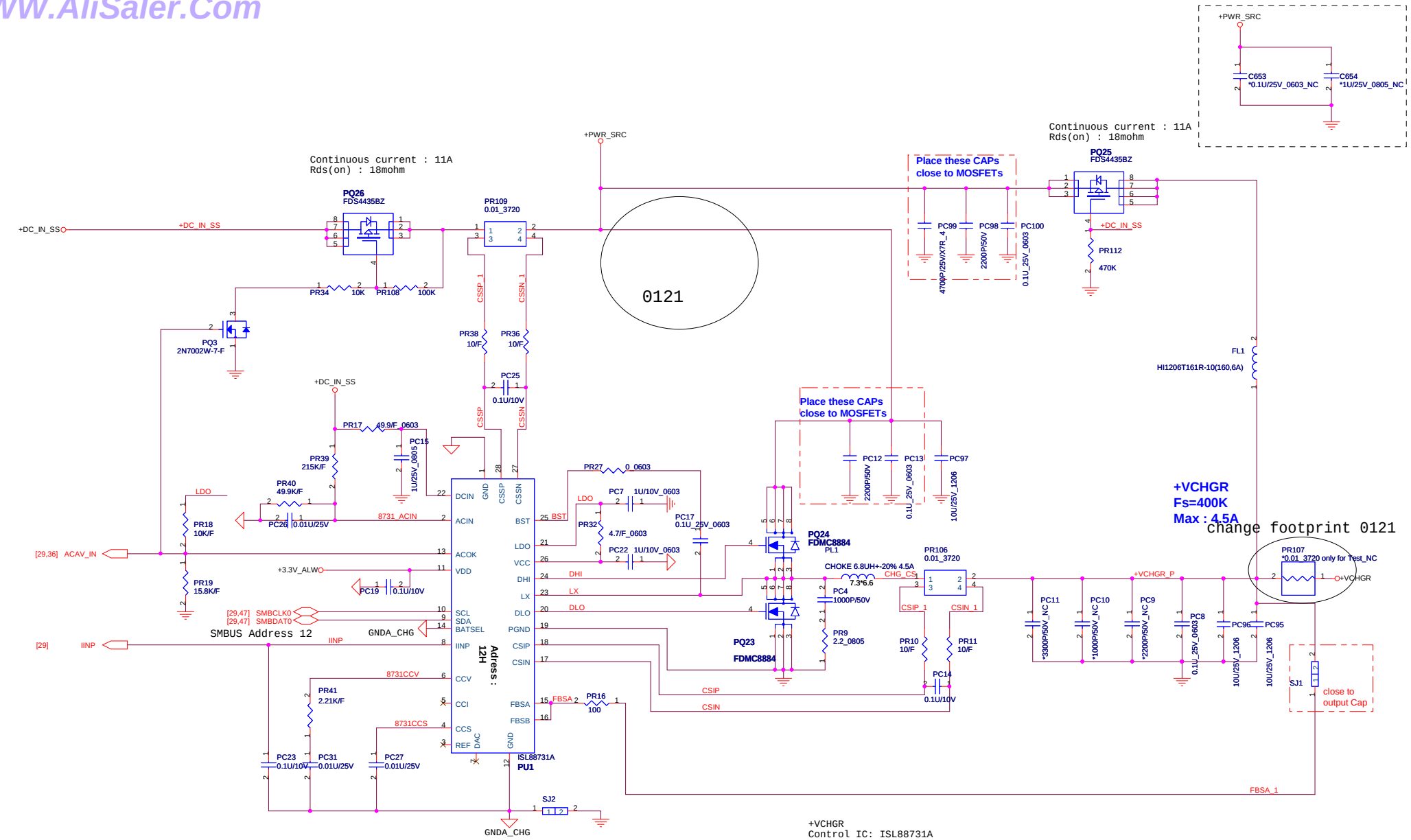


VTTPWRGOOD
SC(V1.0)P18:
VTT_1.1 VR power good
signal to processor. Signal
voltage level is 1.1 V.

Quanta Computer Inc.

PROJECT : UM7 DIS

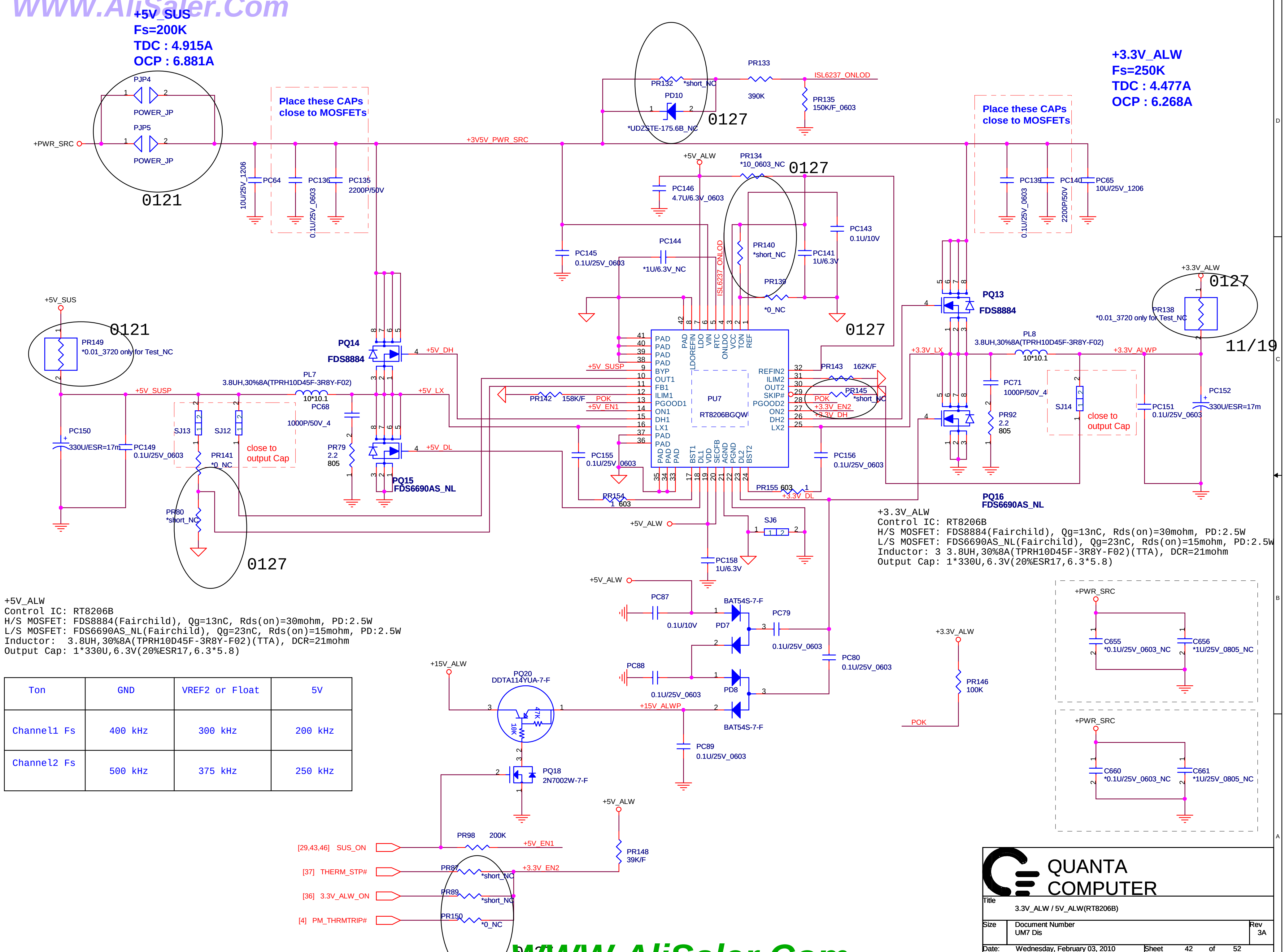
Size	Document Number	Rev
	System Reset Circuit	3A
Date: Wednesday, February 03, 2010	Sheet 40 of 52	



+VCHGR
Control IC: ISL88731A
H/S MOSFET: FDMC8884(FAC), Qg=7nC, Rds(on)=30mohm, PD:2.3W
L/S MOSFET: FDMC8884(FAC), Qg=7nC, Rds(on)=30mohm, PD:2.3W
Inductor: CHOKE 6.8UH+-20% 4.5A DCR=44mohm
Output Cap: 2*10U 25V(+-10%,X6S,1206)

QUANTA COMPUTER

Title	Charger (ISL88731)	
Size	Document Number UM7 Dis	Rev 3A
Date: Wednesday, February 03, 2010	Sheet 41 of 52	



+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,6.3*5.8)

+5V_ALW
Control IC: RT8206B
H/S MOSFET: FDS8884(Fairchild), Qg=13nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS_NL(Fairchild), Qg=23nC, Rds(on)=15mohm, PD:2.5W
Inductor: 3.8UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,6.3*5.8)

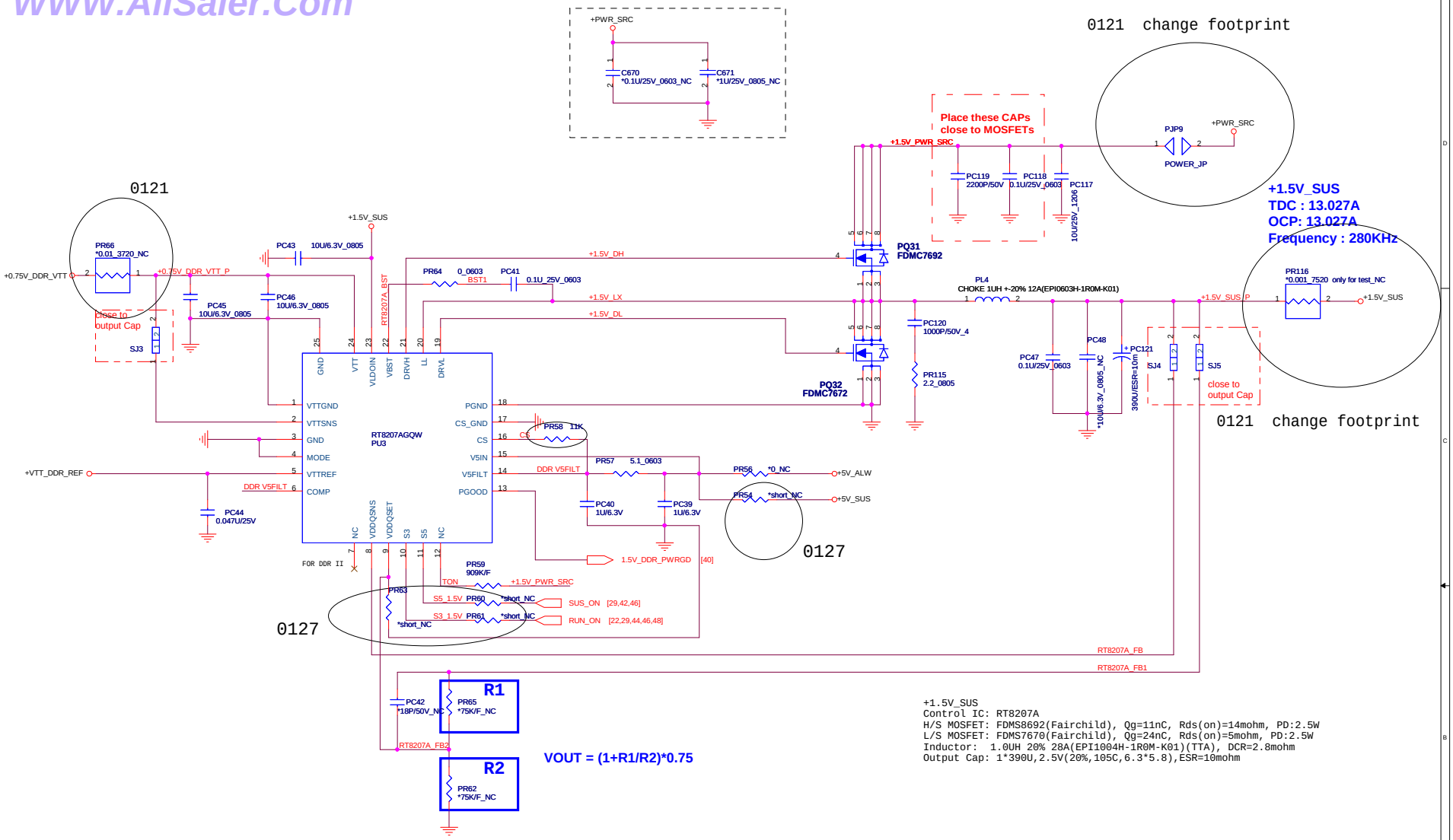
Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

QUANTA COMPUTER

Title: 3.3V_ALW / 5V_ALW(RT8206B)

Size | Document Number: UM7 Dis | Rev: 3A

Date: Wednesday, February 03, 2010 | Sheet 42 of 52



VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

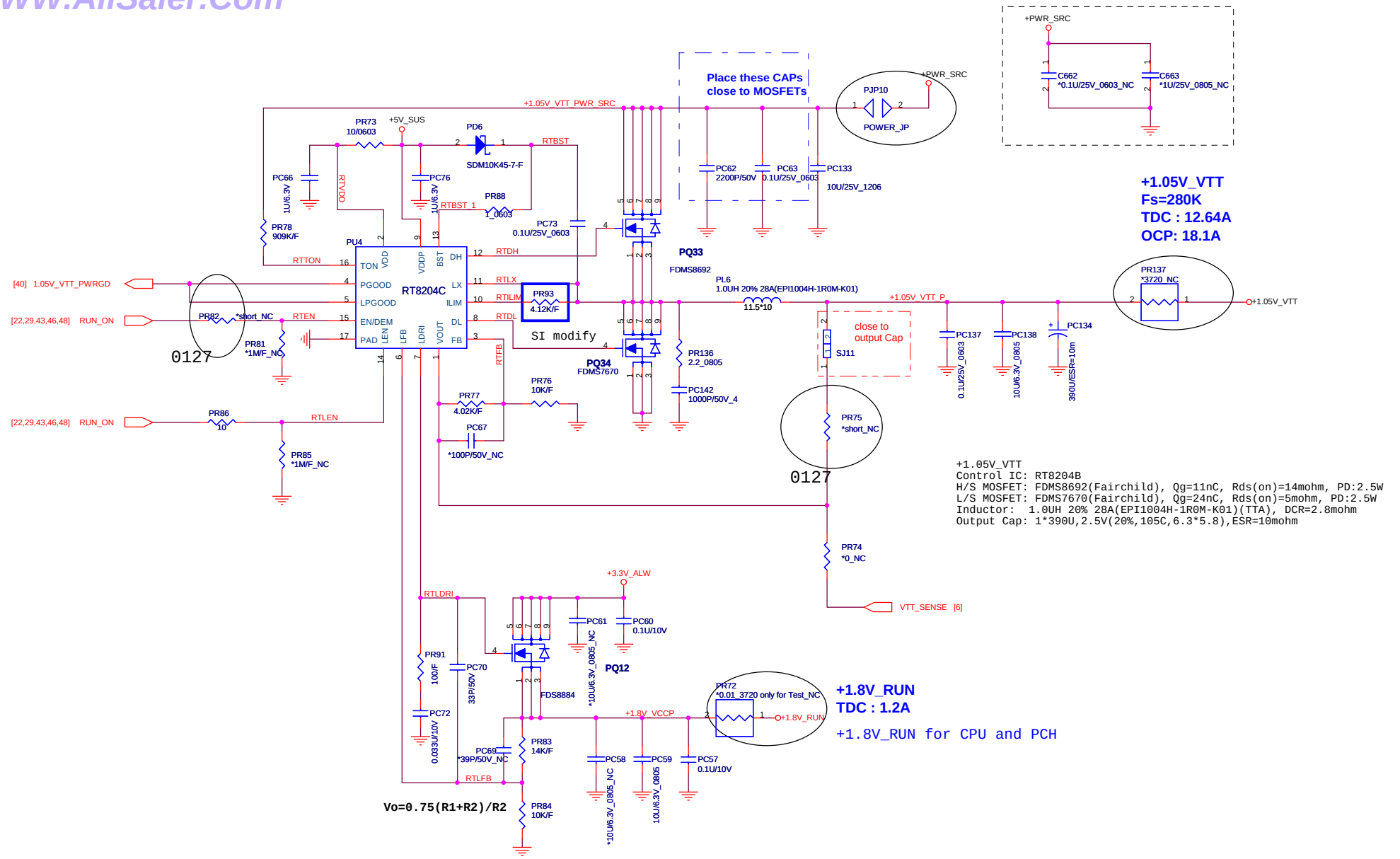
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

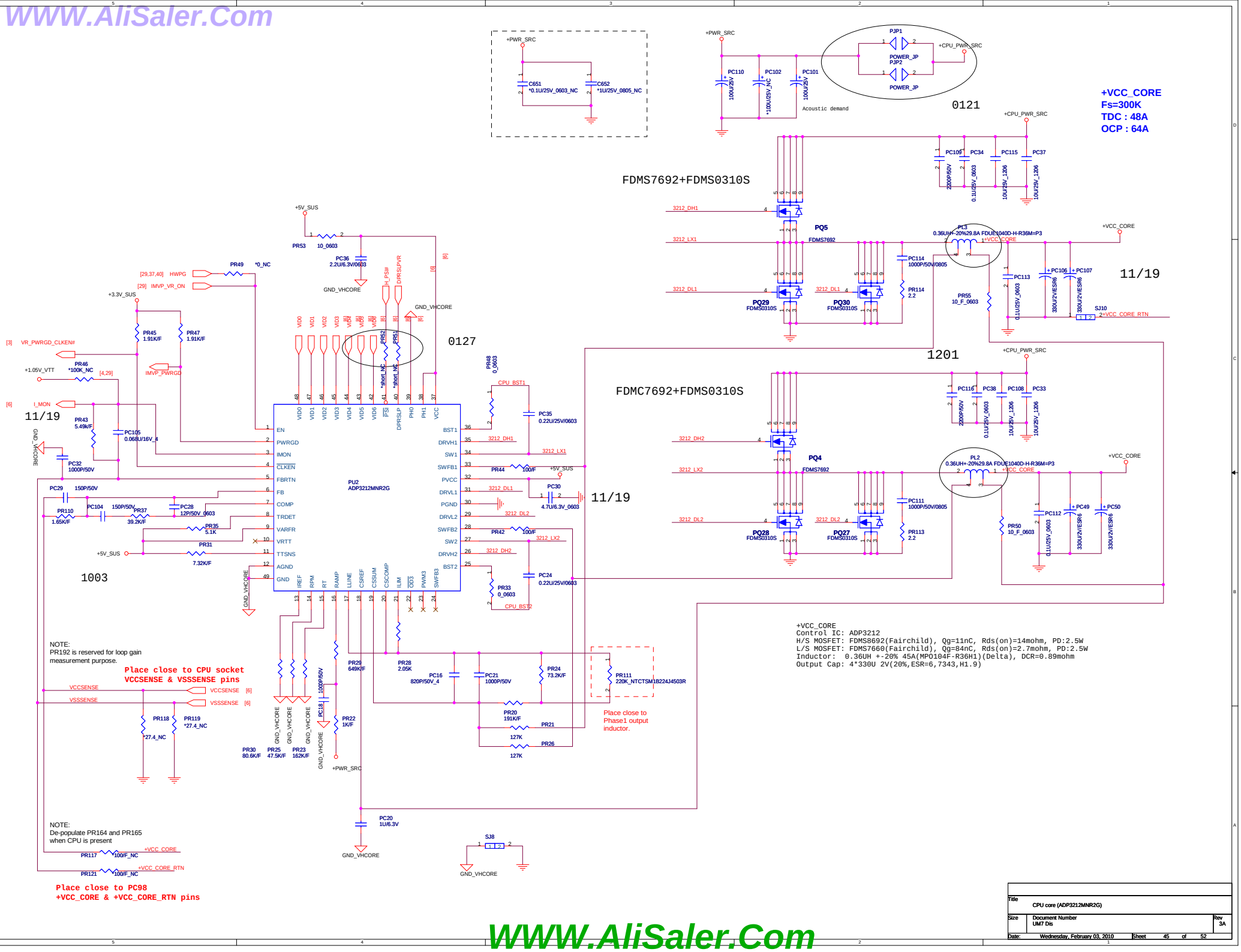
Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Title	DDR3 +1.5V_SUS(RT8207AGQW)		
Size	Document Number UM7 Dis		Rev 3A
Date: Wednesday, February 03, 2010	Sheet 43 of 52		

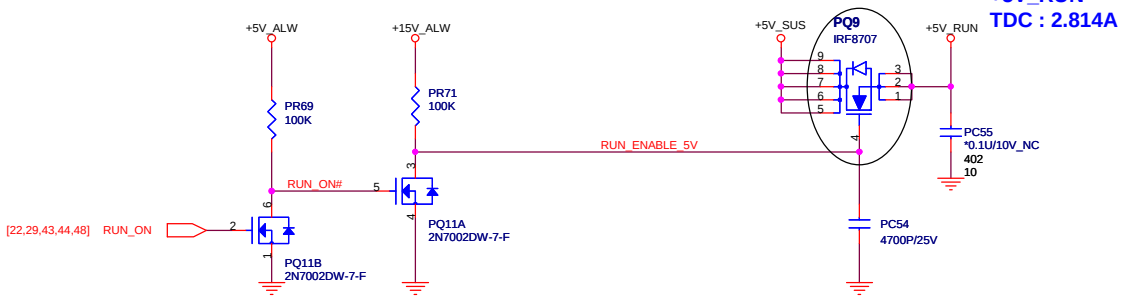


Title	+1.05V_VTT(RT8204B)	
Size	Document Number UM7 Dis	Rev 3A
Date: Wednesday, February 03, 2010	Sheet 44 of 52	

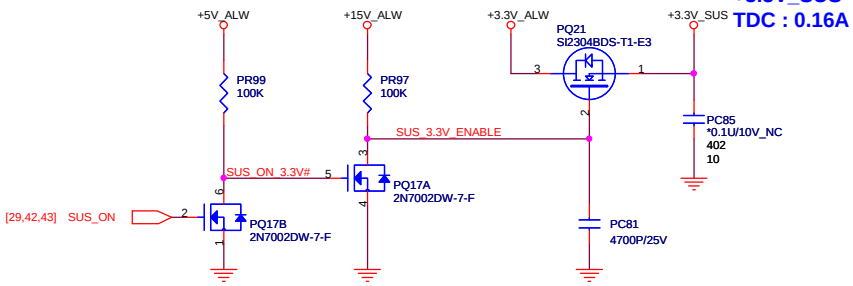


Title	CPU core (ADP3212MNR2G)		
Size	Document Number UM7 Dis		Rev 3A
Date:	Wednesday, February 03, 2010	Sheet 45 of 52	

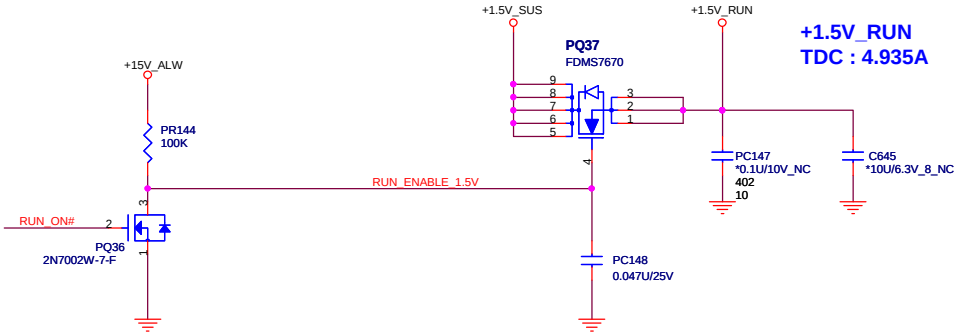
+5V_RUN
TDC : 2.814A

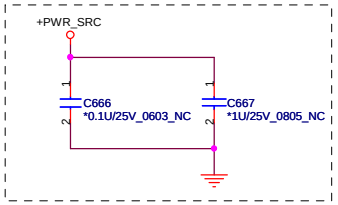


+3.3V_SUS
TDC : 0.16A

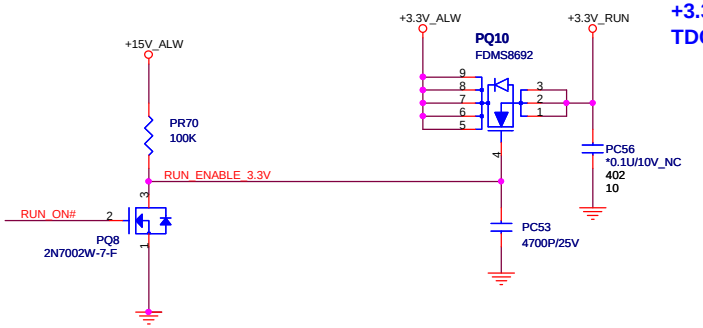


+1.5V_RUN
TDC : 4.935A

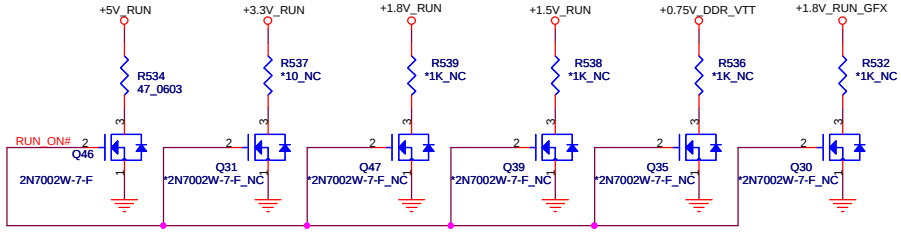


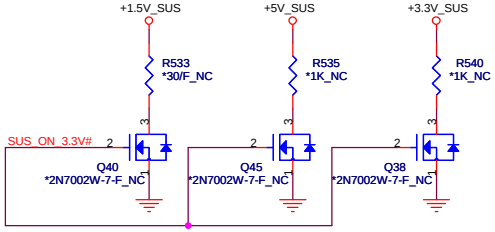


+3.3V_RUN
TDC : 2.237A



Reserve discharge path





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Title	RUN / SUS POWER SW	
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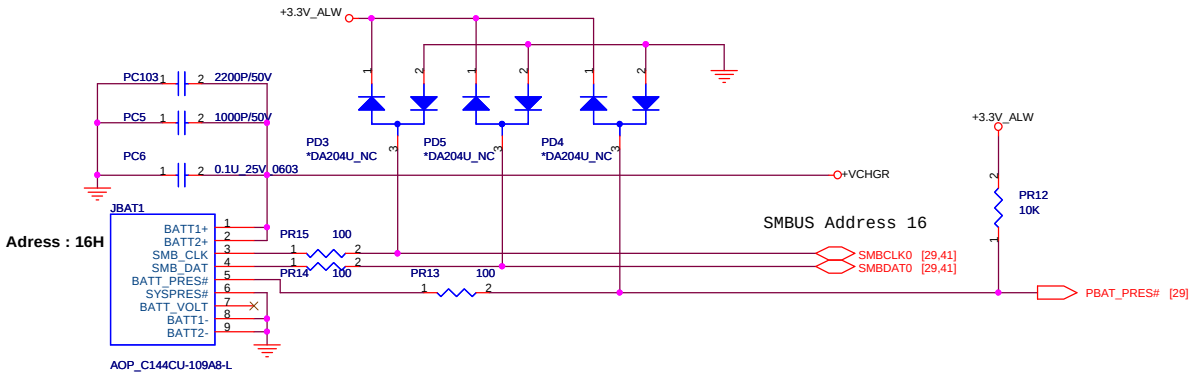

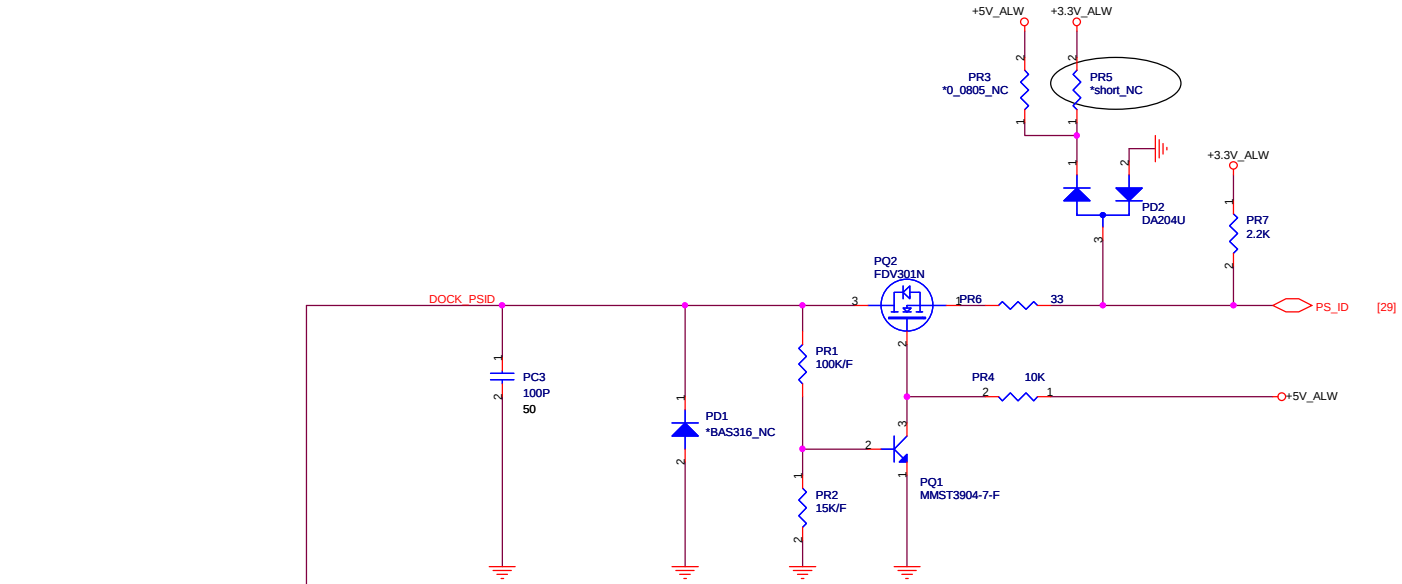

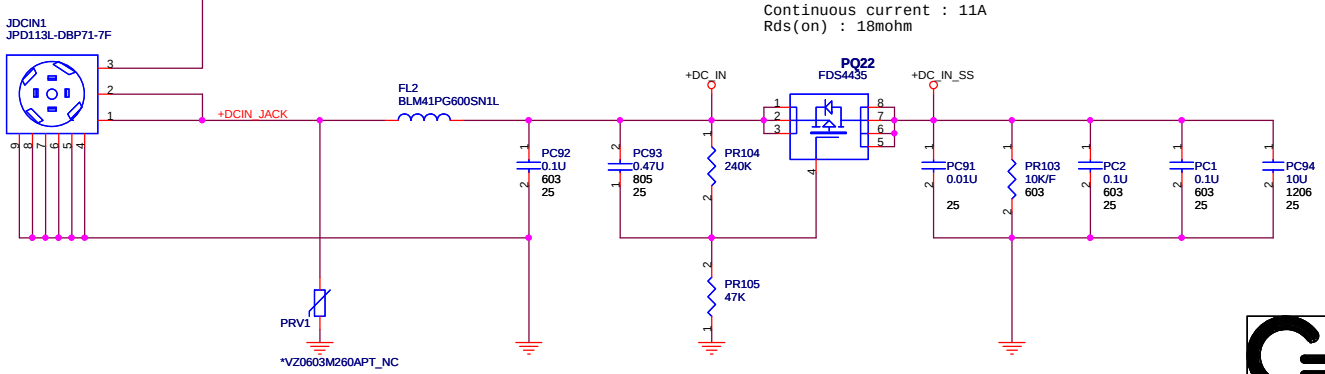

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Title	DCIN,BATT CONNECTOR	
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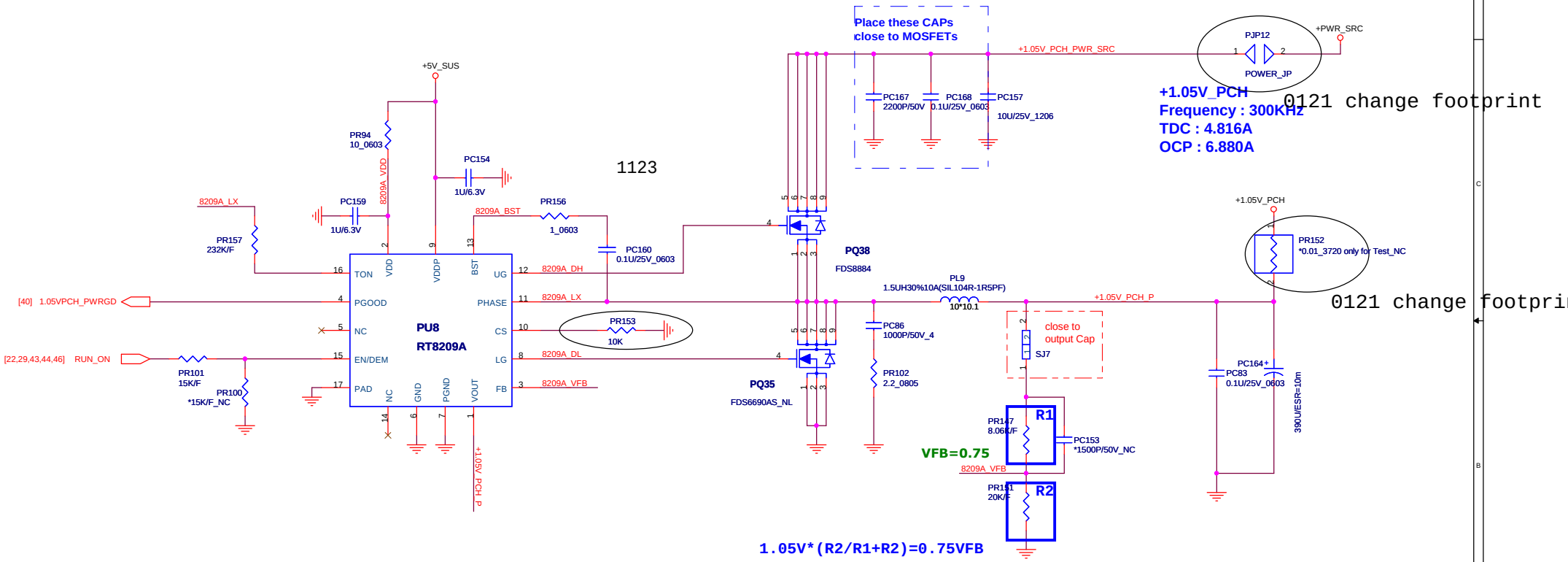

0121 change footprint

Title	+1.05V_PCH(RT8209A)	
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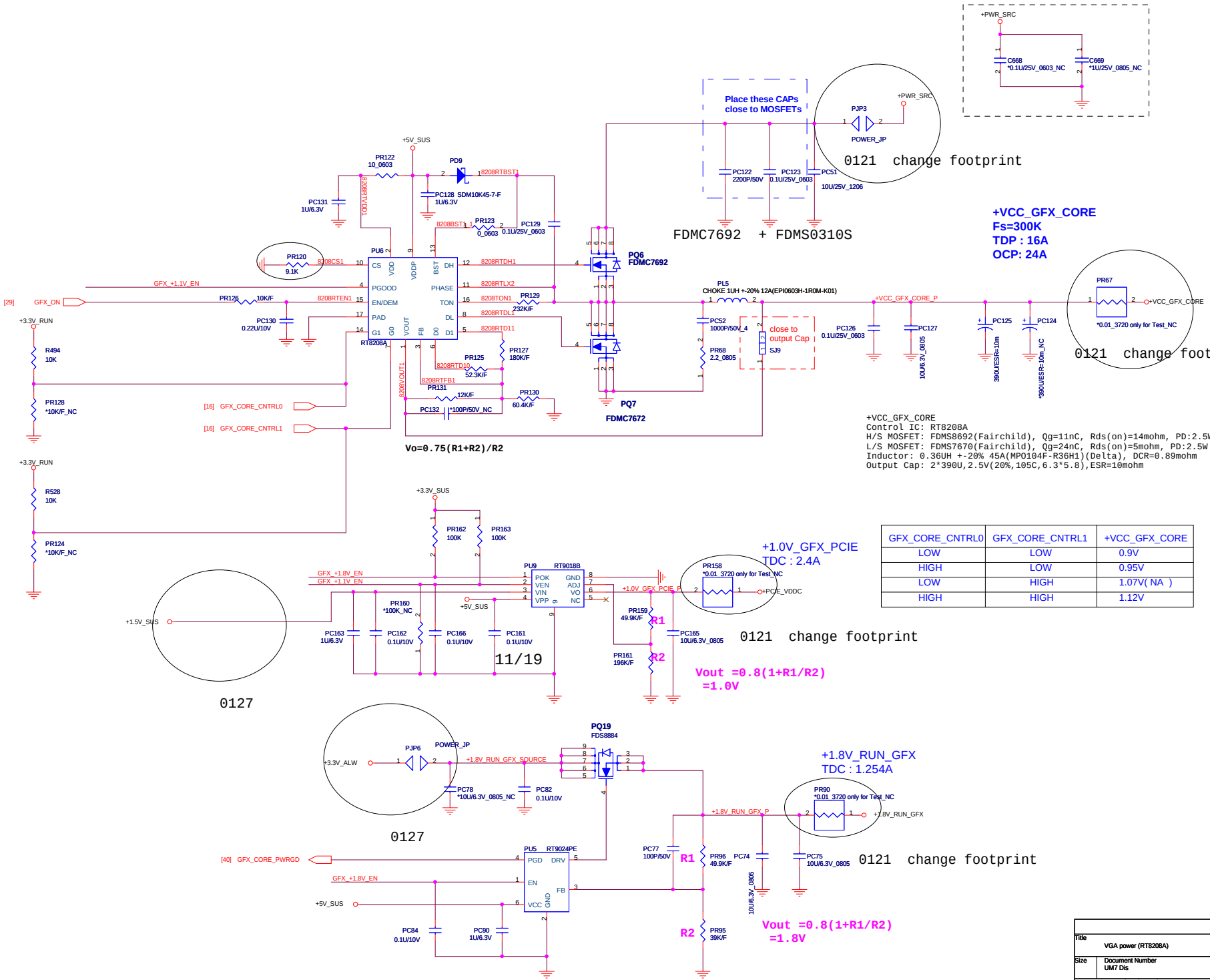

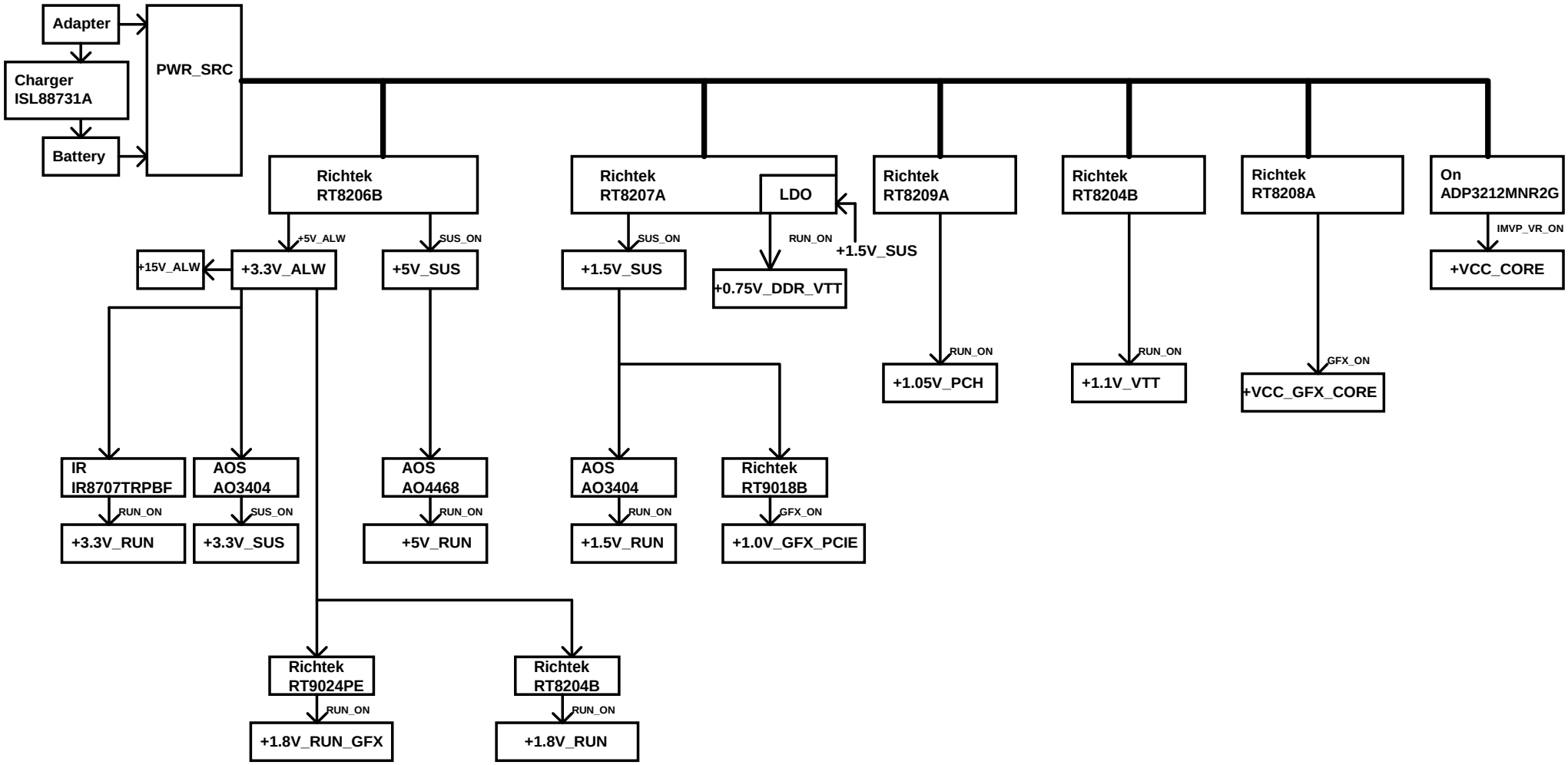

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Power Design Block Diagram 2009/08/24

(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2) SYS_PWR_SW#
(3) 3.3V_ALW_ON, ALW_ON
(4) +3.3V_ALW, +5V_ALW, +15V_ALW
(5) SUS_ON
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
(7) ICH_RSMRST#
(8) SIO_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) GFX_ON
(11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
(12) RUN_ON_1(RUN_ON)
(13) +0.75V_DDR_VTT
(14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
(16) IMVP_VR_ON
(17) +VCC_CORE, IMVP_PWRGD
(18) RESET_OUT#
(19) ICH_PWRGD
(20) PM_DRAM_PWRGD
(21) CLK_CPU_BCLK(PCH to CPU)
(22) H_PWRGOOD
(23) PLTRST#(PCI_PLTRST#)

Power Jack
Adapter input
+DC_IN
SI4835
+DC_IN_SS
SI4835
+PWR_SRC
Charger
ISL88731
Page 45
Battery
+VCHGR
SI4835
+PWR_SRC

+5V_VCC1 (from +5V_ALW2)
SYSTEM POWER
RT8206
Page 46
LDO
VR
+5V_ALW2
+3.3V_ALW
+5V_ALW
+3.3V_ALW_ON(From 3VALW ON POWER LOGIC)
ALW_ON(For +5V_ALW and +15V_ALW turn on)

+5V_ALW
Diode & Cap
Page 46
+15V_ALW
3V_ALW_PWRGD
5V_ALW_PWRGD

+5V_ALW
VRAM DDR3 POWER
RT8207
Page 47
VR
LDO
+1.5V_SUS
1.5V_DDR_PWRGD
+0.75V_DDR_VTT
SUS_ON
RUN_ON

+5V_ALW
PCH CORE POWER
RT8204
Page 48
VR
+1.05V_PCH
1.05V_PWRGD
RUN_ON

SI4800 Page 52 — +5V_ALW → +5V_SUS; SUS_ON
SI4800 Page 52 — +3.3V_ALW → +3.3V_SUS; SUS_ON
SI4800 Page 52 — +5V_ALW → +5V_RUN; RUN_ON
FDS8880 Page 52 — +3.3V_ALW → +3.3V_RUN; RUN_ON
SI2303 Page 17 — +3.3V_RUN → +3.3V_DELAY; GFX_ON
FDS6298 Page 52 — +1.5V_SUS → +1.5V_RUN; RUN_ON

+5V_SUS
GFX CORE POWER
RT8208
Page 50
VR
+VCC_GFX_CORE
GFX_CORE_PWRGD
GFX_ON

+5V_ALW
GFX PCIE POWER
RT9018B
Page 50
VR
+1.1V_GFX_PCIE
GFX_PCIE_PWRGD
GFX_ON

+5V_ALW
GFX POWER
RT9024PE
Page 44
VR
+1.8V_RUN_GFX
1.8V_RUN_GFX_PWRGD
RUN_ON

+5V_SUS
+3.3V_SUS
CPU CORE POWER
MAX17036GTL+
TWO PHASE SOLUTION
Page 51
VR
+VCC_CORE
IMVP_PWRGD
VR_PWRGD_CLKEN#
IMVP_VR_ON

+5V_ALW
CPU Memory Control & I/O Power
RT8209
Page 49
VR
+1.1V_VTT
1.1V_VTT_PWRGD
RUN_ON

+5V_ALW
CPU VCCPLL
RT9018B
Page 44
VR
RUN_ON
+1.8V_RUN
1.8V_RUN_PWRGD

CLK GEN
Page 15
CK_PWRGD_R

Reset Circuit
Page 42
Inverter
AND Gate
Wire AND
AND Gate
VR_PWRGD_CLKEN# → CK_PWRGD_R
1.5V_DDR_PWRGD, RUN_ON_1 → RUN_ON
1.1V_VTT_PWRGD, 1.05V_PWRGD, GFX_PCIE_PWRGD, GFX_CORE_PWRGD, 1.8V_RUN_PWRGD, 1.8V_RUN_GFX_PWRGD, IMVP_PWRGD, RESET_OUT# → HWPG, H_VTTPWRGD, ICH_PWRGD

SYS_PWR_SW#
EC IT8502
Page 29
3.3V_ALW_ON
ALW_ON
SUS_ON
SIO_PWRBTN#
ICH_RSMRST#
SIO_SLP_S5#
SIO_SLP_S3#
RUN_ON_1
IMVP_VR_ON
RESET_OUT#
HWPG
IMVP_PWRGD
ICH_PWRGD
PCH
Page 7~12
SIO_SLP_S4#
PM_DRAM_PWRGD
CLK_CPU_BCLK
H_PWRGOOD
PLTRST#(PCI_PLTRST#)
To control DIMM VREF
H_VTTPWRGD
CPU
Page 3~6

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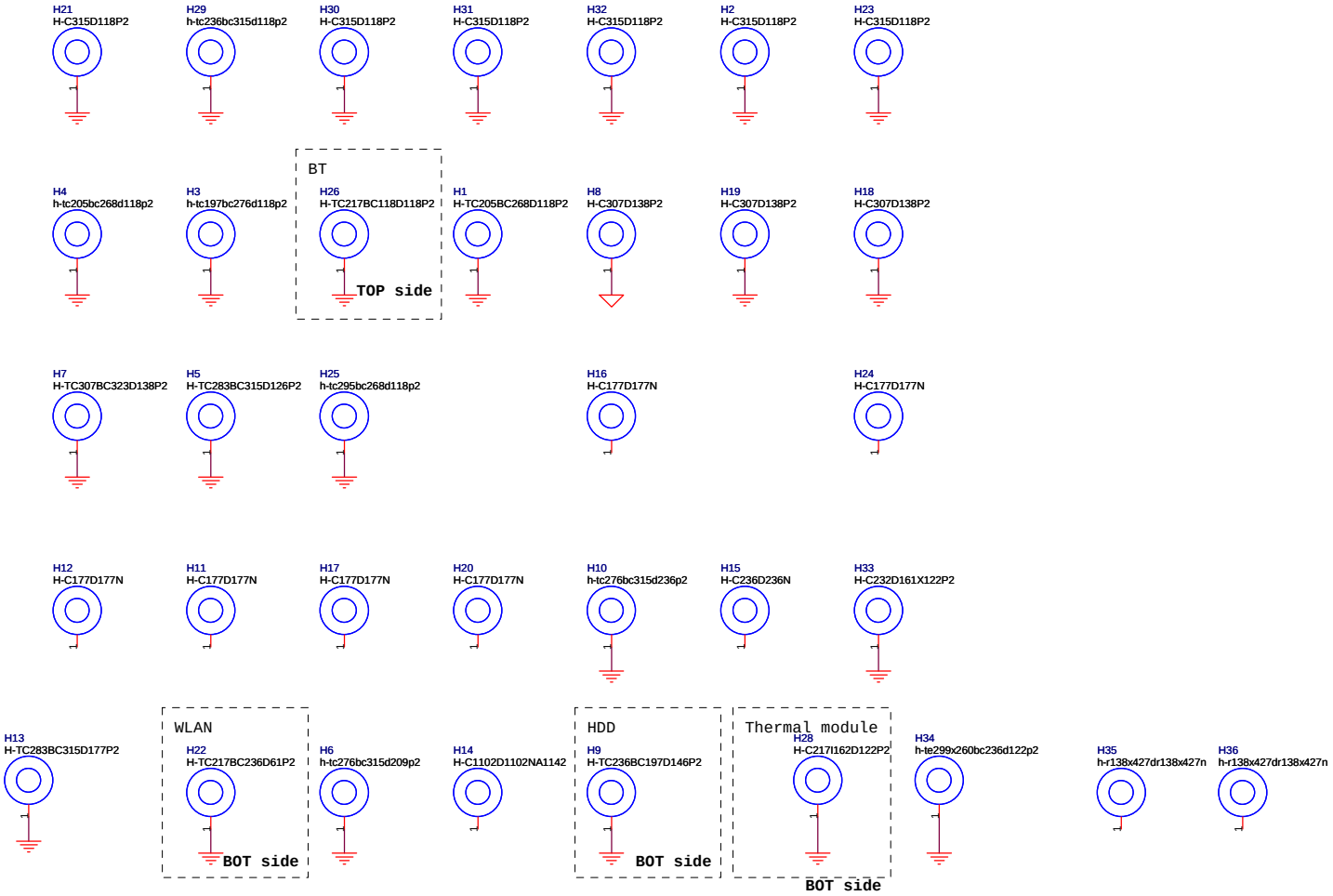

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