

LCFC Confidential

NANO G ACL CG521 M/B Schematics Document


AMD FP4 Carrizo L SOC with DDRIII L

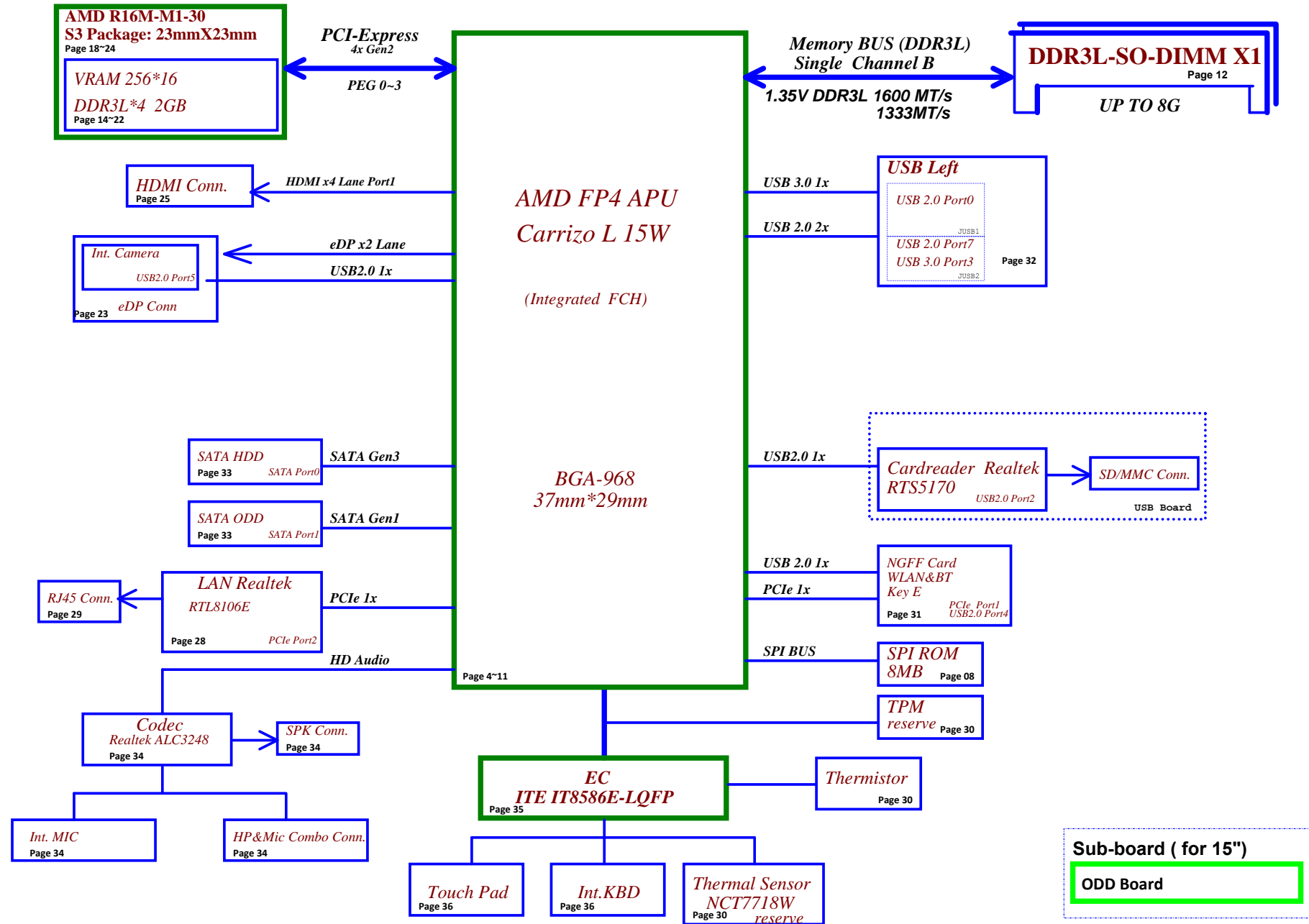
AMD R16M-M1-30

2016-02-24

REV:1.0

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Voltage Rails (O --> Means ON , X --> Means OFF)

power plane	B+ (+20VSB)	+5VALW (+3VALW_APU)	+1.35V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.675VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
State	+3VL +5VLP	+1.8VALW +0.95VALW +0.775VALW		
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

BOARD Config.	BOARD_ID0	BOARD_ID1	BOARD_ID2	Function
	0: 14''	0: Dis		
	1: 15''	1: UMA		

USB Port Table for CarrizoL

USB 2.0	USB 3.0	Port	Port device
EHCI0		0	RIGHT USB (2.0)
		1	N/A
		2	Card Reader
		3	Touch screen
EHCI1		4	Blue Tooth
		5	Camera
		6	LEFT USB (3.0)
		7	LEFT USB (3.0)
xHCI		0	
		1	

USB Port Table for Carrizo

USB 2.0	USB 3.0	Port	Port device
EHCI0		0	RIGHT USB (2.0)
		1	N/A
		2	Card Reader
		3	Touch screen
		4	Blue Tooth
		5	Camera
		6	LEFT USB (3.0)
		7	LEFT USB (3.0)
xHCI		2	
		3	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_PX@	EMC GPU part
EMC_CZ@	EMC Carrizo APU part
EMC_15@	EMC 15 part
RF_NS@	RF reserve Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
AOAC@	AOAC support part
HDT@	HDT Debug part
TS@	Touch screen part
CZ@	Carrizo Part
CZL@	CarrizoL part
CZPX@	Carrizo Discrete Part
CZLPX@	CarrizoL Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2GX4@	X76 SAMSUNG 1G
M2GX4@	X76 MICRON 1G
H2GX4@	X76 HYNIX 1G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
S1G@	SAMSUNG 1G
M1G@	MICRON 1G
H1G@	HYNIX 1G
CZLUMA@	CarrizoL UMA Part
CZUMA@	Carrizo UMA Part
SIVCD@	SIV COST down material
HDMI@	HDMI Logo

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	HDMI Convert Reserve
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS +3VS_VGA	V	X		X	X	V	V APU SID 1.8VS for CPU 3VS for GPU	X	V
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Battery	0X16	Thermal Sensor	1001_100xb(reserve)
Charger	0001 0010 b	GPU	0x41(default)
		APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting
		HDMI Convert	RSVD

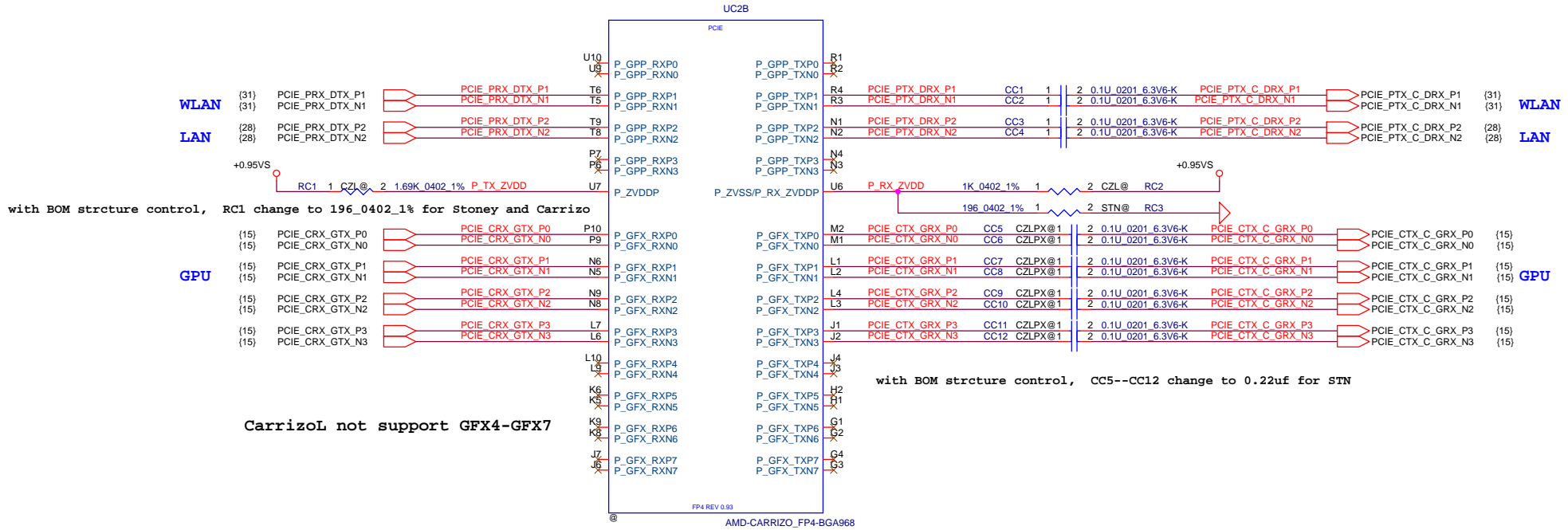
APU SM Bus address

Device	Address
DDR DIMMA	0xA0h
DDR DIMMB	0xA2h
WLAN	RSVD

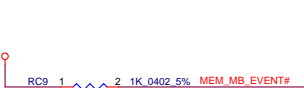
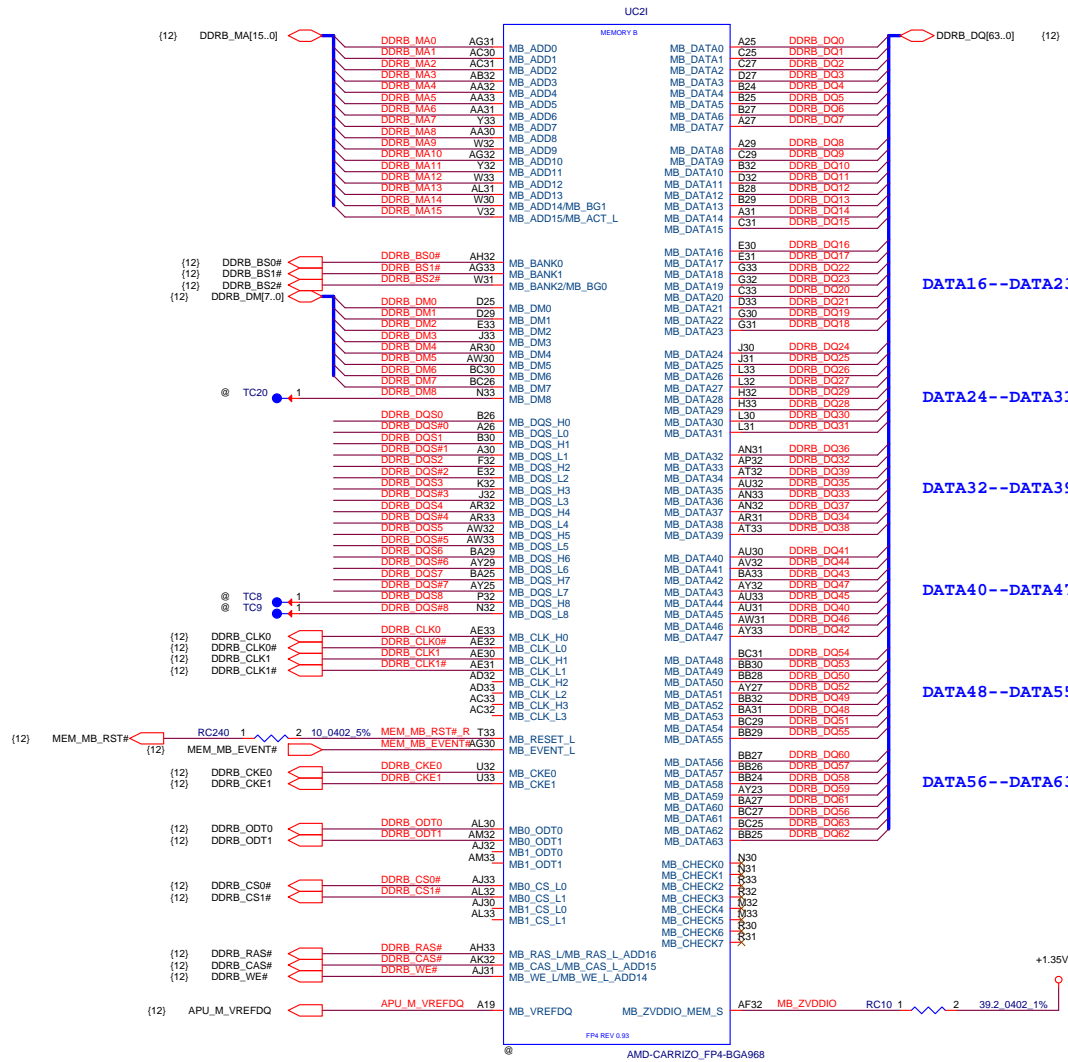
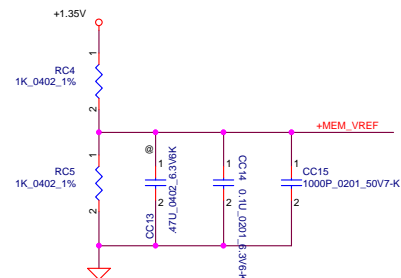
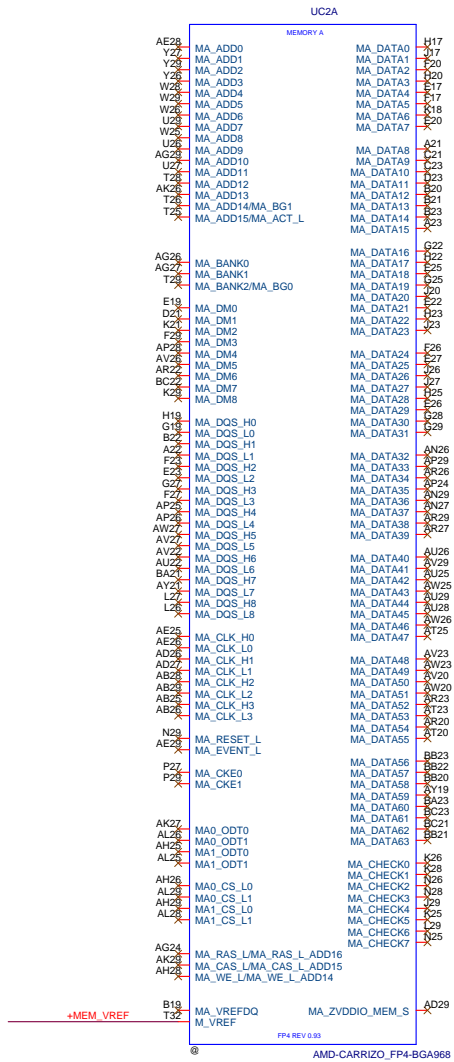
PCIe PORT LIST

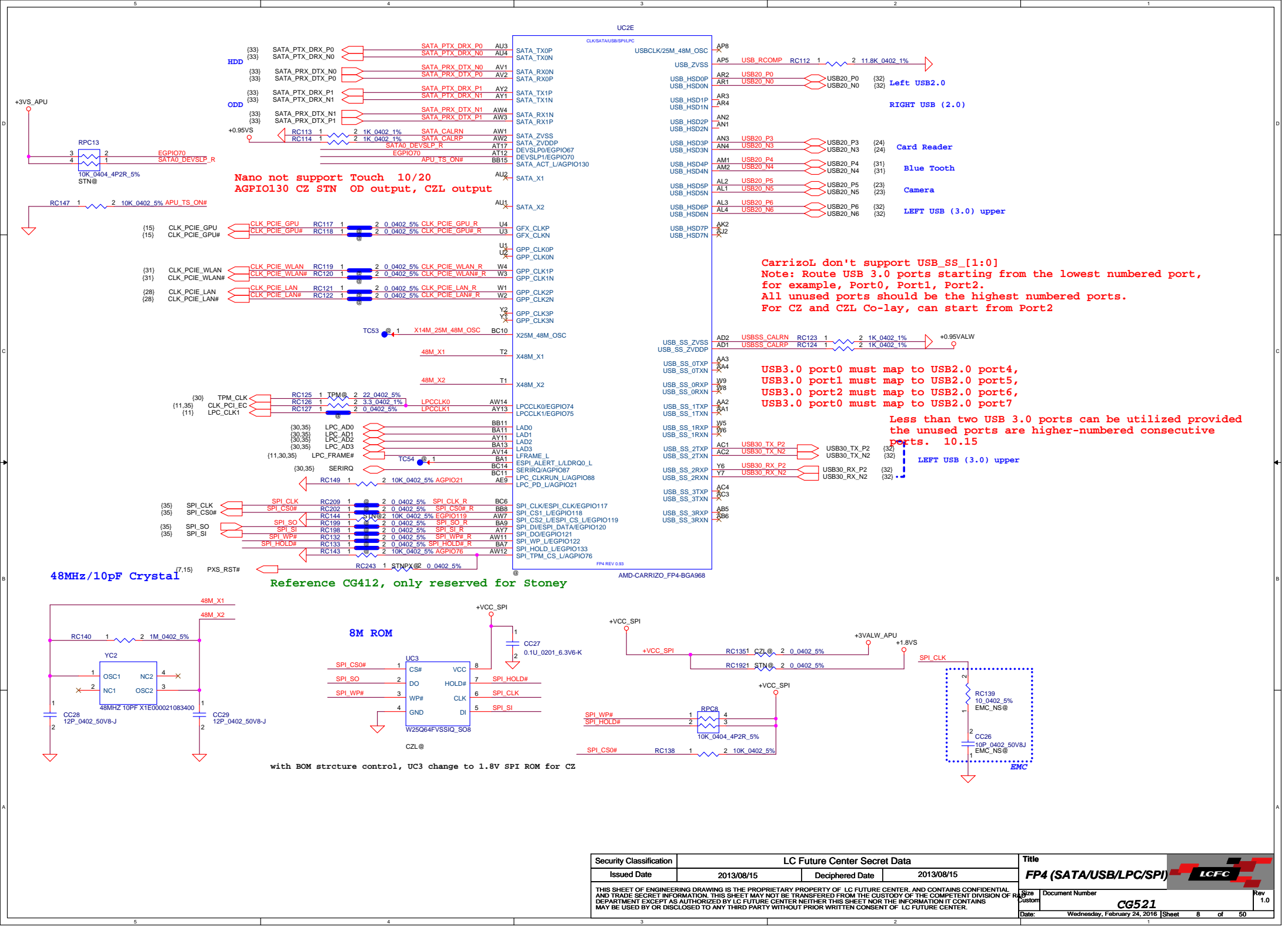
	Port	Device	
GPP	0	N/A	
	1	WLAN	
	2	LAN	
	3	N/A	
GFX	0	CZL GPU	CZ GPU
	1		
	2		
	3		
	4	N/A	
	5		
	6		
	7		

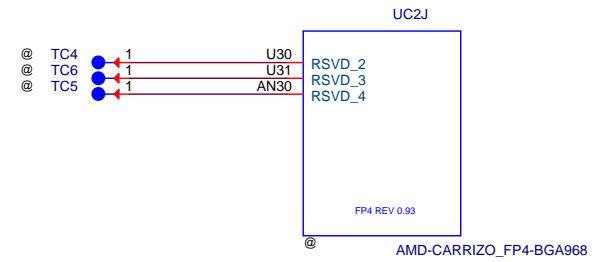
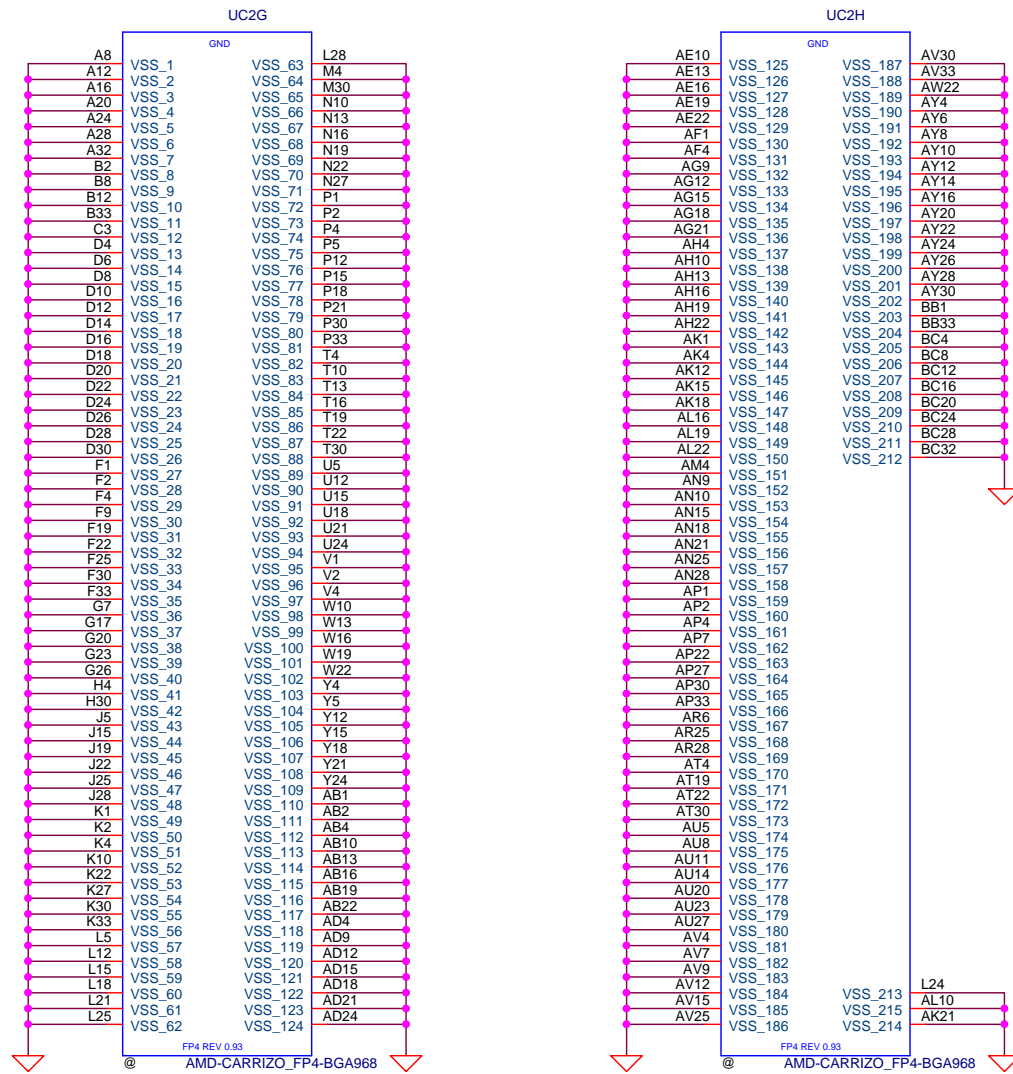
VRAM




CarrizoL not support ChannelA

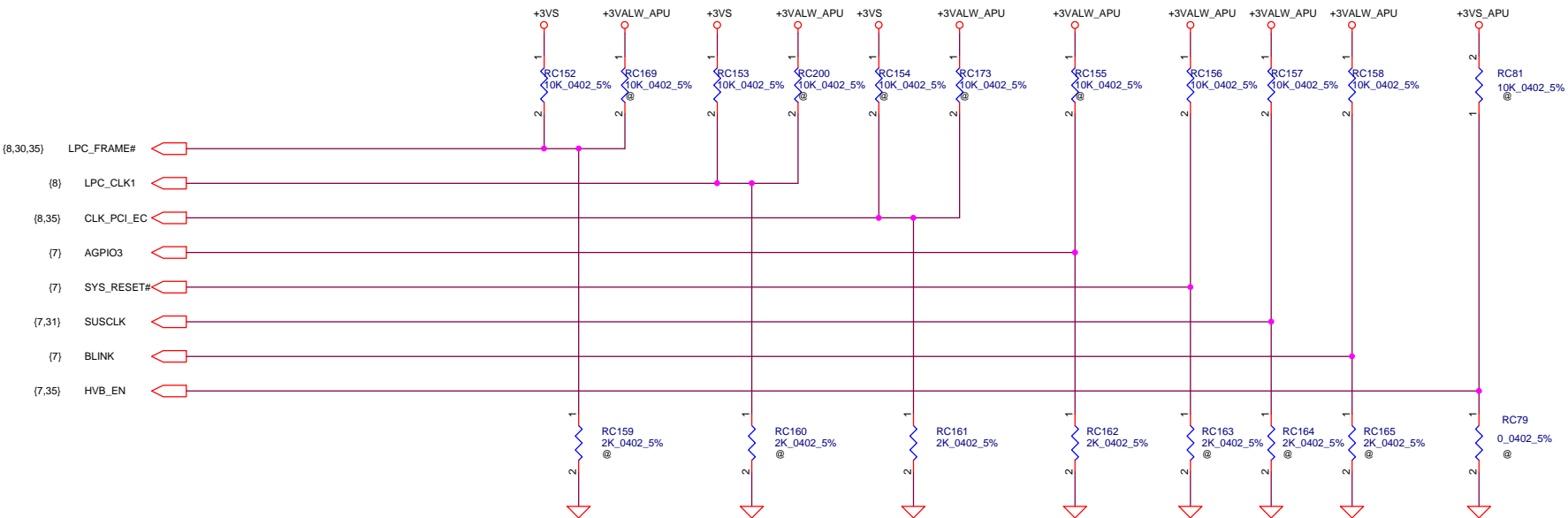






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STRAP PINS



Signal	LFRAME_L	LPCCLK1	LPCCLK0	GEVENT2_L/AGPIO3		SYS_RESET_L	RTCCLK	BLINK(for CZL strap)	HVB_EN
				Int pull-up		Int pull-up	Int pull-up	Int pull-up	
Type	II	II	II	II	I	I	I	I	
PULL HIGH	SPI ROM	Internal CLK Gen	Boot Fail Timer Enabled	CZL	CZ	Normal Power Up &Reset Timing	Coin Battery	PWROK and RST_L pin routed to APU	floating Disable HVB on FP4 platforms
	Default	Default		1.8V SPI	Enhanced reset logic (for quicker S5 resume) Default				
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	3.3VSPi Default	Default to traditional reset logic	Reserved	Direct DC	Reserved	connected to VSS Enable HVB on FP4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST_L,they are captured only once when power is first applied to the processor

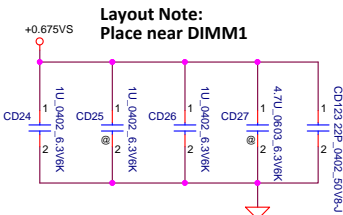
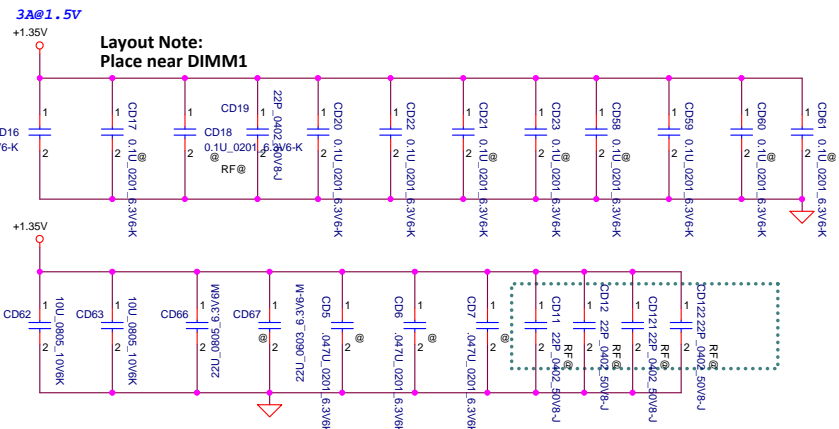
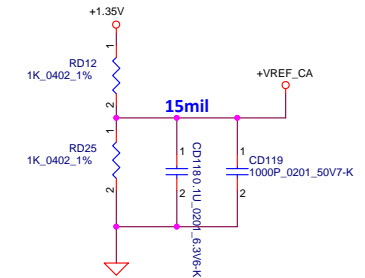
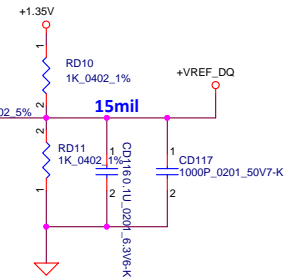
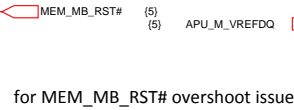
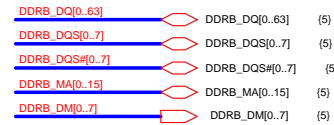
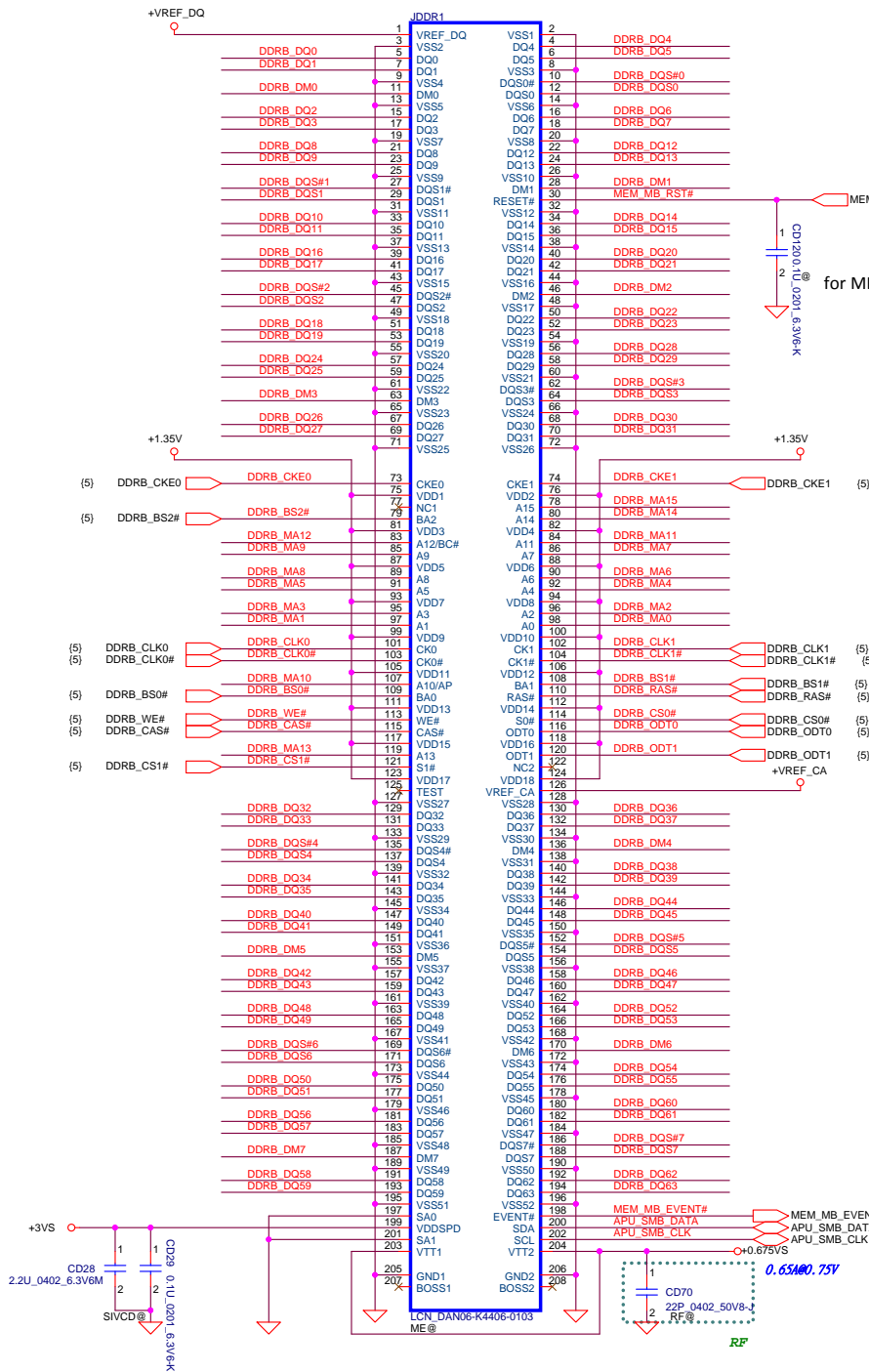
Type II straps become valid after PWR_GOOD is asserted, straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.

Type II straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.


If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

Platforms that are designed for AOAC complaint are recommended to use the Alternate Reset by strapping this pin to '1' for CZ AGPIO3

DDR3 SO-DIMM A

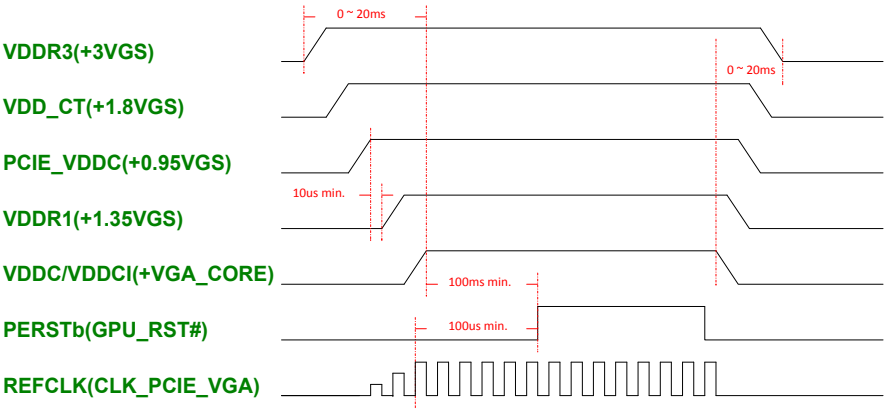
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DDRIII SO-DIMM A			
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Power-Up/Down Sequence

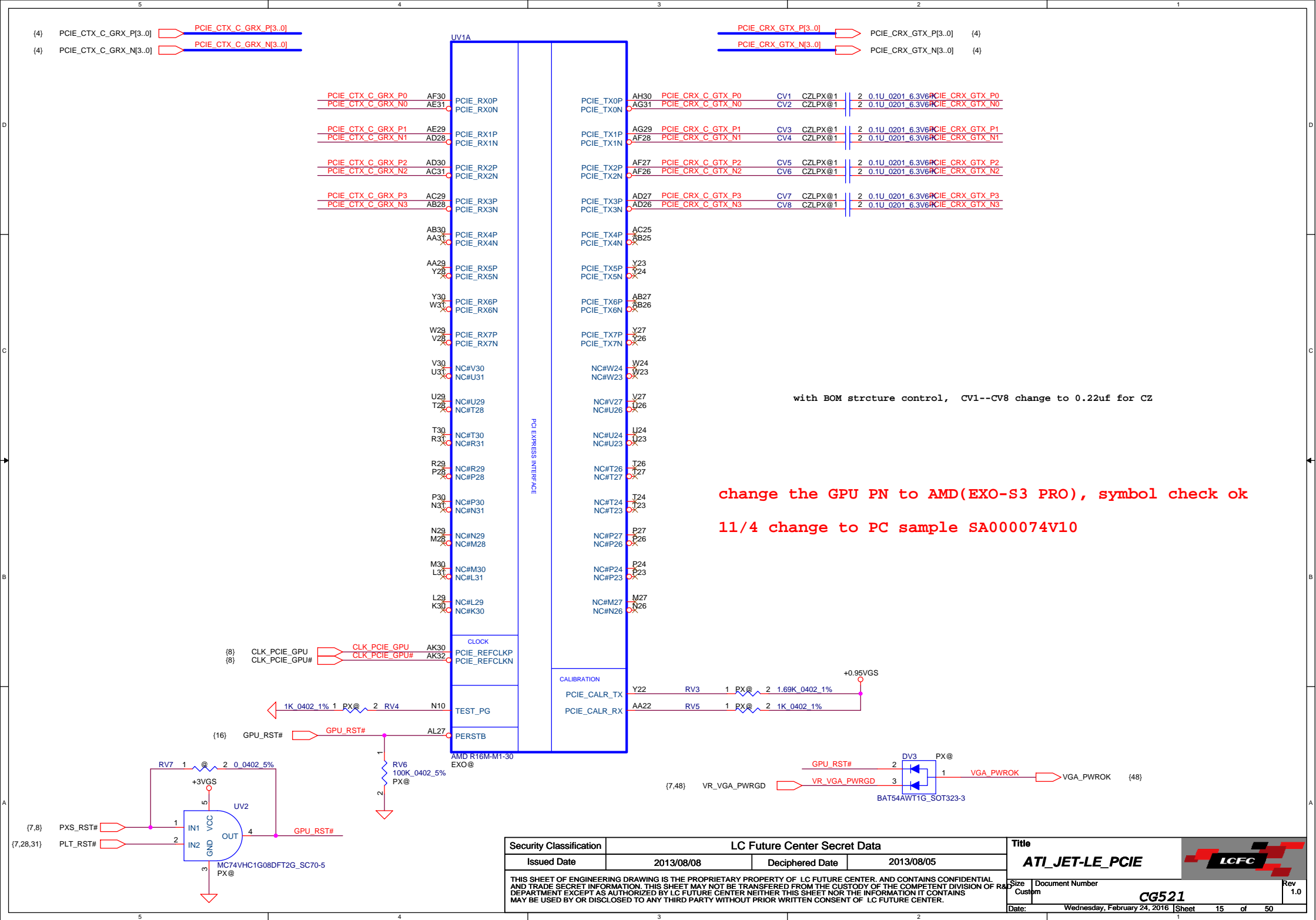
"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

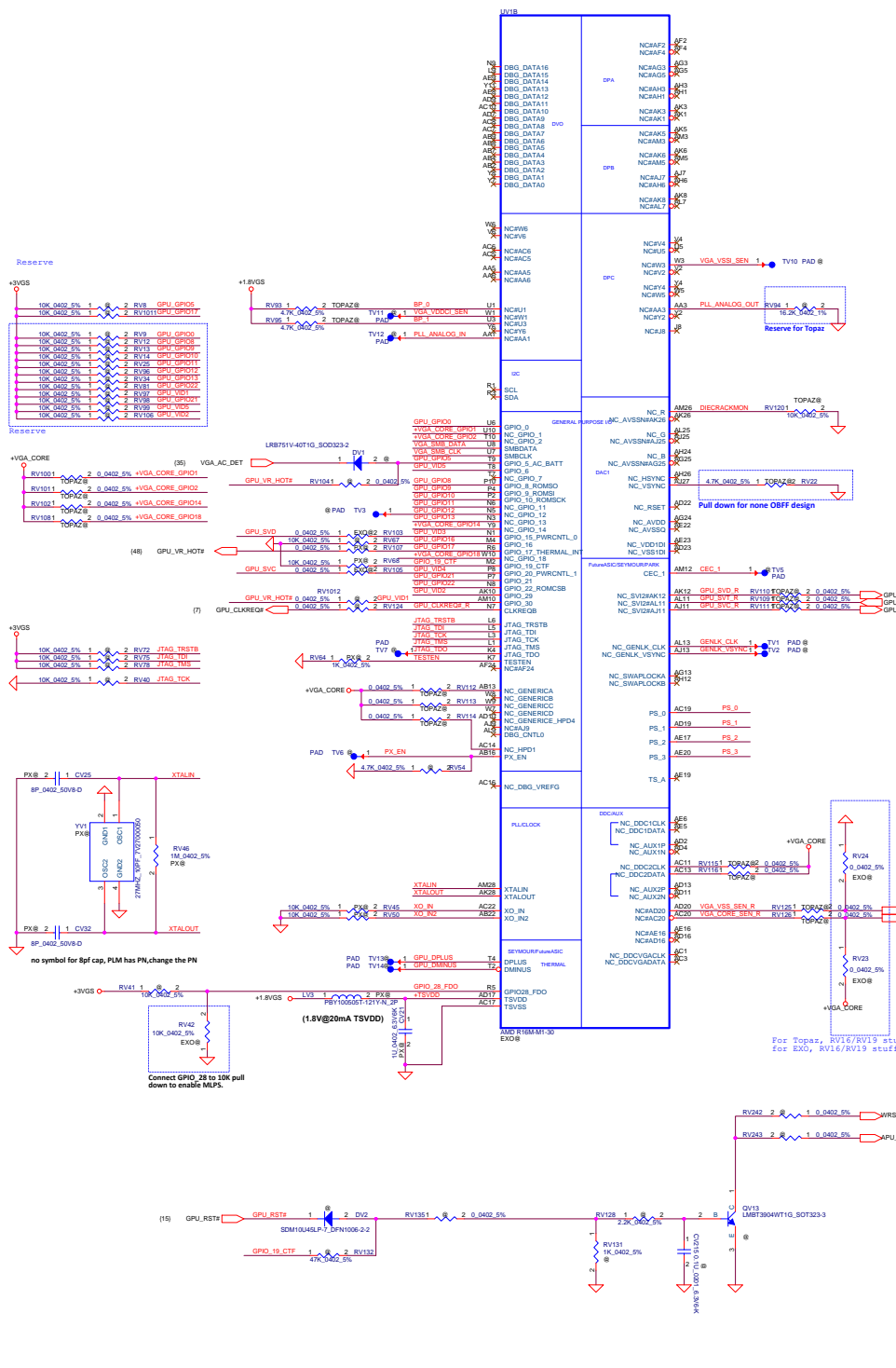
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
It is recommended that the 3.3-V rail ramp up first.
The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up.
The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μs).
For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K





CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[0]	ROM_CFG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	0 = Do not install resistor 1 = Install 10K resistor NA = Not applicable
PS_0[1]	ROM_CFG[1]	Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0	100 = 256MB
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONFL_PINTRAP[0]	The L58 (least significant bit) of the strap option that indicates the number of multi-ported display outputs	X
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is supported 1 = PCIe GEN3 is not supported	0 = Not support
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ# power management capability is disabled 1 = The CLKREQ# power management capability is enabled	0
PS_1[4]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter full-swing is enabled 1 = The transmitter full-swing is disabled	1
PS_1[5]	STRAP_TX_DEMPEM_EN	0 = Tx desemphasis disabled 1 = Tx desemphasis enabled	1 = Enable
PS_2[1]	N/A	Reserved	NA
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	STRAP_BIF_VGA_DES	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_3[1]	BOARD_CONFIG[0]	Board configuration related straps, such as for memory ID	X
PS_3[2]	BOARD_CONFIG[1]	Board configuration related straps, such as for memory ID	X
PS_3[3]	BOARD_CONFIG[2]	Board configuration related straps, such as for memory ID	NA
PS_3[4]	AUD_PORT_CONFL_PINTRAP[0]	The L58 (least significant bit) of the strap option that indicates the number of multi-ported display outputs	X

MLPS	Bit	BOM
PS_0[5:1]	1 1 0 1 0	R_pu() R_pd() CV15=NC
PS_1[5:1]	1 1 0 1 0	RV71=8.45K RV77=2K CV16=NC
PS_2[5:1]	1 1 0 1 0	RV74=NC RV76=4.75K CV18=NC
PS_3[5:1]	1 1 1 X X	RV63=X76 RV69=X76 CV19=X76

with BOM structure control, RV63, RV70 change to different value to adjust VRAN config

with BOM structure control, when config PB03 RV74 change to 8.45K, RV60 change to 2K

Capacitor Value (nF)	Bits [5:4]
560	00
560	01
560	10
560	11

Note: 0402 1% resistors are required

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Rev 01

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UV1F

NC_VARY_BL
NC_DIGON

AB11 RV117 1 2 0 0402 5% TOPAZ@
AB12 RV119 1 2 0 0402 5% TOPAZ@

+VGA_CORE

NC_UPHYAB_TMDPA_TX0N
NC_UPHYAB_TMDPA_TX0P

AL15
AK14

NC_UPHYAB_TMDPA_TX1N
NC_UPHYAB_TMDPA_TX1P

AH16
AJ15

NC_UPHYAB_TMDPA_TX2N
NC_UPHYAB_TMDPA_TX2P

AL17
AK16

NC_UPHYAB_TMDPA_TX3N
NC_UPHYAB_TMDPA_TX3P

AH18
AJ17

NC_TXOUT_L3P
NC_TXOUT_L3N

AL19
AK18

TMDP

NC_UPHYAB_TMDPB_TX0N
NC_UPHYAB_TMDPB_TX0P

AH20
AJ19

NC_UPHYAB_TMDPB_TX1N
NC_UPHYAB_TMDPB_TX1P

AL21
AK20

NC_UPHYAB_TMDPB_TX2N
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AH22
AJ21


NC_UPHYAB_TMDPB_TX3N
NC_UPHYAB_TMDPB_TX3P

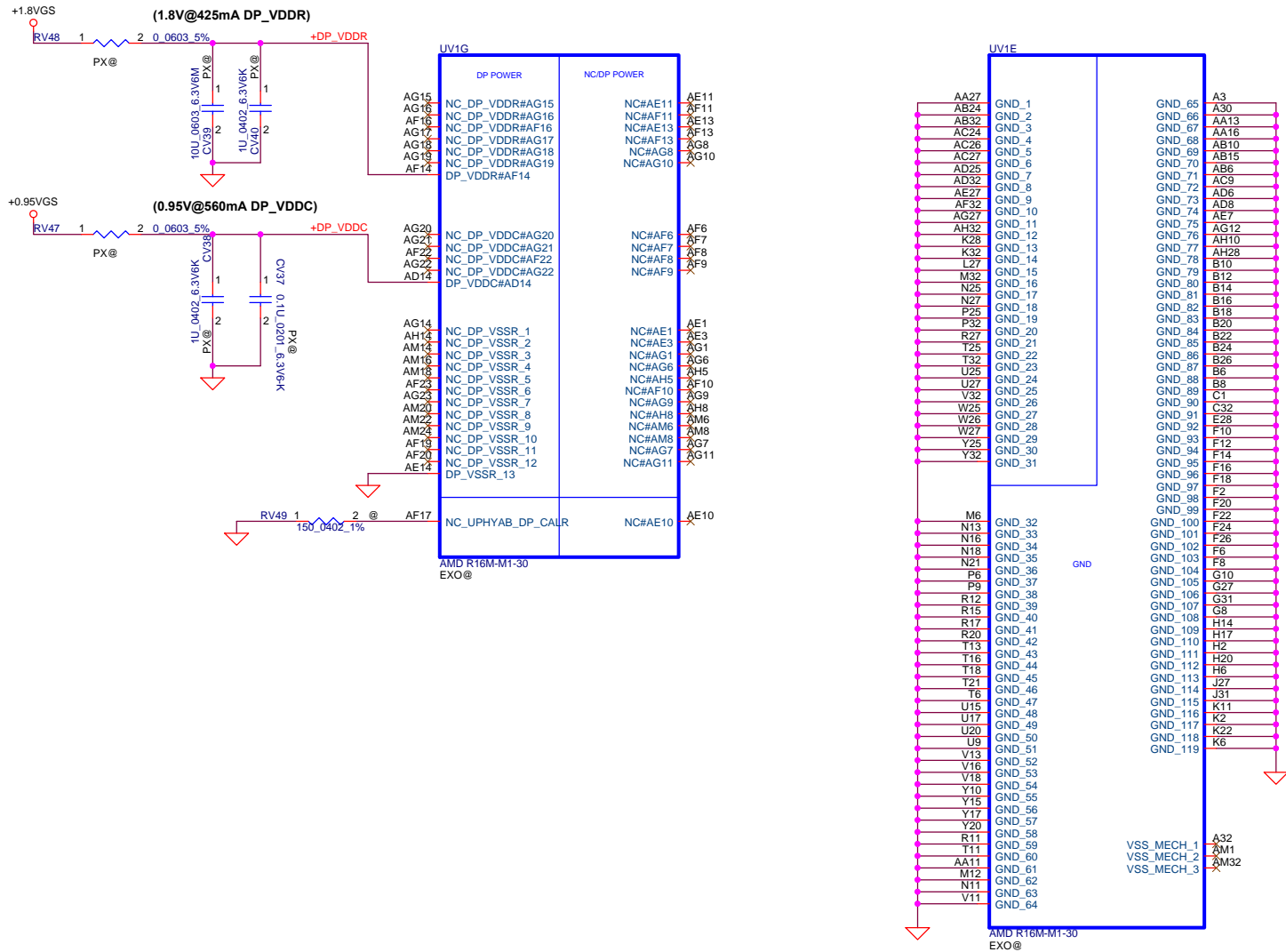
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AK22


NC_TXOUT_U3P
NC_TXOUT_U3N

AH24
AJ23

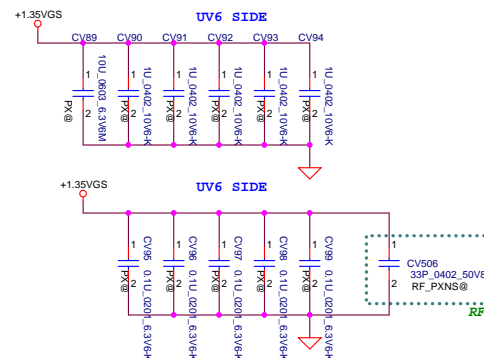
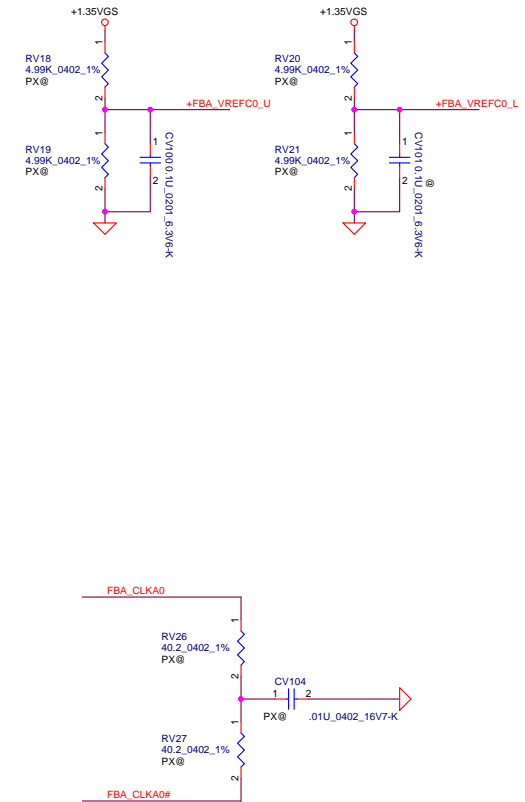
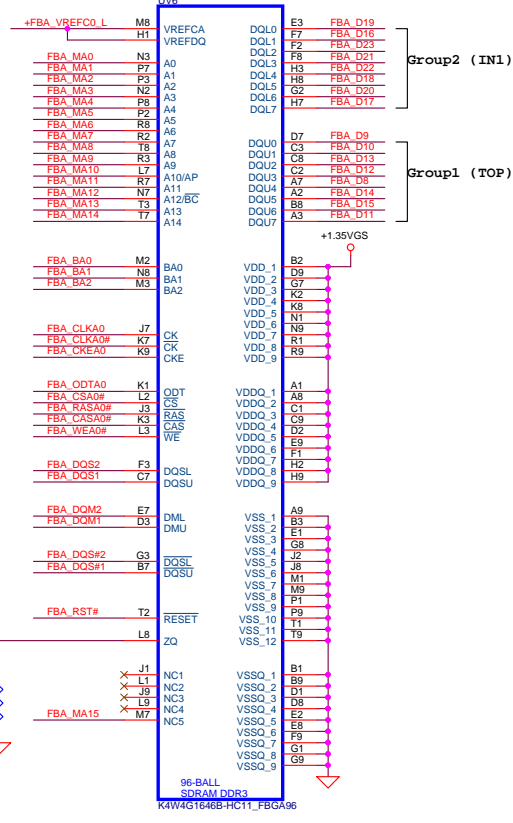
AMD R16M-M1-30
EXO@

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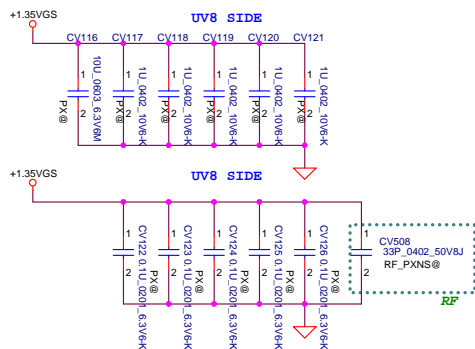
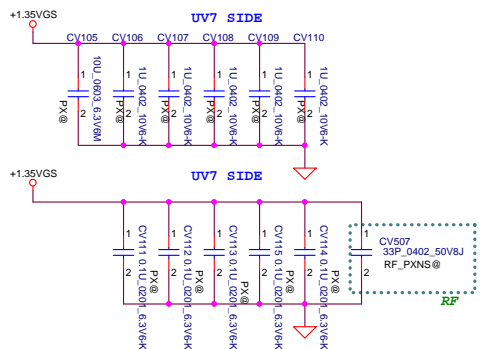
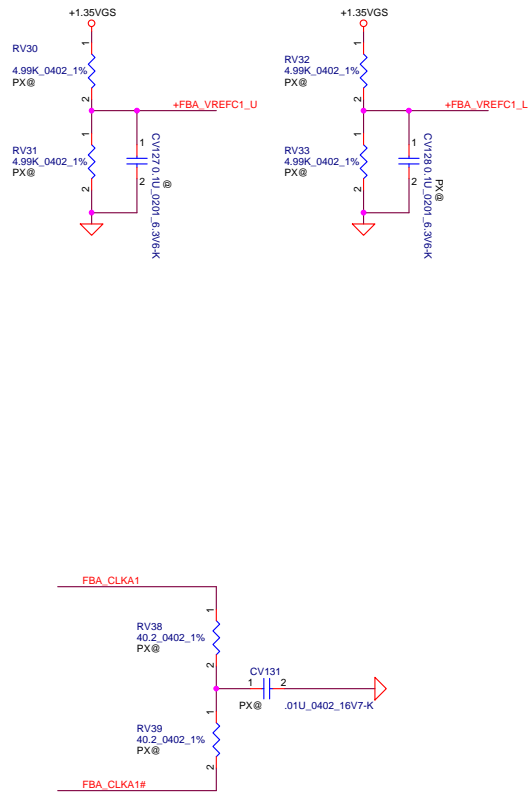
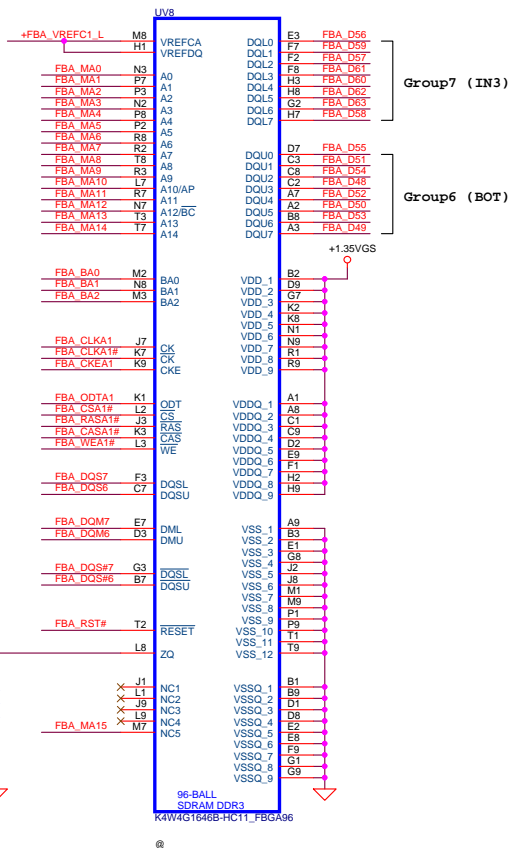
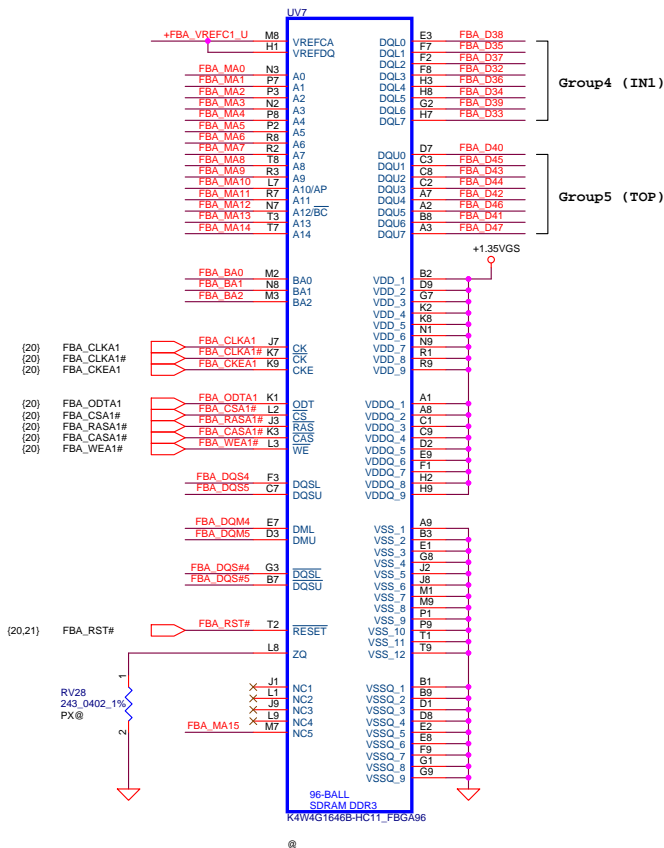



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	FBA_BA[2..0]	{20,22}
	FBA_DQS[3..0]	{20}
	FBA_DQM[3..0]	{20}
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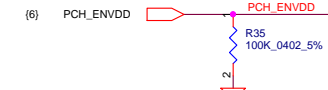
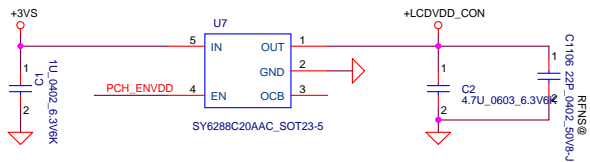


Memory Partition A - Upper 32 bits

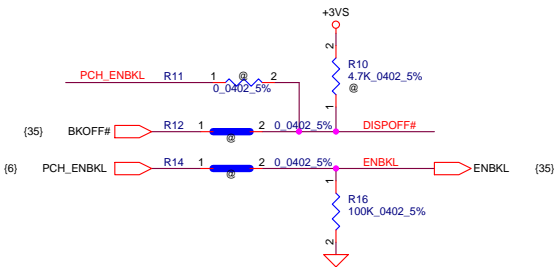


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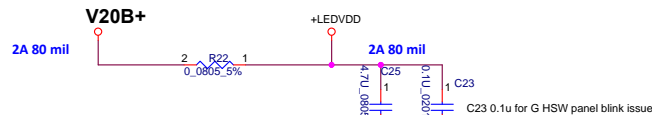
LCD POWER CIRCUIT



CZL enable is 3.3V, CZ is 1.8V, AP228002AW is 3.3V

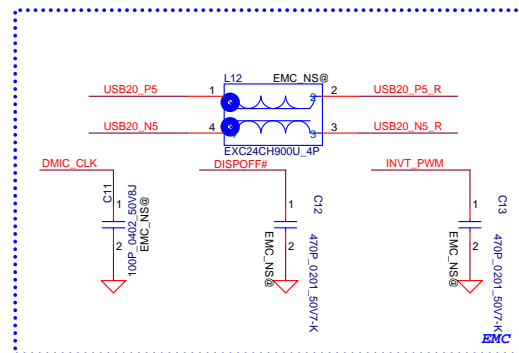
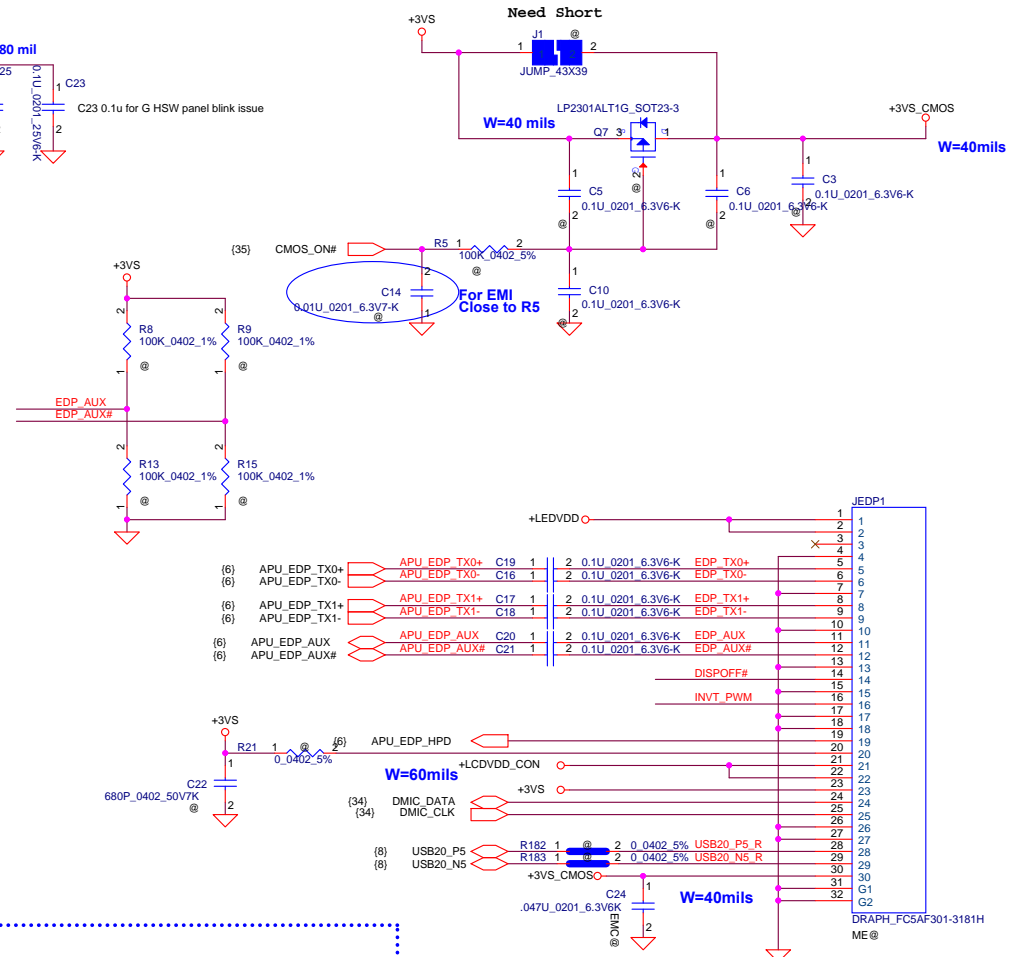


B+ to +LEDVDD POWER

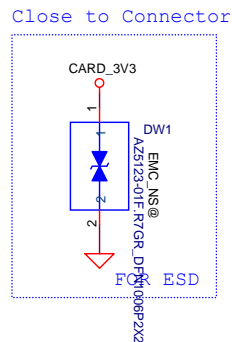
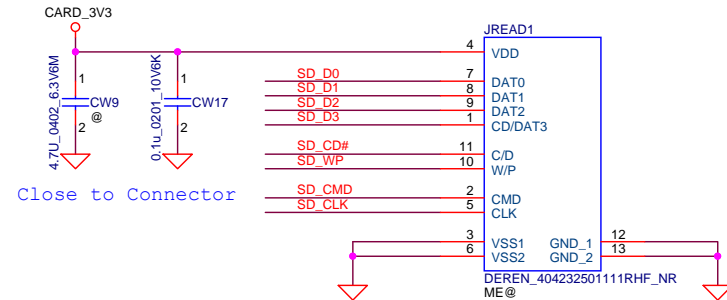
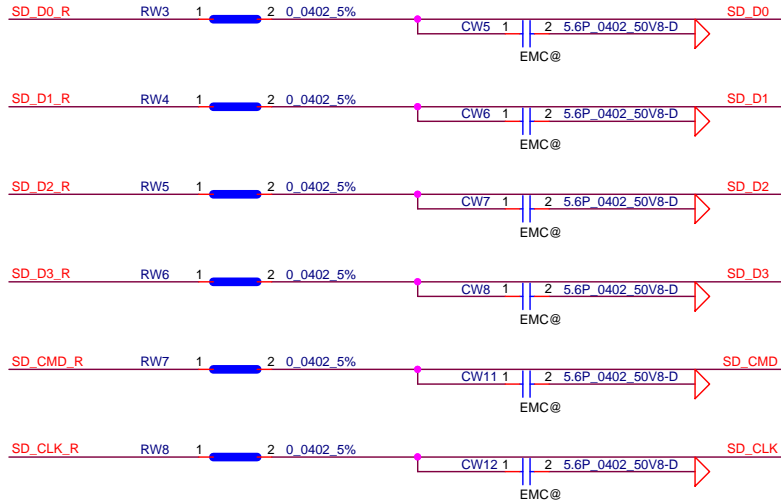
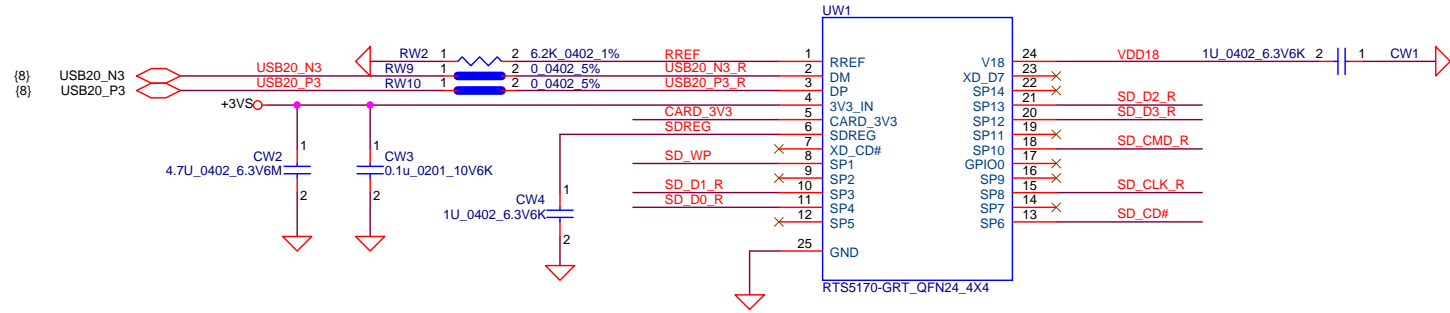
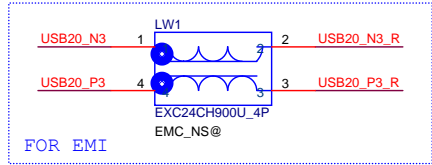



can cost down R20 for CZ

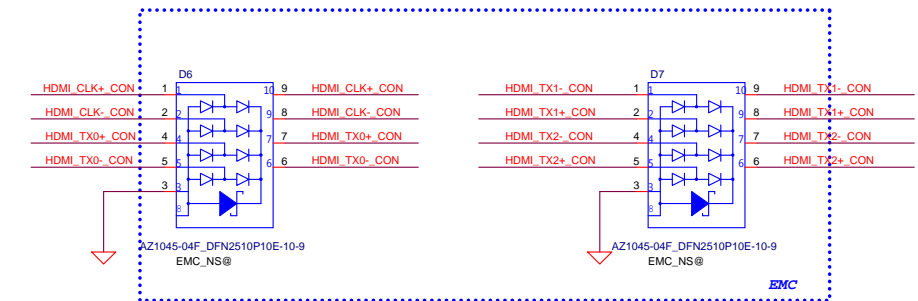
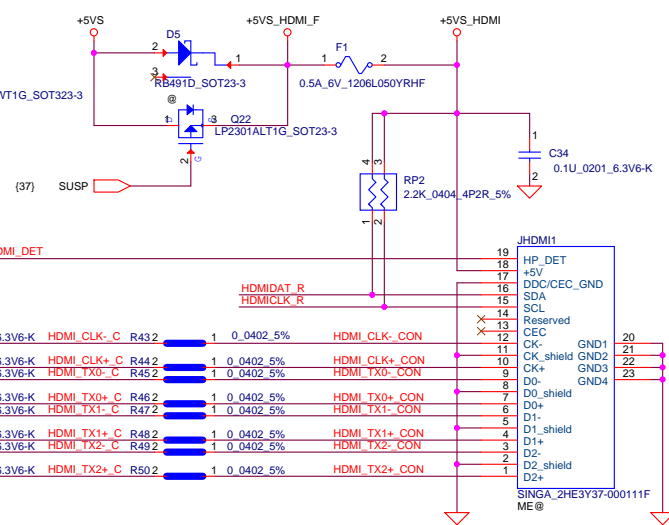
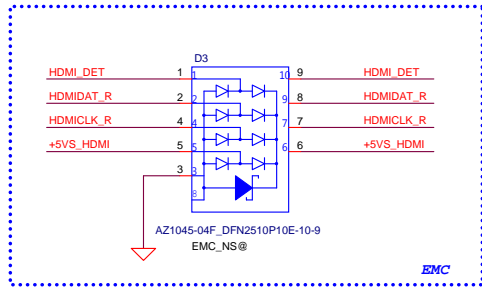
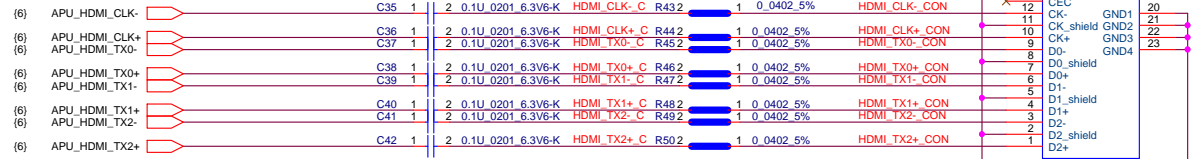
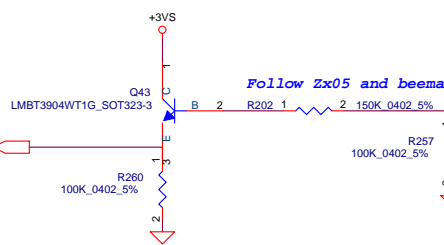
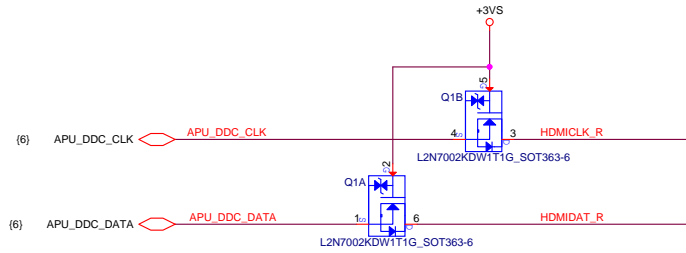
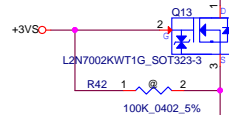
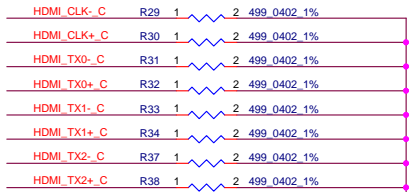
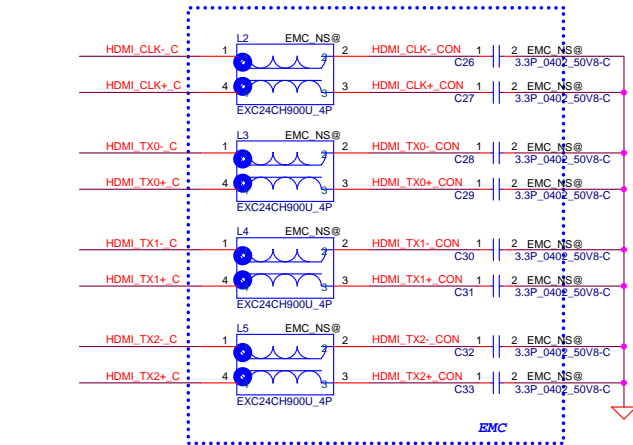
CMOS Camera

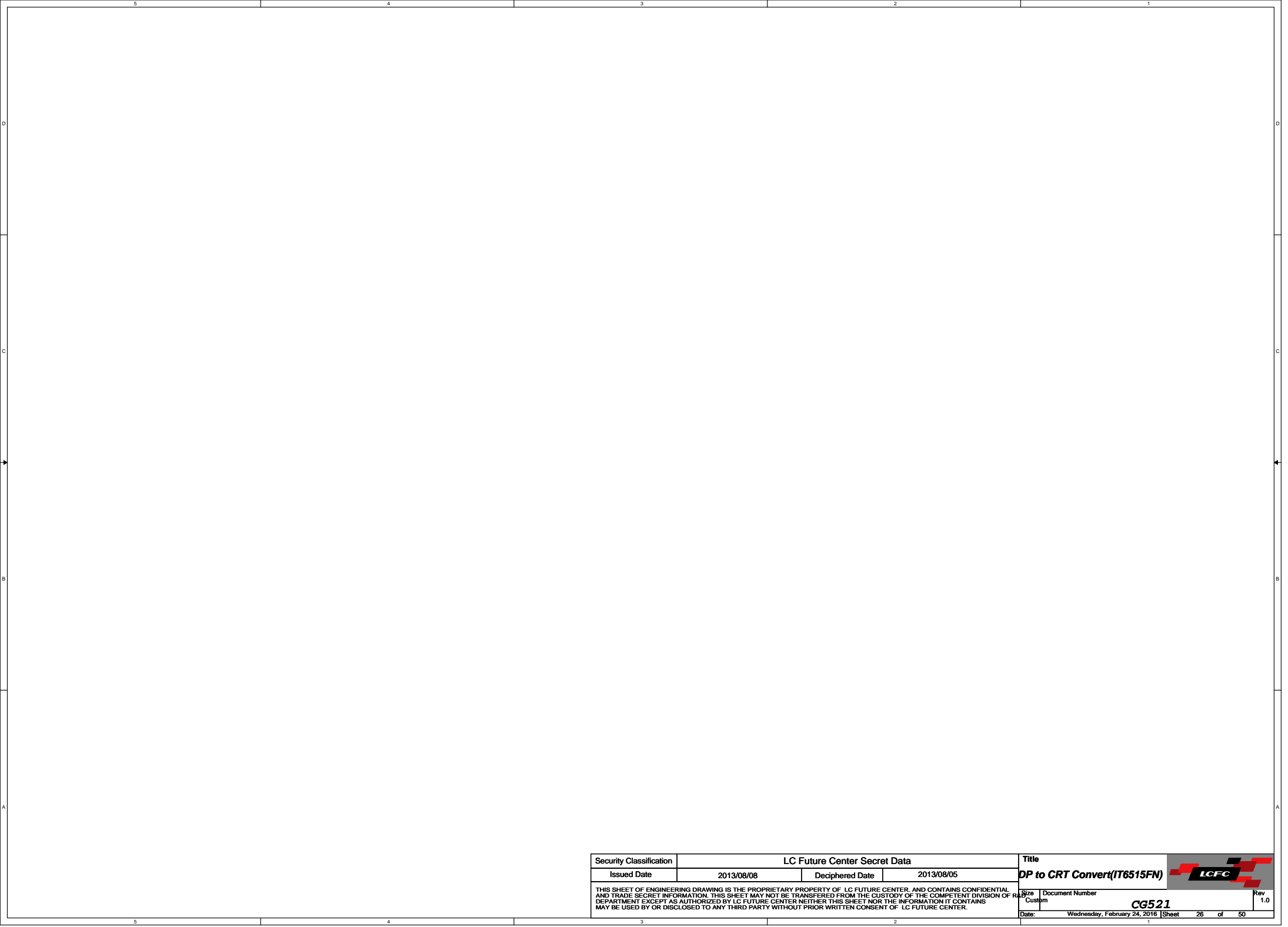


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		CG521		1.0	
Date:		Wednesday, February 24, 2016		Sheet	
		23		of	
		50			



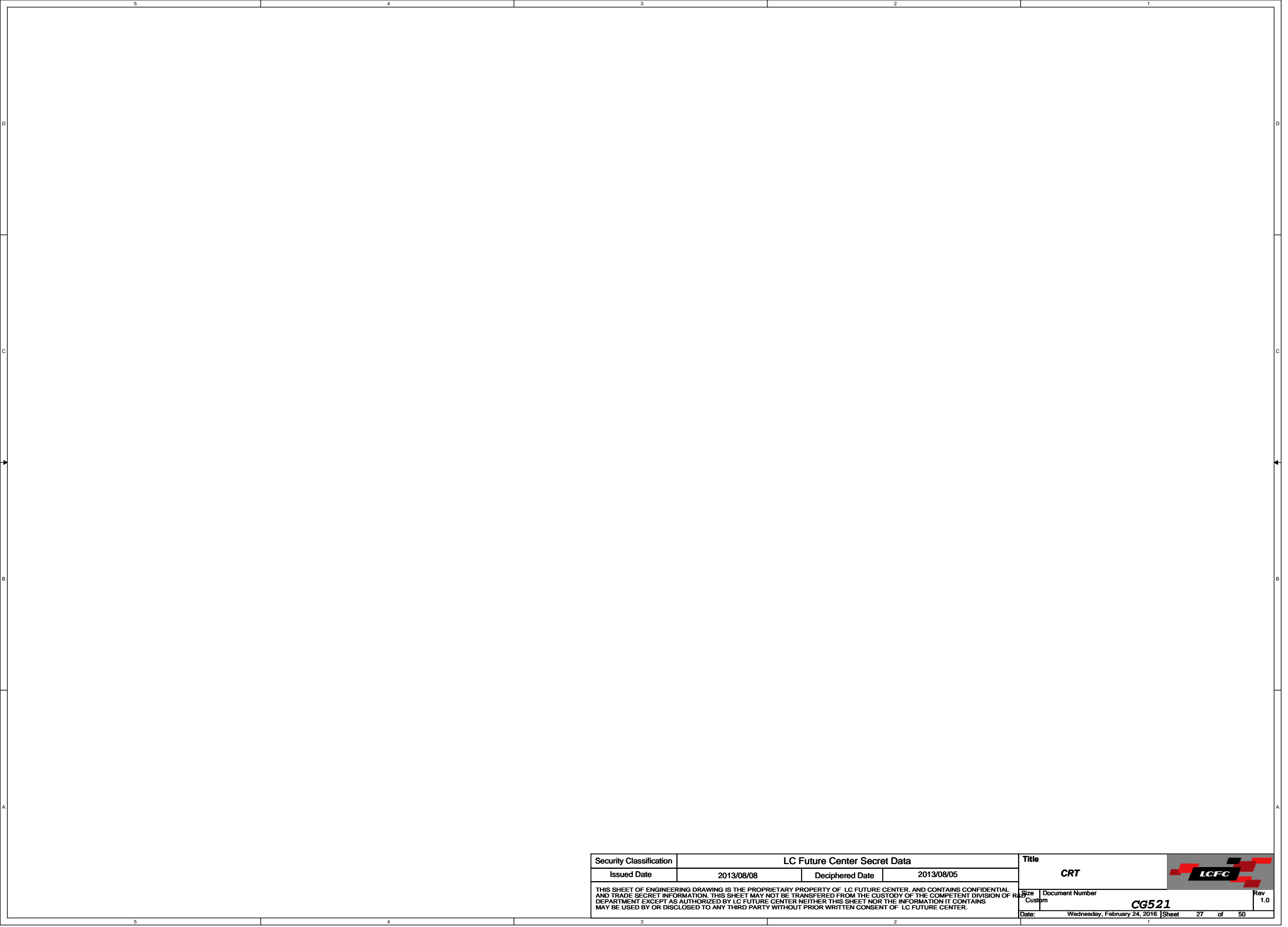
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2013/08/08	Deciphered Date	2013/08/05	CardReader			
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	DP to CRT Convert(IT6515FN)	
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				Date: Wednesday, February 24, 2016	Rev 1.0
				Sheet 26	of 50





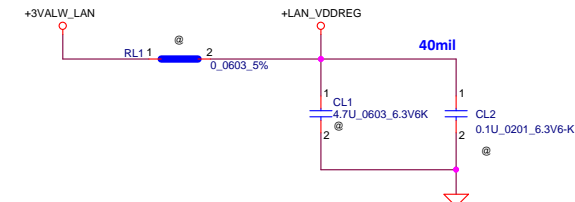
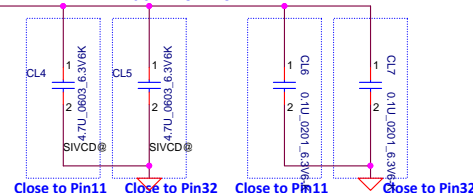
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2013/08/08	Deciphered Date	2013/08/05	CRT			
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				Custpm	CG521	1.0	
Date:				Wednesday, February 24, 2016			
				Sheet 27 of 50			

+3VALW TO +3VALW_LAN

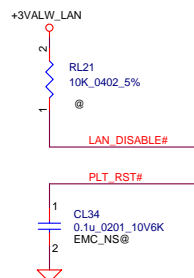
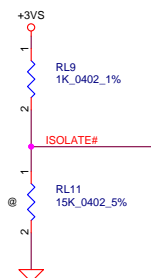
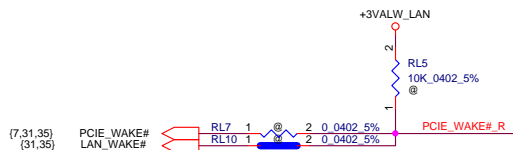
+3VALW_LAN rising time (10%~90%):
0.5ms<spec<100ms

Need short

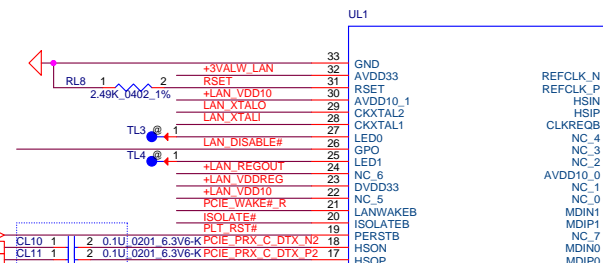
width : 40 mils



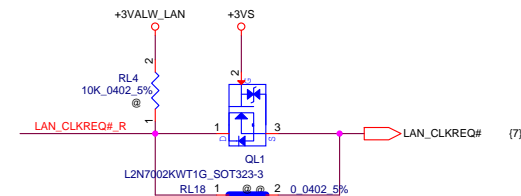
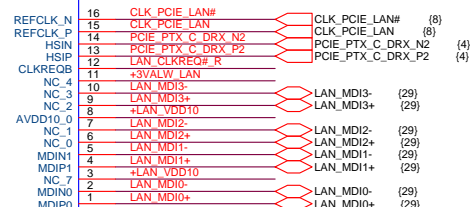
change the Lan Chip PN to RTL8107ECG



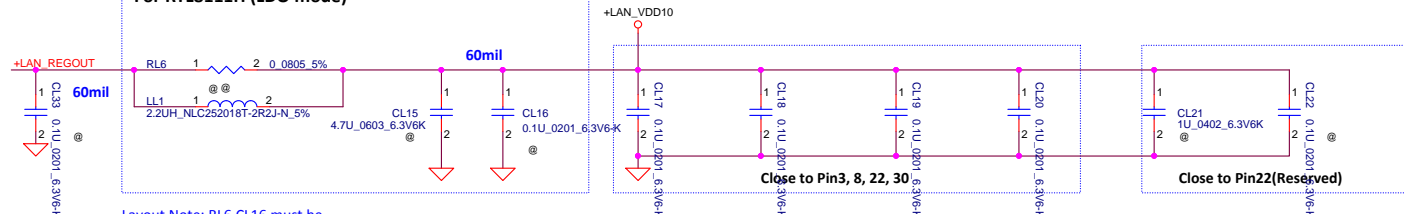
(7,15,31) PLT_RST#
(4) PCIE_PRX_DTX_N2
(4) PCIE_PRX_DTX_P2



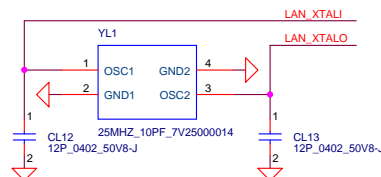
CL10 close to Pin18
CL11 close to Pin17



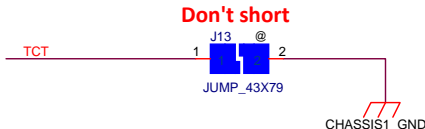
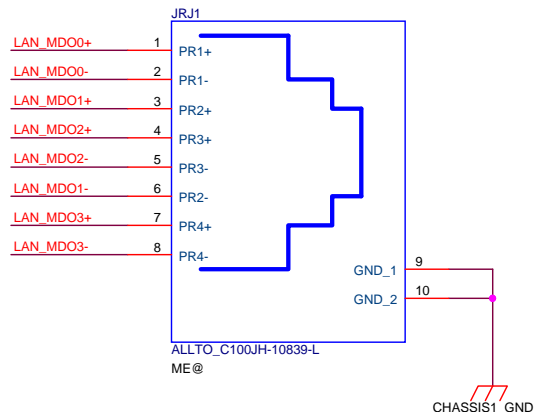
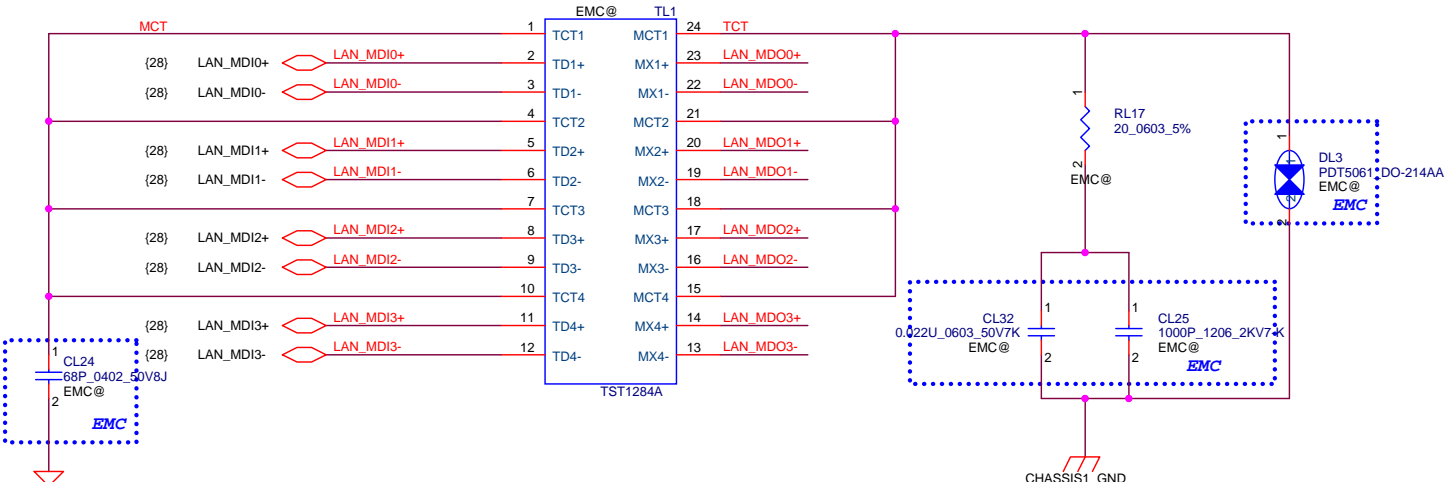
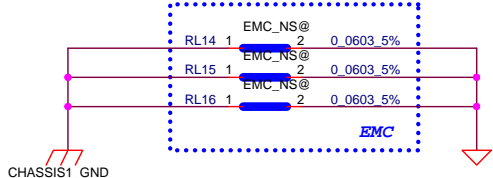
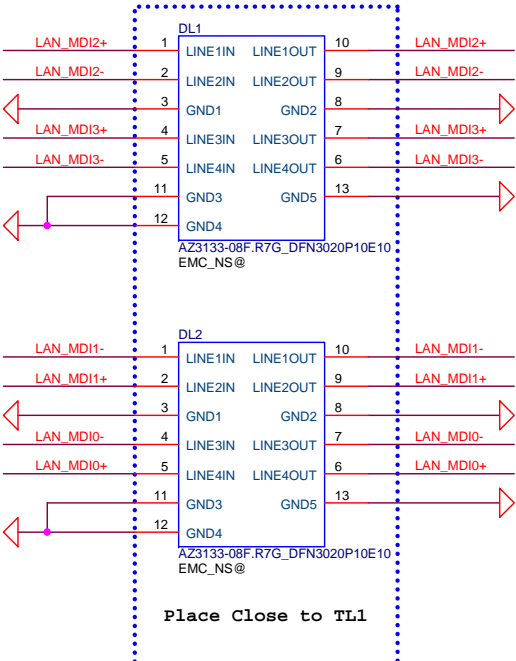
For RTL8111H (LDO mode)




Layout Note: RL6, CL16 must be
within 200mil to Pin36,
+LAN_REGOUT: Width = 60mil



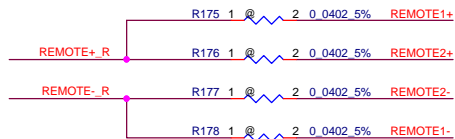
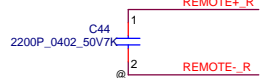
DL1/DL2
1'S PN:SC300003M00



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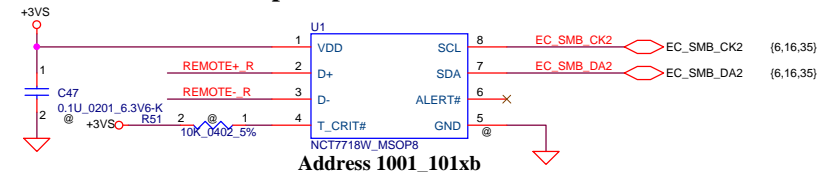
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Close to U1

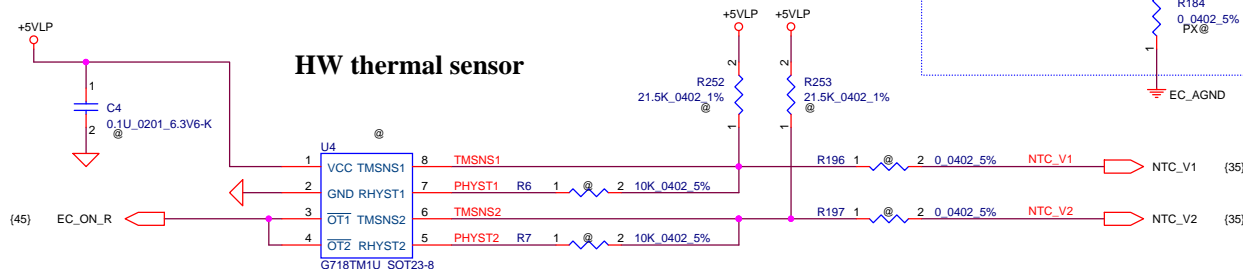


REMOTE+/_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

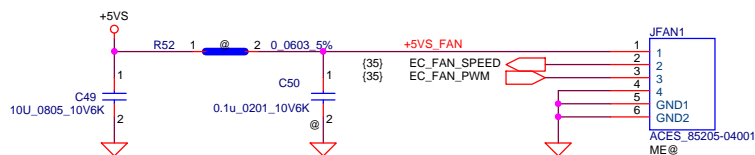
SMSC thermal sensor placed near DIMM



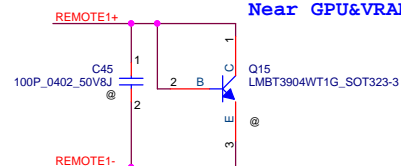
HW thermal sensor



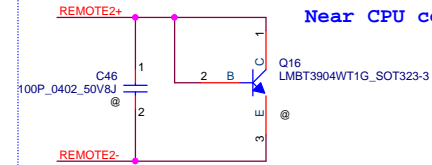
over temperature threshold:
 $RSET = 3 * RTMH$
 $92 \pm 30C$
Hysteresis temperature threshold.
 $RHYST = (RSET * RTML) / (3 * RTML - RSET)$
 $56 \pm 30C$



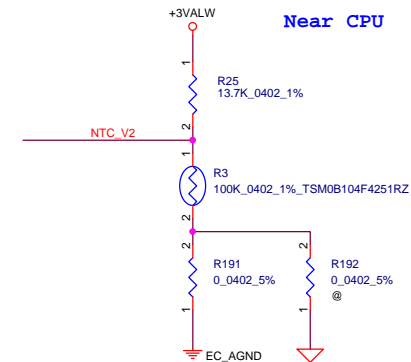
Near GPU&VRAM



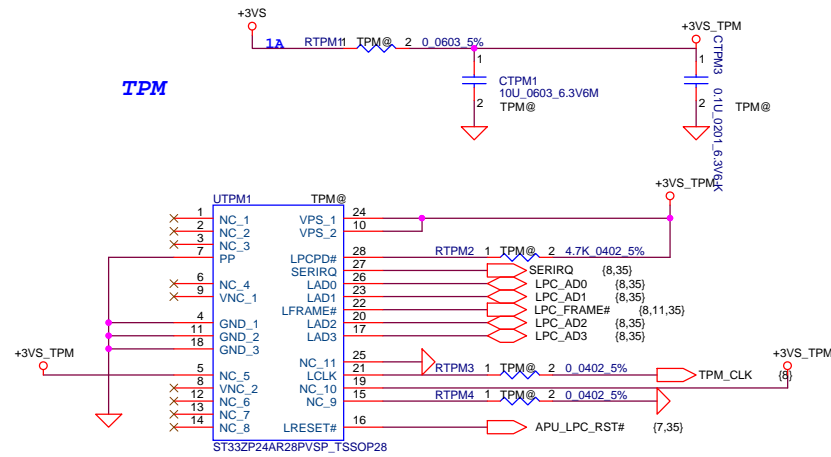
Near CPU core



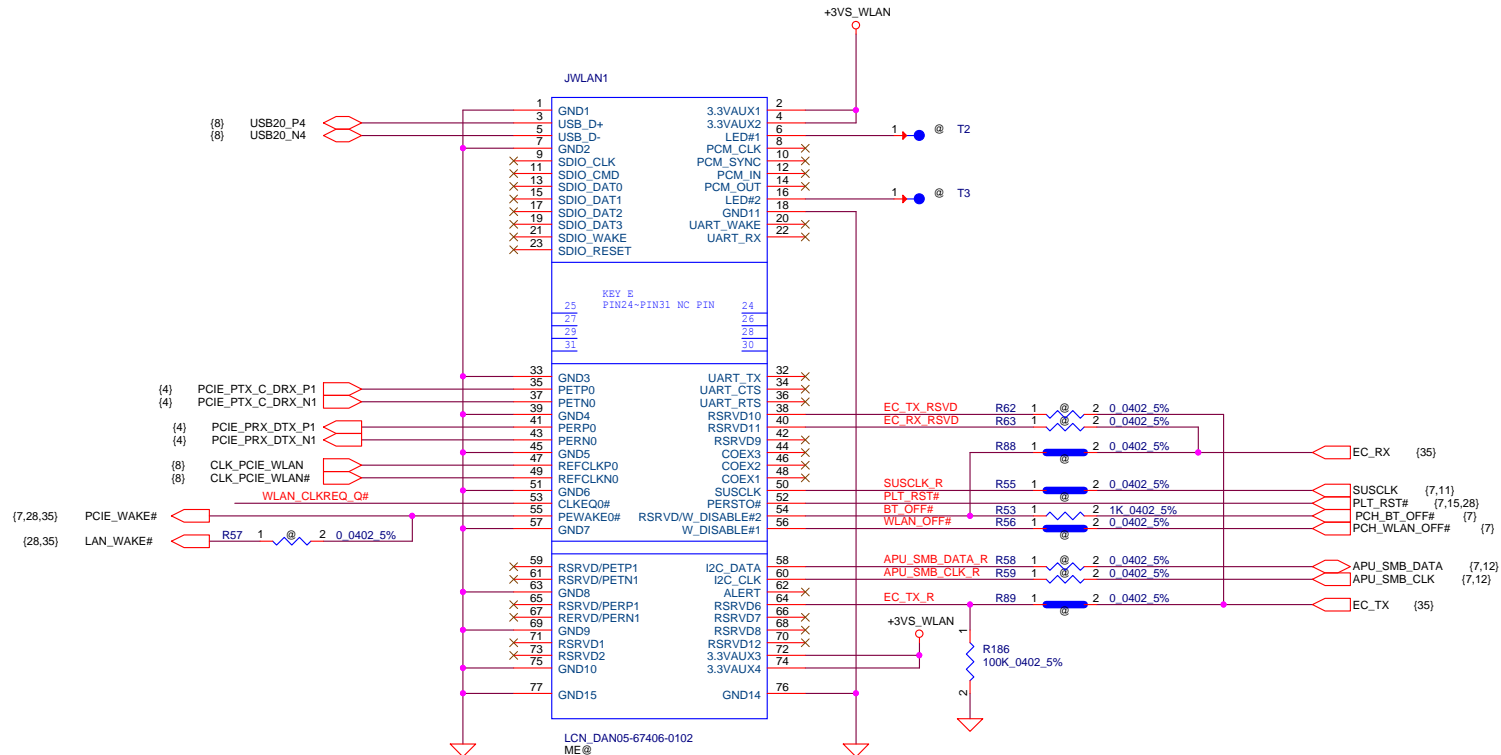
Near CPU



TPM



Mini-Express Card(WLAN/WiMAX)

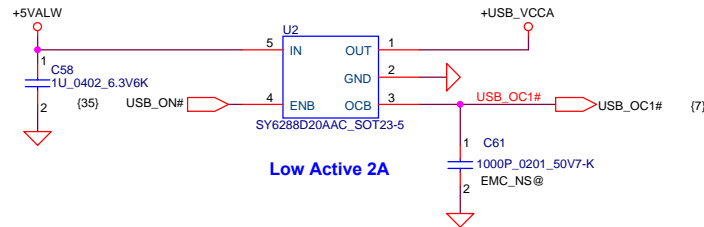


Not support AOAC, delete AOAC power circuit

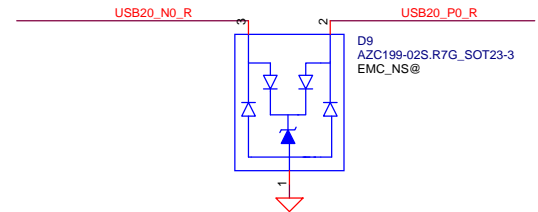
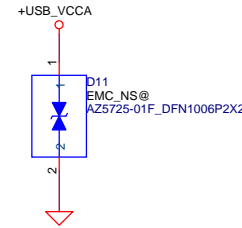


If support AOAC, NC R61;
if not support AOAC, stuff R61.

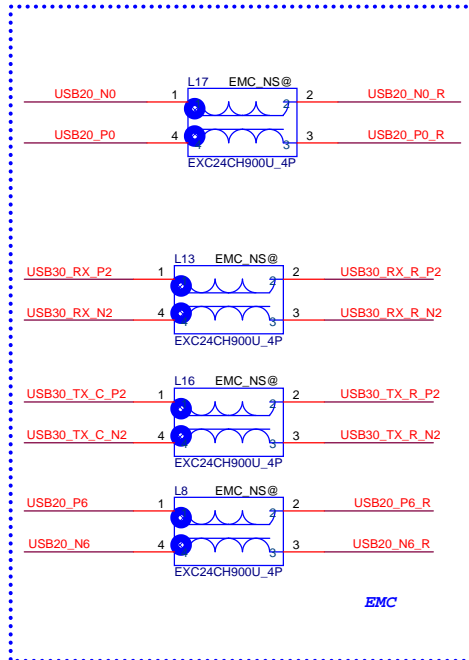
LEFT SIDE USB PORT X2



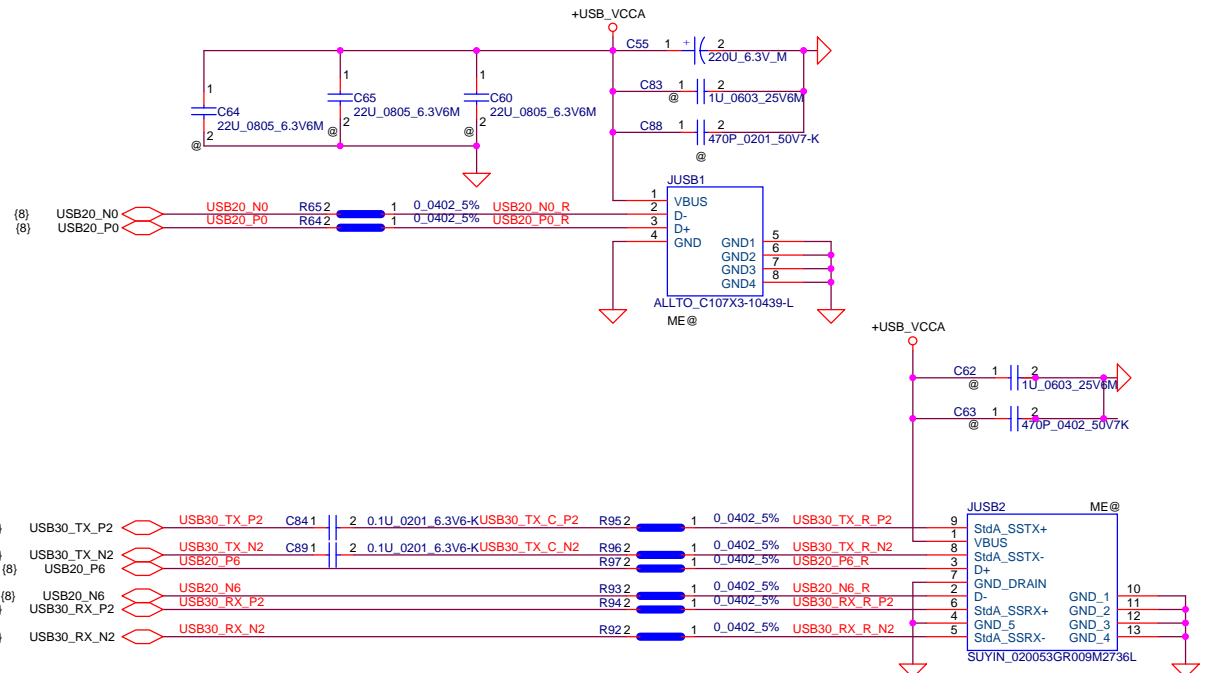
Low Active 2A



EMC solution need double check 1015

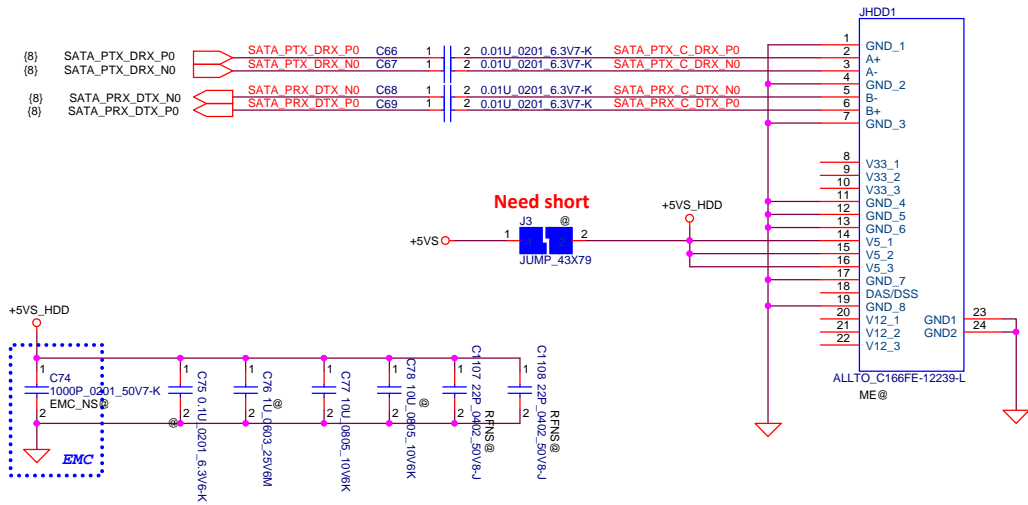


EMC



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2013/08/08				2013/08/05				P32-USB3.0 PORT (LEFT)			
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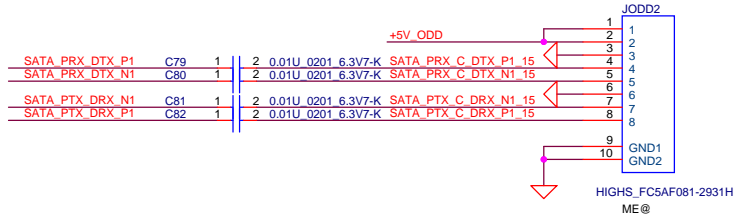
SATA HDD Conn.



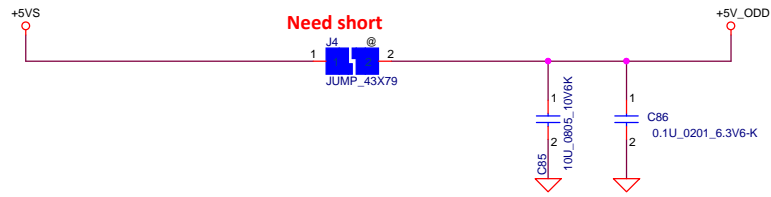
FOR 14" SATA ODD Conn.



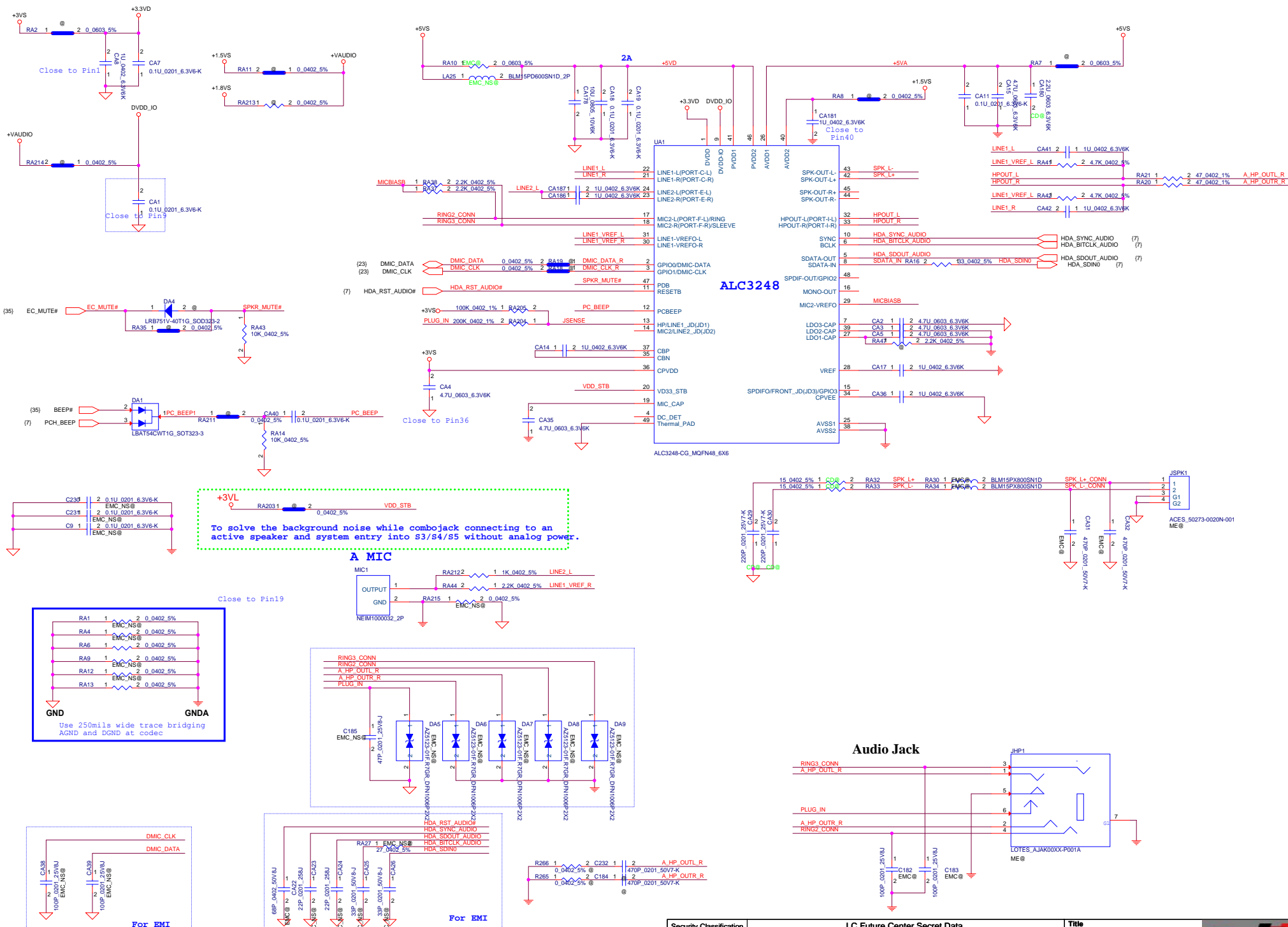
FOR 15" SATA ODD FFC Conn

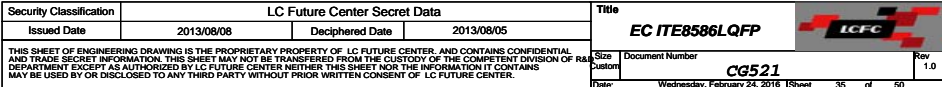


+5VS to +5V_ODD

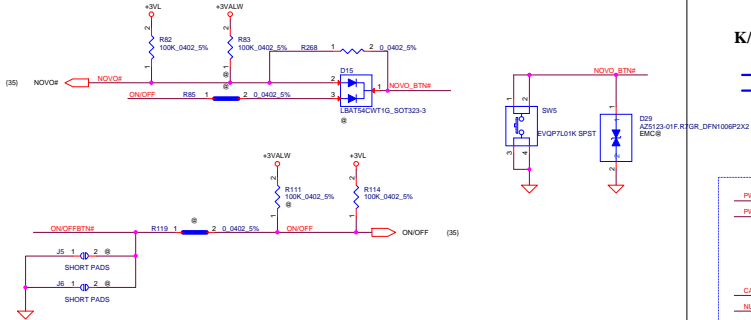


Delete Zero ODD circuit 10/19

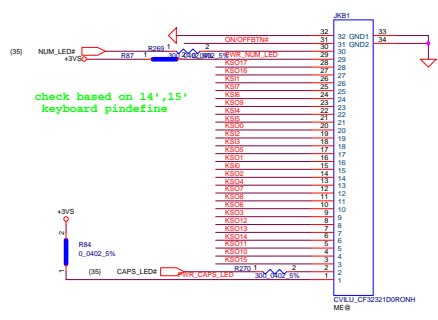
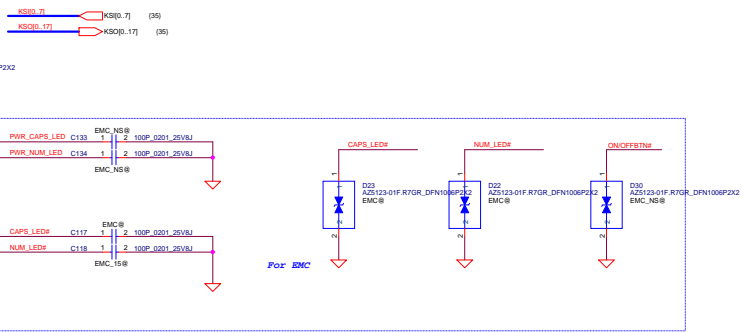




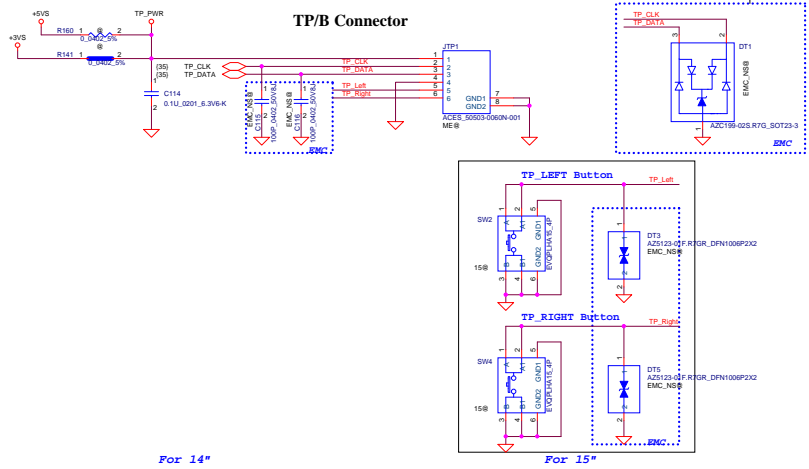
ON/OFF switch



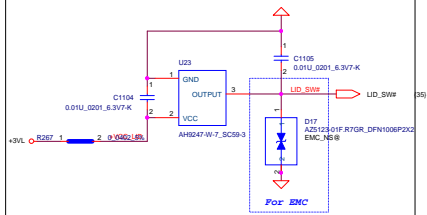
K/B Connector



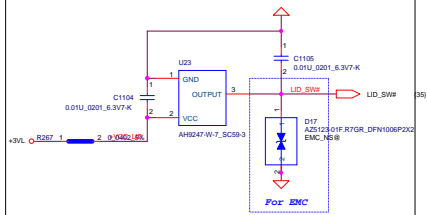
TP/B Connector



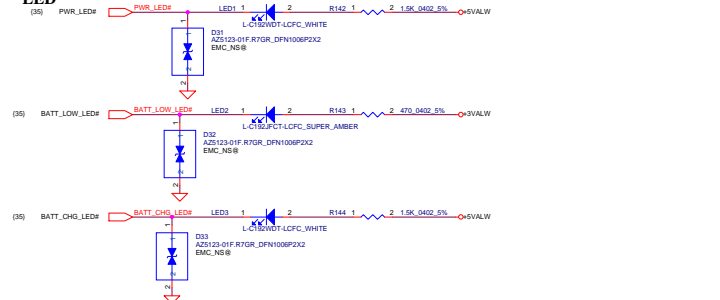
PWR/B Connector

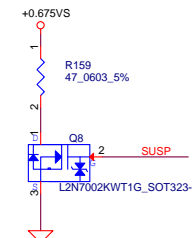
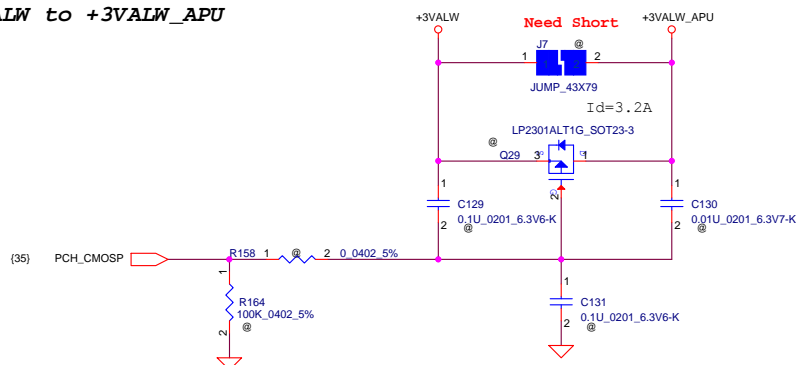
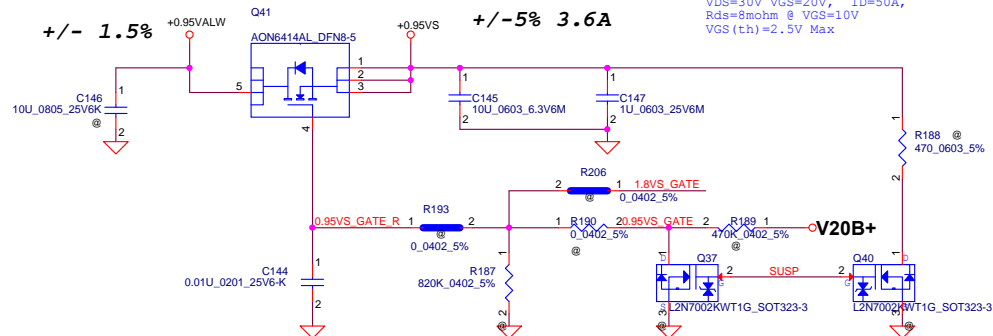
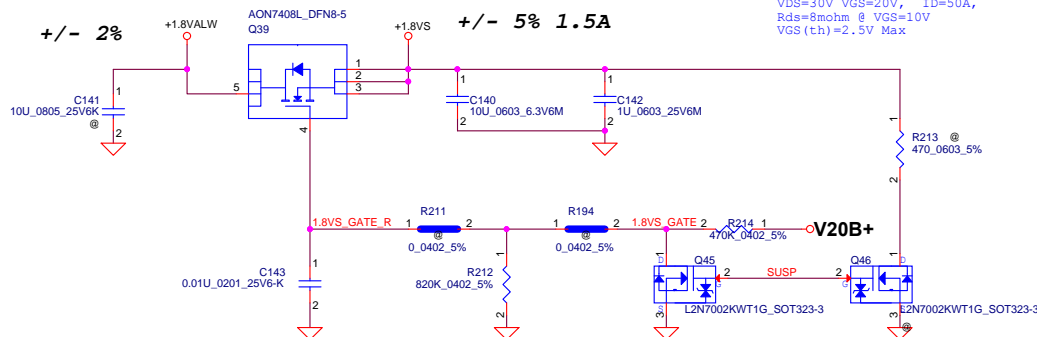
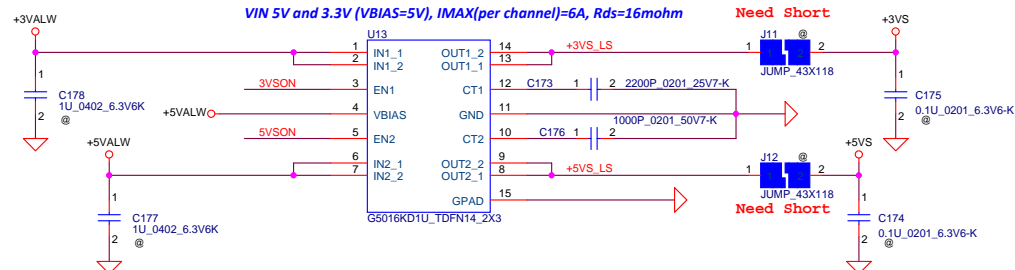
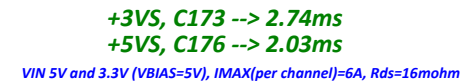
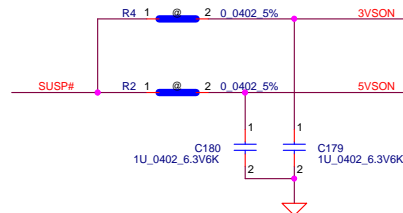



USB I/O Connector

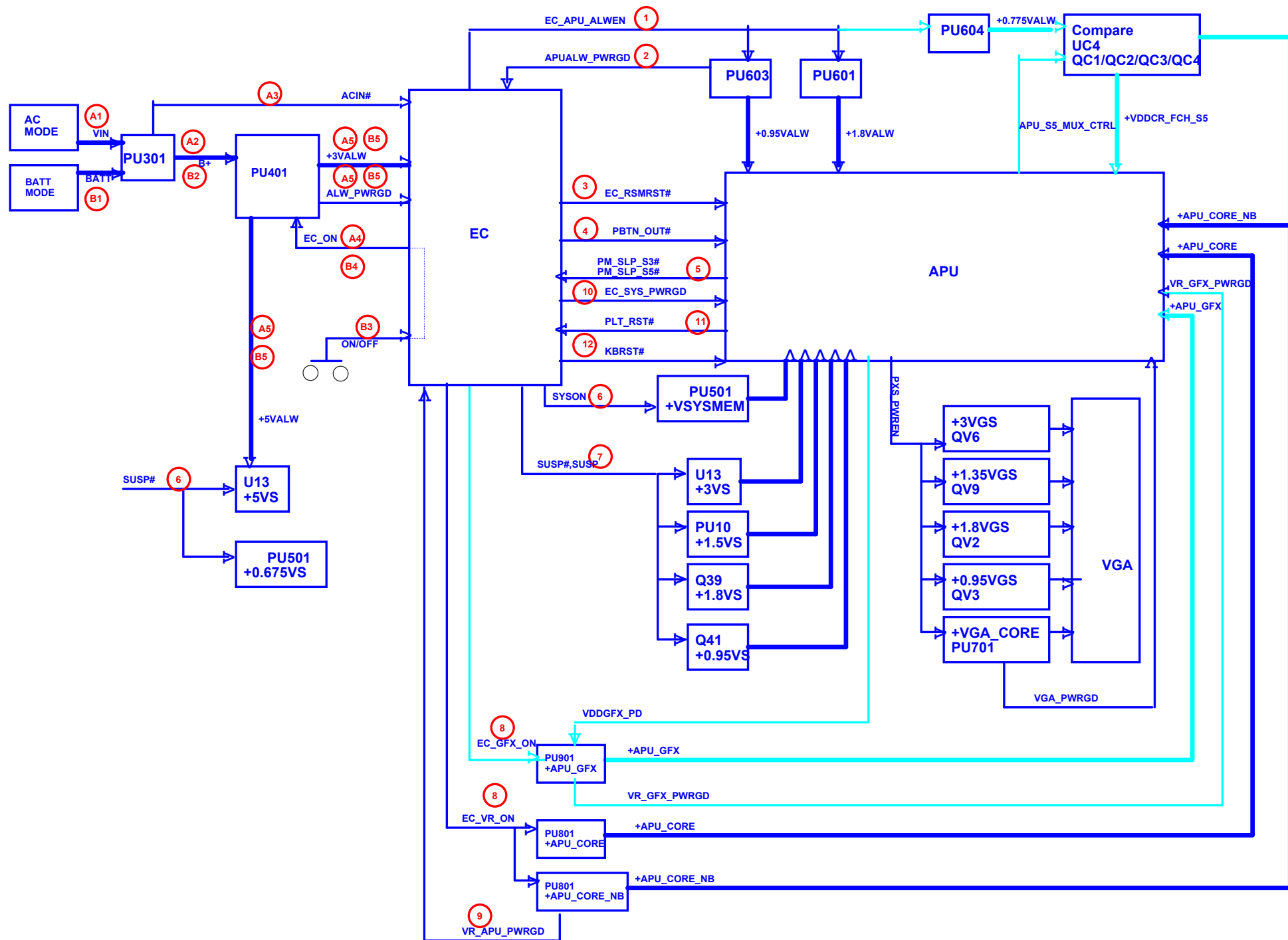


LED



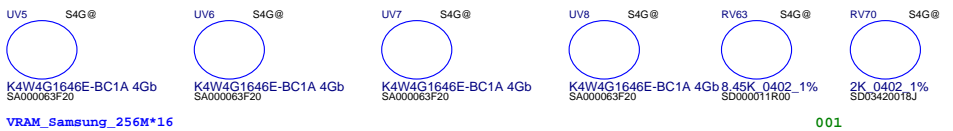
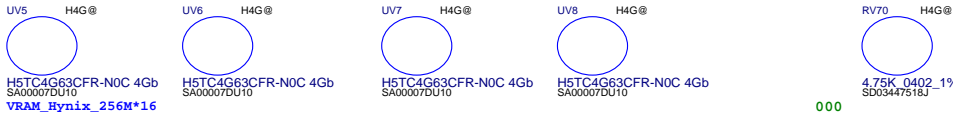
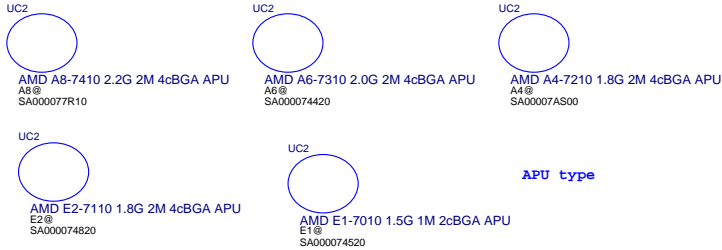


Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	DC V TO VS INTERFACE	
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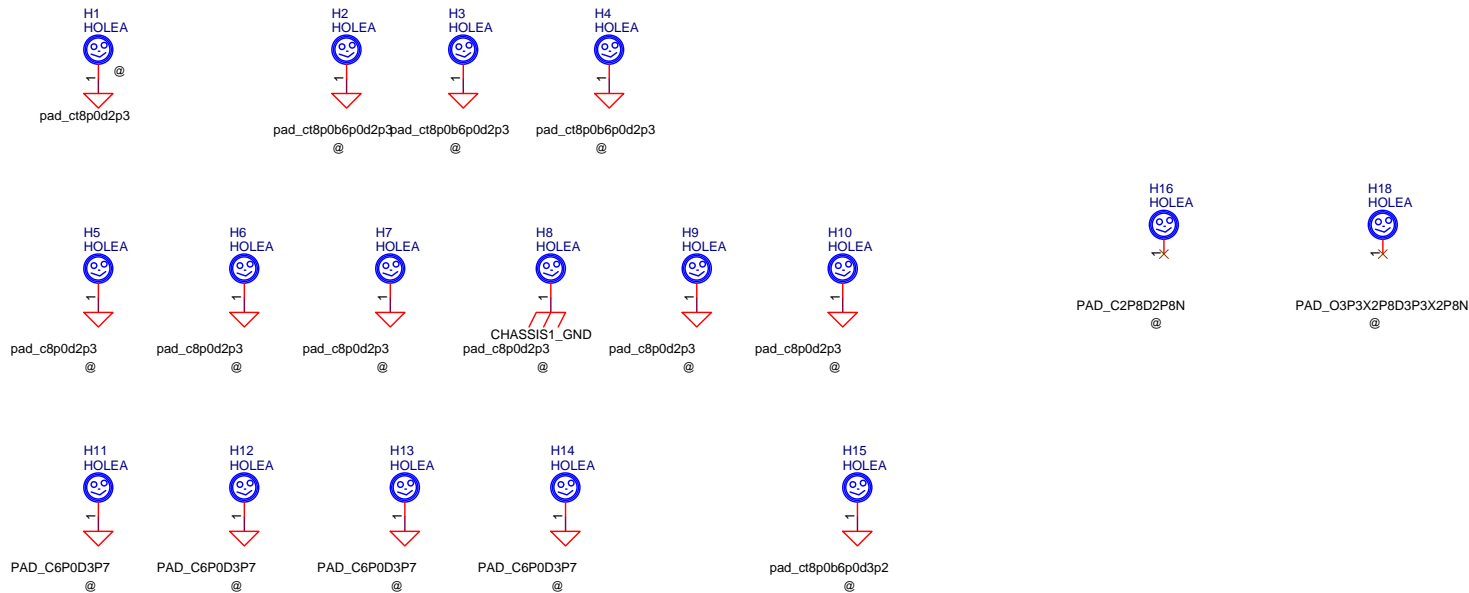
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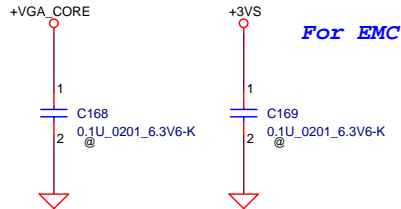
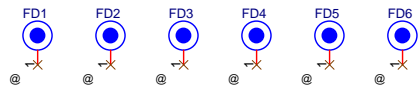



VRAM ID config

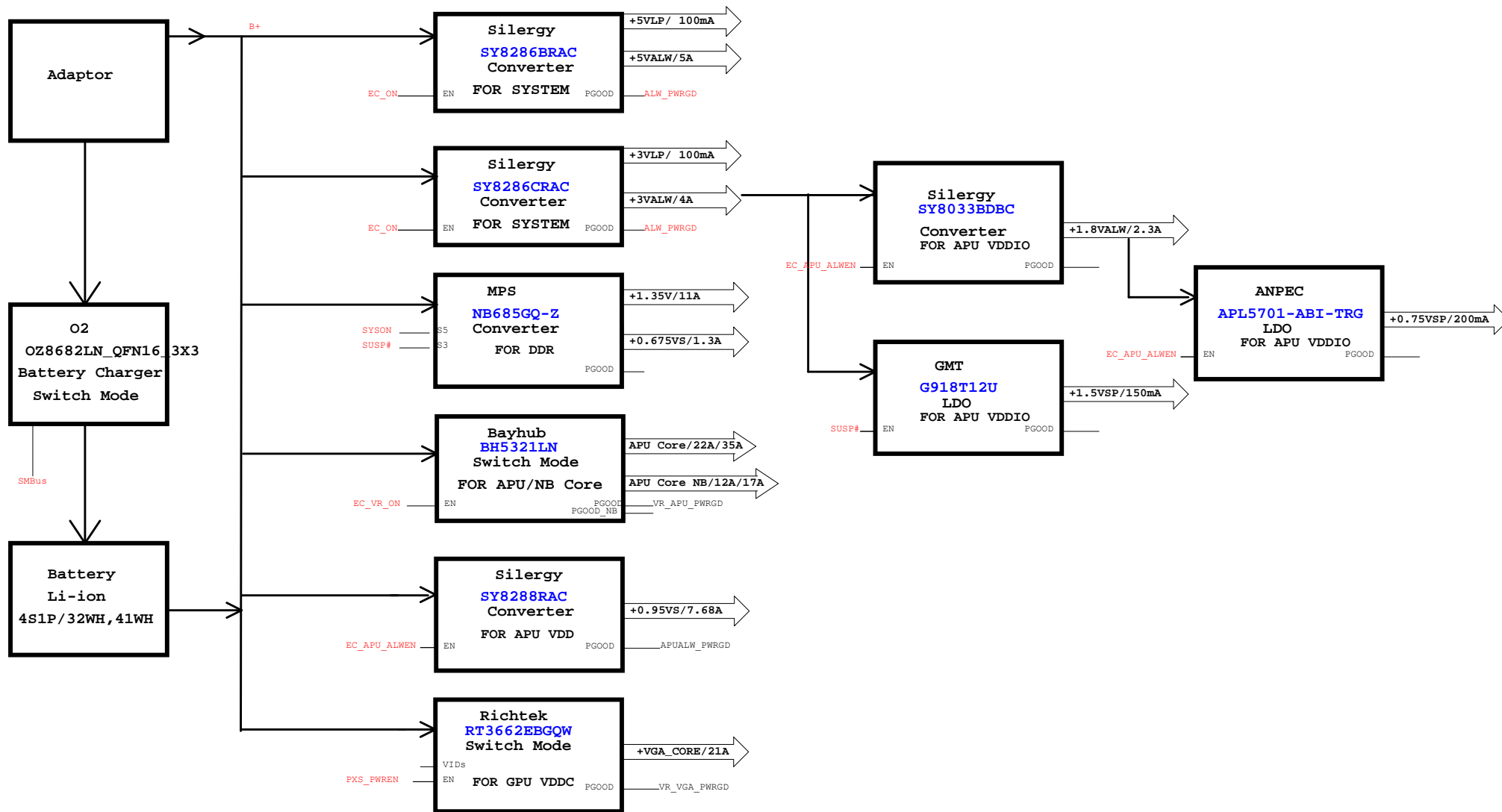
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128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

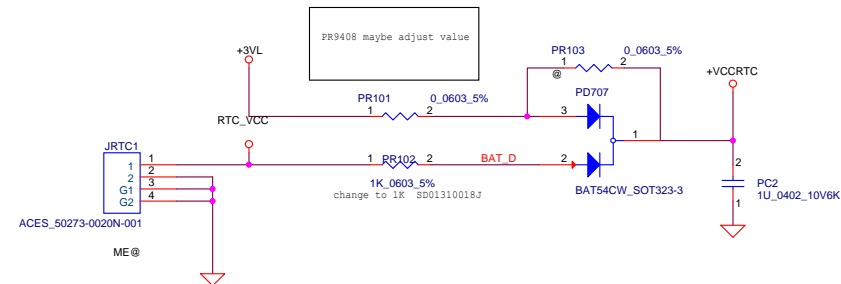
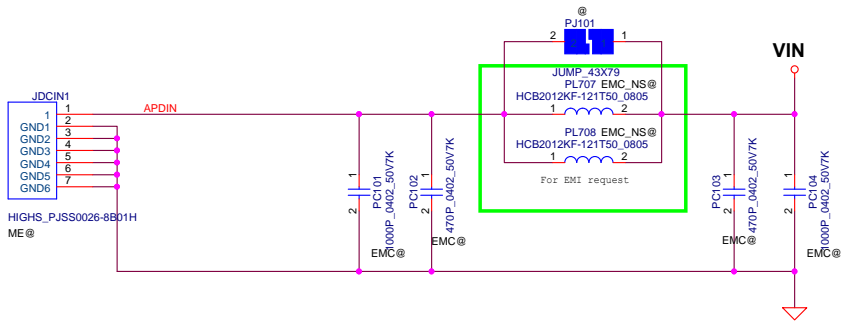


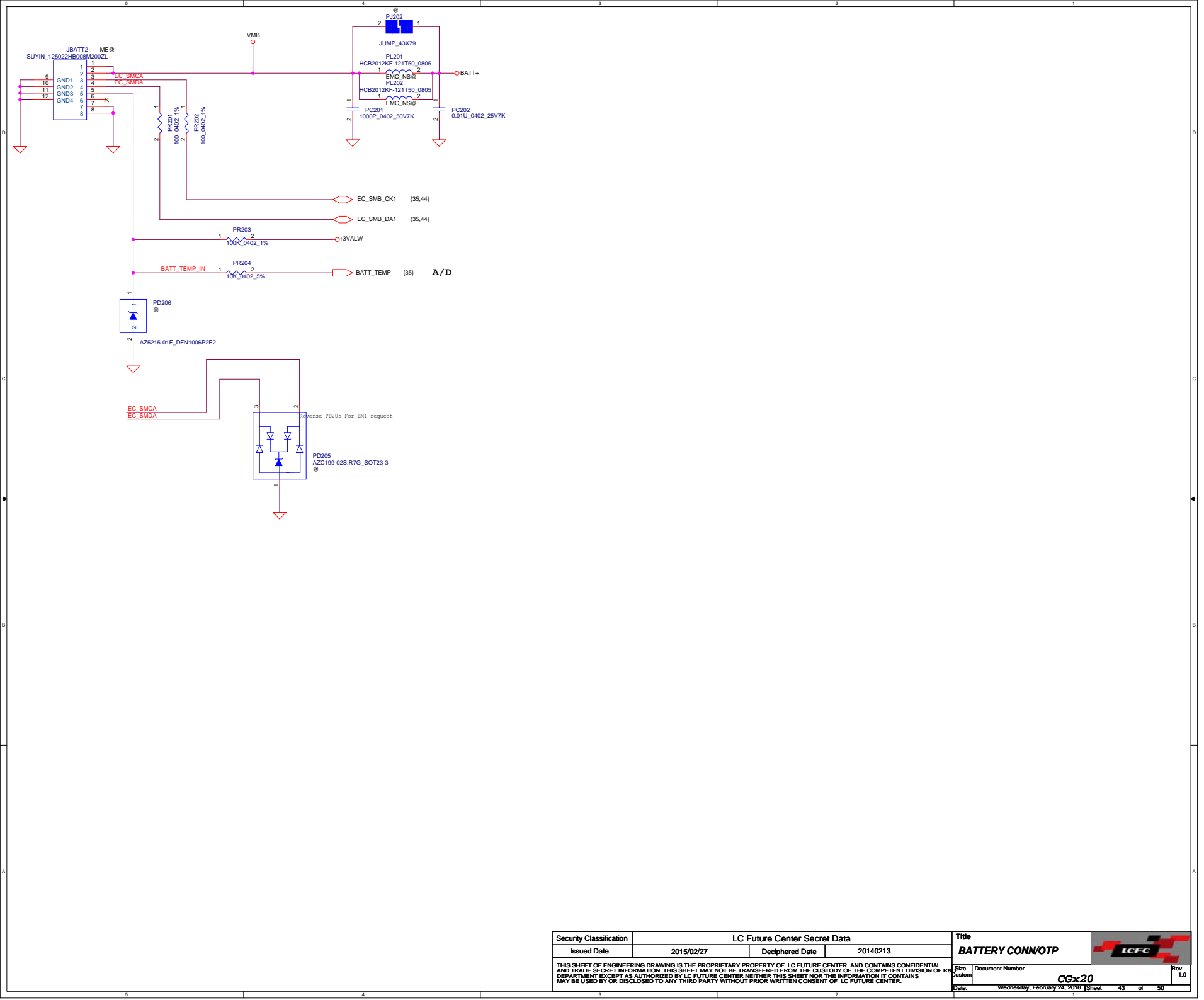
PCB Fedical Mark PAD

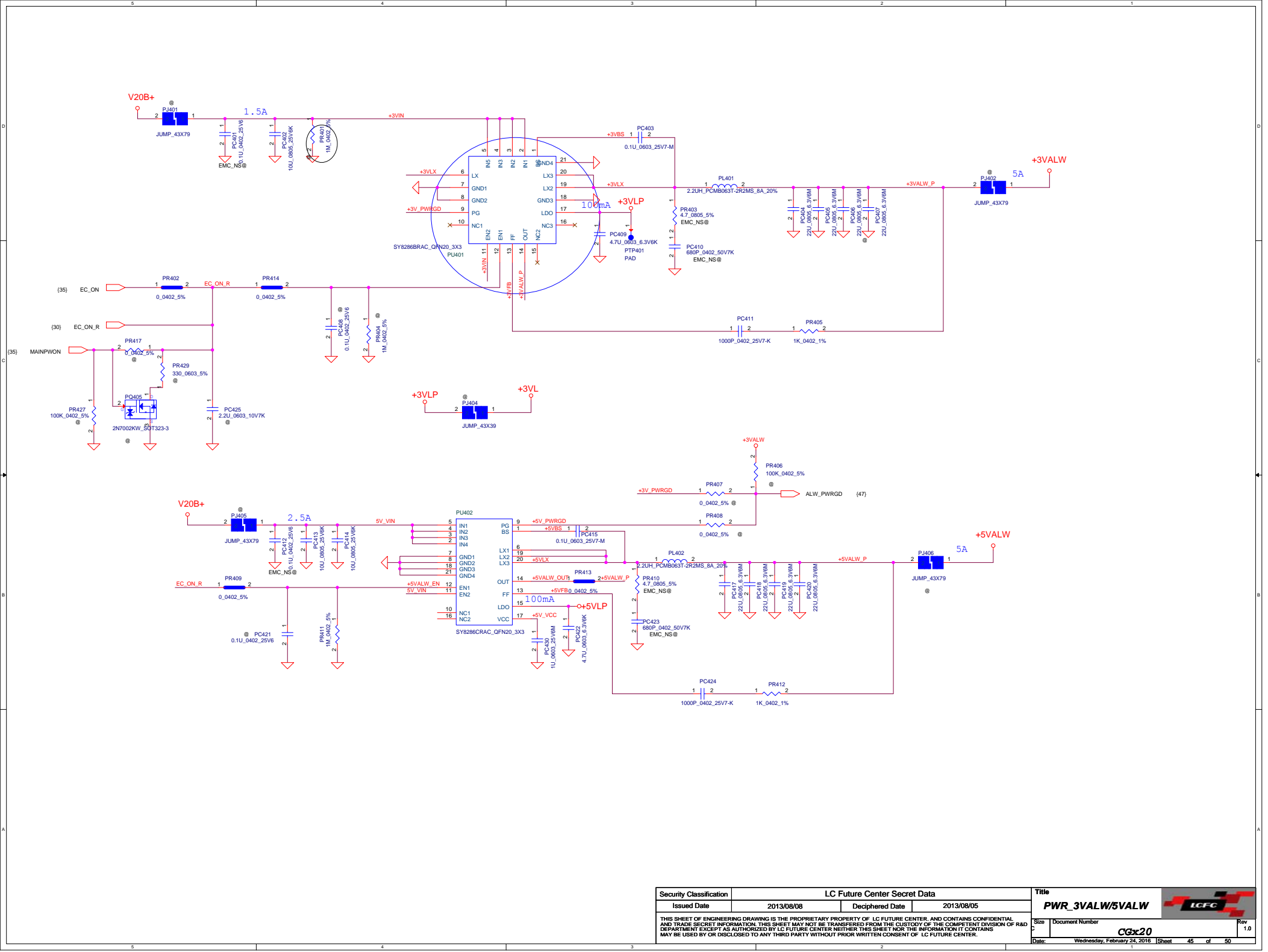


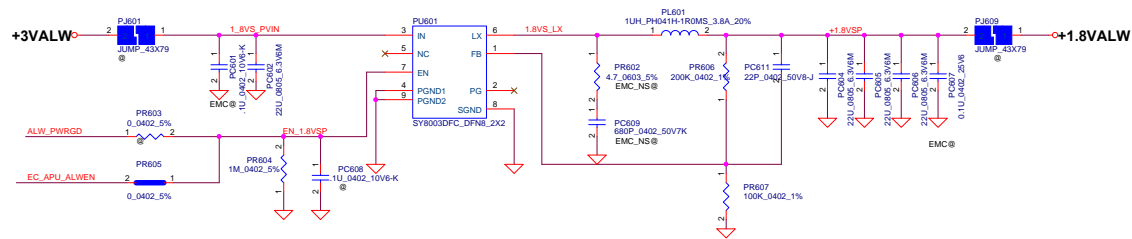
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Hole	
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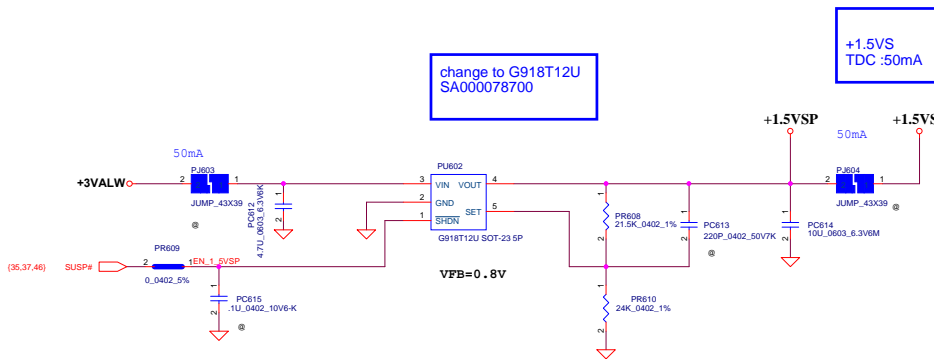






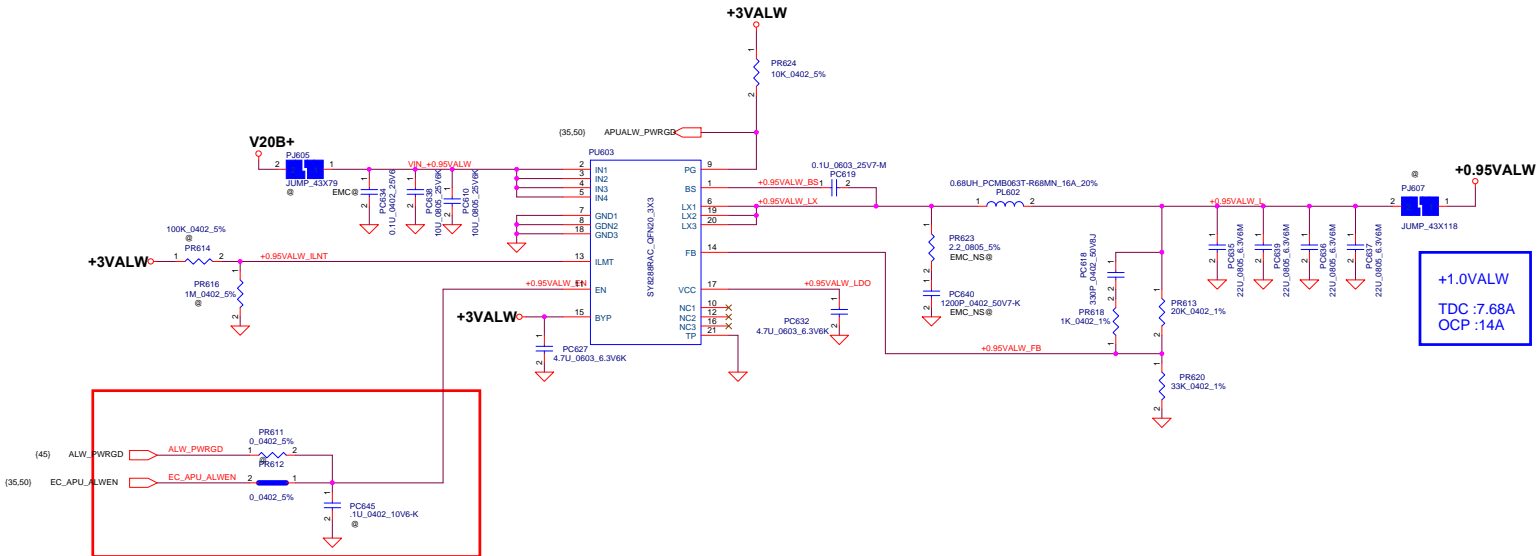


+1.8VALW
TDC :2.3A
OCP :3.8A



change to G918T12U
SA000078700

+1.5VS
TDC :50mA



+1.0VALW
TDC :7.68A
OCP :14A

