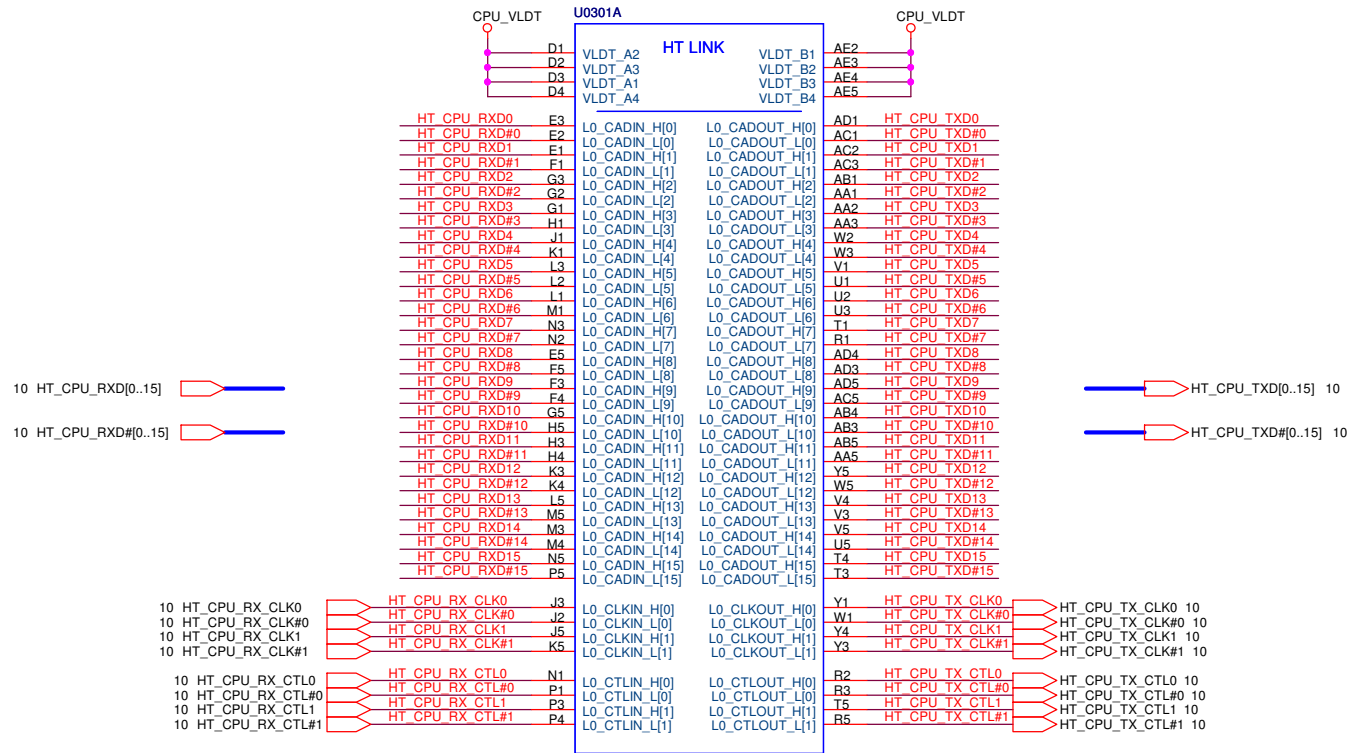
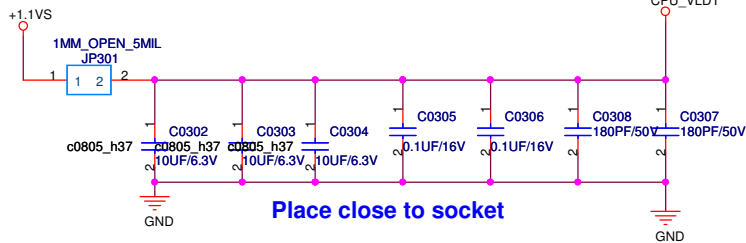


1.5A

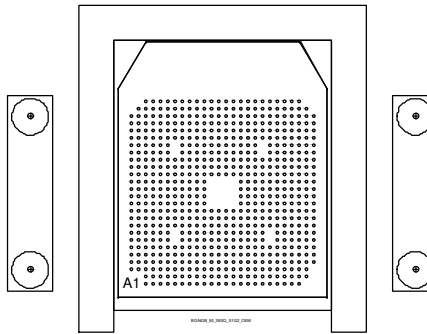


SOCKET638  
 Change P/N to 12G011306380  
 071113

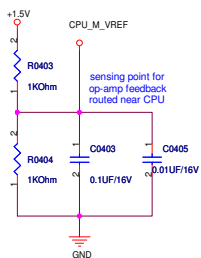
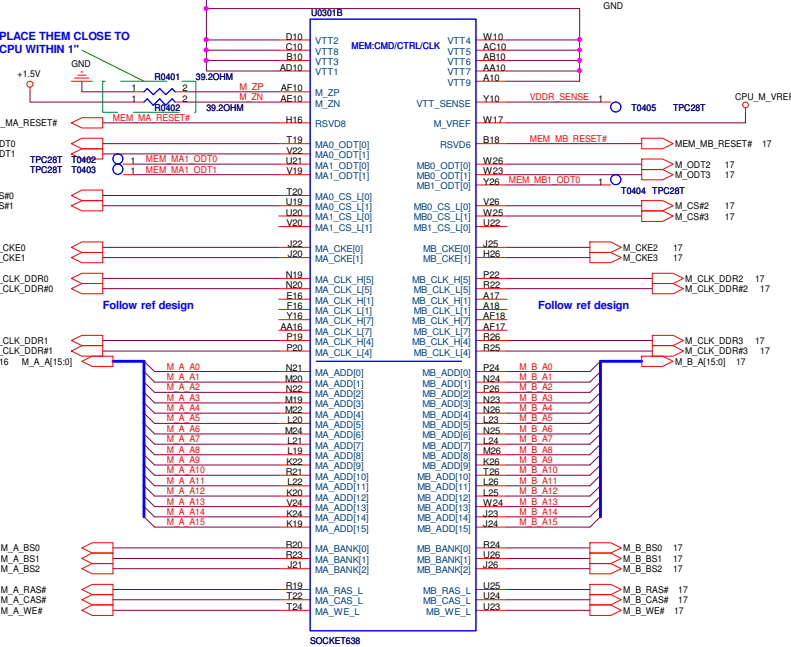
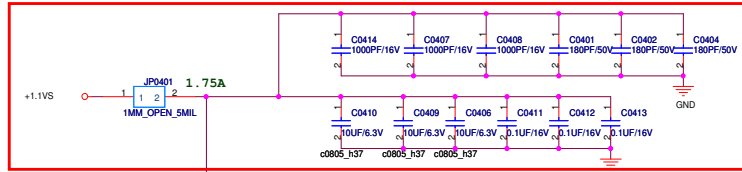
Do not cross plane.



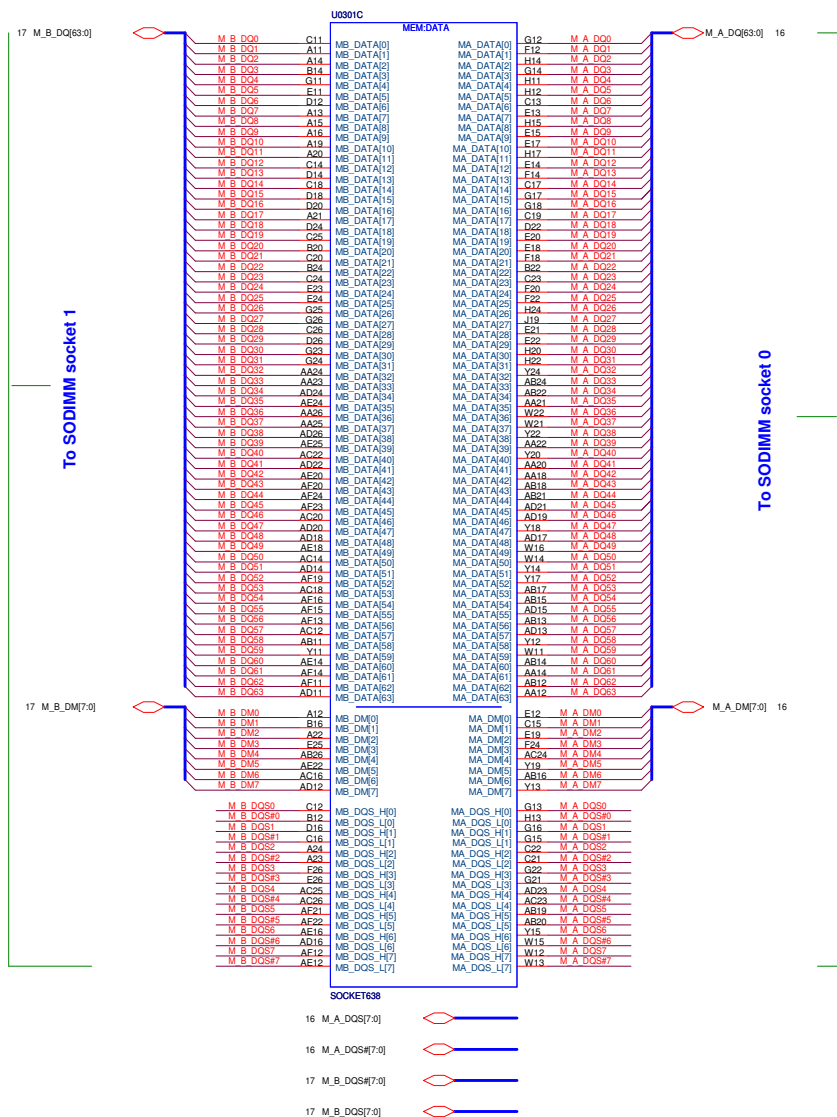
\* If VLDT is connected only on one side,  
 one 4.7uF cap should be added to  
 the island side

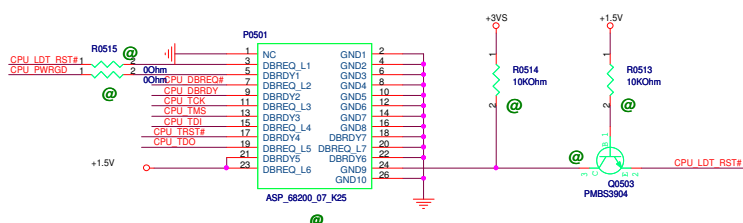
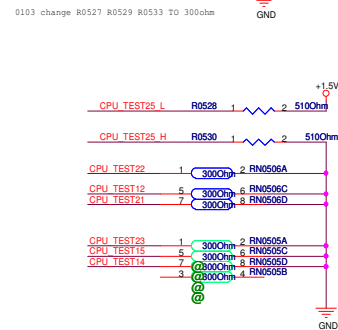


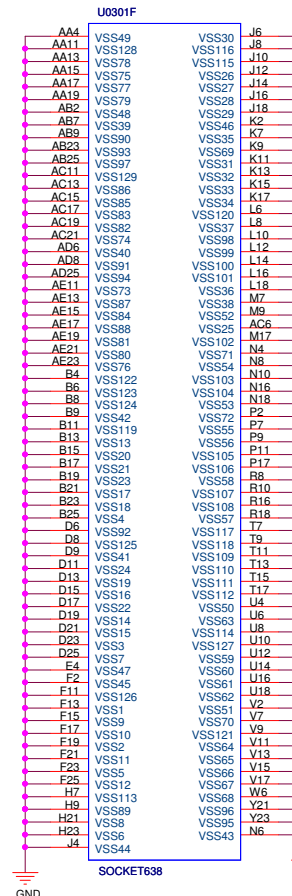
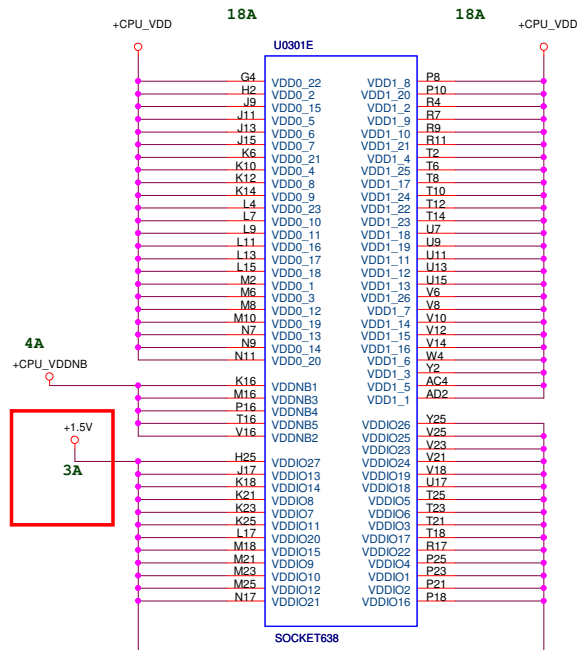
place close to socket



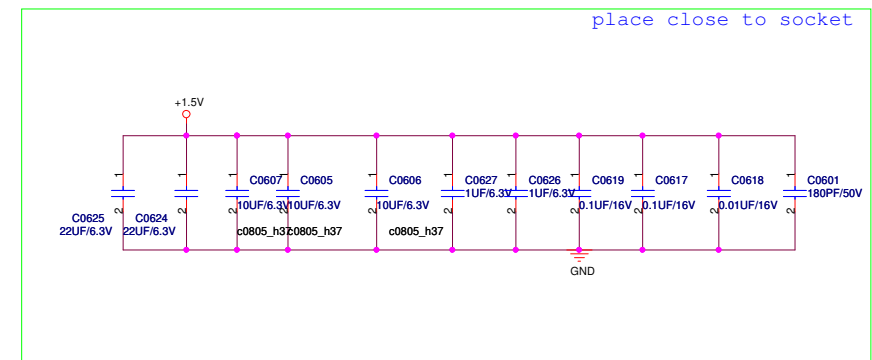
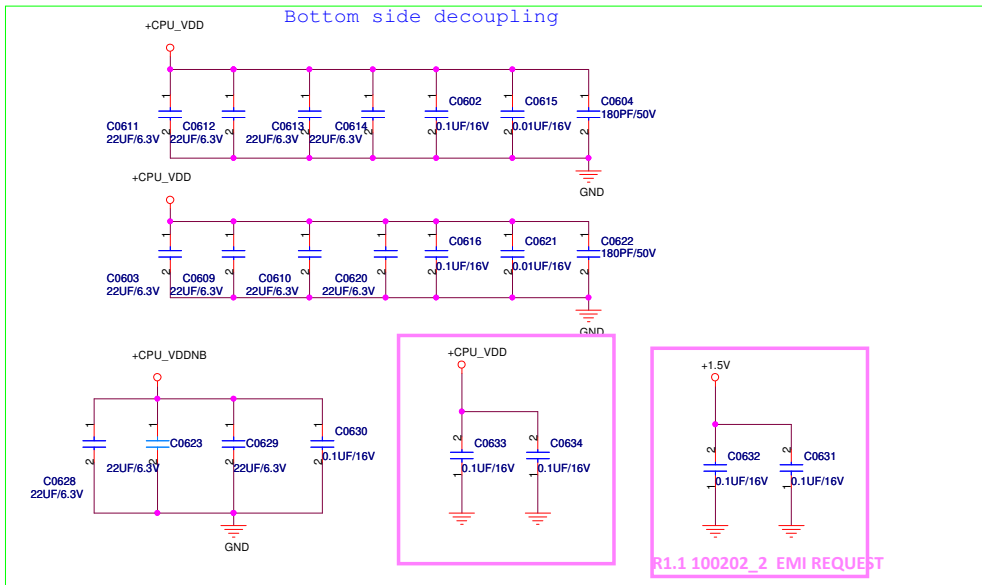
## Processor Memory Interface







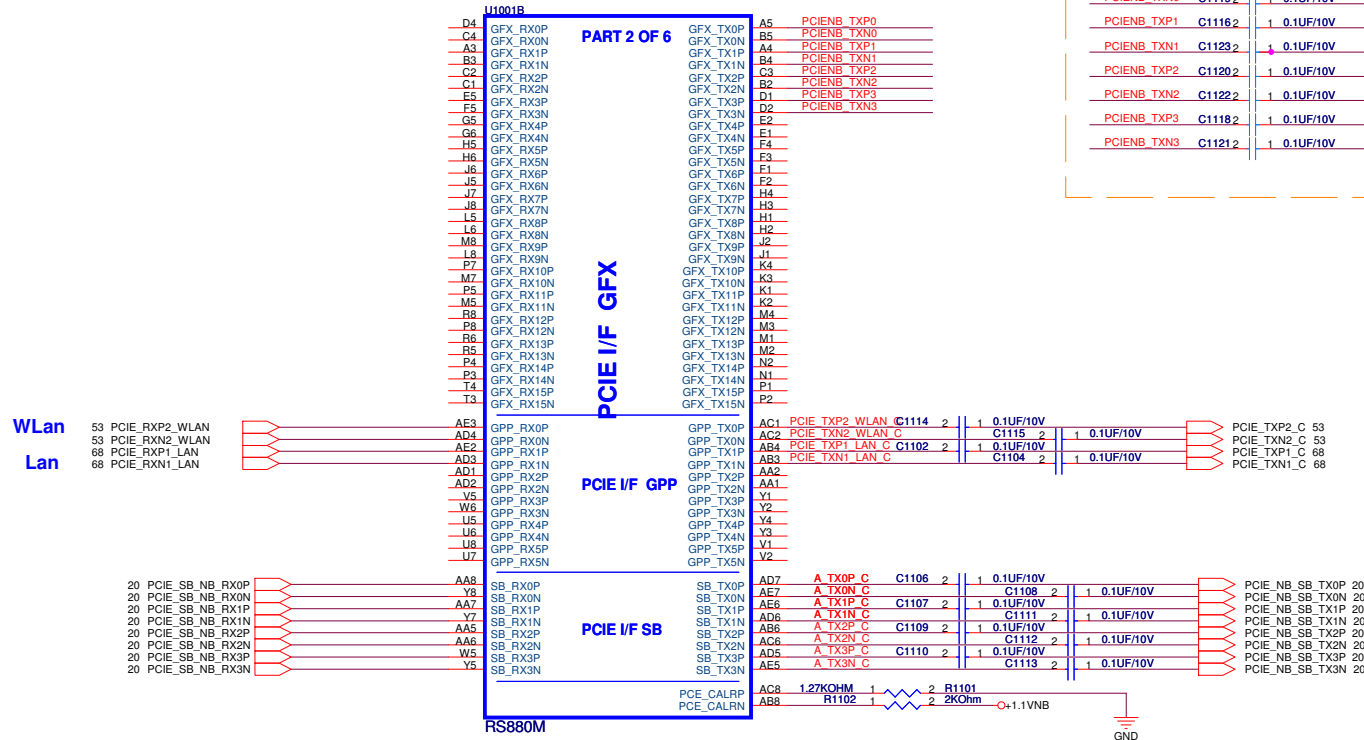
Decoupling between Processor and DIMMs, Place close to Porcessor as possible





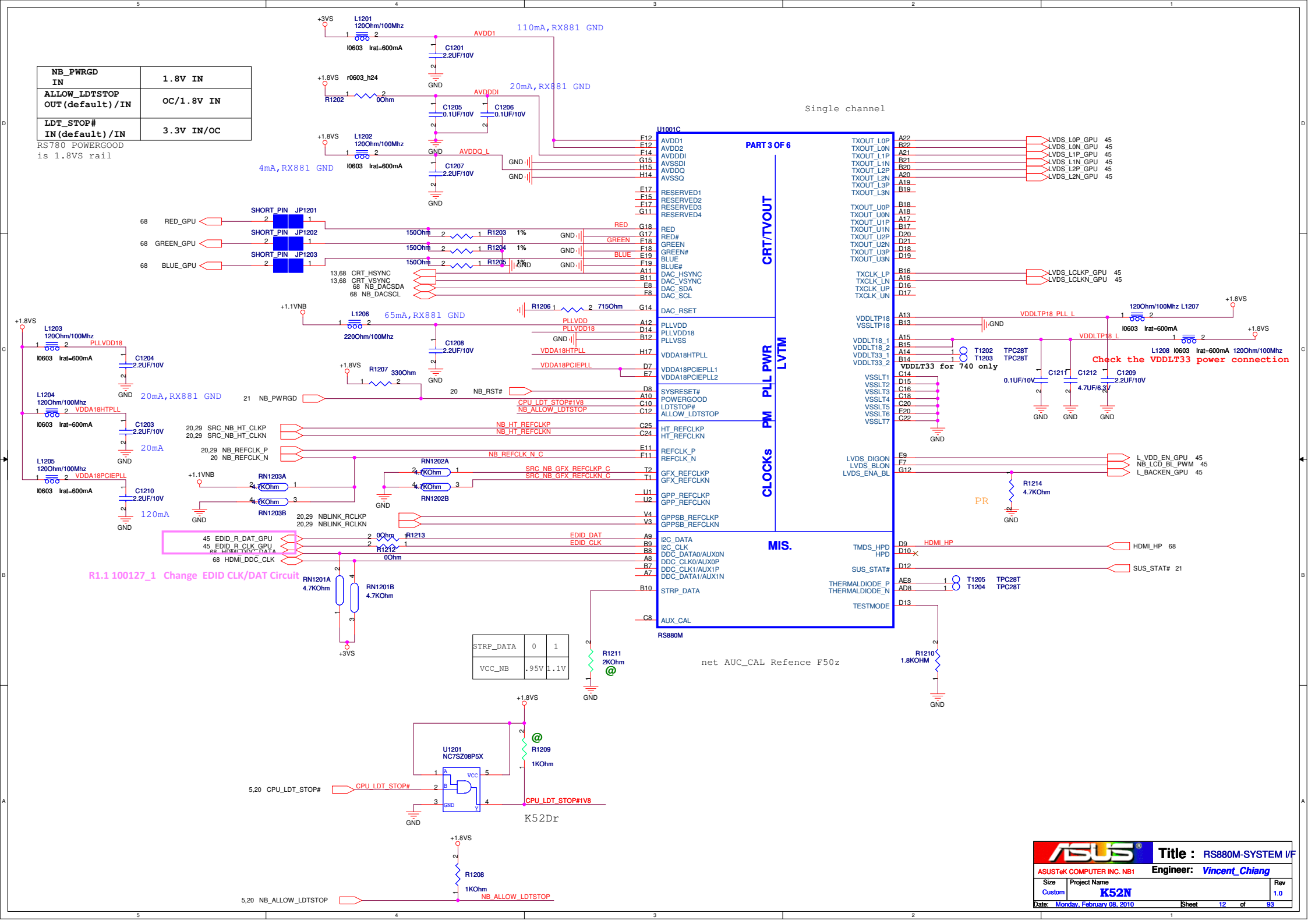
PCI-E:  
0-3 HDMI@ RS780M  
4-7 NC  
8-15 VGA8x

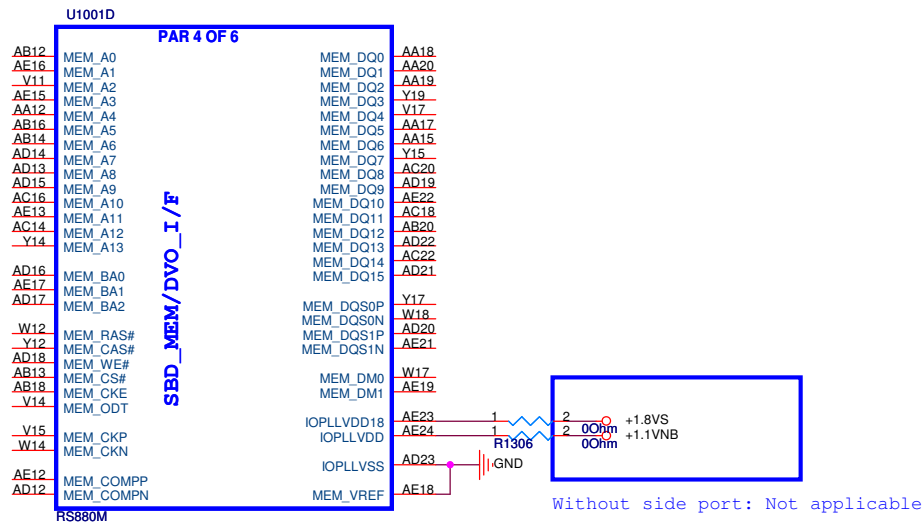
HDMI



NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

RS780 POWERGOOD  
is 1.8VS rail





#### DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS780:SUS\_STAT

#### STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

Enables the Test Debug Bus using PCIE bus:  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

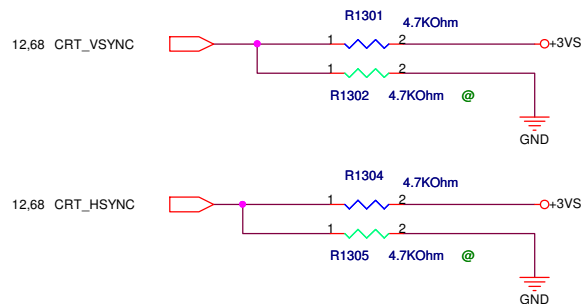
RS780: configurable thru register setting only

#### RS740/RS780: Enables Side port memory

RS780:HSYNC#

Selects if Memory SIDE PORT is available or not  
1 = Memory Side port Not available  
0 = Memory Side port available  
Register Readback of strap: NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]

080118  
Disable Side Port Memory  
R1.1



<b>ASUS</b>		<b>Title : RS880M-SPMEM/STRAPS</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Vincent_Chiang</b>	
Size B	Project Name <b>K52N</b>	Rev 1.0	
Date: Monday, February 08, 2010		Sheet 13 of 93	



R1.1 100127\_2 Modify +1.1V\_NB to +1.1VNB

2 x 4.7uF  
4 x 0.1uF

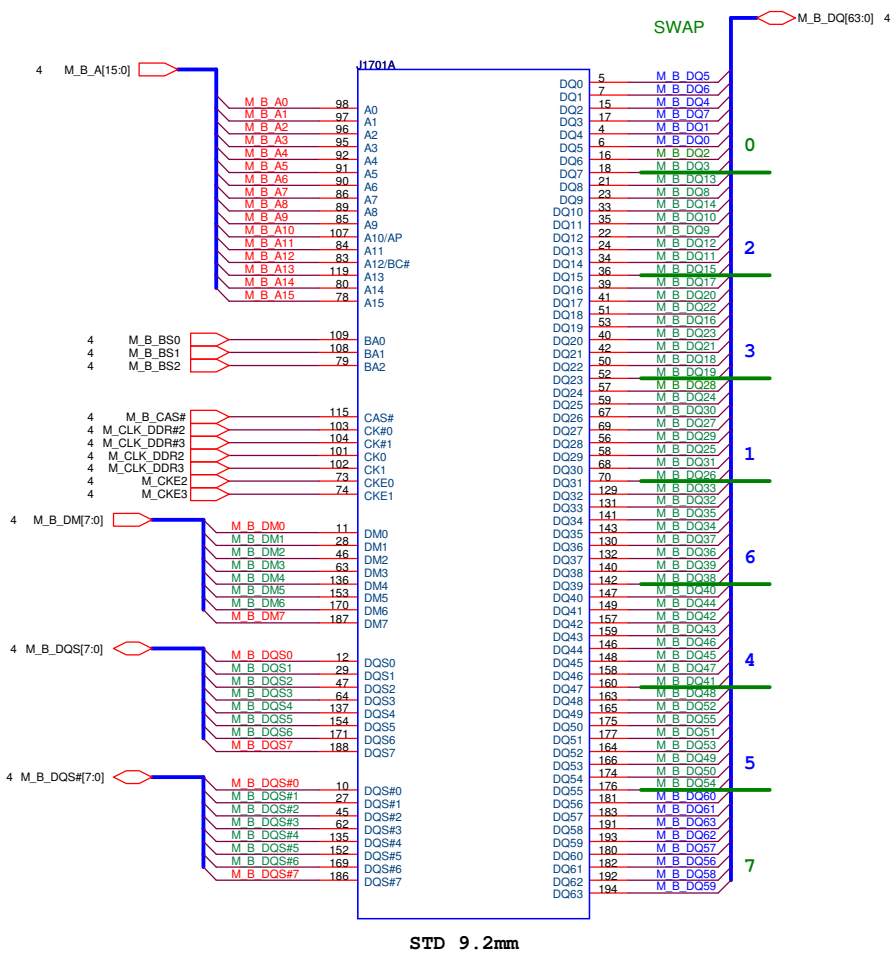
AMD recommended:  
side port not used, connect to GND

AMD recommended:  
side port not used, connect to GND

RS880M POWER TABLE

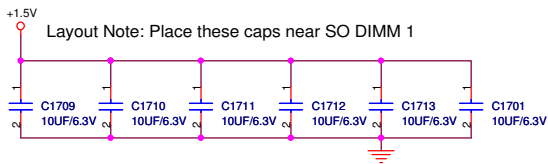
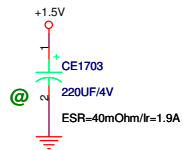
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL13	NC



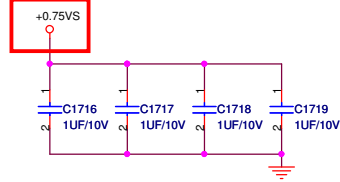
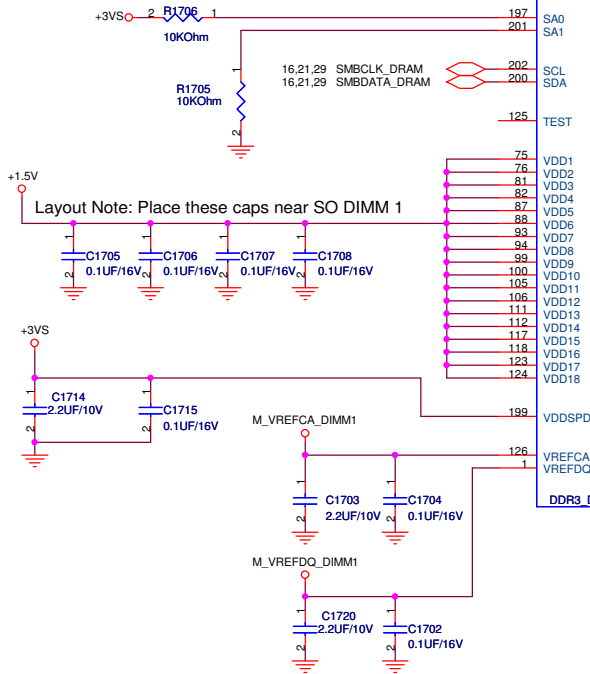


STD 9.2mm

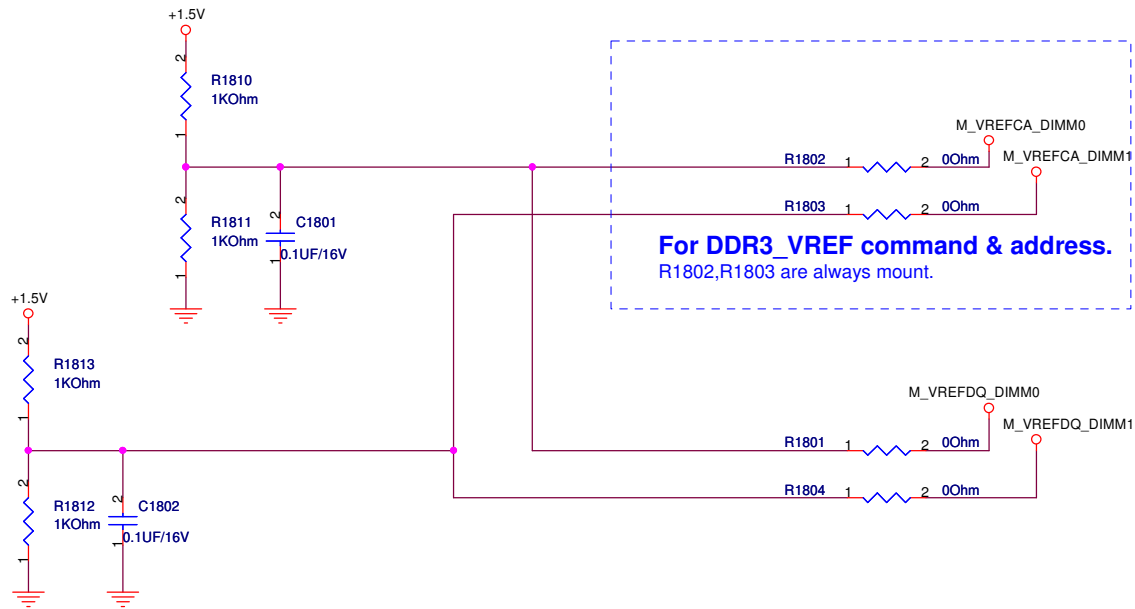
DDR3\_DIMM\_204P




SMBus Slave Address: A2H



DDR3 Vref





Title

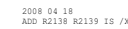
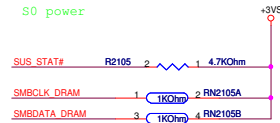
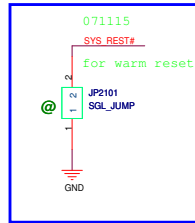
DDR3 CA\_DQ VOLTAGE

ASUSTeK COMPUTER INC. NB6

Engineer: Vincent\_Chiang

Size	Project Name	Rev
Custom	K52N	2.0
Date: Monday, February 08, 2010		Sheet 18 of 99

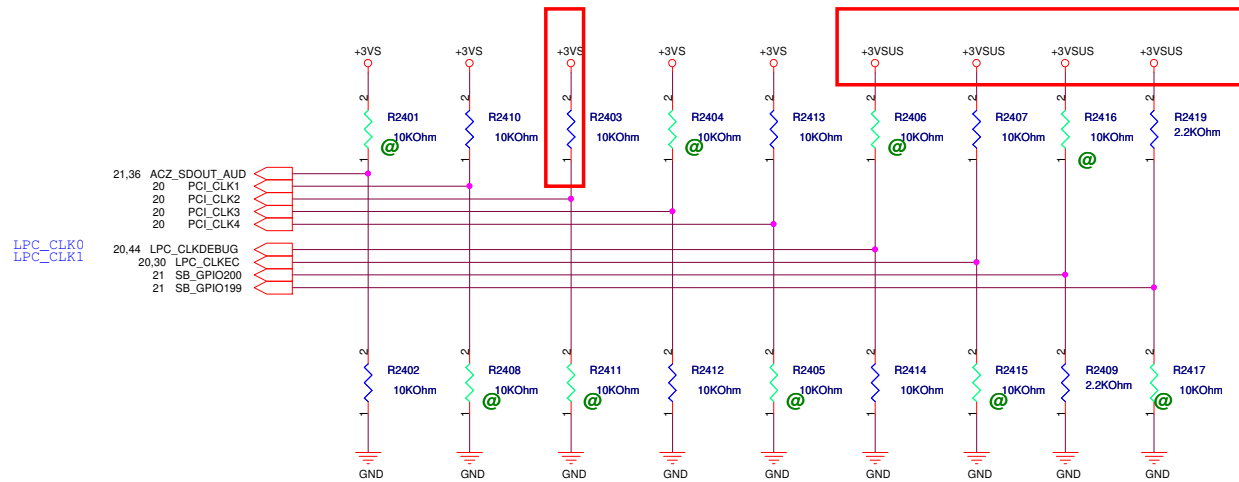






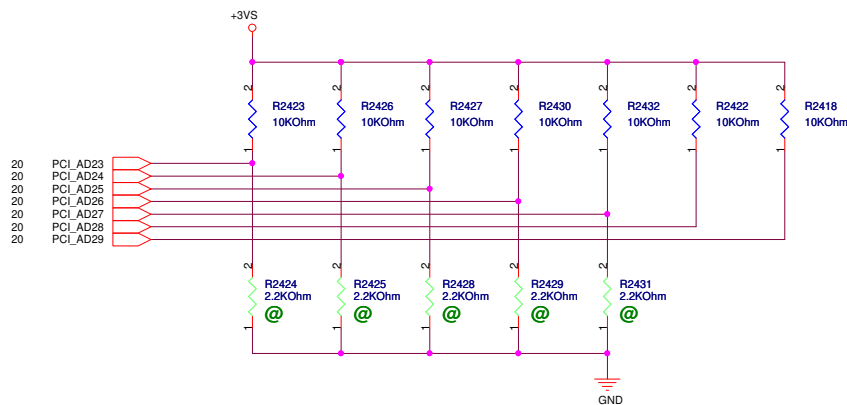




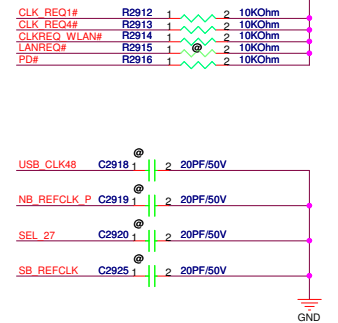
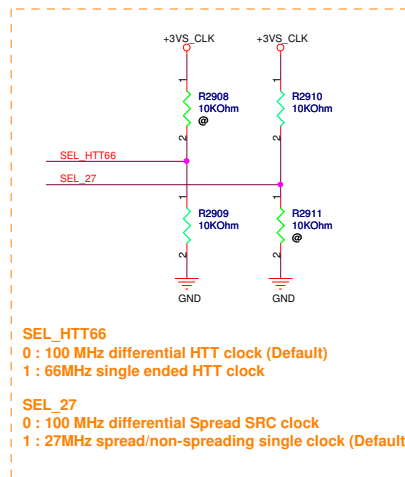
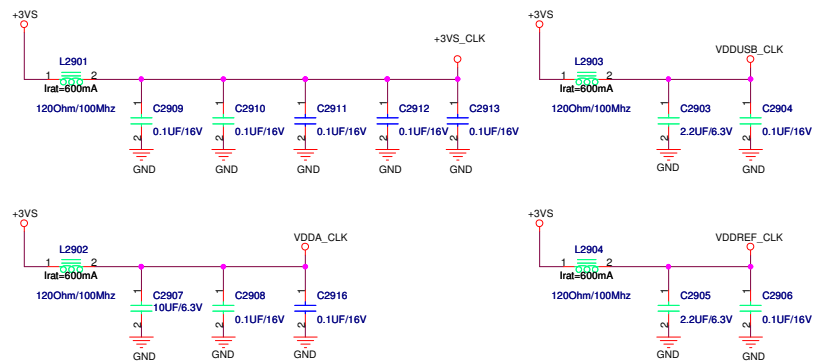
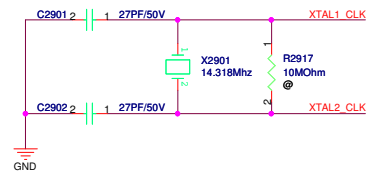
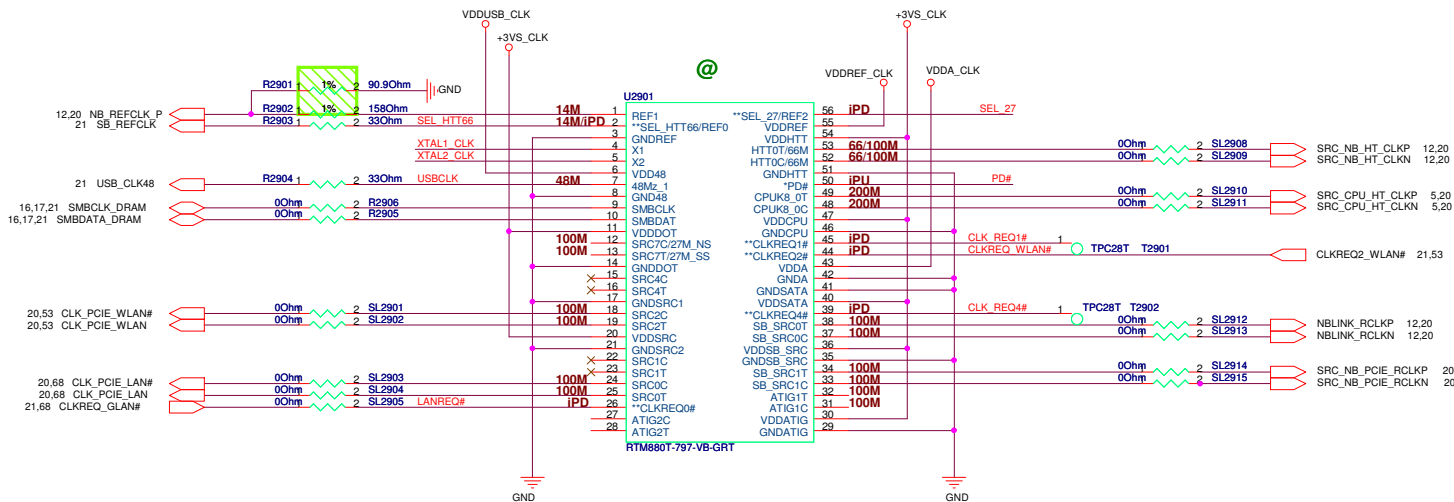


# REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled Modify	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

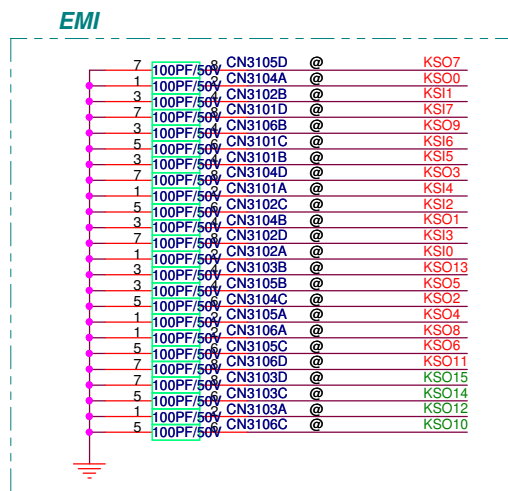
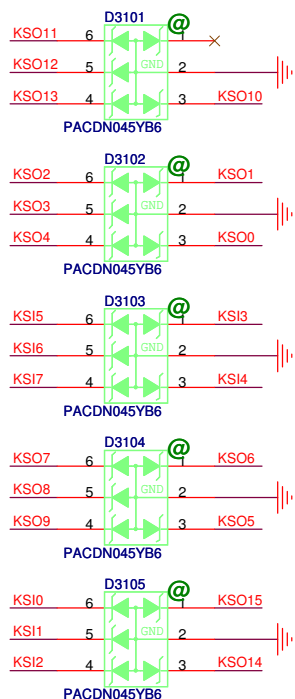


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

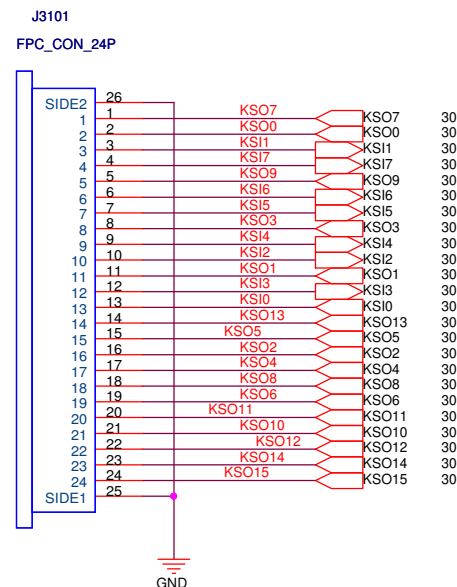


<Variant Name>			
<b>ASUS</b>		<b>Title : ICS9LPRS489AGLFT</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	<b>K51AB</b>	2.0	
Date: Monday, February 08, 2010	Sheet 29	of 93	

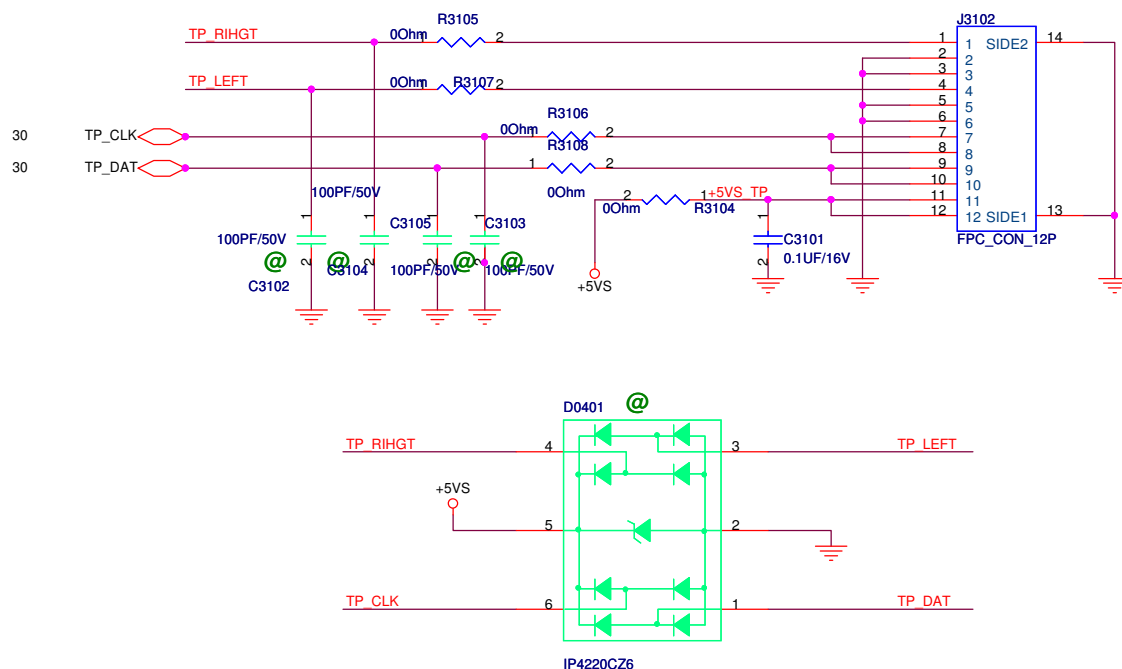




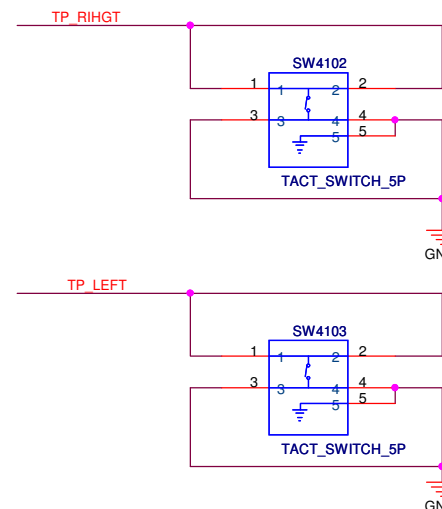
Keyboard

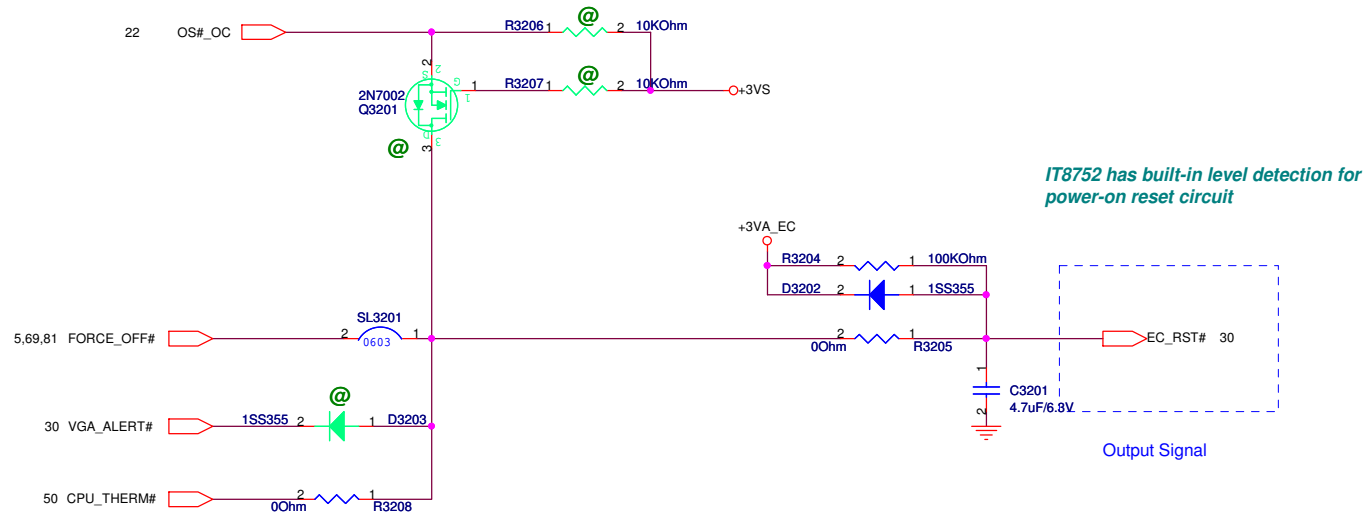


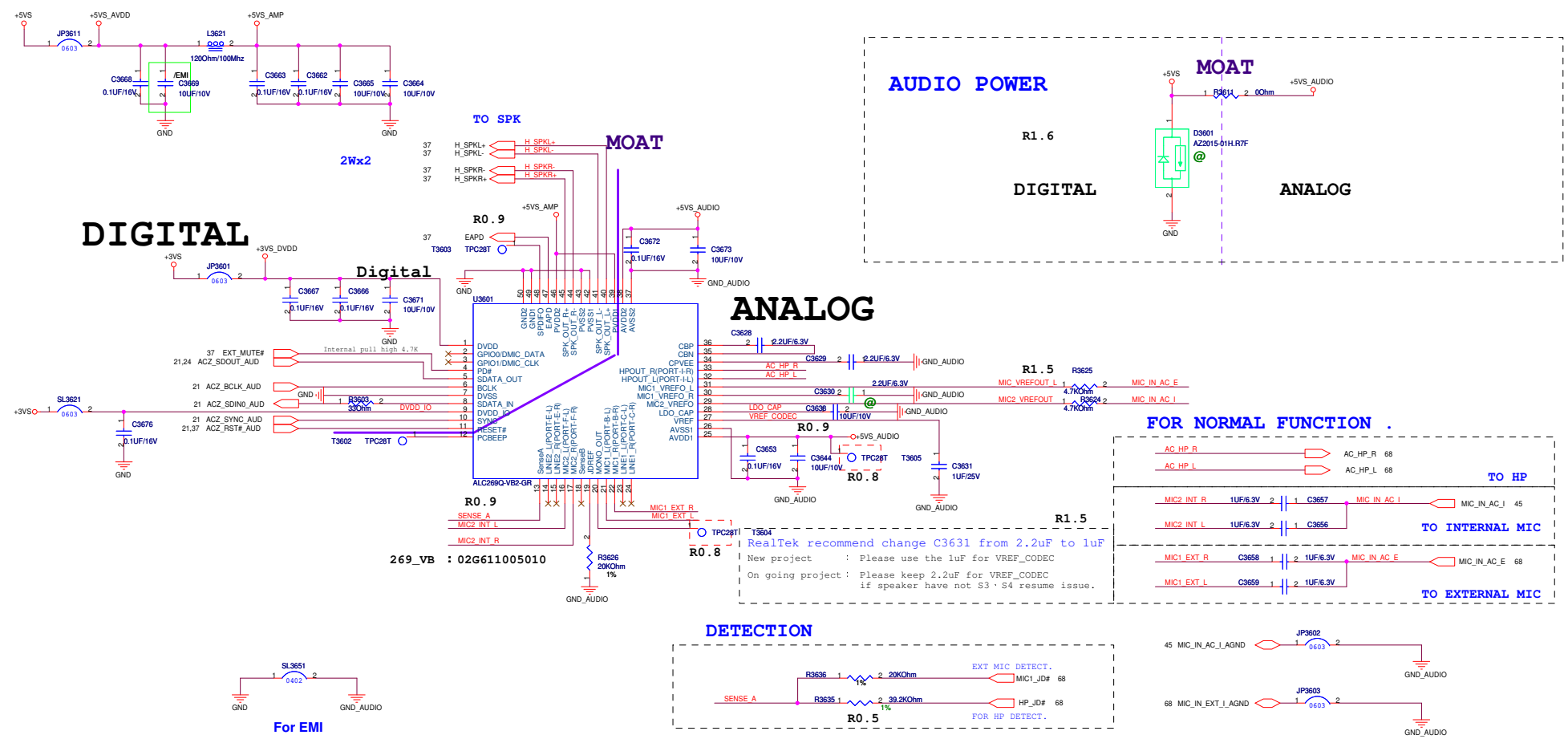
Touchpad

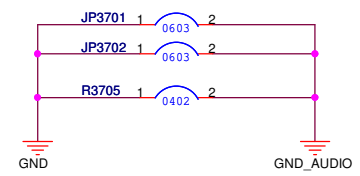
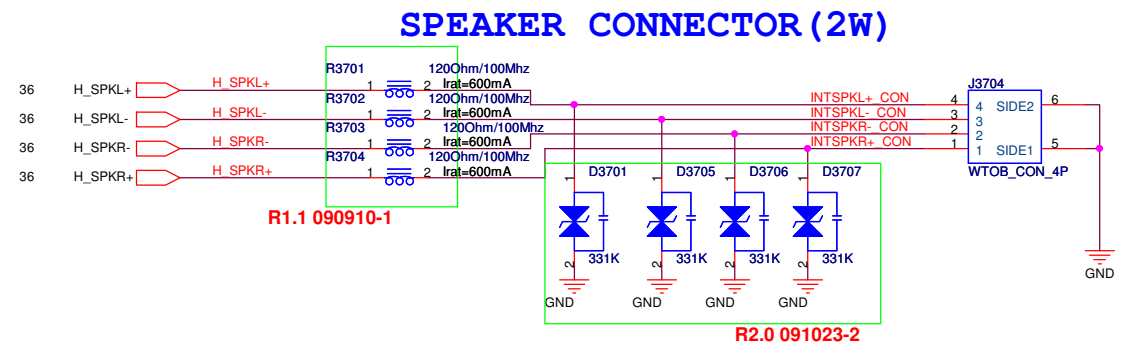
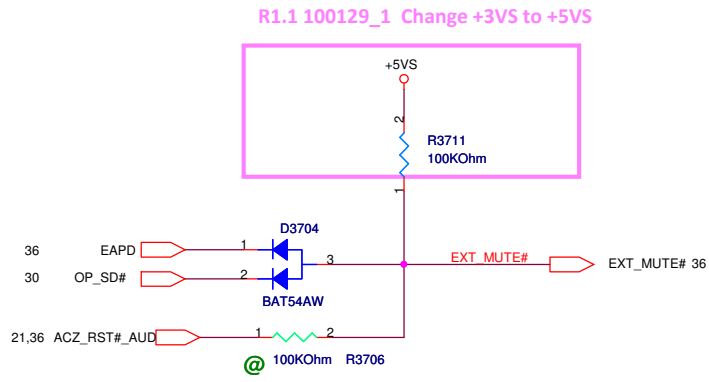


SW4102, SW4103 use PCB footprint of 12G091030050

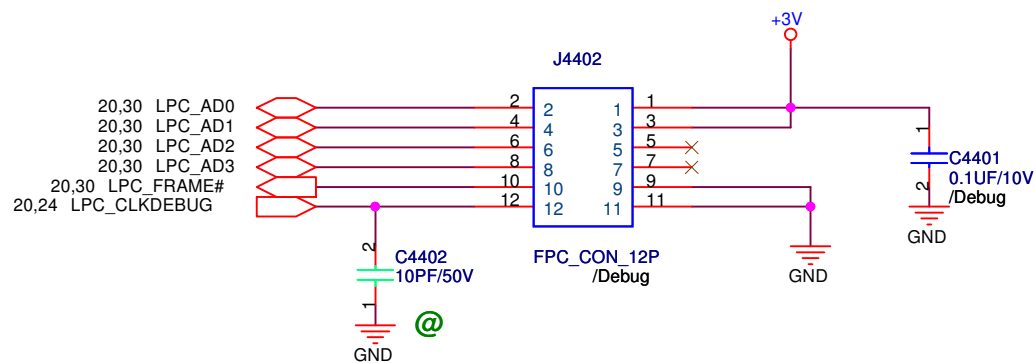







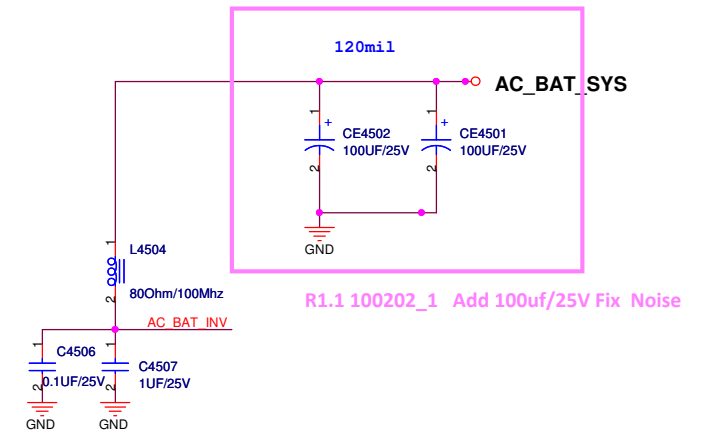
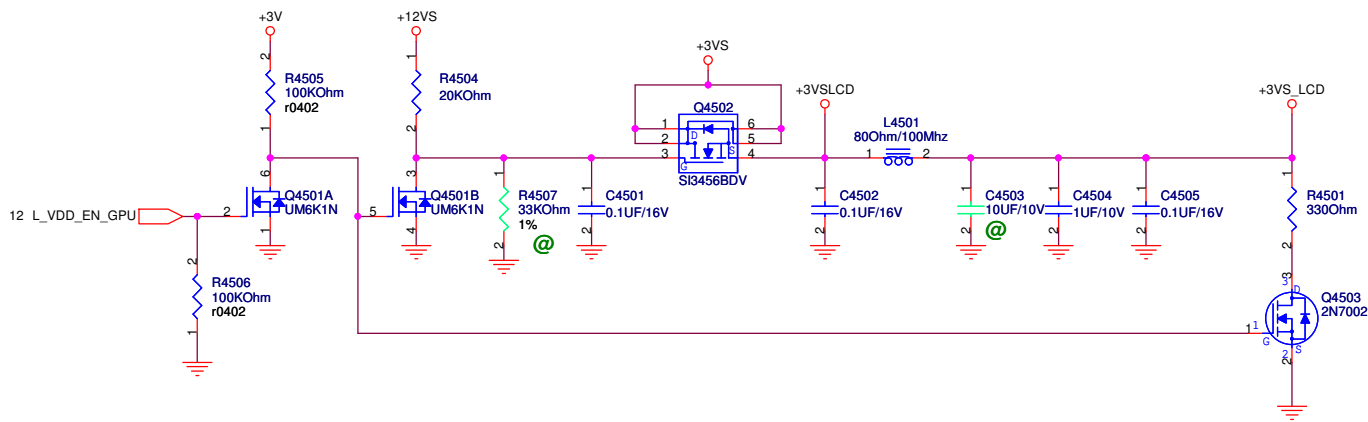


## LPC Debug Port

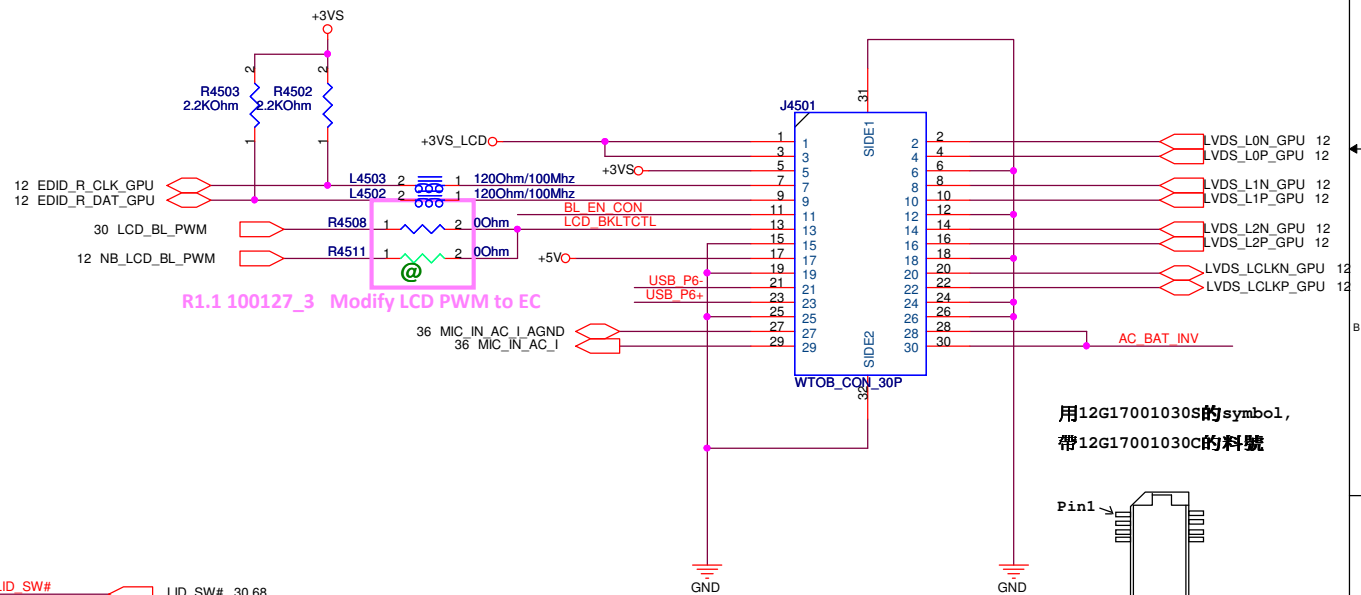
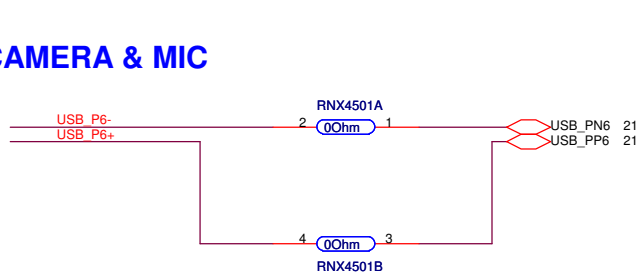


		<b>Title :</b> <u>BUG_Debug</u>	
ASUSTeK COMPUTER INC. NB4		<b>Engineer:</b> <u>Vincent_Chiang</u>	
Size Custom	Project Name <b>K52N</b>		Rev 1.0
Date: <u>Monday, February 08, 2010</u>		Sheet	<u>44</u> of <u>99</u>

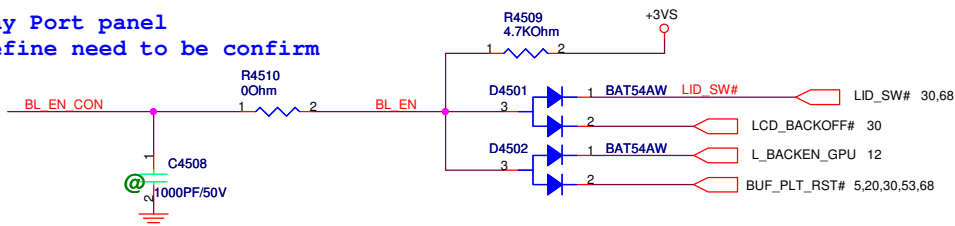




## CAMERA & MIC



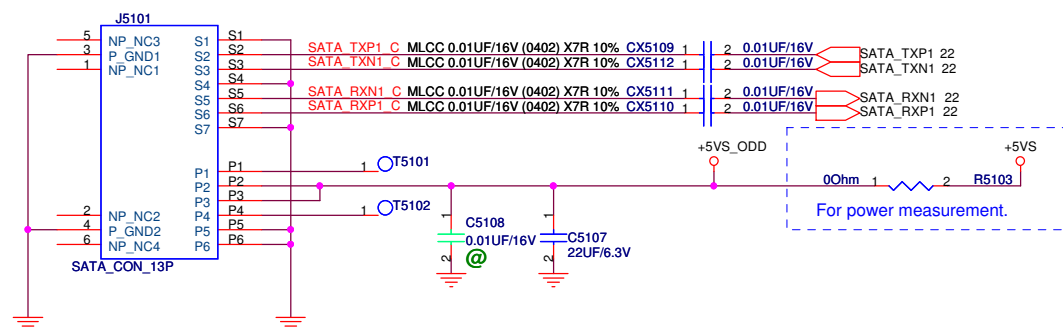
## Display Port panel pin define need to be confirm



<b>ASUS</b>		Title : <b>CRT_LCD Panel</b>	
ASUSTeK COMPUTER INC. NB4		Engineer: <b>Vincent_Chiang</b>	
Size B	Project Name <b>K52N</b>	Rev 1.0	
Date: <b>Monday, February 08, 2010</b>		Sheet <b>45</b> of <b>99</b>	



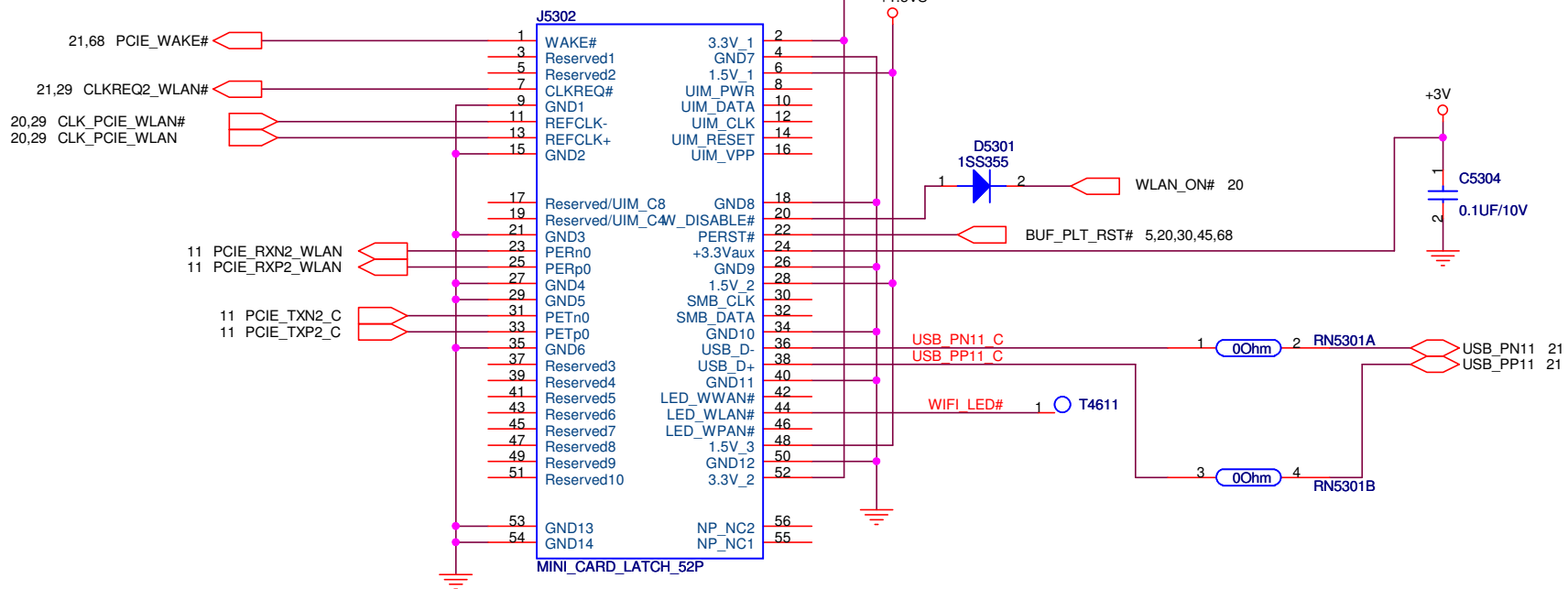
## Main Board



The diagram illustrates the electrical connections for the J5103 connector, specifically the SATA controller and power supply sections. The SATA signals (TXP0, TXN0, RXN0, RXP0) are connected to the MLCC capacitors (C5101, C5102, C5103, C5104) and the SATA controller (SATA\_TXP0, SATA\_TXN0, SATA\_RXN0, SATA\_RXP0). The power supply connections for +3VS\_HDD1 and +5VS\_HDD1 are shown, including the SL5101 and R5101 components. The diagram is labeled 'J5103' and 'SATA CON 22P'.

Support wake from S3 only

使用12G03010052F symbol

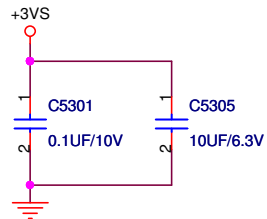


## WLAN

### WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

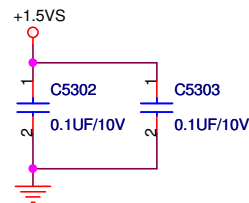
Place 10UF near +3VAUX\_WLAN source side.



### WLAN +1.5VS bypass capacitor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side

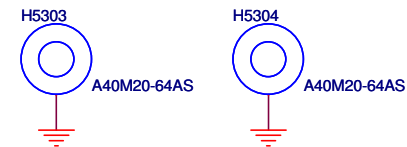



### WLAN nuts:

Minicard spec R1.2:

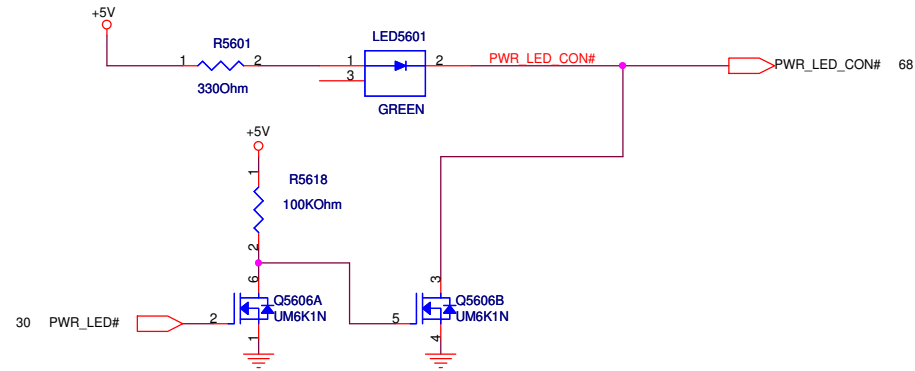
Full size card= 2pcs.

Half size card= 2pcs.

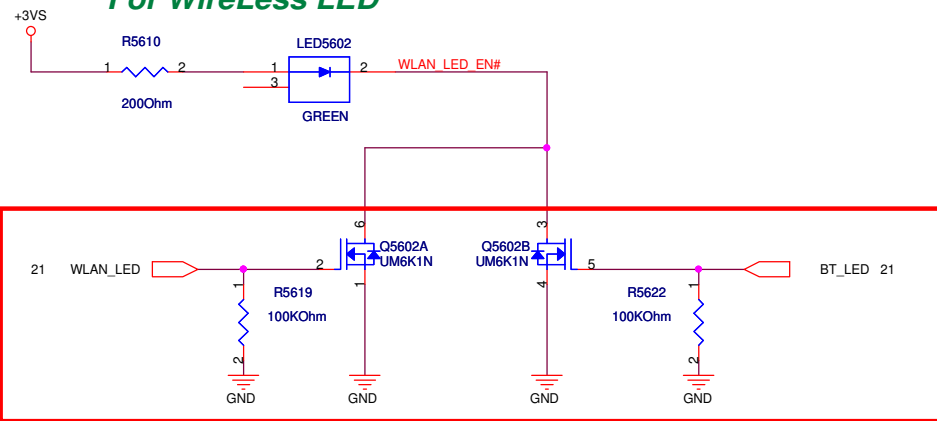


		Title : <b>MINICARD(WLAN)</b>	
ASUSTeK COMPUTER INC. NB6		Engineer: <b><i>Vincent_Chiang</i></b>	
Size Custom	Project Name <b>K52N</b>		Rev 1.0
Date: <b>Monday, February 08, 2010</b>		Sheet <b>53</b> of <b>99</b>	

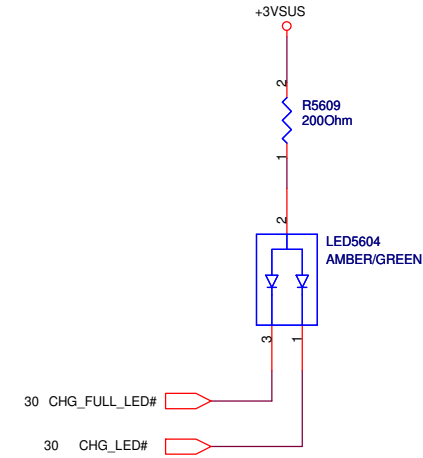
## For POWER LED



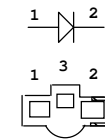
## For WireLess LED



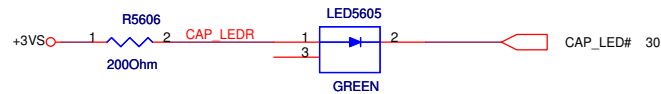
## Charge LED



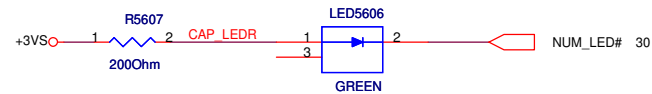
## Side Light LED symbol



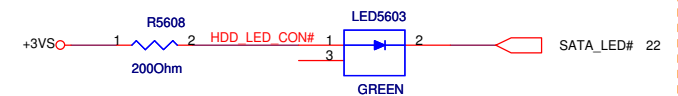
## Cap. Lock LED



## for Num Lock

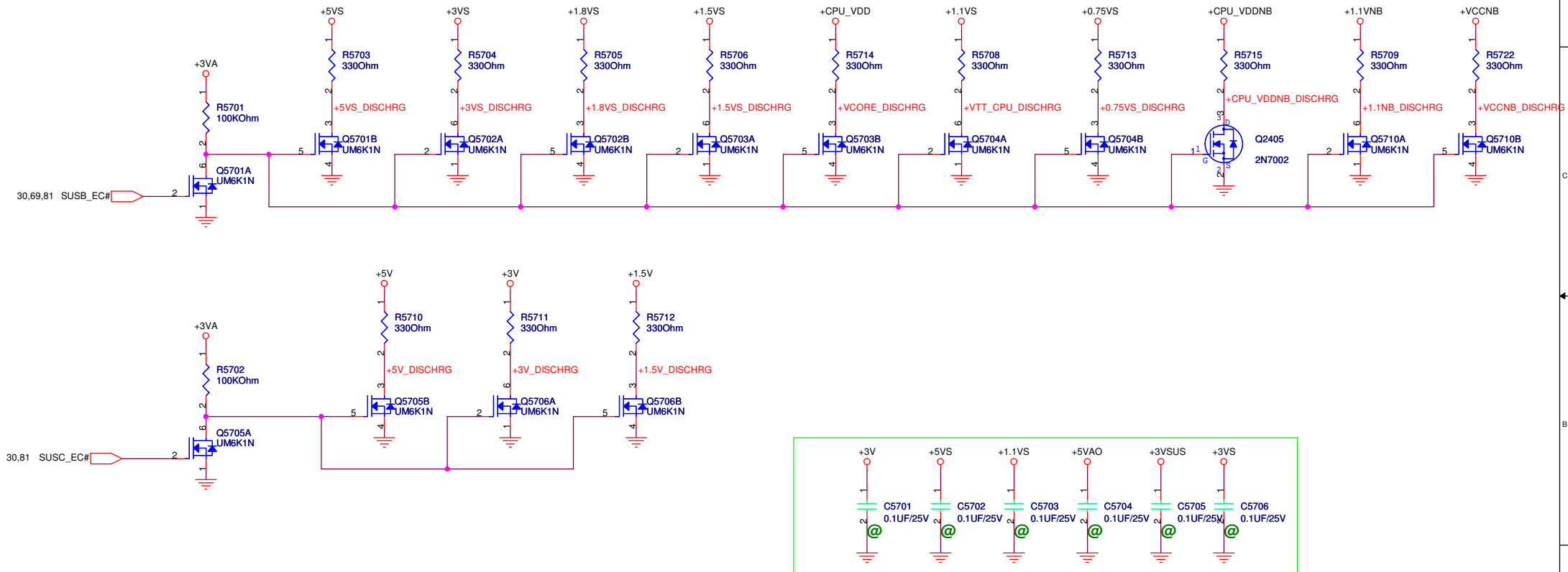


## HDD LED



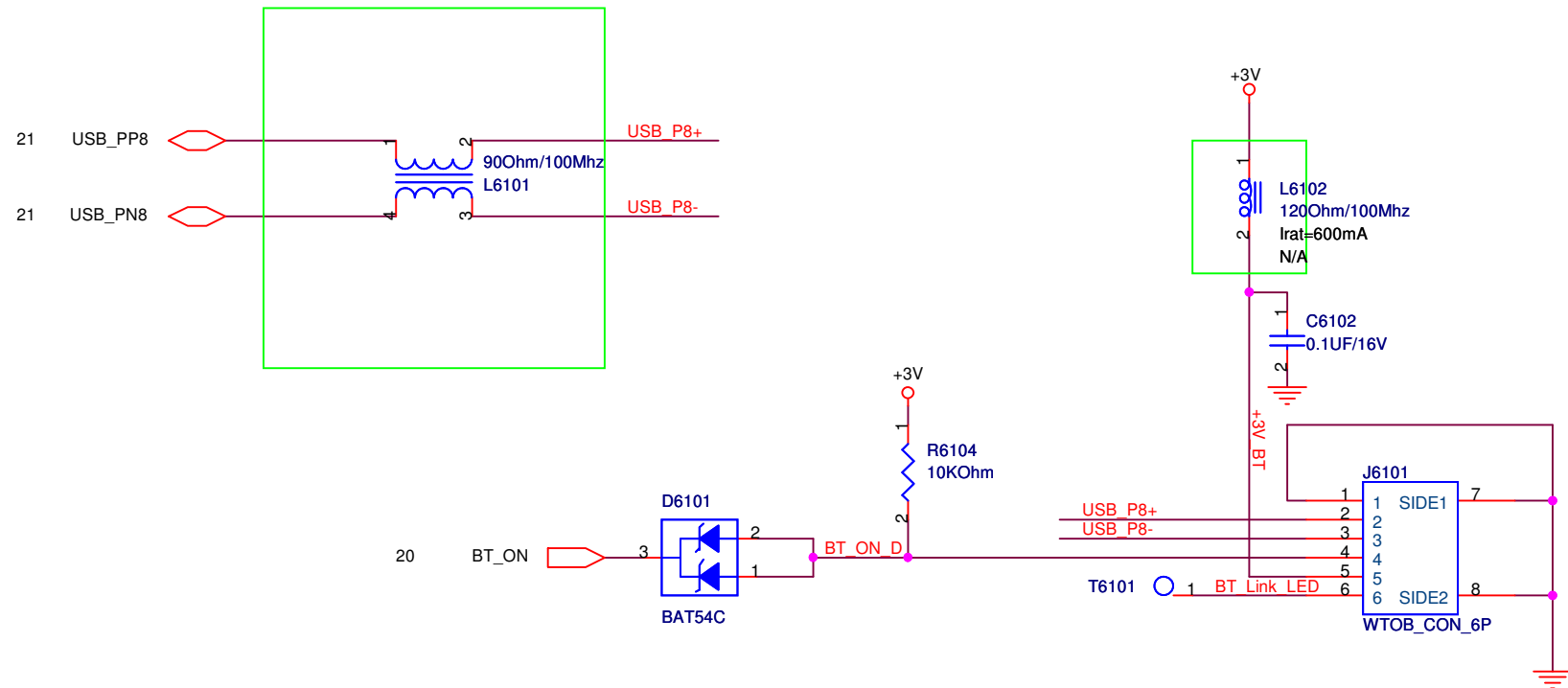
# Main Board

Remove +2.5Vs is for ATI GFX

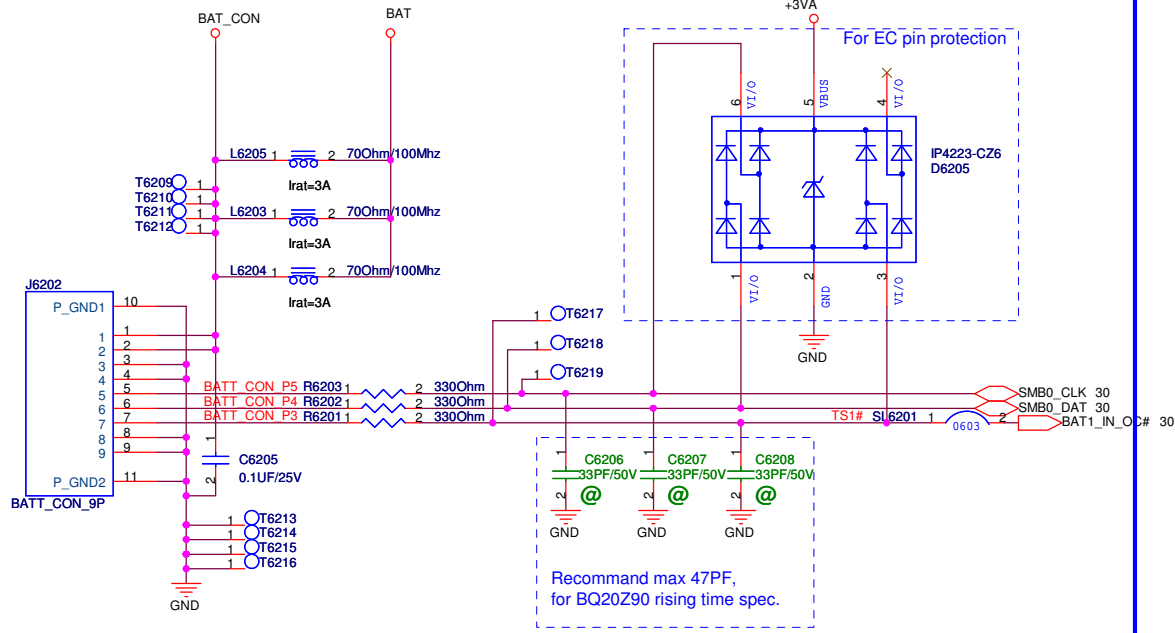


		Title : <b>DSG_Discharge</b>	
ASUSTeK COMPUTER INC. NB4		Engineer: <b><i>Vincent_Chiang</i></b>	
Size <b>B</b>	Project Name <b>K52N</b>		Rev <b>1.0</b>
Date: <b>Monday, February 08, 2010</b>		Sheet <b>57</b>	of <b>99</b>

# BLUETOOTH



# Battery Connector



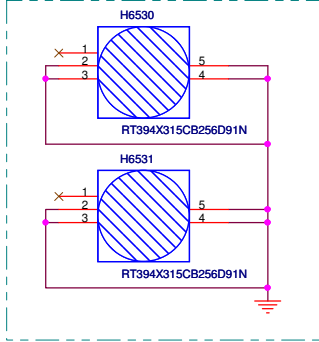
Total count: 11 pcs

<b>ASUS</b>		Title : DC_DC & BAT Conn.	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size B	Project Name <b>K52N</b>		Rev 1.0
Date: Monday, February 08, 2010		Sheet 62 of 99	

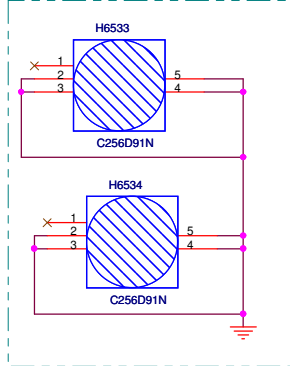


# Main Board

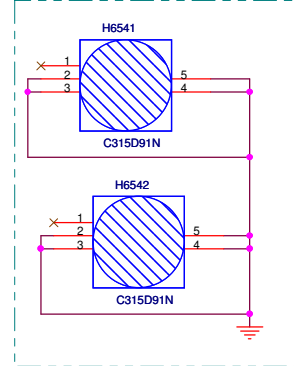
Screw Hole A



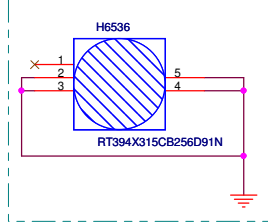
Screw Hole B



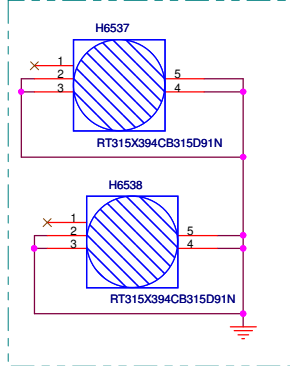
Screw Hole I



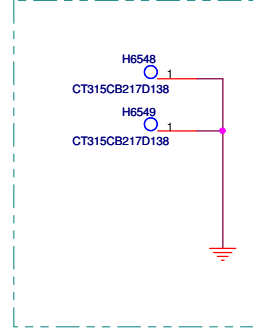
Screw Hole C



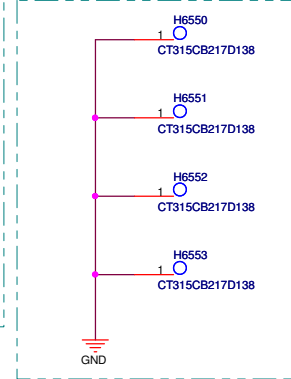
Screw Hole F



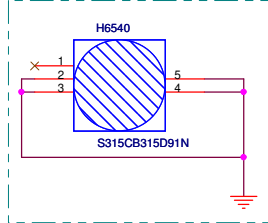
Screw Hole E



Screw from k52JR



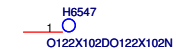
Screw Hole H



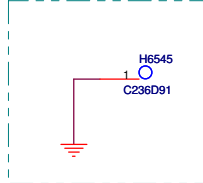
Tooling Hole K

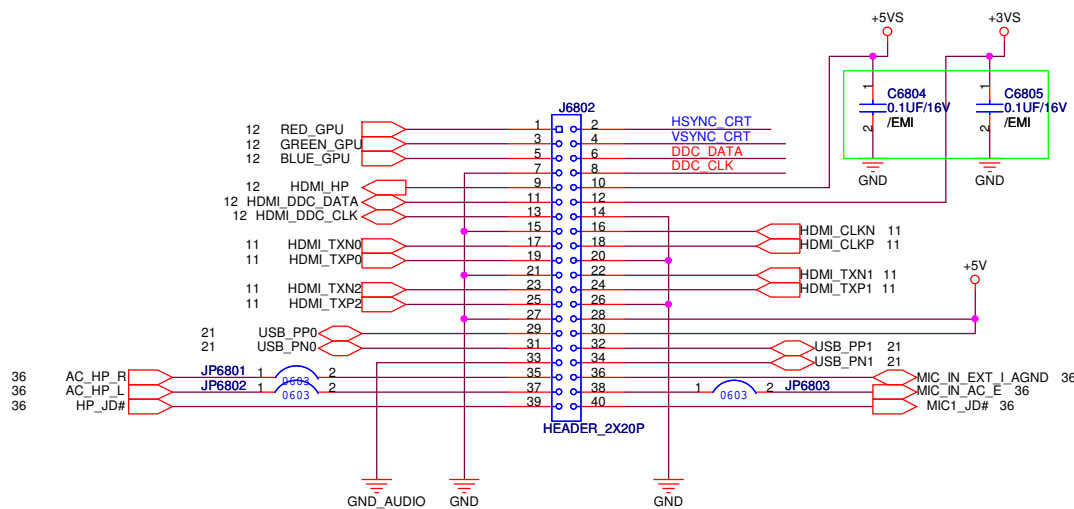
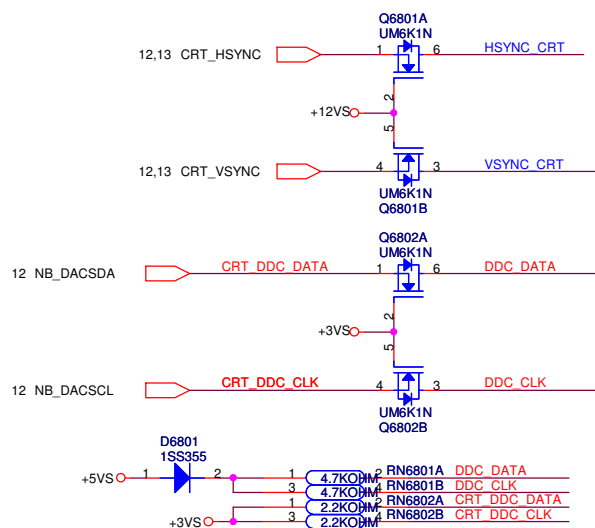
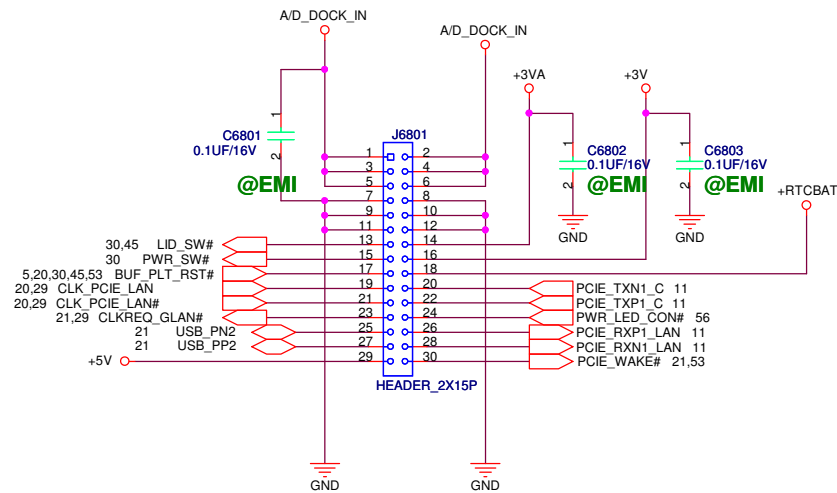


Tooling Hole L



Screw Hole O

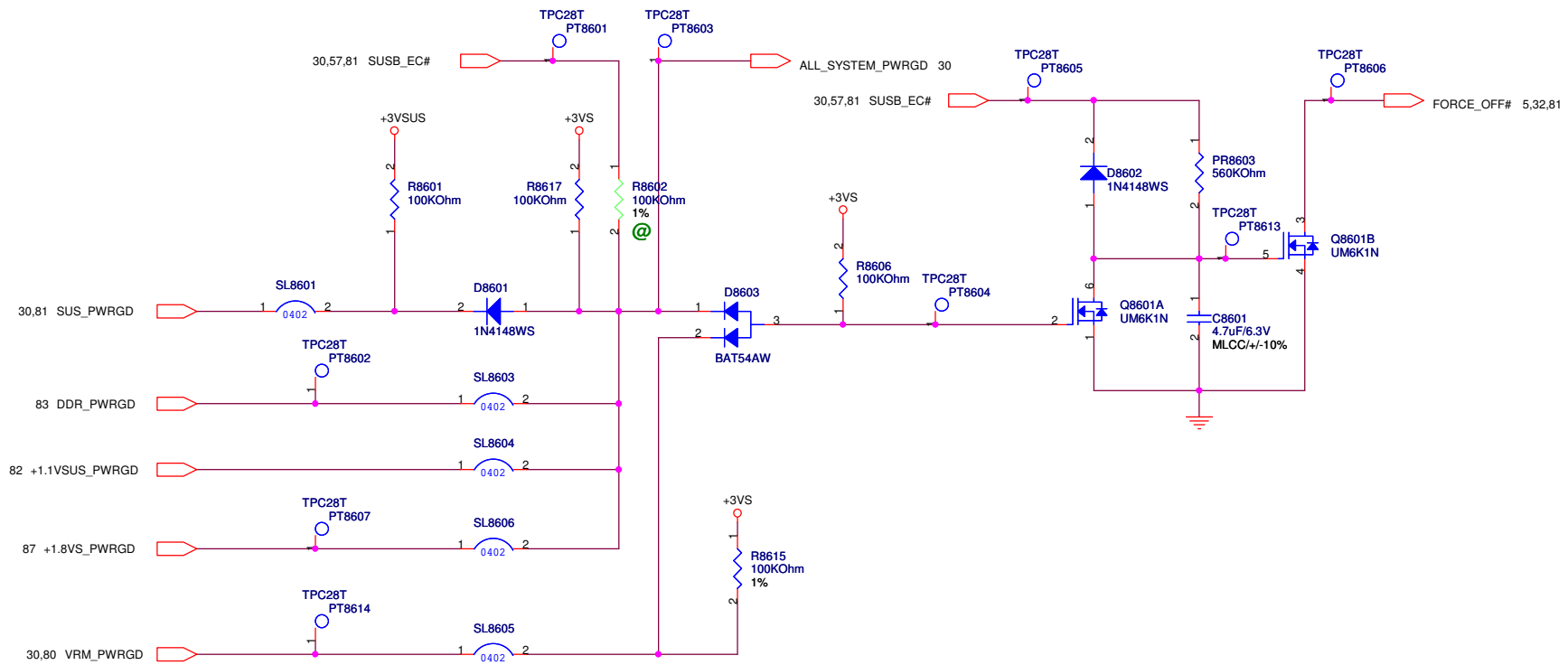




J6802 use PCB footprint of 12G061210401

<b>ASUS</b>		<b>Title :IO Connector</b>	
ASUSTeK COMPUTER INC. NB4		Engineer: Vincent_Chiang	
Size B	Project Name <b>K52N</b>	Rev 1.0	
Date: Monday, February 08, 2010		Sheet	68 of 99

## POWER GOOD DETECTOR

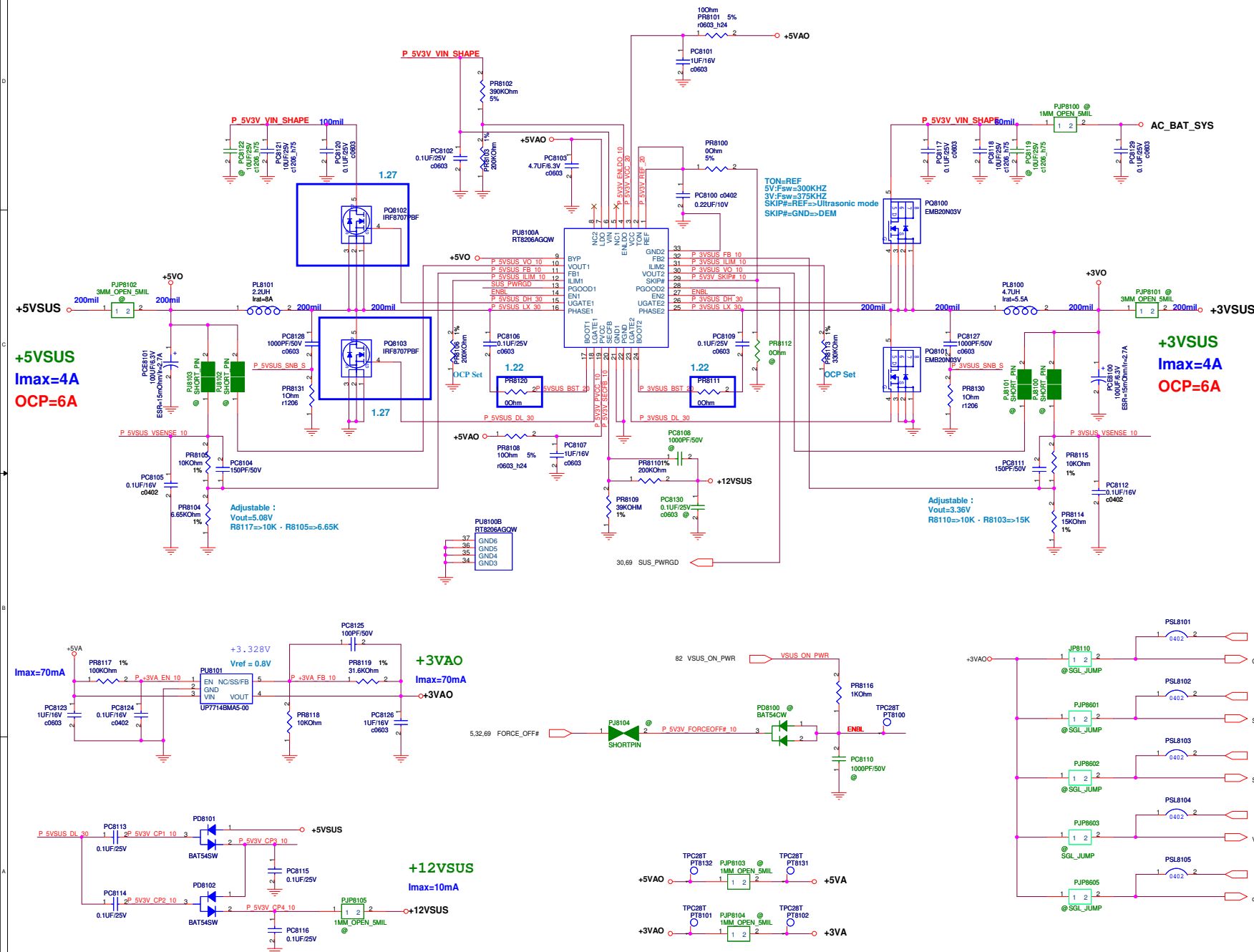


<Variant Name>

<b>ASUS</b>		<b>Title : GOOD_DETECTOR</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Vincent_Chiang</i>	
Size B	Project Name		Rev 1.0
Date: Monday, February 08, 2010		Sheet 69 of 95	

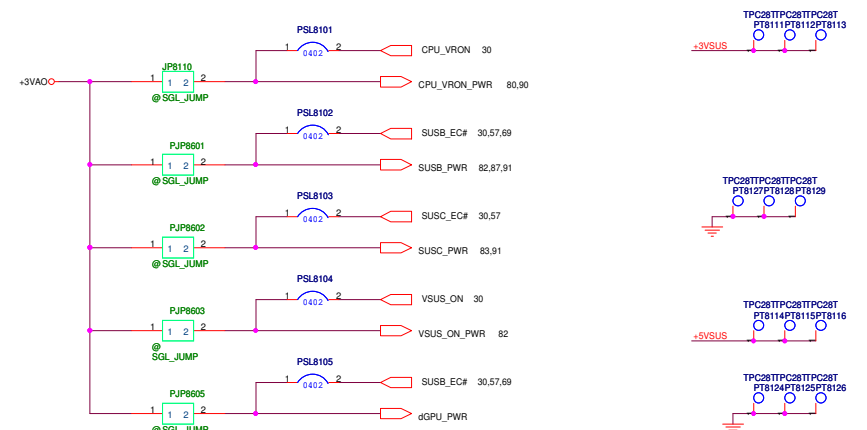


## +5VSUS / +3VSUS POWER SUPPLY

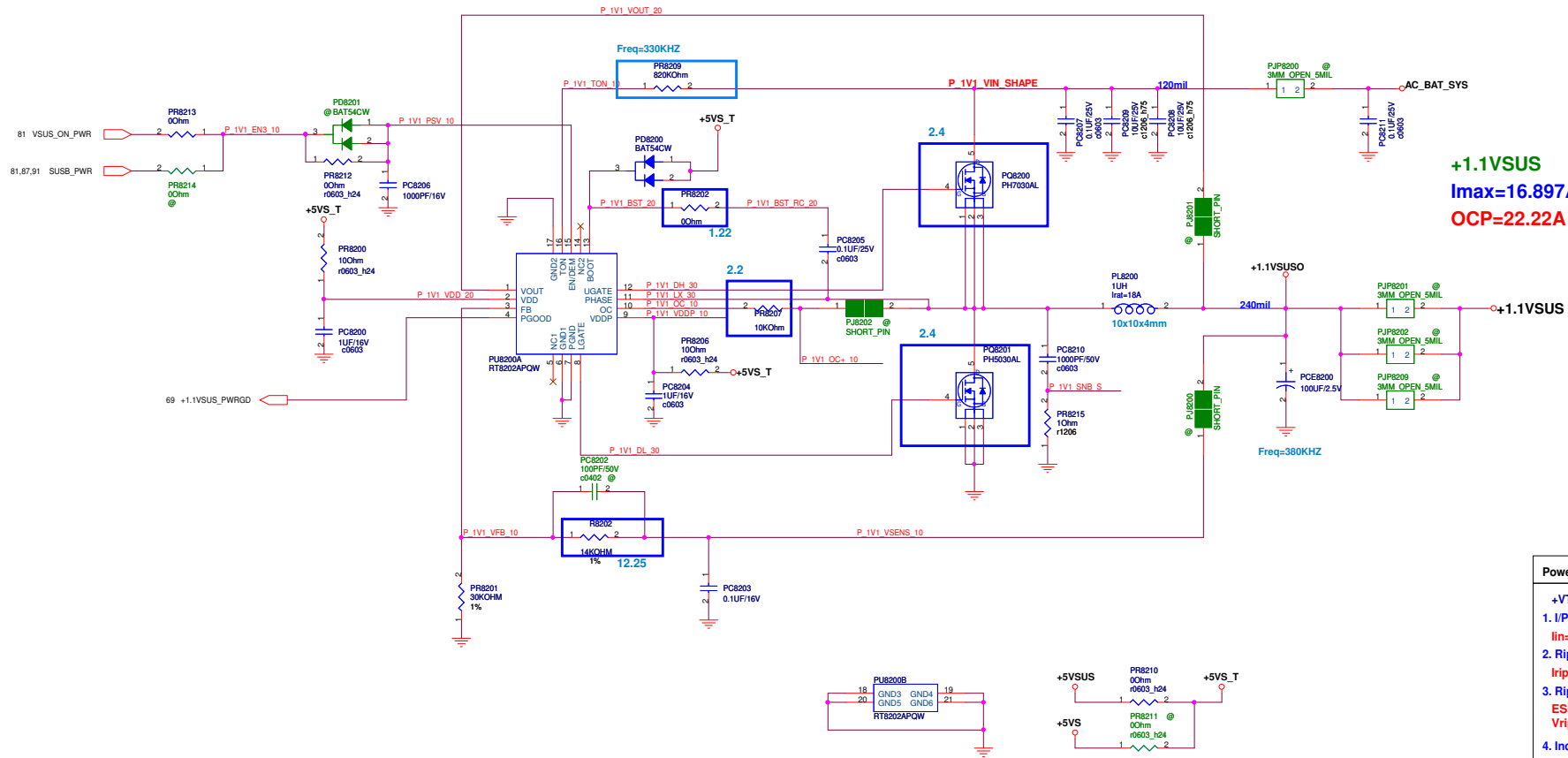


Power stage	
<b>+5VSUS:</b>	<b>+3VSUS:</b>
1. I/P Current: $I_{in} = V_o^* I_o / (0.75 * V_{in}) = 2.96A$	1.I/P Current: $I_{in} = V_o^* I_o / (0.75 * V_{in}) = 1.96A$
2. Ripple Current: $I_{rip} = 2.61A$	2.Ripple Current: $I_{rip} = 1.55A$
3. Ripple Voltage: $ESR / I = 15mohm$ $V = 39.15mV$	3.Ripple Voltage: $ESR / I = 15mohm$ $V = 23.25mV$
4. Inductor Spec:	4.Inductor Spec:
$I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36mohm$	$I_{sat} = 6.2A$ $I_{dc} = 4.6A$ $DCR = 36mohm$
<b>5.MOSFET Spec:</b>	
<b>H-side MOSFET: FDMC8884</b>	
$R_{ds}(ON) = 30mohm$ $I_{cont} = 9A$ $I_{peak} = 15A$	$(V_{gs} = 4.5 V)$ $(T = 25 ^\circ C)$ $(Pause = 10 us)$
<b>L-side MOSFET: FDMC8884</b>	
$R_{ds}(ON) = 30mohm$ $I_{cont} = 9A$ $I_{peak} = 15A$	$(V_{gs} = 4.5 V)$ $(T = 25 ^\circ C)$ $(Pause = 10 us)$

Controller	
+5VSUS:	+3.VSUS
1. Voltage & Current: +5VSUS: 5V / 4A	1.Voltage & Current: +3VSUS: 3.3V / 4A
2.Frequency: F=300KHZ	2.Frequency: F=375KHZ
3. OCP: Set PR8106=357 Kohm Iocp=5uA*Rocp/10*Rds(on) Iocp=6A	3.OCP: Set PR8113=357Kohm Iocp=5uA*Rocp/10*Rds(on) Iocp=6A
4. Soft start time: The Soft Start duration is 2ms	
5.Inrush Current: C total = 100 uF I inrush=C*Vout/SS_time I inrush= 0.25 A	4.Inrush Current: C total = 100 uF I inrush=C*Vout/SS_time I inrush= 0.165 A



# +1.1VSUS POWER SUPPLY

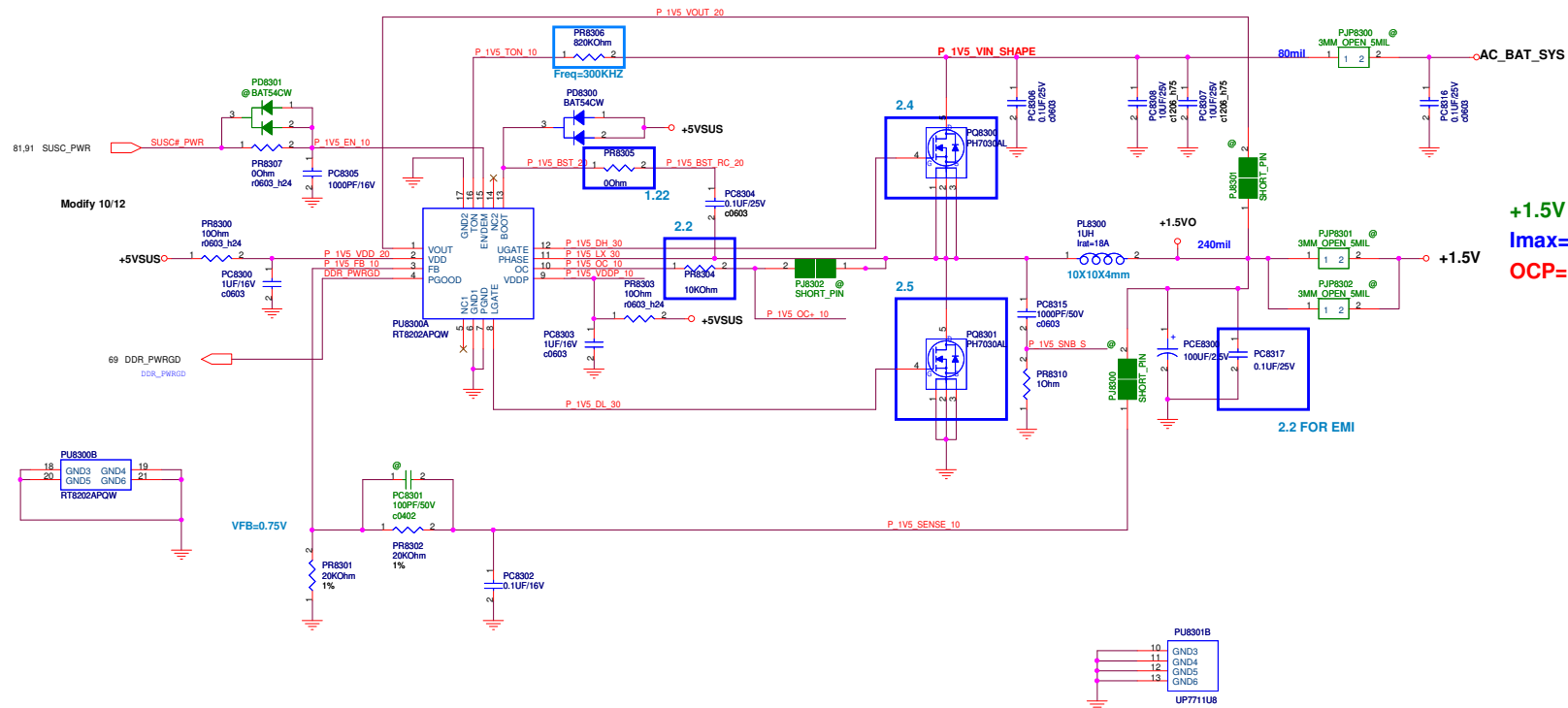


**+1.1VSUS**  
**I<sub>max</sub>=16.897A**  
**OCP=22.22A**

- Controller**
- +VTT\_CPU:**  
 1. Voltage & Current:  
 +VTT\_CPU: 1.05V / 15A
  - Frequency:**  
 F=330KHZ
  - OCP:**  
 Set PR8207=4.99 Kohm  
 I<sub>ocp</sub>=R<sub>ocp</sub>\*20uA/R<sub>ds(on)</sub>  
 I<sub>ocp</sub>=26A
  - Soft start time:**  
 The SS duration is 1.35ms
  - Inrush Current:**  
 C total = 440 uF  
 I<sub>inrush</sub>=C\*V<sub>out</sub>/SS\_time  
 I<sub>inrush</sub>= 0.342 A

- Power stage**
- +VTT\_CPU:**  
 1. I/P Current:  
 I<sub>in</sub>=V<sub>o</sub>/I<sub>o</sub>/(0.75\*V<sub>in</sub>)=2.33A
  - Ripple Current:**  
 I<sub>rip</sub>=5.36A
  - Ripple Voltage:**  
 ESR/2=7.5mohm  
 V<sub>ripple</sub>=40.26mV
  - Inductor Spec:**  
 I<sub>sat</sub>=40A  
 I<sub>dc</sub>=25A  
 DCR=1.6mohm
  - MOSFET Spec:**  
 H-side MOSFET: RJK0355DPA  
 R<sub>ds(ON)</sub>=16.5mohm (V<sub>gs</sub>=4.5 V)  
 I<sub>cont</sub> = 30A (T=25 °C)  
 I<sub>peak</sub> = 120 A (Pause ≥10 us)  
 L-side MOSFET: RJK0353DPA  
 R<sub>ds(ON)</sub>=7.6mohm (V<sub>gs</sub>=4.5 V)  
 I<sub>cont</sub> = 35A (T=25 °C)  
 I<sub>peak</sub> = 140 A (Pause ≥10 us)

# +1.5V & +0.75VS POWER SUPPLY



Power stage

DDR III:

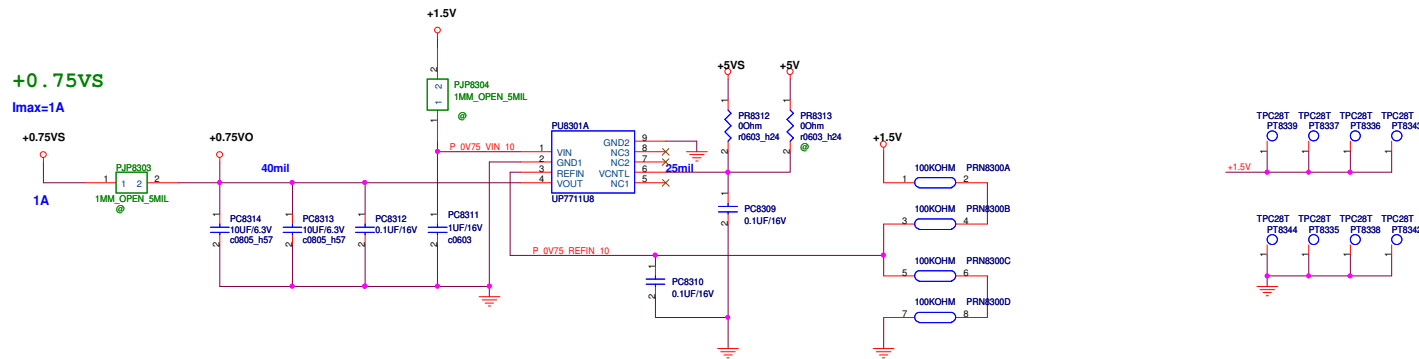
1. I/P Current:  
 $I_{in} = V_o / I_o (0.75 \cdot V_{in}) = 2.22A$

2. Ripple Current:  
 $I_{rip} = 4.62A$

3. Ripple Voltage:  
 $ESR / 1 = 15mohm$   
 $V = 69.3mV$

4. Inductor Spec:  
 $I_{sat} = 12.7A$   
 $I_{dc} = 9.5A$   
 $DCR = 8.5mohm$

5. MOSFET Spec:  
H-side MOSFET: RJK0355DPA  
 $R_{ds(ON)} = 16.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 120A$  (Pause = 10 us)  
L-side MOSFET: RJK0355DPA  
 $R_{ds(ON)} = 16.5mohm$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 120A$  (Pause = 10 us)



Controller

DDR III:

1. Voltage & Current:  
 $+1.5V: 1.5V / 10A$

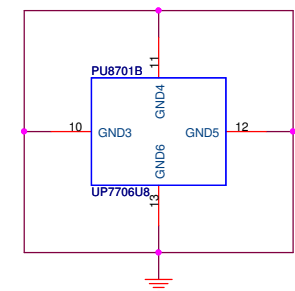
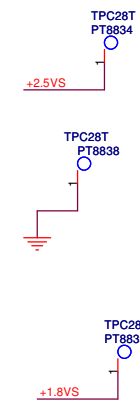
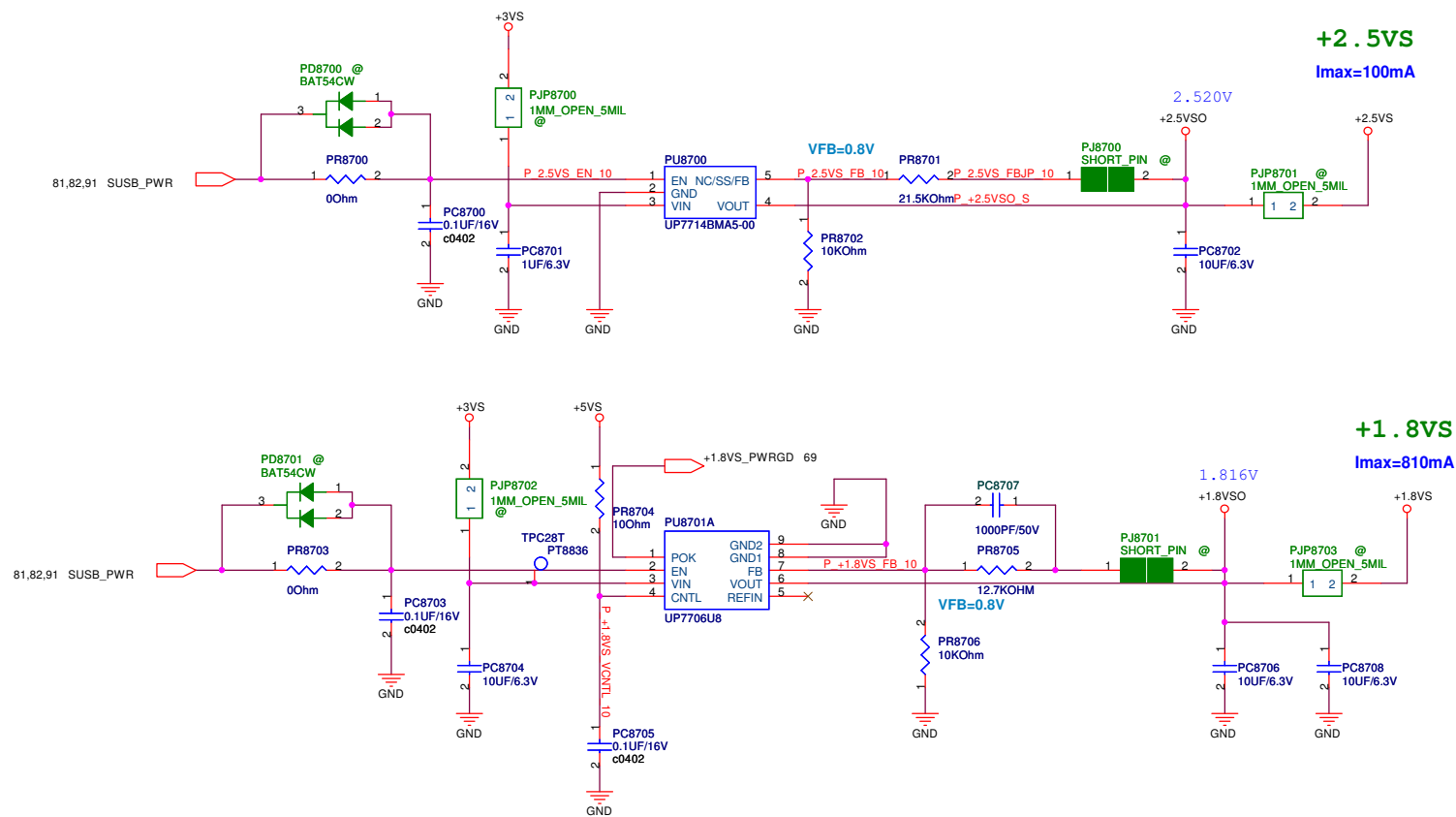
2. Frequency:  
 $F = 300KHZ$

3. OCP:  
Set R8302 = 12 Kohm  
 $I_{ocp} = R_{ocp} \cdot 20uA / R_{ds(on)}$   
 $I_{ocp} = 14.3A$

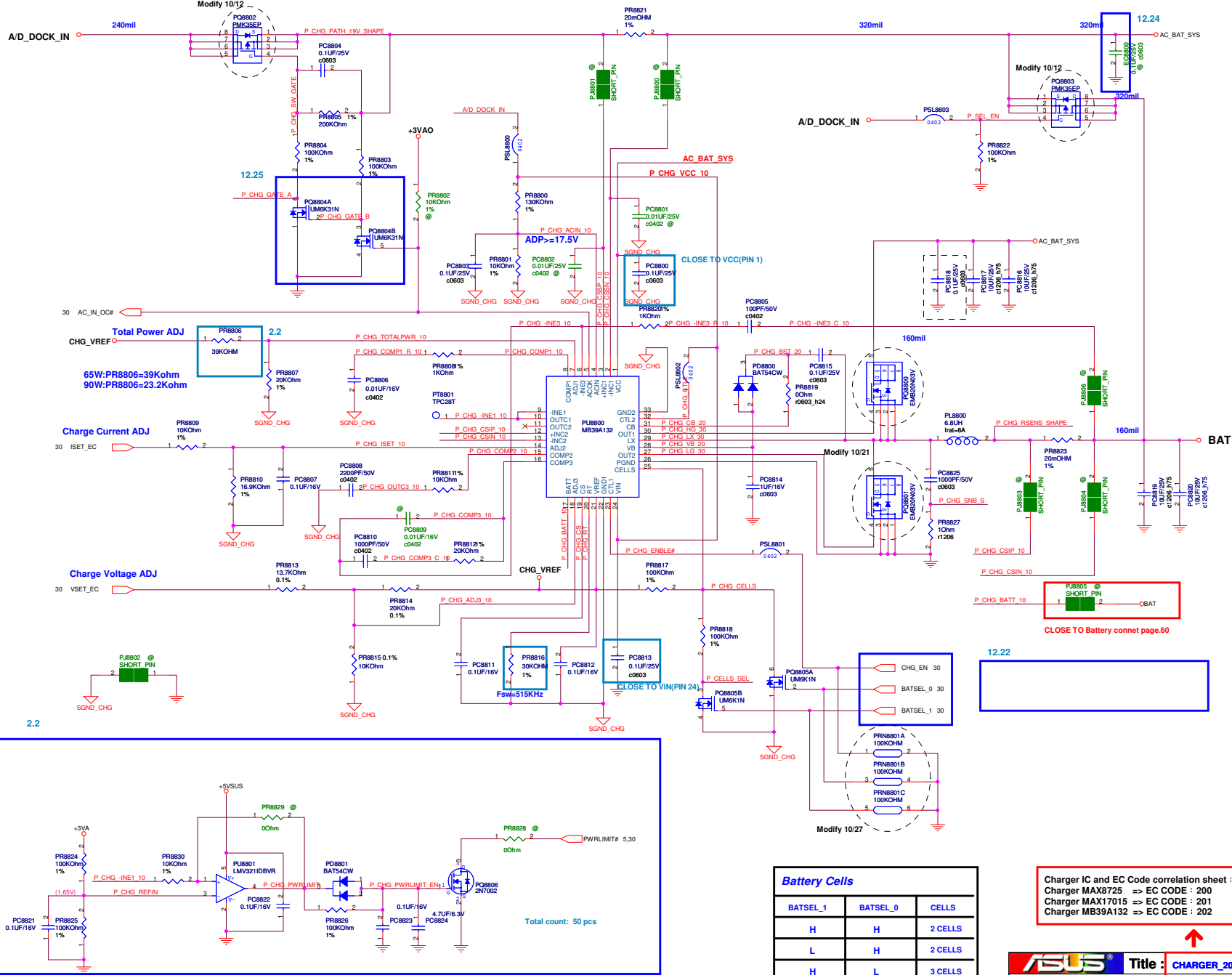
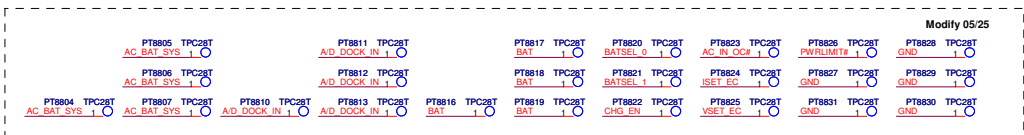
4. Soft start time:  
The Soft Start duration is 1.35ms

5. Inrush Current:  
 $C_{total} = 220uF$   
 $I_{inrush} = C \cdot V_{out} / SS\_time$   
 $I_{inrush} = 0.244A$

1. Voltage & Current:  
 $+0.75V: 0.75V / 1A$







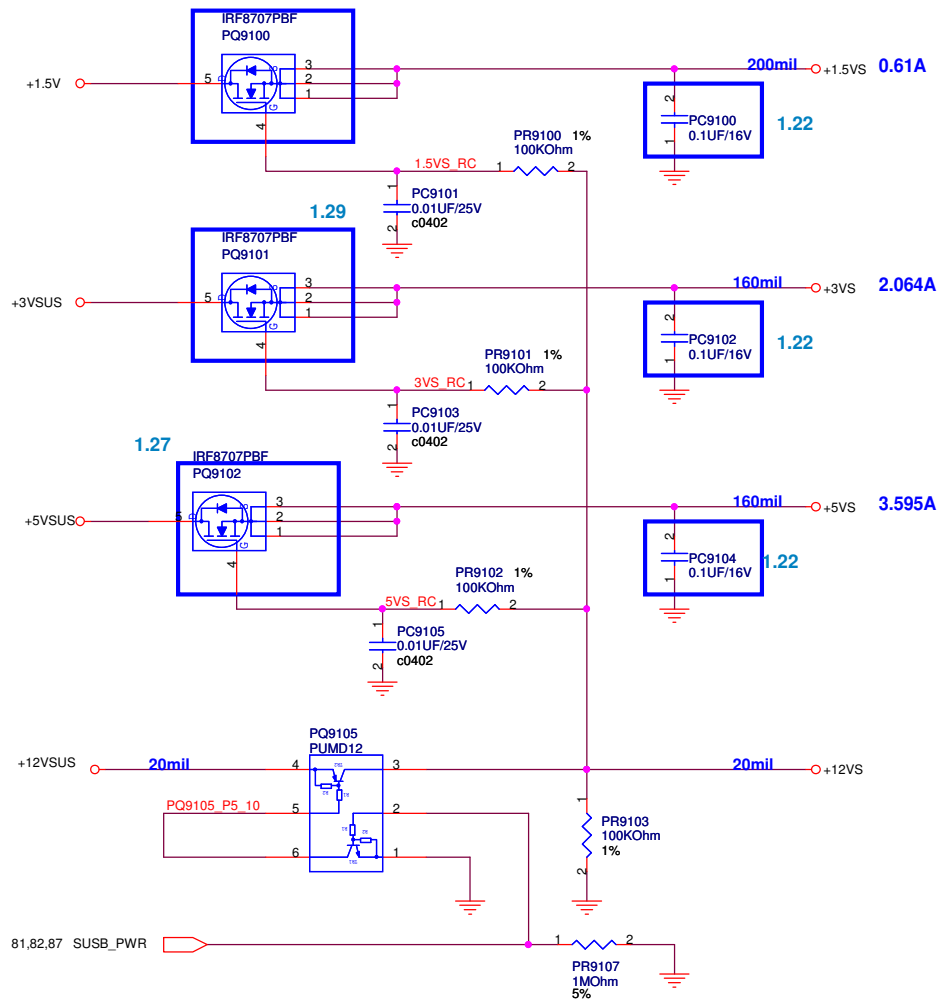
**Battery Cells**

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

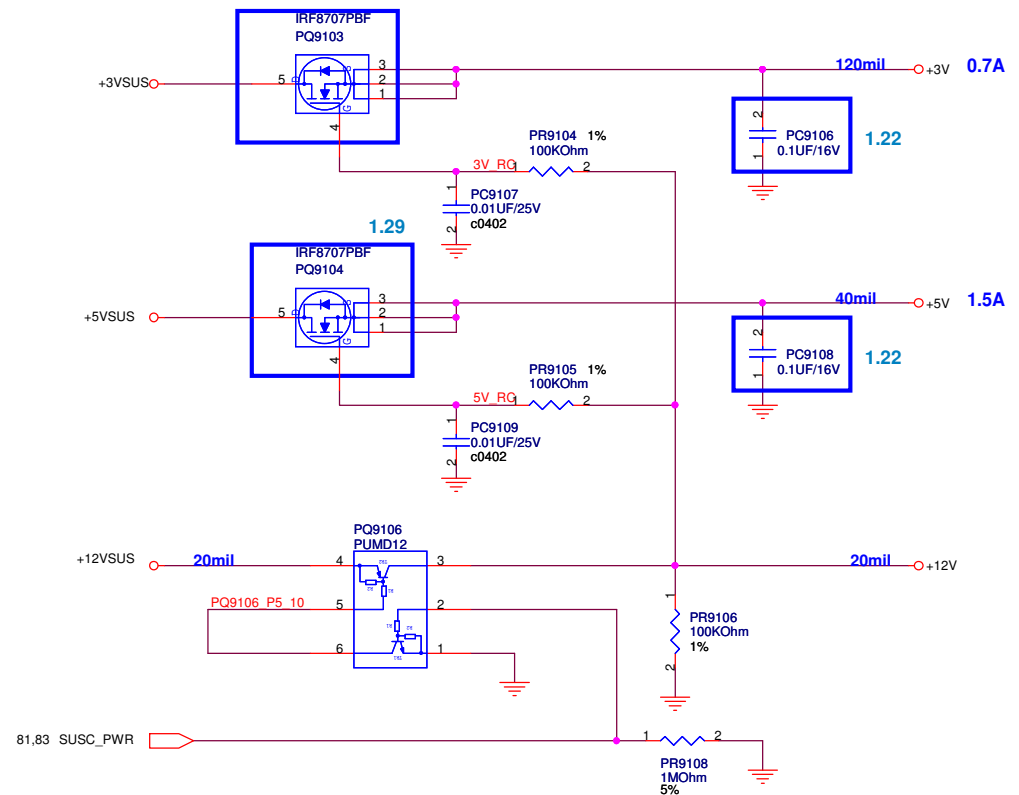
Charger IC and EC Code correlation sheet :  
 Charger MAX8725 => EC CODE : 200  
 Charger MAX17015 => EC CODE : 201  
 Charger MB39A132 => EC CODE : 202



## SUSB\_PWR POWER 1.29



## SUSC\_PWR POWER 1.29



<Variant Name>

<b>ASUS</b>		<b>Title : POWER_LOAD SWITCH</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <b>Matt_Wang</b>	
Size B	Project Name <b>Design_IP</b>		Rev 1.0
Date: <b>Monday, February 08, 2010</b>		Sheet <b>91</b> of <b>95</b>	