Compal Confidential

QCL40 MB Schematic Document

LA-8221P

Rev: 0.2

2011.09.28

Security Classification	Compal Secret Data		
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Title: *Cover Sheet*

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QCL40

ZZZ1
PCB-MB
PCB P/N for Load BOM

NV N13P-GL
(N13M-GE1)
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PEG 16X

Mobile
Ivy Bridge
Processor
rPGA 988B Socket
Page 4 ~ 9
+VCC_CORE, +VCCP,
+VCC_GFXCORE_AVG, +1.5V_CPU_VDDQ,
+1.8VS, _VCCSA

DDR3 1333/1600MHz 1.5V
Dual Channel

DDR3-SO-DIMM X 2
BANK 0, 1, 2, 3
+1.5V, +0.75VS
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FDI x8
(UMA)
100MHz
2.7GT/s

DMI x4
100MHz
5GB/s

LCD conn
Page 30
LVDS, EDID, DISPOFF#, PWM

CRT Conn
Page 30
RGB, HV Sync, DDC

HDMI
Page 35
HDMI, DDC

Intel
PANTHER-POINT
PCH

HM77

FCBGA 989 Balls

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+1.05VS, +1.8VS, +3VS,
+3V_PCH, +5V_PCH, +RTCVCC,
+VCCAFDI_VRM

USB2.0

port 4
USB conn x1
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port 8
Camera
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Card Reader
RTS5137 Page 34

Memory Card Slot
SD/MMC
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MiniCard-2
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Realtek
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Audio Jack (HP)
Page 33

Audio Jack (MIC)
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Speaker Connector
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SATA

port 0
2.5" SATA HDD Connector
Page 31

port 2
SATA ODD Connector
Page 31

SPI

SPI ROM
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Page 12

PCI-e

port 1
LAN/CRT Board
10/100/1000 LAN
Realtek GbE
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port 2
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WLAN
Bluetooth
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LPC BUS

Touch Pad CONN.
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ENE KB9012QF
Reserve KB930F
+3VLP/+3VALW page 39

Int. KBD
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SPI ROM
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External board

DC/DC Interface CKT.
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Fan Control
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Title: Block Diagram

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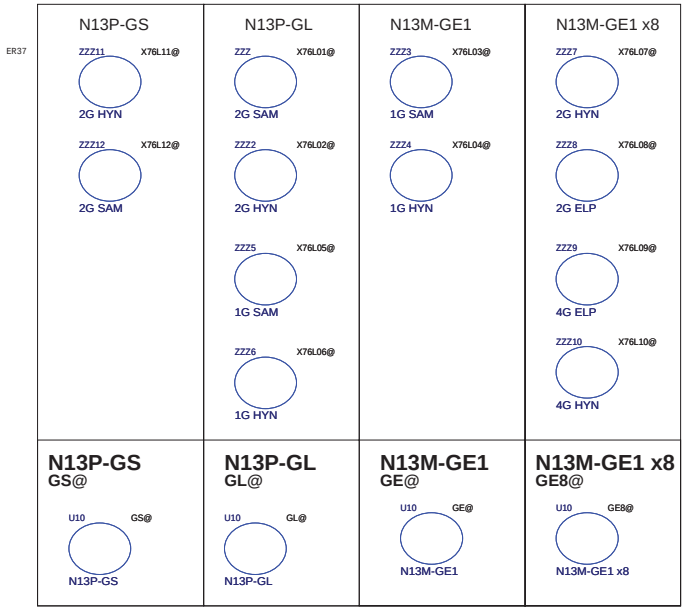
X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8



DIS@: VGA componet
GEL@: N13P-GL or N13M-GE1
GSL@: N13P-GL or N13P-GS
GS@: N13P-GS

9012@: EC(ENE 9012 chip)

930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

	USB3 PORT	DESTINATION
PCH	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

	USB2 PORT	DESTINATION
PCH	0	USB2.0+3.0
	1	USB2.0+3.0
	2	None
	3	None
	4	JMINI1 (WLAN) Bluetooth
	5	None
	6	None
	7	None
	8	CAMERA
	9	USB2
	10	Card Reader
	11	None
	12	None
	13	None

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 51ON power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: Notes List

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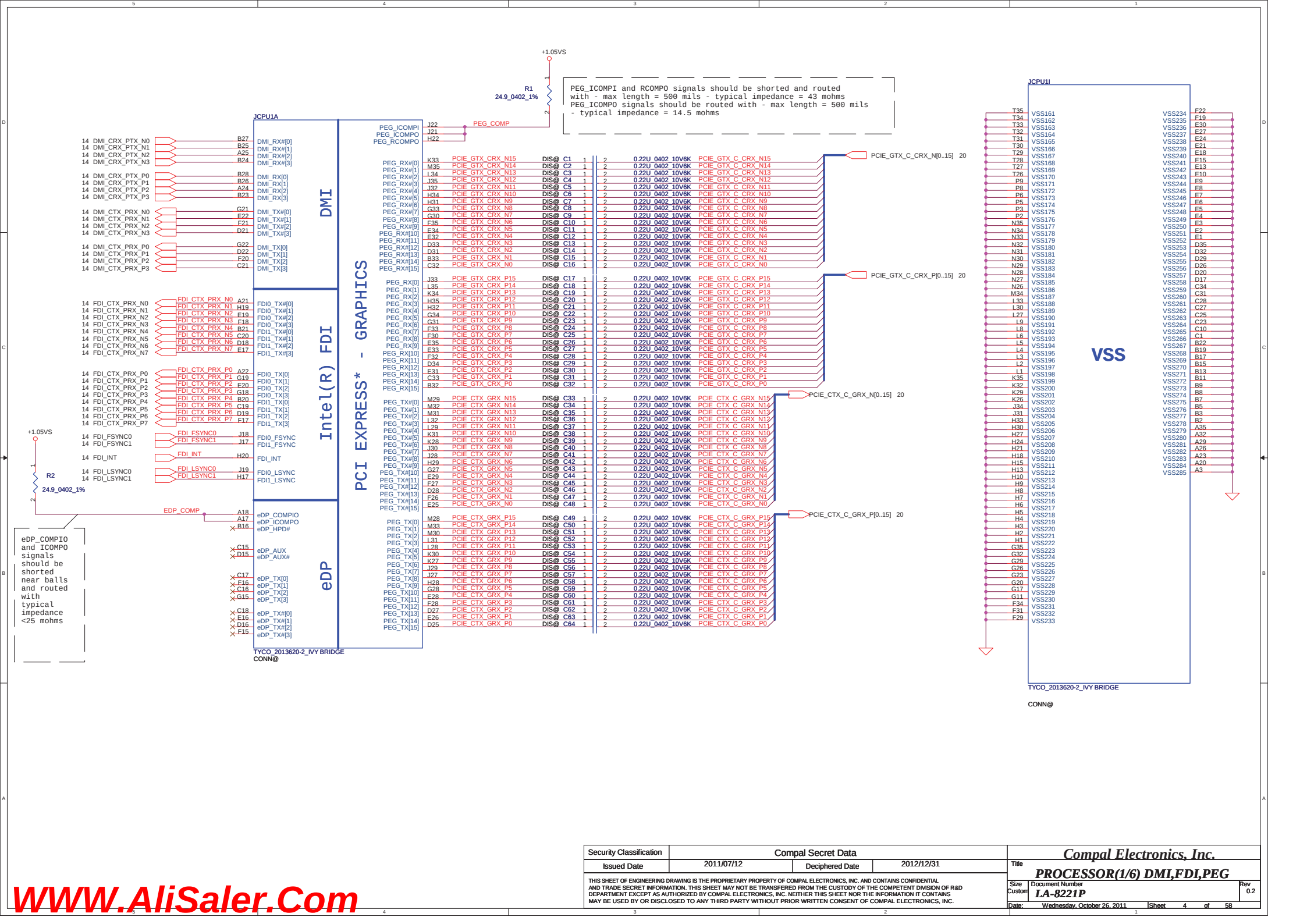

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Title: PROCESSOR(1/6) DMI,FDI,PEG

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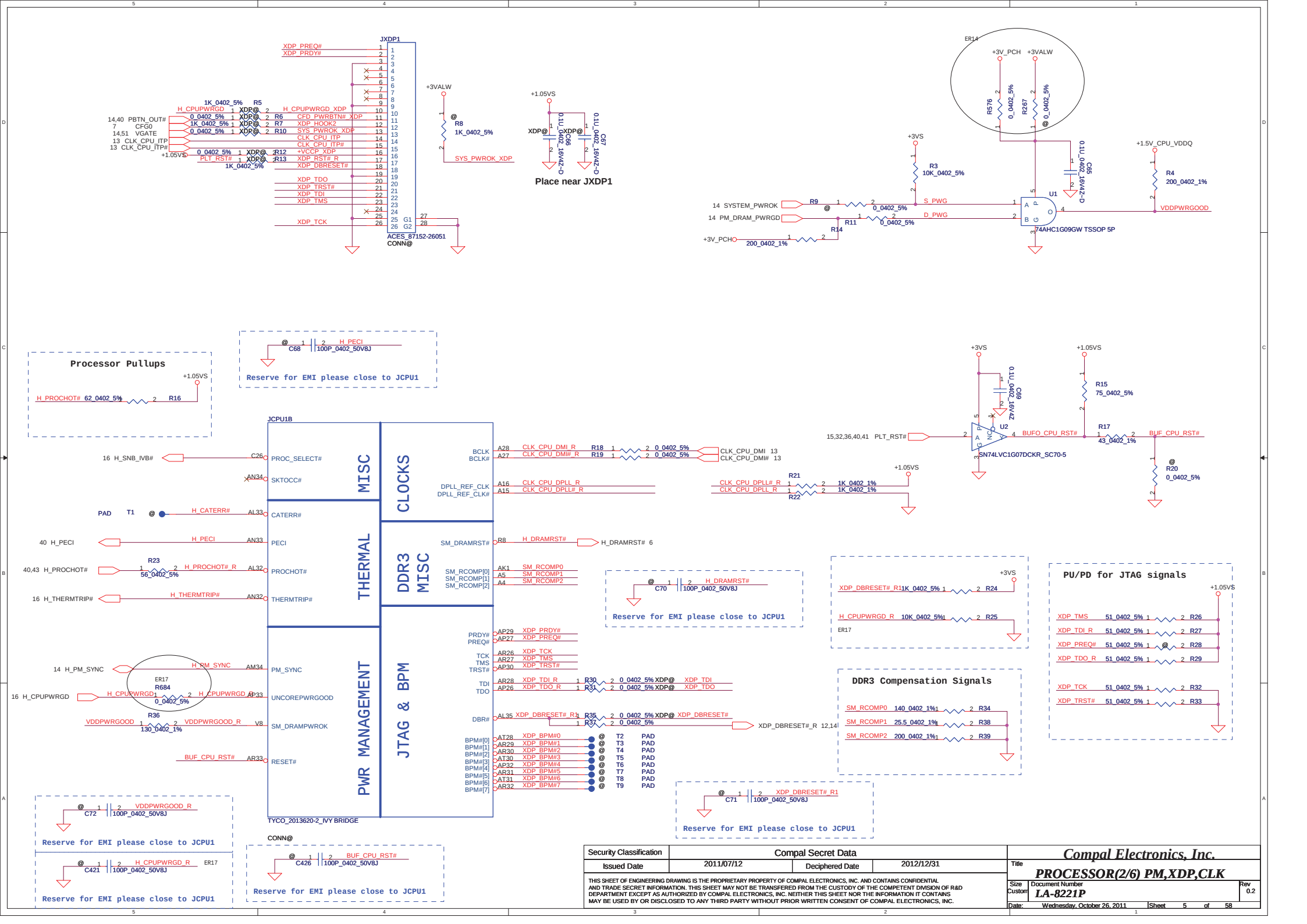

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Title: PROCESSOR(2/6) PM,XDP,CLK

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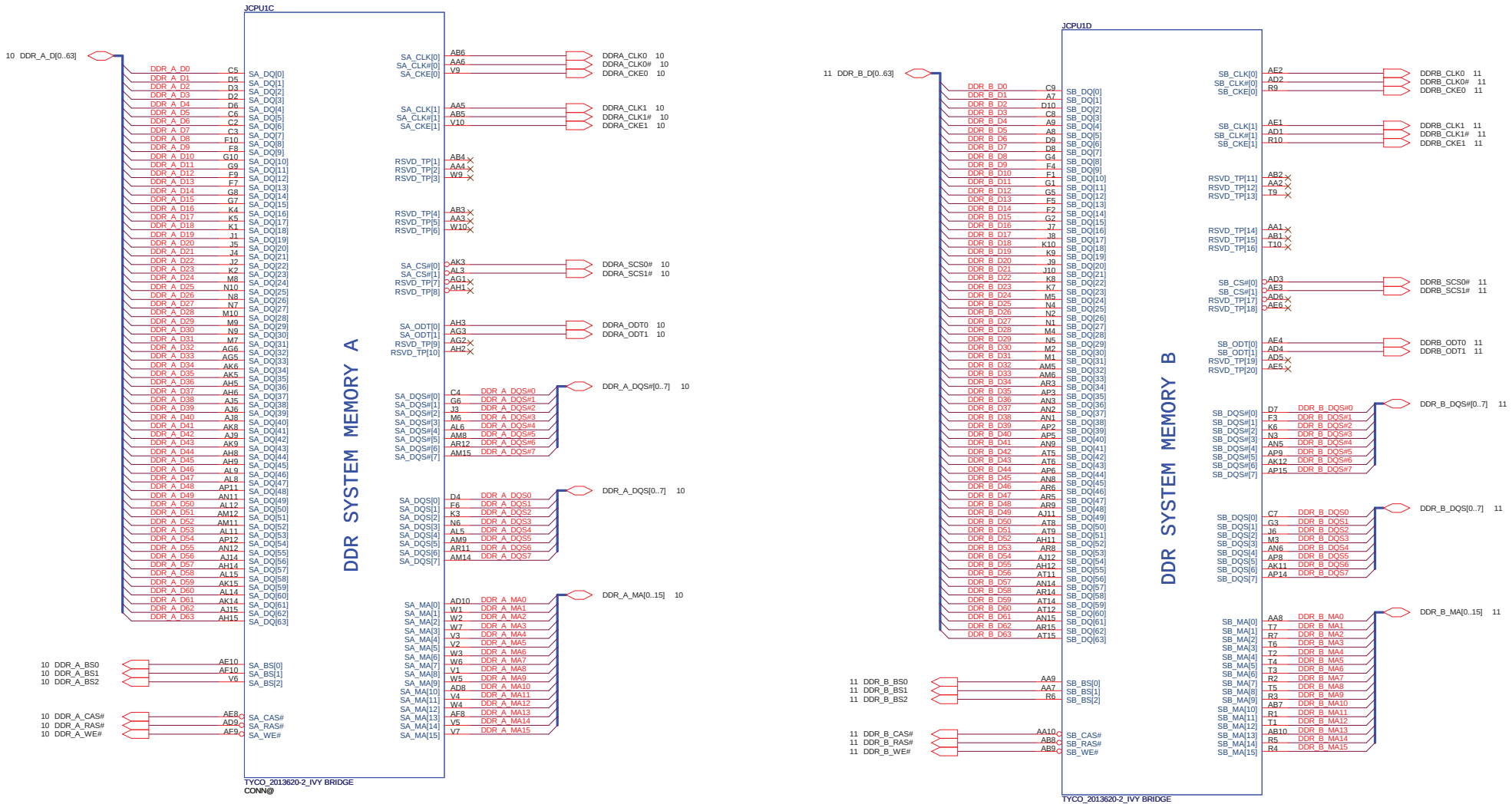

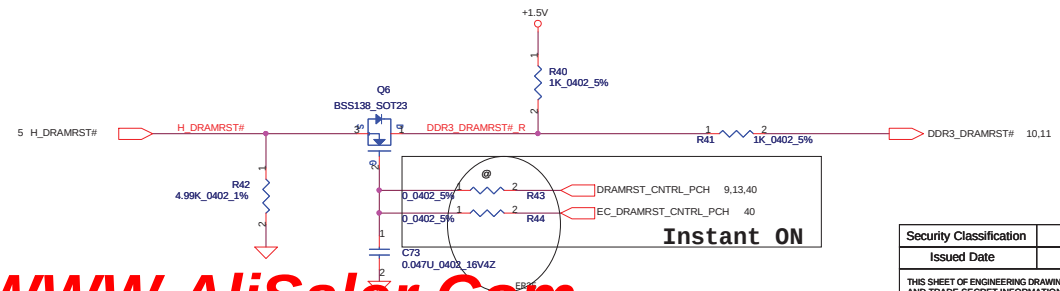

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Title: PROCESSOR(3/6) DDRIII

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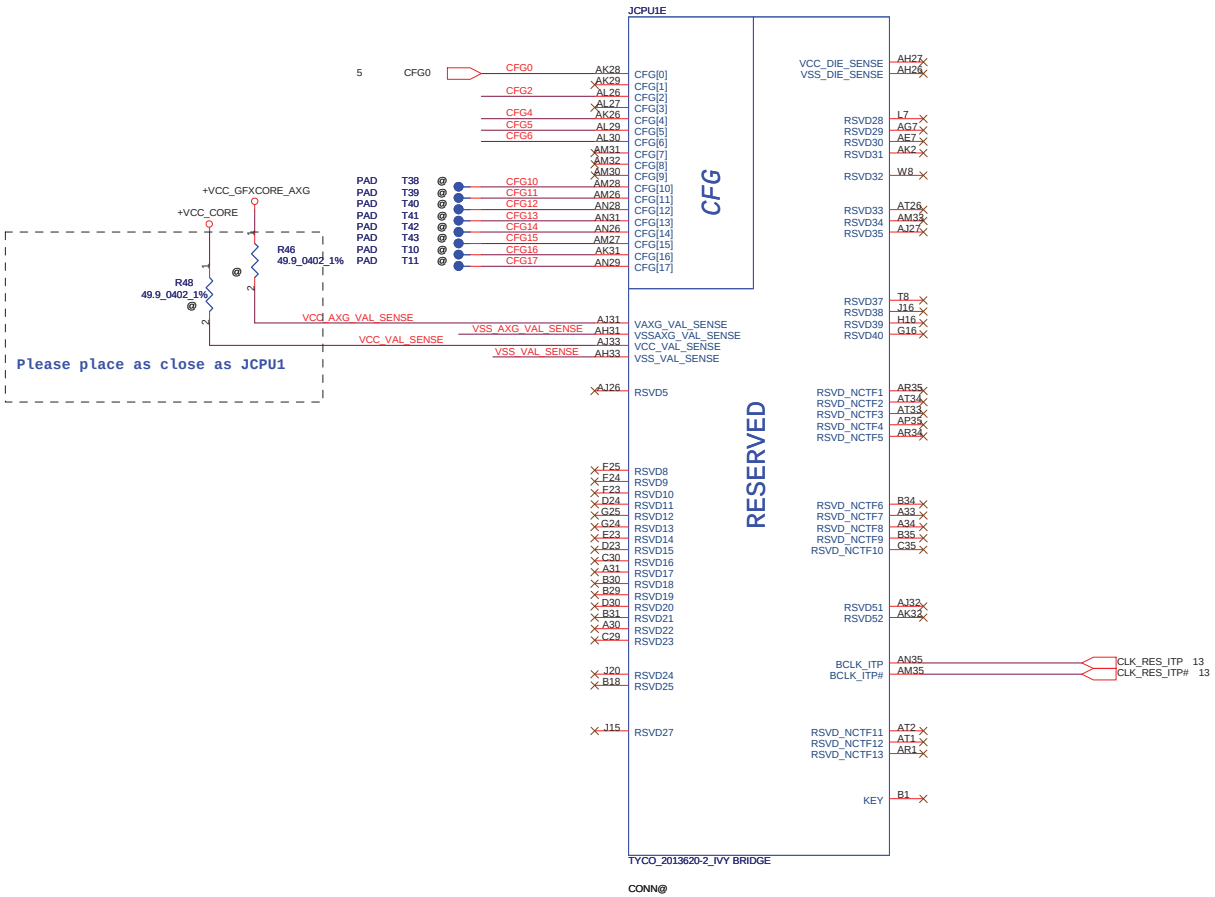
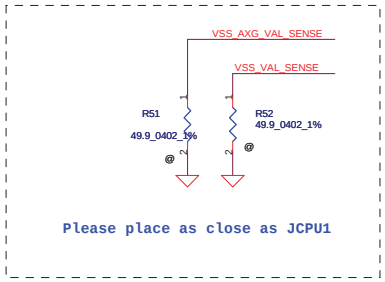
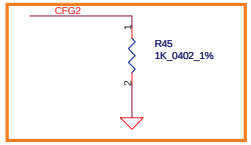
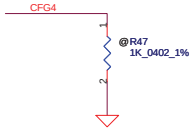
CFG Straps for Processor



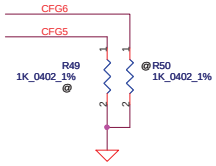




PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Title: PROCESSOR(4/6) RSVD,CFG

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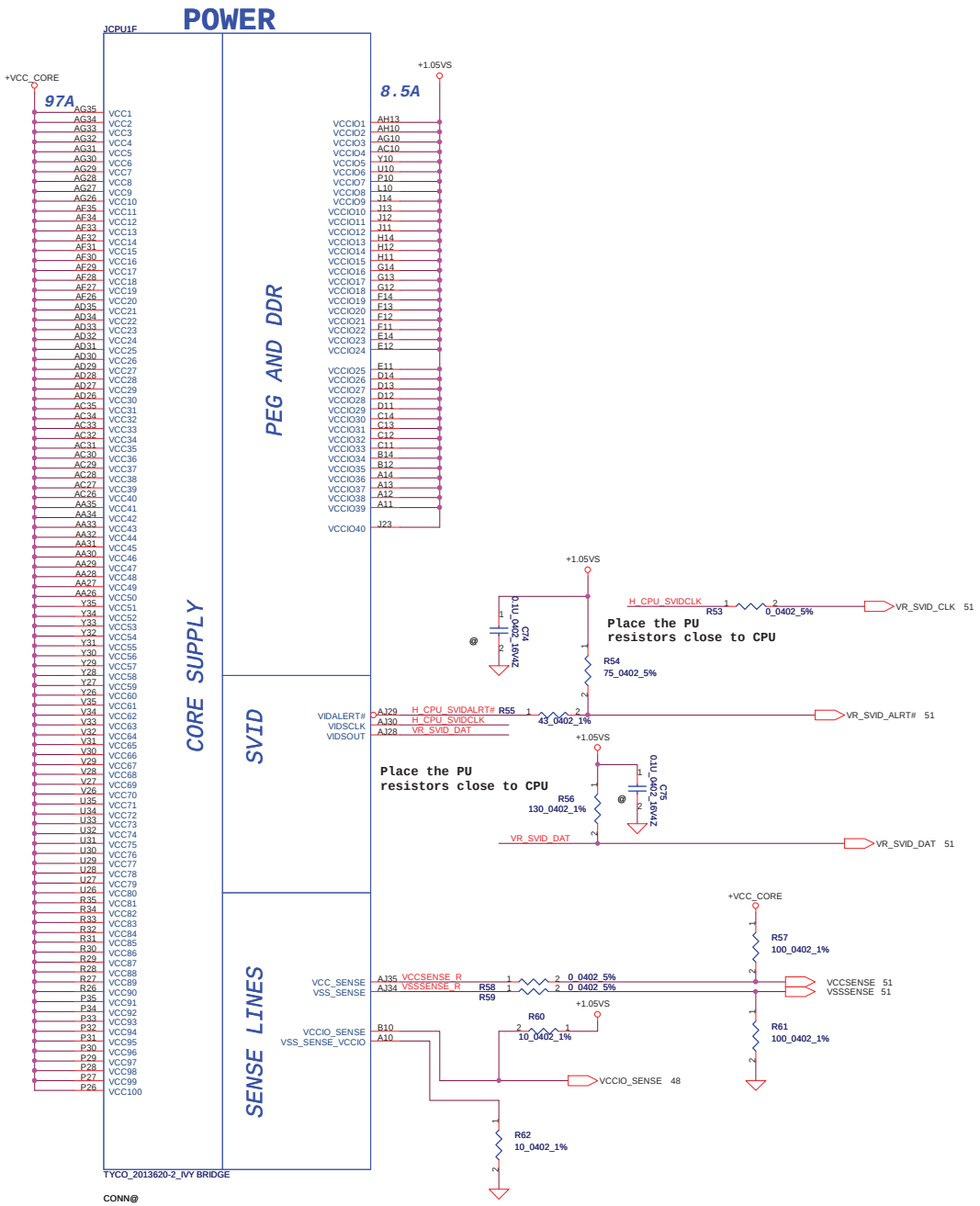

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Title: PROCESSOR(5/6) PWR,BYPASS

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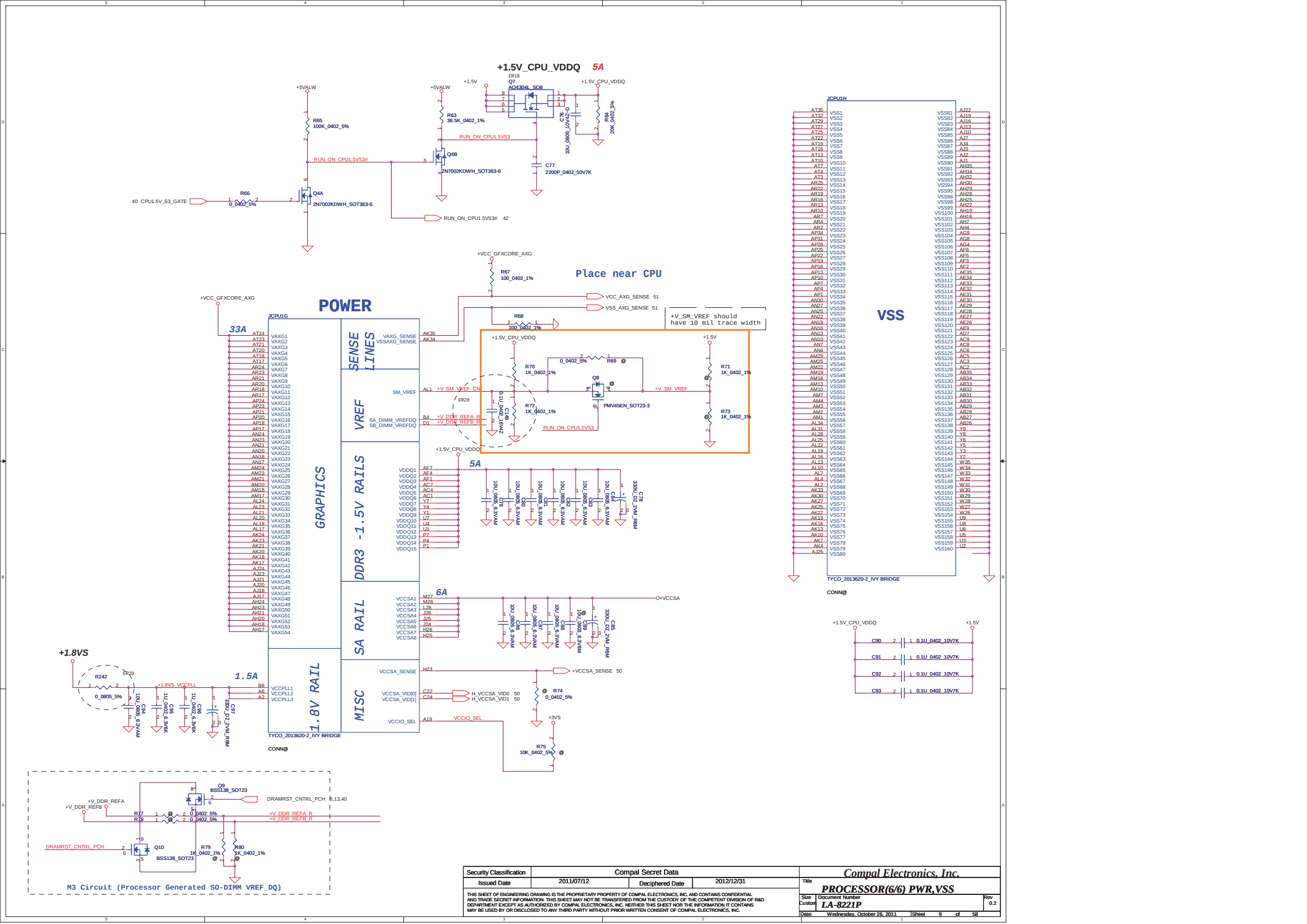

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Title: PROCESSOR(6/6) PWR,VSS

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3.56A

DDR3 SO-DIMM A

JDIMM1

+1.5V

R81 1K_0402_1%

R82 1K_0402_1%

+V_DDR_REFA

ER12

C98 0.1U_0402_10V6K

C89 2.2U_0402_6.3V6M

6 DDR_A_D[0..63]
6 DDR_A_DQS[0..7]
6 DDR_A_DQS#[0..7]
6 DDR_A_MA[0..15]

1	VREF_DQ	VSS1	2
3	VSS2	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS3	8
9	VSS4	DQS#0	10
11	DM0	DQS0	12
13	VSS5	DQ6	14
15	DQ2	DQ7	16
17	DQ3	VSS8	18
19	VSS7	DQ12	20
21	DQ8	DQ13	22
23	DQ9	VSS10	24
25	VSS9	DM1	26
27	DQS#1	RESET#	28
29	DQS1	VSS12	30
31	VSS11	DQ14	32
33	DQ10	DQ15	34
35	DQ11	VSS14	36
37	VSS13	DQ20	38
39	DQ16	DQ21	40
41	DQ17	VSS16	42
43	VSS15	DM2	44
45	DQS#2	VSS17	46
47	DQS2	DQ22	48
49	VSS18	DQ23	50
51	DQ18	VSS19	52
53	DQ19	DQ28	54
55	VSS20	DQ29	56
57	DQ24	VSS21	58
59	DQ25	DQS#3	60
61	VSS22	DQS3	62
63	DM3	VSS24	64
65	VSS23	DQ30	66
67	DQ26	DQ31	68
69	DQ27	VSS26	70
71	VSS25		72
73	CKE0	CKE1	74
75	VDD1	VDD2	76
77	NC1	A15	78
79	BA2	A14	80
81	VDD3	VDD4	82
83	A12/BC#	A11	84
85	A9	A7	86
87	VDD5	VDD6	88
89	A8	A6	90
91	A5	A4	92
93	VDD7	VDD8	94
95	A3	A2	96
97	A1	A0	98
99	VDD9	VDD10	100
101	CK0	CK1	102
103	CK0#	CK1#	104
105	VDD11	VDD12	106
107	A10/AP	BA1	108
109	BA0	RAS#	110
111	VDD13	VDD14	112
113	WE#	S0#	114
115	CAS#	ODT0	116
117	VDD15	VDD16	118
119	A13	ODT1	120
121	S1#	NC2	122
123	VDD17	VDD18	124
125	NCTEST	VREF_CA	126
127	VSS27	VSS28	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS29	VSS30	134
135	DQS#4	DM4	136
137	DQS4	VSS31	138
139	VSS32	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS33	144
145	VSS34	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS35	150
151	VSS36	DQS#5	152
153	DM5	DQS5	154
155	VSS37	VSS38	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS39	VSS40	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS41	VSS42	168
169	DQS#6	DM6	170
171	DQS6	VSS43	172
173	VSS44	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS45	178
179	VSS46	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS47	184
185	VSS48	DQS#7	186
187	DM7	DQS7	188
189	VSS49	VSS50	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS51	VSS52	196
197	SA0	EVENT#	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT1	VTT2	204
205	G1	G2	206

TYCO 2-1932323-1

DDR_A_D0, DDR_A_D1, DDR_A_D2, DDR_A_D3, DDR_A_D4, DDR_A_D5, DDR_A_D6, DDR_A_D7, DDR_A_D8, DDR_A_D9, DDR_A_D10, DDR_A_D11, DDR_A_D12, DDR_A_D13, DDR_A_D14, DDR_A_D15, DDR_A_D16, DDR_A_D17, DDR_A_D18, DDR_A_D19, DDR_A_D20, DDR_A_D21, DDR_A_D22, DDR_A_D23, DDR_A_D24, DDR_A_D25, DDR_A_D26, DDR_A_D27, DDR_A_D28, DDR_A_D29, DDR_A_D30, DDR_A_D31, DDR_A_D32, DDR_A_D33, DDR_A_D34, DDR_A_D35, DDR_A_D36, DDR_A_D37, DDR_A_D38, DDR_A_D39, DDR_A_D40, DDR_A_D41, DDR_A_D42, DDR_A_D43, DDR_A_D44, DDR_A_D45, DDR_A_D46, DDR_A_D47, DDR_A_D48, DDR_A_D49, DDR_A_D50, DDR_A_D51, DDR_A_D52, DDR_A_D53, DDR_A_D54, DDR_A_D55, DDR_A_D56, DDR_A_D57, DDR_A_D58, DDR_A_D59, DDR_A_D60, DDR_A_D61, DDR_A_D62, DDR_A_D63

DDR_A_DQS#0, DDR_A_DQS0, DDR_A_DQS#1, DDR_A_DQS1, DDR_A_DQS#2, DDR_A_DQS2, DDR_A_DQS#3, DDR_A_DQS3, DDR_A_DQS#4, DDR_A_DQS4, DDR_A_DQS#5, DDR_A_DQS5, DDR_A_DQS#6, DDR_A_DQS6, DDR_A_DQS#7, DDR_A_DQS7

DDR3_DRAMRST# → DDR3_DRAMRST# 6,11

6 DDRA_CKE0 → DDRA_CKE0, DDRA_CKE1 → DDRA_CKE1 6

6 DDR_A_BS2 → DDR_A_BS2

DDR_A_MA12, DDR_A_MA9, DDR_A_MA8, DDR_A_MA5, DDR_A_MA3, DDR_A_MA1, DDR_A_MA15, DDR_A_MA14, DDR_A_MA11, DDR_A_MA7, DDR_A_MA6, DDR_A_MA4, DDR_A_MA2, DDR_A_MA0

6 DDRA_CLK0 → DDRA_CLK0, DDRA_CLK0#, DDRA_CLK1, DDRA_CLK1#
DDRA_CLK1 6
DDRA_CLK1# 6

6 DDR_A_BS0 → DDR_A_BS0, DDR_A_BS1, DDR_A_RAS#
DDR_A_BS1 6
DDR_A_RAS# 6

6 DDR_A_WE# → DDR_A_WE#, DDRA_SCS0#
6 DDR_A_CAS# → DDR_A_CAS#, DDRA_ODT0
DDRA_SCS0# 6
DDRA_ODT0 6

6 DDRA_SCS1# → DDRA_SCS1#, DDRA_ODT1
DDRA_ODT1 6

+1.5V

R83 1K_0402_1%

R84 1K_0402_1%

+VREF_CA

C108 0.1U_0402_10V6K

C109 2.2U_0402_6.3V6M

ER12

+3VS

C119 0.1U_0402_10V6K

C118 2.2U_0402_6.3V6M

R85 10K_0402_5%

R86 10K_0402_5%

PCH_SMBDATA, PCH_SMBCLK → PCH_SMBDATA 11,13,41, PCH_SMBCLK 11,13,41

+0.75VS

0.65A@0.75V

Layout Note: Place near JDDRL

+1.5V

C100 330U_B2_2.5V_M_R15M

C101 10U_0603_6.3V6M

C102 10U_0603_6.3V6M

C103 10U_0603_6.3V6M

C104 10U_0603_6.3V6M

C105 10U_0603_6.3V6M

C106 10U_0603_6.3V6M

C107 10U_0603_6.3V6M

Layout Note: Place these 4 Caps near Command and Control signals of JDDRL

+1.5V

C110 1U_0402_6.3V6K

C111 1U_0402_6.3V6K

C112 1U_0402_6.3V6K

C113 1U_0402_6.3V6K

Layout Note: Place near JDDRL.203,204

+0.75VS

C114 1U_0402_6.3V6K

C115 1U_0402_6.3V6K

C116 1U_0402_6.3V6K

C117 1U_0402_6.3V6K

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Title: DDRIII-DDRL

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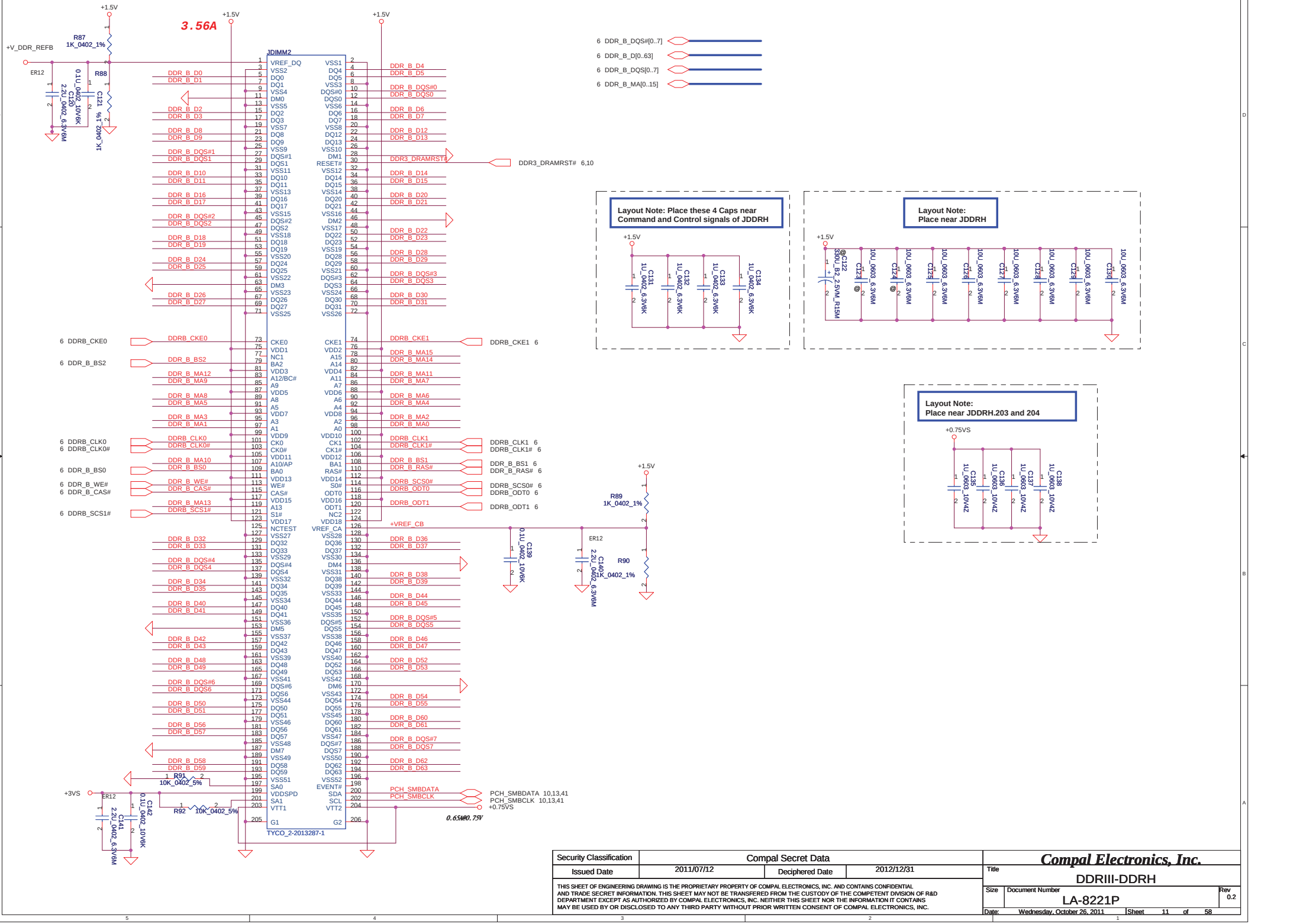

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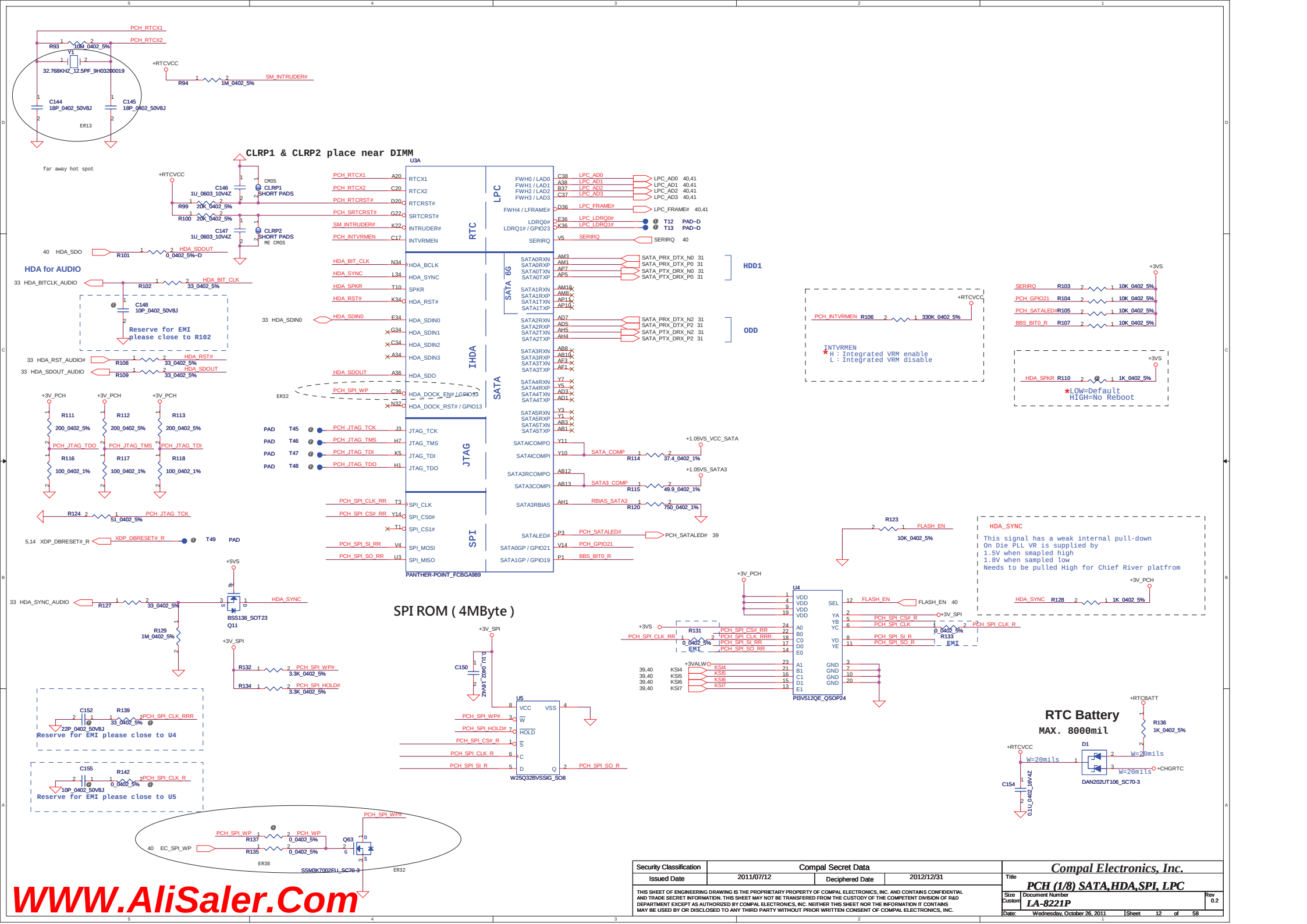
Title	DDRIII-DDRH	
Size	Document Number: LA-8221P	Rev: 0.2
Date: Wednesday, October 26, 2011	Sheet 11 of 58	



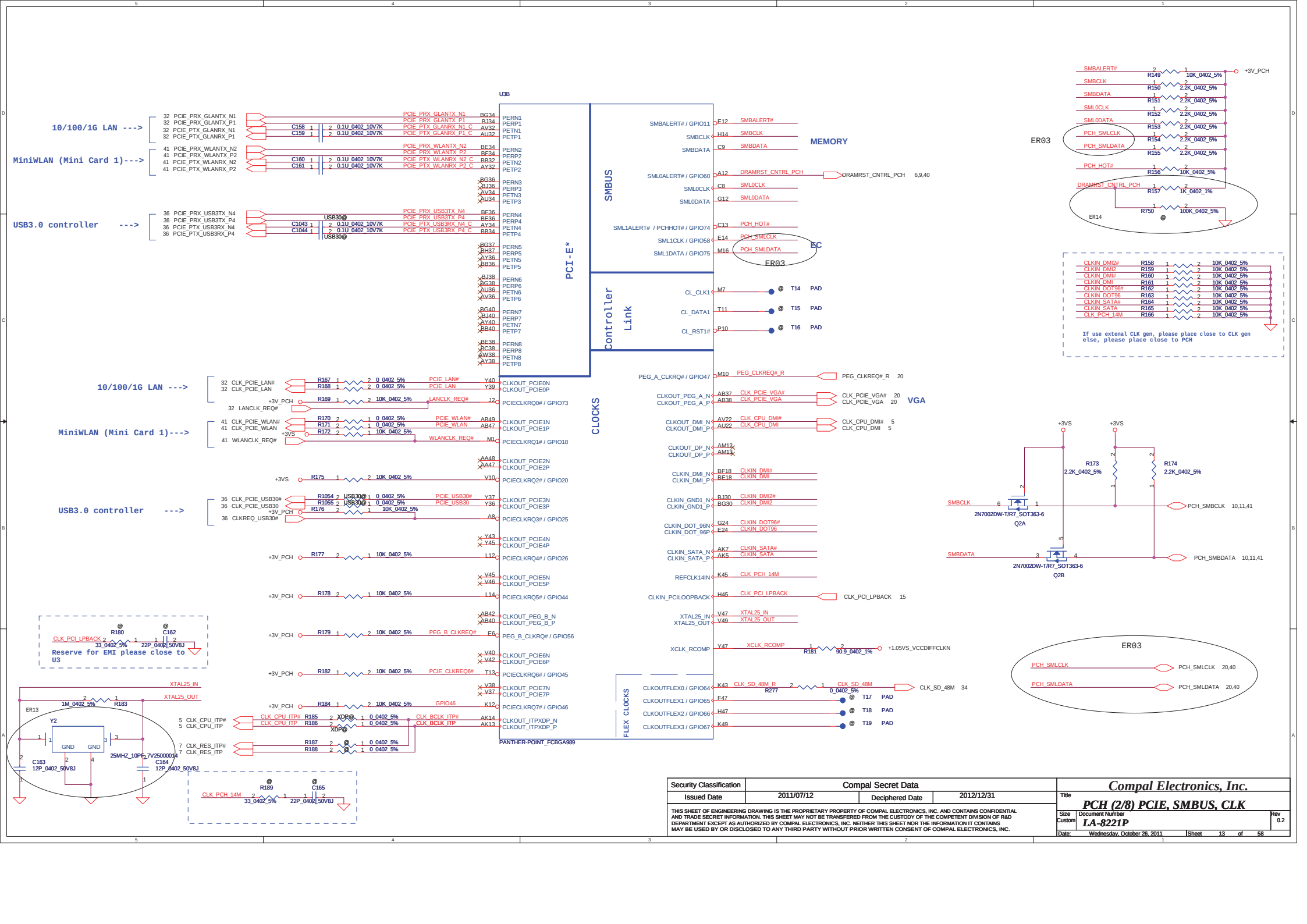
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 | Sheet 12 of 58



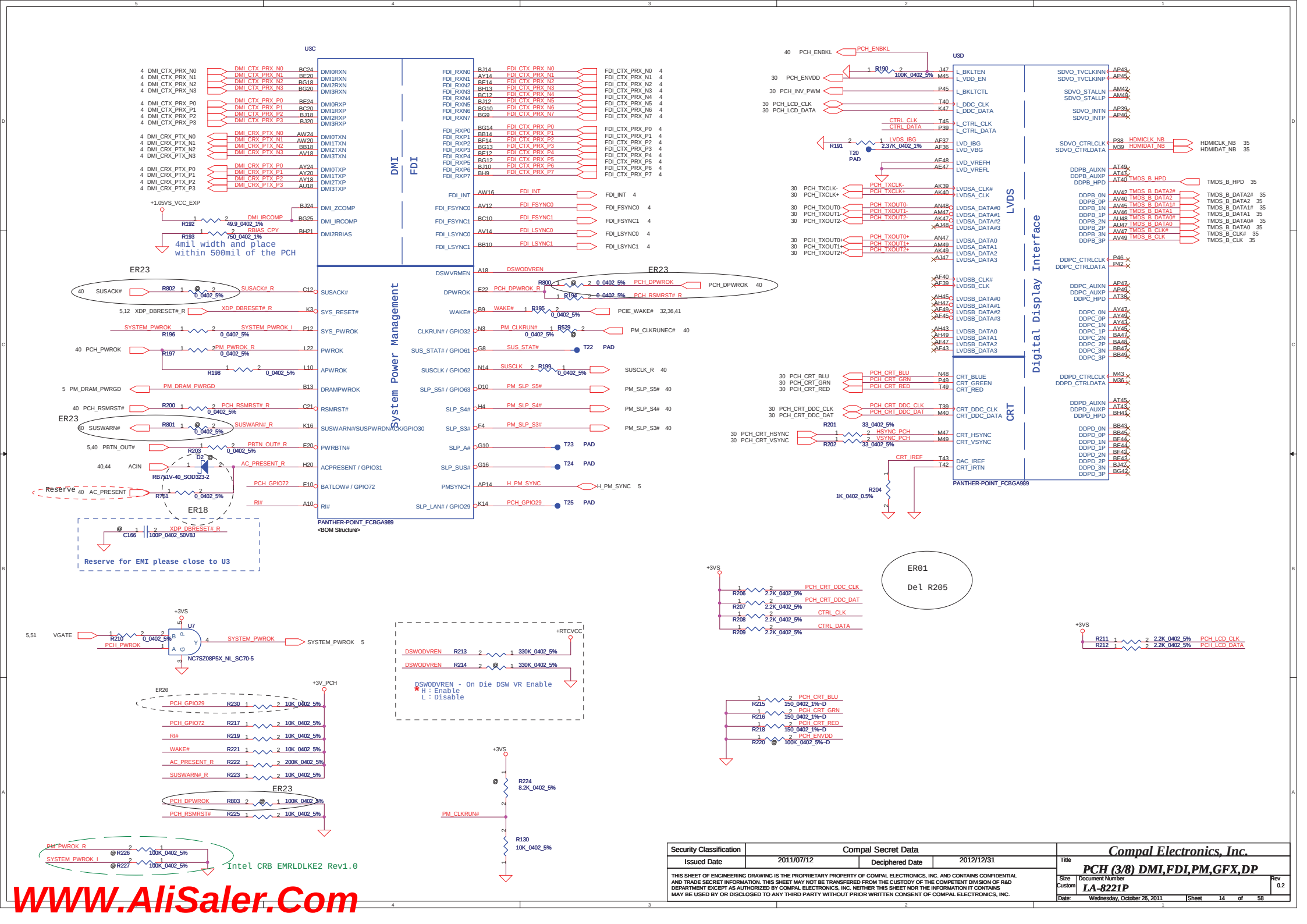
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 | Sheet 13 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
Custom	LA-8221P	0.2

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GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap

BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI *

Intel Anti-Theft Techonlogy

NV_ALE	
	High=Endabled
	Low=Disable(floating) *

NV_ALE @R228 1 2 1K_0402_5%

Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

USB2/3 port 1
USB2/3 port 2
Mini Card(WLAN) Bluetooth
HM76 not Support USB Port6,7
Camera
USB2 Conn. R
Card Reader

ER11

Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13

Reserve for EMI please close to U3

Within 500 mils

(For USB Port0, 1)
(For USB Port9)

ER11

PANTHER-POINT_FCBGA989

MC74VHC1G08DFT2G_SC70-5
NC7SZ08P5X_NL_SC70-5

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (4/8) PCI, USB, NVRAM

Size	Document Number	Rev
Custom	LA-8221P	0.2

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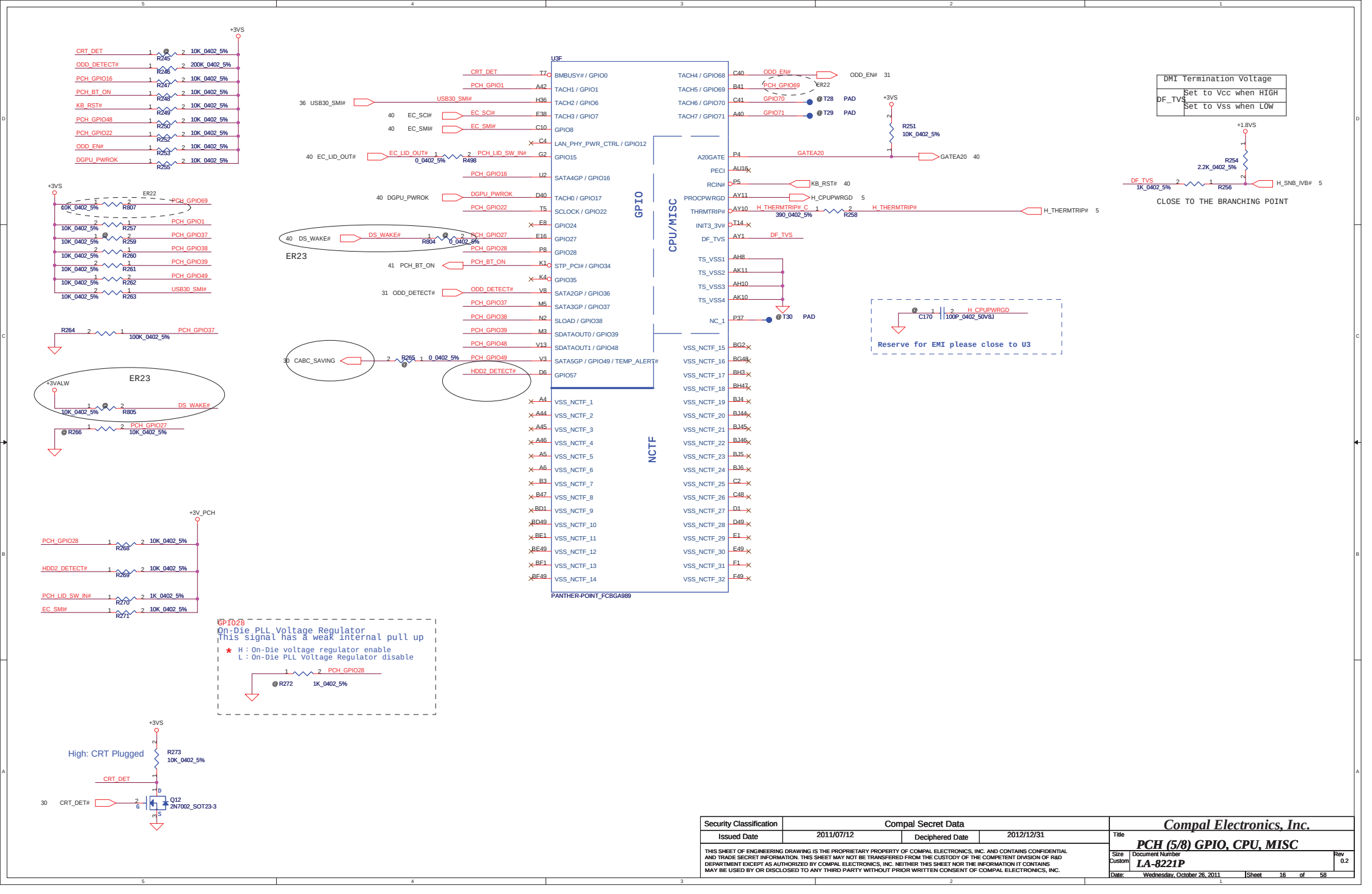


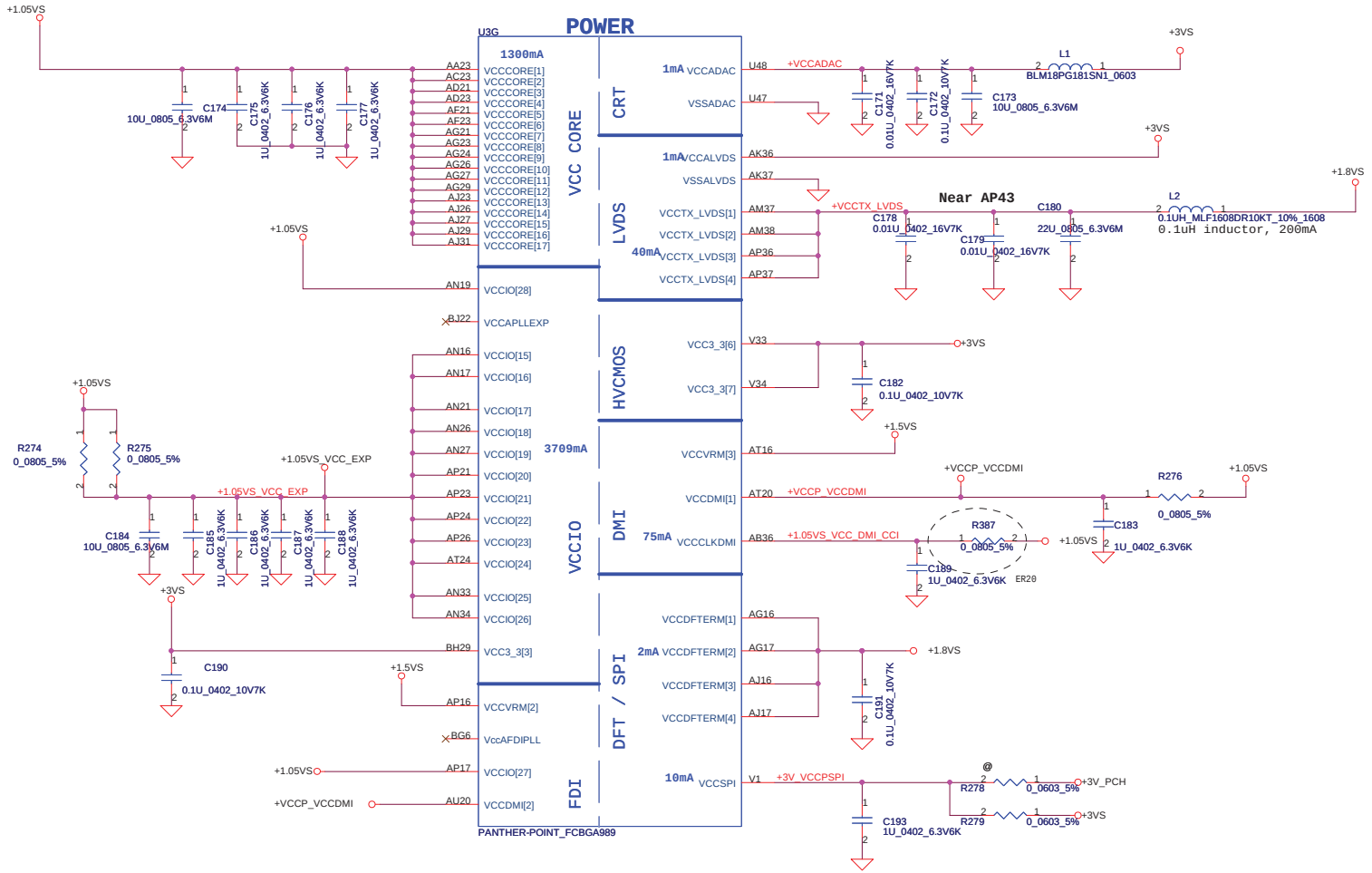
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 16 of 58



PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: Custom | Document Number: LA-8221P | Rev: 0.2

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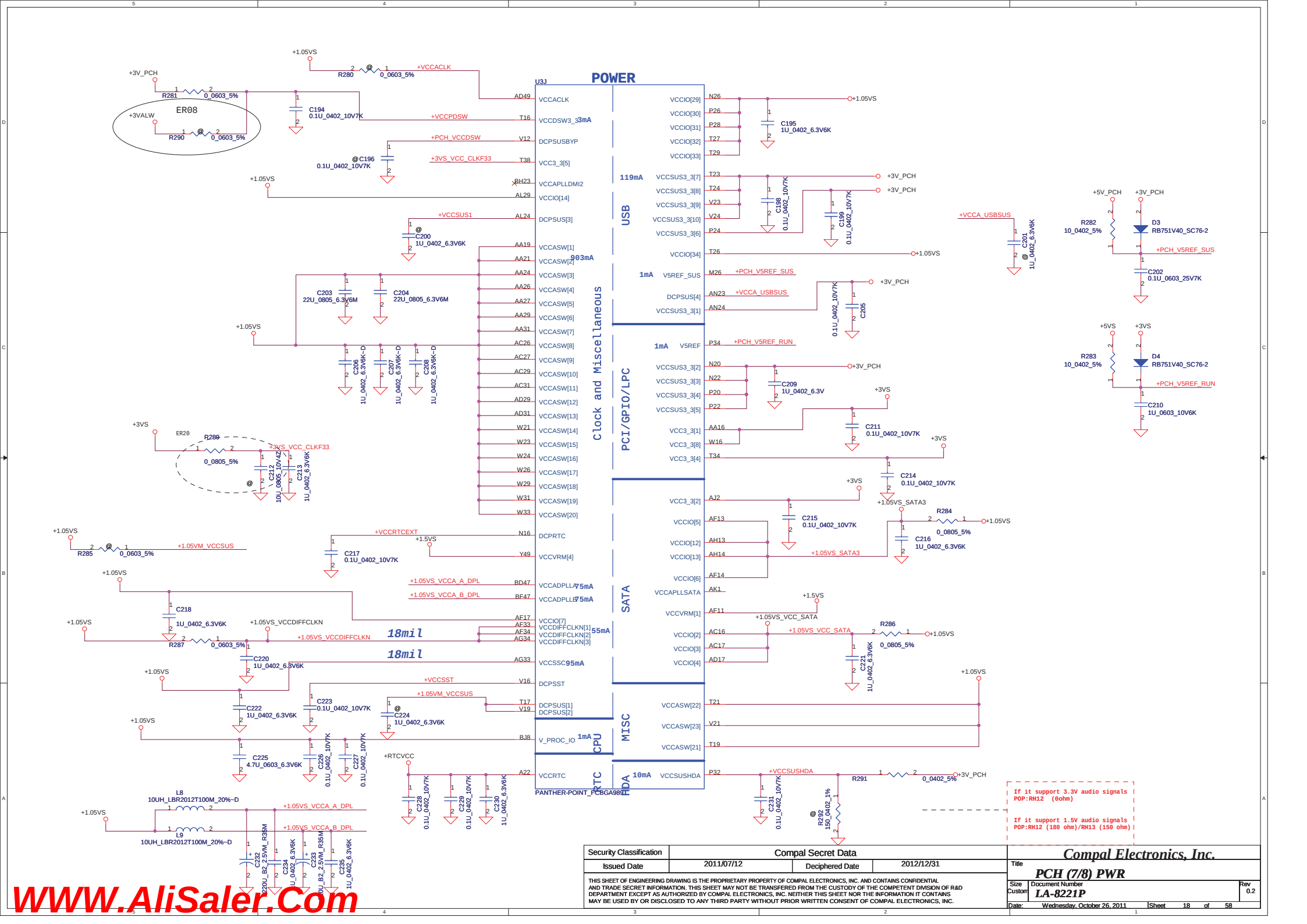


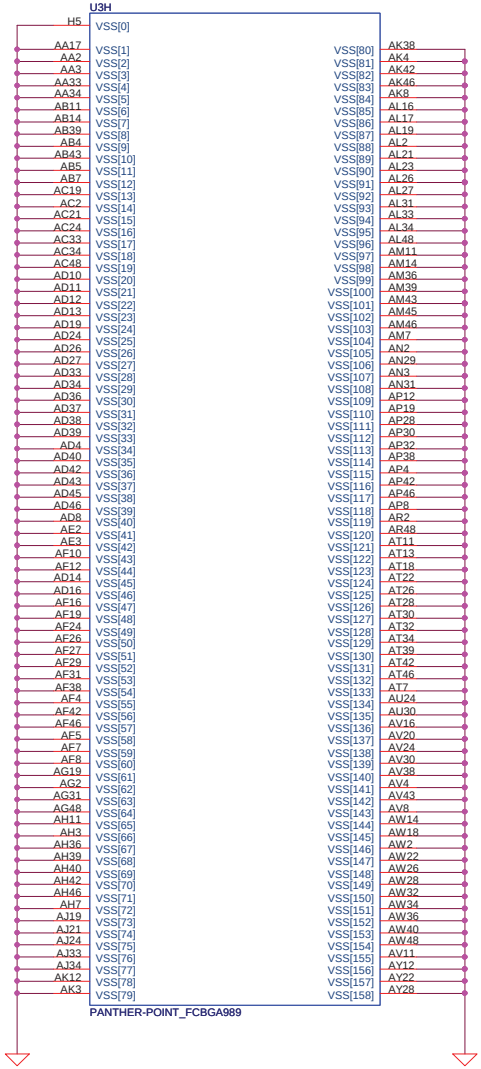
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

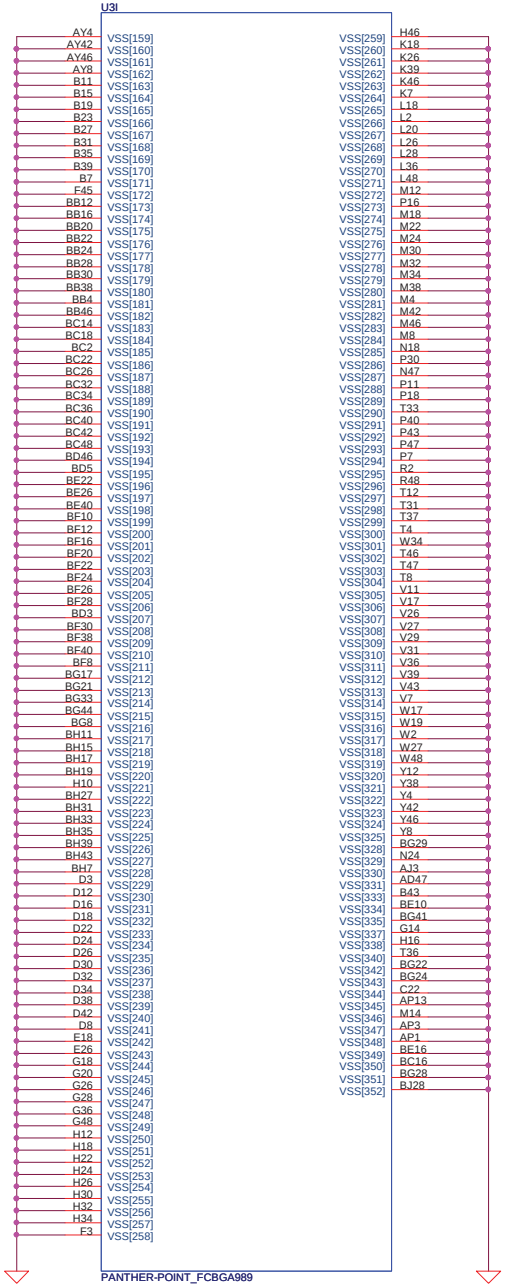
Compal Electronics, Inc.

Title: PCH (7/8) PWR

Size: Custom | Document Number: LA-8221P | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 18 of 58





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
Custom	LA-8221P	0.2

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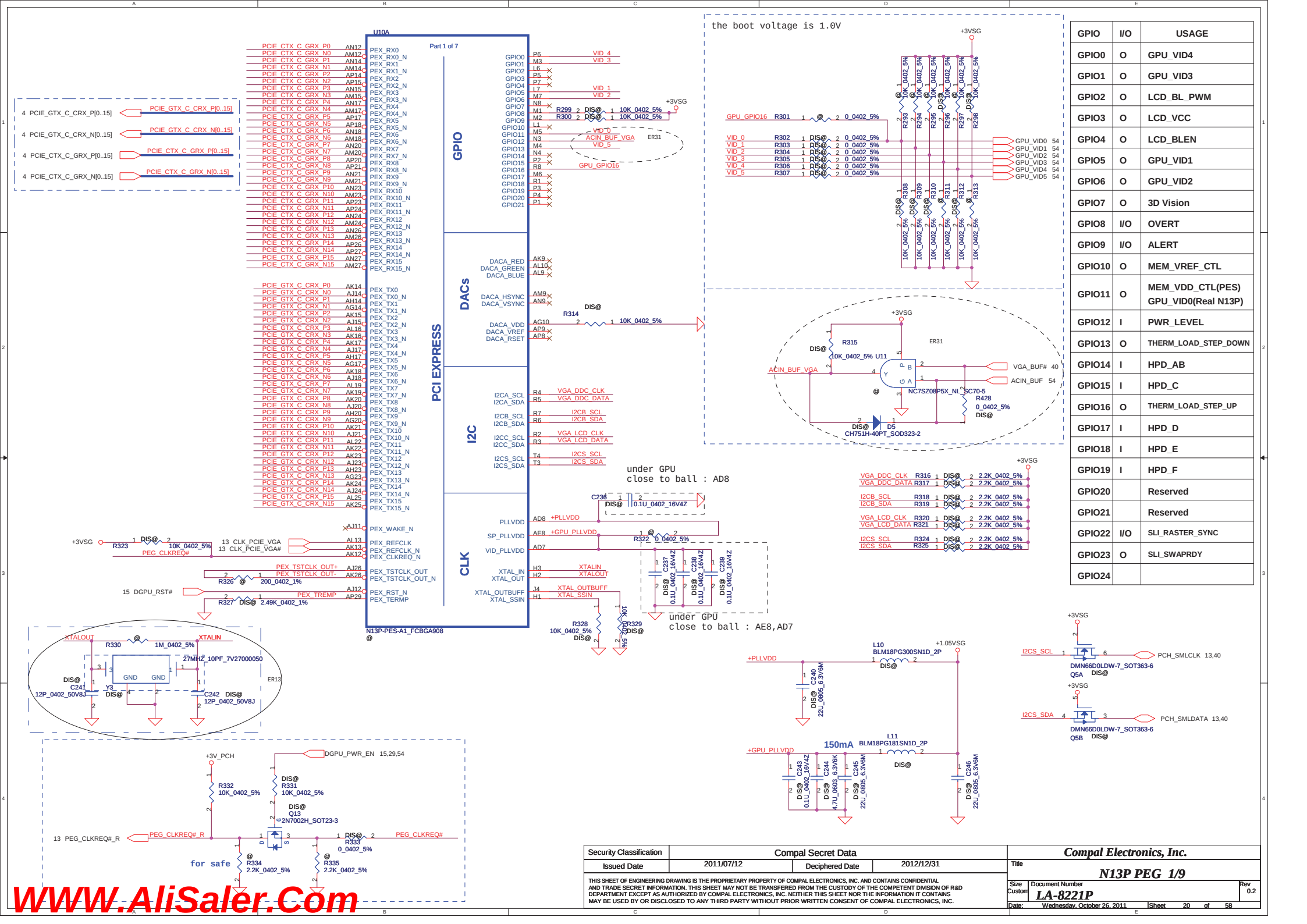

GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date 2012/12/31

Compal Electronics, Inc.

Title: N13P PEG 1/9

Size: Custom | Document Number: LA-8221P | Rev: 0.2

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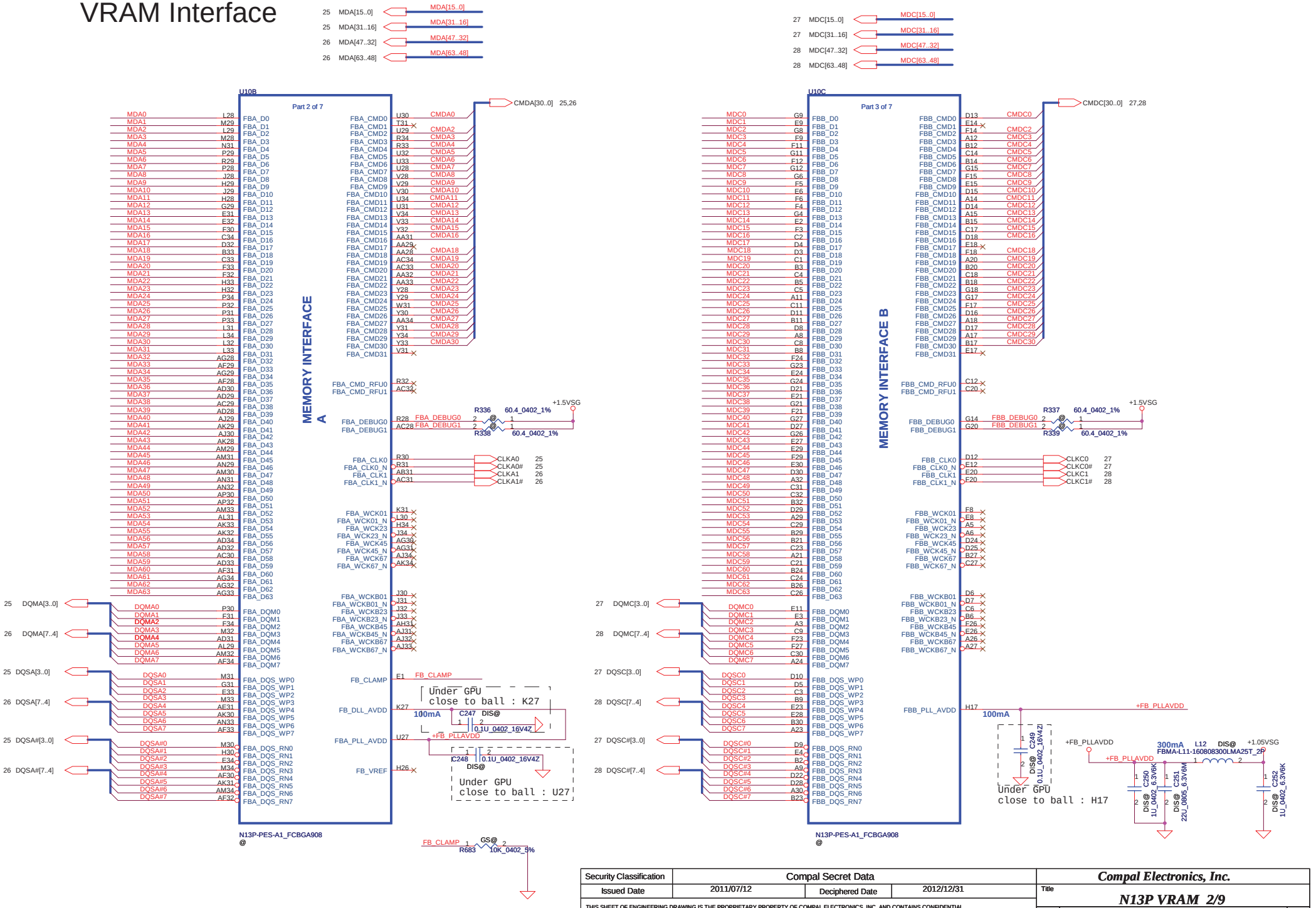
VRAM Interface



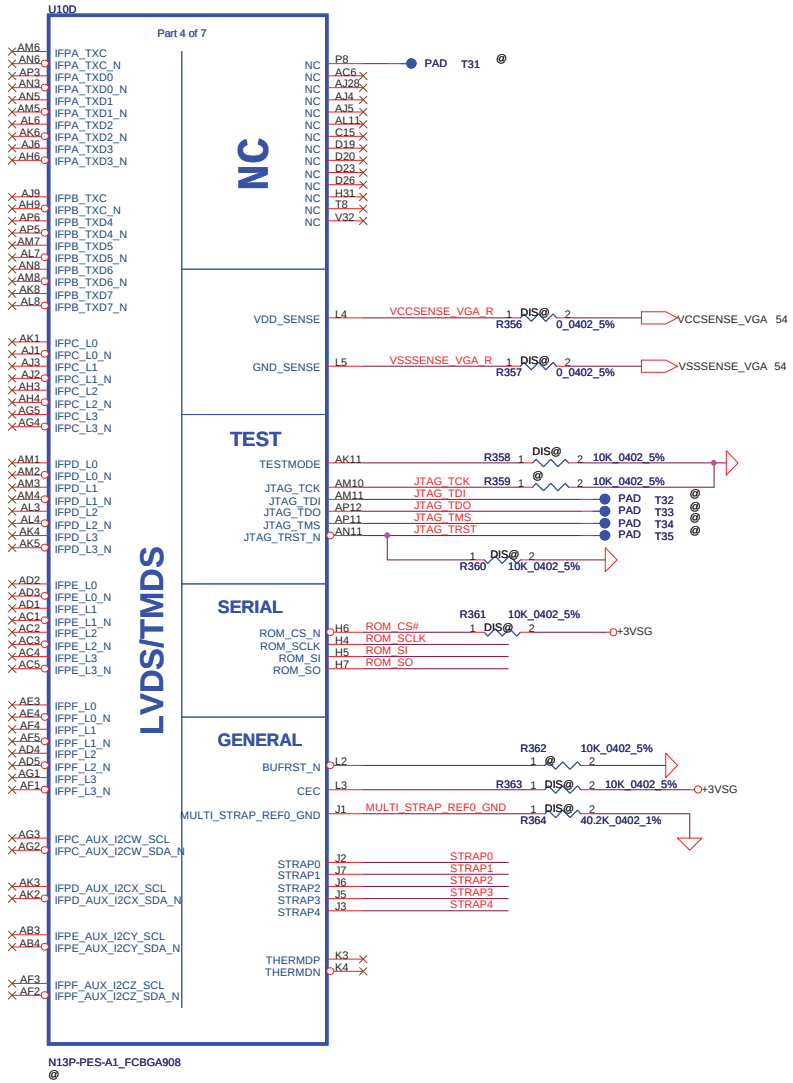
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

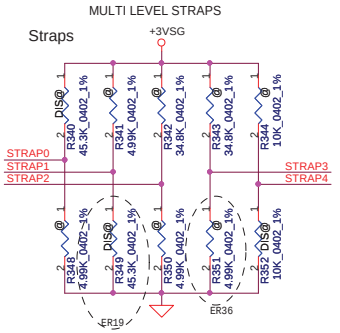
Compal Electronics, Inc.

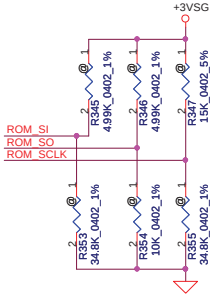
Title: **N13P VRAM 2/9**

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 | Sheet 21 of 58







Need check with NVIDIA

10/12 nVidia Keven Strap1

10/17 nVidia Keven N13P-GS ER36 Strap2 / Strap3

For N13P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 45K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO30	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 35K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS30	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 20K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S60	R PU 45K	R PD 45K	R PU 20K	R PD 25K	R PD 10K	R PD 15K	R PU 10K	R PU 5K

For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 45K	R PD 30K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO30	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 35K	R PD 30K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS30	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 20K	R PD 30K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix SA000041S60	R PU 45K	R PD 45K	R PU 10K	R PD 5K	R PD 10K	R PD 15K	R PD 30K	R PD 15K

For N13M-GE1 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	128M* 16* 4 1GB	Samsung SA000047QA0	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 45K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	128M* 16* 4 1GB	Hynix SA00003YO30	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 35K	R PD 30K	R PU 5K

For N13M-GE1 GB1b-64 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE1	900 MHz	256M* 8* 8 2GB	ELPIDA SA000056P00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 5K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	256M* 8* 8 2GB	Hynix SA000056Q00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 10K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	512M* 8* 8 4GB	HYNIX SA00005BL00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 15K	R PD 30K	R PU 5K
N13M-GE1	900 MHz	512M* 8* 8 4GB	ELPIDA SA00005AA00	R PU 45K	R PD 45K	R PU 5K	R PD 5K	R PD 10K	R PD 20K	R PD 30K	R PU 5K

Compal Electronics, Inc.

Title: N13P LVDS 3/9

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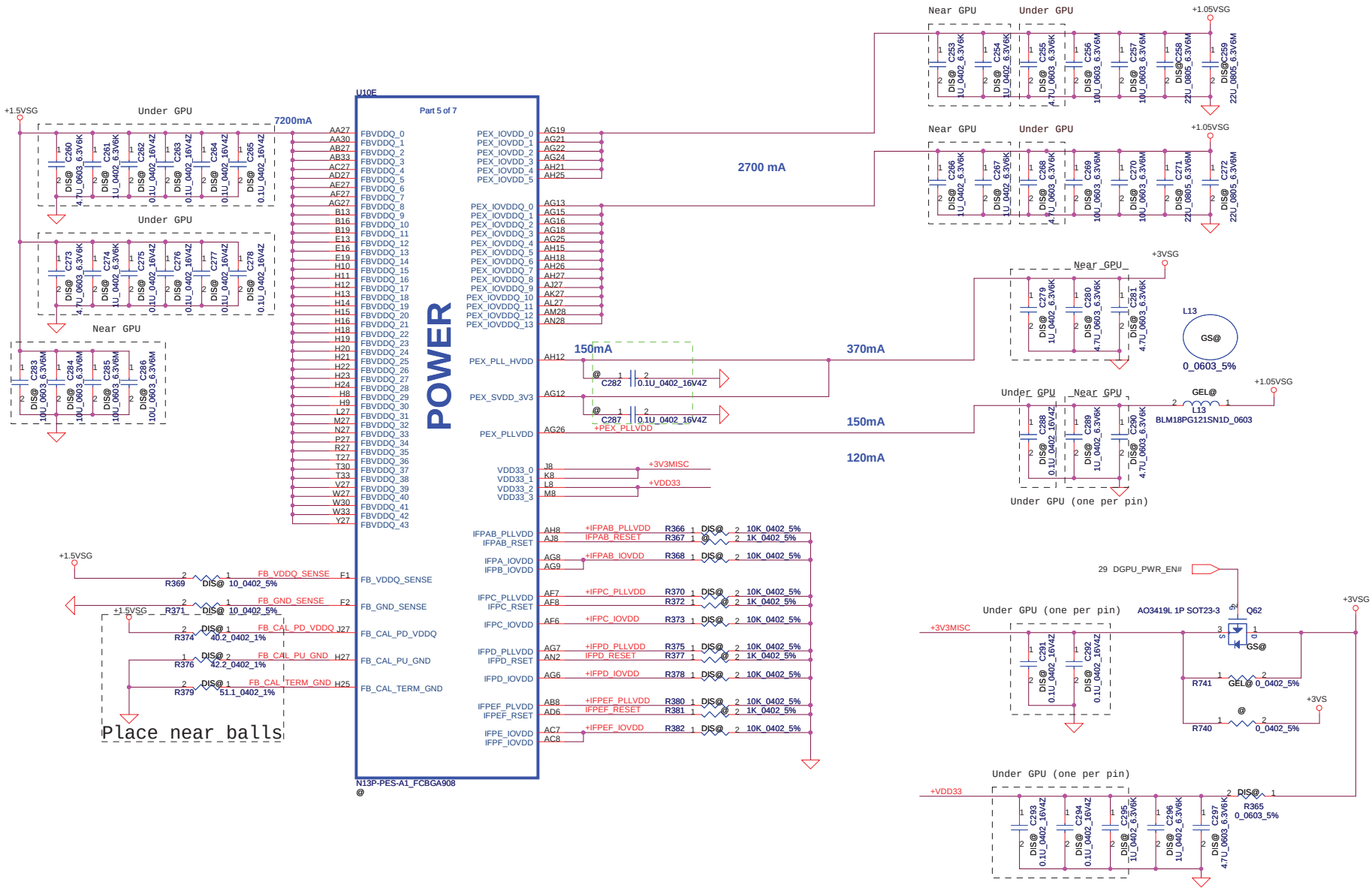

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **N13P POWER & GND 4/9**

Size	Document Number	Rev
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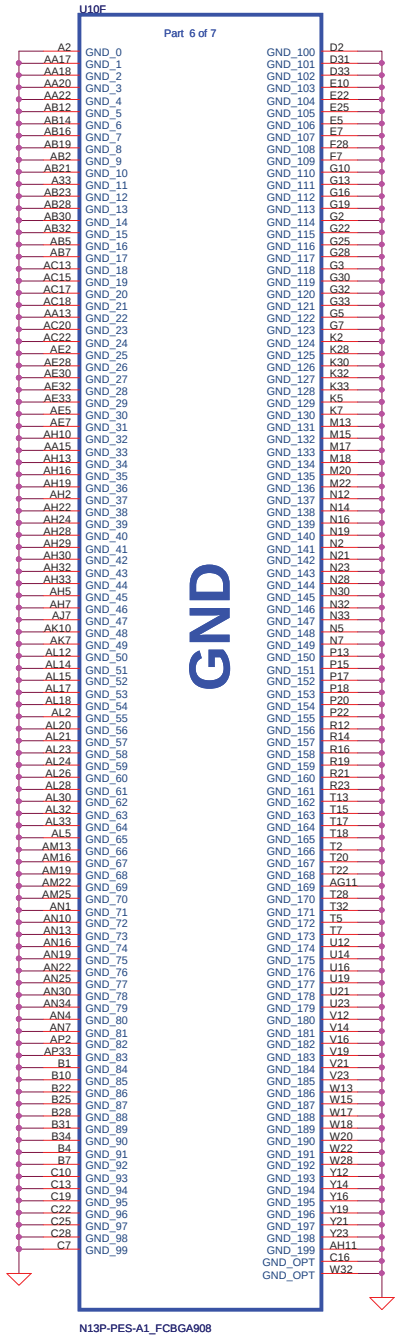

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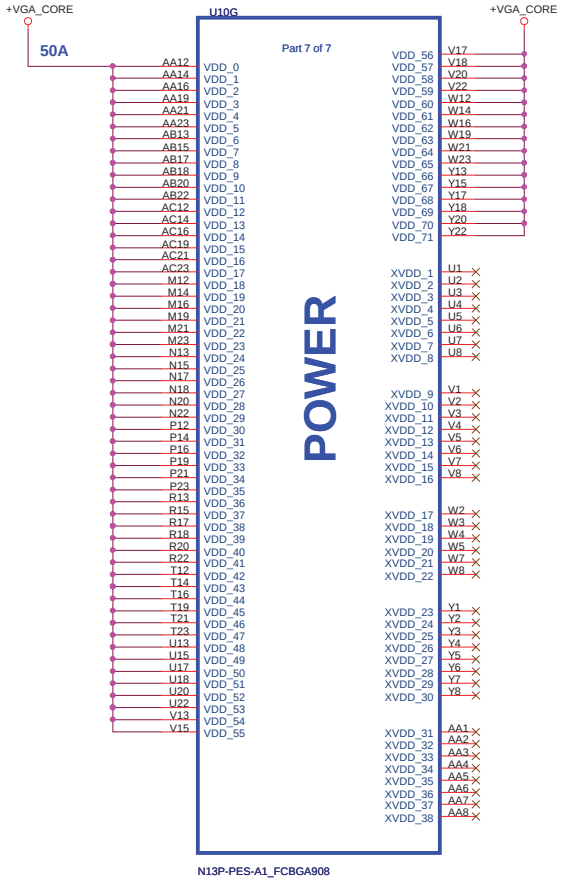

Compal Electronics, Inc.

Title: N13P POWER & GND 5/9

Size: Custom | Document Number: LA-8221P | Rev: 0.2

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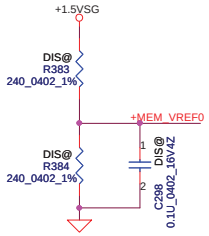
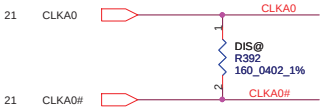
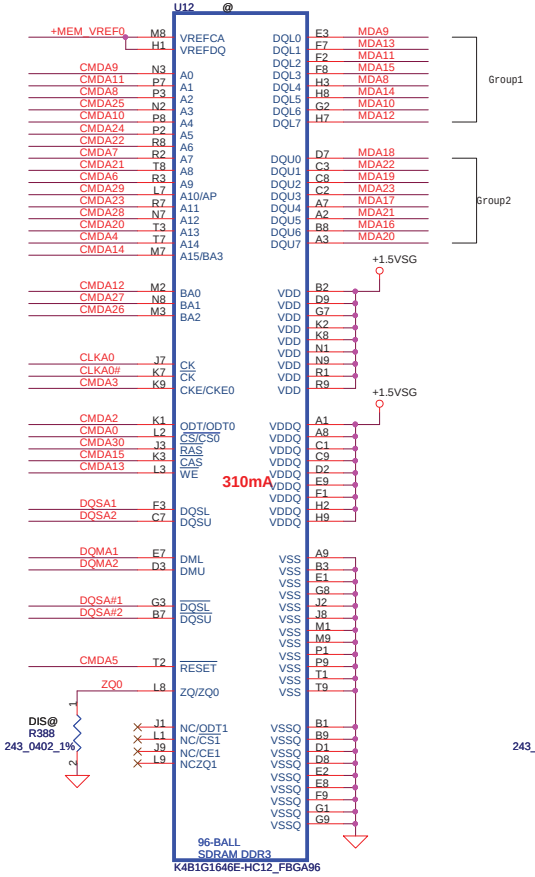
VRAM DDR3 chips (1GB)

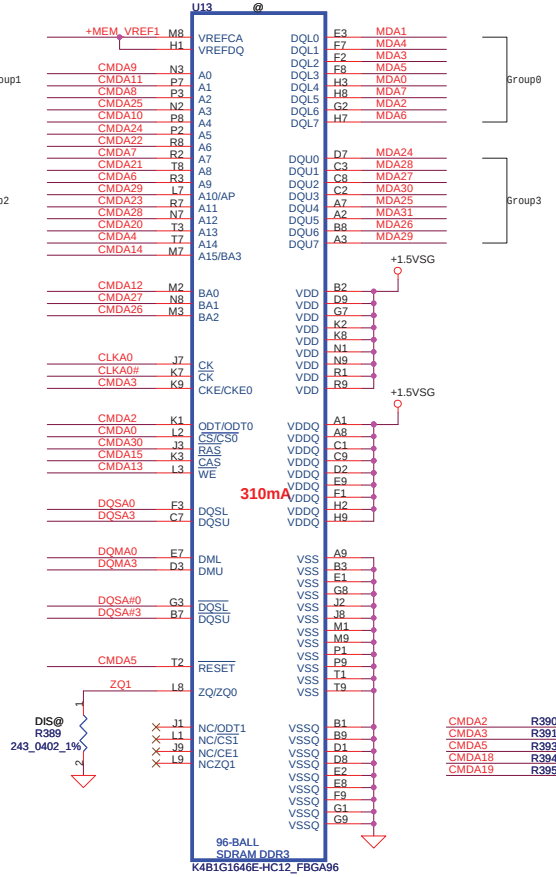
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



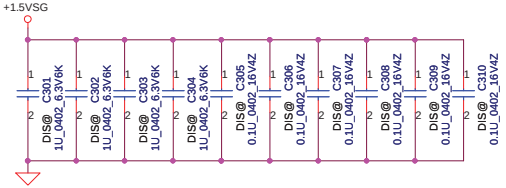


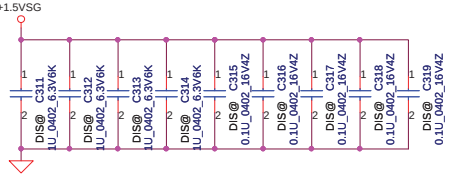
NV recommand 0720





	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

Compal Electronics, Inc.

Title: N13P DDR3 6/9

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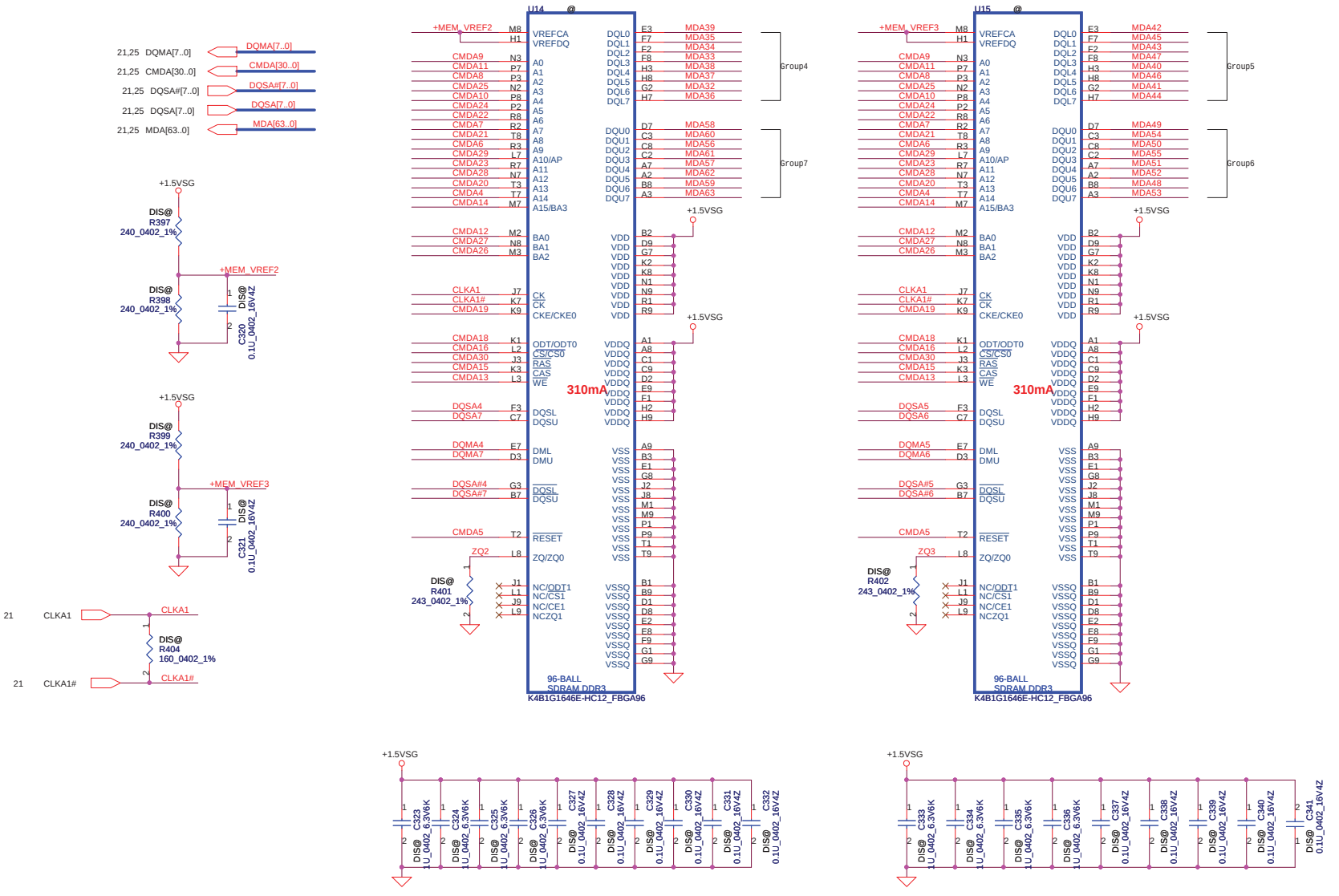
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P DDR3 7/9

Size: Custom | Document Number: LA-8221P | Rev: 0.2

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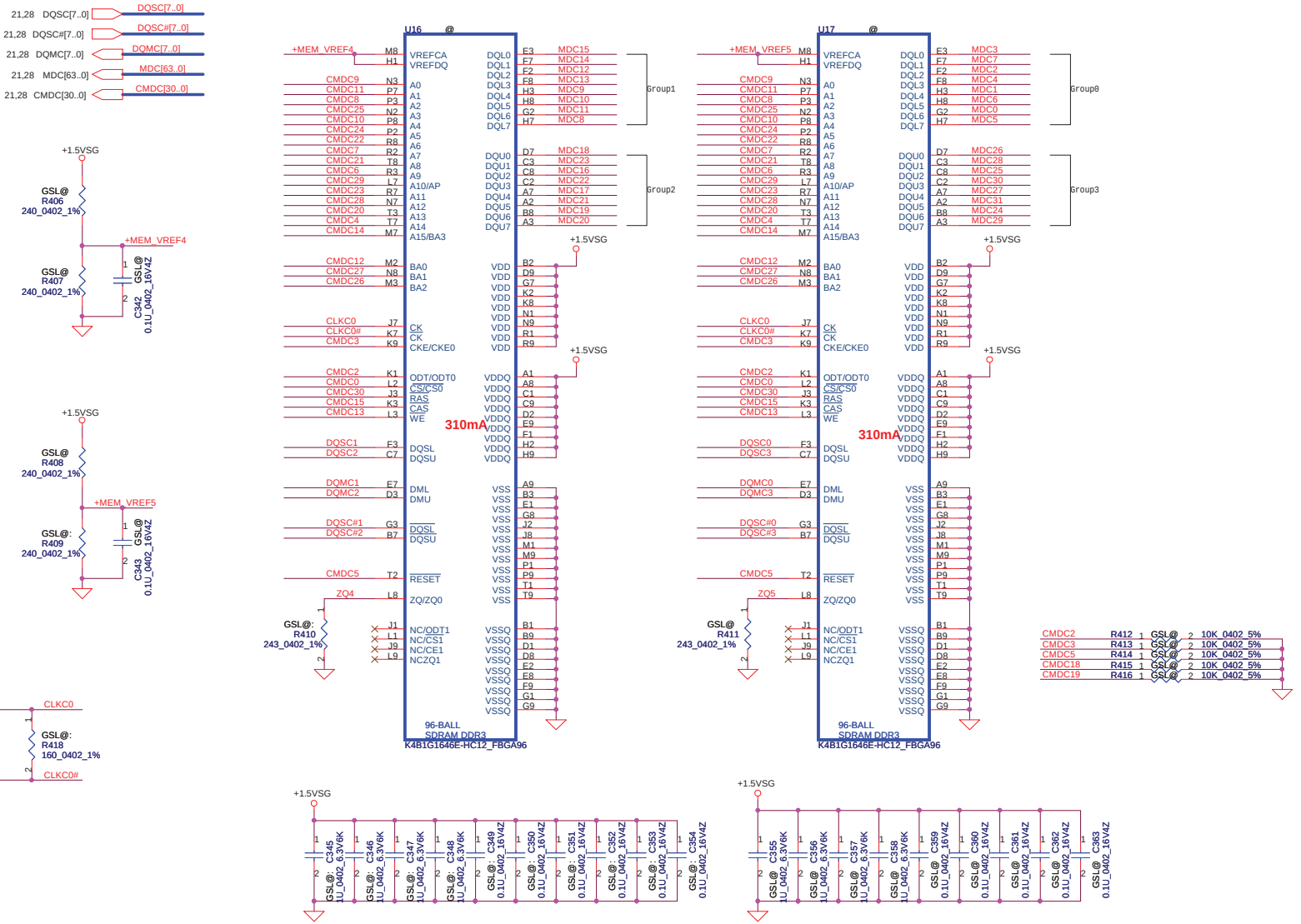
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P DDR3 8/9

Size: Custom | Document Number: LA-8221P | Rev: 0.2

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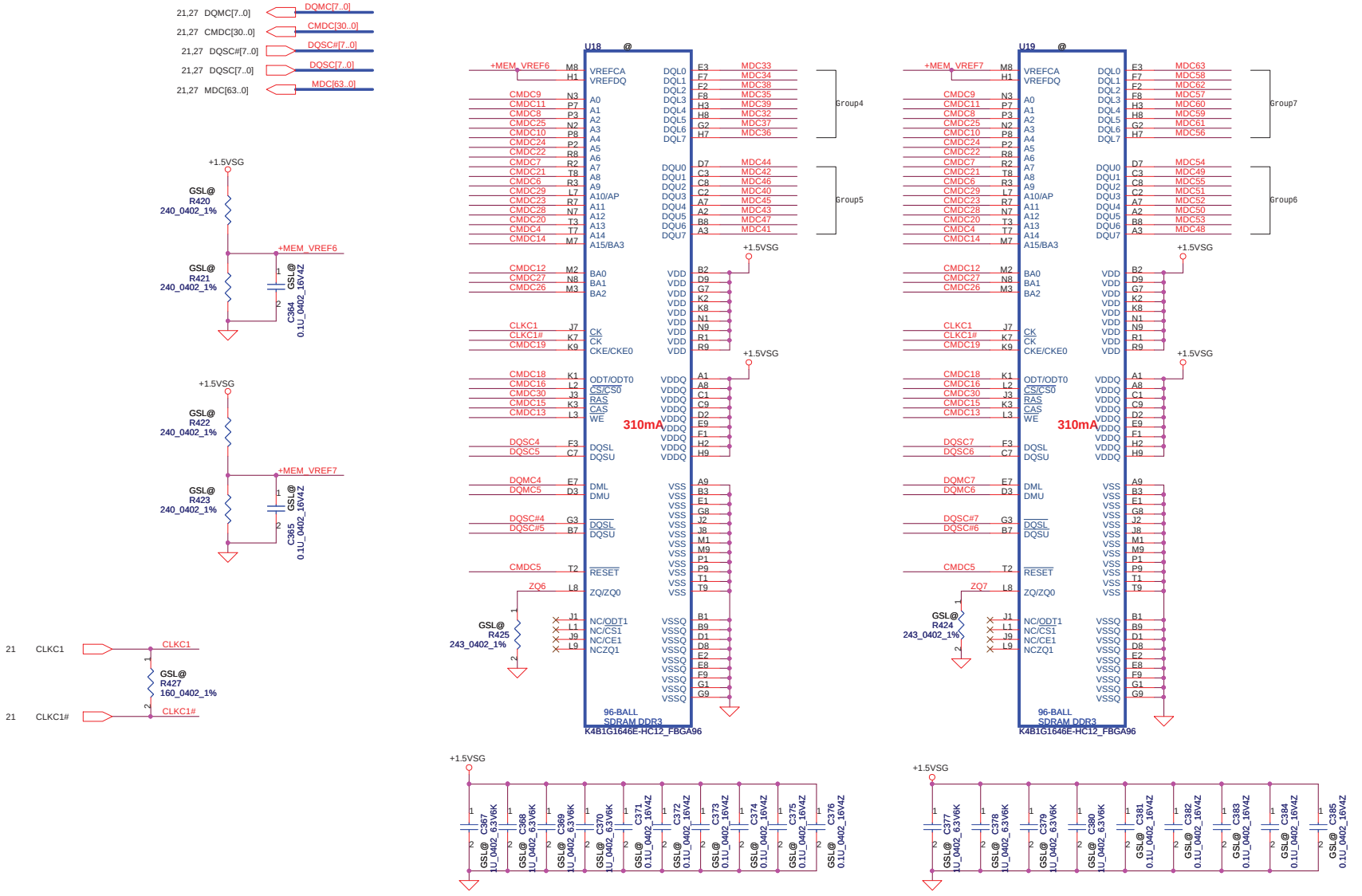
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

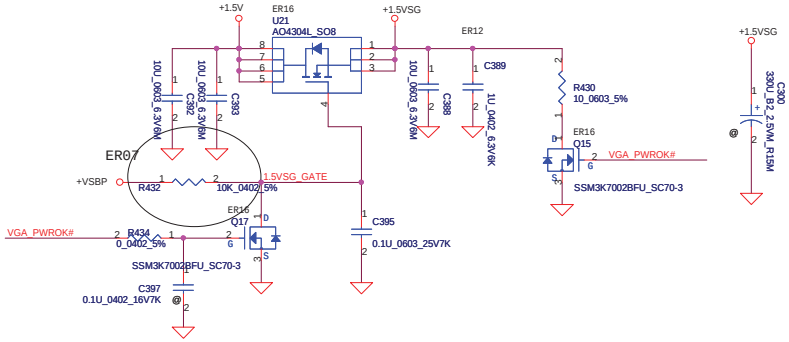
Compal Electronics, Inc.

Title: N13P DDR3 9/9

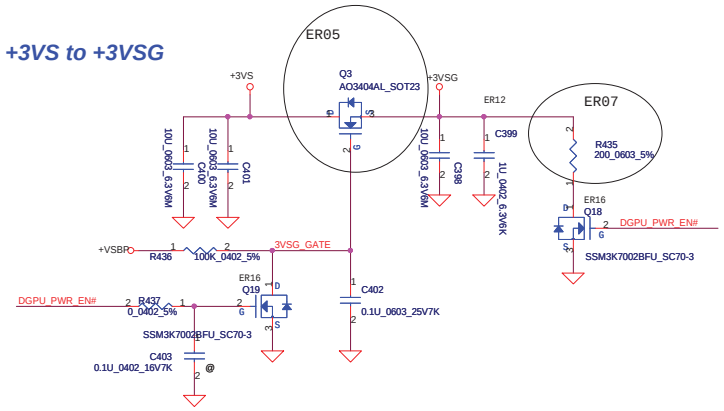
Size: Custom | Document Number: LA-8221P | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 28 of 58

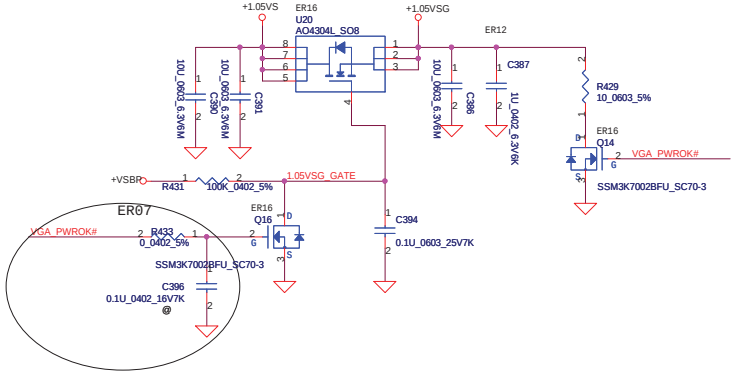
+1.5V to +1.5VSG

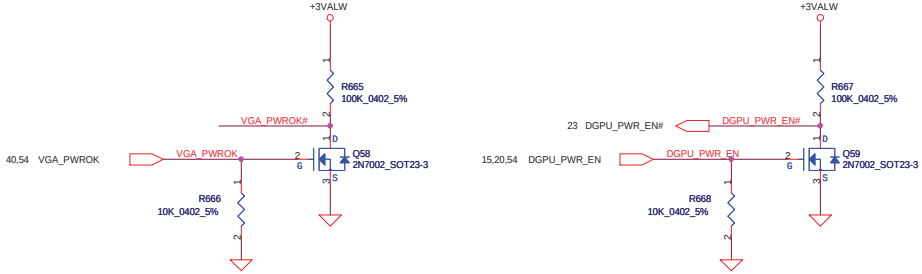


+3VS to +3VSG



+VCCP to +1.05VSG





Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

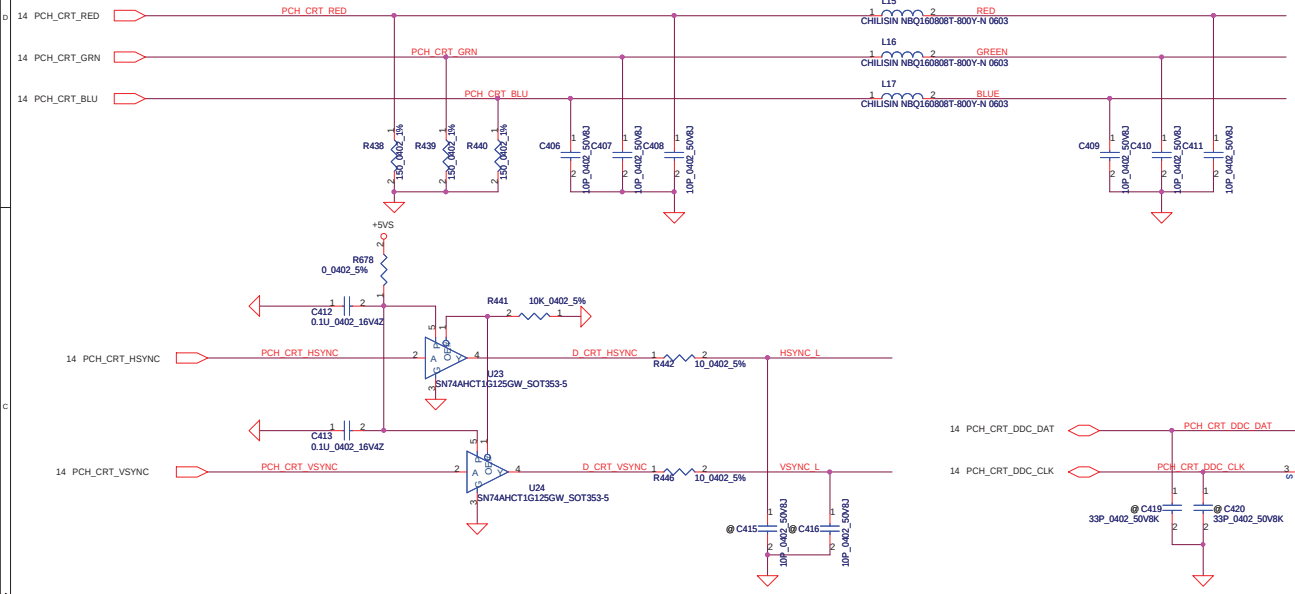
Compal Electronics, Inc.

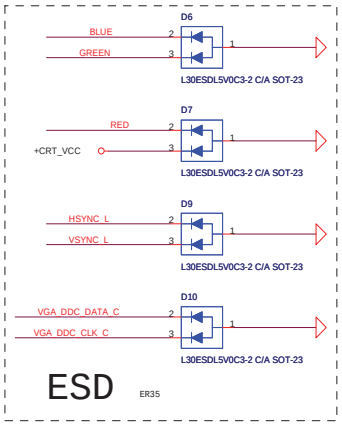
Title: **PCH (2/8) PCIE, SMBUS, CLK**

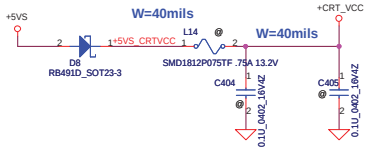
Size	Document Number	Rev
Custom	LA-8221P	0.2

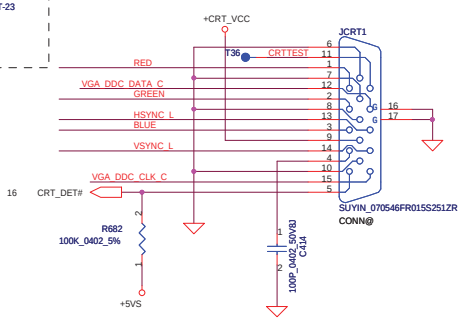
Date: Wednesday, October 26, 2011 | Sheet 29 of 58

C R T

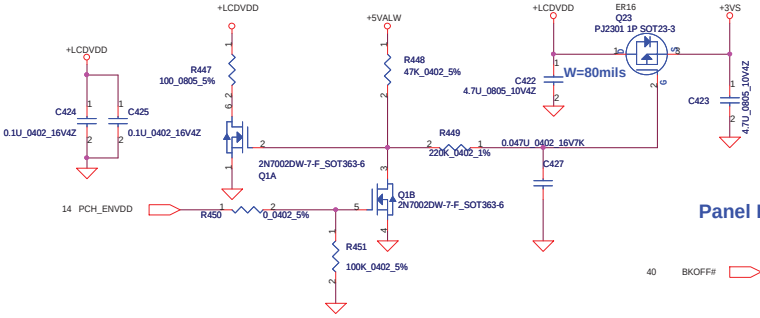




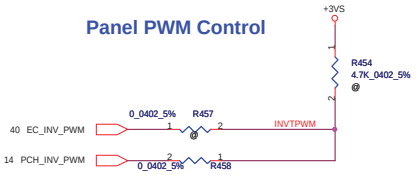




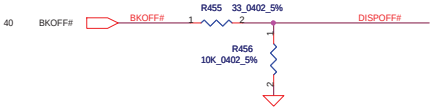
LCD POWER CIRCUIT

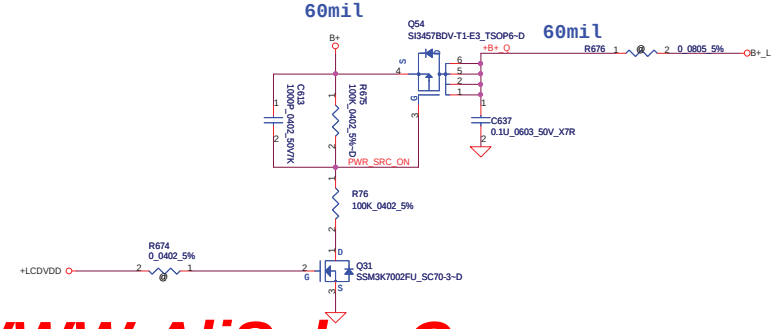


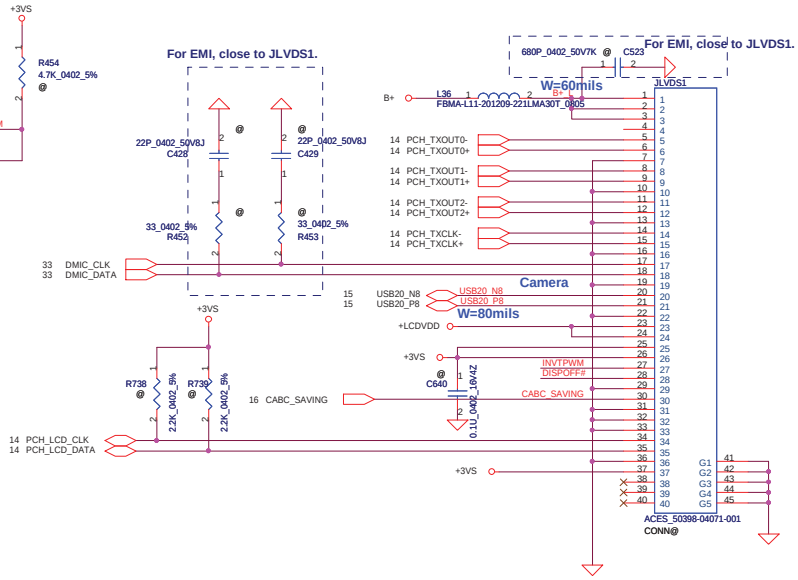
Panel PWM Control



Panel Backlight Control







Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

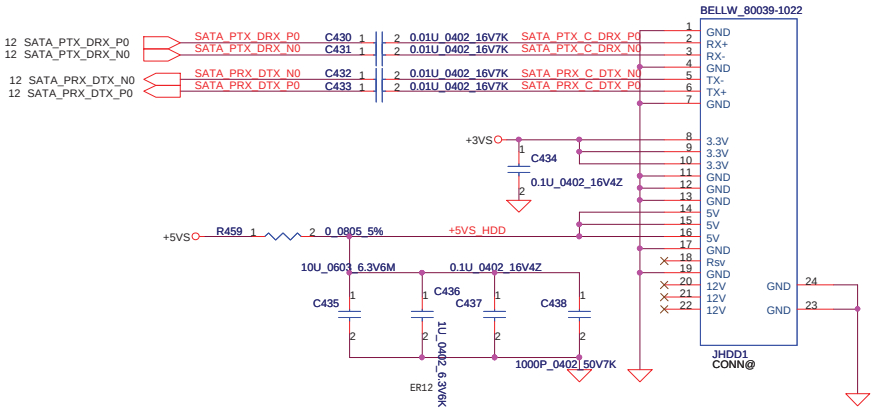
Compal Electronics, Inc.

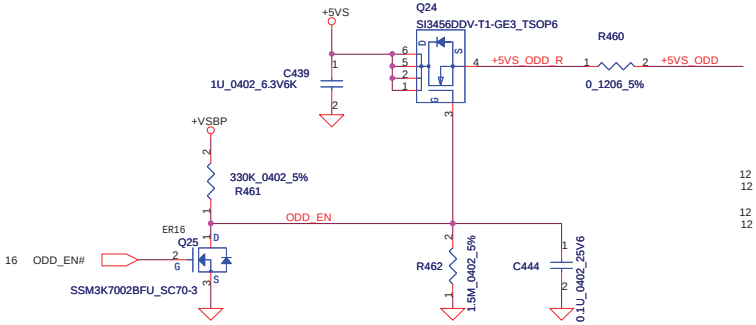
Title: LVDS/CRT CONN

Size	Document Number	Rev
C	LA-8221P	0.2

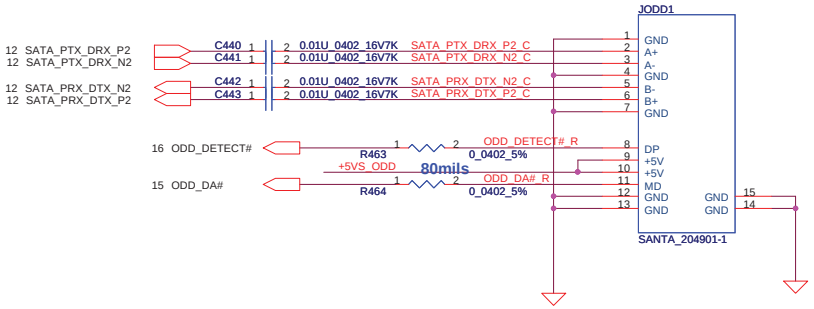
Date: Wednesday, October 26, 2011 Sheet 30 of 58

SATA HDD Conn.

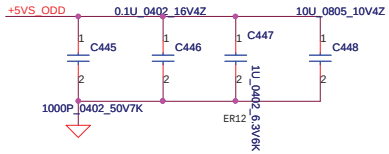




SATA ODD Conn.



Placea caps. near ODD CONN.



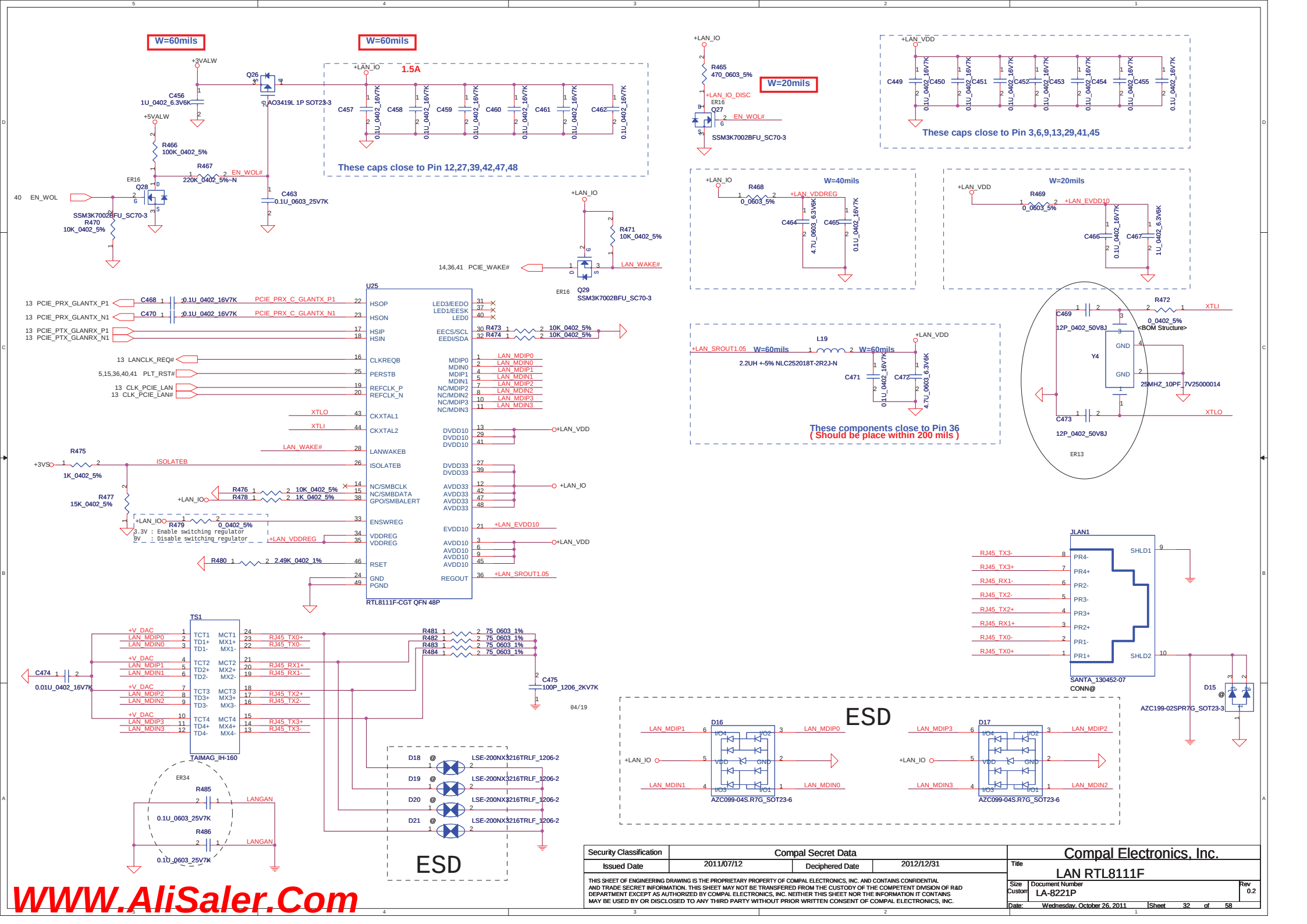
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: HDD & ODD CONN

Size	Document Number	Rev
B	LA-8221P	0.2

Date: Wednesday, October 26, 2011 | Sheet 31 of 58



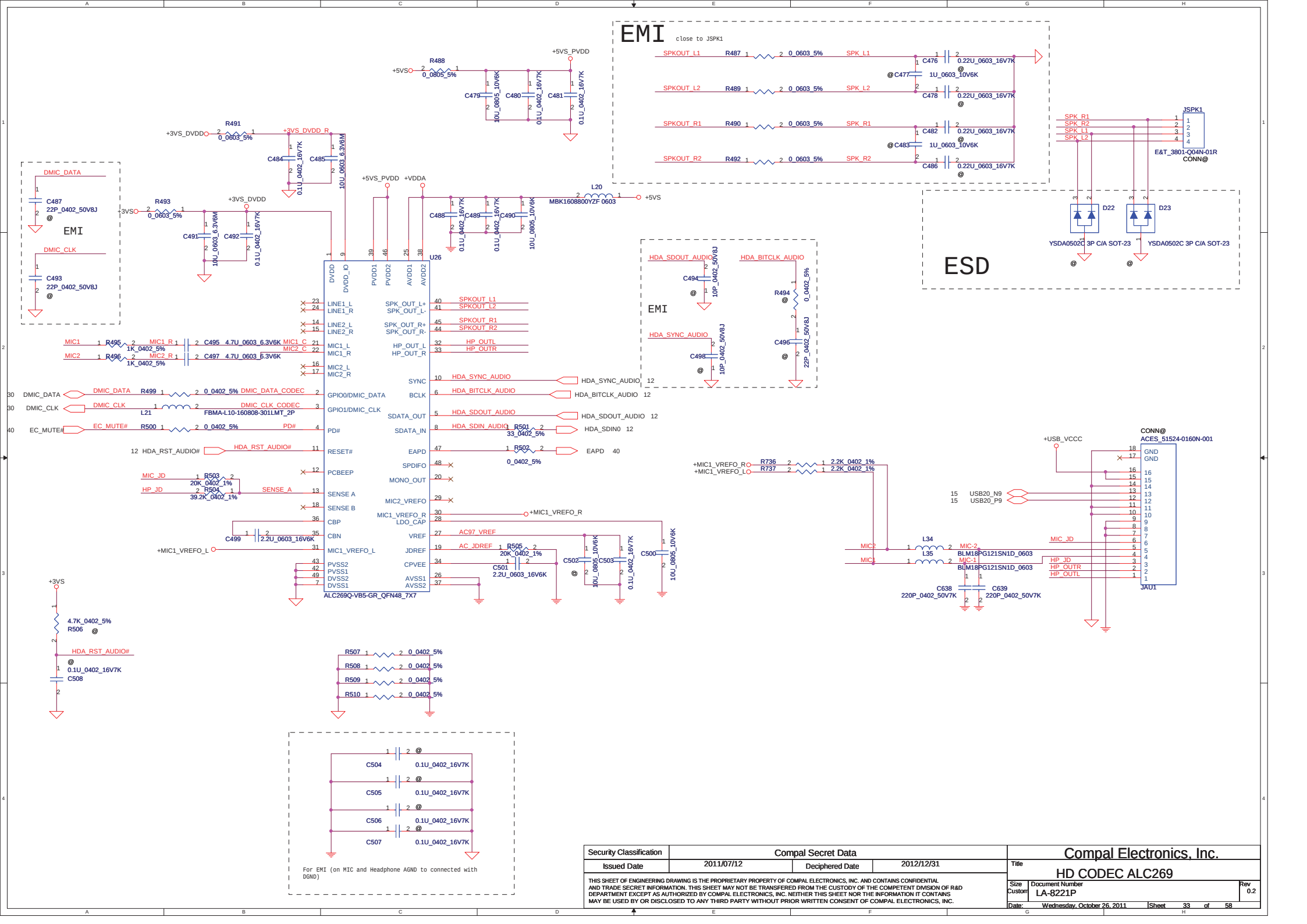
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LAN RTL8111F

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 32 of 58



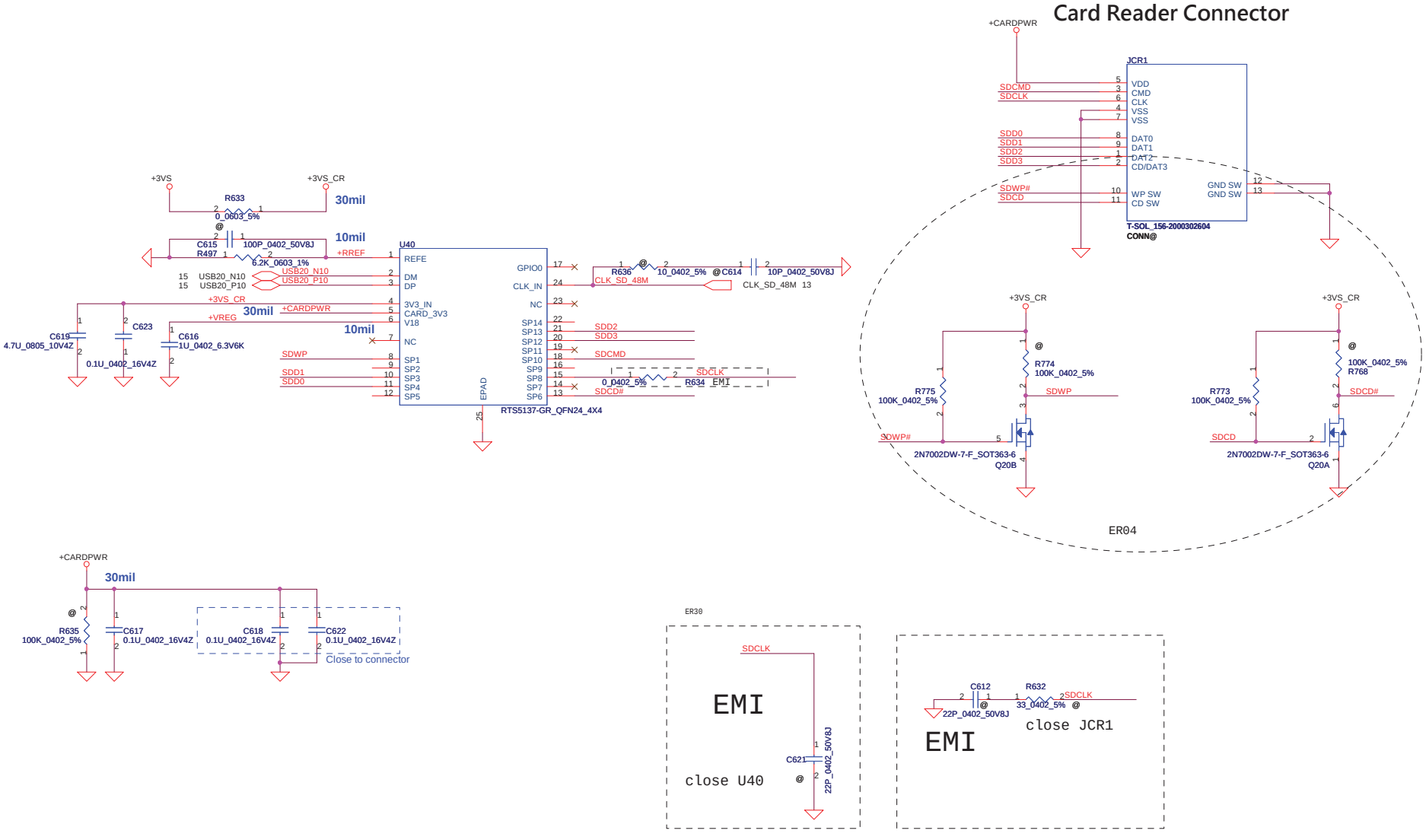
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: HD CODEC ALC269

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 33 of 58



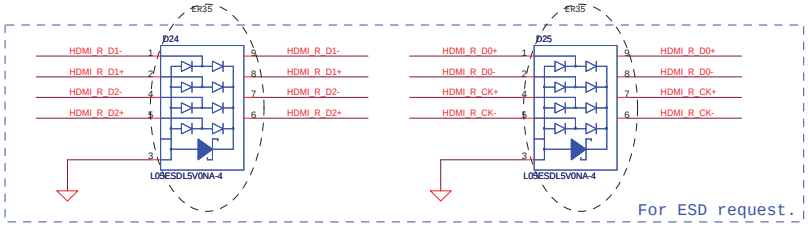
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

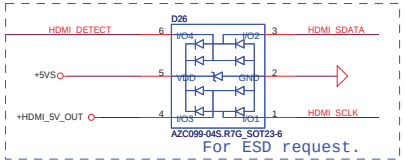
Compal Electronics, Inc.

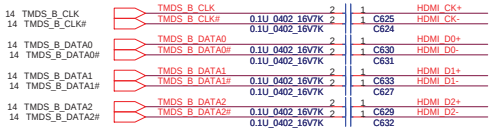
Title: RTS5137 Media Card Controller

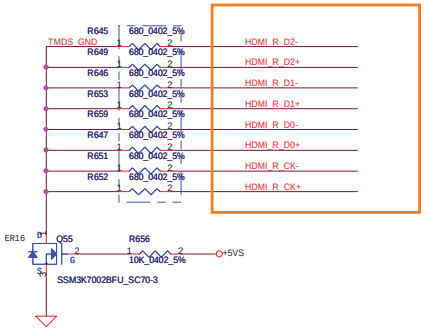
Size	Document Number	Rev
Custom	LA-8221P	0.2

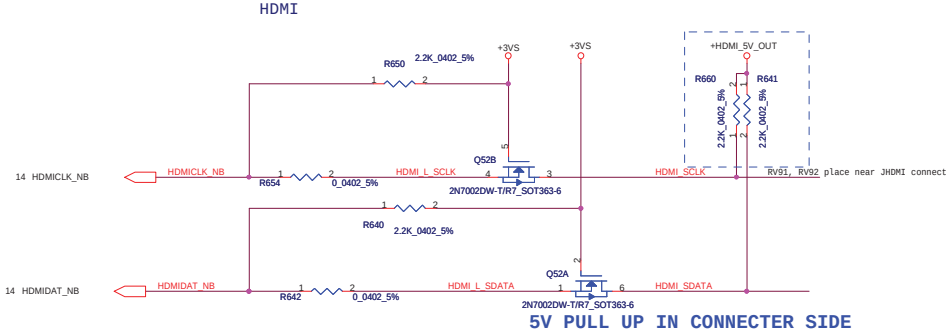
Date: Wednesday, October 26, 2011 Sheet 34 of 58

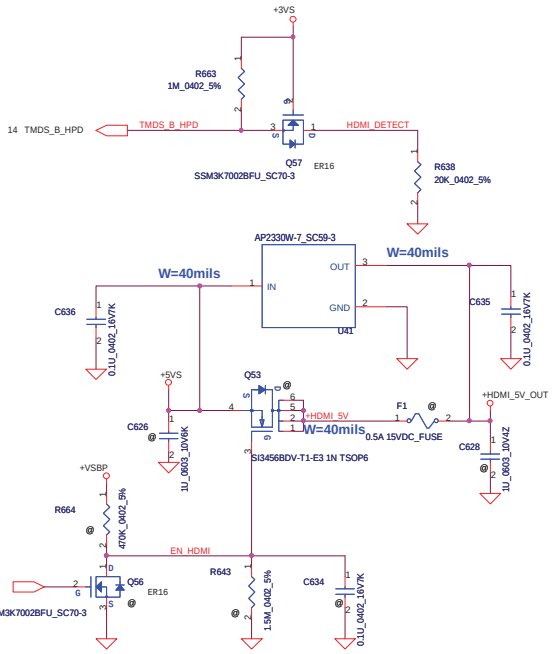


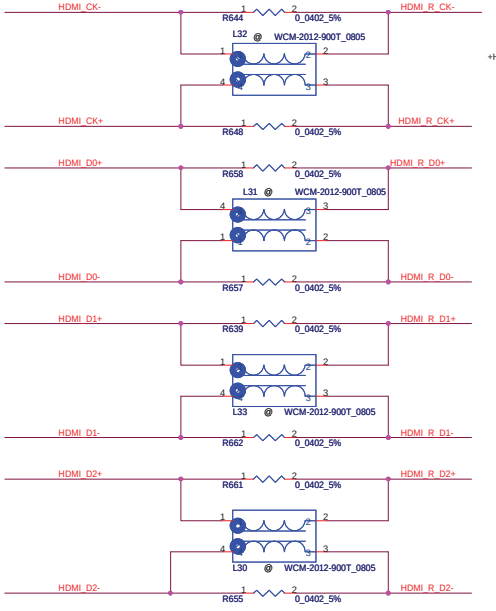


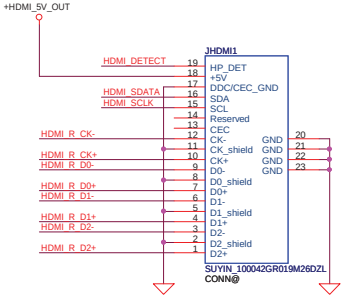


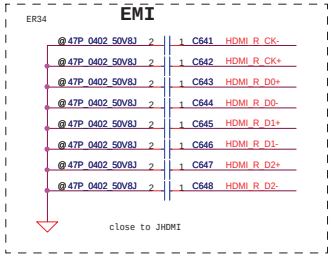












Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
C	LA-8221P	0.2

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ER02 Add USB3.0 (ASM1042)

	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

For WAKE Function

USB_PEPWRDET

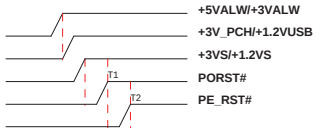
	R1034	R1022
S1	Mount	@
* S3	@	Mount

USB_PESEL

	R1033
* Other applaction	@
Express Card/Mini Card	Mount

Power Sequence

ASM1042



T1: 2~80ms
T2: >200ms

ASM1042 (TQFN 64)

Close to ASM1042

+3VALW to +1.2V Transfer

reference delay circuit

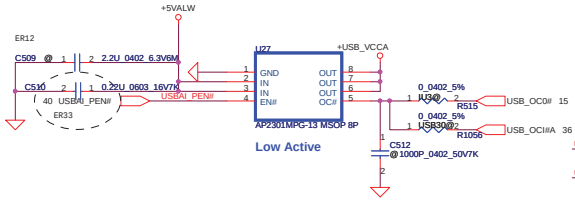
Security Classification	Compal Secret Data
Issued Date	2010/10/1
Deciphered Date	2012/06/30

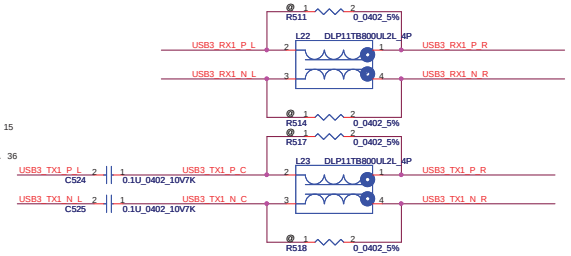
Compal Electronics, Inc.

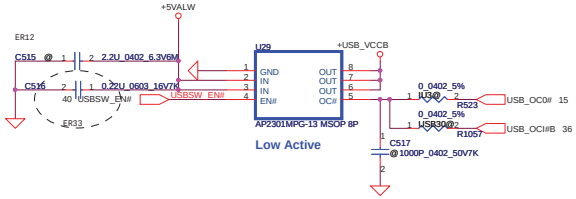
Title: USB3.0 controller

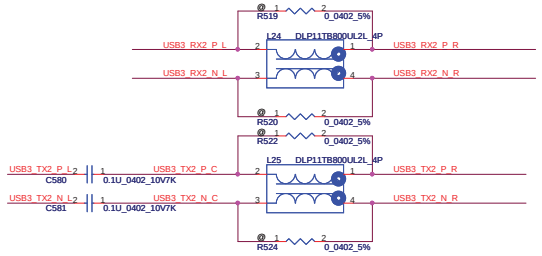
Size: Custom | Document Number: LA-8221P | Rev: 0.2

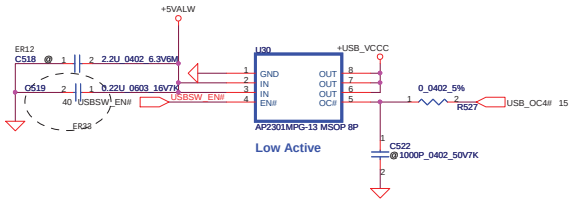
Date: Wednesday, October 26, 2011 | Sheet 36 of 58

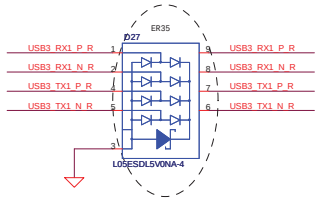




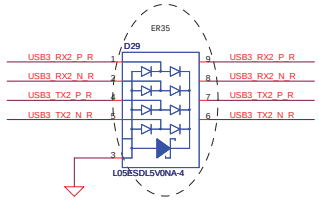




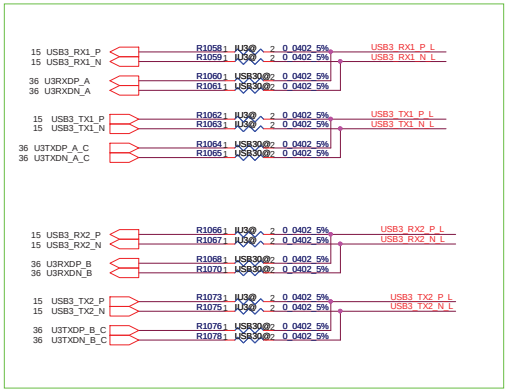


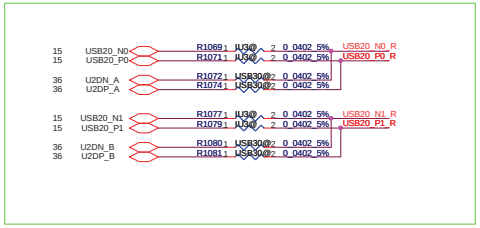


Co-lay USB3.0 (PCH & ASM1042)

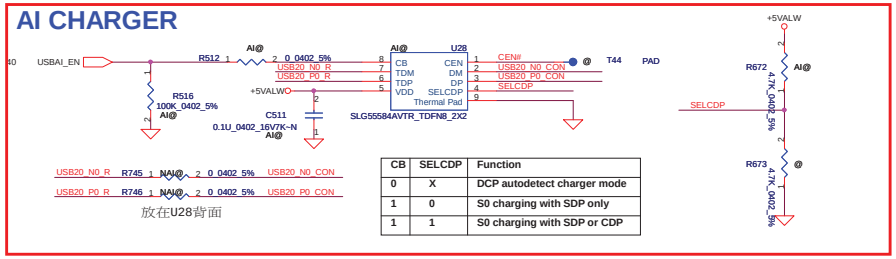


Co-lay USB3.0 (PCH & ASM1042)



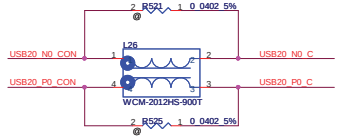


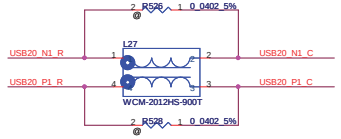
AI CHARGER



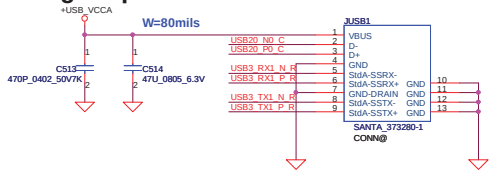
放在U28背面

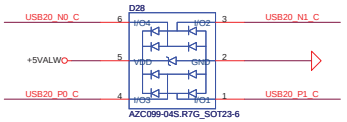
CB	SELCDP	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP

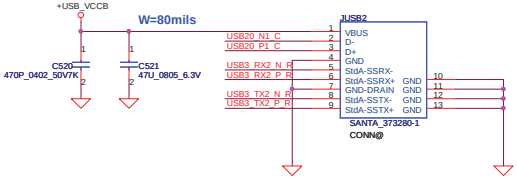




charger port: left side & near user







ER02 Add USB3.0 (ASM1042)

Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: USB2.0/USB3.0 CONN

Size	Document Number	Rev
Custom	LA-8221P	0.2

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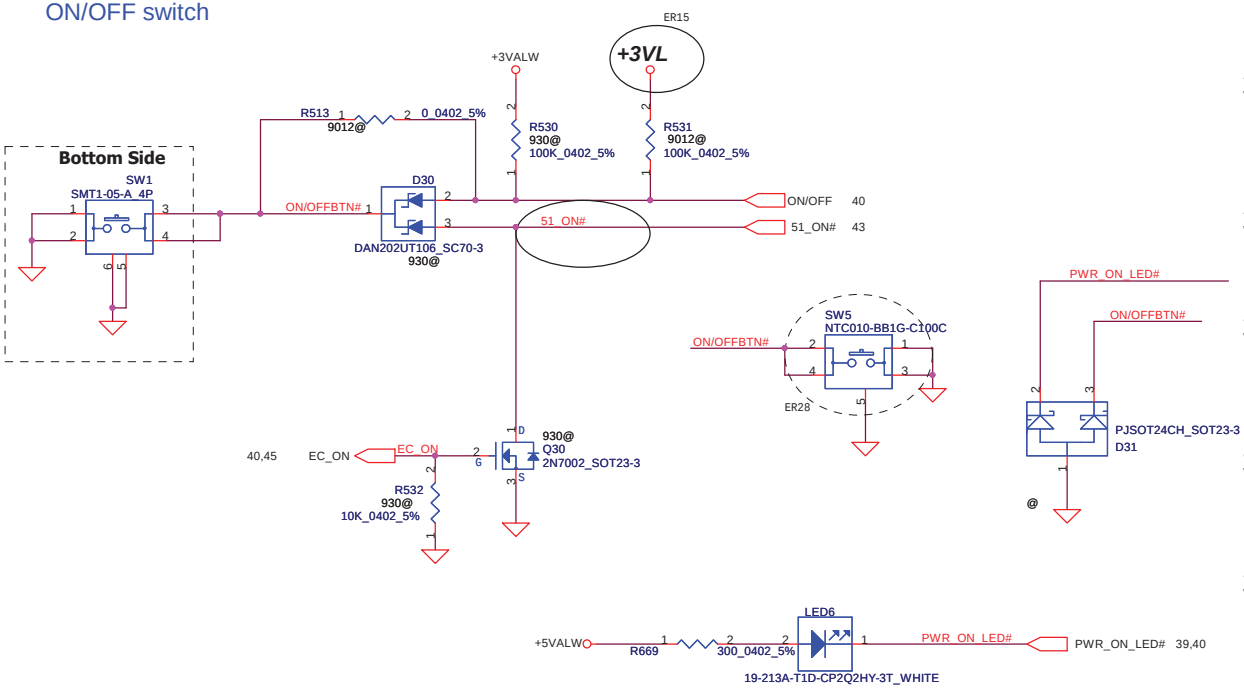
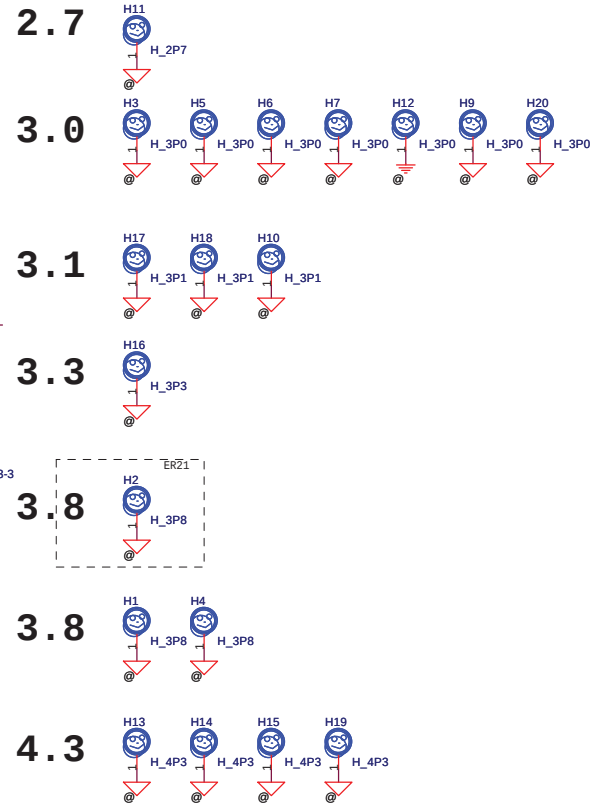
Power Button

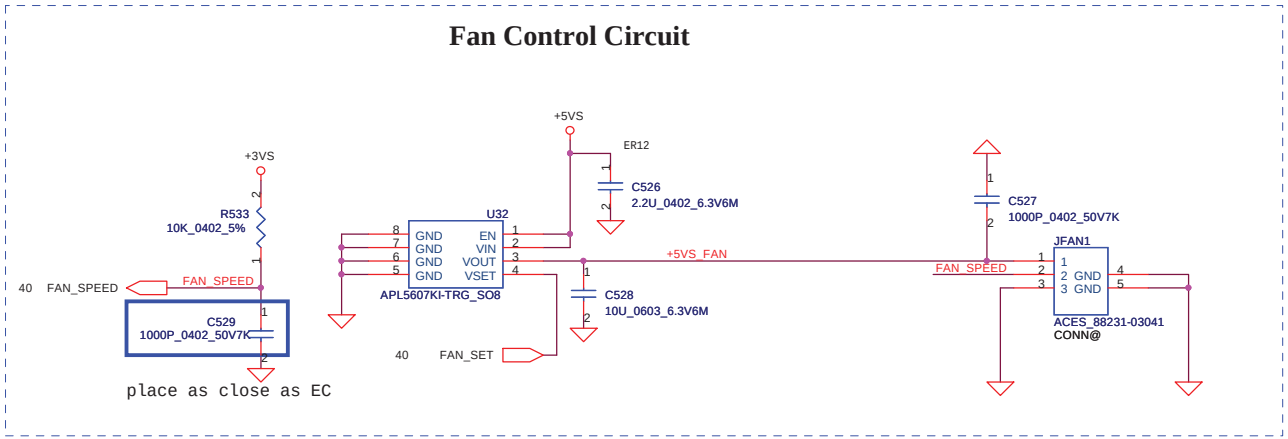
ON/OFF switch



Screw Hole



Fan Control Circuit



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

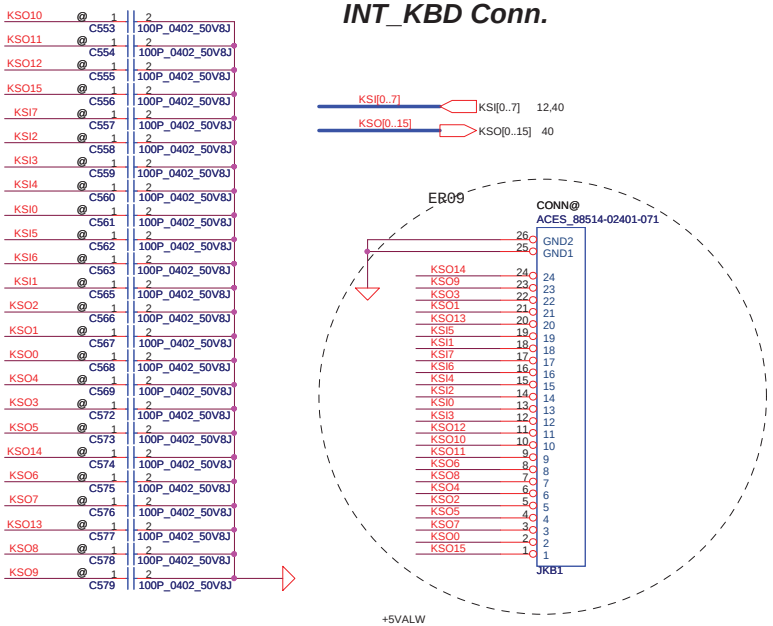
Compal Electronics, Inc.

Title: PWRBTN/ FAN / Screws

Size: Custom | Document Number: LA-8221P | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 38 of 58

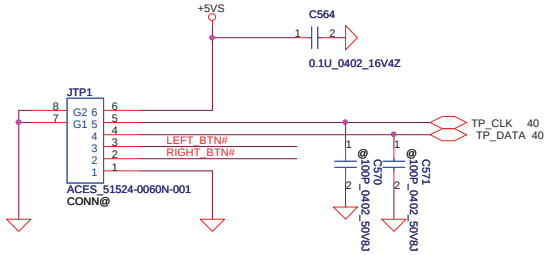
INT_KBD Conn.

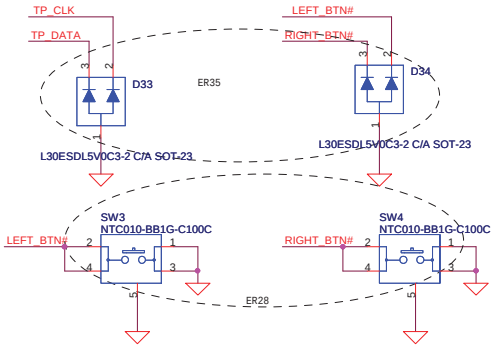


KSI[0..7] KSI[0..7] 12,40

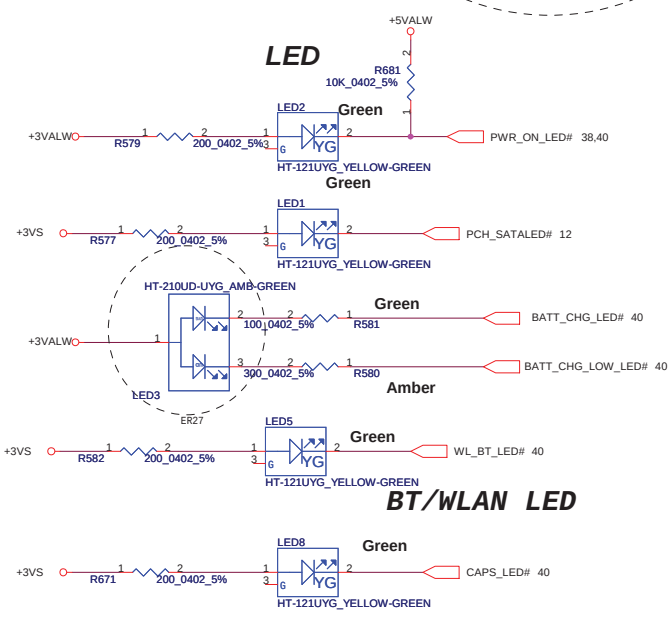
KSO[0..15] KSO[0..15] 40

Touch/B Connector

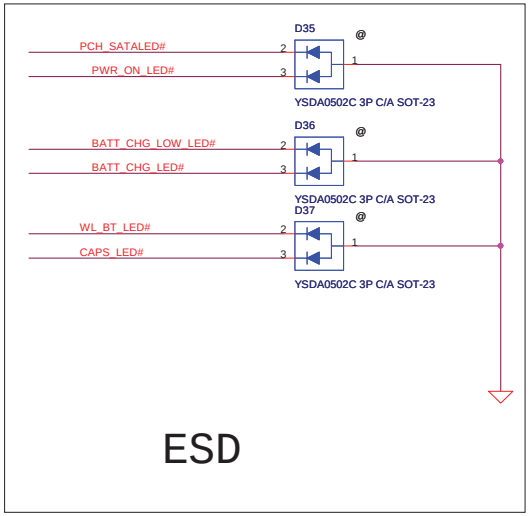




LED

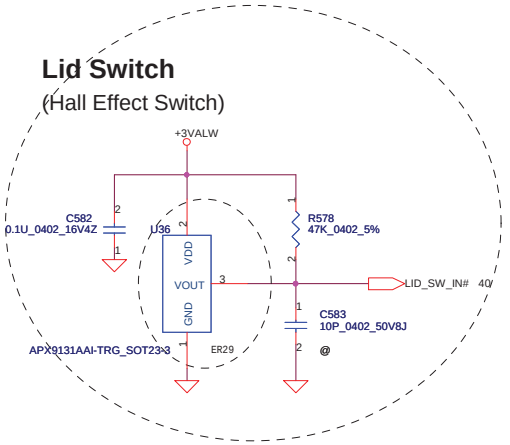


BT/WLAN LED



Lid Switch

(Hall Effect Switch)



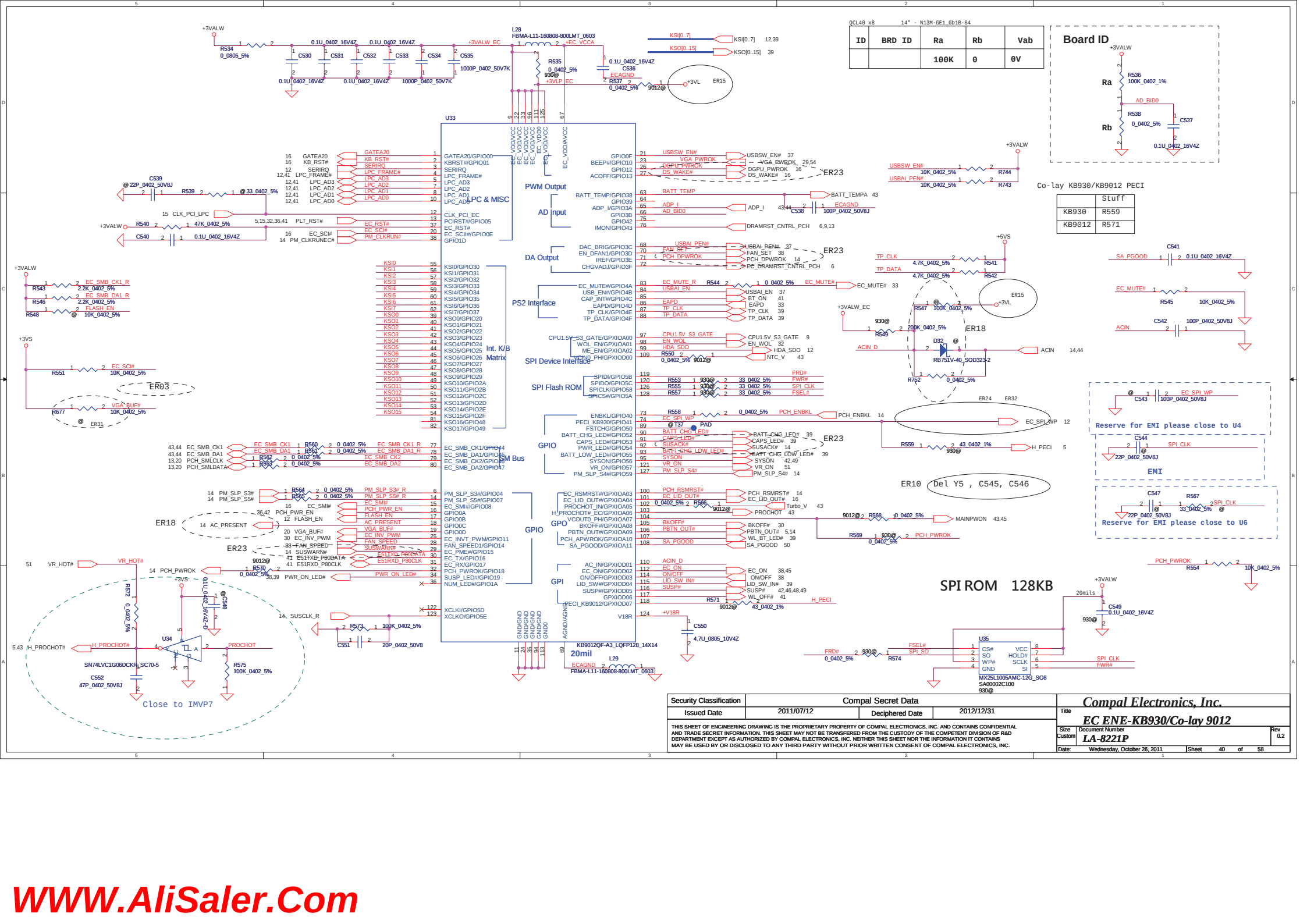
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

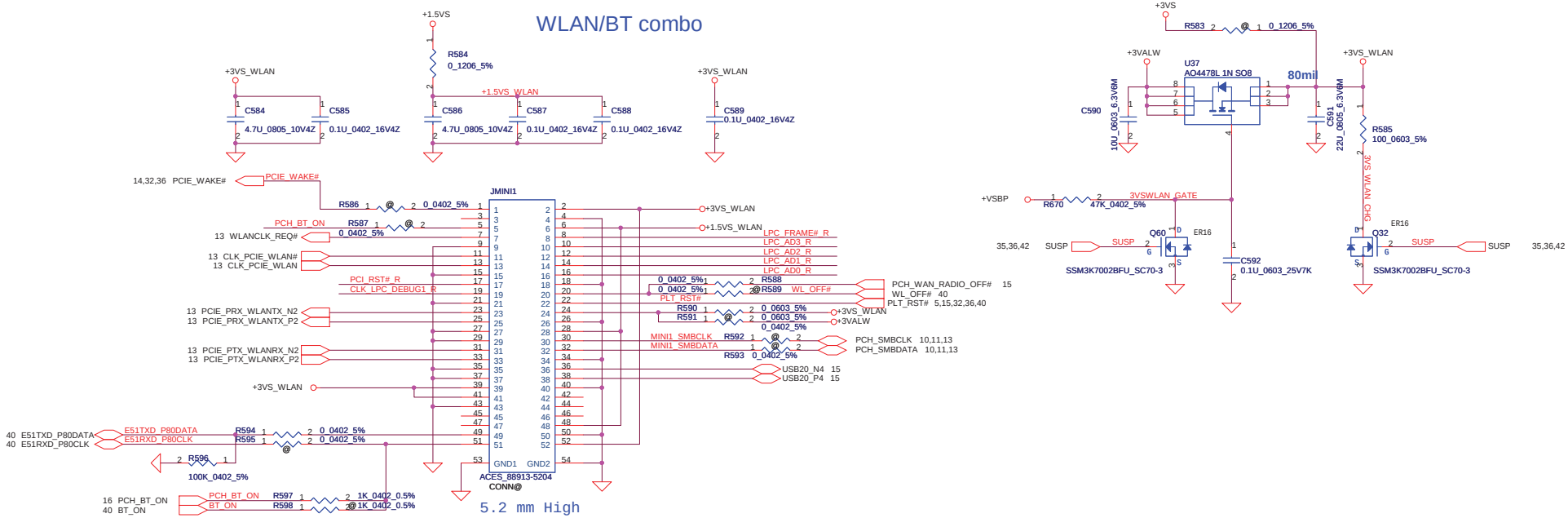
Title: KB/EC ROM/TP/FUN/LED

Size	Document Number	Rev
B	LA-8221P	0.2

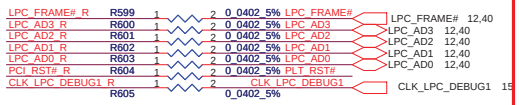
Date: Wednesday, October 26, 2011 Sheet 39 of 58

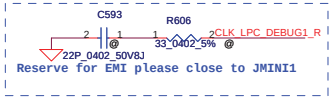


WLAN/BT combo



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.





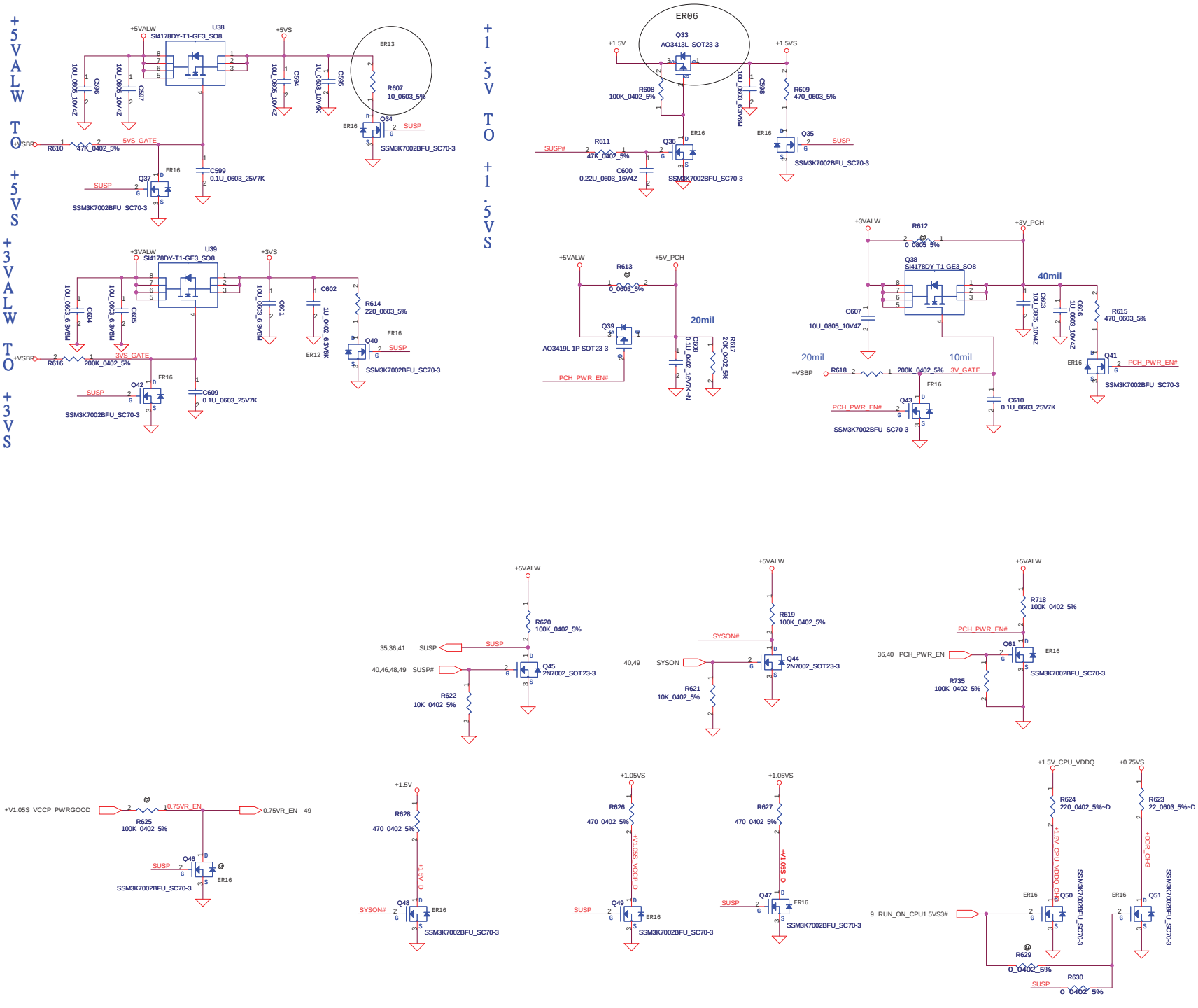
Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **WLAN/ WWAN/ m-SATA**

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 41 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/07/12	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: DC/DC Interface

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 42 of 58

DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

PJPDC1
GND_1
GND_2
GND_3
GND_4
V-
V+
V-
@SINGA_SDC2003-004111F

ADPIN

PL1 HCB2012KF-121T50_0805
PL2 HCB2012KF-121T50_0805

PC1 1000P_0402_50V7K
PC2 100P_0402_50V8J
PC3 1000P_0402_50V7K
PC5 100P_0402_50V8J

VIN

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56

VL
+3VL
+3VS

PC4 @0.1U_0603_16V7K

PU1
VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2
@G718TM1U_SOT23-8

PR5 @100K_0402_1%
PR2 1K_0402_1%
PR56 12.1K_0402_1%
PR3 @21.5K_0402_1%
PR4 @10K_0402_1%
PR6 @29.4K_0402_1%
PR7 20K_0402_1%
PH1 100K_0402_1%_NCP15WF104F03RC

PQ1 @SSM3K7002FU_SC70-3
PR73 @0_0402_5%
PR9 @0_0402_5%

40,44 ADP_I
5,40 H_PROCHOT#
40 PROCHOT
OTP_N_002
OTP_N_003
ADP_OCP_1
ADP_OCP_2
Turbo_V
NTC_V
MAINPWON 40,45

PJP2
@SUYIN_200045GR009G28DZR
EC_SMCA
EC_SMDA
TS_A
GND
GND

PL3 HCB2012KF-121T50_0805
PL4 HCB2012KF-121T50_0805
VMB
BATT+

PC6 1000P_0402_50V7K
PC128 10U_0805_25V6K
PC7 0.01U_0402_25V7K
PR27 1K_0402_1%

PD1 @PJSOT24CW_SOT323-3
PD2 @PJSOT24CW_SOT323-3

PR28 100_0402_1%
PR31 100_0402_1%
EC_SMB_CK1 40,44
EC_SMB_DA1 40,44

PR29 100K_0402_5%
+3VALW

PR30 1K_0402_1%
BATT_TEMPA 40

B+
+VSBP
VL
+3VL
+CHGRTC

PR13 100K_0402_1%
PC8 0.22U_0603_25V7K
PQ3 TP0610K-T1-E3_SOT23-3
PC9 0.1U_0603_25V7K
PR14 22K_0402_1%
VSB_N_001
VSB_N_003
PR16 100K_0402_1%
PR18 0_0402_5%
VSB_N_002
PQ4 SSM3K7002FU_SC70-3
PC10 .1U_0402_16V7K
45 POK

PJ3 JUMP_43X39

RTC Battery
PBJ1
@LOTES_AAA-BAT-054-K01
+RTCBATT

VIN
PD3 RLS4148_LL34-2
VS_N_001
BATT+
PD4 LL4148_LL34-2
PQ5 TP0610K-T1-E3_SOT23-3
N1
PR19 68_1206_5%
PR20 68_1206_5%
VS
PR23 100K_0402_1%
PC11 0.22U_0603_25V7K
PC12 0.1U_0603_25V7K
38 51_ON#
PR24 22K_0402_1%
VS_N_002

For KB9012 --> Remove all 51_ON# circuit

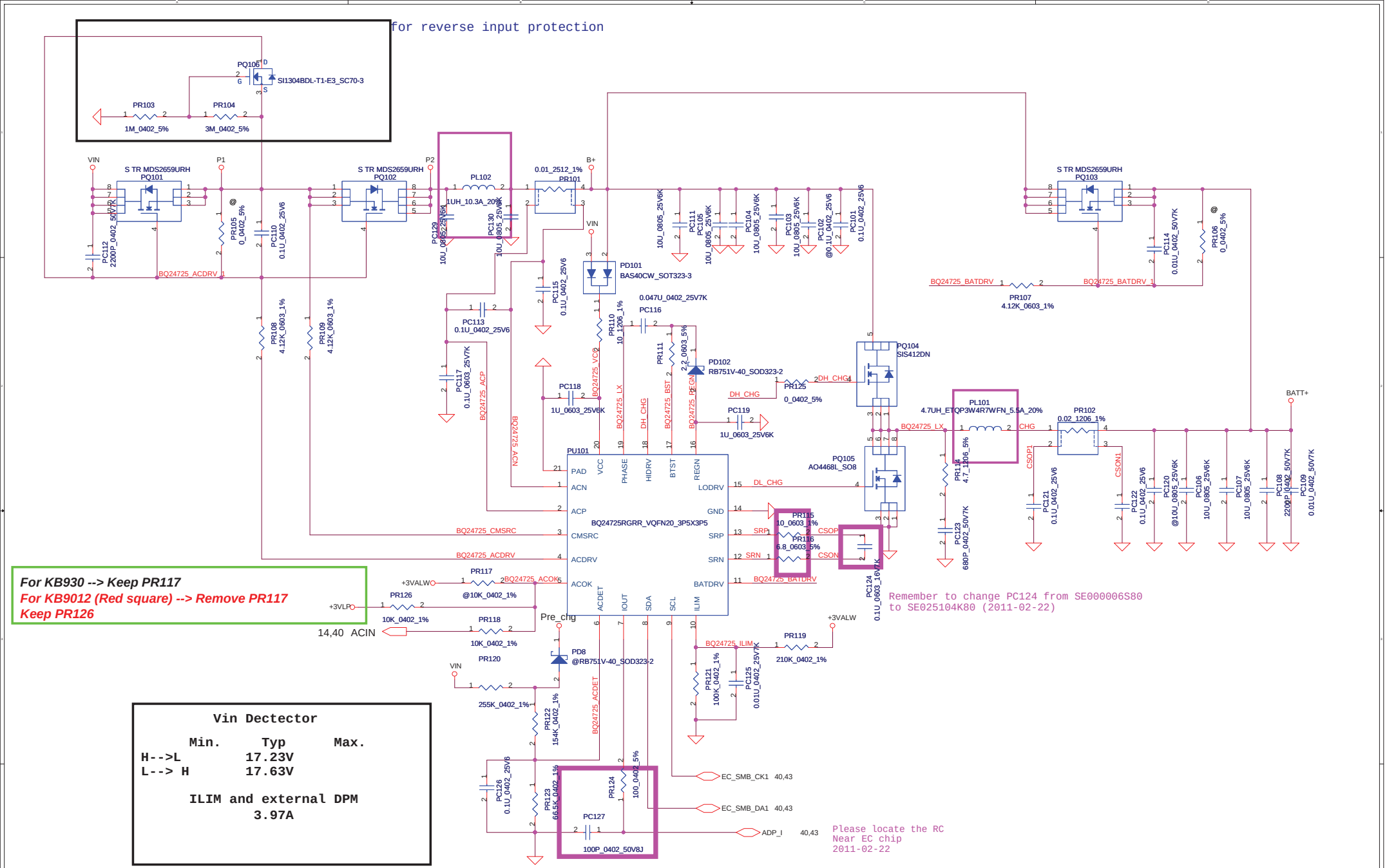
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

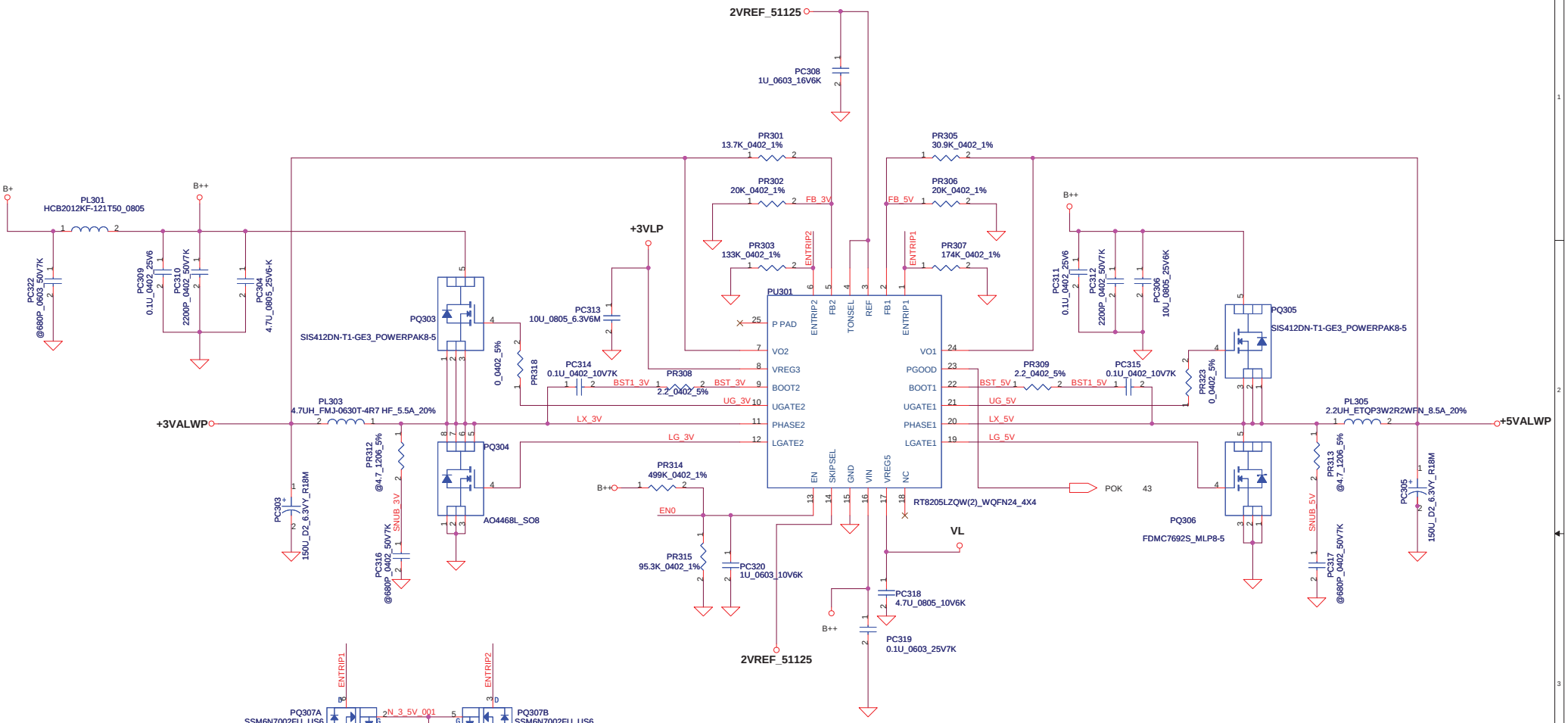
Size: | Document Number: PBL22 LA-7391P M/B | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 43 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.			
Title	PWR-CHARGER		
Size	Document Number	PBL22 LA-7391P M/B	Rev 0.2
Date: Wednesday, October 26, 2011	Sheet 44 of 58		



For KB930 --> Keep PR319, Remove PR322
For KB9012 (Red square) --> Remove PR319
Keep PR322

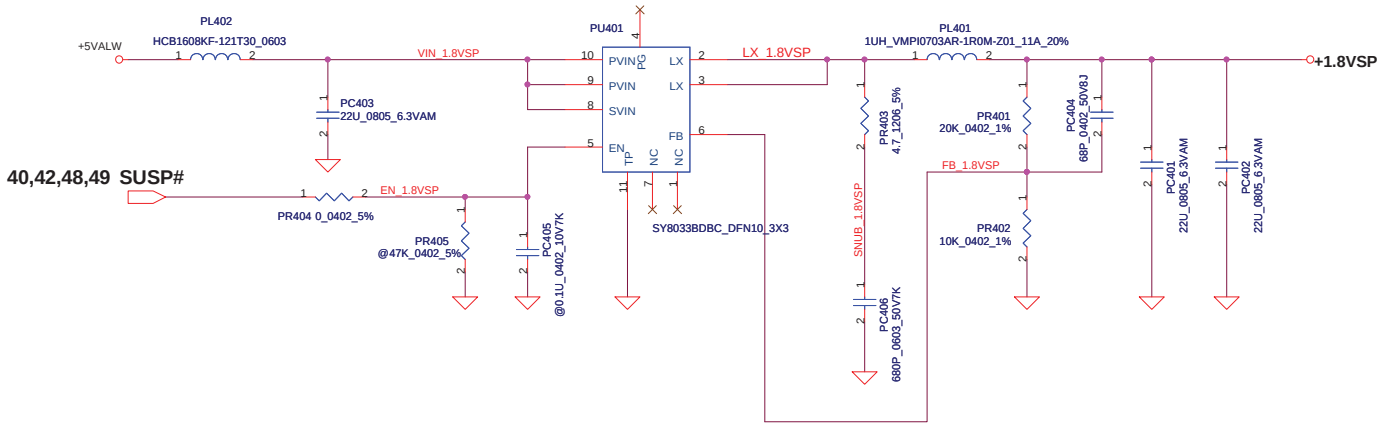
Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **PWR-3.3VALWP/5VALWP**

Size	Document Number	Rev
Custom	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 45 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **PWR-1.8VSP**

Size	Document Number	Rev
	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 46 of 58

(8.5A,360mils ,Via NO.= 17)

PJP606,PJP607先斷開,確定拿掉PU605再接上

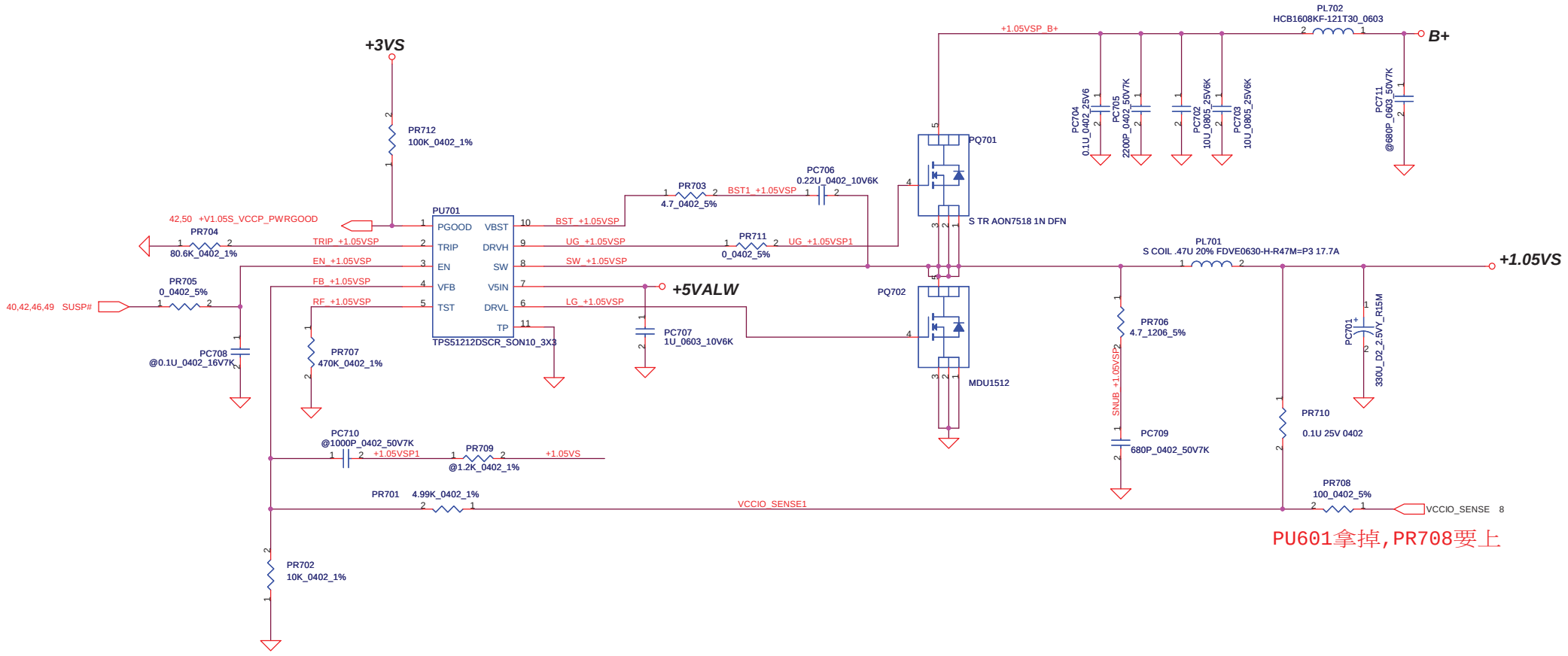
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **PWR-V1.05S_VCCP**

Size: Custom | Document Number: PBL22 LA-7391P M/B | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 47 of 58



PU601拿掉,PR708要上

(12A,480mils ,Via NO.= 24)

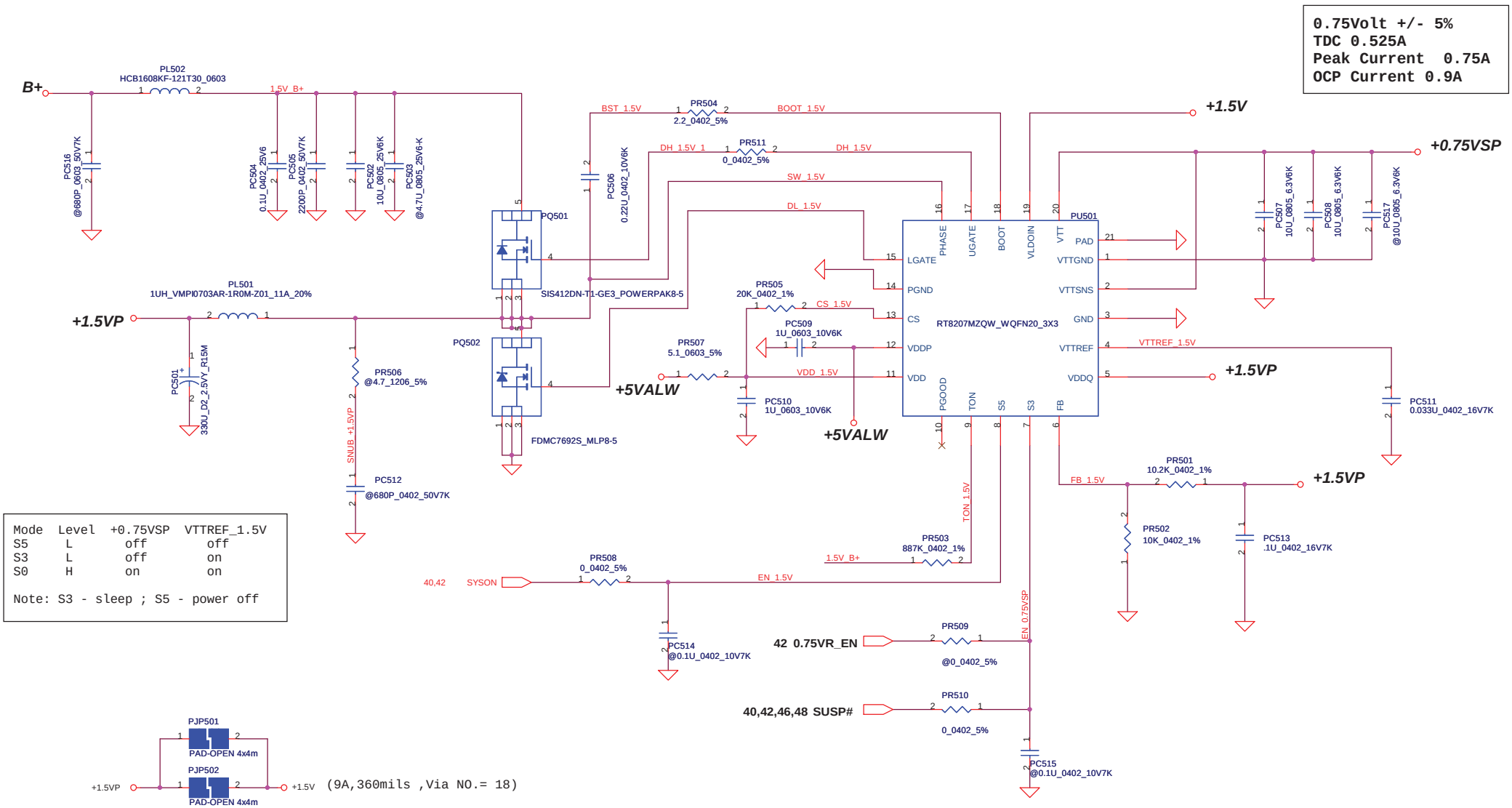
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-V1.05SP

Size: Custom | Document Number: PBL22 LA-7391P M/B | Rev: 0.2

Date: Wednesday, October 26, 2011 | Sheet 48 of 58



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

Size: Custom | Document Number: PBL22 LA-7391P M/B | Rev: 0.2

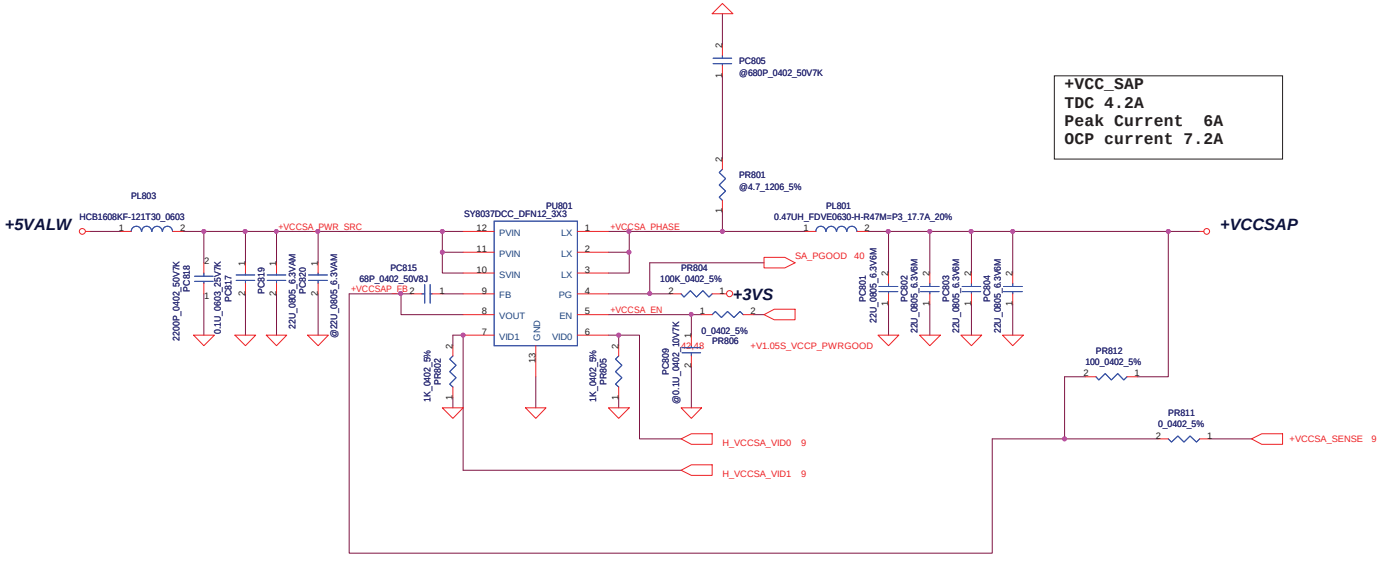
Date: Wednesday, October 26, 2011 | Sheet 49 of 58

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A



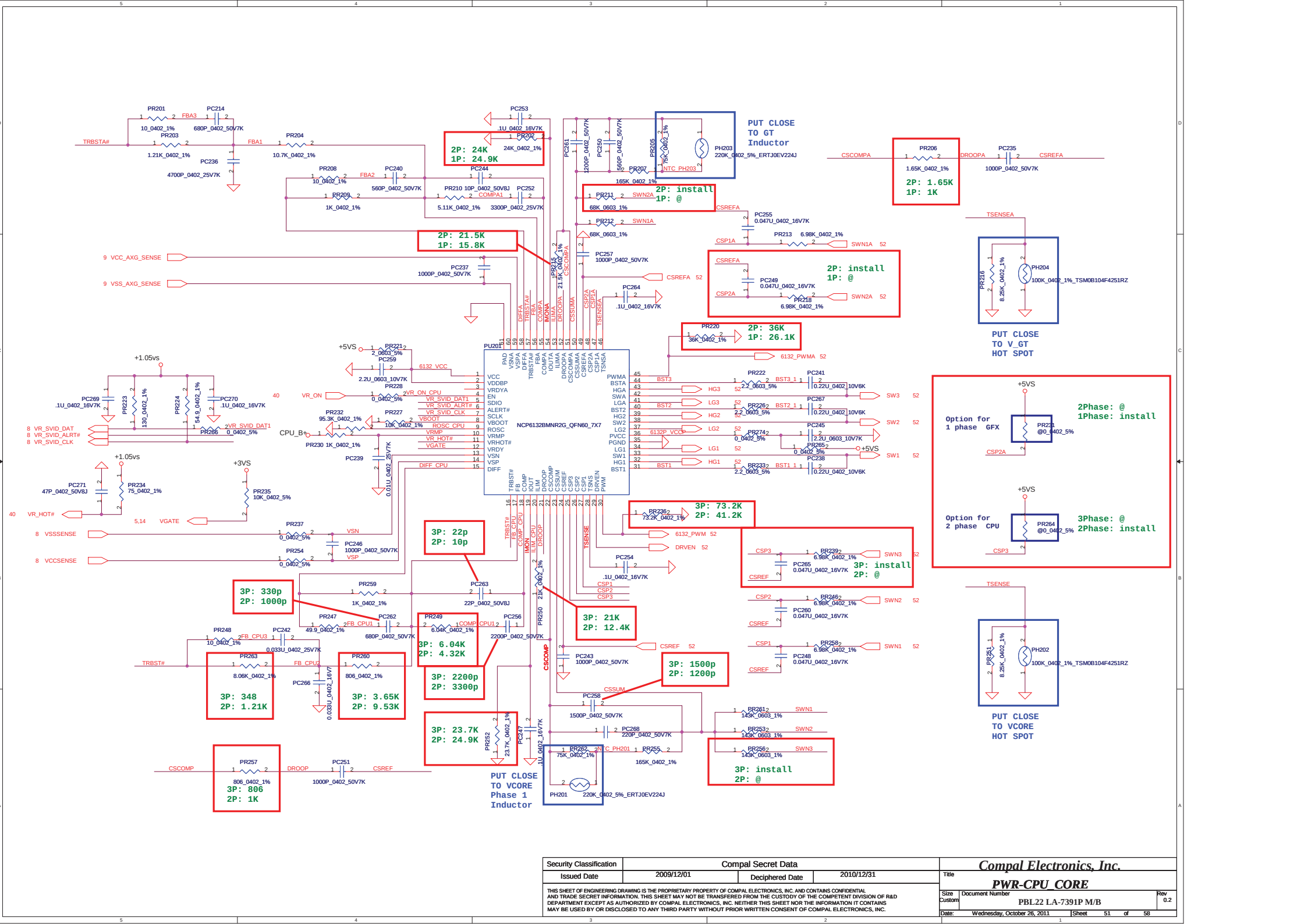
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size	Document Number	Rev
C	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 50 of 58



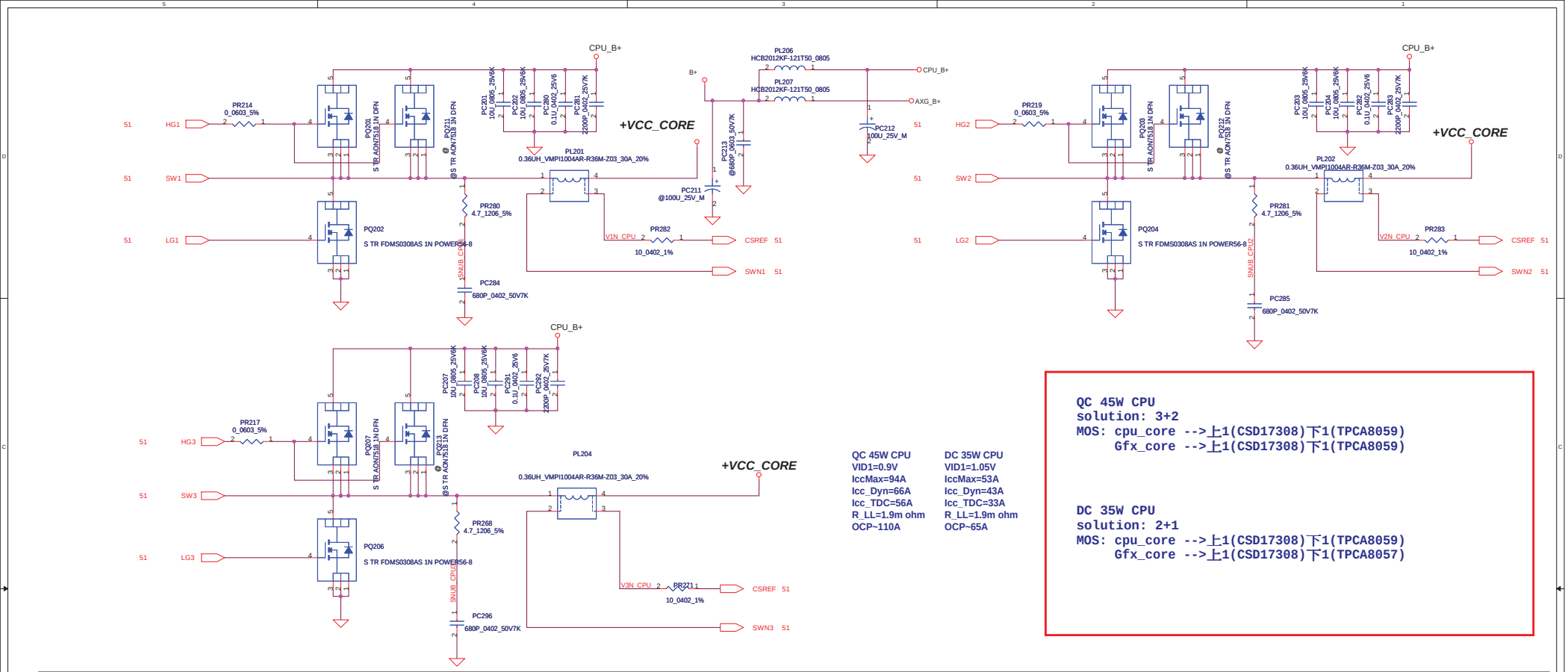
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.2

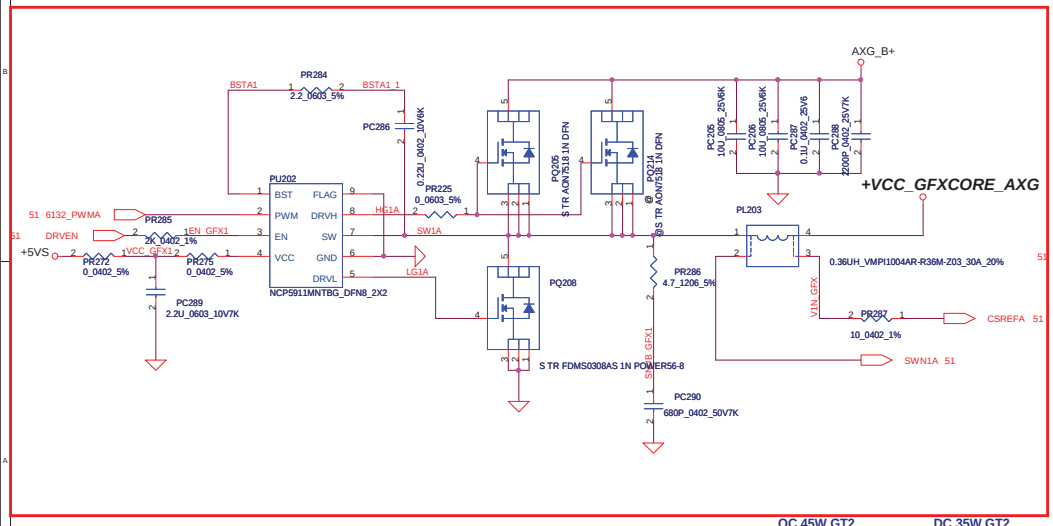
Date: Wednesday, October 26, 2011 Sheet 51 of 58



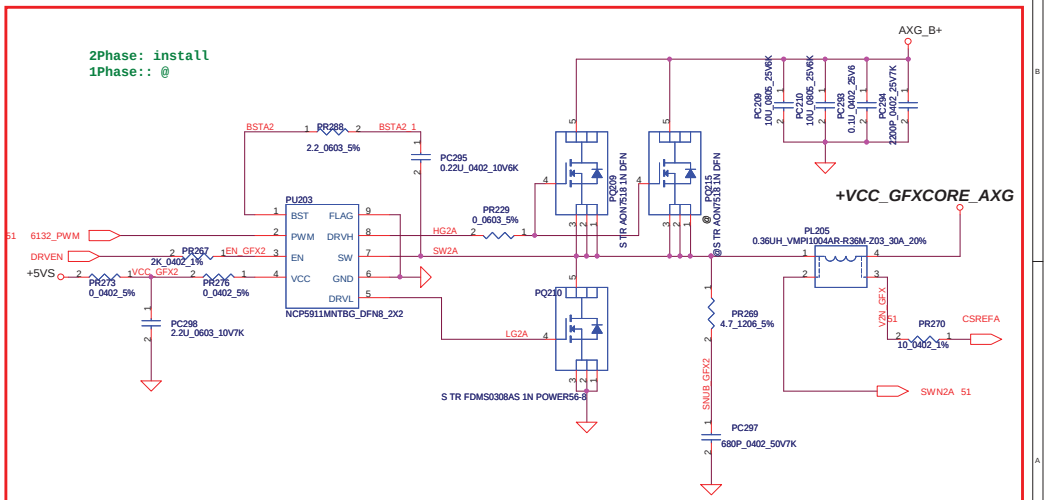
QC 45W CPU
solution: 3+2
MOS: cpu_core -->上1(CSD17308)下1(TPCA8059)
Gfx_core -->上1(CSD17308)下1(TPCA8059)

DC 35W CPU
solution: 2+1
MOS: cpu_core -->上1(CSD17308)下1(TPCA8059)
Gfx_core -->上1(CSD17308)下1(TPCA8057)

QC 45W CPU	DC 35W CPU
VID1=0.9V	VID1=1.05V
IccMax=94A	IccMax=53A
Icc_Dyn=66A	Icc_Dyn=43A
Icc_TDC=56A	Icc_TDC=33A
R_LL=1.9m ohm	R_LL=1.9m ohm
OCP~110A	OCP~65A



2Phase: install
1Phase:: @



QC 45W GT2	DC 35W GT2
VID1=1.23V	VID1=1.23V
IccMax=46A	IccMax=33A
Icc_Dyn=37A	Icc_Dyn=20.2A
Icc_TDC=38A	Icc_TDC=21.5A
R_LL=3.9m ohm	R_LL=3.9m ohm
OCP~55A	OCP~40A

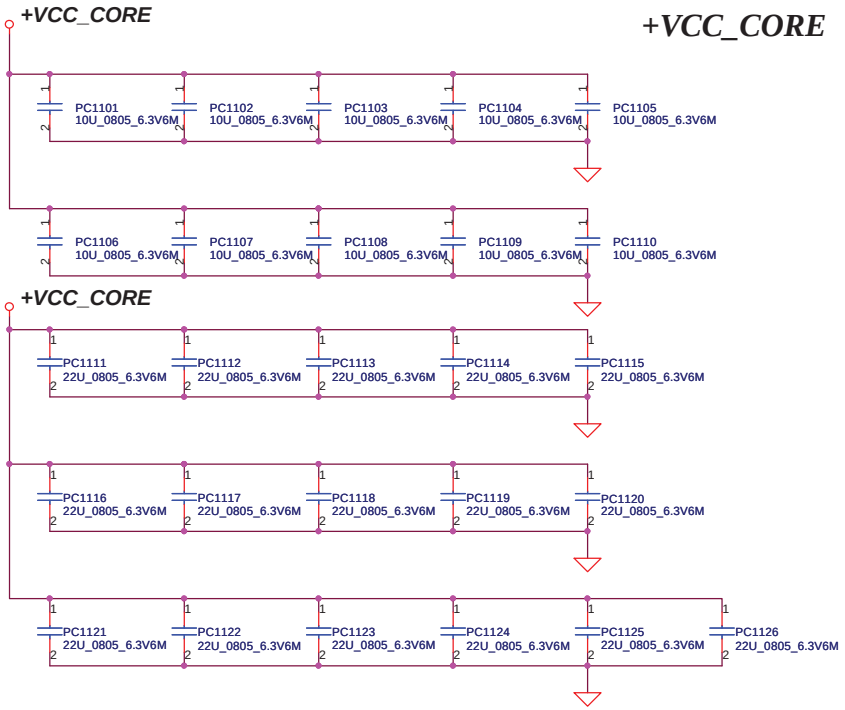
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

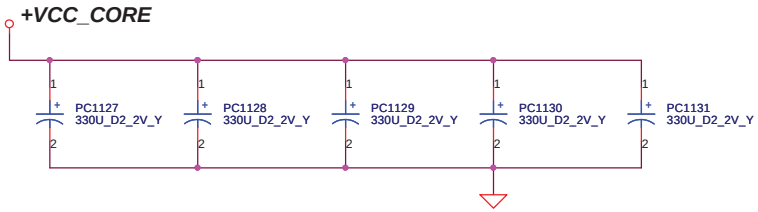
Compal Electronics, Inc.

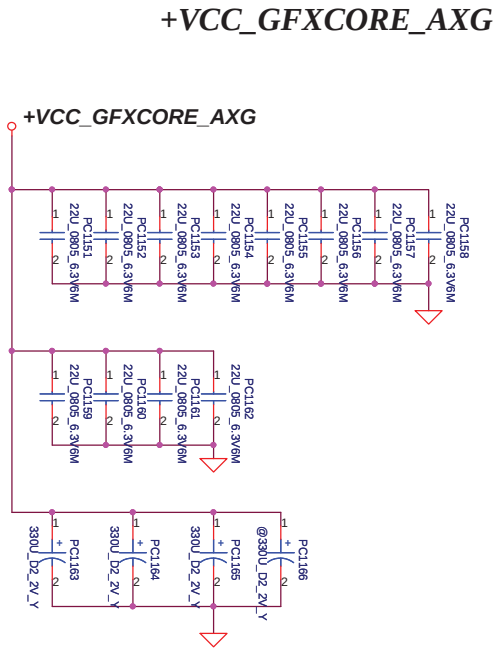
Title: PWR-CPU_CORE

Size	Document Number	Rev
C	PBL22 LA-7391P M/B	0.2

Date: Wednesday, October 26, 2011 Sheet 52 of 58

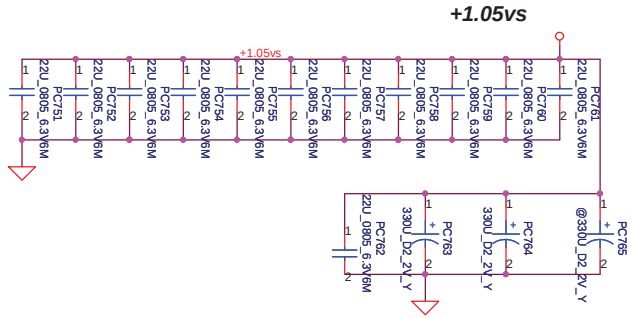






Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

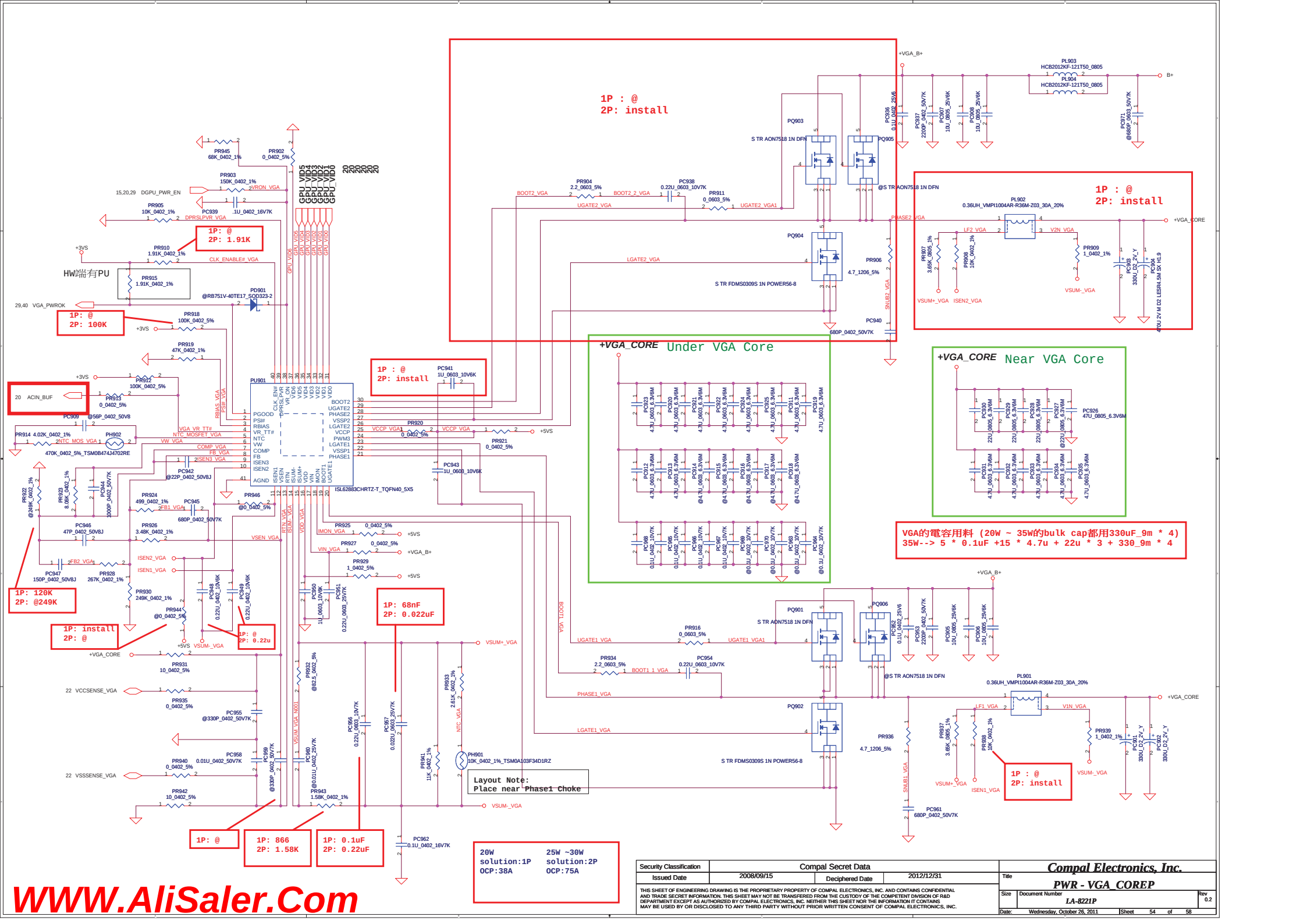
Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-8221P	0.2

Date: Wednesday, October 26, 2011 Sheet 53 of 58


1P : @
2P: install
+VGA_B+
PL903
HCB2012KF-121T50_0805
PL904
HCB2012KF-121T50_0805
B+
PQ903
S TR AON7518 1N DFN
PQ905
@S TR AON7518 1N DFN
PR904
2.2_0603_5%
BOOT2_VGA
BOOT2_2_VGA
PC938
0.22U_0603_10V7K
PR911
0_0603_5%
UGATE2_VGA
UGATE2_VGA1
PHASE2_VGA
PQ904
LGATE2_VGA
S TR FDMS0309S 1N POWER56-8
PR906
4.7_1206_5%
SNUB2_VGA
PC940
680P_0402_50V7K
PL902
0.36UH_VMPI1004AR-R36M-Z03_30A_20%
+VGA_CORE
LF2_VGA
V2N_VGA
PR907
3.65K_0805_1%
PR908
10K_0402_1%
PR909
1_0402_1%
VSUM+_VGA
ISEN2_VGA
VSUM-_VGA
PC903
330U_D2_2V_Y
PC904
470U 2V M D2 LESR4.5M 5X 11.9
1P : @
2P: install
+VGA_CORE Under VGA Core
+VGA_CORE Near VGA Core
PC926
47U_0805_6.3V6M
VGA的電容用料 (20W ~ 35W的bulk cap都用330uF_9m * 4)
35W--> 5 * 0.1uF +15 * 4.7u + 22u * 3 + 330_9m * 4
PR945
68K_0402_1%
PR902
0_0402_5%
PR903
150K_0402_1%
15,20,29 DGPU_PWR_EN
VRON_VGA
PR905
10K_0402_1%
DPRSLPVR_VGA
PC939
.1U_0402_16V7K
GPU_VID5
GPU_VID4
GPU_VID3
GPU_VID2
GPU_VID1
GPU_VID0
1P: @
2P: 1.91K
+3VS
PR910
1.91K_0402_1%
CLK_ENABLE#_VGA
HW端有PU
PR915
1.91K_0402_1%
PD901
@RB751V-40TE17_SOD323-2
29,40 VGA_PWROK
1P: @
2P: 100K
PR918
100K_0402_5%
PR919
47K_0402_1%
PR912
100K_0402_5%
20 ACIN_BUF
PR913
0_0402_5%
PC909
@56P_0402_50V8
PR914 4.02K_0402_1%
PH902
470K_0402_5%_TSM0B474J4702RE
NTC_MOS_VGA
VGA_VR_TT#
NTC_MOSFET_VGA
VW_VGA
COMP_VGA
FB_VGA
ISEN3_VGA
PC942
@22P_0402_50V8J
PR923
8.06K_0402_1%
PR922
@249K_0402_1%
PC944
1000P_0402_50V7K
PR924
499_0402_1%
PC945
680P_0402_50V7K
PR946
@0_0402_5%
PC946
47P_0402_50V8J
PR926
3.48K_0402_1%
PC947
150P_0402_50V8J
PR928
267K_0402_1%
PR930
249K_0402_1%
1P: 120K
2P: @249K
PR944
@0_0402_5%
1P: install
2P: @
PC948
0.22U_0402_10V6K
PC949
0.22U_0402_10V6K
1P: @
2P: 0.22u
PU901
ISL62883CHRTZ-T_TQFN40_5X5
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
ISEN3
ISEN2
AGND
CLK_EN#
PRSLPVR
VR_ON
VID5
VID4
VID3
VID2
VID1
VID0
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
PWM3
LGATE1
VSSP1
PHASE1
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
BOOT1
UGATE1
1P : @
2P: install
PC941
1U_0603_10V6K
PR920
0_0402_5%
VCCP_VGA
+5VS
PR921
0_0402_5%
PC943
1U_0603_10V6K
PR925
0_0402_5%
IMON_VGA
PR927
0_0402_5%
VIN_VGA
+VGA_B+
PR929
1_0402_5%
PC950
1U_0603_10V6K
PC951
0.22U_0603_25V7K
1P: 68nF
2P: 0.022uF
VSUM+_VGA
PR932
@82.5_0402_5%
PR933
2.61K_0402_1%
NTC_VGA
PC956
0.22U_0603_10V7K
PC957
0.022U_0603_25V7K
PR941
11K_0402_1%
PH901
10K_0402_1%_TSM0A103F34D1RZ
Layout Note:
Place near Phase1 Choke
PR943
1.58K_0402_1%
VSUM-_VGA
PC962
0.1U_0402_16V7K
1P: @
1P: 866
2P: 1.58K
1P: 0.1uF
2P: 0.22uF
PQ901
S TR AON7518 1N DFN
PQ906
PR916
0_0603_5%
UGATE1_VGA
UGATE1_VGA1
PR934
2.2_0603_5%
BOOT1_1_VGA
PC954
0.22U_0603_10V7K
PHASE1_VGA
PQ902
LGATE1_VGA
S TR FDMS0309S 1N POWER56-8
PR936
4.7_1206_5%
SNUB1_VGA
PC961
680P_0402_50V7K
@S TR AON7518 1N DFN
PL901
0.36UH_VMPI1004AR-R36M-Z03_30A_20%
LF1_VGA
V1N_VGA
PR937
3.65K_0805_1%
PR938
10K_0402_1%
PR939
1_0402_1%
VSUM+_VGA
ISEN1_VGA
VSUM-_VGA
PC901
330U_D2_2V_Y
PC902
330U_D2_2V_Y
1P : @
2P: install
20W
solution:1P
OCP:38A
25W ~30W
solution:2P
OCP:75A
Security Classification
Compal Secret Data
Issued Date
2008/09/15
Deciphered Date
2012/12/31
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Title
PWR - VGA_COREP
Size
Document Number
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Rev
0.2
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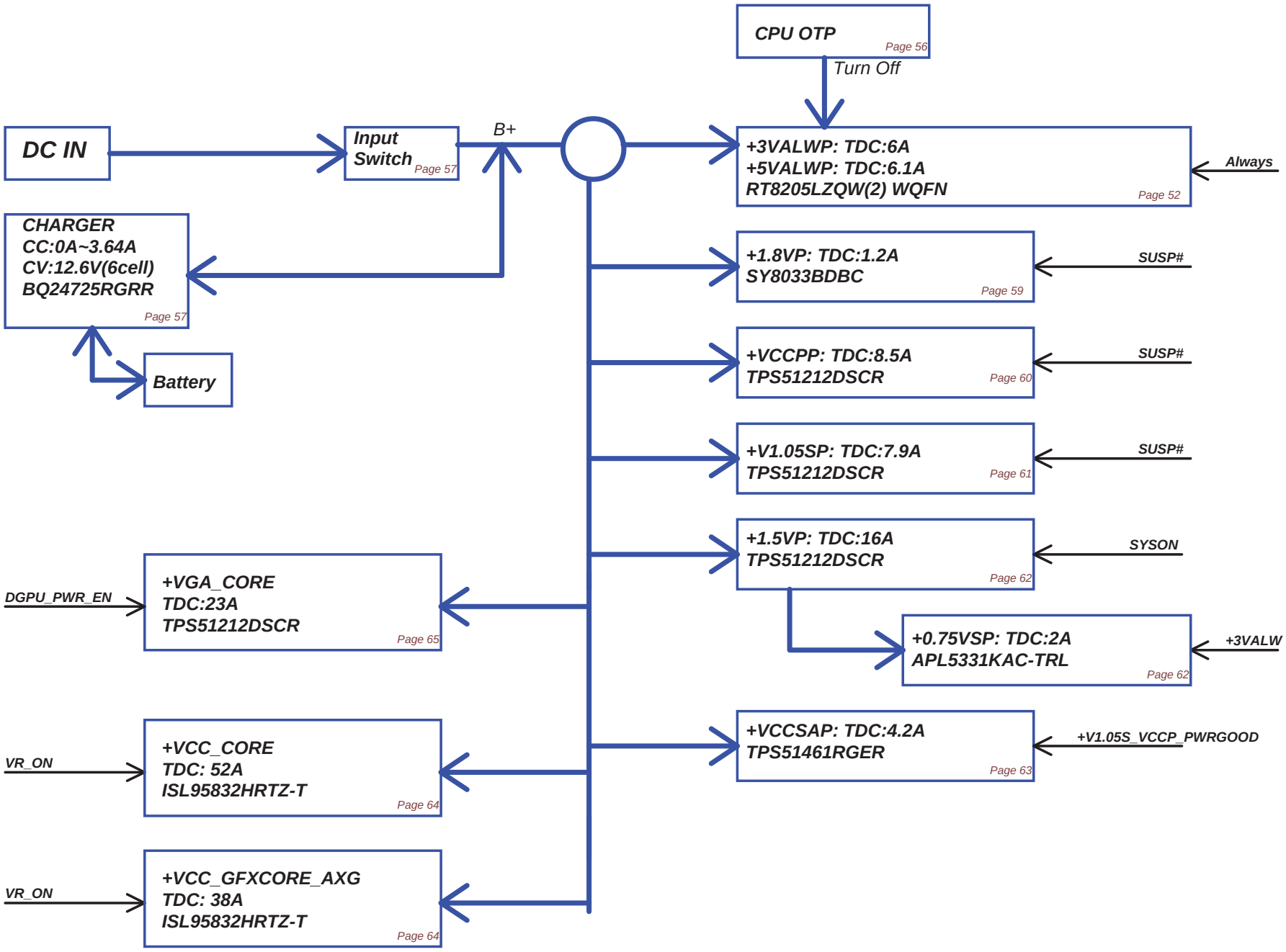
Power block



Security Classification	Compal Secret Data		
Issued Date	2010/08/03	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: POWER BLOCK DIAGRAM

Size	Document Number	Rev
Custom	LA-8221P	0.2

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	PWR - PIR		
Size	Document Number		Rev
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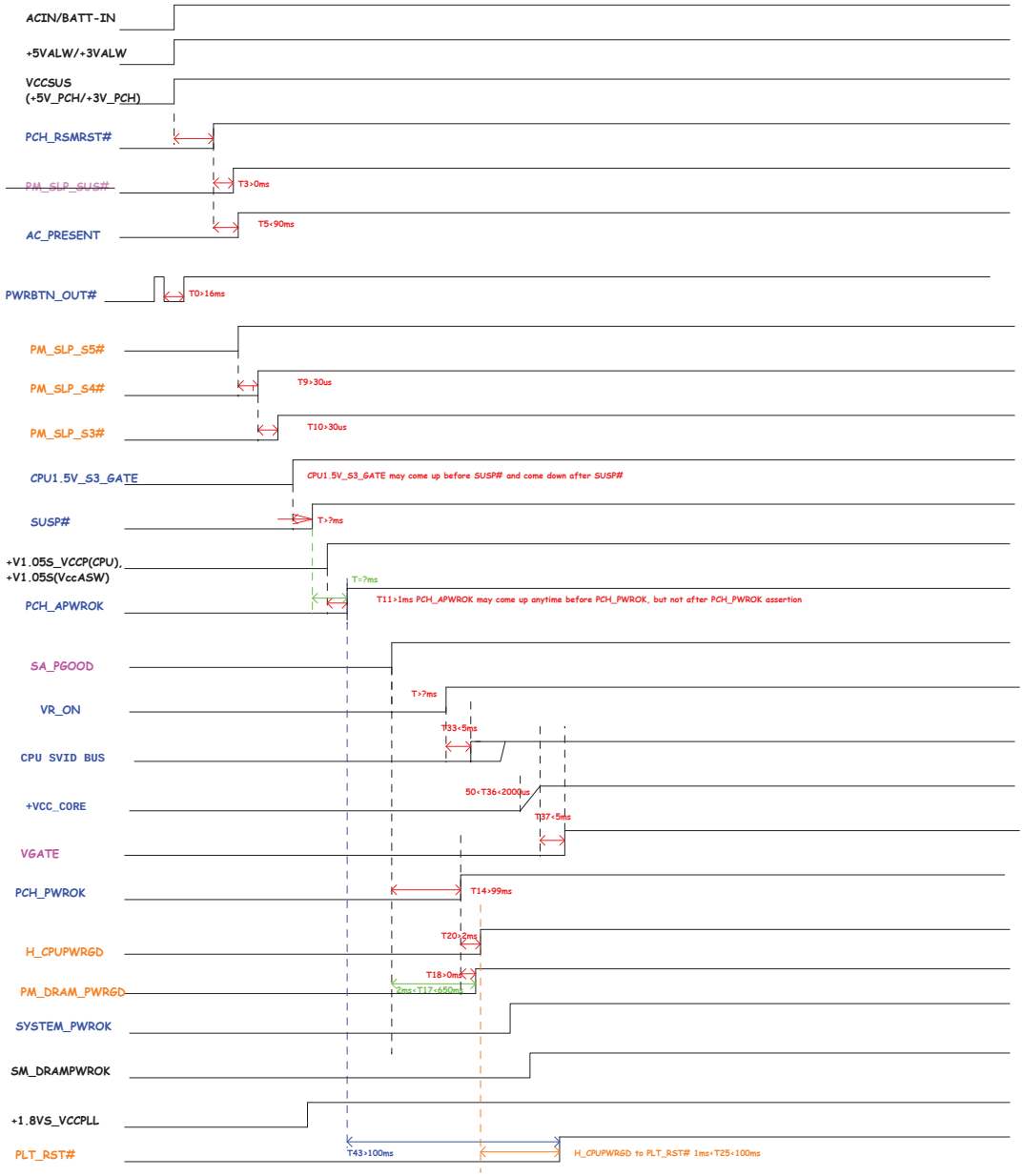
Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Title: Power Sequence
Size: B | Document Number: LA-8221P | Rev: 0.4
Date: Wednesday, October 26, 2011 | Sheet: 57 of 58

Version Change List (P. I. R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		Add USB3.0(ASM1042) & non AI co-lay	0.2	36 37	Add ASM1042 co-lay AI parts change to AI@	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13 40	Delete Q3. (connect pin S & D) remove R135, R137 Del R552, R556	09/21	
ER04		Design change for card reader	0.2	34	Add Q20,R773,R775 Reserve R768,R774. Change Net name at Card reader Conn	09/21	
ER05		HW Design (PURC demand)	0.2	29	Change to Q3(AO3404L) from U22(AO4430L)	09/21	
ER06		HW Design (PURC demand)	0.2	42	Change Q33 to AO3413L from AP2301GN	09/21	
ER07		Fine-tune GPU timing	0.2	29	Change R433 to 0 ohm un-stuff C396 Change R432 to 10K Change R435 to 200 ohm	09/21	
ER08		HW Design (reserve)	0.2	18	Reserve R290	09/21	
ER09	KB connector reverse	HW Design (change)	0.2	39	Reverse JKB1 connector	09/30	
ER10		HW Design	0.2	40	Del Y5 , C545 , C546	09/30	
ER11		HW Design (PURC demand)	0.2	15	Del R229,R230 (10K) Add R776~R783 (10K) Del R237,R239,R242 (8.2K) Add R784~R793 (8.2K)	09/30	
ER12		HW Design (PURC demand)	0.2	29,31 37,38 10,11	Change P/N C387,C389,C399,C436,C447,C602 Change P/N C509,C515,C518,C526.(0402) Change P/N C99,C109,C118,C120,C140,C141.(0402)	10/03	
ER13		HW Design(XTAL fine-tune)	0.2	42,12 13,32 20,36	Change R607 to 10 ohm Change Y3,C241,C242. Change Y1,C144,C145 Change Y4,C469,C473. Change Y2,C163,C164 Change Y9	10/07	
ER14		HW Design for instant on function	0.2	13 5	Reserve R750 R576 pin2 change to +3V_PCH from +3VS Change R576 to 0	10/07	
ER15		HW Design (power jumper change to +3VL)	0.2	38 40	jumper PJP302 (change +3VLP to +3VL @P38,P40)	10/07	
ER16		HW Design (PURC demand)	0.2		Change P/N Q7,U20,U21. Change P/N Q14~Q19,Q25,Q27~Q29,Q32,Q34~Q37,Q40~Q43, Q46~Q51,Q55~Q57,Q60,Q61,Q902,Q903,Q905. Change P/N Q23	10/14	
ER17		EMI solution	0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
ER18		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/14	
ER19		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/14	
ER20		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R242 Add C149 0.1uf Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER21		Modify H2 size	0.2	38	Modify H2 size	10/17	

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			Date: Wednesday, October 26, 2011; Sheet 58 of 58

Version Change List (P. I. R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER22		Refer to Intel review feedback item 45.	0.2	16	Add R807	10/19	
ER23		Reserve for Deep Sx	0.2	14,16 40	Add unstuff R800,R801,R802,R803,R804,R805 Add PCH_DPWROK,DS_WAKE#,SUSACK#,SUSWARN#	10/19	
ER24		Reserve for ROM protect	0.2	40	Add unstuff R806	10/19	
ER25		For Instant On function control by EC	0.2	06	Stuff R44, Unstuff R43	10/19	
ER26		For EMI request	0.2	36	Reserve R1082 , C1045	10/19	
ER27		For LED issue	0.2	39	change LED3 footprint to LED_HT-210UD-UYG_3P	10/20	
ER28		For PRUC request	0.2	38 39	Change SW3,SW4,SW5 P/N	10/20	
ER29		For PRUC request	0.2	39	Change U36 P/N	10/20	
ER30		For EMI request (without MS_CLK)	0.2	34	Remove R637,C611,R631,C620.	10/20	
ER31		dGPU thermal throttling.	0.2	20 40	Add R428, Revise U11 I/O signal. Un-stuff R730.	10/20	
ER32		SPI flash data crisis prevention.	0.2	12 40	Add Q63, R135, R137. Change U33.41 net to EC_SPI_WP. remove R806.	10/20	
ER33		Power switch EOS issue prevention.	0.2	37	Change C510, C516, C519 to 0.22uF/16V.	10/20	
ER34		For EMI request	0.2	32 35	Change R485 , R486 to 0.1uF Reserve C641~C648	10/20	
ER35		For ESD request	0.2	37,35 30,39	Change D27,D29,D24,D25. Change D6,D7,D9,D10,D33,D34.	10/20	
ER36		Modify X76 table (N13P-GS)	0.2	22	update X76 table (Strap1,Strap2,Strap3)	10/24	
ER37		Modify X76 table (N13P-GS & N13M-GE1 x8)	0.2	3	update X76 table (add ZZZ9 ~ZZZ12 for N13P-GS & N13M-GE1 x8) & update P/N	10/25	
ER38		Modify PCH_SPI_WP# singal control by EC	0.2	12	Stuff R135	10/26	

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Title: EE-PIR-2

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