

# ACER\_BAP31

## MAIN BOARD

2008.12.29

Tuesday, March 10, 2009		X01
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE ACER JM31			
DESIGN								
CHECK								
RESPONSIBLE								
SIZE=					SIZE	CODE	DOC NUMBER	REV
FILE NAME: XXXX.XXXXXXXX					C	X01	D-CS-1310A2284501.ALG	X01
PN	XXXXXXXXXXXX				SHEET 1 of 38			

# 1. Schematic Page Description :

## Montevina Schematic Ver : X01

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal

18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)
24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/IDE/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

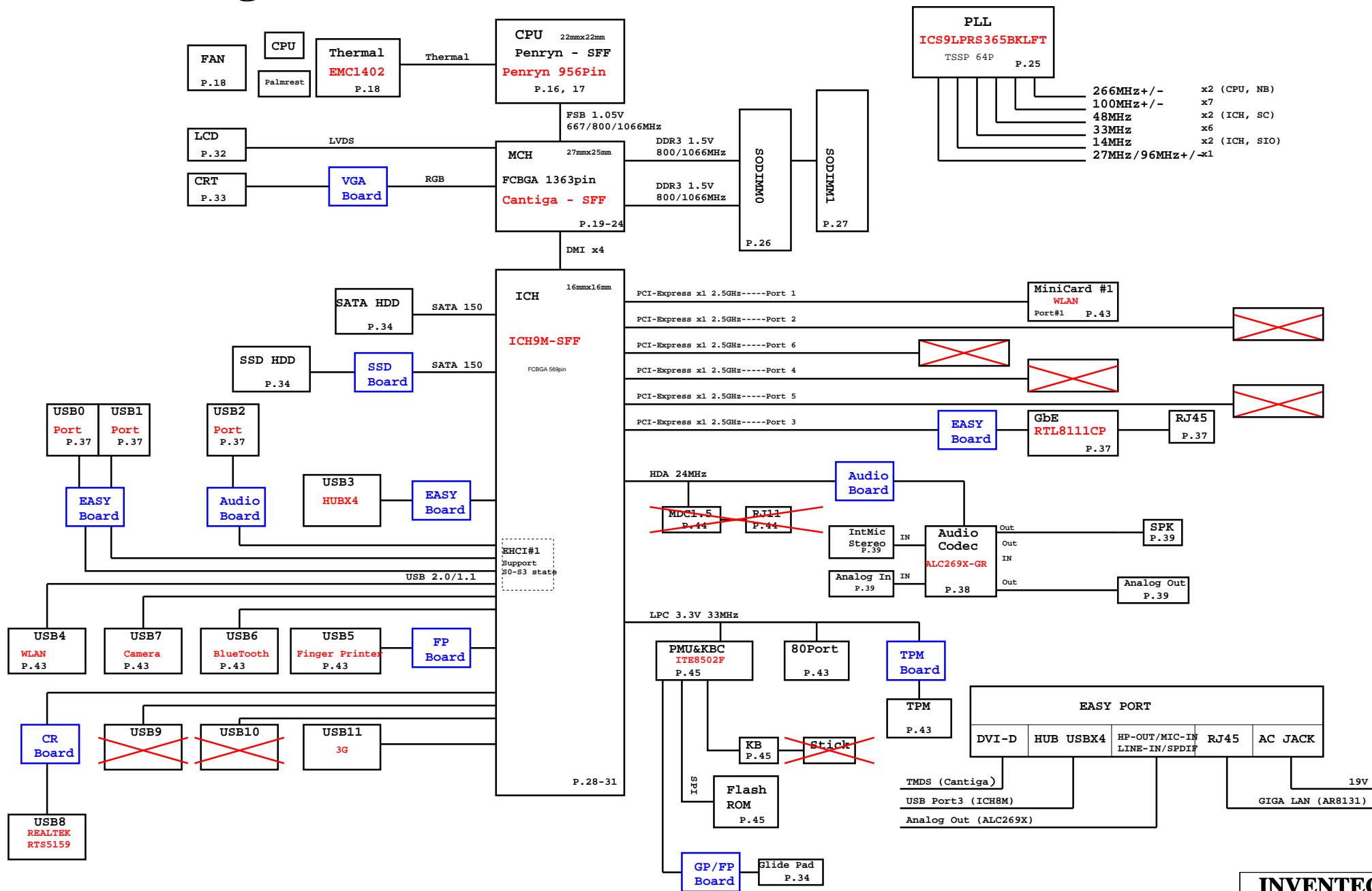
31. LCD CNN/SATA/3G/WLAN

32. KBC ITE8512F

33. IO CN

INVENTEC			
TITLE			
BAP31 (Penryn+Cantiga+ICH9M)SFF			
Schematic Page			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A284501-ALG	X01
SHEET		1 2 of 38	

# 3. Block Diagram :



**INVENTEC**

TITLE  
BAP31 (Penryn+Cantiga+ICH9M)SFF  
Block Diagram

SIZE CODE DOC NUMBER REV  
Custom X01 D-CS-1310A264501-ALG X01  
SHEET

CHANGE by Miles Liu DATE Tuesday, March 10, 2009

# 4. Net name Description :

## Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9M by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

## Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

## Net Name Suffix

#	=	Active Low signal
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# 5. Board Stack up Description

## PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	SO Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	4.75V-5.0V-5.25V 5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

INVENTEC

BAP31 (Penryn+Cantiga+ICH9M)SFF			
ANNOTATIONS			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A284501-ALG	X01
SHEET		4	of 36

# 6.Schematic modify Item and History :

2009.0108

- 1. ADD USB P3 for Docking, USB P5 for Finger printer, Modify CN5 -----P28
- 2. Modify CN20 to 50pin-----P33
- 3. Move PWR\_SWIN# from CN14 to CN20
- 4. ADD TPM module-----P34

2009.0109

- 1. ADD DOCK\_USB\_EN, DOCK\_CRT\_IN#-----P32,33

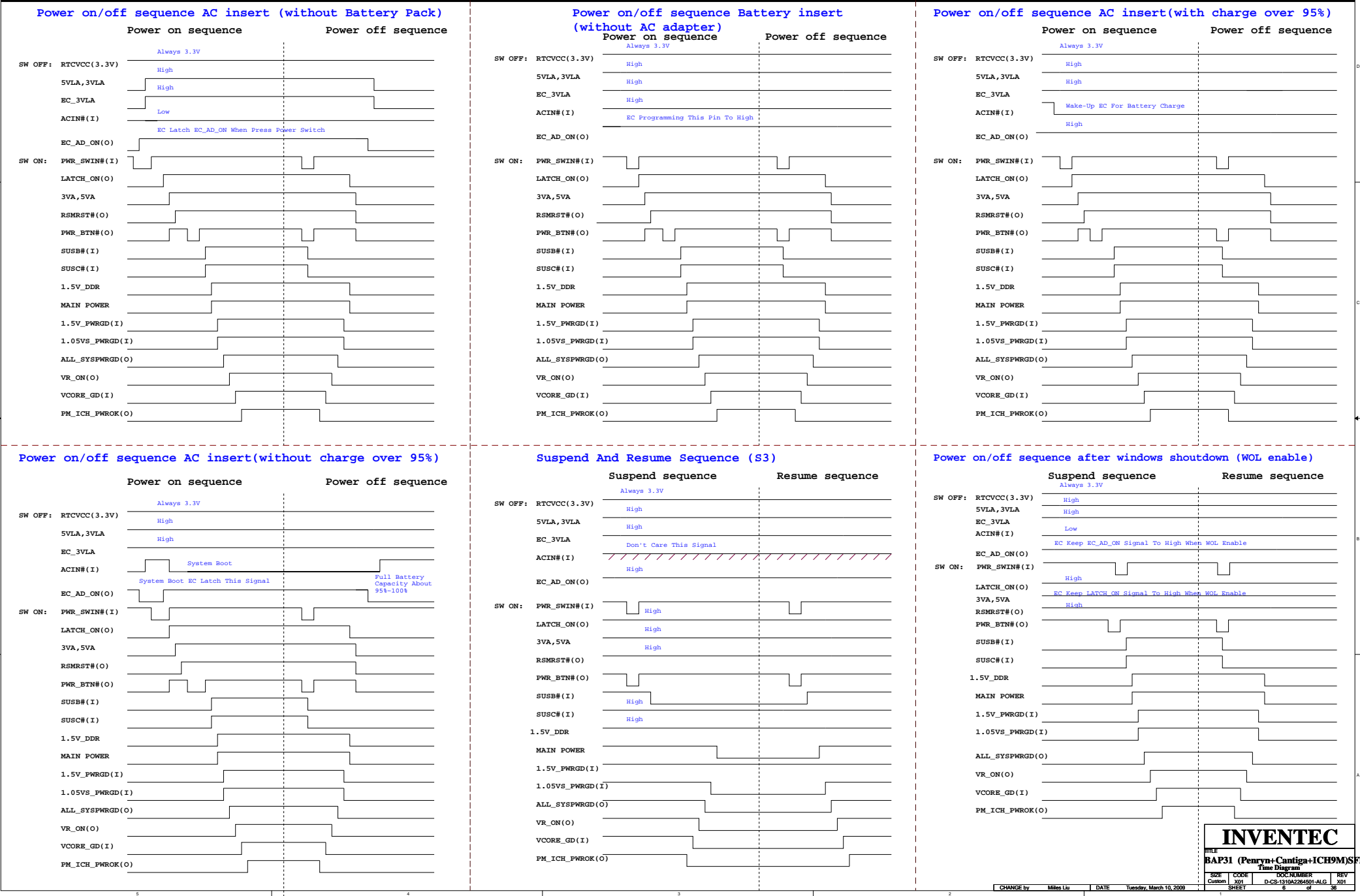
2009.0112

- 1. Change power item: R490,R291,BAT CNN TH PIN

<b>INVENTEC</b>			
TITLE BAP31 (Penryn+ Cantiga+ICH9M)SFF			
Schematic Modify			
SIZE Custom	CODE X01	DOC NUMBER D-CS-1310A284501-ALG	REV X01

SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang



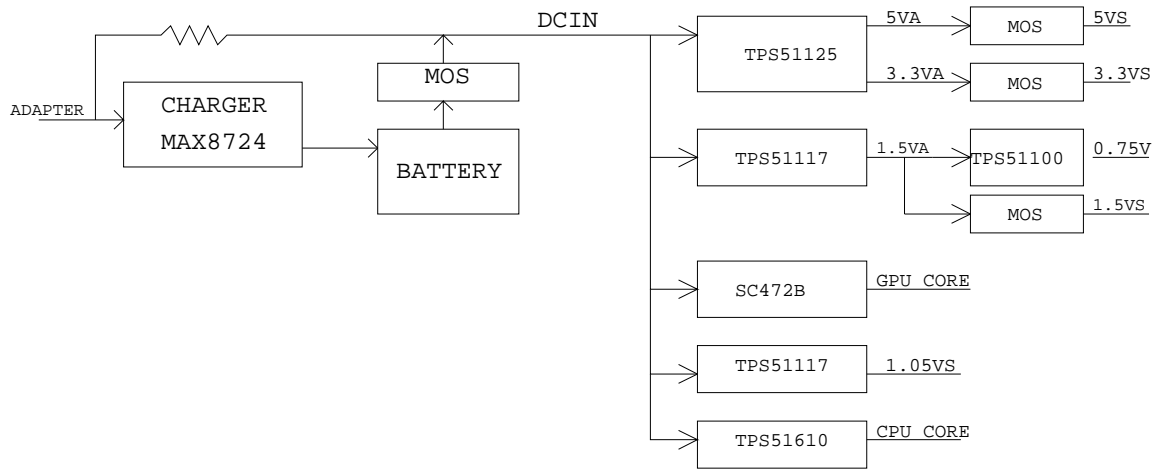
INVENTEC

RAP31 (Penryn+Cantiga+ICH9M)SFF

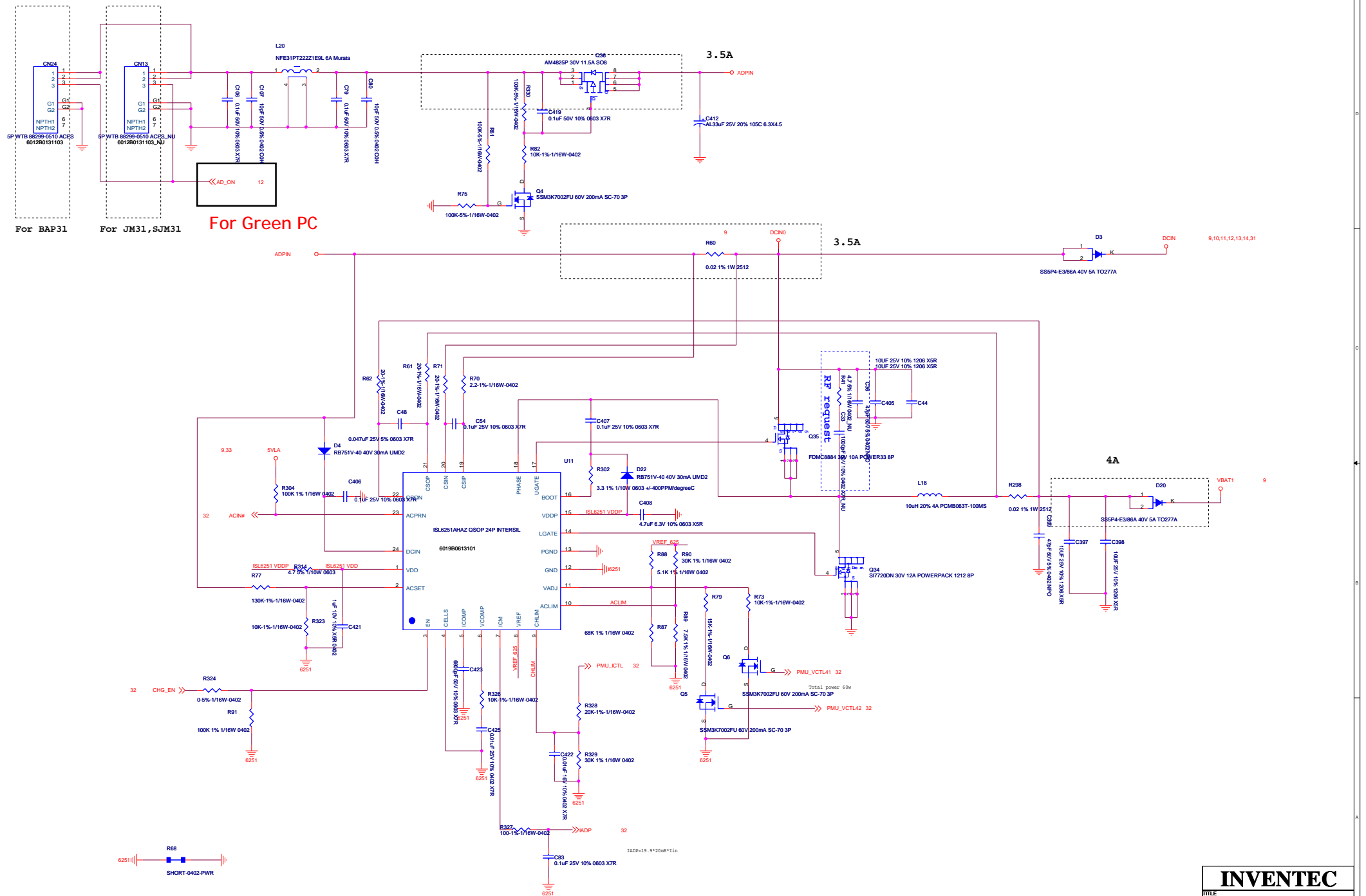
Time Diagram

SIZE	CODE	DOC NUMBER	REV
Custom	YH	D-05-1310A2986001-ALG	YH
SHEET	6	of	36

# Power Block Diagram :



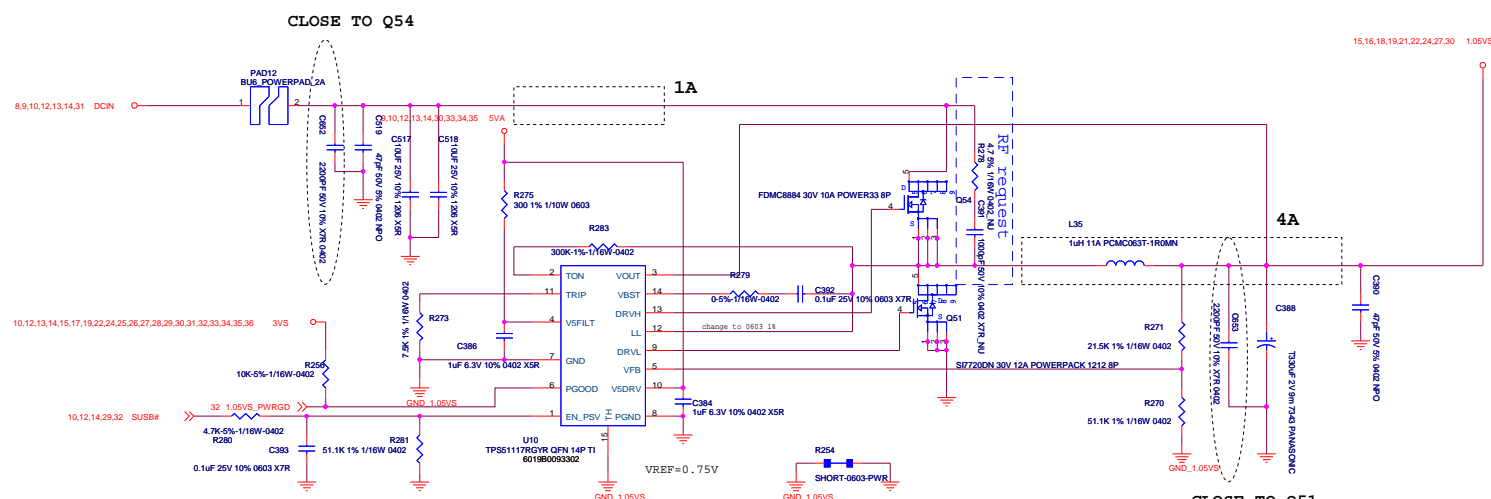
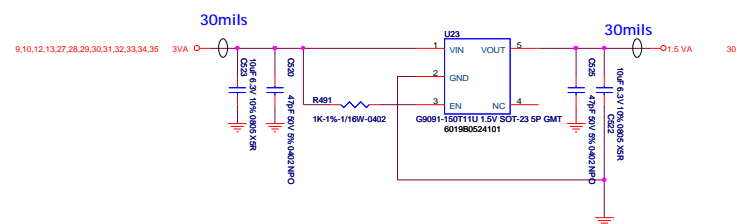
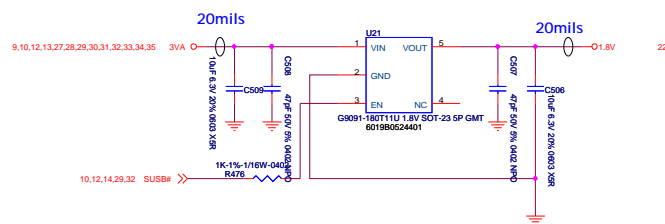
INVENTEC			
TITLE			
BAP31 (Penryn+ Cantiga+ ICH9M)SFF			
Power Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	X01	D-CS-1310A2264501-ALG	X01
SHEET			





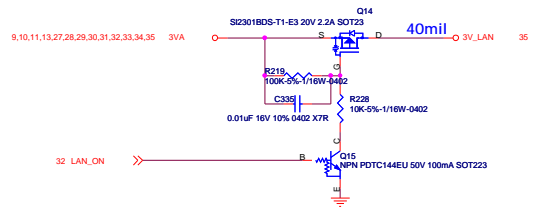
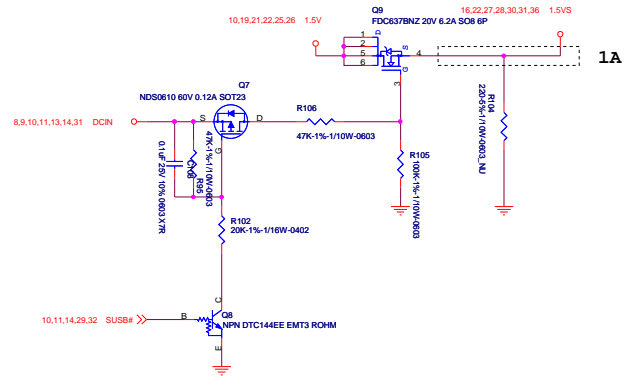




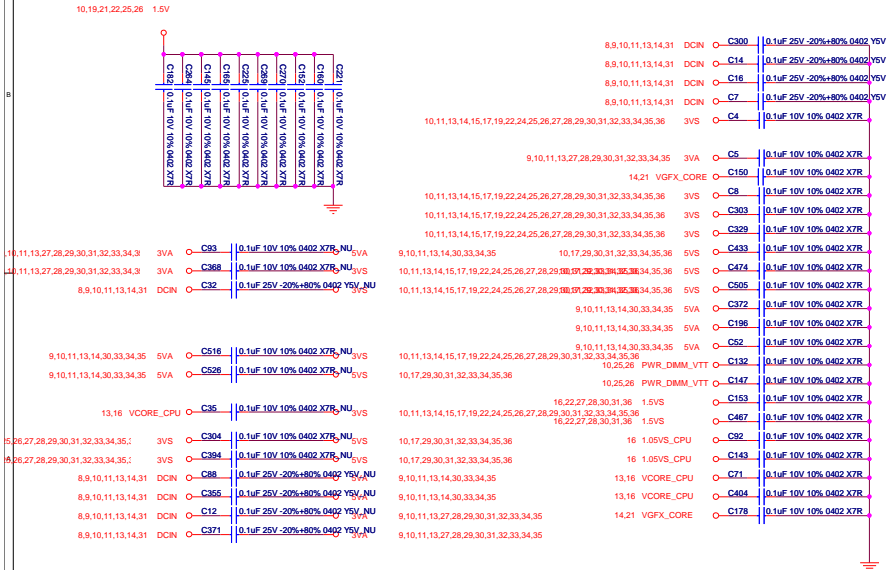


INVENTEC			
TITLE			
BAP31 (Penryn+Cantiga+ICH9M)			
1.05VS/1.5V/1.8V/1.5V			
SIZE	CORE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

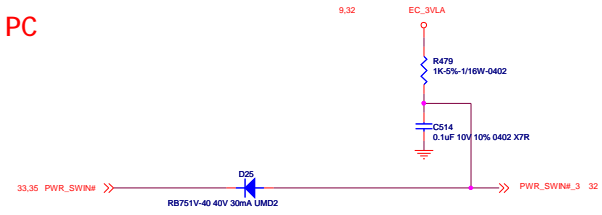
1.5VS



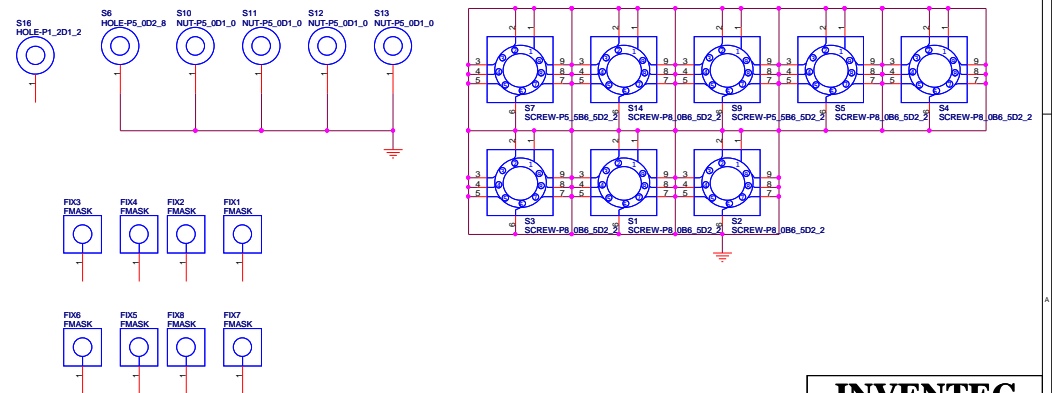
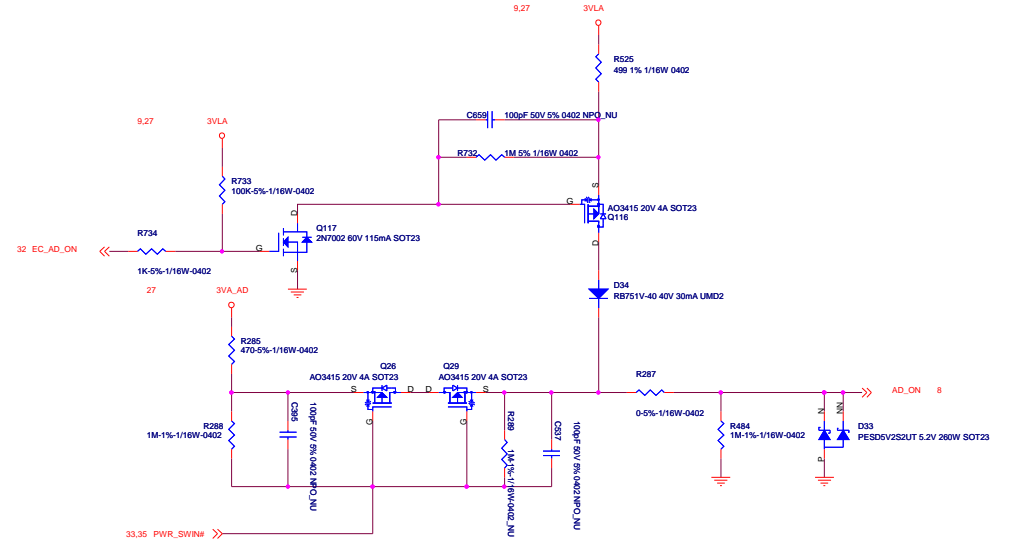
## EMI Cap



For Green PC



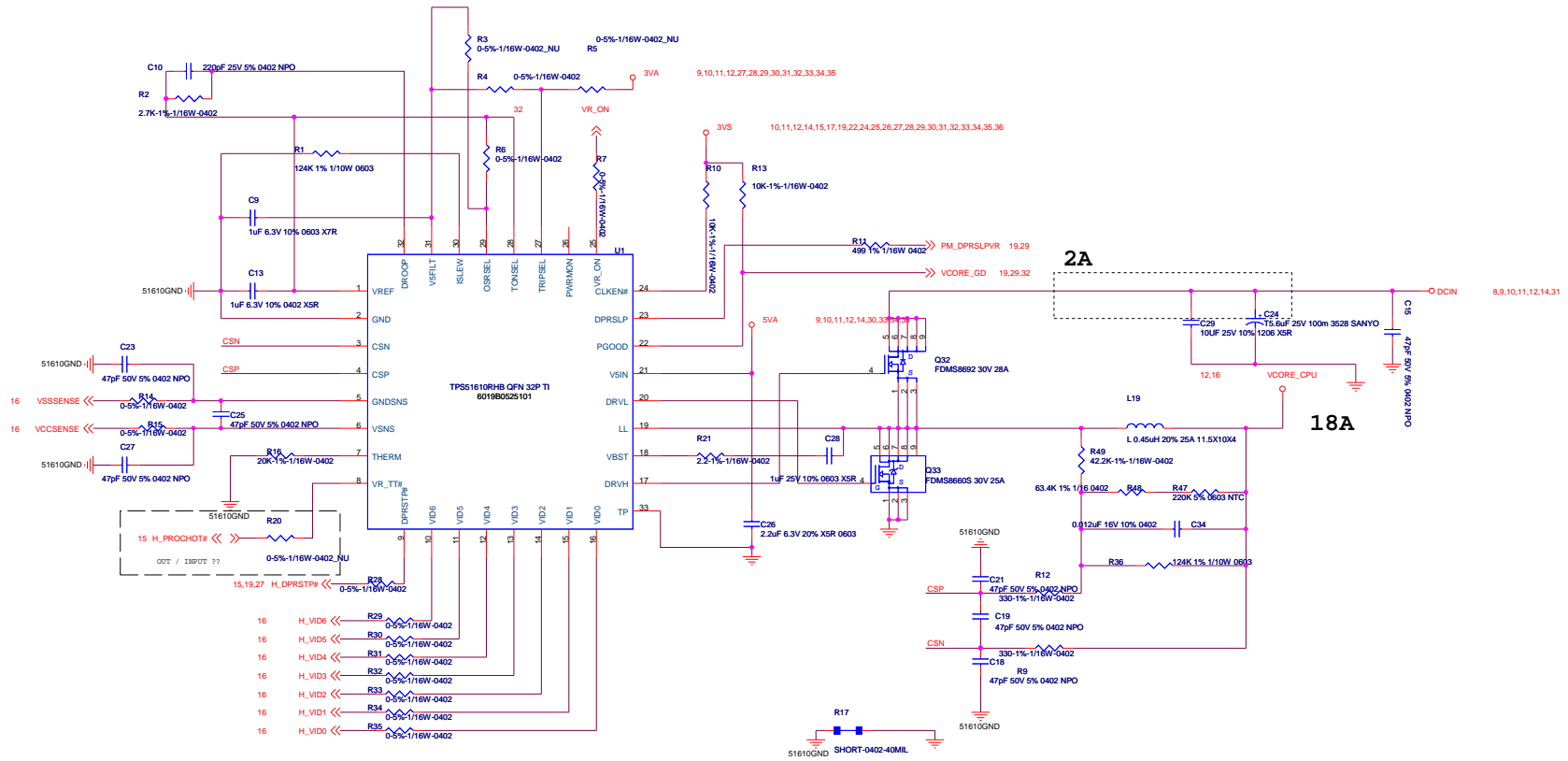
None Green PC ---- NU

**INVENTEC**

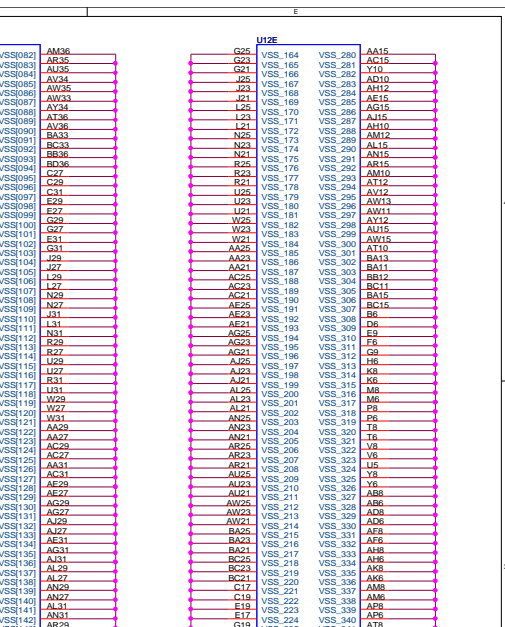
TITLE	BAP31 (Penryn+Cantiga+ICH9M)SF1
	Power on latch

SIZE Custom	CODE X01	DOC. NUMBER D-CS-1310A2264501-ALG	REV X01
SHEET		12	of 36

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009
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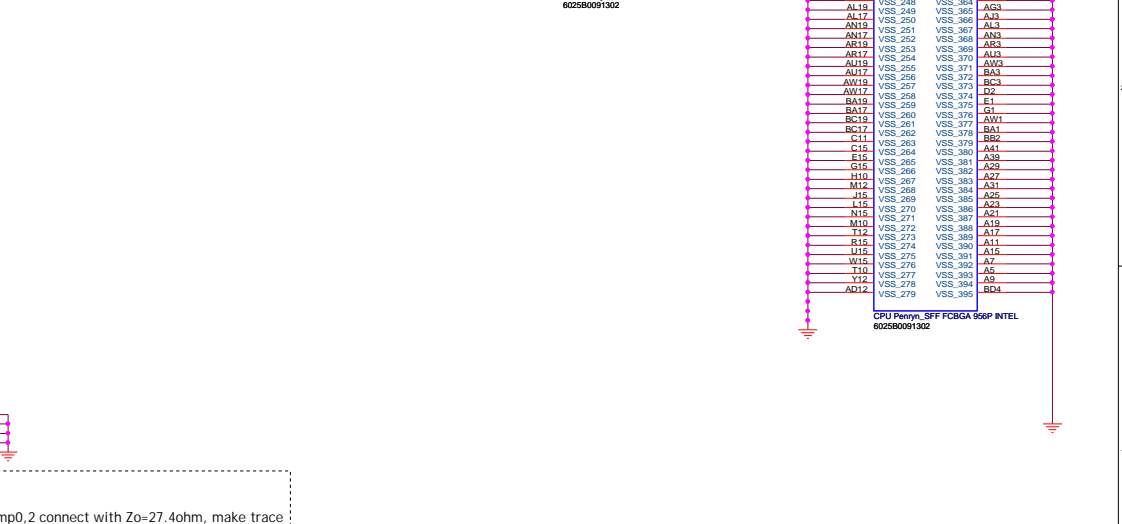




**XDP P/U & P/D**

Signal	Pin	Configuration	Supply	IOs
XDP_DBRESET#	R308	1K-5% 1/16W-0402	3VS	10,11,12,13,14,17,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36
XDP_TDO	R331	54.9-1% 1/16W-0402 NUJ	1.05VS	11,16,18,19,21,22,24,27,30
XDP_TMS	R311	54.9-1% 1/16W-0402		
XDP_TDI	R310	54.9-1% 1/16W-0402		
XDP_BPMMS	R321	54.9-1% 1/16W-0402		
XDP_TRST#	R309	649-1% 1/16W-0402		
XDP_TCK	R319	54.9-1% 1/16W-0402		

CPU Penryn\_SFF FCBGA 956P INTEL  
6025B0091302



Comp0,2 connect with  $Z_0=27.4\Omega$ , make trace length shorter than 0.5" and width is 18mils.  
Comp1,3 connect with  $Z_0=55\Omega$ , make trace





**THERMAL SENSOR**

10,11,12,13,14,15,19,22,24,25,26,27,28,29,30,31,32,33,34,35,36 3VS

0.1uF 10% 0402 50V C52

10mil

15 H\_THERMDA >> H\_THERMDA R67 100-1%-1/16W-0402

15 H\_THERMDC << H\_THERMDC R66 100-1%-1/16W-0402

100pF 50V 5% 0402 NPO C55

1402 Q+ 1402 Q- 1402 Q

U5

1 VDD 2 D+ 3 D- 4 THERM# 5 GND

8 THRMSC 7 THRMDSA 6 R92 0-5%-1/16W-0402\_NU 5

32,36 THRMSC 32,36 THRMDSA 29,36 PM\_THRM#

EMC1402-1-ACZL-TR MSOP 6P 601860437701

36 THERM# >> THERM#

29,32 PM\_ICH\_PVROK >> R255 100K-5%-1/16W-0402

15,19,27 PM\_THRMTRIP# >> R289 330-5%-1/16W-0402

3VS

10K-5%-1/16W-0402 R247

47K-5%-1/16W-0402 R242

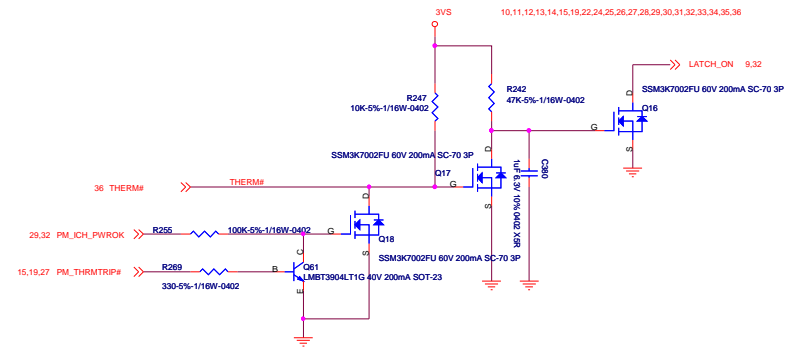
SSM3K7002FU 60V 200mA SC-70 3P Q17

SSM3K7002FU 60V 200mA SC-70 3P Q18

LMBT3904LT1G 40V 200mA SOT-23 Q61

SSM3K7002FU 60V 200mA SC-70 3P Q16

LATCH\_ON 9,32



### Fan control

The schematic diagram illustrates the fan control circuitry. It begins with a 5VS supply connected through a network of capacitors (C79, C86) and resistors (R117, R118) to two transistors, Q10 and Q11. Q10 is an NPN MOSFET (SI2301BDS-T1-E3) driving the FANCTL1 pin of connector CN15. Q11 is an NPN PNP transistor (PDT144EU) driven by FAN\_ON from EC pin106. Both transistors are connected to a common 30mil trace leading to the FAN pin of connector CN15. The circuit also includes a feedback path from EC pin29 (FANCTL1) back to the base of Q10 via a capacitor (C48). A green 'OK' label is present near the connector.

From EC pin106(new)

32 FAN\_ON

Q10  
SI2301BDS-T1-E3 20V 2.2A SOT23

R117  
1K-5%-1/16W-0402

R118  
0-5%-1/16W-0402

Q11  
NPN PDT144EU 50V 100mA SOT223

30mil

5VS\_FAN

32 FANCTL1

From EC pin29

32 FAN\_TACH1

From EC pin47

CN15

G1

G2

4P PPC-81206-00401 ACES  
601280152003

OK

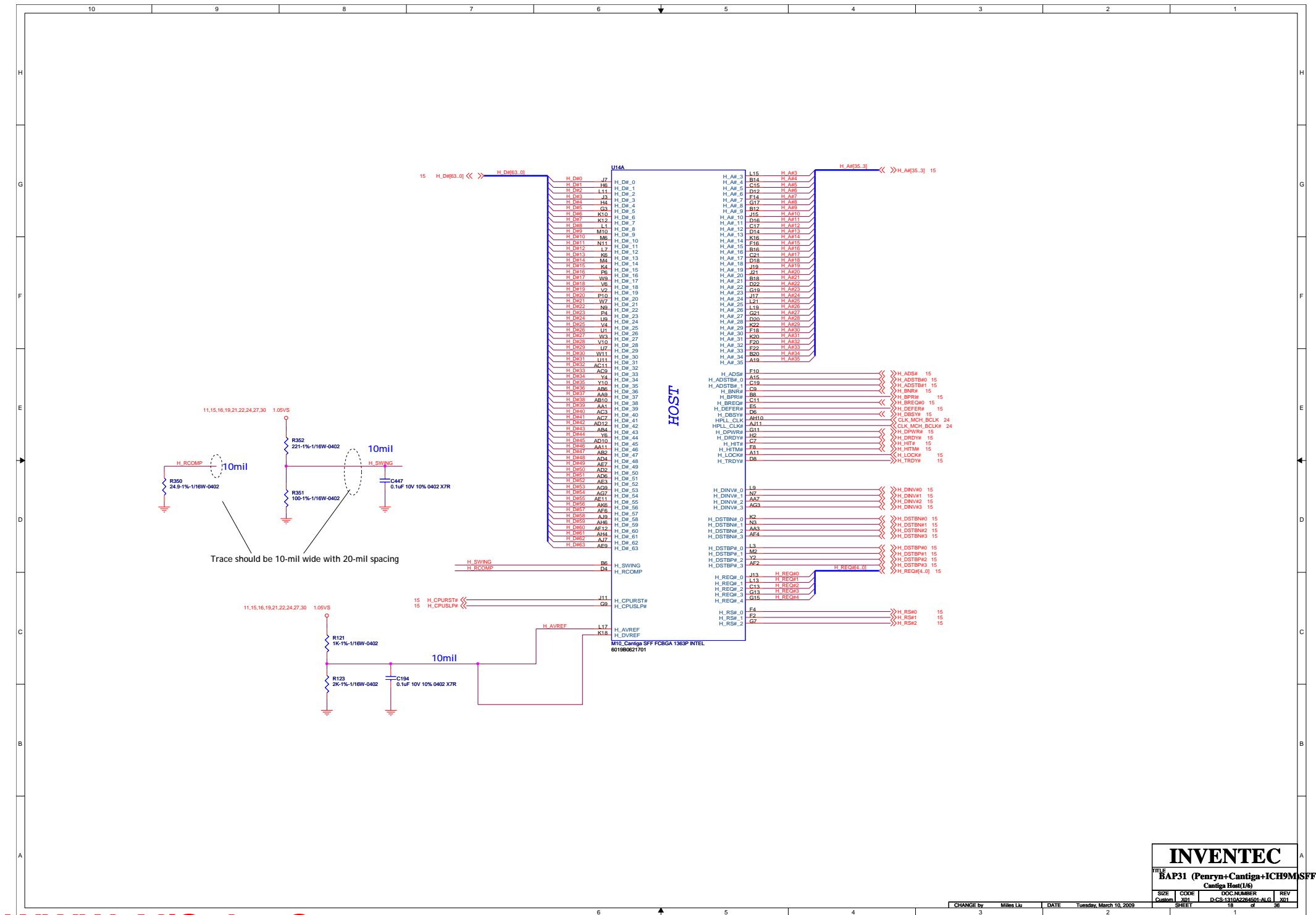
INVENTEC			
TITLE			
BAP31 (Penryn+Contiga+ICH9M)SFF			
CPU Thermal			
SIZE	CODE	DWG NUMBER	REV
Custom	X01	D-CS-1310A2284501-ALG	X01
SHEET			

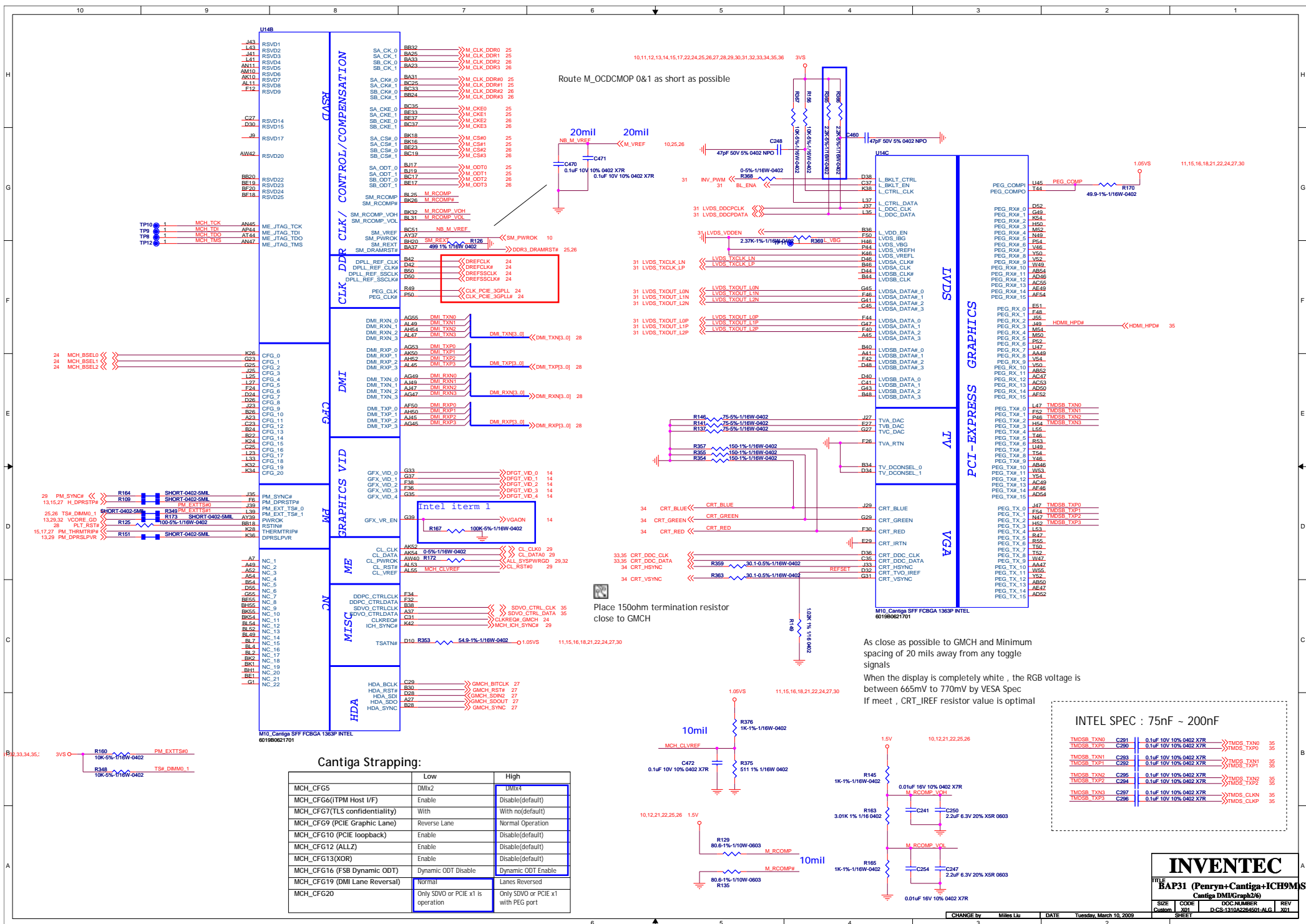
CHANGE by Miles Liu DATE Tuesday, March 10, 2009

[illegible]

OK

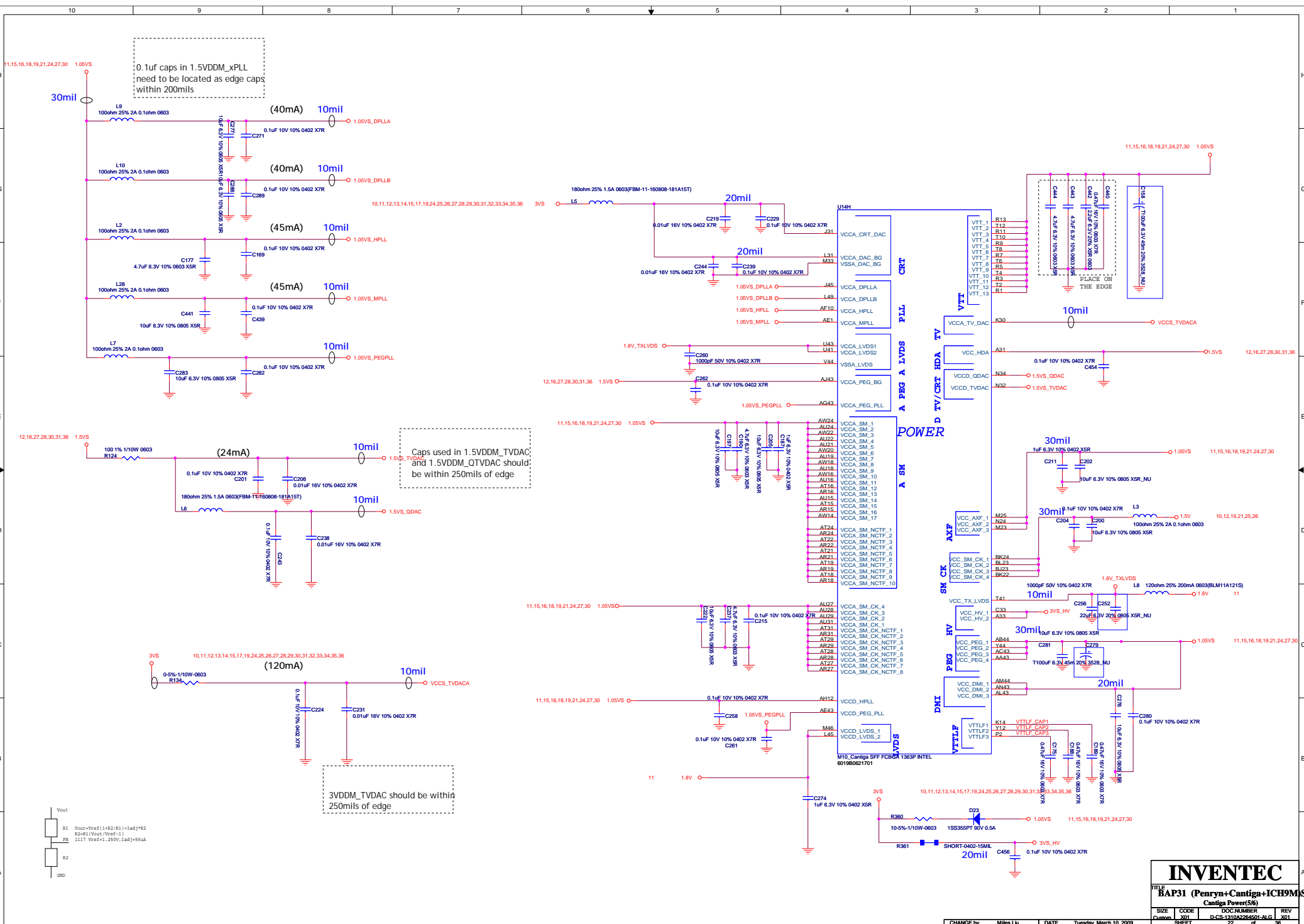
<b>INVENTEC</b>			
TITLE <b>BAP31 (Penryn+Centiga+ICH9M)SFF</b>			
CPU Thermal			
SIZE Custom	CODE X01	DOC NUMBER D-CS-1310A284051-ALG	REV X01
SHEET			







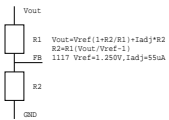




0.1uF caps in 1.5VDDM\_xPLL need to be located as edge caps within 200mils

Caps used in 1.5VDDM\_TVDAC and 1.5VDDM\_QTVDAC should be within 250mils of edge

3VDDM\_TVDAC should be within 250mils of edge

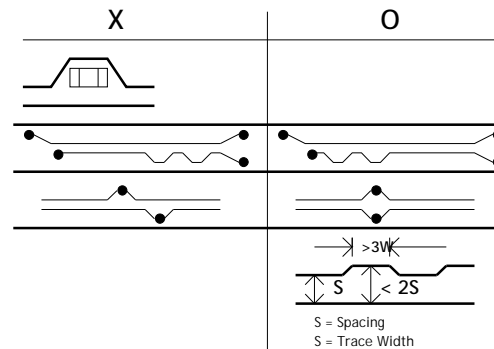


<b>INVENTEC</b>			
BAP31 (Penryn+Cantiga+ICH9M+SFF Cantiga Power(56))			
SIZE	CODE	DOC NUMBER	REV
Custom	201	D-CS-1310A2264921-ALG	201
SHEET		22	of 36

Breakout/in LA/LZ	Main Route LB/LV		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Diddifferential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV ( ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

[illegible]

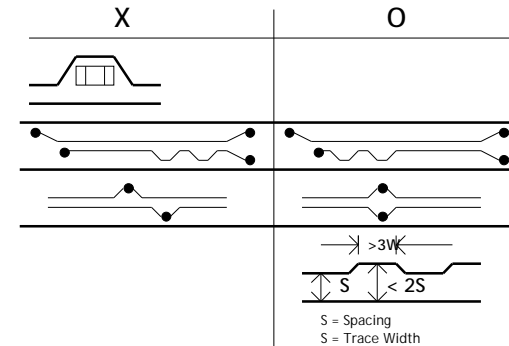
```

graph LR
    subgraph GMCH
        Tx1[Tx]
        Rx1[Rx]
        LA[LA]
        LB[LB]
        LZ[LZ]
        LY[LY]
    end
    subgraph ExpressMiniCard [Express/Mini Card]
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --- LA
    LA --- LB
    LB --- C1[Capacitor]
    C1 --- LC[LC]
    LC --- Rx2
    Rx1 --- LZ
    LZ --- LY
    LY --- Tx2
  
```

Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe ON)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe ON to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

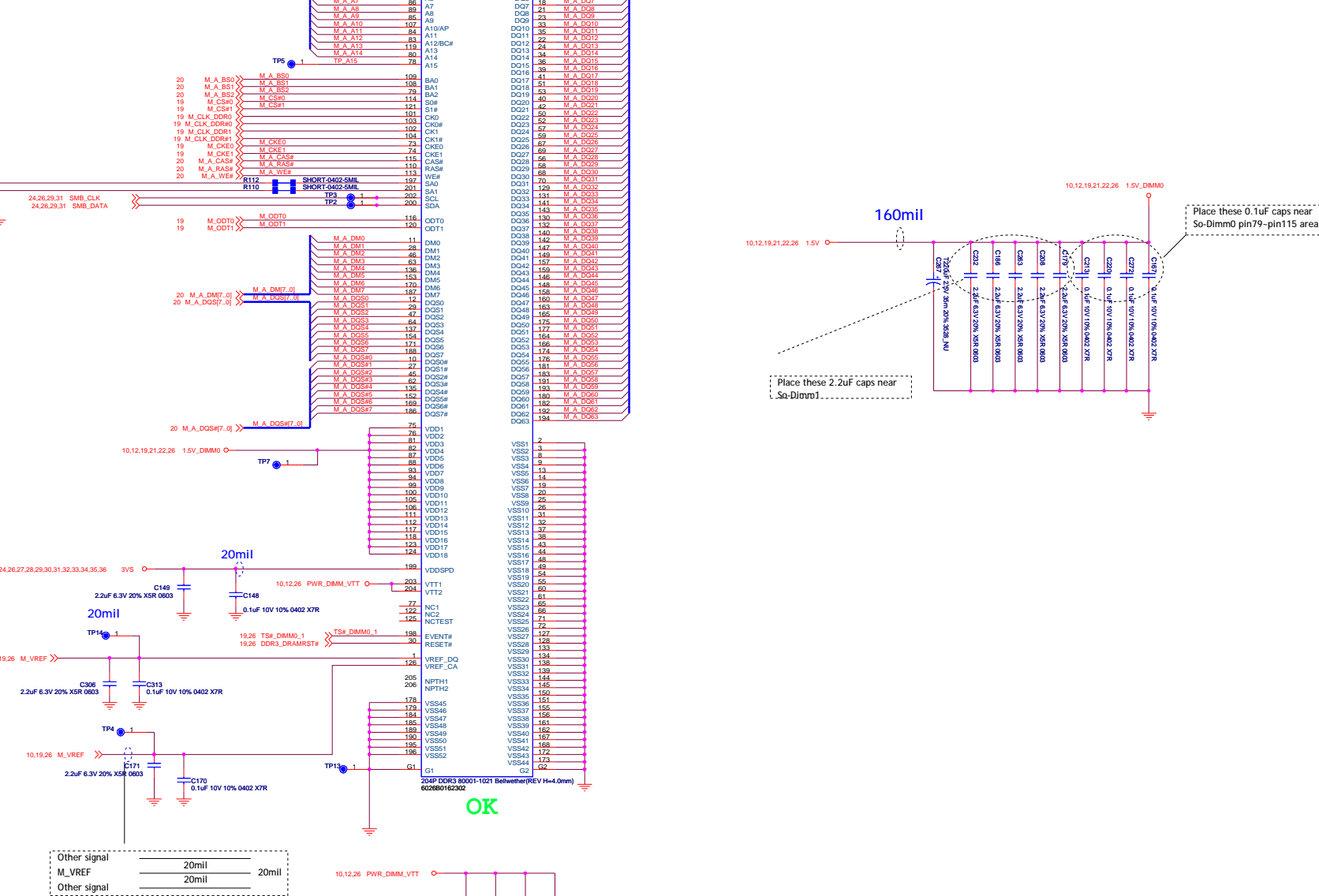
**INVENTEC**

TITLE	BAP31 (Penryn+Cantiga+ICH9M)SFF Cantiga Ground(6/6)
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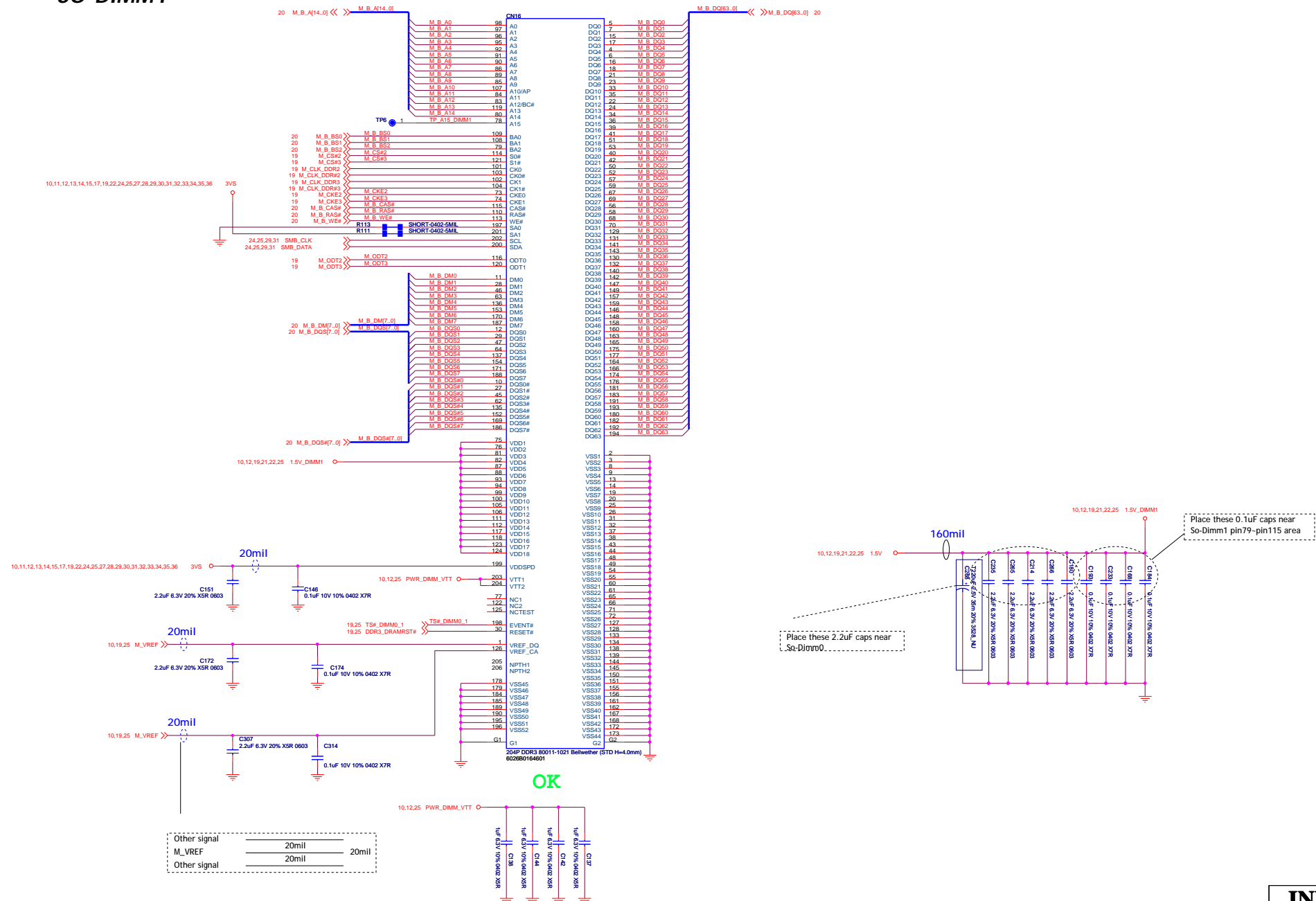
SIZE Custom	CODE X01	DOC. NUMBER D-CS-1310A2264501-ALG	REV X01
SHEET		23 of	36





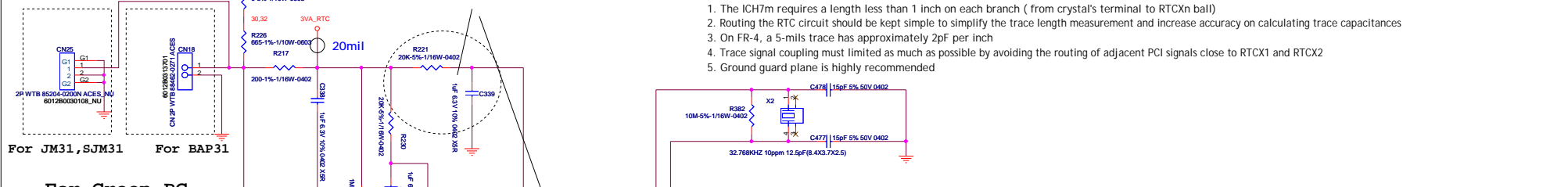


TITLE			
BAP31 (Penryn+Cantiga+ICH9M+SFT)			
DDR3 SDRAM SO-DIMM0			
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01
SHEET			

***SO-DIMM1***

9,12 3VLA

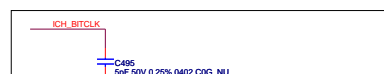
- 



	Enable	Disable
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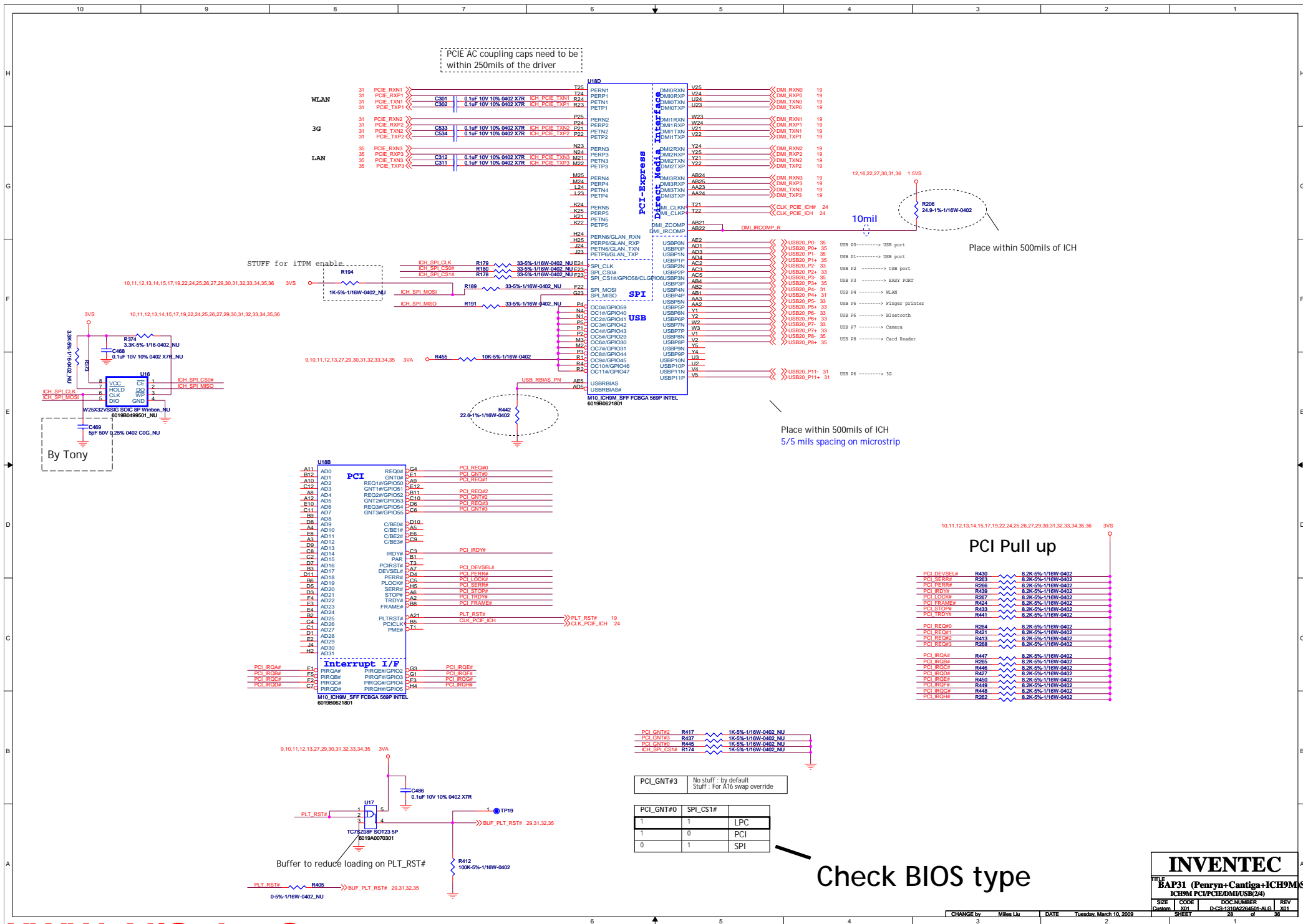
Internal VRM enabled for

101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554
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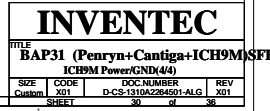


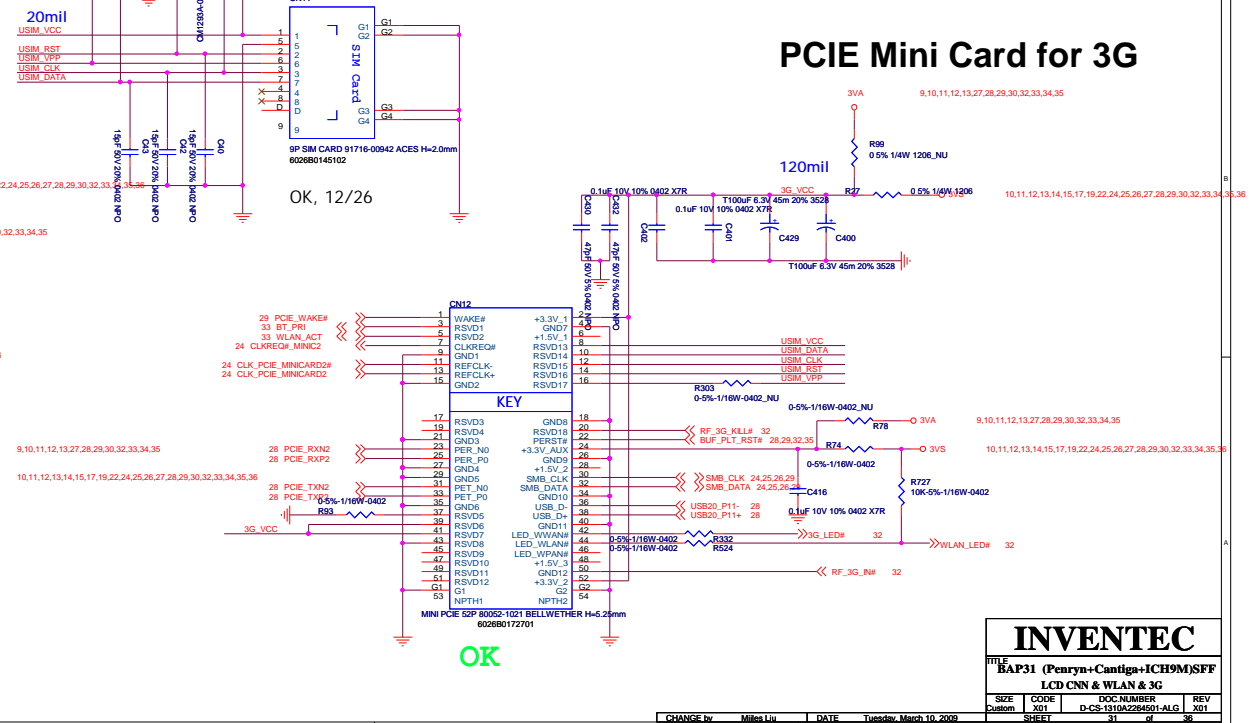
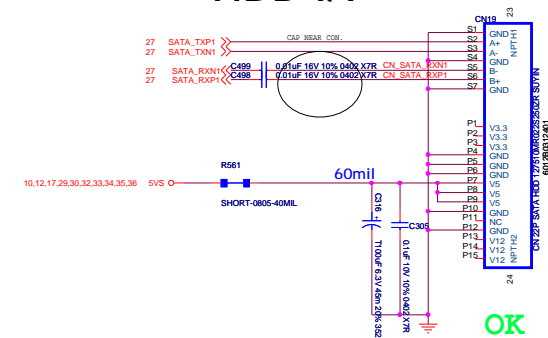
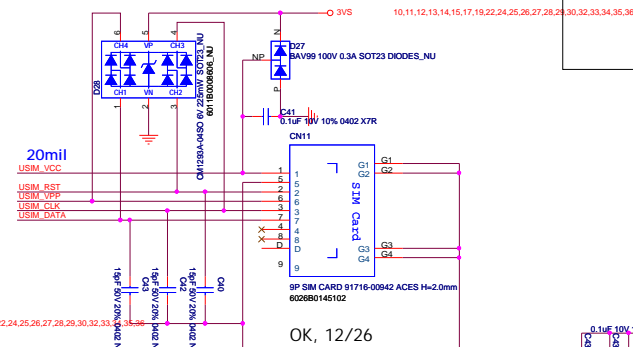
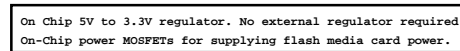
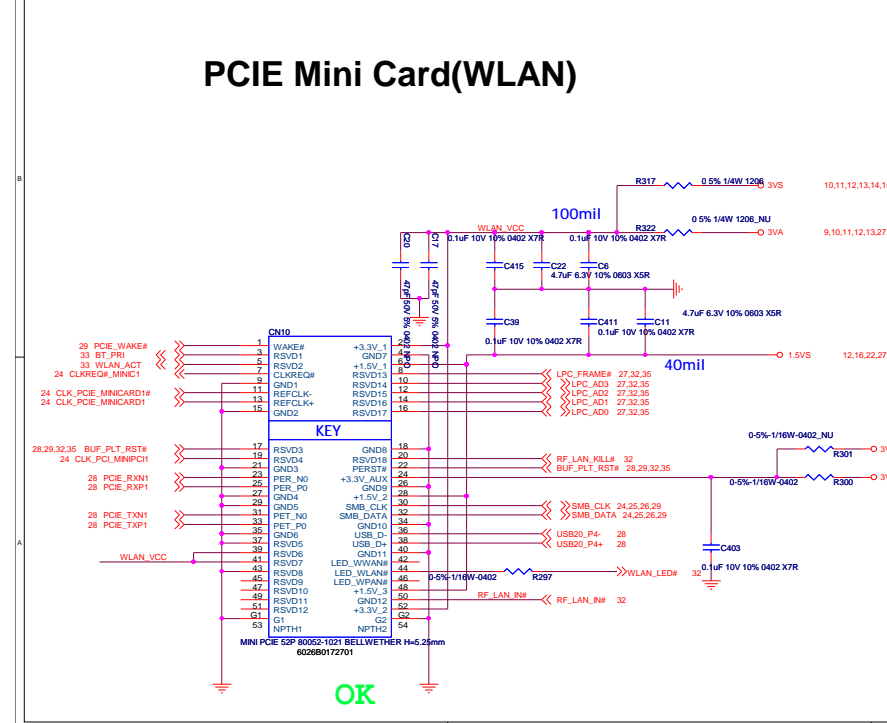
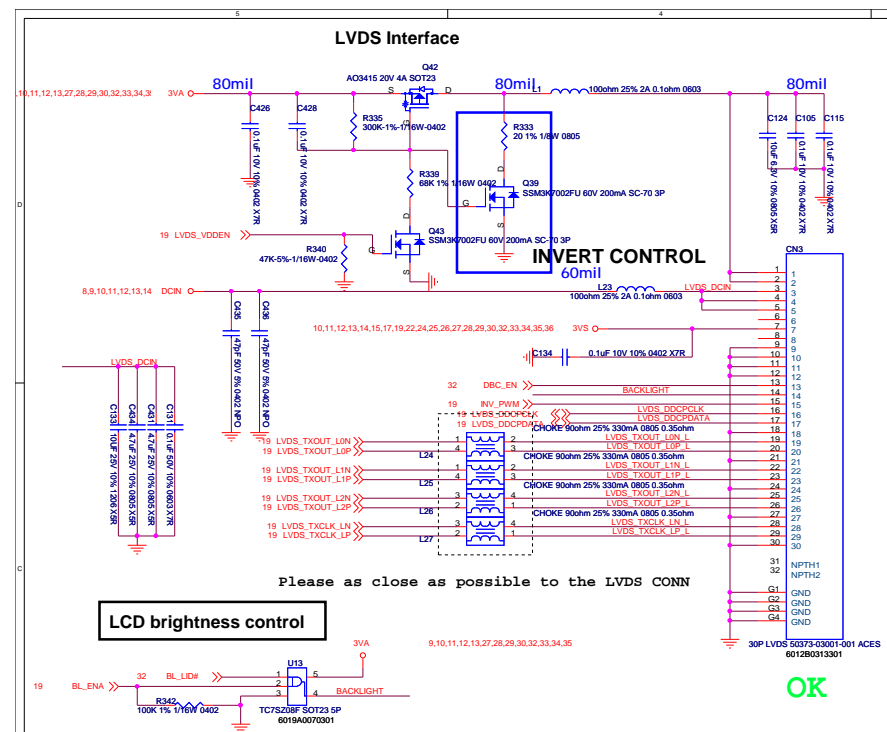
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## INVENTEC





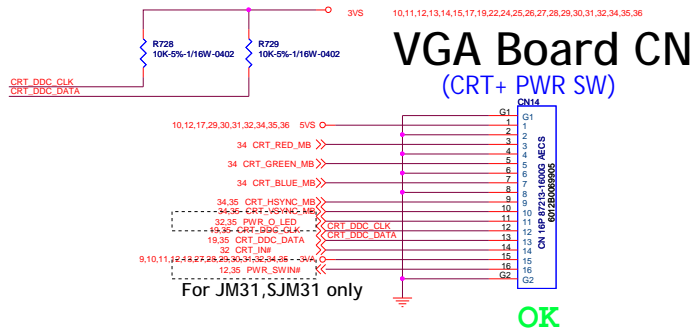




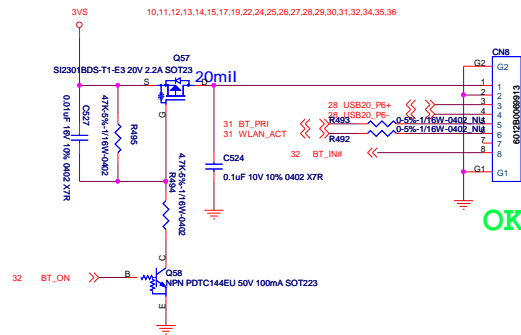




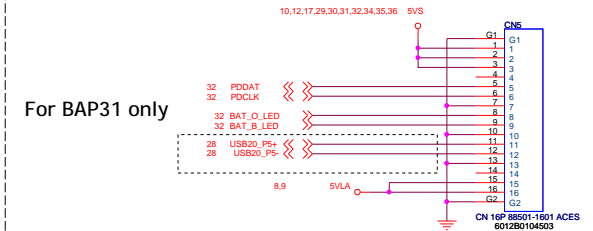




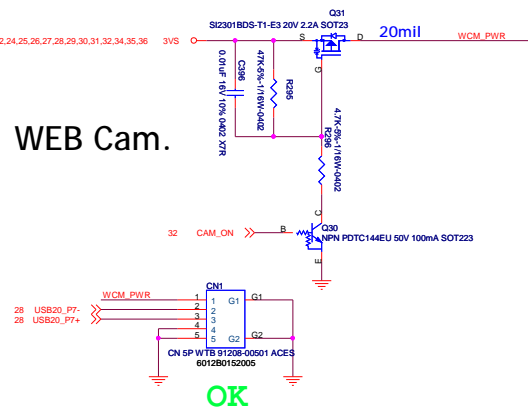
## Bluetooth CON.



## GLIDE PAD Board

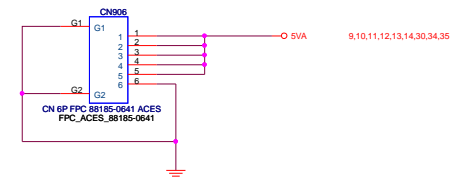
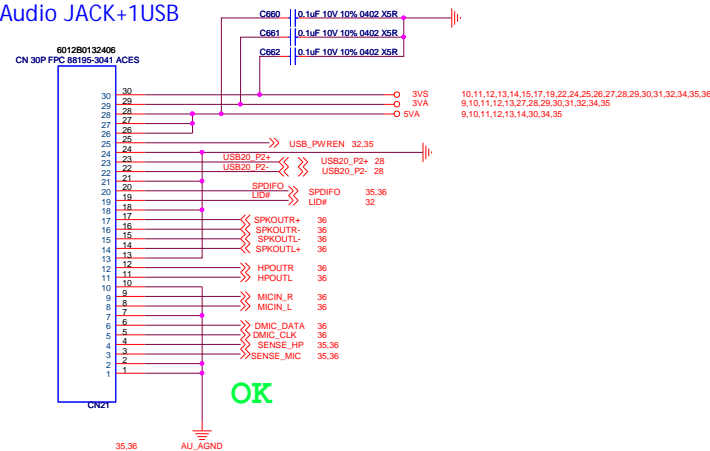


## WEB Cam.



## AUDIO Board CN

(Audio JACK+1USB)



**INVENTEC**

FILE  
**BAP31 (Penryn+Contiga+ICH9M)MSI**  
Daughter Connector

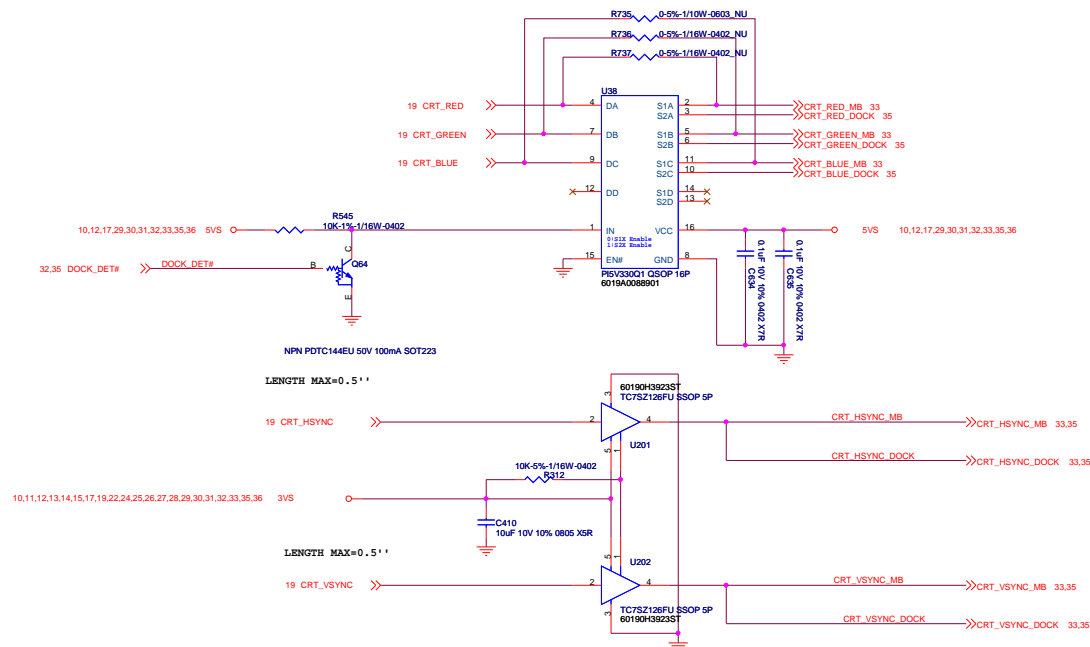
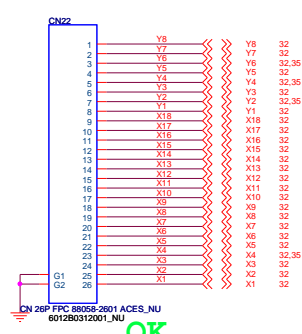
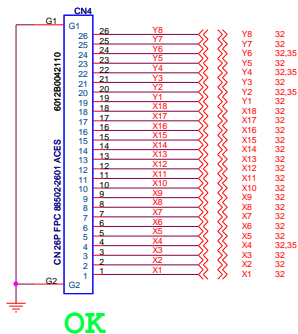
SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by: Miles Lin DATE: Tuesday, March 10, 2009

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To K/B(For JM31,BAP31)

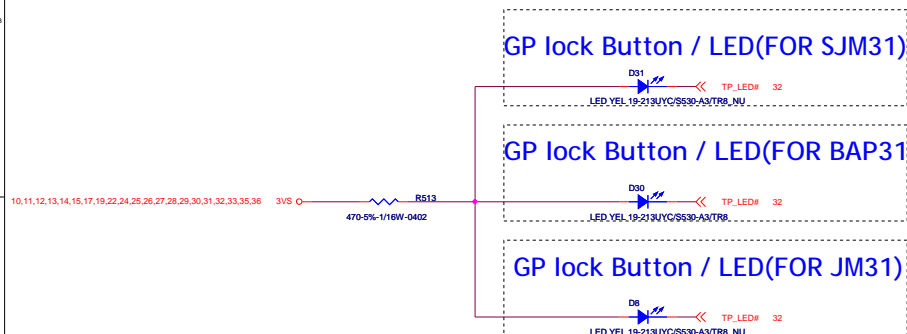
To K/B (For SJM31)



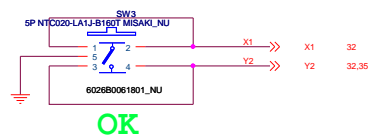
GP lock Button / LED(FOR SJM31)

GP lock Button / LED(FOR BAP31)

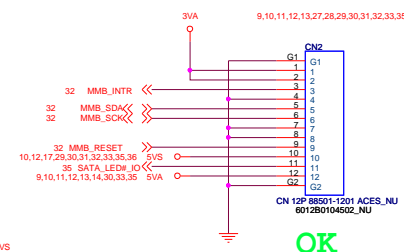
GP lock Button / LED(FOR JM31)



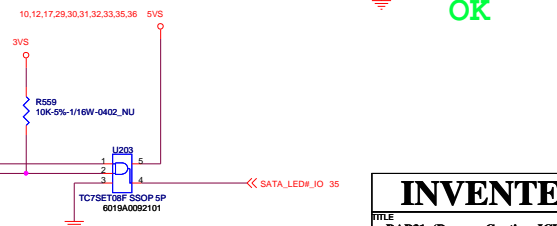
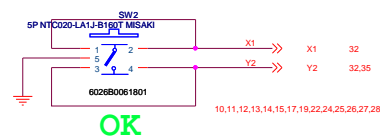
SW (FOR SJM31)



SW Sensor BOARD(For JM31,SJM31)



SW (FOR JM31,BAP31)



INVENTEC

BAP31 (Penryn+Cantiga+ICH9M)SFF

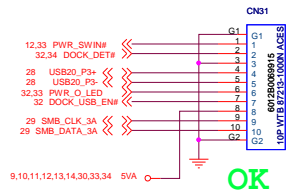
DOC NUMBER REV

SIZE CODE D-CS-1310A2264501-ALG X01

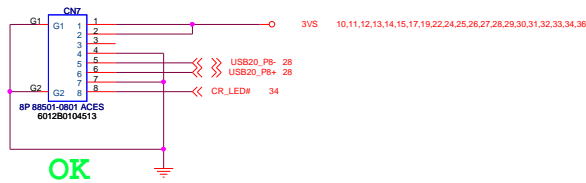
SHEET 34 of 36

CHANGE by Miles Lin DATE Tuesday, March 10, 2009

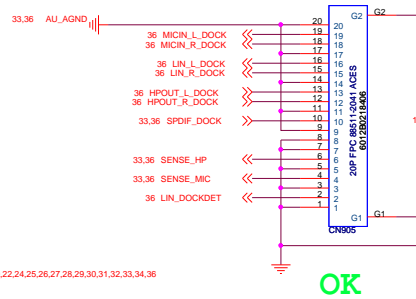
## MB(USB) TO EASY/B



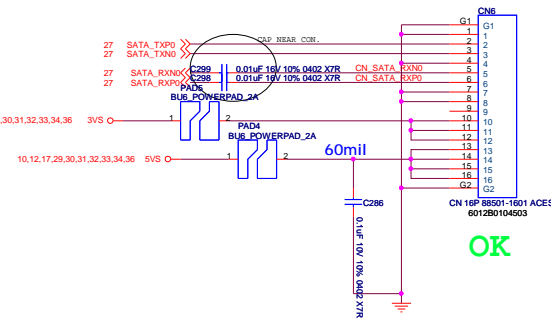
## Card Reader BOARD CN



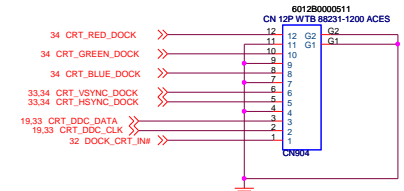
## MB(AUDIO) TO EASY/B(For BAP31)



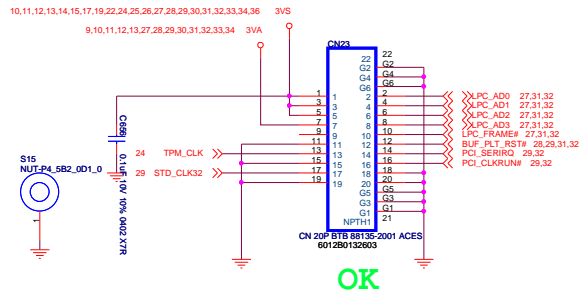
## SSD I/F



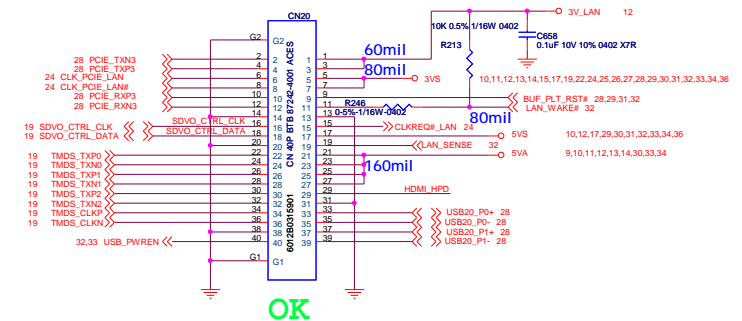
## MB(RGB) TO EASY/B



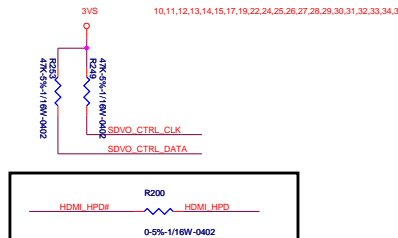
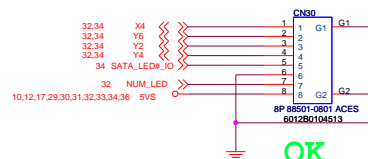
## TPM CN



## USB Board CN (LAN+HDMI+2USB)



## SW/B CN



**INVENTEC**

TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF

Doc NUMBER REV

Custom X01 D-CS-1310A2264501-ALG X01

SHEET 35 of 36

CHANGE by Miles Liu DATE Tuesday, March 10, 2009

