


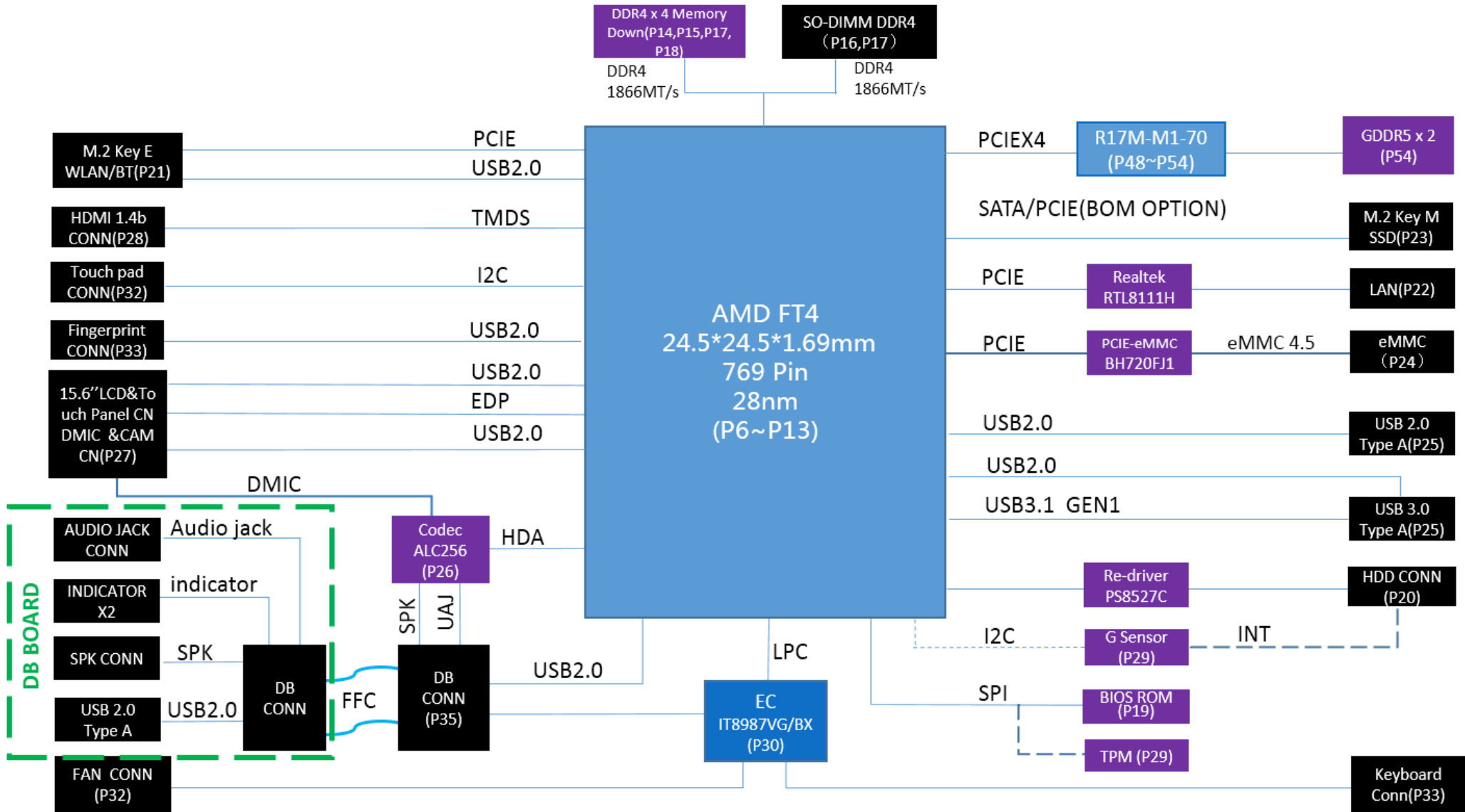
COVER PAGE

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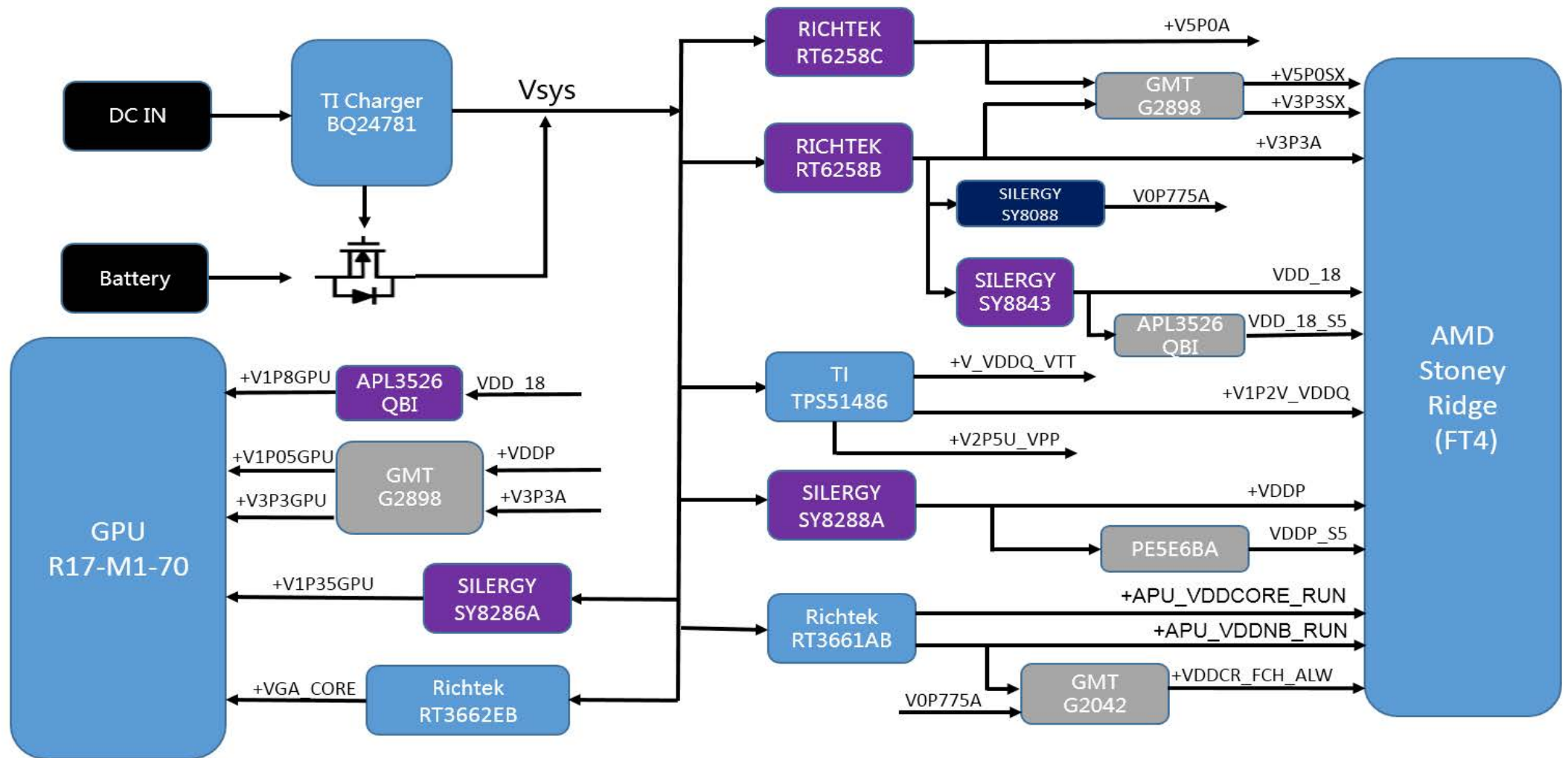
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MB Block Diagram



MB Power Map



Power States(Adapter)																				
Signal	+VCC3P3_LDO_OUT	+V5P0A	+V3P3A	+V1P8A	+VOP95A	+VOP776A	+VDDCR_PCH_ALW	+V1P2V_VDDQ	+V5P0SX	+V3P3SX	+V1P8SX	+VDDP_S0	+V_VDDQ_VTT	+APU_VDDC0R8_RUN	+APU_VDDNB_RUN	+V3P3GPU	+V1P8GPU	+VOP95GPU	+V1P35GPU	+VGA_CORE
S0 (Pull On)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3 (STM)	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5 (SoftOff)	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Power States(Battery)

Signal	+VCC3P3_LDO_OUT	+V5P0A	+V3P3A	+V1P8A	+VOP95A	+VOP776A	+VDDCR_PCH_ALW	+V1P2V_VDDQ	+V5P0SX	+V3P3SX	+V1P8SX	+VDDP_S0	+V_VDDQ_VTT	+APU_VDDC0R8_RUN	+APU_VDDNB_RUN	+V3P3GPU	+V1P8GPU	+VOP95GPU	+V1P35GPU	+VGA_CORE
S0 (Pull On)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3 (STM)	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5 (SoftOff)	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

BOARD ID

BOARD ID5 1--RUI83 0--RUI91	BOARD ID4 1--RUI82 0--RUI90	BOARD ID3 1--RUI81 0--RUI89	BOARD ID2 1--RUI80 0--RUI88	BOARD ID1 1--RUI79 0--RUI87	BOARD ID0 1--RUI78 0--RUI86
1--DGPU 0--UMA	1--SATA SSD 0--PCIe SSD	RESERVE	MEMORY ID		

SMBUS/I2C Control Table

	SOURCE	GPU	BATT	IT8987E	SODIMM	Touch Pad	Thermal Sensor	APU	Charger	G-SENSOR Sensor
SM_BAT_CLK SM_BAT_DATA	IT8987E +V3P3A_EC	X	V		X	X	X	X	V	X
SM_THRM_SCL SM_THRM_SDA	IT8987E +V3P3SX_EC	V	X		X	X	V	V APU_SIC APU_SID +V1P8SX	X	X
APU_SMB_CLK APU_SMB_DATA	APU +V3P3SX	X	X	X	V	X	X		X	X
GSEN_I2C0_SCL GSEN_I2C0_SDA	APU +V1P8_GSENSOR	X	X	X	X	X	X		X	V
TOUCHPAD_I2C_CLK TOUCHPAD_I2C_SDA	APU +V3P3A_CP	X	X	X	X	V	X		X	X

PCIe/GFX Port

PCIE	Device
0	LAN
1	WLAN
2	eMMC
3	SSD
GFX	Device
0~3	DGPU

SATA Port

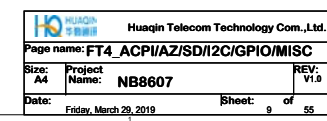
Port	Device
0	HDD
1	SSD

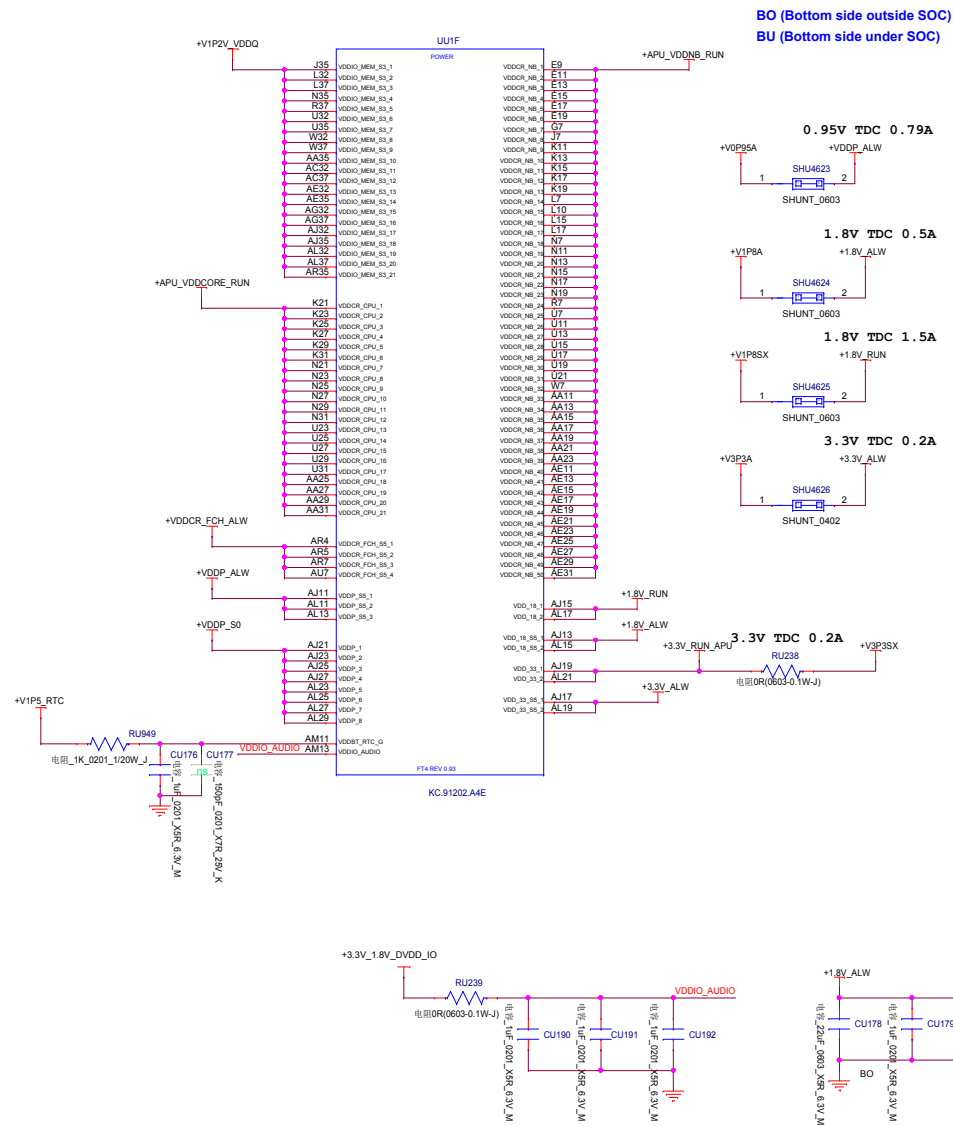
USB2.0 Port

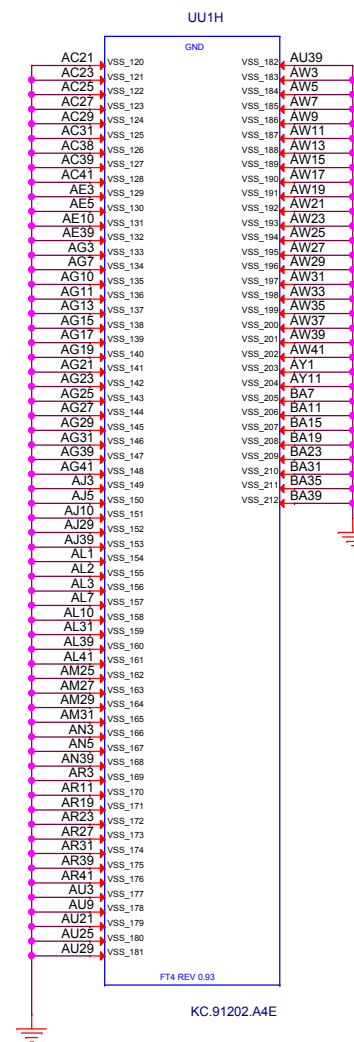
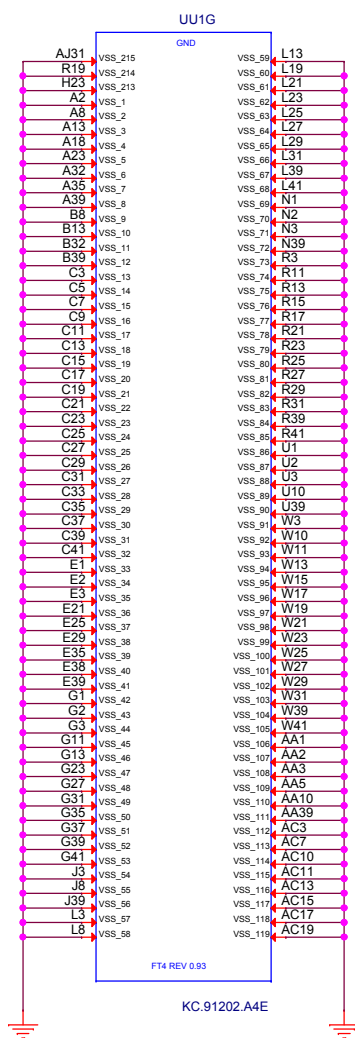
Port	Device
0	Blue Tooth
1	DB USB2.0
2	Finger print
4	USB 3.0 Port
5	USB2.0
6	Touch Panel
7	Camera

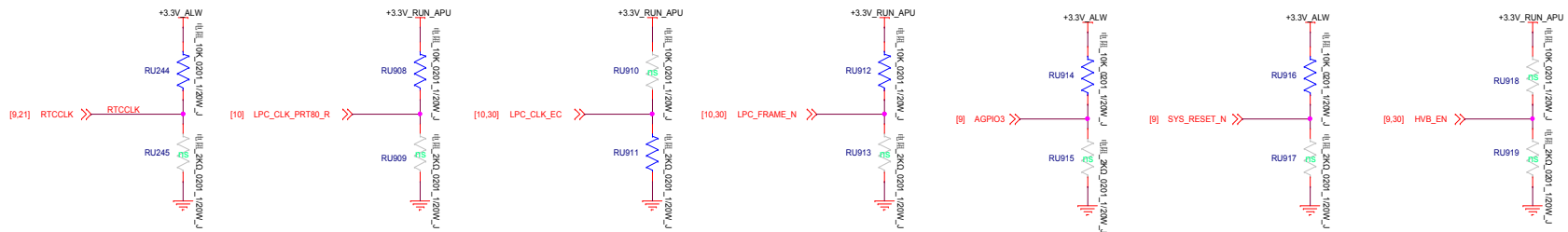
USB3.0 Port

Port	Device
0	USB3.0 Type-A
1	NA

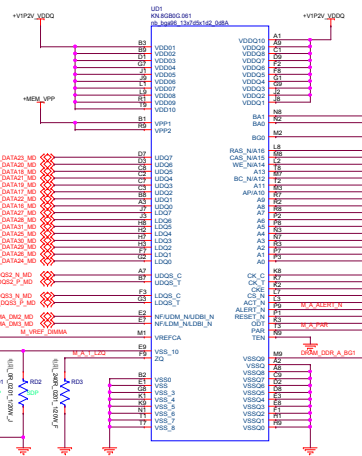




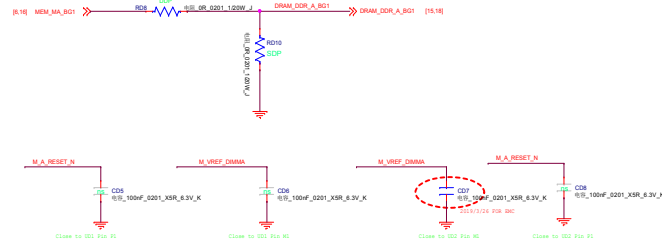
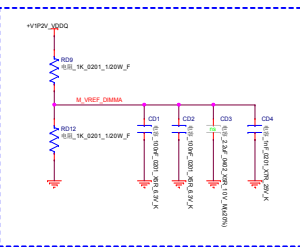


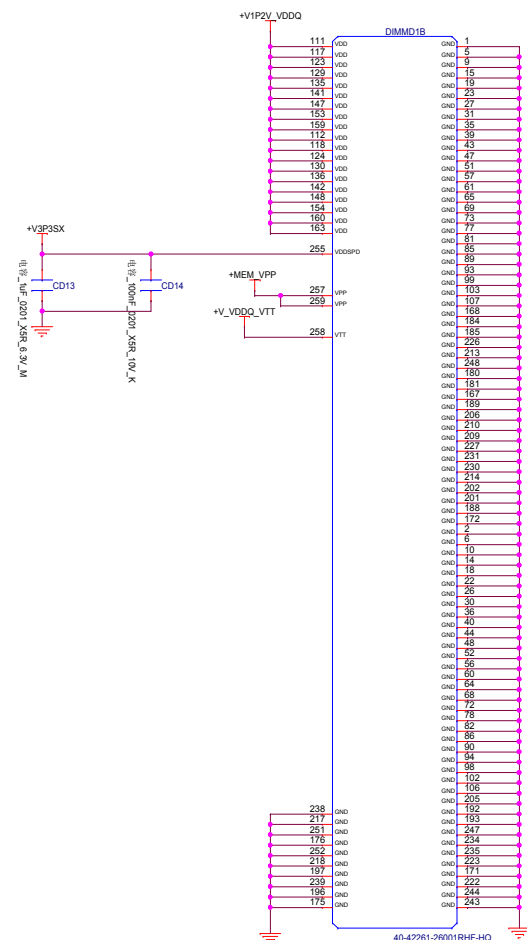


	LPC_CLK0 (LPC_CLK_EC)	LPC_CLK1 (LPC_CLK_PRT80_R)	LFRAME_L	AGPIO3 Int pull-up	RTC_CLK Int pull-up	SYS_RST# Int pull-up	HVB_EN
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	SPI ROM (DEFAULT)	Enhanced reset (for quicker S5 (DEFAULT)	Coin battery is on board. (DEFAULT)	normal reset mode (DEFAULT)	floating Disable HVB
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	Default to traditional reset logic	Coin battery is not on board.	short reset mode	connected to VSS Enable HVB

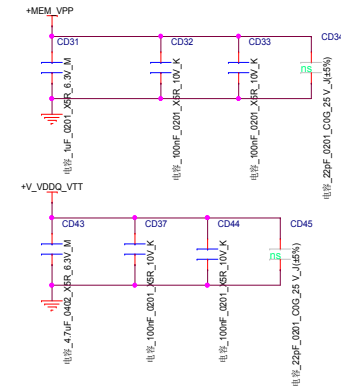
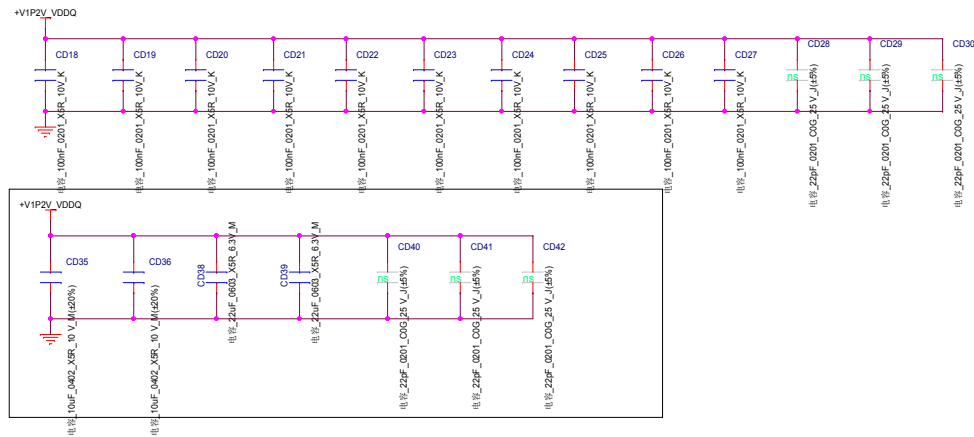


SDRAM REF GENERATION

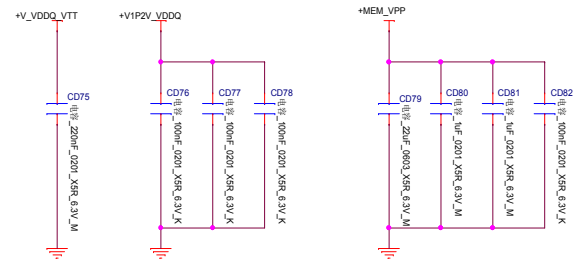
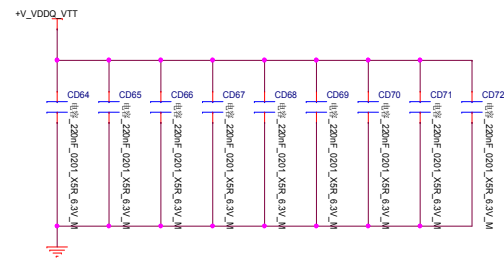
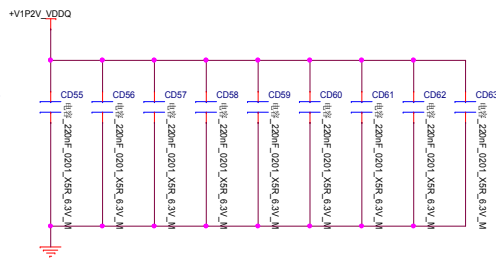
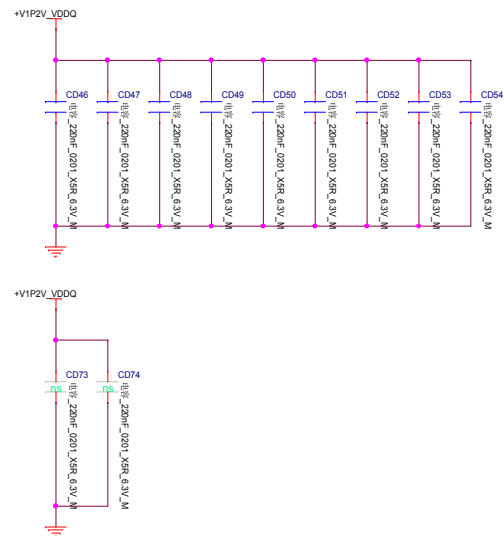




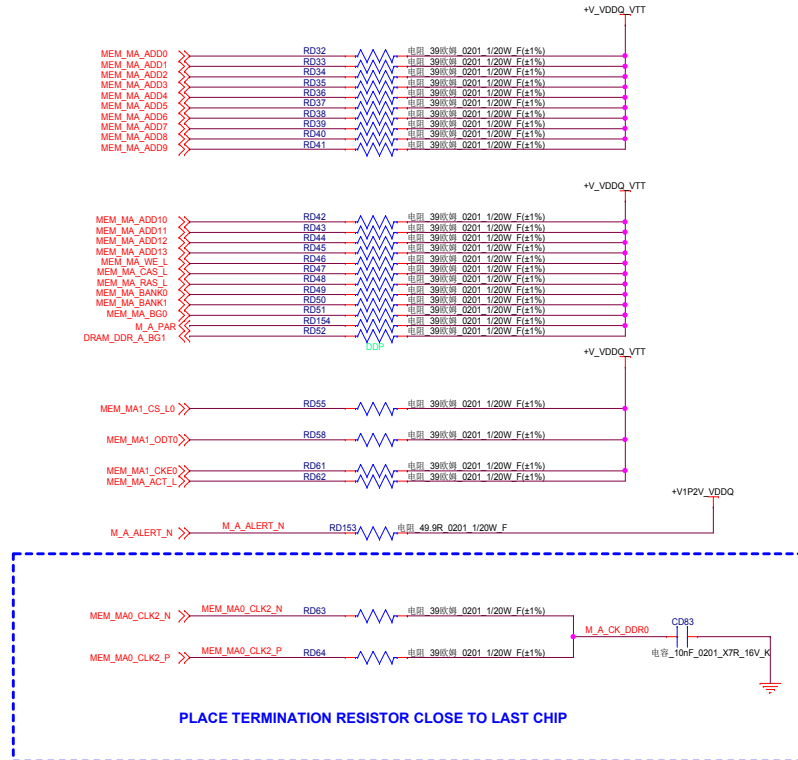
Layout Note: Place near SODIMM

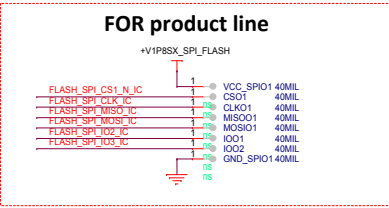
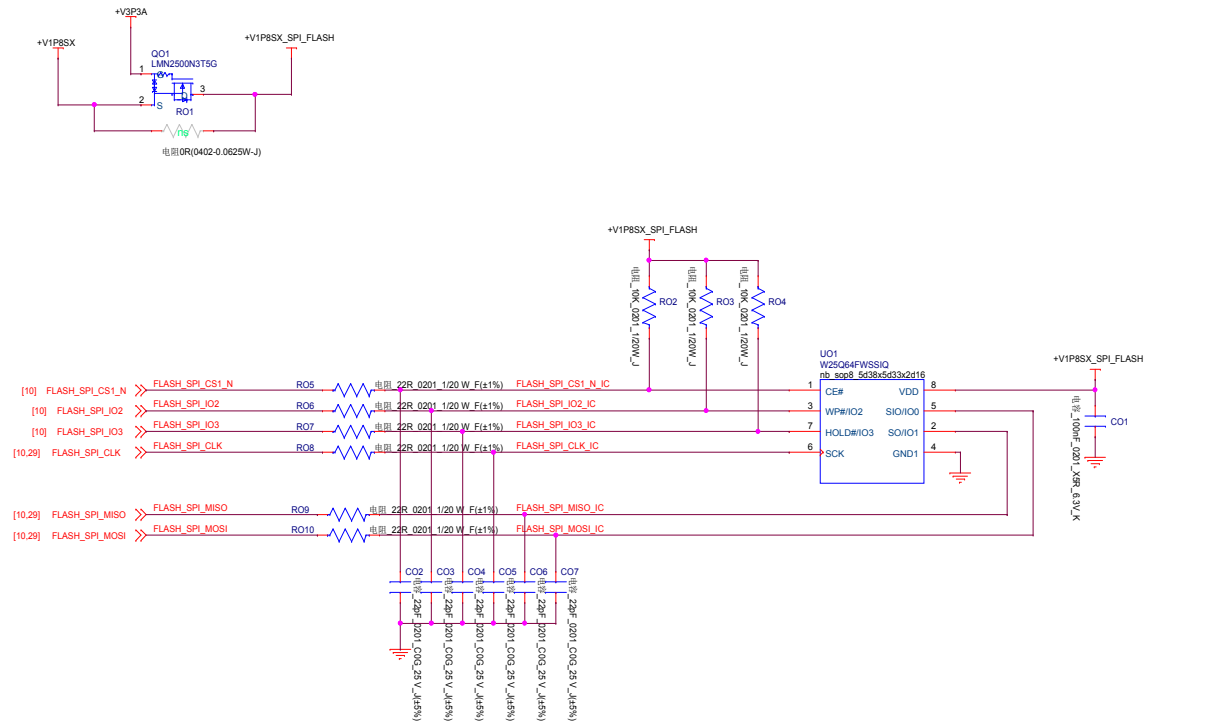


DECOUPLING CAPACITORS FOR MEMORY DOWN

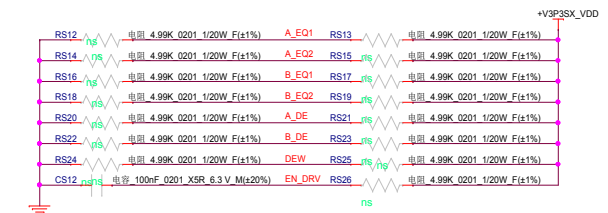


MEMORY TERMINATIONS FOR MEMORY DOWN

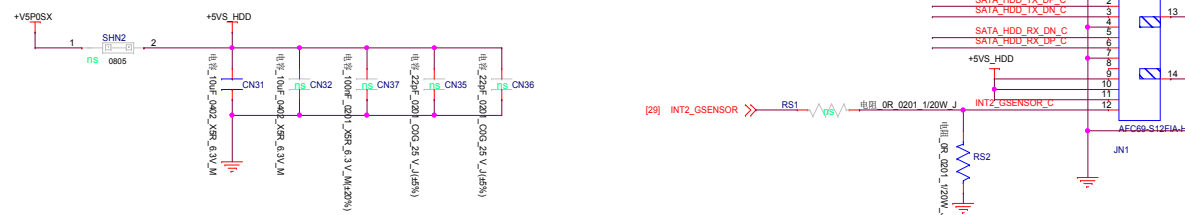




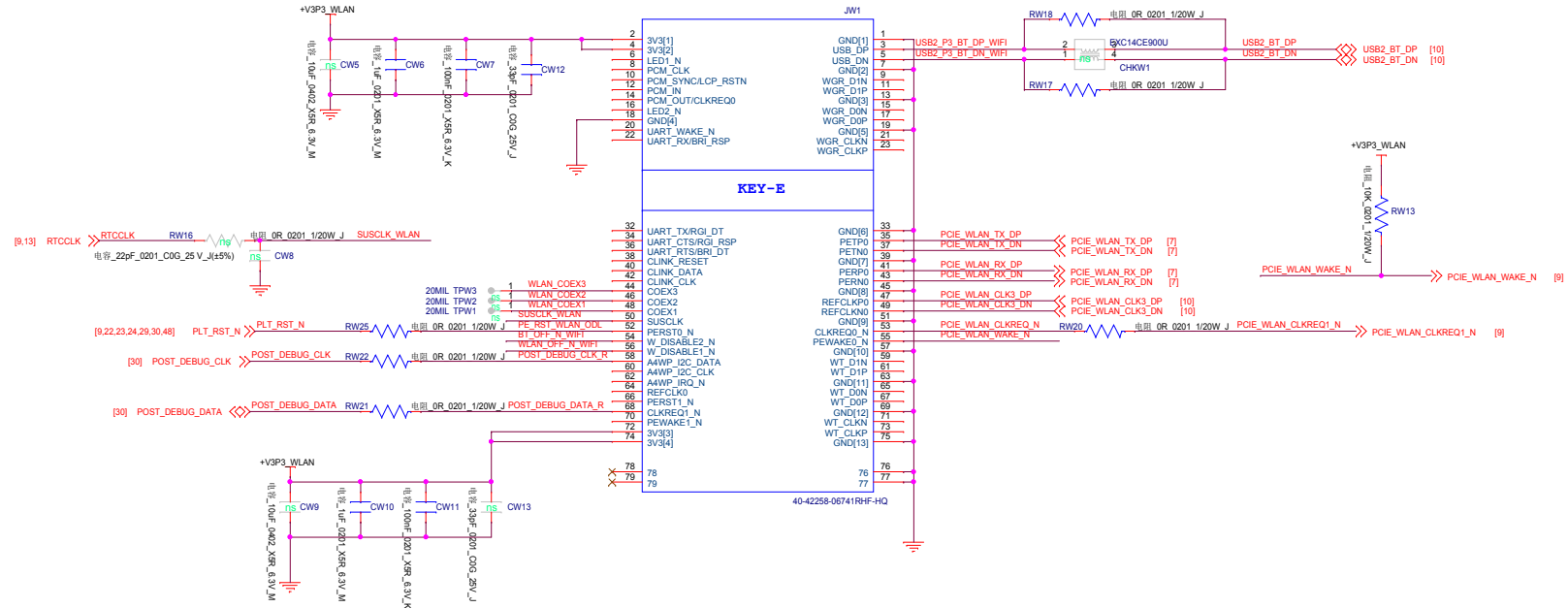
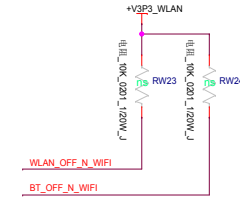
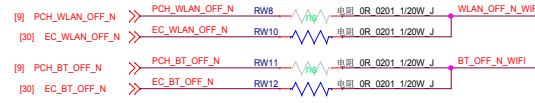
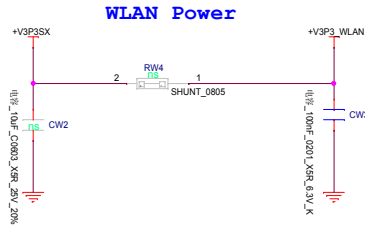
SATA HDD CONN



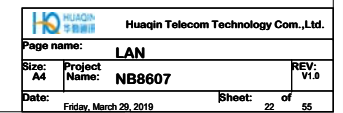
De-emphasis width adjustment, internally pulled down
[DEW] ==
L: for SATA3
H: for SATA2



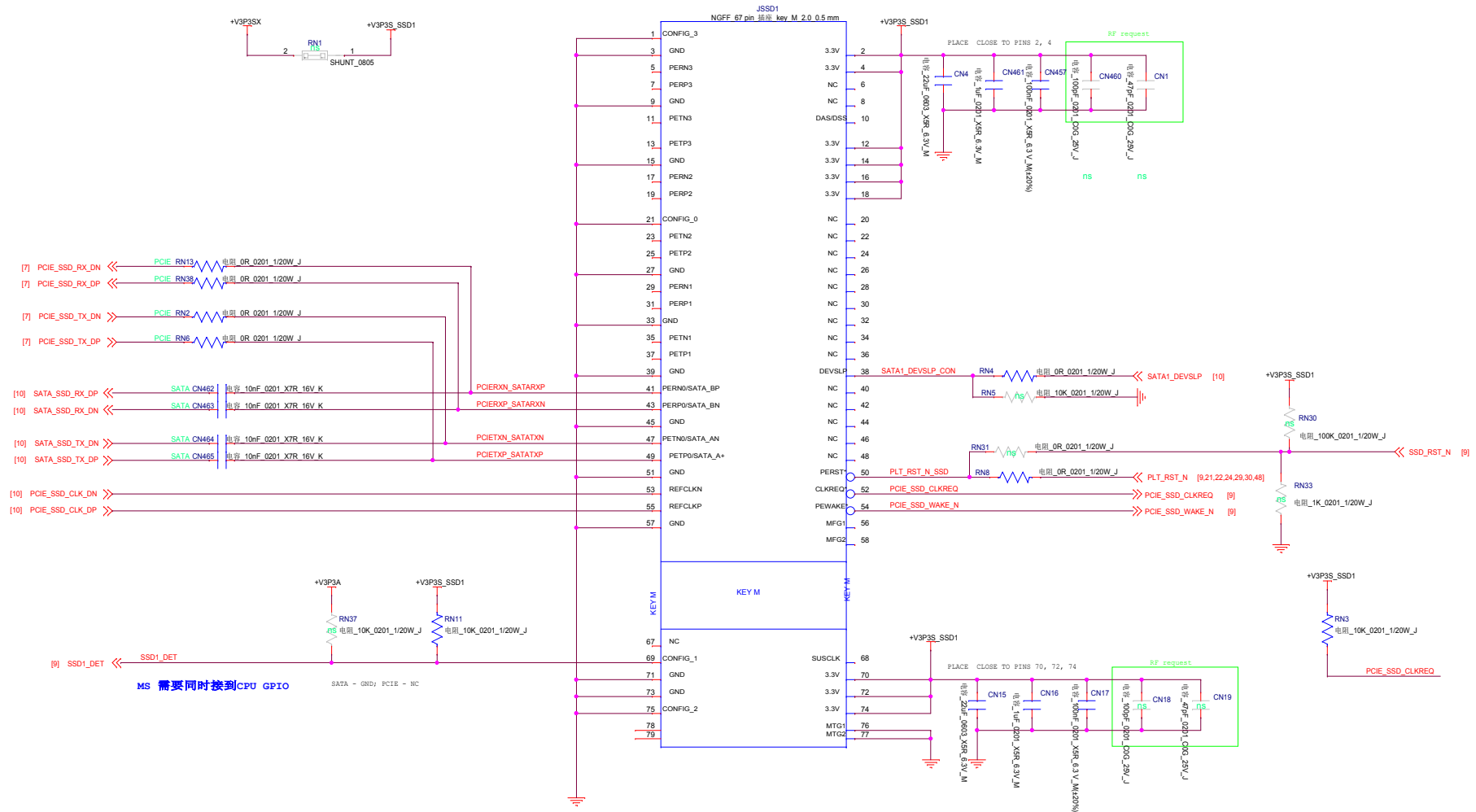
WLAN

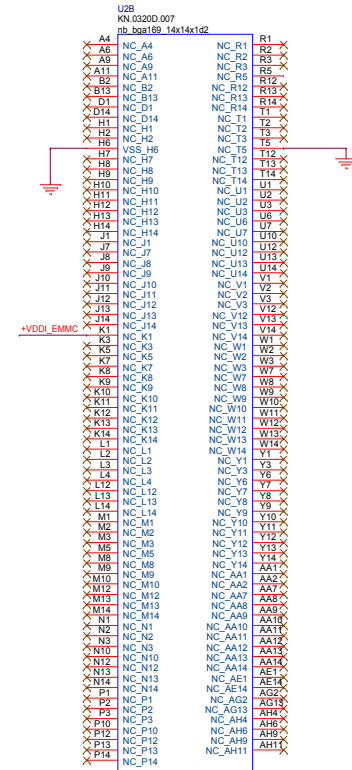
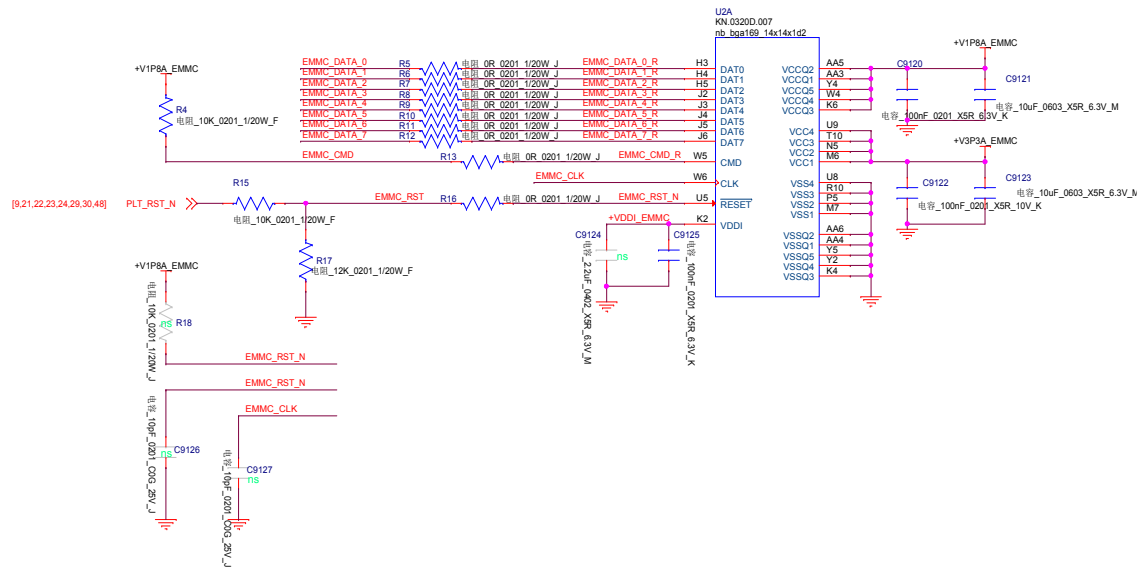
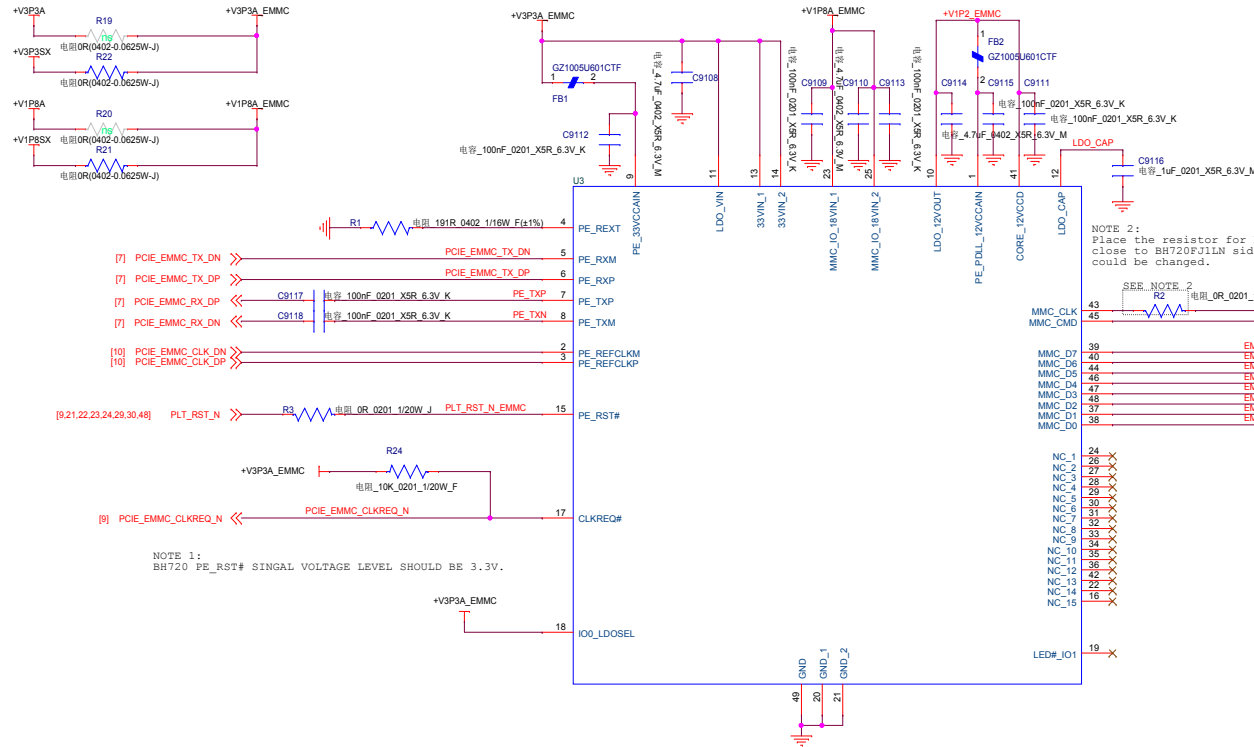


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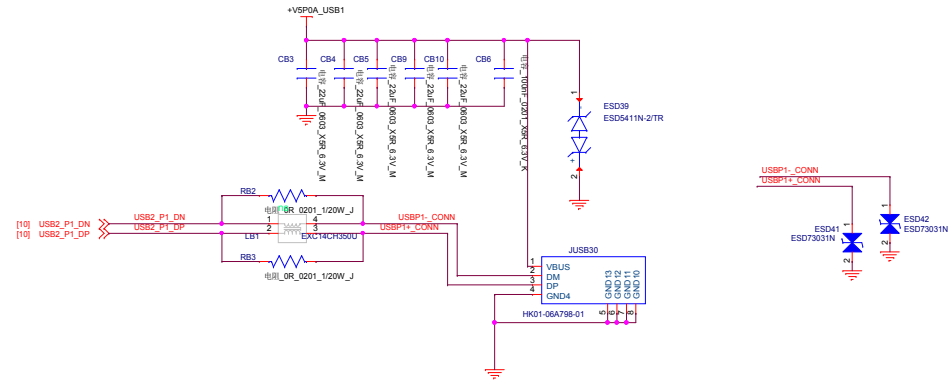


SSD CONN

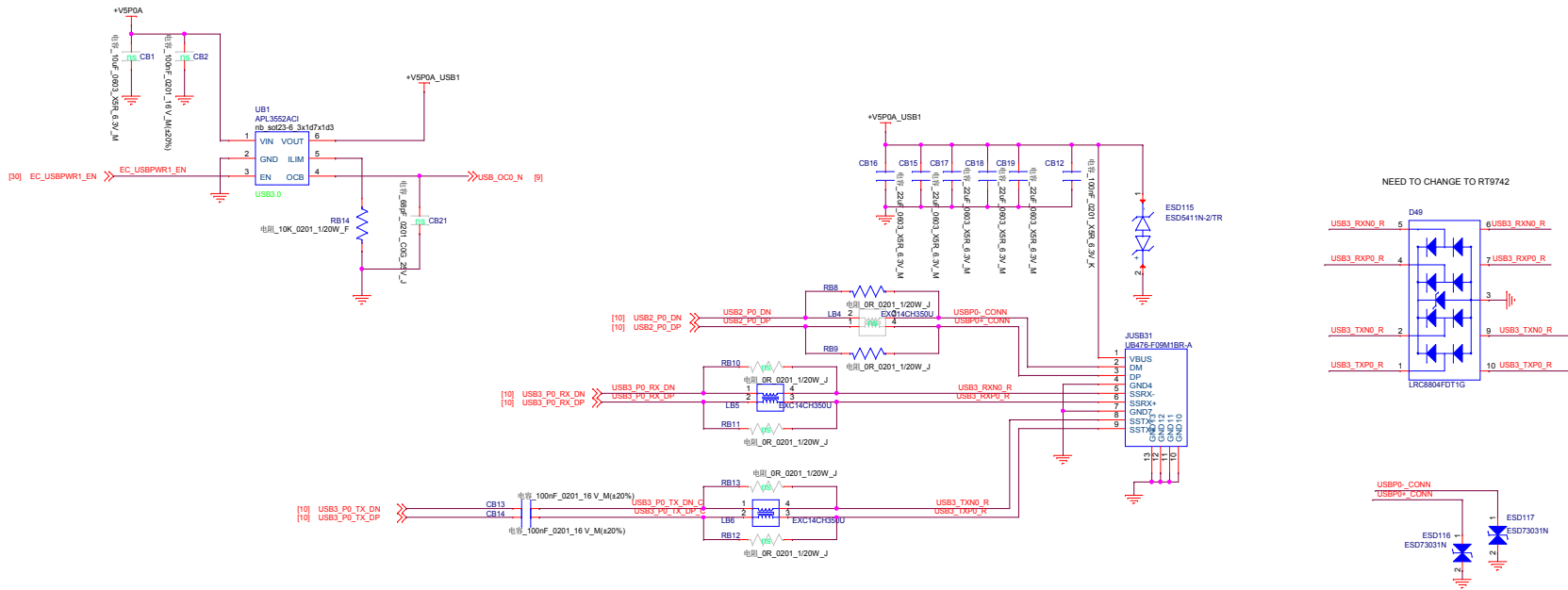




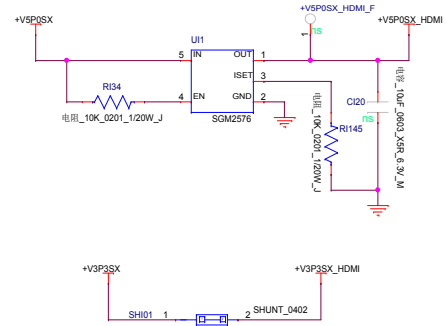
USB2.0 CONN



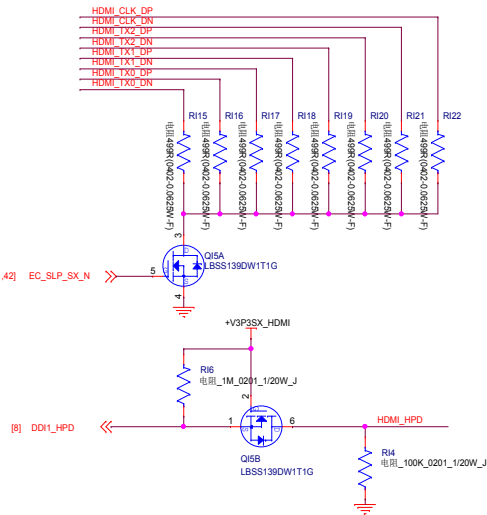
USB3.0 CONN



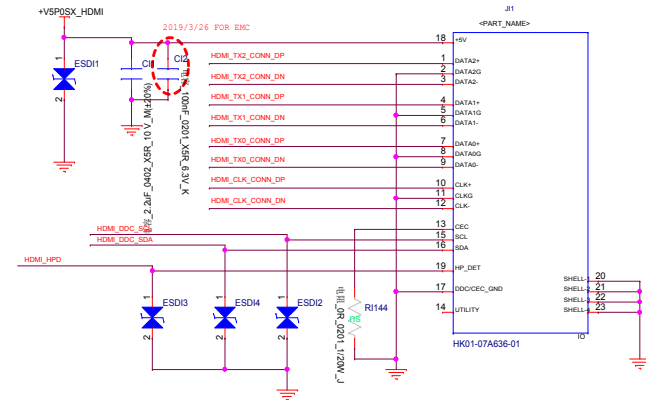
HDMI power



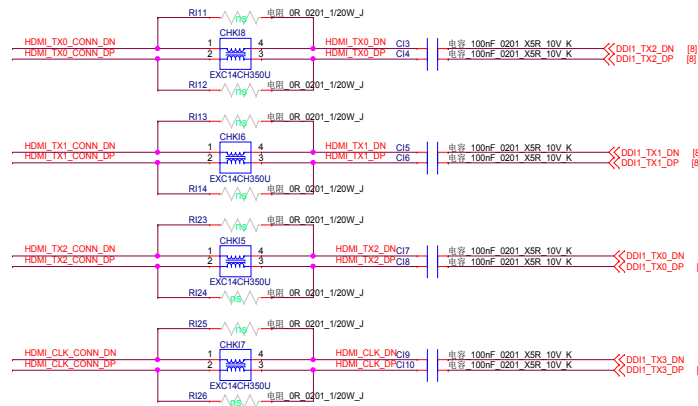
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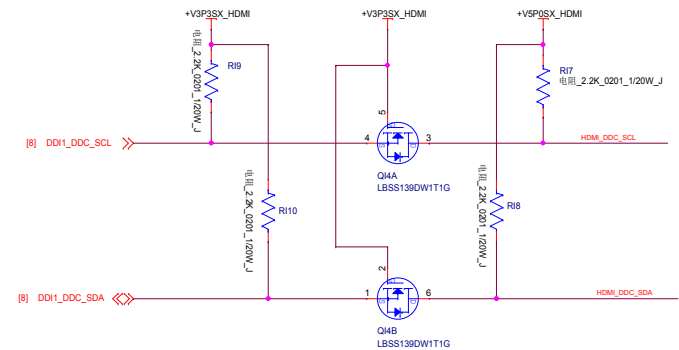
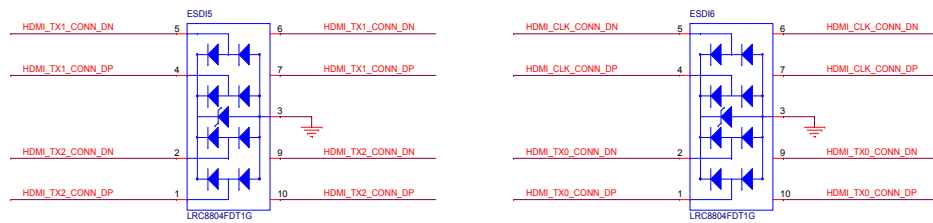
HDMI CONN



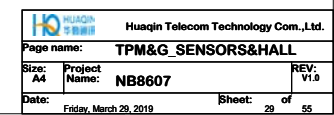
Signal

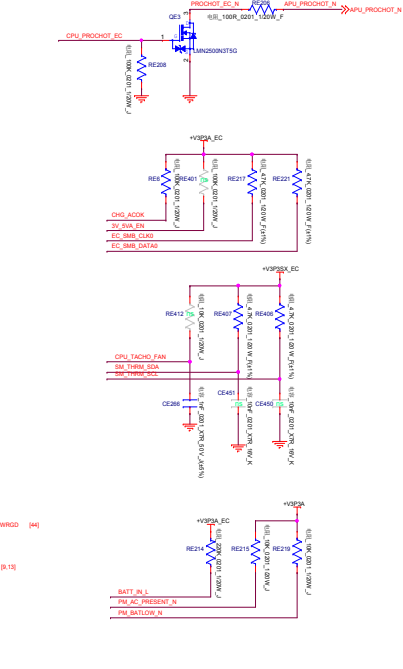
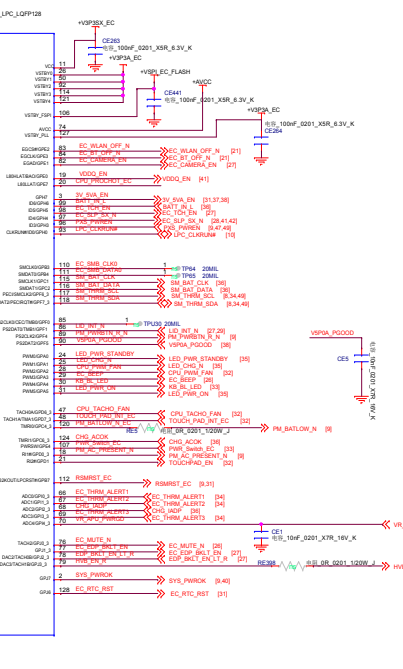
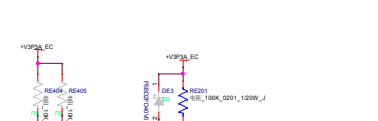
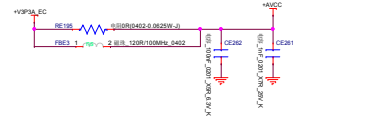
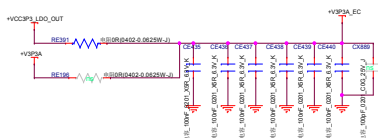


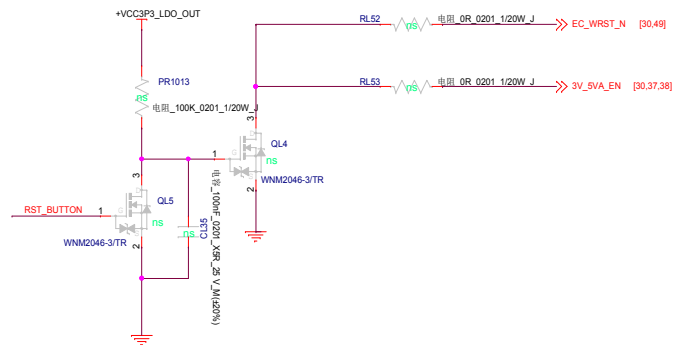
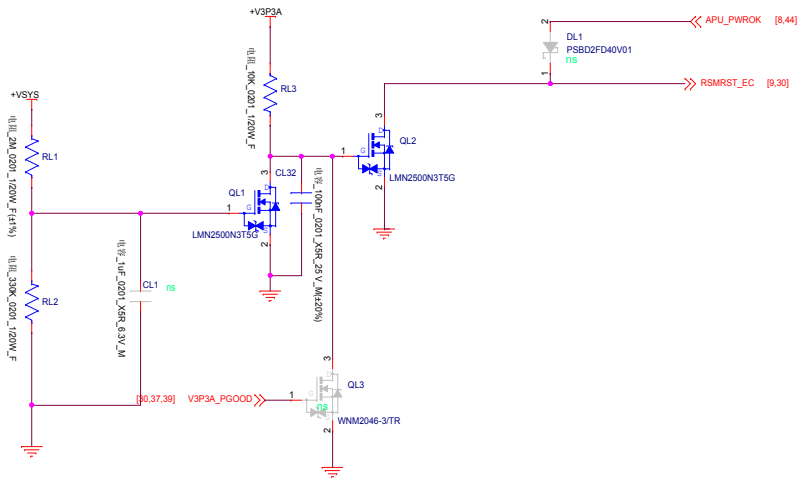
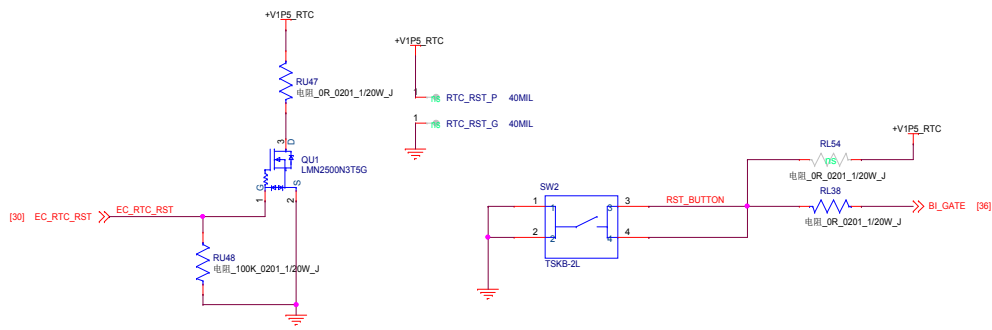
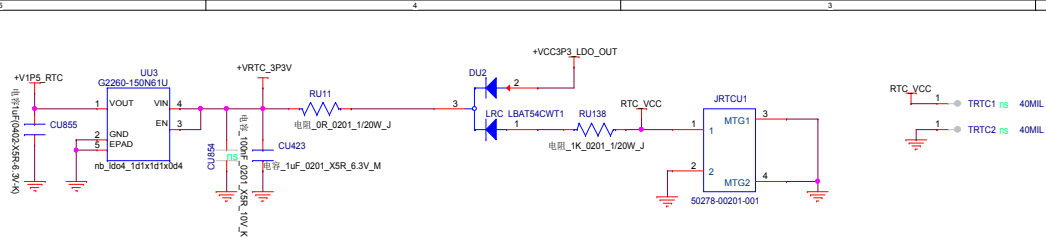
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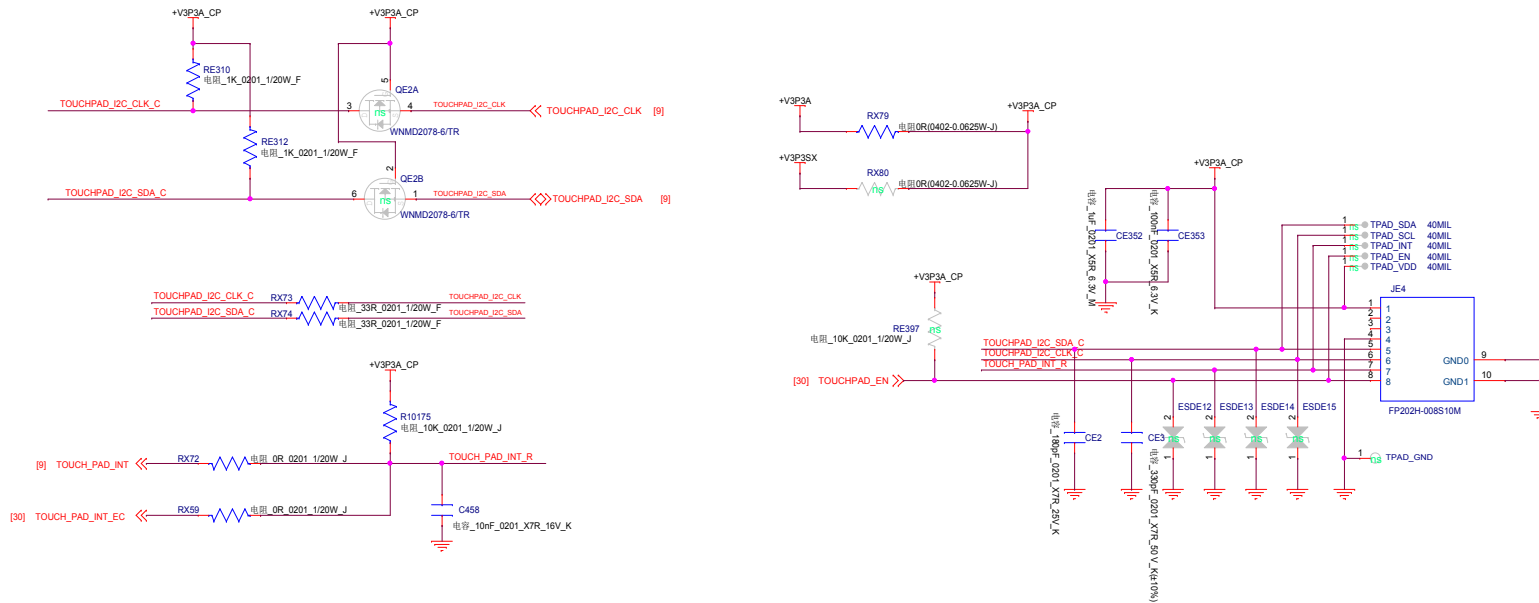
G-SENSOR



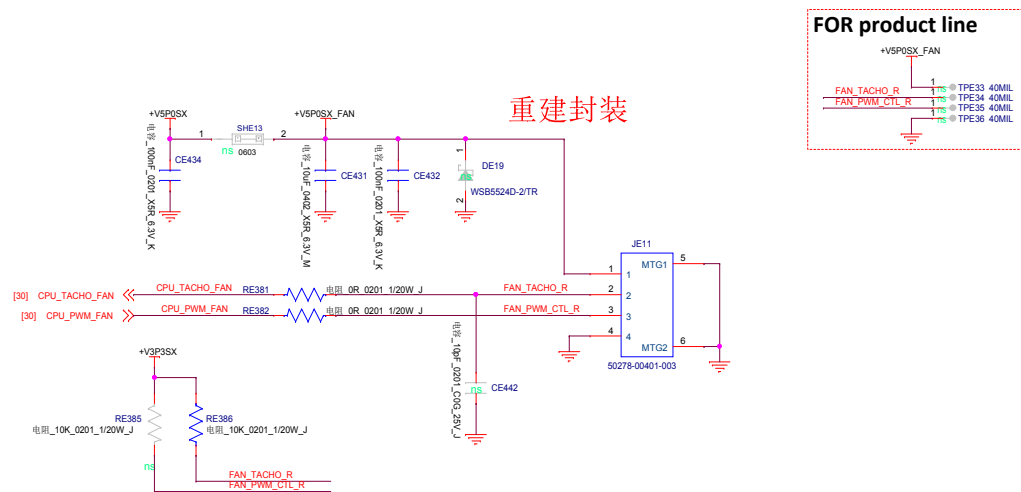




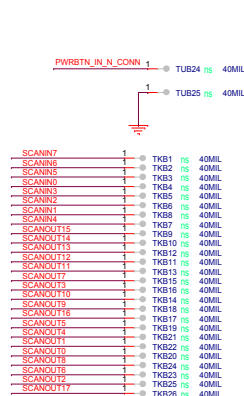
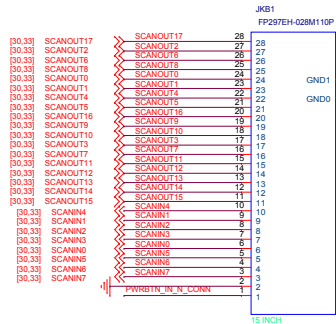
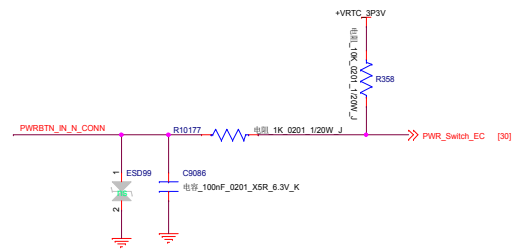
TOUCH PAD



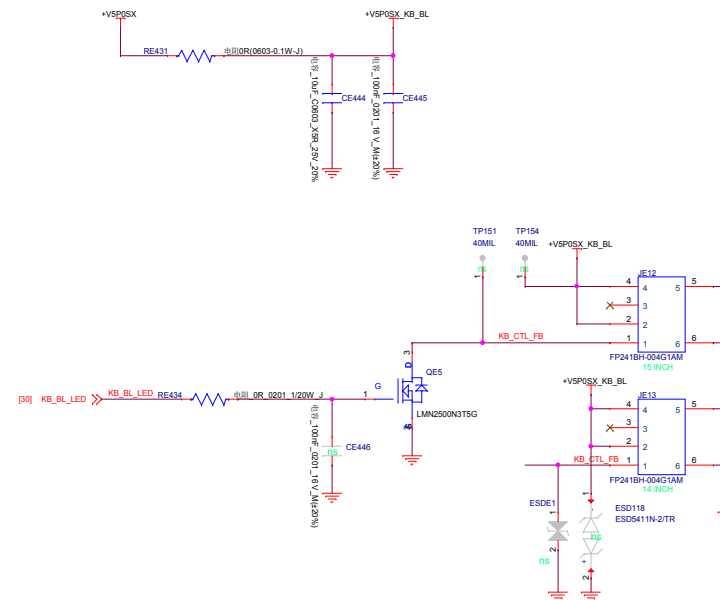
FAN CONN



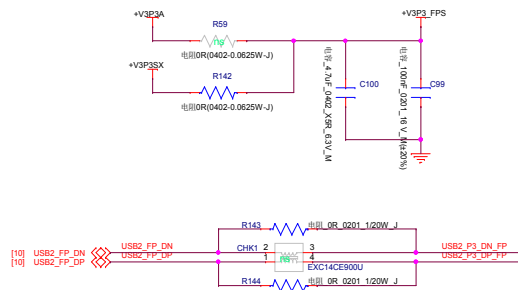
KB CONN



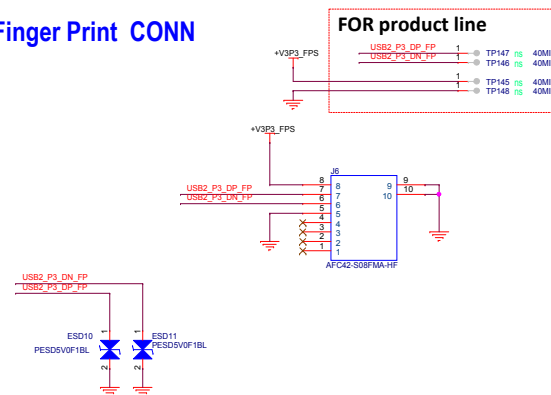
KB Backlight



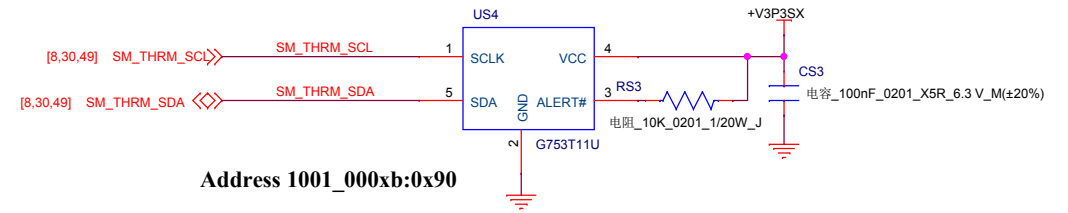
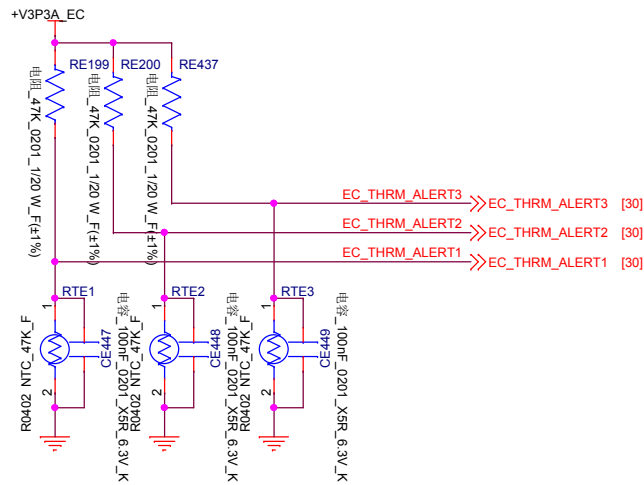
Finger Print




Finger Print CONN



Thermal sensor

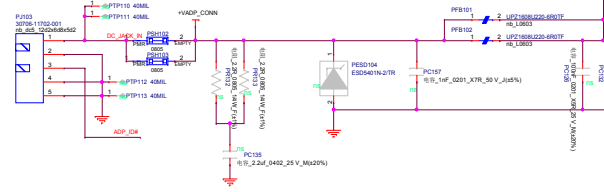


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Size: A4	Project Name: NB8607	REV: V1.0	
Date: Saturday, March 30, 2019	Sheet: 34	of 55	

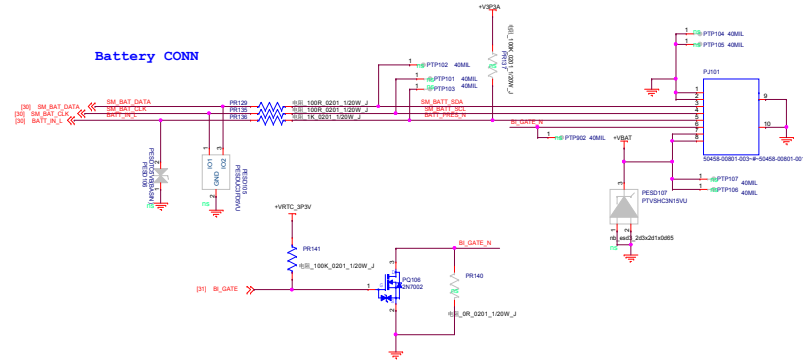
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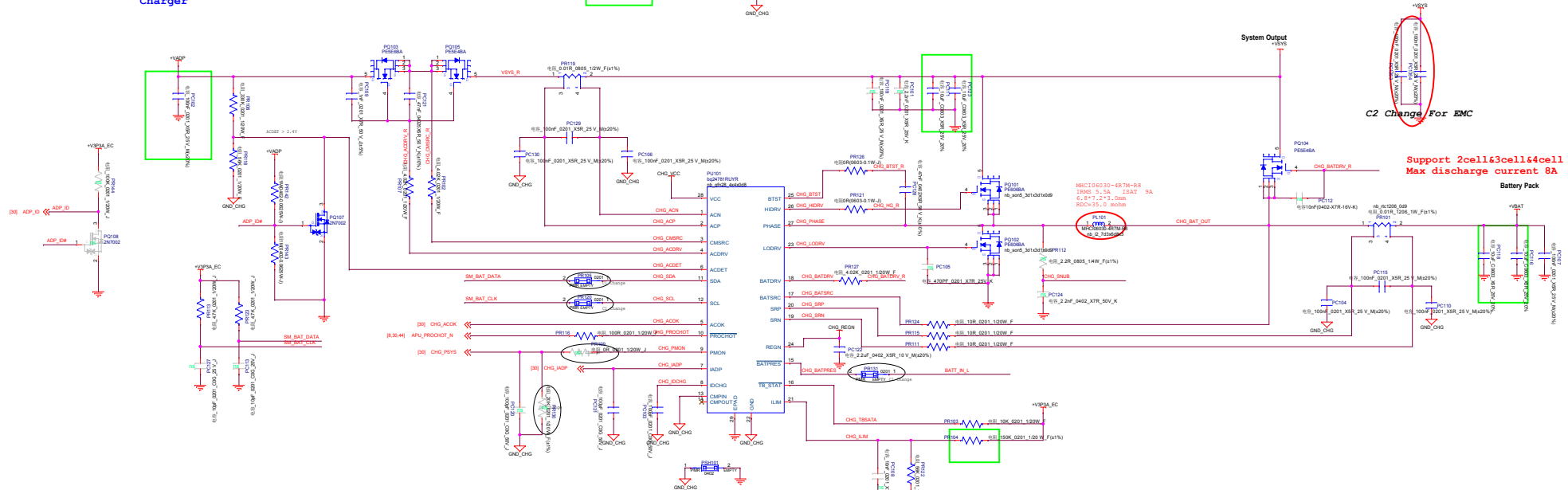
DC-IN



Battery CONN



Charger

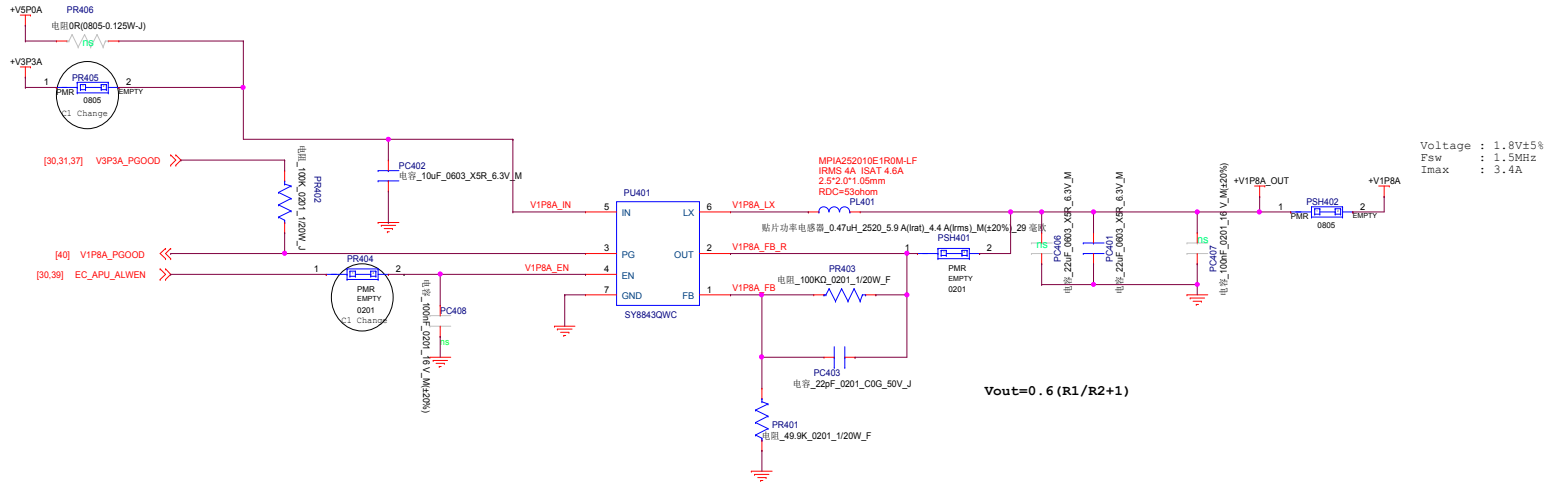


C2 Change For EMC

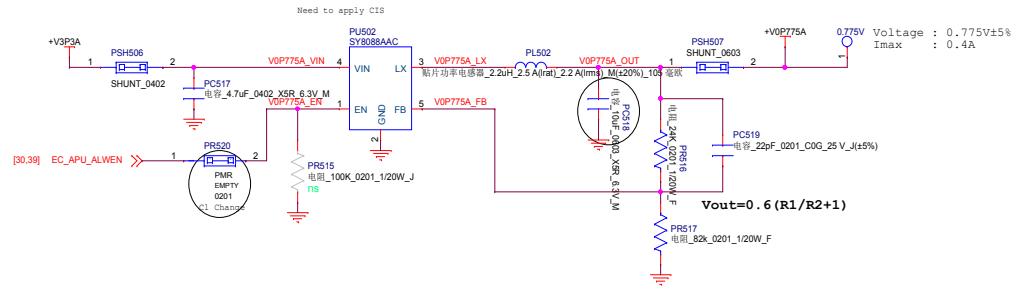
Support 2cell16cell14cell 48W
Max discharge current 8A

Battery Pack

+V1P8A

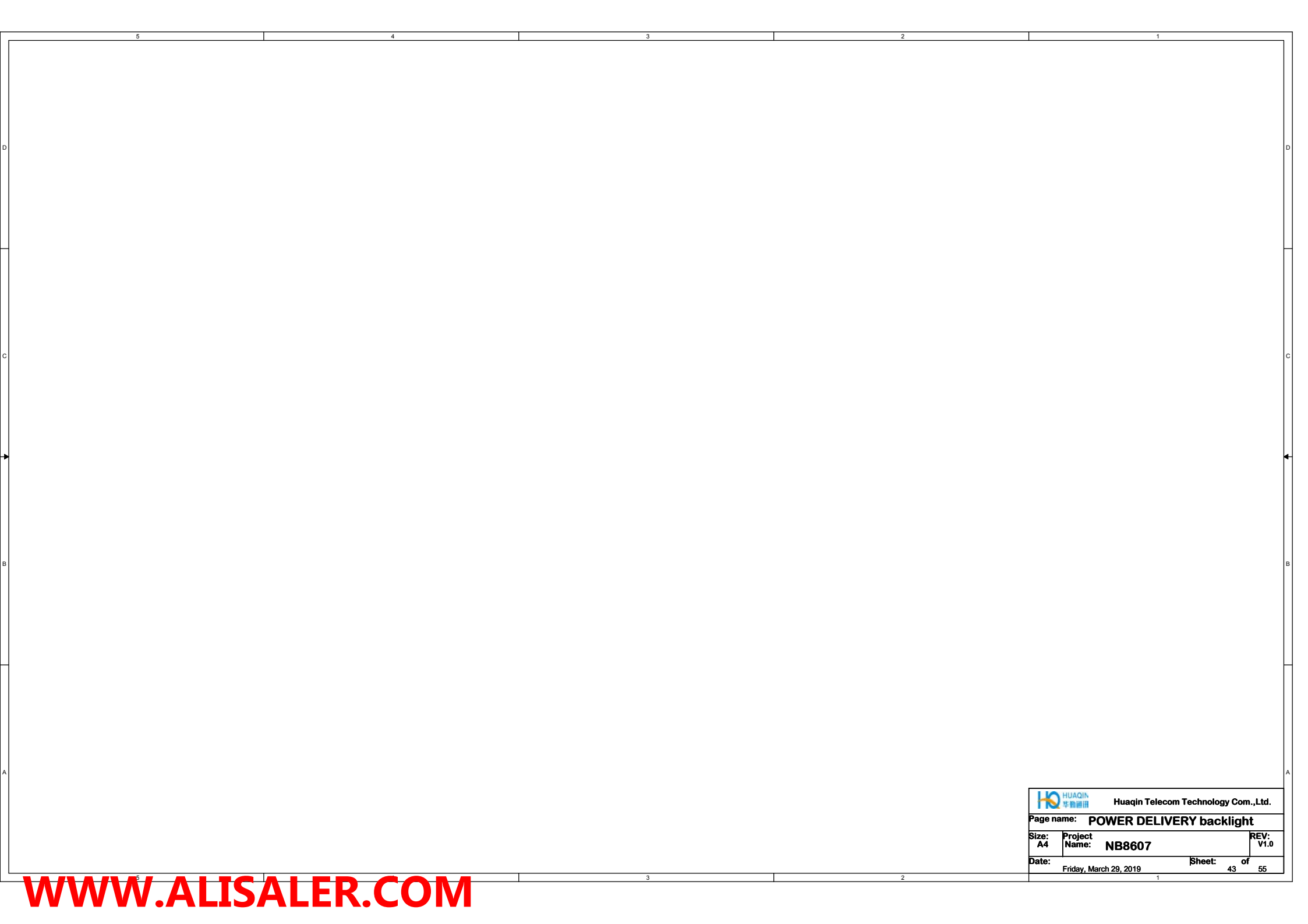



+V0P775A

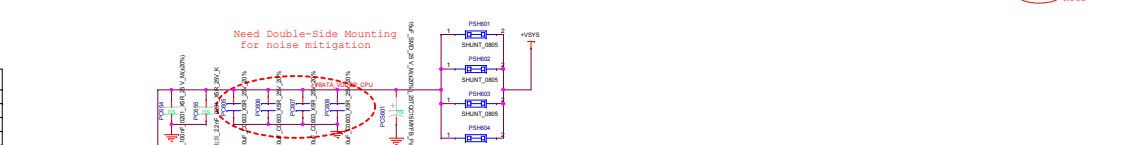
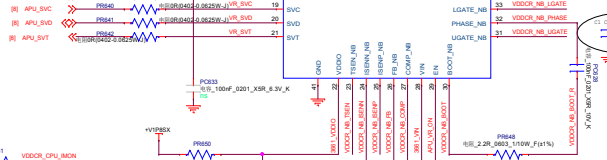
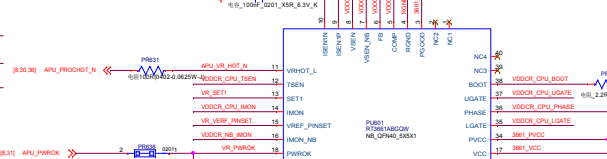
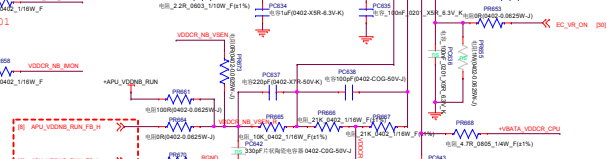
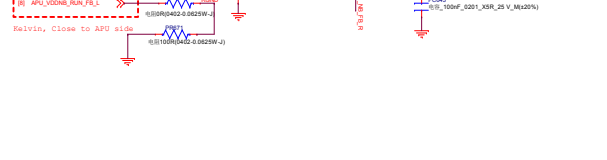



[illegible]

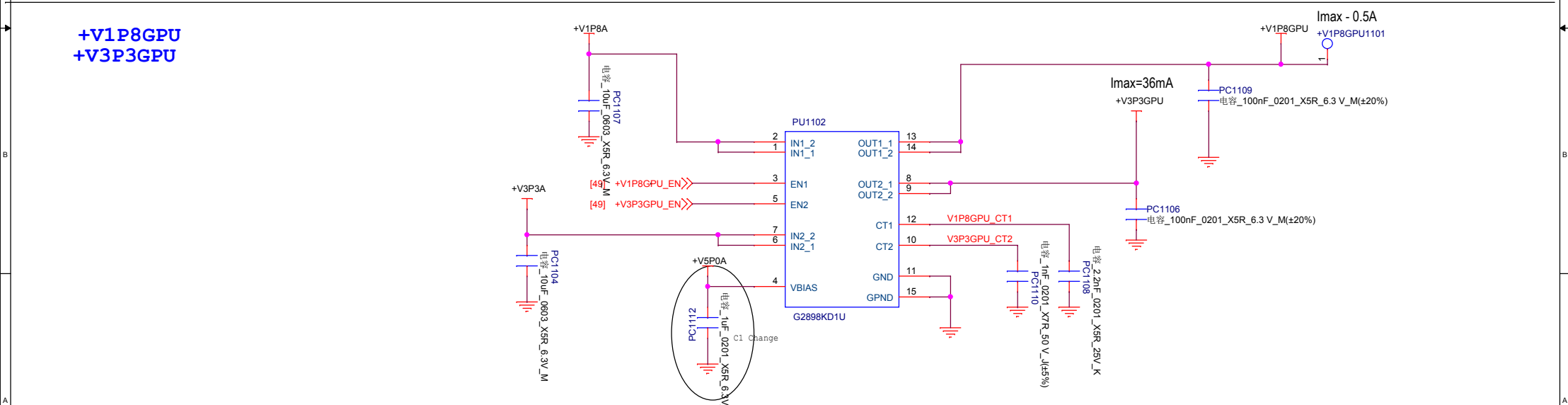
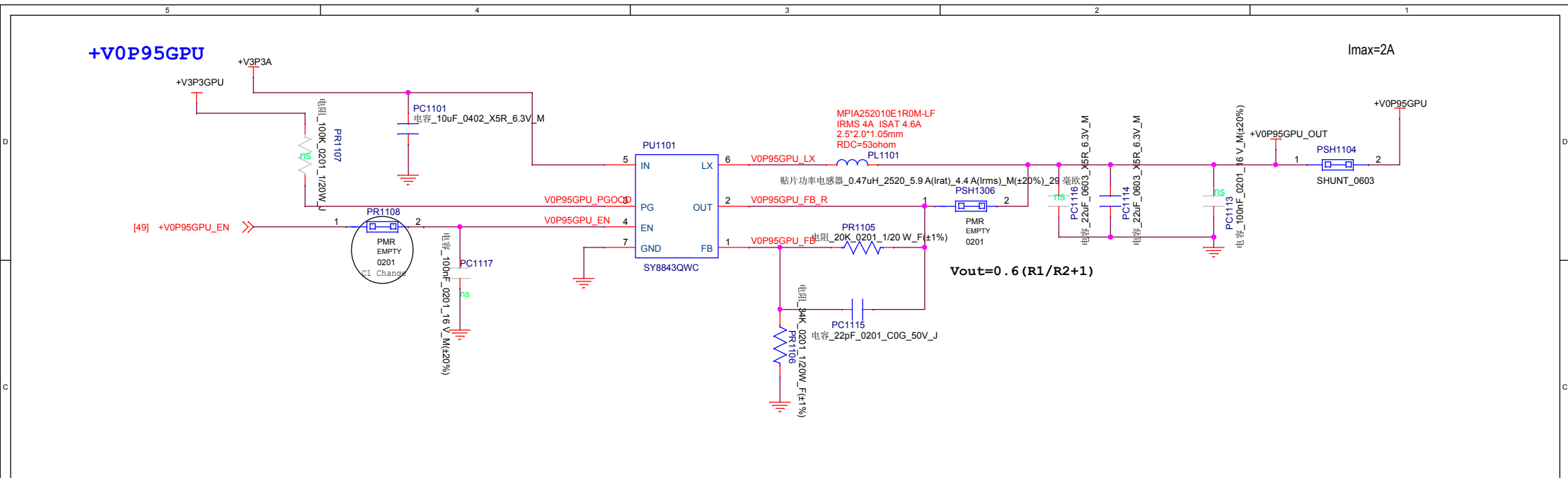
ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A




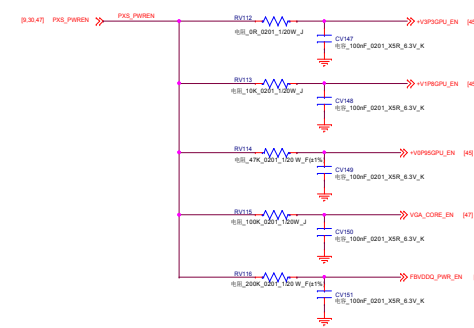
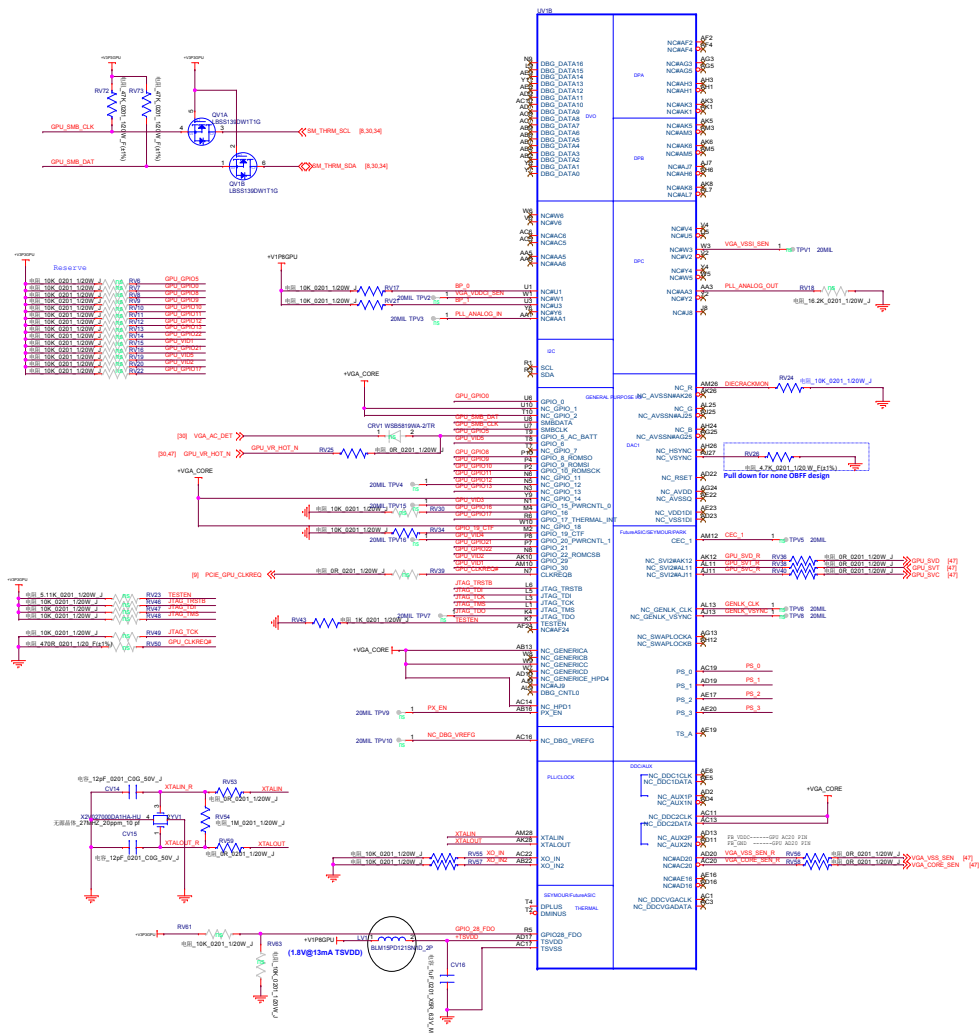
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Page name: POWER DELIVERY backlight			
Size: A4	Project Name:	NB8607	REV: V1.0
Date:	Friday, March 29, 2019		Sheet: 43 of 55

[illegible][illegible][illegible]

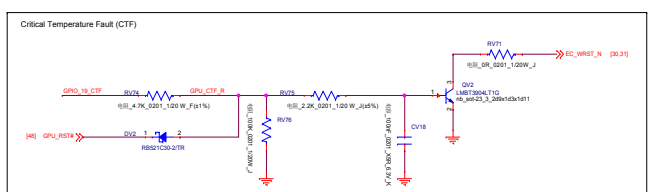
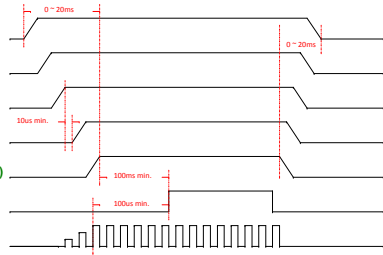
 Huaqin Telecom Technology Com., Ltd.	
Page name: CORE & NB	
Size: A4 Date: Friday, March 29, 2019	Project Name: NB8607 REV: V1.8 Sheet: 44 of 55



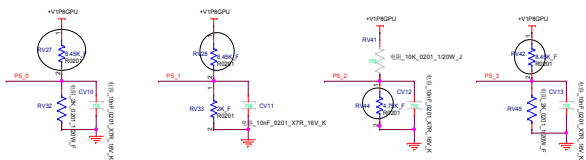
		Huaqin Telecom Technology Com., Ltd.	
Page name:		GPU_LOADSWITCH	
Size: A4	Project Name: NB8607	REV: V1.0	
Date: Tuesday, April 02, 2019	Sheet: 45	of 55	



VDD3(+V3P3GPU)
VDDCT(+V1P8GPU)
PCIE_VDDC(+V0P95GPU)
VDDR1(+V1P35GPU)
VDDC/VDDCI(+VGA_CORE)
PERSTb(GPU_RST#)
REFCLK(CLK_PCIE_VGA)



SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[0]	NA	Reserved for internal use only. Must be 0 at reset.	0
PS_0[1]	NA	Reserved.	0
PS_0[2]	NA	Reserved.	0
PS_0[3]	NA	Reserved.	0
PS_0[4]	NA	Reserved.	0
PS_0[5]	NA	Reserved.	0
PS_0[6]	NA	Reserved.	0
PS_0[7]	NA	Reserved.	0
PS_0[8]	NA	Reserved.	0
PS_0[9]	NA	Reserved.	0
PS_0[10]	NA	Reserved.	0
PS_0[11]	NA	Reserved.	0
PS_0[12]	NA	Reserved.	0
PS_0[13]	NA	Reserved.	0
PS_0[14]	NA	Reserved.	0
PS_0[15]	NA	Reserved.	0
PS_0[16]	NA	Reserved.	0
PS_0[17]	NA	Reserved.	0
PS_0[18]	NA	Reserved.	0
PS_0[19]	NA	Reserved.	0
PS_0[20]	NA	Reserved.	0
PS_0[21]	NA	Reserved.	0
PS_0[22]	NA	Reserved.	0
PS_0[23]	NA	Reserved.	0
PS_0[24]	NA	Reserved.	0
PS_0[25]	NA	Reserved.	0
PS_0[26]	NA	Reserved.	0
PS_0[27]	NA	Reserved.	0
PS_0[28]	NA	Reserved.	0
PS_0[29]	NA	Reserved.	0
PS_0[30]	NA	Reserved.	0
PS_0[31]	NA	Reserved.	0
PS_0[32]	NA	Reserved.	0
PS_0[33]	NA	Reserved.	0
PS_0[34]	NA	Reserved.	0
PS_0[35]	NA	Reserved.	0
PS_0[36]	NA	Reserved.	0
PS_0[37]	NA	Reserved.	0
PS_0[38]	NA	Reserved.	0
PS_0[39]	NA	Reserved.	0
PS_0[40]	NA	Reserved.	0
PS_0[41]	NA	Reserved.	0
PS_0[42]	NA	Reserved.	0
PS_0[43]	NA	Reserved.	0
PS_0[44]	NA	Reserved.	0
PS_0[45]	NA	Reserved.	0
PS_0[46]	NA	Reserved.	0
PS_0[47]	NA	Reserved.	0
PS_0[48]	NA	Reserved.	0
PS_0[49]	NA	Reserved.	0
PS_0[50]	NA	Reserved.	0
PS_0[51]	NA	Reserved.	0
PS_0[52]	NA	Reserved.	0
PS_0[53]	NA	Reserved.	0
PS_0[54]	NA	Reserved.	0
PS_0[55]	NA	Reserved.	0
PS_0[56]	NA	Reserved.	0
PS_0[57]	NA	Reserved.	0
PS_0[58]	NA	Reserved.	0
PS_0[59]	NA	Reserved.	0
PS_0[60]	NA	Reserved.	0
PS_0[61]	NA	Reserved.	0
PS_0[62]	NA	Reserved.	0
PS_0[63]	NA	Reserved.	0
PS_0[64]	NA	Reserved.	0
PS_0[65]	NA	Reserved.	0
PS_0[66]	NA	Reserved.	0
PS_0[67]	NA	Reserved.	0
PS_0[68]	NA	Reserved.	0
PS_0[69]	NA	Reserved.	0
PS_0[70]	NA	Reserved.	0
PS_0[71]	NA	Reserved.	0
PS_0[72]	NA	Reserved.	0
PS_0[73]	NA	Reserved.	0
PS_0[74]	NA	Reserved.	0
PS_0[75]	NA	Reserved.	0
PS_0[76]	NA	Reserved.	0
PS_0[77]	NA	Reserved.	0
PS_0[78]	NA	Reserved.	0
PS_0[79]	NA	Reserved.	0
PS_0[80]	NA	Reserved.	0
PS_0[81]	NA	Reserved.	0
PS_0[82]	NA	Reserved.	0
PS_0[83]	NA	Reserved.	0
PS_0[84]	NA	Reserved.	0
PS_0[85]	NA	Reserved.	0
PS_0[86]	NA	Reserved.	0
PS_0[87]	NA	Reserved.	0
PS_0[88]	NA	Reserved.	0
PS_0[89]	NA	Reserved.	0
PS_0[90]	NA	Reserved.	0
PS_0[91]	NA	Reserved.	0
PS_0[92]	NA	Reserved.	0
PS_0[93]	NA	Reserved.	0
PS_0[94]	NA	Reserved.	0
PS_0[95]	NA	Reserved.	0
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PS_0[100]	NA	Reserved.	0
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PS_0[102]	NA	Reserved.	0
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PS_0[107]	NA	Reserved.	0
PS_0[108]	NA	Reserved.	0
PS_0[109]	NA	Reserved.	0
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PS_0[124]	NA	Reserved.	0
PS_0[125]	NA	Reserved.	0
PS_0[126]	NA	Reserved.	0
PS_0[127]	NA	Reserved.	0
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PS_0[137]	NA	Reserved.	0
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PS_0[140]	NA	Reserved.	0
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PS_0[162]	NA	Reserved.	0
PS_0[163]	NA	Reserved.	0
PS_0[164]	NA	Reserved.	0
PS_0[165]	NA	Reserved.	0
PS_0[166]	NA	Reserved.	0
PS_0[167]	NA	Reserved.	0
PS_0[168]	NA	Reserved.	0
PS_0[169]	NA	Reserved.	0
PS_0[170]	NA	Reserved.	0
PS_0[171]	NA	Reserved.	0
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PS_0[174]	NA	Reserved.	0
PS_0[175]	NA	Reserved.	0
PS_0[176]	NA	Reserved.	0
PS_0[177]	NA	Reserved.	0
PS_0[178]	NA	Reserved.	0
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PS_0[180]	NA	Reserved.	0
PS_0[181]	NA	Reserved.	0
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PS_0[193]	NA	Reserved.	0
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PS_0[197]	NA	Reserved.	0
PS_0[198]	NA	Reserved.	0
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PS_0[205]	NA	Reserved.	0
PS_0[206]	NA	Reserved.	0
PS_0[207]	NA	Reserved.	0
PS_0[208]	NA	Reserved.	0
PS_0[209]	NA	Reserved.	0
PS_0[210]	NA	Reserved.	0
PS_0[211]	NA	Reserved.	0
PS_0[212]	NA	Reserved.	0
PS_0[213]	NA	Reserved.	0
PS_0[214]	NA	Reserved.	0
PS_0[215]	NA	Reserved.	0
PS_0[216]	NA	Reserved.	0
PS_0[217]	NA	Reserved.	0
PS_0[218]	NA	Reserved.	0
PS_0[219]	NA	Reserved.	0
PS_0[220]	NA	Reserved.	0
PS_0[221]	NA	Reserved.	0
PS_0[222]	NA	Reserved.	0
PS_0[223]	NA	Reserved.	0
PS_0[224]	NA	Reserved.	0
PS_0[225]	NA	Reserved.	0
PS_0[226]	NA	Reserved.	0
PS_0[227]	NA	Reserved.	0
PS_0[228]	NA	Reserved.	0
PS_0[229]	NA	Reserved.	0
PS_0[230]	NA	Reserved.	0
PS_0[231]	NA	Reserved.	0
PS_0[232]	NA	Reserved.	0
PS_0[233]	NA	Reserved.	0
PS_0[234]	NA	Reserved.	0
PS_0[235]	NA	Reserved.	0
PS_0[236]	NA	Reserved.	0
PS_0[237]	NA	Reserved.	0
PS_0[238]	NA	Reserved.	0
PS_0[239]	NA	Reserved.	0
PS_0[240]	NA	Reserved.	0
PS_0[241]	NA	Reserved.	0
PS_0[242]	NA	Reserved.	0
PS_0[243]	NA	Reserved.	0
PS_0[244]	NA	Reserved.	0
PS_0[245]	NA	Reserved.	0
PS_0[246]	NA	Reserved.	0
PS_0[247]	NA	Reserved.	0
PS_0[248]	NA	Reserved.	0
PS_0[249]	NA	Reserved.	0
PS_0[250]	NA	Reserved.	0
PS_0[251]	NA	Reserved.	0
PS_0[252]	NA	Reserved.	0
PS_0[253]	NA	Reserved.	0
PS_0[254]	NA	Reserved.	0
PS_0[255]	NA	Reserved.	0

Capacitor Value (nF)	Bits [5:4]
100	00
200	01
400	10
800	11

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
5450	2000	001
4950	2000	010
5950	4000	011
4050	4900	100
3240	5920	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

