

# DJ Montevina UMA Schematics Document

## uFCPGA Mobile Penryn

### Intel GM45+ICH9M

2009-08-18

REV : X00

*DY : Nopop Component*

*DJ2 : ASM for DJ2*

*DJ3: ASM for DJ3*

<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title

**Cover Page**

Size  
A3

Document Number

**DJ2 Montevina UMA**

Rev

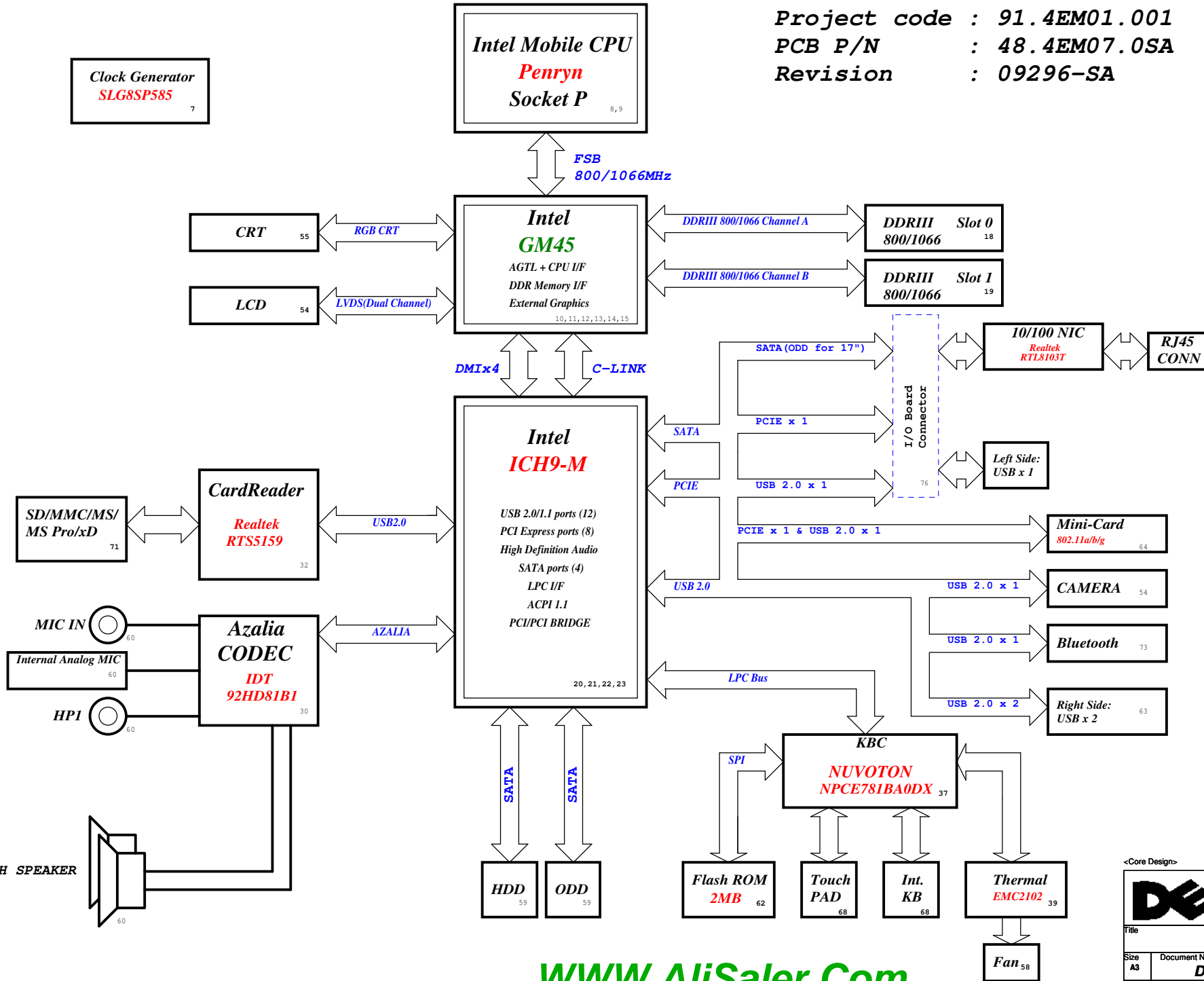
**X00**

Date: Tuesday, August 18, 2009

Sheet 1 of 88

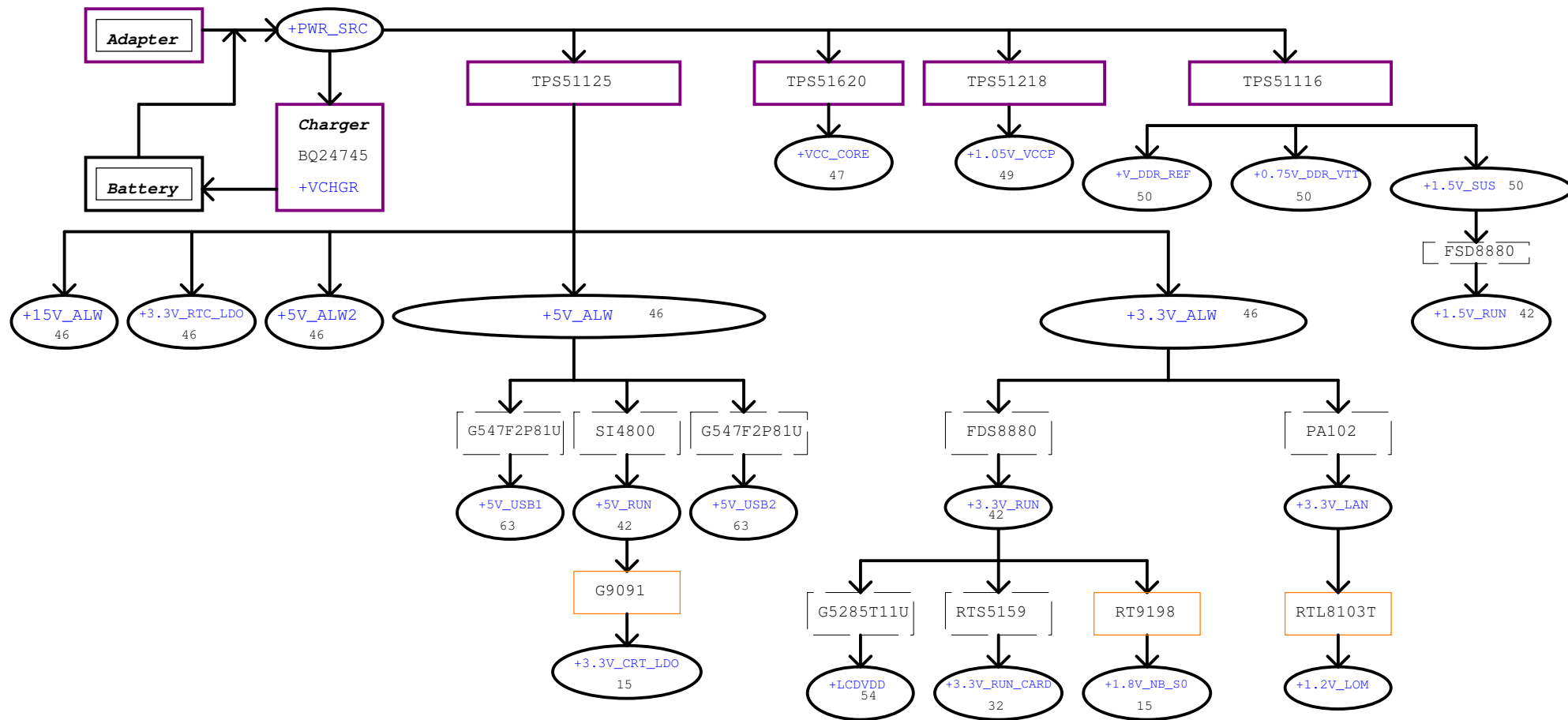
# DJ2 Montevina UMA Block Diagram

Project code : 91.4EM01.001  
PCB P/N : 48.4EM07.0SA  
Revision : 09296-SA



CPU DC/DC TPS51620 <sub>47</sub>	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC TPS51218 <sub>49</sub>	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP
SYSTEM DC/DC TPS51125 <sub>46</sub>	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC TPS51116 <sub>50</sub>	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC Switches <sub>42</sub>	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

# DJ2 Montevina UMA Power Block Diagram



Power Shape

Regulator

LDO

Switch

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Title

**Power Block Diagram**

Size

Document Number

Rev

A3

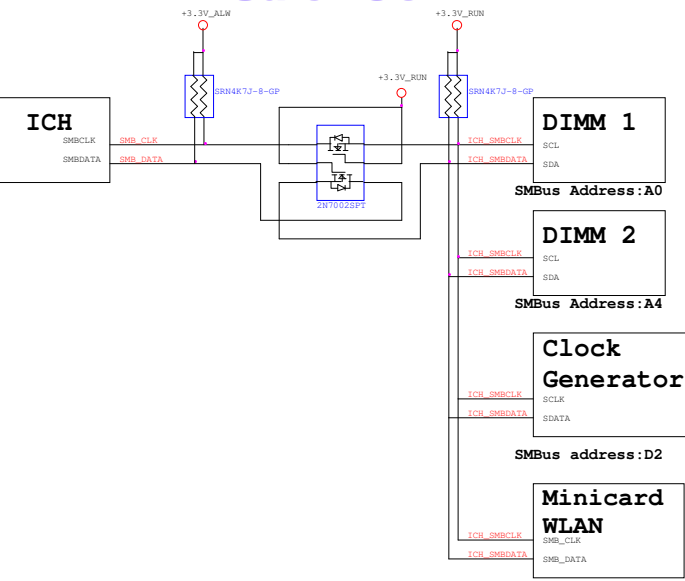
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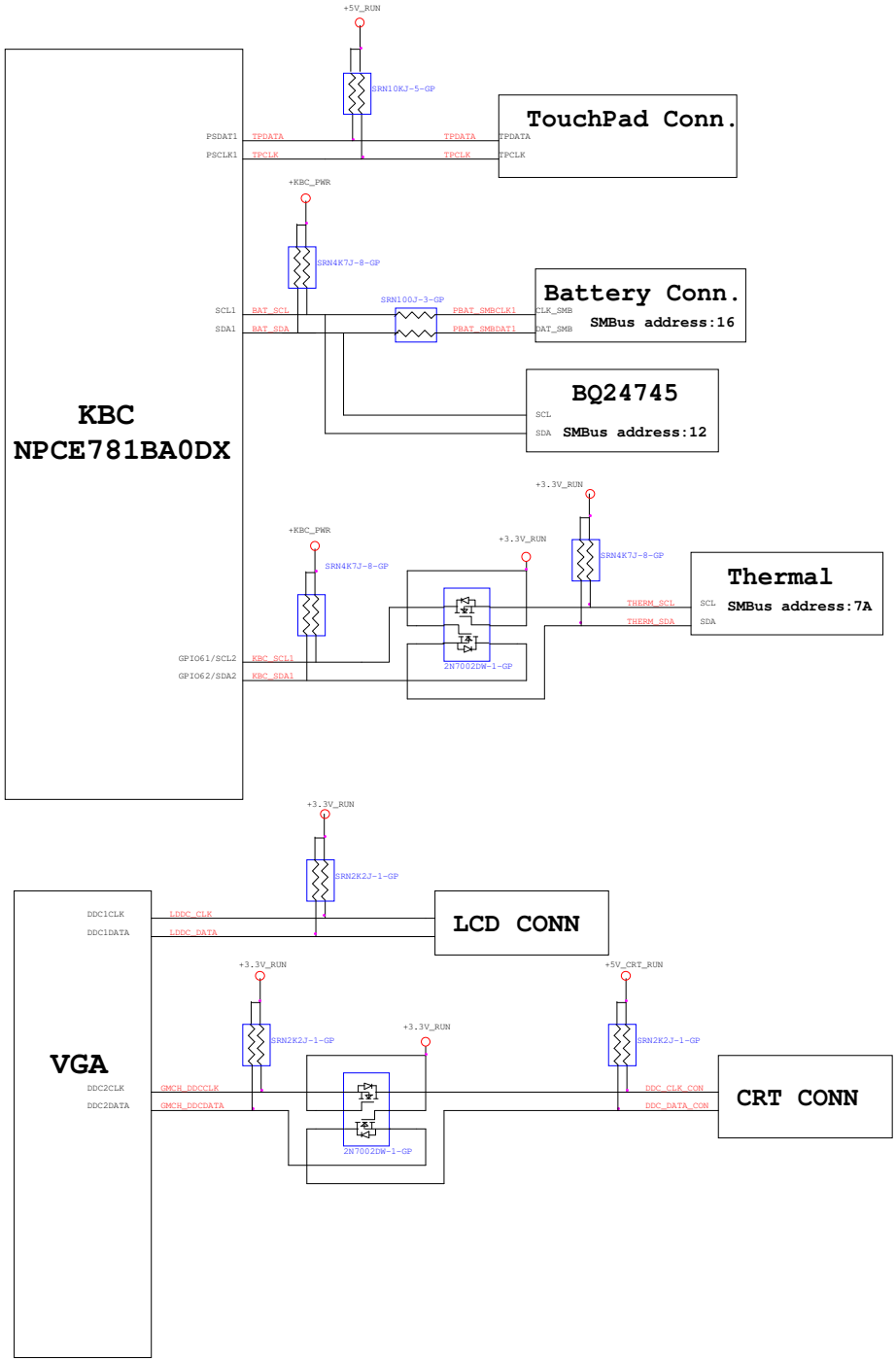
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Sheet 3 of 88

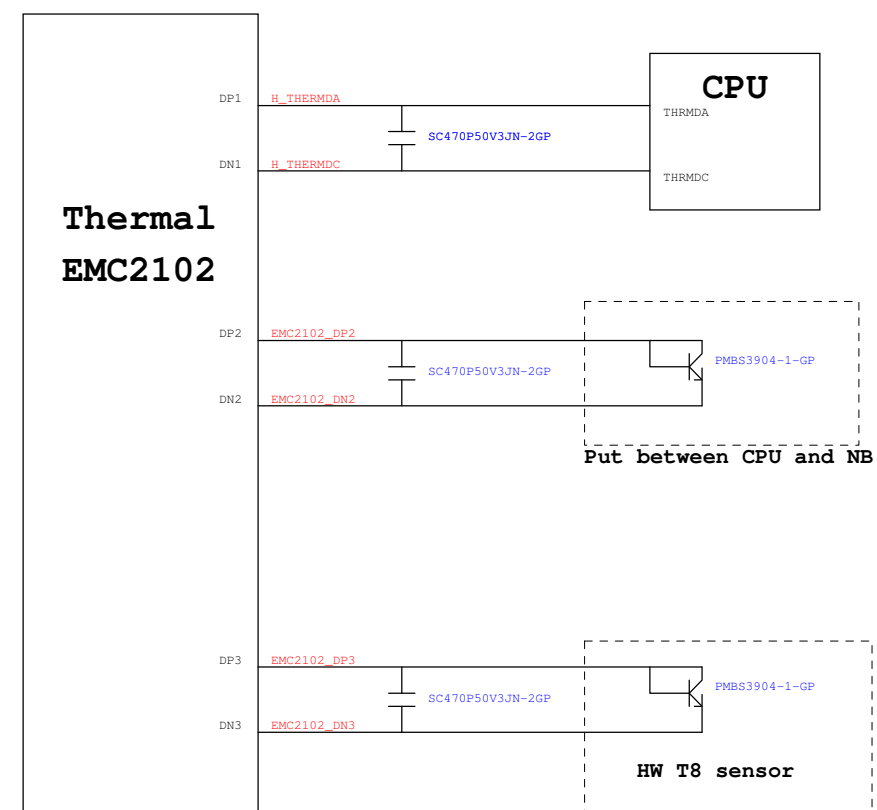
# ICH SMBus Block Diagram



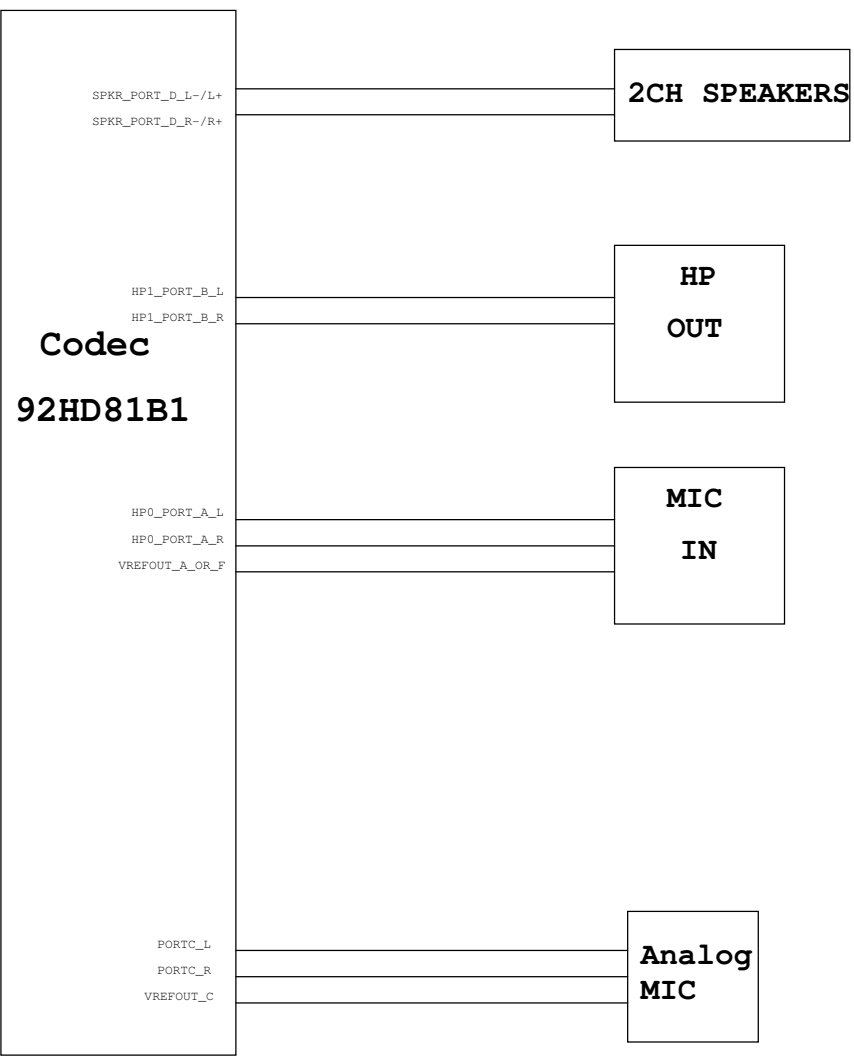
# KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



## ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.2.3

Signal	Usage/When Sampled	Comment															
HDA_SDOUT	XOR Chain Entrance / PCI Express* Port Config 1 bit 1 (Port 1-4), Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset 224h). This signal has a weak internal pull-down.															
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4), Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h).															
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6), Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers: Offset 0224h) when sampled low.															
GPIO20	Reserved, Rising Edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high															
GNT1# / GPIO51	ESI Strap (Server Only), Rising Edge of PWROK.	Tying this strap low configures DMI for ESIncompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.															
GNT3# / GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h: bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.															
GNT0#	Boot BIOS Destination Selection 1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <table border="1"> <thead> <tr> <th>Bit11 (GNT0#)</th><th>Bit 10 (SPI_CS1#)</th><th>Boot BIOS Destination</th></tr> </thead> <tbody> <tr> <td>0</td><td>1</td><td>SPI</td></tr> <tr> <td>1</td><td>0</td><td>PCI</td></tr> <tr> <td>1</td><td>1</td><td>LPC</td></tr> <tr> <td>0</td><td>0</td><td>Reserved</td></tr> </tbody> </table>	Bit11 (GNT0#)	Bit 10 (SPI_CS1#)	Boot BIOS Destination	0	1	SPI	1	0	PCI	1	1	LPC	0	0	Reserved
Bit11 (GNT0#)	Bit 10 (SPI_CS1#)	Boot BIOS Destination															
0	1	SPI															
1	0	PCI															
1	1	LPC															
0	0	Reserved															
SPI_CS1# / GPIO58	Boot BIOS Destination Selection 0, Rising Edge of CLPWROK	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <table border="1"> <thead> <tr> <th>Bit11 (GNT0#)</th><th>Bit 10 (SPI_CS1#)</th><th>Boot BIOS Destination</th></tr> </thead> <tbody> <tr> <td>0</td><td>1</td><td>SPI</td></tr> <tr> <td>1</td><td>0</td><td>PCI</td></tr> <tr> <td>1</td><td>1</td><td>LPC</td></tr> <tr> <td>0</td><td>0</td><td>Reserved</td></tr> </tbody> </table>	Bit11 (GNT0#)	Bit 10 (SPI_CS1#)	Boot BIOS Destination	0	1	SPI	1	0	PCI	1	1	LPC	0	0	Reserved
Bit11 (GNT0#)	Bit 10 (SPI_CS1#)	Boot BIOS Destination															
0	1	SPI															
1	0	PCI															
1	1	LPC															
0	0	Reserved															
SATALED#	PCI Express Lane Reversal (Lanes 1-4). Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)															
SPKR	No Reboot, Rising Edge of PWROK.	Sampled high: this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h: bit 5).															
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.															
GPIO33 / HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK. (Mobile Only)	Sampled low: the Flash Descriptor Security will be overridden. Sampled high: the security measures will be in effect. This strap should only be enabled in manufacturing environments.															
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be high for mobile applications.															
SPI_MOSI (Mobile Only)	Integrated TPM Enable. Rising Edge of CLPWROK.	Sampled low: the Integrated TPM will be disabled. Sampled high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. NOTE: This signal is required to be floating or pulled low for desktop applications.															

## ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.2.3

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRLPVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT0#, GNT[3:1]# / GPIO[55, 53, 51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LAD[3:0]# / FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ0	PULL-UP 20K
LDRQ1 / GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1# / GPIO58 (Desktop Only) / CLGPIO6 (Digital Office Only)	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP3	PULL-UP 20K
USB[11:0] [P,N]	PULL-DOWN 15K

## PCIE Routing

LANE1	
LANE2	MiniCard WLAN
LANE3	LAN

## USB Table

USB Pair	Device
0	USB0 (I/O Board)
1	USB1 (I/O Board 17")
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

## Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 355648 Rev.2.3

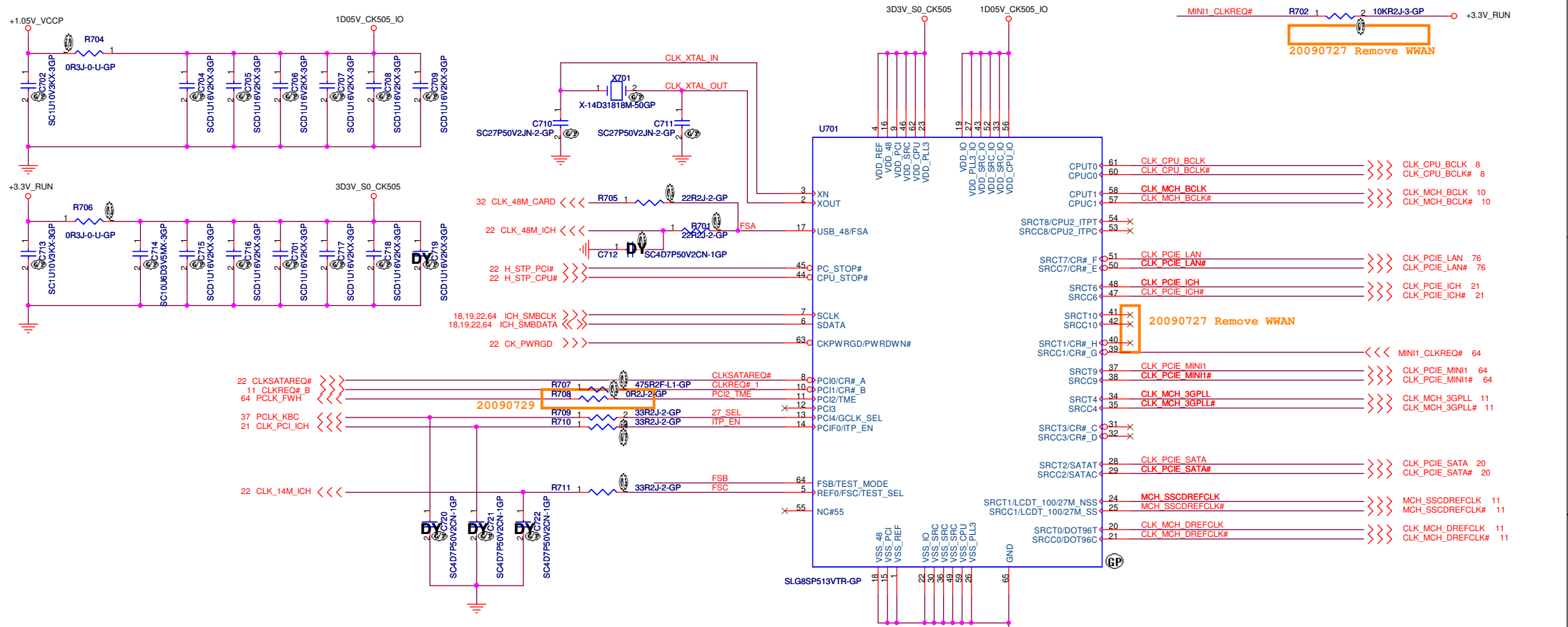
Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2). 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 etc. 1 = Normal operation (default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) 1 = Disable (Default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disable (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE	0 = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) 1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA (Note4)	SDVO Present	0 = No SDVO/HDMI/DP interface disabled (default) 1 = SDVO/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Note4)	Digital Display Present	0 = Digital display (HDMI/DP) device absent (default) 1 = Digital display (HDMI/DP) Device Present
CFG4:3 CFG8 CFG11 CFG14 CFG15 CFG17 CFG18	Reserved	

### NOTE:

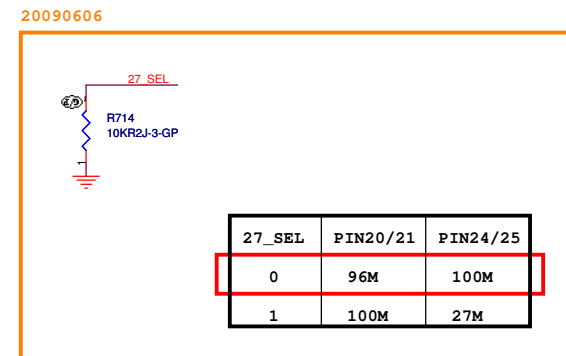
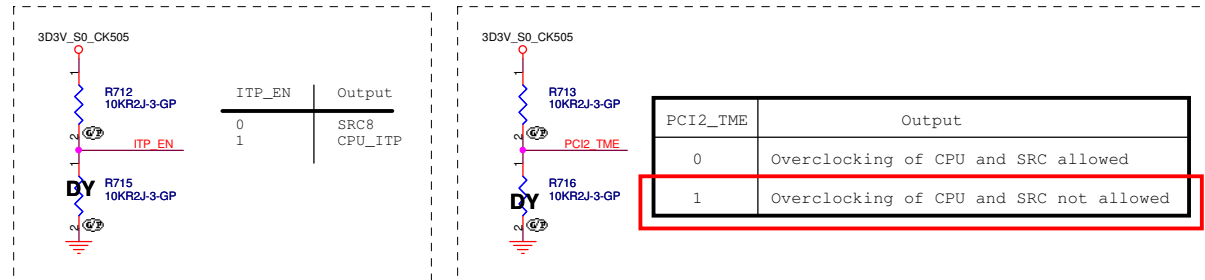
- All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
- DDPC\_CTRL\_DATA & SDVO\_CTRL\_DATA straps should both be high to enable Display Port.

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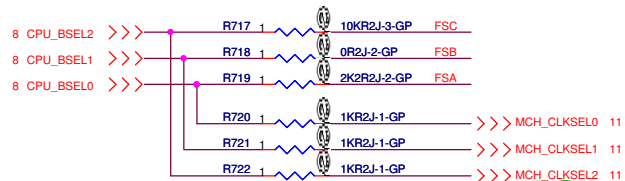
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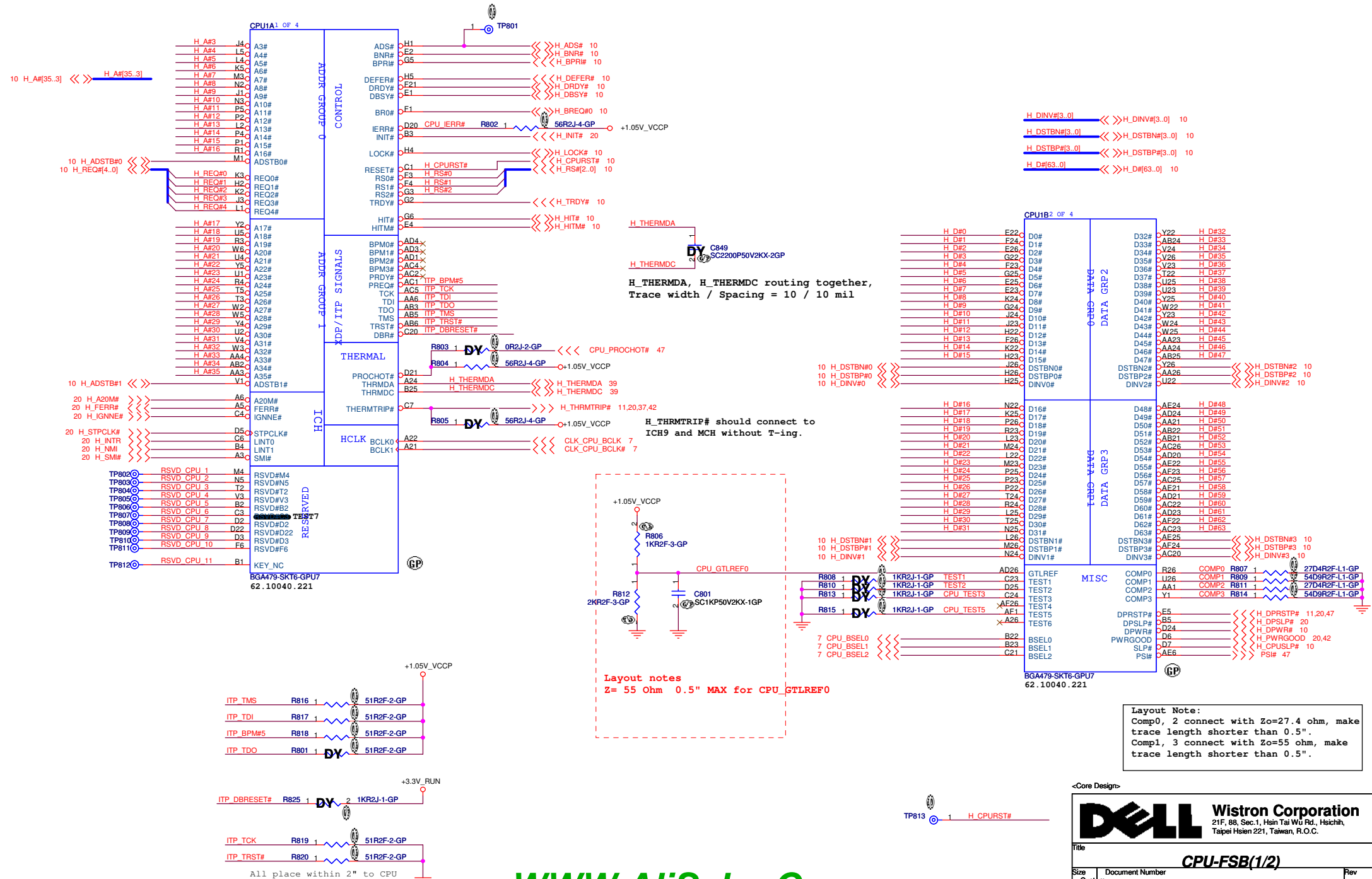


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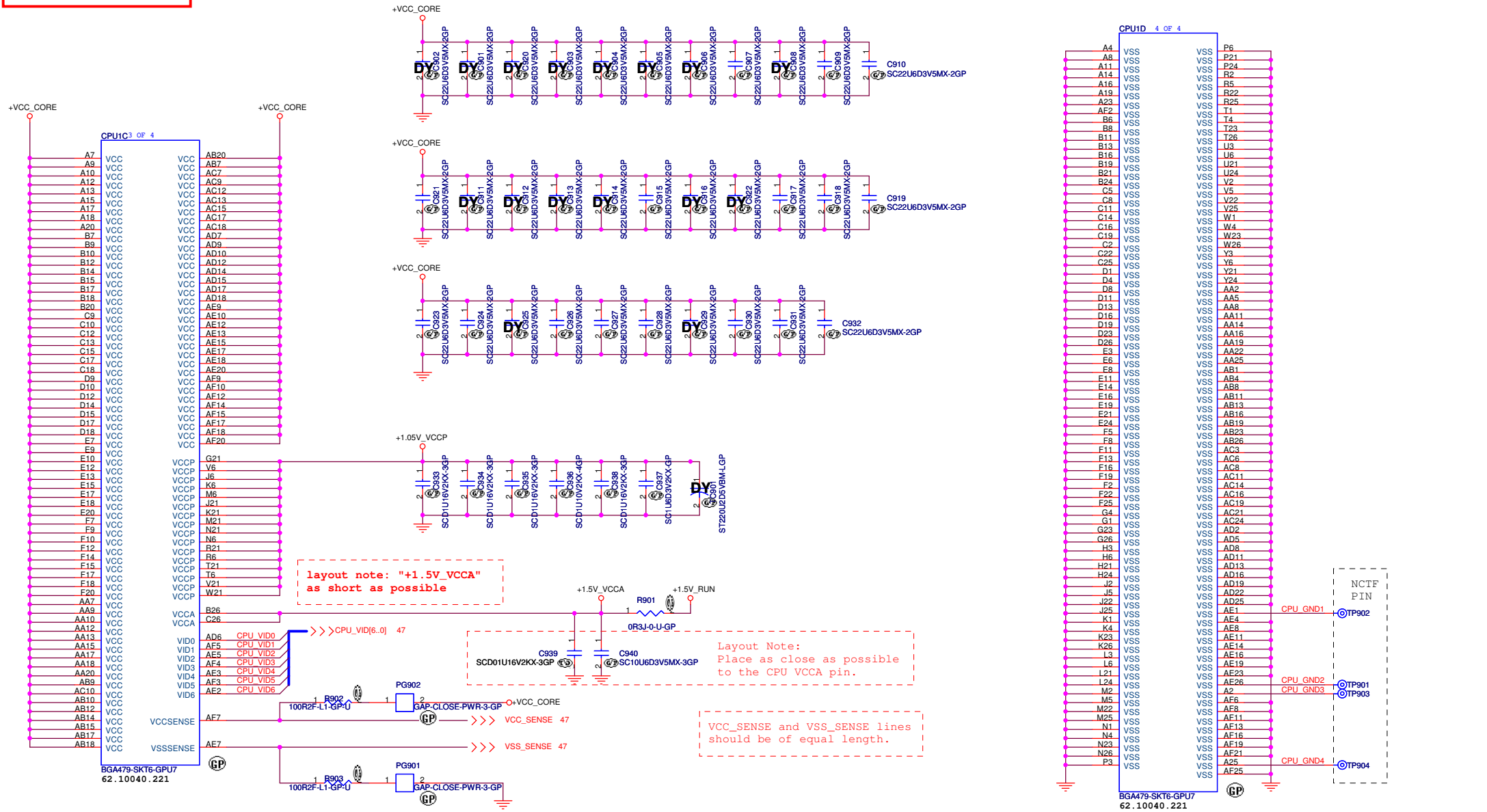


SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

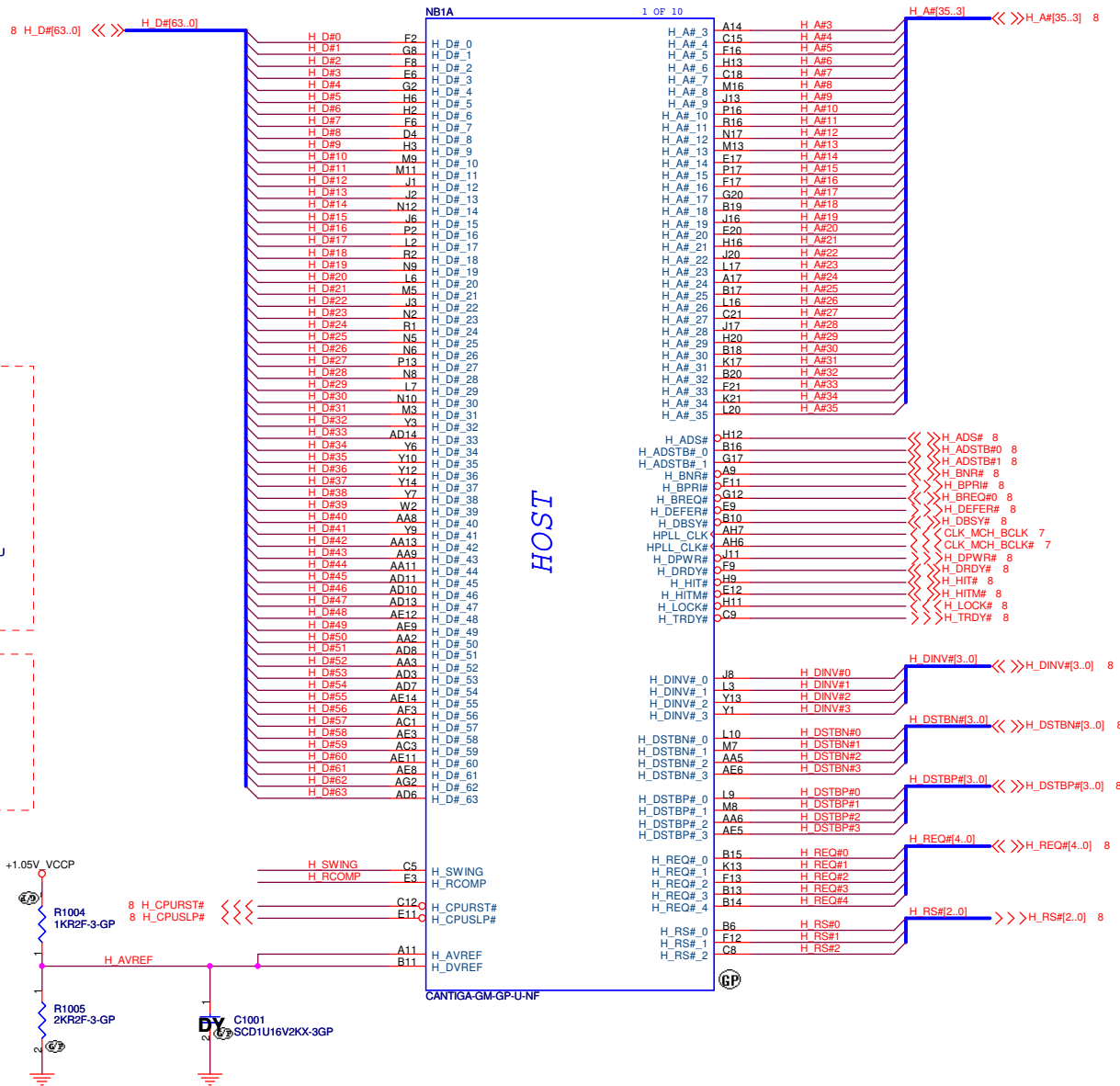
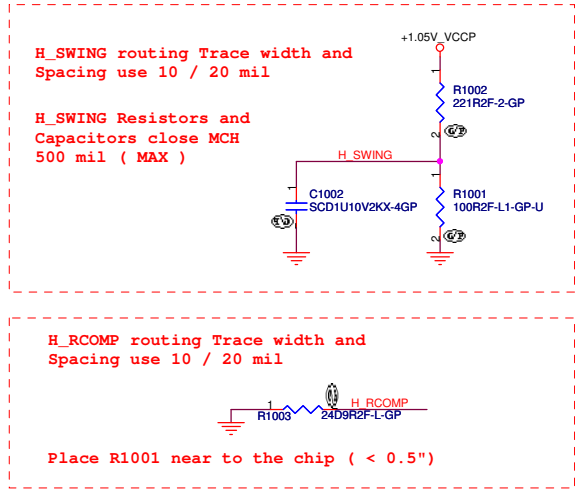






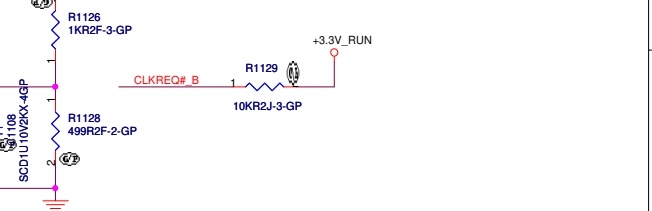
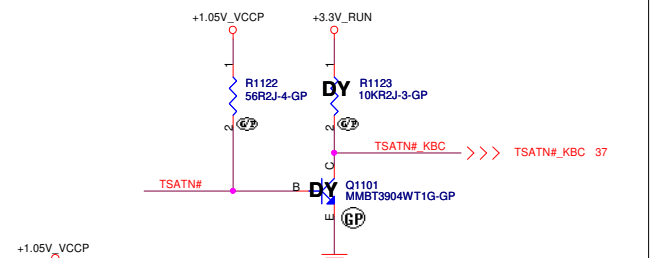
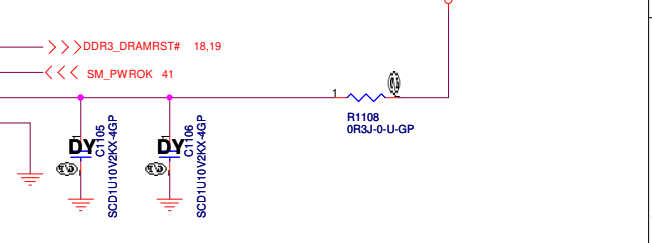
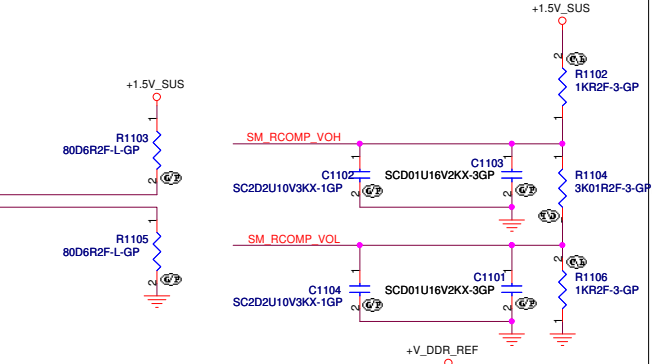
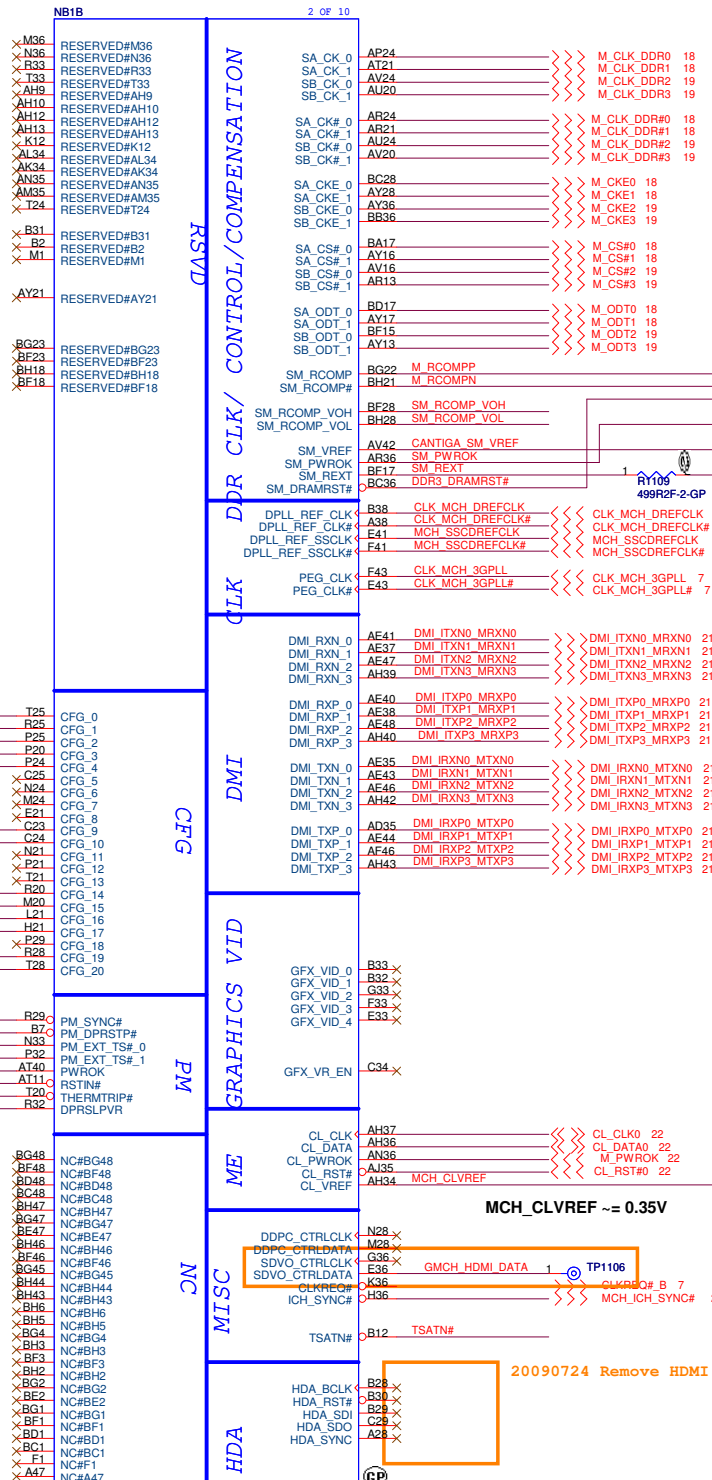
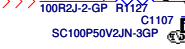
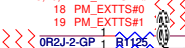
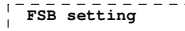
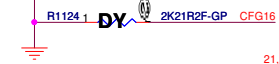
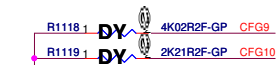
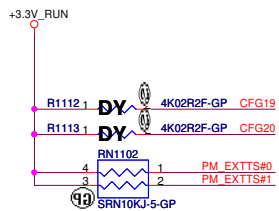


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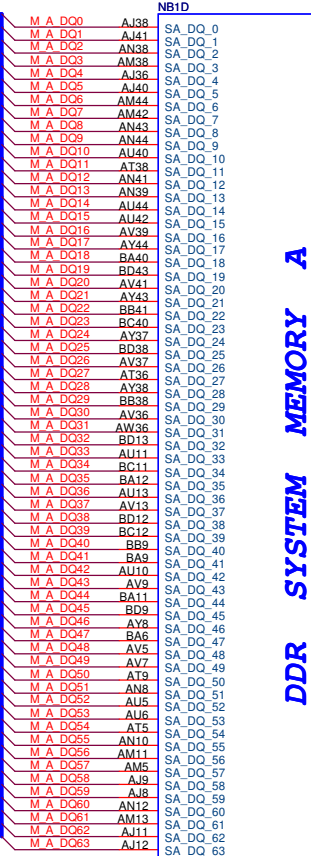


\* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 <span style="color: red;">★</span>
CFG 6	ITPM enable	ITPM disable <span style="color: red;">★</span>
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality <span style="color: red;">★</span>
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in order <span style="color: red;">★</span>
CFG 10	PCIE loopback enable	PCIE loopback disable <span style="color: red;">★</span>
CFG 12	ALLZ mode enable	ALLZ mode disable <span style="color: red;">★</span>
CFG 13	XOR mode enable	XOR mode disable <span style="color: red;">★</span>
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable <span style="color: red;">★</span>
CFG 19	Normal operation <span style="color: red;">★</span>	Reverse DMI lanes
DMI Lane Reserved		PCIE and SDVO are operating simultaneously via the PEG port
CFG 20		
SDVO concurrent with PCIE	Only PCIE or SDVO is operational <span style="color: red;">★</span>	
SDVO_CTRLDATA	SDVO interface disable <span style="color: red;">★</span>	SDVO interface enable
L_DDC_DATA	LFP disable <span style="color: red;">★</span>	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled <span style="color: red;">★</span>	SDVO/iHDMI/DP interface enabled

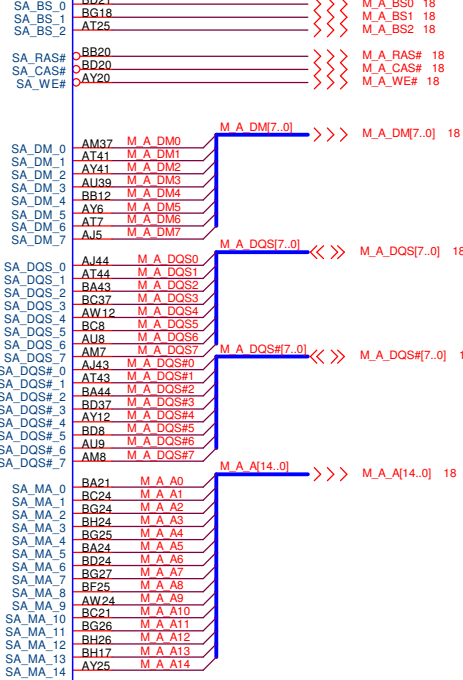


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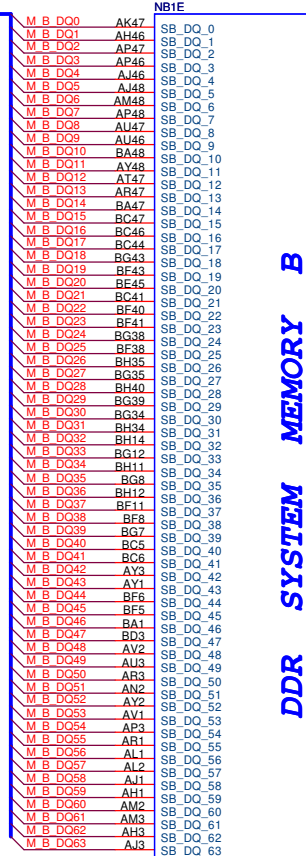


CANTIGA-GM-GP-U-NF

4 OF 10

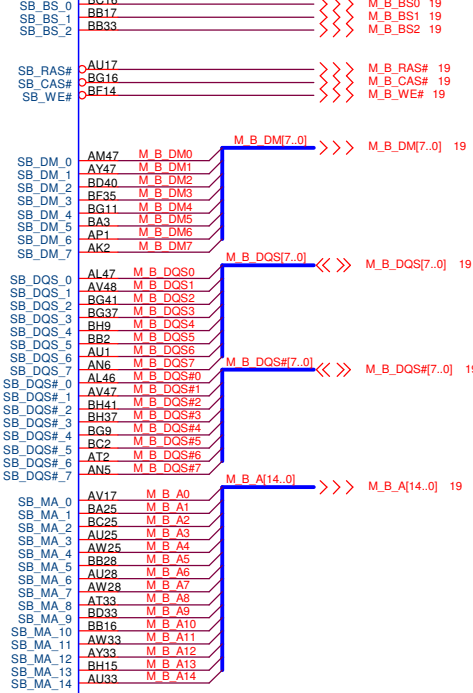


19 M\_B\_DQ[63..0] <<>> M\_B\_DQ[63..0]



CANTIGA-GM-GP-U-NF

5 OF 10



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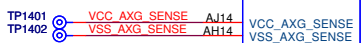
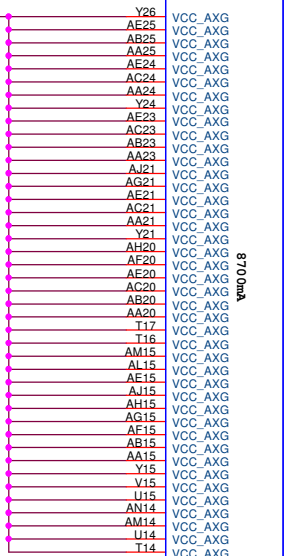
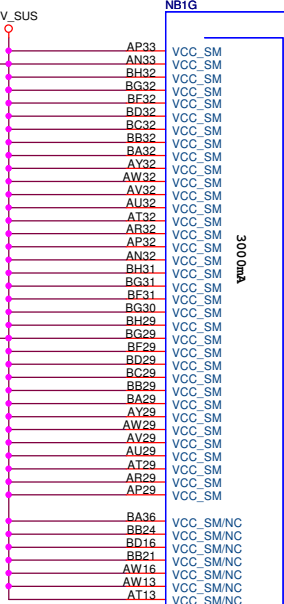
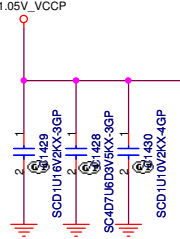
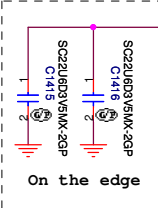
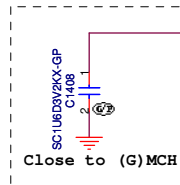
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**Cantiga-DDR(3/6)**

Size Custom Document Number **DJ2 Montevina UMA** Rev **X00**

Date: Thursday, August 20, 2009 Sheet 12 of 88







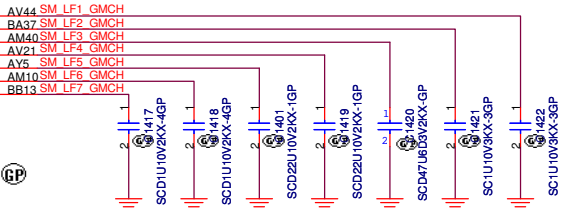
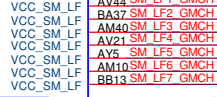
CANTIGA-GM-GP-U-NF

VCC SM POWER

VCC GFX NCTF

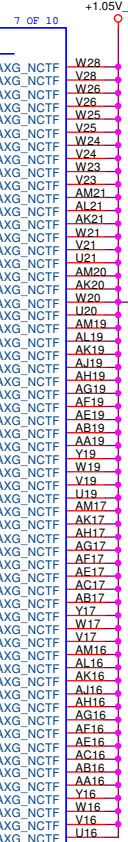
VCC GFX

VCC SM LF

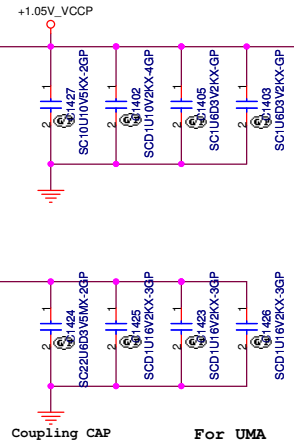
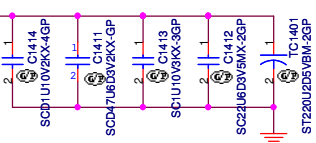


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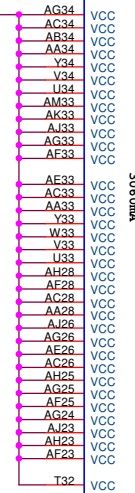
+1.05V\_VCCP



Coupling CAP



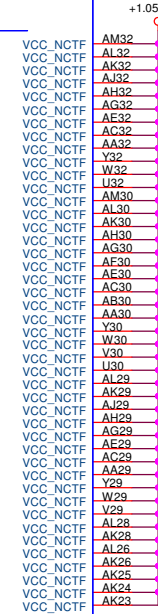
For UMA



VCC CORE

POWER

VCC NCTF



+1.05V\_VCCP



CANTIGA-GM-GP-U-NF

Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

<Core Design>

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Title  
**Cantiga-Power(5/6)**

Size  
Custom

Document Number  
**DJ2 Montevina UMA**

Rev  
**X00**


Date: Wednesday, July 29, 2009

Sheet 14 of 88



(Blanking)

<Core Design>



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Size  
A3

Document Number  
**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009

**Reserved**


Rev  
**X00**

Sheet 16 of 88



(Blanking)

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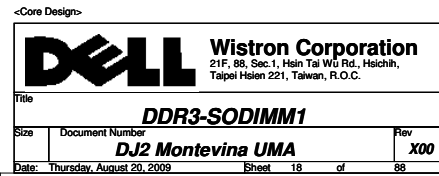
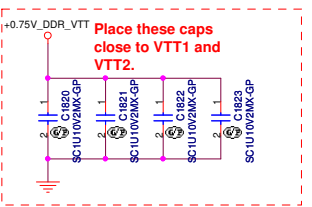
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

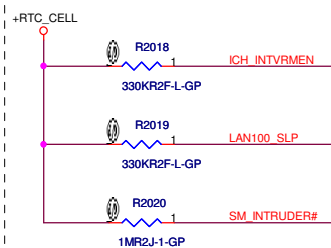
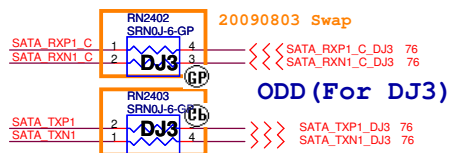
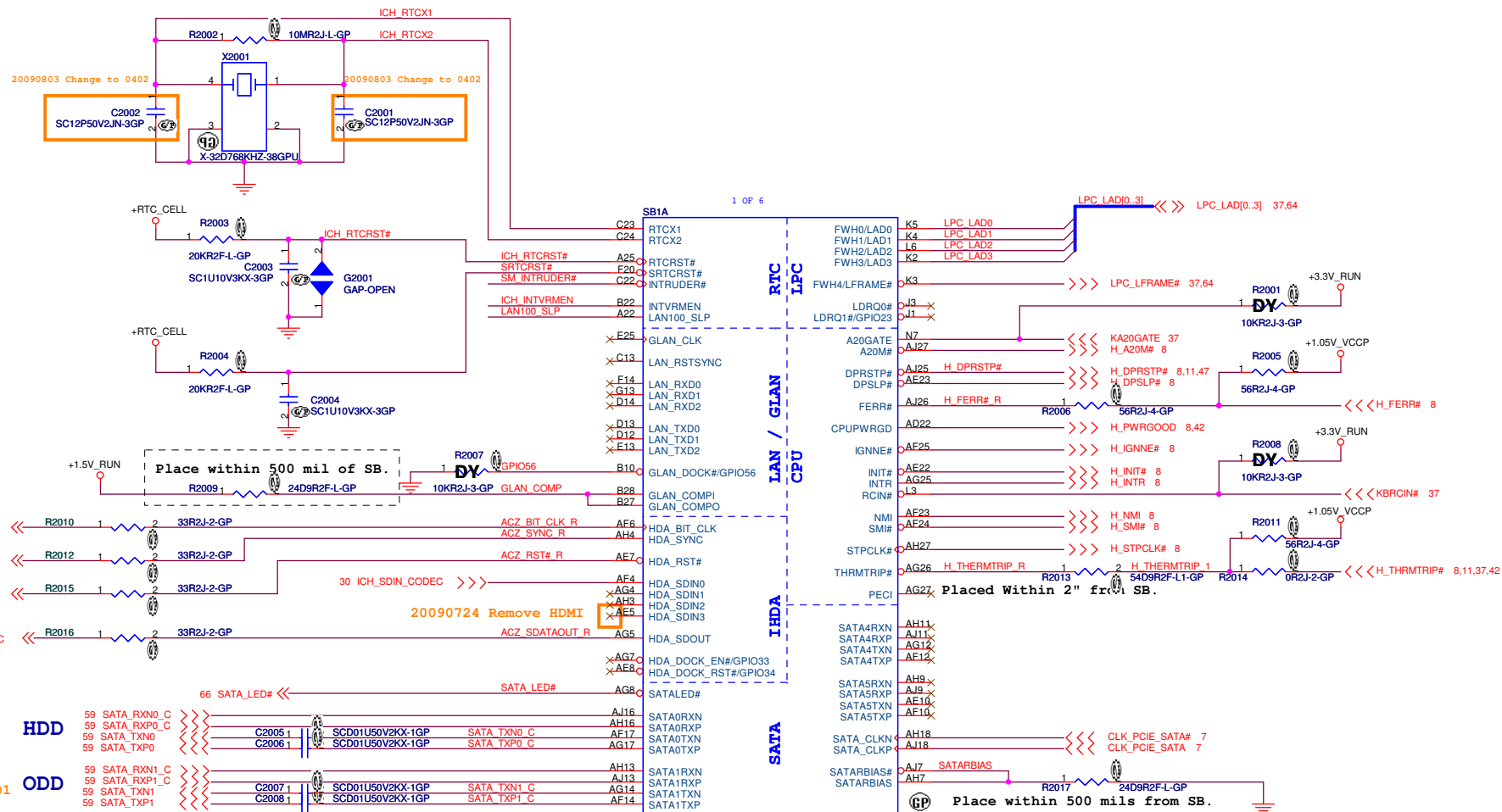
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Size A3	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
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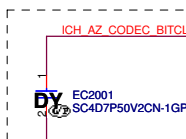
Date: Wednesday, July 29, 2009	Sheet 17 of 88
--------------------------------	----------------



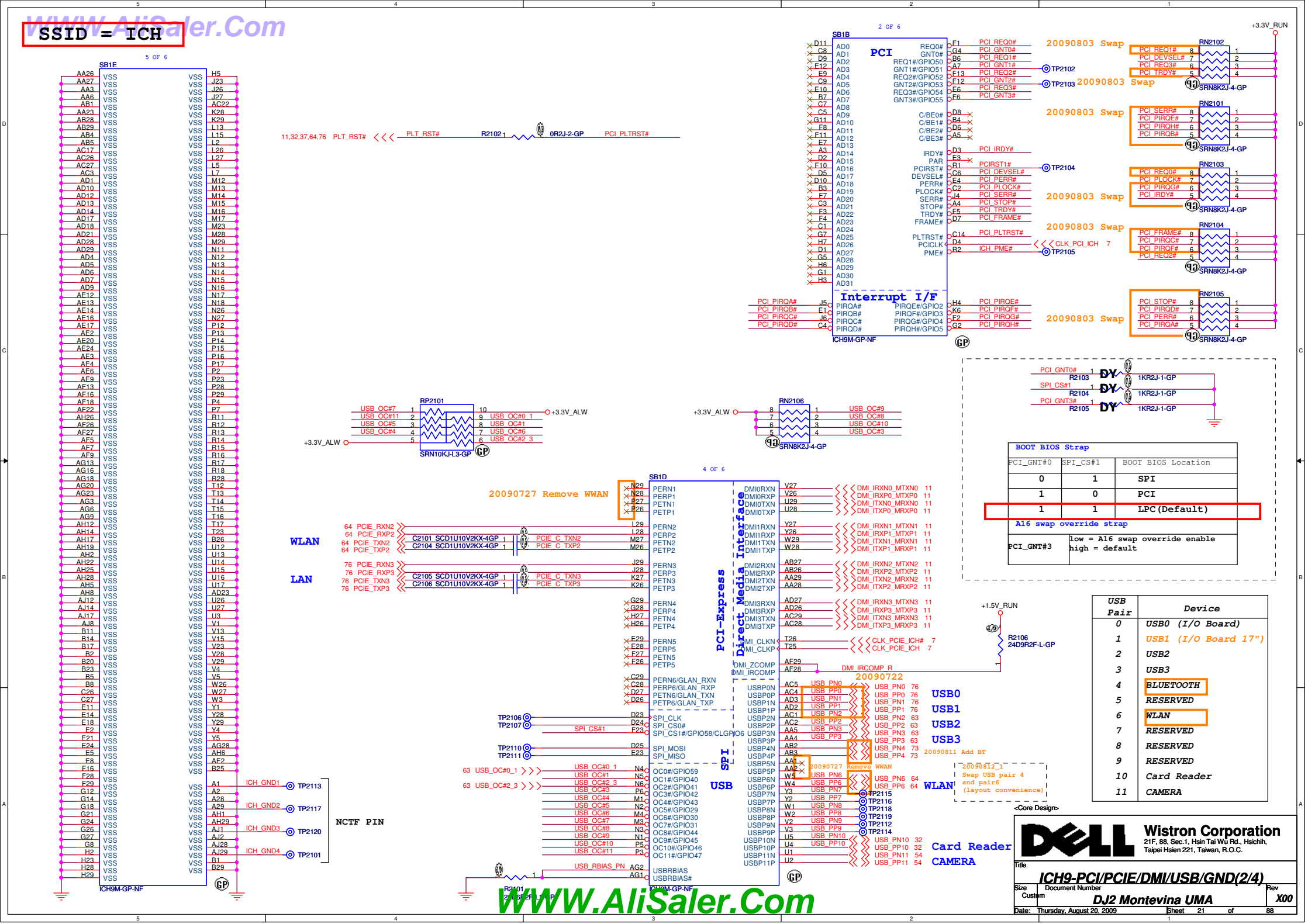


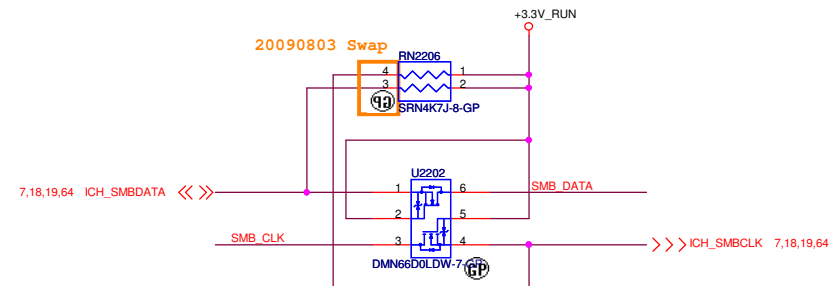
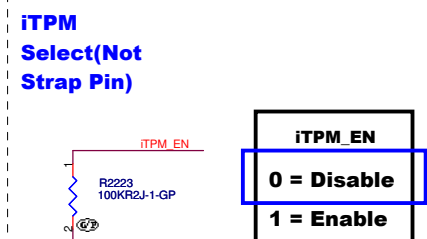
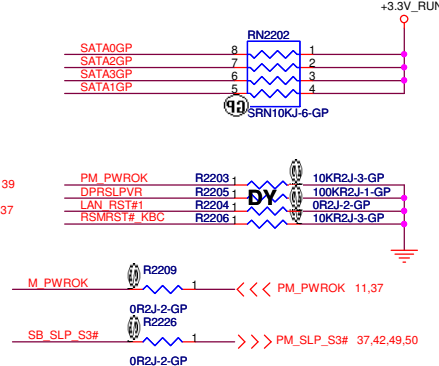
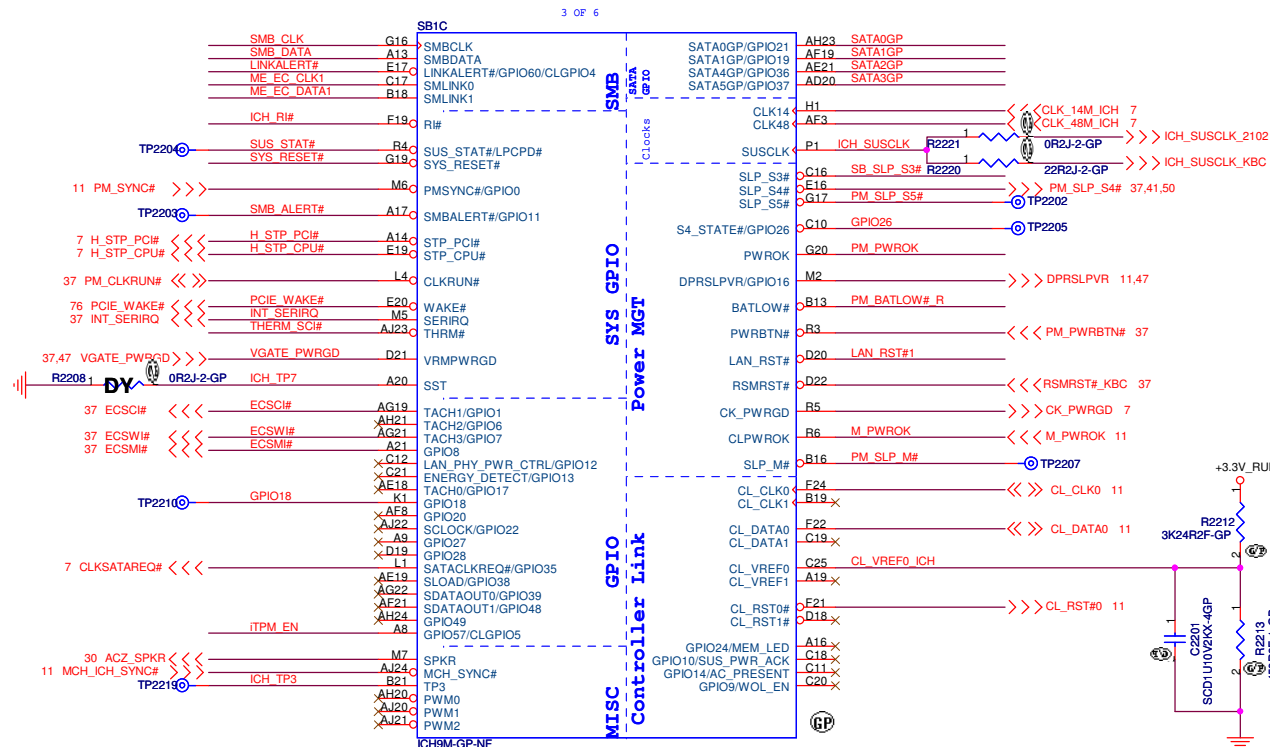
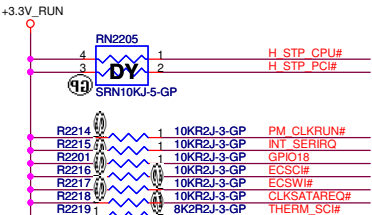


integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



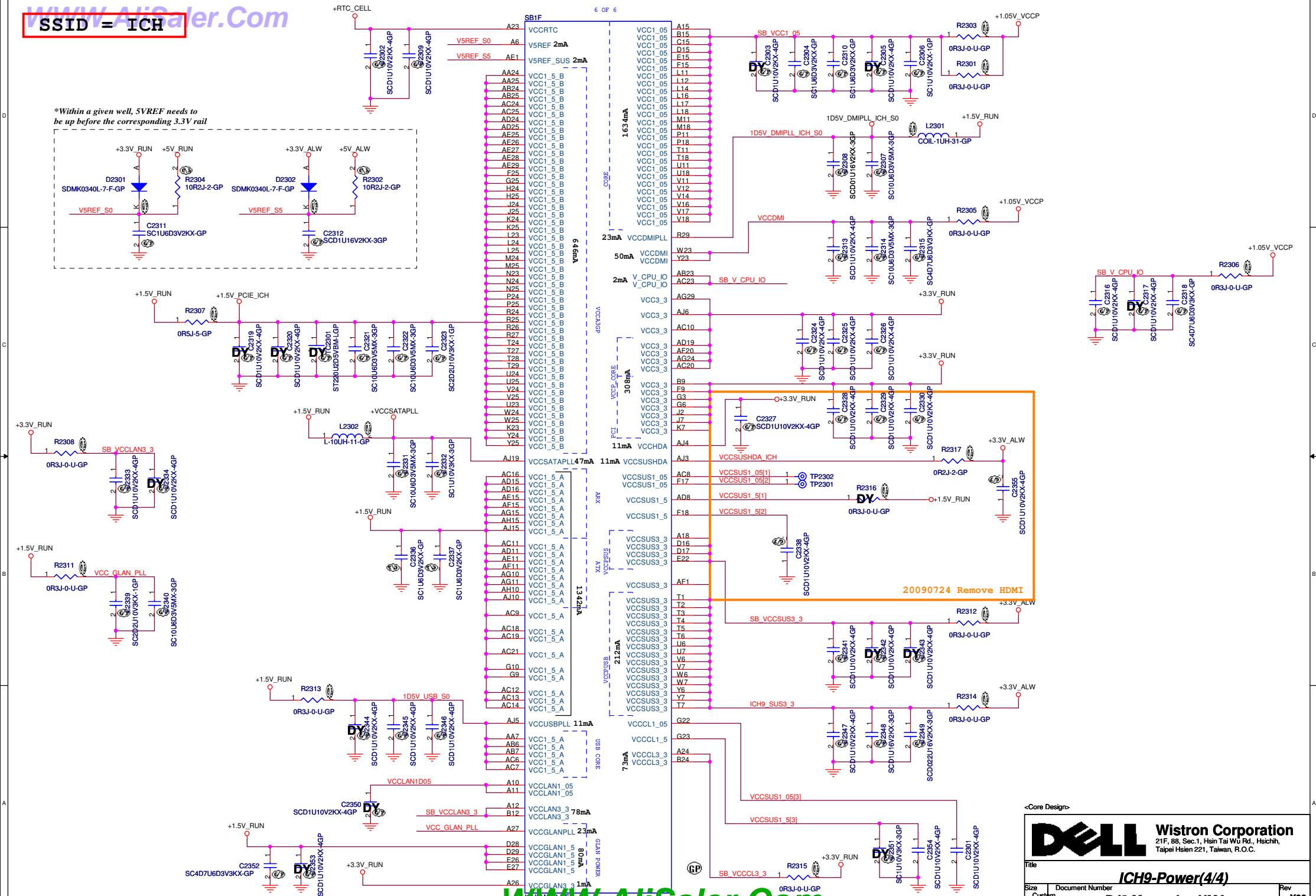
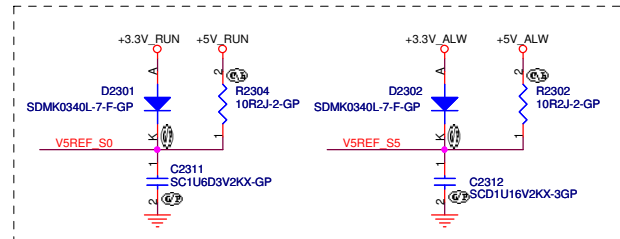
## 20090724 Remove HDMI







*\*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail*



**<Core Design>**



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<b>ICH9-Power(4/4)</b>			
Size	Document Number		Rev
Custom	<b>DJ2 Montevina UMA</b>		<b>X00</b>
Date:	Wednesday, July 29, 2009	Sheet 23 of	88

(Blanking)

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DELL

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Title

Size  
Custom

Document Number  
**DJ2 Montevina UMA**

Rev  
**X00**


Date: Wednesday, July 29, 2009

Sheet 24 of 88



(Blanking)

<Core Design>



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Size

Document Number

Rev

Custom

DJ2 Montevina UMA

X00

Date: Wednesday, July 29, 2009

Sheet 25 of 88

(Blanking)

<Core Design>

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Size  
Custom

Document Number  
**DJ2 Montevina UMA**


Rev  
**X00**

Date: Wednesday, July 29, 2009

Sheet 26 of 88

(Blanking)

<Core Design>



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Title

Size

Document Number

Rev

Custom

DJ2 Montevina UMA

X00

Date: Wednesday, July 29, 2009

Sheet 27 of 88

(Blanking)

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DELL

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Reserved

Size

Document Number

Rev

Custom

DJ2 Montevina UMA


X00

Date: Wednesday, July 29, 2009

Sheet 28 of 88

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**


Size	Document Number	Rev
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>

Date: Wednesday, July 29, 2009	Sheet 29 of 88
--------------------------------	----------------



(Blanking)

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Title

Size

A3

Document Number

DJ2 Montevina UMA

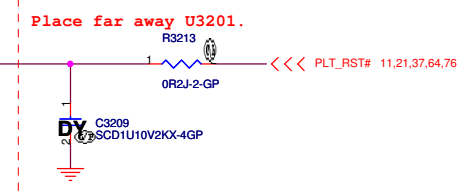
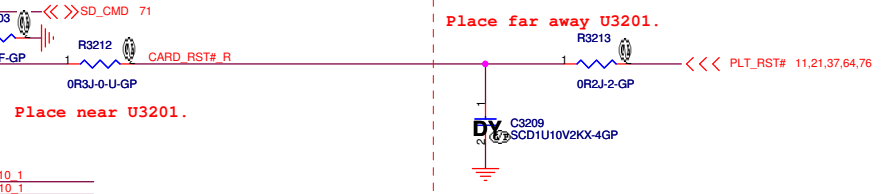
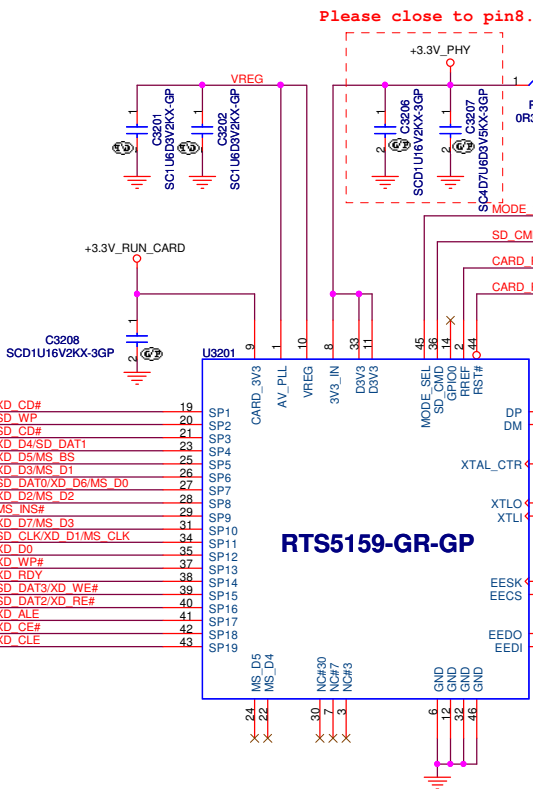
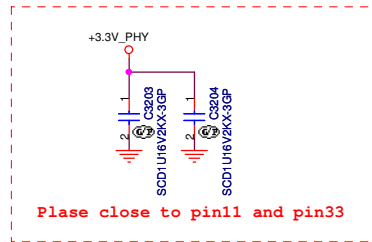
Rev

X00

Date: Wednesday, July 29, 2009

Sheet 31 of 88

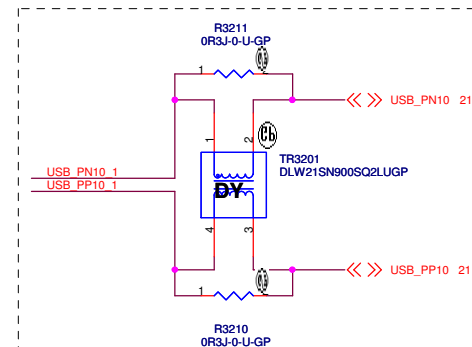
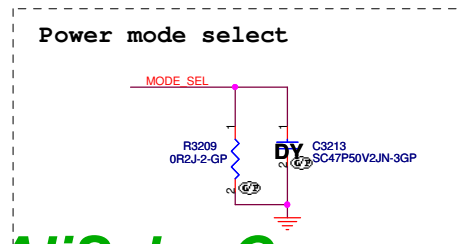
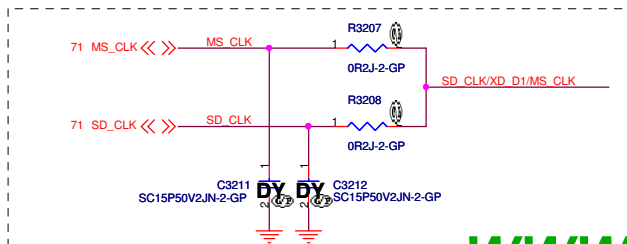
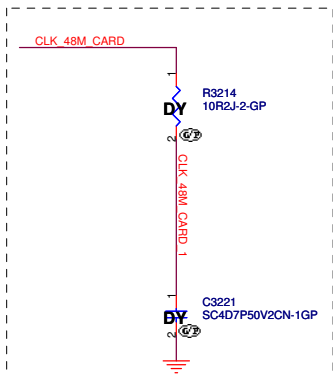
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71 XD\_CD#  
71 SD\_WP  
71 SD\_CD#  
71 XD\_D4/SD\_DAT1  
71 XD\_D5/MS\_BS  
71 XD\_D3/MS\_D1  
71 SD\_DAT0/XD\_D6/MS\_D0  
71 XD\_D2/MS\_D2  
71 MS\_INS#  
71 XD\_D7/MS\_D3  
71 SD\_CLK/XD\_D1/MS\_CLK  
71 XD\_D0  
71 XD\_WP#  
71 XD\_RDY#  
71 SD\_DAT3/XD\_WE#  
71 SD\_DAT2/XD\_RE#  
71 XD\_ALE  
71 XD\_CE#  
71 XD\_CLE

XD\_CD#  
SD\_WP  
SD\_CD#  
XD\_D4/SD\_DAT1  
XD\_D5/MS\_BS  
XD\_D3/MS\_D1  
SD\_DAT0/XD\_D6/MS\_D0  
XD\_D2/MS\_D2  
MS\_INS#  
XD\_D7/MS\_D3  
SD\_CLK/XD\_D1/MS\_CLK  
XD\_D0  
XD\_WP#  
XD\_RDY#  
SD\_DAT3/XD\_WE#  
SD\_DAT2/XD\_RE#  
XD\_ALE  
XD\_CE#  
XD\_CLE


RTS5159-GR-GP





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Title

Size  
A3

Document Number  
**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009


**Reserved**

Rev  
**X00**

Sheet 33 of 88

(Blanking)

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**Reserved**

Size	Document Number	Rev
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>

Date: Wednesday, July 29, 2009	Sheet 34 of 88
--------------------------------	----------------

(Blanking)

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(Reserved)

Size	Document Number	Rev
	DJ2 Montevina UMA	X00

Date: Wednesday, July 29, 2009	Sheet 35 of 88
--------------------------------	----------------

(Blanking)

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Title

Size  
A3

Document Number  
**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009

**Reserved**


Rev  
**X00**

Sheet 36 of 88



(Blanking)

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**Reserved**


Size A3	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
------------	---------------------------------------------	-------------------

Date: Wednesday, July 29, 2009	Sheet 38 of 88
--------------------------------	----------------



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Title

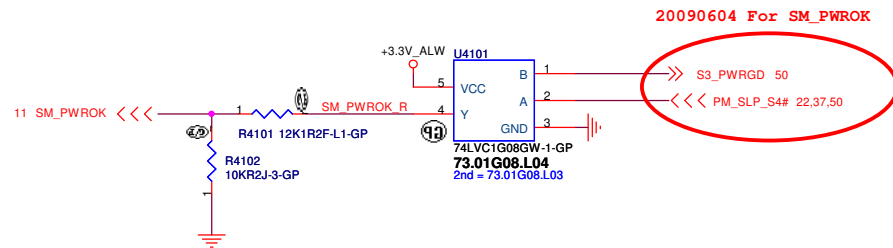
**Reserved**

Size A3	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
------------	---------------------------------------------	-------------------

Date: Wednesday, July 29, 2009	Sheet 40 of 88
--------------------------------	----------------



SSID = Reset.Suspend



<Core Design>



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Title

**Power On Logic**

Size  
A3

Document Number

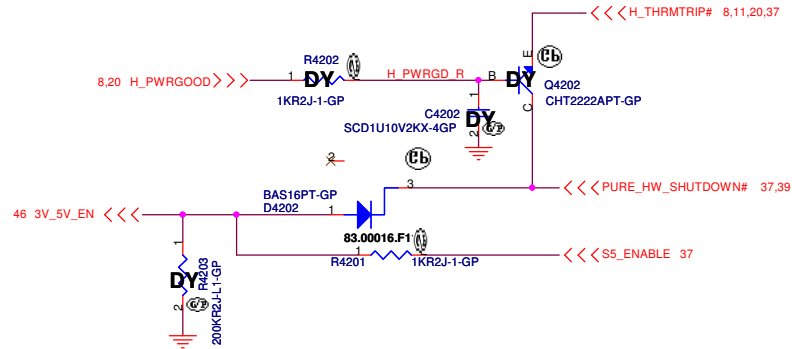
**DJ2 Montevina UMA**

Rev

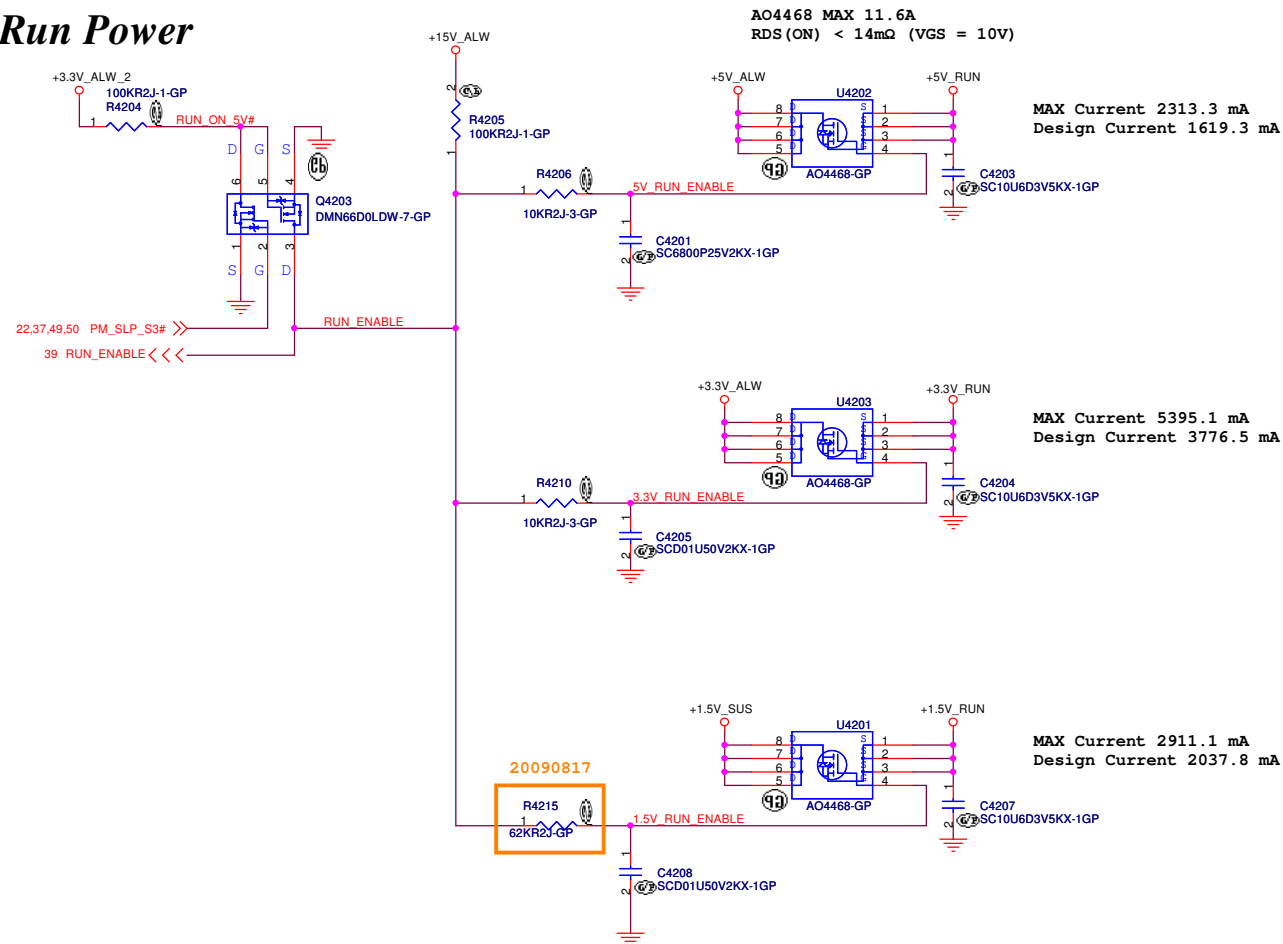
**X00**

Date: Thursday, August 20, 2009

Sheet 41 of 88




## Run Power



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<Core Design>



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Size  
A3

Document Number  
**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009


**Reserved**

Rev  
**X00**

Sheet 43 of 88

(Blanking)

<Core Design>



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Size

A3

Document Number

DJ2 Montevina UMA

Rev


X00

Date: Wednesday, July 29, 2009

Sheet 44 of 88

(Blanking)

<Core Design>



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Title

Size

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Document Number

DJ2 Montevina UMA

Date: Wednesday, July 29, 2009

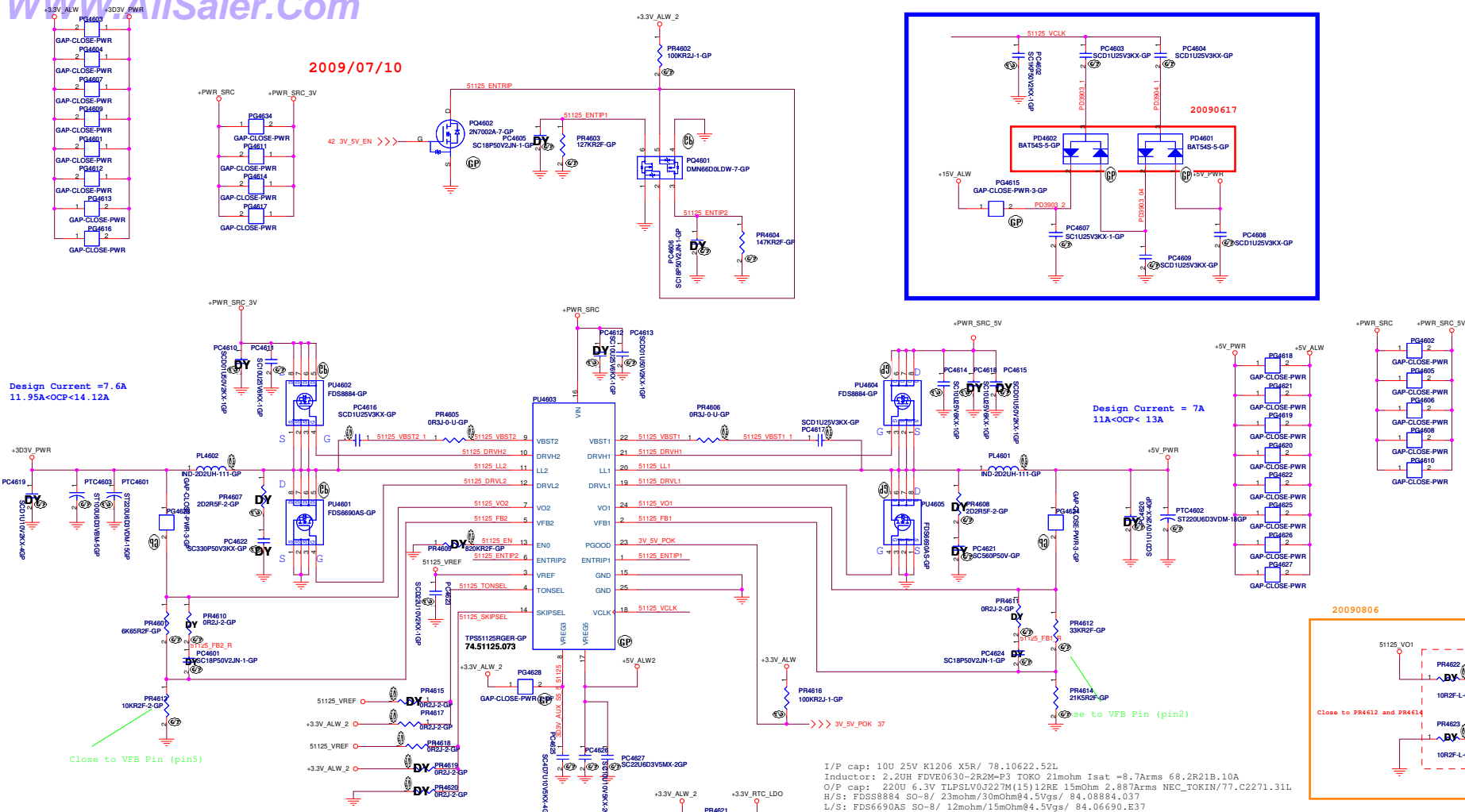
Sheet 45 of 88

Rev

X00

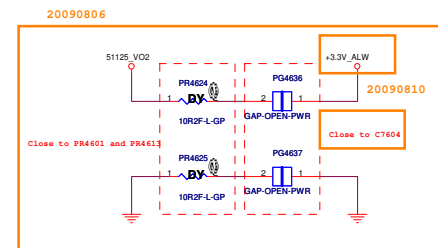
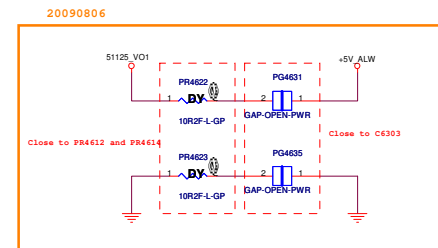
**Reserved**

2009/07/10



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 2.2UH FDVE0630-2R2M-P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A  
O/P cap: 220U 6.3V TPLSV0J227M(25) 25mohm 2.236Arms NEC\_TOKIN/77.C2271.00L  
O/P cap: 100U 6.3V TEPSLB2J107M(45) 8R 45mohm 1.374Arms NEC\_TOKIN/77.C1071.081  
H/S: FDS8884 SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037  
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz	EN0	Open	820kΩ to GND	GND
VREG5	365kHz	460kHz	Operating Mode	enable both LDs, VCLK on and ready to turn on switcher channels	enable both LDs, VCLK off and ready to turn on switcher channels	disable all circuit




<Core Design>



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<Core Design>



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Title

**CPU VCORE POWER(2/2)**

Size	Document Number	Rev
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>

Date: Wednesday, July 29, 2009	Sheet 48 of 88
--------------------------------	----------------



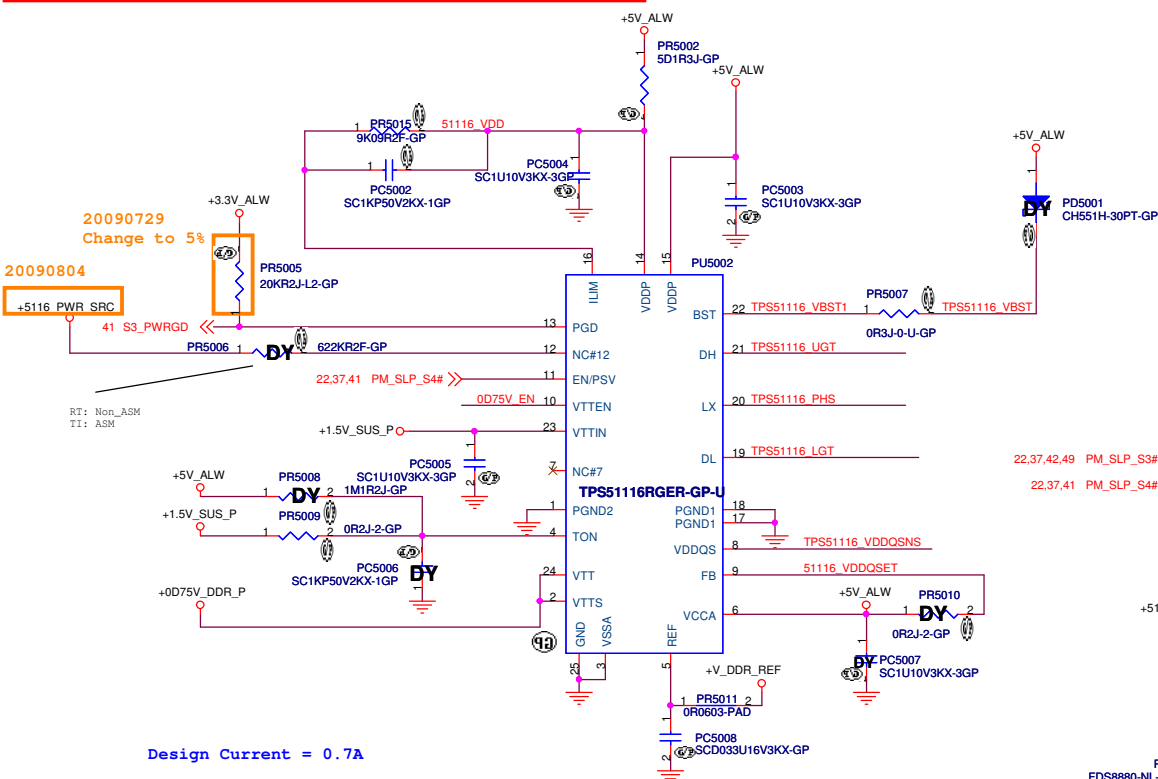
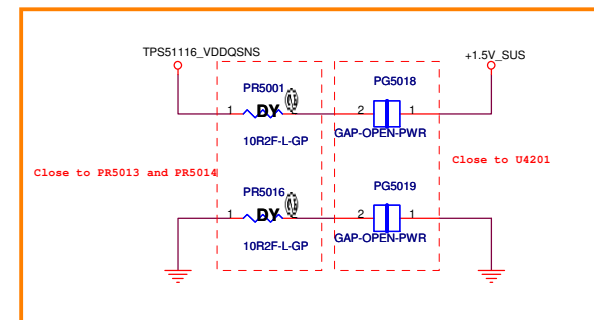
2009/07/22



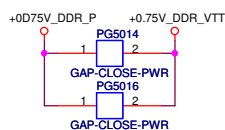
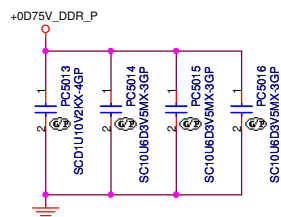
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Title			
<b>TPS51218 +1.05V VCCP</b>			
Size	Document Number	Rev	
Custom	<b>DJ2 Montevina UMA</b>	<b>X00</b>	
Date:	Thursday, August 20, 2009	Sheet	49 of 88

```
SSID = PWR.Plane.Regulator_1p5v0p75v
```

20090806



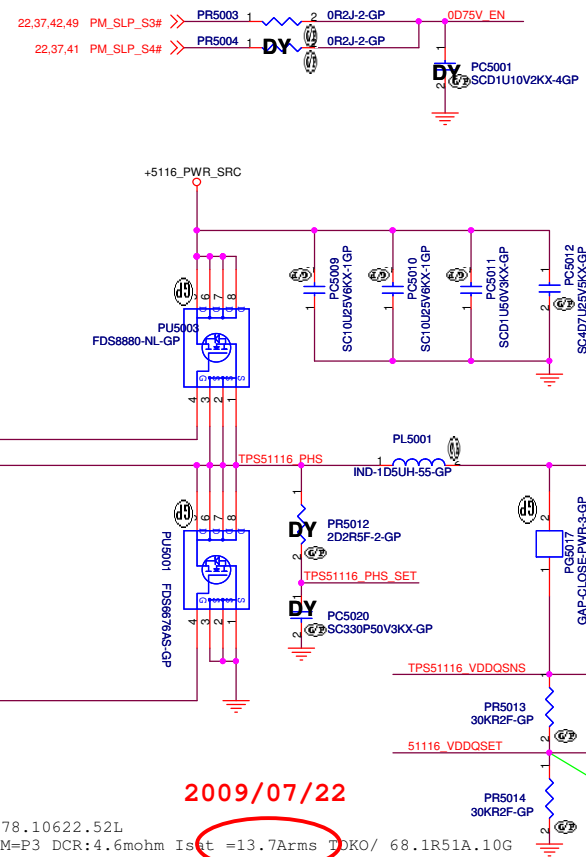
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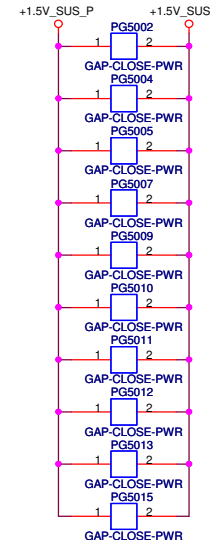
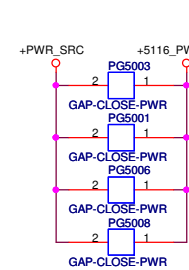
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.5UH FVDE1040-1R5M=P3 DCR:4.6mohm Isat =13.7Arms TDKO/ 68.1R51A.10G  
O/P cap: 330U 2.5V EEFCCO5310R 150mOhm 2.7Arms PANASONIC/ 79.3371V.20L  
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037  
L/S: FDS6676AS/ 5.9mOhm/7.25mohm@4.5Vgs/ 84.06676.A37  
Switching freq-->400KHz



Design Current = 9.82A  
15.43A < OCP < 18.24A



2009/07/22

Close to VFB Pin (pin5)

### <Core Design>




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Title			
<b>TPS51116 +1.5V SUS</b>			
Size	Document Number	Rev	
Custom	<b>DJ2 Montevina UMA</b>	<b>X00</b>	
Date: Thursday, August 20, 2009		Sheet 50 of	88

(Blanking)

<Core Design>



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.


Title

(Reserved)

Size A3	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
Date: Wednesday, July 29, 2009	Sheet 51 of 88	

(Blanking)

<Core Design>



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Title

Size  
A3

Document Number  
**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009


**Reserved**

Rev  
**X00**

Sheet 52 of 88

(Blanking)

<Core Design>



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Title

Size

A3

Document Number

DJ2 Montevina UMA

Rev

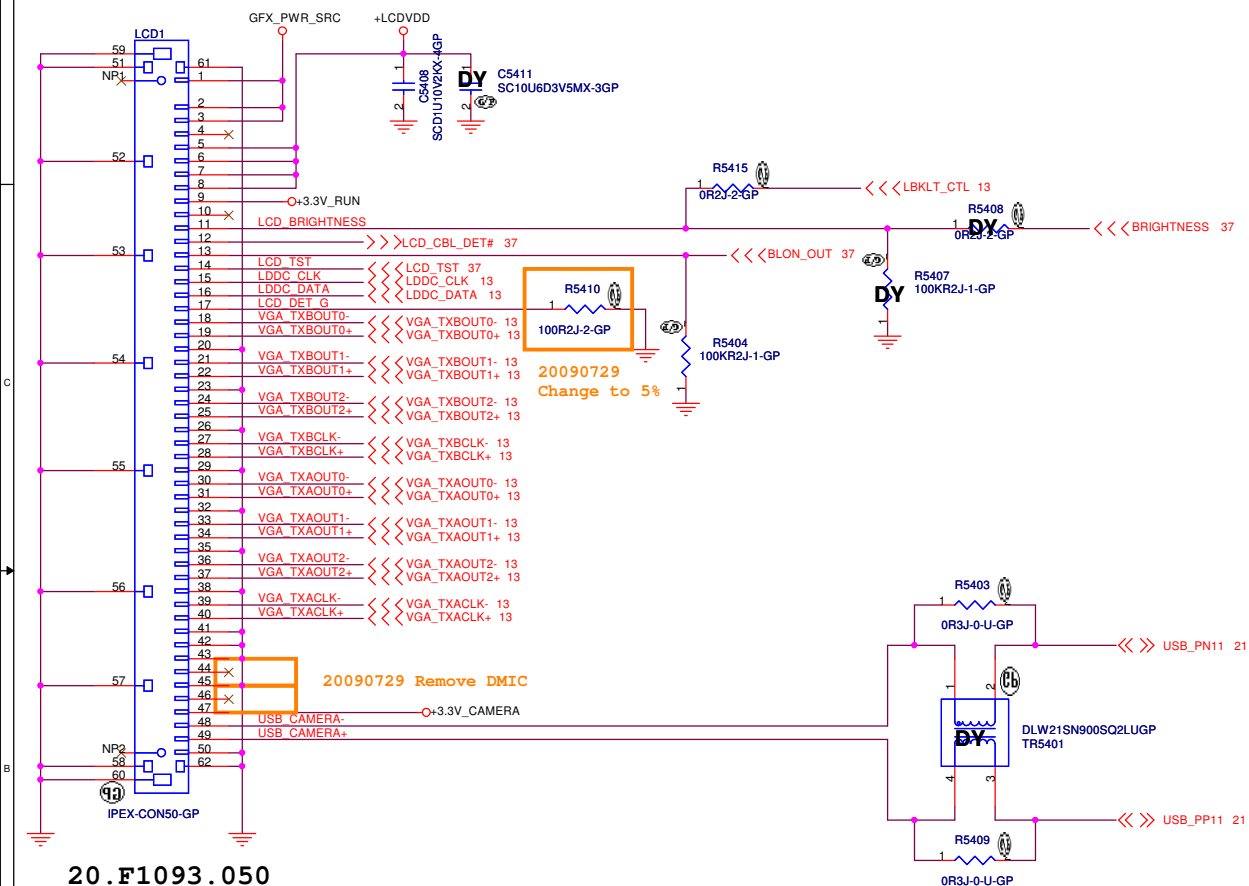
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Date: Wednesday, July 29, 2009

Sheet 53 of 88

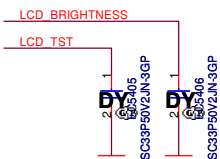
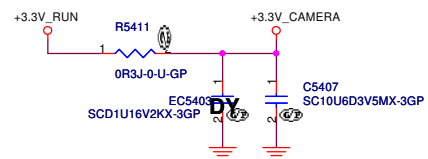
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## LVDS CONNECTOR



20090729 Remove DMIC

### Camera Power

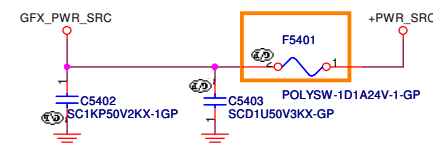


For EMT request

SSID = Inverter

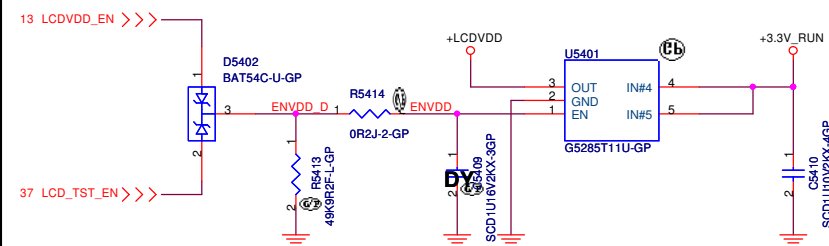
## INVERTER POWER

20090817



SSID = VIDEO

## LCD POWER



<Core Design>

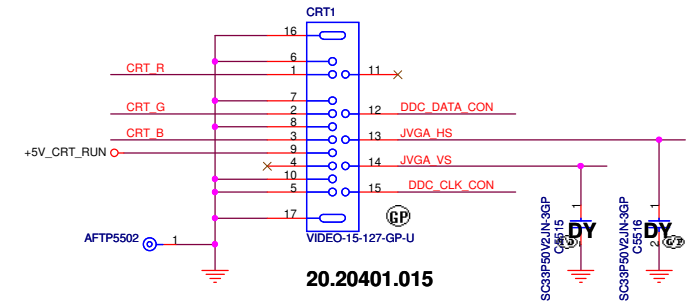
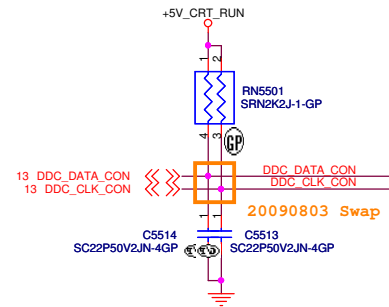
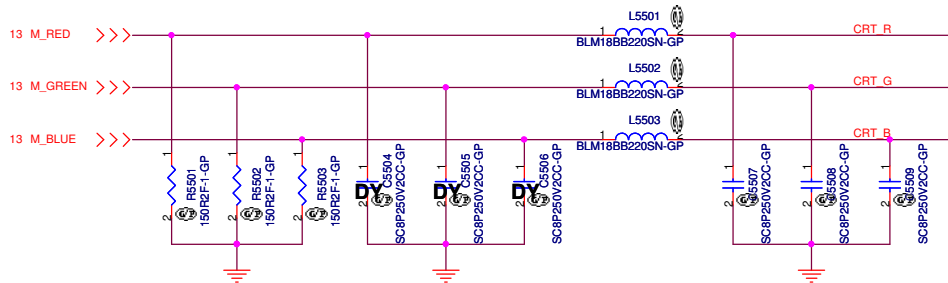


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Title			LCD/Inverter Connector	
Size	Document Number	Rev		
A3	DJ2 Montevina UMA	X00		
Date:	Thursday, August 20, 2009	Sheet	54	of 88

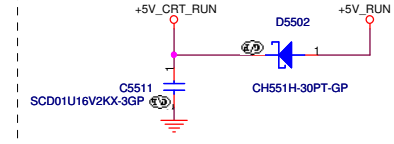
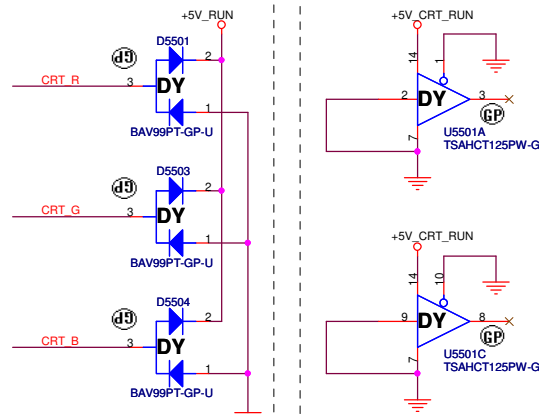
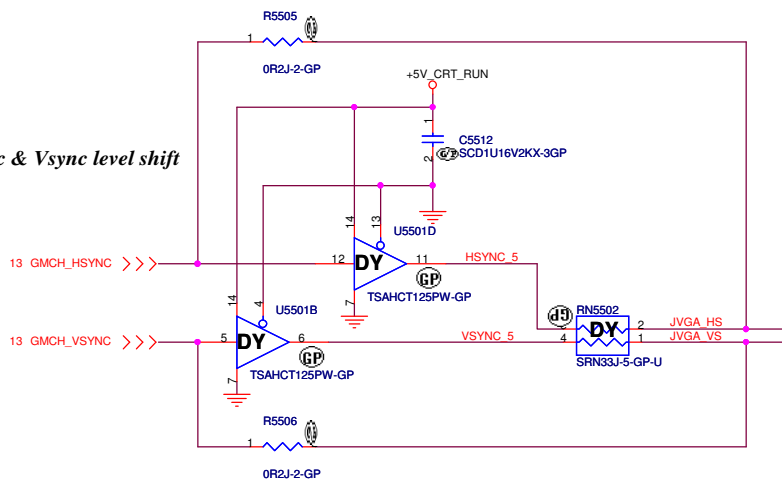
**Layout Note:**

- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



AFTP5501	1	+5V_CRT_RUN
AFTP5506	1	DDC_DATA_CON
AFTP5503	1	DDC_CLK_CON
AFTP5506	1	CRT_R
AFTP5507	1	CRT_G
AFTP5504	1	CRT_B
AFTP5505	1	JVGGA_HS
AFTP5506	1	JVGGA_VS

**Hsync & Vsync level shift**




<Core Design>

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Title <b>CRT Connector</b>		
Size	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
Date: Thursday, August 20, 2009	Sheet 55	of 88

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<Core Design>



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Title

**Reserved**


Size	Document Number	Rev
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>

Date: Wednesday, July 29, 2009	Sheet 56 of 88
--------------------------------	----------------



20090724 Remove HDMI

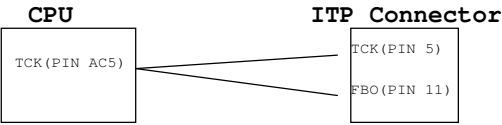
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>HDMI</b>			
Size	Document Number		Rev
A3	<b>DJ2 Montevina UMA</b>		<b>X00</b>
Date:	Wednesday, July 29, 2009	Sheet	57 of 88

SSID = User.Interface

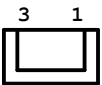
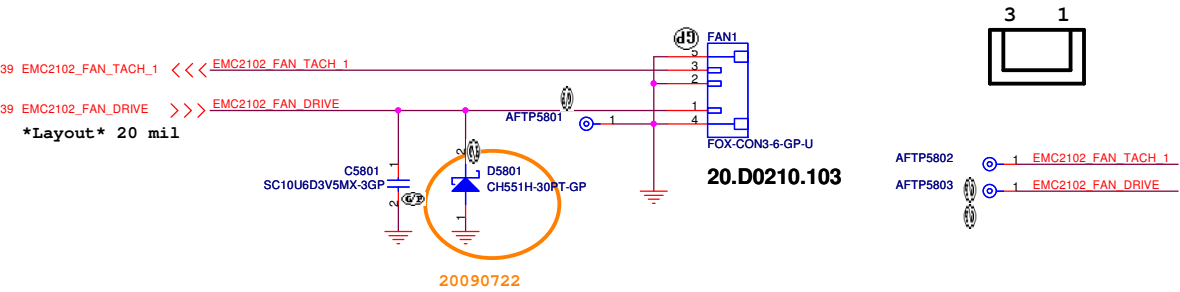
# ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



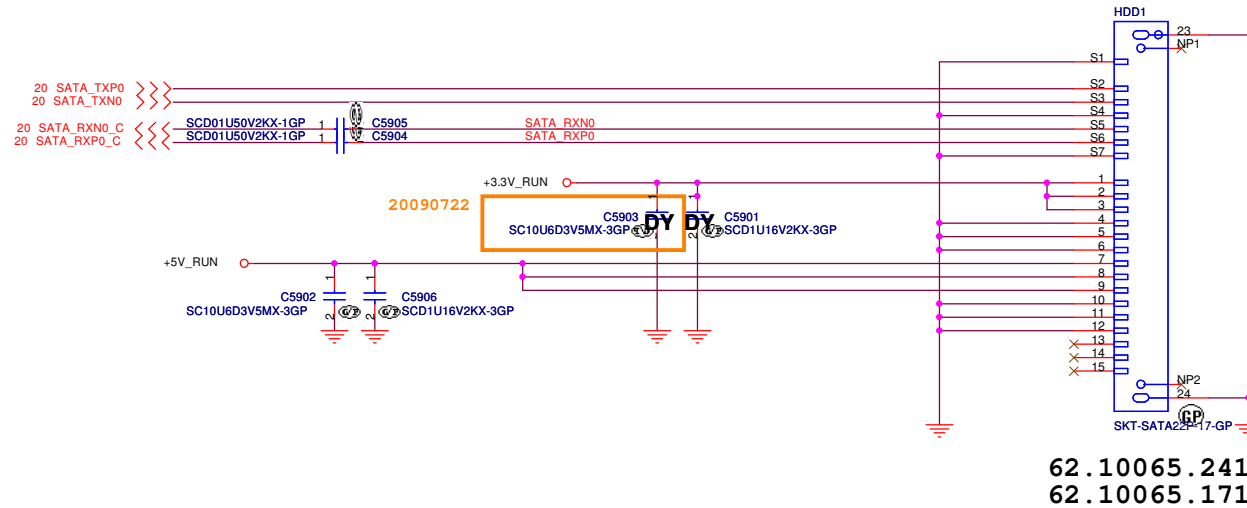
SSID = Thermal

# Fan Connector

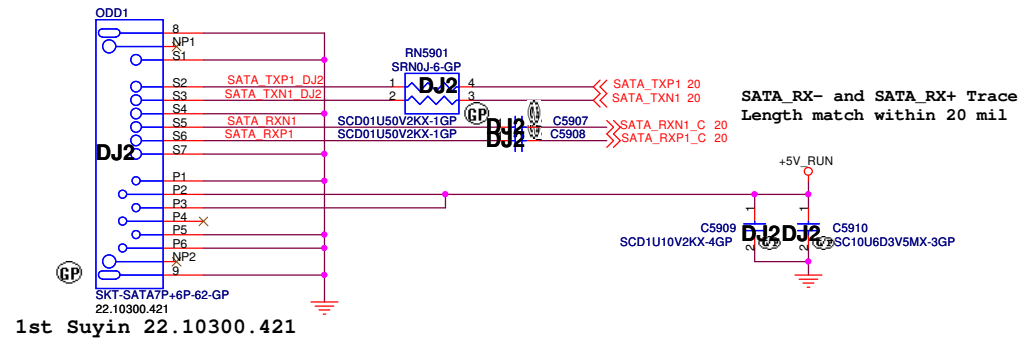


SSID = SATA

## SATA HDD Connector



## ODD Connector



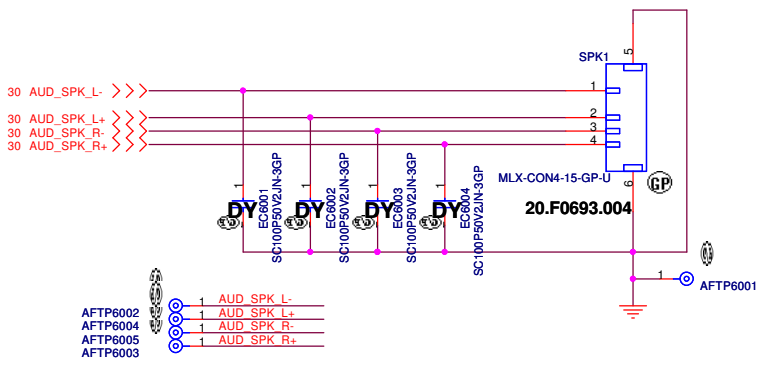
<Core Design>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>HDD/ODD</b>			
Size	Document Number	Rev	
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>	
Date:	Thursday, August 20, 2009	Sheet	59 of 88

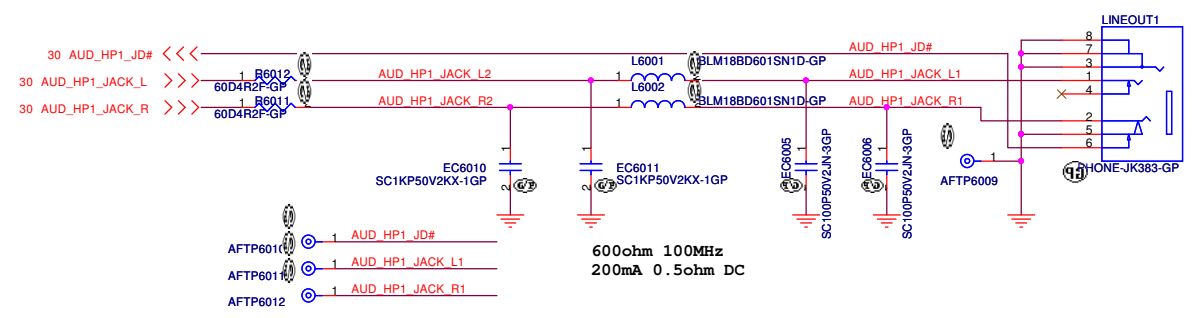
WWW.AliSaler.Com

SSID = AUDIO

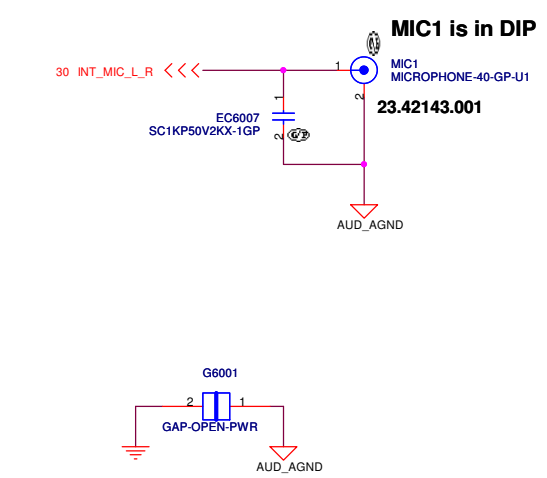
## Speaker Connector



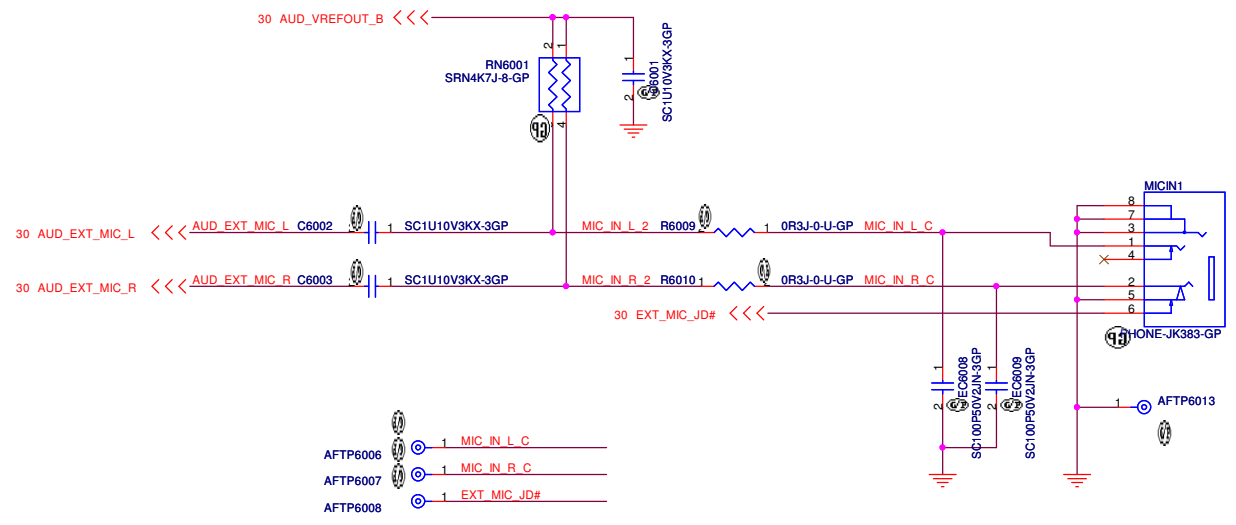
## LINE1 OUT



## Internal Microphone




## MIC IN



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Title

Size  
A3

Document Number  
**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009

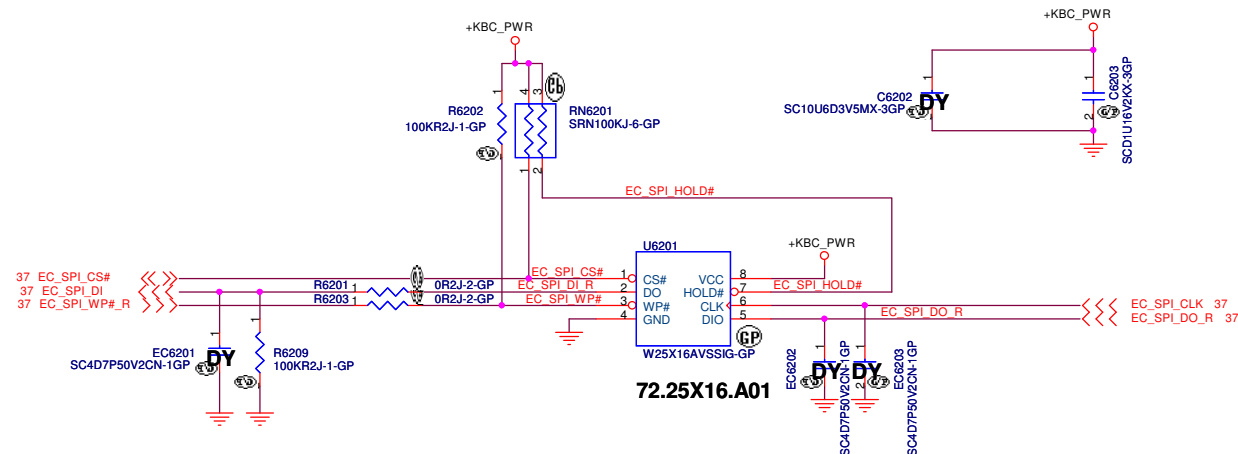
**Reserved**

Rev  
**X00**

Sheet 61 of 88

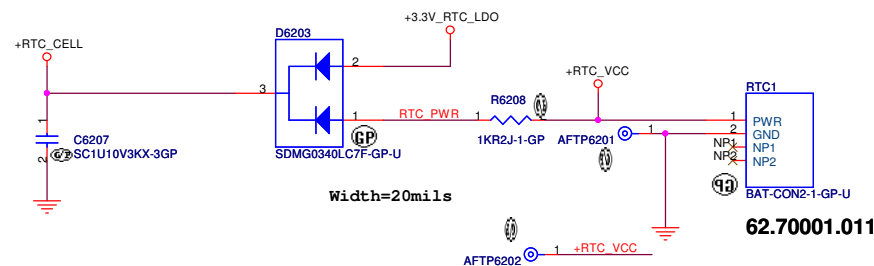
SSID = Flash.ROM

## SPI FLASH ROM (16M bits) for KBC



**SSID = RBATT**

## RTC Connector



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Title

### **Flash/RTC**

Size  
A3

	Document Number
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**DJ2 Montevina UMA**

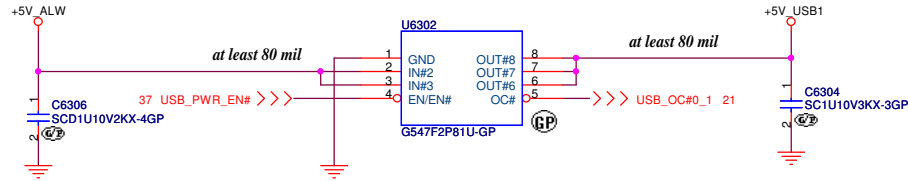
Rev	X00
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Date: Thursday, August 20, 2009

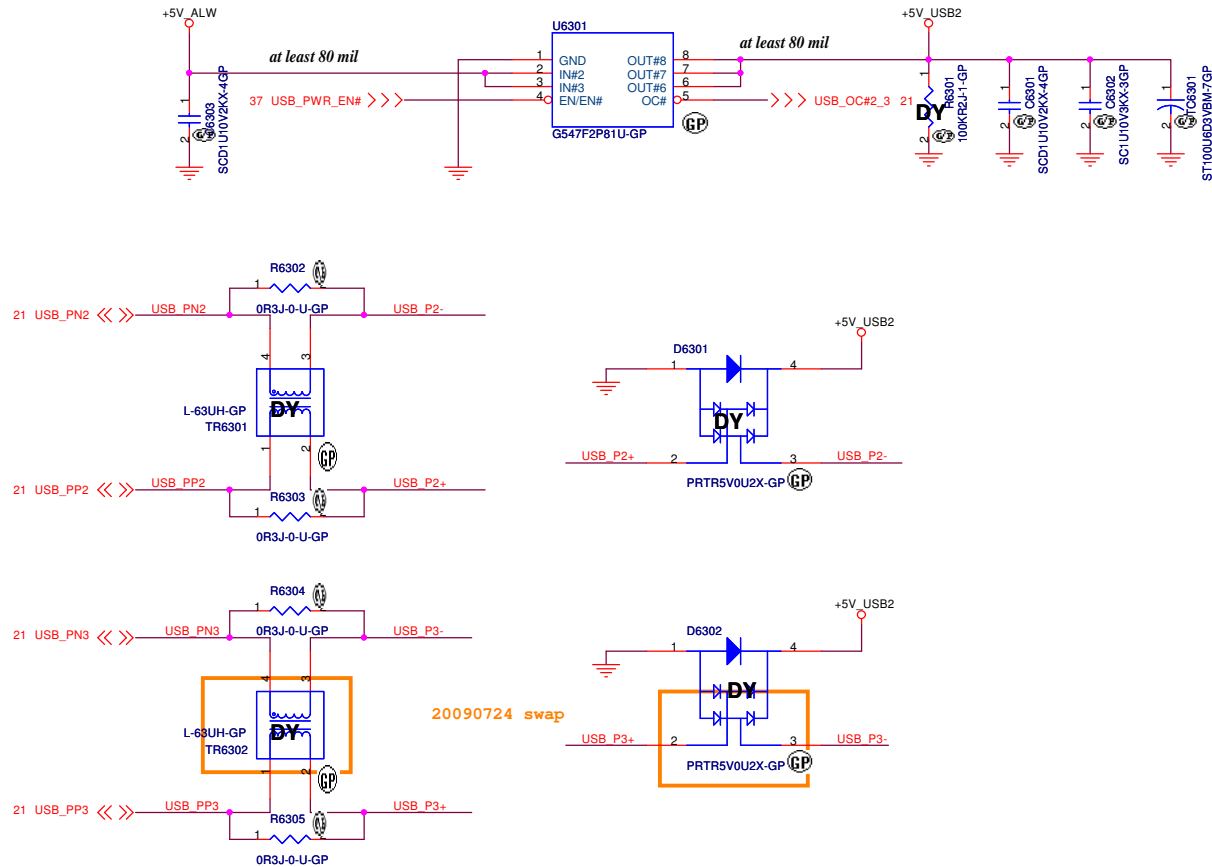
Sheet 62 of 88

88

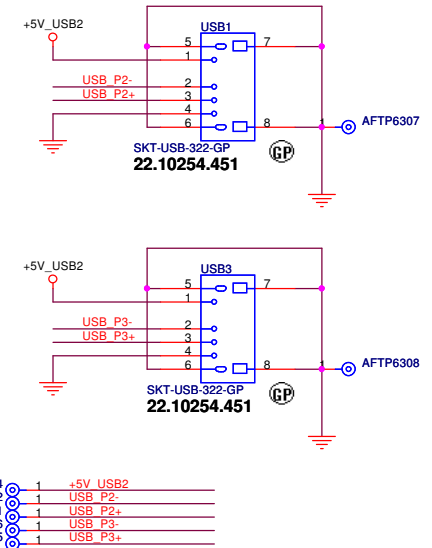
## IO Board USB Power



## Right USB Power



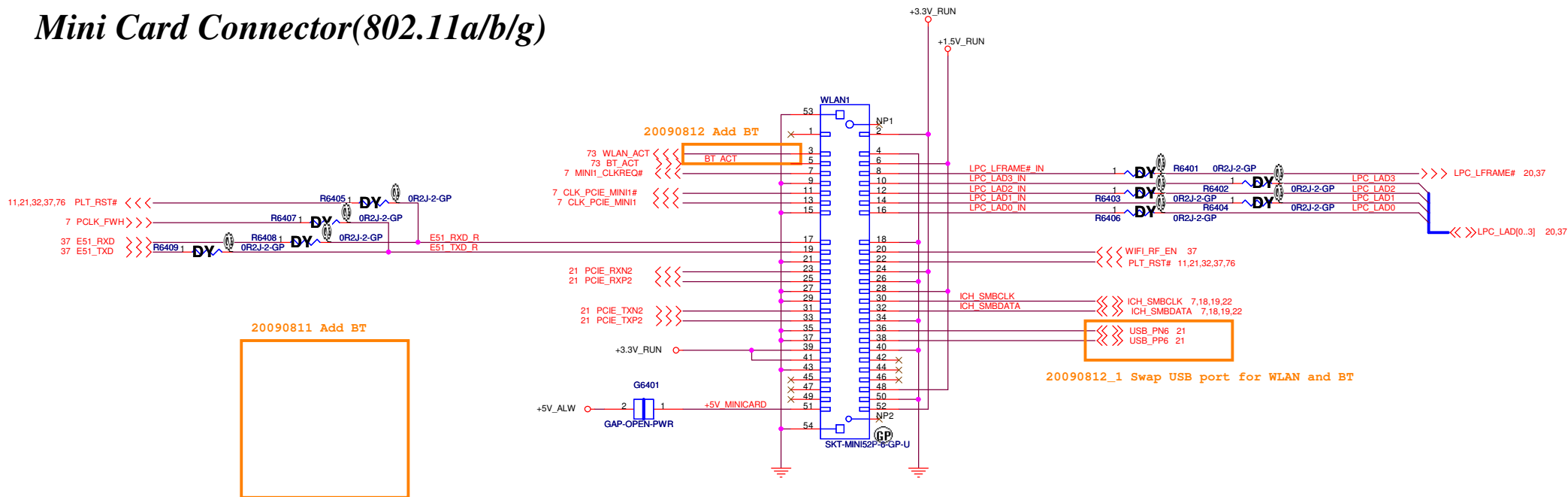
## USB Socket



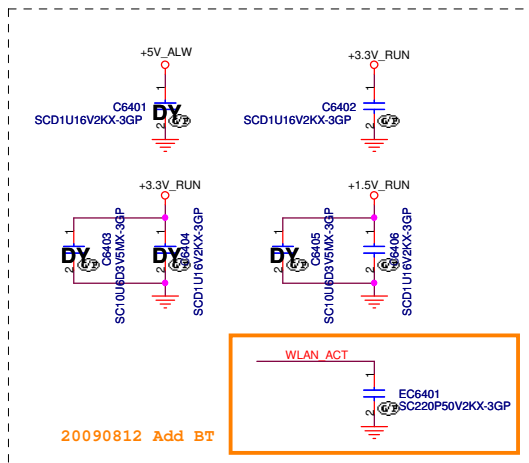
<Core Design>

SSID = Wireless

## Mini Card Connector(802.11a/b/g)



62.10043.261




<Core Design>

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Title <b>MINICARD</b>		
Size Custom	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
Date: Thursday, August 20, 2009	Sheet 64	of 88



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<Core Design>



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Title

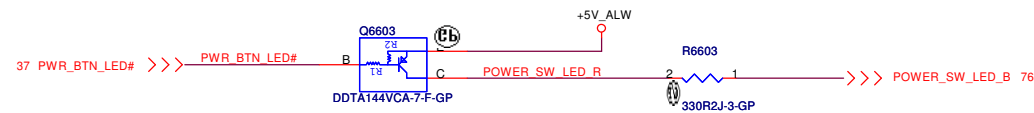
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Size	Document Number	Rev
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>

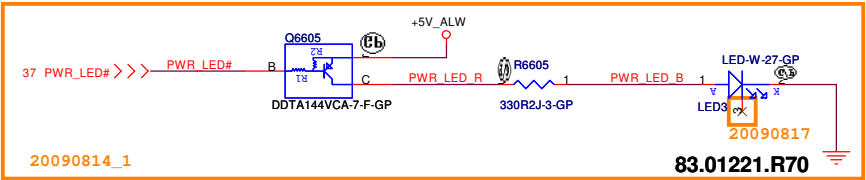
Date: Wednesday, July 29, 2009	Sheet 65 of 88
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SSID = LED

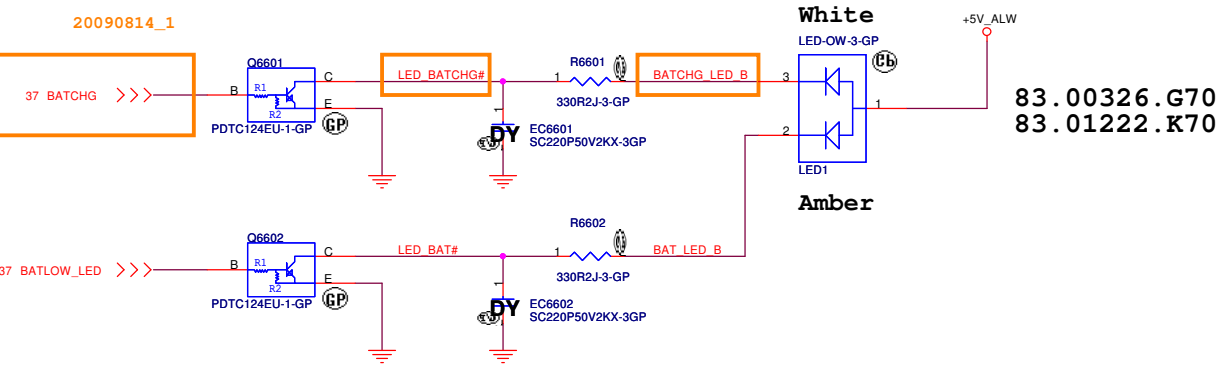
Power button LED



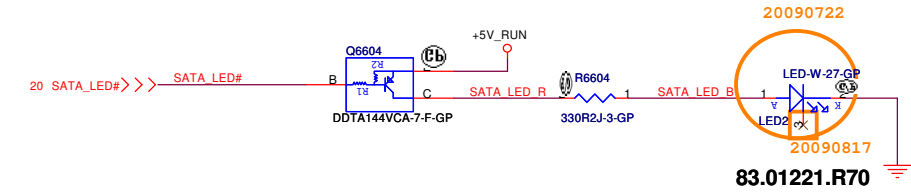
Power LED



Battery LED



HDD LED



<Core Design>


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Title: **LED**

Size: A3	Document Number: <b>DJ2 Montevina UMA</b>	Rev: <b>X00</b>
Date: Thursday, August 20, 2009	Sheet: 66 of 88	

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<Core Design>



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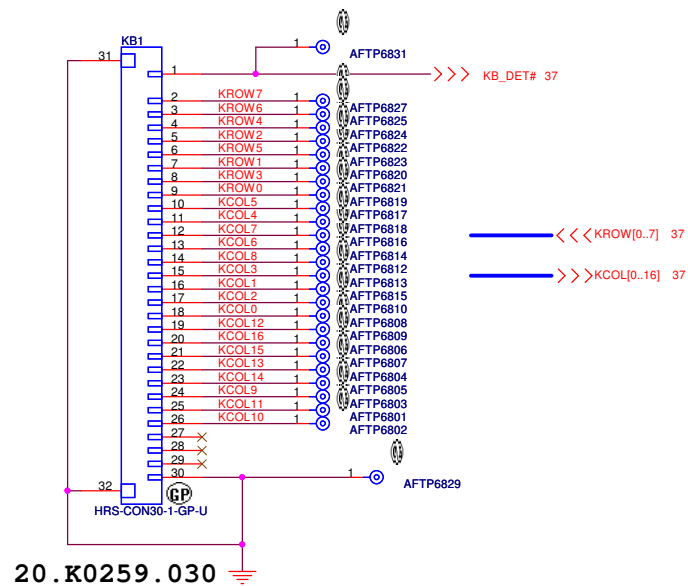
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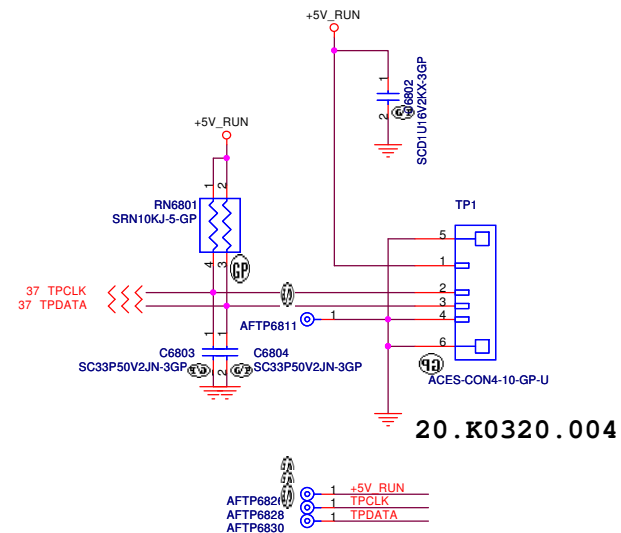
Size	Document Number	Rev
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>

Date: Wednesday, July 29, 2009	Sheet 67 of 88
--------------------------------	----------------

### Internal KeyBoard Connector



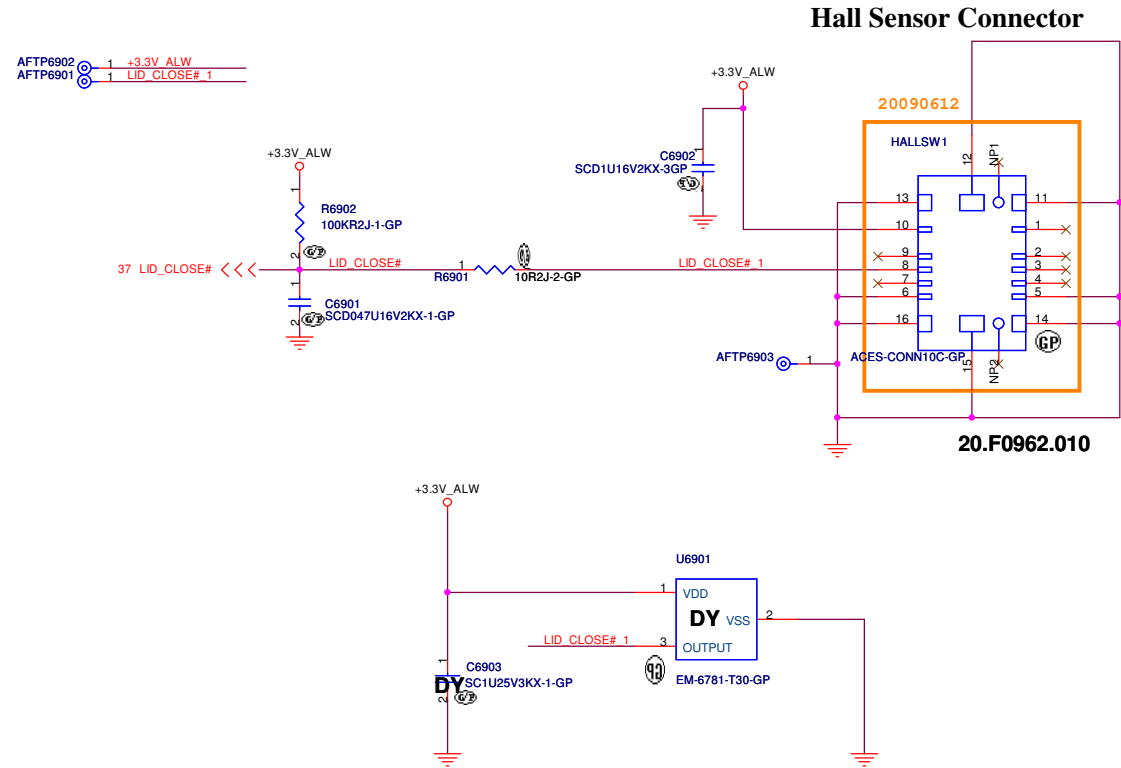
### TouchPad Connector



<Core Design>

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Title			Key Board/Touch Pad
Size	Document Number	Rev	X00
A3	DJ2 Montevina UMA		
Date:	Thursday, August 20, 2009	Sheet	68 of 88



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Title

**Hall Sensor**

Size  
A3

Document Number

**DJ2 Montevina UMA**

Rev


**X00**

Date: Thursday, August 20, 2009

Sheet 69 of 88

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Title

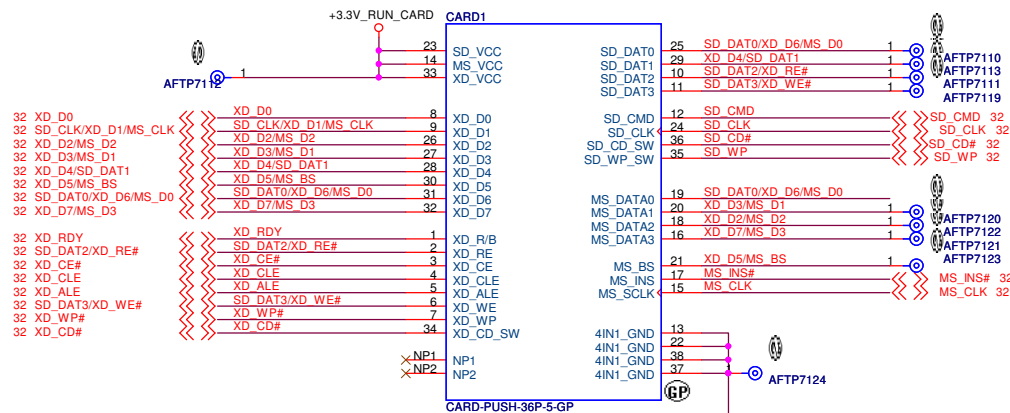
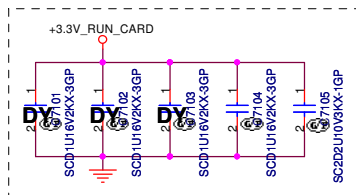
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Size A3	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
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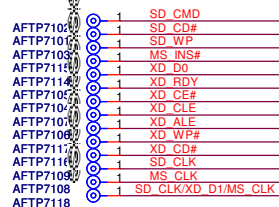
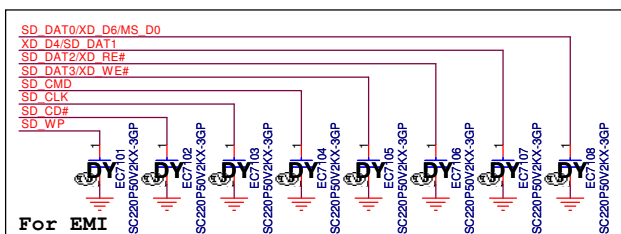
Date: Wednesday, July 29, 2009	Sheet 70 of 88
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# SD/XD/MS Card Reader

SSID = SDIO



20.I0081.011




<Core Design>

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Title		CARD Reader Connector	
Size	Document Number	Rev	
A3	DJ2 Montevina UMA	X00	
Date:	Thursday, August 20, 2009	Sheet	71 of 88

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Title

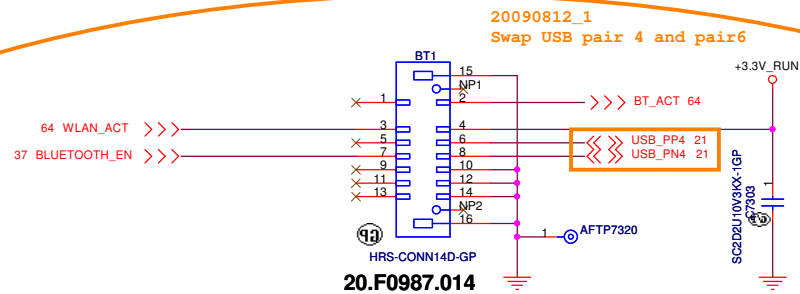
**RESERVED**

Size A3	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
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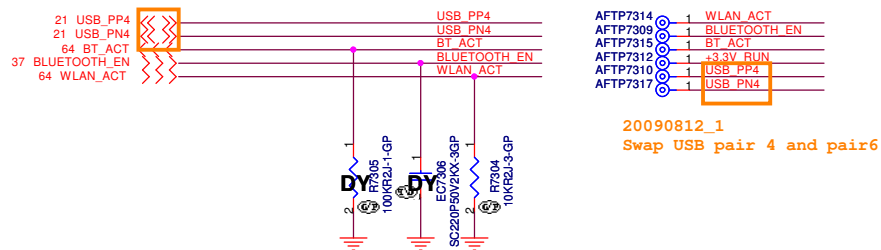
Date: Wednesday, July 29, 2009	Sheet 72 of 88
--------------------------------	----------------



20090811 Add BT




```
20090812_1
Swap USB pair 4 and pair6
```



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Title

Size  
A3

Document Number  
**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009


**Reserved**

Rev  
**X00**

Sheet 74 of 88

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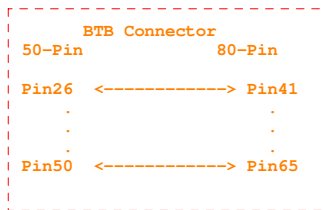


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Taipei Hsien 221, Taiwan, R.O.C.

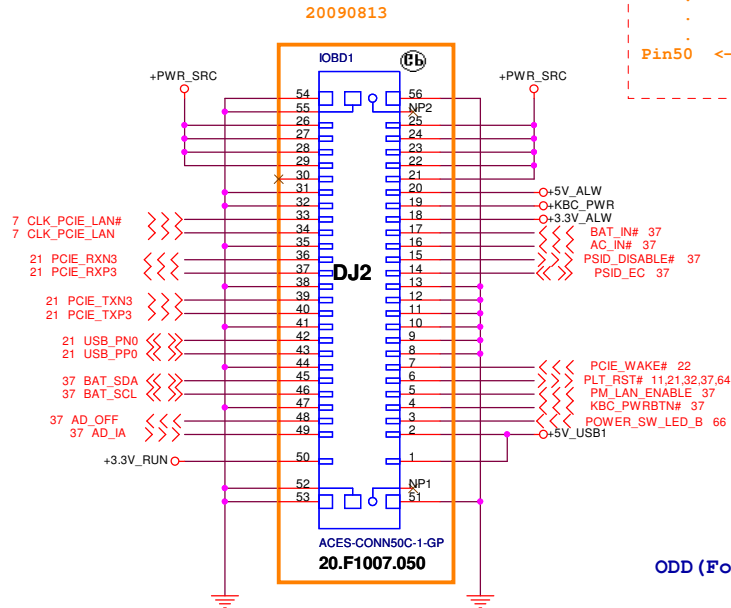
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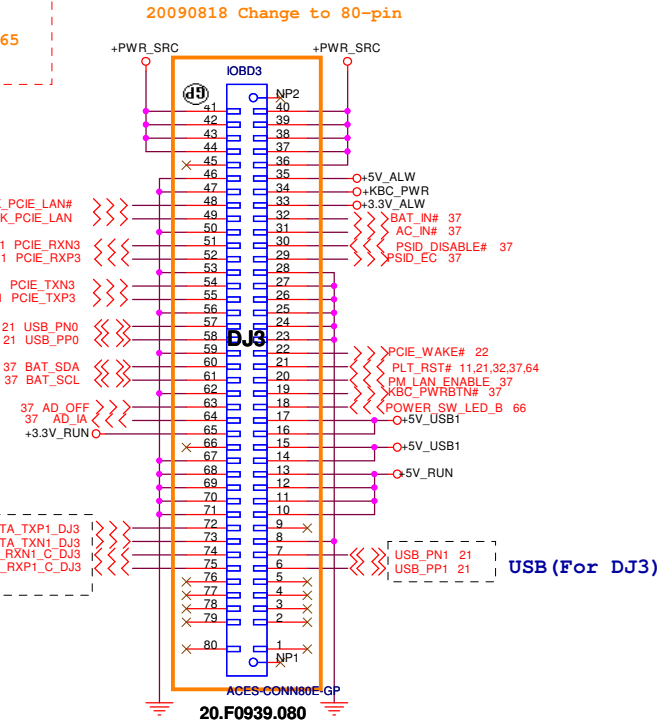
Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00
Date:	Wednesday, July 29, 2009	Sheet 75 of 88



LAN CLK  
LAN PCIE  
LAN PCIE  
USB Port  
BATT SMBUS

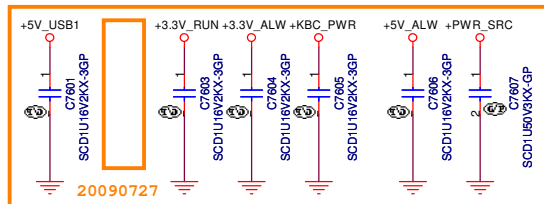


LAN CLK  
LAN PCIE  
LAN PCIE  
USB Port  
BATT SMBUS



ODD (For DJ3)

20090707



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Title

**IO Board Connector**

Size  
A3

Document Number  
**DJ2 Montevina UMA**


Rev  
**X00**

Date: Thursday, August 20, 2009

Sheet 76 of 88

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Title

**Reserved**

Size	Document Number	Rev
A3	<b>DJ2 Montevina UMA</b>	<b>X00</b>
Date:	Wednesday, July 29, 2009	Sheet 77 of 88

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Title

Size  
A3

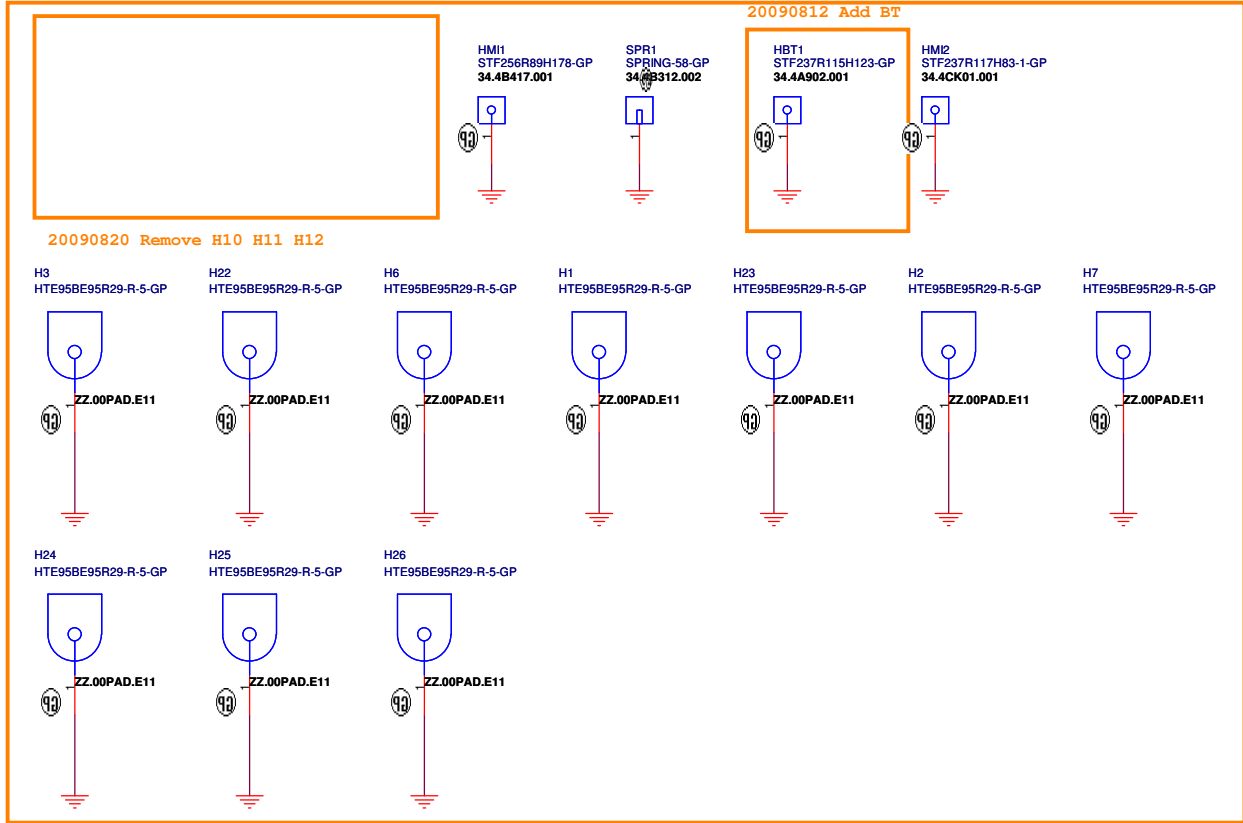
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**DJ2 Montevina UMA**

Date: Wednesday, July 29, 2009

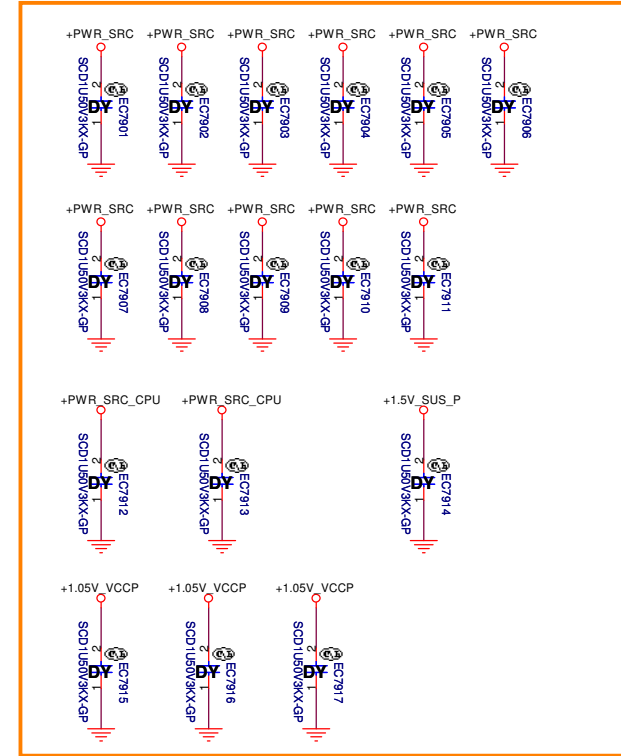
**Reserved**

Rev  
**X00**

Sheet 78 of 88




20090804 EMI request



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Title

(Reserved)

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00
Date: Wednesday, July 29, 2009	Sheet 80 of	88



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Title <b>(Reserved)</b>			
Size <b>C</b>	Document Number <b>DJ2 Montevina UMA</b>		Rev <b>X00</b>
Date: Wednesday, July 29, 2009		Sheet 81	of 88

The image shows a blank A2 drawing sheet with a grid. The grid lines are spaced at 100mm intervals. The sheet is oriented horizontally. In the bottom right corner, there is a title block with the following information:

-Core Design-		
<b>DELL</b> Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>(Reserved)</b>		
Size <b>A2</b>	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
Date: Wednesday, July 28, 2009	Sheet 82 of 88	

The text "WWW.AliSaler.Com" is visible in the top left and bottom center of the sheet.

WWW.AliSaler.Com

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<b>DELL</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipet Hsien 221, Taiwan, R.O.C.		
File		
<b>(Reserved)</b>		
Size <b>C</b>	Document Number <b>DJ2 Montevina UMA</b>	Rev <b>X00</b>
Date: Wednesday, July 29, 2009		Sheet 83 of 88

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Title

(Reserved)

Size

Document Number

Rev

Custom

DJ2 Montevina UMA

X00

Date: Wednesday, July 29, 2009

Sheet 84 of 88

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<Core Design>

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Title

(Reserved)

Size

Document Number

Rev

Custom

DJ2 Montevina UMA


X00

Date: Wednesday, July 29, 2009

Sheet 85 of 88

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Title

(Reserved)

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00
Date:	Wednesday, July 29, 2009	Sheet 86 of 88

(Blanking)

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Title


(Reserved)

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00

Date: Wednesday, July 29, 2009	Sheet 87 of 88
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Title

Change History

Size	Document Number	Rev
A3	DJ2 Montevina UMA	X00
Date:	Wednesday, July 29, 2009	Sheet 88 of 88