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Ansenal DJ1 UMA Schematics Document

AMD Danube CPU S1G4

RS880M + SB820M

2010-03-23

REV : X02

DY : Nopop Component

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Title	Cover Page	
Size: Custom	Document Number: Ansenal DJ1 AMD UMA	Rev: X02
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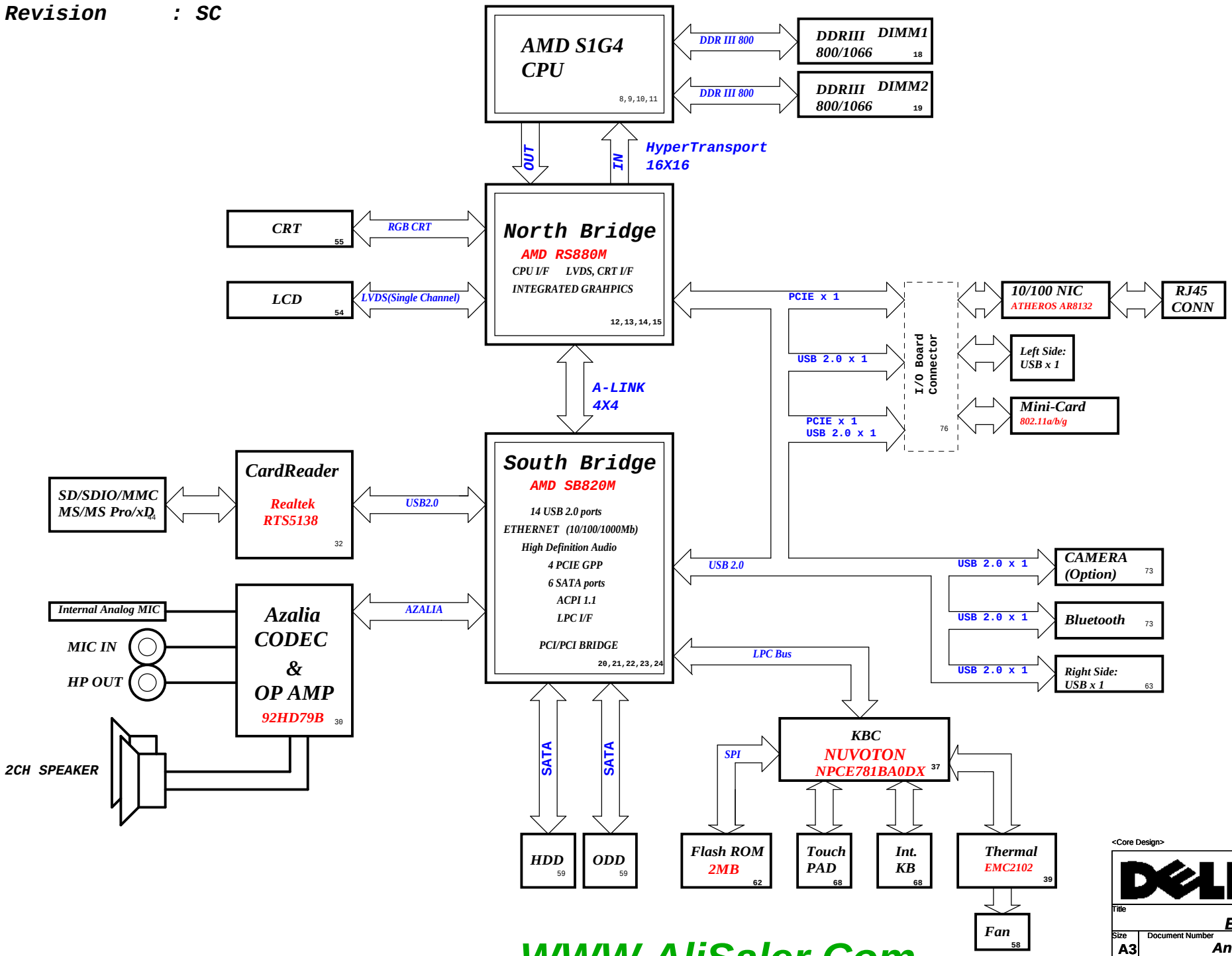
Project code : 91.4EK01.001
PCB P/N : 09940
Revision : SC

Ansenal DJ1 AMD UMA Block Diagram



CHARGER BQ24745RHDR	
INPUTS	OUTPUTS
+DC_IN_SS +CHAGER_SRC	+PWR_SRC

SYSTEM DC/DC RT8205BGQW-GP 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC RT8209EGQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_RUN

CPU CORE ISL6265AHRTZ-T-GP 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE +VDDNB

DDR III SUS&VTT RT8207GQW-GP 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS

SYSTEM DC/DC APL5930KAI 52	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

SYSTEM DC/DC Swithes/RT9013 42,53	
INPUTS	OUTPUTS
+3.3V_ALW +5V_ALW +1.5V_SUS +3.3V_RUN	+3.3V_RUN +5V_RUN +1.5V_RUN +2.5V_RUN

SYSTEM DC/DC RT9025 48,51	
INPUTS	OUTPUTS
+3.3V_ALW +1.5V_SUS	+1.1V_ALW +CPU_VDDR

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Title: Block Diagram

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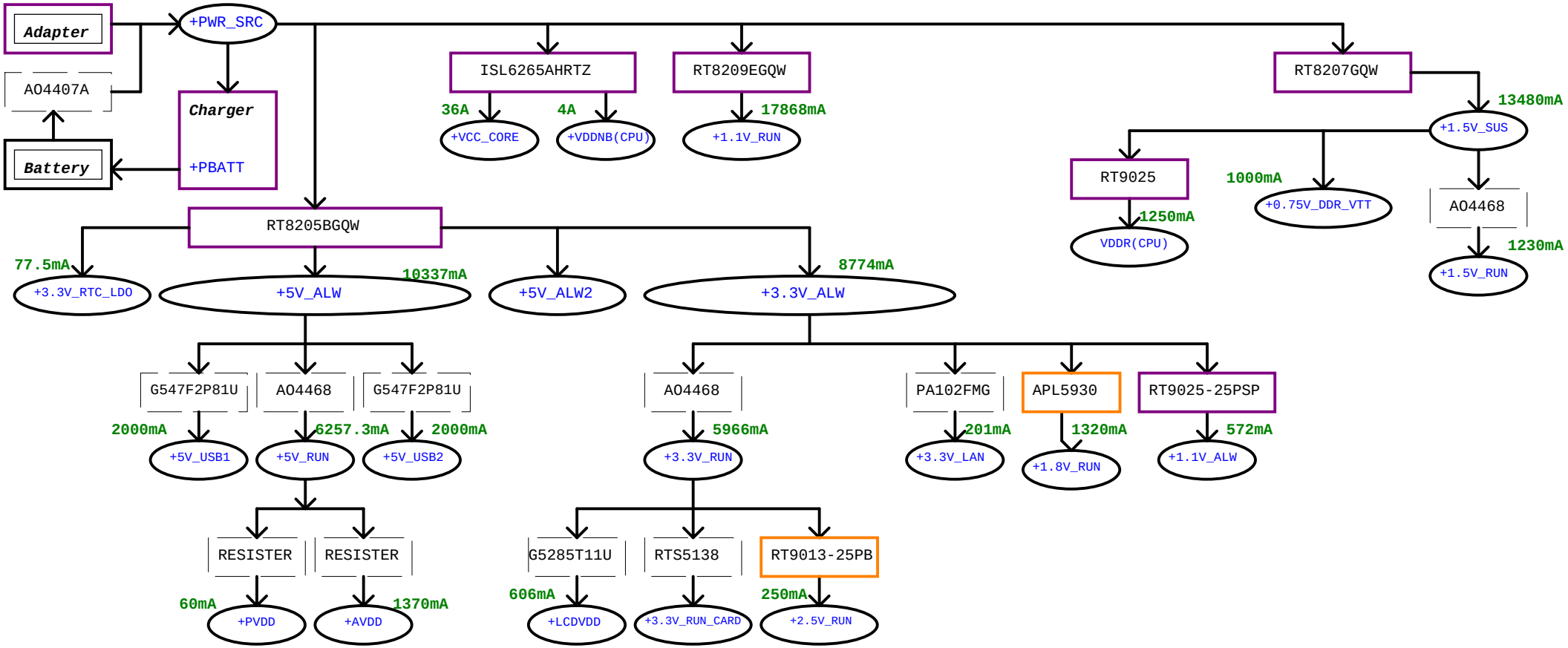
Power Block Diagram



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Title: Power Block Diagram

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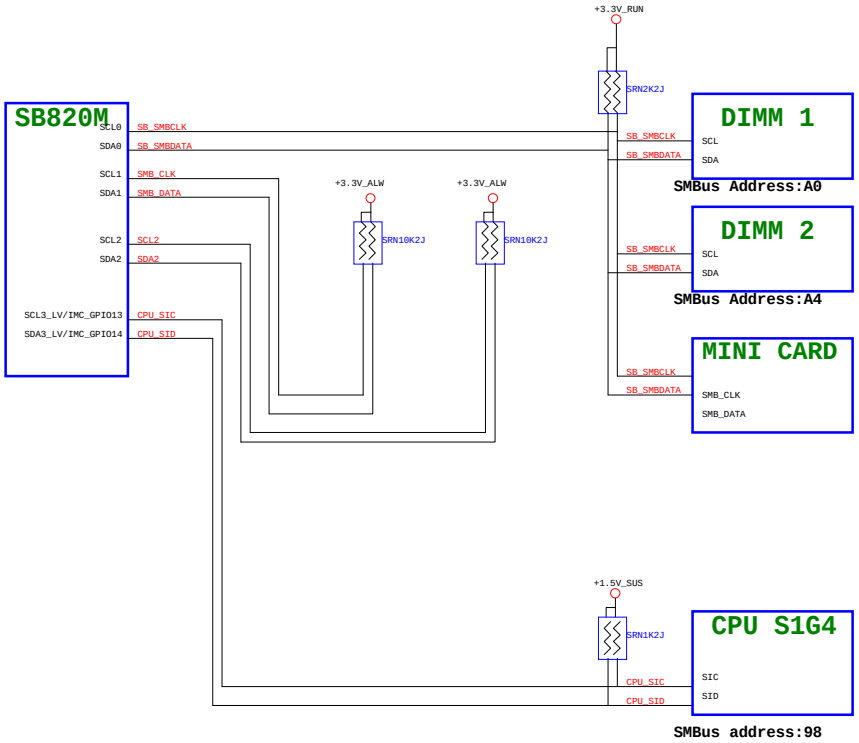
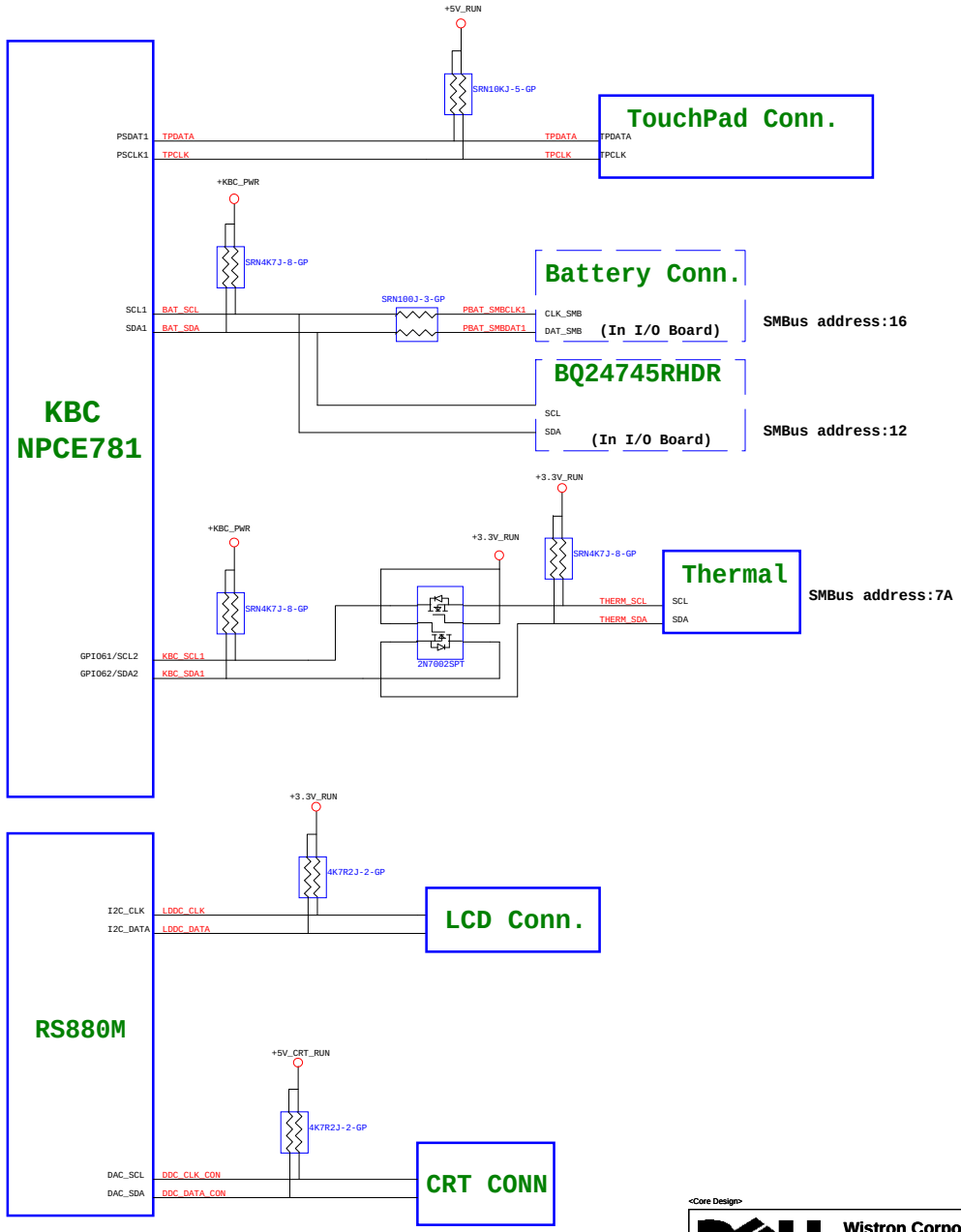
SB820M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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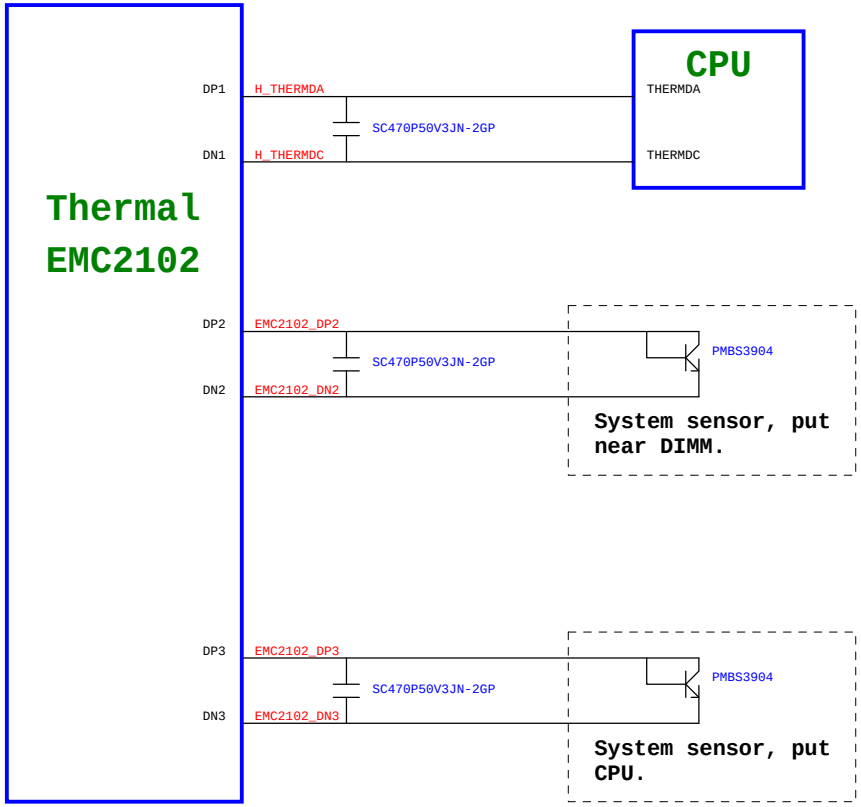
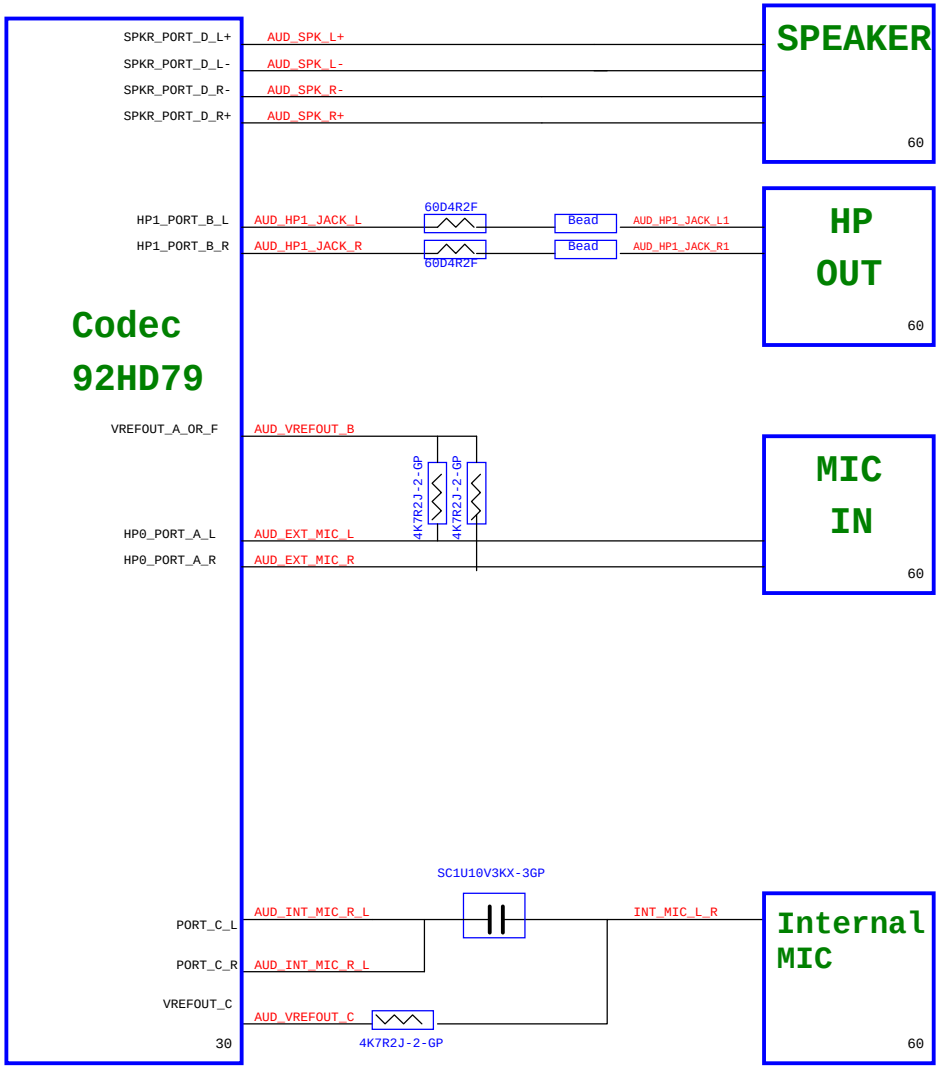
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V – Disabled 3.3 V - Enabled
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	ROMTYPE_1 / ROMTYPE_0 / ROM TYPE 3.3V / 0V / SPI ROM 3.3V / 3.3V / Reserved 0V / 0V / Firmware Hub * 0V / 3.3V / LPC ROM (supports both LPC and PMC ROM types)
LPCCLK1	CLKGEN	Defines clock generator 0V – External clock mode: Use 100-MHz PCIeR clock as reference clock and generate i nternal clocks only. * 3.3V– Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks
PCICLK1	BIF_GEN2_ COMPLIANCE_Strap	Set PCIe to Gen II mode 0V– Force PCIe interface at Gen I mode * 3.3V- PCIe interfacce is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.
PCICLK2	BootFailTmrEn	Watchdog function * 0V– Disable the boot fail timer function 3.3V- Enable the boot fail timer function
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V– Disable Debug Straps. 3.3V– Select external Debug Straps
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection 0V– Reserved. * 3.3V– Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V– Performance mode 3.3V- Low Power mode

NB880M Strapping

Capture from 46113_rs880m_ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO _ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available * 1: Not available
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	USB2 (I/O Board)
3	Reserve
4	WLAN
5	Reserve
6	Reserve
7	Reserve
8	Reserve
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	Reserve
13	Reserve

PCIE Routing

LANE0	LAN
LANE1	MiniCard WLAN

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Title: Table of Content

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Title: Clock Generator ICS9LPRS480

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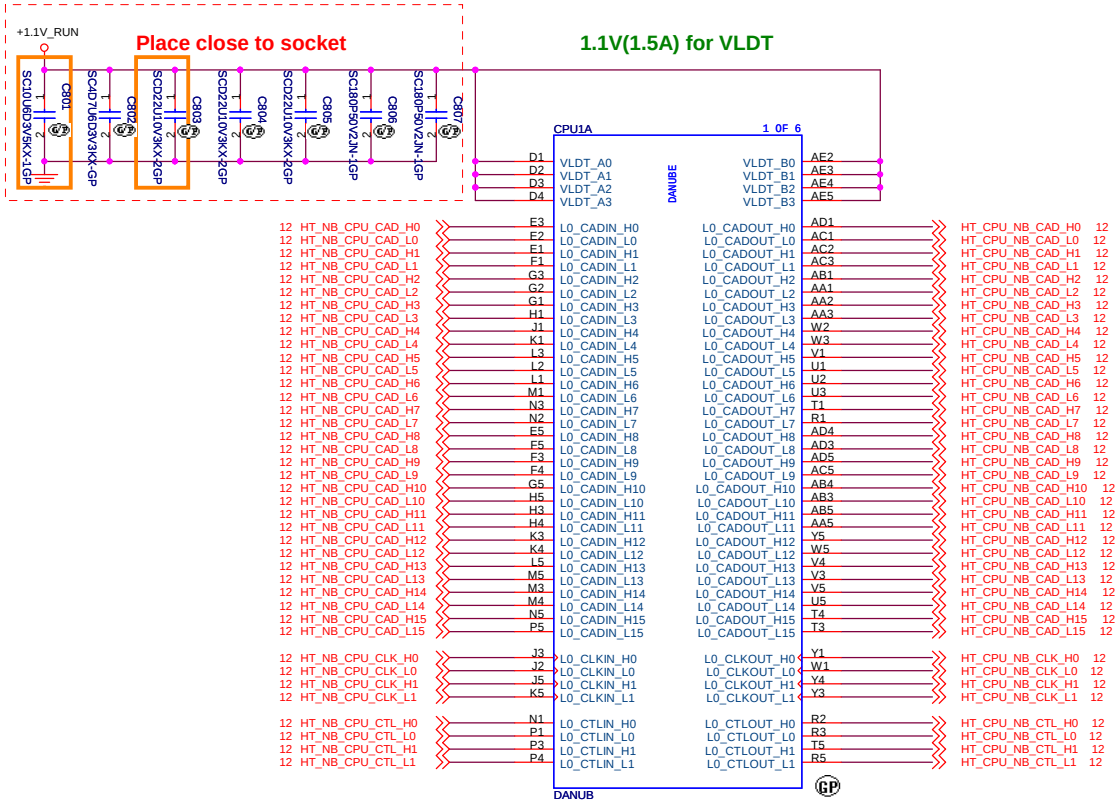
SSID = CPU



SKT-BGA638H176
1'nd 62.10055.111
2'nd 62.10055.171

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Title: CPU_HT_LINK I/F_(1/4)

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Date: Thursday, March 25, 2010 | Sheet 8 of 90

SSID = CPU

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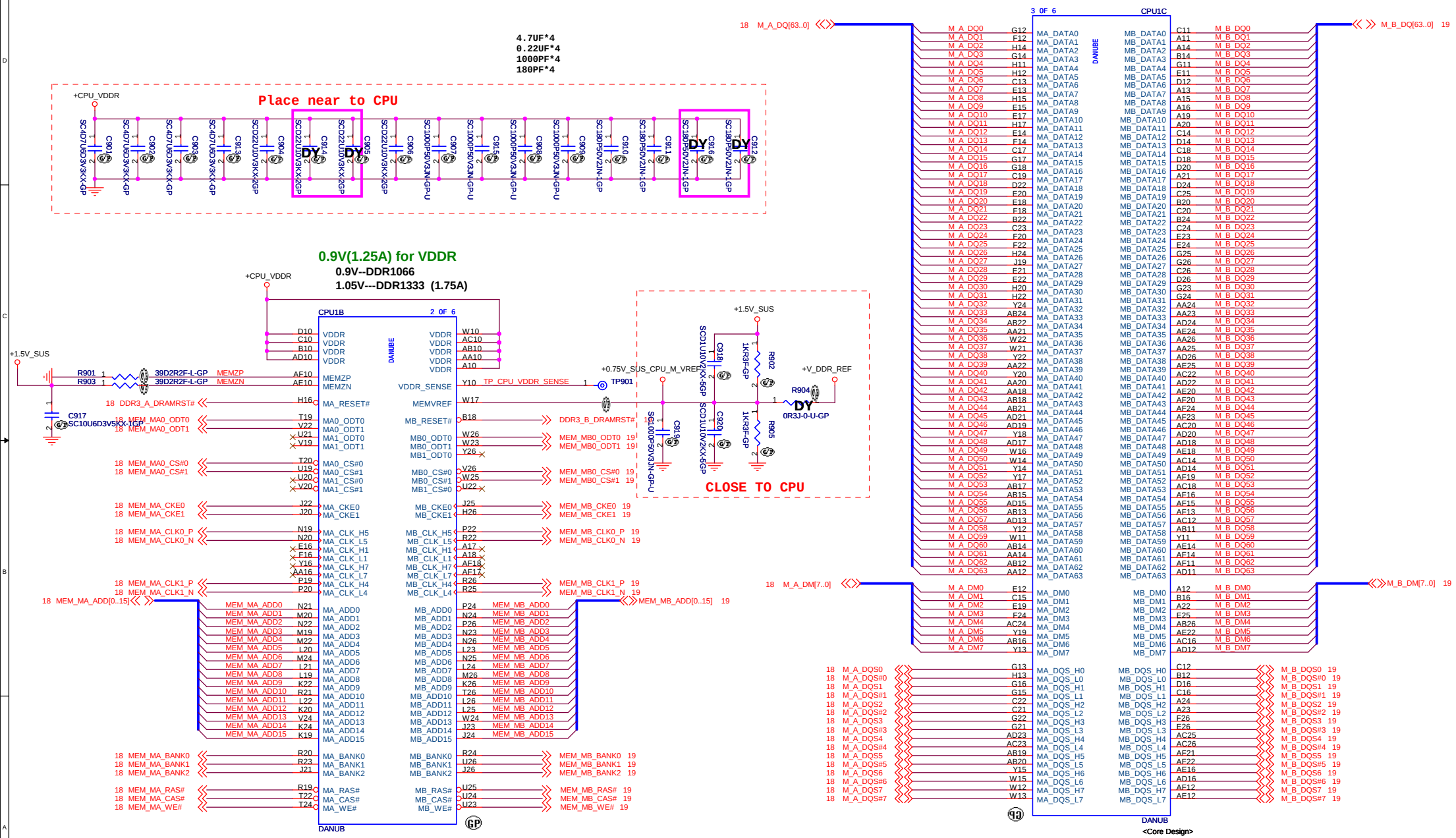
4.7UF*4
0.22UF*4
1000PF*4
180PF*4

Place near to CPU

0.9V(1.25A) for VDDR
0.9V--DDR1066
1.05V---DDR1333 (1.75A)

CLOSE TO CPU



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Title	CPU_DDR(2/4)
Size	Custom
Document Number	Ansenal DJ1 AMD UMA
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Date:	Thursday, March 25, 2010
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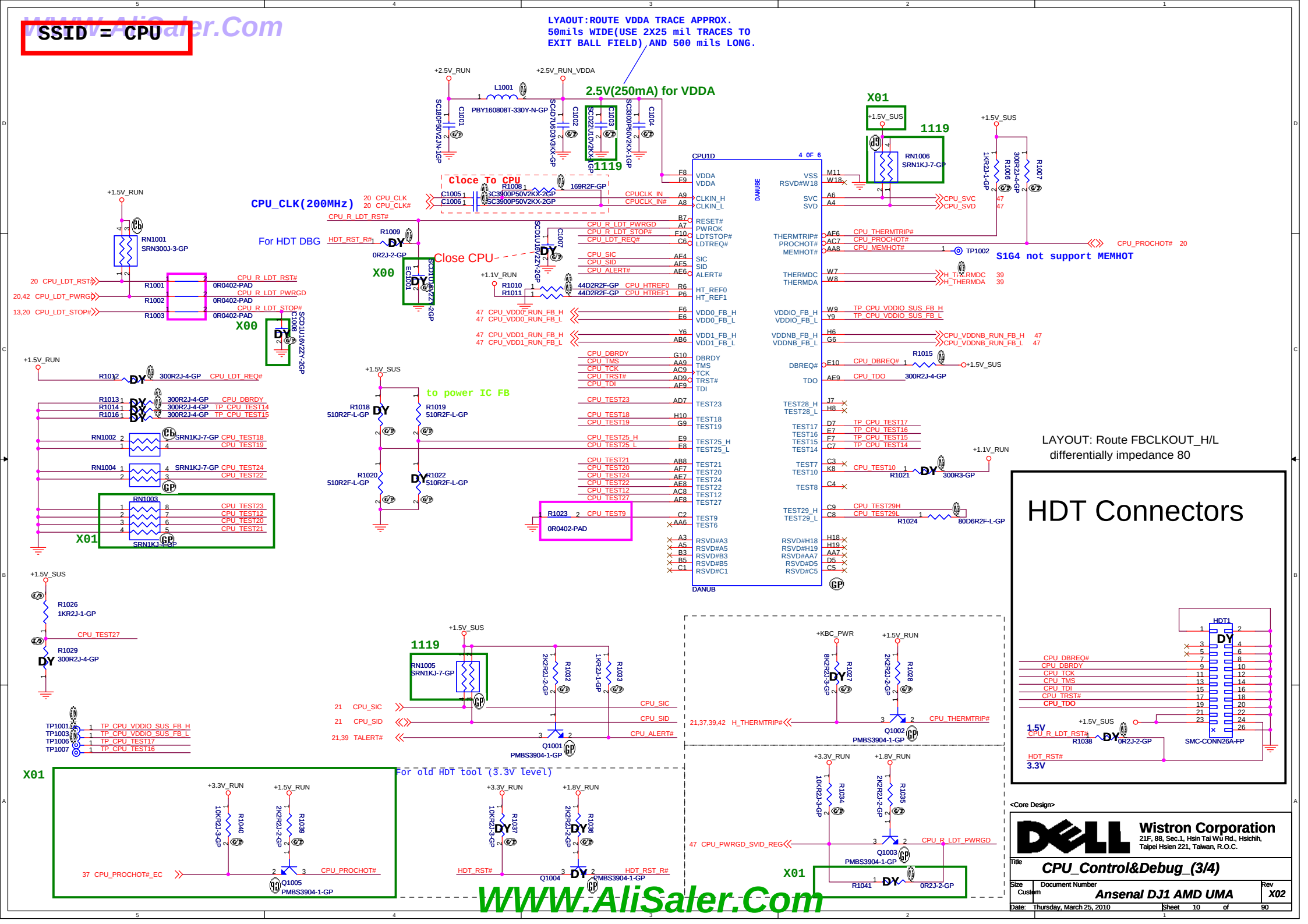
SSID = CPU
LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
2.5V(250mA) for VDDA
Cloce to CPU
CPU_CLK(200MHz)
For HDT DBG
Close CPU
S1G4 not support MEMHOT
to power IC FB
LAYOUT: Route FBCLKOUT_H/L differentially impedance 80
HDT Connectors
For old HDT tool (3.3V level)
CPU_Control&Debug_(3/4)
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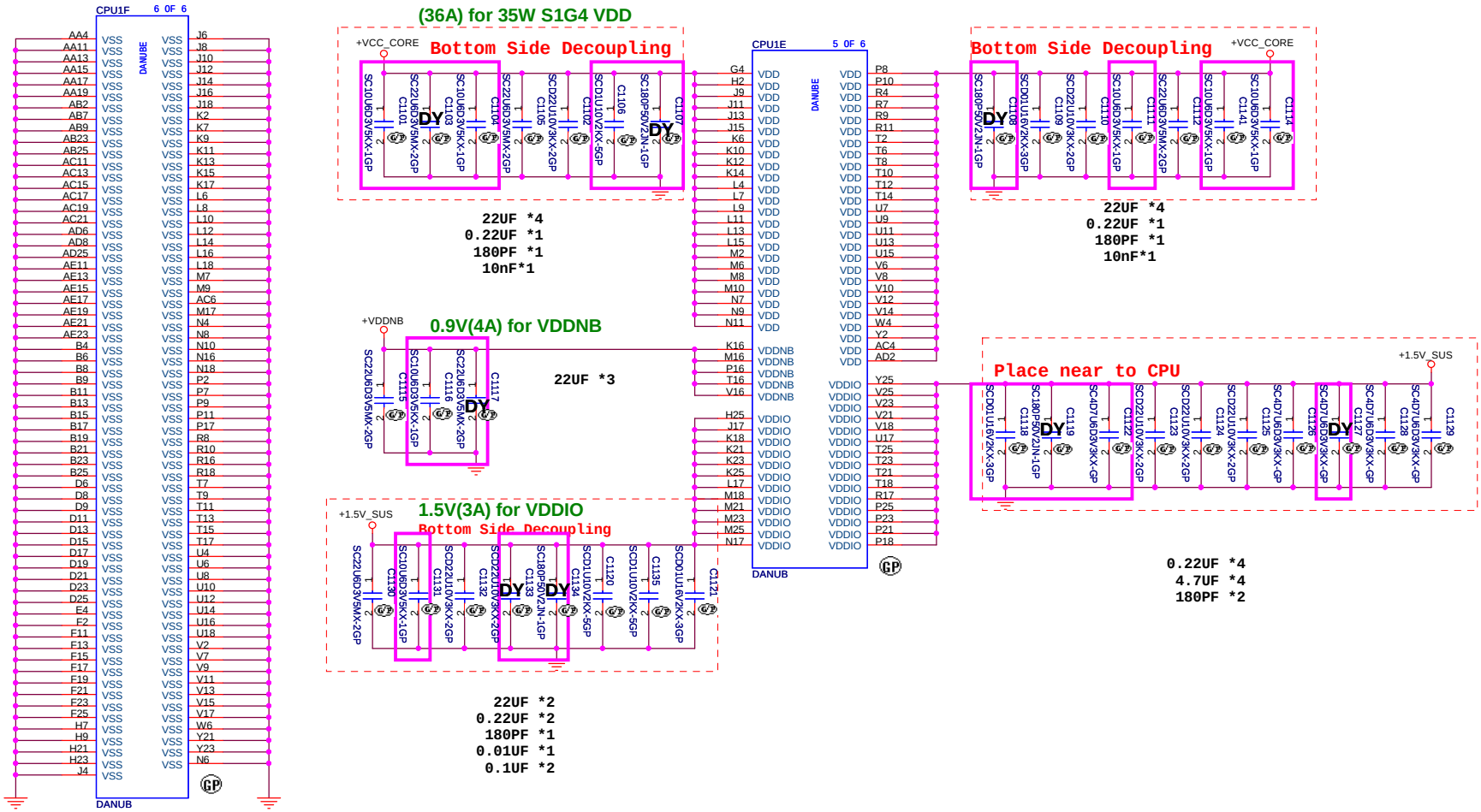
SSID = CPU



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Title: CPU_Power_(4/4)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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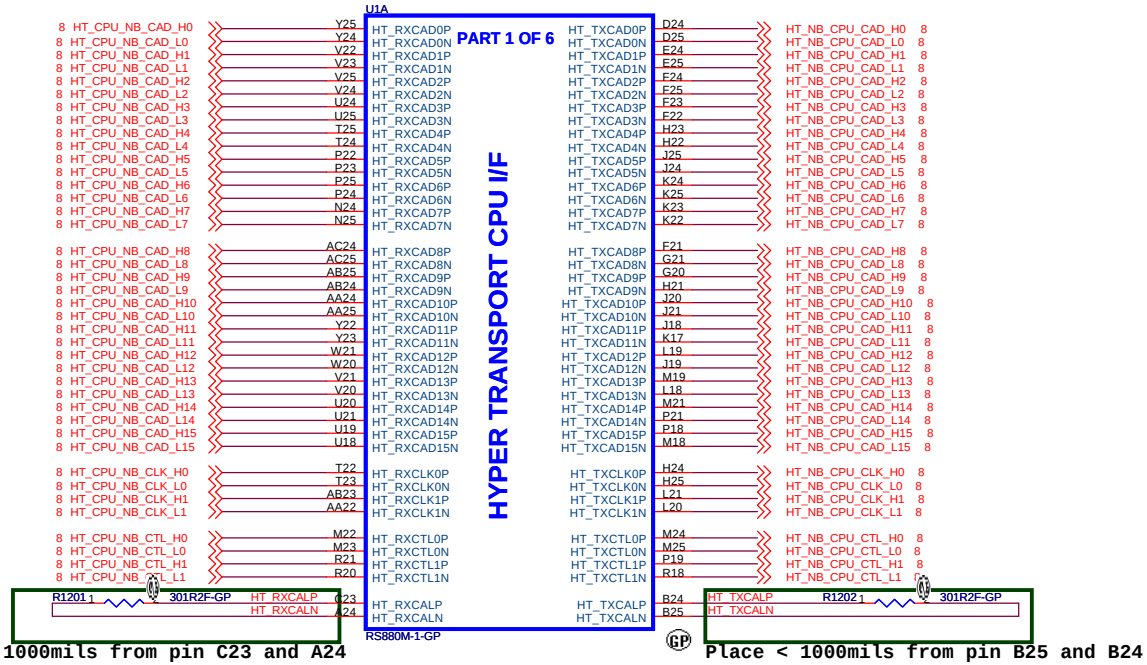
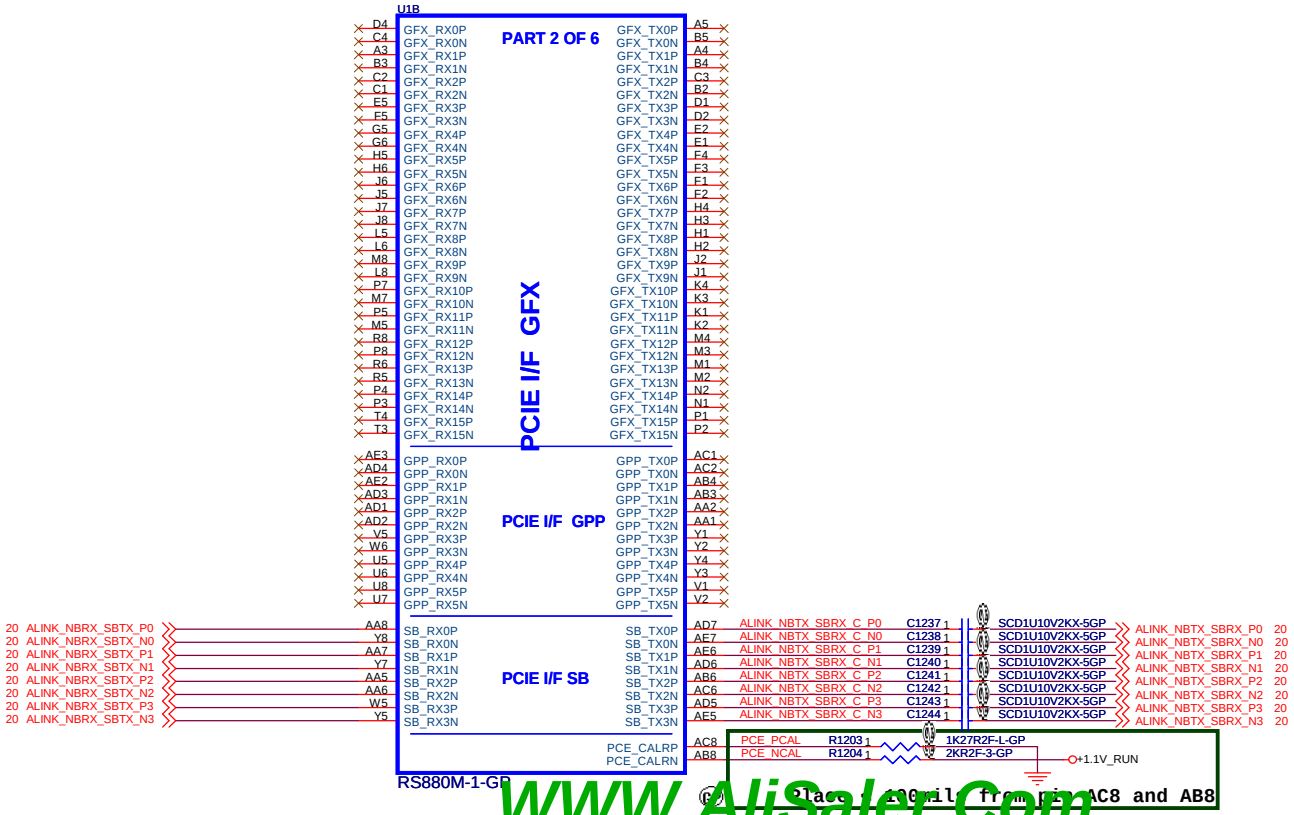
SSID = N.B

RS880M : 71.RS880.M05



Place < 1000mils from pin C23 and A24

Place < 1000mils from pin B25 and B24



Place < 1000mils from pin AC8 and AB8

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Title: AMD-RS880M_HT LINK&PCIe(1/4)

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SSID = N.B

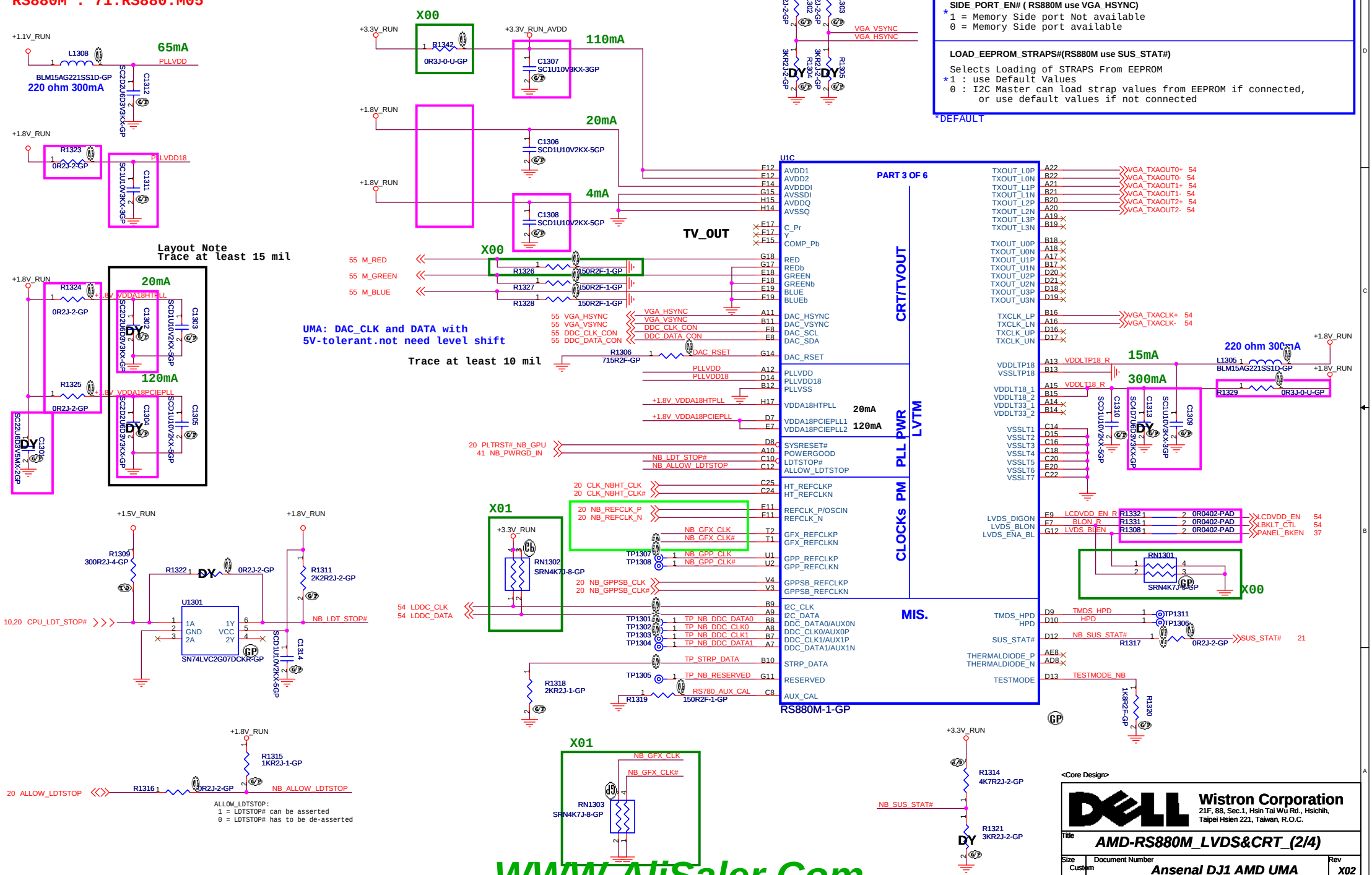
RS880M : 71.RS880.M05

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use VGA_VSYNC)
Enables debug bus access through memory I/O pads and GPIOs.
*1 : Disable
0 : Enable

SIDE_PORT_EN# (RS880M use VGA_HSYNC)
*1 = Memory Side port Not available
0 = Memory Side port available

LOAD_EEPROM_STRAPS#(RS880M use SUS_STAT#)
Selects Loading of STRAPS From EEPROM
*1 : use Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

*DEFAULT



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Title: **AMD-RS880M_LVDS&CRT_(2/4)**

Size: Custom | Document Number: **Ansenal DJ1 AMD UMA** | Rev: X02

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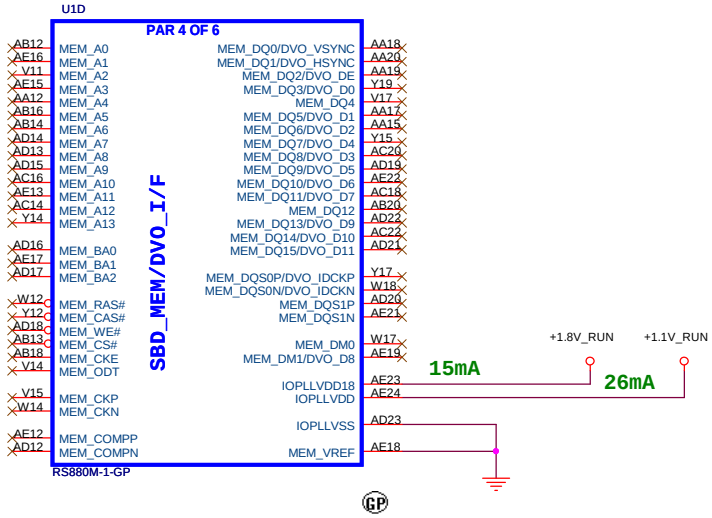
SSID = N.B



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Title: AMD-RS880M_SidePort_(3/4)

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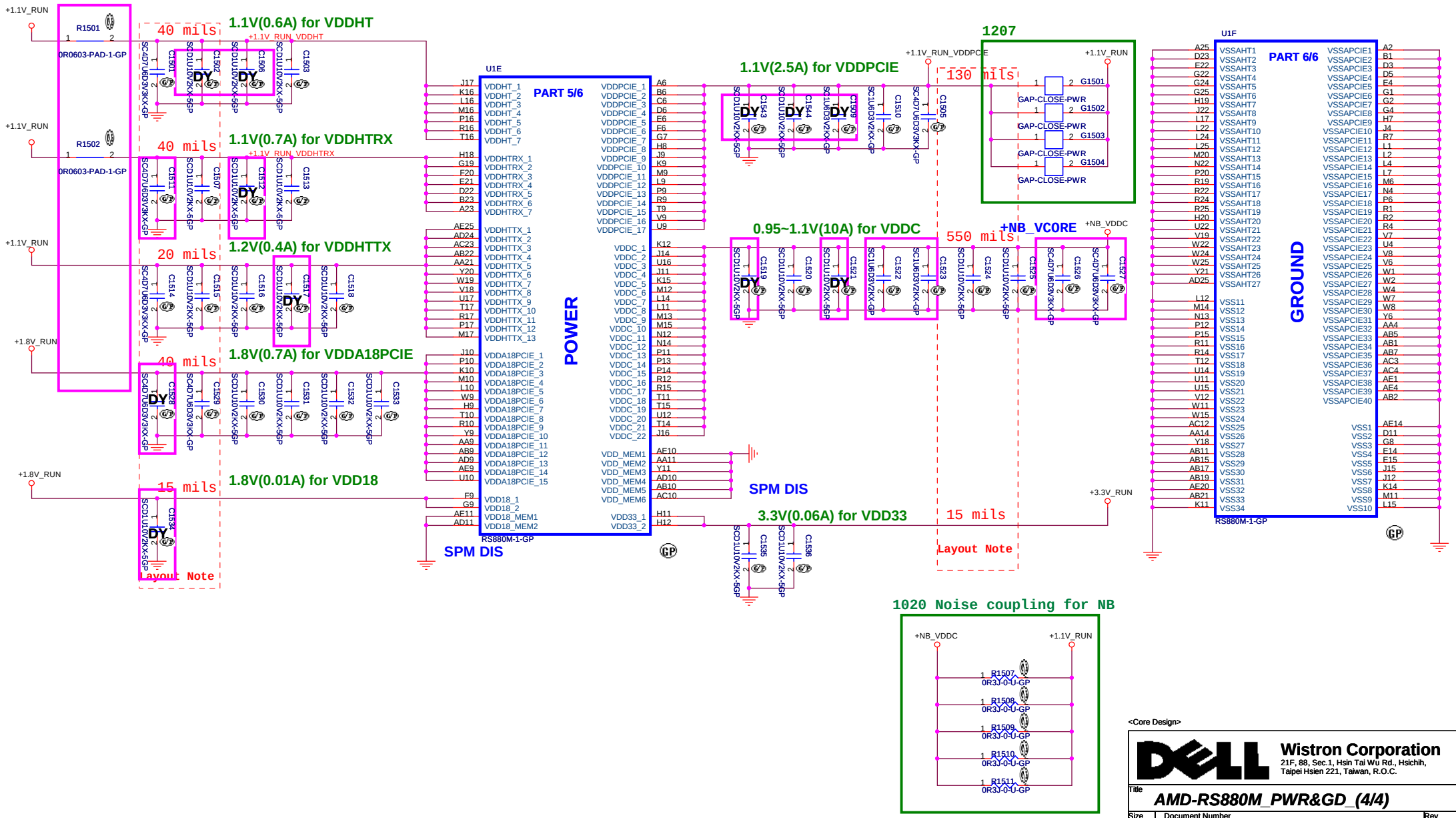
SSID = N.B



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Title: AMD-RS880M_PWR&GD_(4/4)

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Title: Reserved

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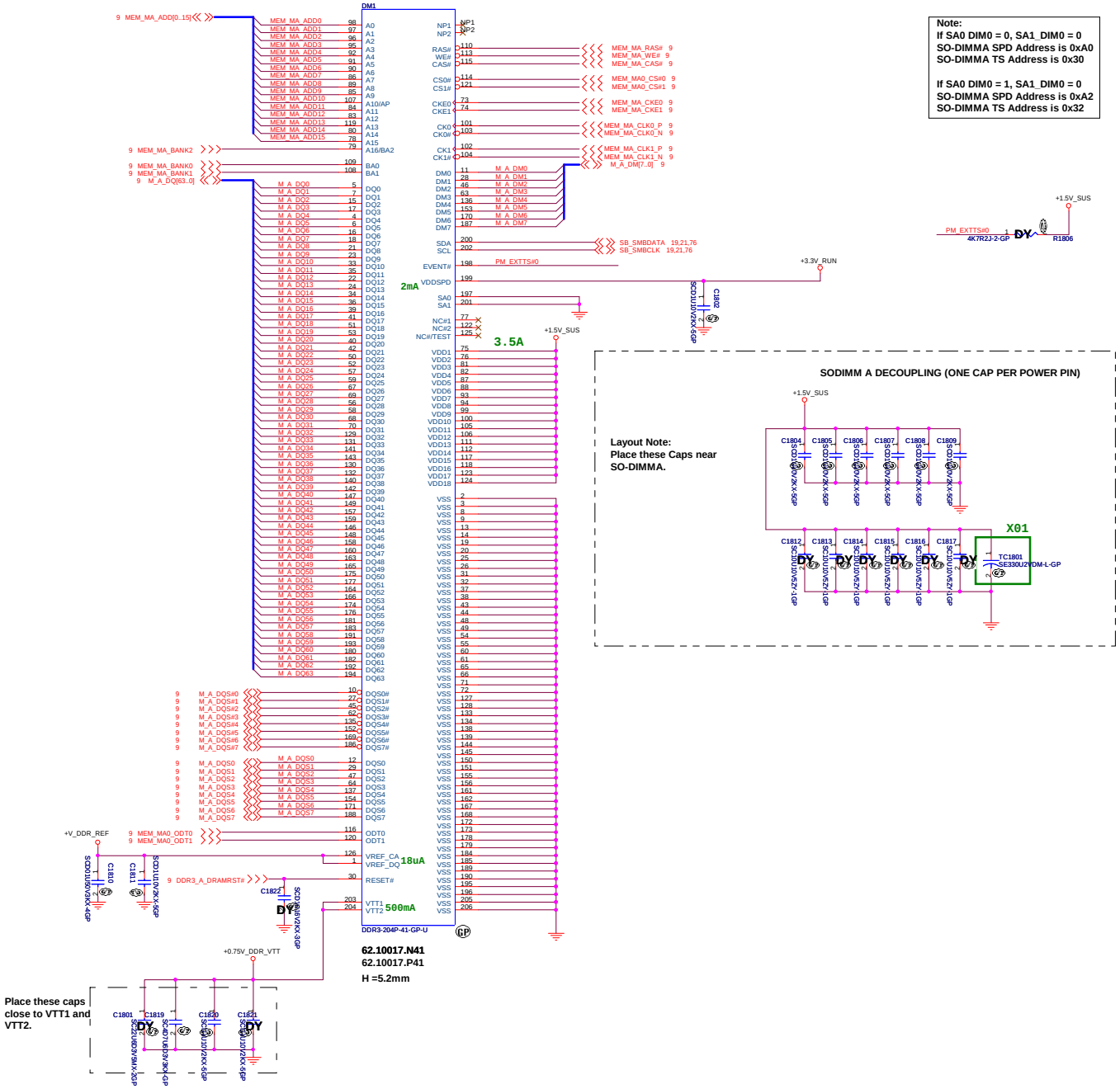

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Title: DDR3-SODIMM1

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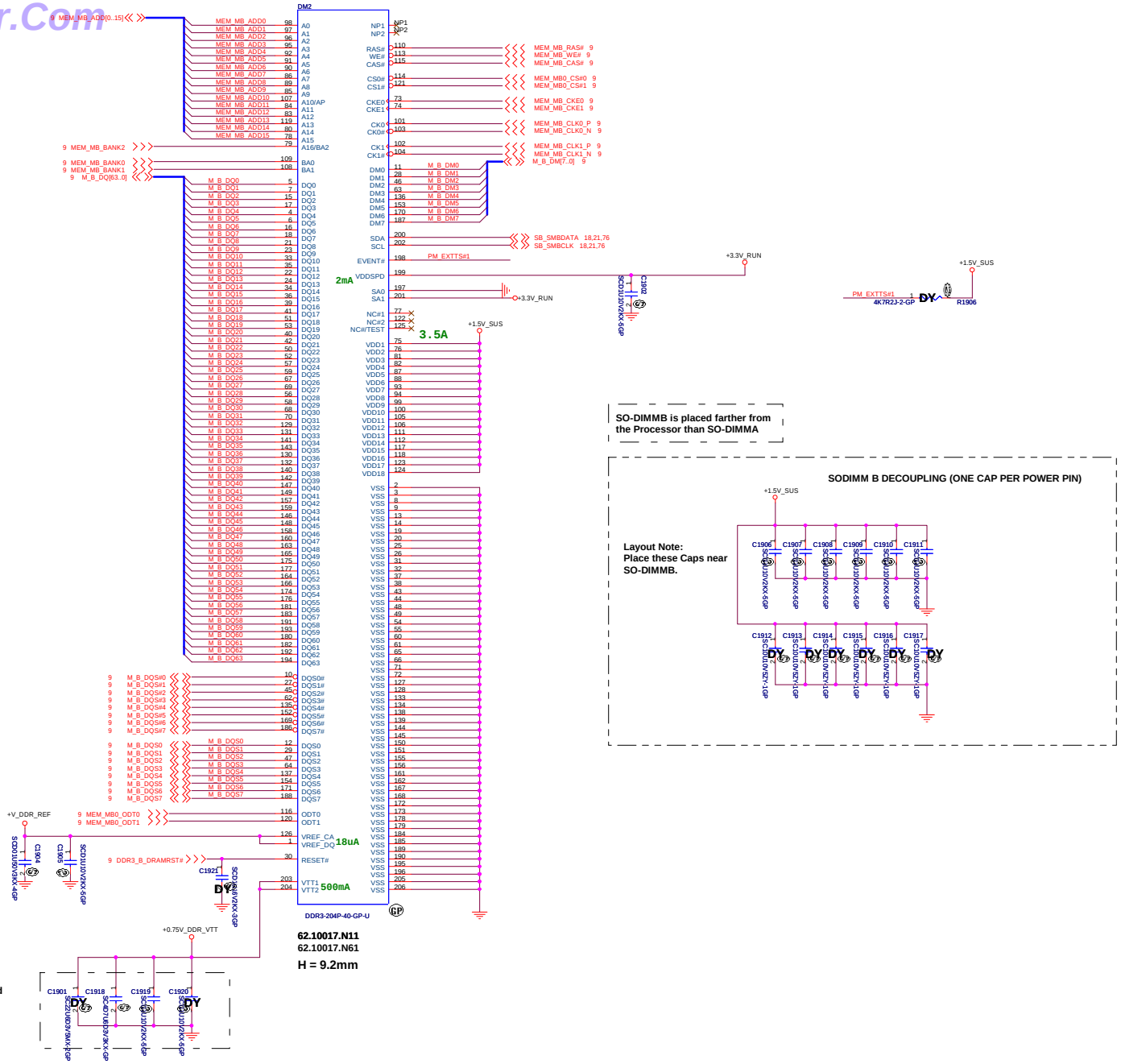

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Title: **DDR3-SODIMM2**

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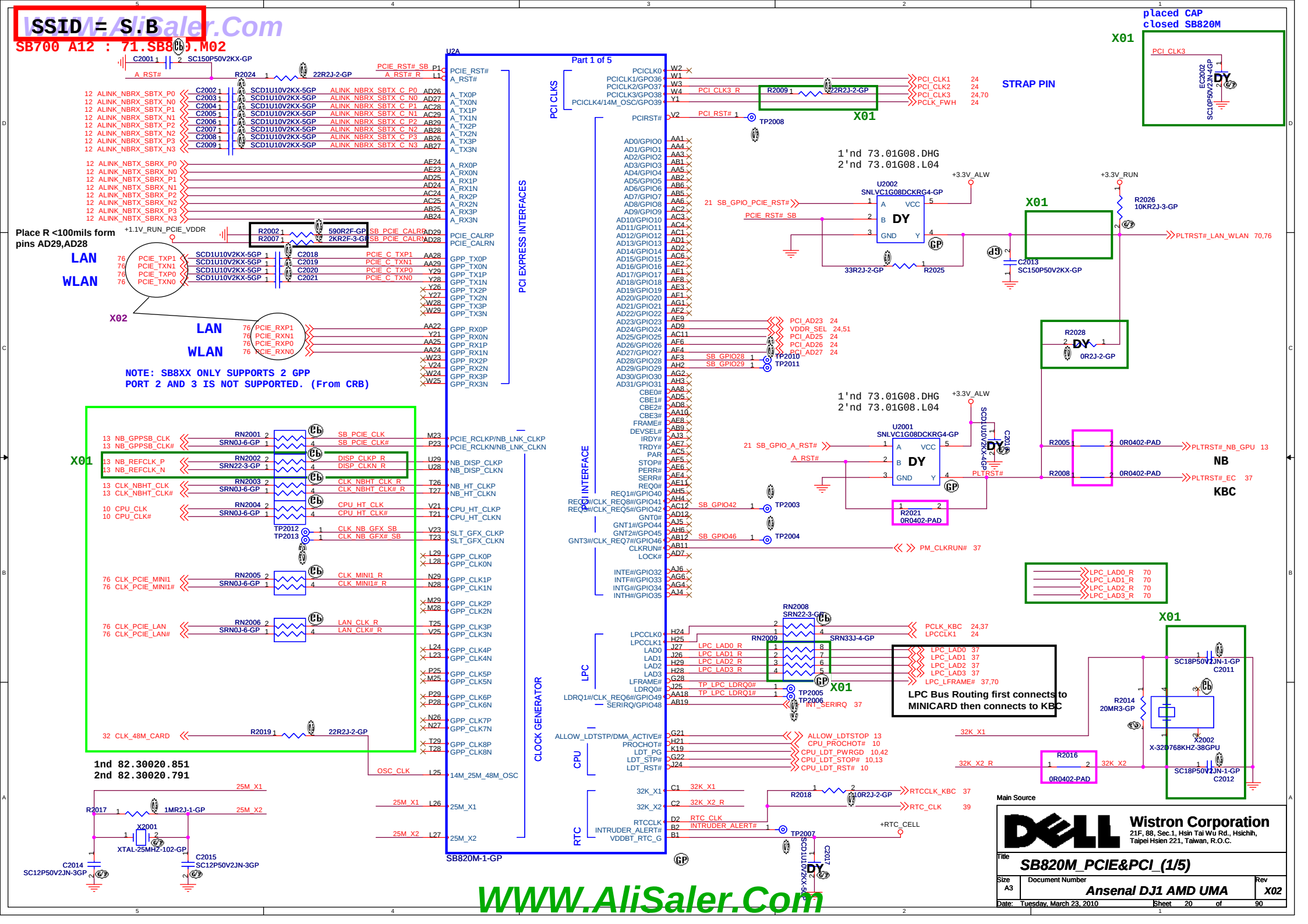
SSID = S.B
SB700 A12 : 71.SB8J0.M02
placed CAP closed SB820M
STRAP PIN
Part 1 of 5
U2A
SB820M-1-GP
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
Place R <100mils form pins AD29,AD28
LAN
WLAN
X01
X02
NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)
1'nd 73.01G08.DHG
2'nd 73.01G08.L04
1nd 82.30020.851
2nd 82.30020.791
LPC Bus Routing first connects to MINICARD then connects to KBC
NB
KBC
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SB820M_PCIE&PCI_(1/5)
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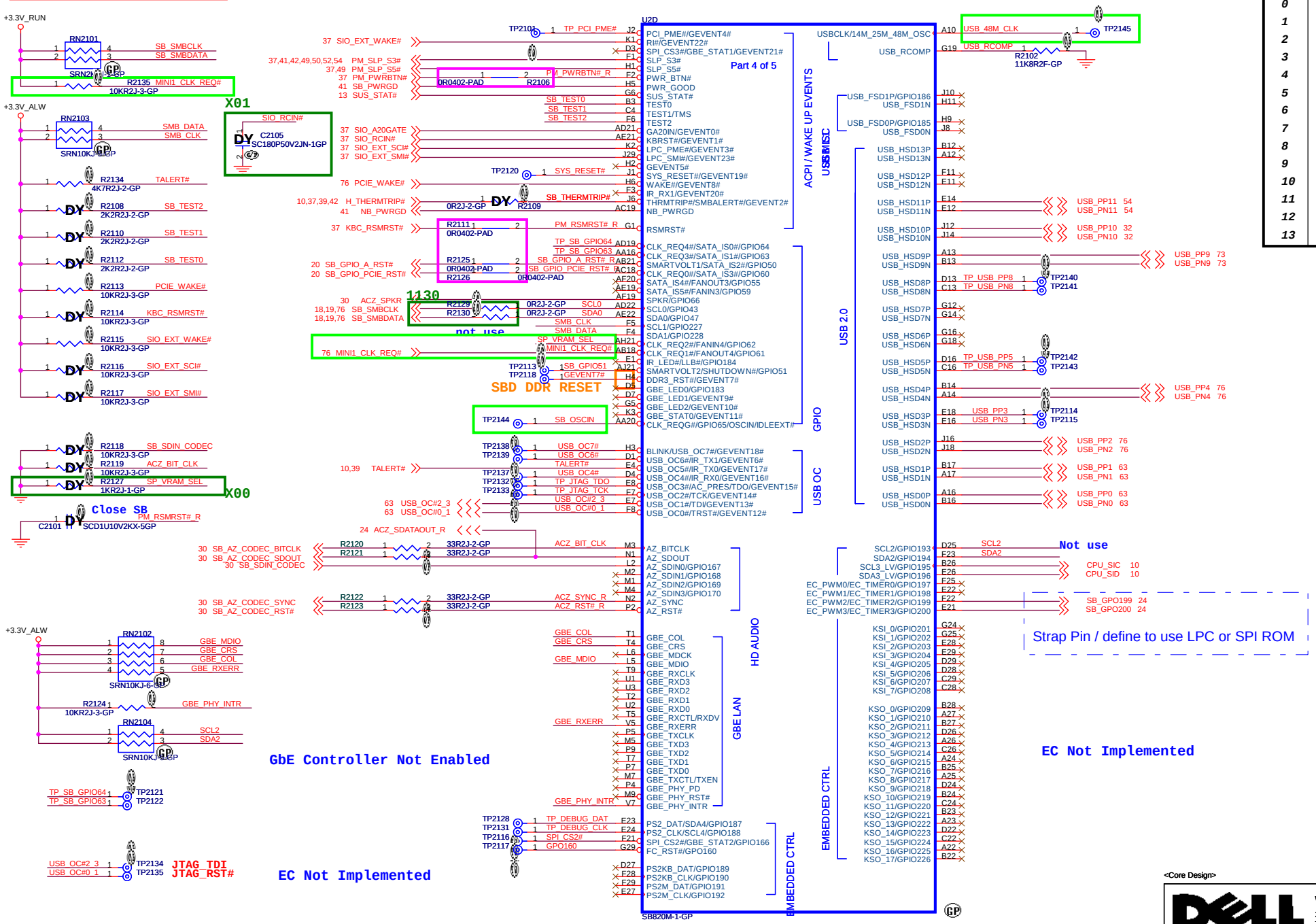
SSID = S.B

USB	
Pair	Device
0	USB1
1	USB3
2	USB2 (I/O Board)
3	RESERVED
4	WLAN
5	RESERVED
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	RESERVED
13	RESERVED



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Title: SB820M_USB&GPIO_(2/5)

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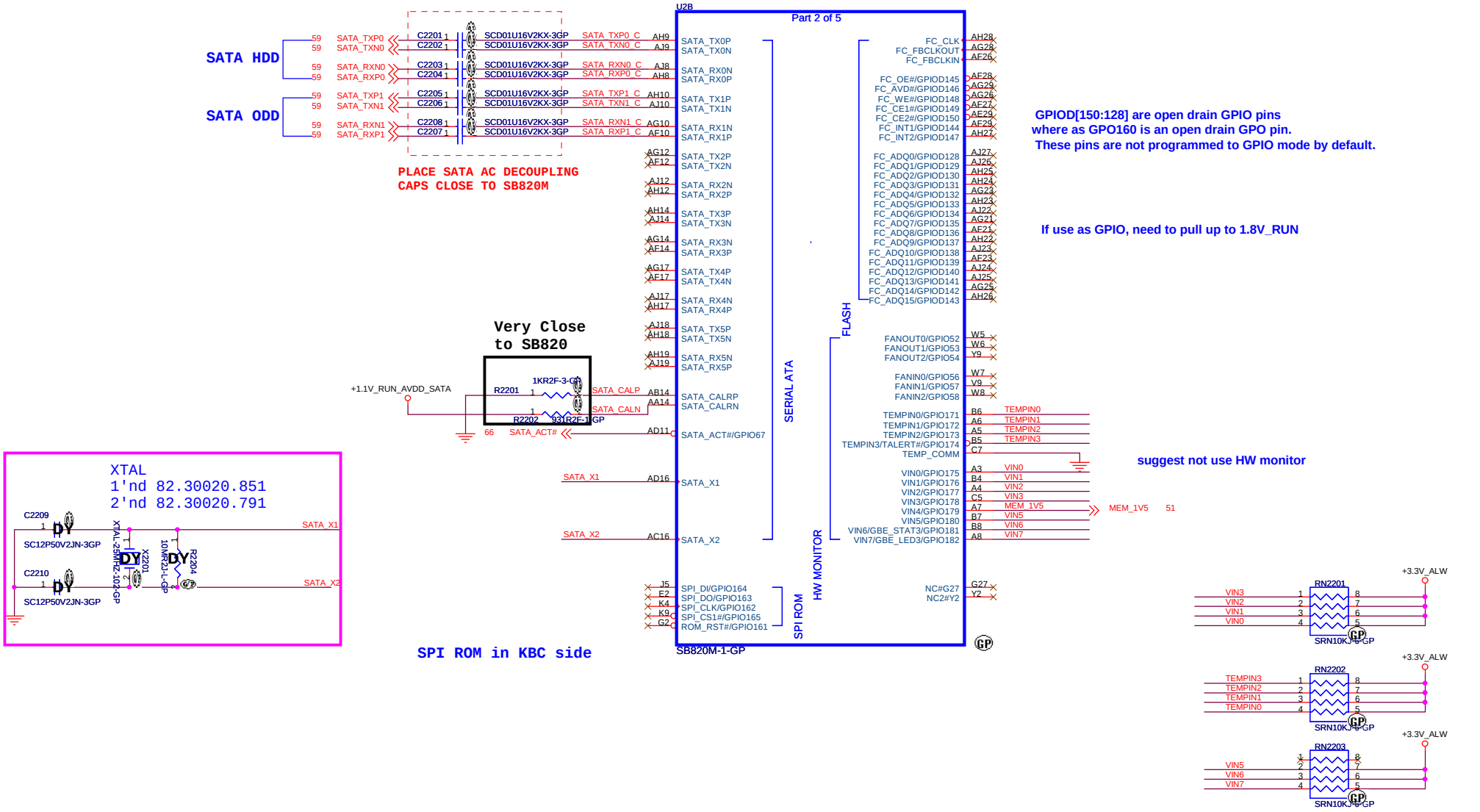
SSID = S.B



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Title: SB820M_SATA-IDE_(3/5)

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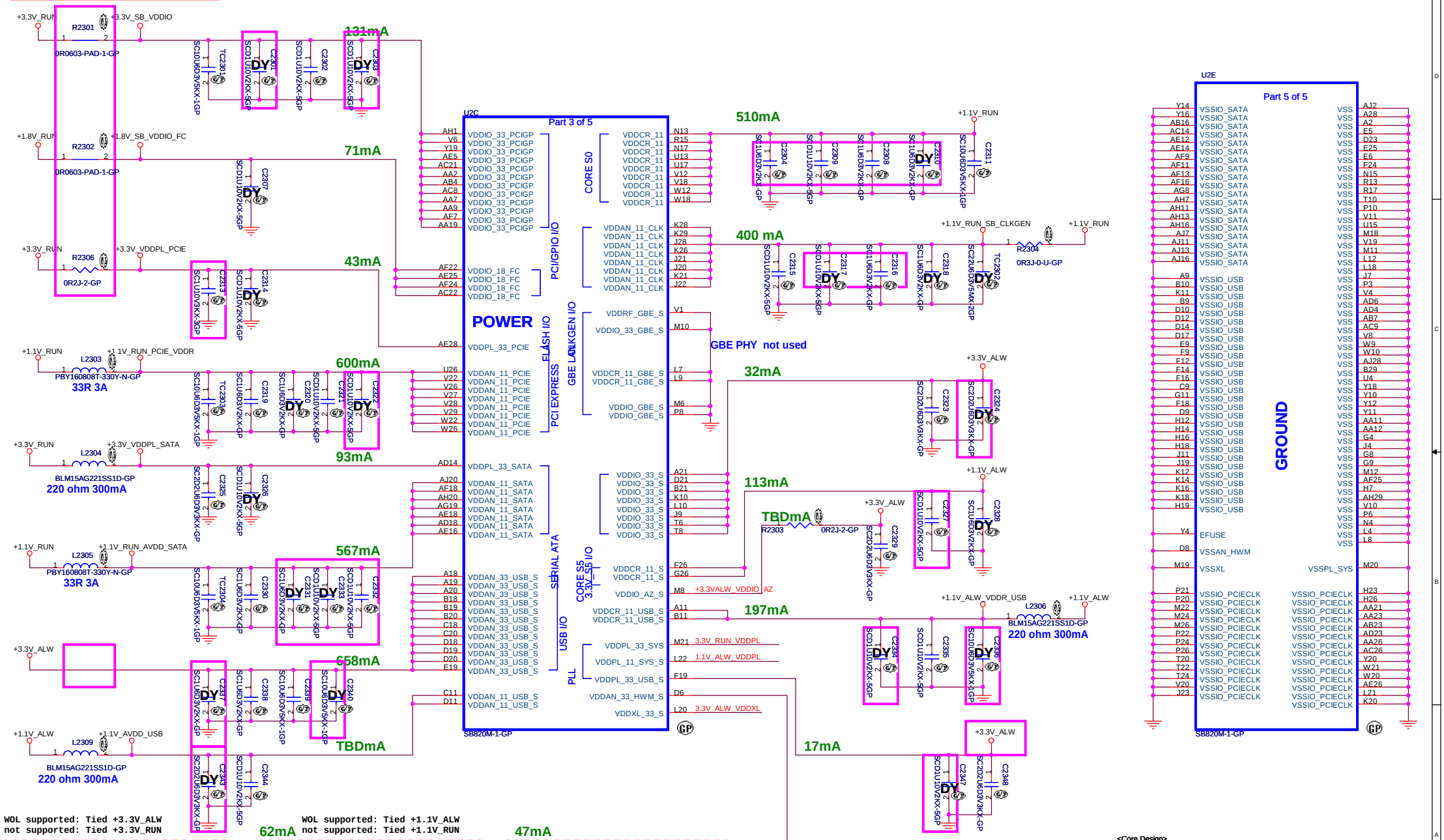
SSID = S.B



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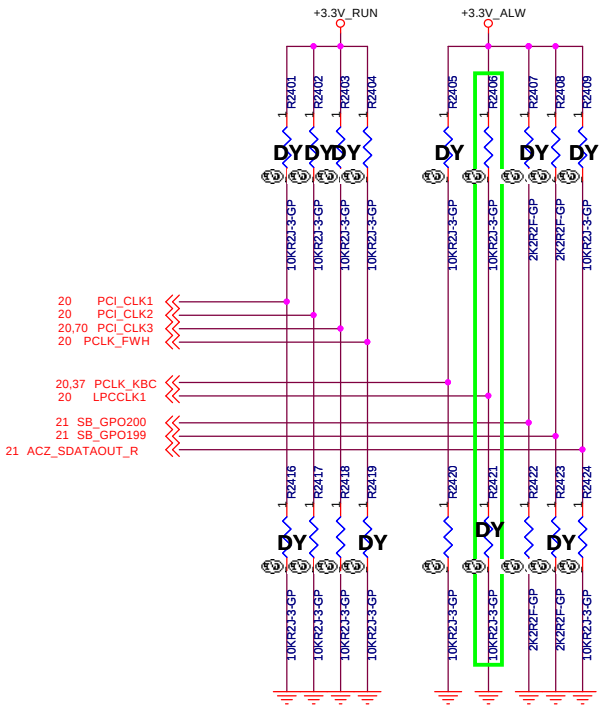
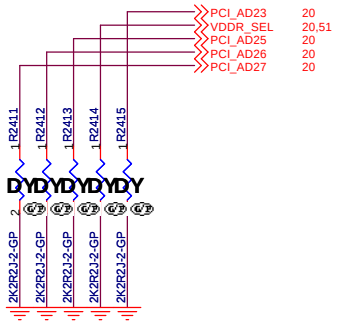
SSID = S.B

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCLK_FWH (PCI_CLK4)	PCLK_KBC (LPCCLK0)	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	DEFAULT CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

Not Applicable to SB820M
but provision for pull-down is required.

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

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Title: SB820M_STRAPPING_(5/5)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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<Core Design>

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Title: CPU (VCC_CORE)

Size | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Tuesday, March 23, 2010 | Sheet 25 of 90

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Title: CPU (VCC_GFXCORE)

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Title: CPU (VSS)

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Title: Reserved

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Title: Reserved

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	X02

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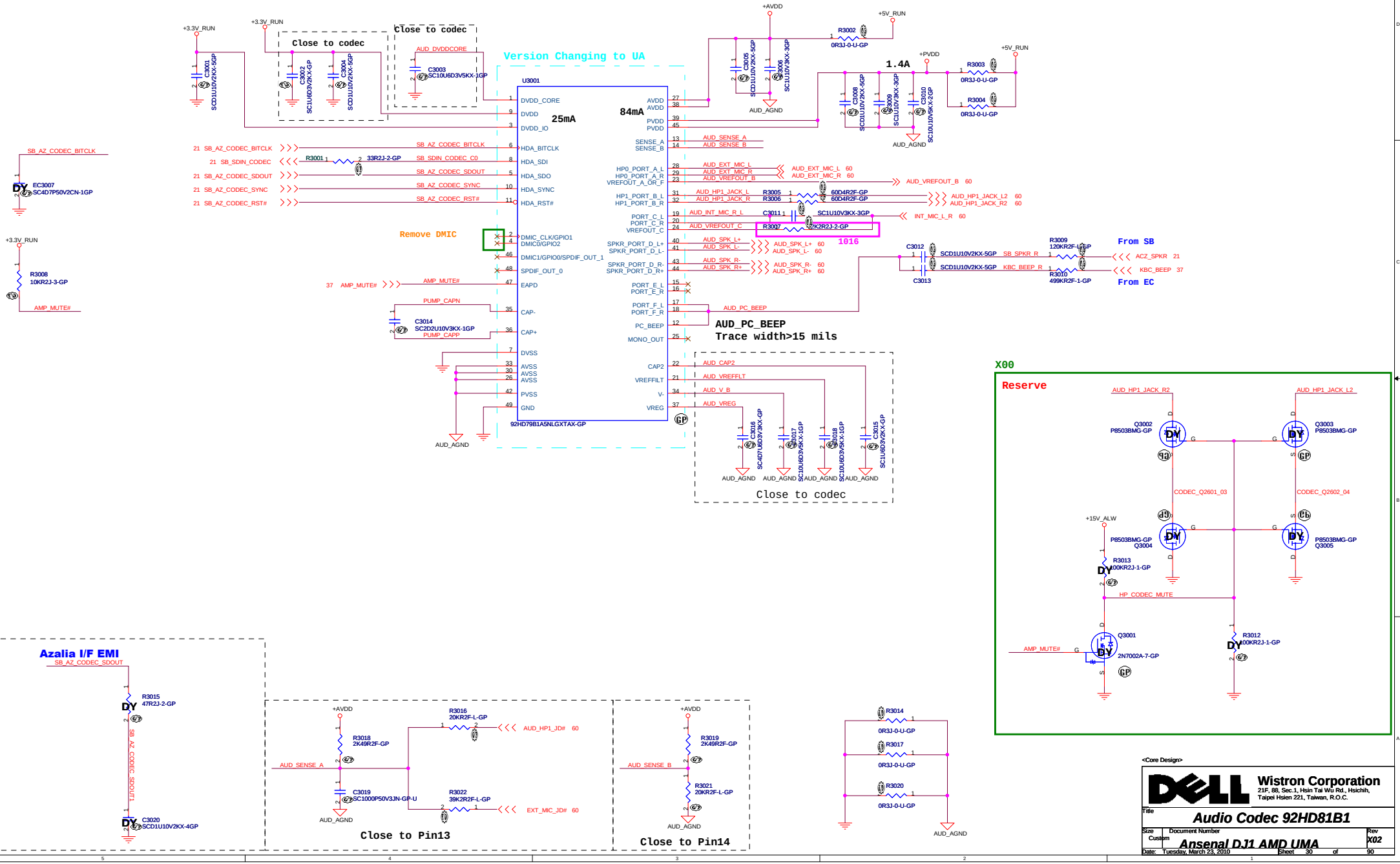
SSID = AUDIO



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<Core Design>

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Title: Audio Codec 92HD81B1

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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Title: Reserved

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	X02

Date: Tuesday, March 23, 2010 Sheet 31 of 90

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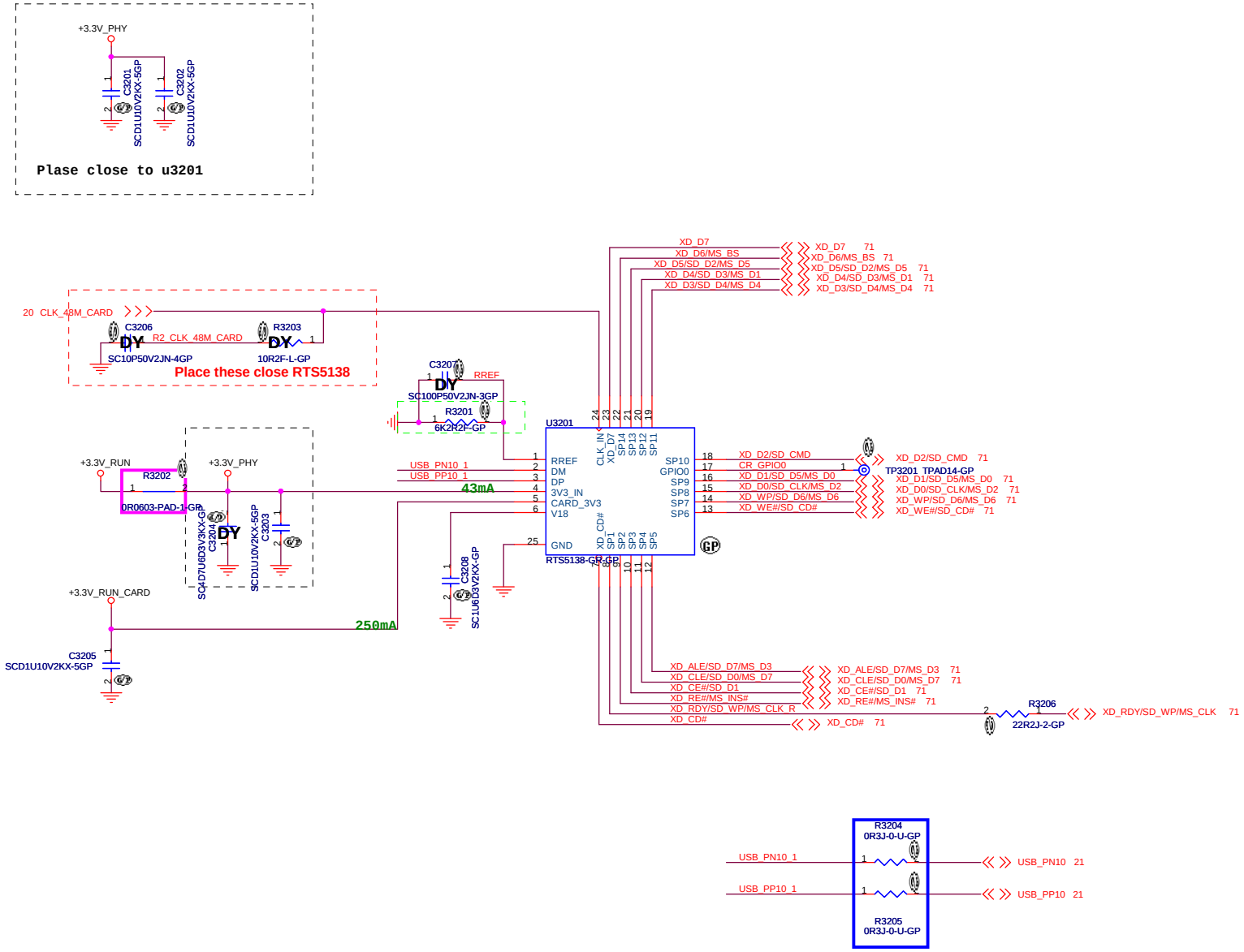
SSID = SDIO



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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Title		
	Reserved	
Size A3	Document Number Ansenal DJ1 AMD UMA	Rev X02
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Title: Reserved

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Title: Reserved

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A3	Ansenal DJ1 AMD UMA	X02

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SSID = KBC

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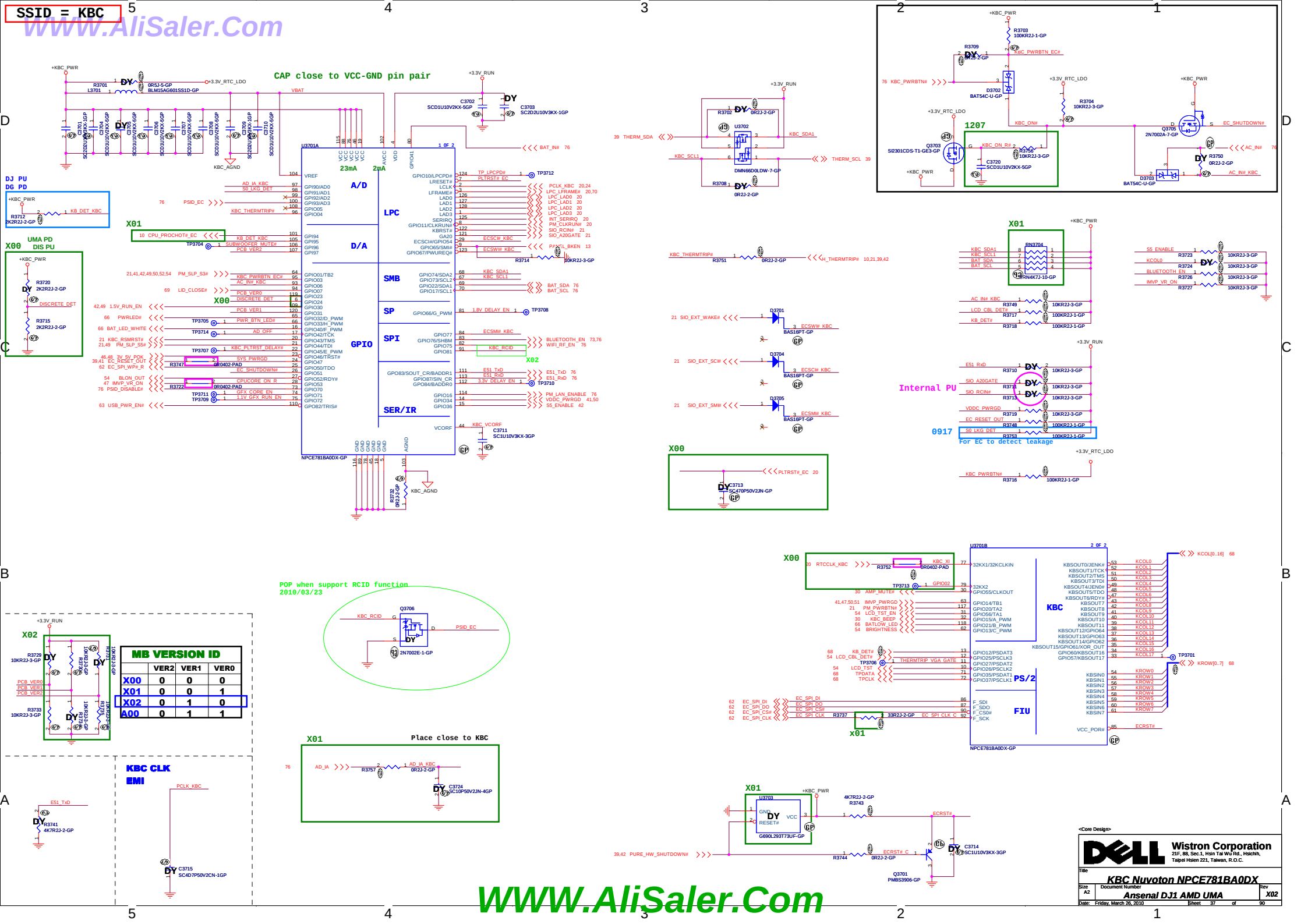

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Title: Reserved

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A3	Ansenal DJ1 AMD UMA	X02

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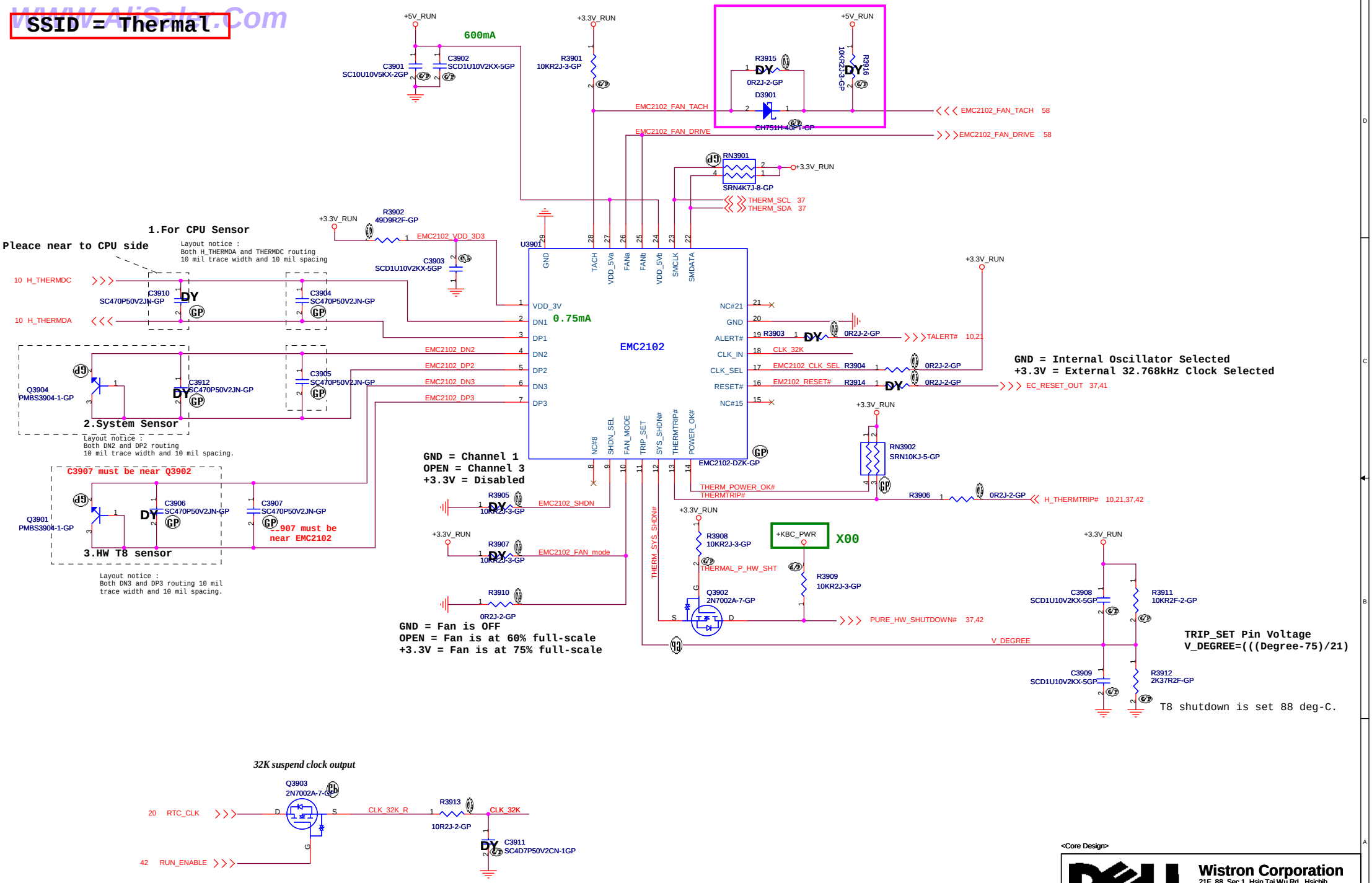
SSID = Thermal



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Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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Title: Reserved

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A3	Ansenal DJ1 AMD UMA	X02

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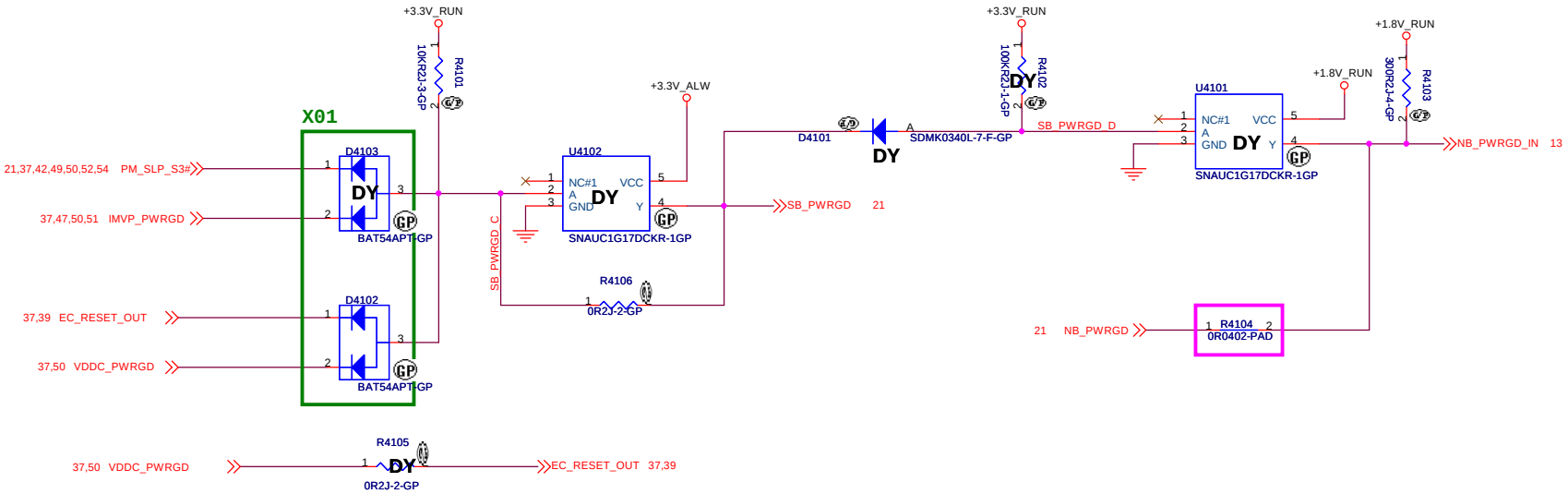
SSID = Reset.Suspend



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<Core Design>

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Title: ***Power On Logic***

Size	Document Number	Rev
A3	***Ansenal DJ1 AMD UMA***	***X02***

Date: Tuesday, March 23, 2010 Sheet 41 of 90

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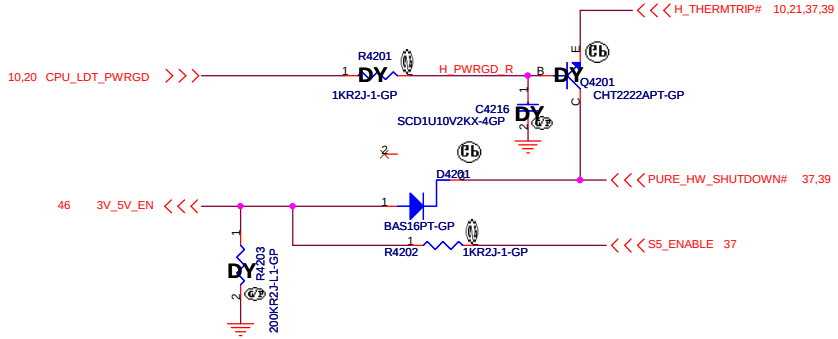
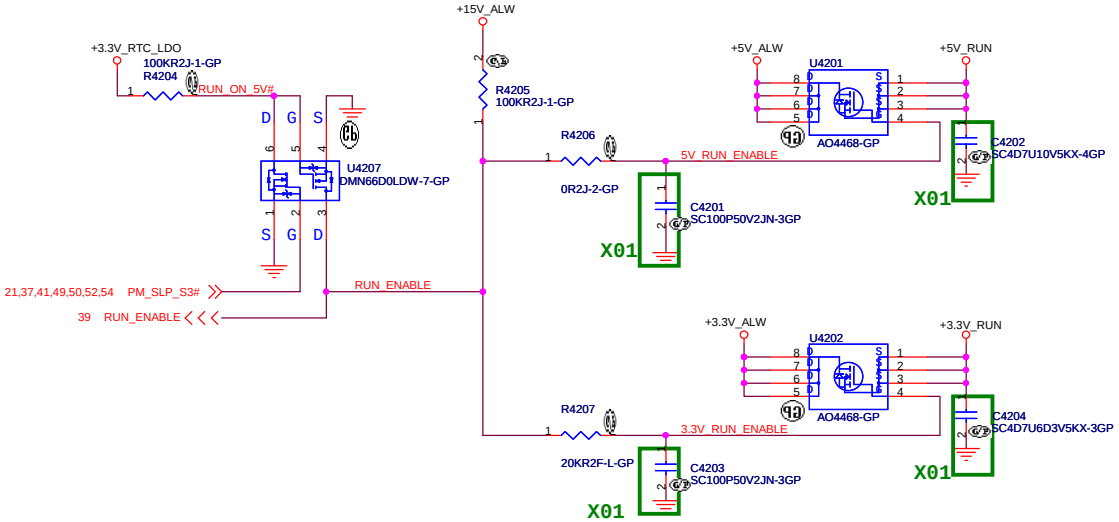
SSID = Reset.Suspend

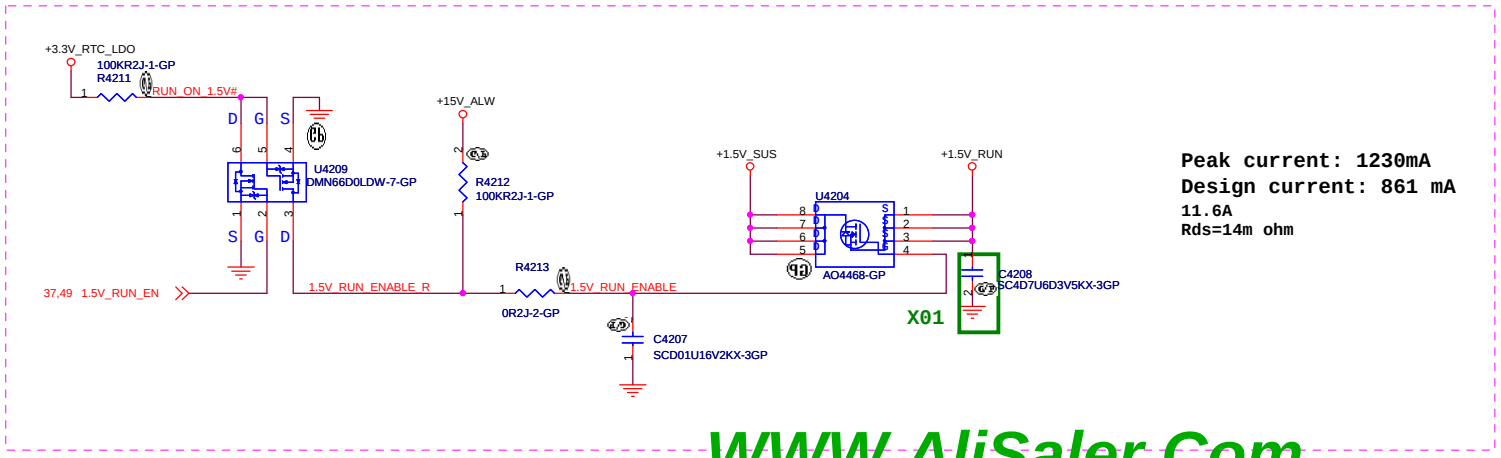


Run Power

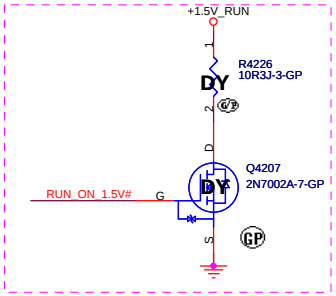


Peak current: 6257.3mA (HD:1100 ODD:2500)
Design current: 4380.11 mA
11.6A
Rds=14m ohm

Peak current: 5966mA
Design current: 4177 mA
11.6A
Rds=14m ohm



Peak current: 1230mA
Design current: 861 mA
11.6A
Rds=14m ohm



<Core Design>

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Title: Power Plane Enable

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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Title: Reserved

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Title: Reserved

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Title: Reserved

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	X02

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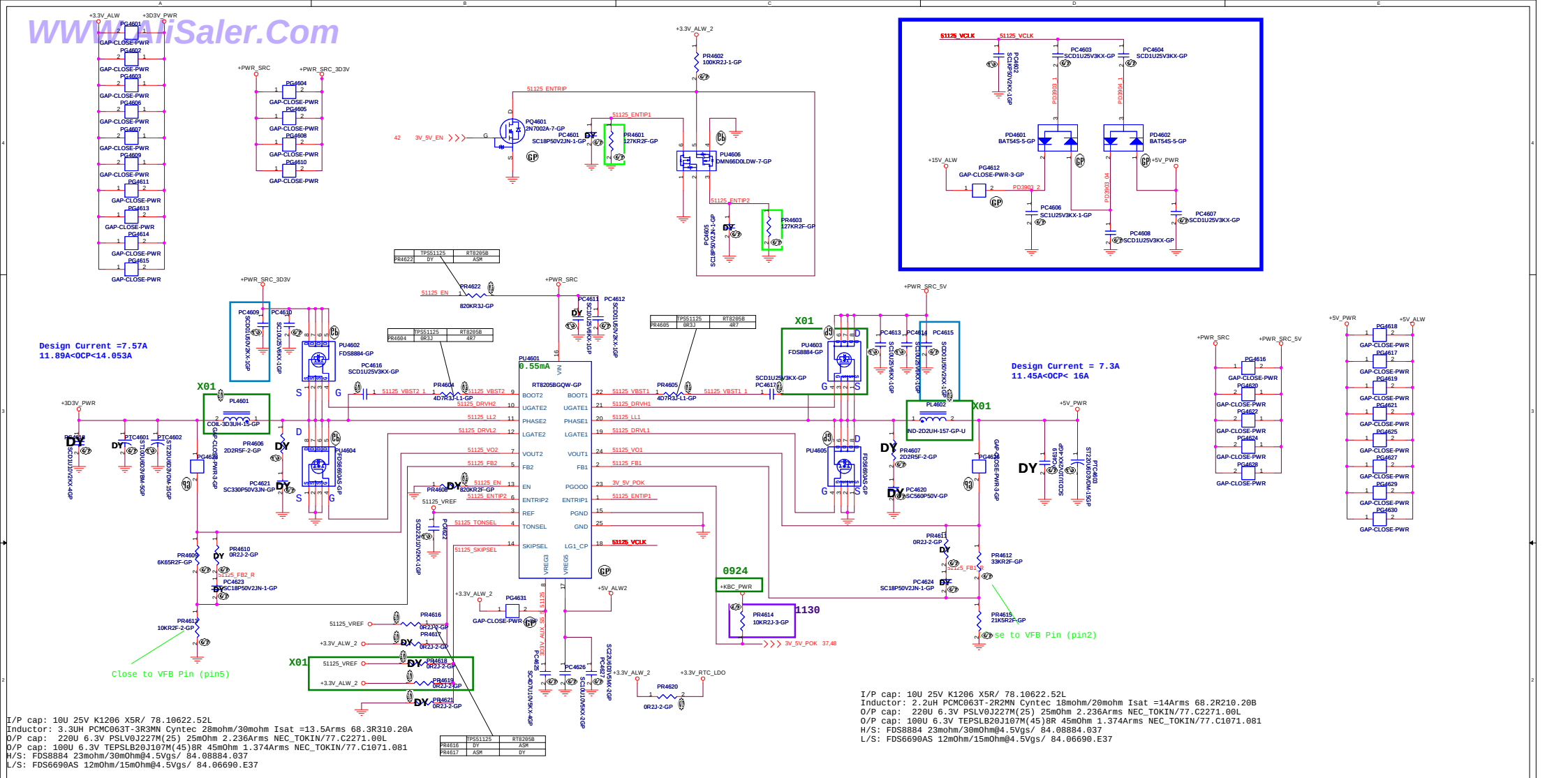

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS 12mOhm/15mOhm@4.5Vgs/ 84.06690.E37

RT8205B(74.08208.A73):

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B(74.08205.B73):

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8205BGQW	74.08205.B73

<Core Design>

Wistron Corporation
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Title: RT8205B_5V/3D3V

Size: A2 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Tuesday, March 23, 2010 | Sheet 46 of 90

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SSID = CPU.Regulator

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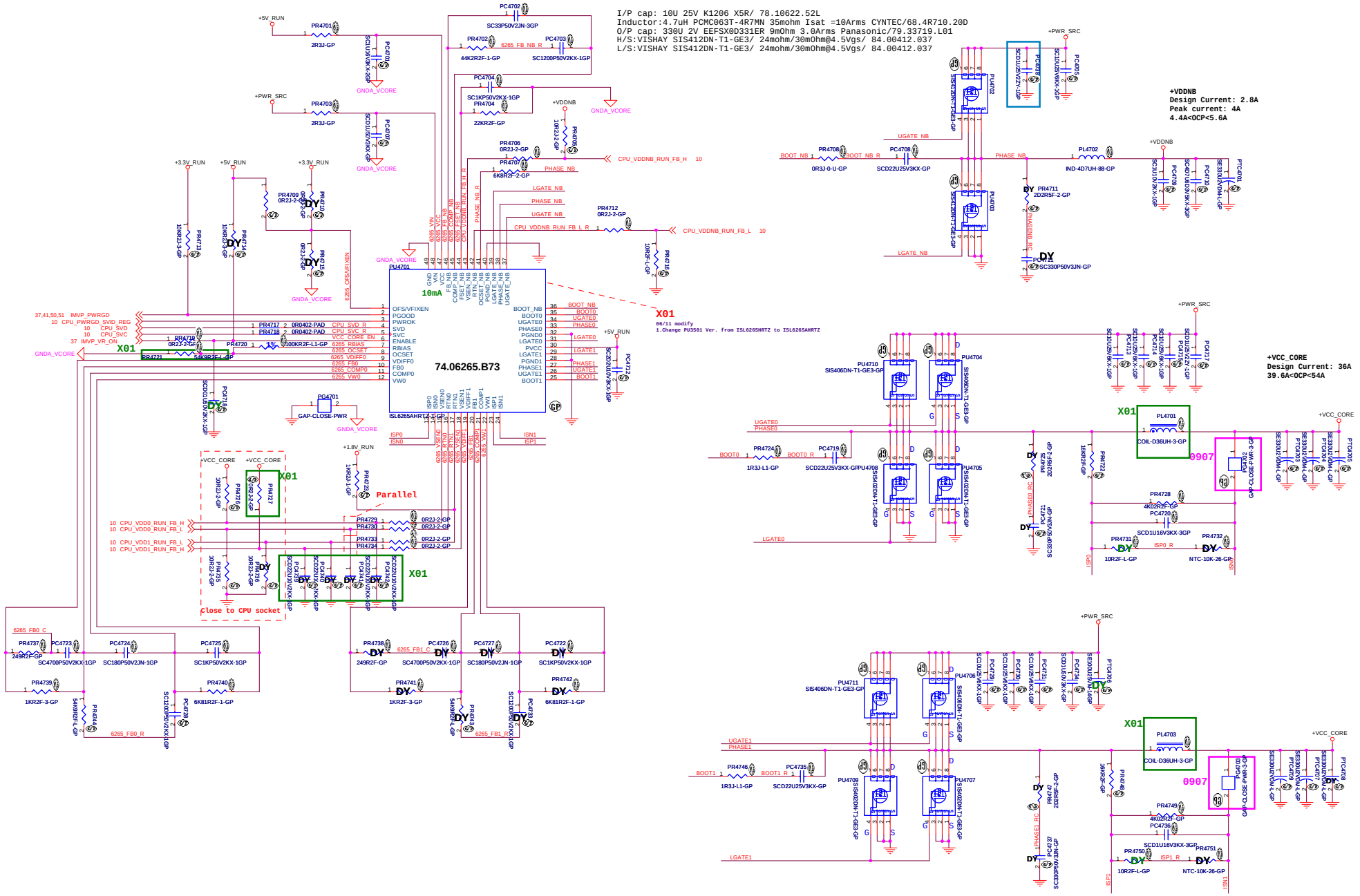
ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

+VDDNB
Design Current: 2.8A
Peak current: 4A
4.4A<OCP<5.6A

+VCC_CORE
Design Current: 36A
39.6A<OCP<54A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

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<Core Design>

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Title: VREG : +VCC_CORE&+VDDNB

Size	Document Number	Rev
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Date: Tuesday, March 23, 2010 Sheet 47 of 90

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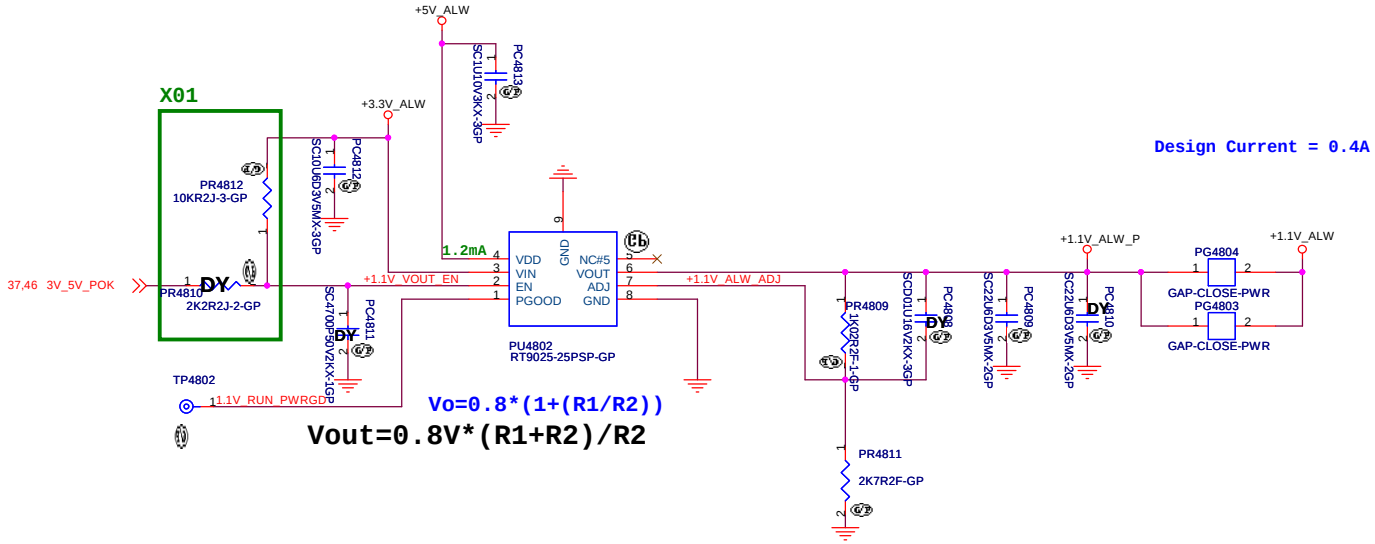
SSID = PWR.Plane.Regulator_+1.1V_RUN

RT9025 for +1.1V_ALW



<Core Design>

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Title: *RT9025_+1.1VALW*

Size: A3 | Document Number: **Ansenal DJ1 AMD UMA** | Rev: *X02*

Date: Tuesday, March 23, 2010 | Sheet 48 of 90

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SSID = PWR.Plane.Regulator_1p5v0p75v

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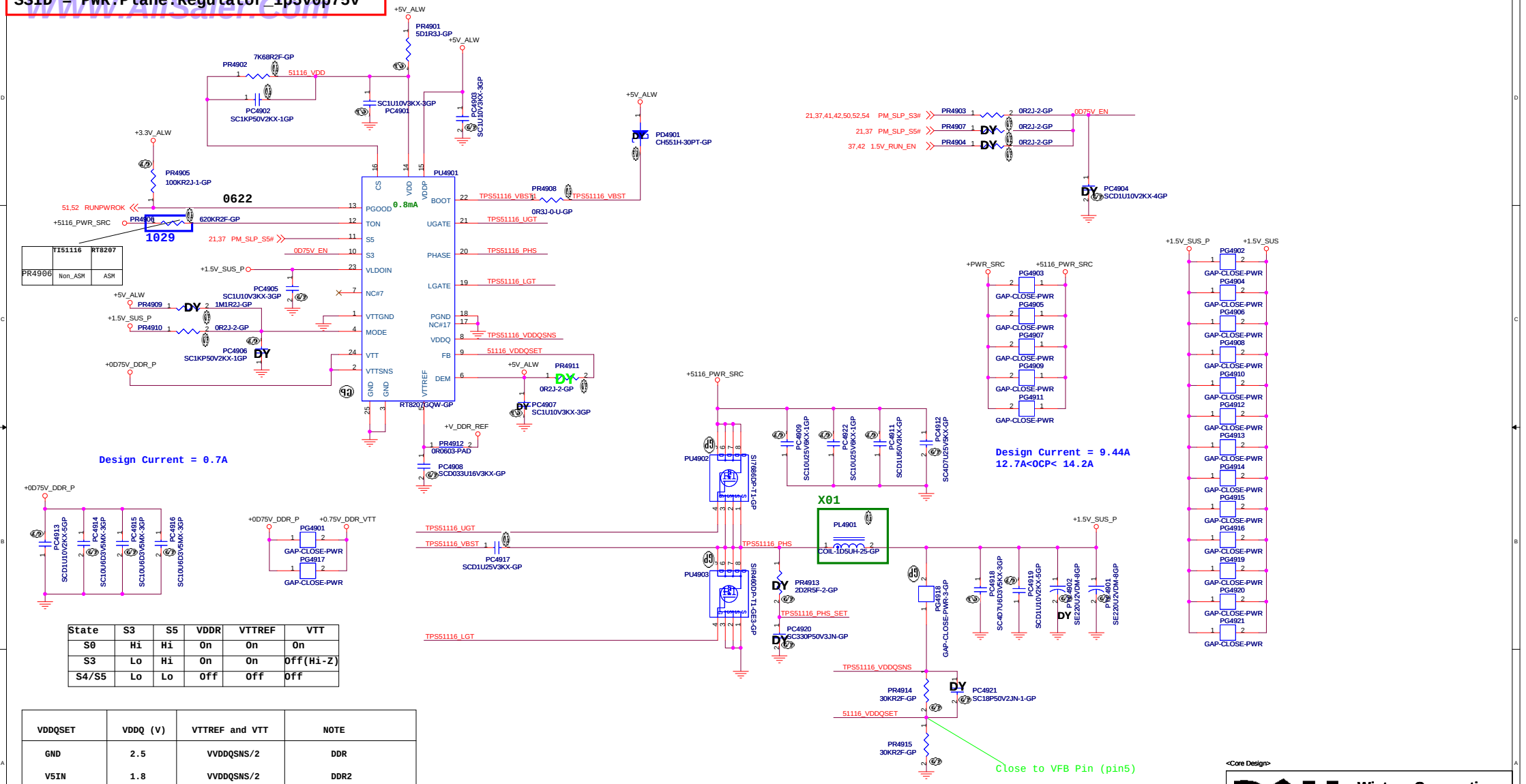

	TI51116	RT8207
PR4906	Non_ASM	ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

<Core Design>

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Title: RT8207GQW_+1.5V_SUS

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Tuesday, March 23, 2010 | Sheet 49 of 90

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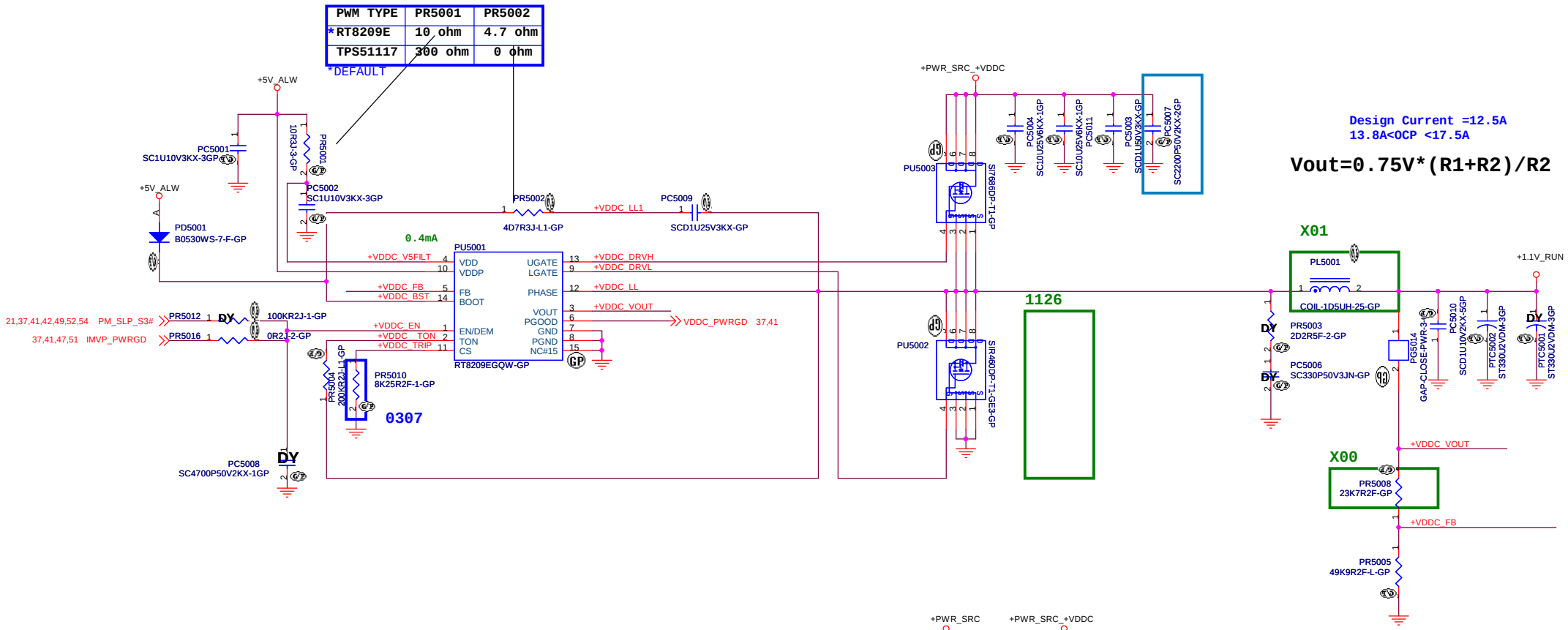
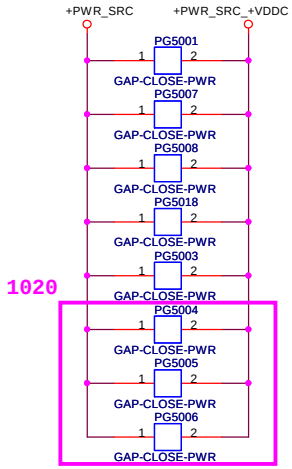
SSID = PWR.Plane.Regulator_VDDC

PWM TYPE	PR5001	PR5002
*RT8209E	10 ohm	4.7 ohm
TPS51117	300 ohm	0 ohm

*DEFAULT





I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209 +1.1V RUN

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Friday, March 26, 2010 | Sheet 50 of 90

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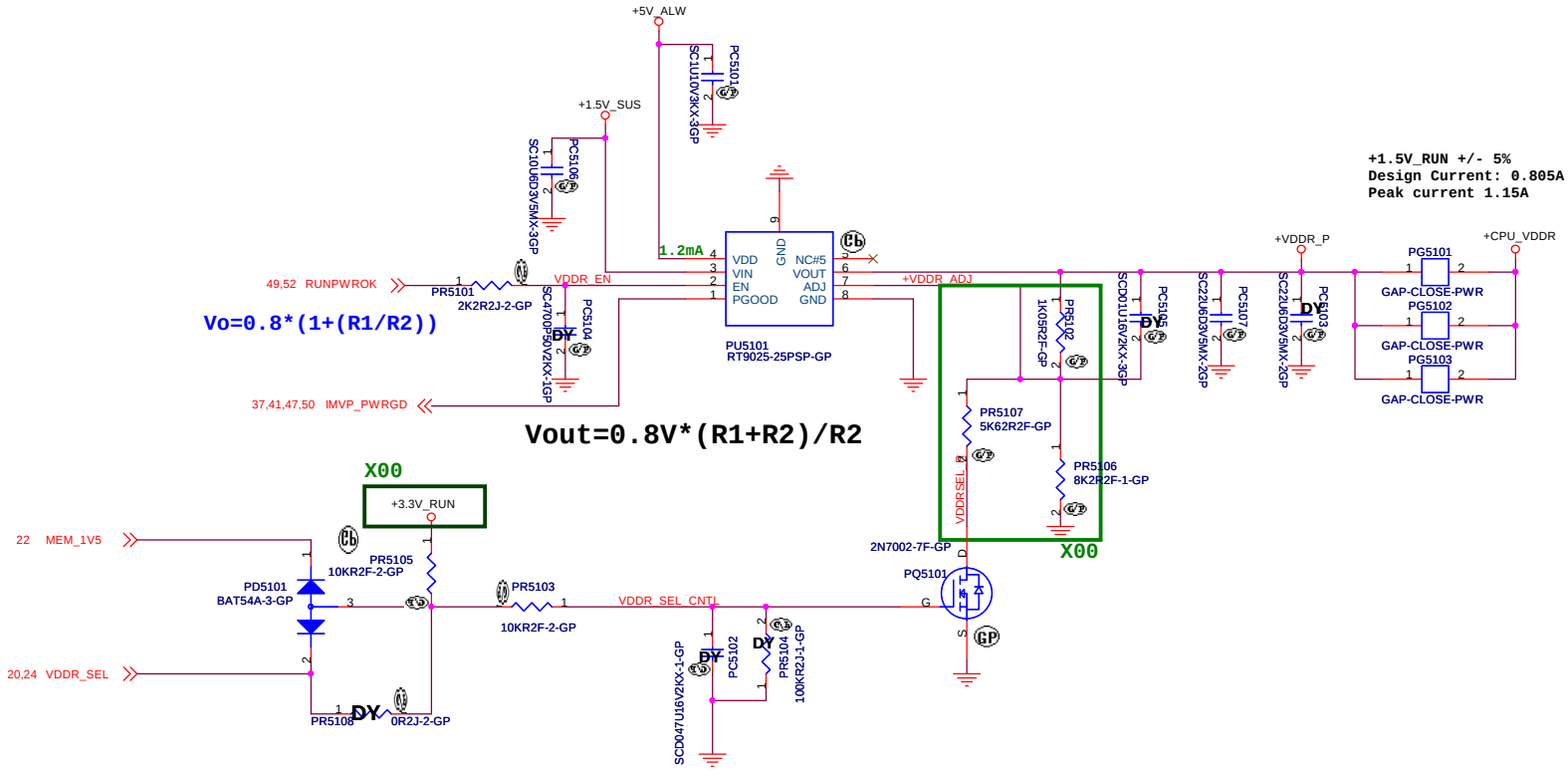
SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *RT9025 +VDDR*

Size: A3 | Document Number: *Ansenal DJ1 AMD UMA* | Rev: *X02*

Date: Tuesday, March 23, 2010 | Sheet 51 of 90

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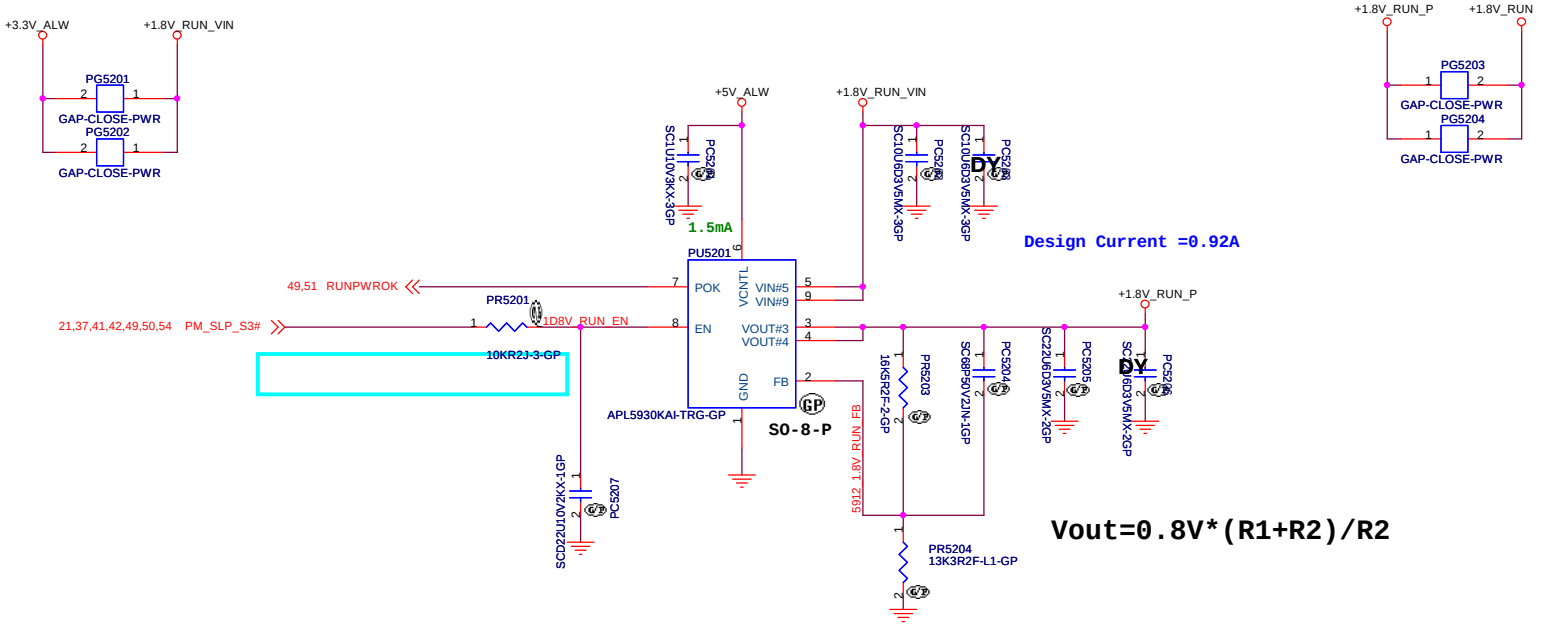
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930 +1.8V RUN

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Tuesday, March 23, 2010 | Sheet 52 of 90

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SSID = PWR.Plane.Regulator_2p5v

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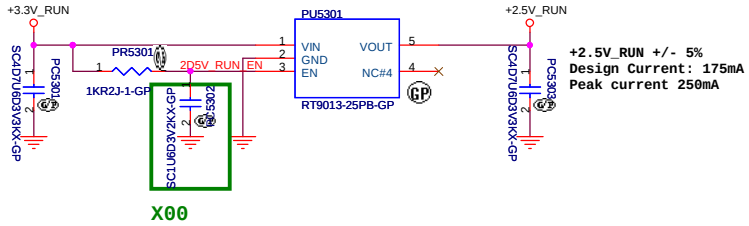
RT9013-25PB for +2.5V_RUN



WWW.AliSaler.Com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +CPU_VDDR&+2.5V_RUN

Size: Custom | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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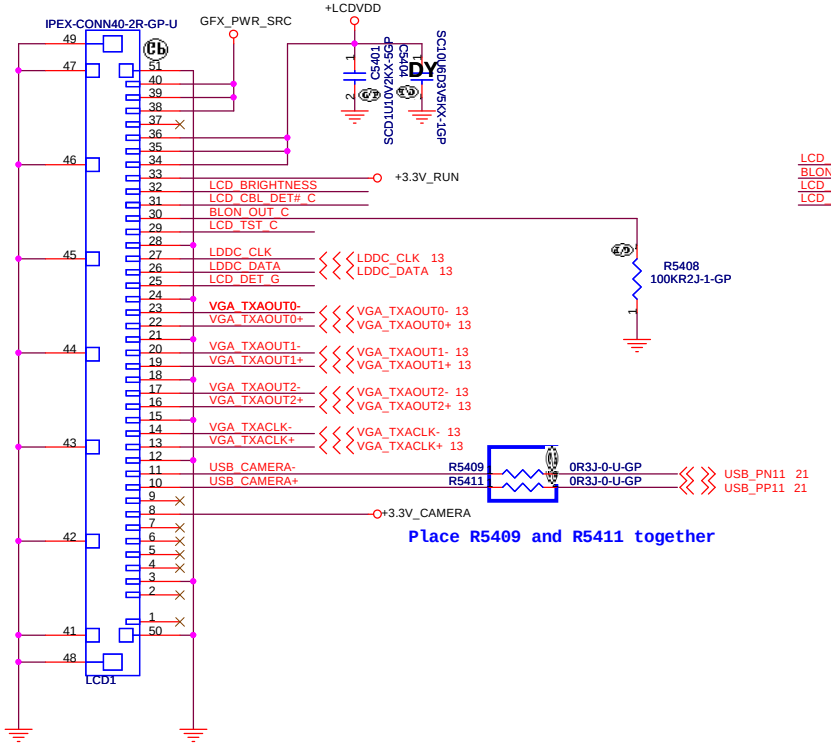
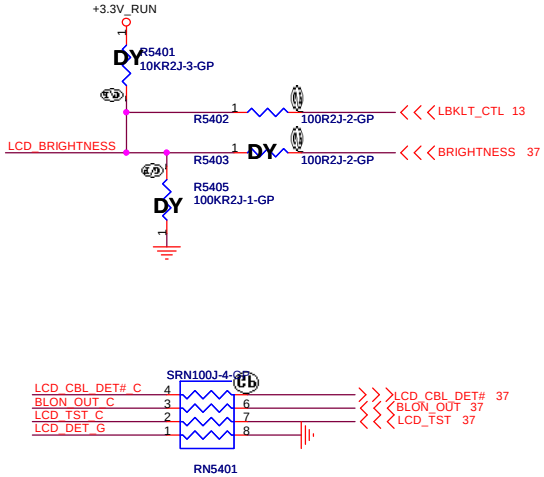
SSID = VIDEO

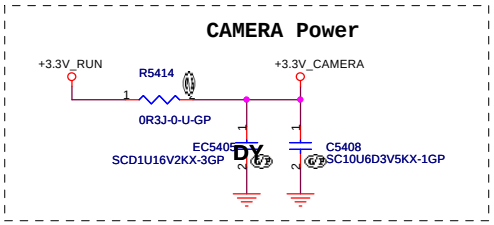
LVDS CONNECTOR

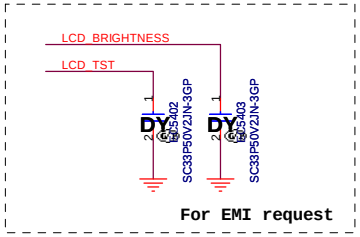


Place R5409 and R5411 together



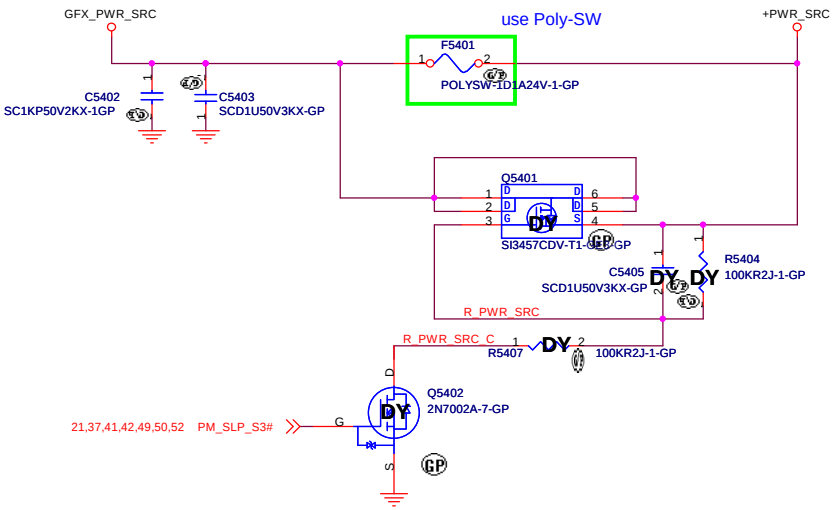
20.F1093.040
20.F1289.040





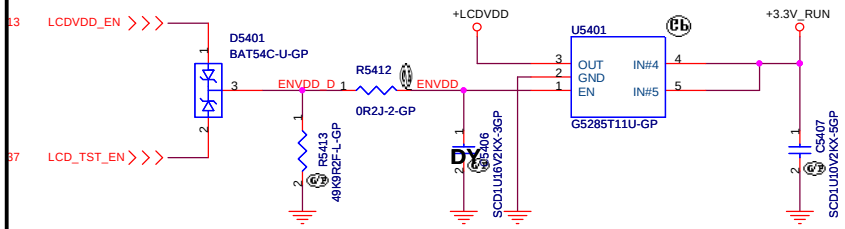
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



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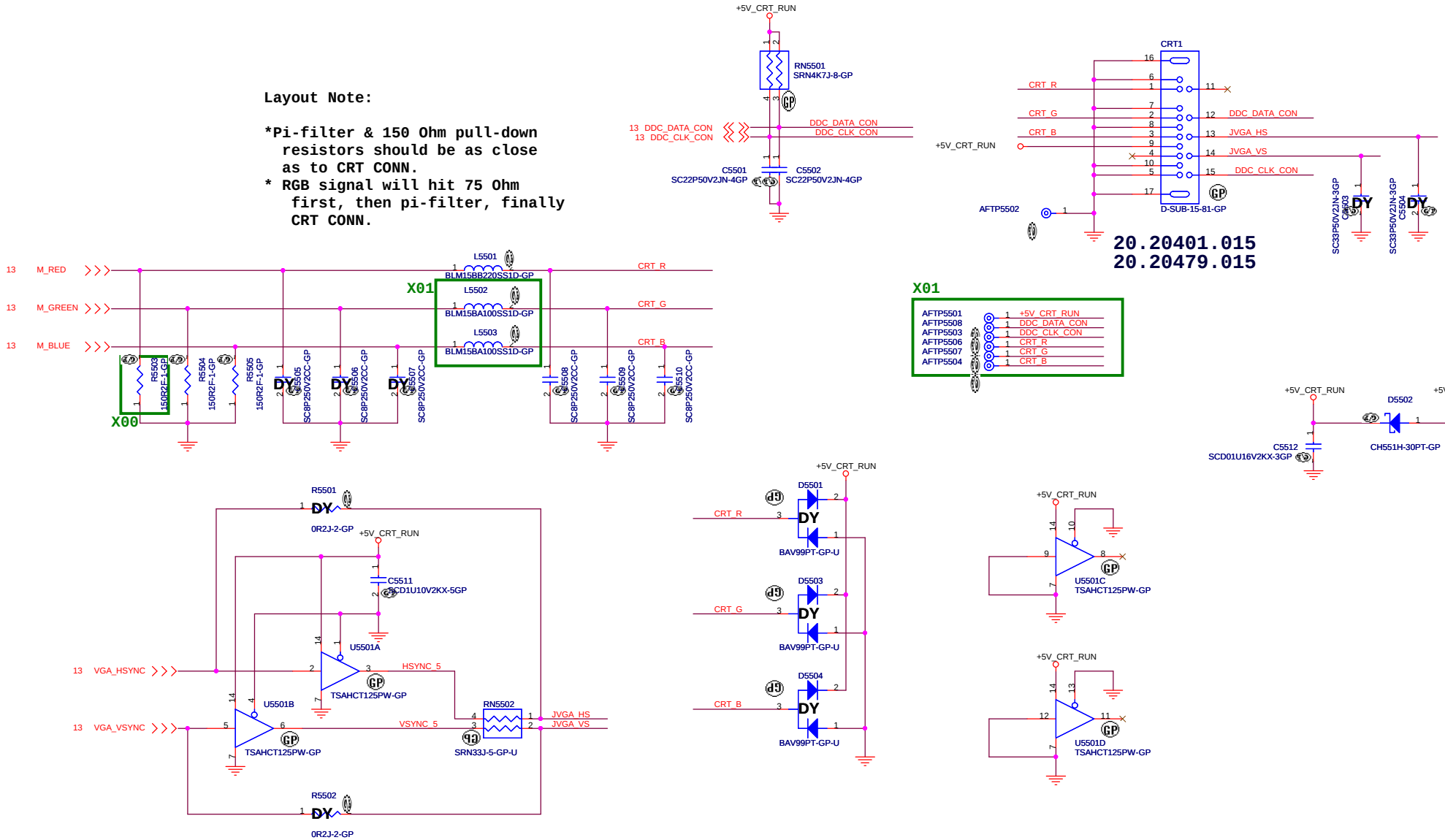
SSID = VIDEO

Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



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Title: CRT Connector

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Title: Reserved

Size	Document Number	Rev
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Title: HDMI (Reserved)

Size	Document Number	Rev
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SSID = Thermal

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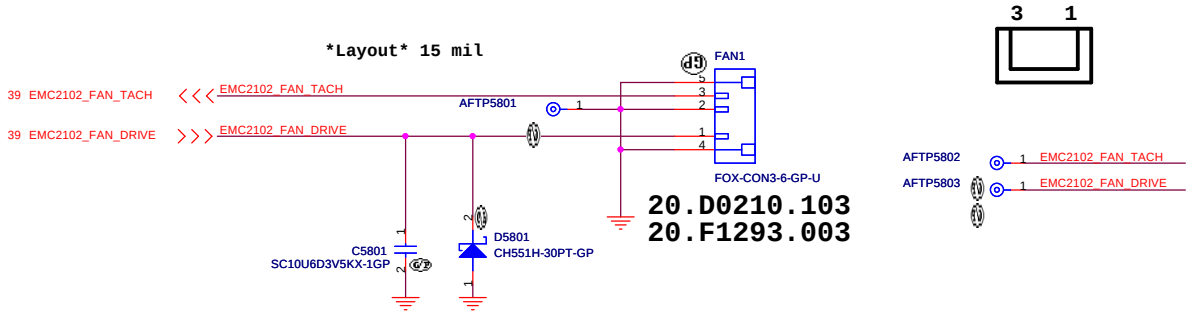
Fan Connector



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<Core Design>

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Title: ITP/Fan Connector

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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SSID = SATA

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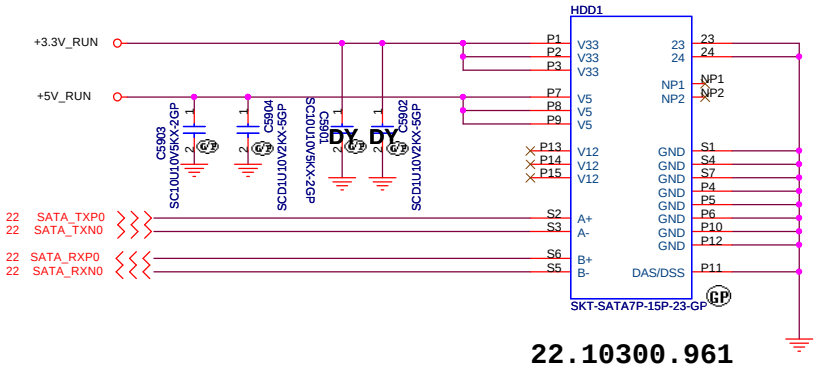
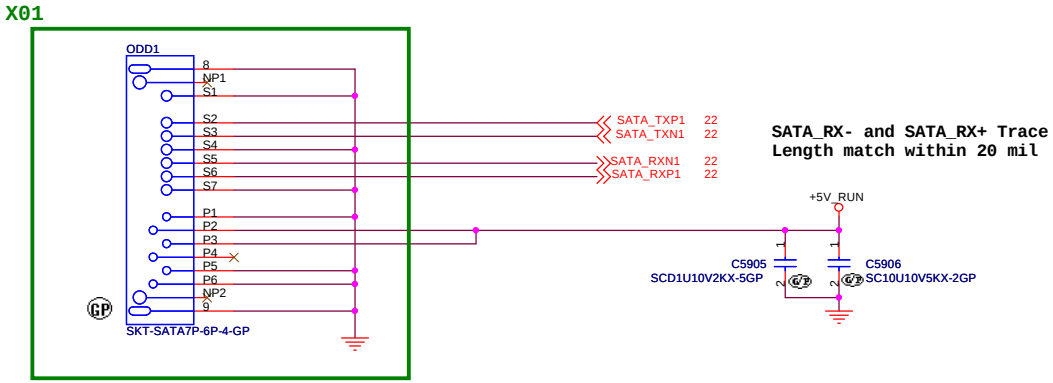
SATA HDD Connector



22.10300.961

ODD Connector



22.10300.811
22.10300.421
22.10300.471

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Title: HDD/ODD

Size	Document Number	Rev
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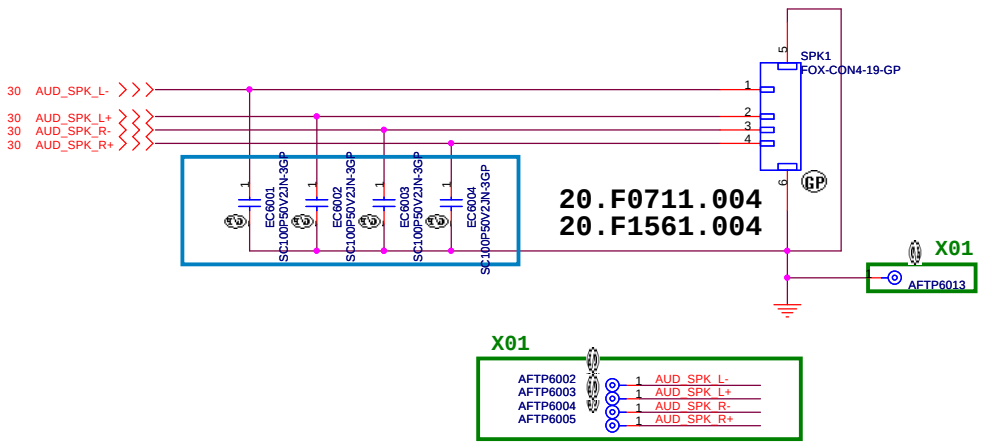
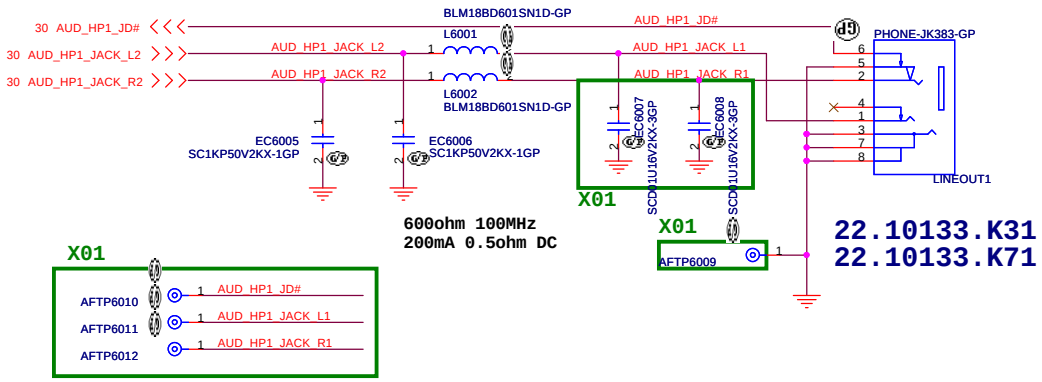
SSID = AUDIO

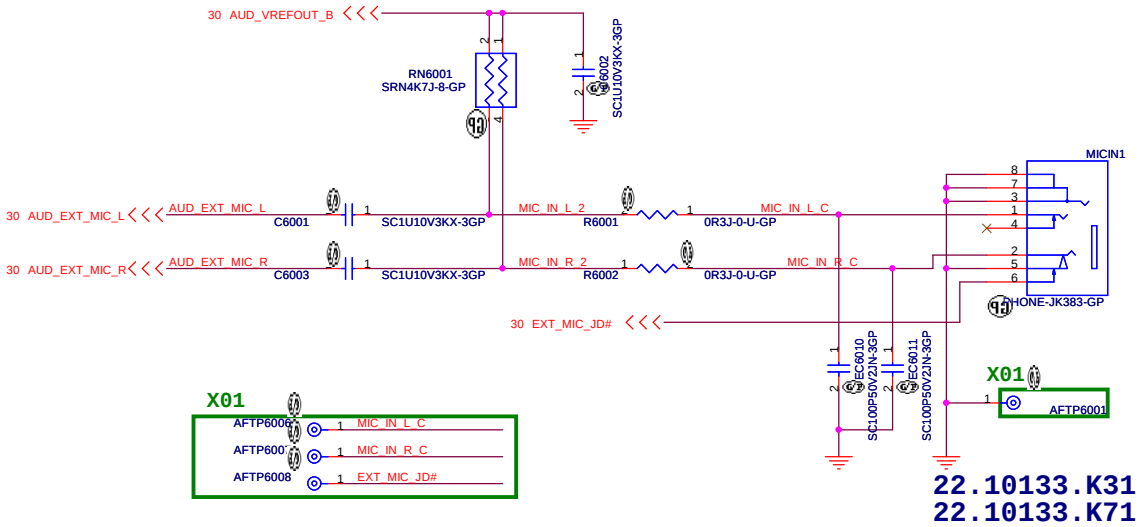
Speaker Connector



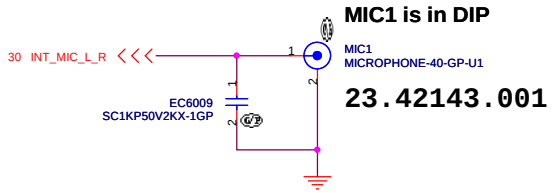
LINE1 OUT



MIC IN



Internal Microphone



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Title	Audio Jack	
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Title: Reserved

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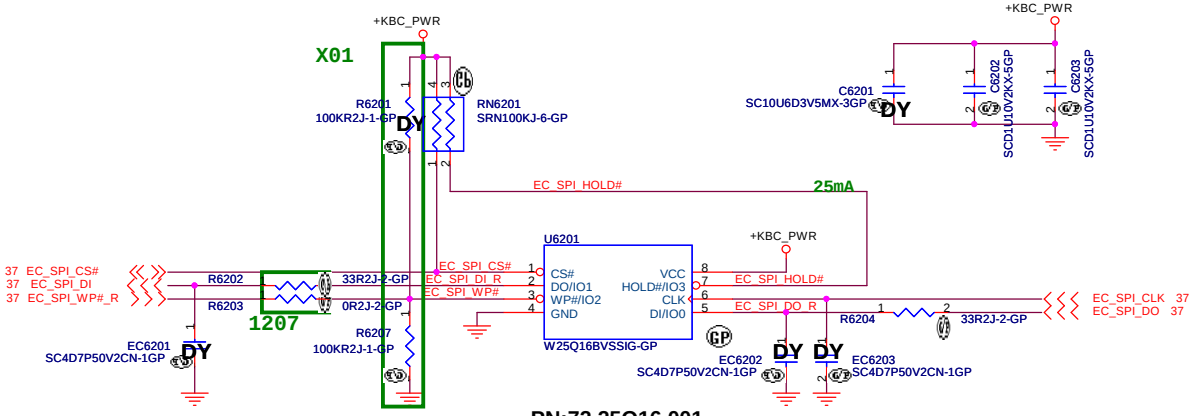
SSID = Flash.ROM

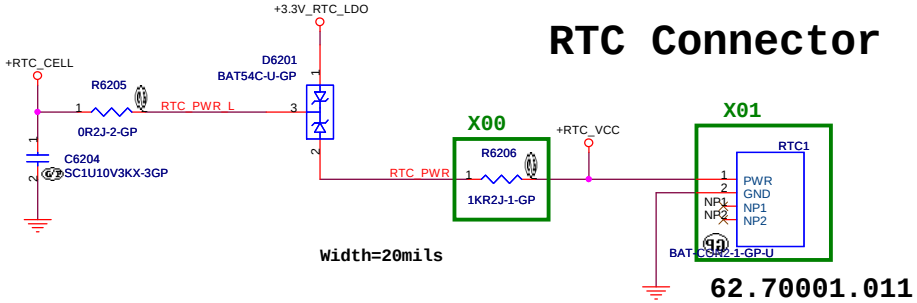
SPI FLASH ROM (16M bits) for KBC



PN:72.25Q16.001

SSID = RBATT

RTC Connector



Width=20mils

62.70001.011

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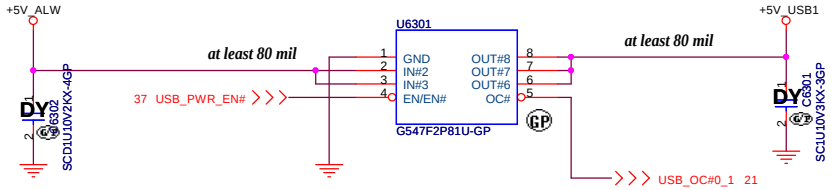
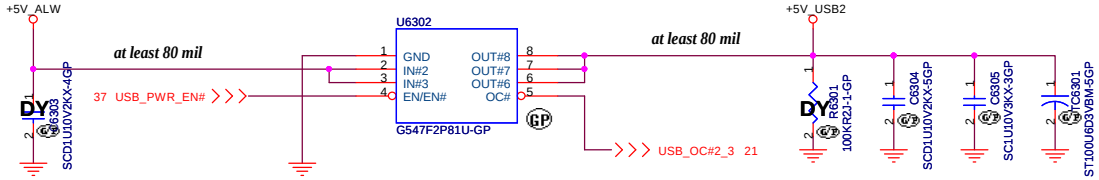
WWW.AliSaler.Com

SSID = USB

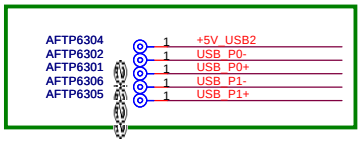
IO Board USB Power



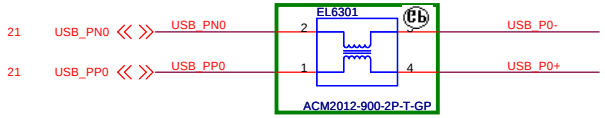
Right USB Power

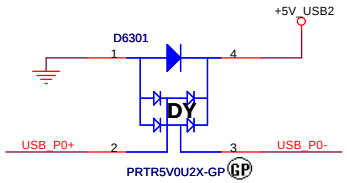


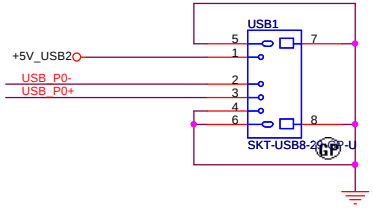
X01



X01

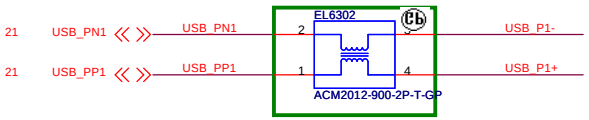


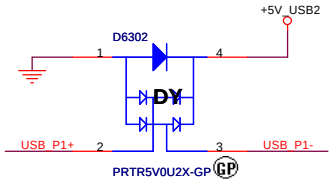


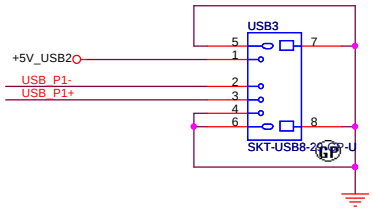


22.10254.451
22.10321.A21

X01







<Core Design>

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Title: USB

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Title: MINICARD

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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Title: Reserved

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SSID = User.Interface

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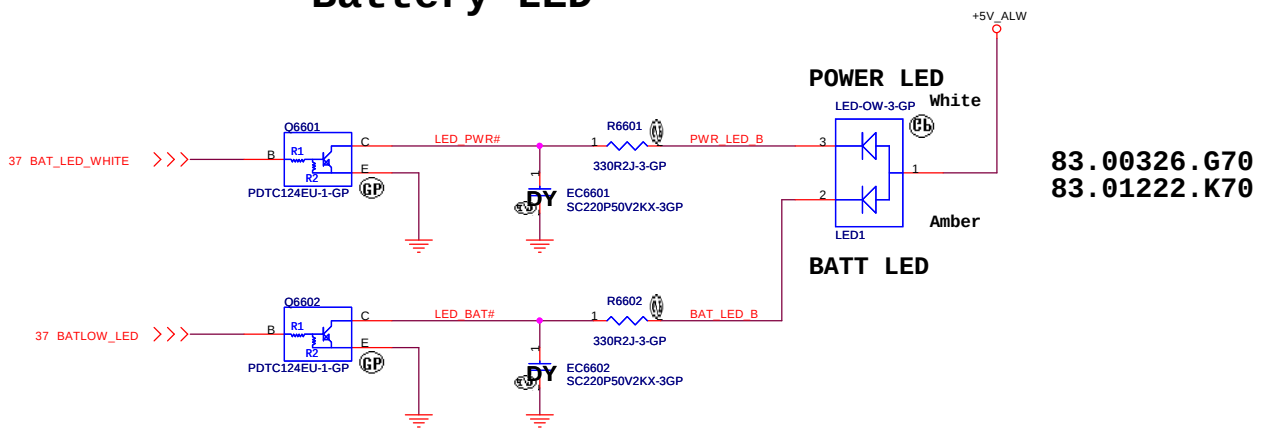
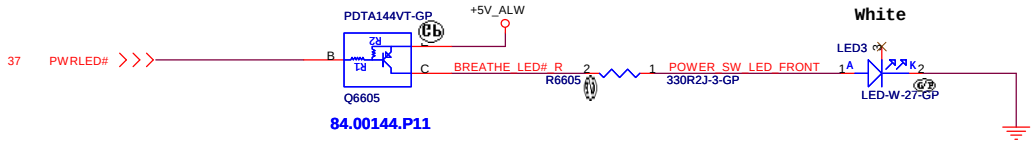
Battery LED



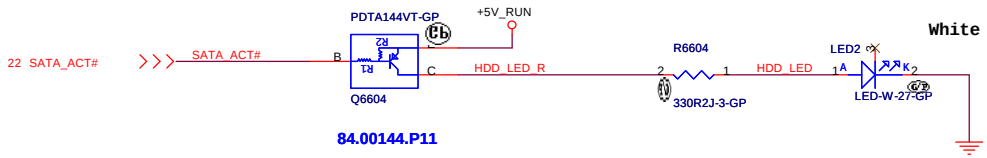
83.00326.G70
83.01222.K70

BREATHE PWR LED (Front)



84.00144.P11

HDD LED



84.00144.P11

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Title: LED

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

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Title: Reserved

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A3	Ansenal DJ1 AMD UMA	X02

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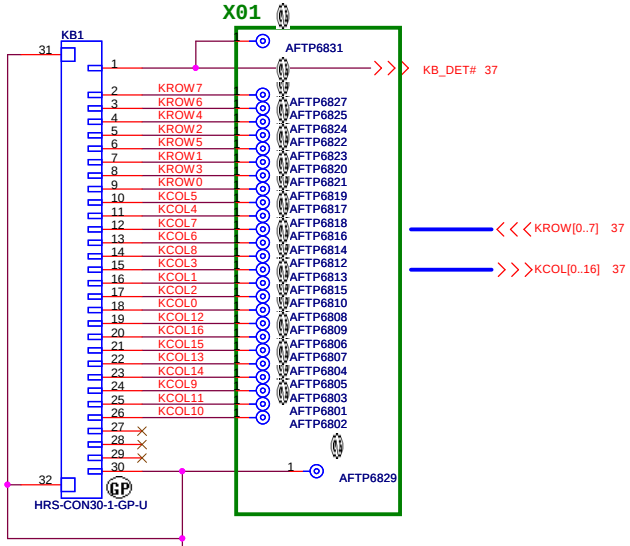
SSID = KBC

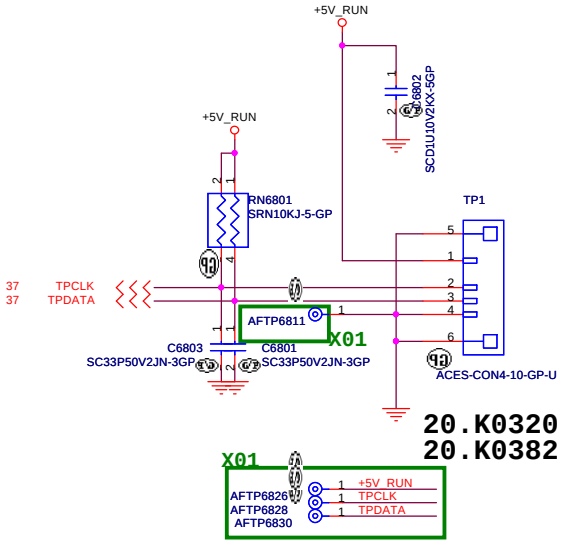
Internal KeyBoard Connector



20.K0259.030
20.K0421.030

SSID = Touch.Pad

TouchPad Connector



20.K0320.004
20.K0382.004

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Title: *Key Board/Touch Pad*

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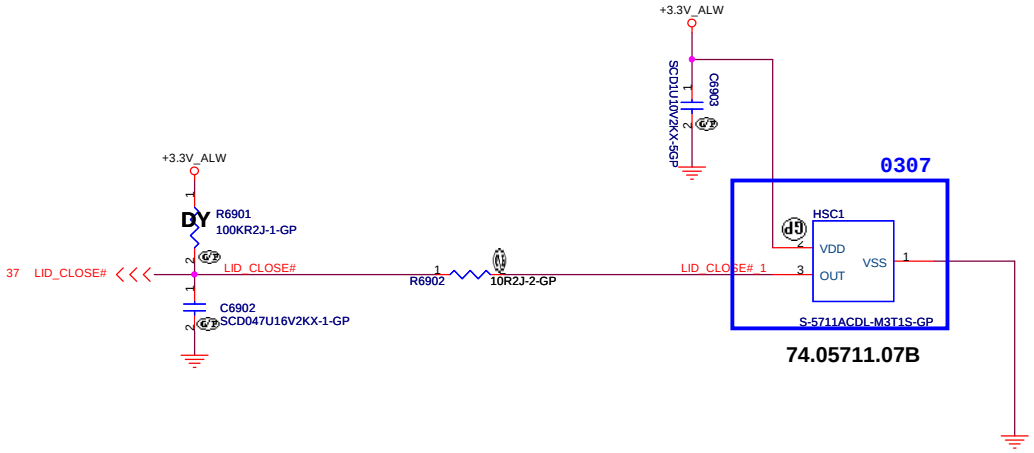

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Title: ***Hall Sensor***

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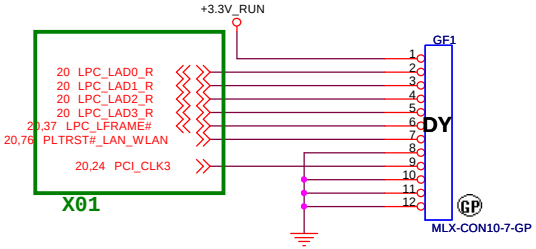

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Title: ***Reserved***

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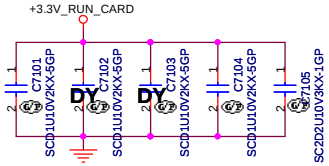
SSID = SDIO

SD/XD/MS Card Reader



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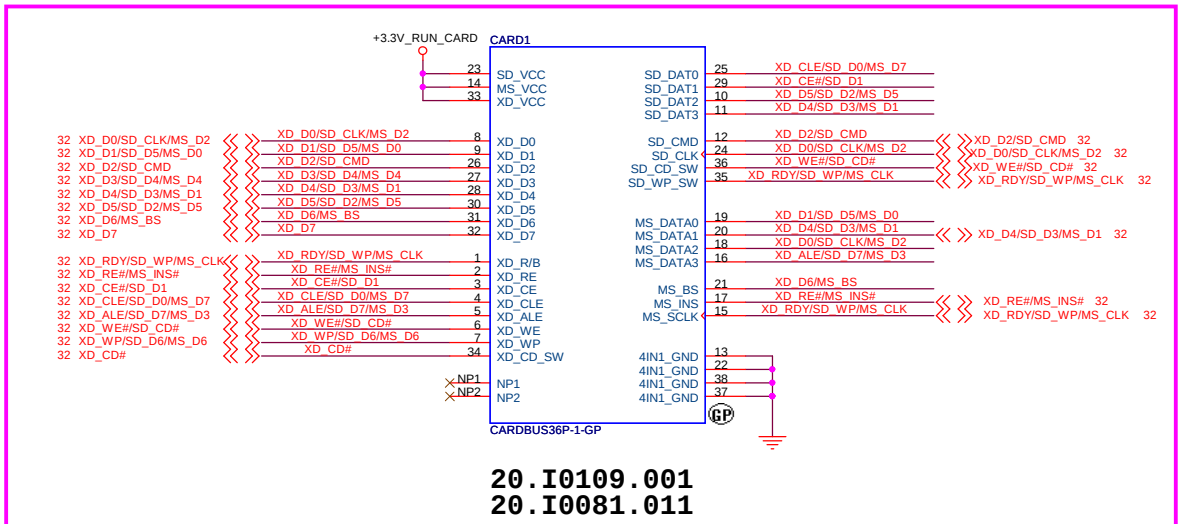

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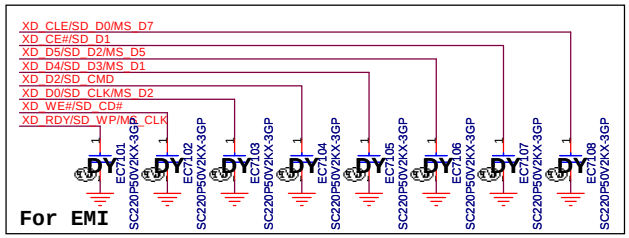
20.I0081.011



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Title: CARD Reader CONN

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Title: RESERVED

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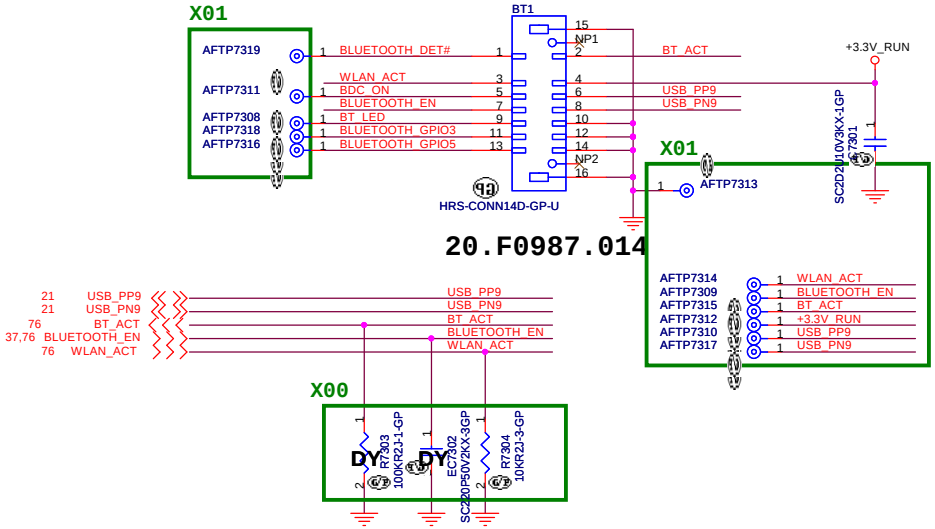
SSID = User.Interface

Bluetooth Module conn.



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Title: ***Bluetooth***

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Title: Reserved

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Title: Reserved

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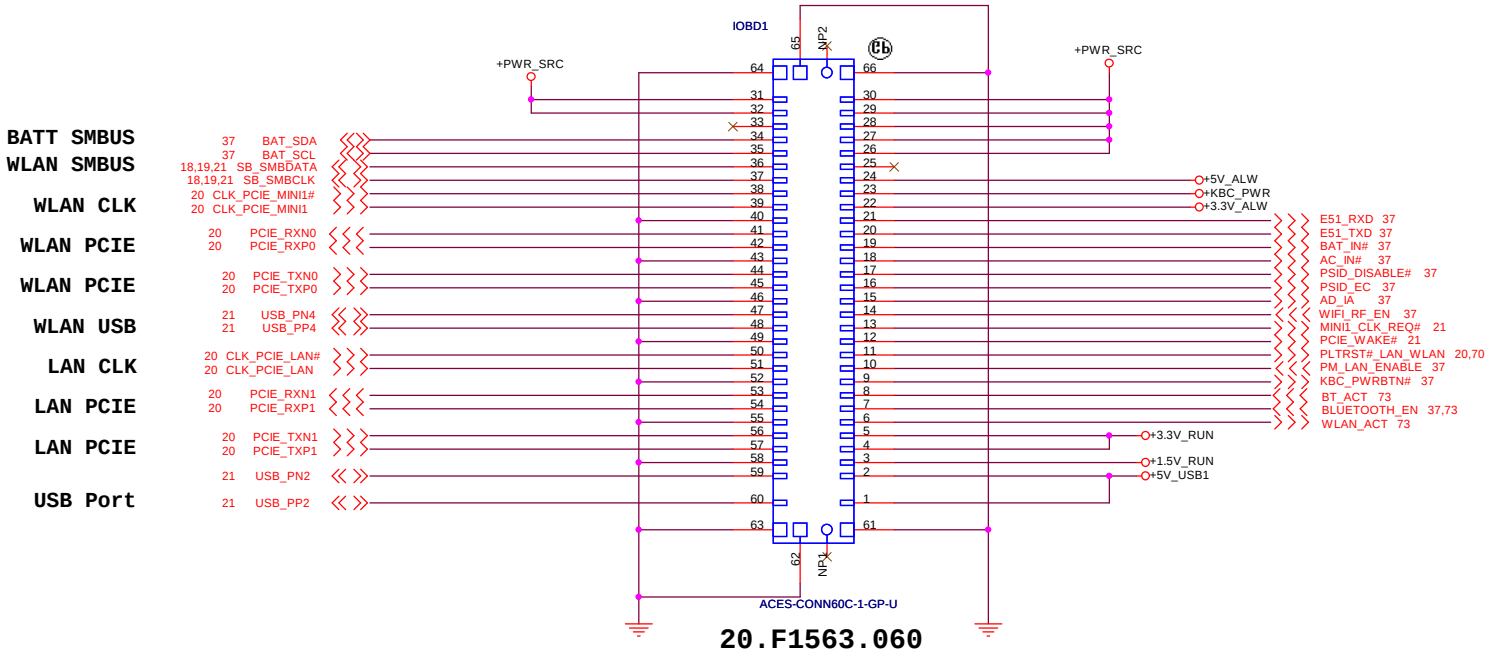
SSID = PWR.Support



20.F1563.060

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: IO Board Connector

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Title: Reserved

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<Core Design>

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Title: Reserved

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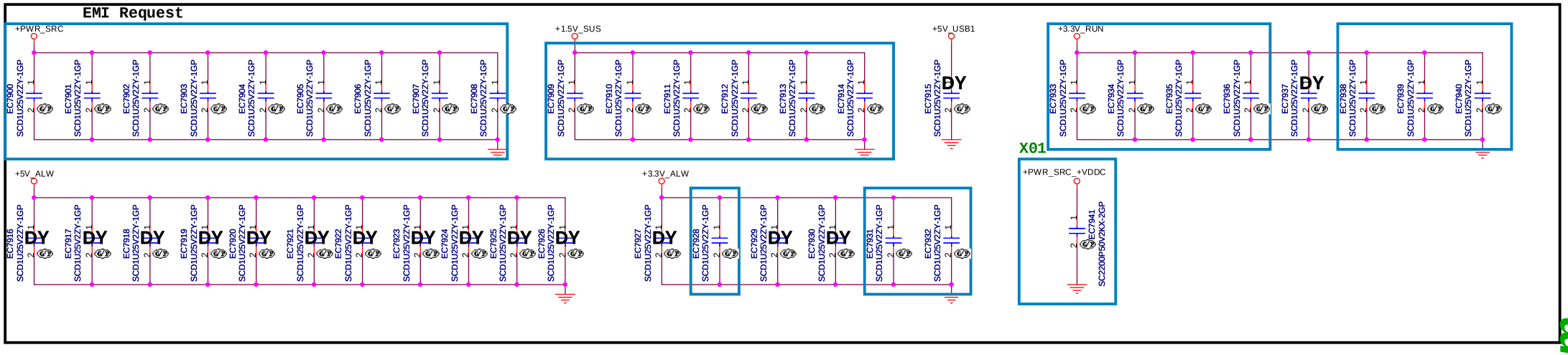
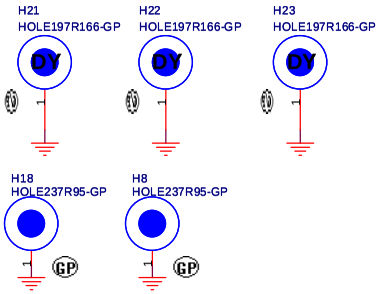
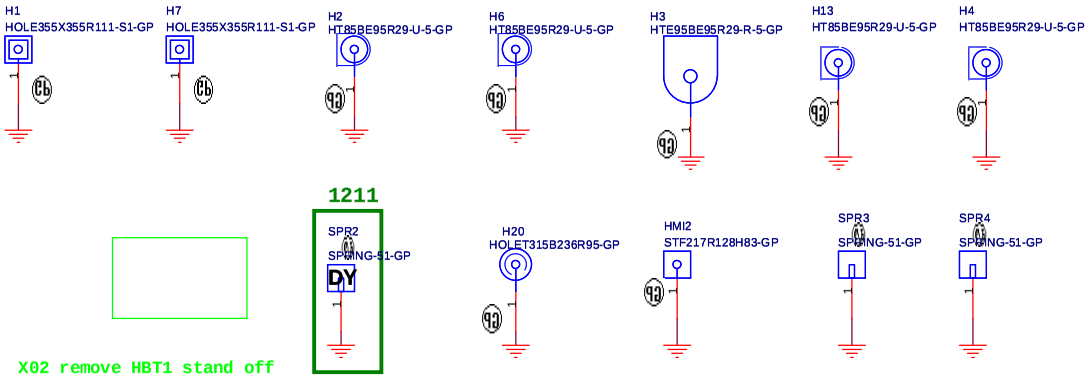
SSID = Mechanical







X02 remove HBT1 stand off
3/25

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Title: UNUSED PARTS/EMI Capacitors

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Thursday, March 25, 2010 | Sheet 79 of 90

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Title: VGA PCIE(1/4)

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	X02

Date: Tuesday, March 23, 2010 Sheet 80 of 90

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Title: VGA LVDS/TV/CRT(2/4)

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Tuesday, March 23, 2010 | Sheet 81 of 90

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Title: VGA POWER/GND(3/4)

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	X02

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Title: VGA MEMORY/STRAPS(4/4)

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Title: GPU-VRAM (1/2)

Size	Document Number	Rev
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Title: GPU-VRAM (2/2)

Size	Document Number	Rev
A3	Ansenal DJ1 AMD UMA	X02

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Title
TPS51117_+VCC_GFXCORE

Size	Document Number	Rev
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Date: Tuesday, March 23, 2010 Sheet 86 of 90

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Title: APL5930_+1.1V_RUN

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Tuesday, March 23, 2010 | Sheet 87 of 90

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Title: Reserved

Size: A3 | Document Number: Ansenal DJ1 AMD UMA | Rev: X02

Date: Tuesday, March 23, 2010 | Sheet 88 of 90

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Change notes - Page 1

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	10	change RN1006 pull-up power plane from +1.5V_RUN to +1.5V_SUS	avoid leakage in S3	EE
		2	20	RN2002 replace to 22R	NB_REFCLK votlage level too high	EE
		3	20	R2009 move to PCI_CLK3, change DF1 clk from PCLK_FWH to PCI_CLK3	PCLK_FWH in internal CLKGEN only support 14MHz DF1 clk need 33MHz	EE
		4	37	pop R3729 & depop R3733	MB version ID	EE
		5	37	reserve U3703, pop R6207 and depop R6201	avioding SPI ROM data loss	EE
		6	46	pop PR4619 & depop PR4618	modify operating mode for+15V_ALW voltage	EE
		7	37,10	add Q1005, pop R1039 and R1040	CPU PROCHOT connect from EC through a level shift allow EC to force CPU enter HTC state when power budge over the limit in DOS mode.	EE
		8	42	C4201, C4203 to 100pF	For power sequence	EE
		9	20	C2011, C2012 to 18pF	vendor measure feedback value	EE
		10	48	Add PR4812 PU +3.3V_ALW	For +1.1V_ALW rising issue	EE
		11	18	Change TC1801 to 330uF, 2V tolerance.	Implement common part for 1.5V power rail.	EE
		12	13 10	remove R1329,R1330 and add RN1302 remove R1323,R1324 and add RN1303 remove RN1007 and change RN1003 to 1K8P	Combine resistor	EE
	X01	13	55 60 63 68 73	arrange CRT conn. AFTP arrange SPKR, MIC, JACK conn. AFTP arrange USB conn. AFTP arrange KB, TP conn. AFTP arrange BT conn. AFTP	Sink with DJ1 CP	EE
		14	20	R2020 to RN2009	For SIV report LPC_LAD bus rising time fail	EE
		15	37	Add C3724, R3757	To set accurate current in EC.	EE
		16	10	Reserve R1041 for CPU_R_LDT_PWRGD	reseve POWOK level for 6265 IC	EE
		17	47	PR4732 and PR4750 to small size	power team request	power
		18	20	Del D2001	solve PLTRST# signal rising time too slow	EE
		19	41	Dummy D4103 and exchange IMVP and VDDC_PWRGD signal	For SB_PWRGD shotdown drop	EE
		20	47	Reserve PC4739, PC4740, PC4741,PC4742	Reserve for FB noise	EE
		21	79	Reserve EC7941	EMI request	EMI
		22	21	Reserve C2105	Reserve for SIO_RCIN# noise	EE
		23	47	PR4727 from 10ohm to 0 ohm	power team request	power
		24	64	DEL R6302,R6303, add EL6301 DEL R6304,R6305, add EL6302	EMI request	

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Change notes - Page 2

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		25	60	EC6007 and EC6008 from 100p to 0.01uF	codec vendor suggestion	EE
		26	37	R3737 from 0R to 33R	for SPI_CLK over and under shoot	EE
		27		PL4701,PL4703,PL4601,PL4602,PL5001,PL4901	Add glue for choke pad	power
		28	55	L5502,L5503 bead to 10ohm	for SIV CRT G, B report fail	EE
		29	42	C4202,C4204, C4208 to 4.7uF	For sequence	EE
	X02	1	50	Change PR5010 from 4.2KR to 8.25KR	Avoid +1.1V_RUN OCP	power
		2	69	Change HSC1 from 74.06781.07B(AKE) to 74.05711.07B(SEKIO)	Avoid AKE and SEKIO footprint not match	EE
		3	20	Exchange Lan & Wlan signal	For lan loop	EE
		4	37	Add one 2N7002 to pull low PSID_EC	For RCID function	EE
		5	37	Change KBC GPI81 from NB_VDDR_EN to KBC_RCID	For RCID function	EE
		6	79	Remove HBT1 stand off	For ME request	ME
		7	37	Change PCB version from X01 to X02	For version change	EE
		8	37	Remove NB_VDD_EN signal	For GPIO change	EE

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