

Compal Confidential

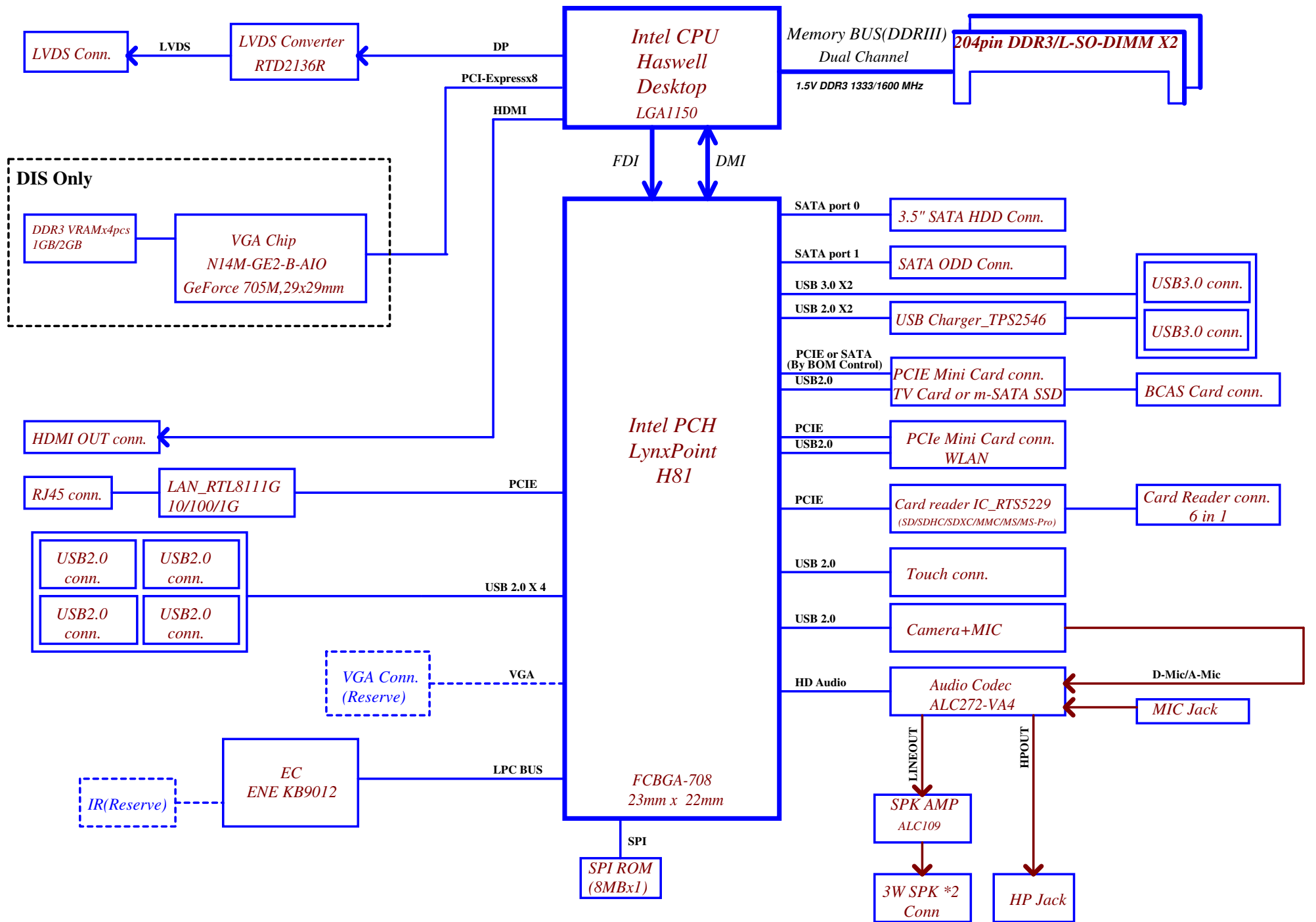
C560 LA-A061P Schematics Document

INTEL Haswell CPU with DDRIII + PCH Lynx-Point
AIO M/B

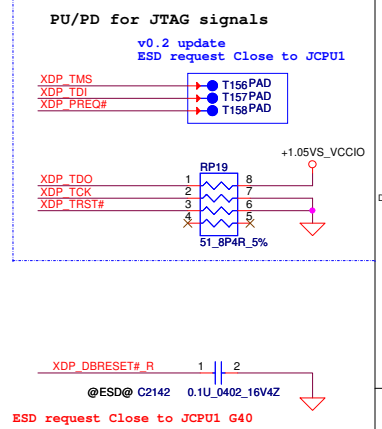
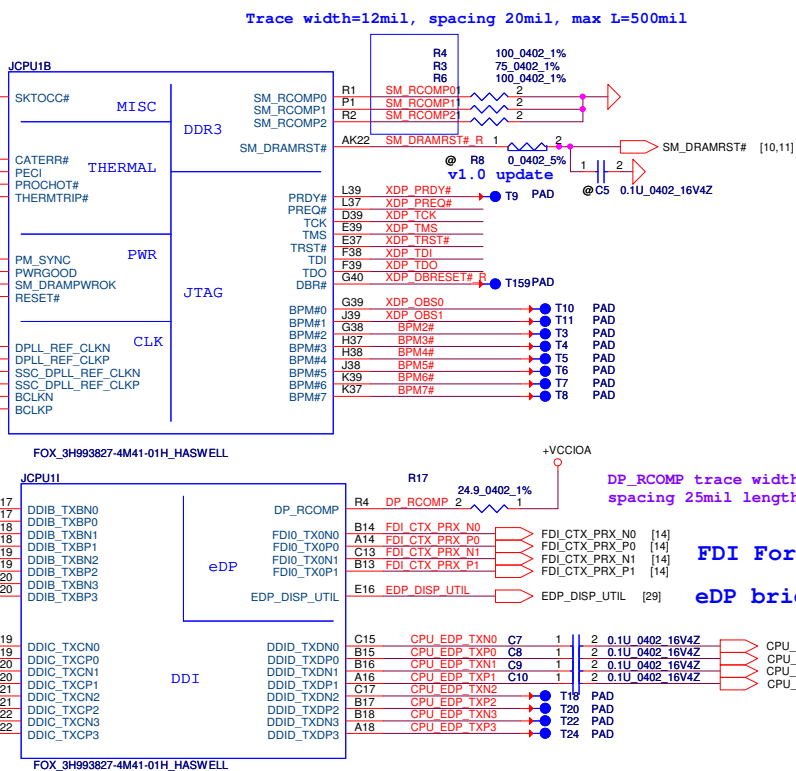
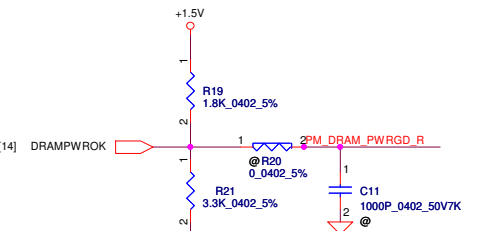
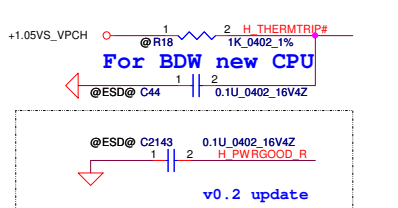
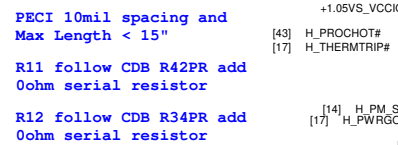
September 24, 2013

REV:1.0

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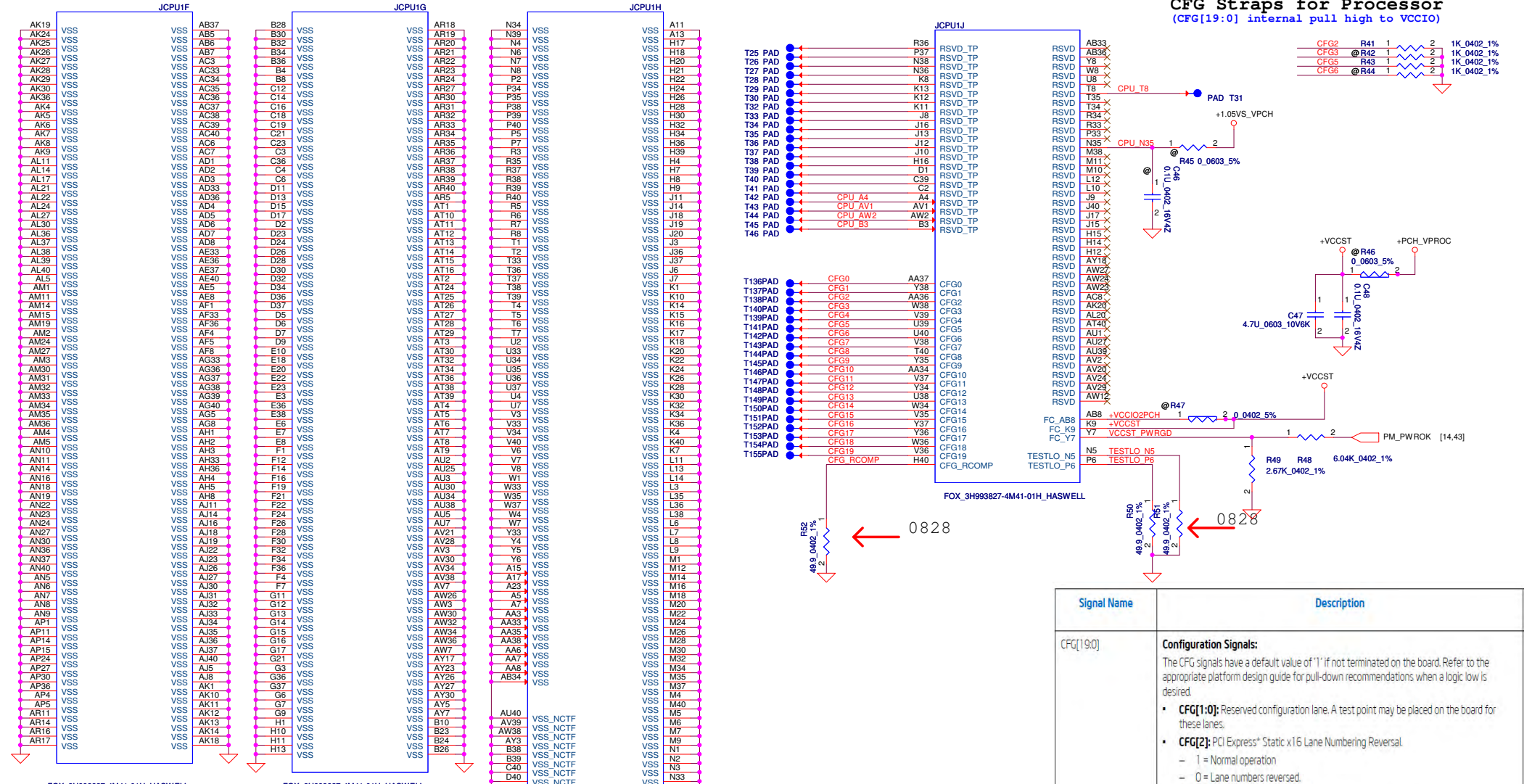
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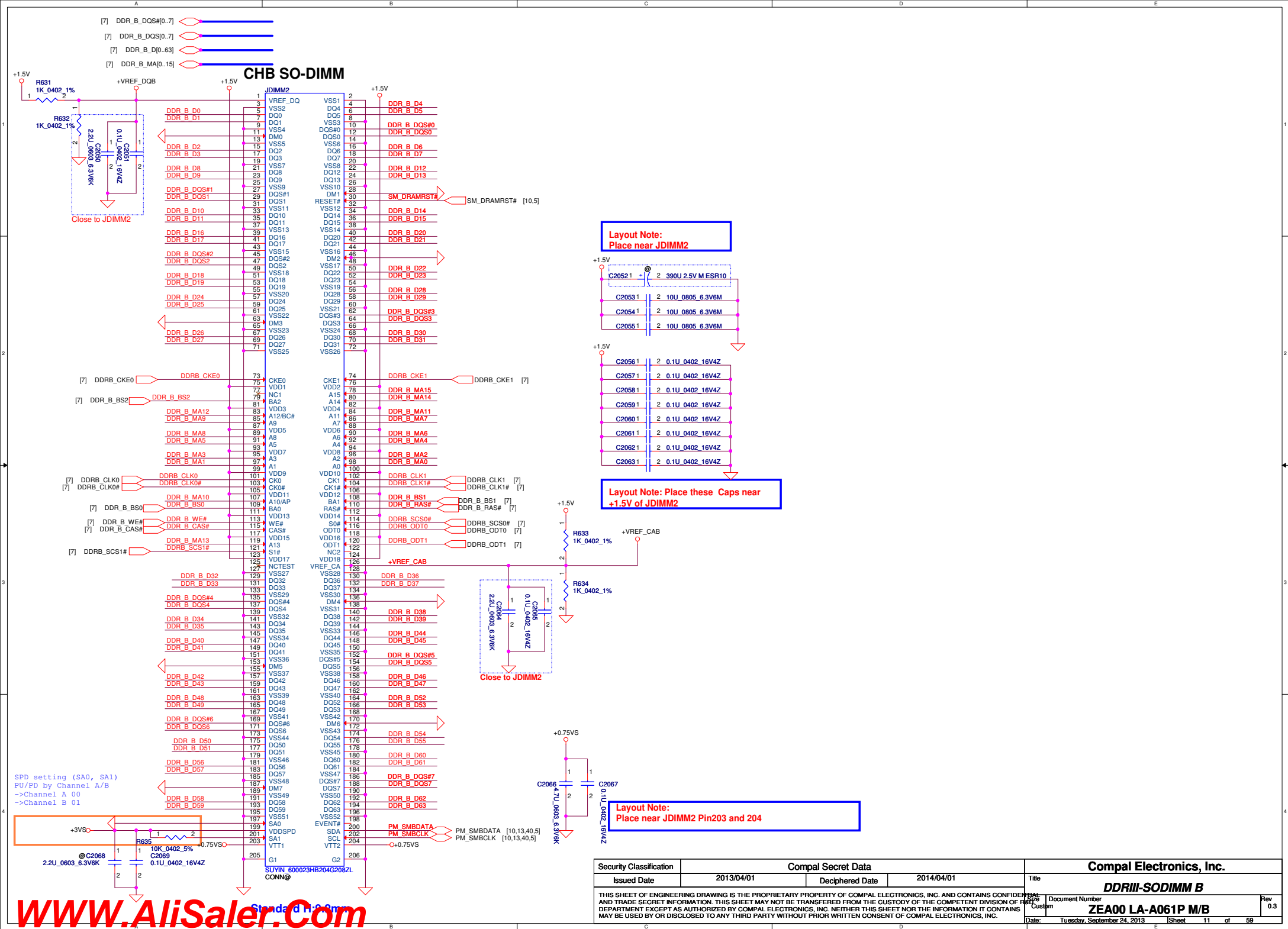


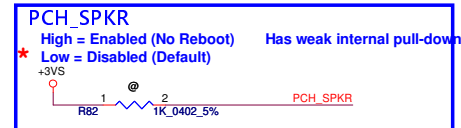
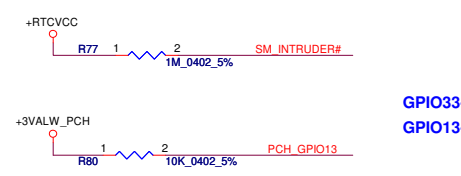
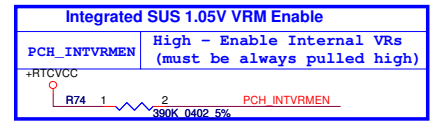
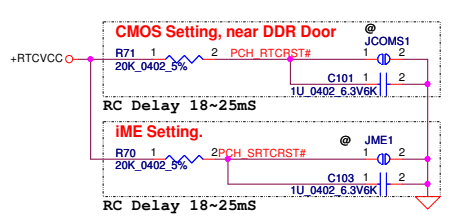
Port	Original Interface Interconnect Signals	HDMI Signals	Processor Digital Video Interface Pins
Port B	DDI0_VT0_IN	HDMI0_VT2_DP	DDI0_VT0[0]
	DDI0_VT0_IN	HDMI0_VT2_DN	DDI0_VT0[1]
	DDI0_VT1_P	HDMI0_VT1_DP	DDI0_VT1[0]
	DDI0_VT1_P	HDMI0_VT1_DN	DDI0_VT1[1]
	DDI0_VT2_P	HDMI0_VT2_DP	DDI0_VT2[0]
	DDI0_VT2_P	HDMI0_VT2_DN	DDI0_VT2[1]
	DDI0_VT3_P	HDMI0_VT3_DP	DDI0_VT3[0]
	DDI0_VT3_P	HDMI0_VT3_DN	DDI0_VT3[1]
	DDI0_VT4_P	DDI0_VT4_DP0	Hot plug detect used by HDMI Port B
	DDI0_VT4_P	DDI0_VT4_GLK	HDMI DDC lines for Port B
	DDI0_VT4_P	DDI0_VT4_DN0	
	DDI0_VT4_P	DDI0_VT4_DN1	
Port C	DDI0_VT0_P	HDMI0_VT2_DP	DDI0_VT0[0]
	DDI0_VT0_P	HDMI0_VT2_DN	DDI0_VT0[1]
	DDI0_VT1_P	HDMI0_VT1_DP	DDI0_VT1[0]
	DDI0_VT1_P	HDMI0_VT1_DN	DDI0_VT1[1]
	DDI0_VT2_P	HDMI0_VT2_DP	DDI0_VT2[0]
	DDI0_VT2_P	HDMI0_VT2_DN	DDI0_VT2[1]
	DDI0_VT3_P	HDMI0_VT3_DP	DDI0_VT3[0]
	DDI0_VT3_P	HDMI0_VT3_DN	DDI0_VT3[1]
	DDI0_VT4_P	DDI0_VT4_DP0	Hot plug detect used by HDMI Port C
	DDI0_VT4_P	DDI0_VT4_GLK	HDMI DDC lines for Port C
	DDI0_VT4_P	DDI0_VT4_DN0	
	DDI0_VT4_P	DDI0_VT4_DN1	
Port D	DDI0_VT0_P	HDMI0_VT2_DP	DDI0_VT0[0]
	DDI0_VT0_P	HDMI0_VT2_DN	DDI0_VT0[1]
	DDI0_VT1_P	HDMI0_VT1_DP	DDI0_VT1[0]
	DDI0_VT1_P	HDMI0_VT1_DN	DDI0_VT1[1]
	DDI0_VT2_P	HDMI0_VT2_DP	DDI0_VT2[0]
	DDI0_VT2_P	HDMI0_VT2_DN	DDI0_VT2[1]
	DDI0_VT3_P	HDMI0_VT3_DP	DDI0_VT3[0]
	DDI0_VT3_P	HDMI0_VT3_DN	DDI0_VT3[1]
	DDI0_VT4_P	DDI0_VT4_DP0	Hot plug detect used by HDMI Port D
	DDI0_VT4_P	DDI0_VT4_GLK	HDMI DDC lines for Port D
	DDI0_VT4_P	DDI0_VT4_DN0	
	DDI0_VT4_P	DDI0_VT4_DN1	

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CFG Straps for Processor
(CFG[19:0] internal pull high to VCCIO)







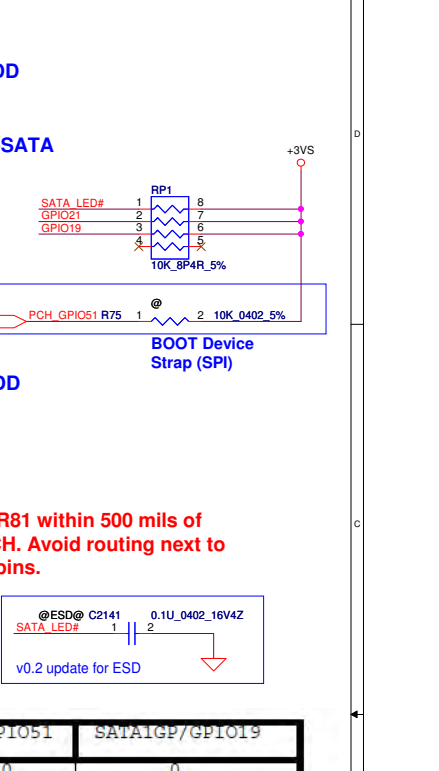
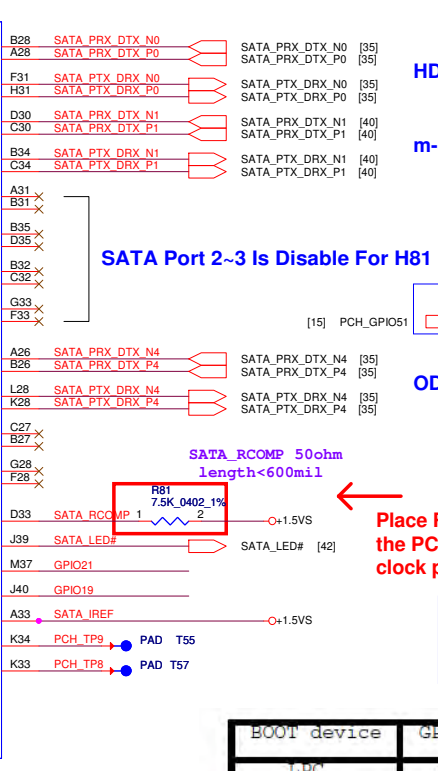
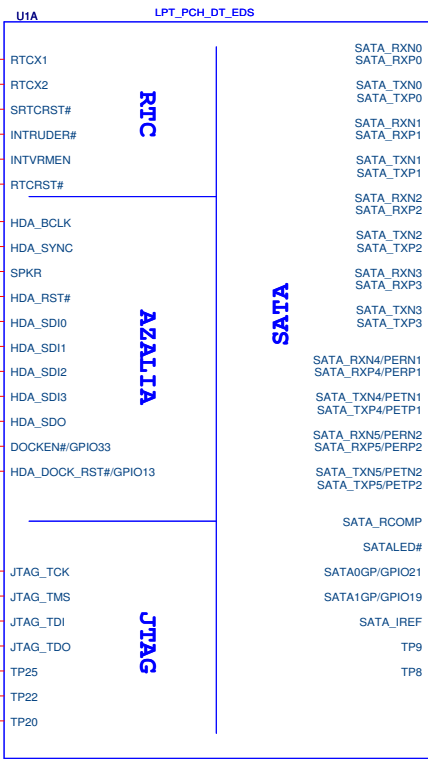
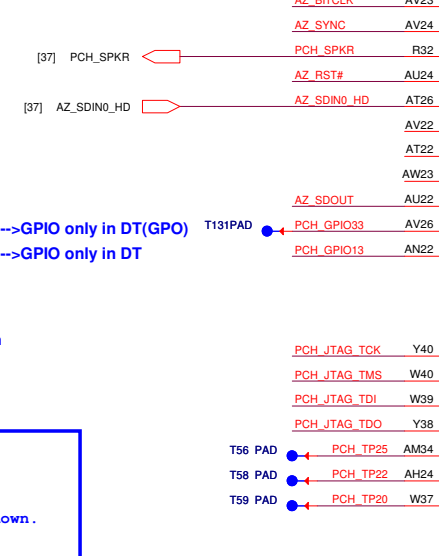
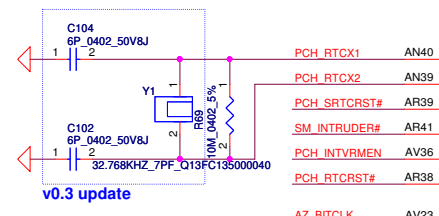
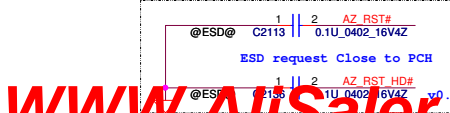
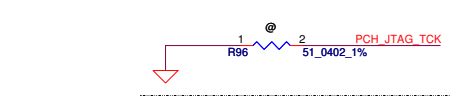
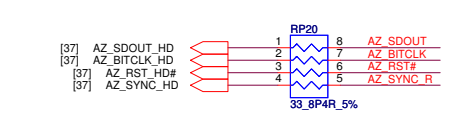
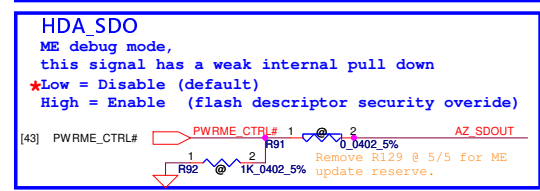
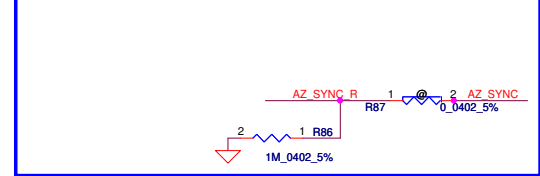
HDA_SYNC

This signal has a weak internal pull down

*H=>On Die PLL is supplied by 1.5V (mobile)

L=>On Die PLL is supplied by 1.8V (DT)

Strap: This signal has a weak internal pull-down. Do not pull high.



BOOT device	GPIO51	SATA1GP/GPIO19
LPC	0	0
SPI	1	1

*GPIO51 with internal pull-up

SATA1GP/ GPIO19, GPIO51

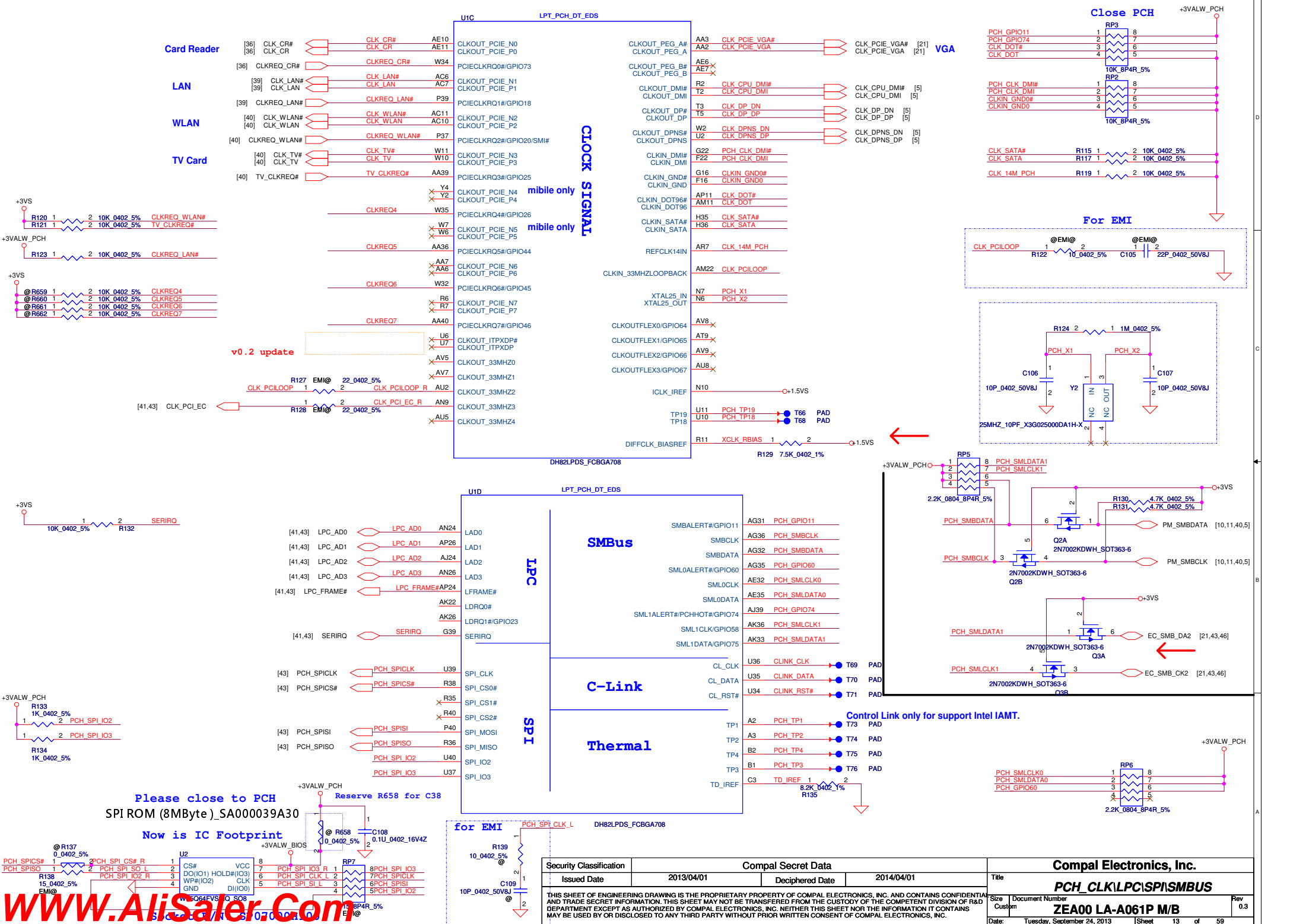
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

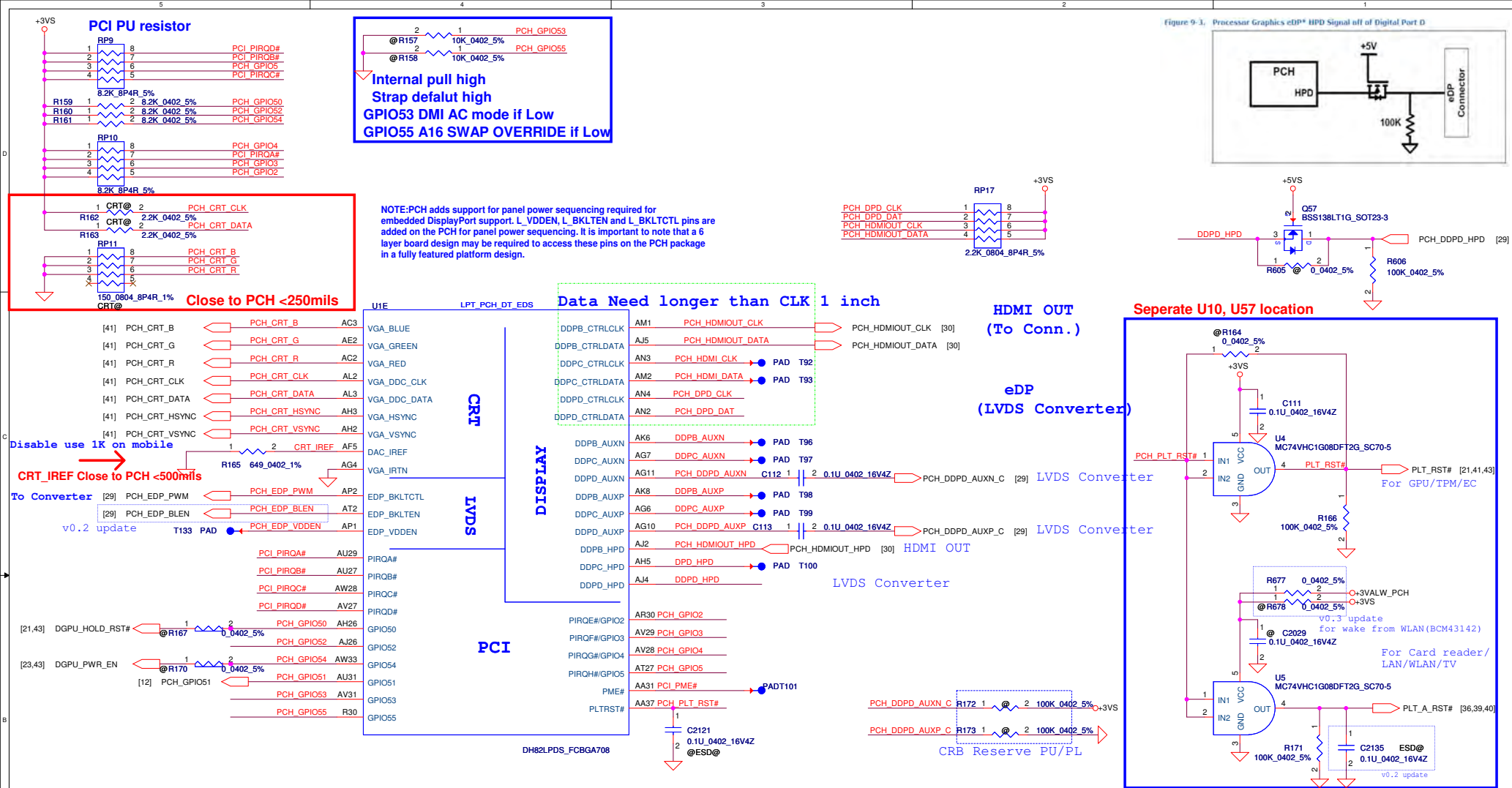
Table 1-3. Desktop Lynx Point SKUs Flexible I/O Map																		
SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
H87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 7	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	NA	NA	SATA 3Gb/s Port 1	SATA 3Gb/s Port 2	SATA 6Gb/s Port 1	NA	NA

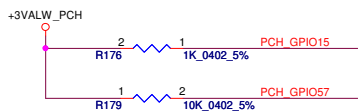
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Issued Date		2013/04/01		Deciphered Date		2014/04/01		Title		PCH_HDA/JTAG/SATA	
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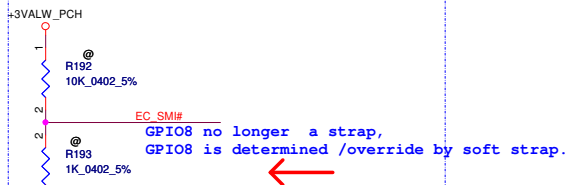




GPIO8

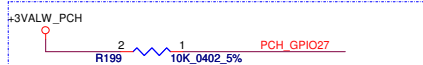
Integrated Clock Chip Enable (Removed)

H: Disable
L: Enable



This signal has a weak internal pull-up but requires an external pull down.

The current default is clock enable

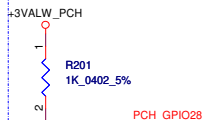


In Deep Sleep Power Well. Unmuxed. Defaults to GPI. Not used Weak pull-up 10kΩ to VccDSW3_3 -->Check list1.5 P402. PD to GND for Huron River!!

GPIO28

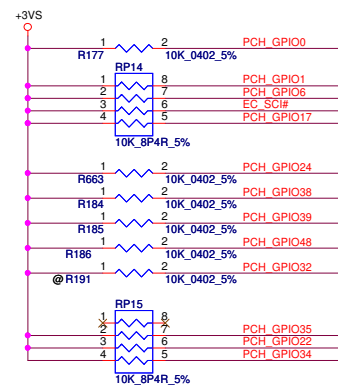
On-Die PLL Voltage Regulator

H: Enable
L: Disable



Clock validation strap
ICG is EN when LOW
*GPIO36 with internal pull-down

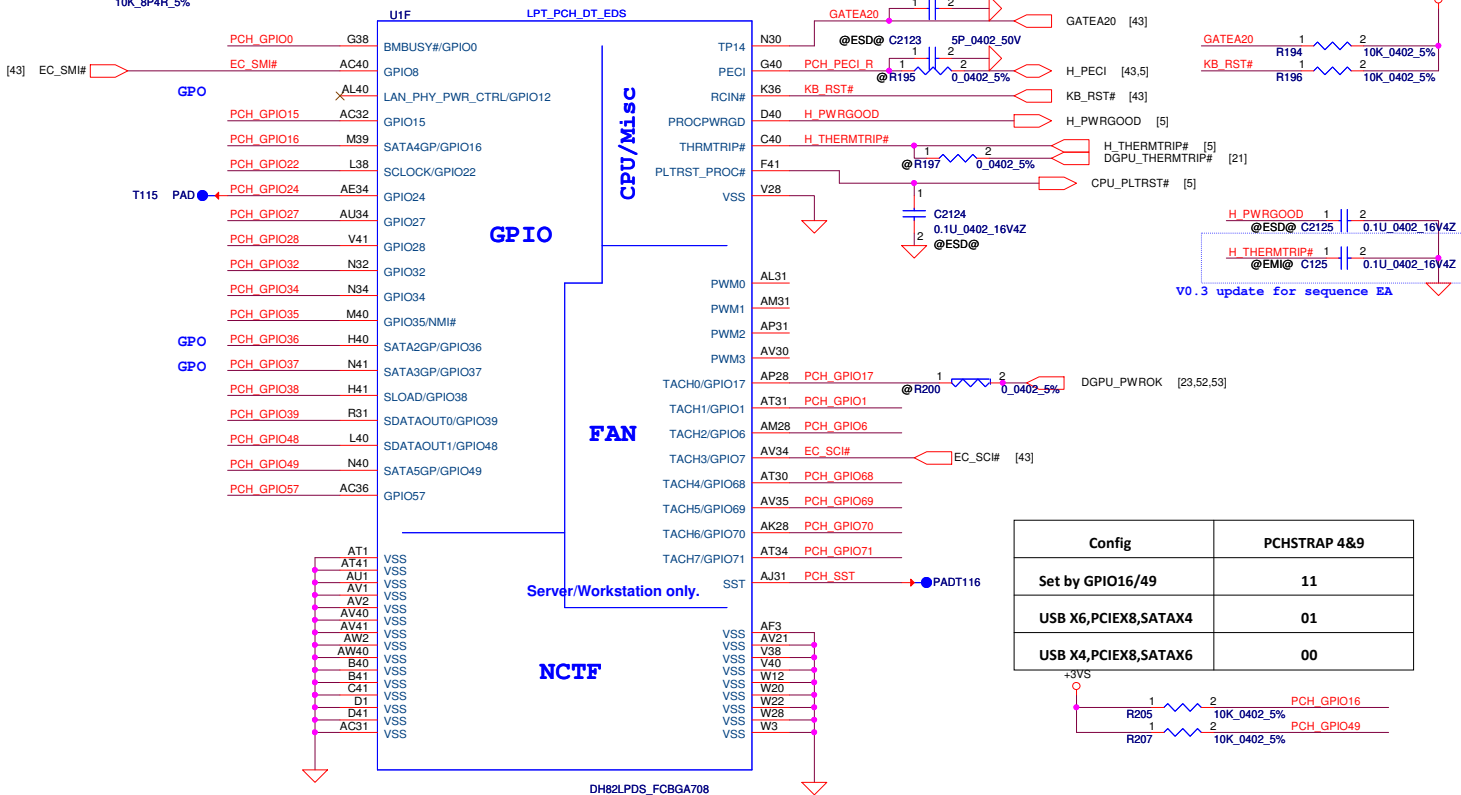
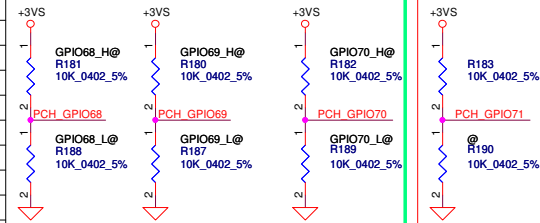
TLS
Hi:with confidentiality
Low:with no confidentiality
*GPIO37 with internal pull-down



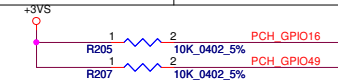
120821

SKU ID	GPIO68	GPIO69	GPIO69
SKU1	0	0	0
SKU2	0	0	1
SKU3	0	1	0
SKU4	0	1	1
SKU5	1	0	0
SKU6	1	0	1
SKU7	1	1	0
SKU8	1	1	1

SKU ID TABLE

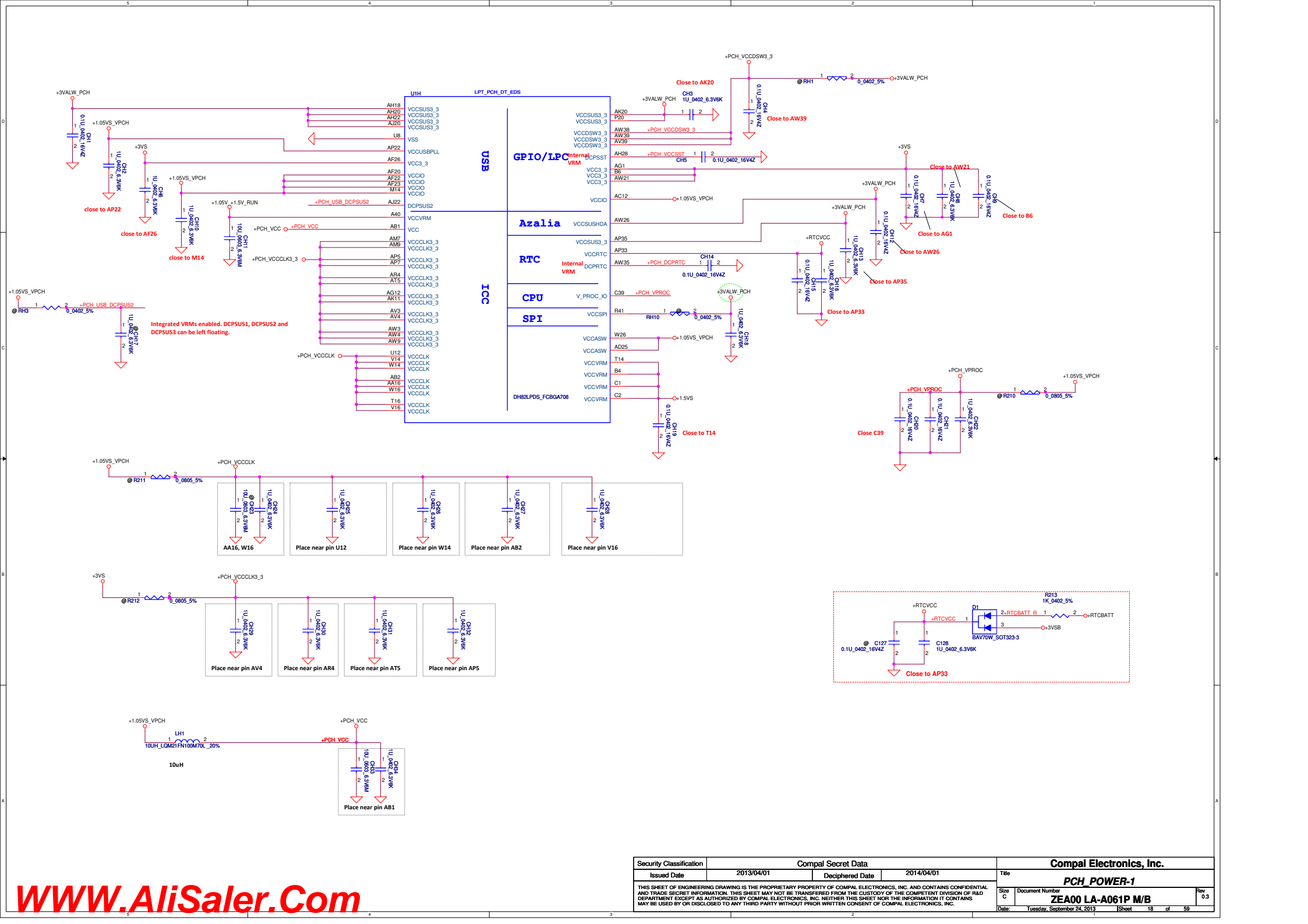


Config	PCHSTRAP 4&9
Set by GPIO16/49	11
USB X6,PCIEX8,SATAx4	01
USB X4,PCIEX8,SATAx6	00

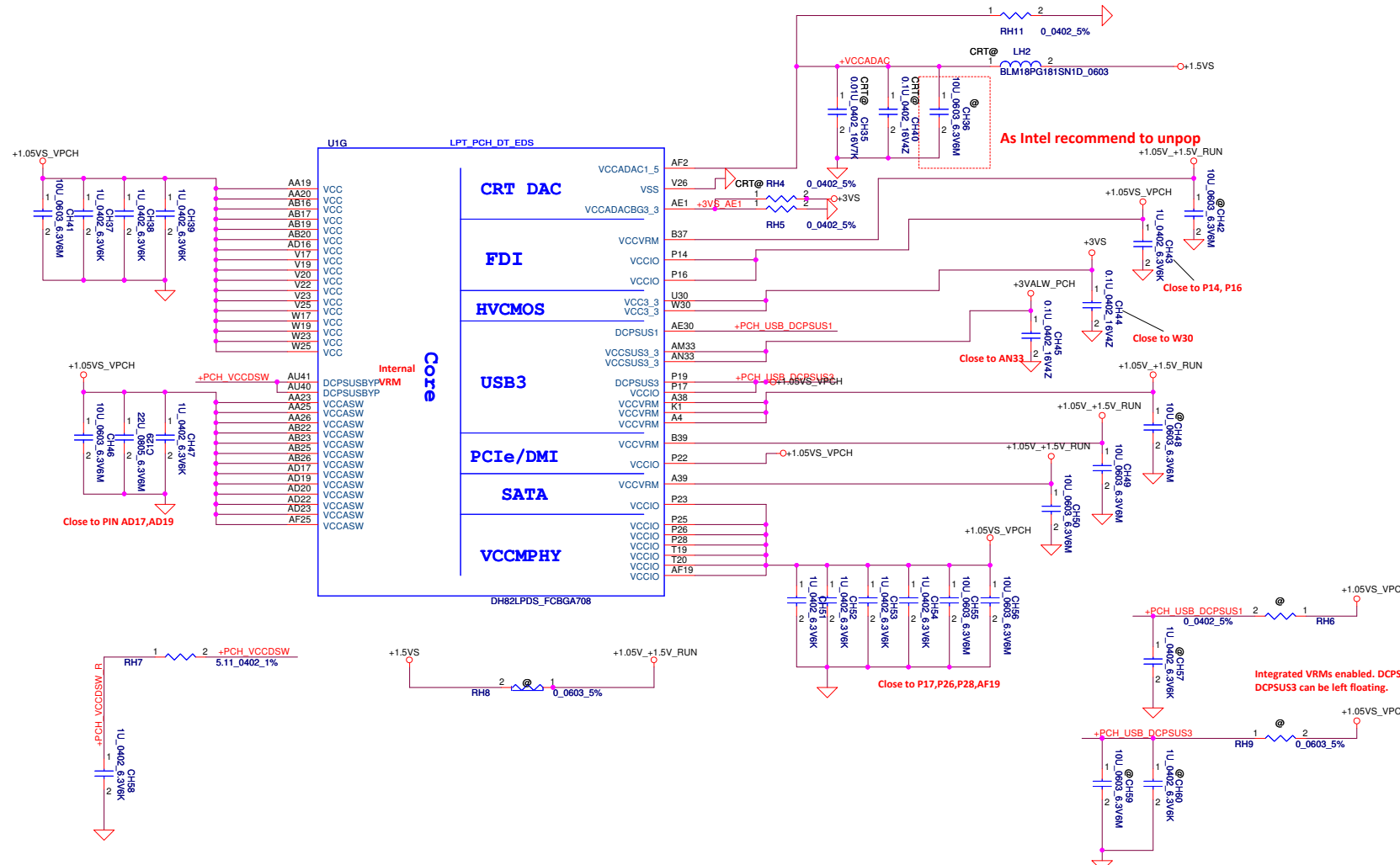


Fixed Signals				Muxed Signals		Fixed Signals				Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1
				(00)	(00)							(00)	(00)		
				USB3 3	USB3 4							PCIE 1	PCIE 2		
				(01)	(01)							(01)	(01)		

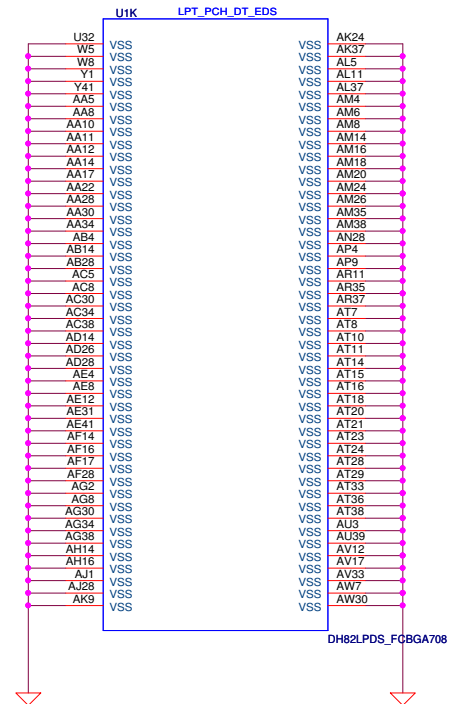
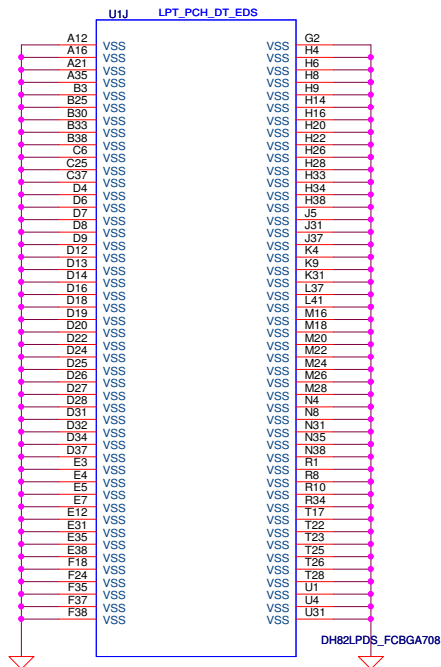
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If CRT disable Pin AF2 & Pin AE1 can connect to GND



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



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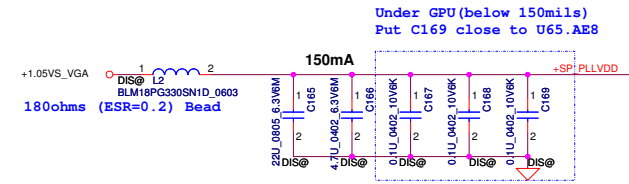
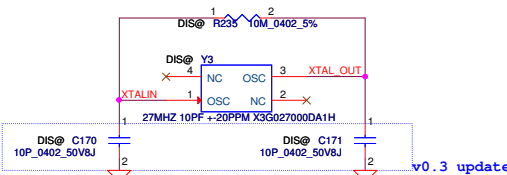
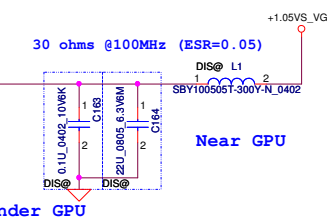
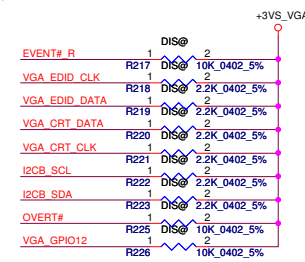
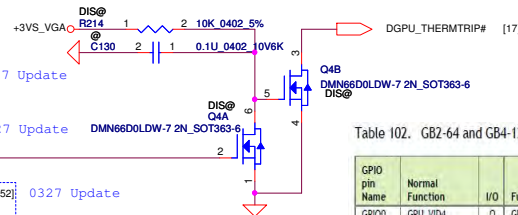
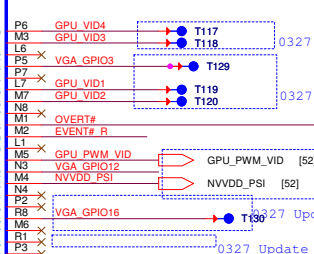
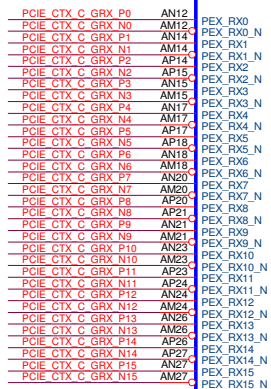
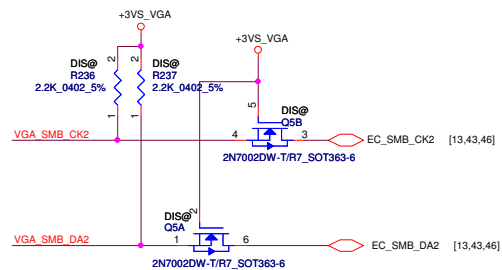
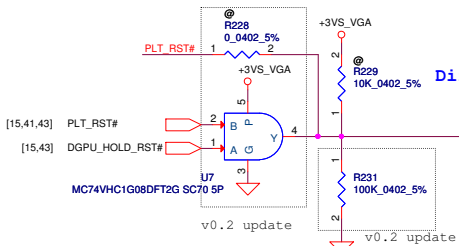
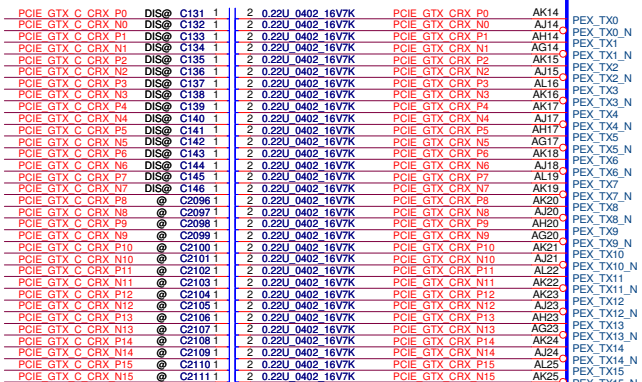
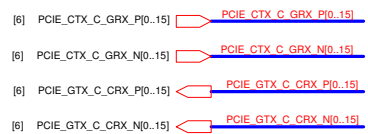


Table 102. GB2-64 and GB4-128 GPIO Description

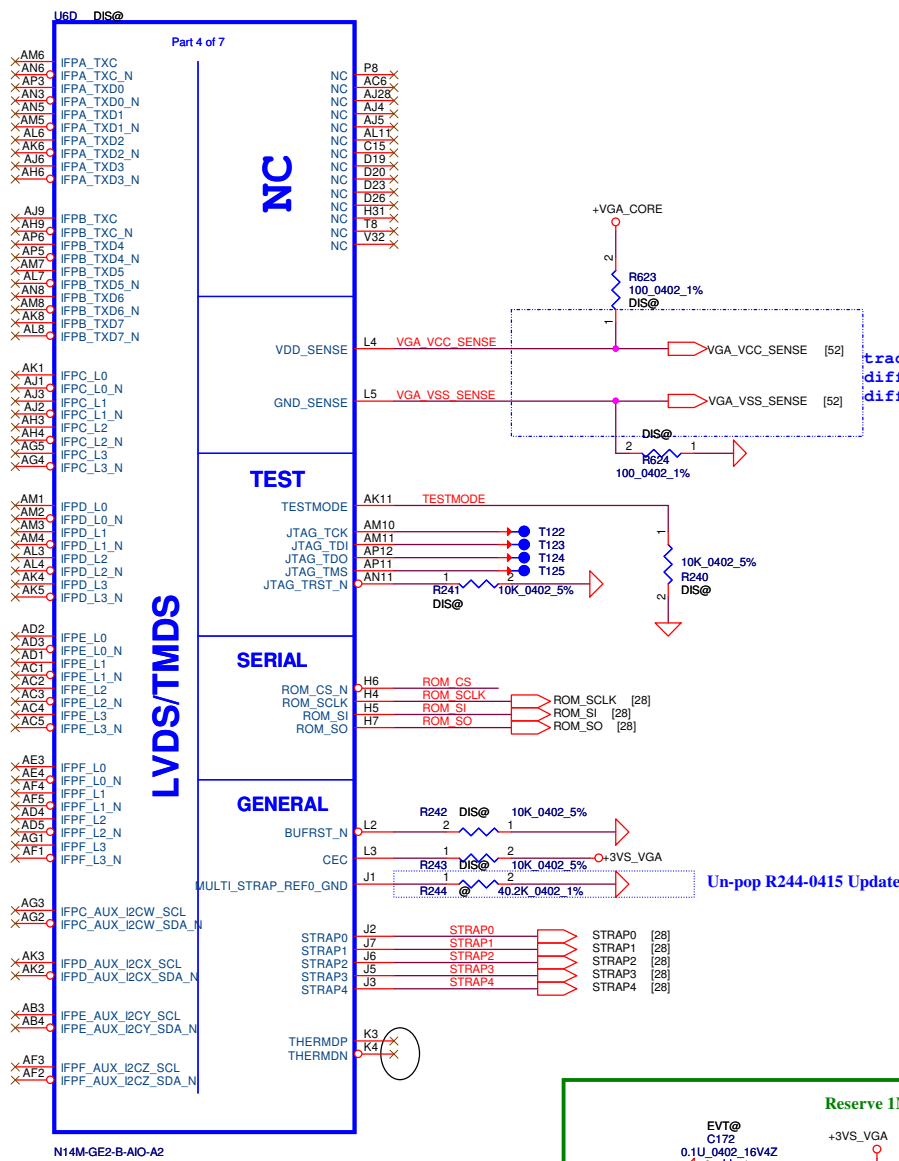
GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPIO_VID0	0	GPU Core VDD0 VID04	Strap to boot HVVDD
GPIO1	GPIO_VID3	0	GPU Core VDD0 VID3	Strap to boot HVVDD
GPIO2	LCD_BL_PWM	0	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	0	Panel Power Enable or Phase Shedding	LCD_VCC: 100k pull-down PSI: 10k pull-up or pull-down strap as needed to disable phase shedding by default
GPIO4	LCD_BLEV	0	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID0	0	GPU Core VDD0 VID0	Strap to boot HVVDD
GPIO6	GPU_VID2	0	GPU Core VDD0 VID2	Strap to boot HVVDD
GPIO7	3D/VID0	0	3D VPort Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	0	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	0	GPU Core VDD0 VID0	Strap to boot HVVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	0	GPU Core VDD0 VID5	Strap to boot HVVDD
GPIO14	HDP_AB	I	Hot Plug Detect for IFFAB	See Figure 76
GPIO15	HDP_C	I	Hot Plug Detect for IFFC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	0	Phase Shedding or Memory VDD VID	PSI: 10k pull-up or pull-down strap as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDDIQ
GPIO17	HDP_D	I	Hot Plug Detect for IFFD	See Figure 76
GPIO18	HDP_E	I	Hot Plug Detect for IFFE	See Figure 76
GPIO19	HDP_F	I	Hot Plug Detect for IFFF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

Reserve pull-up and down.
Don't have to install
component for default, NV
reply on 5/4. when system
no support CLKREQ

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				Date:	Tuesday, September 24, 2013	Sheet 21 of 59

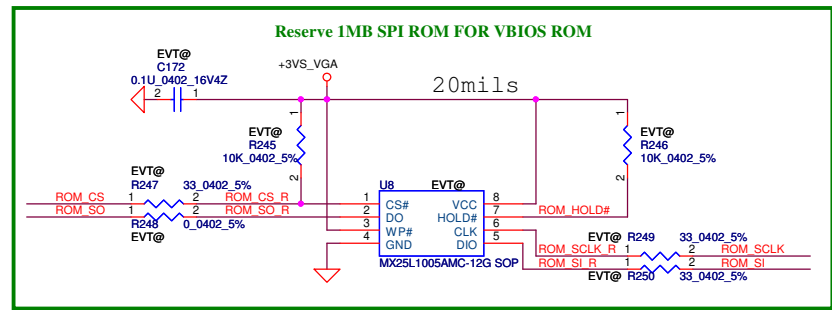
Table 66. N13x Family Display Link Summary

Link	Description
Link A	LVDS (Single Link or Dual Link with IFPB)
Link B	LVDS (Dual Link with IFPA)
Link C	DisplayPort, HDMI
Link D	DisplayPort, eDP
Link E	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI
Link F	DisplayPort, DVI (Dual Link with IFPE), HDMI

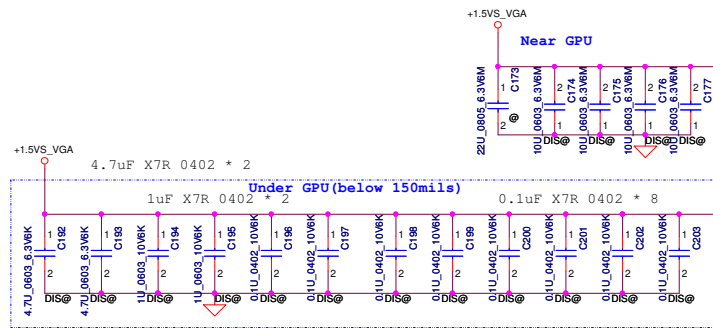


trace width: 16mils
differential voltage sensing.
differential signal routing.

Un-pop R244-0415 Update



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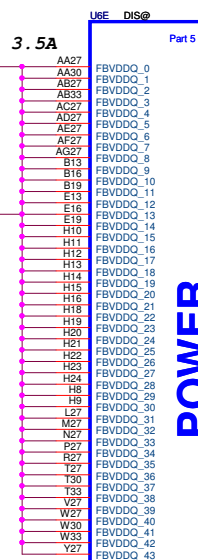
rise 1.5v system source voltage to 1.55-1.57V

Follow PUN-05893

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2ohm
FB_CAL_x_PU_GND	42.2ohm
FB_CAL_xTERM_GND	51.1ohm

+1.5V to +1.5VS_VGA

Supply from Power-0411 update.



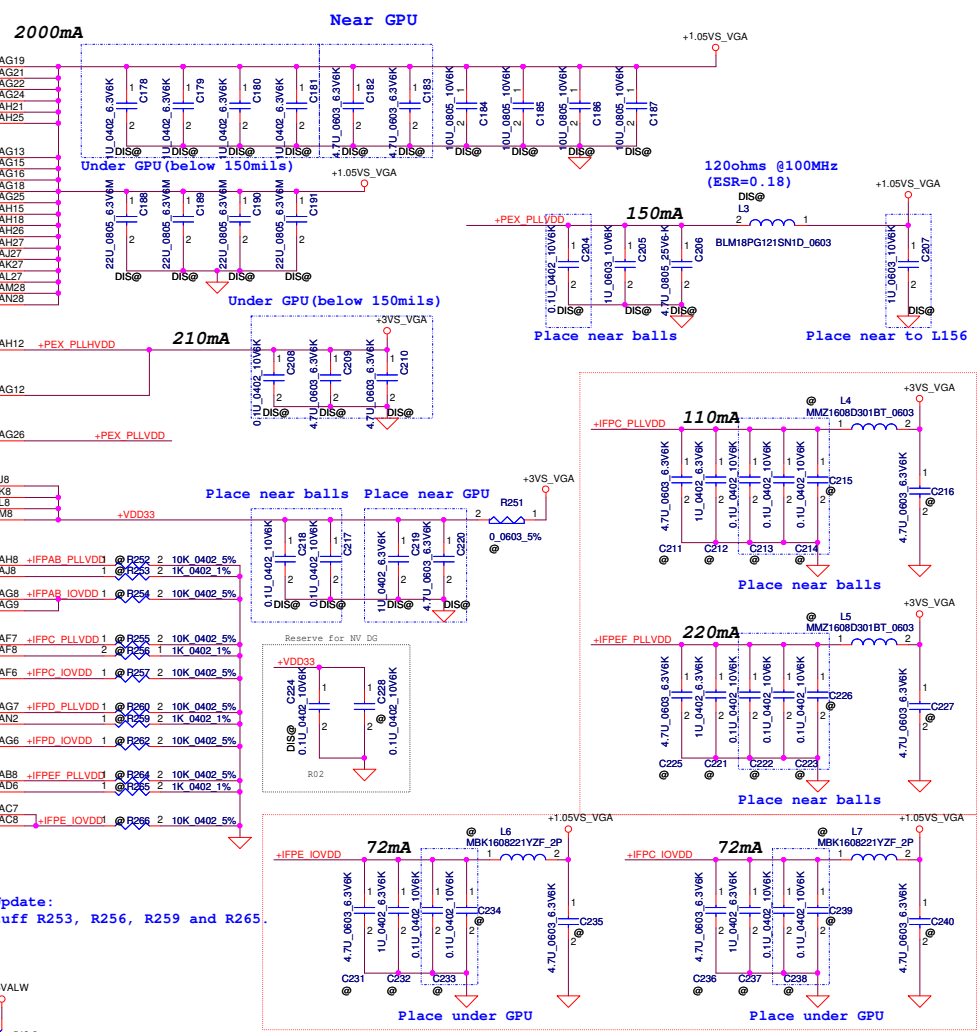
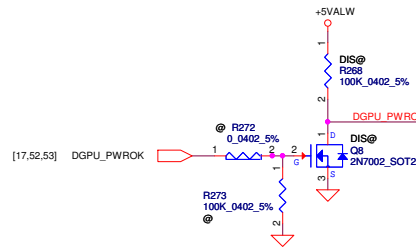
POWER

F1 FB_VDDQ_SENSE

F2 FB_GND_SENSE

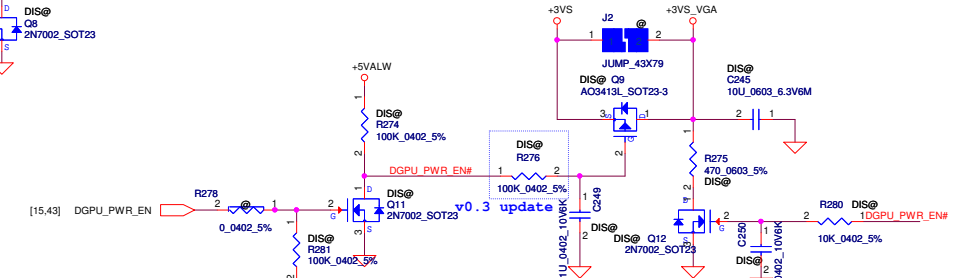
N14M-GE2-B-AIO-A2

4/3 Update:
Un-stuff R253, R256, R259 and R265.

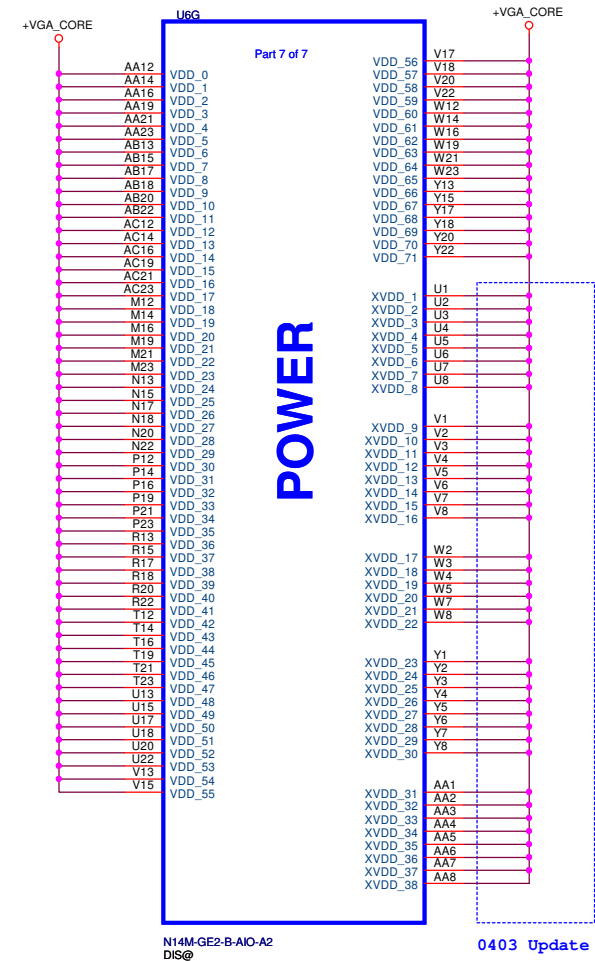
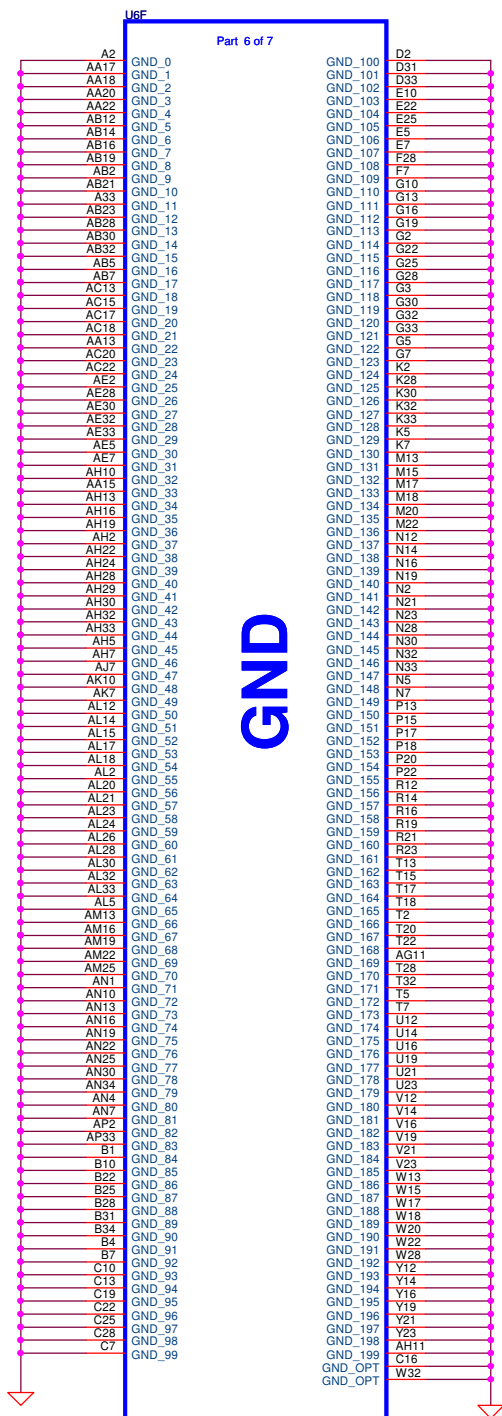


Un-pop update-0415

+3VS to +3VS_VGA



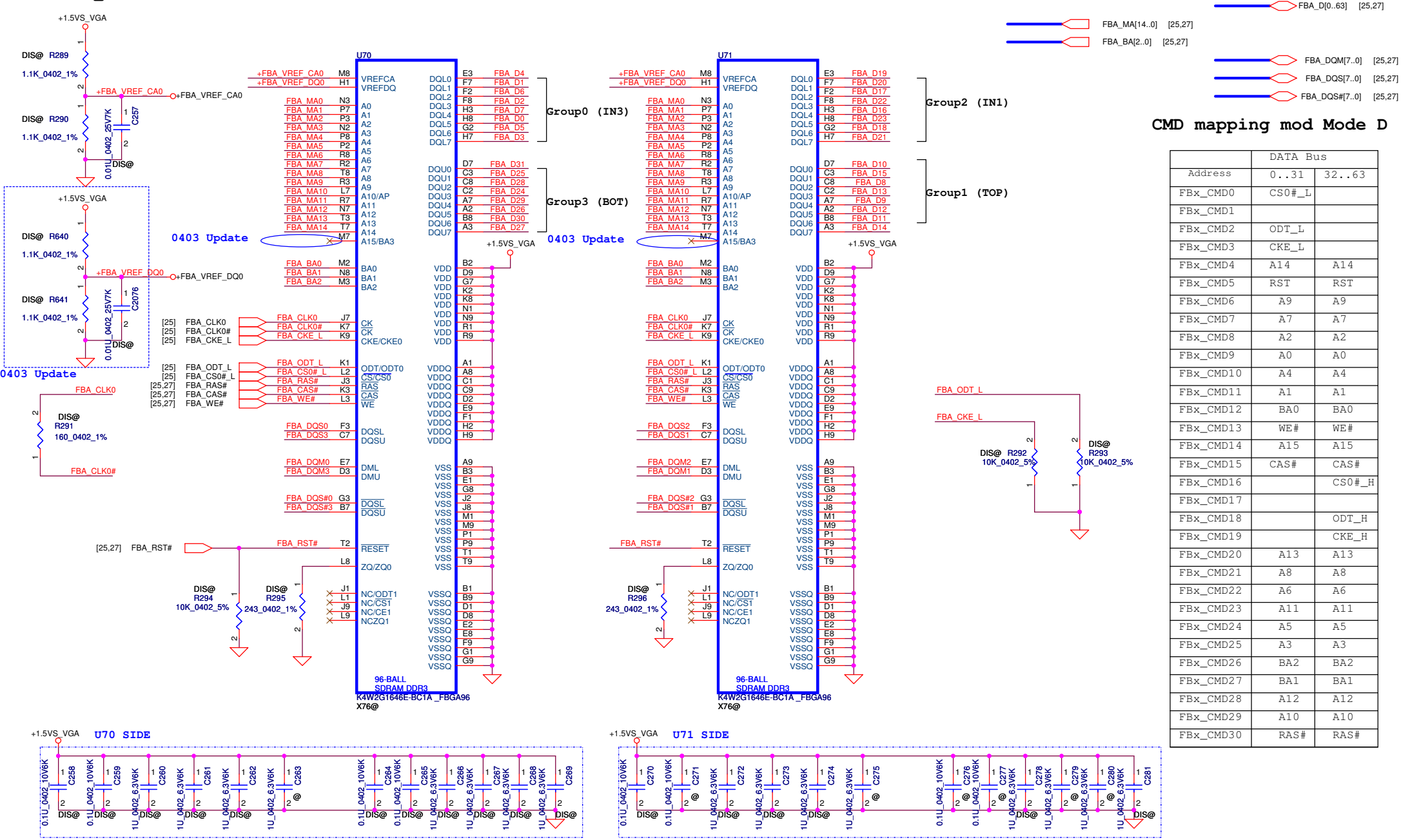
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								N14M-GE2-VGA CORE, GND	
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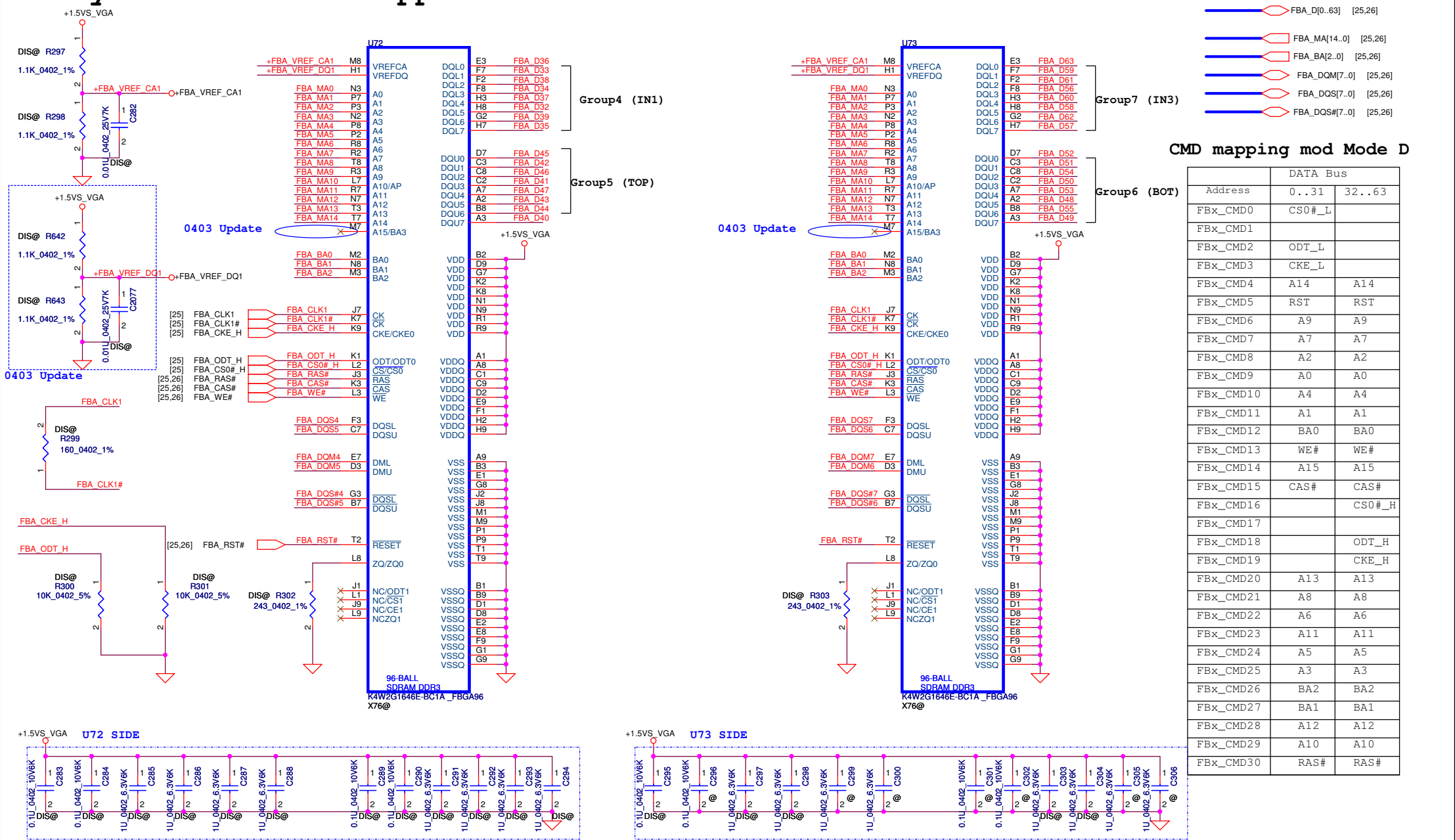


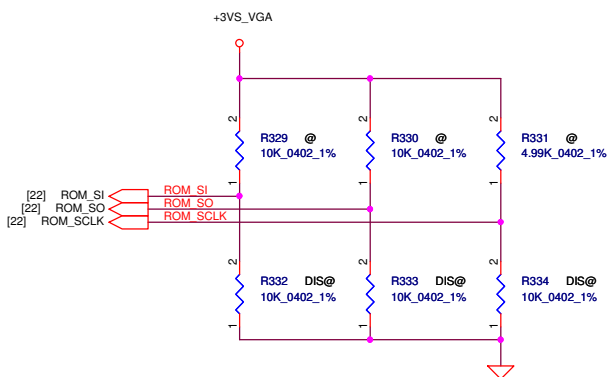
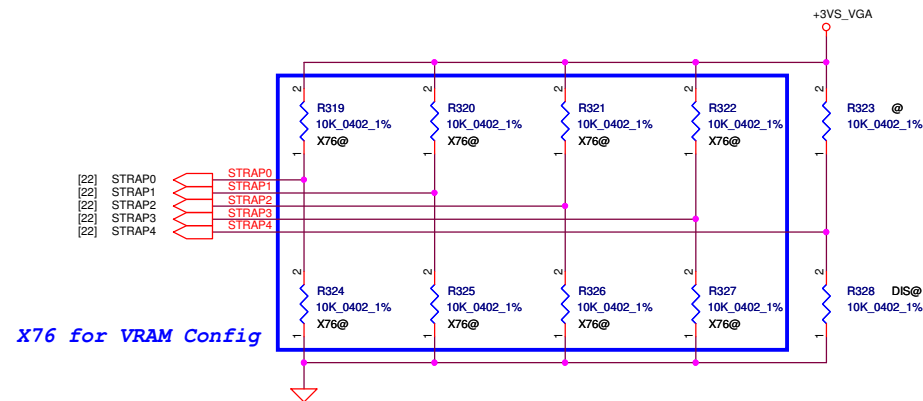
Memory Partition A - Lower 32 bits



Security Classification		Compal Secret Data		Title	
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Memory Partition A - Upper 32 bits





[PUN-06026-001]

Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

[VRAM Config-RVL-06366-001]

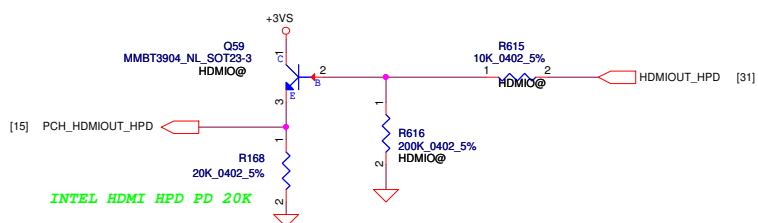
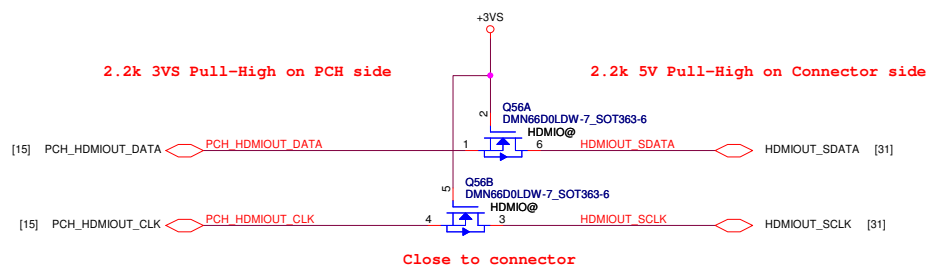
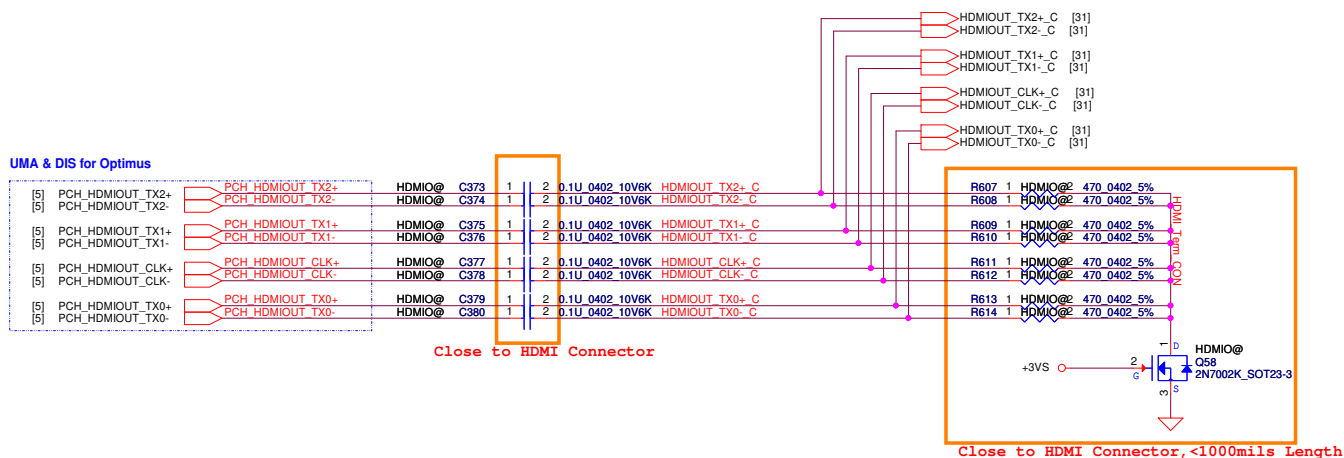
GPU	Frenq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0
N14M-GE2	900 MHz	128M* 16* 4 1GB	Hynix (0x6) H5TQ2G63BF8-11C SA00003YO10	0 R327 PD 10K	1 R321 PU 10K	1 R320 PU 10K	0 R324 PD 10K
			Samsung (0x5) K4W2G1646E-BC11 SA00005SH00	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Micron (0x1) MT41J128M16JT-107G:K SA00005SM30	0 R327 PD 10K	0 R326 PD 10K	0 R325 PD 10K	1 R319 PU 10K
N14M-GE2	900 MHz	256M* 16* 4 2GB	Micron (0xD) MT41K256M16HA-107G:E SA000065D20	1 R322 PU 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Samsung (0xB) K4W4G1646B-HC11 SA000068R10	1 R322 PU 10K	0 R326 PD 10K	1 R320 PU 10K	1 R319 PU 10K
			Hynix (0x4) H5TC4G63AF8-11C SA00006E800	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	0 R324 PD 10K

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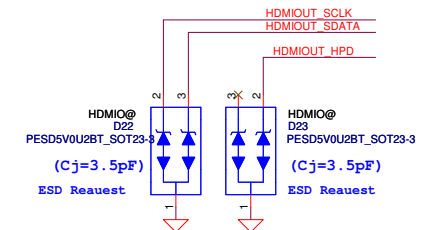
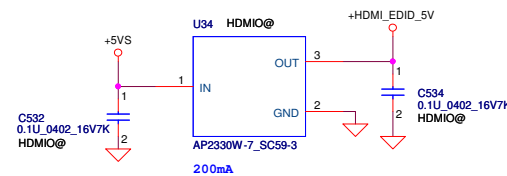
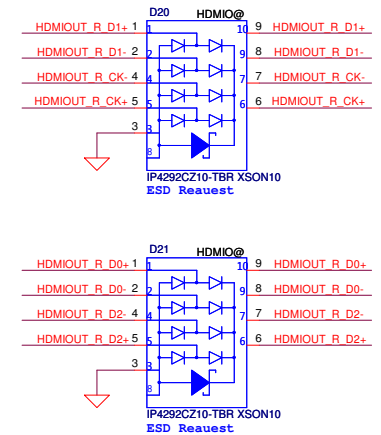
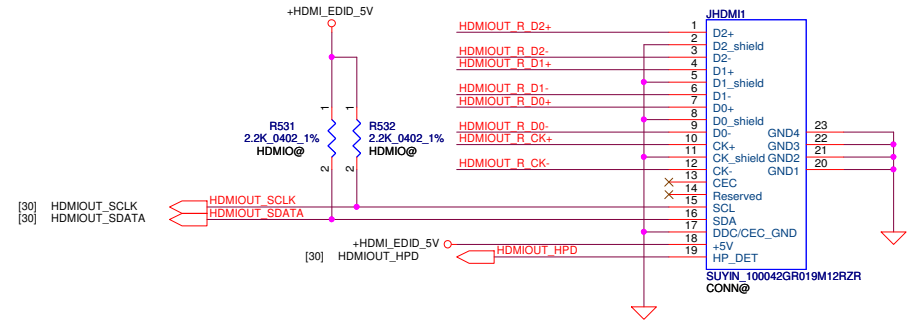
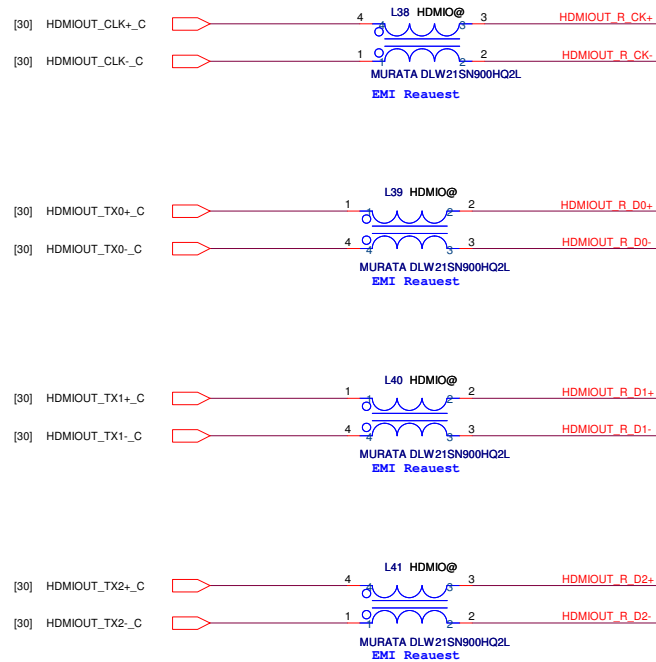
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UMA & DIS for Optimus

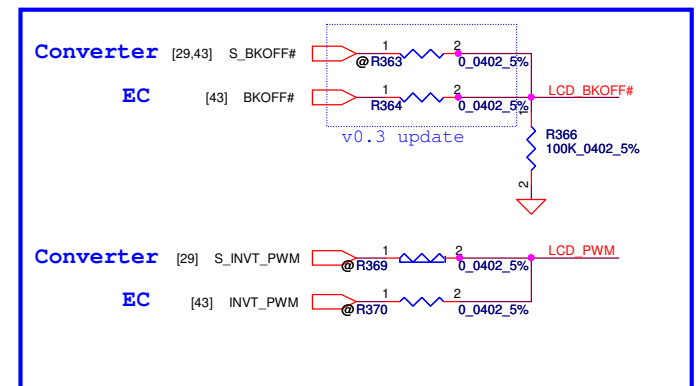
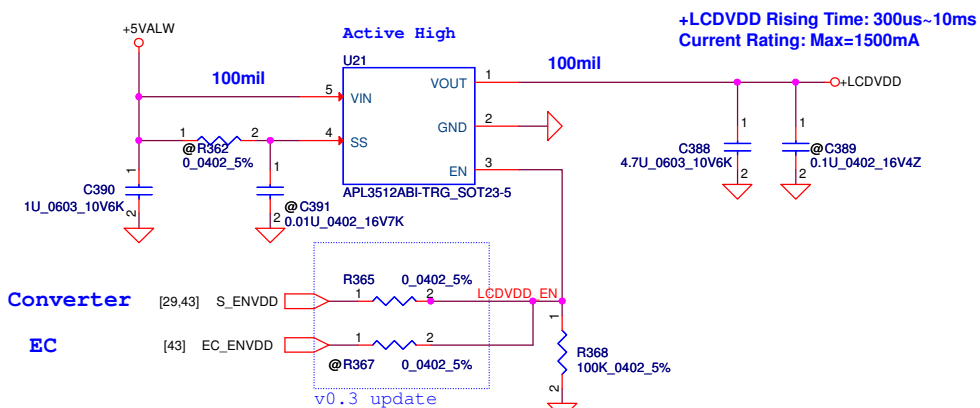
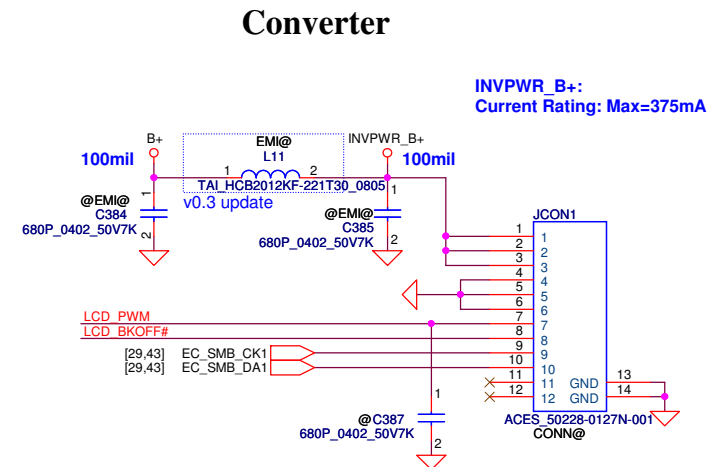
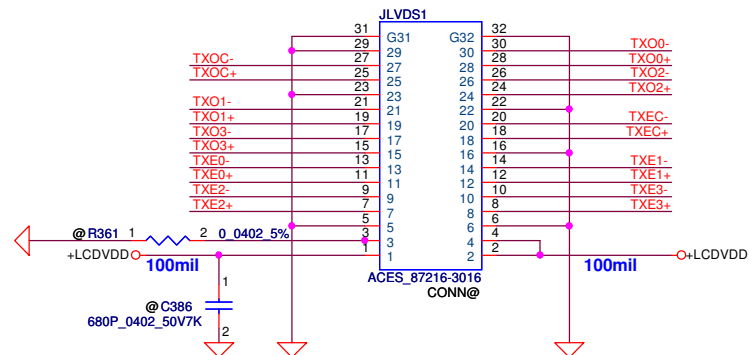


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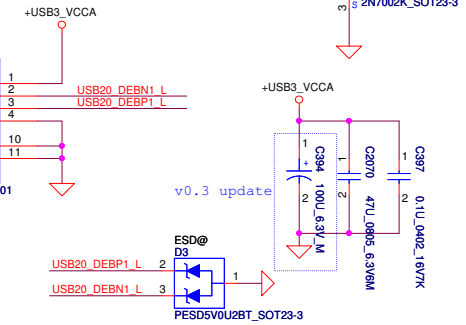
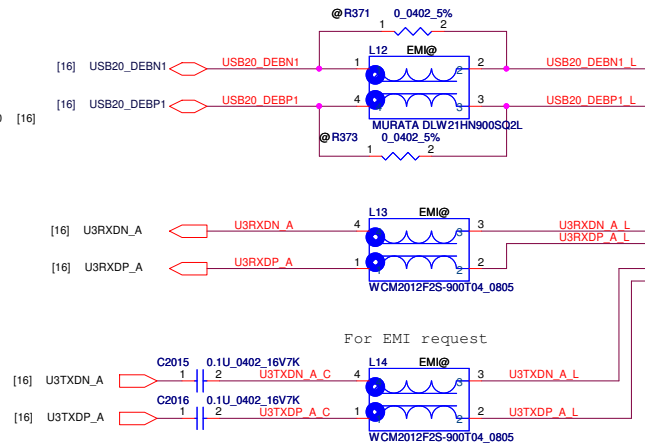
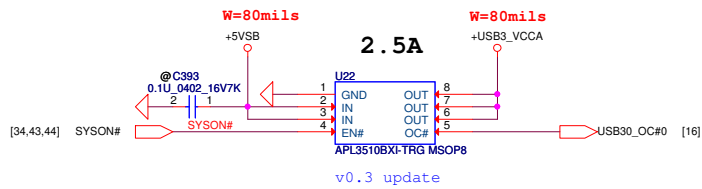
HDMI-OUT Connector



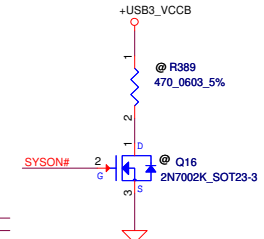
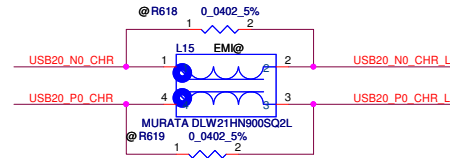
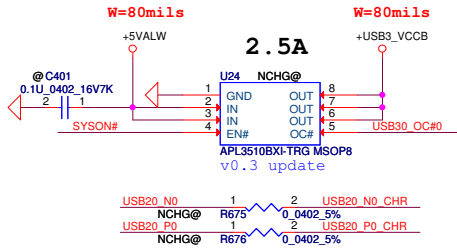
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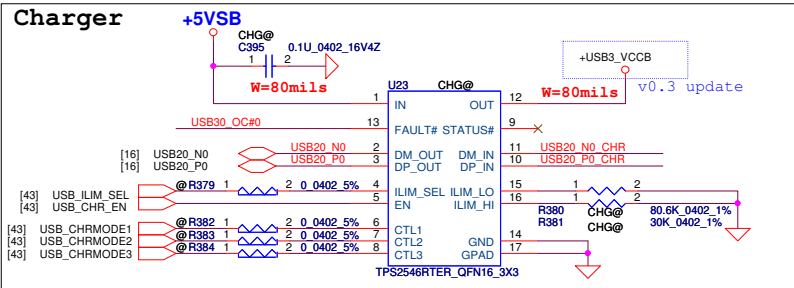
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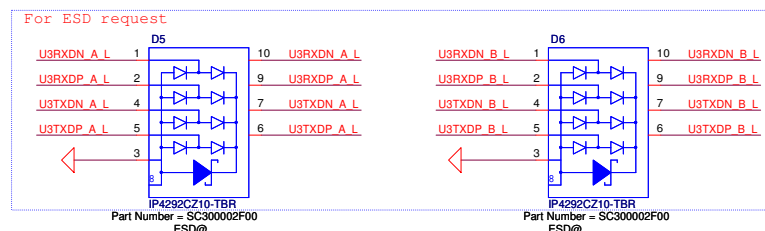
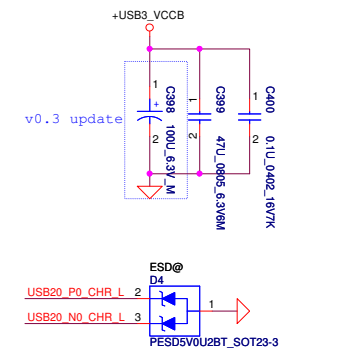
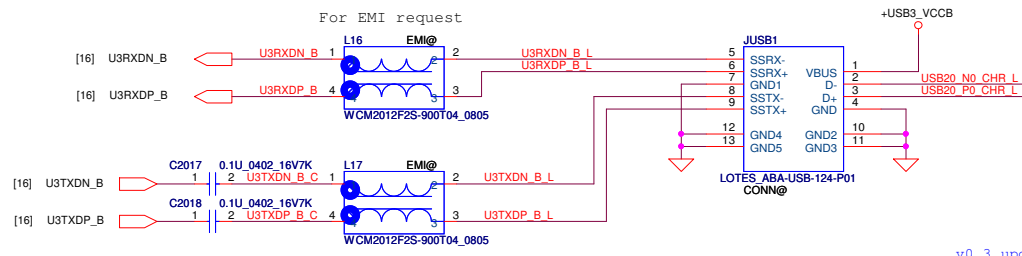
Non Changer



Charger



Charge USB Port



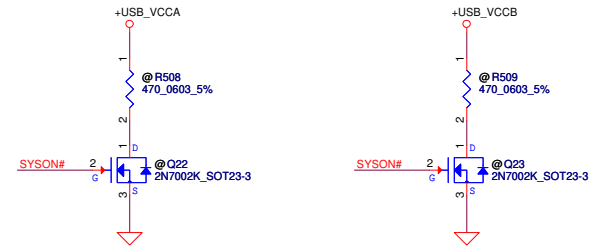
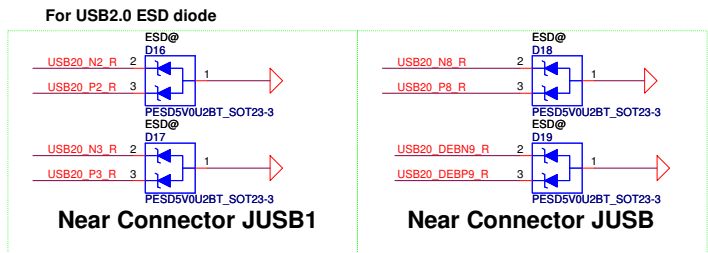
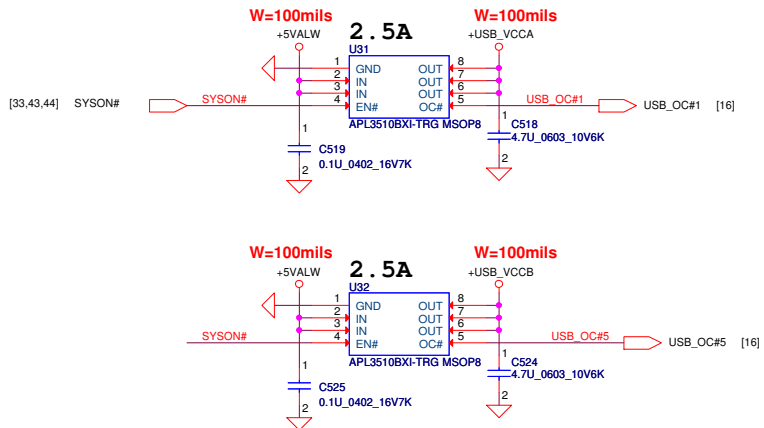
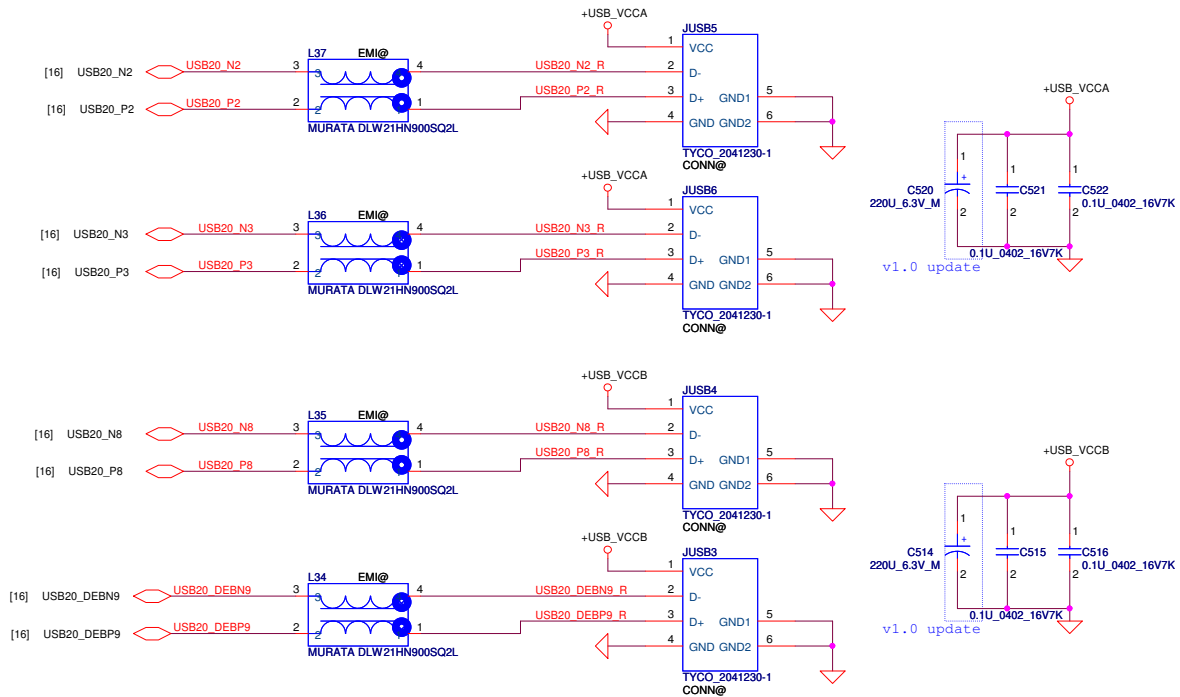
Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPIOA07(pin104)	GPIO22(pin41)	GPIOA11(pin108)	GPIO12(pin40)
S0 (CDP)	1	1	1	1
S3 (SDP)	1	1	1	1
S4/S5 (DCP)	0	0	0	0

System Global Power State	TPS2546/TPS2544 Mode	Charging	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP		1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs		1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no house		0	0	0	1	ILIM_HI

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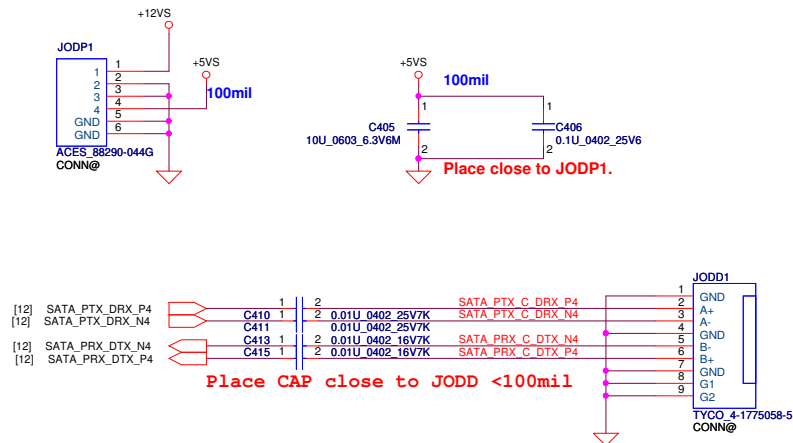
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USB20

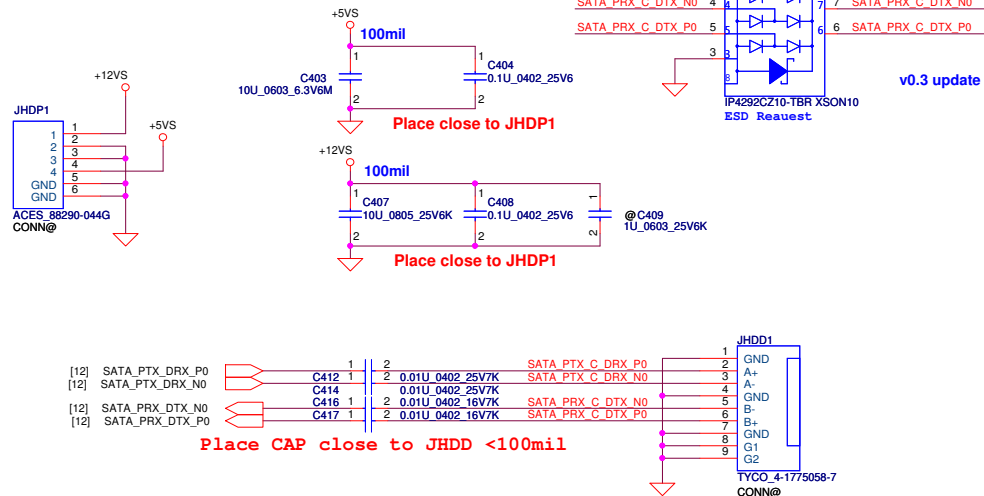


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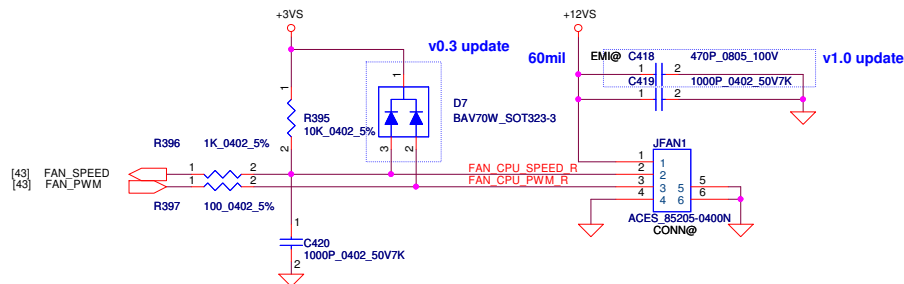
SATA ODD Conn



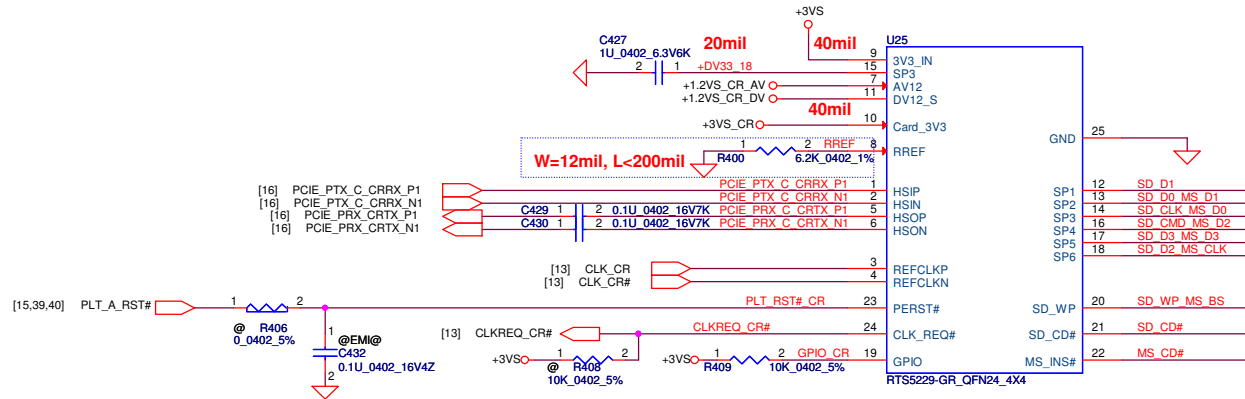
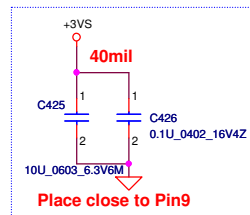
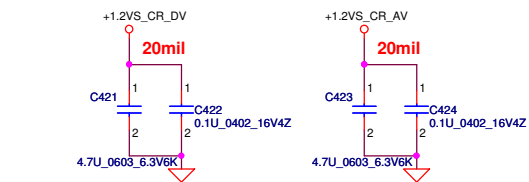
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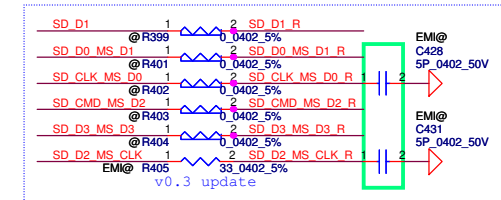
FAN Control Circuit



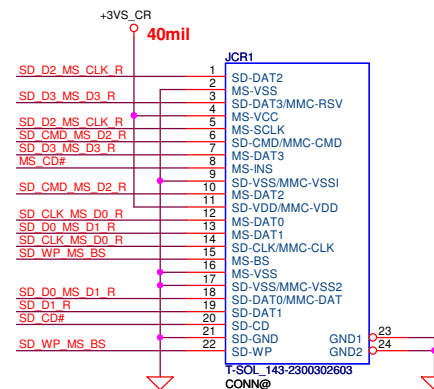
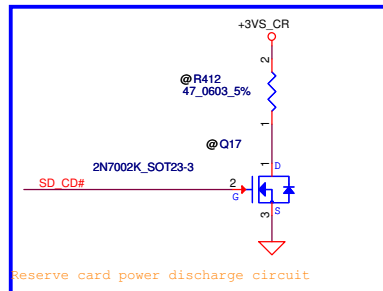
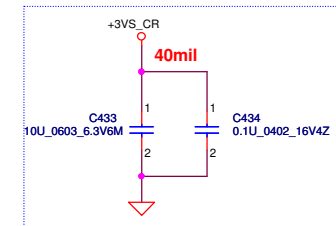
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/04/01	Deciphered Date	2014/04/01	Title	SATA-HDD/ODD/USB	
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					ZEA00 LA-A061P M/B	0.3
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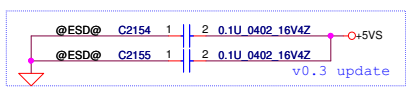
Length of per trace 2inch no more 2 via
mismatch trace length <100mil
50ohm +/-15% impedance.



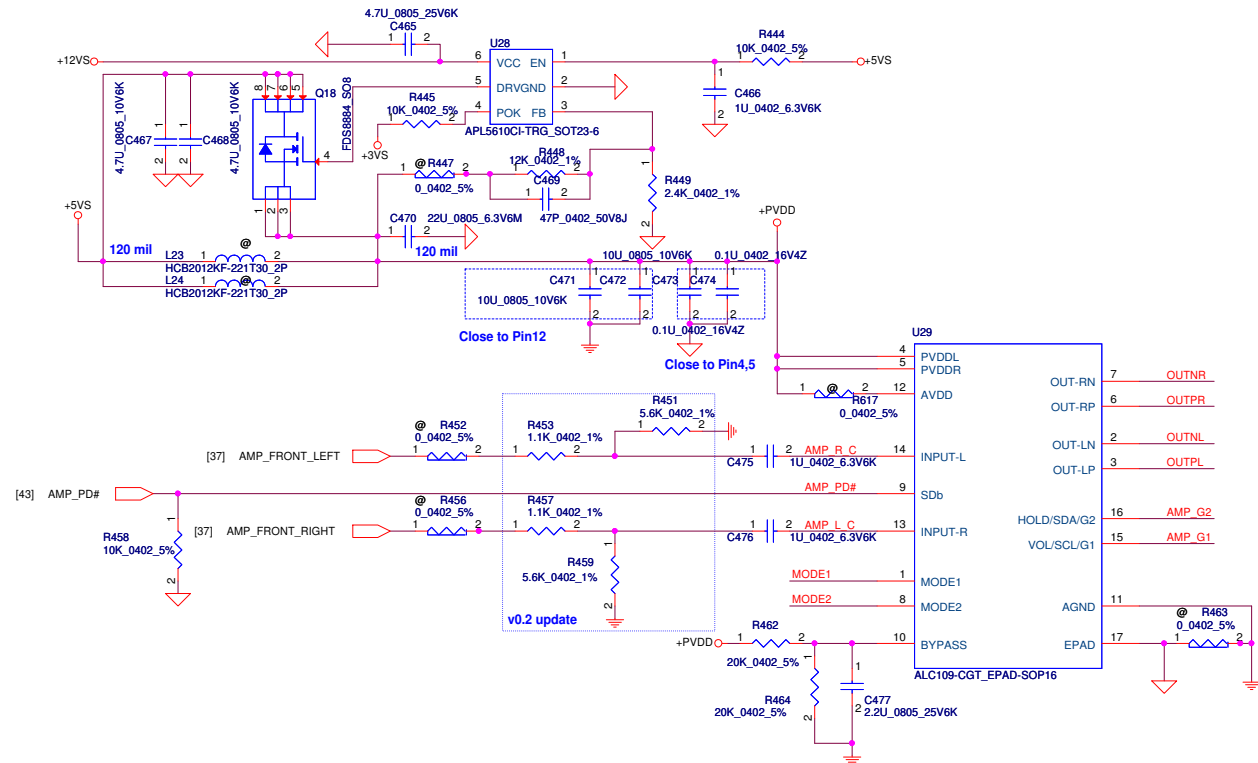
Place close to JCR1 pin 12,21



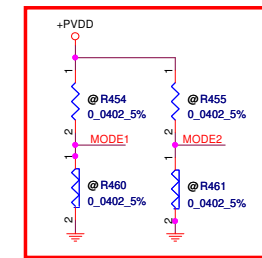
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/04/01	Deciphered Date	2014/04/01	RTSS5229 Media Card Controller	
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				Custom	0.3
				Date:	Tuesday, September 24, 2013
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$V_o = 0.8 (1 + R_{606} / R_{607})$
 Output: 4.8V
 Max I: 7.5A

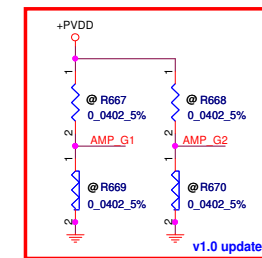


Mode selet: Fix Gain



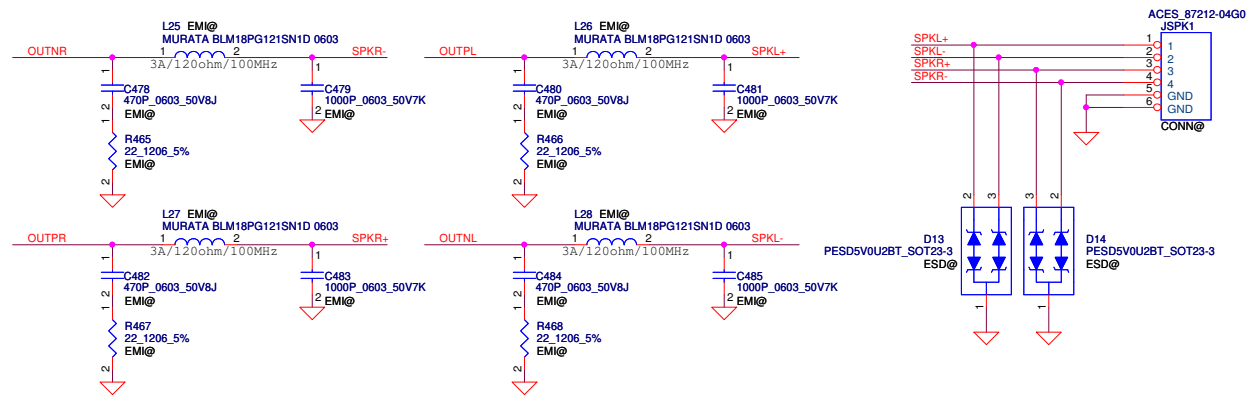
Model1	Model2	Option	Pin15	Pin16
0	0	Fixed Gain	G1	G2
0	1	I2C	SCL	SDA
1	0	PWM	PWM	Hold
1	1	DC	DC	Hold

Gain Select

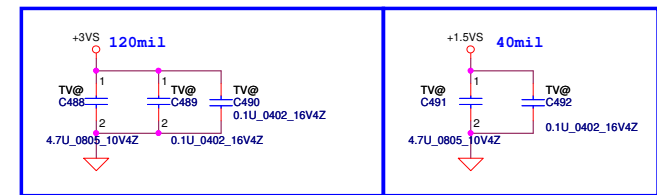


AMP_G1	AMP_G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

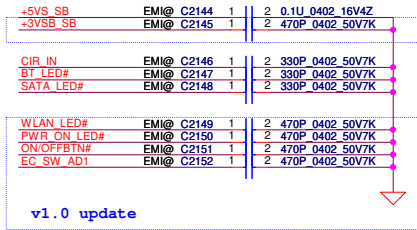
(Default)

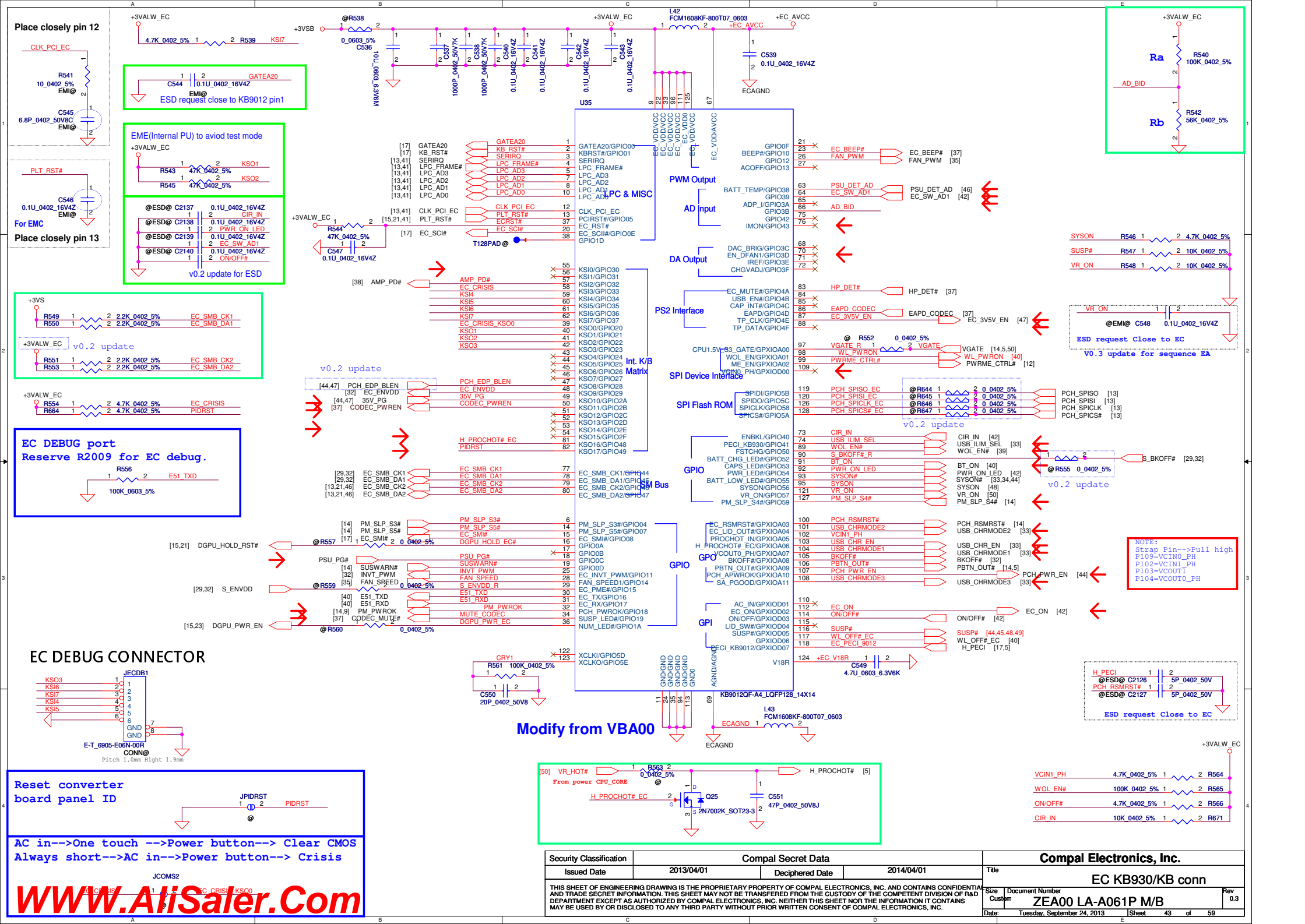


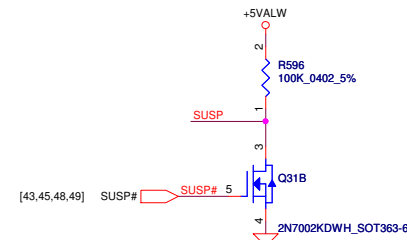
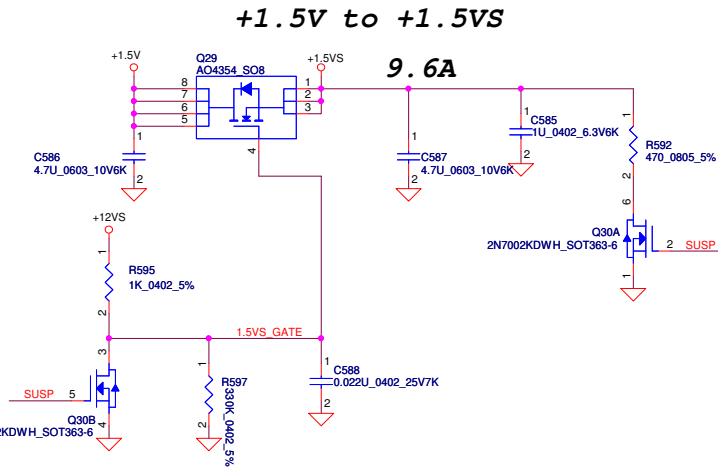
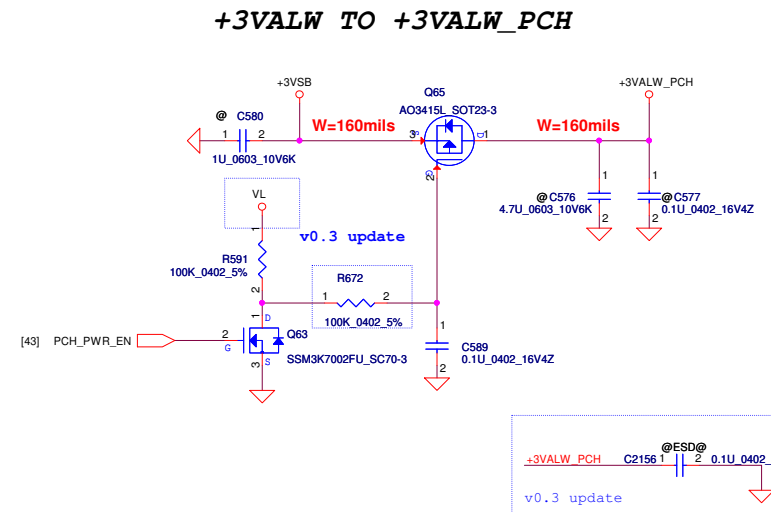
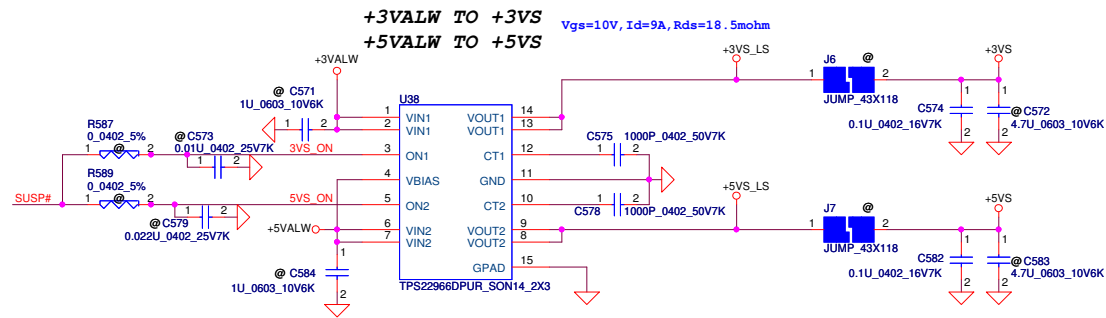
Mini Card Slot 1---TV tuner Current: +3VS : 2750mA, 1.5V: 500mA



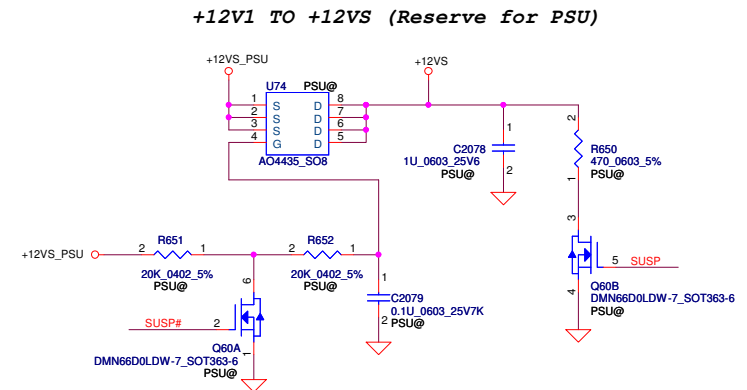
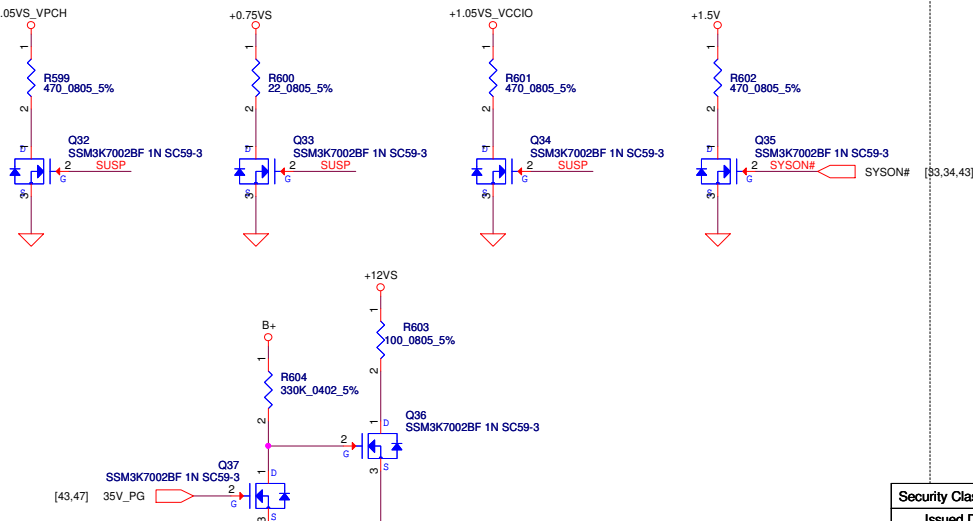
8Pin sub-board Connctor



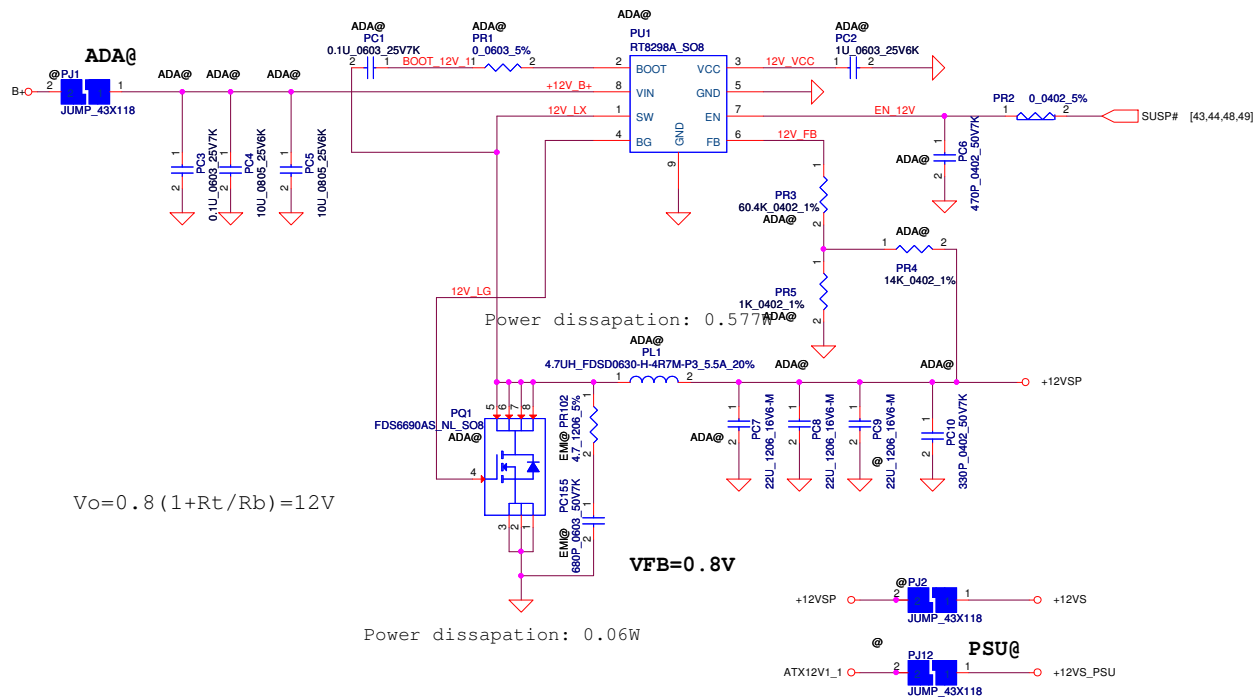




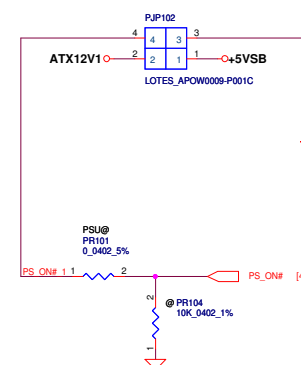
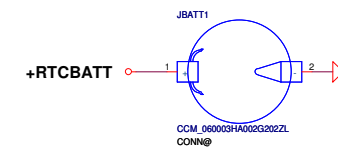
Discharge circuit



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				Size	Document Number
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				Rev	0.3
				Date	Tuesday, September 24, 2013
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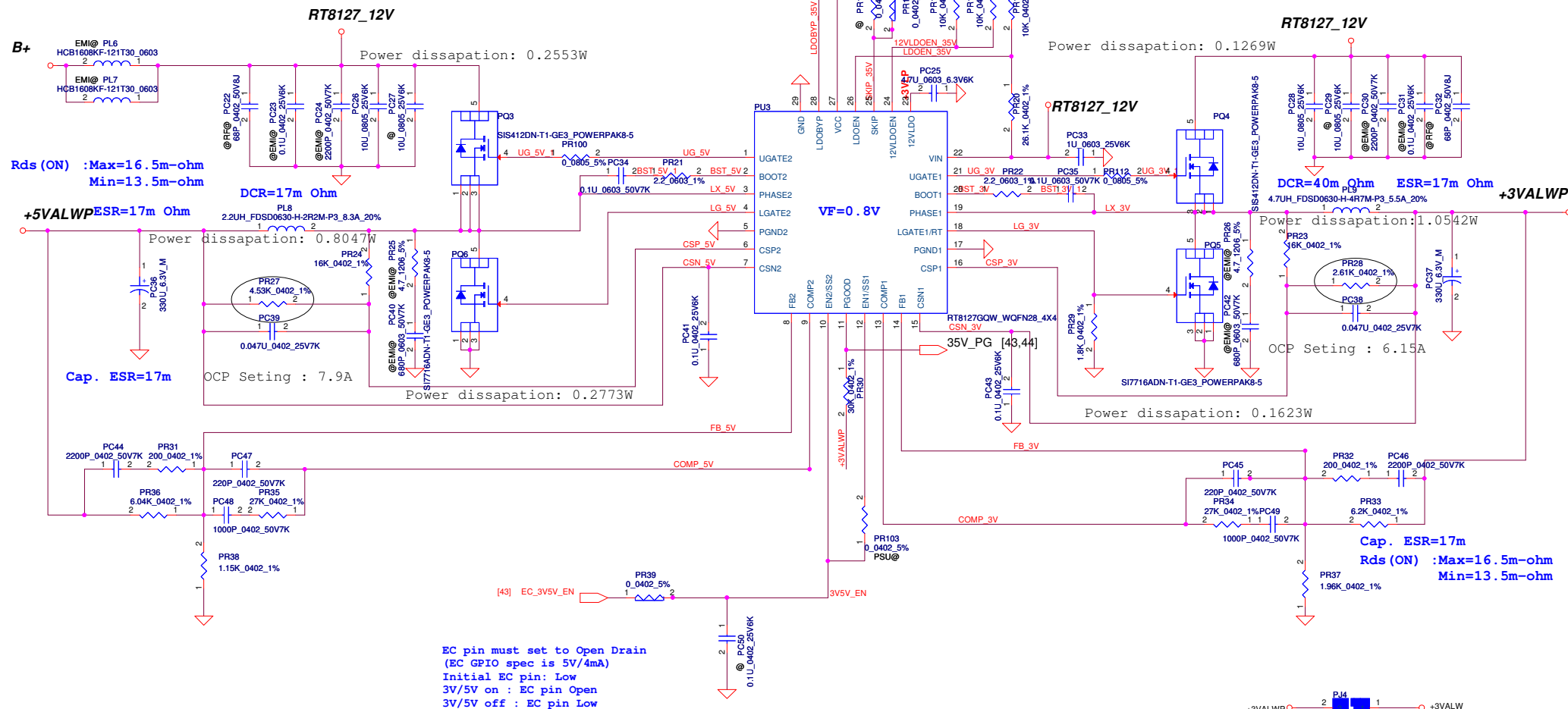


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				Deciphered Date				PWR- 12VSP			
				2013/04/27				Document Number			
								VB111 LA-A111 M/B			
								Date: Tuesday, September 24, 2013			
								Sheet 45 of 56			



Ventura for CPU side
slave address : 1000001
please placemnet near R-sense

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				Size C	Document Number	Rev 0.1
				Date:	Tuesday, September 24, 2013	Sheet 46 of 56



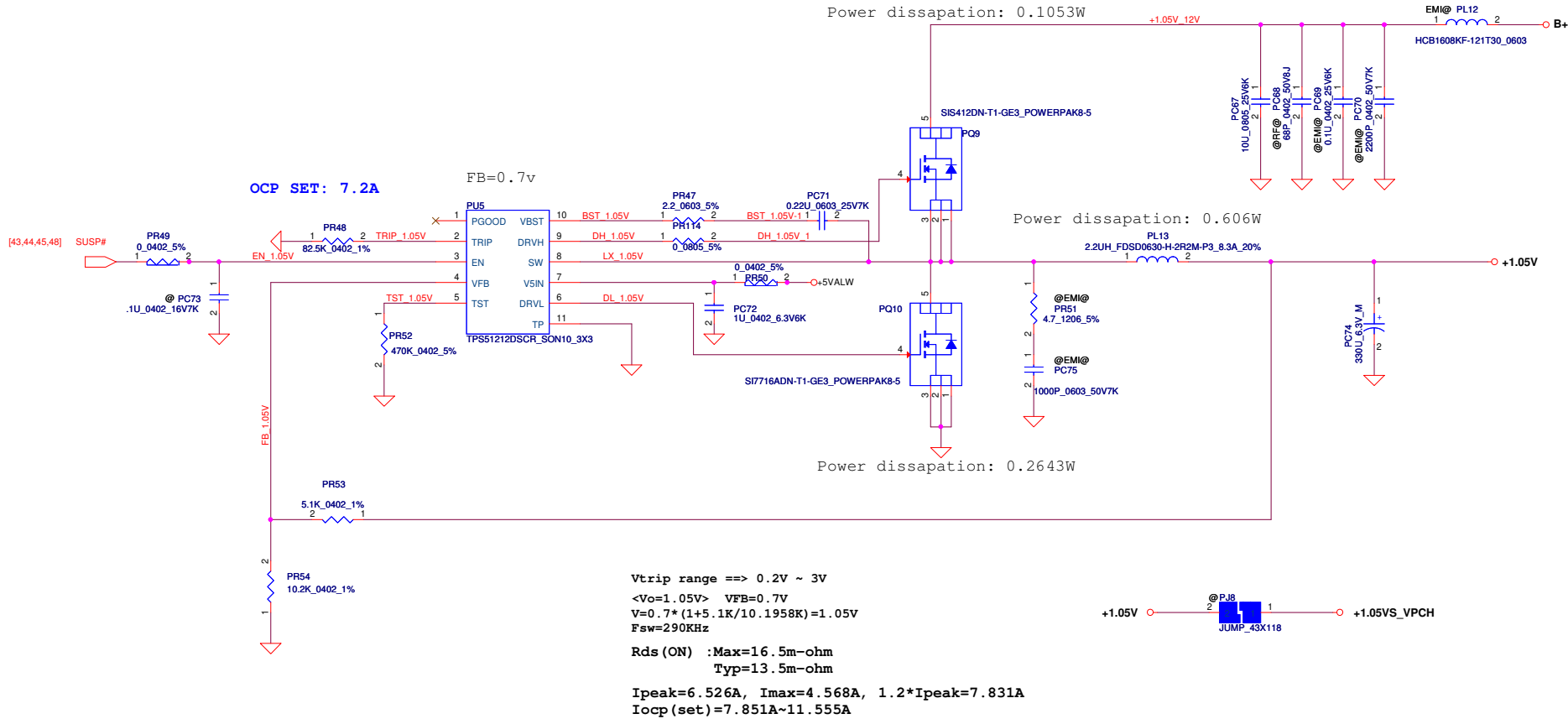
+V_5VP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
Fsw=300K,
Iocp>=8.66A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

+V_3.3VP
Ipeak=4.437A ; 1.2Ipeak=5.325A; Imax=3.106A
Fsw=300K
Iocp>=5.33A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

WWW.AliSaler.Com

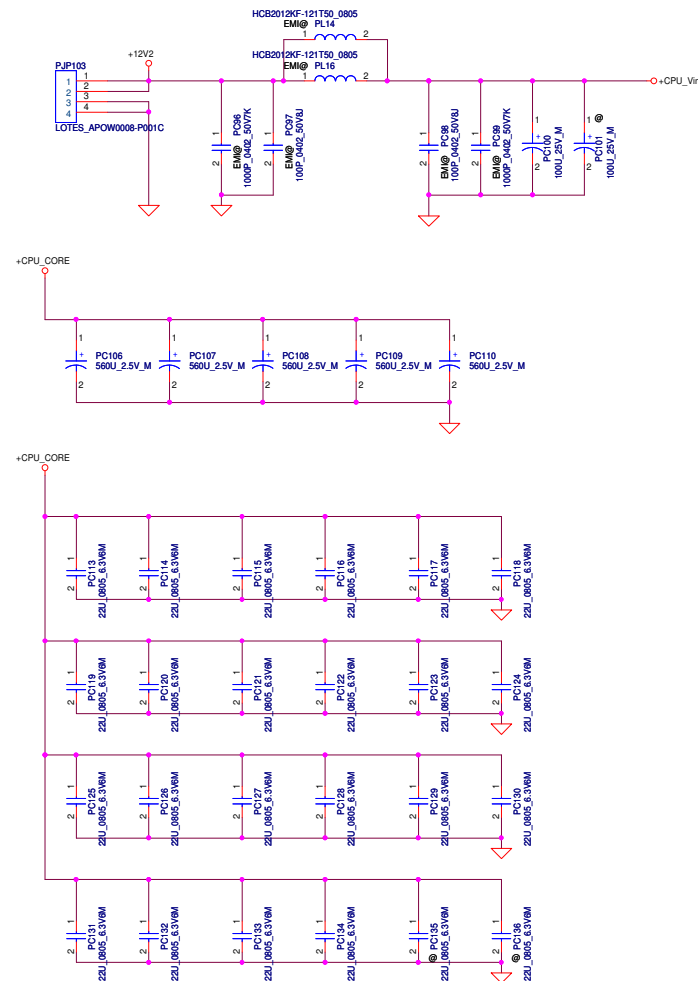
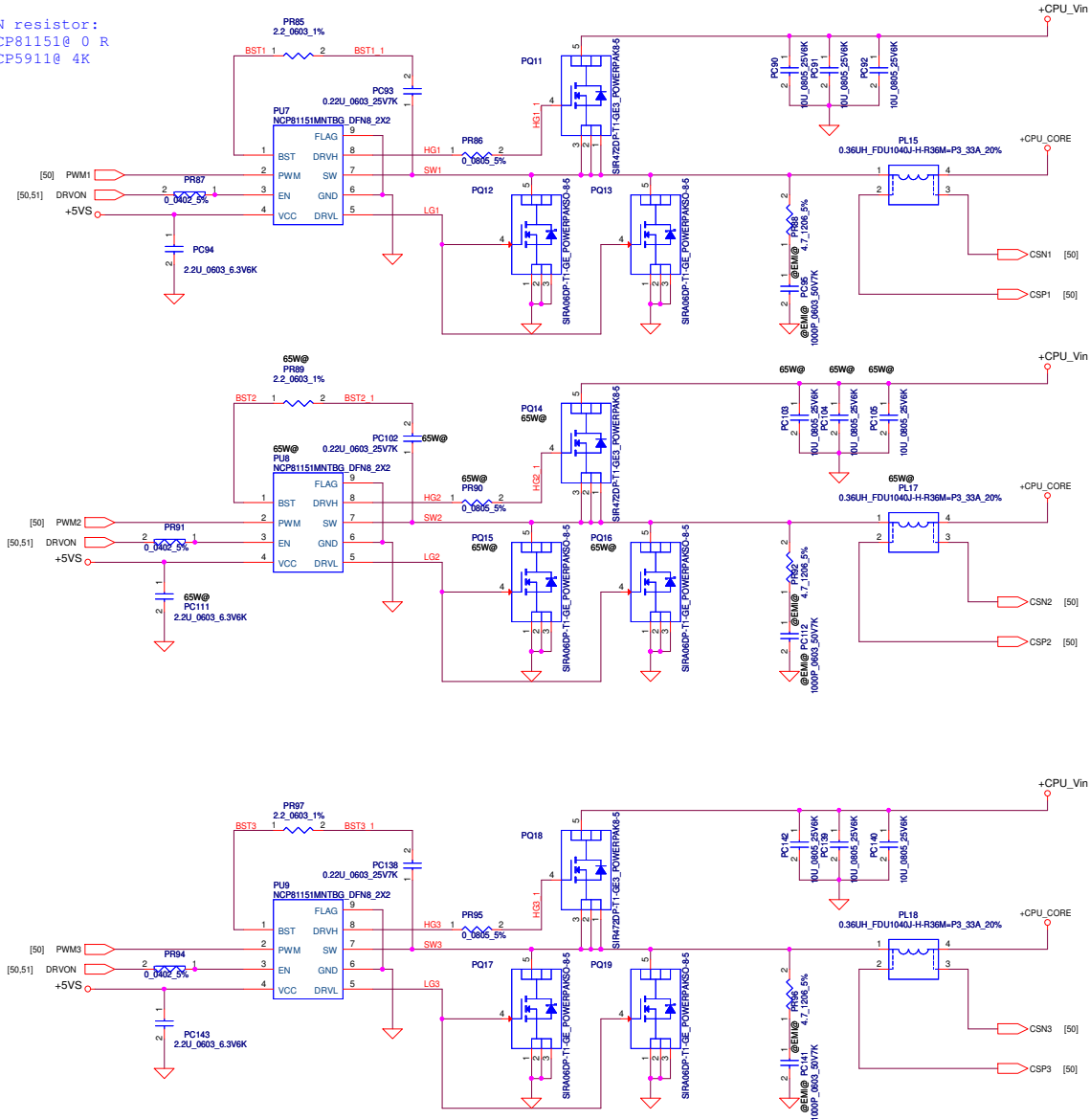
TON (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=300KHZ (+3VALWP)

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Issued Date	2012/09/01	Deciphered Date	2013/12/31	Compal Electronics, Inc.	
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				PWR- 3VALWP/5VALWP	0.1
				VCA00 LA-9792P M/B	
				Date: Tuesday, September 24, 2013	Sheet 47 of 56



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				Date	Tuesday, September 24, 2013
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EN resistor:
NCP81151@ 0 R
NCP5911@ 4K

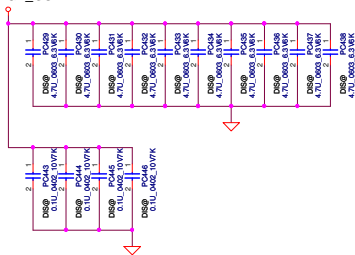


Title		
Power Stage		
Size	Document Number	Rev
VCA00	LA-9792P-M/B	0.1
Date:	Tuesday, September 24, 2013	Sheet 51 of 56

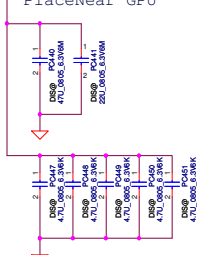
Design for
N14M-GE2

Follow GB4-128 demand

+VGA_CORE Place Under GPU



+VGA_CORE PlaceNear GPU

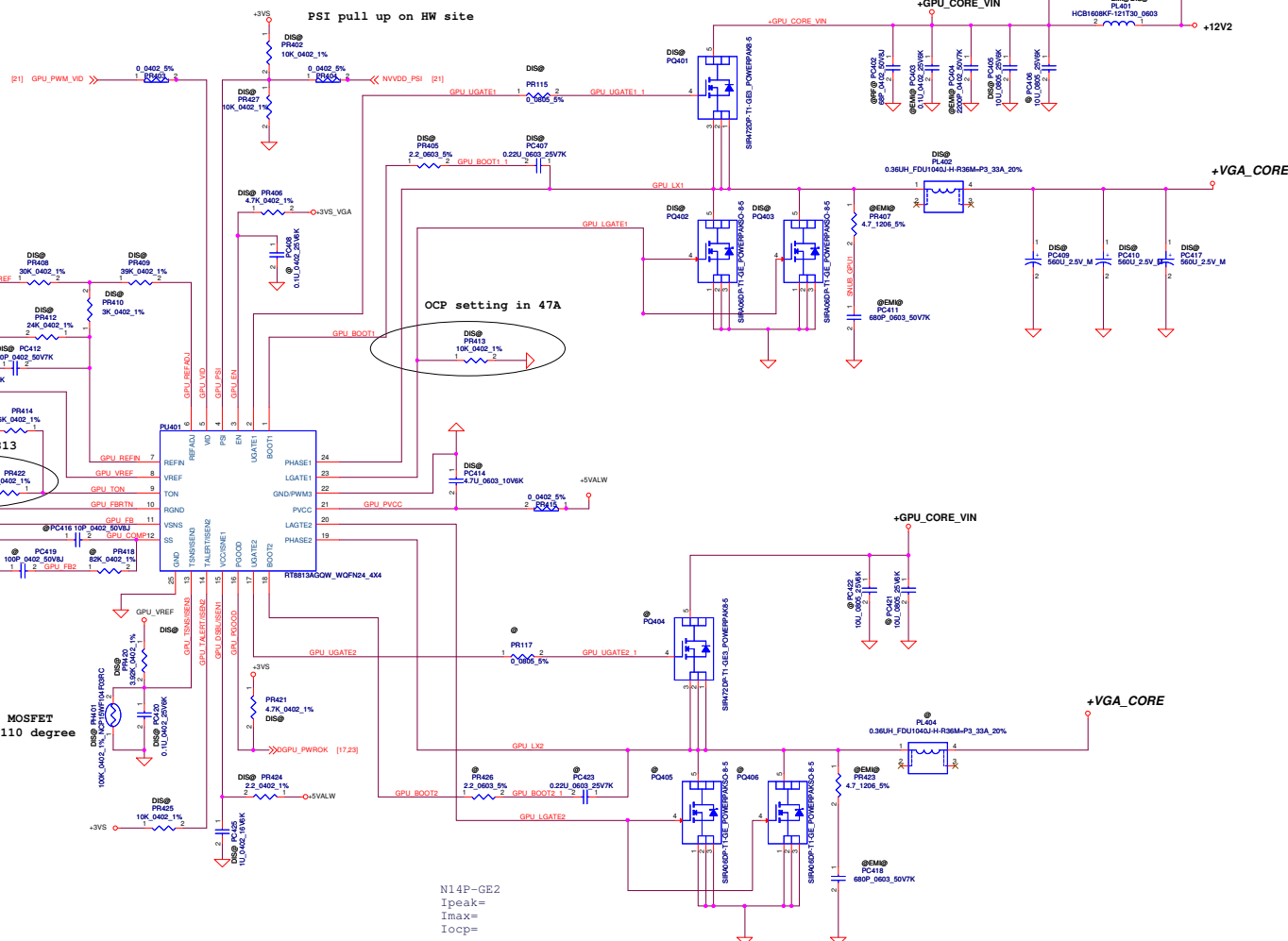


PH701 close to MOSFET
Trigger point 110 degree

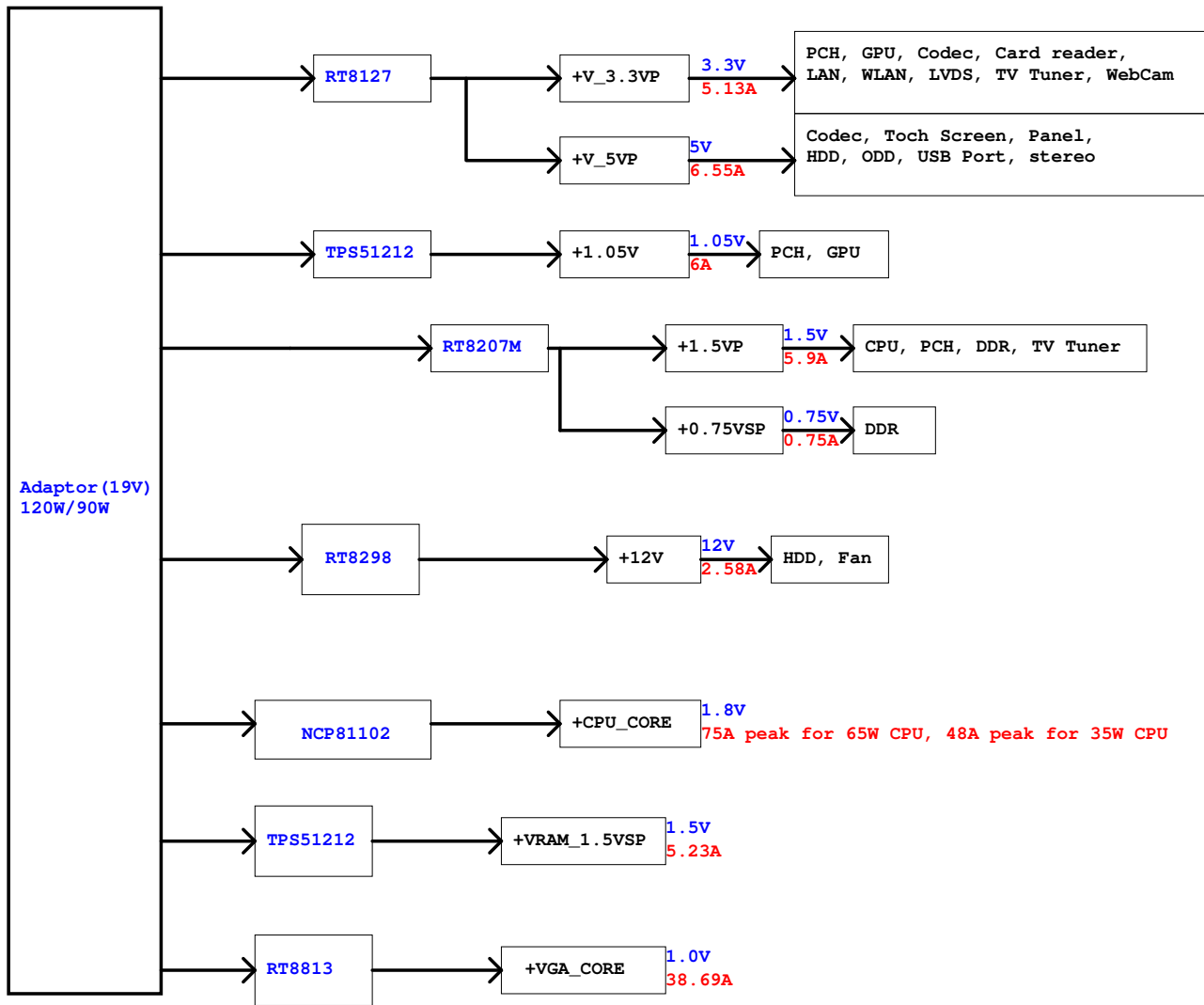
For RT8813
+GPU_CORE_VIN

N14P-GE2
Ipeak=
Imax=
Iocp=

OCP setting in 47A
DIS@ PR413
10K_0402_1%

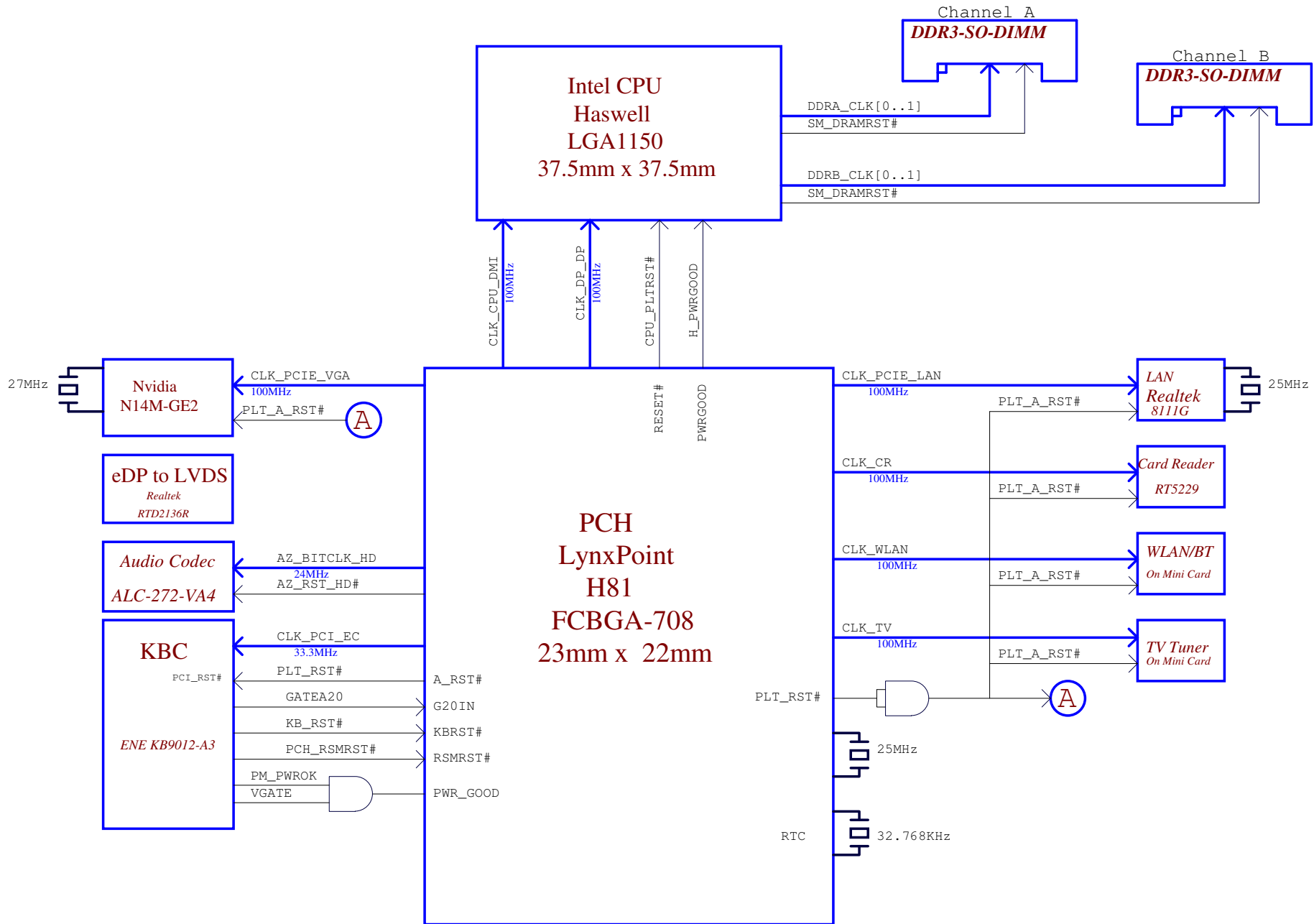


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				Date	Tripoli
				Version	September 24, 2013
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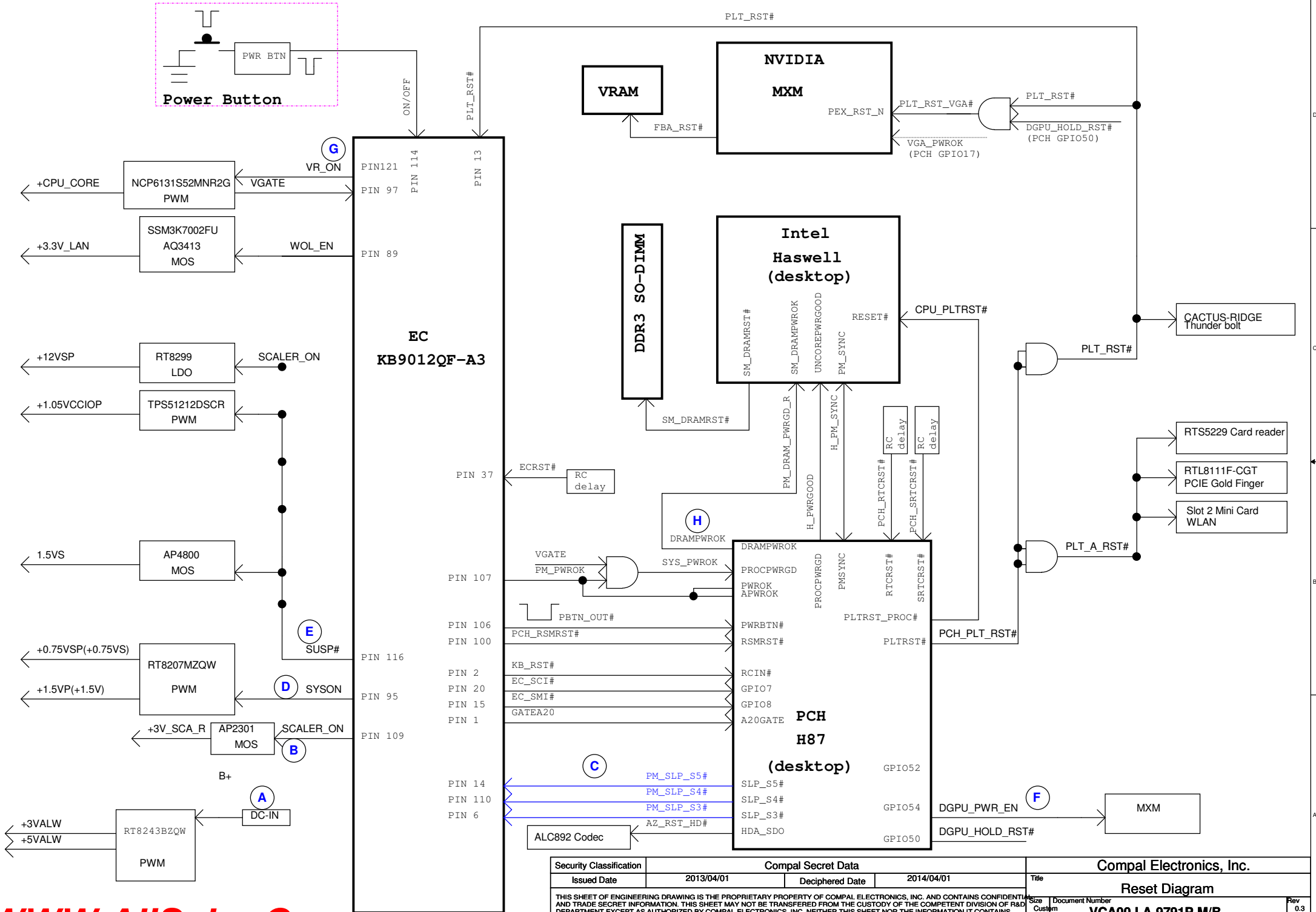
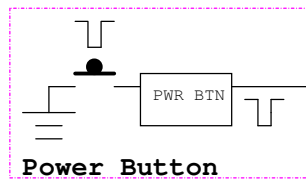


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Clock and Reset Diagram



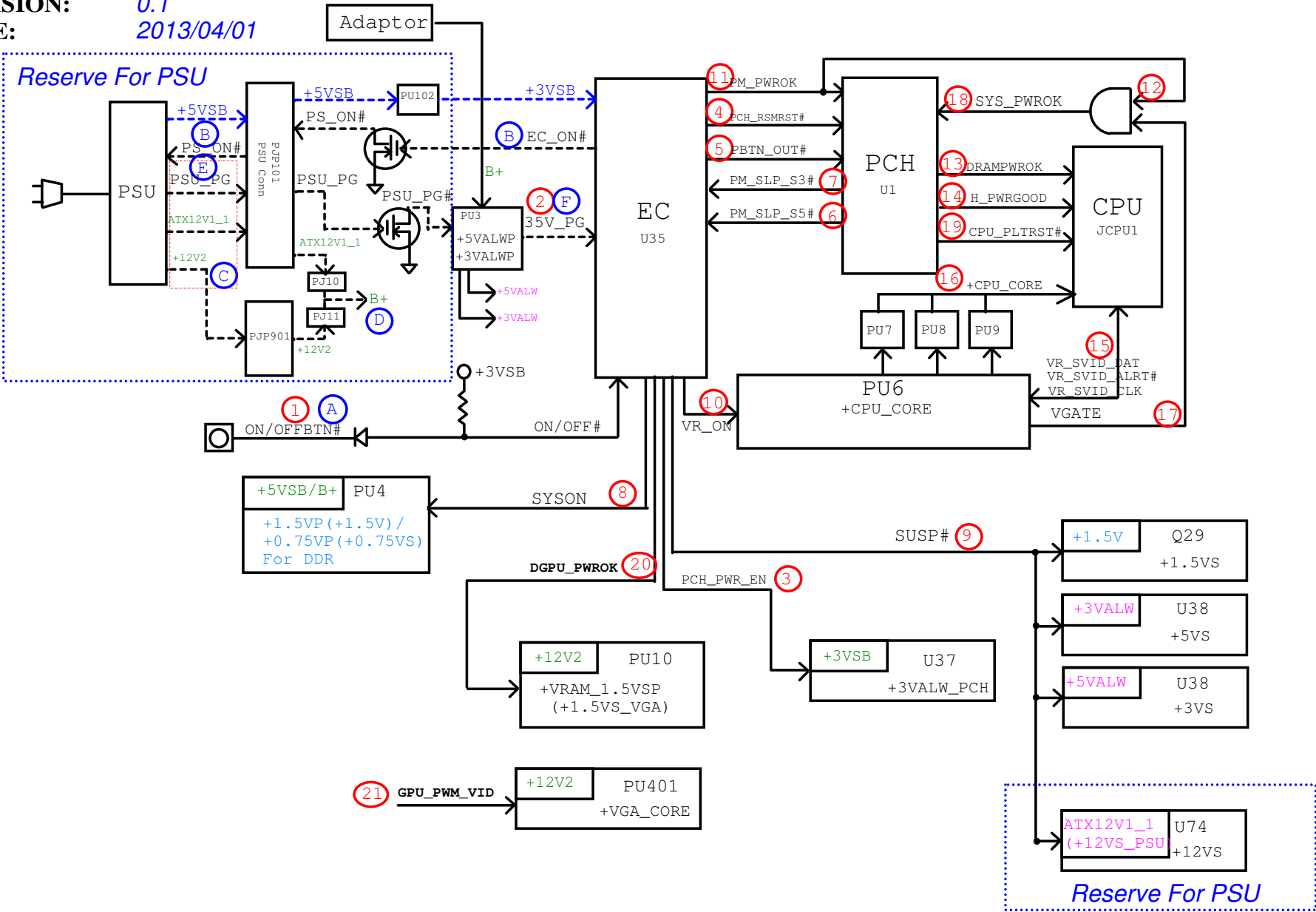
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				Document Number
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				0.3
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NO		DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	20130604	P47		Add PC154 and Change the pu101 to SA00005A600	For Pericom issue
2.	20130729	P45		Add PR105 ,PC155 Shaber	For ENI Request
3.	20130729	P45		Add PR1	For ENI Request
3.	20130729	P45		Add PR39	For S5 power loss issue

COMPAL CONFIDENTIAL

MODEL NAME: ZEA00 Power Sequence Block Diagram (Discrete)
PCB NAME: LA-A061P
REVISION: 0.1
DATE: 2013/04/01



HW PIR (Product Improve Record)

ZEA00 LA-A061P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 --> 0.2

GERBER-OUT DATE: 2013/06/20

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1.			Change C45 from SF000002V00 to SF000003X00	
2.			Change +LCDVDD enable control from EC to LVDS convertor,un-pop R367 and R365 change short pad.	
3.			Change LCD_BACKLIGHT control from EC to LVDS convertor,un-pop R364 and R363 change 0 ohm.	
4.			Remove un-used components(U18,R335,R336,C357,C359,C360,R338,R339) for eDP to LVDS convertor.	
5.			Pop R428 for AZ_SDIN0_HD.	
6.			U2 footprint change from socket to IC.	
7.			Add RH11	
8.			Change Y2 from SJ10000CU00 to SJ10000DE00,change C106 & C107 from 27pF to 4.7pF	
9.			Change R423 location to L45	
10.			Change D7 from SC2N202U010 to SC600000B00 for 替代料	
11.			Change Q29 from SB548000210 to SB000002N00.	
12.			Change D8&D9 from SCS00002G00 to SCS00000Z00	
13.			X1 code change:1.Change Q2,Q3,Q4,Q5,Q30,Q31 from SB01000JE00 to SB00000EO00. 2.Change Q9 from SB934130020 to SB934130000. 3.Change Q10 from SB00000FC00 to SB00000F400. 4.Change L1 from SM01000JE00 to SB01000JN00.	
14.			Change R551 & R553 pull-high from +3VS to +3VALW_PCH for leakage.	
15.			Add R677 & R678 & R679 for PTC request, Change R473,R490,R679,R677,R678 from 0ohm to PTC(SP040005X00).	
16.			Change Q10 from SB00000FC00 to SB00000L800 for 替代料	
17.			Remove R469 0ohm for TV.	
18.			Add C2134 ,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2143 for ESD.	
19.			Remove JXDP1,OC1,OC2,RC3,RC4,R125,R126.	
20.			Pop U7&R231, un-pop R228 for PLT_RST_VGA#.	
21.			Swap SATA_PRX_DTX_N1 & SATA_PRX_DTX_P1 for m-SATA pin define.	
22.			Un-pop LAN power components Q26,Q27,R573,R574,C562.	
23.			0 ohm change to short pad: R347,R585,R507,R674,R644,R645,R646,R647	
24.			Change R453&R457 from 0ohm to 1.1K, R451&R459 from 300ohm to 5.6Kohm.	
25.			Pop R438,R439 for ESD request.	

PVT change list:

1. Change Q10 from SB00000FC00(EOL soon) to SB00000ZN00(同Q29),SB00000FC00 as 2nd source.Schematic,需驗證

2. Change U23 pin12_+USB3_VCCA to +USB3_VCCB, pop U22, un-pop U24 for USB charger

3. R365 change from short pad to 0ohm.

4. U5 pin5 change from +3VSto +3VALW_PCH for BCM43142 wake from WLAN issue.

5. Change R473,R490,R677,R678,R679 from SP040005X00_0603 size to F1,F2,F4,F5,F3 SP040003S00_1206 size.

6. Change L11 from SM010014520 to SM01000EJ00 for ACL request

7. Change L8 from SM010007W00 to SM010019400 for ACL request

8. Change D7 from SC2N202U010 to SC600000B00(same as D1/D2), SC2N202U010 as 2nd source..

9. Change RP19 from SD309510A80(T88 P/N) to SD309510A10.

11. Change R276 from 10k to 100k for +3VS_VGA rise time.

12. Change R672 from 10k to 100k for +3VALW_PCH rise time.

14. Change R438 & R439 from 0_0603 to short pad.

15. Un-pop C125 & C548 for sequence EA.

16. Change C394, C398,C520 & C514 from 220uF (LELON_SF000001F00) to 100uF (Panasonic_SF000005100) to meet Inrush EA & ACL request.

17. Change C170 & C171 from 12pF to 10pF for EA.

20. Change C106 & C107 from 4.7pF to 10pF for 25MHz crystal.

21. Add R677 & reserve R678 on U5 AND gate for PLT_A_RST#

13. Change USB1 & USB2 from DC23300AE00 to DC233008R00(VBA11)

24. Change R591 pull-high from +5VSB to VL for power S5 Erp request.

22. Change D20 & D21 from SC300001Y00 to SC300002F00 for ESD request

23. Change D22 & D23 from SCA00001100 to SCA00000T00 for ESD ACL request

10. Add C2144-C2152 for EMI request.

18. Change R402 from short pad to 22ohm for EMI, R399,R401,R403 & R404 change from short pad to 0 ohm for EMI request.

19. Reserve C2153,C2154,C2155,C2156, add D29 for ESD.

20. Change R282 from 100k to 2k, R277 from 470 to 22 ohm for GPU power sequence.

21. Change Y1 from SJ100001K00 to SJ10000FA00 ,C102 & C107 to 6pF.

pre-MP change list:

1. Change R399,R401,R402,R403,R404 from 0ohm to short pad.

2. Add C2157 and reserve C2158.

3. Change R8,R470,R669,R670,R416 from 0ohm to short pad.

4. Un-pop JECDB1 & SW1.

5. For R3 P/N, change PCH P/N from SA00006RF00 to SA00006RF20, PCB P/N from DA60011S000 to DA60011S010 and GPU P/N from SA00006ZF00 to SA00006ZF10.

6. Change C520 & C514 from 100uF to 220uF.

7. Pop C2149~C2152 for ESD request.

8. Change C559 & C2128 from 0603 to 0805.

9. Change C2145 from 0.1uF to 470pF, change C2149~C2152 from 330pF to 470pF for EMI.

10. Add C418 for EMI.

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				Size	Document Number	0.3
				VCA00 LA-9791P M/B		
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