

Intel BayTrail-D Platform

Date : 2013/12/27
Version 1.0

Compal Confidential

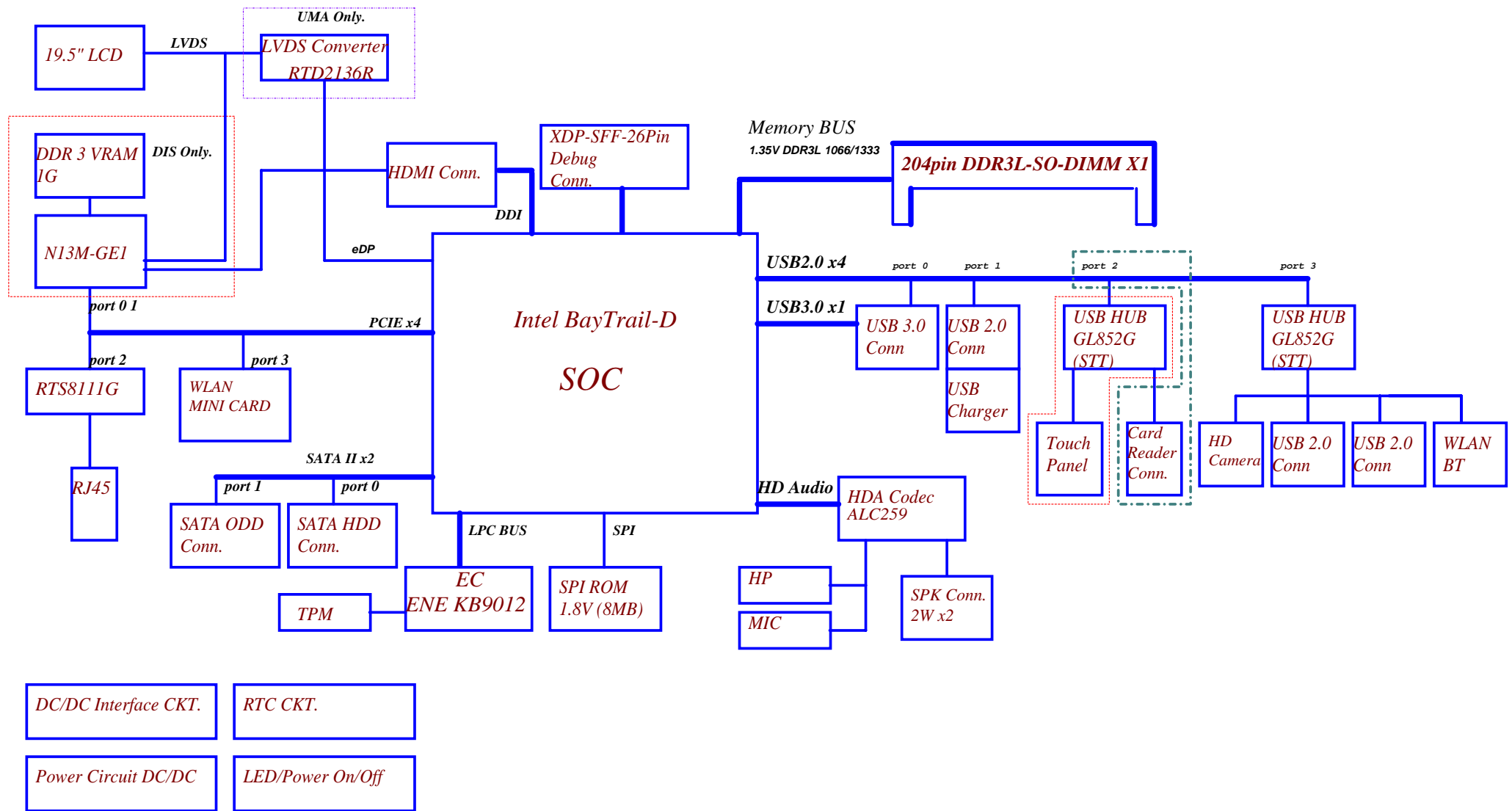
ZAA00(C260) LA-B001P Schematics Document

Intel BayTrail-D Platform

AIO M/B

REV: 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/01/03	Deciphered Date	2014/01/03	Title Cover Page	
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EC SM Bus1 address		EC SM Bus2 address	
Device	Address	Device	Address
Smart Battery	0001 011X b		
SOC SM Bus address			
Device	Address		
SO-DIMM A (JDIMM1)	A0h		
SO-DIMM B (JDIMM2)	A2h		

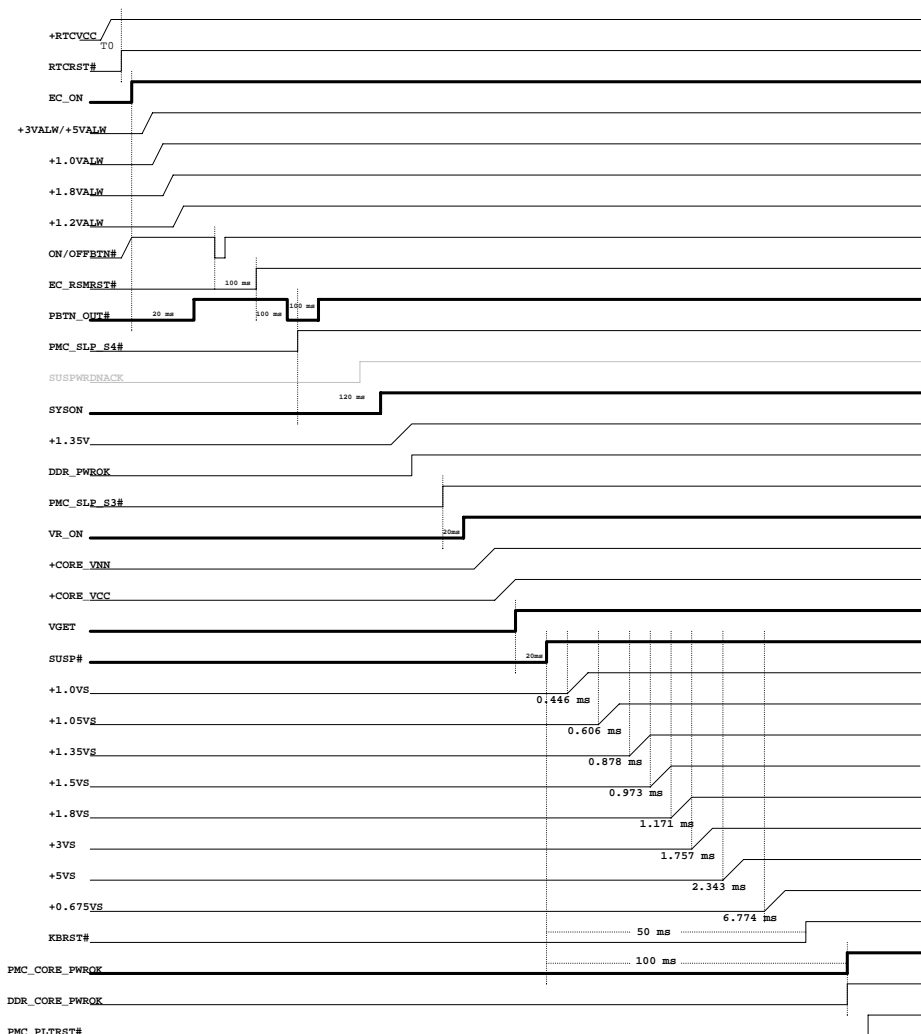
	0(D18)	1(UMA)	
AD_PID1	R297=10K Ohm ; R298 open	R297 open ; R298=10K Ohm	
UD	R330 = 10K Ohm; R299 open	R330 open ; R299 10K Ohm	

Date		Time		Date		Time	
Start Date	End Date	Start Date	End Date	Start Date	End Date	Start Date	End Date
1	1/1/2020	1	1/1/2020	1	1/1/2020	1	1/1/2020
2	1/2/2020	2	1/2/2020	2	1/2/2020	2	1/2/2020
3	1/3/2020	3	1/3/2020	3	1/3/2020	3	1/3/2020
4	1/4/2020	4	1/4/2020	4	1/4/2020	4	1/4/2020
5	1/5/2020	5	1/5/2020	5	1/5/2020	5	1/5/2020
6	1/6/2020	6	1/6/2020	6	1/6/2020	6	1/6/2020
7	1/7/2020	7	1/7/2020	7	1/7/2020	7	1/7/2020
8	1/8/2020	8	1/8/2020	8	1/8/2020	8	1/8/2020
9	1/9/2020	9	1/9/2020	9	1/9/2020	9	1/9/2020
10	1/10/2020	10	1/10/2020	10	1/10/2020	10	1/10/2020
11	1/11/2020	11	1/11/2020	11	1/11/2020	11	1/11/2020
12	1/12/2020	12	1/12/2020	12	1/12/2020	12	1/12/2020
13	1/13/2020	13	1/13/2020	13	1/13/2020	13	1/13/2020
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15	1/15/2020	15	1/15/2020	15	1/15/2020	15	1/15/2020
16	1/16/2020	16	1/16/2020	16	1/16/2020	16	1/16/2020
17	1/17/2020	17	1/17/2020	17	1/17/2020	17	1/17/2020
18	1/18/2020	18	1/18/2020	18	1/18/2020	18	1/18/2020
19	1/19/2020	19	1/19/2020	19	1/19/2020	19	1/19/2020
20	1/20/2020	20	1/20/2020	20	1/20/2020	20	1/20/2020

43 Level	Description	BOM Structure
4319RF38L01~20	ZAA00	None Touch SKU
4319RF38L30~50	ZAA20	Touch SKU

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Power ON



T0: +RTCVCC stable to RTCRST# high > 9ms
T1: VR ramp up time from 10% to 90% voltage level < 2ms
T2 :Rail to subsequent rail turn on delay < 2ms
T3 :+VALWAS stable to EC_RSMRST# high > 10ms
T4 :+VS rails stable to PMC_CORE_PWROK > TBD

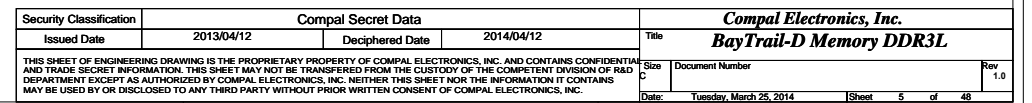
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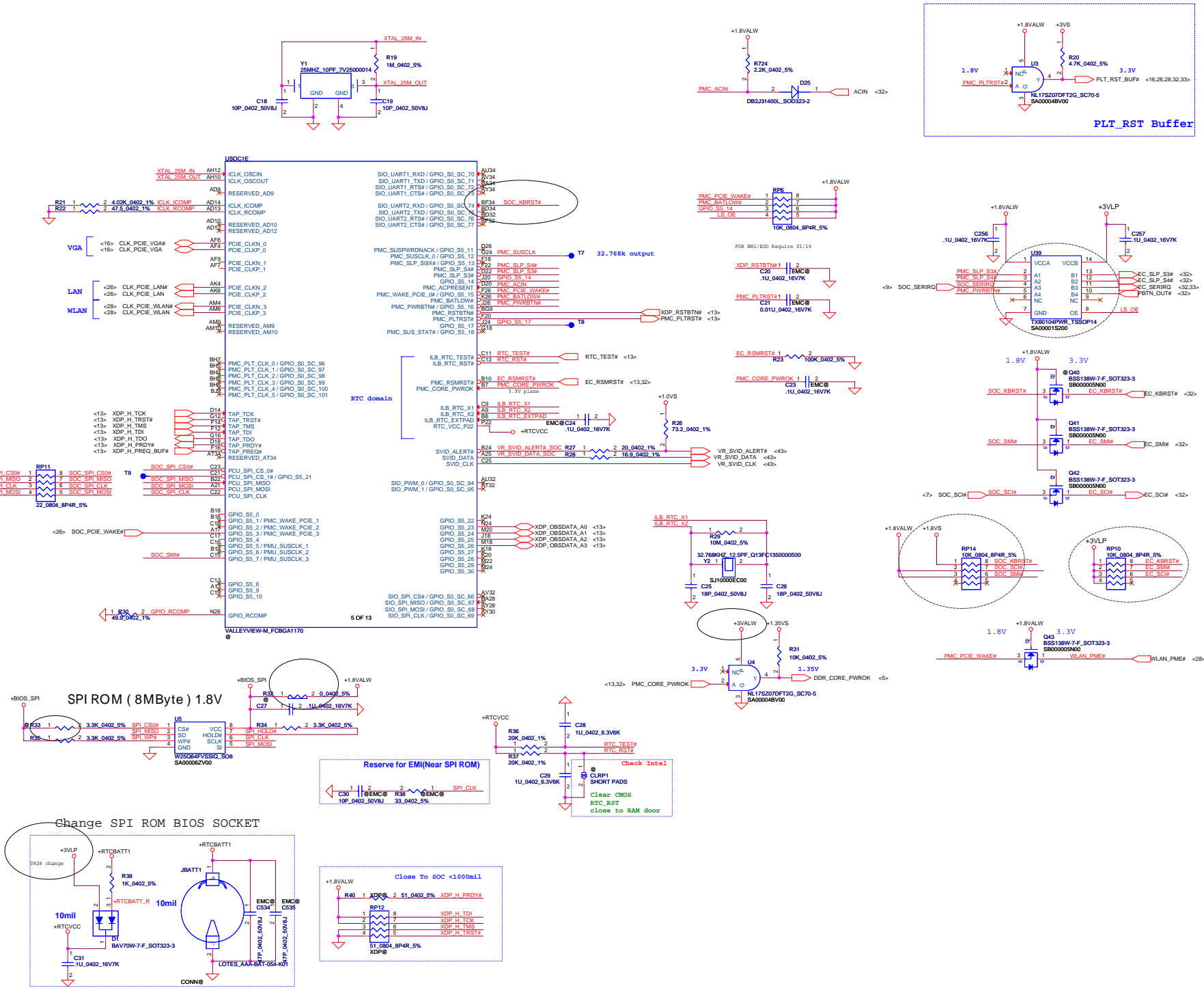
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirements.

File: Power Sequence	Compal Secret Data		Compal Electronics, Inc.	
Security Classification	2013/04/12	Deciphered Date	2014/04/12	Title
Issued Date	2013/04/12	Deciphered Date	2014/04/12	Power Sequence
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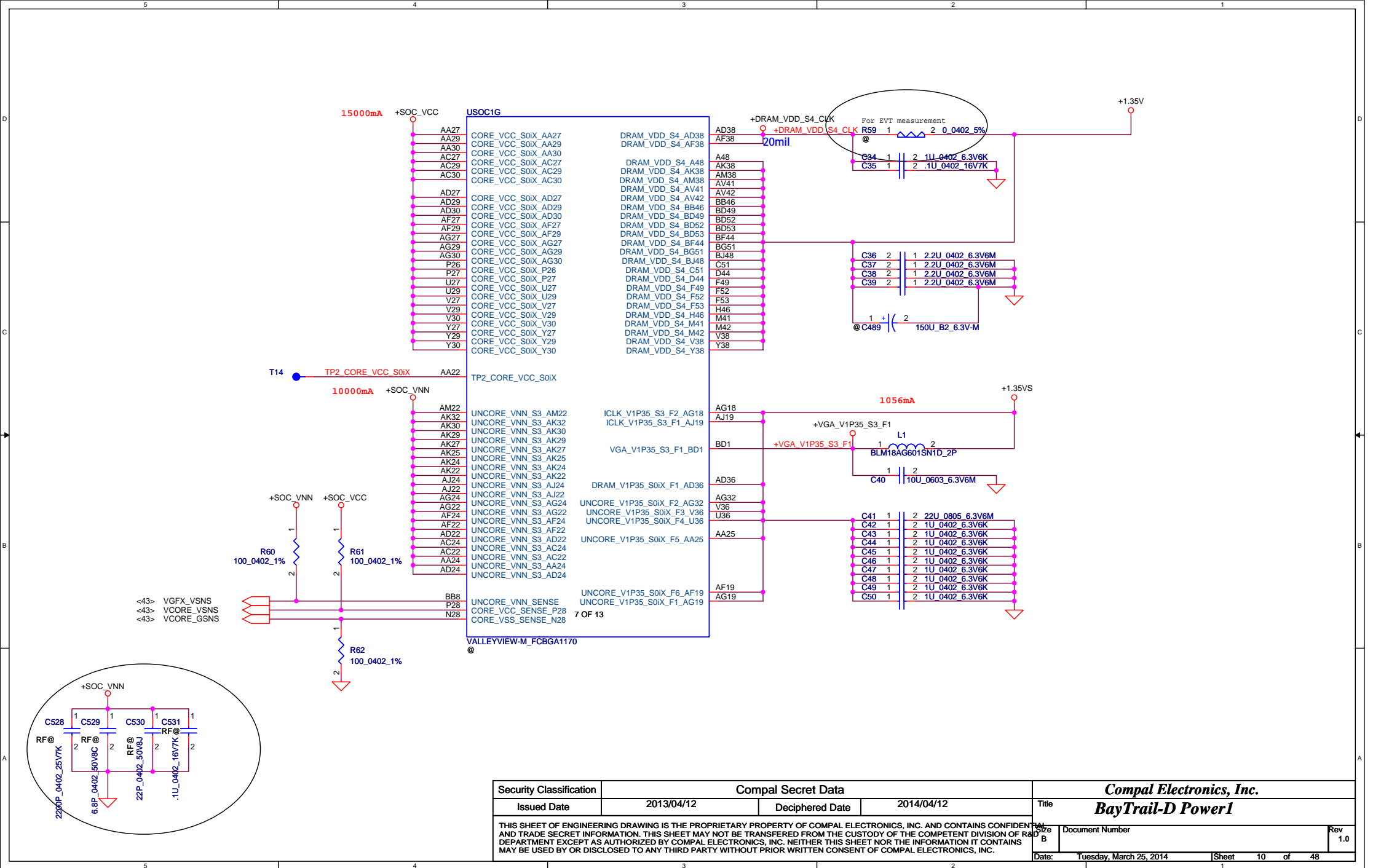
Channel B open

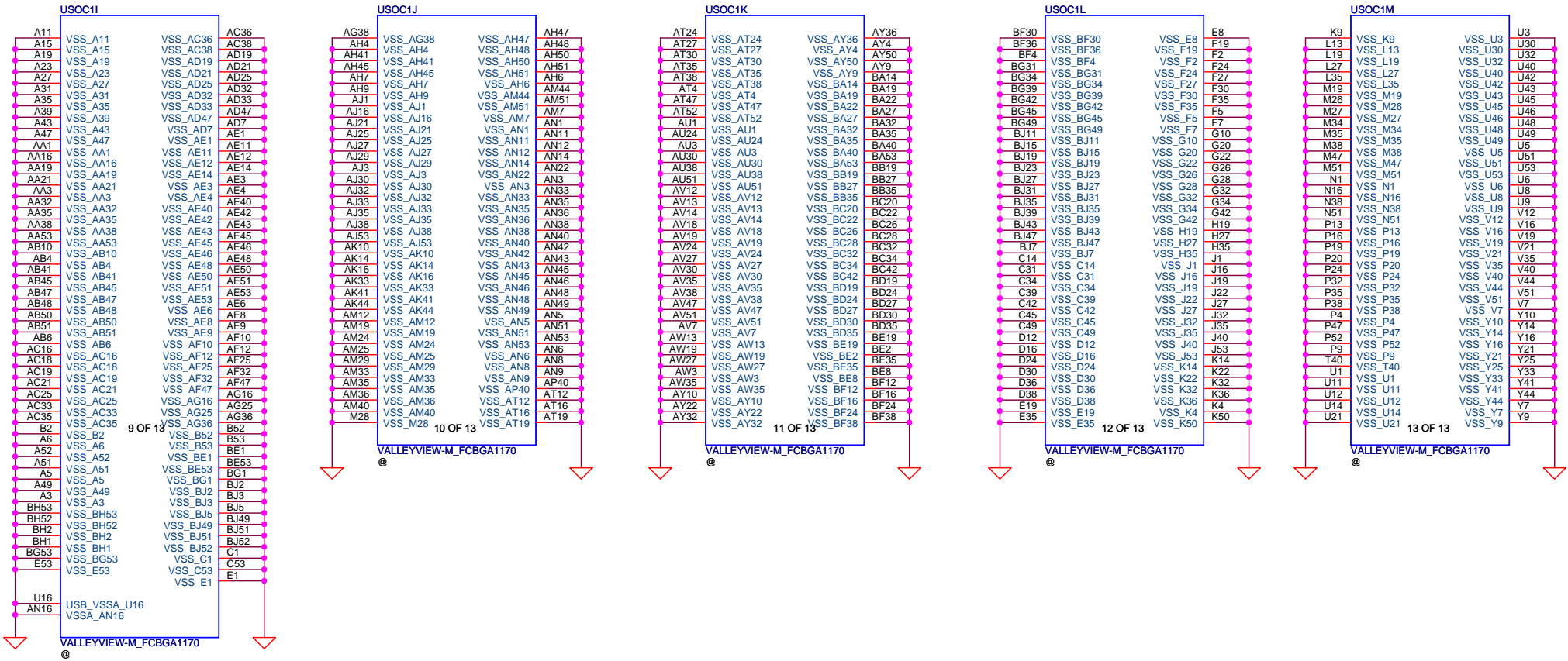




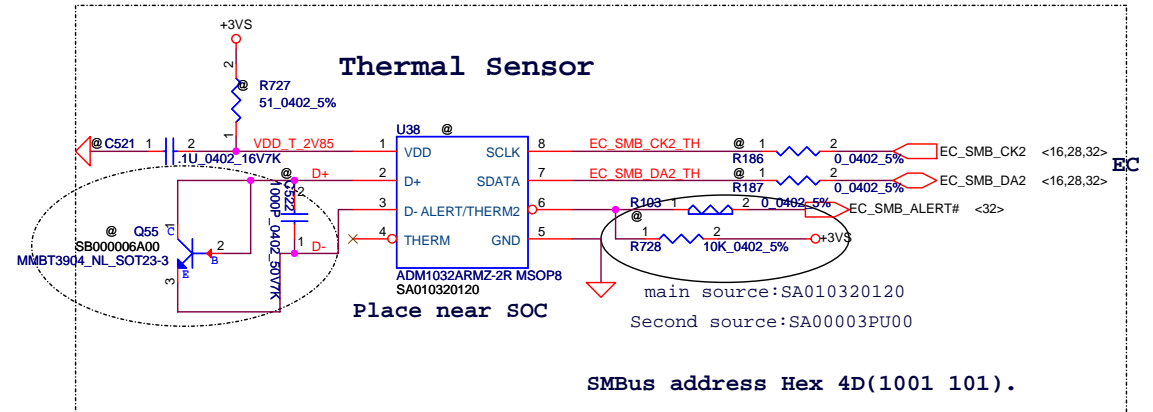
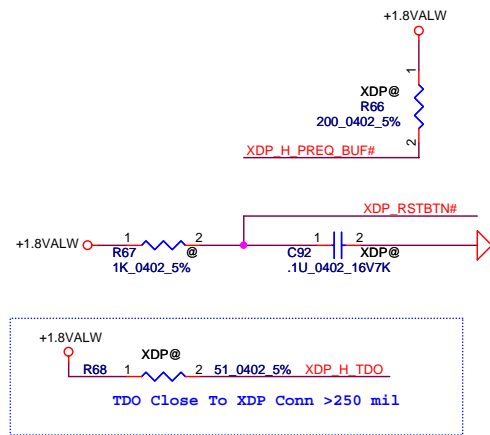
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Issued Date		Deciphered Date		Title	
2013/04/12		2014/04/12		BayTrail-D CLK/PMU/SPI/RTC	
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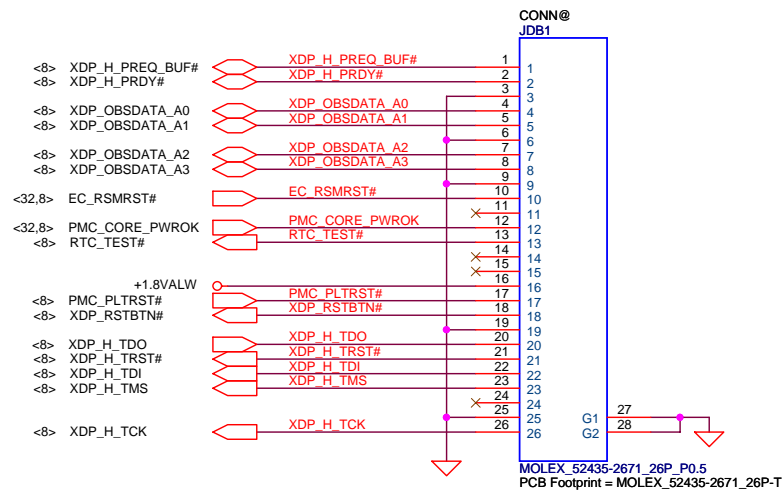




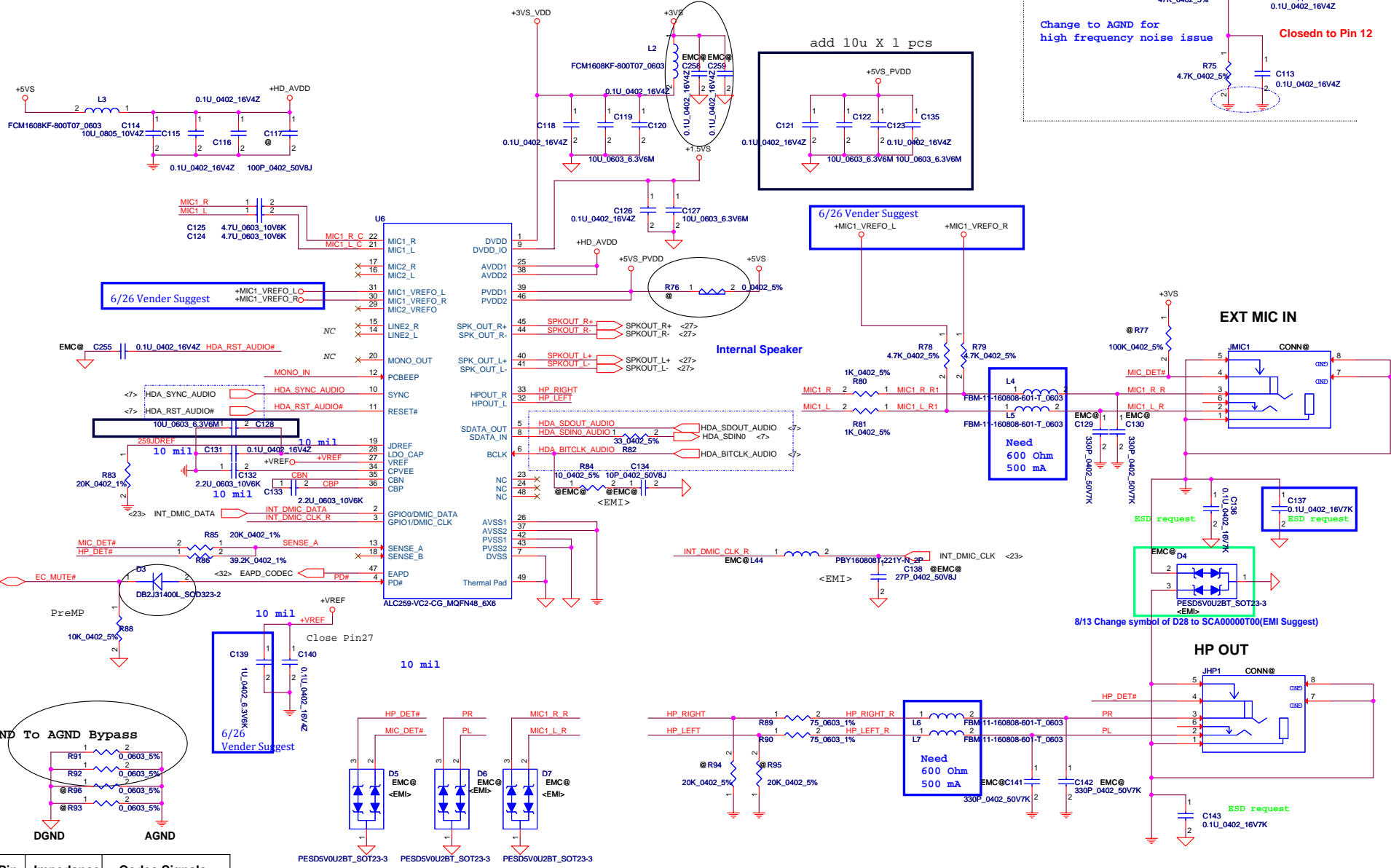
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XDP-SFF-26Pin





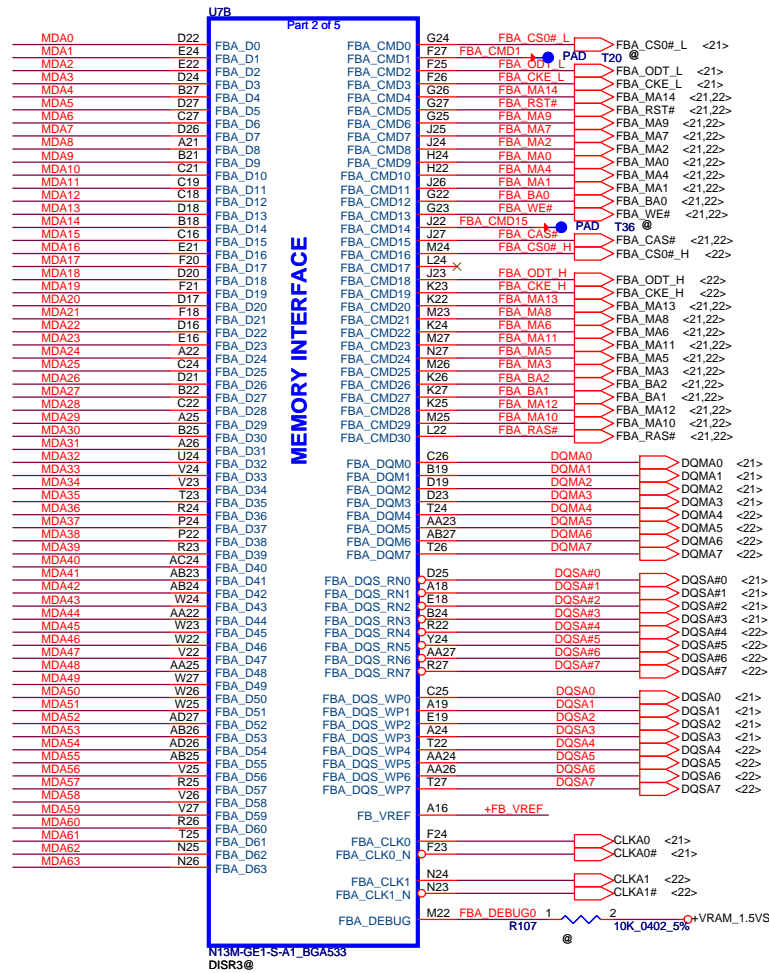
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Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	HP-OUT (PIN 32,33)
	20K	MIC1 (PIN 21, 22)

VRAM Interface

<21> MDA[31..0] 
<22> MDA[63..32] 



Mode	D Address	DATA Bus
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT#_L	
FBx_CMD3	CKE#_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT#_H
FBx_CMD19		CKE#_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

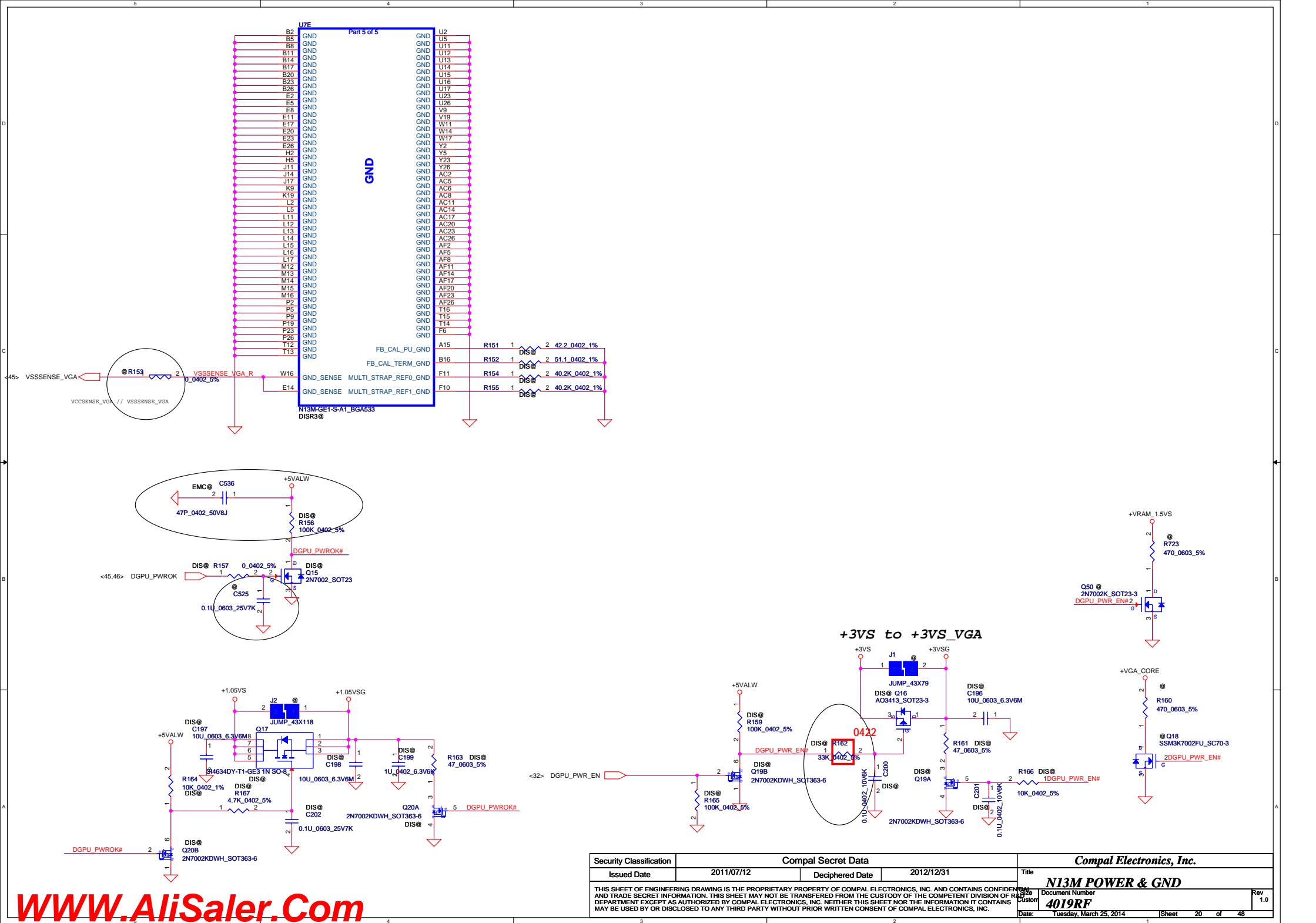
* A15 is not required for any x16 device, even up to 4Gb density
* A15 is only needed if we support x8 configurations, and only at 4Gb

Place close to the first T point

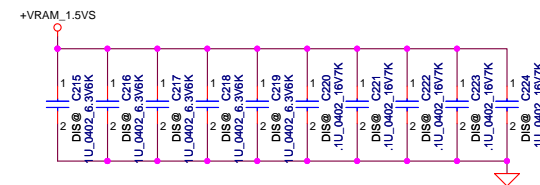
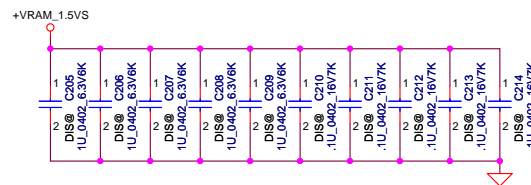
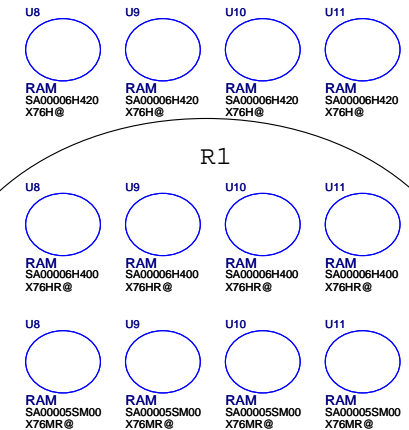
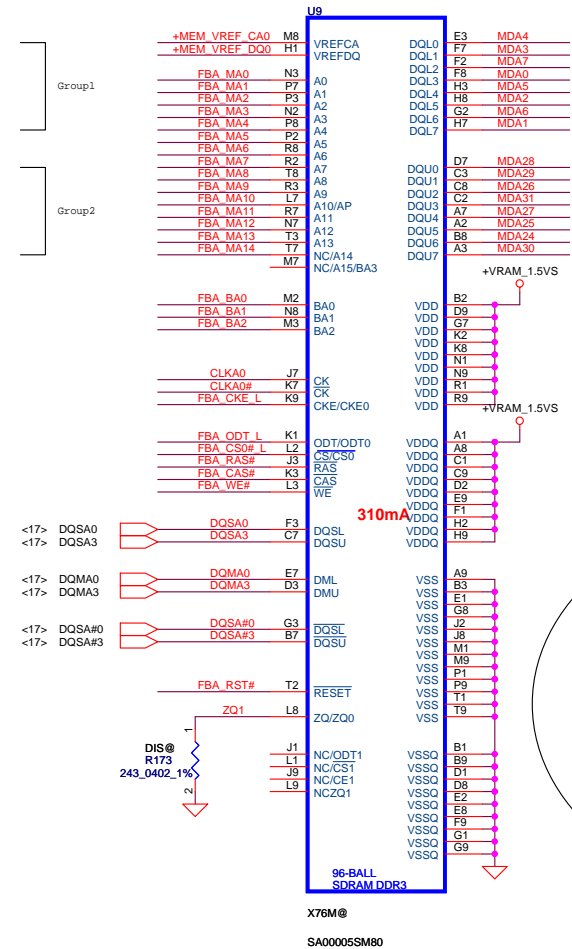
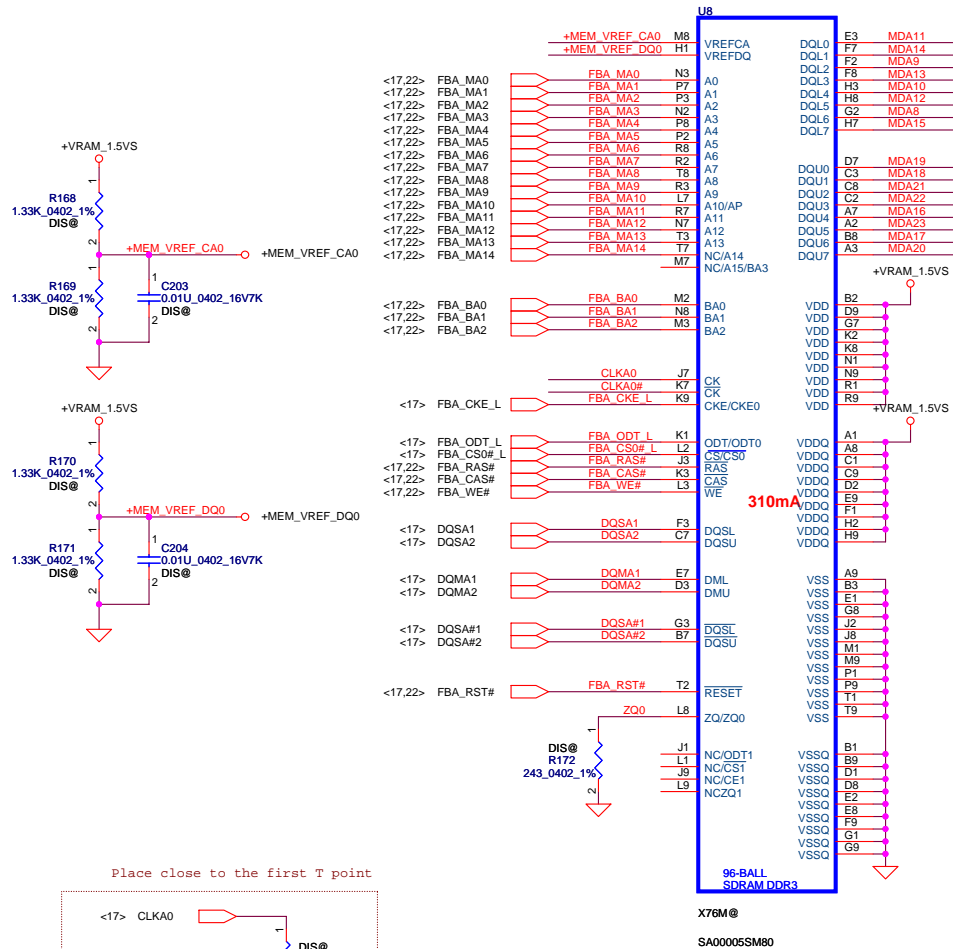
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

FBA_ODT#_H R108 1 DIS@ 2 10K 0402 5%
FBA_ODT#_L R109 1 DIS@ 2 10K 0402 5%
FBA_CKE#_H R110 1 DIS@ 2 10K 0402 5%
FBA_CKE#_L R111 1 DIS@ 2 10K 0402 5%
FBA_RST# R112 1 DIS@ 2 10K 0402 5%

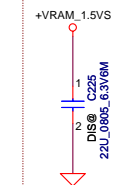
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VRAM DDR3 Chips



Place close to RANK0 VRAM

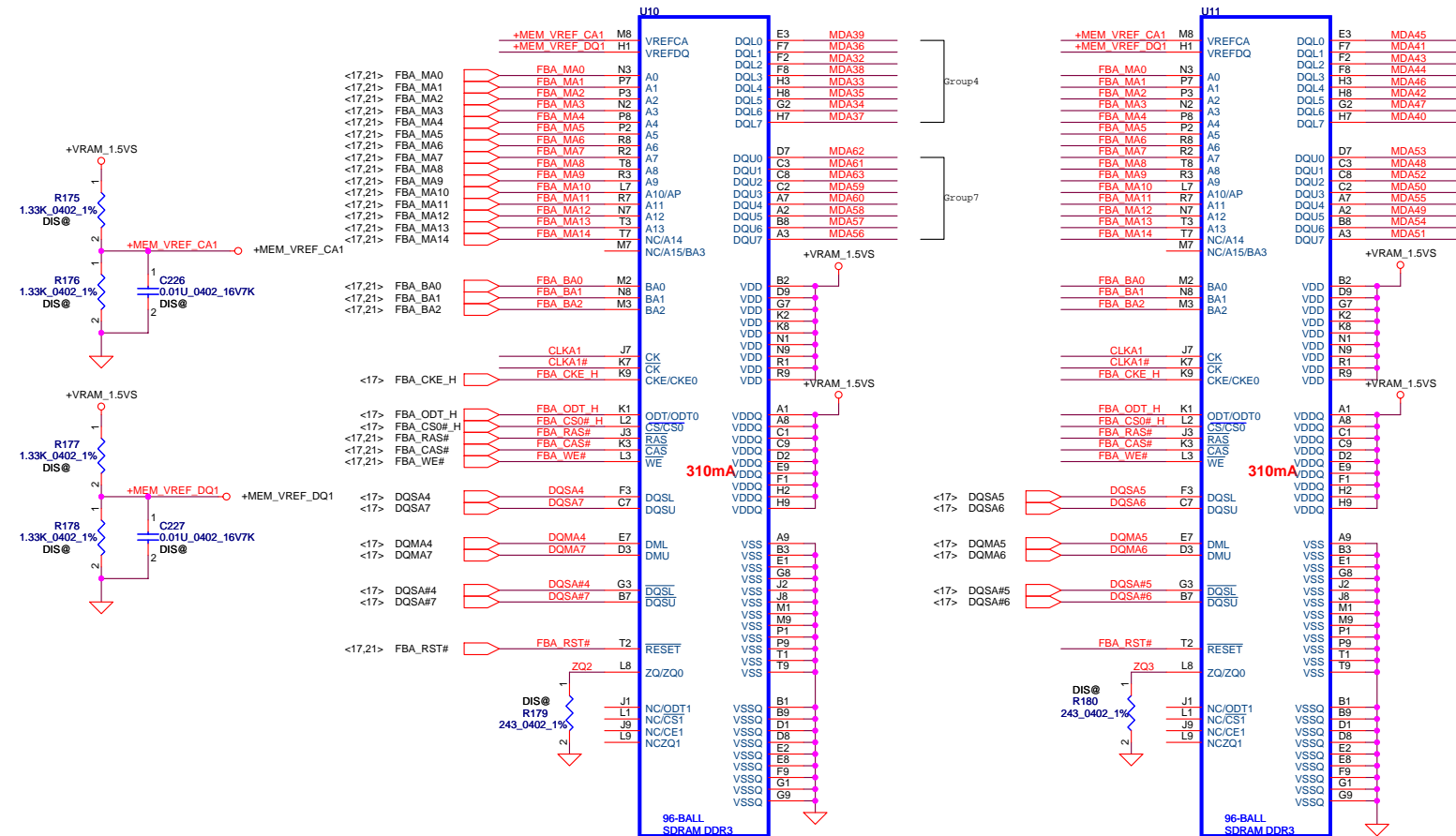


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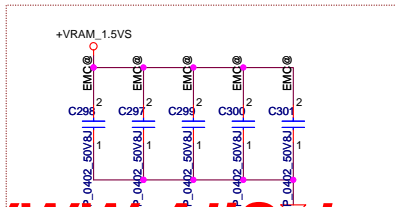
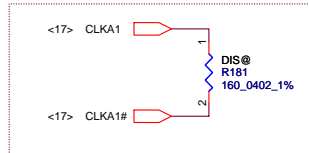
RANK 0 [63...32]

VRAM DDR3 Chips

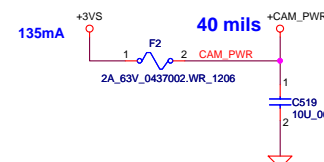
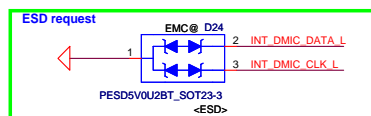
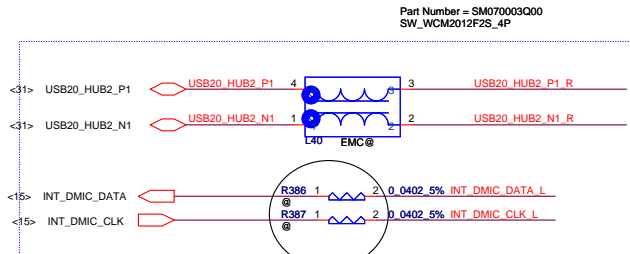
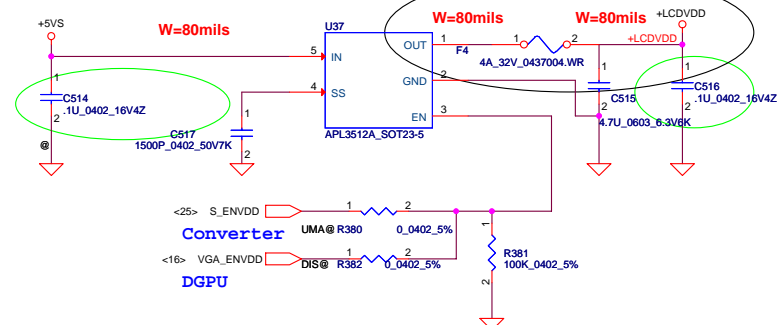
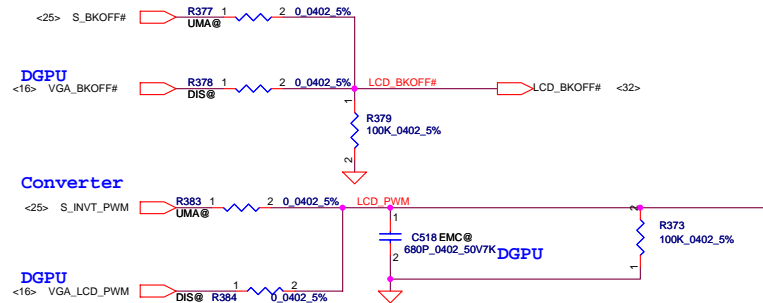
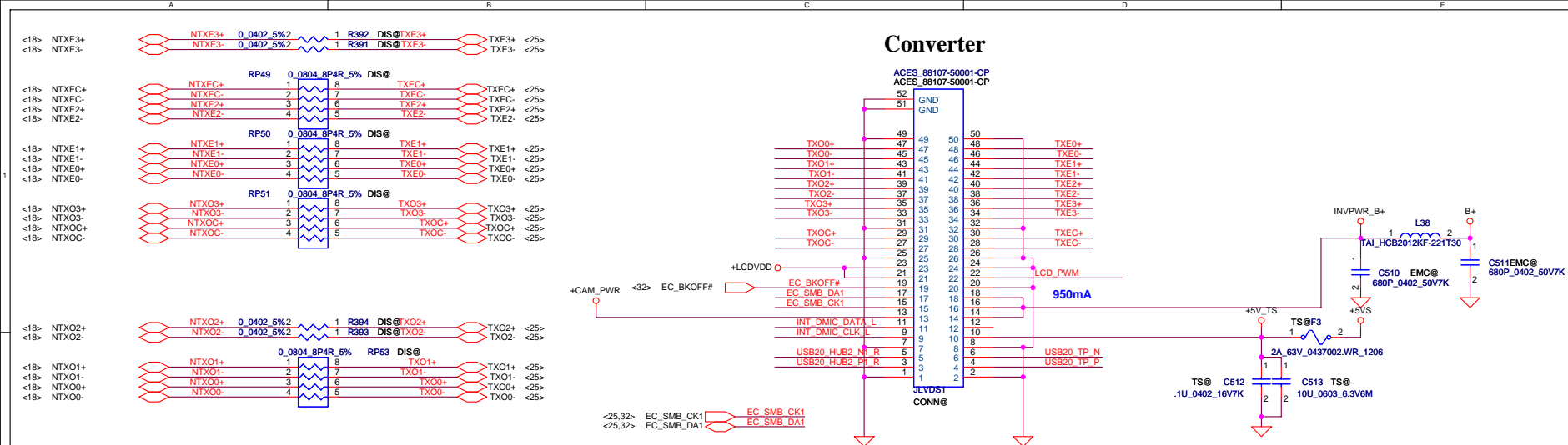
<17> MDA[63..32] MDA[63..32]



Place close to the first T point



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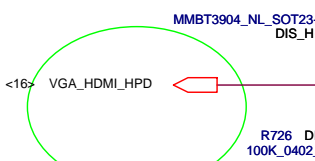
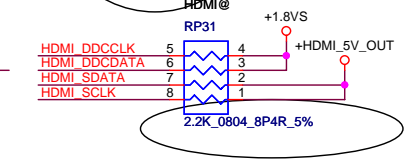
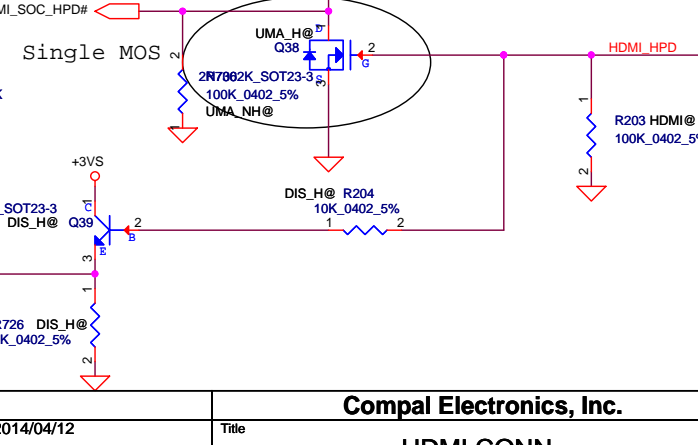
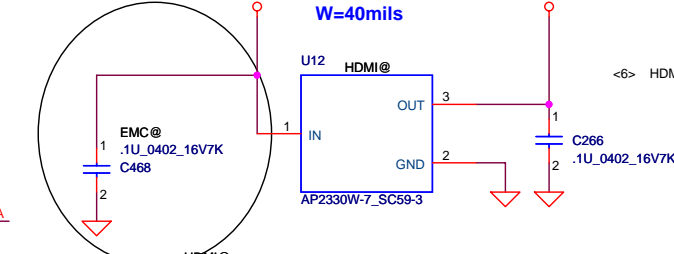
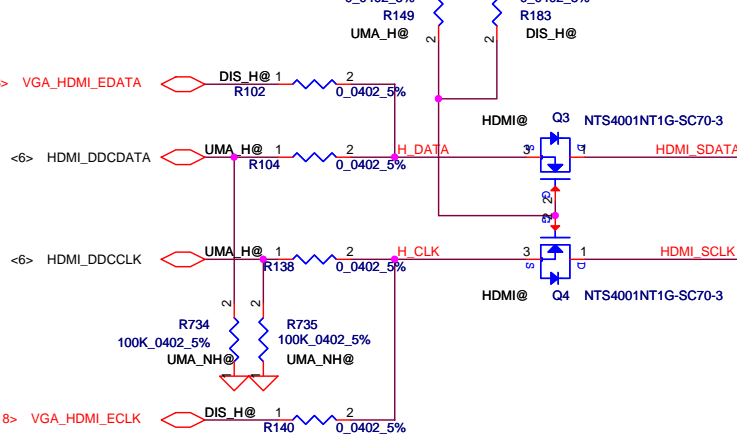
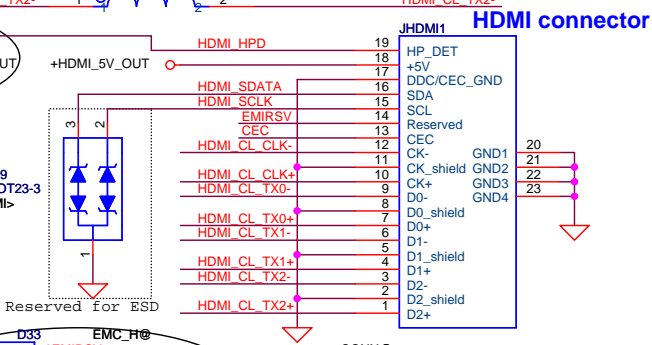
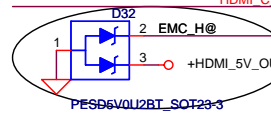
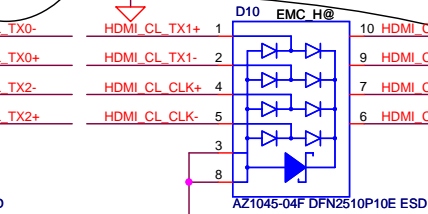
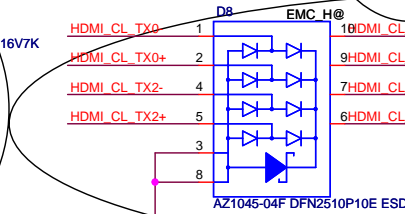
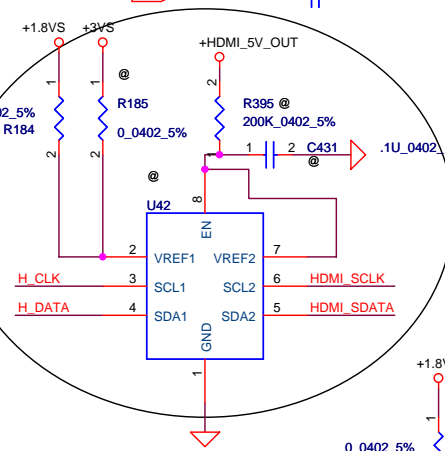
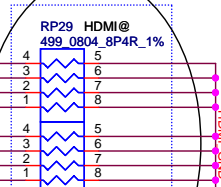
DIS only

<18> VGA_HDMI_CLK+	VGA_HDMI_CLK+	DIS_H@260	1	2	0.1U 0402 10V7K	HDMI_C_CLK+
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<18> VGA_HDMI_TX0+	VGA_HDMI_TX0+	DIS_H@262	1	2	0.1U 0402 10V7K	HDMI_C_TX0+
<18> VGA_HDMI_TX0-	VGA_HDMI_TX0-	DIS_H@263	1	2	0.1U 0402 10V7K	HDMI_C_TX0-
<18> VGA_HDMI_TX1+	VGA_HDMI_TX1+	DIS_H@264	1	2	0.1U 0402 10V7K	HDMI_C_TX1+
<18> VGA_HDMI_TX1-	VGA_HDMI_TX1-	DIS_H@265	1	2	0.1U 0402 10V7K	HDMI_C_TX1-
<18> VGA_HDMI_TX2+	VGA_HDMI_TX2+	DIS_H@267	1	2	0.1U 0402 10V7K	HDMI_C_TX2+
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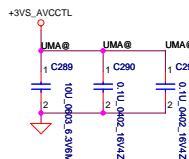
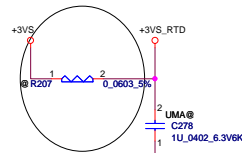
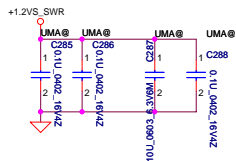
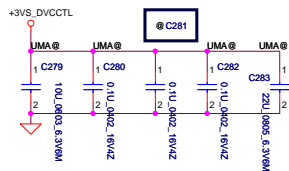
Verify Value

UMA only

<6> HDMI_P2	UMA_H@C274	2	1	.1U 0402 16V7K	HDMI_C_TX2+
<6> HDMI_N2	UMA_H@C273	2	1	.1U 0402 16V7K	HDMI_C_TX2-
<6> HDMI_P0	UMA_H@C271	2	1	.1U 0402 16V7K	HDMI_C_TX0+
<6> HDMI_N0	UMA_H@C270	2	1	.1U 0402 16V7K	HDMI_C_TX0-
<6> HDMI_CLKN	UMA_H@C275	2	1	.1U 0402 16V7K	HDMI_C_CLK-
<6> HDMI_CLKP	UMA_H@C276	2	1	.1U 0402 16V7K	HDMI_C_CLK+
<6> HDMI_N1	UMA_H@C269	2	1	.1U 0402 16V7K	HDMI_C_TX1-
<6> HDMI_P1	UMA_H@C272	2	1	.1U 0402 16V7K	HDMI_C_TX1+



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Power Consumption:

Pin 22 (PVCC) < 50 mA
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)

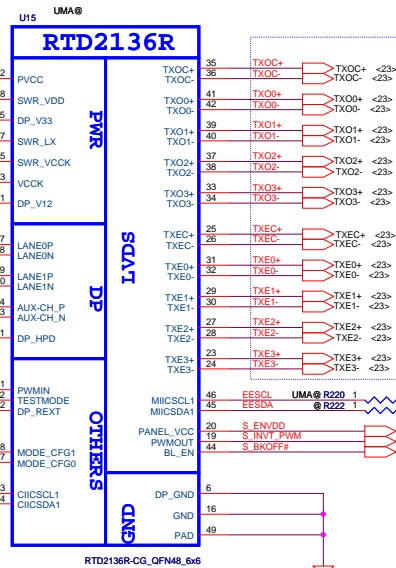
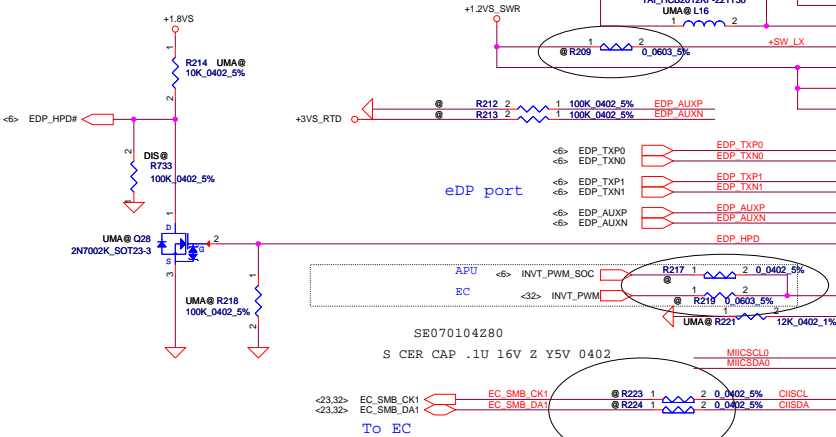
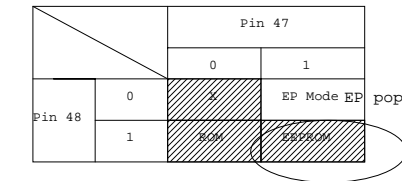
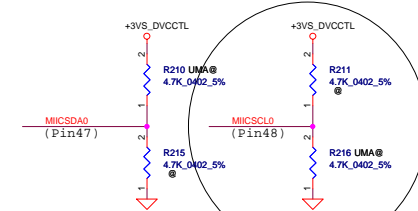
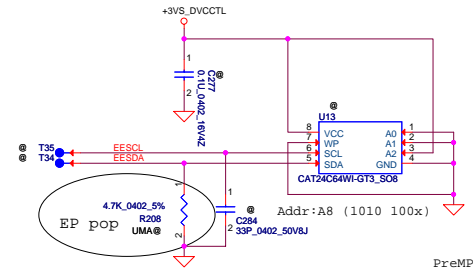
Pin5 (DPV33) < 20mA

Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)

Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)

Pin 43 (VCCK) < 50mA

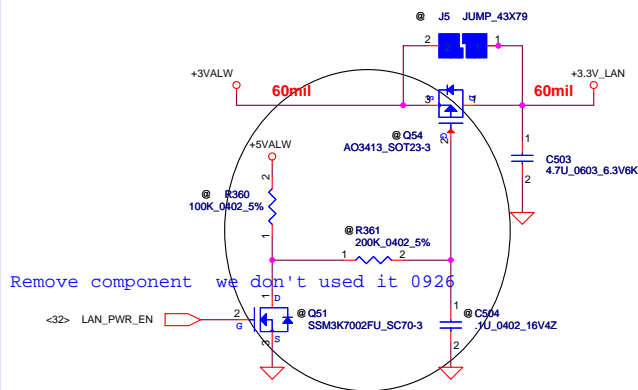
Pin 11 (DPV12) < 100mA



RTD2136R
S IC RTD2136R-CG QFN 48P DP/LVDS CTRL

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Rev 1.0				Document Number
LVDS Converter RTD2136R				Rev 1.0

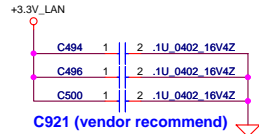
WOL circuit (Connect +3V_LAN to +3VALW)



+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

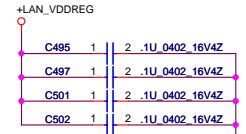
Power (Decoupling Cap.)

40 mils



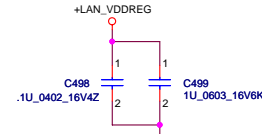
C494, C496, C500 close to U36
Pin 11,32 ,23, respectively

60 mils



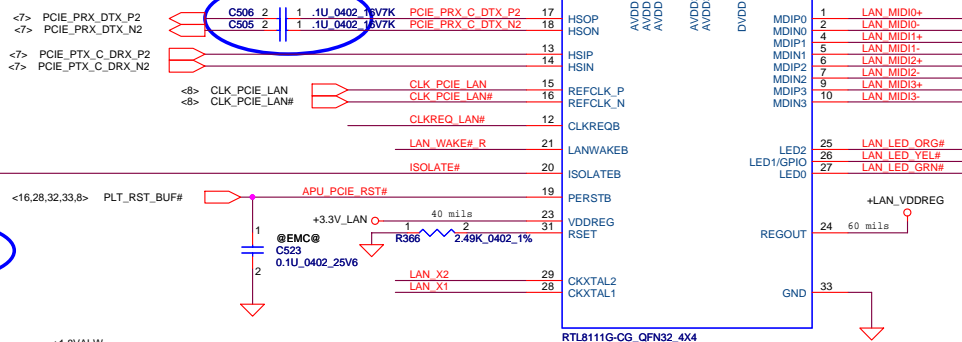
C495, C497, C501, C502, close to U36
Pin 3,8,24,30, respectively

60 mils

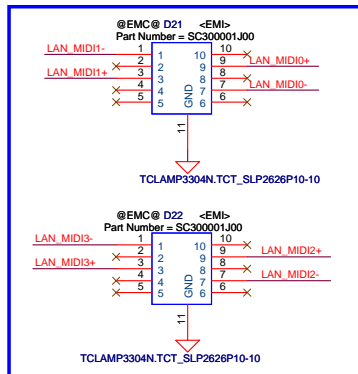
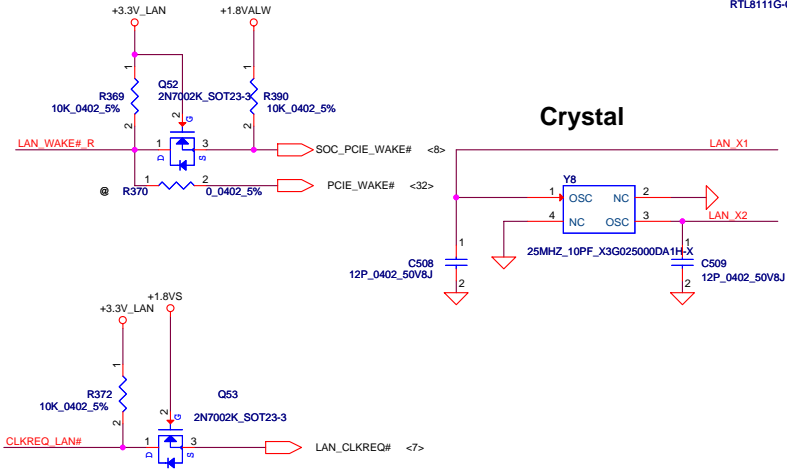


C498, C499 close to U36
Pin22

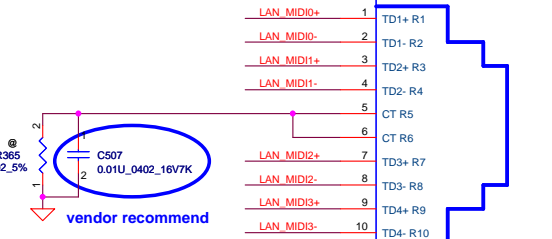
C505, C506, close to U36
Pin 17,18, respectively



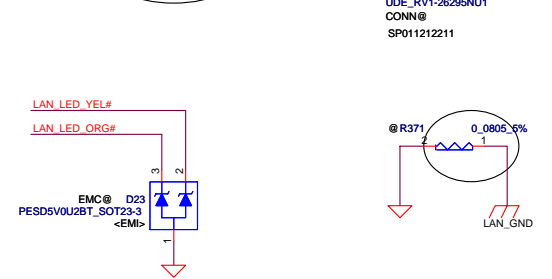
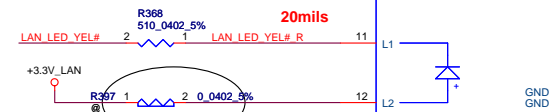
Crystal



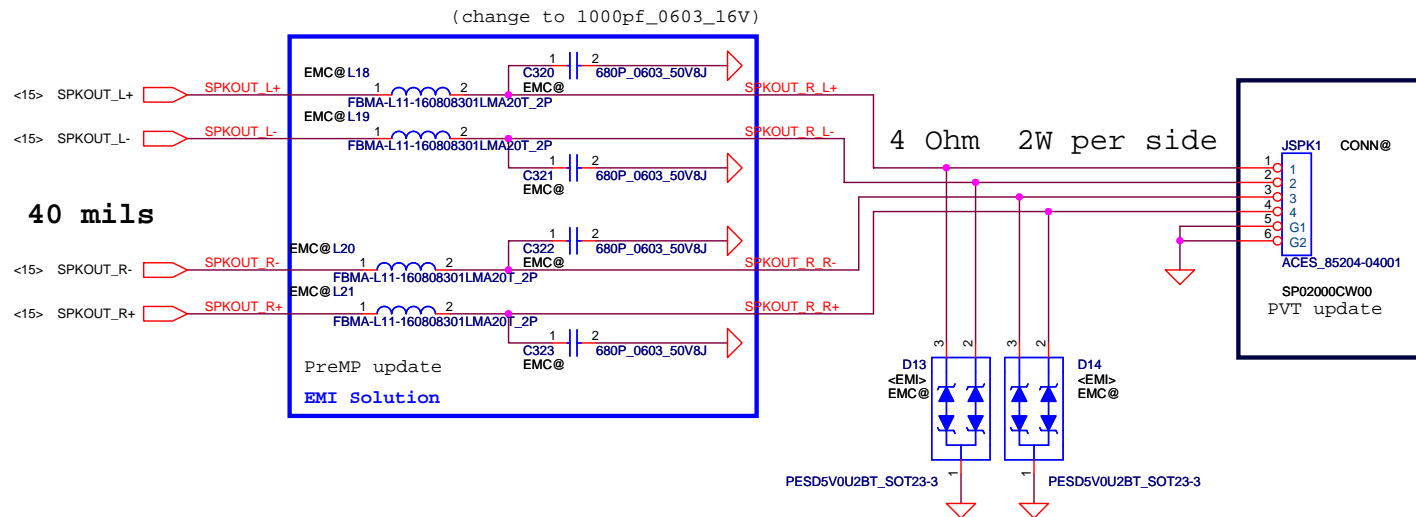
Green / Orange



Yellow

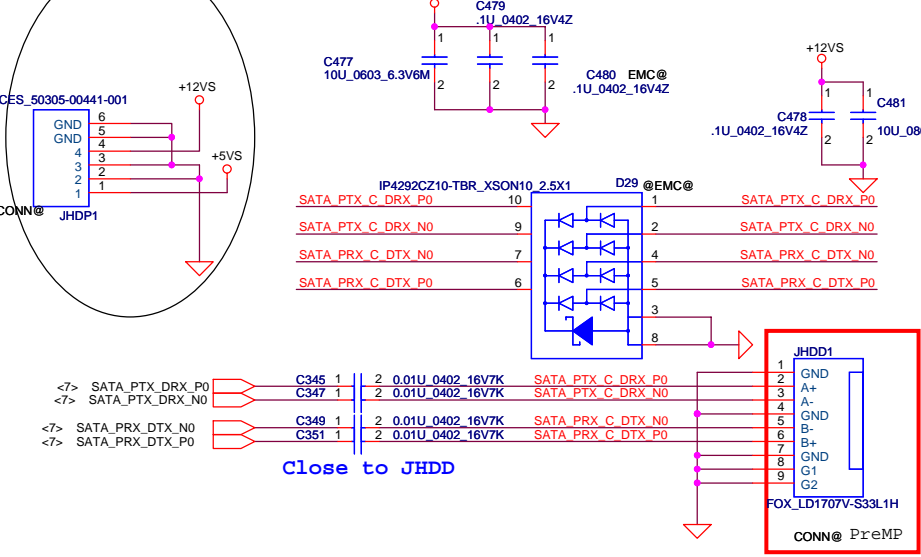


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								LAN RTL8111			
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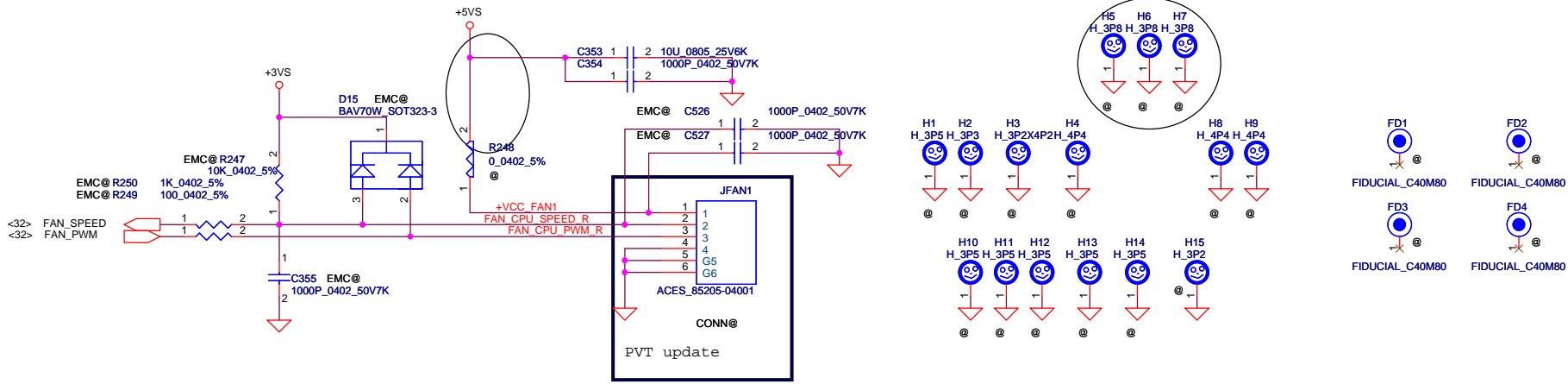
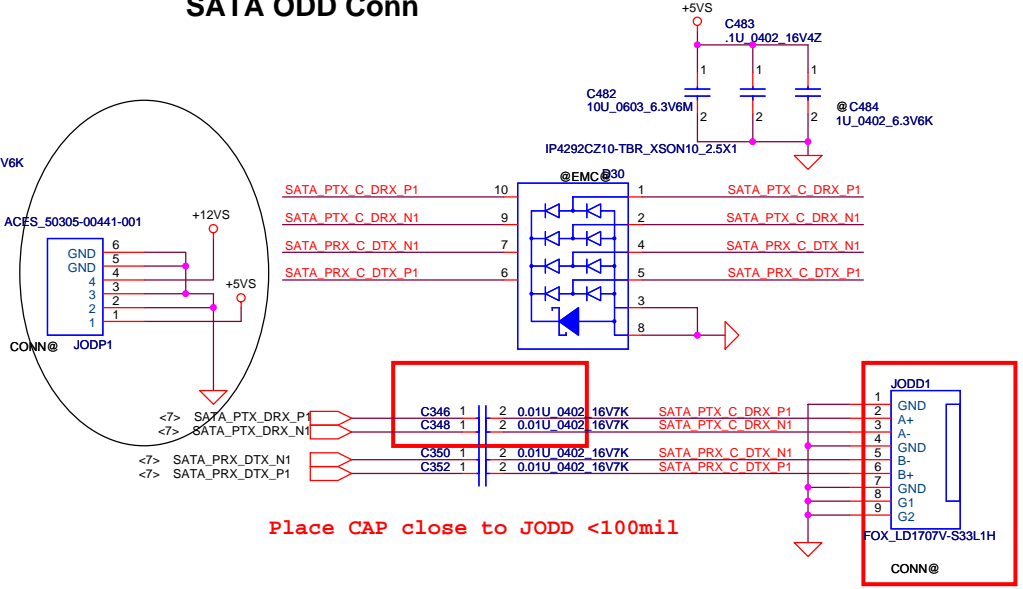


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SATA HDD Conn.



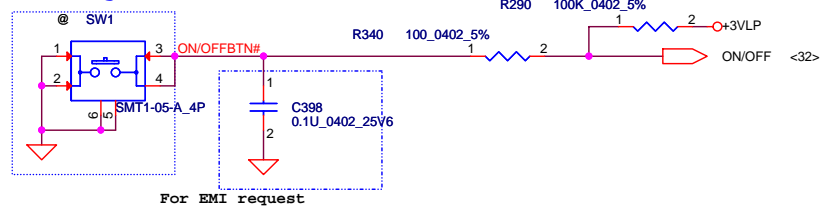
SATA ODD Conn



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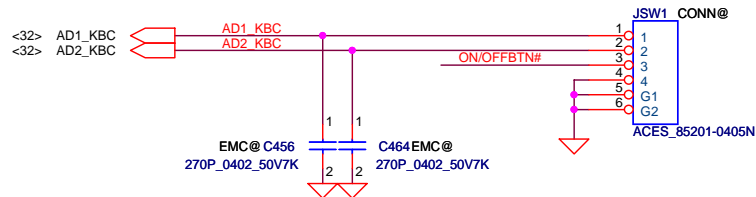


TOP side
For debug

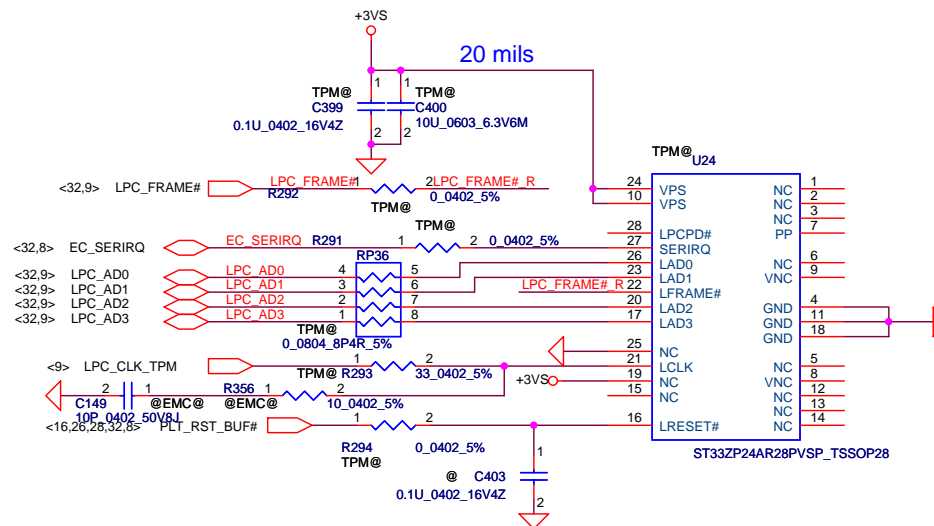


Power Brd Connector

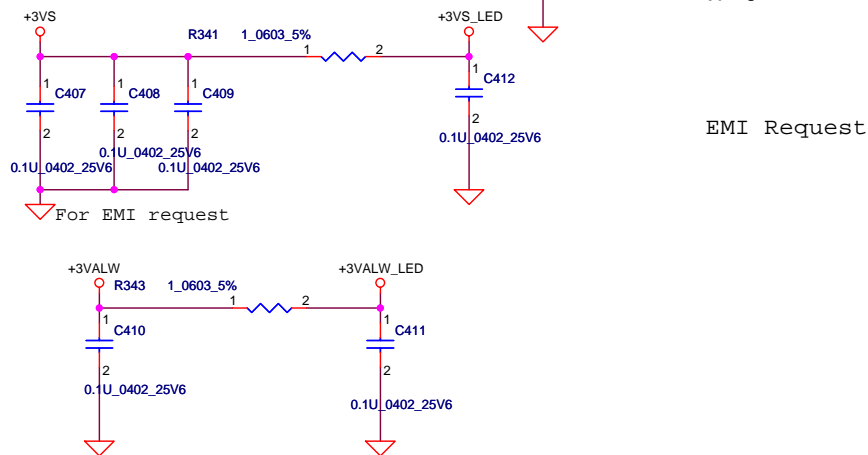
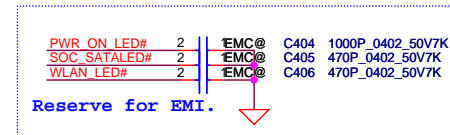
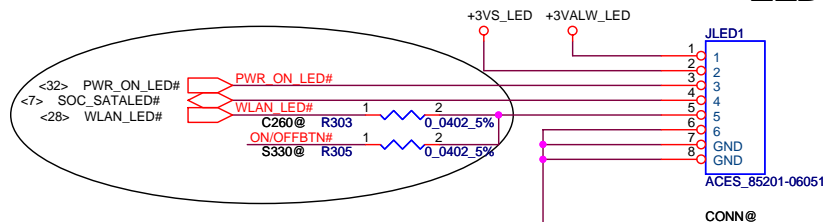
PU 4.7K on EC side



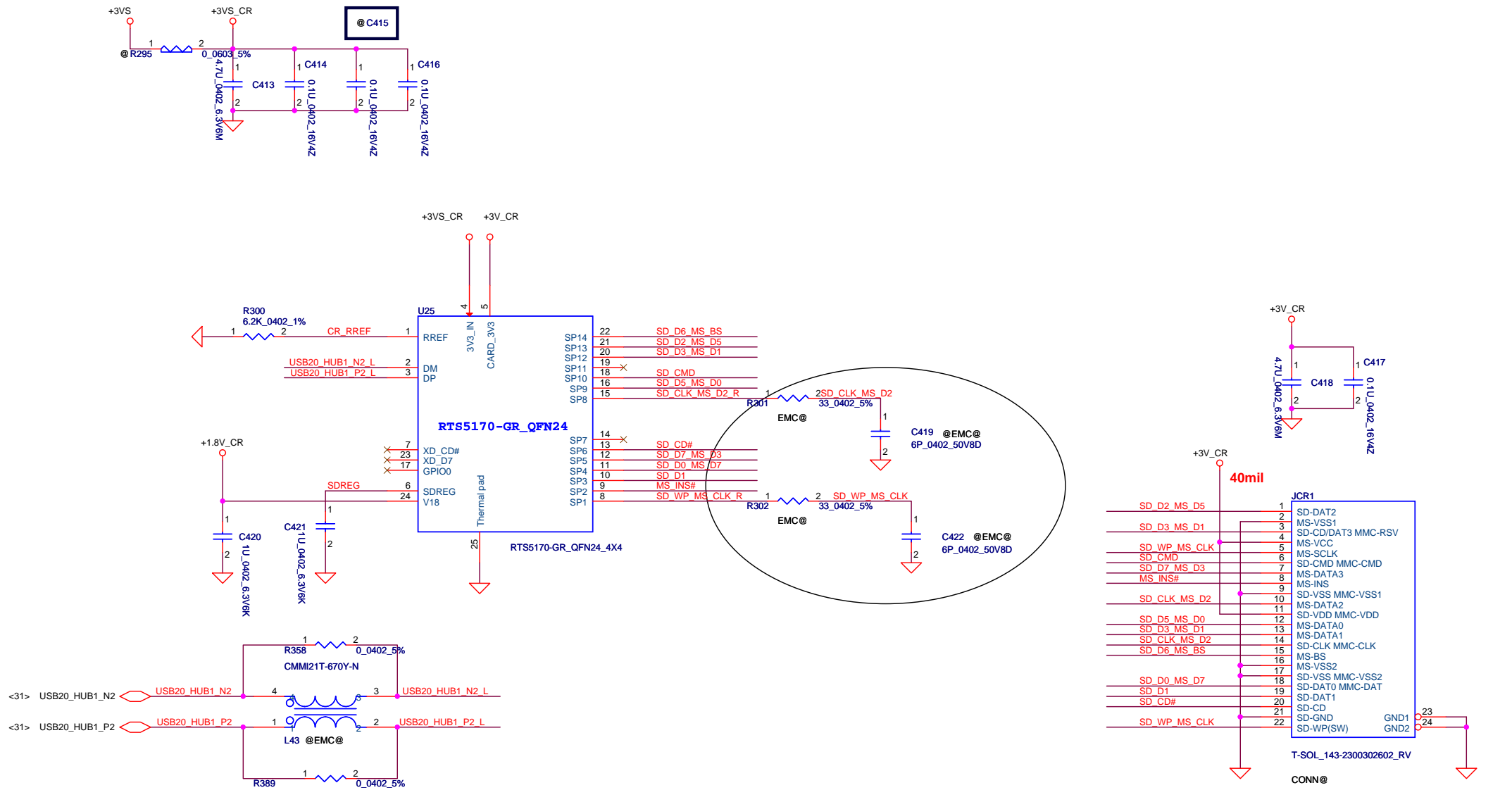
TPM(Reserve)



LED Brd Connector

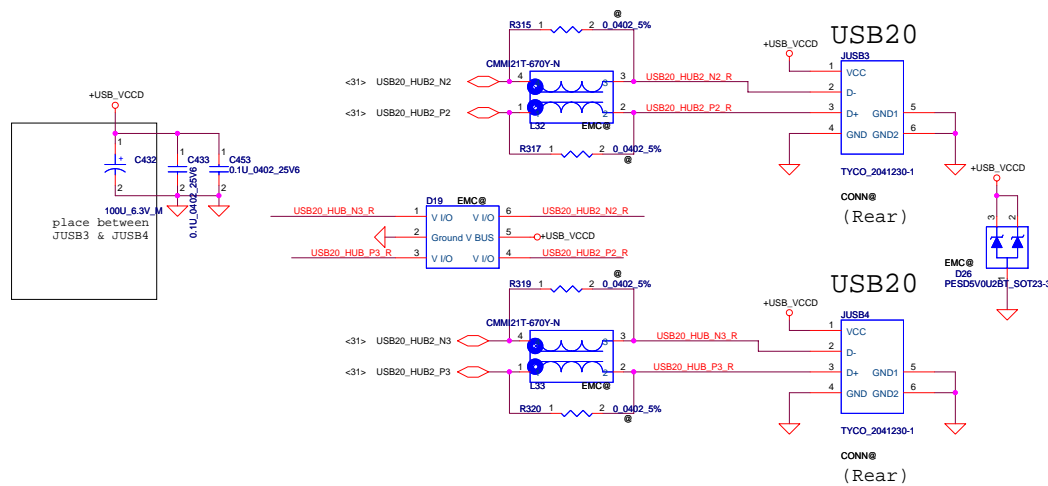
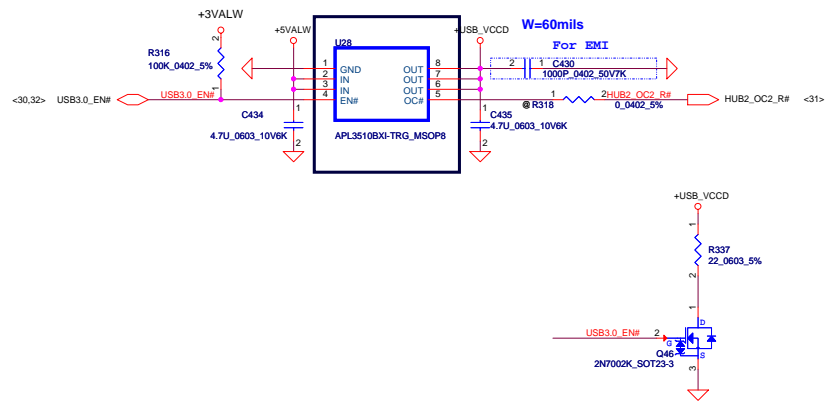


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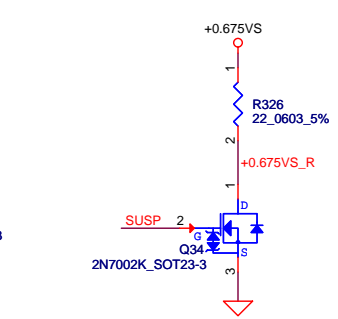
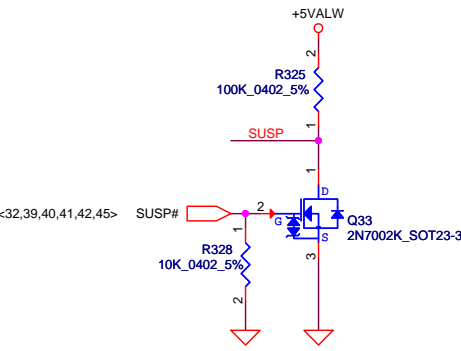
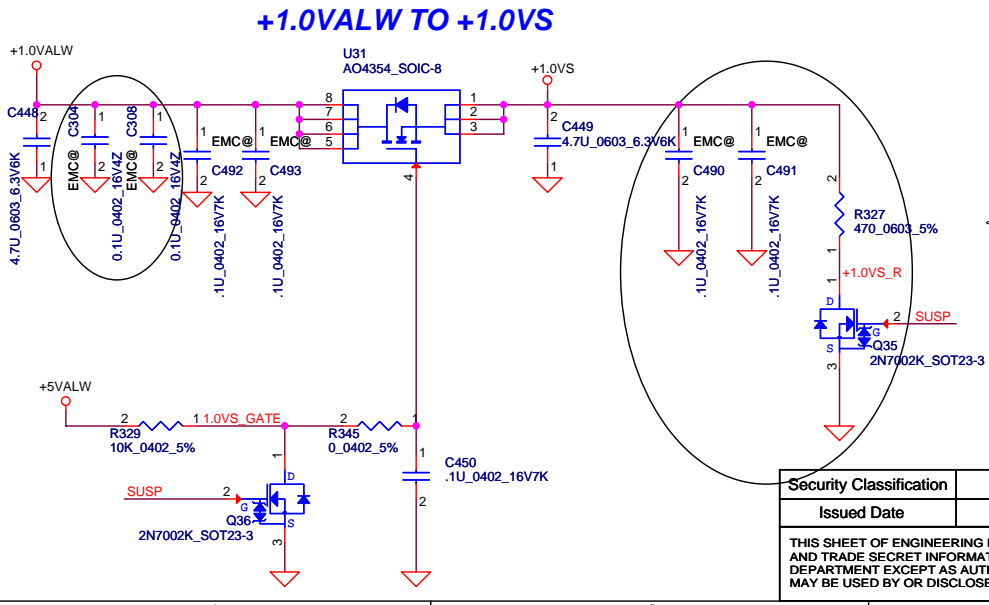
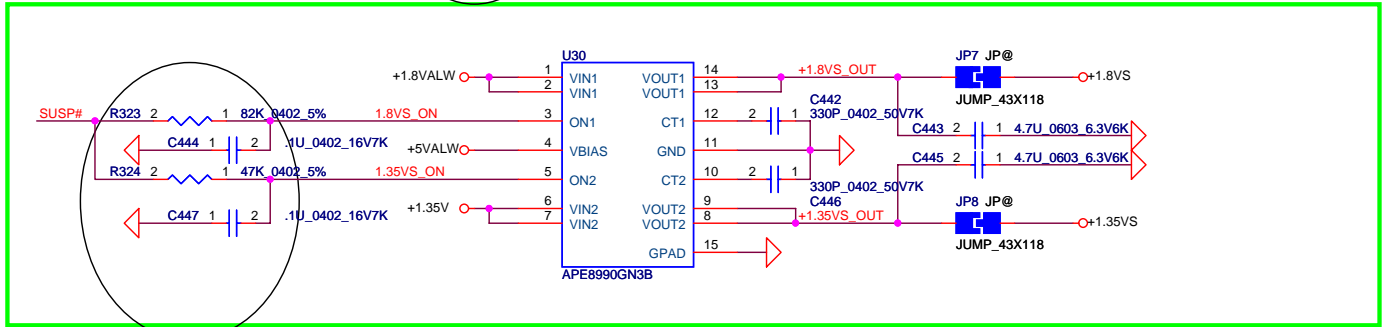
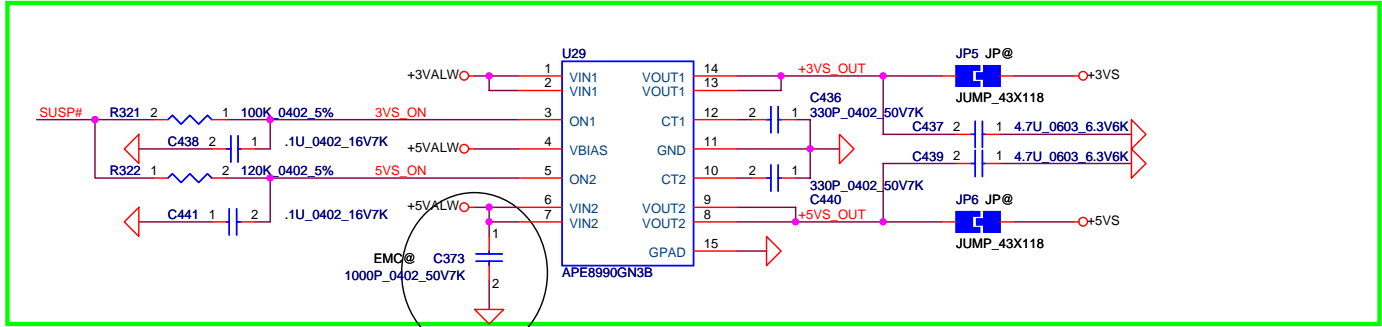
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USB2.0 Power

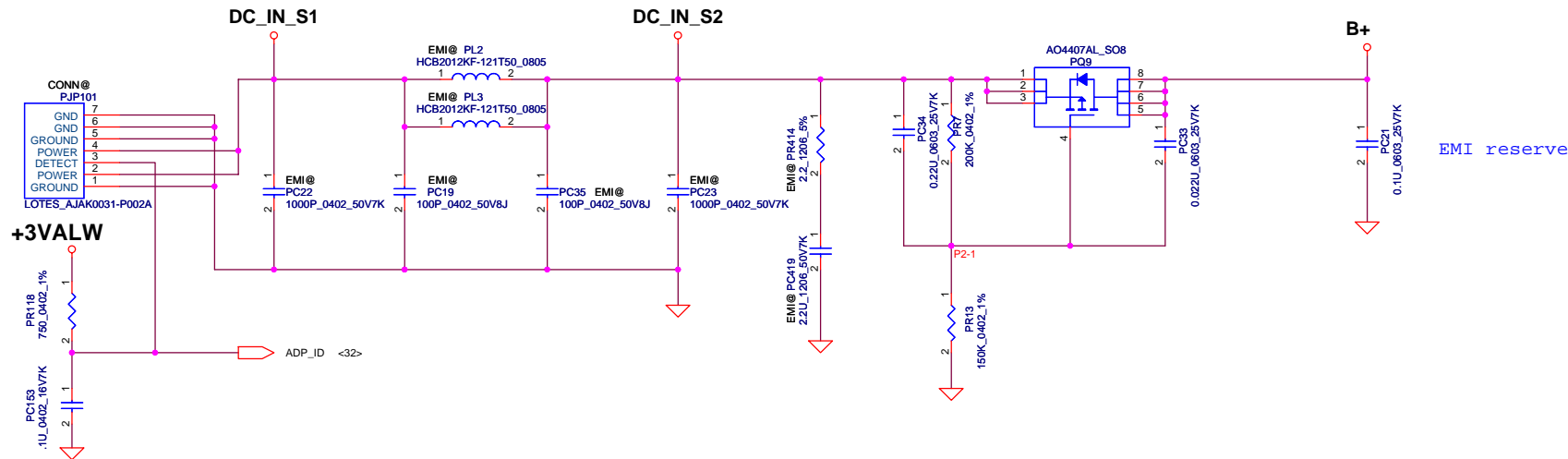


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Normal Platform (Not support M-STATE and Deep Sleep)



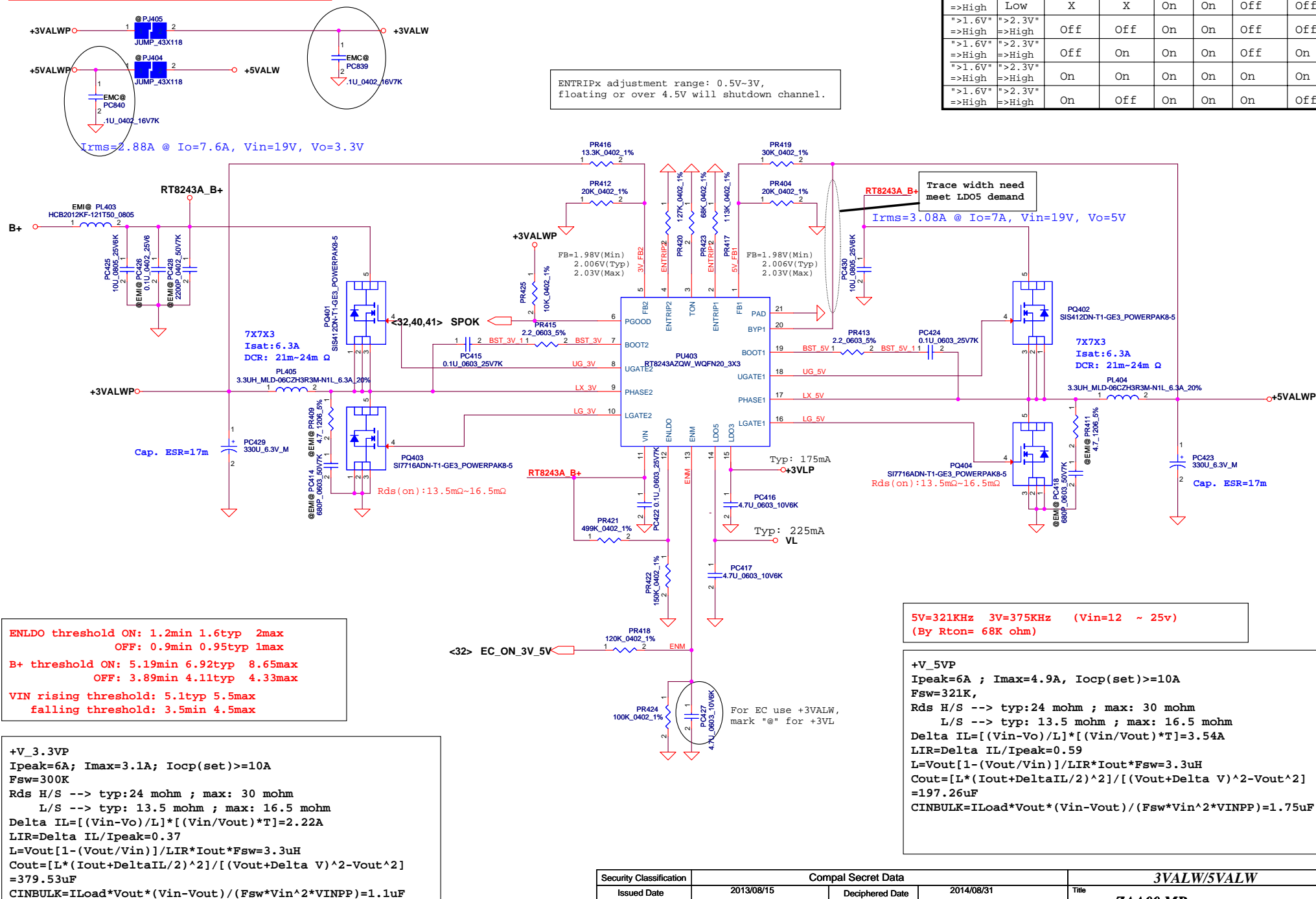
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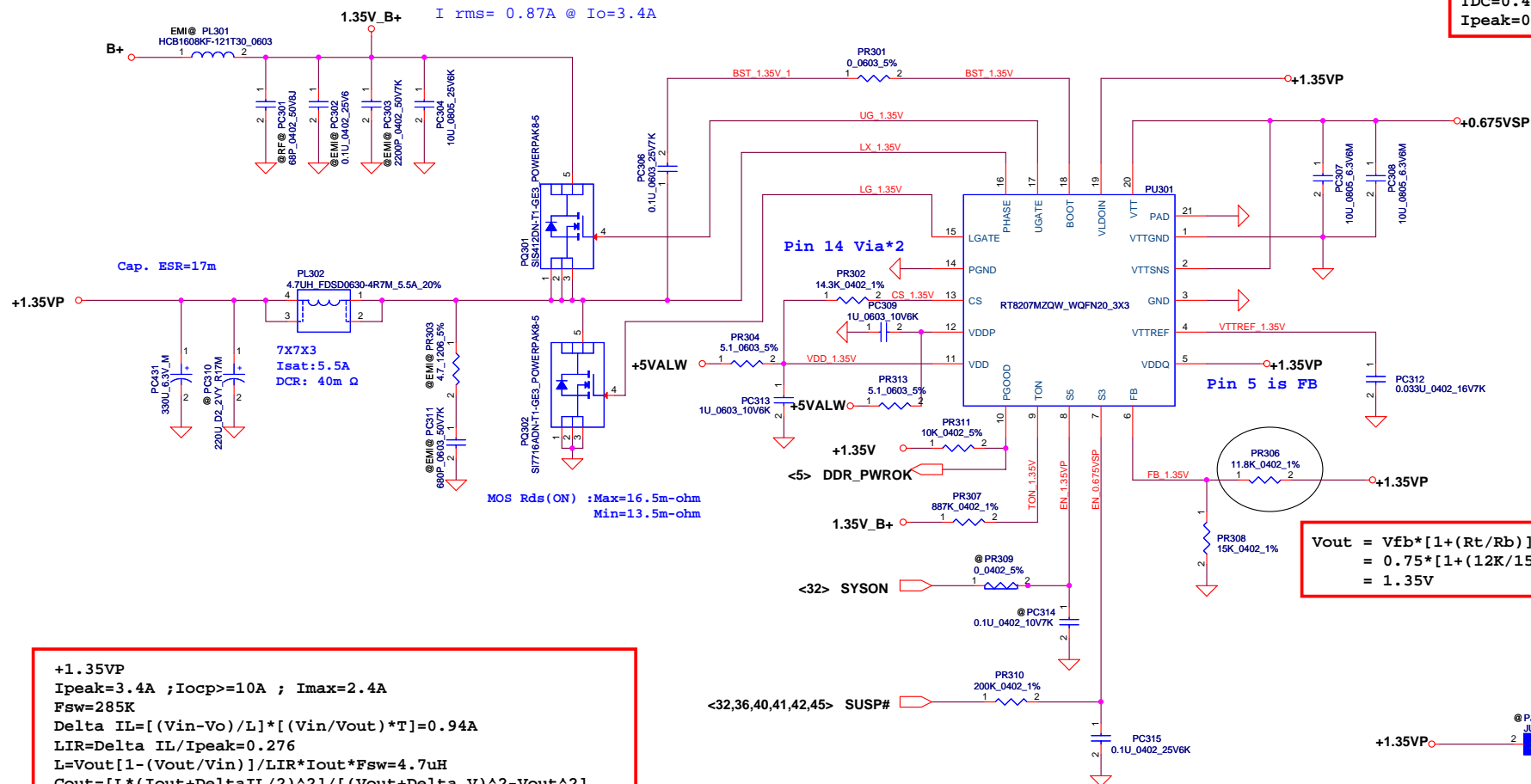
RT8243A_V1.mdd

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LD05	LD03	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off



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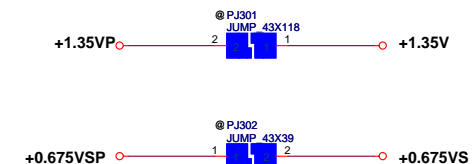
+0.675VSP
TDC=0.42A
Ipeak=0.6A ; 1.2Ipeak=0.72A

+1.35VP
Ipeak=3.4A ; Iocp>=10A ; Imax=2.4A
Fsw=285K
 $\Delta IL = [(V_{in}-V_o)/L] * [(V_{in}/V_{out}) * T] = 0.94A$
LIR=Delta IL/Ipeak=0.276
L=Vout[1-(Vout/Vin)]/LIR*Iout*Fsw=4.7uH
Cout=[L*(Iout+Delta IL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=634.18uF
CINBULK=Iload*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.38uF

Pin 14 Via*2

Pin 5 is FB

$$V_{out} = V_{fb} * [1 + (R_t/R_b)] = 0.75 * [1 + (12K/15K)] = 1.35V$$

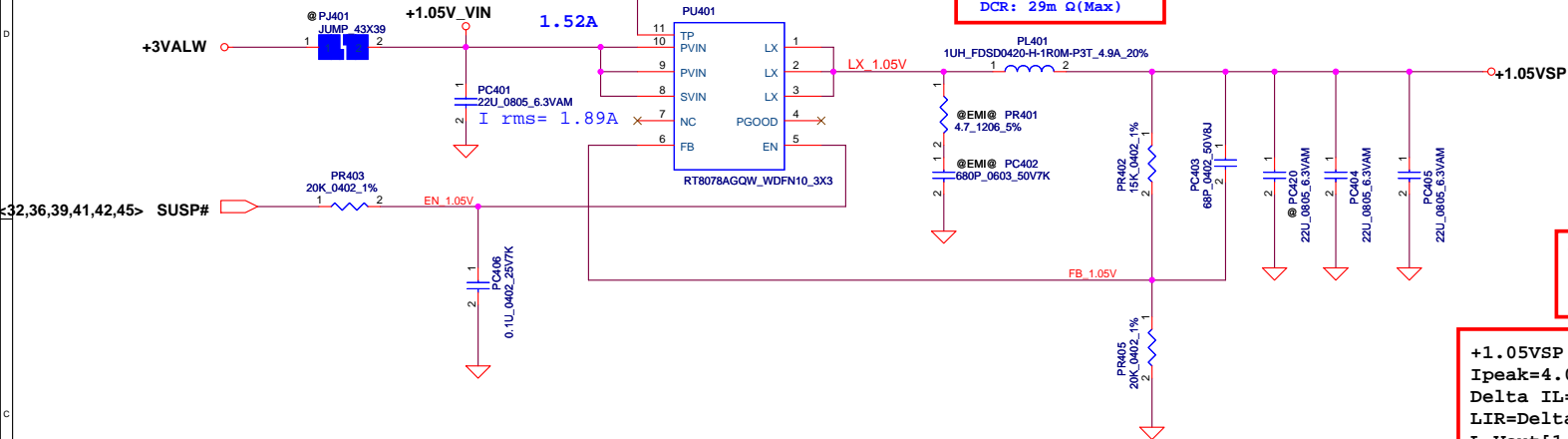


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+1.05VSP
 $V_{in} = 3.3V$
 $I_{in} = 4.05 \times 1.05 / 0.85 / 3.3$
 $= 1.52A$

+1.05VSP

4*4*2
 $I_{sat}: 9A$
 $DCR: 29m \Omega (Max)$



$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.6 * [1 + (15K / 20K)]$$

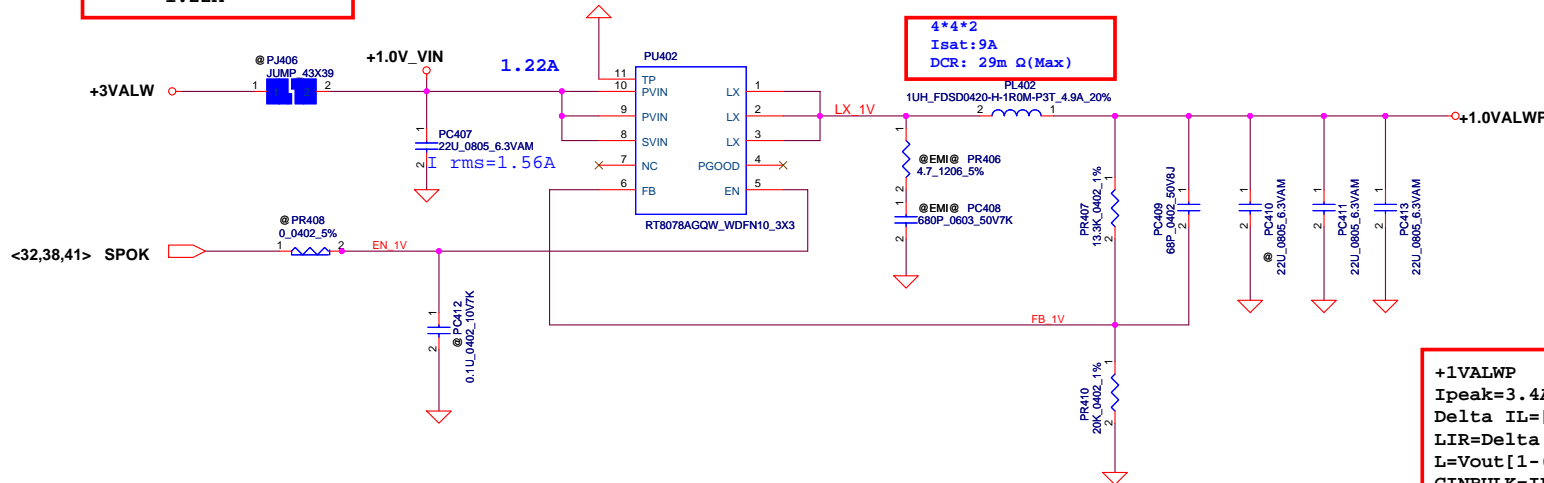
$$= 1.05V$$

+1.05VSP
 $I_{peak} = 4.05A$; $CL(min) \geq 4.4A$; $F_{sw} = 1MHz$
 $\Delta IL = [(V_{in} - V_o) / L] * [(V_{in} / V_{out}) * T] = 0.716A$
 $LIR = \Delta IL / I_{peak} = 0.177$
 $L = V_{out} [1 - (V_{out} / V_{in})] / LIR * I_{out} * F_{sw} = 1.0uH$
 $CINBULK = I_{Load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * VINPP) = 2.66uF$

+1.0VALWP
 $V_{in} = 3.3V$
 $I_{in} = 3.4 * 1.0 / 0.85 / 3.3$
 $= 1.22A$

+1.0VALWP

4*4*2
 $I_{sat}: 9A$
 $DCR: 29m \Omega (Max)$



$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.6 * [1 + (9.76K / 14.7K)]$$

$$= 1V$$

+1VALWP
 $I_{peak} = 3.4A$; $CL(min) \geq 4.4A$; $F_{sw} = 1MHz$
 $\Delta IL = [(V_{in} - V_o) / L] * [(V_{in} / V_{out}) * T] = 0.697A$
 $LIR = \Delta IL / I_{peak} = 0.205$
 $L = V_{out} [1 - (V_{out} / V_{in})] / LIR * I_{out} * F_{sw} = 1.0uH$
 $CINBULK = I_{Load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * VINPP) = 2.18uF$

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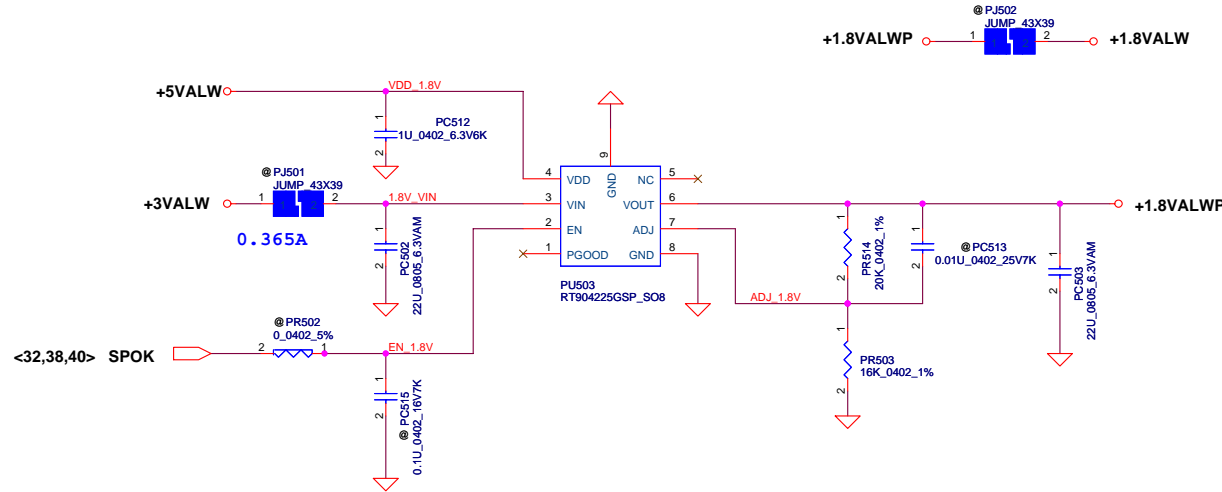
$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.8 * [1 + (20K / 16K)]$$

$$= 1.8V$$

+1.8VALWP
Ipeak=0.365A ;
Iocp>=3.1A

RT9042:
Quiescent Current (GND Current)
IQ(typ)=0.6mA, IQ(max)=1.2mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.551W
θ JA= 75°C/W*0.551=41.35°C



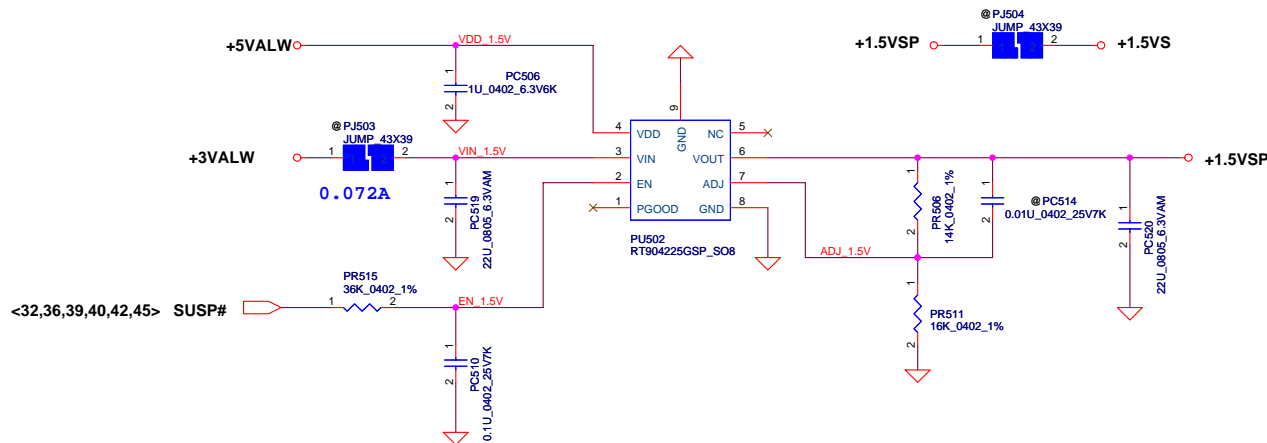
$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.8 * [1 + (14K / 16K)]$$

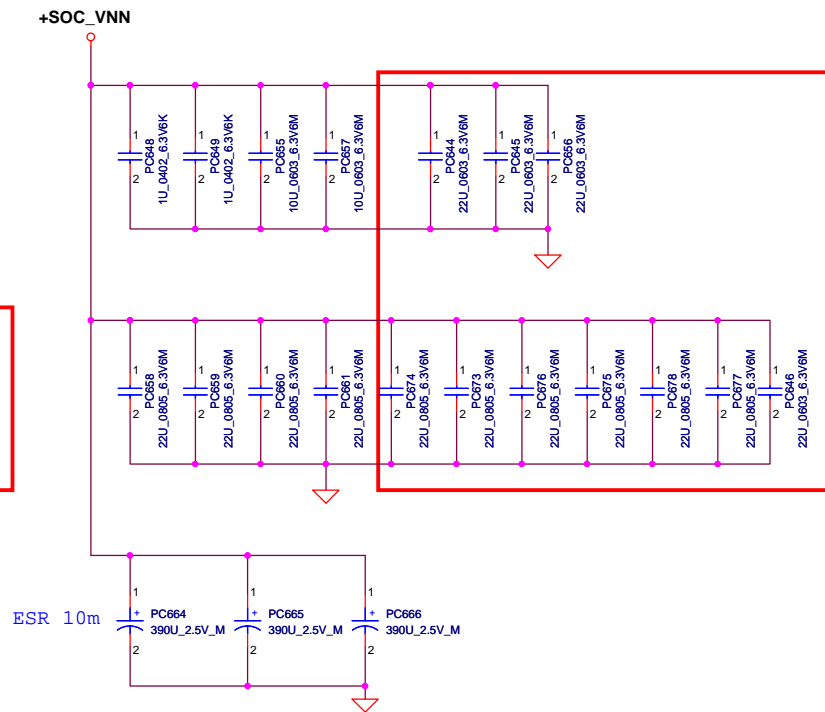
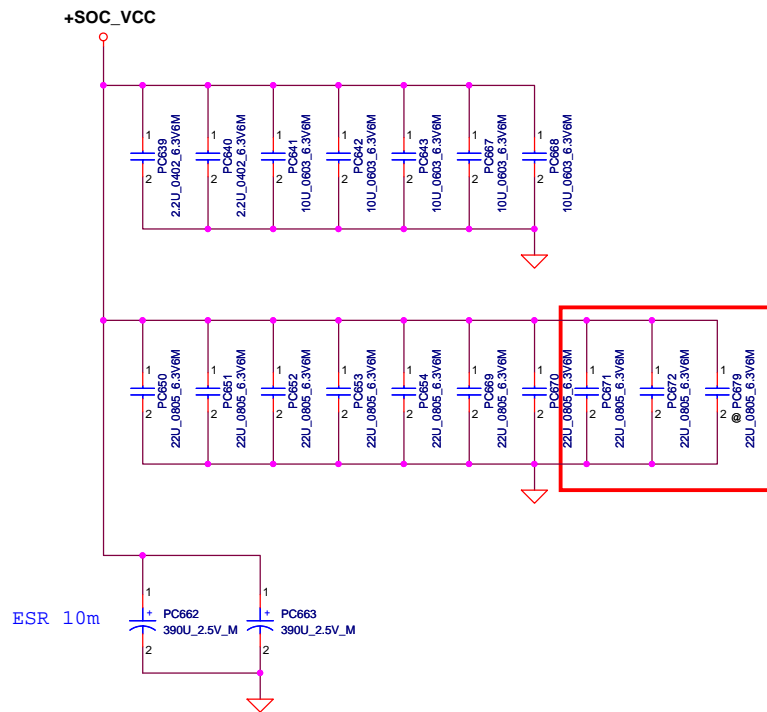
$$= 1.5V$$

+1.5VSP
Ipeak=0.072A
Iocp>=3.1A

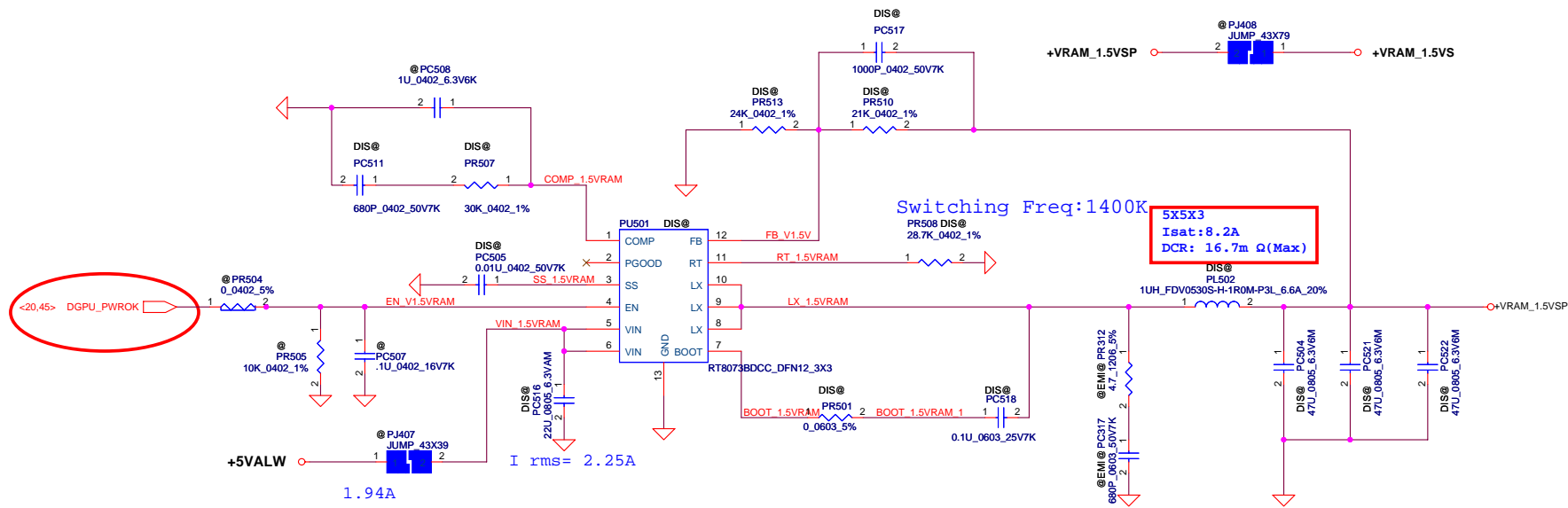
RT9042:
Quiescent Current (GND Current)
IQ(typ)=0.6mA, IQ(max)=1.2mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.133W
θ JA= 75°C/W*0.551=10.01°C



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$I_{peak} = 5.5A$, $I_{max} = 3.84A$, $F_{sw} = 1400KHz$
 $CL(min) = 7A$, $CL(typ) = 9A$
 $\Delta IL = [(V_{in} - V_o) / L] * [(V_{in} / V_{out}) * T] = 0.75A$
 $LIR = \Delta IL / I_{peak} = 0.136$
 $L = V_{out} [1 - (V_{out} / V_{in})] / LIR * I_{out} * F_{sw} = 1.0uH$
 $CINBULK = I_{Load} * V_{out} * (V_{in} - V_{out}) / (F_{sw} * V_{in}^2 * VINPP) = 1.65uF$

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POWER PIR (Product Improve Record)

ZAA00 LA-XXXX SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/08/xx

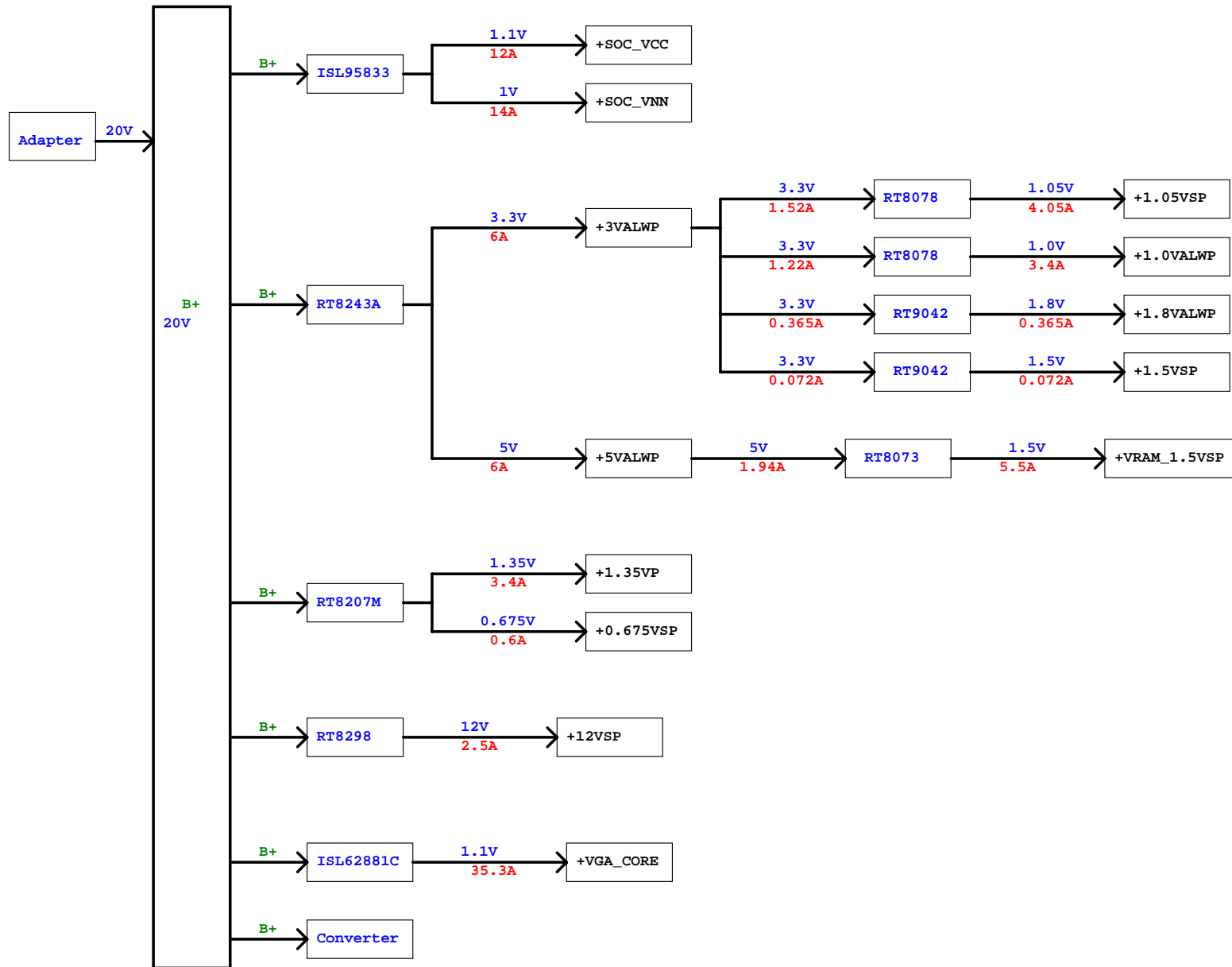
NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2013/08/12	43	PR814, PR833 change to 0402	module layout

NO	DATE	PAGE	MODIFICATION LIST(DVT)	PURPOSE
2	2013/09/14	39	change PR311 to 10K and pull high to +1.35V	design change
3	2013/09/17	43	change PC829 and PC817 to 0603 size	meet C38 MB design guide
4	2013/09/23	39	change PR306=12K, PR308=15K	meet voltage level
5	2013/09/23	44	add PC671,PC672,PC673,PC674,PC675,PC676, reserve PC677,PC678, PC679,PC646	meet Intel spec
6	2013/09/23	38	change PR418=12K, PR424=10K, PC417=un-pop	meet C38 MB design guide, light load Switching freq. >22KHz
7	2013/09/24	43	change PR807=324, PC815=0.022uF, PR839=274, PR837=100,PC830=1000pF, PL803=0.36uF, PL804=0.36uF, PC819= un-pop	meet Intel spec
8	2013/09/26	40,41	change PR403=20K, PR515=36K, PC406=0.1uF, PC510=0.1uF	meet Power sequence
9	2013/10/04	43	change PR802=100, PC805=220pF, PC812=1000pF	meet Intel spec
10	2013/10/04	37	change PC34=0.22uF, PC33=0.022uF	meet inrush spec
11	2013/10/08	46	change PC504=47uF, PC521=47uF, PC522=47uF, PR507=30k	meet Vram spec
12	2013/10/09	39	PC310=SGA00008S00	meet design spec

NO	DATE	PAGE	MODIFICATION LIST(PVT)	PURPOSE
13	2013/10/14	46	add PC517=1000pF	meet Vram spec
14	2013/10/29	43	1. Change the PC831 from 68pF to 120pF. 2. Change the PC834 from 150pF to 1000pF. 3. Change the PR838 from 649 Ohm to 2kOhm. 4. Change the PC804 from 68pF to 120pF. 5. Change the PC807 from 150pF to 1000pF. 6. Change the PR803 from 649 Ohm to 2kOhm.	solve can't boot issue
15	2013/11/12	38	1.PR418=120K 2.P424=100K	reduce current sink
16	2013/11/13	44	PC644,PC645,PC646,PC656= 22uF(0603 size) PU801= ISL95833B(SA000071G00)	meet Intel spec
17	2013/11/18	38,39	PR425=10K PR306=11.8K	HW request
18	2013/11/21	38	PC839, PC840=0.1uF	EMC request

NO	DATE	PAGE	MODIFICATION LIST(Pre MP)	PURPOSE
1	2013/12/20	ALL	Change to short pad PR171,PR819 PR2,PR168,PR177,PR178,PR179, PR182,PR183,PR184,PR186,PR188, PR189,PR203,PR309,PR502,PR504, PR822,PR821,PR408	cost down

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