

Compal Confidential

PLA00 LA6951P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

2011-02-24

REV: 1 . A

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File Name : LA6951P

2 :3D Display



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Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	ON	ON	OFF
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@ (VRAM:Hynix)
0	1	0	DIS@ (VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

BOARD ID Table

Board ID	Ra/Rb	Vad-bid
AV SKU	R442 100K	3.3V
NON AV SKU	R445 0 ohm	0 V

USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
	UHCI3	6	USB 2.0
7		3D IR	
EHCI2	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(WLAN)
	UHCI6	12	Mini Car(TV Tuner)
		13	

BTO Option Table

BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
CRT	CRT@
PCML606	1606@
Samsung VRAM (1G)	x76_SAM@
Hynix VRAM (1G)	x76_HYN@
Samsung VRAM (2G)	x76_SAM2G@
Hynix VRAM (2G)	x76_HYN2G@
AV-IN SKU	AV@
No AV-IN SKU	NON_AV@

EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

PCH SM Bus address

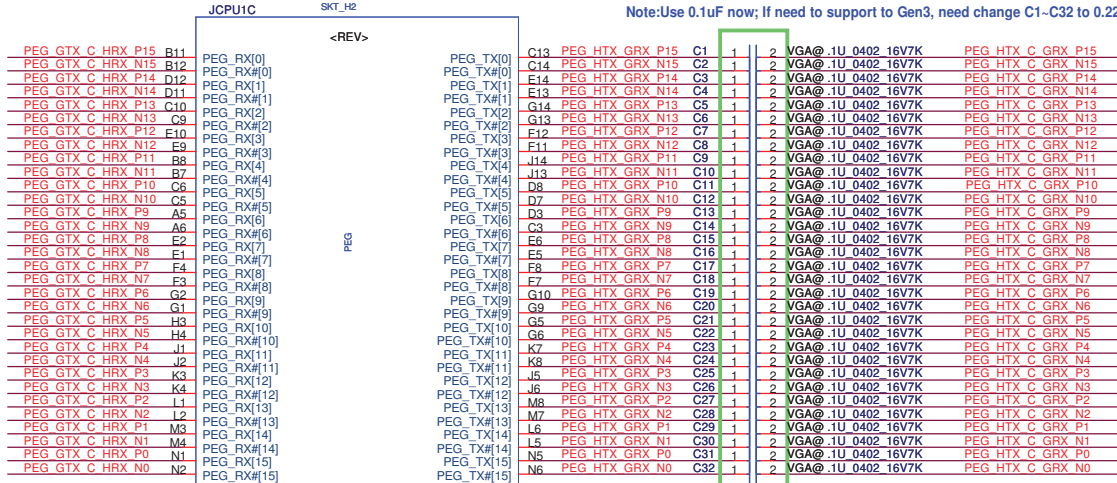
Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

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DMI_PTX_HRX_N[0..3] <14>
DMI_PTX_HRX_P[0..3] <14>
DMI_HTX_PRX_N[0..3] <14>
DMI_HTX_PRX_P[0..3] <14>

PEG GTX_C_HRX_P[0..15] <22>
PEG GTX_C_HRX_N[0..15] <22>
PEG HTX_C_GRX_P[0..15] <22>
PEG HTX_C_GRX_N[0..15] <22>

Note:Use 0.1uF now; If need to support to Gen3, need change C1~C32 to 0.22uF.

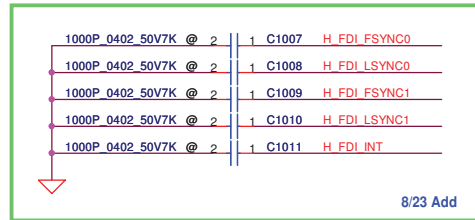


DMI_PTX_HRX_P0 W5
DMI_PTX_HRX_N0 W4
DMI_PTX_HRX_P1 V3
DMI_PTX_HRX_N1 V4
DMI_PTX_HRX_P2 V3
DMI_PTX_HRX_N2 Y4
DMI_PTX_HRX_P3 AA4
DMI_PTX_HRX_N3 AA5
DMI_RX[0] DMI_TX[0]
DMI_RX[1] DMI_TX[1]
DMI_RX[2] DMI_TX[2]
DMI_RX[3] DMI_TX[3]
DMI_RX[4] DMI_TX[4]
DMI_RX[5] DMI_TX[5]
DMI_RX[6] DMI_TX[6]
DMI_RX[7] DMI_TX[7]
DMI_RX[8] DMI_TX[8]
DMI_RX[9] DMI_TX[9]
DMI_RX[10] DMI_TX[10]
DMI_RX[11] DMI_TX[11]
DMI_RX[12] DMI_TX[12]
DMI_RX[13] DMI_TX[13]
DMI_RX[14] DMI_TX[14]
DMI_RX[15] DMI_TX[15]

7/20 PE_RX[0~3]/PE_TX[0~3] only use on Workstation.

7/20 PE_TX[0~3]/PE_TX[0~3] only use on Workstation.

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - ;Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils
- Width/Space (12 mils/15mils)



8/23 Add

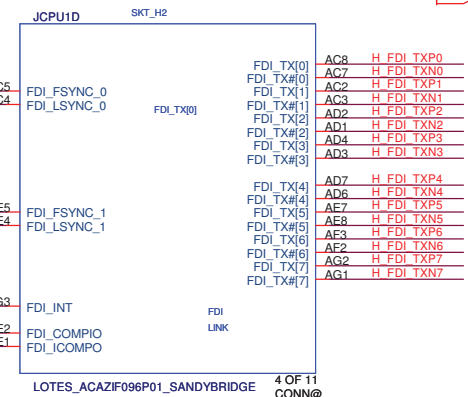
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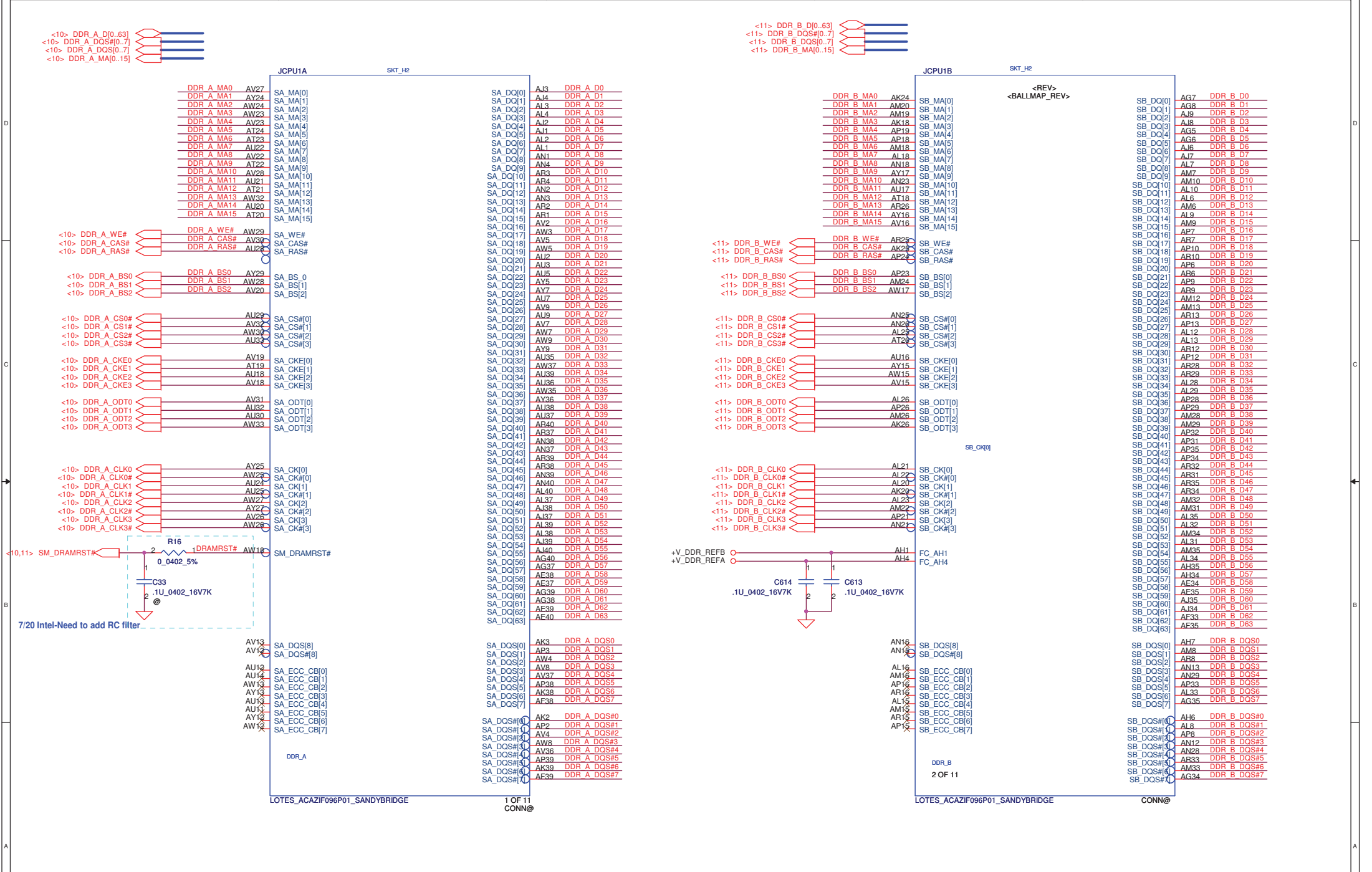
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24.9_0402_1% 2 R2

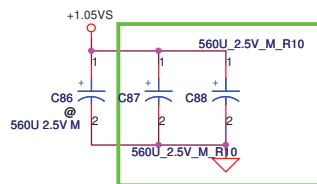
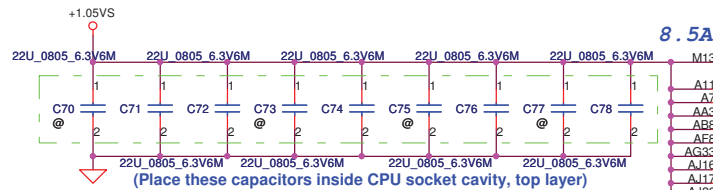


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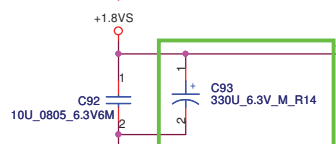
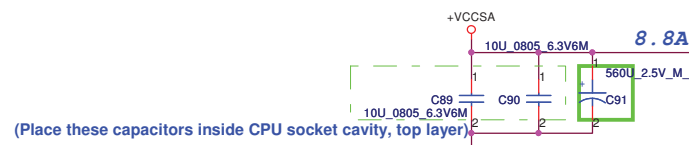


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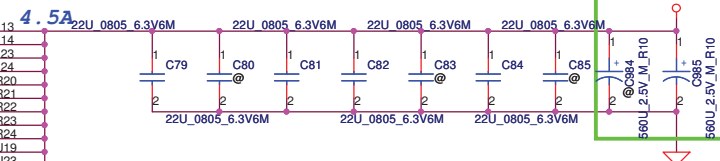
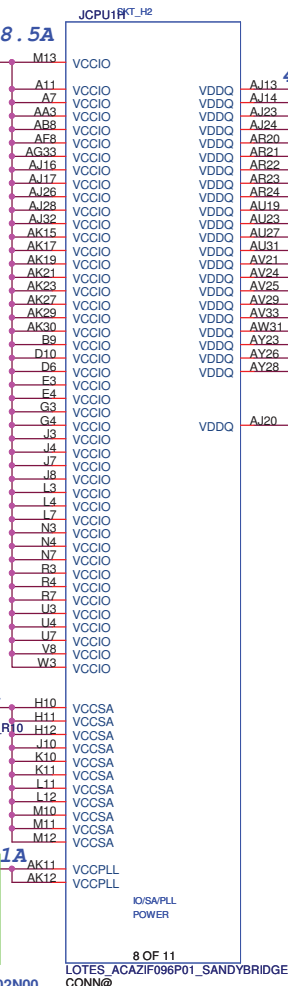


11/2 Change PN of C87/C88 from SF000001P00 to SF000001K00

11/4 Change PN of C91 from SF000001P00 to SF000001K00

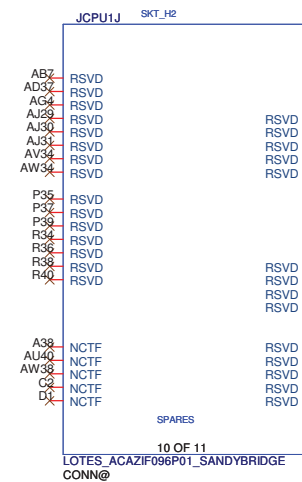
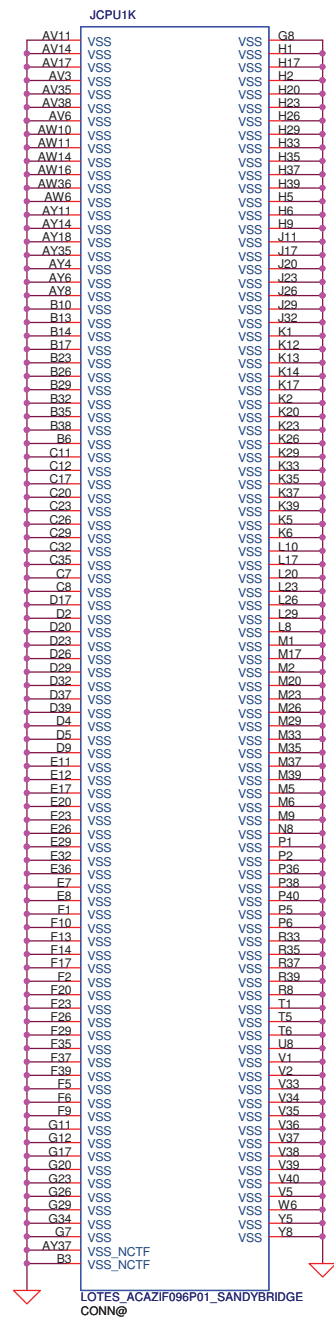
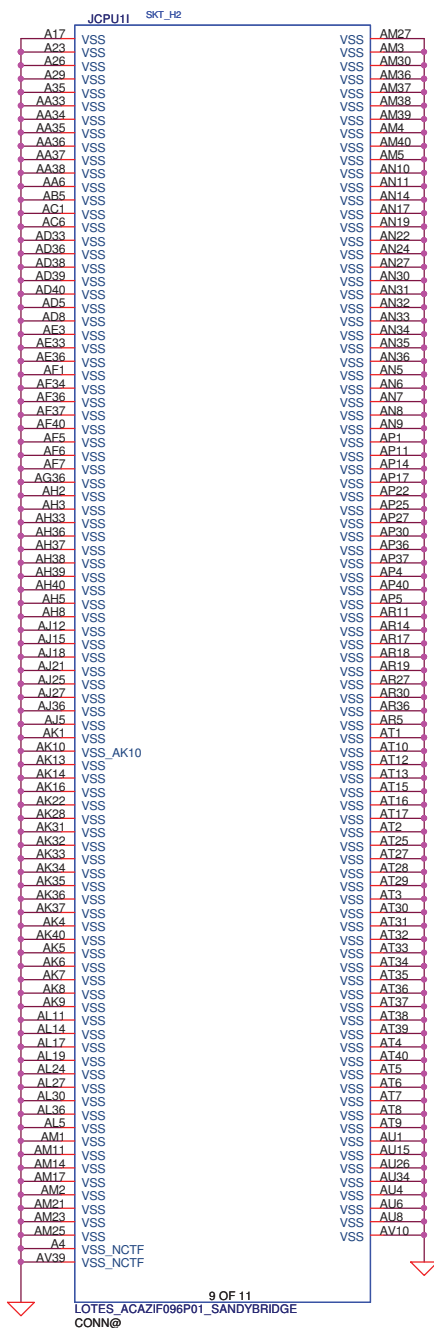


10/23 Change symbol of C93 from SGA00000Y80 to SF000002N00
11/4 Change PN of C93 from SF000002N00 to SF000001G00



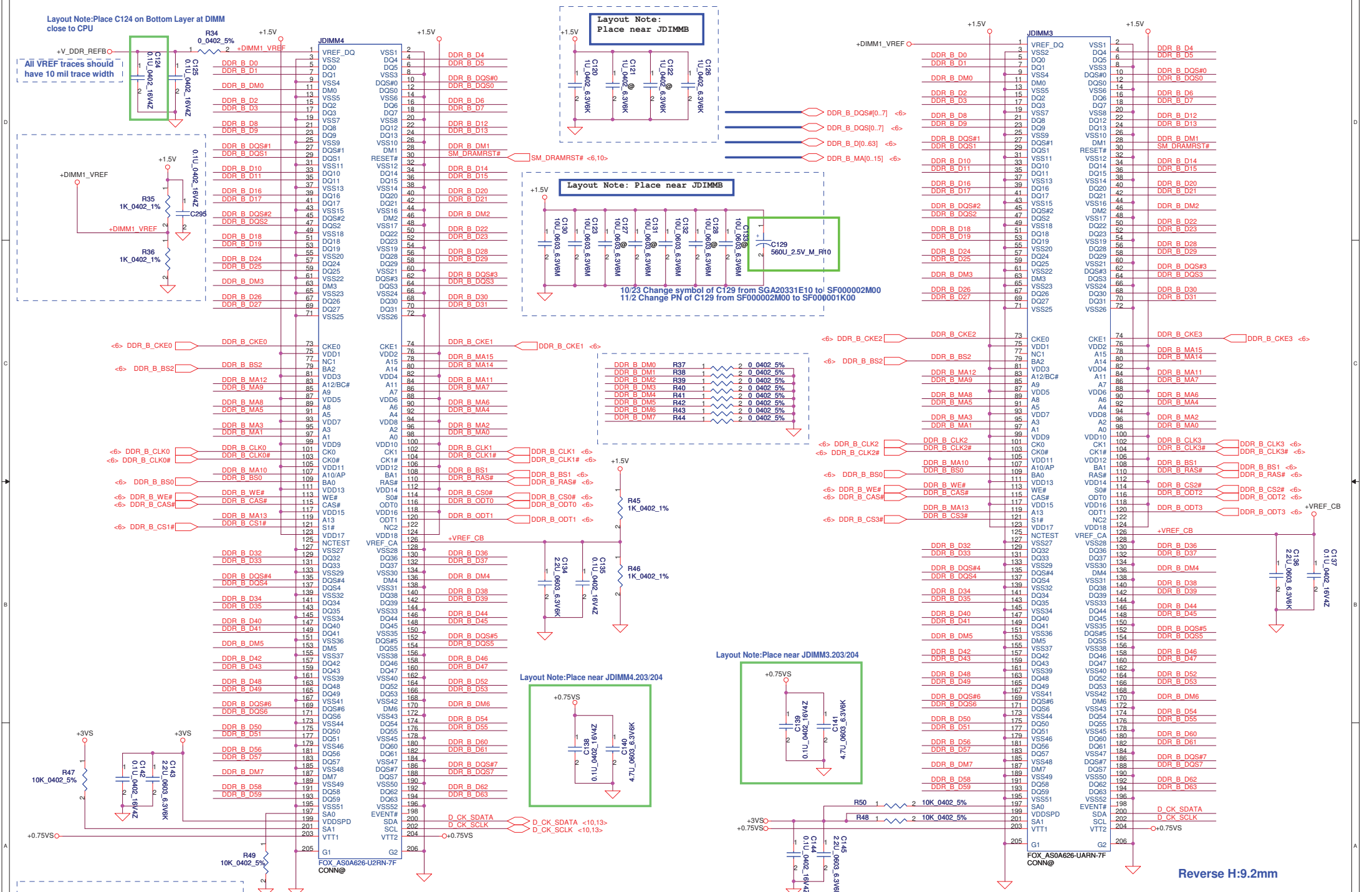
11/2 Change PN of C984/C985 from SF000002000 to SF000001K00

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<41> HDA_BITCLK_AUDIO <R69> 1 2 HDA_BITCLK_PCH 33_0402_5%

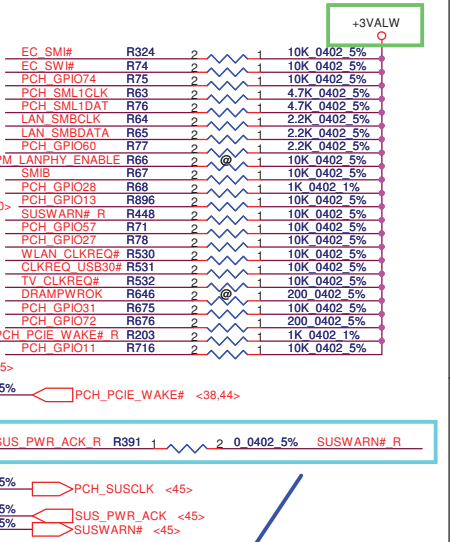
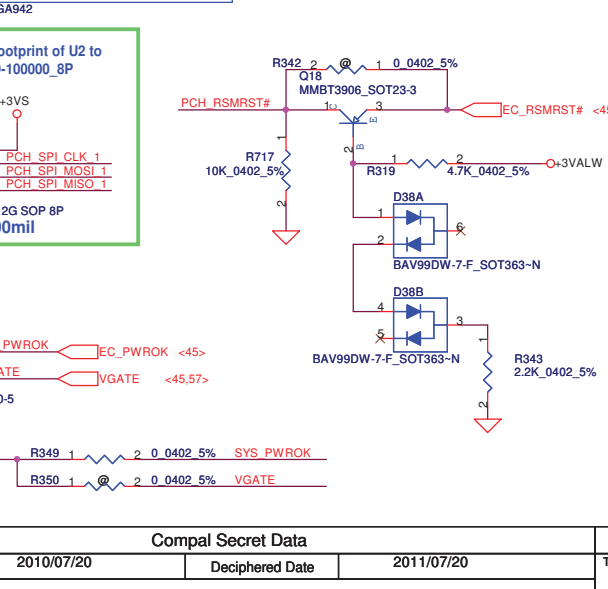
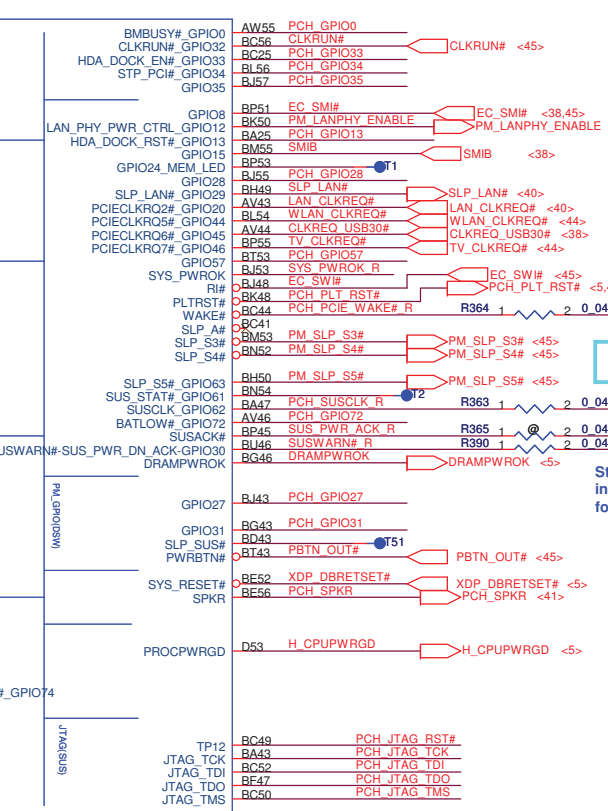
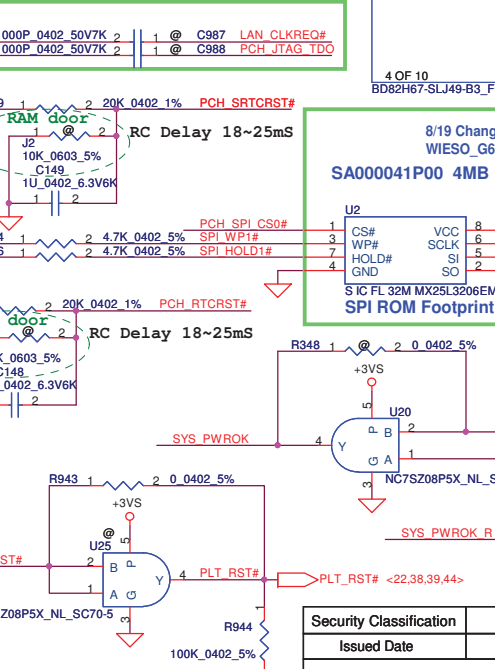
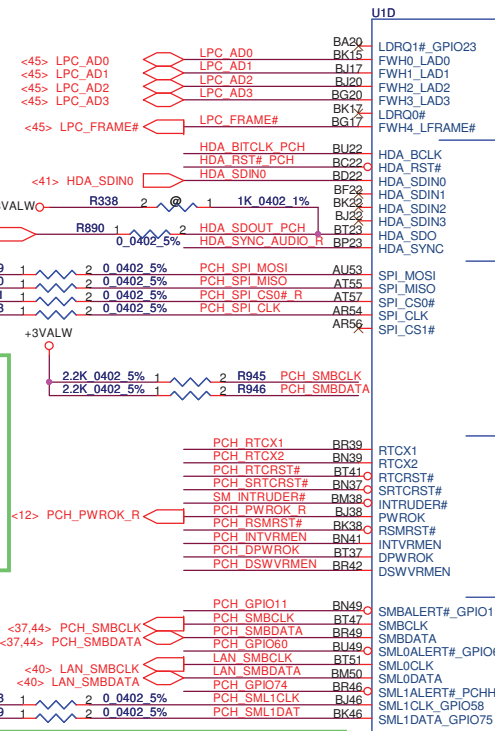
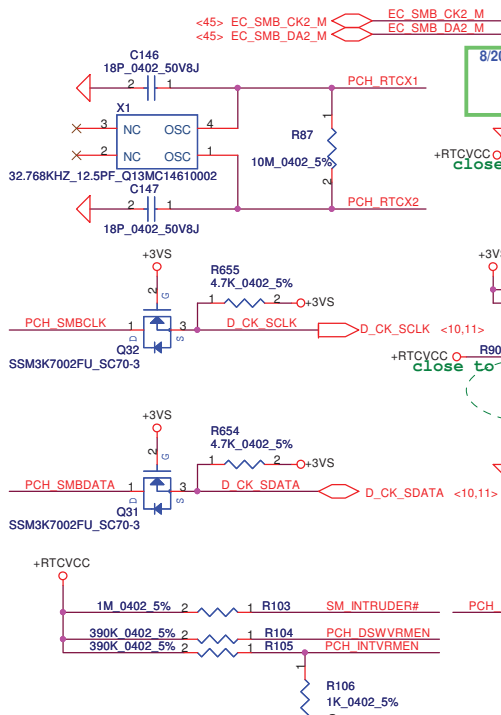
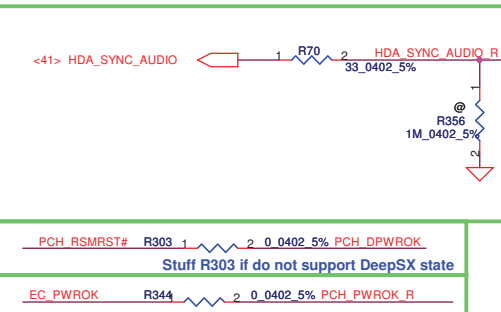
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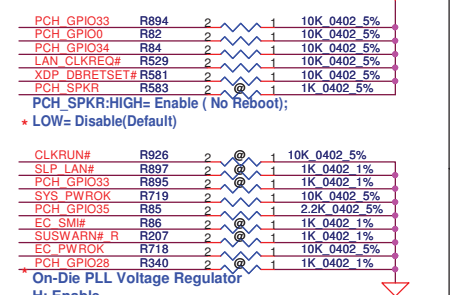
ME debug mode,
this signal has a weak internal pull down

- ★ Low = Disable (default)
- High = Enable (flash descriptor security override)

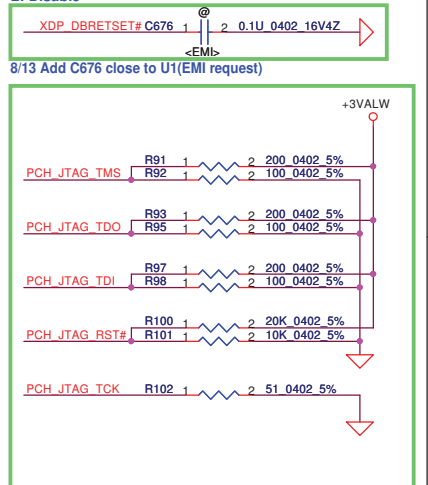
This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
★Need to pull high for Huron River platform



Stuff R391 if EC don't want to involve in the handshake mechanism for the DeepSX state entry and exit



On-Die PLL Voltage Regulator
H: Enable
L: Disable



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<4> DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
<4> DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
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+1.05VS_PCH
R107
49.9_0402_1%
1 2

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DMI_HTX_PRX_P0 B33
DMI_PTX_HRX_N0 J36
DMI_PTX_HRX_P0 H36
DMI_HTX_PRX_N1 A36
DMI_HTX_PRX_P1 B35
DMI_PTX_HRX_N1 P38
DMI_PTX_HRX_P1 B37
DMI_HTX_PRX_N2 B38
DMI_HTX_PRX_P2 C36
DMI_PTX_HRX_N2 H38
DMI_PTX_HRX_P2 J38
DMI_HTX_PRX_N3 E37
DMI_HTX_PRX_P3 F38
DMI_PTX_HRX_N3 M41
DMI_PTX_HRX_P3 P41
DMI_COMP E31

U1B CPT_CRB

DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_IRCOMP
DMI_ZCOMP
CLKIN_DMI_N
CLKIN_DMI_P

CLK_BUF_CPU_DMI# P33
CLK_BUF_CPU_DMI R33
PCIE_DTX_C_PRX_N1 J20
PCIE_DTX_C_PRX_P1 L20
PCIE_PTX_DRX_N1 E25
PCIE_PTX_DRX_P1 F23
PCIE_DTX_C_PRX_N2 P20
PCIE_DTX_C_PRX_P2 R20
PCIE_PTX_DRX_N2 C22
PCIE_PTX_DRX_P2 A22

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PETP8

5D82H67-SLJ49-B3_FCBGA942

DMI

PCI

PCI

2 OF 10

USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P

BF36 USB20_N0
BD36 USB20_P0
BA33 USB20_N1
BM33 USB20_N2
BM35 USB20_P2
BT33 USB20_N3
BR32 USB20_P3
BT31 USB20_P4
BN29 USB20_N5
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BK33 USB20_N6
BJ33 USB20_P6
BF31 USB20_N7
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USB20_N7 <48>
USB20_P7 <48>

USB Conn
USB Conn
USB Conn
USB Conn
Touch Screen
Web Camera
USB 2.0
3D IR
USB 2.0
Bluetooth
Mini Card(WLAN)
Mini Card(TV Tuner)

EHCI 1

EHCI 2

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

OC0#_GPIO59
OC1#_GPIO40
OC2#_GPIO41
OC3#_GPIO42
OC4#_GPIO43
OC5#_GPIO9
OC6#_GPIO10
OC7#_GPIO14
BM43 USB_OC#0
BD41 USB_OC#1
BG41 USB_OC#2
BK43 USB_OC#34
BP43
BJ41 USB_OC#5 R
BT45 USB_OC#6 R
BM45 USB_OC#7 R

USB_OC#0 <46>
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USB_OC#34 <38>

USBRBIAS#
USBRBIAS
CLKIN_DOT_96N
CLKIN_DOT_96P
DMI2RBIAS

BP25 USB_BIAS
BM25
BD38 CLK_BUF_DREF_96M#
BF38 CLK_BUF_DREF_96M
A32 DMI2RBIAS

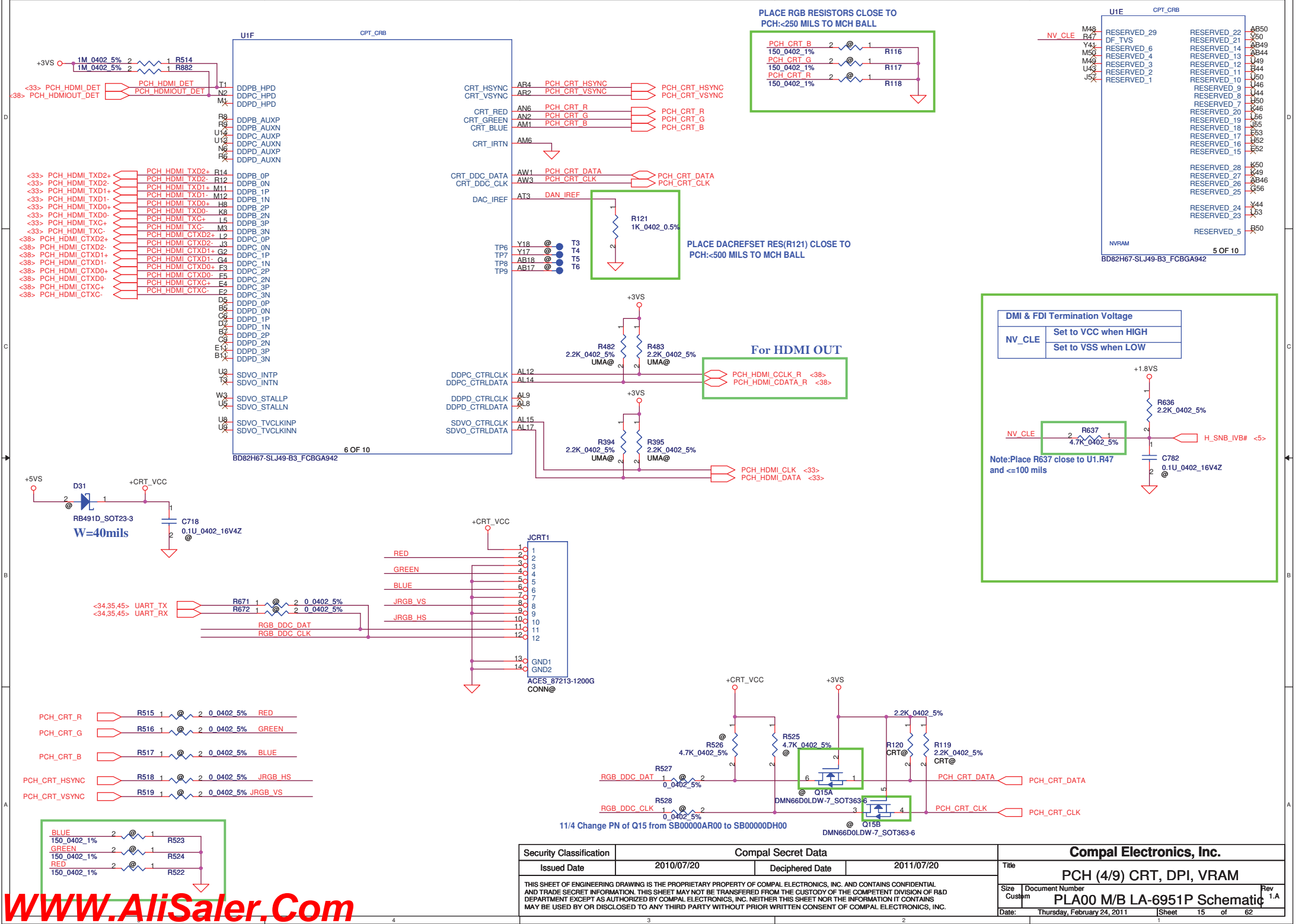
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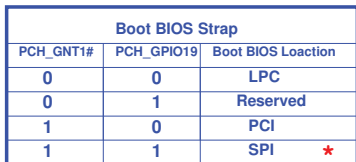
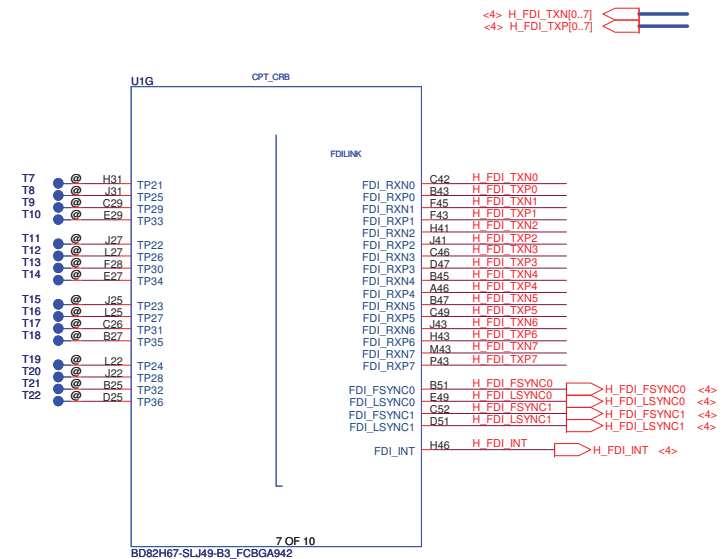
R108
22.6_0402_1%
R109
750_0402_1%

USB_OC#2 R R110 1 2 10K 0402 5%
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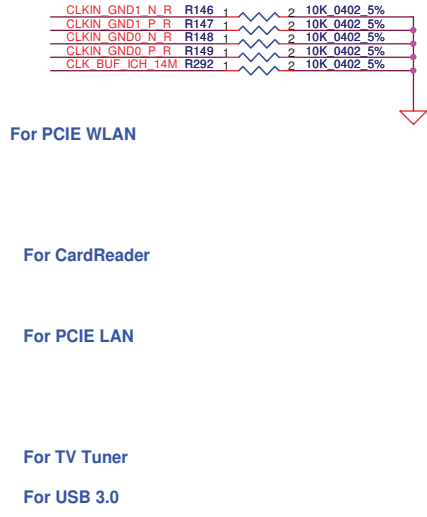
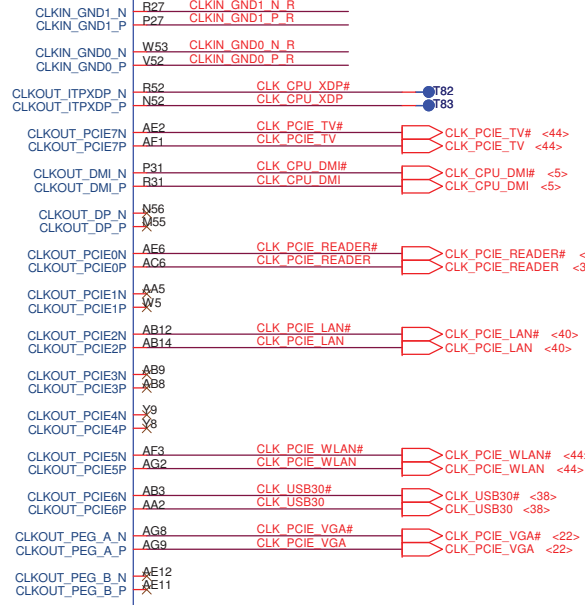
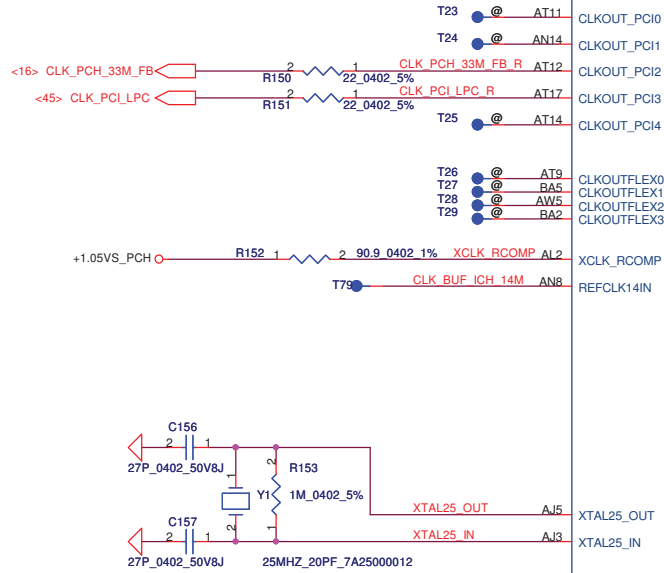
CLK_BUF_DREF_96M# R357 1 2 10K 0402 5%
CLK_BUF_DREF_96M R358 1 2 10K 0402 5%
CLK_BUF_CPU_DMI# R359 1 2 10K 0402 5%
CLK_BUF_CPU_DMI R360 1 2 10K 0402 5%

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Size A	Document Number	PLA00 M/B LA-6951P Schematic		Rev	1.A
Date:	Thursday, February 24, 2011	Sheet	14	of	62





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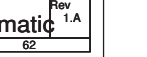
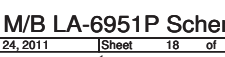
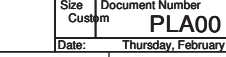
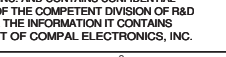
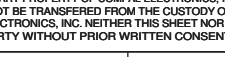
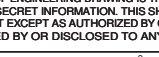
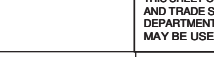
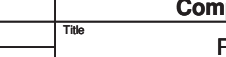
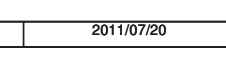
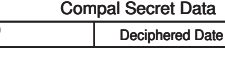
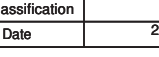
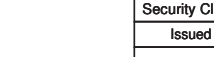
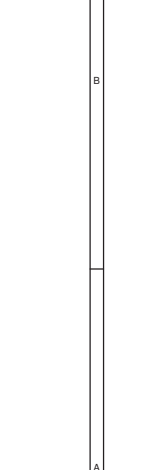
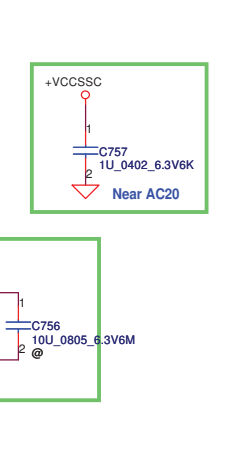
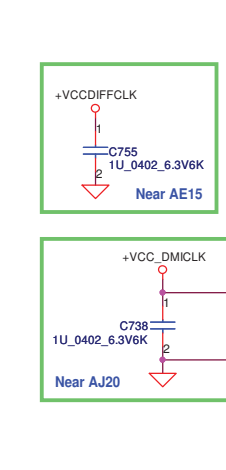
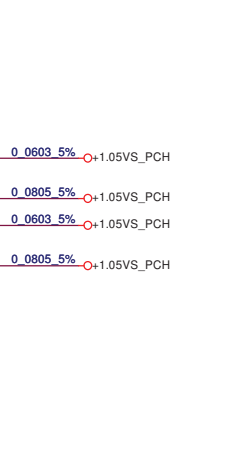
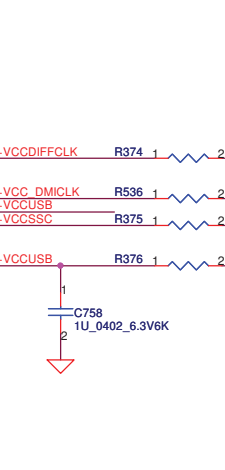
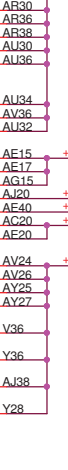
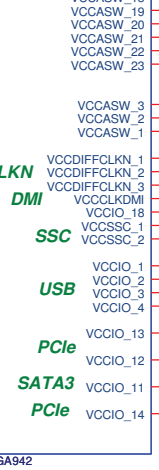
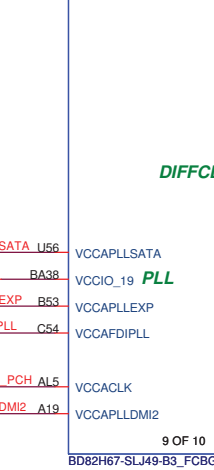
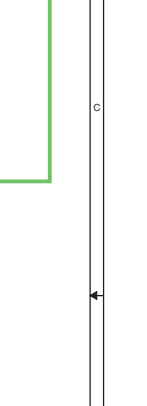
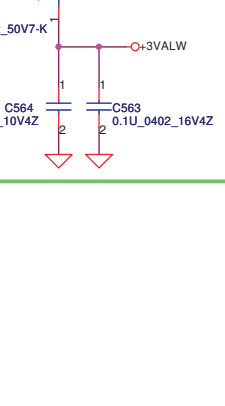
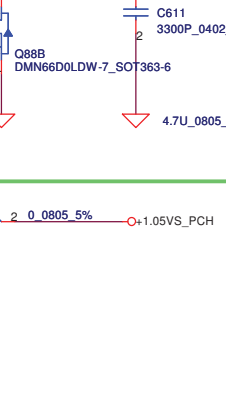
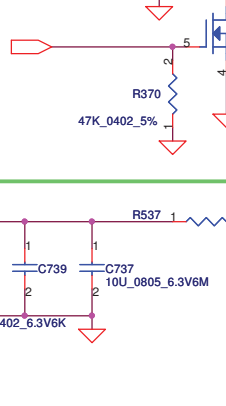
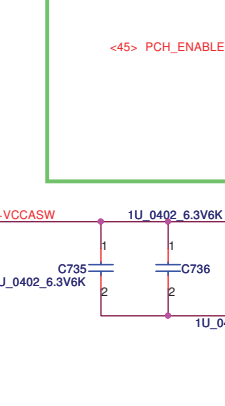
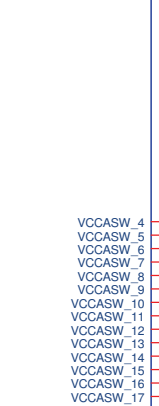
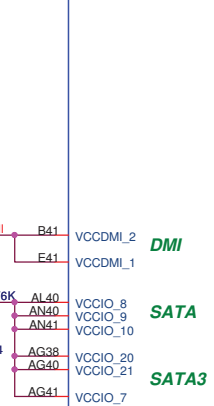
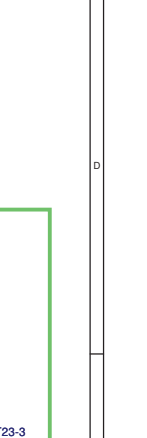
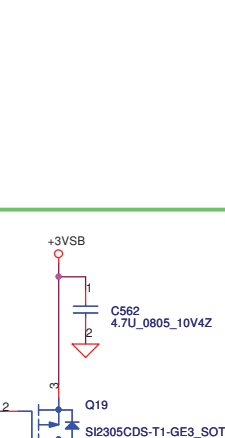
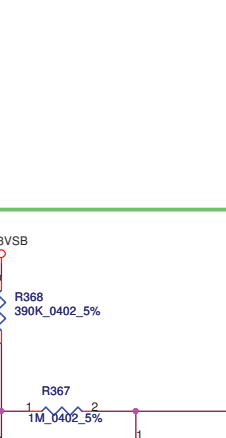
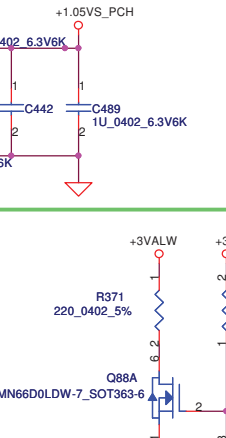
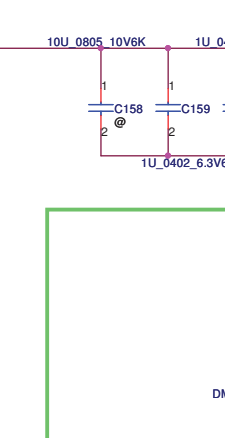
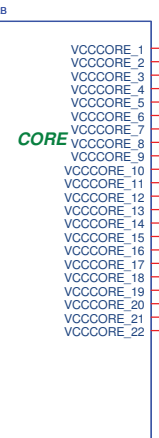
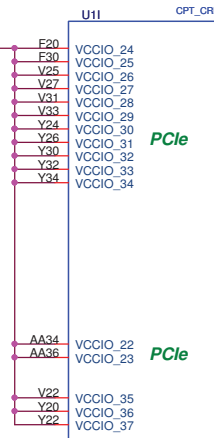
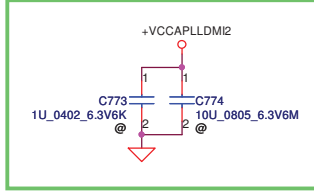
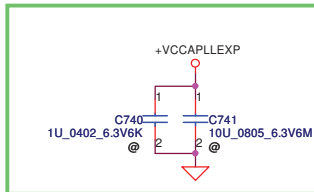
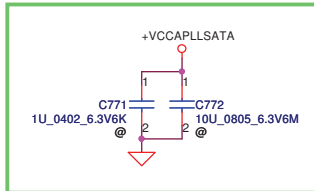
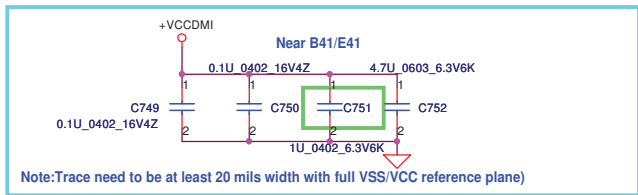
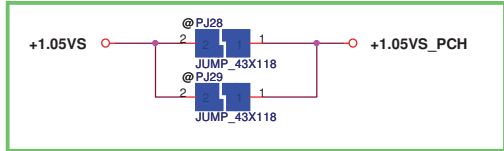
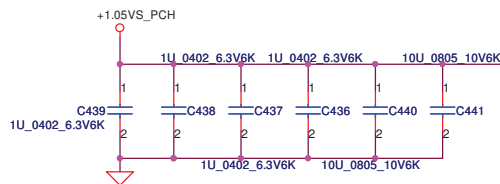


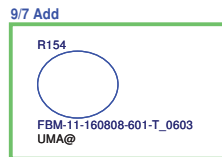
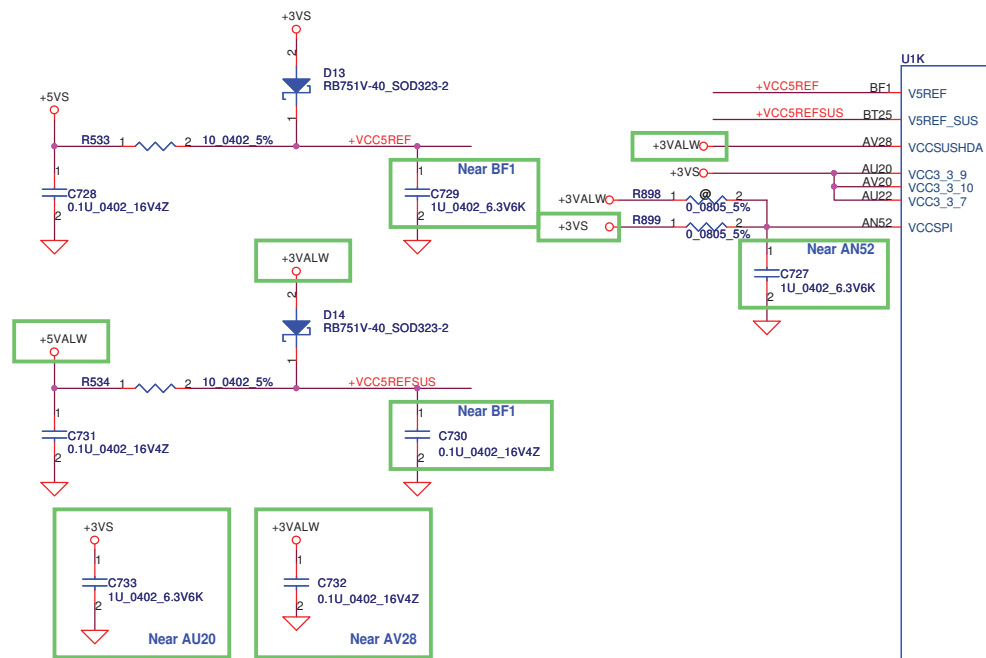
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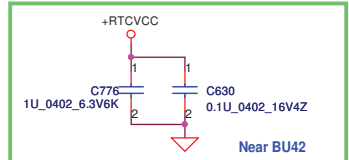
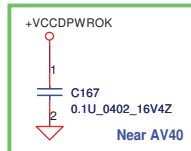
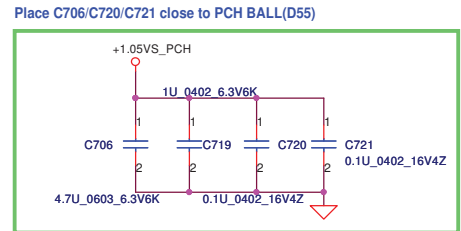
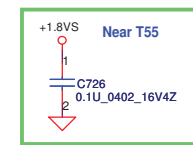
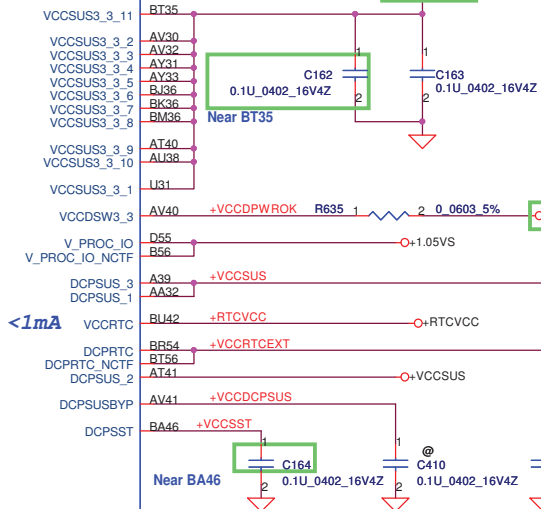
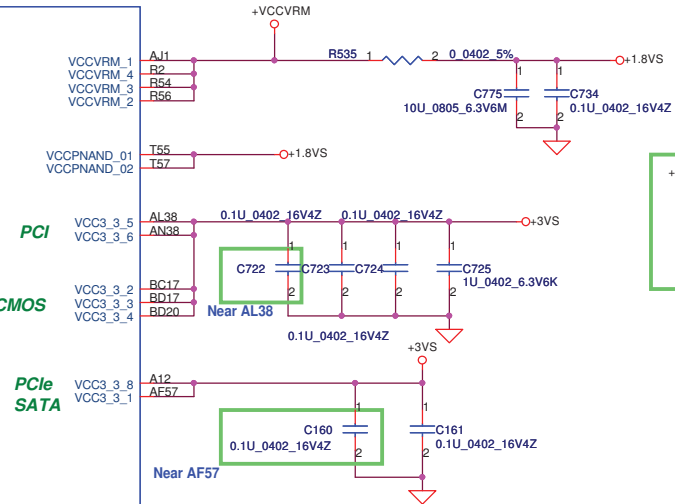
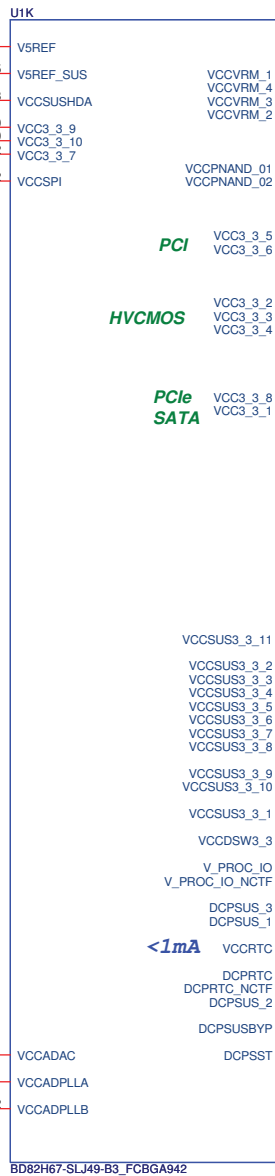
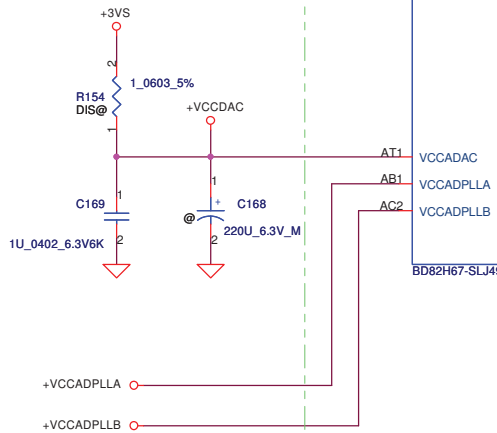
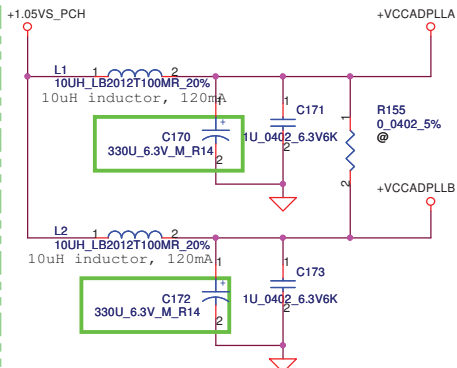
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Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic	Rev	1.A
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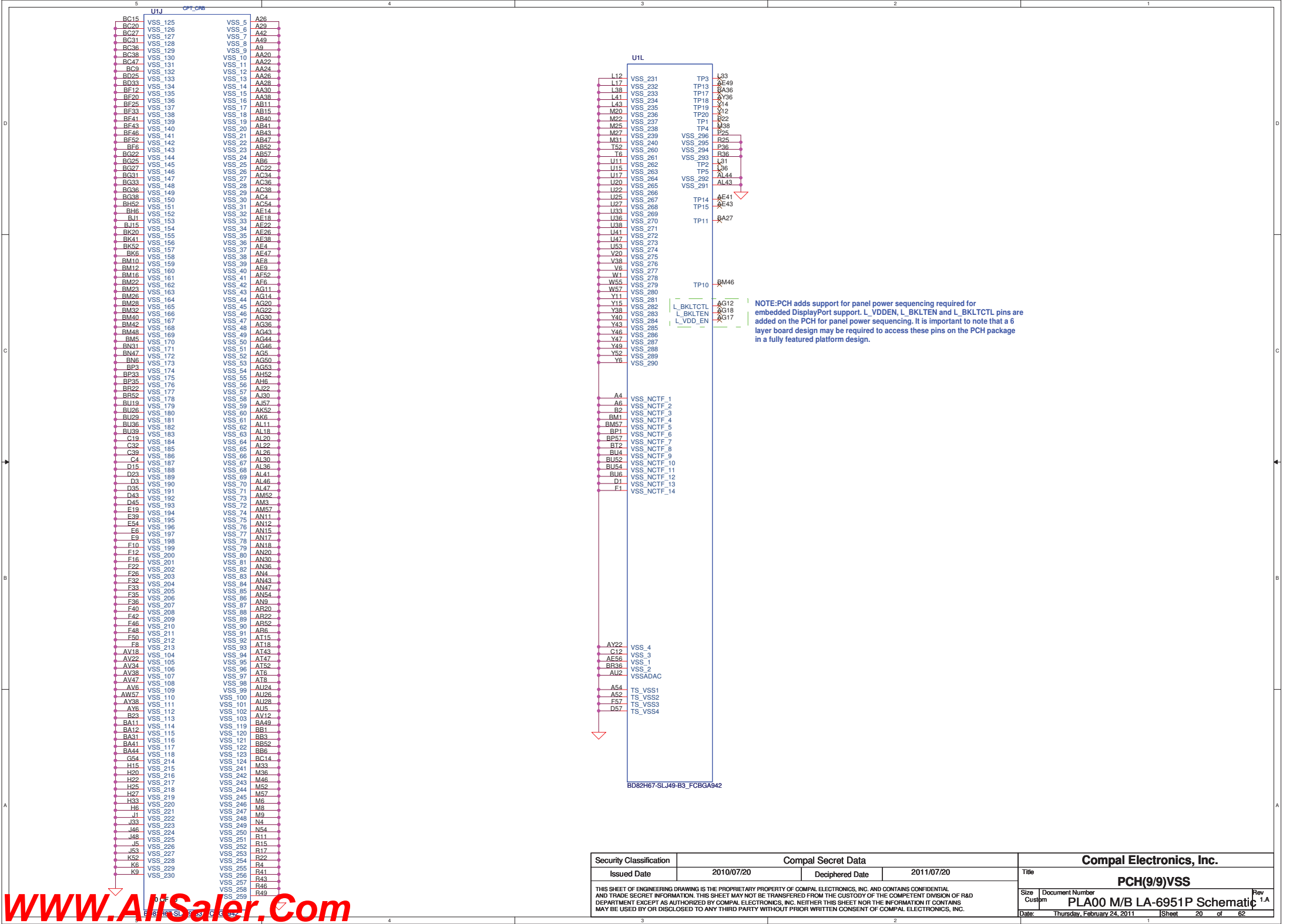


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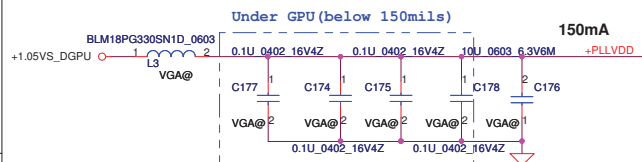


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Size	Document Number	Rev		Date	
Custom	PLA00 M/B LA-6951P Schematic	1.A		Thursday, February 24, 2011	
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62					

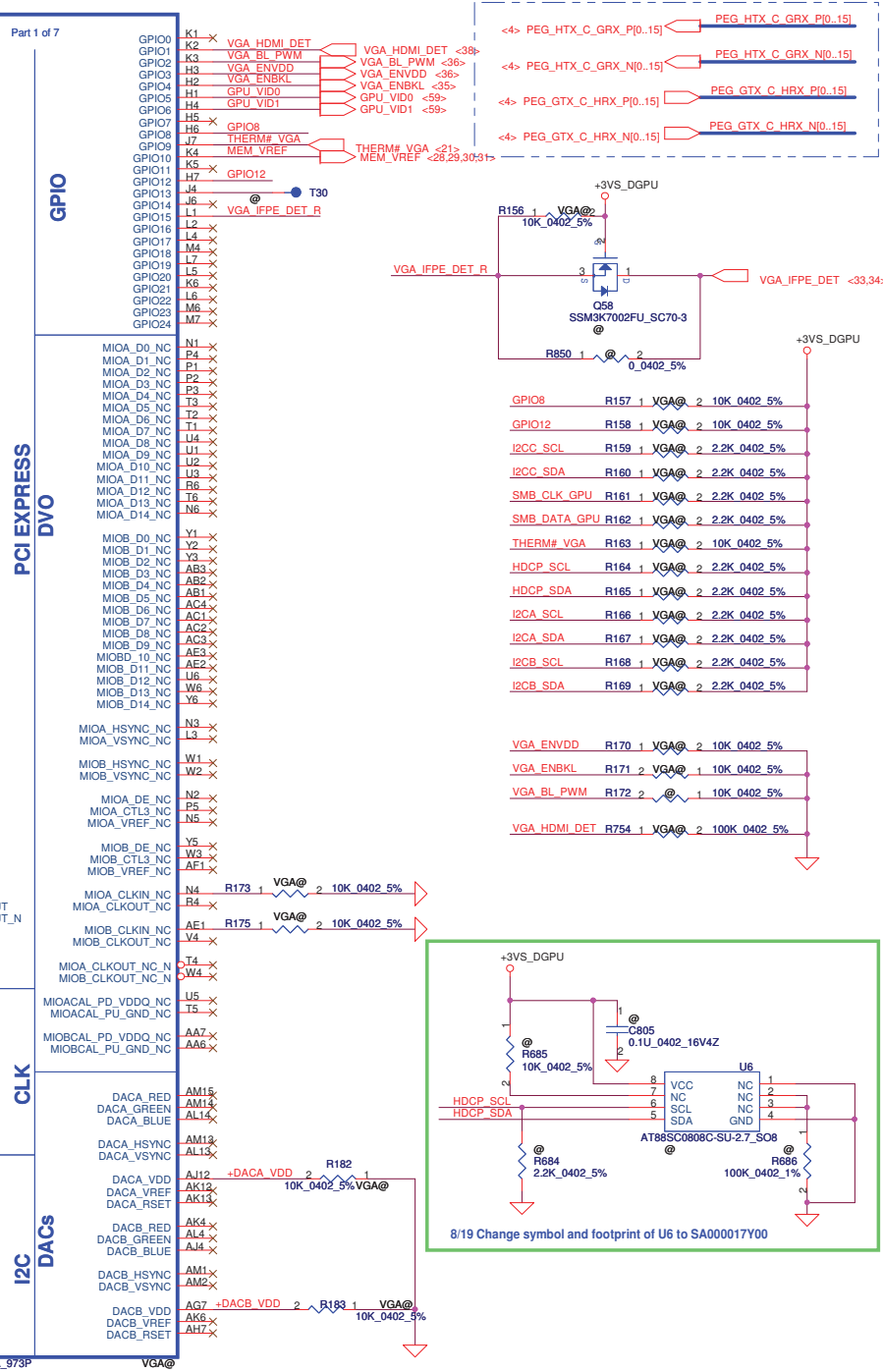
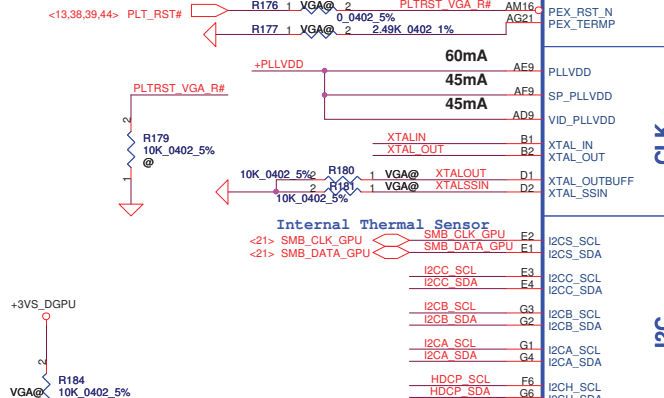
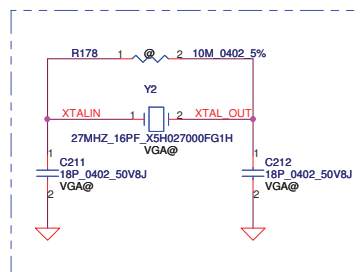
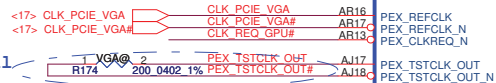


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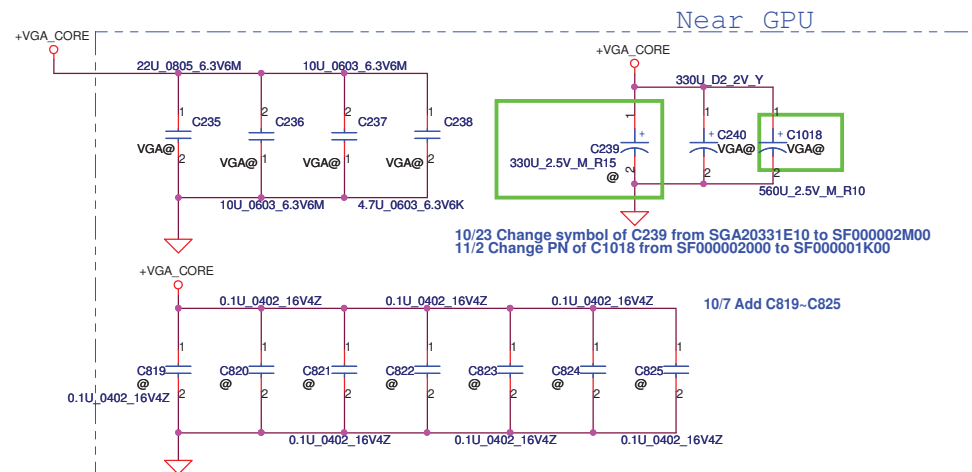
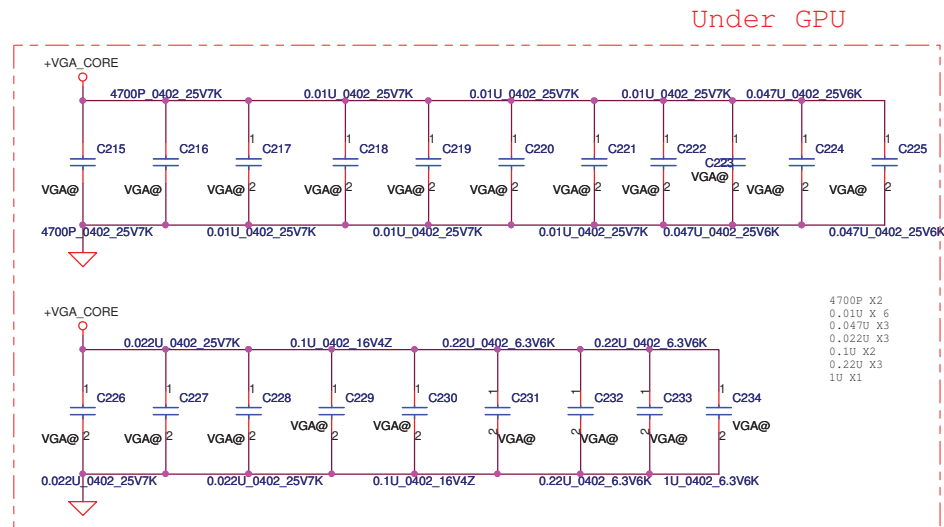
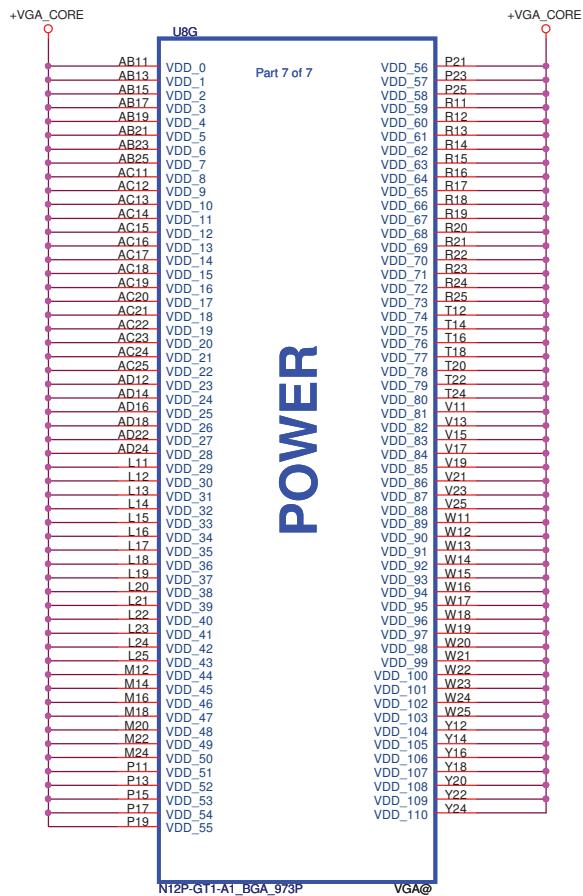
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						Date:		Thursday, February 24, 2011		Sheet 20 of 62	



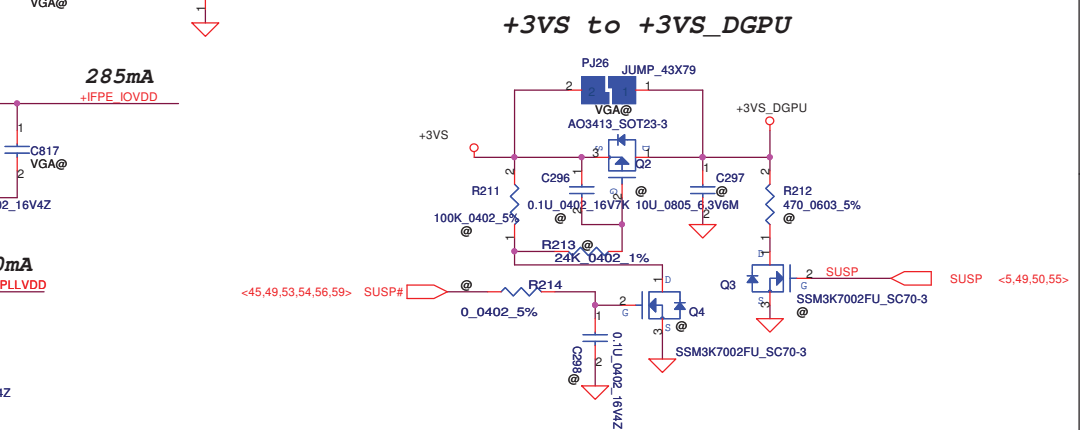
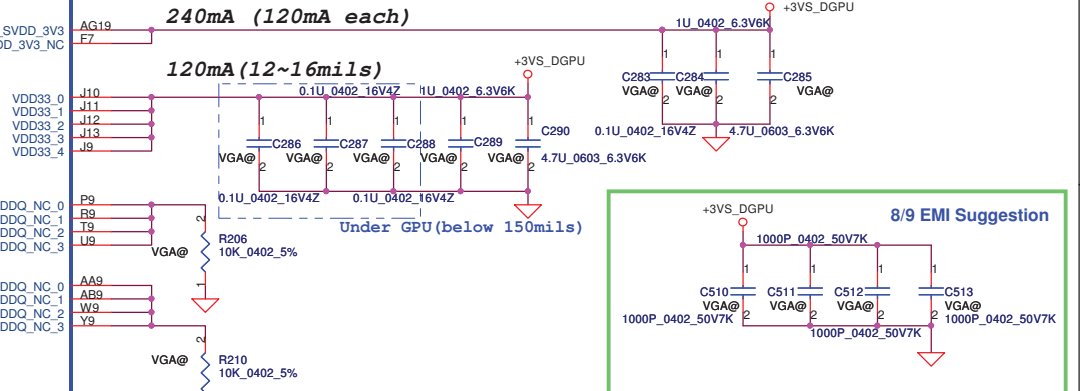
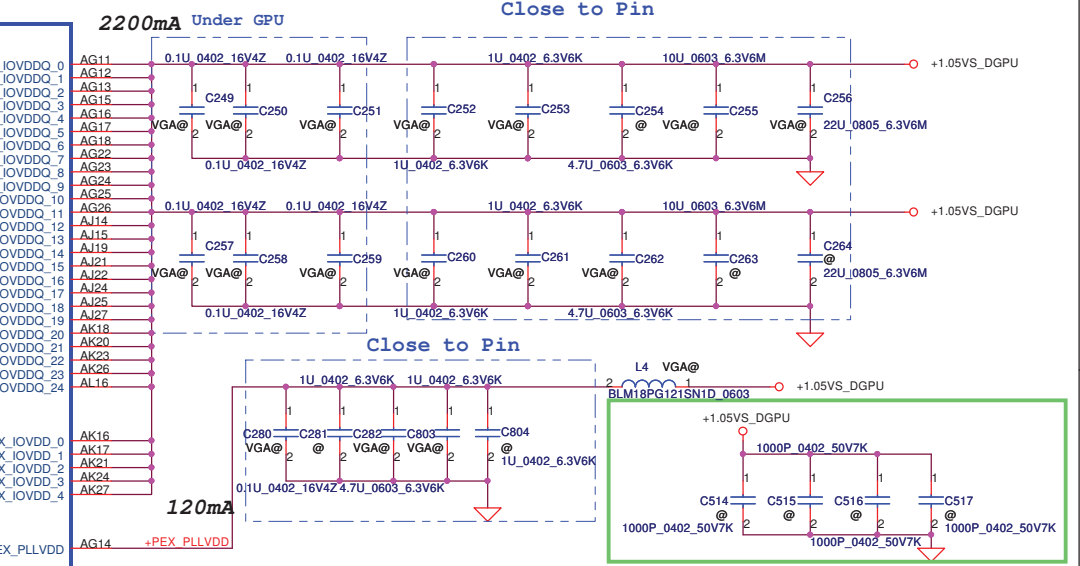
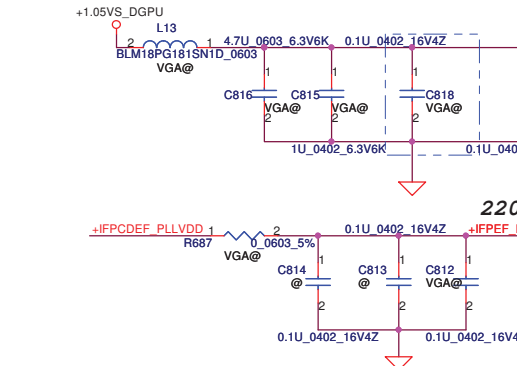
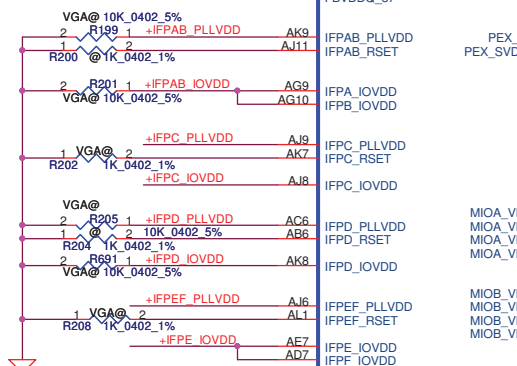
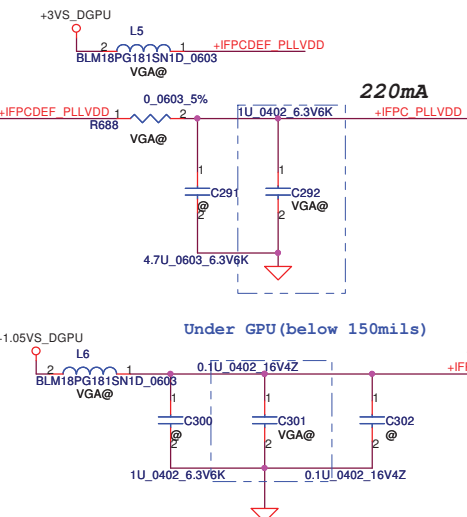
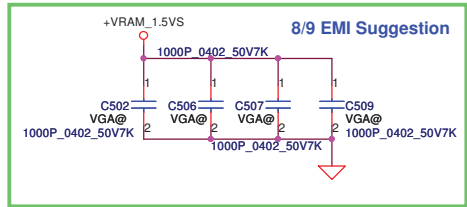
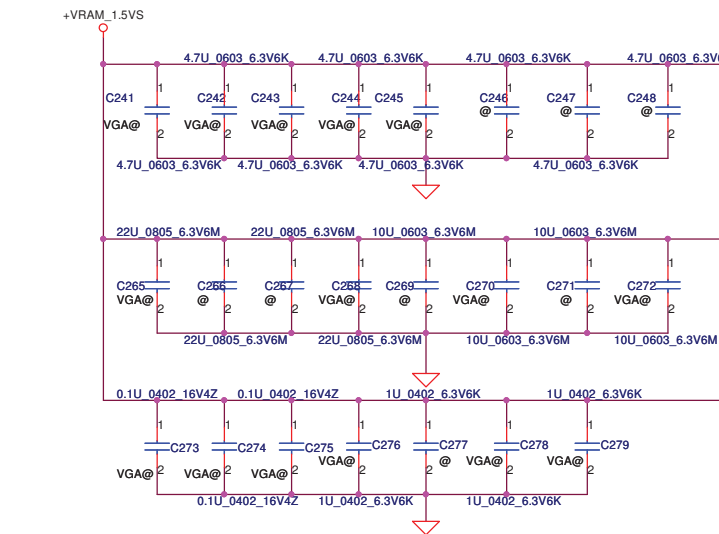
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PEG GTX C HRX N5	C190	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N5	AM23	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P6	C191	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P6	AL23	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N6	C192	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N6	AM23	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P7	C193	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P7	AM24	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N7	C194	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N7	AM25	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P8	C195	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P8	AL25	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N8	C196	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N8	AK25	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P9	C197	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P9	AL26	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N9	C198	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N9	AM26	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P10	C199	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P10	AM27	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N10	C200	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N10	AM28	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P11	C201	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P11	AL28	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N11	C202	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N11	AM29	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P12	C203	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P12	AK29	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N12	C204	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N12	AL29	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P13	C205	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P13	AM29	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N13	C206	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N13	AM30	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P14	C207	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P14	AM31	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N14	C208	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N14	AM32	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX P15	C209	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX P15	AM32	1	2	VGA@ 1U 0402 16V7K
PEG GTX C HRX N15	C210	1	2	VGA@ 1U 0402 16V7K	PEG GTX HRX N15	AP32	1	2	VGA@ 1U 0402 16V7K



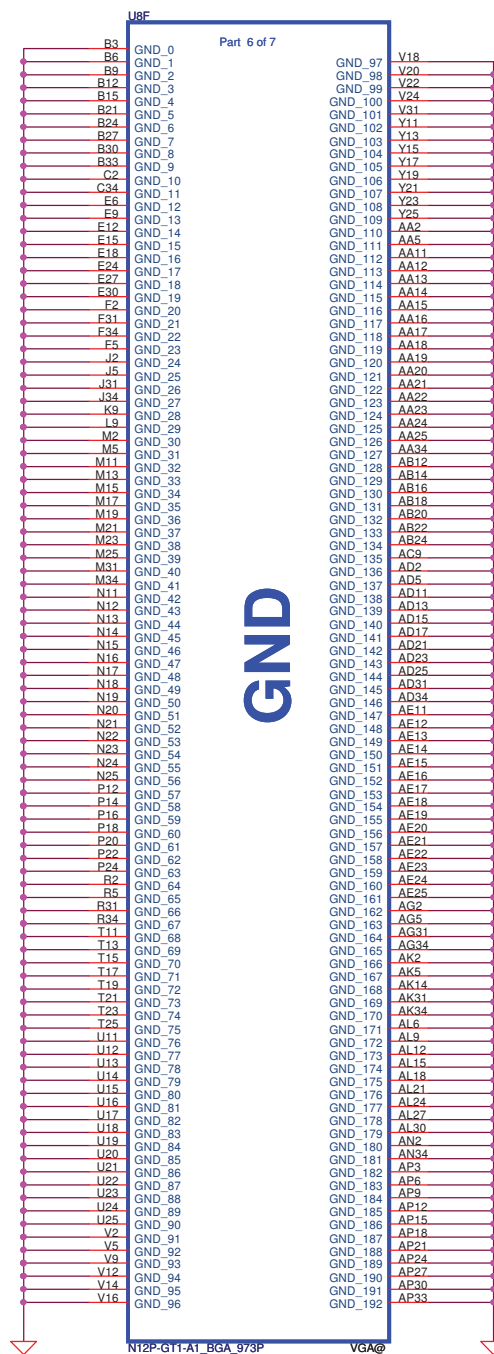
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Issued Date	2010/07/20	Deciphered Date	2011/07/20
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<div> <div> <div>Compal Electronics, Inc.</div> <div>VGA(2/12)-PCIE/DAC/GPIO</div> <div>PLA00 M/B LA-6953P Schematic</div> </div> <div> <div>Title</div> <div>Size</div> <div>Date</div> </div> <div> <div>Document Number</div> <div>Thursday, February 24, 2011</div> </div> <div> <div>Rev 1.A</div> <div>Sheet 22 of 62</div> </div> </div>			



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Size	Document Number	PLA00 M/B LA-6953P Schematic		Rev	1.A
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<30,31> MDB[0..63]

MDB0 B13
MDB1 D13
MDB2 A13
MDB3 A14
MDB4 C16
MDB5 B16
MDB6 A17
MDB7 D16
MDB8 C13
MDB9 B11
MDB10 C11
MDB11 A11
MDB12 C10
MDB13 B8
MDB14 B8
MDB15 A8
MDB16 E8
MDB17 F8
MDB18 F10
MDB19 F9
MDB20 D8
MDB21 D8
MDB22 D11
MDB23 E11
MDB24 D12
MDB25 E13
MDB26 F13
MDB27 E14
MDB28 F15
MDB29 E16
MDB30 F16
MDB31 F17
MDB32 D29
MDB33 E27
MDB34 E28
MDB35 E28
MDB36 D26
MDB37 F25
MDB38 D24
MDB39 E25
MDB40 E32
MDB41 E32
MDB42 D33
MDB43 E31
MDB44 C33
MDB45 F29
MDB46 D30
MDB47 E29
MDB48 B29
MDB49 C31
MDB50 C29
MDB51 B31
MDB52 C32
MDB53 B32
MDB54 B35
MDB55 B34
MDB56 A29
MDB57 B28
MDB58 A28
MDB59 C26
MDB60 D25
MDB61 D25
MDB62 B25
MDB63 A25

U8C

Part 3 of 7

MEMORY INTERFACE C

FBC_CMD0 E18
FBC_CMD1 E19
FBC_CMD2 G17
FBC_CMD3 E19
FBC_CMD4 C19
FBC_CMD5 C19
FBC_CMD6 B17
FBC_CMD7 E20
FBC_CMD8 B19
FBC_CMD9 D20
FBC_CMD10 A19
FBC_CMD11 D19
FBC_CMD12 C20
FBC_CMD13 F20
FBC_CMD14 B20
FBC_CMD15 G21
FBC_CMD16 F22
FBC_CMD17 F24
FBC_CMD18 E23
FBC_CMD19 C25
FBC_CMD20 C23
FBC_CMD21 E22
FBC_CMD22 D21
FBC_CMD23 F23
FBC_CMD24 A23
FBC_CMD25 D22
FBC_CMD26 B23
FBC_CMD27 C22
FBC_CMD28 B22
FBC_CMD29 A22
FBC_CMD30 A20
FBC_CMD31 G20

FBC_DOM0 A16
FBC_DOM1 D10
FBC_DOM2 D15
FBC_DOM3 D27
FBC_DOM4 D34
FBC_DOM5 A34
FBC_DOM6 D28
FBC_DOM7 D28

FBC_DQS_RN0 B14
FBC_DQS_RN1 B10
FBC_DQS_RN2 D9
FBC_DQS_RN3 E14
FBC_DQS_RN4 F26
FBC_DQS_RN5 D31
FBC_DQS_RN6 A31
FBC_DQS_RN7 A26

FBC_DQS_WP0 C14
FBC_DQS_WP1 A10
FBC_DQS_WP2 E10
FBC_DQS_WP3 D14
FBC_DQS_WP4 E26
FBC_DQS_WP5 D32
FBC_DQS_WP6 A32
FBC_DQS_WP7 B26

FBC_WCK0 G14
FBC_WCK0_N G15
FBC_WCK1 G11
FBC_WCK1_N G12
FBC_WCK2 G27
FBC_WCK2_N G28
FBC_WCK3 G24
FBC_WCK3_N G25

FBC_CLK0 E17
FBC_CLK0_N D17
FBC_CLK1 D23
FBC_CLK1_N E23

CMDB0 E18
CMDB1 E19
CMDB2 G17
CMDB3 E19
CMDB4 C19
CMDB5 C19
CMDB6 B17
CMDB7 E20
CMDB8 B19
CMDB9 D20
CMDB10 A19
CMDB11 D19
CMDB12 C20
CMDB13 F20
CMDB14 B20
CMDB15 G21
CMDB16 F22
CMDB17 F24
CMDB18 E23
CMDB19 C25
CMDB20 C23
CMDB21 E22
CMDB22 D21
CMDB23 F23
CMDB24 A23
CMDB25 D22
CMDB26 B23
CMDB27 C22
CMDB28 B22
CMDB29 A22
CMDB30 A20
CMDB31 G20

DOMB0 A16
DOMB1 D10
DOMB2 D15
DOMB3 D27
DOMB4 D34
DOMB5 A34
DOMB6 D28
DOMB7 D28

T43 @ B14
T44 @ B10
T45 @ D9
T46 @ E14
T47 @ F26
T48 @ D31
T49 @ A31
T50 @ A26

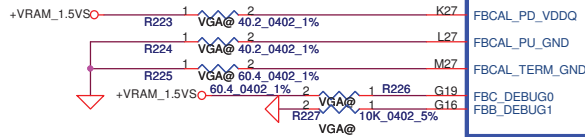
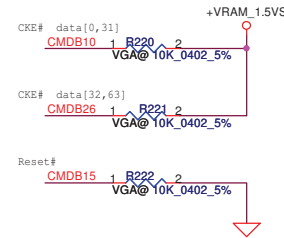
DQSB0 C14
DQSB1 A10
DQSB2 E10
DQSB3 D14
DQSB4 E26
DQSB5 D32
DQSB6 A32
DQSB7 B26

FBB_WCK01# G15
FBB_WCK01# G11
FBB_WCK23# G12
FBB_WCK23# G27
FBB_WCK45# G28
FBB_WCK45# G24
FBB_WCK67# G25

CLKB0 E17
CLKB0# D17
CLKB1 D23
CLKB1# E23

DQMB[7..0] <30,31>

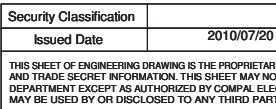
DQSB[7..0] <30,31>



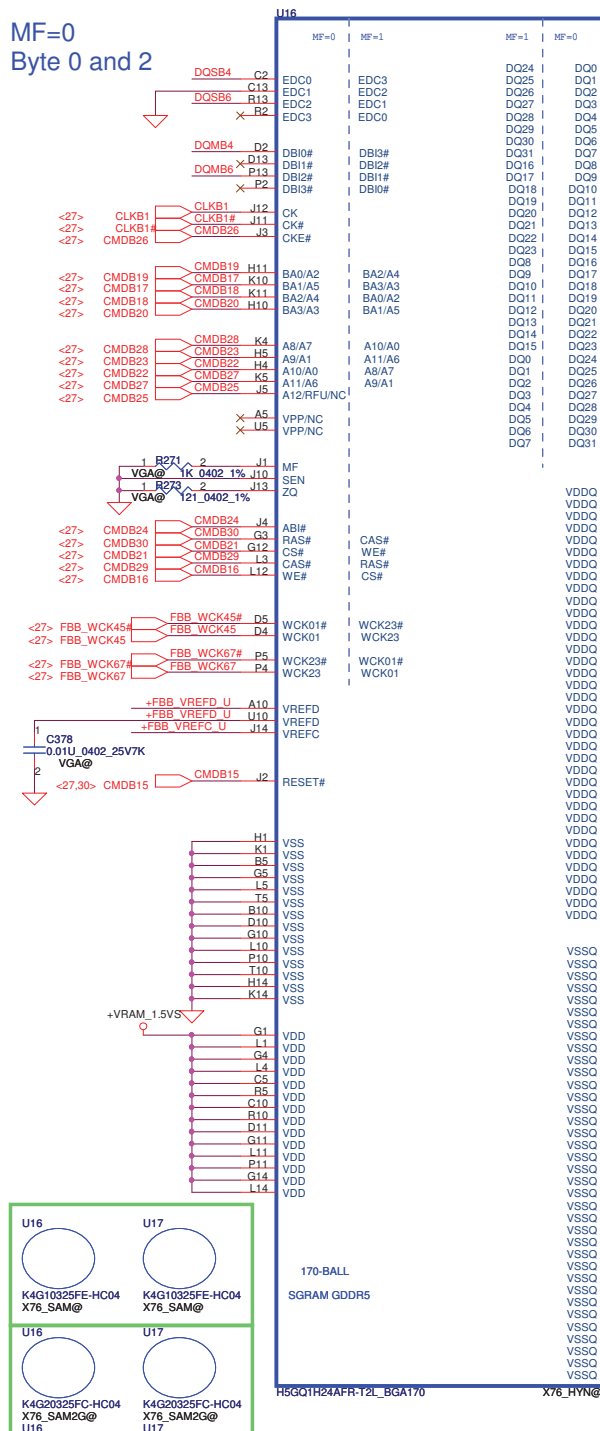
Mode G- Mapping

DATA Bus		
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

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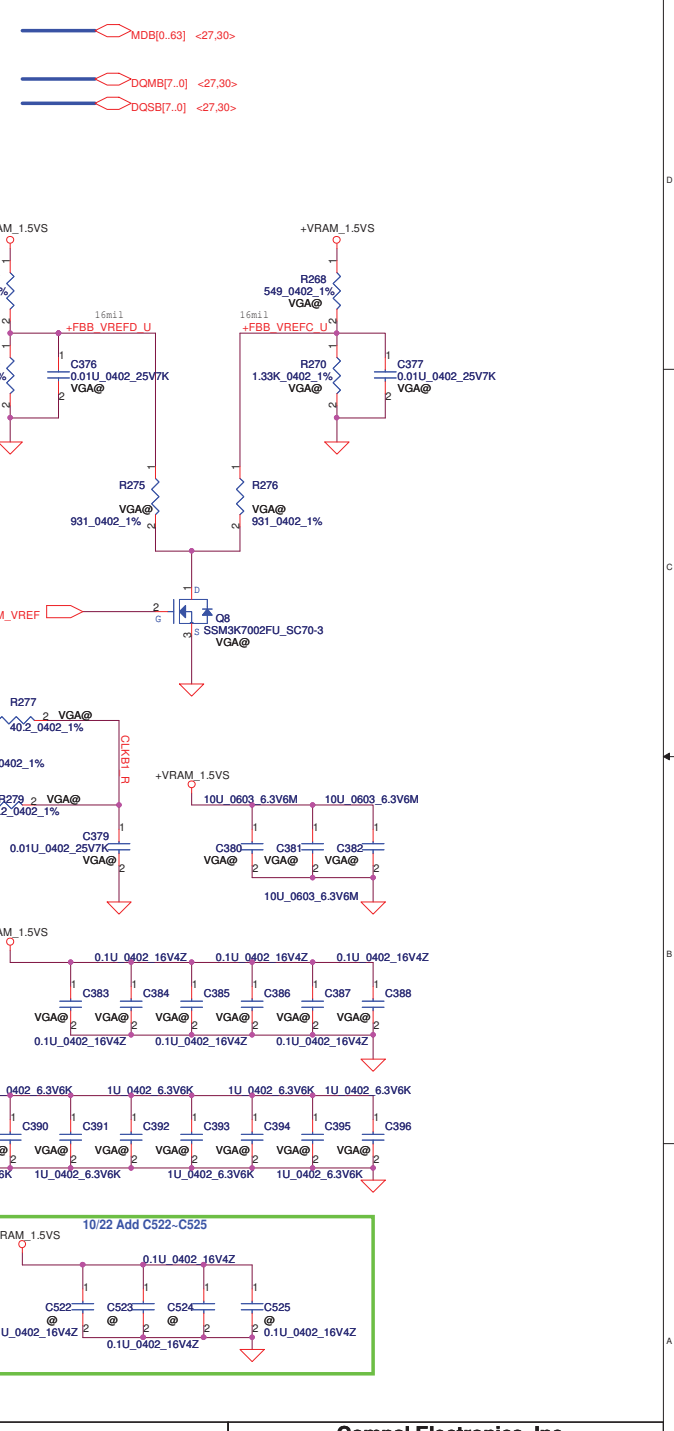
MF=0
Byte 0 and 2



MF=1
Byte 1 and 3

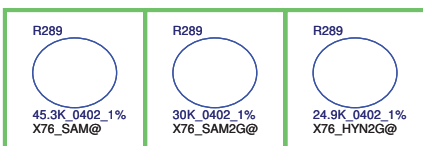
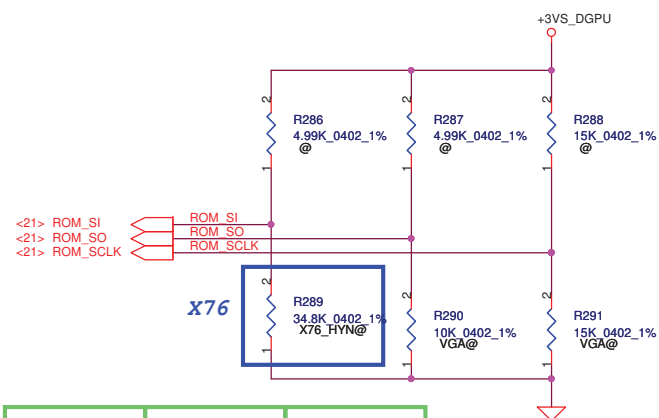
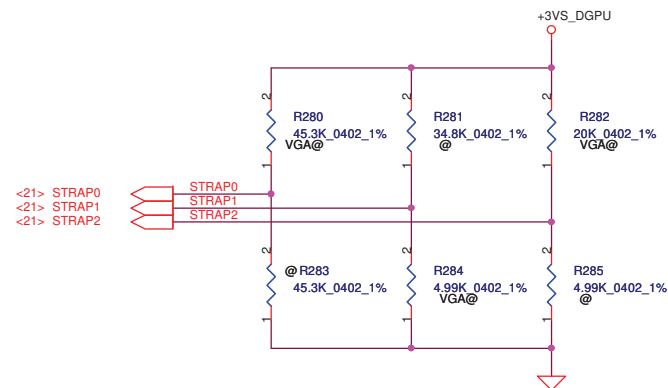


MF=0
Byte 0 and 2



WWW.AllSaler.Com

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Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0010	PD 15K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0011	PD 20K

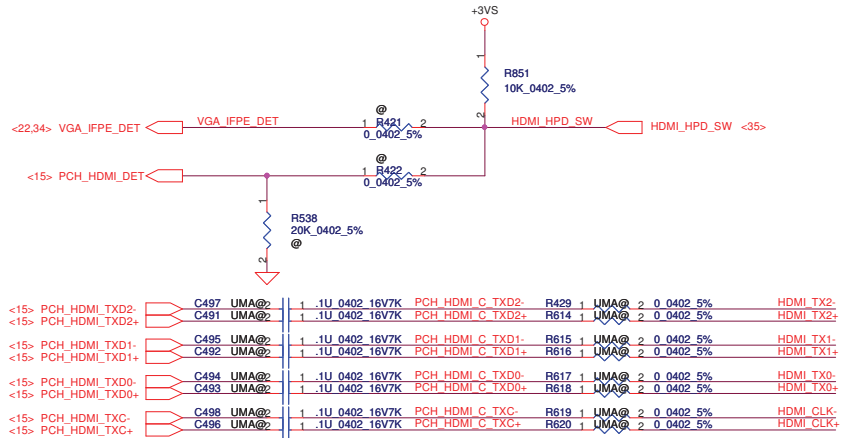
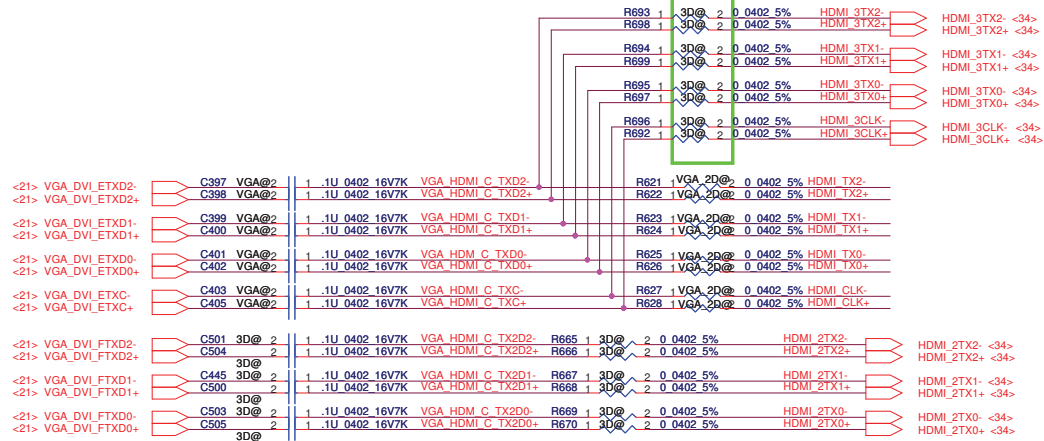
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR		XCLK_417	
0	No VBIOS ROM	0	277MHz (Default)
1	BIOS ROM is present (Default)	1	Reserved
FB_0_BAR_SIZE		USER Straps	
0	256MB (Default)	User[3:0]	
1	Reserved	1000-1100	Customer defined
3GIO_PADCFG		PEX_PLL_EN_TERM	
3GIO_PADCFG[3:0]		0	Disable (Default)
0110	Notebook Default	1	Enable
SLOT_CLK_CFG			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

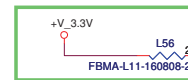
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0804 Vendor suggest close to Cap.

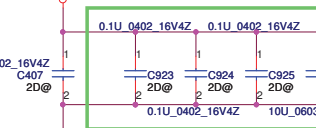


S2 (pin33)	S1 (pin32)	TMDS/DDC output
H	H	PORT1/SCL1, SDA1
H	L	PORT2/SCL2, SDA2
L	H	All disconnected

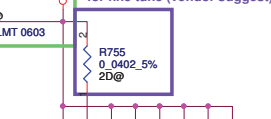
8/18 Add L56 (Vendor suggest)



8/18 Add C923-C926 (Vendor suggest)

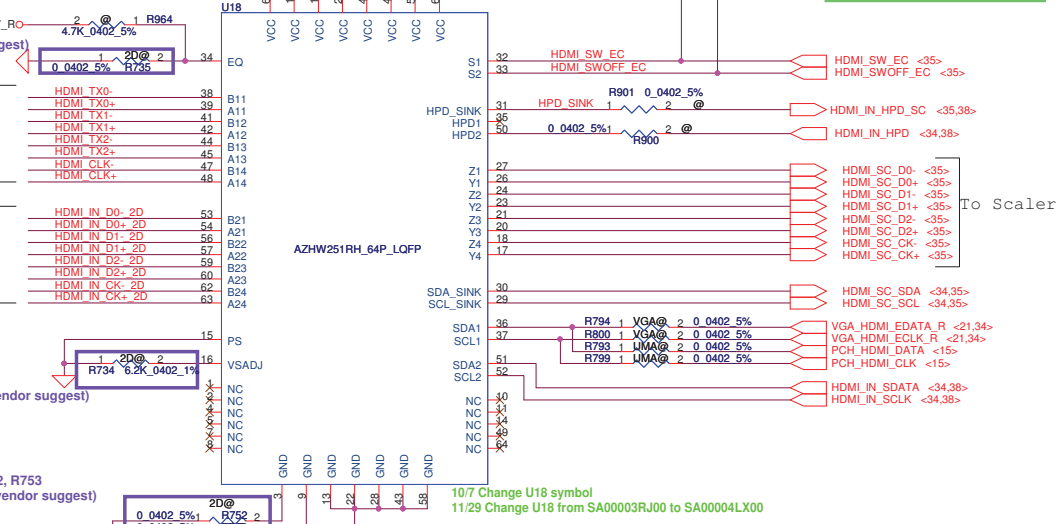


11/29 Add R755 for fine tune (vendor suggest)

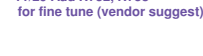


PORT 1
(PC-mode)

PORT 2
(Monitor-mode)

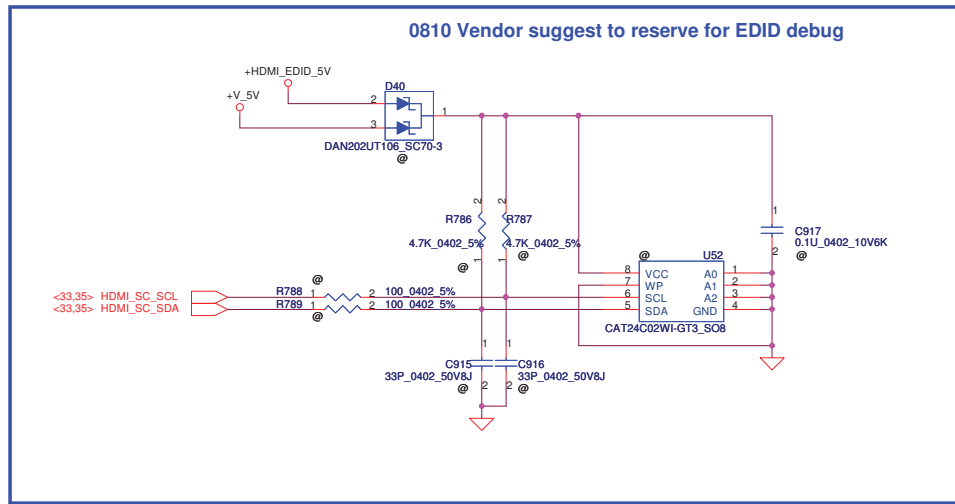


11/29 Add R752, R753 for fine tune (vendor suggest)

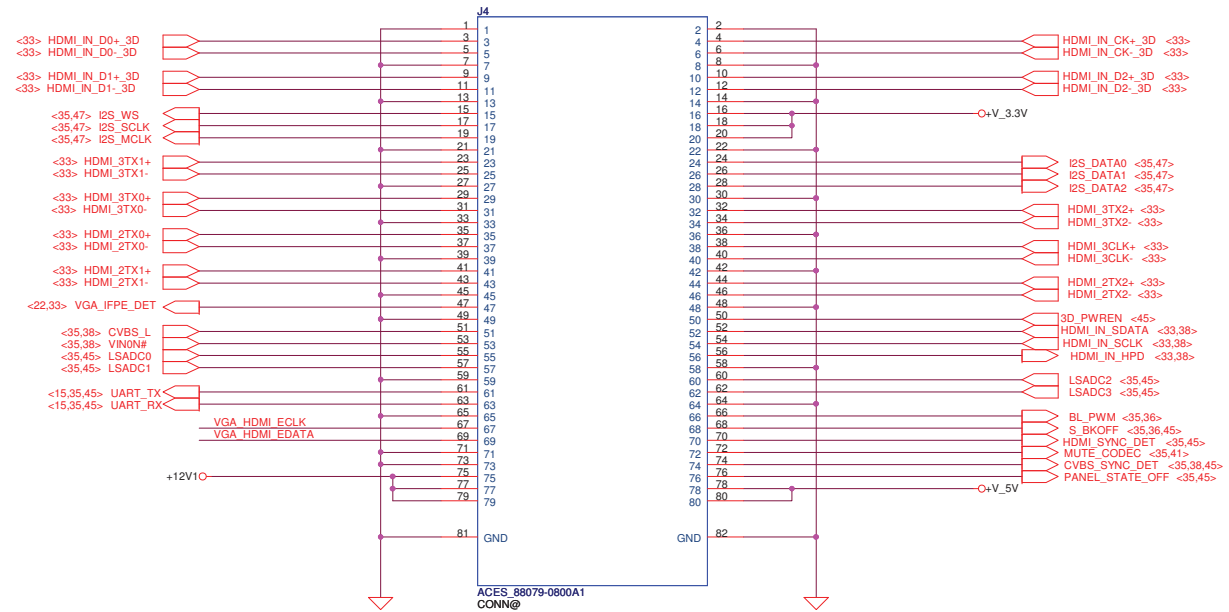


10/7 Change U18 symbol
11/29 Change U18 from SA00003RJ00 to SA00004LX00

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2011/07/20		
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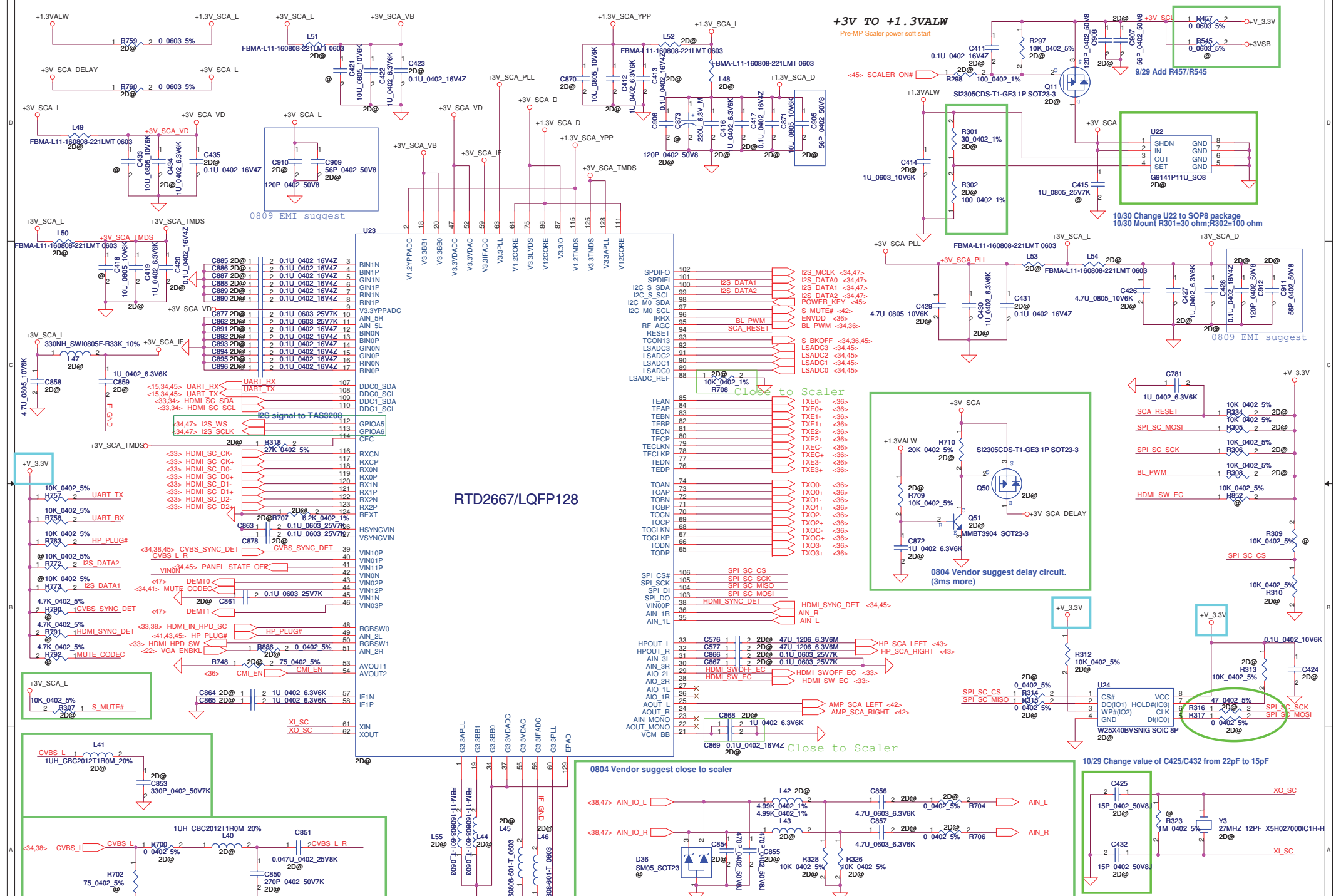
12/11 3D Scaler Pin define update



12/6 Change symbol of J4 from LTCX002TM00 to SP010011B00(60pin to 80pin)

<21,33> VGA_HDMI_ECLK_R R939 1 3D 2 0 0402 5% VGA_HDMI_ECLK
 <21,33> VGA_HDMI_EDATA_R R940 1 3D 2 0 0402 5% VGA_HDMI_EDATA

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				Size	Document Number	Rev
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Custpm		PLA00 M/B LA-6951P Schematic	
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5/18 Change R332 from 100K to 10K ohm

135mA

+3VS

R332
10K 0402 5%

0.1uF 0402 16V

R331
0.0402 5%

40 mils

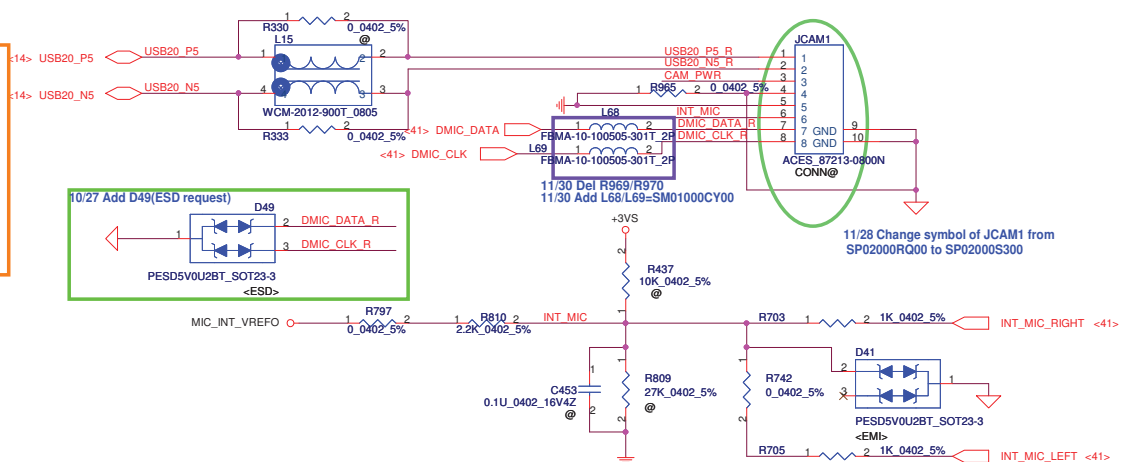
C444
10uF 0603 6.3V6M

CAM_PWR

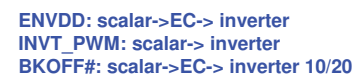
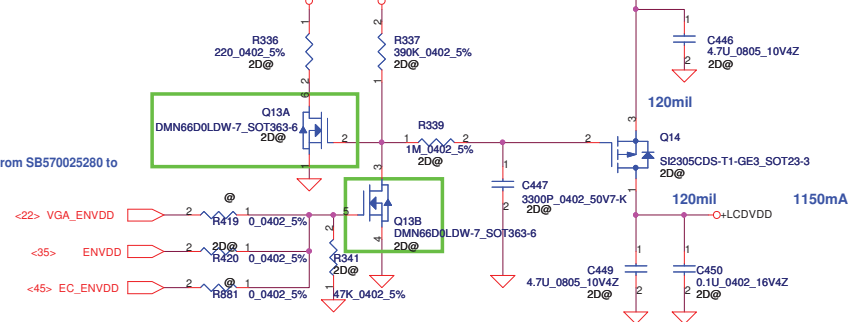
R335
10K 0402 5%

<12> CAM_OFF

<45> EC_CAM_OFF



Pinout diagram for the ACES_87242-3001-09 connector. The diagram shows two rows of pins. The top row (pins 1-32) is labeled 'JLVDS1' and includes TX00- (<35V), TX01- (<35V), TX02- (<35V), TX03+ (<35V), TX04- (<35V), TX05+ (<35V), TXE1- (<35V), TXE2+ (<35V), TXE3- (<35V), TXE4+ (<35V), TXE5+ (<35V), and LCDVDD. The bottom row (pins 31-32) is labeled 'GND GND' and 'CONN@'. The diagram also shows a power supply symbol and a ground symbol.

[illegible]

Touch Panel

PVT change from alw to vs for EUP.

100mA

+5V

USB20_P4_R

USB20_N4_R

@D11

VIN IO1

IO2 GND

PRT85V0U2X_SOT143-4

C458 0.1U_0402_16V4Z

C459 1U_0603_10V6K

@ 1 2

1 2

1 2

3 4

5 6

7 GND

JTOUCH

USB20_N4

USB20_P4

0 0402 5% 1

2 R345

0 0402 5% 1

2 R346

USB20_N4_R

USB20_P4_R

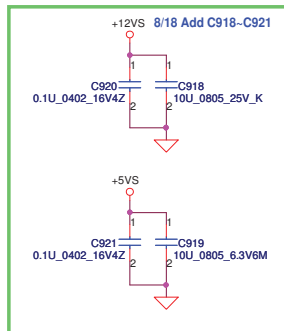
Shield GND

ACES_87213-0500G_5F

CONN

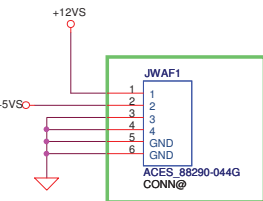
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title LCD CONN. / WebCam			
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				Custom	PLA00 M/B LA-6951P Schematic ^A		
				Date:	Thursday, February 24, 2011	Sheet	36 of 62

HDD POWER Conn



Layout Note: Place C918/C919/C920/C921 close to JWAFER1

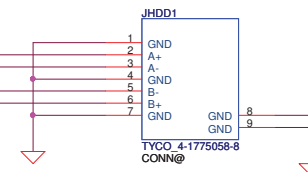
HDD



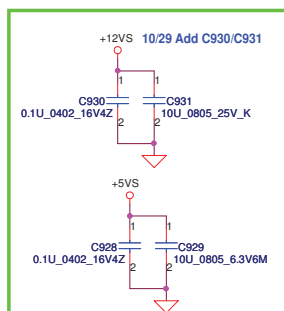
12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00



SATA HDD Conn.

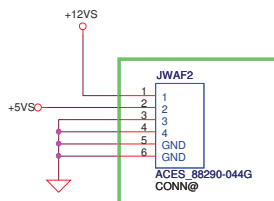


ODD POWER Conn



10/28 Add C928/C929

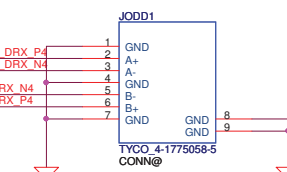
Layout Note: Place C928/C929 close to JWAFER2



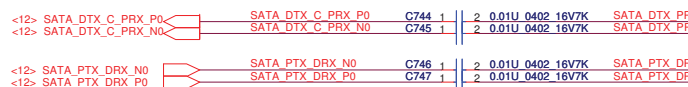
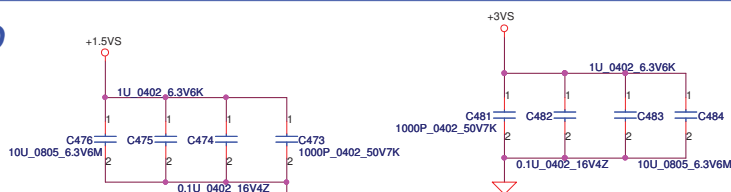
12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00



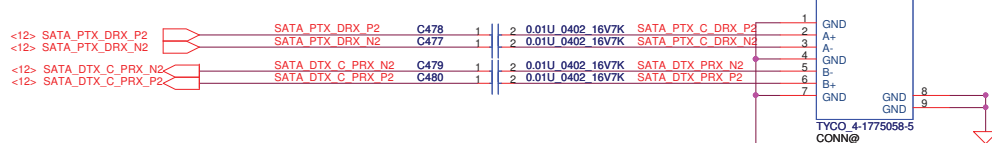
SATA ODD Conn.



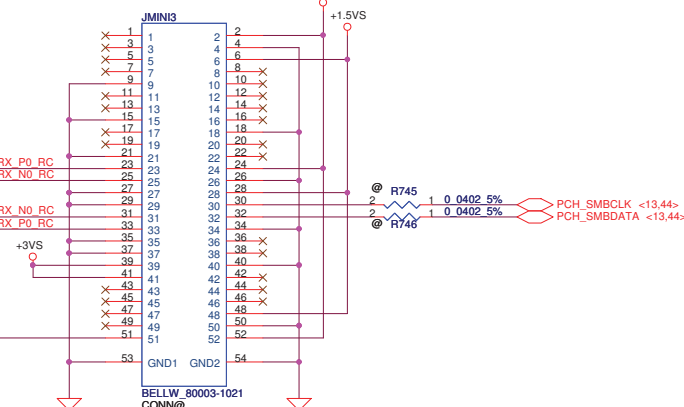
SSD



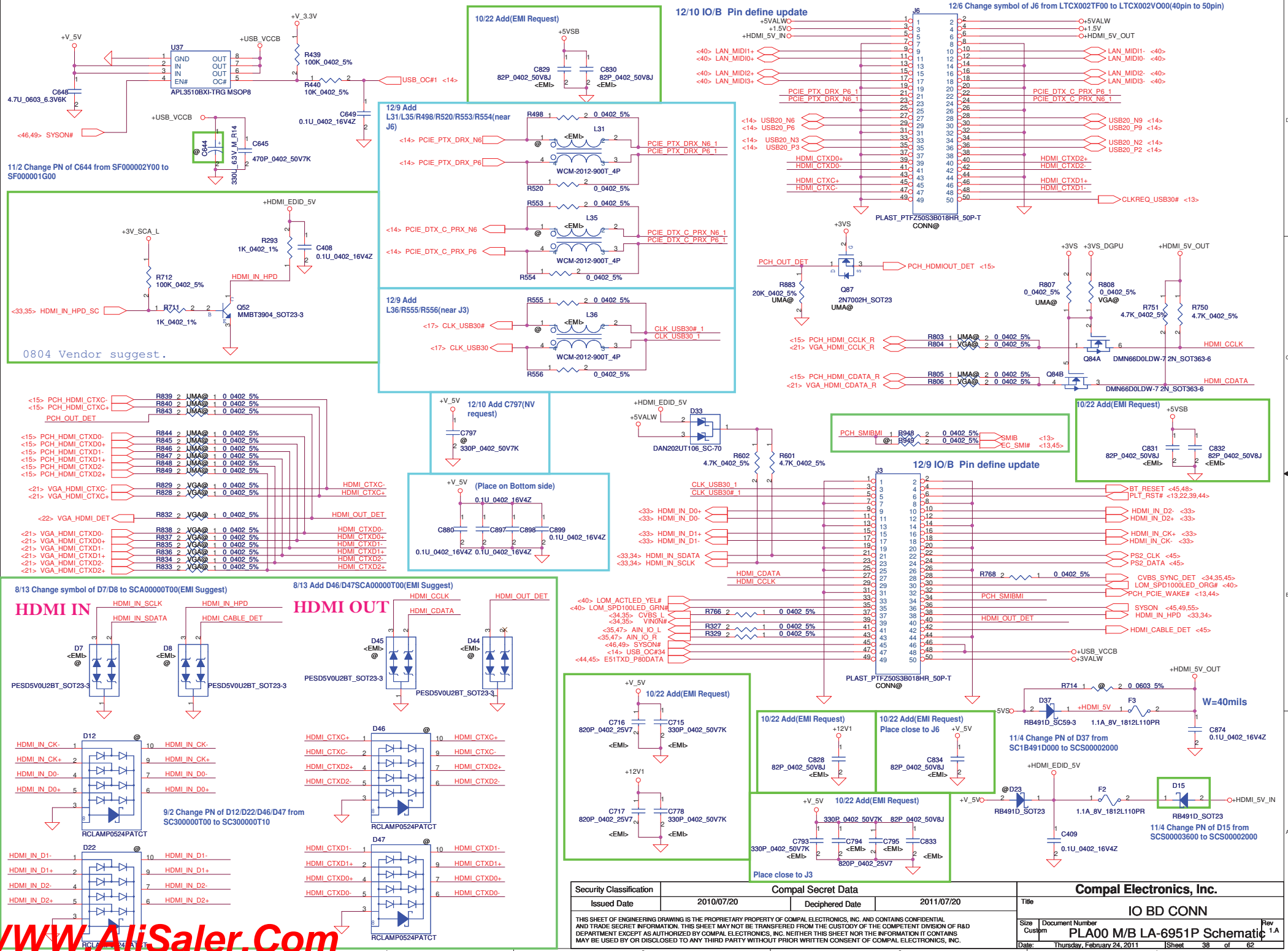
SATA SSD Conn.



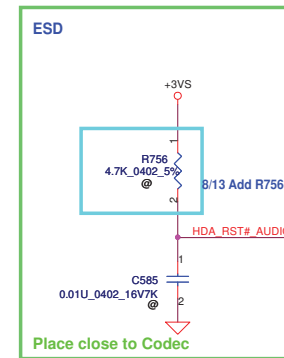
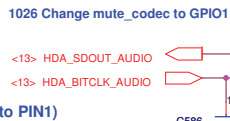
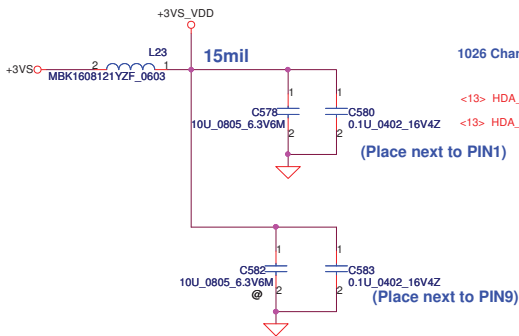
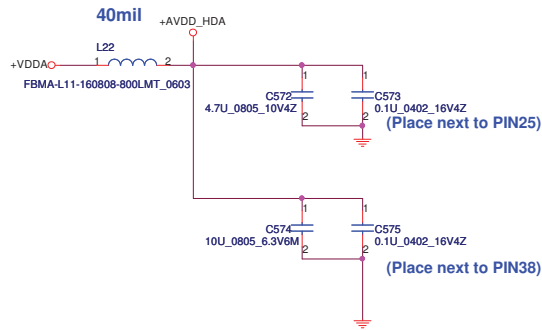
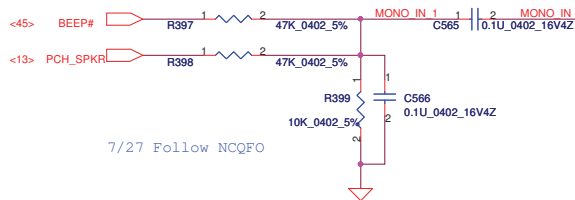
MINI SSD Conn.



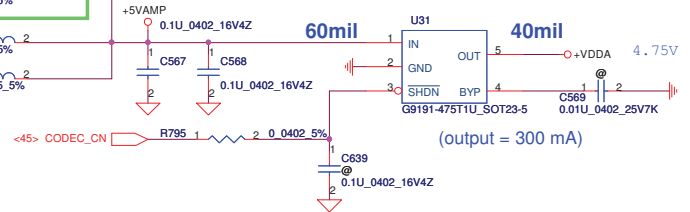
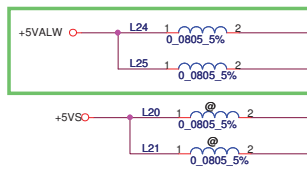
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size B	Document Number	PLA00 M/B LA-6951P Schematic		Rev	1.A
Date:	Thursday, February 24, 2011	Sheet	37	of	62



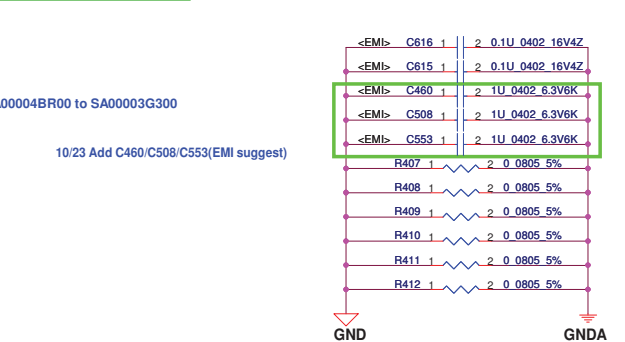
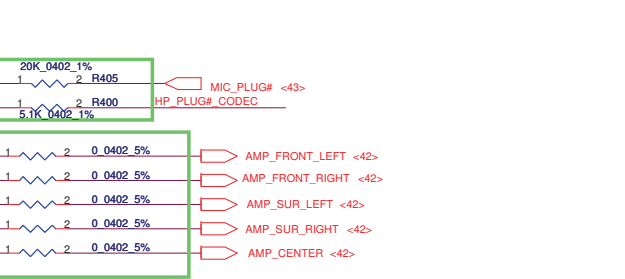
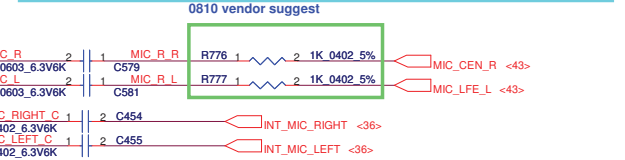
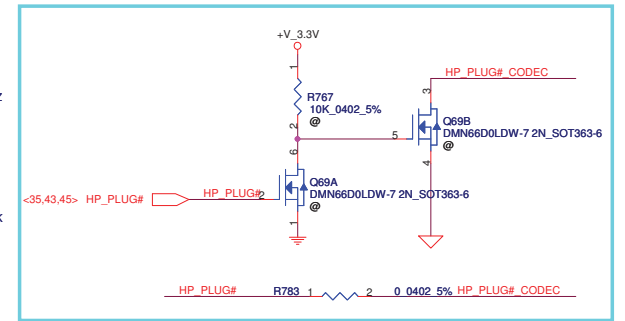
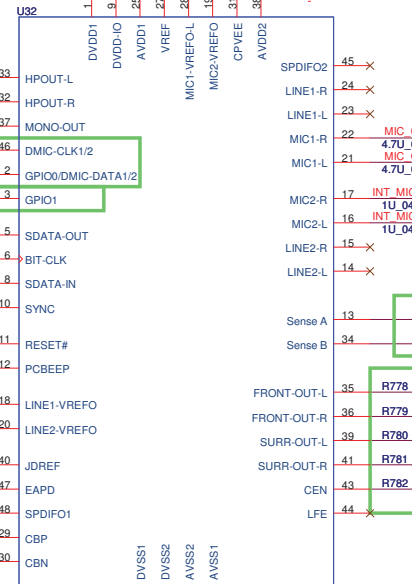
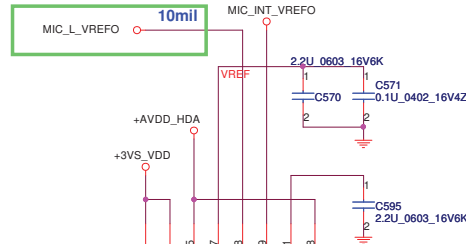
Security Classification		Compal Secret Data	
Issued Date	2010/07/20	Deciphered Date	2011/07/20
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Title		Compal Electronics, Inc.	
Size		IO BD CONN	
Document Number		PLA00 M/B LA-6951P Schematic	
Date		Thursday, February 24, 2011	
Sheet		38 of 62	



0105 Add L24/L25

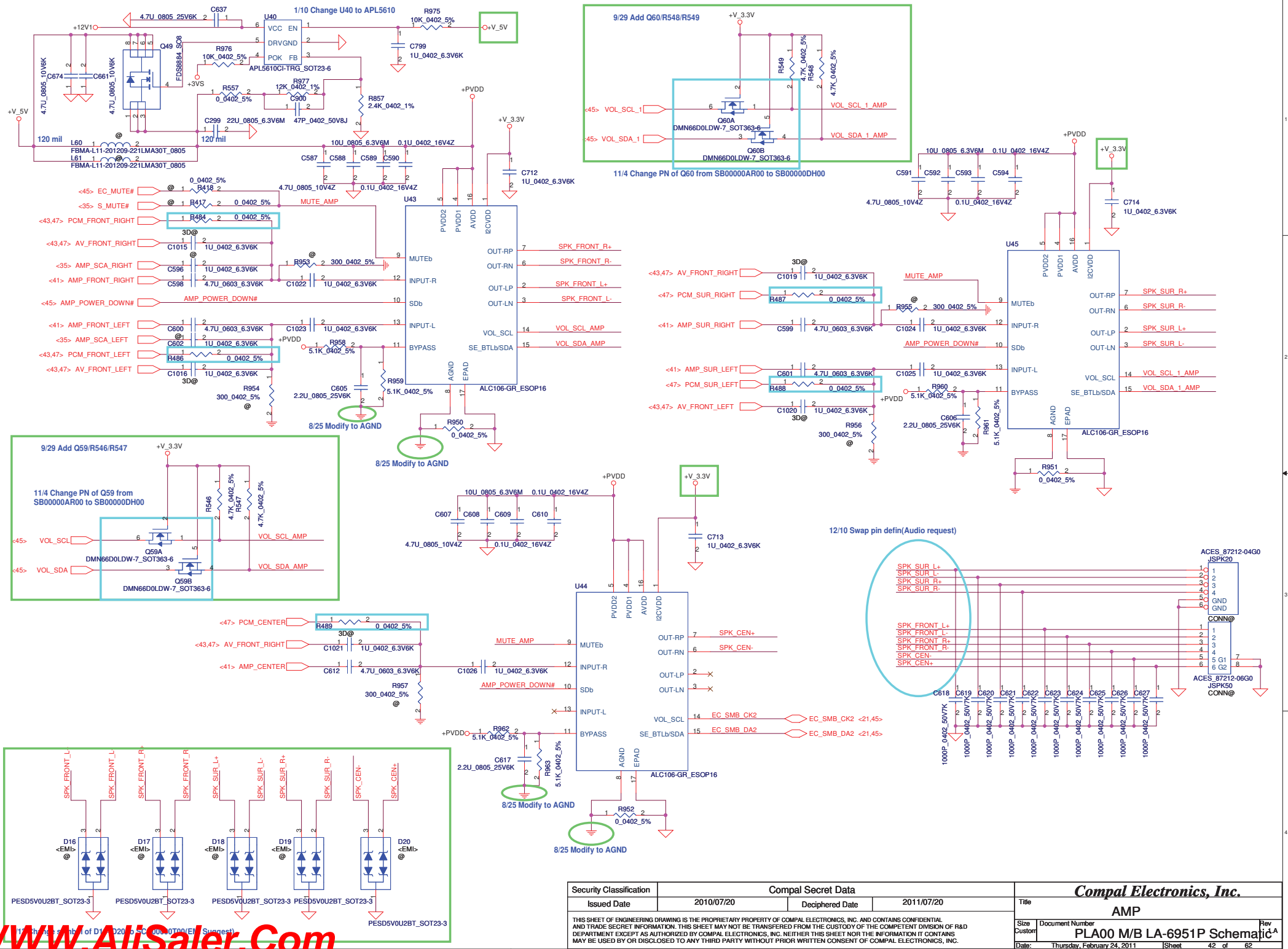


1026 DEL MIC_R_VREF0

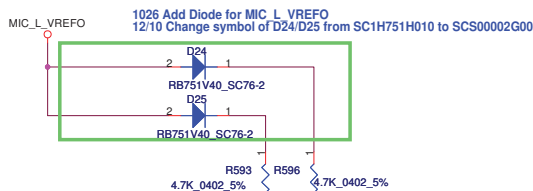


Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

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Size B	Document Number	PLA00 M/B LA-6951P Schematic		Rev 1.A	
Date	Thursday, February 24, 2011	Sheet	41	of 62	

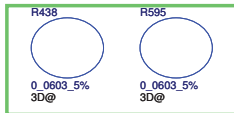


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Issued Date	2010/07/20	Deciphered Date	2011/07/20	AMP	
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				Date	Thursday, February 24, 2011
				Sheet	42 of 62

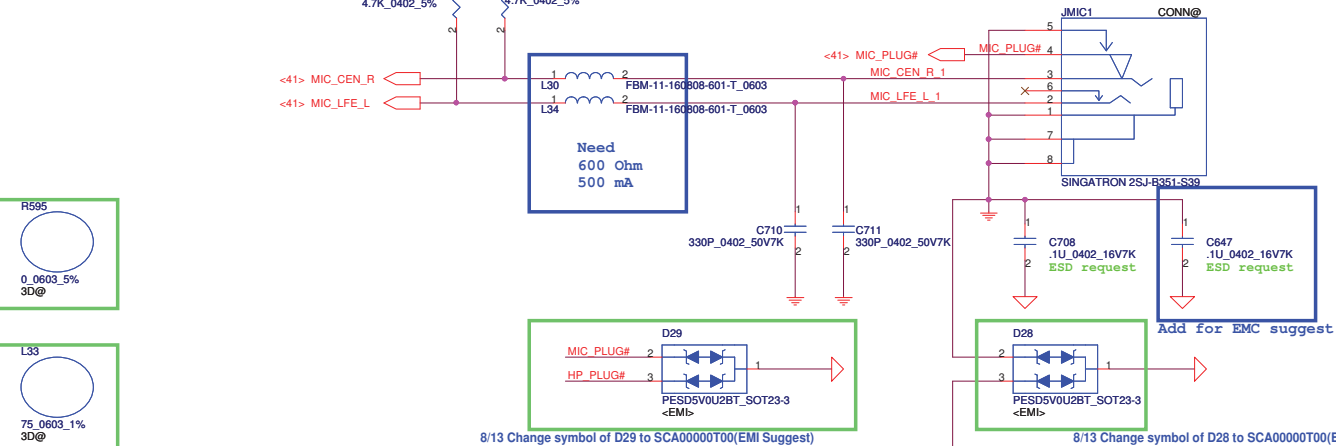
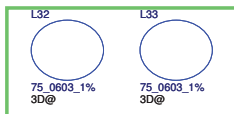


EXT MIC IN

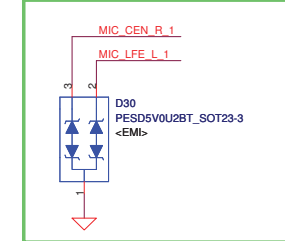
2/18 Add



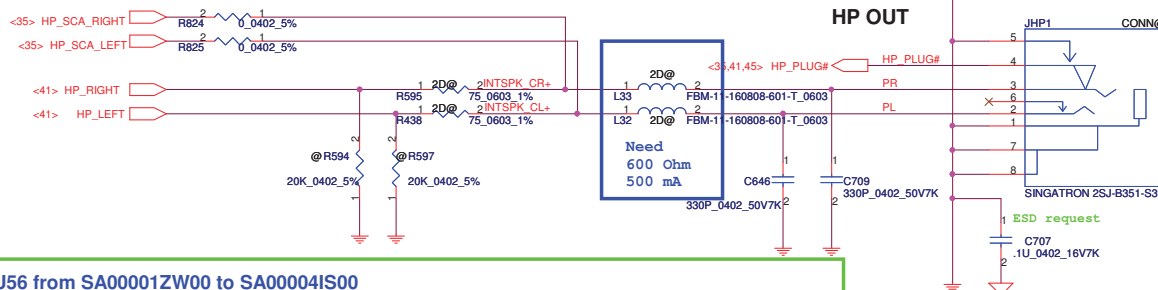
2/24 Add



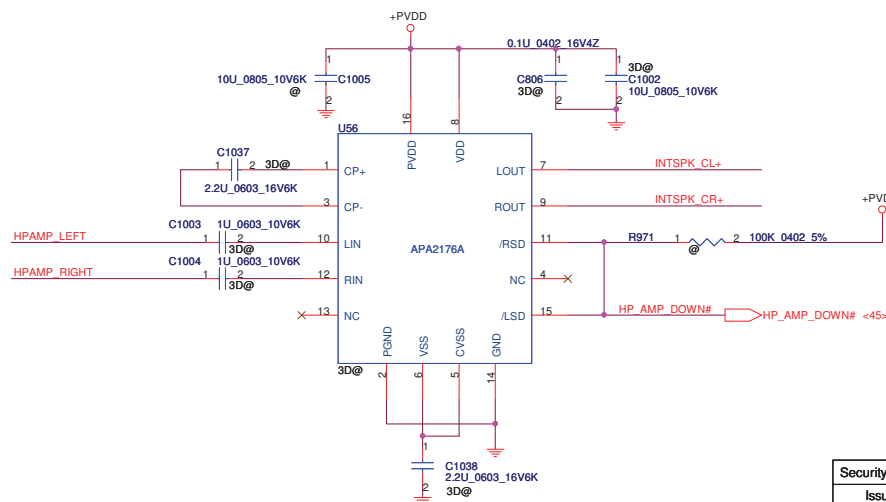
8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)



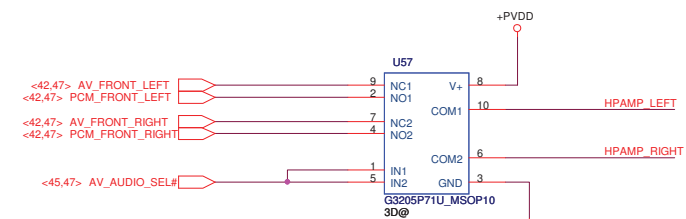
HP OUT



10/22 Change U56 from SA00001ZW00 to SA00004IS00



12/09 Add U57

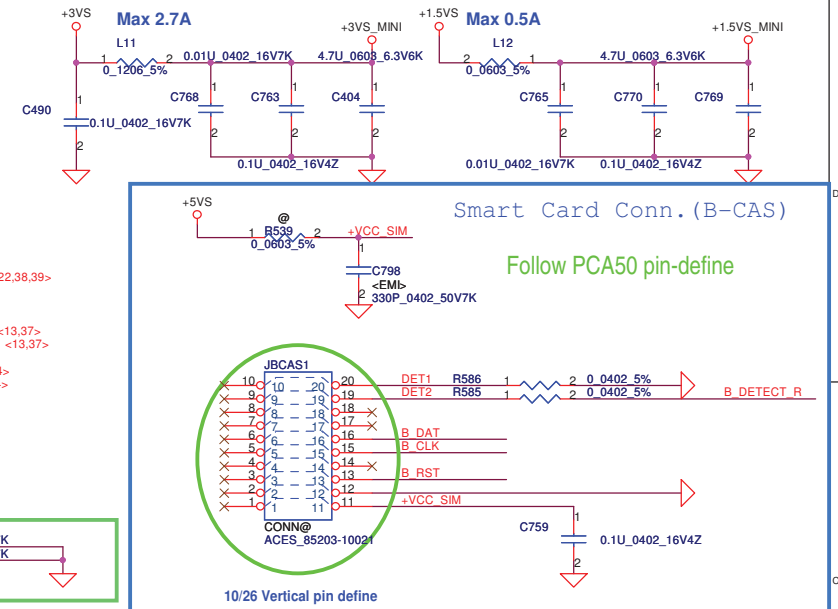
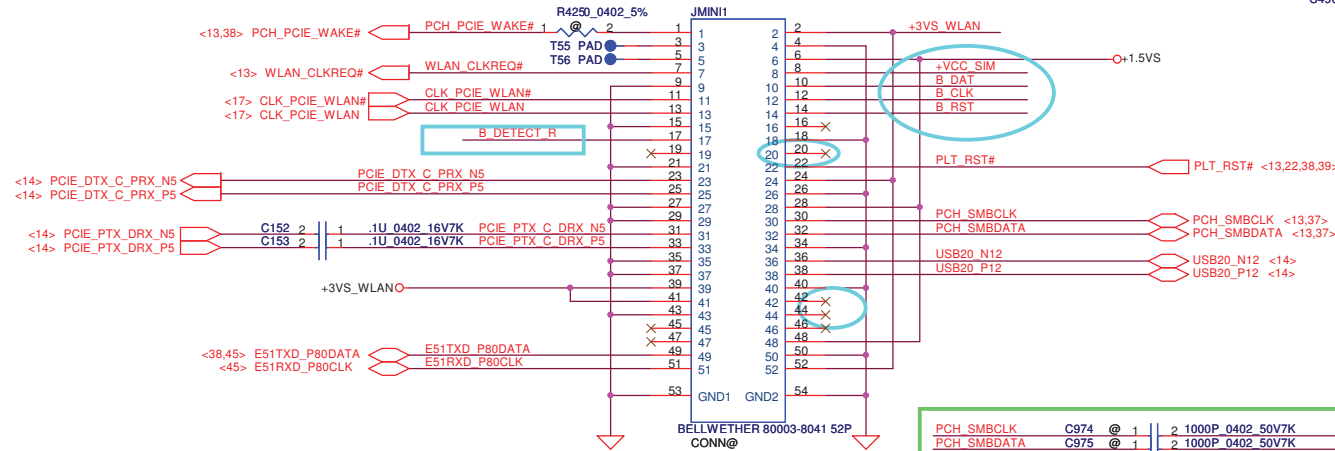


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Size	Document Number	Customer	Rev	PLA00 M/B LA-6951P Schematic	
Date:	Thursday, February 24, 2011	Sheet	43 of 62	1.A	

MINI (TV)

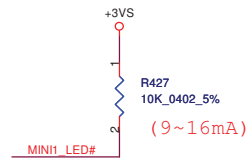
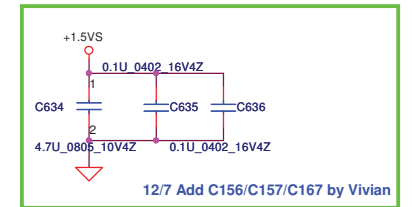
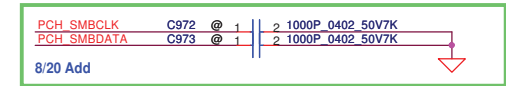
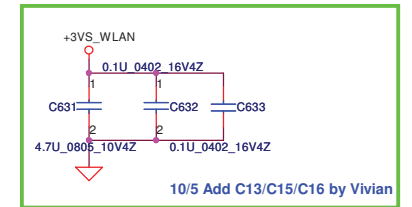
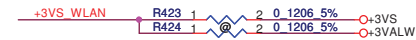
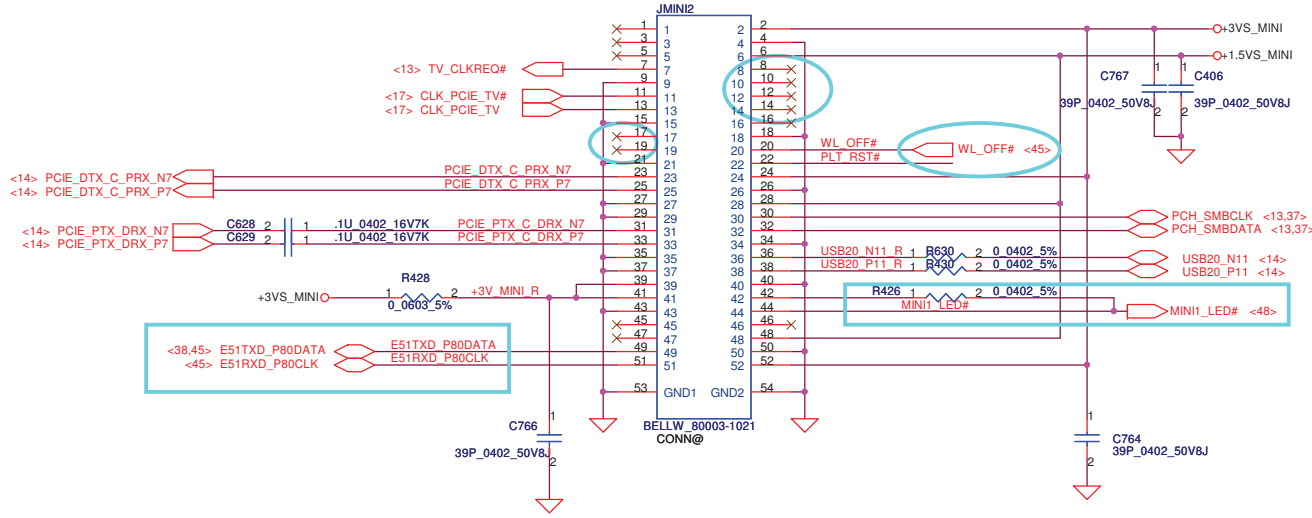
Mini Card Slot 1---TV tuner Currecnt: 3.3 : 2750mA, 1.5: 500mA

H=9mm



WLAN

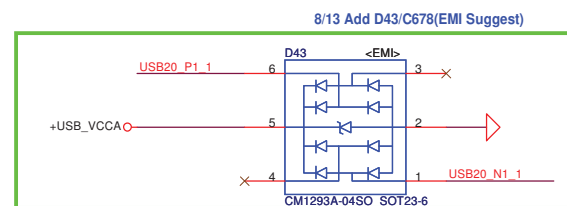
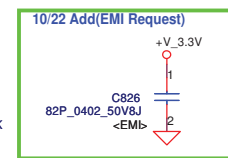
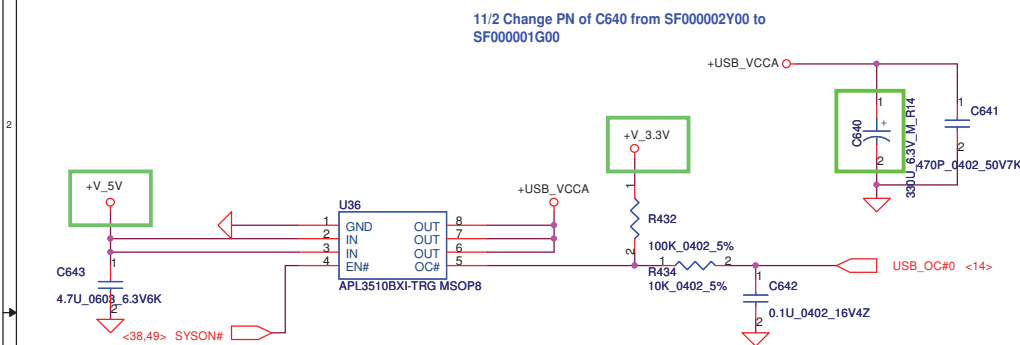
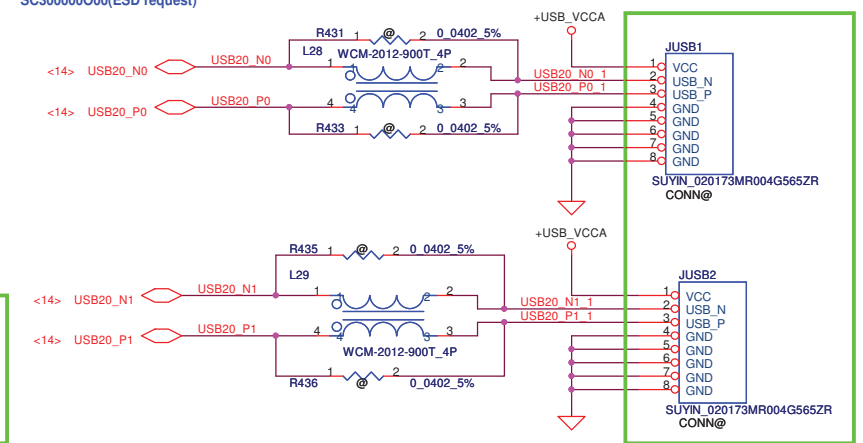
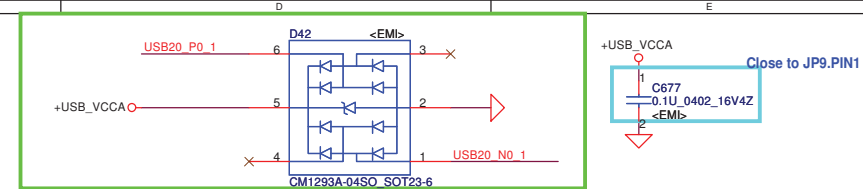
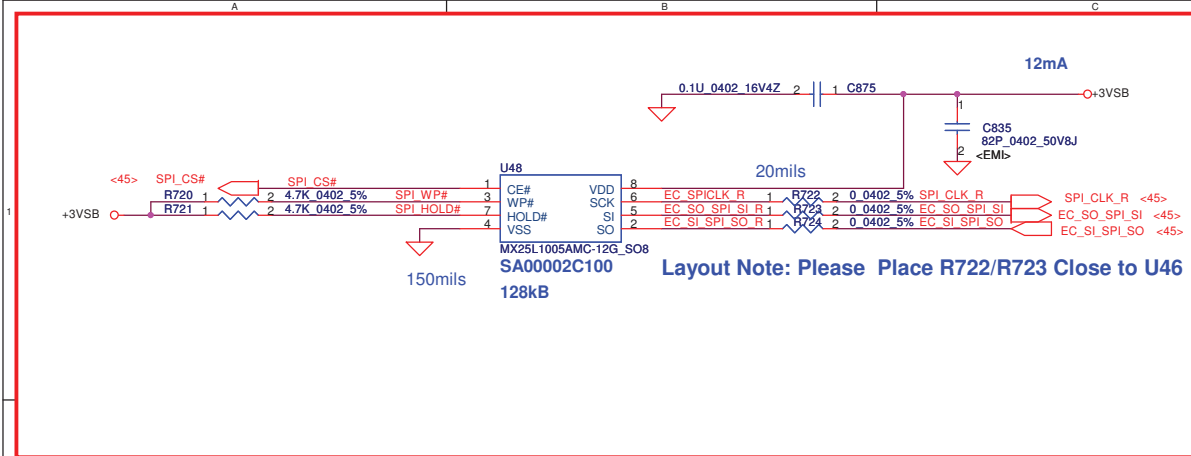
H=4mm



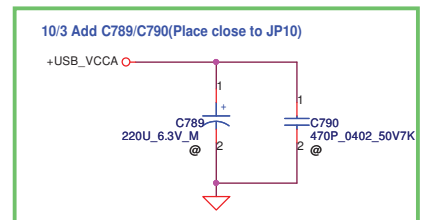
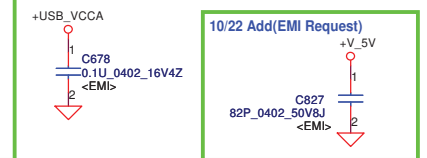
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size Custom	Document Number	PLA00 M/B LA-6951P Schematic		Rev 1.A	
Date:	Thursday, February 24, 2011	Sheet	44 of 62		



Security Classification	Compal Secret Data			Compal Electronics, Inc. Title EC KB930/KB conn		
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Size	Document Number	Rev
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				Date:	Thursday, February 24, 2011	Sheet 45 of 62

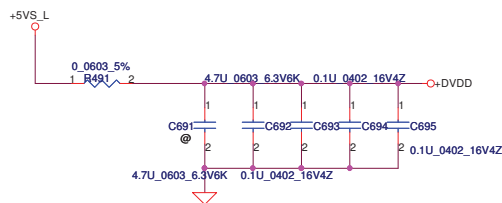
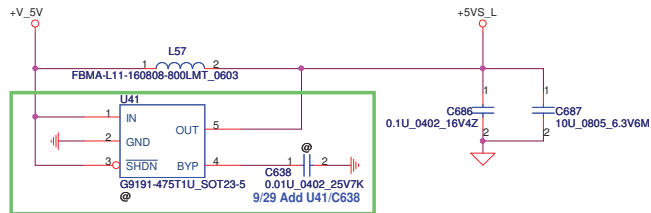


10/25 Change symbol and footprint of D43 from SC300000100 to SC300000000(ESD request)

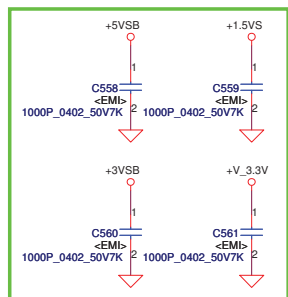


USB Conn. (SIDE)

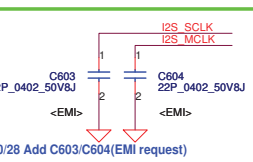
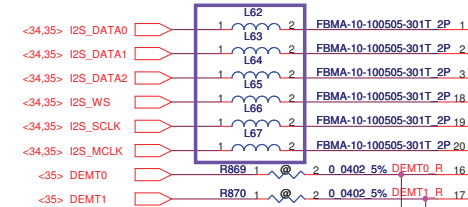
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title	
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Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic	Rev	1.A
Date:	Thursday, February 24, 2011	Sheet	46	of	62



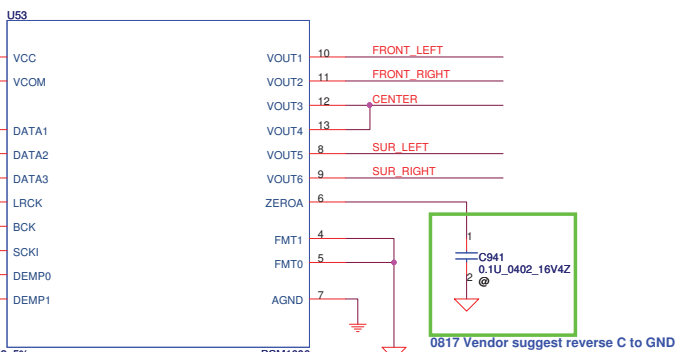
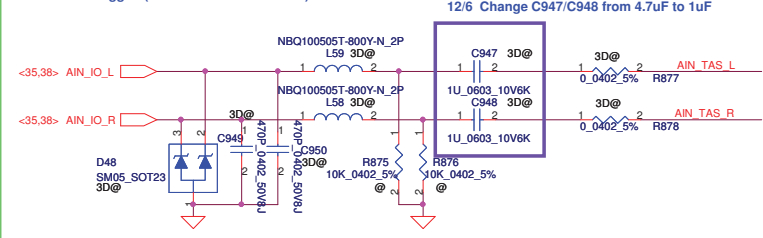
10/27 Add C558-C561(EMI request)



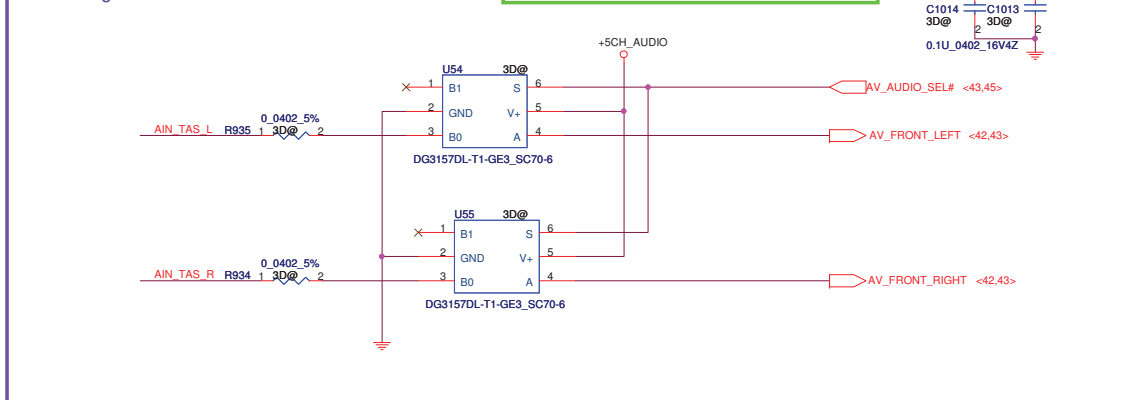
11/30 Del R858-R863
11/30 Add L62-L67=SM01000CY00



0818 Vendor suggest(Close to U42.Pin43/44)



8/23 Add TS5A23157 (SA000017M00)
11/29 Change SA000017M00 to SA000039D00 *2

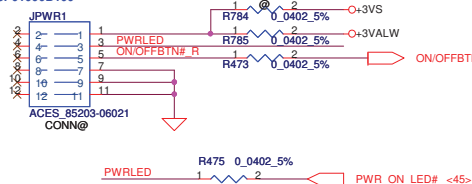


De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

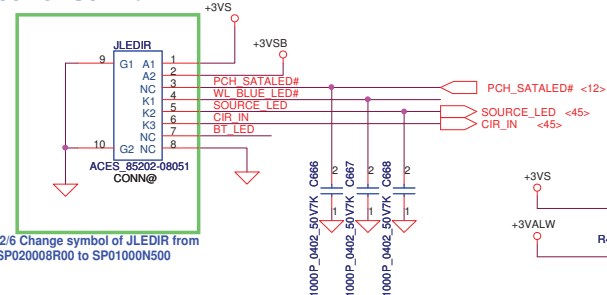
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Power switch board

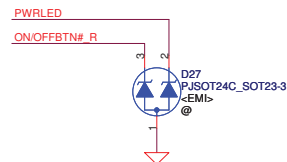
12/6 Change symbol of JPWR1 from SP02000U100 to SP01000B100



LED board conn.

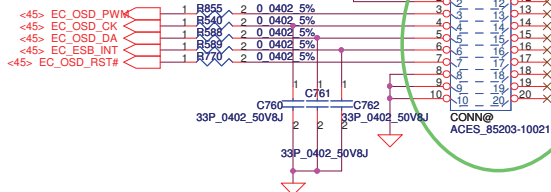


8/13 Change symbol of D27 to SCA0000E00(EMI Suggest)

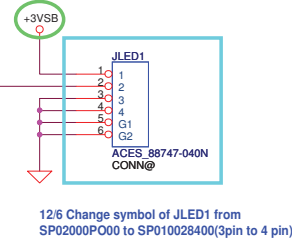


SENSOR BOTTOM

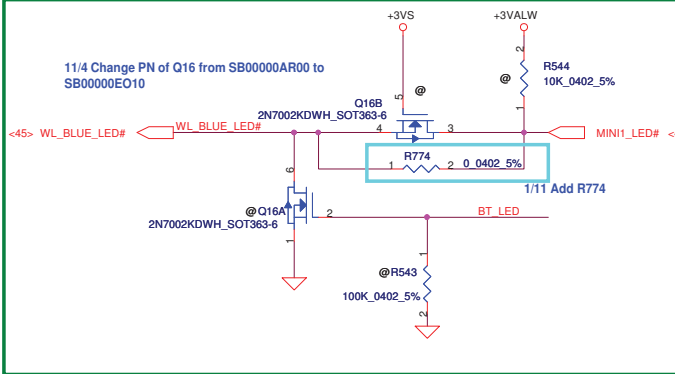
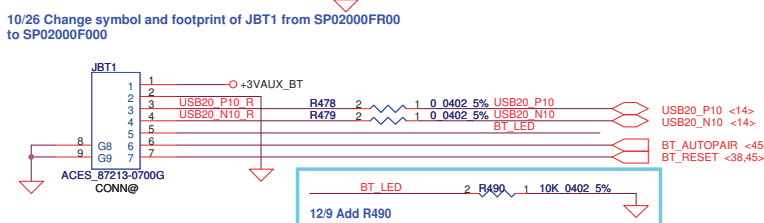
Follow NCQD0



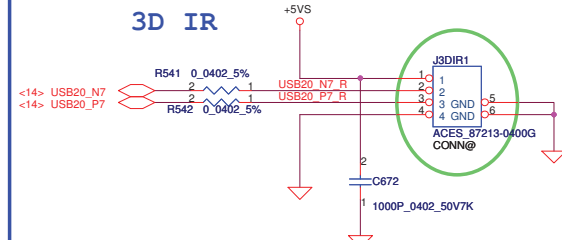
DECO LED board conn.



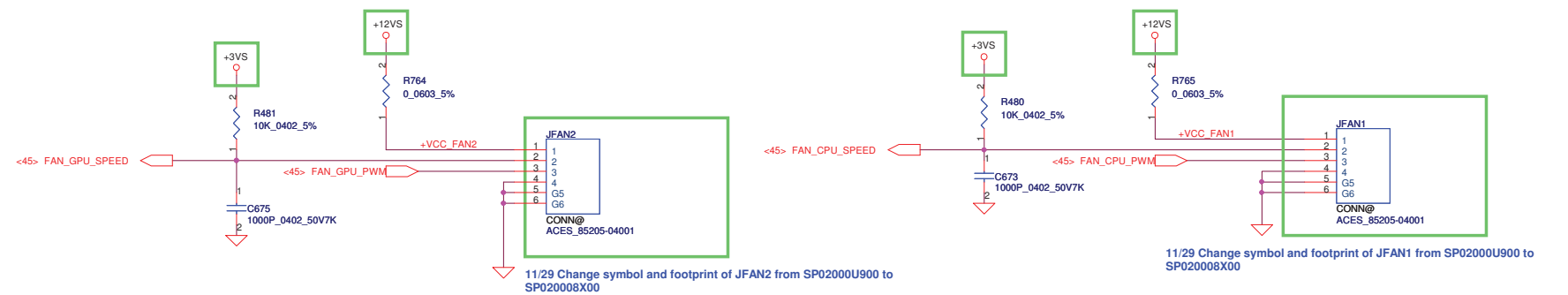
BT Connector



3D IR

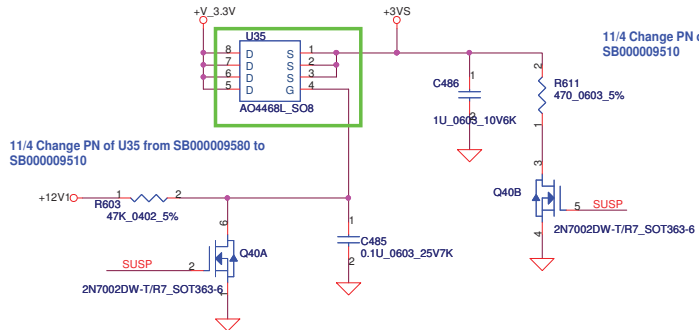


Fan Control circuit

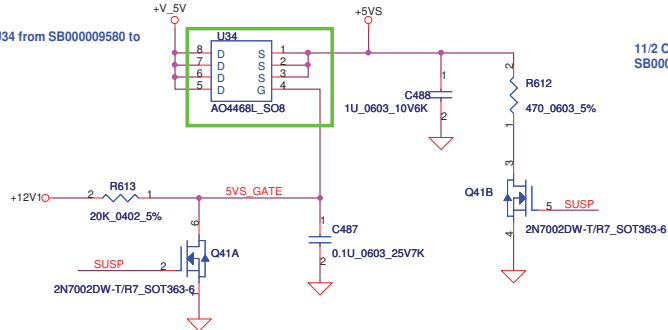


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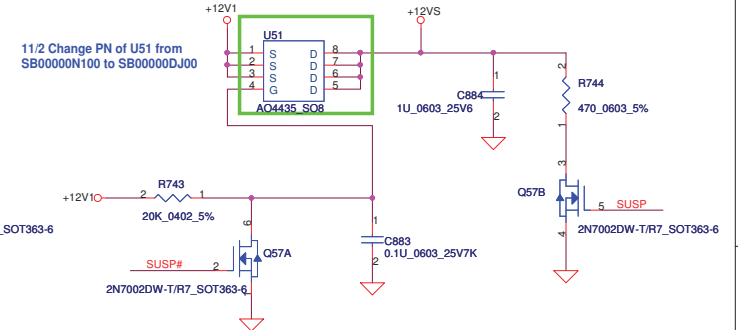
+V_3.3V TO +3VS



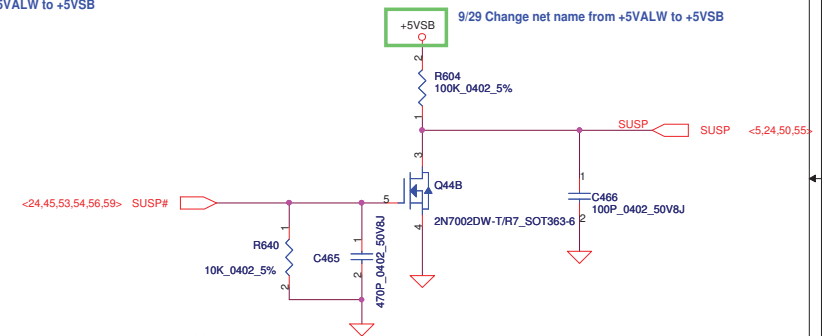
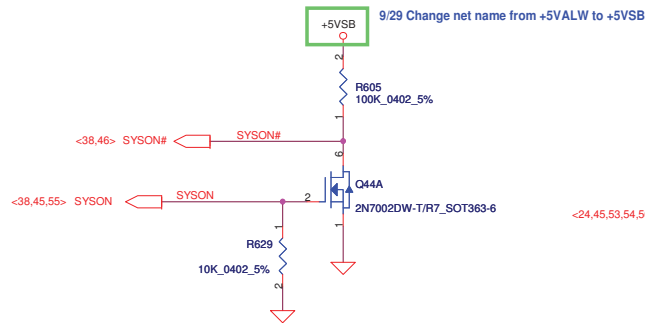
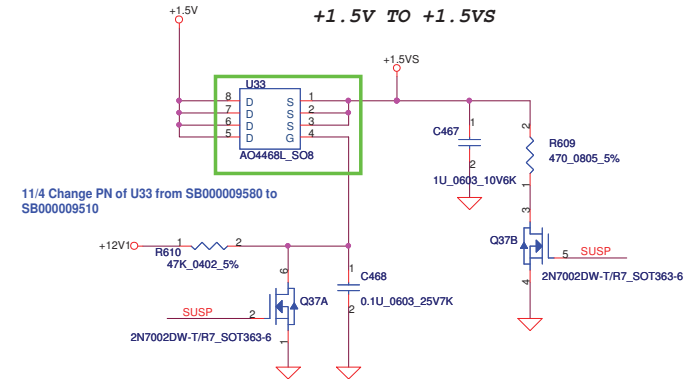
+V_5V TO +5VS



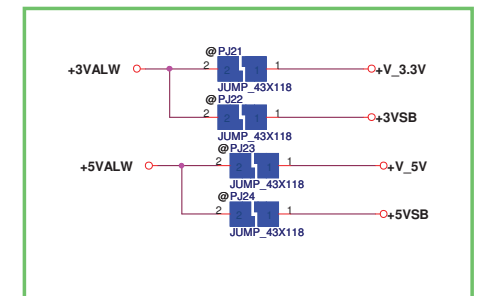
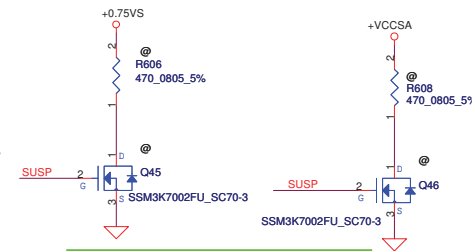
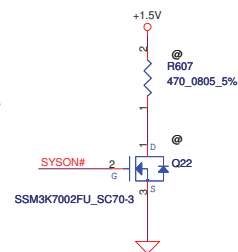
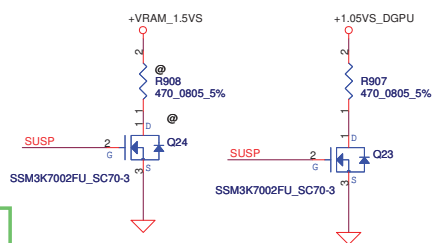
+12V1 TO +12VS



+1.5V TO +1.5VS



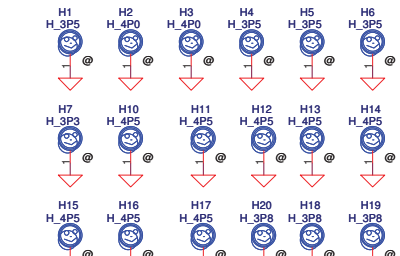
Discharge circuit



NON-PDH



Screw



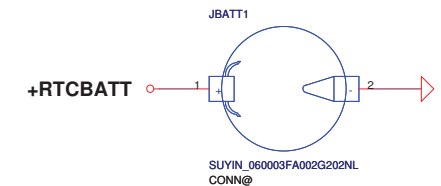
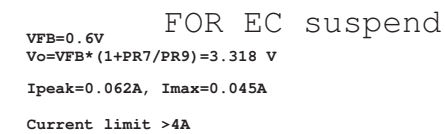
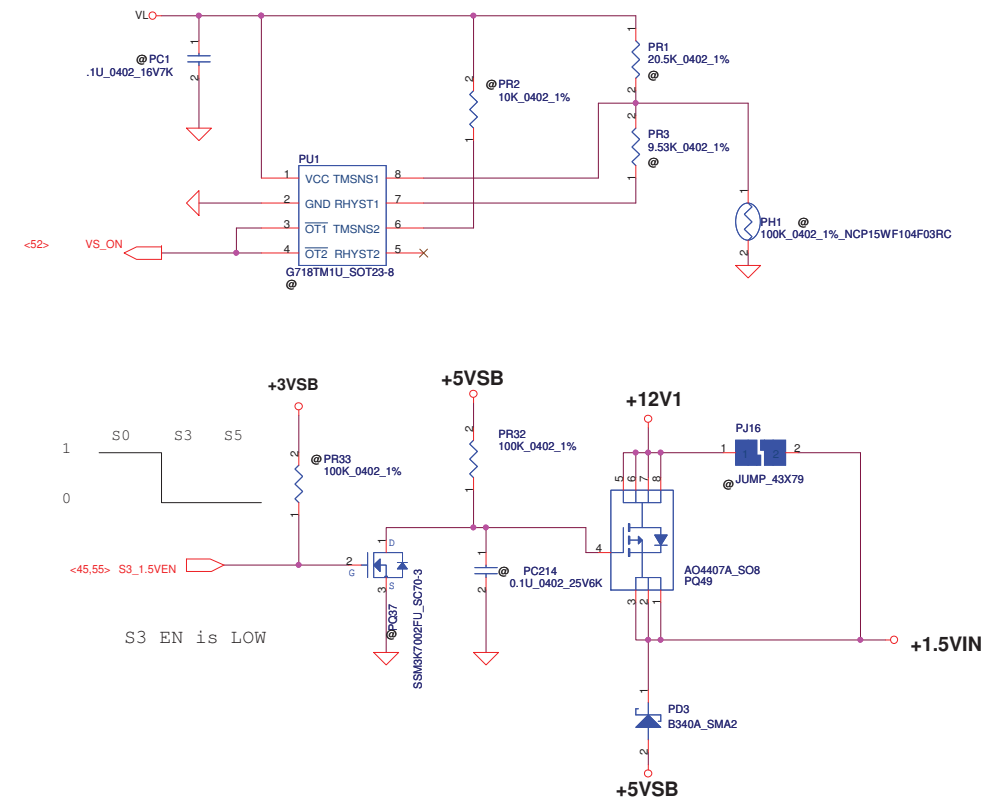
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	DC Interface/Screw	
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Power Button

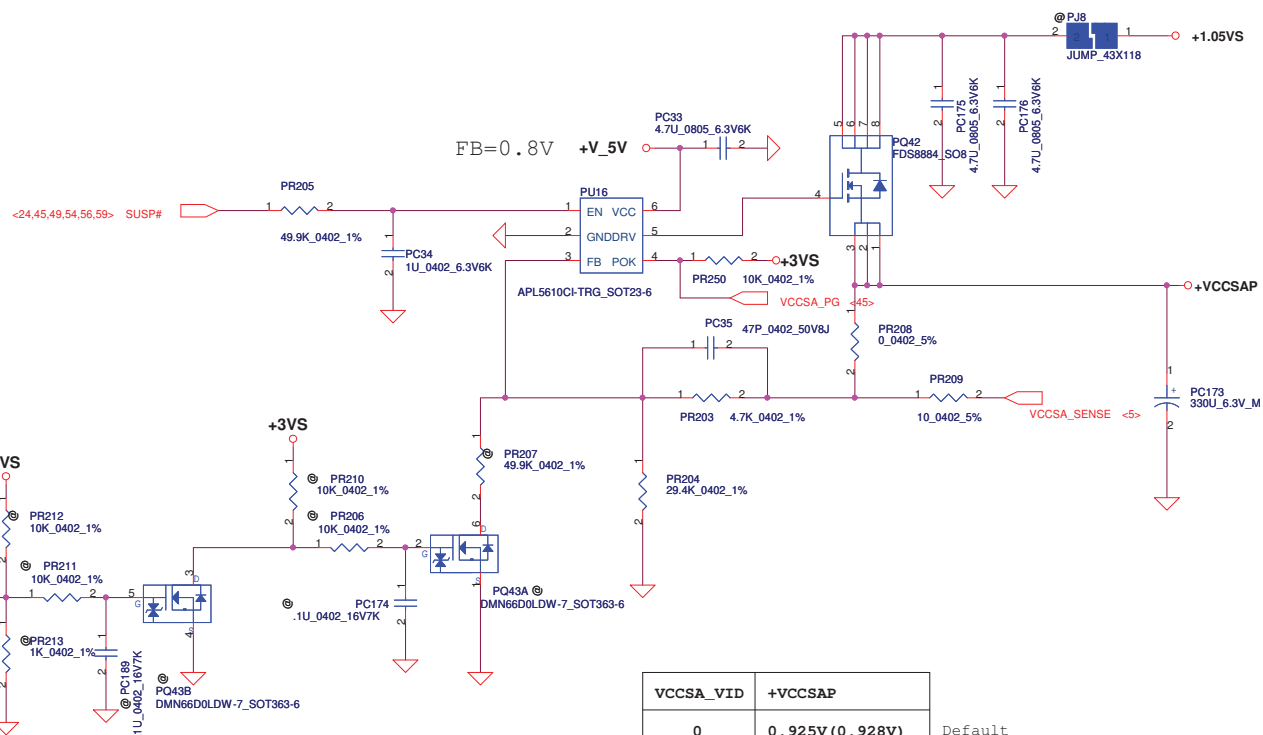
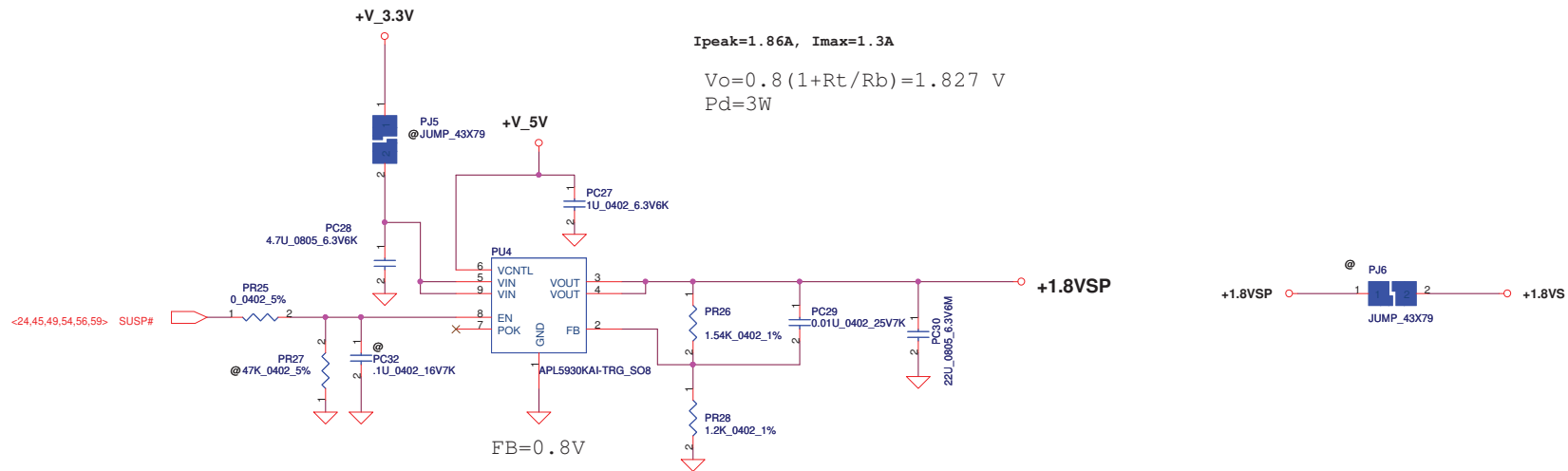


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				Power OK/PBN				
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CPU thermal protection at 92 degree C
Recovery at 57 degree C



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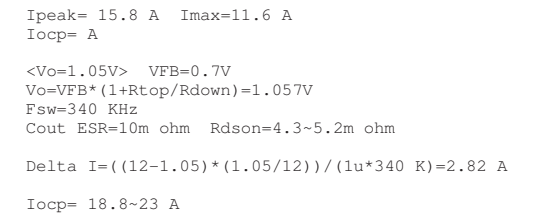


VCCSA_VID	+VCCSAP
0	0.925V (0.928V)
1	0.85V (0.851V)

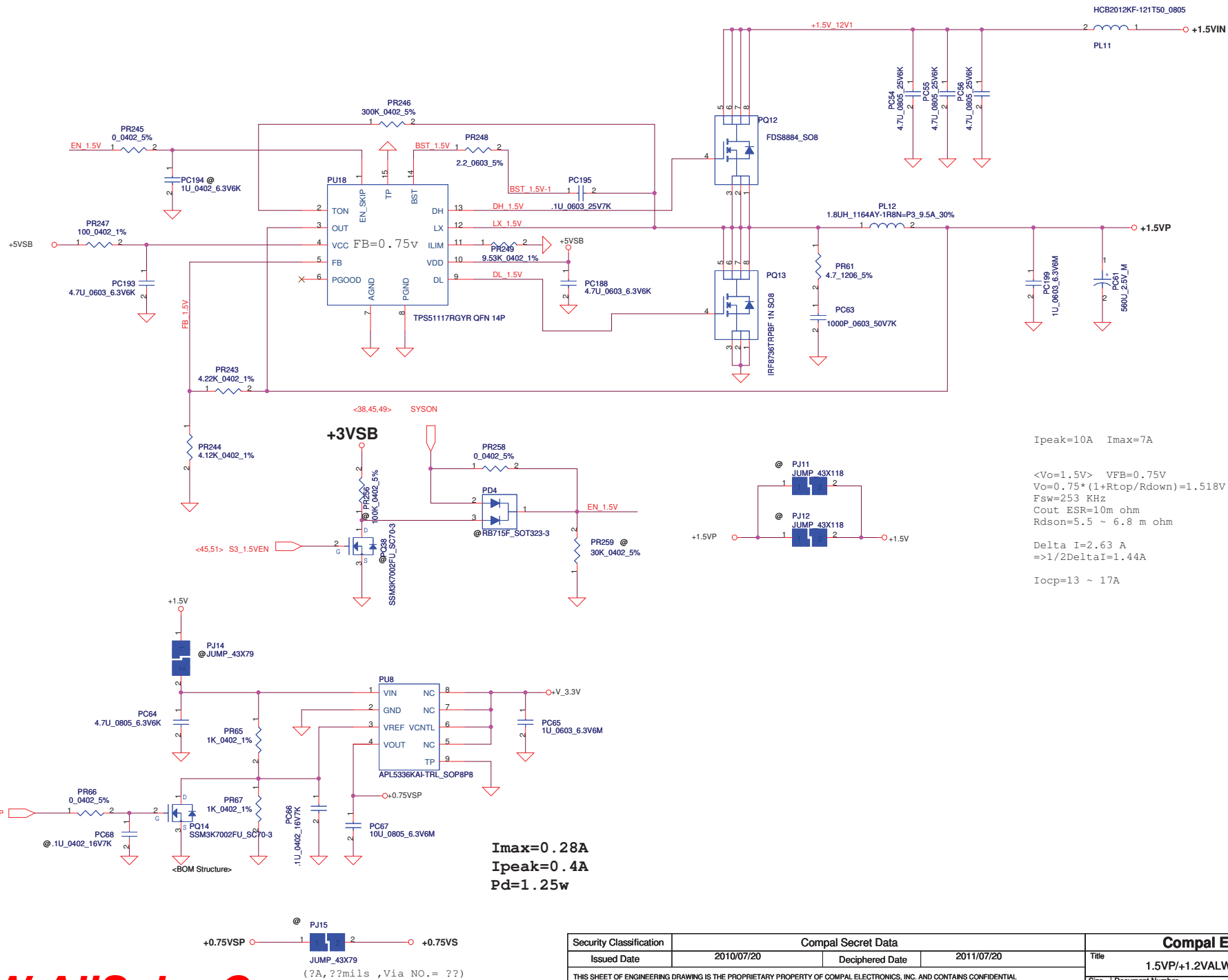
Default



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								+VCCSA+1.8VSP	
								Size	
								Document Number	
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Ipeak=10A Imax=7A

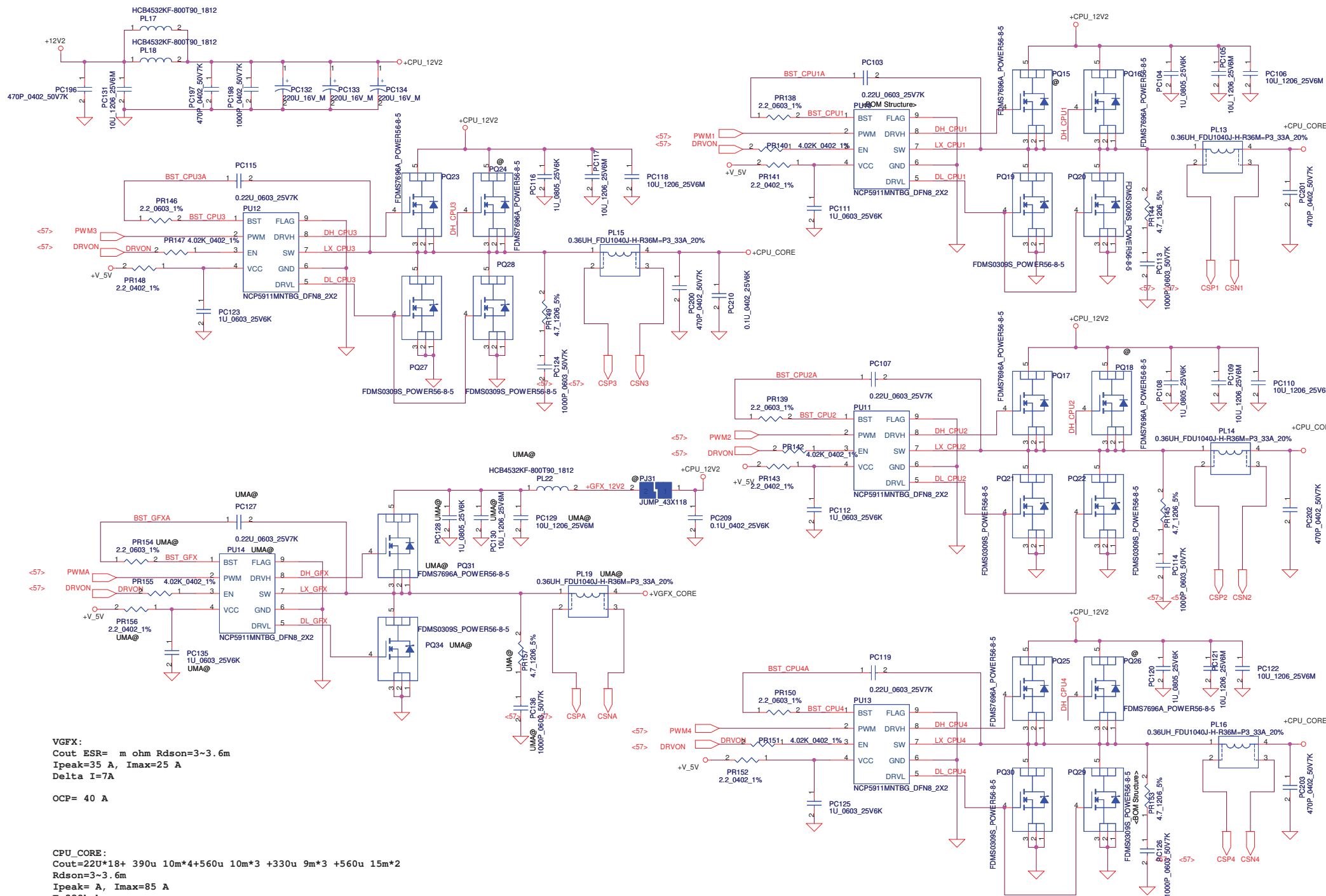
<Vo=1.5V> VFB=0.75V
 Vo=0.75*(1+Rtop/Rdown)=1.518V
 Fsw=253 KHz
 Cout=ESR=10m ohm
 Rds(on)=5.5 ~ 6.8 m ohm

Delta I=2.63 A
 =>1/2DeltaI=1.44A

Iocp=13 ~ 17A

Imax=0.28A
 Ipeak=0.4A
 Pd=1.25w

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VGFX:
 $C_{out} ESR = m \text{ ohm}$ $R_{dson} = 3 \sim 3.6m$
 $I_{peak} = 35 \text{ A}$, $I_{max} = 25 \text{ A}$
 $\Delta I = 7 \text{ A}$

OCP= 40 A

CPU_CORE:
 $C_{out} = 220\mu + 390\mu$ $10m \times 4 + 560\mu$ $10m \times 3 + 330\mu$ $9m \times 3 + 560\mu$ $15m \times 2$
 $R_{dson} = 3 \sim 3.6m$
 $I_{peak} = A$, $I_{max} = 85 \text{ A}$
 $F = 338k \text{ hz}$
 $\Delta I =$

OCP= 135 A

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5

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A

				A
Title				
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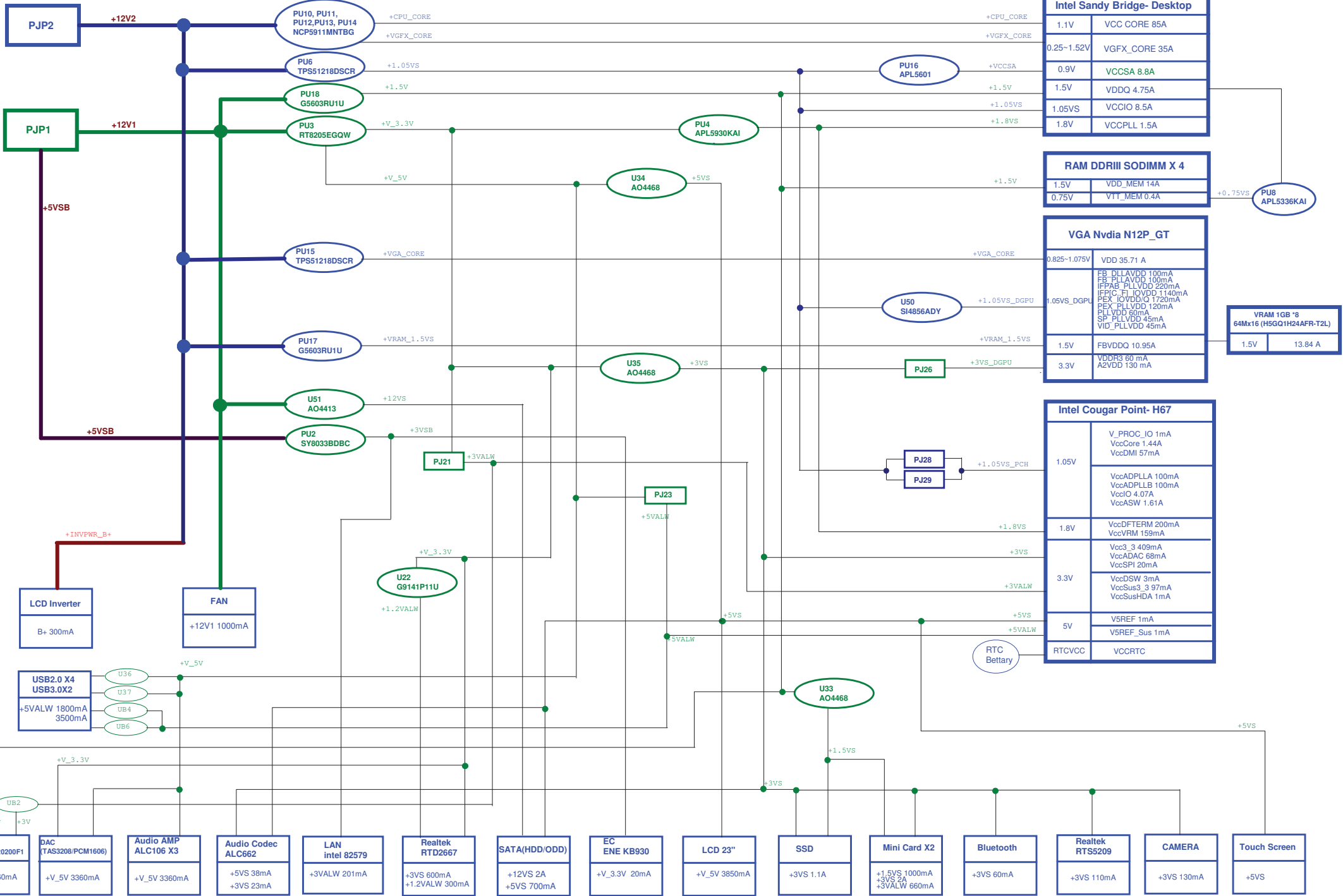
5

4

3

2

1



Intel Sandy Bridge- Desktop	
1.1V	VCC CORE 85A
0.25~1.52V	VGFX_CORE 35A
0.9V	VCCSA 8.8A
1.5V	VDDQ 4.75A
1.05VS	VCCIO 8.5A
1.8V	VCCPLL 1.5A

RAM DDRIII SODIMM X 4	
1.5V	VDD_MEM 14A
0.75V	VTT_MEM 0.4A

VGA Nvidia N12P_GT	
0.825~1.075V	VDD 35.71 A
1.05VS_DGPU	FB DLLAVDD 100mA FB PLLAVDD 100mA IFPAB PLLVDD 220mA IFPAB PLLVDD 1140mA PEX IOVDD/O 1720mA PEX PLLVDD 120mA PLVDD 60mA SP PLLVDD 45mA VID PLLVDD 45mA
1.5V	FBVDDQ 10.95A
3.3V	VDDR3 60 mA A2VDD 130 mA

VRAM 1GB *8 64Mx16 (H5GQ1H24AFR-T2L)	
1.5V	13.84 A

Intel Cougar Point- H67	
1.05V	V_PROC_IO 1mA VccCore 1.44A VccDMI 57mA VccADPLLA 100mA VccADPLLB 100mA VccIO 4.07A VccASW 1.61A
1.8V	VccDFTERM 200mA VccVRM 159mA
3.3V	Vcc3_3 409mA VccADAC 68mA VccSPI 20mA VccDSW 3mA VccSus3_3 97mA VccSusHDA 1mA
5V	V5REF 1mA V5REF_Sus 1mA
RTCVC	VCCRTC

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