

LCFC Confidential


CGx20 M/B Schematics Document

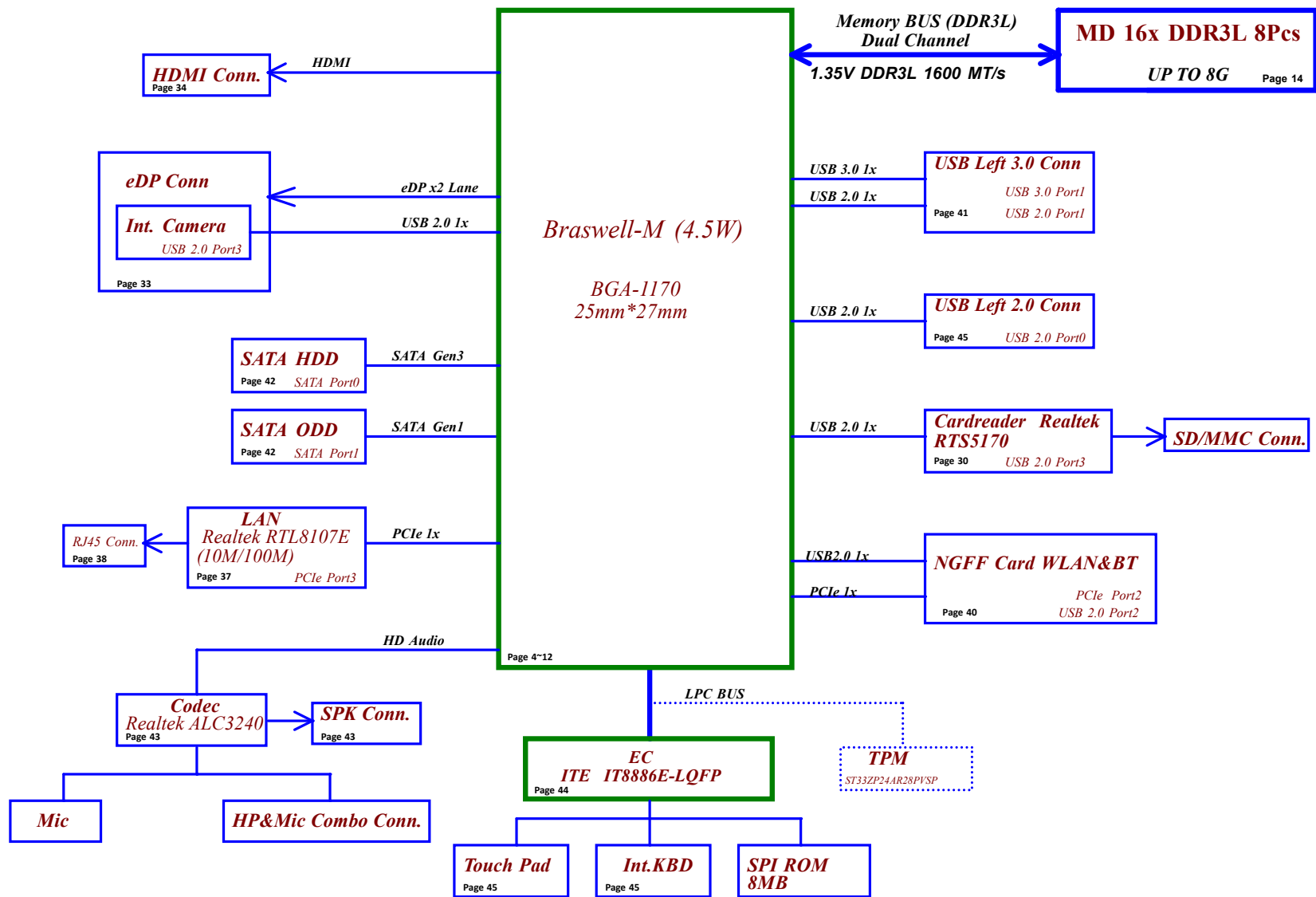
NM-A805 REV:0.1

Intel Braswell M-Processor with DDRIII

2015-10-09

REV: 0.1

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/10/08	Deciphered Date	2015/03/23	Cover Page			
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Issued Date	2015/10/08	Deciphered Date	2015/03/23	Block Diagram	
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Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane \ State	B+	+3VALW +3VL	+3VALW_SOC +1.0VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS +0.68VS CPU_CORE GFX_CORE
S0	0	0	0	0	0
S3	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	EC +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	USB Port (Left Side)
	1	USB3.0 Card Reader
USB 2.0	0	USB Port (Left Side)
	1	USB Port (Right Side)
	2	BT
	3	Camera
	4	USB Port (Right Side)
USB HUB	1	
	2	
	3	
	4	

BOM Structure Table

BOM Structure	BTO Item
AOAC@	AOAC support part
OPT@	GPU Part
UMA@	UMA SKU ID part
14@	For 14" part
15@	For 15" part
100M@	100M LAN part
N15SGT@	N15SGT Part
N15VGM@	N15GSM Part
GIGA@	GIGA LAN Part
GC6@	GPU GC6 Part
TS@	Touch Screen part
RANKA@	GPU VRAM RANKA PART
RANKB@	GPU VRAM RANKB PART
ME@	Connector
CD@	COST DOWN
@	Not stuff
H4T@	Hynix VRAM Part
M4T@	Micron VRAM Part
S4T@@	Samsung VRAM Part

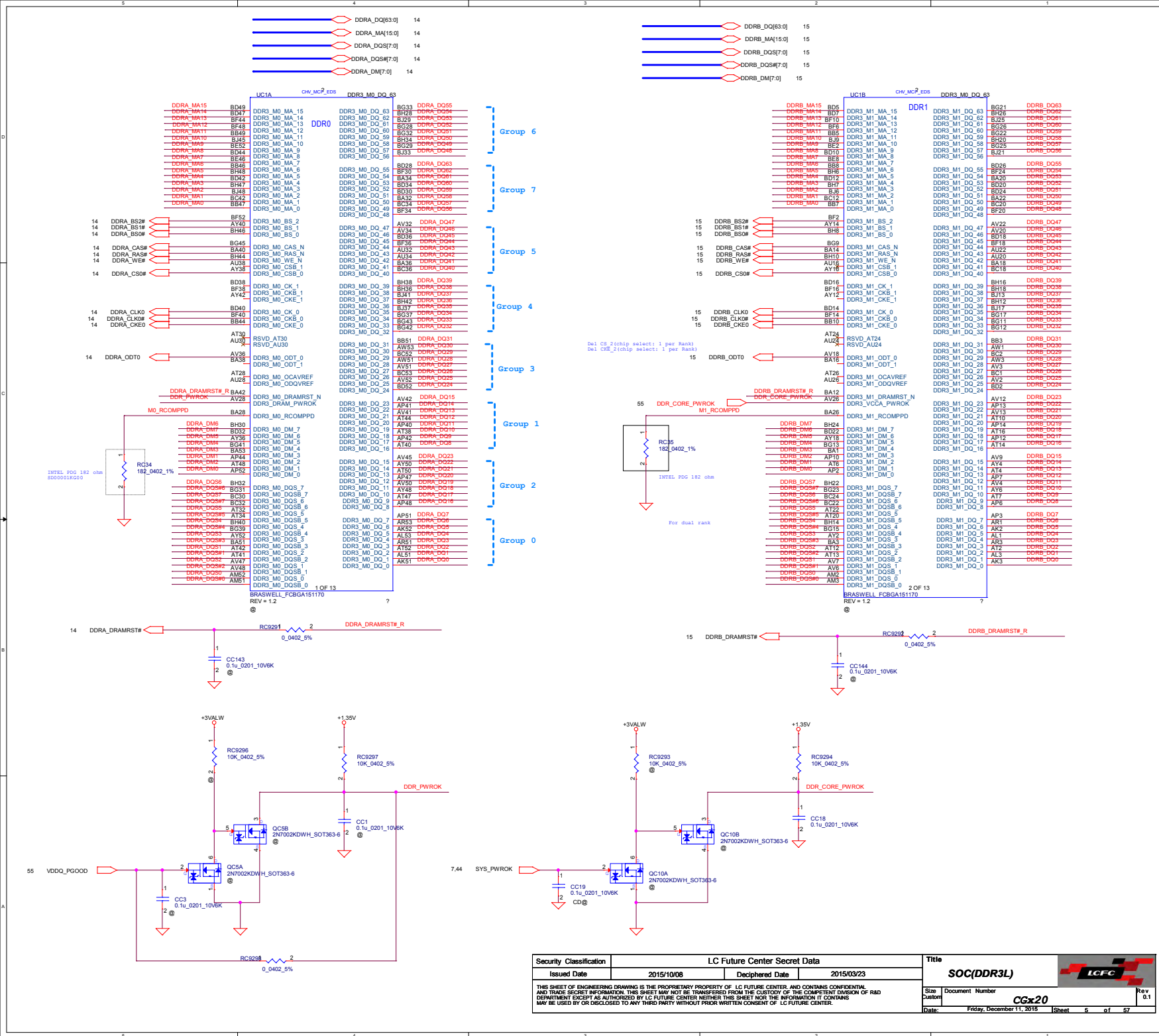
PCIE PORT LIST

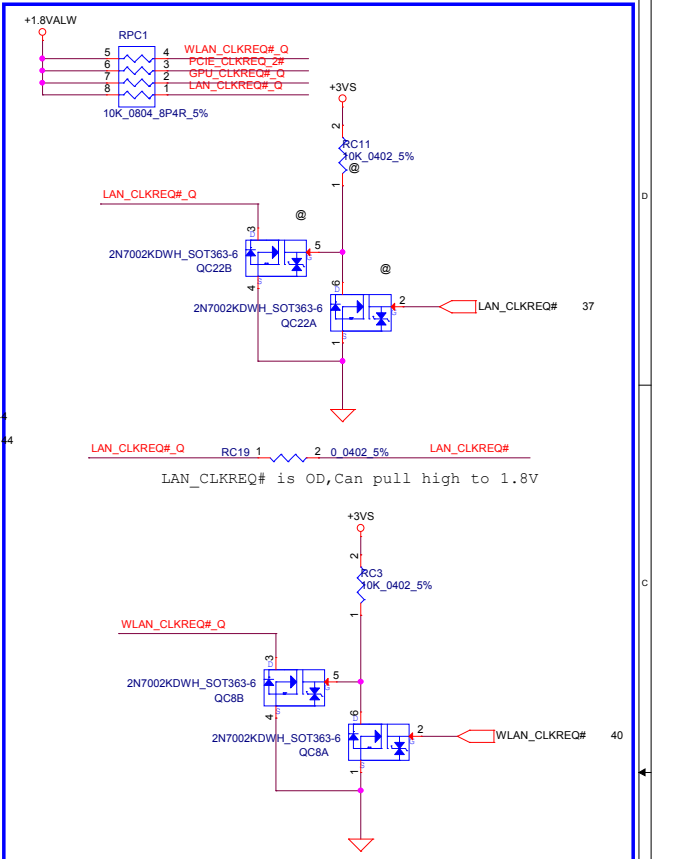
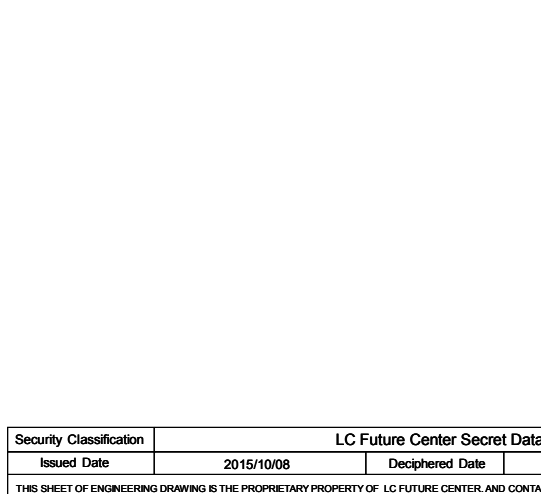
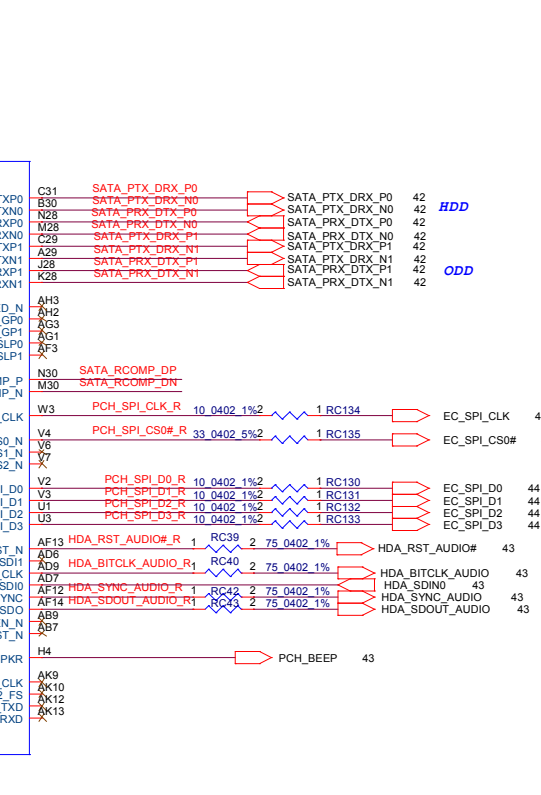
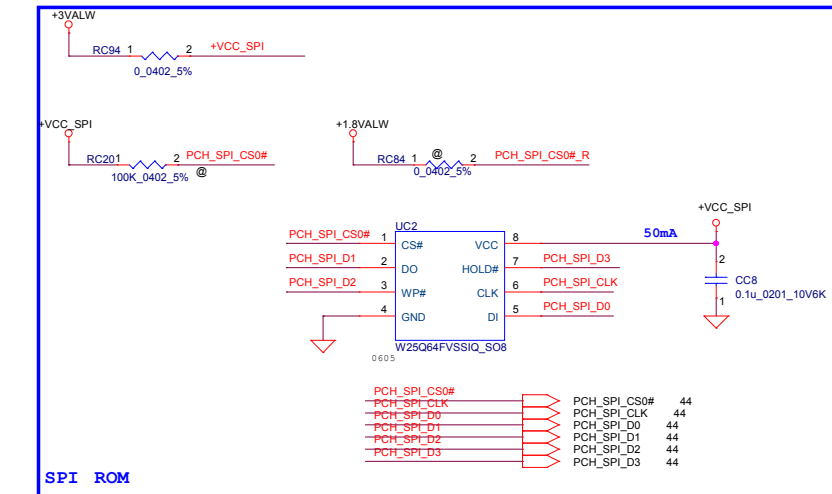
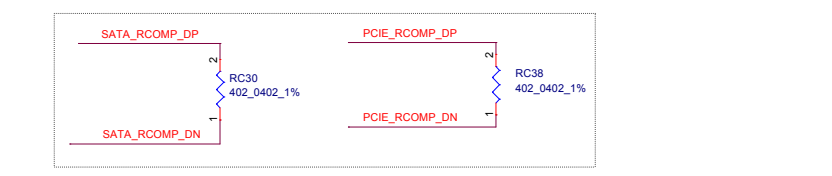
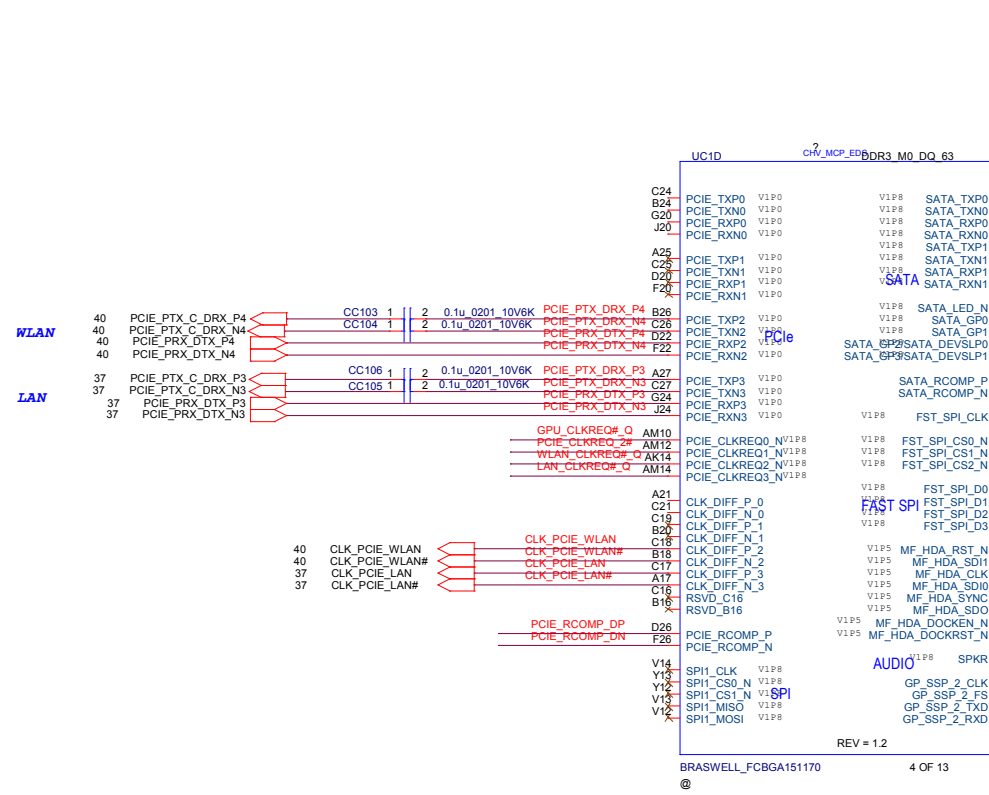
Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI

EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_100xb(reserve)	DDR DIMMA	1010 000Xb
Charger	need to update	VGA	0x9E(base on NV default)	Wlan	Rsvd
				TP	need to update



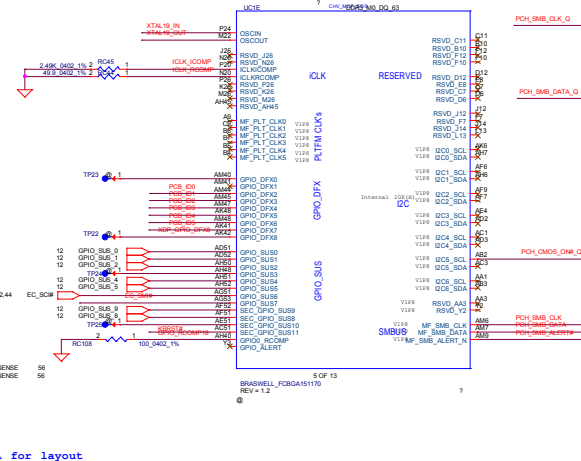
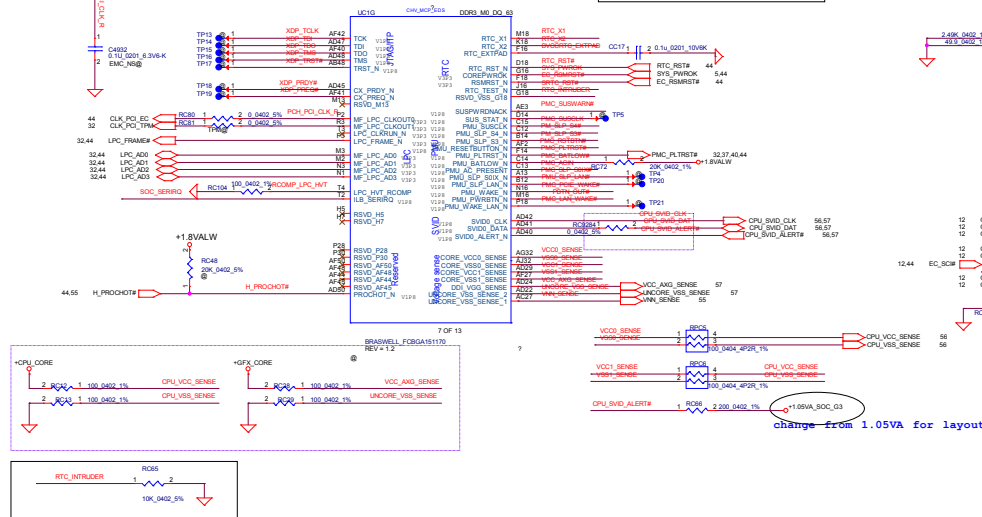
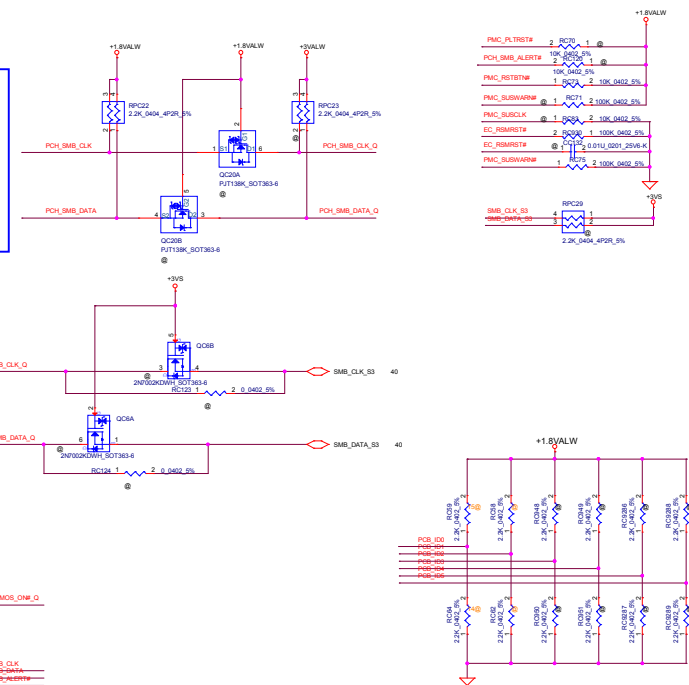
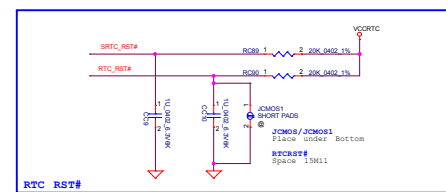
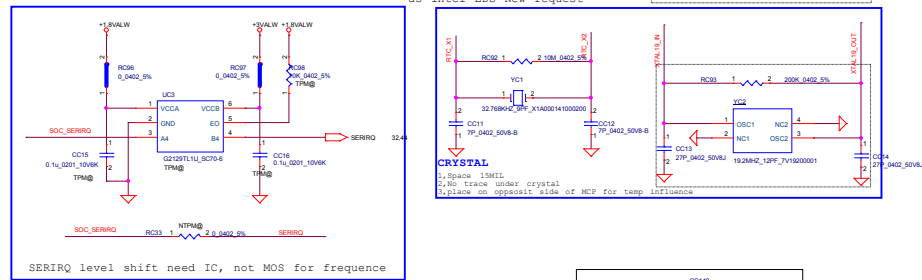


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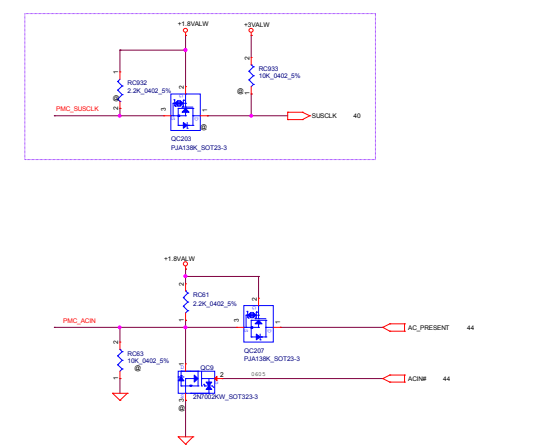
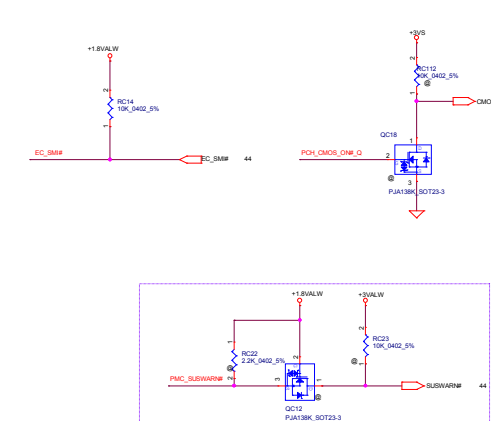
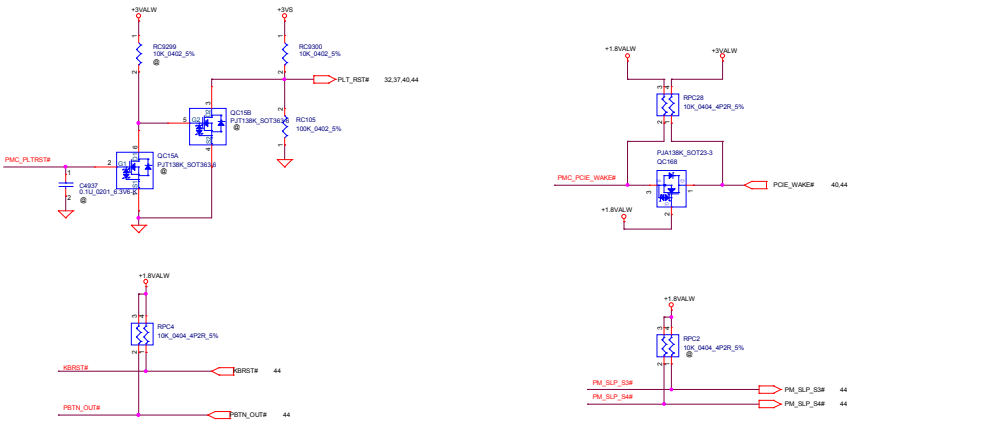
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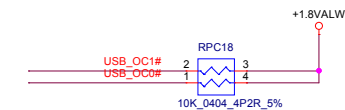
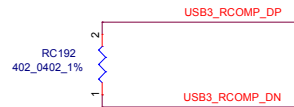
1,Spec. request 19.2MHz, Cp=12pf, RC=200K
32.768K need change to SJ10000IM0D,
as intel EDS New request

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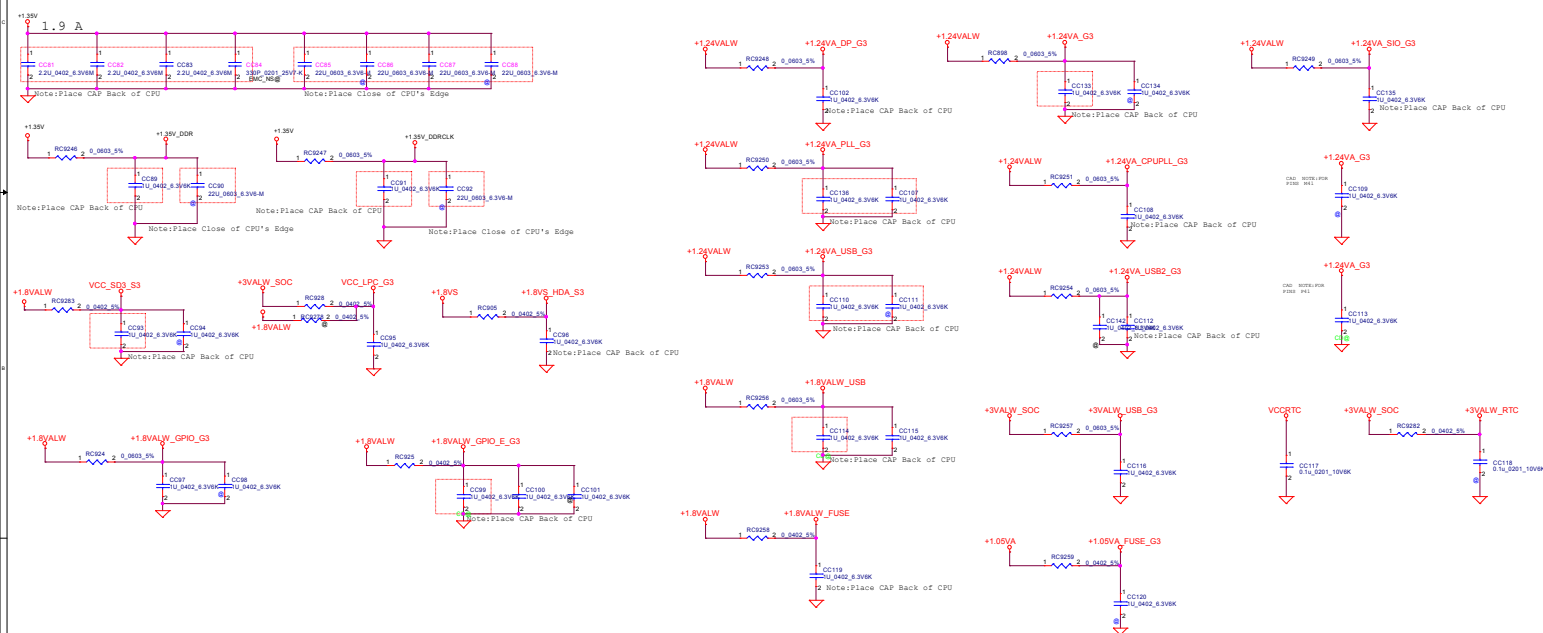
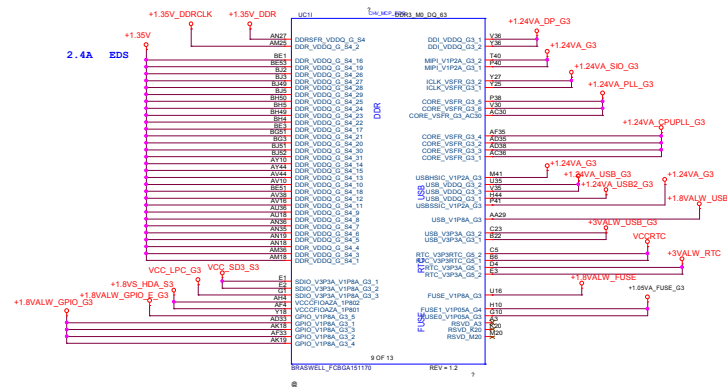




PWB 100	PWB 101	PWB 102	PWB 103	PWB 104	Description
0	X	X	X	X	Reserve 14** BMT
1	X	X	X	X	Reserve 15** BMT
X	0	X	X	X	single channel DEMO CDSB
X	1	X	X	X	Reserve dual channel DEMO CDSB and CDSB
X	X	0	0	1	Reserve Deming 45 (450401-0410-0305)
X	X	0	0	0	Reserve Mytic 45 (0507-050378-2500)
X	X	0	1	1	Reserve Mytic 45 (0507-07000-0700-17-19)
X	X	1	0	0	Reserve Mytic 45 (0507-050378-2500)
X	X	1	0	1	Reserve Mytic 45 (0507-07000-0700-17-19)

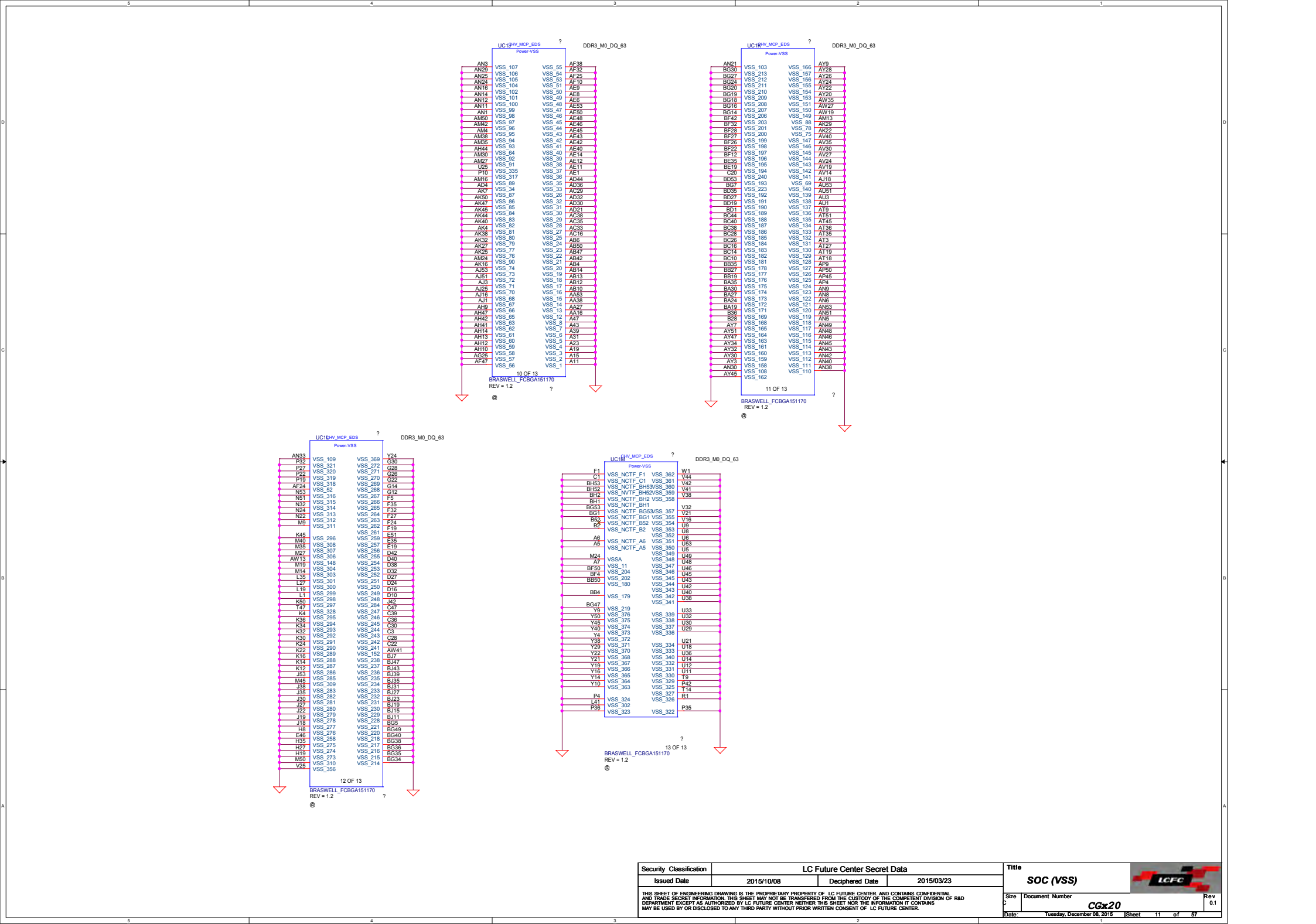




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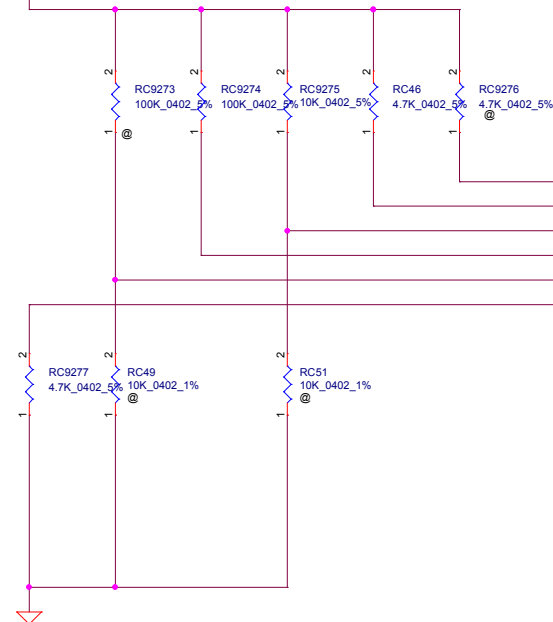


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Date: Sunday, December 13, 2020			Rev 01	Rev 01



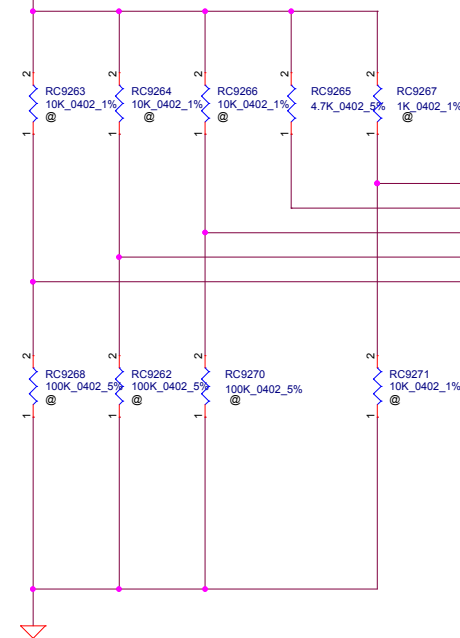
Hardware STRAPS (Follow up CRB)

+1.8VALW



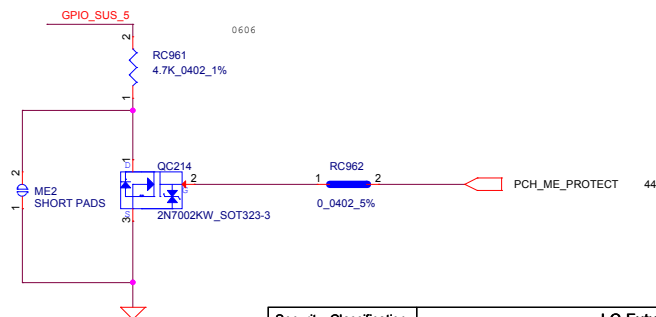
GPIO_SUS_0 7
GPIO_SUS_1 7
GPIO_SUS_2 7
GPIO_SUS_4 7
GPIO_SUS_5 7
GPIO_SUS_8 7

+1.8VALW



GPIO_SUS_9 7
EC_SC# 7.44
GPIO_CAM_8 4
GPIO_CAM_9 4
GPIO_CAM_11 4

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak internal (20k PD)	0 = DSI Port not detected 1 = DSI Port detected Note: DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak internal (20k PU)	1 = Normal Operation Note: This strap MUST be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V
GPIO_CAMERASB08	IClk Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass





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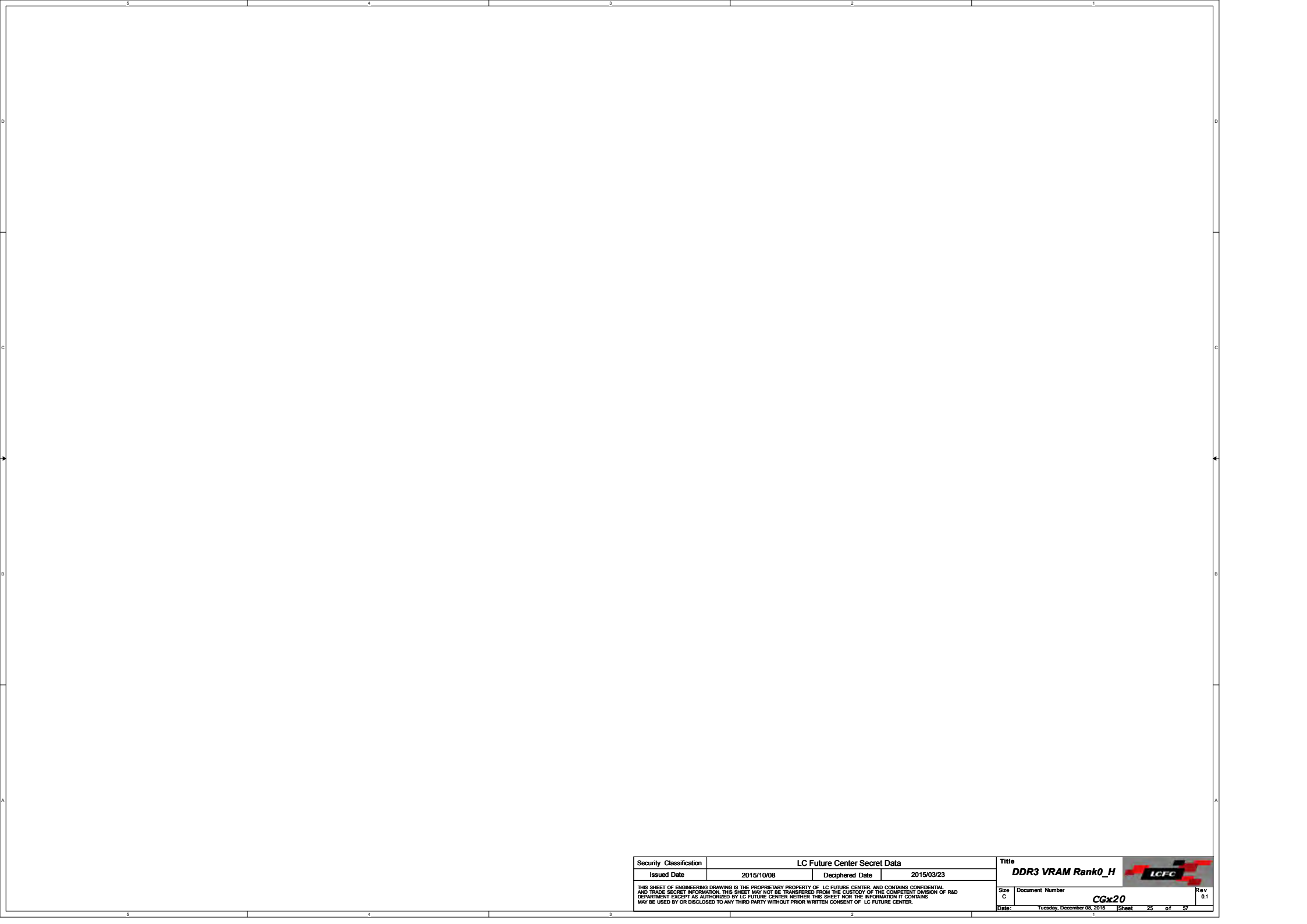
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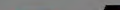


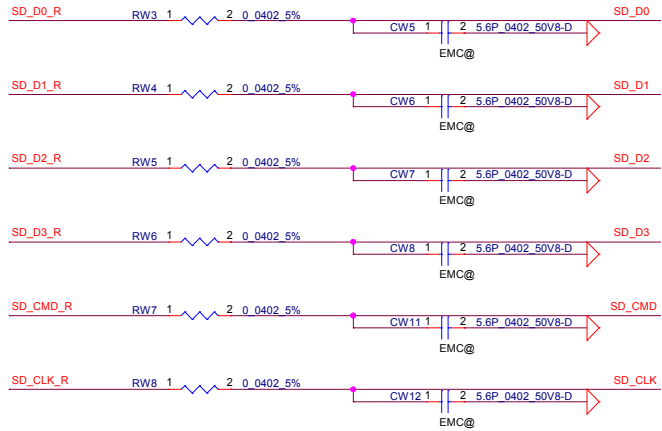
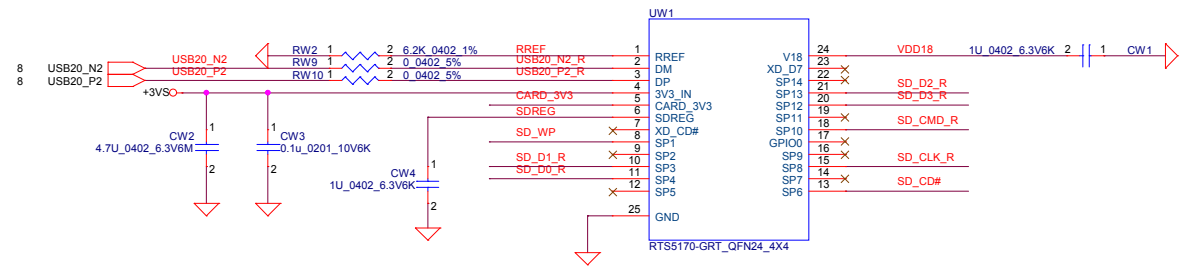
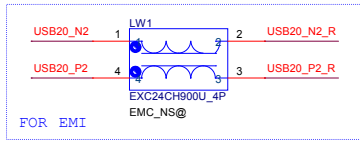
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Issued Date		2015/10/08	Deciphered Date	2015/03/23	DDR3 VRAM Rank0_H
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</small>					
Size	Document Number				Rev
C	CGx20				0.1
Date:		Tuesday, December 08, 2015		Sheet	25 of 57



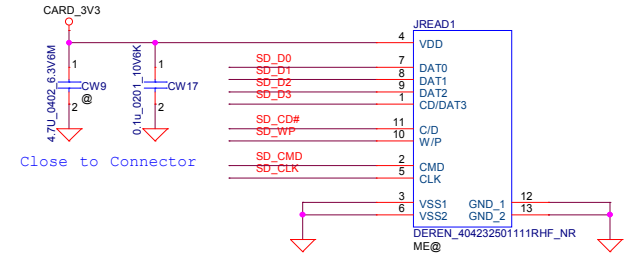
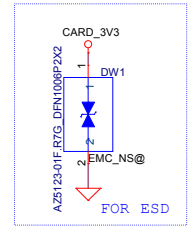
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Size	Document Number				Rev	
C	CGx20				0.1	
Date: Tuesday, December 08, 2015					Sheet 26 of 57	

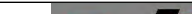
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Size C	Document Number CGx20				Rev 0.1	
Date: Tuesday, December 08, 2015						Sheet 28 of 57

Security Classification		LC Future Center Secret Data		<div>Title</div> <div>Blank</div> <div></div>	
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<div>Date:</div> <div>Tuesday, December 08, 2015</div> <div>Sheet</div> <div>29</div> <div>of</div> <div>57</div>					






Close to Connector



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/08	Deciphered Date	2015/03/23	Cardreader	
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Size	Document	Number	Rev		
Custom		CGx20	0.1		
Date:	Tuesday, December 08, 2015	Sheet	30	of	57

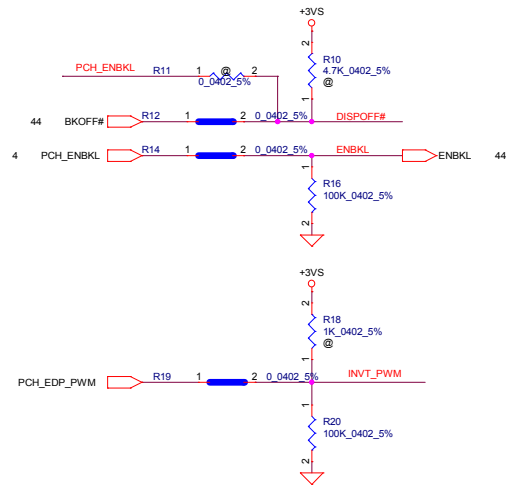
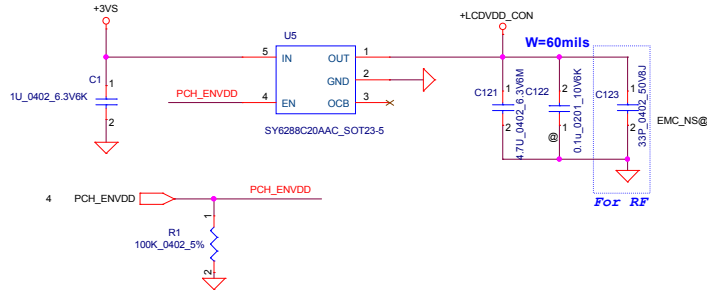


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D				D																				
C				C																				
B				B																				
A				A																				
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Issued Date	2015/10/08	Deciphered Date	2015/03/23	Blank																				
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Date: Tuesday, December 08, 2015				Sheet 31 of 57																				
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Security Classification	LC Future Center Secret Data																										
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Size Custom	Document Number	CGx20		Rev 0.1																							
Date:	Tuesday, December 08, 2015	Sheet 32 of 57																									
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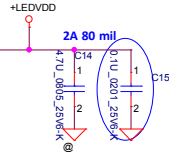
LCD POWER CIRCUIT

W=60mils



V20B+

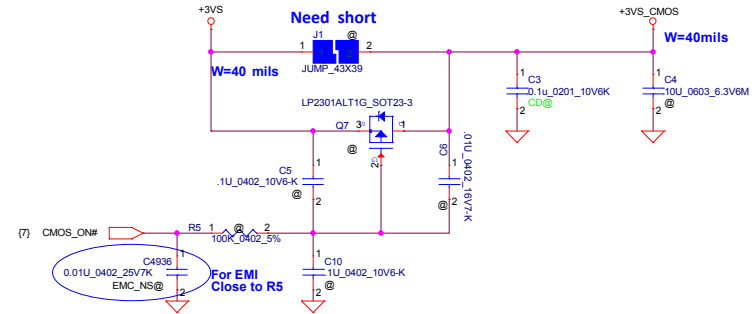
2A 80 mil



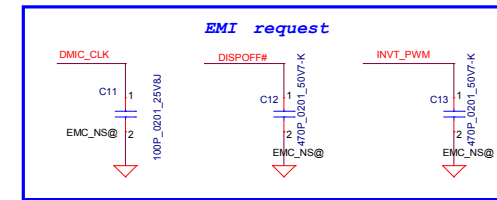
CMOS Camera

Need short

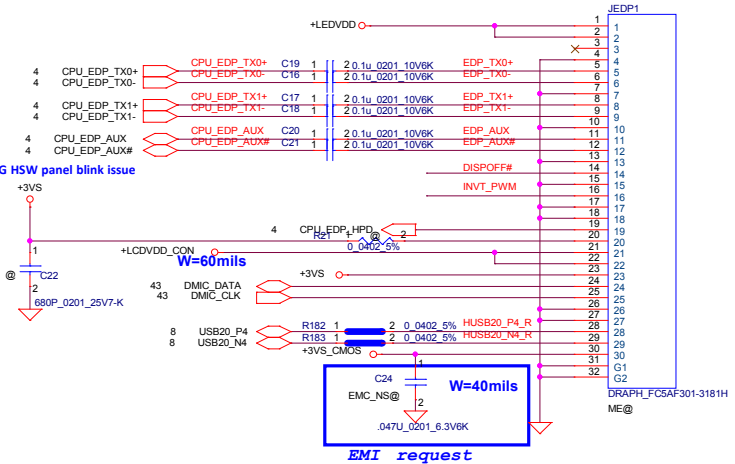
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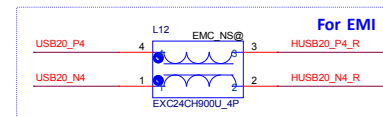
EMI request



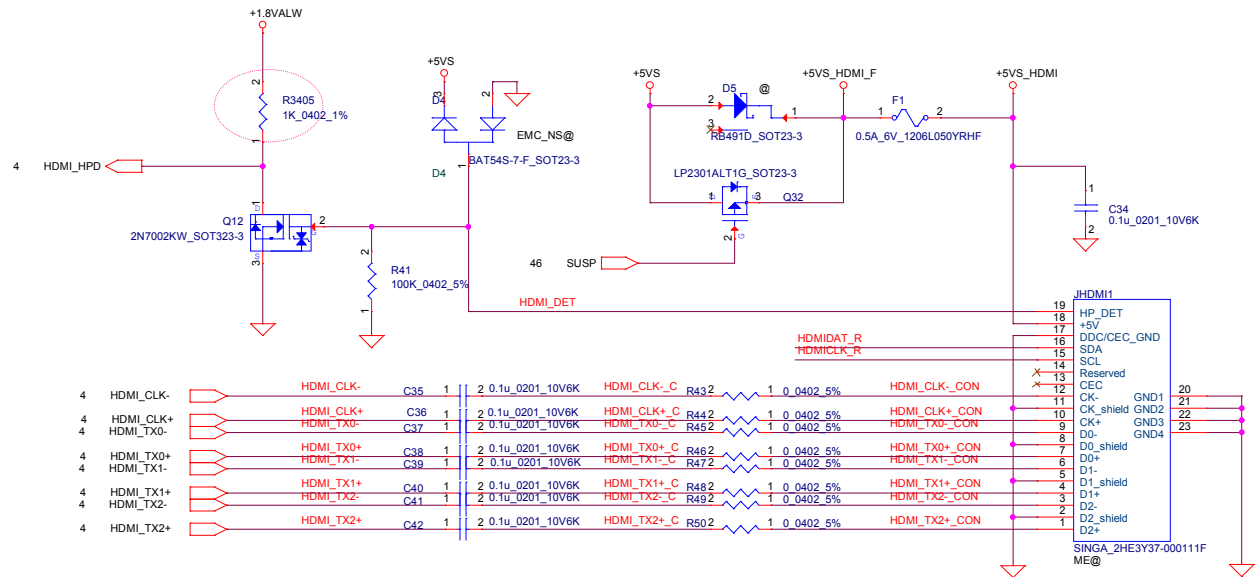
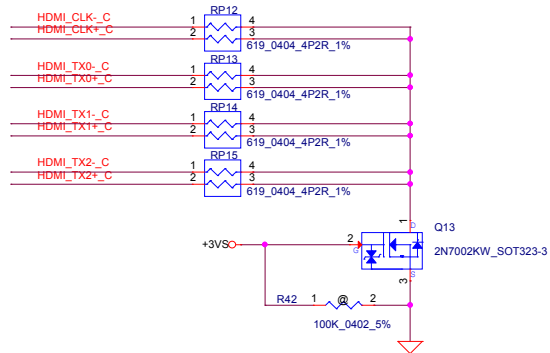
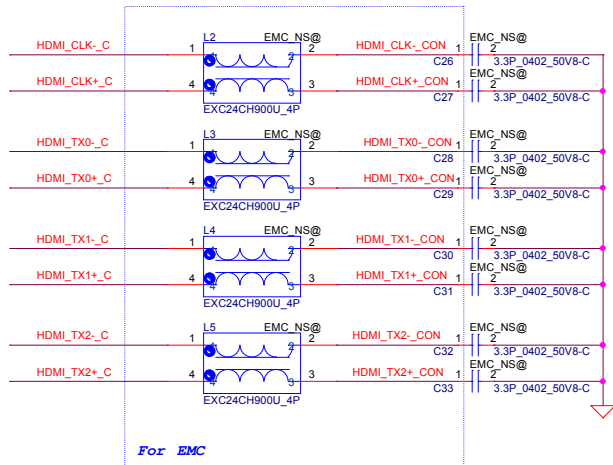
C23 0.1u for G HSW panel blink issue



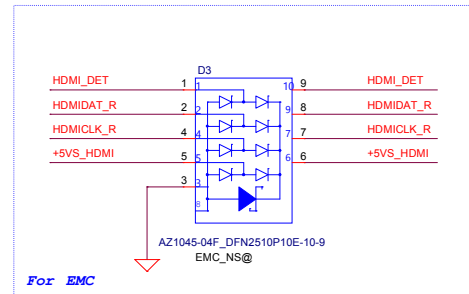
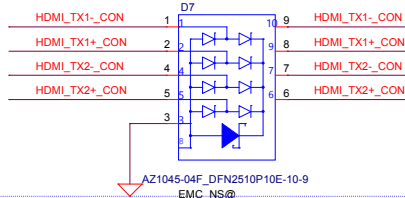
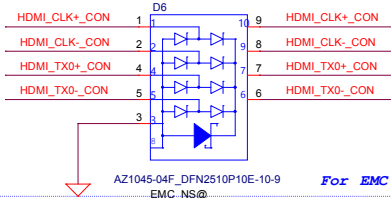
EMI request



Security Classification	LC Future Center Secret Data			Title	eDP/ CMOS/Touch screen		
Issued Date	2015/10/08	Deciphered Date	2015/03/23	Size	Document	Number	Rev
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				Date:	Tuesday, December 08, 2015	Sheet	33 of 57



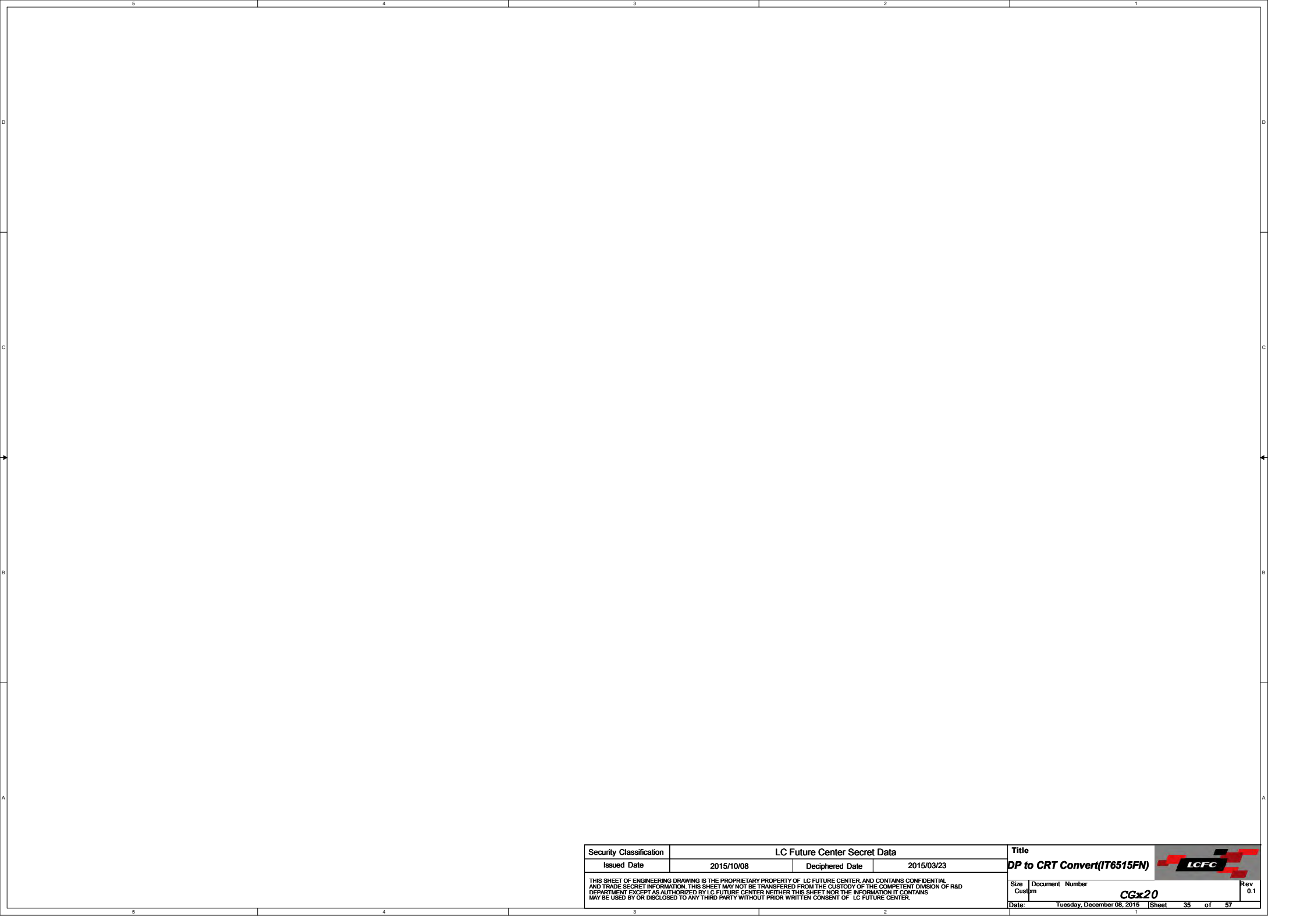
Close to JHDMI1





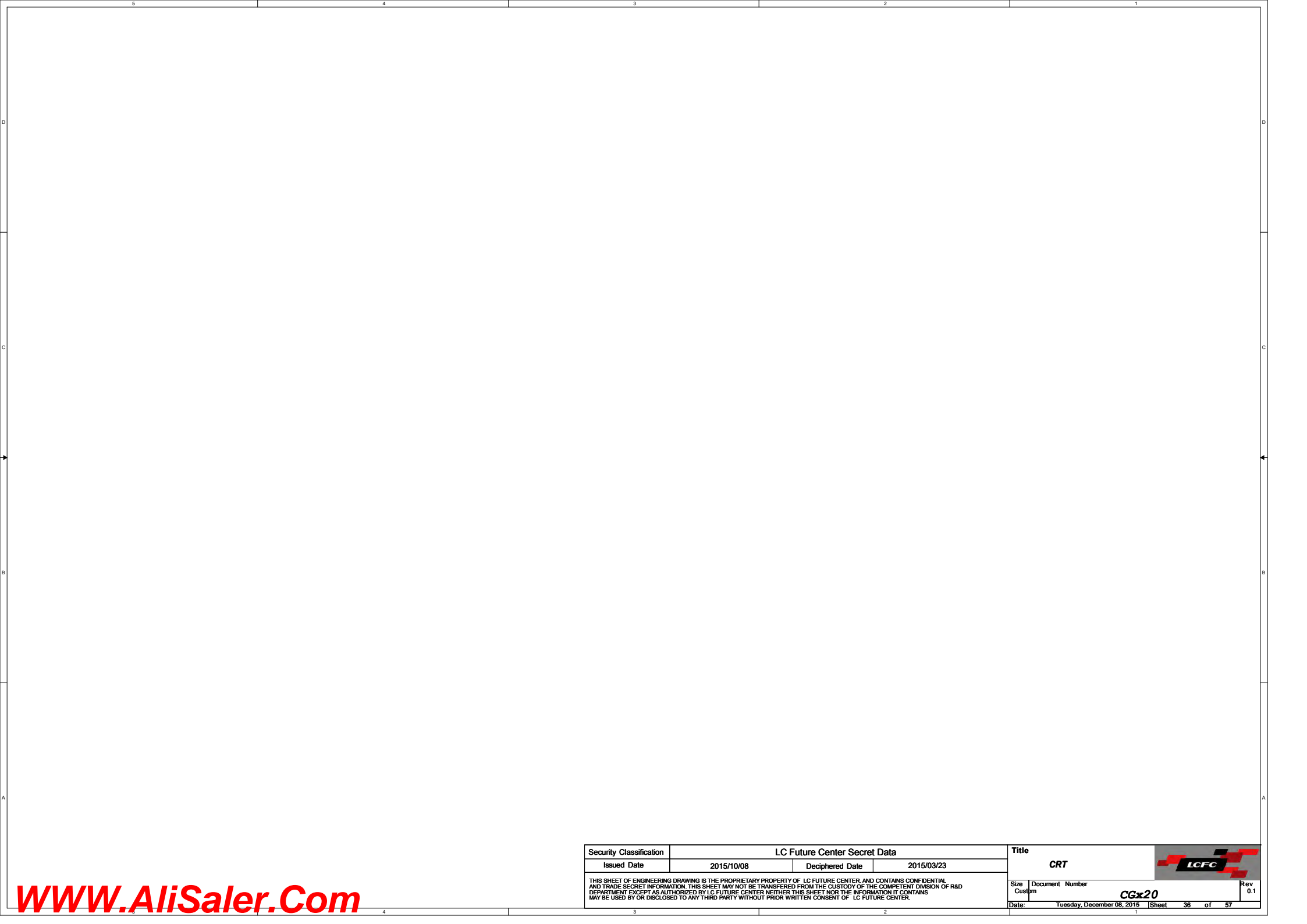
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LC Future Center Secret Data			
Issued Date	2015/10/08	Deciphered Date	2015/03/23
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Title			
HDMI_CONN			
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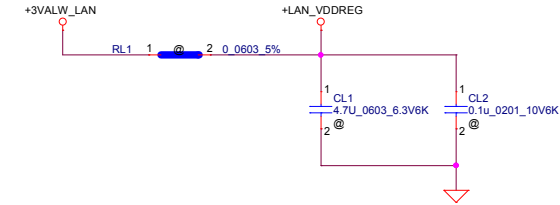
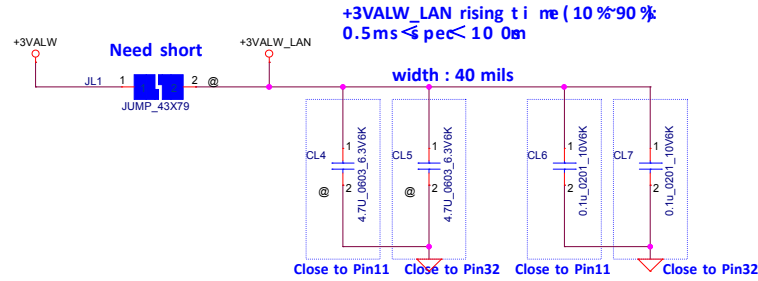


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Issued Date	2015/10/08	Deciphered Date	2015/03/23	DP to CRT Convert(IT6515FN)							
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Issued Date	2015/10/08	Deciphered Date	2015/03/23	CRT			
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				Custom	CGx20	0.1	
				Date:	Tuesday, December 08, 2015	Sheet	36 of 57

+3VALW TO +3VALW_LAN

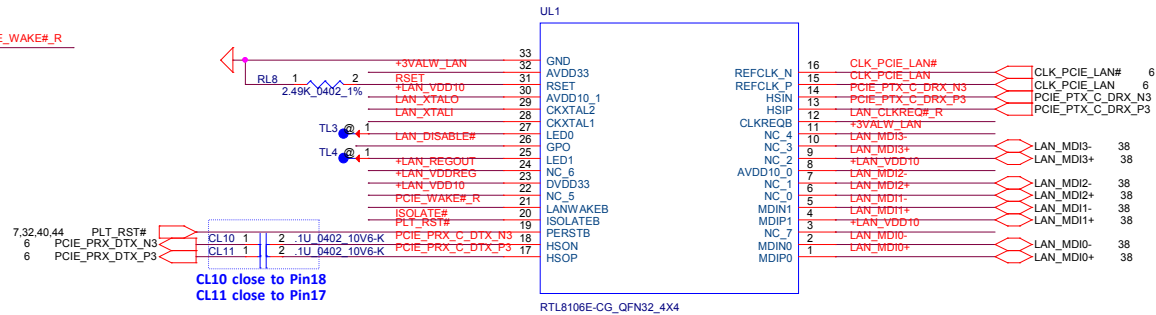
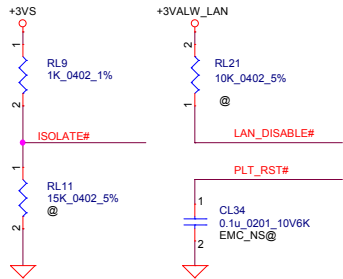


40,44 LAN_WAKE#

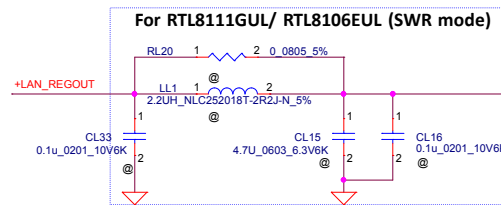
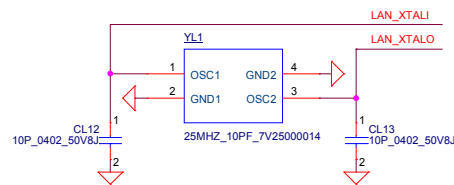
RL61 1 2 @

0.0402_5%

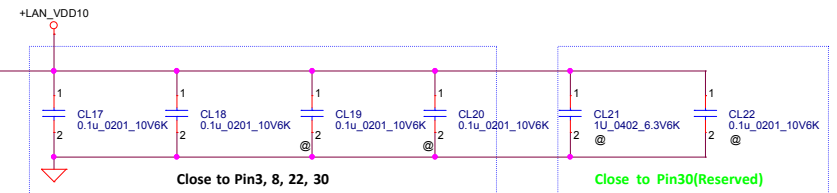
PCIE_WAKE#_R




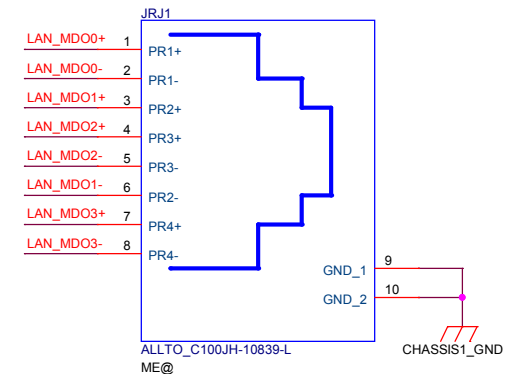
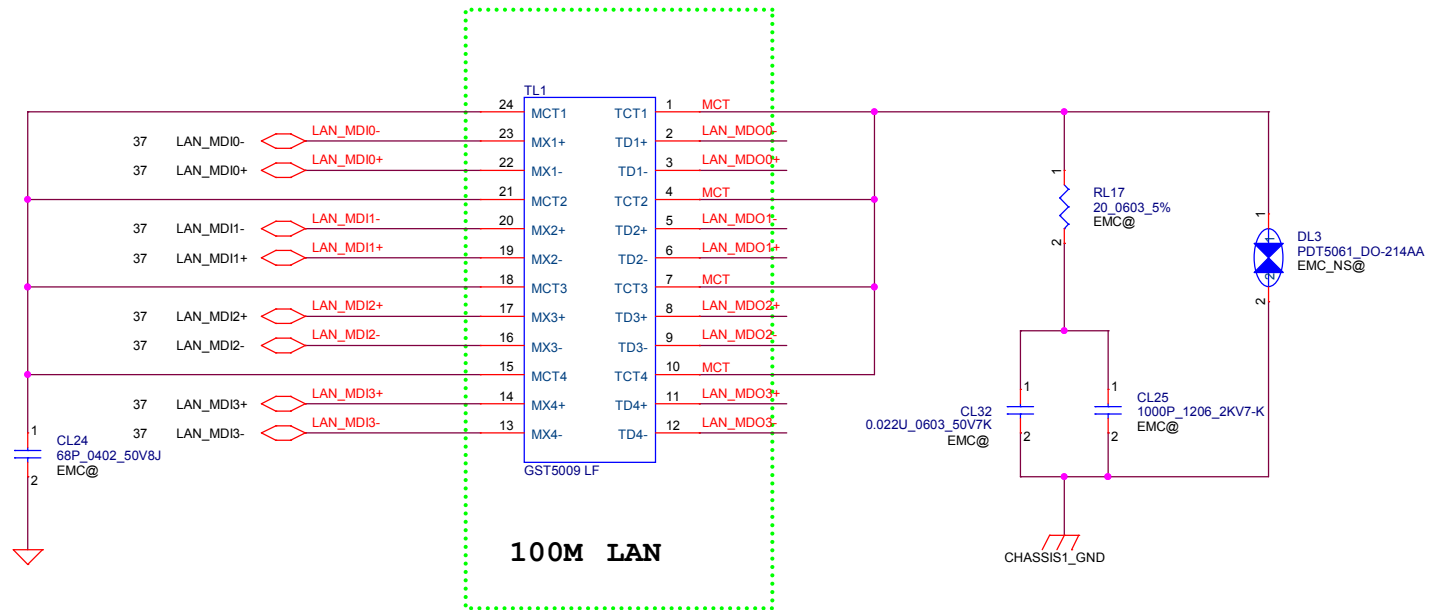
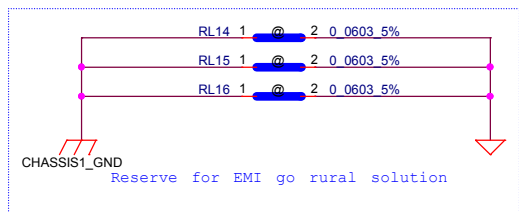
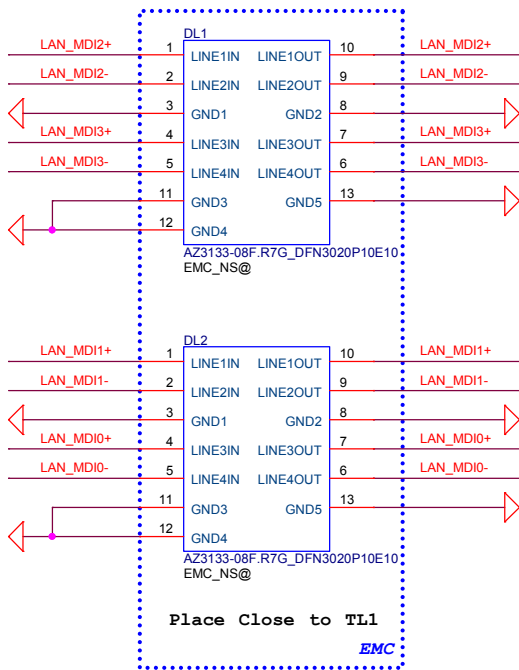
100M LAN



Layout Note: LL1 must be within 200mil to Pin24,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil



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Size Custom		Document Number		CGx20		Rev 0.1		
Date:		Wednesday, December 09, 2015		Sheet 37 of 57				

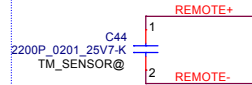


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/10/08	Deciphered Date	2013/08/05	LAN_Transformer	
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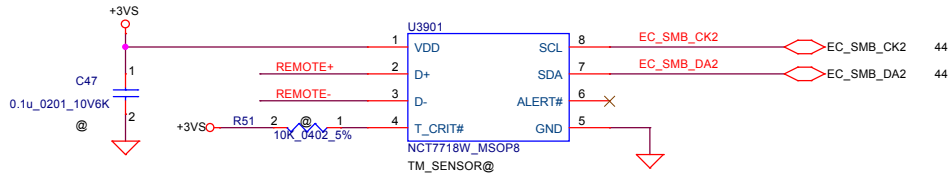
CGx20

Close to U3901



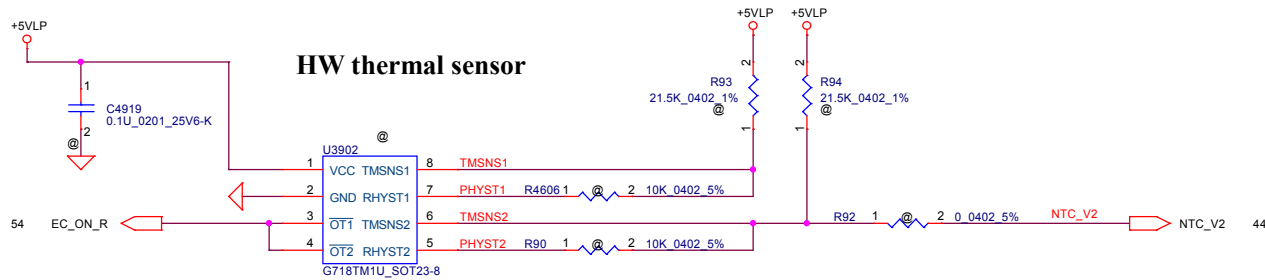
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM



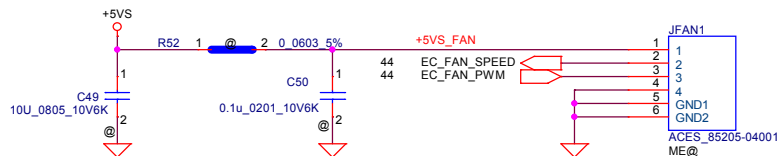
Address 1001_100xb

HW thermal sensor

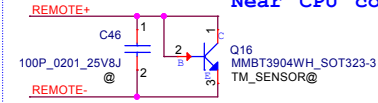


over temperature threshold:
 $RSET=3*RTM$
 $92+/-30C$
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
 $56+/-30C$

FAN Conn

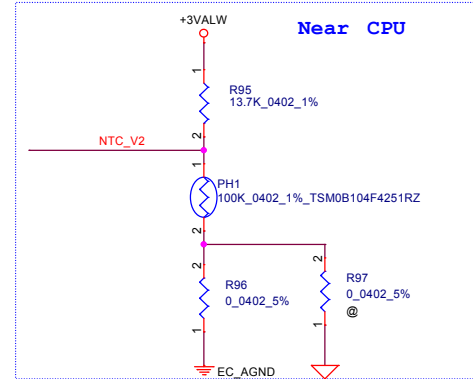



Near CPU core



Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal

Near CPU

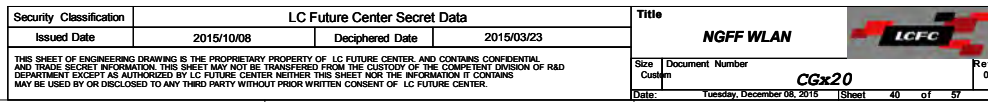


Security Classification		LC Future Center Secret Data		Title		
Issued Date	2015/10/08	Deciphered Date	2015/03/23	Thermal sensor/FAN CONN		
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				Custom	CGx20	0.1
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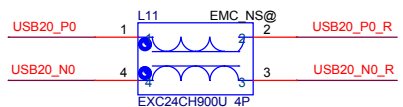
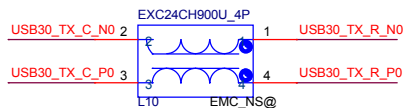
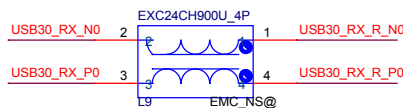
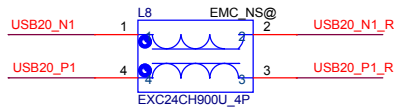
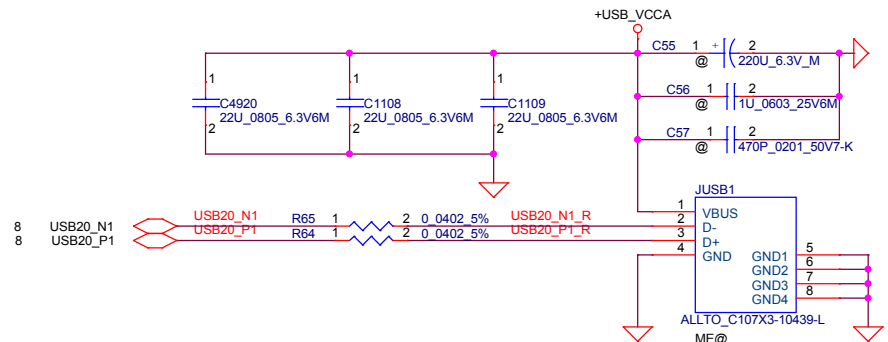
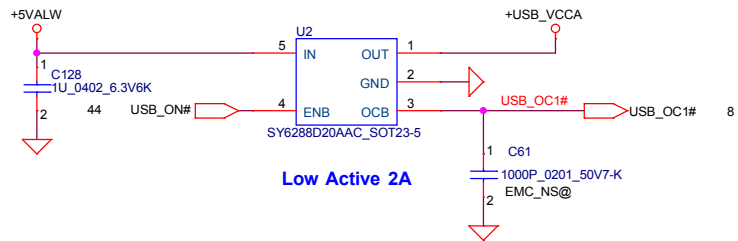


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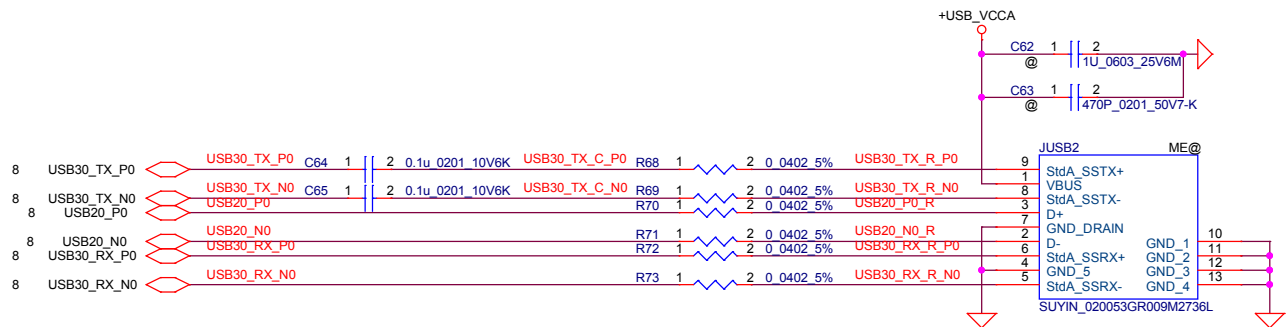
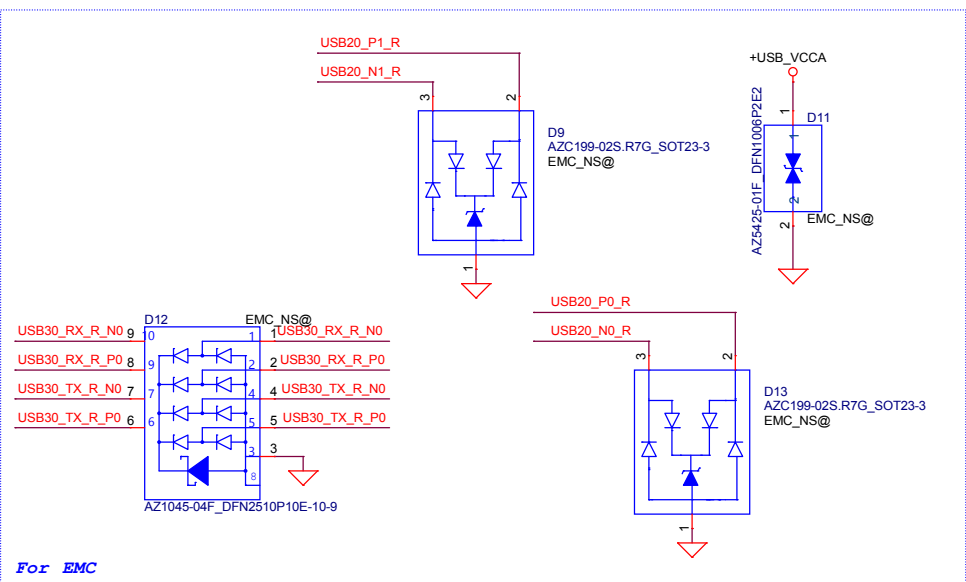
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LEFT SIDE USB PORT X2



For EMC

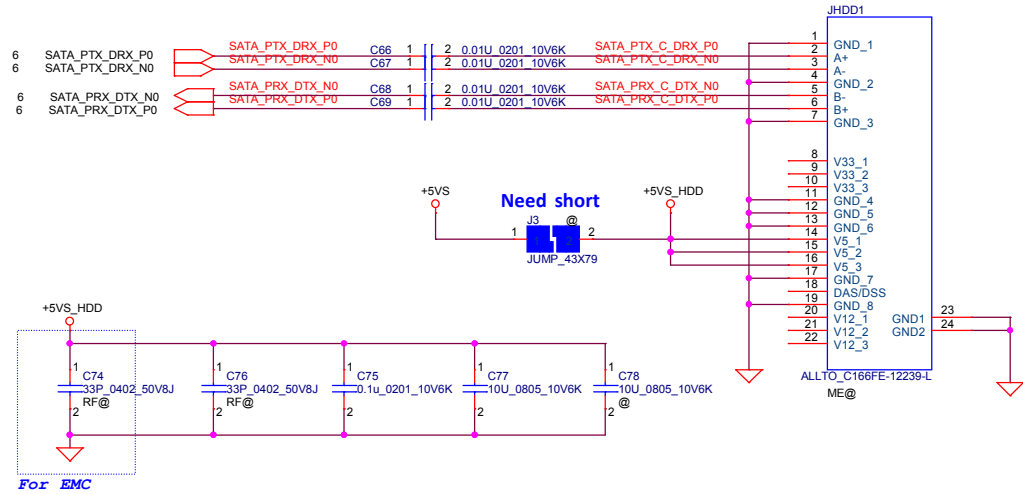


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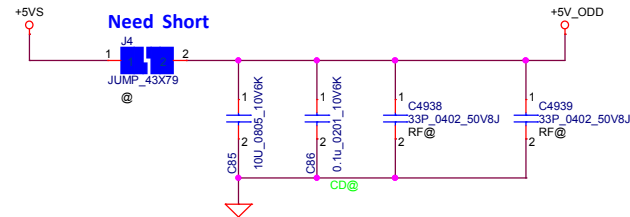
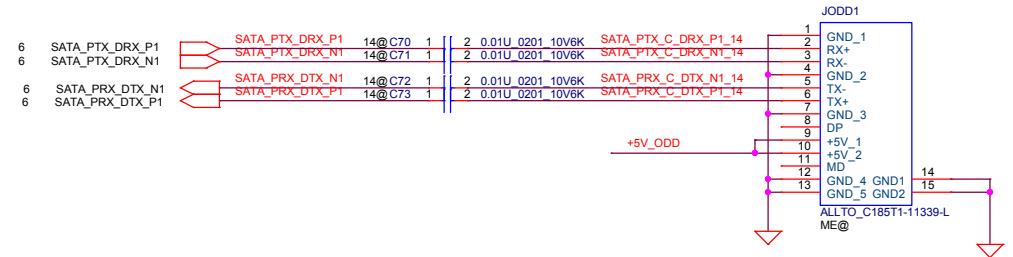
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SATA HDD Conn.

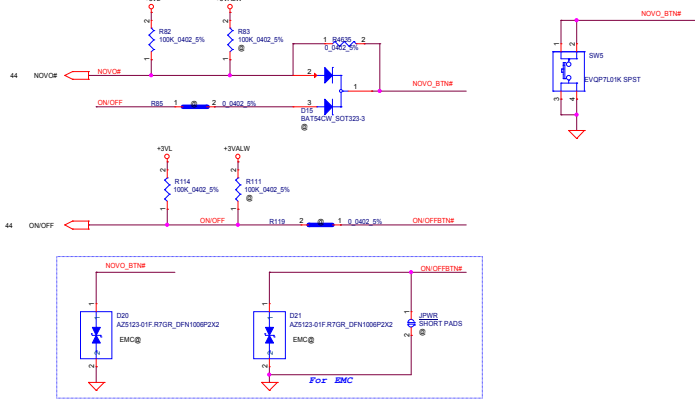


FOR 14" SATA ODD Conn.

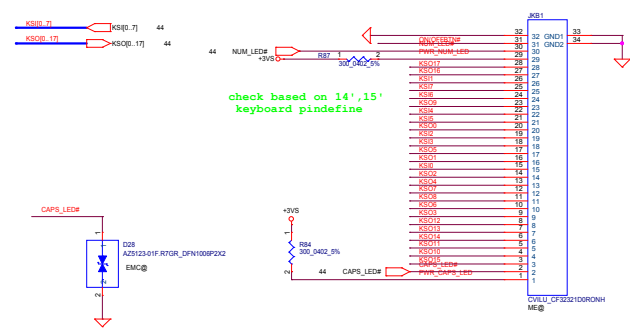


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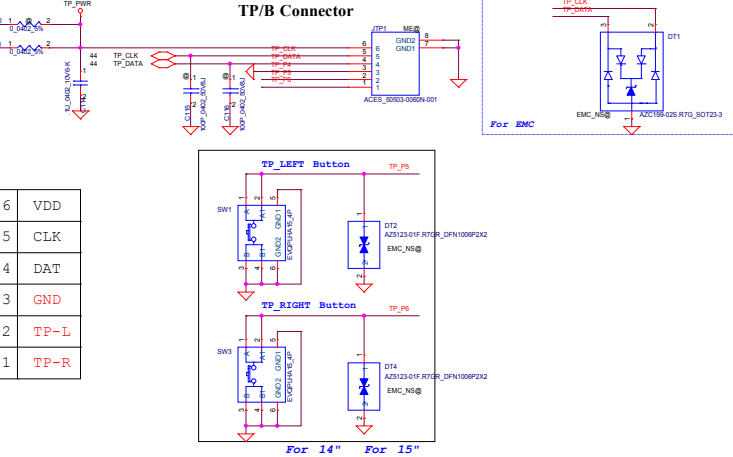
ON/OFF switch



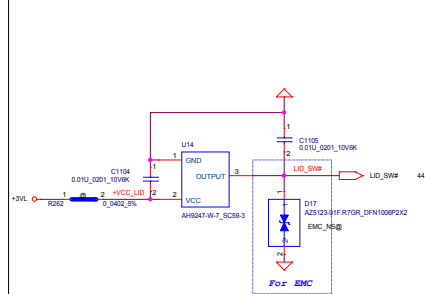
K/B Connector



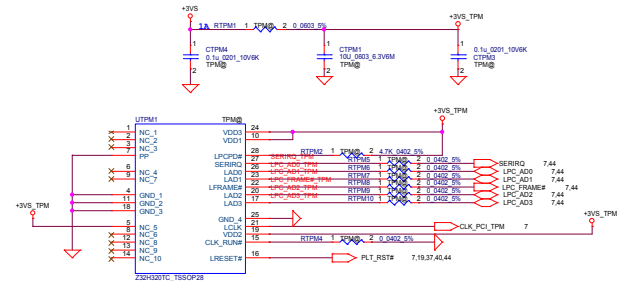
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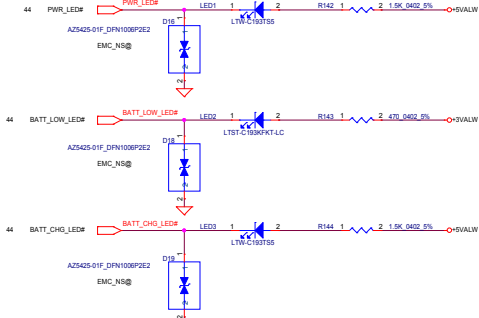
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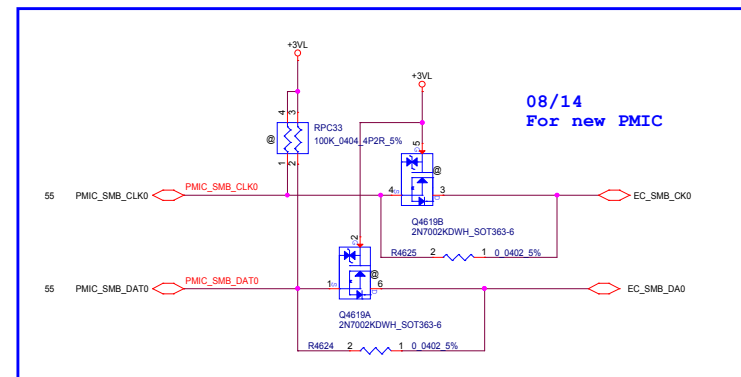
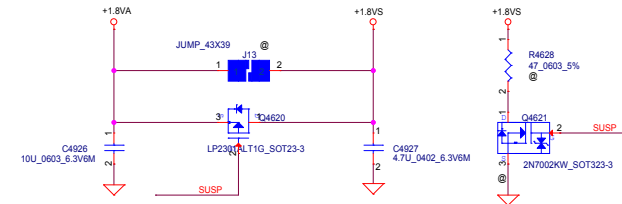
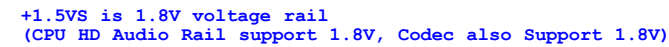
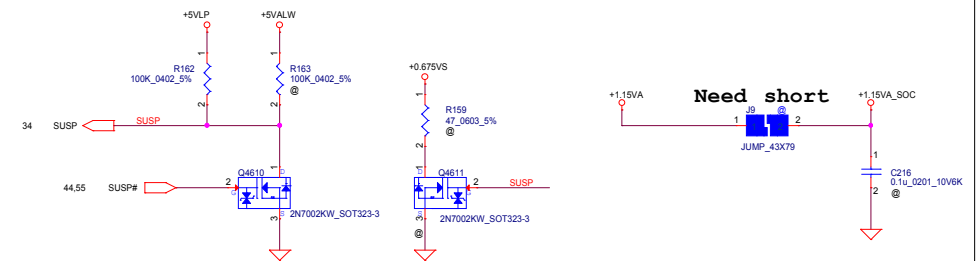
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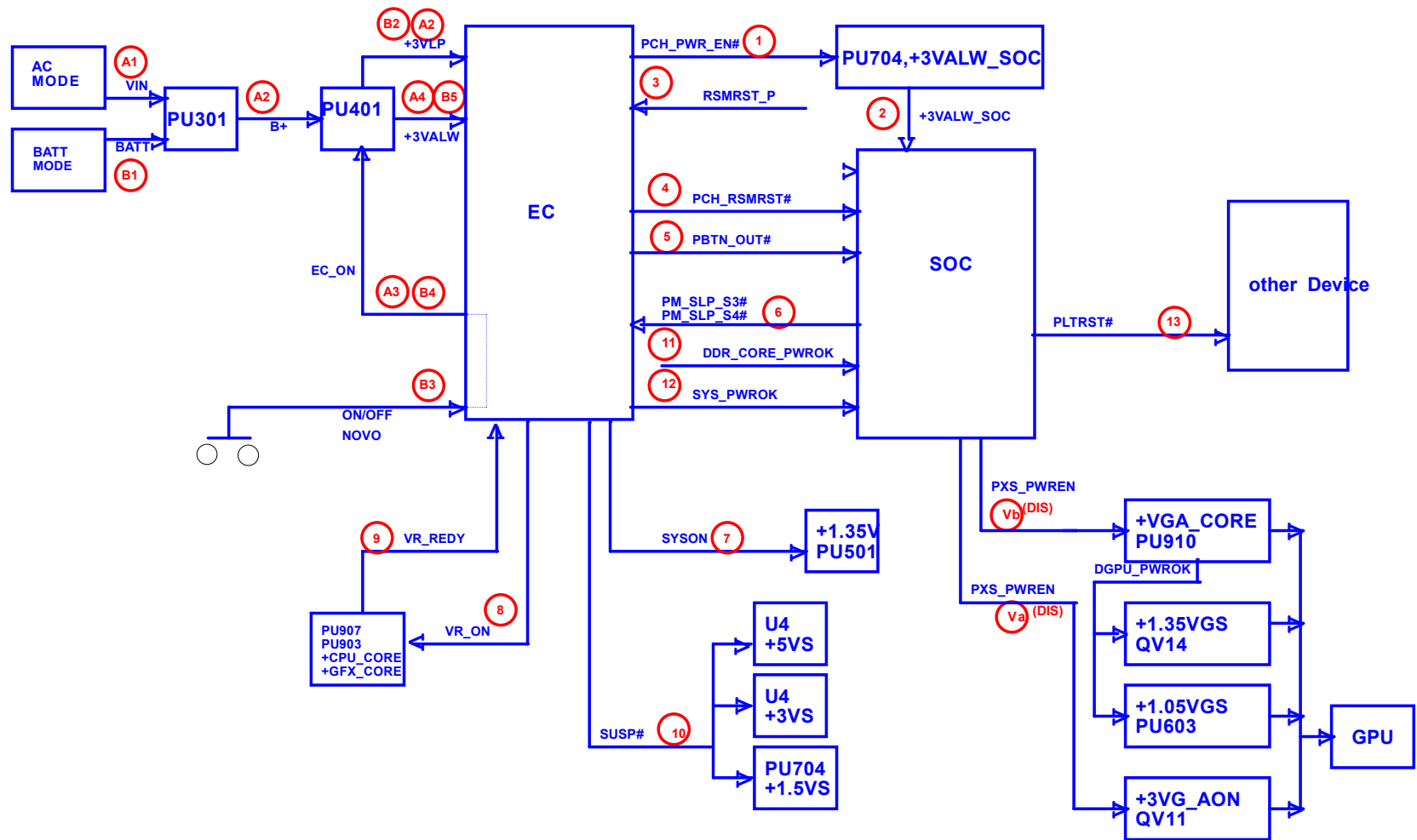



LED

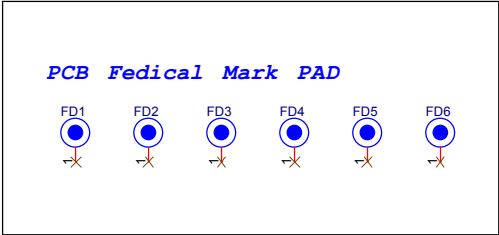
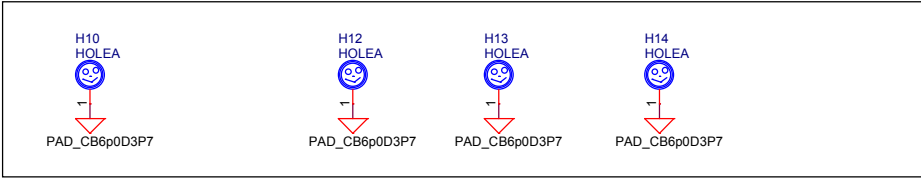
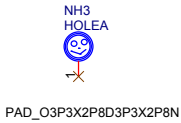
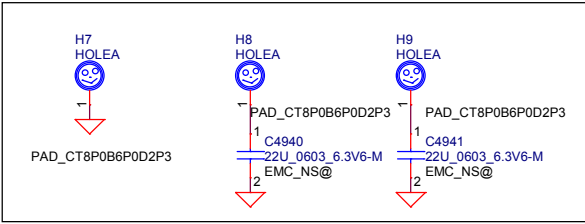
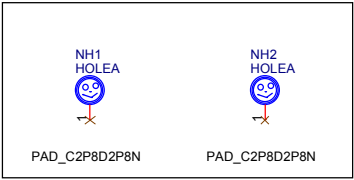
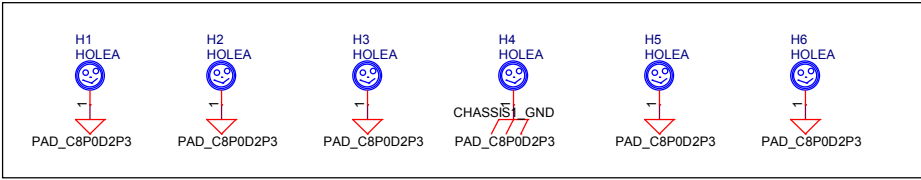



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