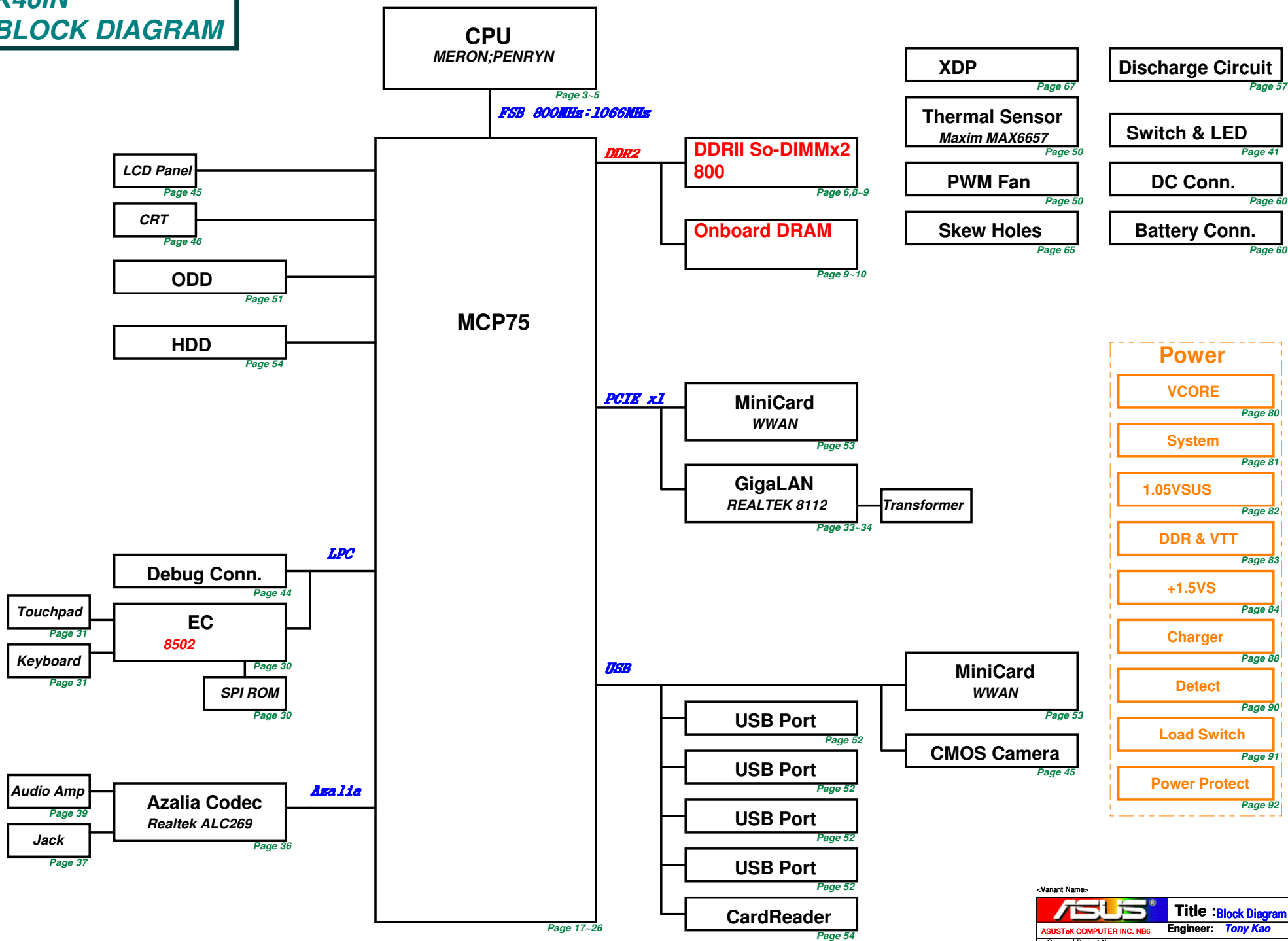
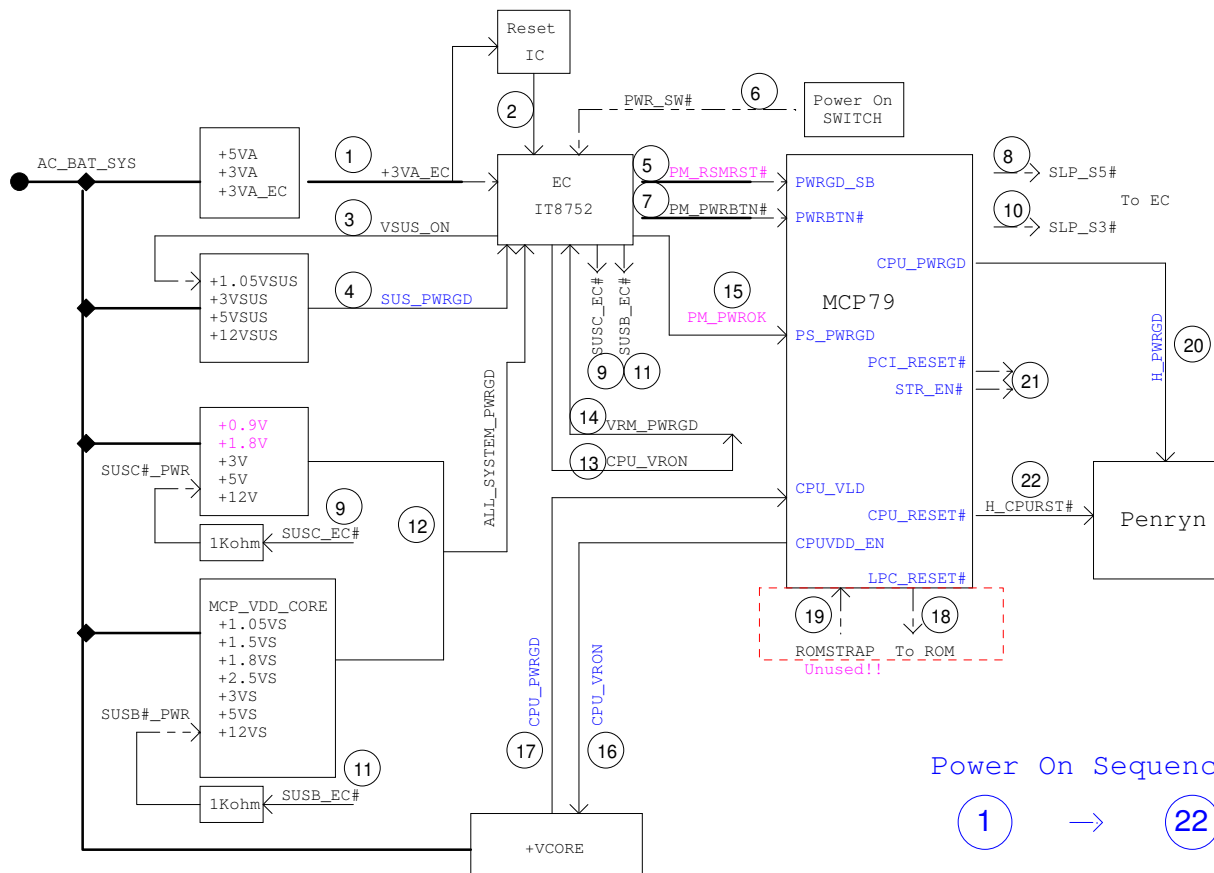


# K40IN BLOCK DIAGRAM





Power On Sequence

1 → 22

[17] H\_D#[63:0] << H\_D#[63:0]  
[17] H\_A#[35:3] << H\_A#[35:3]  
[17] H\_REQ#[4:0] << H\_REQ#[4:0]

Place beside CPU ball out

QC

+VCCP\_CPU

R0342  
510hm

+VCCP\_CPU

R343  
510hm

+VCCP\_CPU

R344  
510hm

BPM\_2[1]#

BPM\_2[2]#

QC  
DC

Comp 0,2: Zo=25 Ohm, trace length < 0.5"  
Comp 1,3: Zo=50 Ohm, trace length < 0.5"

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"  
Comp 1,3: Zo=55 Ohm, trace length < 0.5"

27.4OHM 1%  
54.9Ohm 1%  
27.4OHM 1%  
54.9Ohm 1%

2 54.9ohm 1%  
R342  
1  
H\_PWRGD\_XDP [67]

H\_DPWR# [17]

H\_DPWR# [17]

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Default Strapping When Not Used

XDP\_BPM#5 R3002 1 2 510hm  
XDP\_TDI R3003 1 2 510hm  
XDP\_TDO R3004 1 2 510hm  
XDP\_TMS R3005 1 2 510hm  
XDP\_DBR# R3006 1 2 1KOhm 1%  
XDP\_TCK R3007 1 2 510hm  
XDP\_TRST# R3008 1 2 649Ohm 1%

Place R3004 & R3006 for XDP function

Default Strapping When Not Used

QC

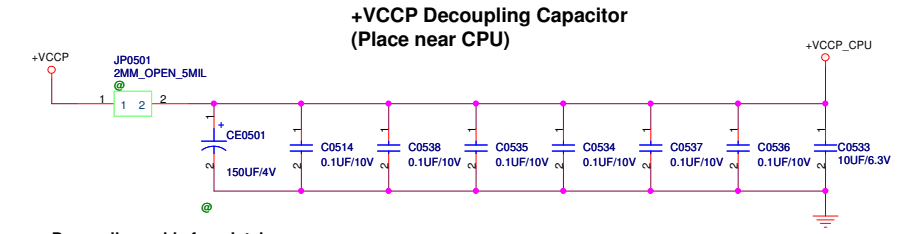
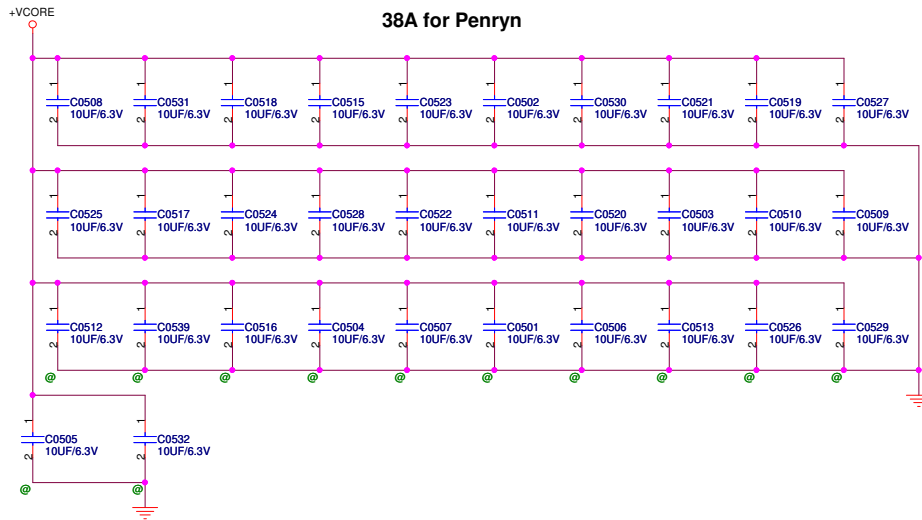
mount QC : /QC  
unmount QC : /QC@

<Variant Name>

ASUS		Title : Penryn CPU (1)	
Engineer:			
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009		Sheet	3 of 91

Pin B2 M4 N5 left as NC for QC Pin T2 V3 change to  
design (BPM\_2# [2] BPM\_2#[1] QC Thermal Diode  
BPM\_2[0]) detect (THRMDC\_2  
THRMDC\_2)





#### Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

#### +VCORE Mid-Frequency Capacitor

Intel: 22UF \*32

F3S: 10UF \*16

A7S: 10UF \*10 ....11/17

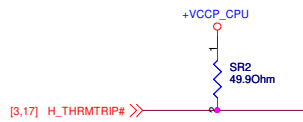
V1V: ?

#### +VCCP Decoupling Capacitor

Intel: 270UF \*1, 0.1UF \*6

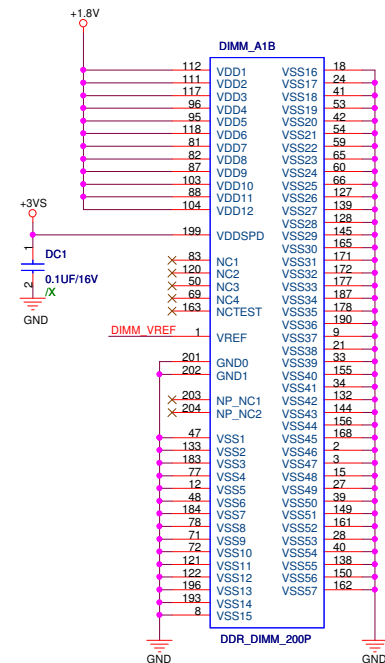
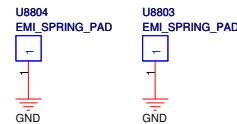
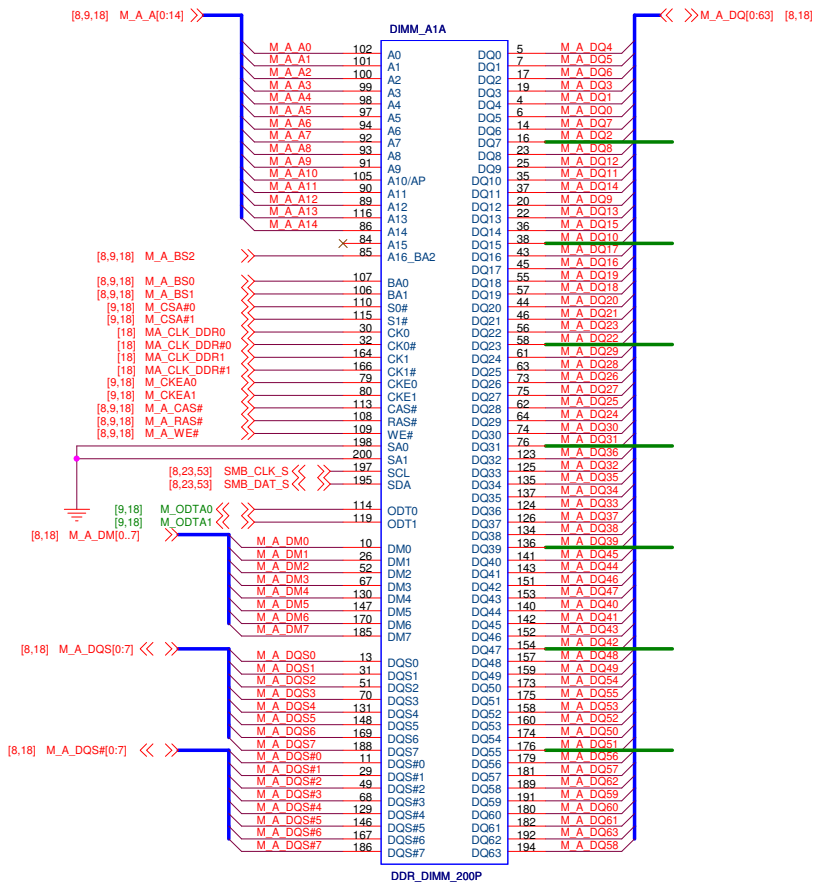
F3S: 100UF \*1, 0.1UF \*4

V1V: ?

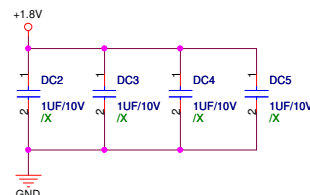


<Variant Name>

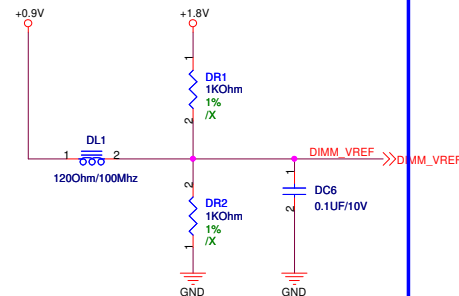
<b>ASUS</b>		<b>Title : CPU CAPS</b>	
		<b>Engineer:</b>	
Size Custom	Project Name		Rev 1.0
Date: Friday, February 13, 2009	Sheet	5 of	91



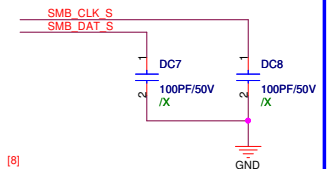
Power Cap Close to DIMM



DIMM\_VREF Close to DIMM



Close to DIMM



<Variant Name>

ASUS		Title :
ASUSTek COMPUTER INC. NB6		Engineer:
Size	Project Name	Rev
A3		1.0
Date:	Friday, February 13, 2009	Sheet 6 of 91







<< >>M\_A\_A[0:14] [6,8,18]

<< >>M\_B\_A[0:14] [10,18]

[6,18] M\_CKEA0 >> 470hm 3 14 RN0901C  
[6,18] M\_CKEA1 >> 470hm 8 9 RN0901H  
[6,8,18] M\_A\_CAS# >> 470hm 2 15 DRN10B  
[6,18] M\_CSA#0 >> 470hm 4 13 DRN16D  
M\_A\_A480hm 2 15 DRN11B  
[6,8,18] M\_A\_BS0 >> 470hm 6 11 DRN10F  
[6,8,18] M\_A\_WE# >> 470hm 7 10 DRN10G  
[6,18] M\_ODTA1 >> 470hm 8 9 DRN16H

[8,19] M\_CSA#2 >> 470hm 2 15 DRN12B  
[8,19] M\_CSA#3 >> 470hm 1 16 DRN10A  
[8,19] M\_ODTA2 >> 470hm 3 14 DRN10C  
[8,19] M\_ODTA3 >> 470hm 7 10 DRN16G  
[8,19] M\_CKEA2 >> 470hm 5 12 RN0901E  
[8,19] M\_CKEA3 >> 470hm 7 10 RN0901G  
470hm 4 13 DRN11D  
470hm 1 16 DRN16A

M\_A\_A470hm 4 13 DRN12D  
M\_A\_A470hm 3 14 DRN12C  
[6,8,18] M\_A\_BS1 >> 470hm 6 11 DRN11F  
M\_A\_A470hm 5 12 DRN10E  
[6,8,18] M\_A\_RAS# >> 470hm 5 12 DRN11E  
M\_A\_A470hm 8 9 DRN11H  
M\_A\_A470hm 7 10 DRN11G  
M\_A\_A470hm 8 9 DRN10H

M\_A\_A470hm 5 12 DRN12E  
M\_A\_A470hm 6 11 DRN12F  
[6,8,18] M\_A\_BS2 >> 470hm 6 11 RN0901F  
M\_A\_A470hm 2 15 RN0901B  
M\_A\_A470hm 8 9 DRN12H  
M\_A\_A470hm 1 16 DRN12A  
M\_A\_A470hm 1 16 RN0901A  
M\_A\_A470hm 7 10 DRN12G

[6,18] M\_CSA#1 >> 470hm 5 12 DRN16E  
[6,18] M\_ODTA0 >> 470hm 6 11 DRN16F  
M\_A\_A14 470hm 4 13 RN0901D  
[18] M\_ODTB1 >> 470hm 1 16 DRN11A  
[18] M\_CSB#1 >> 470hm 2 15 DRN16B  
M\_B\_A14 470hm 3 14 DRN16C  
M\_B\_A14 470hm 3 14 DRN11C

M\_B\_A4 470hm 6 11 DRN17F  
M\_B\_A1 470hm 4 13 DRN17D  
M\_B\_A10 470hm 7 10 DRN15G  
[10,18] M\_B\_BS0 >> 470hm 1 16 DRN17A  
M\_B\_A8 470hm 3 14 DRN17C  
M\_B\_A5 470hm 5 12 DRN14C  
M\_B\_A3 470hm 6 11 DRN14E  
M\_B\_A3 470hm 6 11 DRN14F

M\_B\_A9 470hm 8 9 DRN17H  
[18] M\_CKEB1 >> 470hm 7 10 DRN14G  
M\_B\_A11 470hm 2 15 DRN14B  
M\_B\_A6 470hm 7 10 DRN17G  
[10,18] M\_CKEB0 >> 470hm 8 9 DRN14H  
M\_B\_A7 470hm 4 13 DRN14D  
[10,18] M\_B\_BS2 >> 470hm 6 11 DRN15F  
M\_B\_A12 470hm 1 16 DRN14A

[10,18] M\_CSB#0 >> 470hm 5 12 DRN15E  
[10,18] M\_ODTB0 >> 470hm 3 14 DRN15C  
M\_B\_A13 470hm 8 9 DRN15H  
[10,18] M\_B\_RAS# >> 470hm 2 15 DRN15B  
M\_B\_A2 470hm 5 12 DRN17E  
[10,18] M\_B\_BS1 >> 470hm 2 15 DRN17B  
[10,18] M\_B\_CAS# >> 470hm 1 16 DRN15A  
[10,18] M\_B\_WE# >> 470hm 4 13 DRN15D

+0.9V

DC14  
0.1UF/10V

DC16  
0.1UF/10V

DC11  
0.1UF/10V

DC12  
0.1UF/10V

DC13  
0.1UF/10V

DC15  
0.1UF/10V

DC17  
0.1UF/10V

DC18  
0.1UF/10V

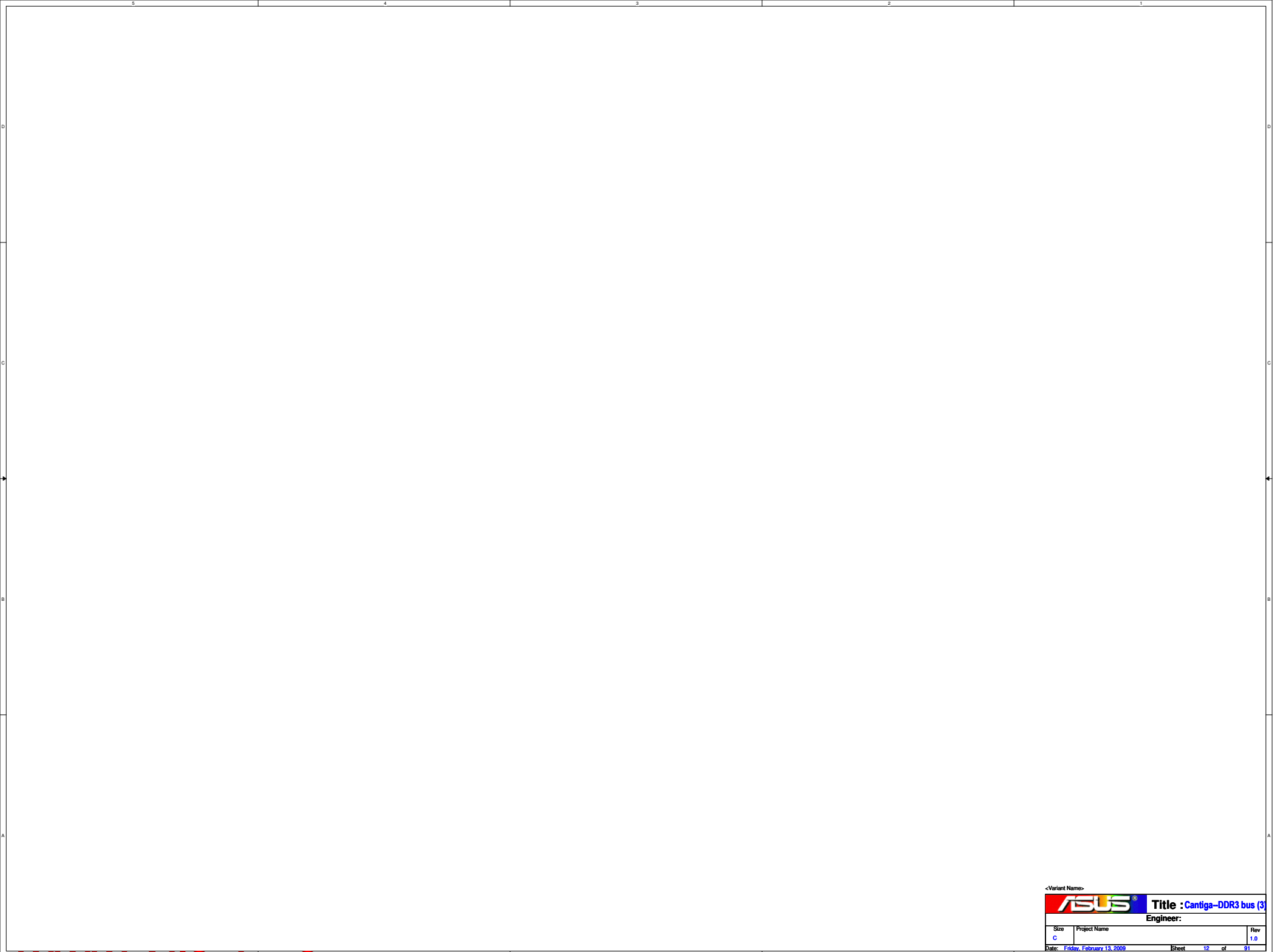
GND


<Variant Name>

<b>ASUS</b>		<b>Title DDR3 termination</b>	
ASUSTek COMPUTER INC. NB6		Engineer: <b>Vincent Chung</b>	
Size	Project Name	Rev	
Custom	<b>G71V</b>	1.0	
Date: Monday, February 16, 2009		Sheet	9 of 91








<Variant Name>		
		Title : Cantiga-DDR3 bus (3)
Engineer:		
Size	Project Name	Rev
C		1.0
Date: Friday, February 13, 2009		
Sheet 12 of 91		




<Variant Name>

**Title : Cantiga-POWER (4)**

Engineer:

Size	Project Name	Rev
C		1.0
Date: Friday, February 13, 2009		Sheet 13 of 91

<Variant Name>

		<b>Title :</b> Cantiga-POWER(5)	
<b>Engineer:</b>			
Size Custom	Project Name		Rev 1.0
Date: Friday, February 13, 2009	Sheet	14 of	91

54321

D

C

B

A

<Variant Name>

ASUS®

Title : Cantiga-GND

Engineer:

Size  
B

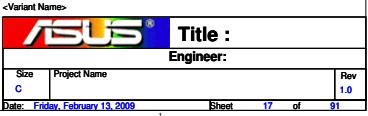
Project Name

Rev  
1.0

Date: Friday, February 13, 2009Sheet 15 of 91

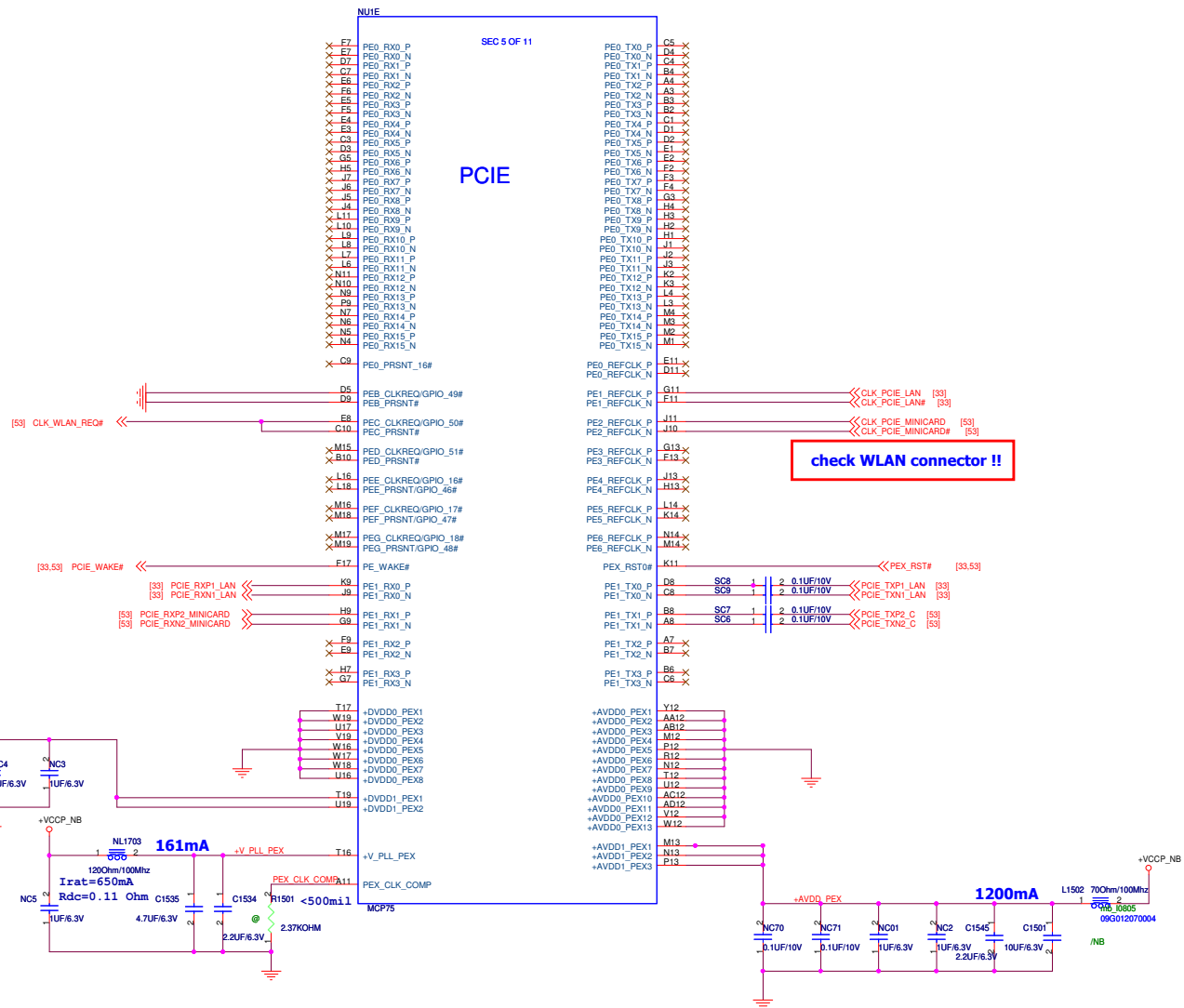


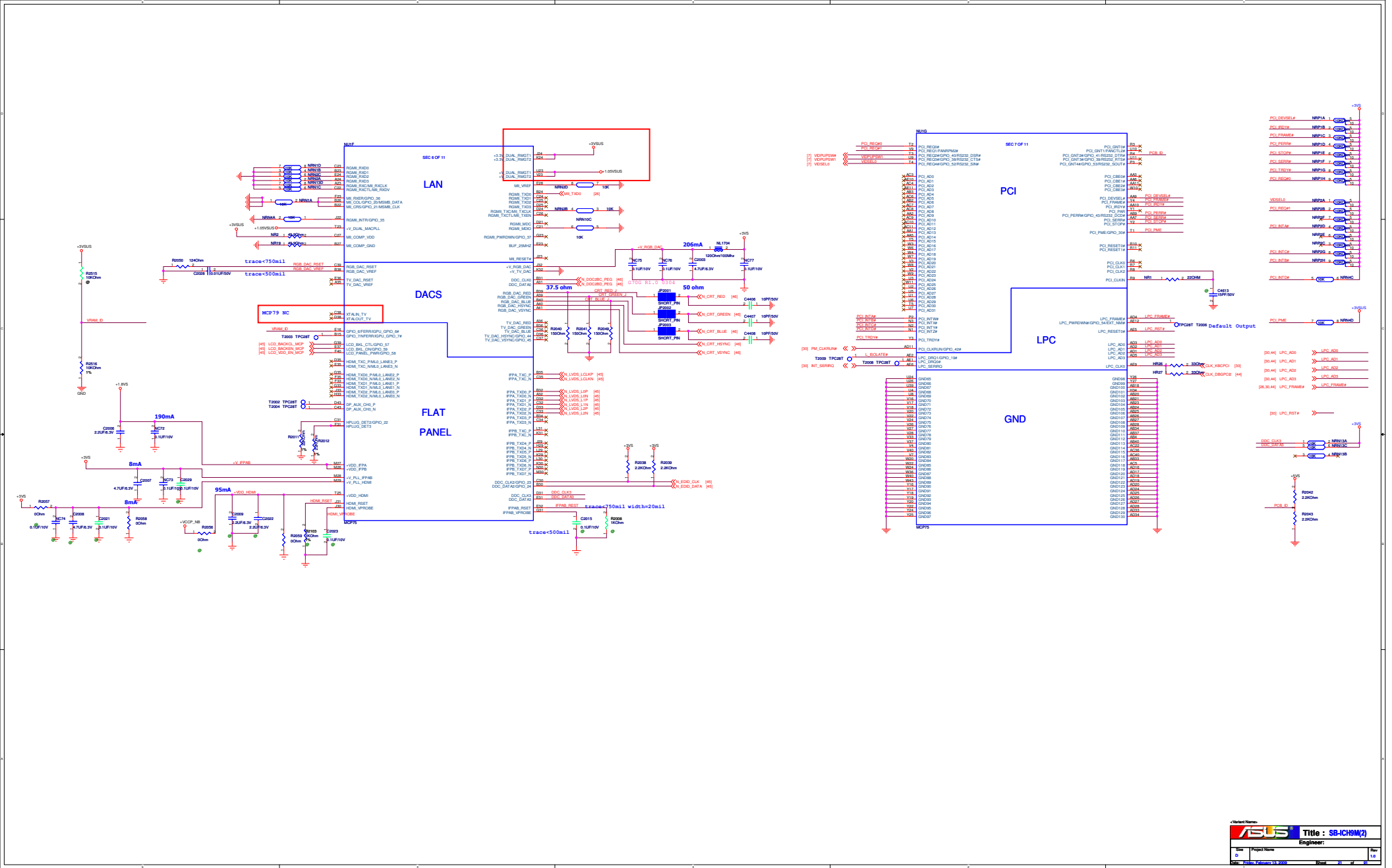




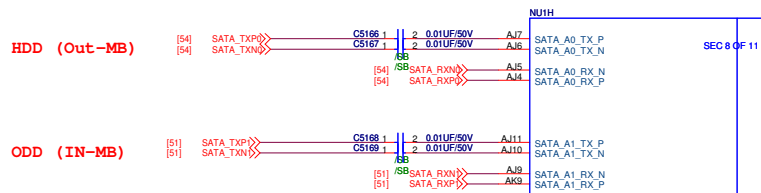








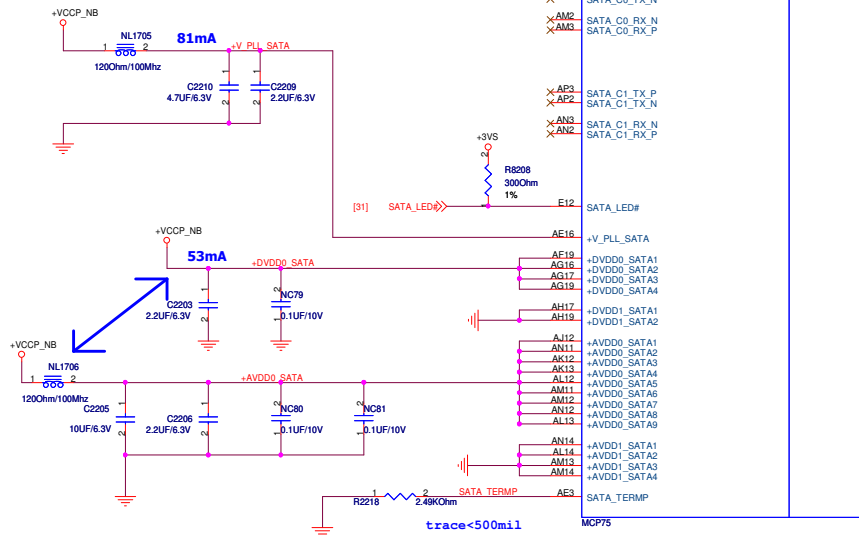
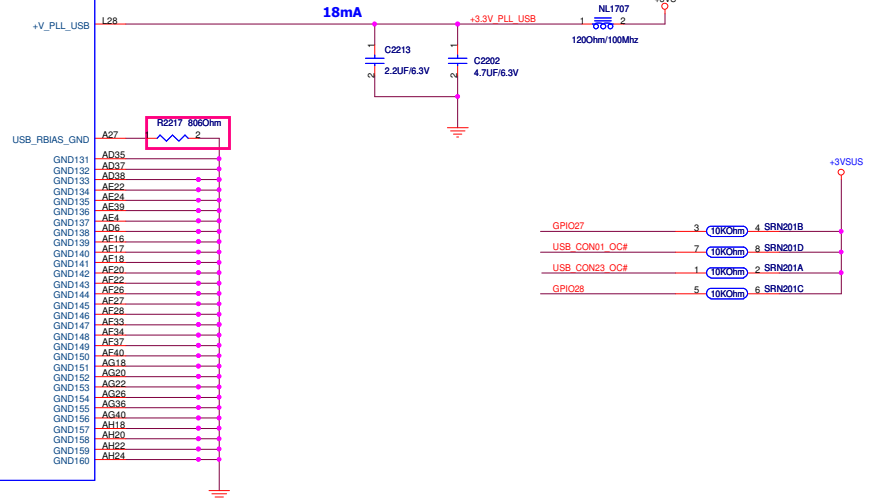
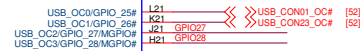
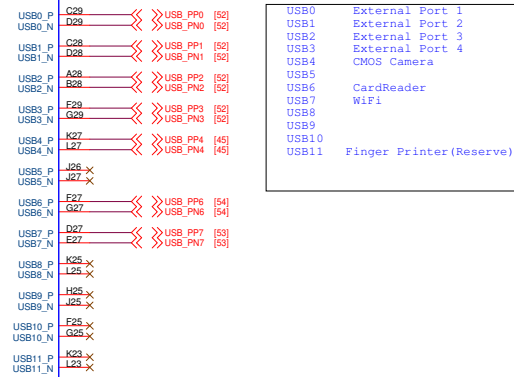
Check connector pin definition !!



SATA

USB

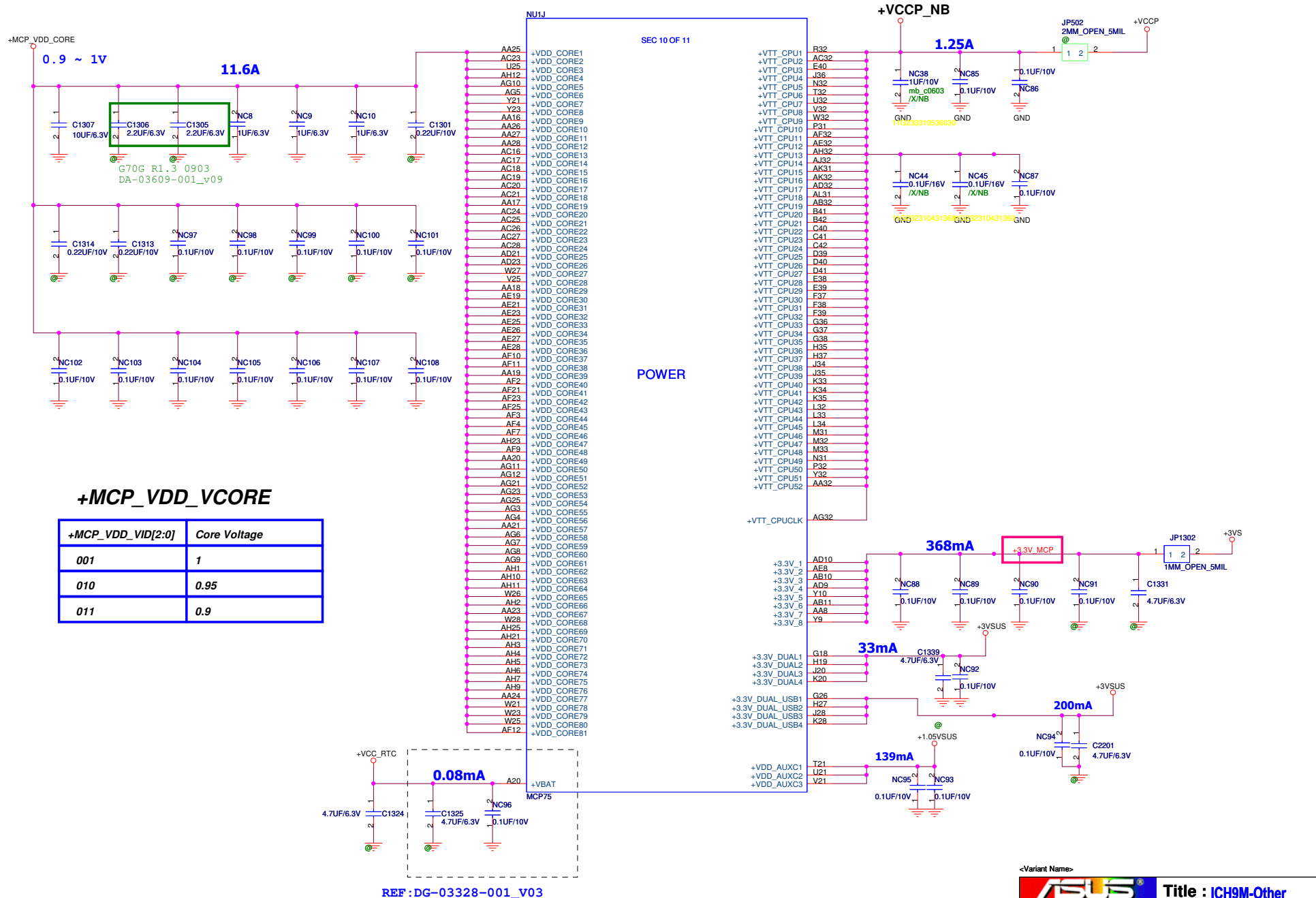
Check connector pin definition !!



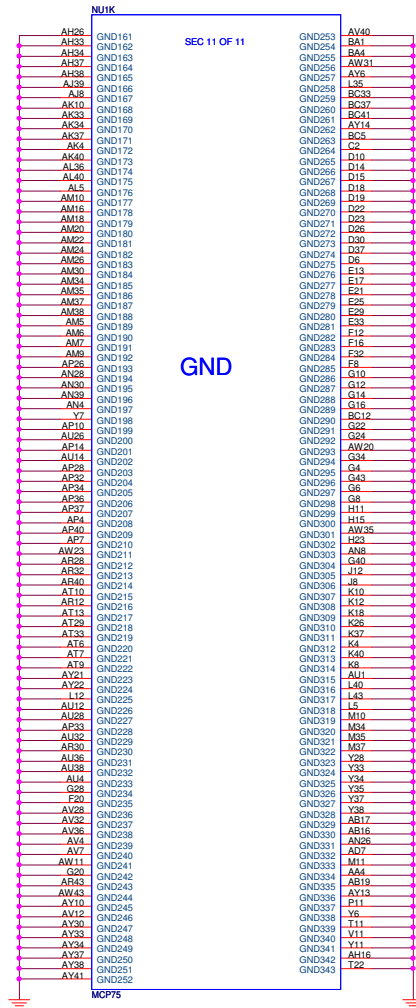
<Variant Name>

<b>ASUS</b>		<b>Title : SB-ICH9M(3)</b>	
		<b>Engineer:</b>	
Size	Project Name		Rev
C			1.0
Date: Friday, February 13, 2009		Sheet	22 of 91









<Variant Name>

		<b>Title : SPI ROM</b>	
<b>Engineer:</b>			
Size	Project Name	Rev	
C		1.0	
Date: Friday, February 13, 2009		Sheet	25 of 91

[6,8,23,53] SCL\_3A << >> SMB\_CLK\_S [6,8,23,53]

[6,8,23,53] SDA\_3A << >> SMB\_DAT\_S [6,8,23,53]

#### Onboard DRAM ID

GPIO_6	GPIO_11	Vendor
0	0	Qimonda HYB18T512161B2F-25
0	1	Samsung K4N51163Q2-NC25
1	0	Hynix HY5PS121621CFP-25

#### HDA\_SYNC STRAP (BUF\_SIO\_CLK)

0	14.318MHz (default)
1	24MHz

#### RGMII\_TXD0

0	MII
1	RGMII

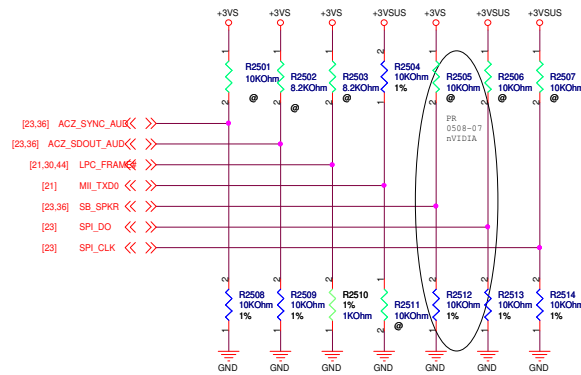
#### SPKR

0	User mode boot Init table
1	Safe mode boot Init table

#### Base on EC

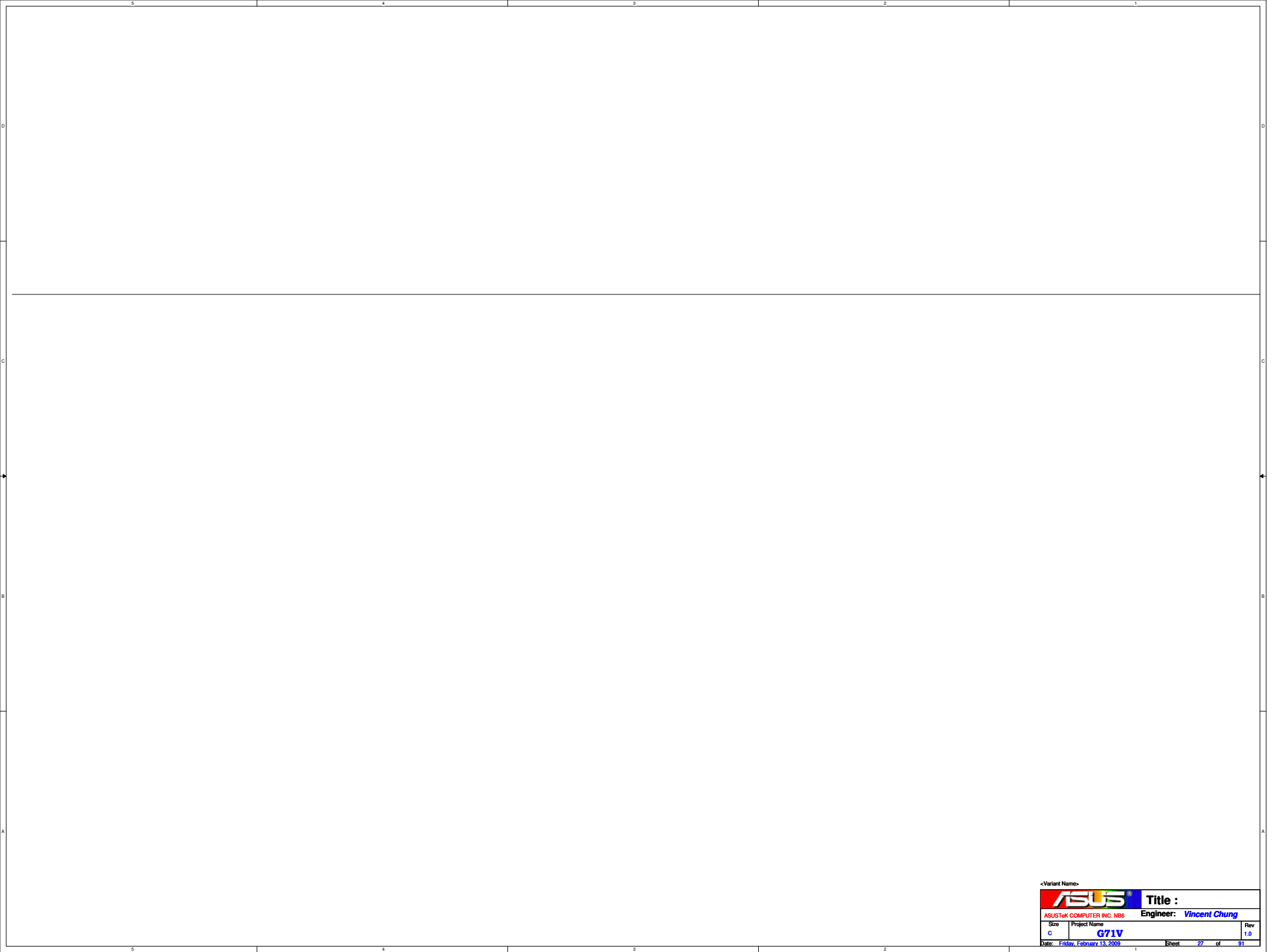
HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_DO	SPI_CLK	FUNCTION
0	0	31MHz
0	1	42MHz
1	0	25MHz
1	1	1MHz




<Variant Name>

ASUS		Title :
Engineer:		
Size	Project Name	Rev
C		1.0
Date: Monday, February 16, 2009		Sheet 26 of 31



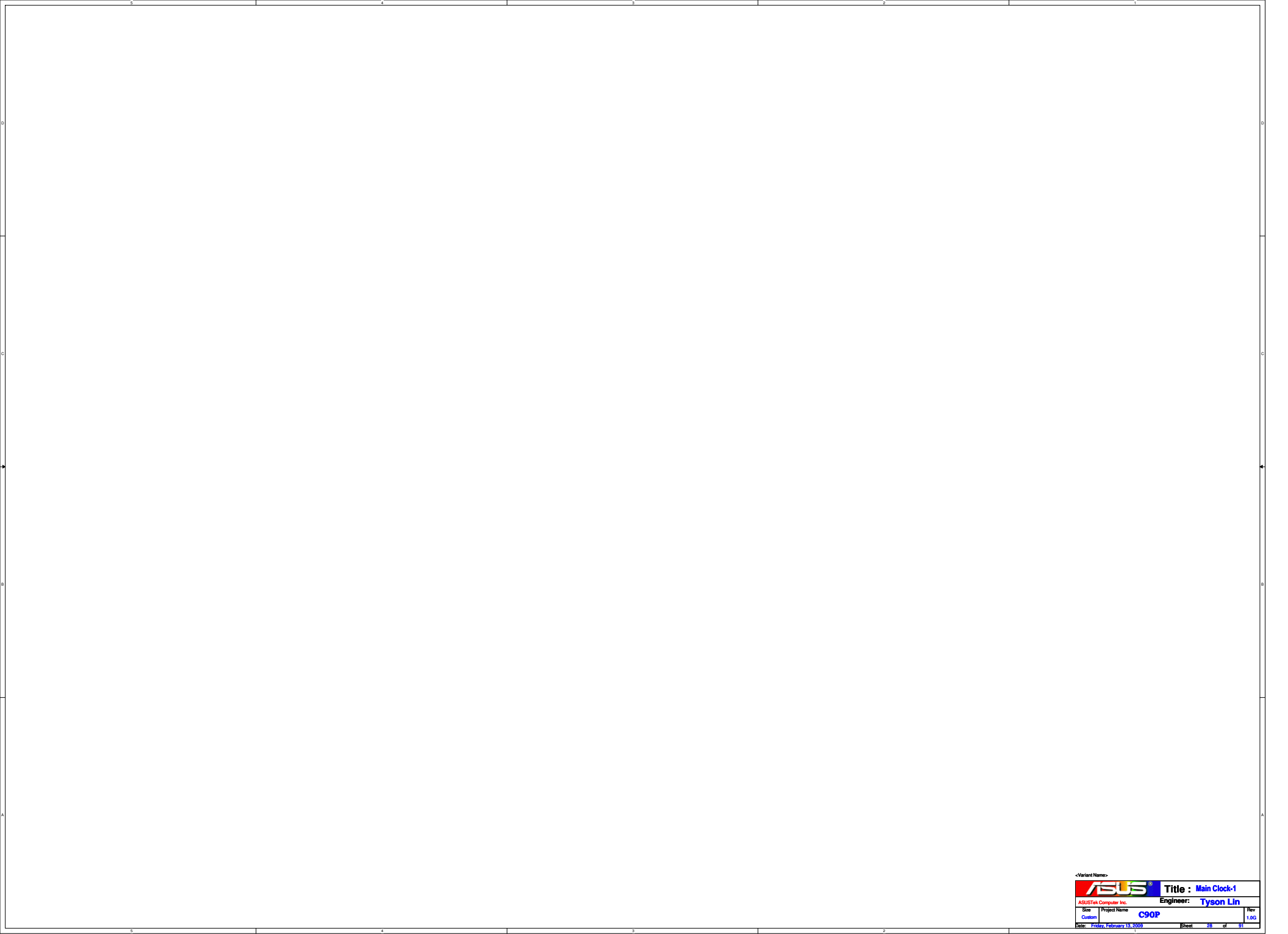
<Variant Name>

  
ASUSTeK COMPUTER INC. NB6

Title :  
Engineer: *Vincent Chung*

Size	Project Name	Rev
C	<b>G71V</b>	1.0

Date: *Friday, February 13, 2009* Sheet *27* of *91*



<Variant Name>

**ASUS**

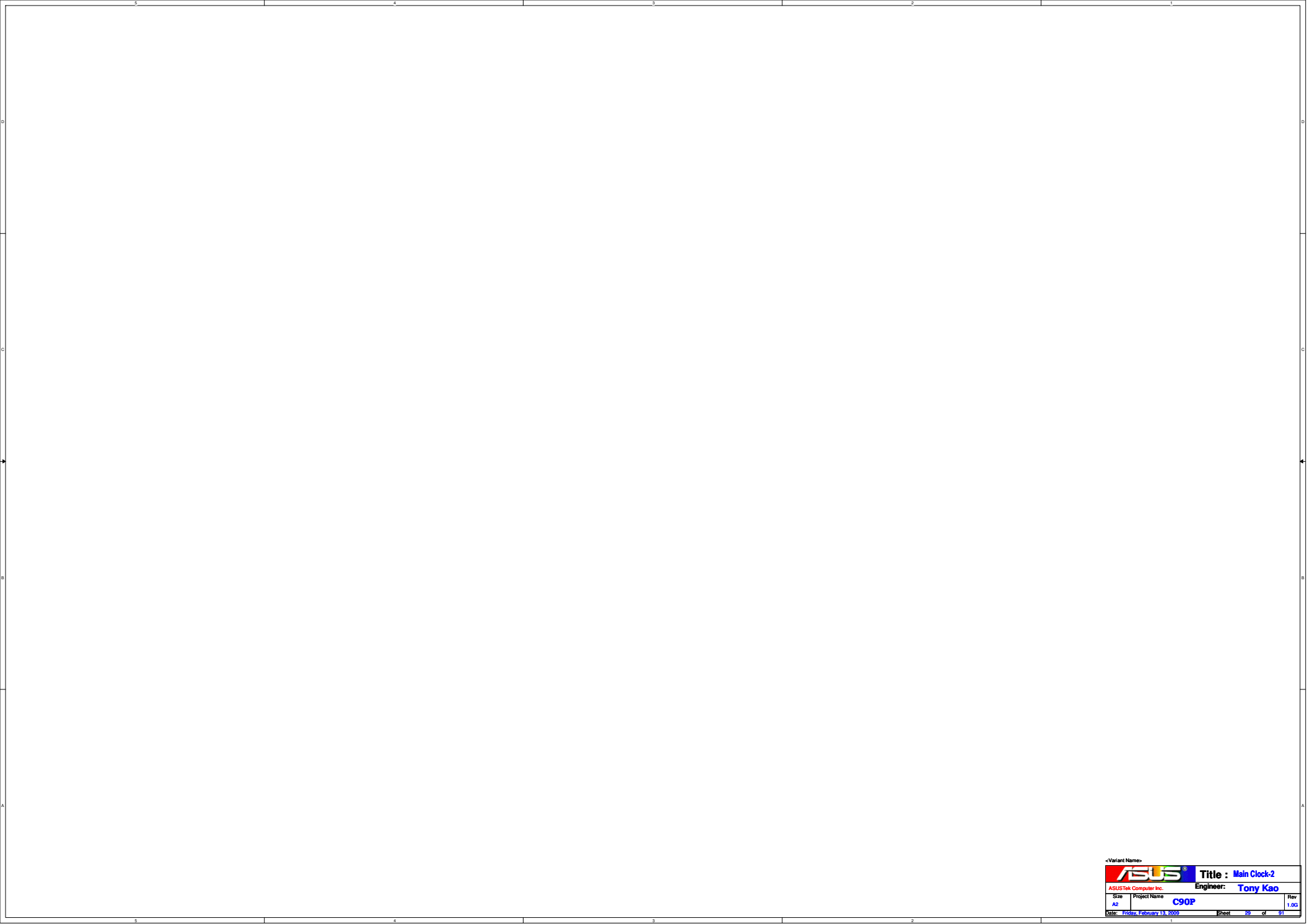
Title : **Main Clock-1**

ASUSTek Computer Inc.

Engineer: **Tyson Lin**

Size	Project Name	Rev
Custom	<b>C90P</b>	1.00

Title: **Friday, February 13, 2009**Sheet **26** of **31**



<Variant Name>

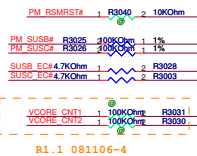
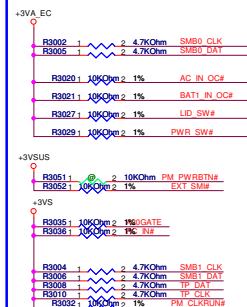
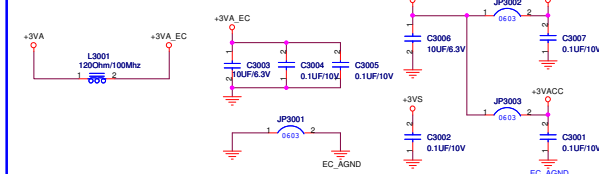
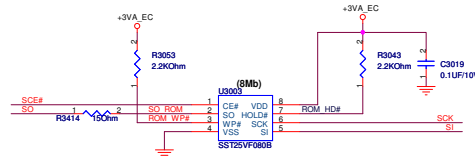
**ASUS**<sup>®</sup>

**Title :** Main Clock-2

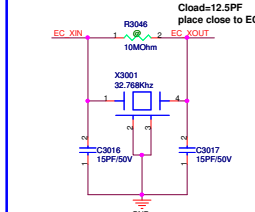
ASUSTek Computer Inc.

**Engineer:** Tony Kao

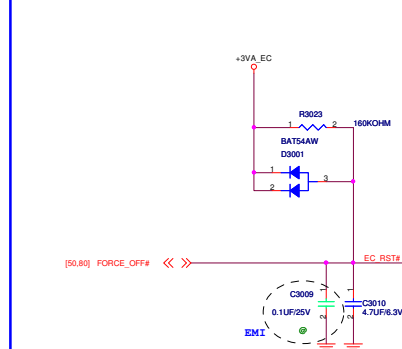
Size	Project Name	Rev
A2	C90P	1.00
Date: Friday, February 13, 2009		Sheet 29 of 91



Note:  
EXT\_SMI#, EXT\_SCI#, PU power plane  
depend on ICH9 GPIO.



Note:  
Clod=12.5PF  
place close to E



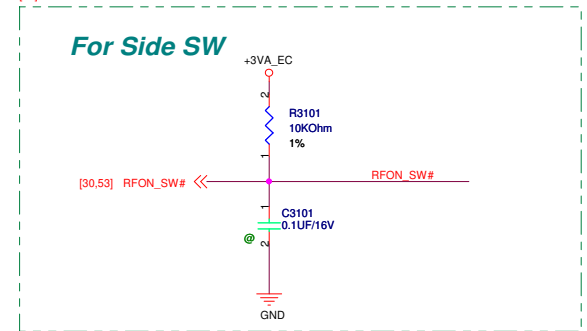
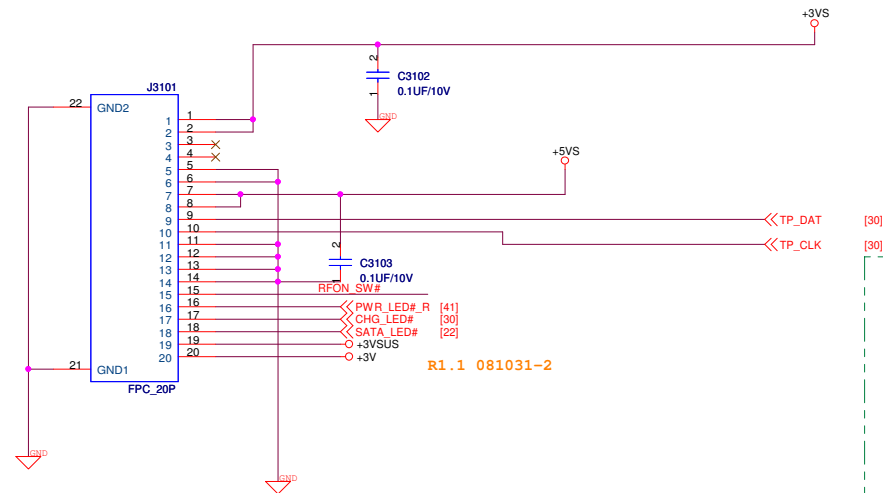
**I/O Base Address**  
Note: It can be programmable by EC firmware

**Share Memory**  
Note: It can be programmable by EC firmware

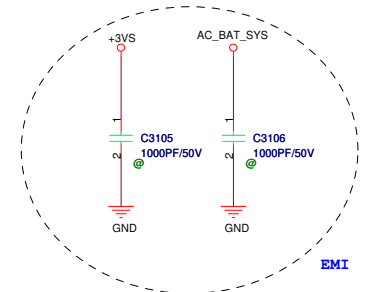
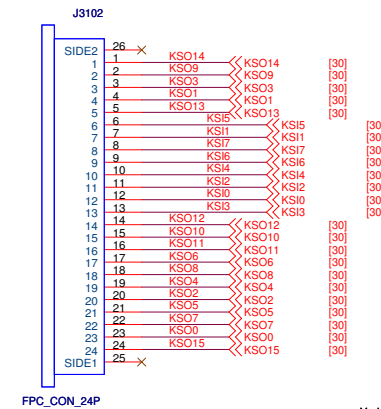
**PP Enable**  
Note: Default Int. Pull-Low

```
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SLPSWDR_ACK
```

## TouchPad & FingerPrint




## Keyboard Connector



### For Thermal Control Method

Remove redundant components

<Variant Name>



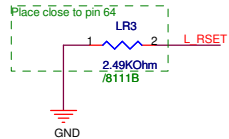
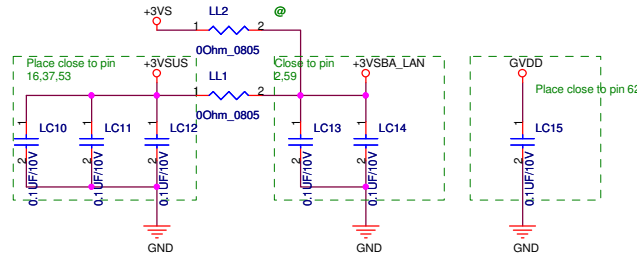
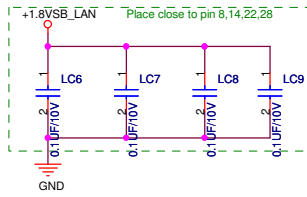
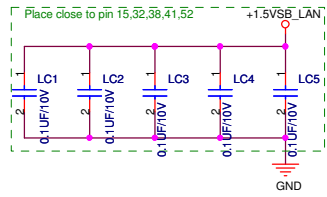
ASUSTeK COMPUTER INC. NB1

Title : RST\_Reset Circuit

Engineer: Vincent Chung

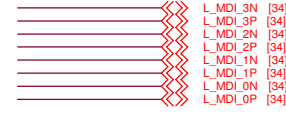
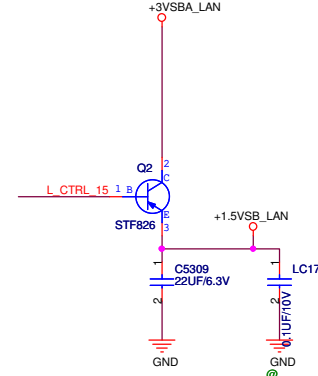
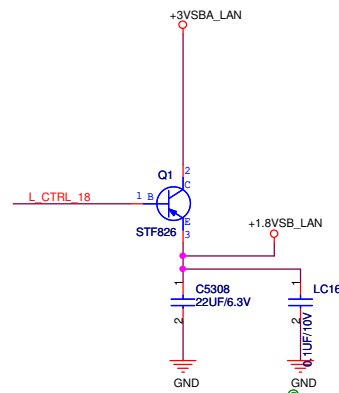
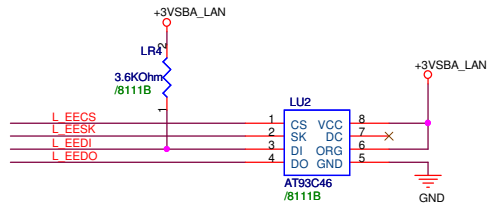
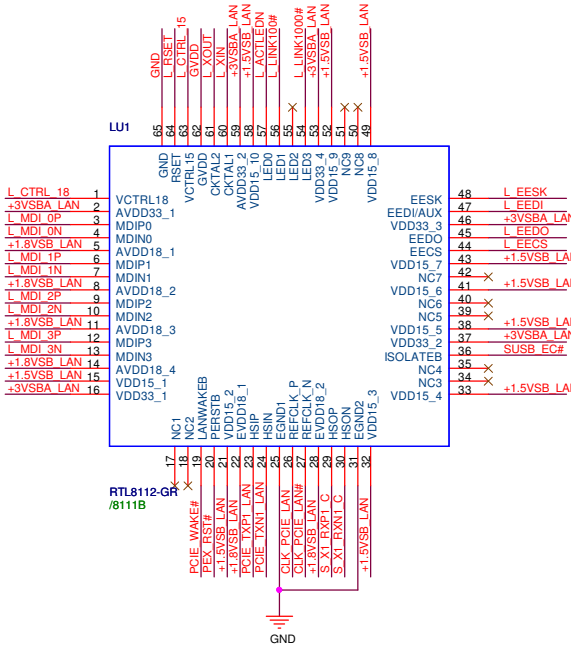
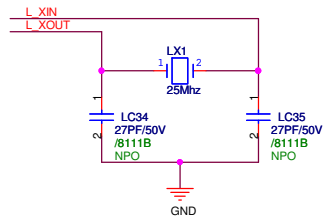
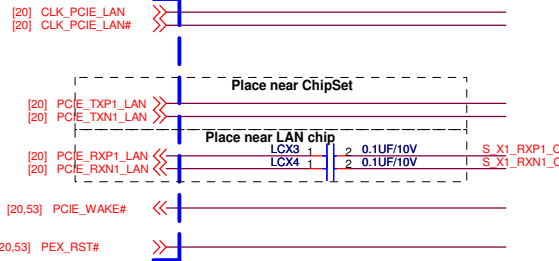
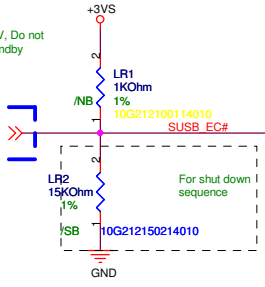
Size	Project Name	Rev
Custom	G71V	1.0
Date: Friday, February 13, 2009		Sheet 32 of 91

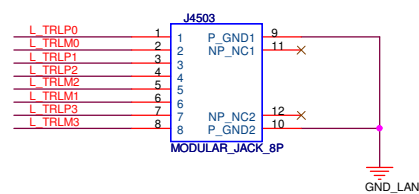
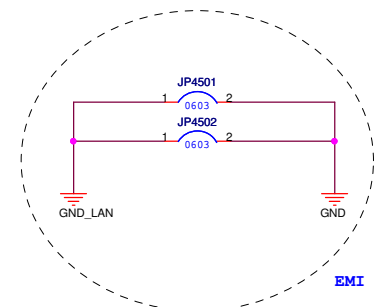
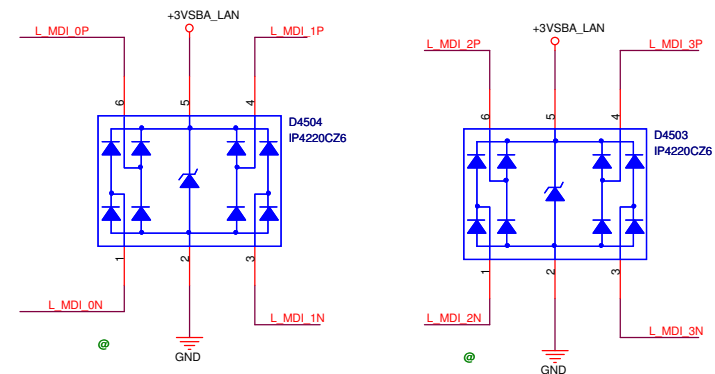
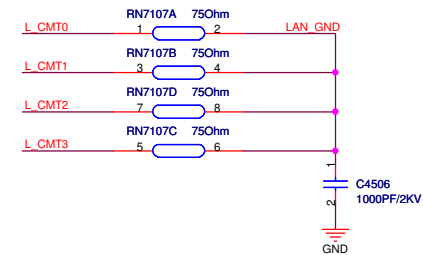
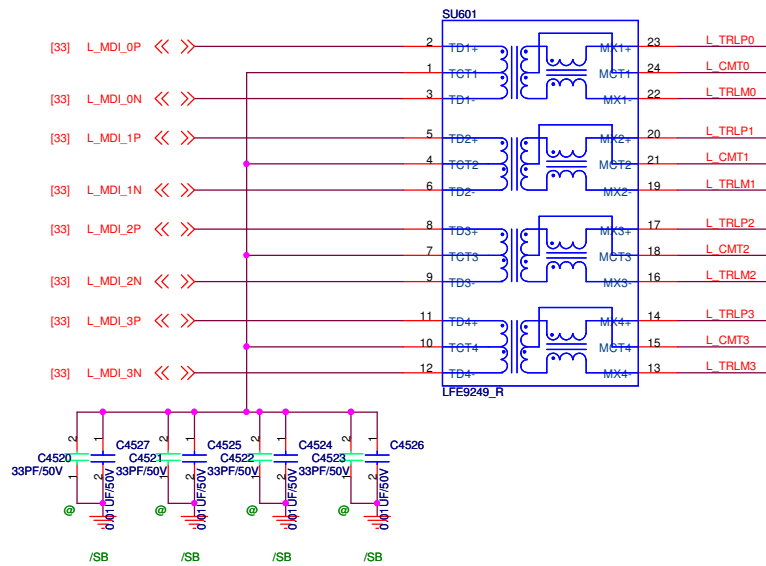




Pull-up by +3V. Do not pull-up by Standby power

[30,57,80,88] SUSB\_EC#






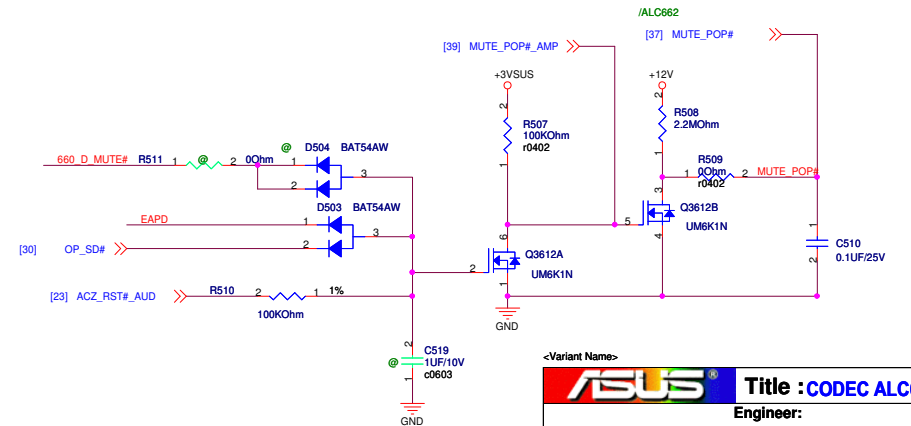
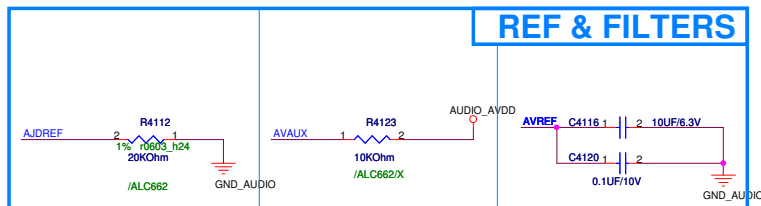
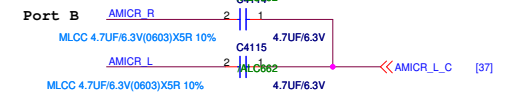
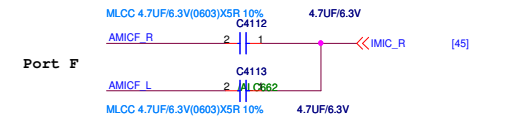
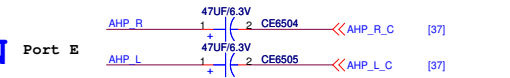
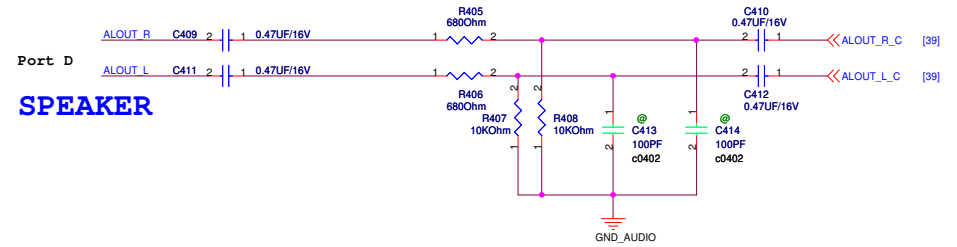
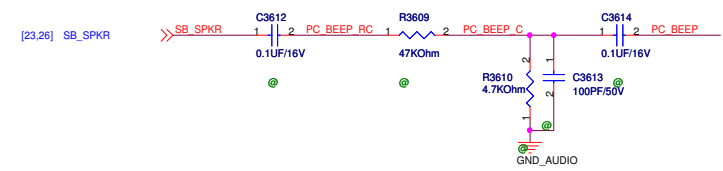
<Variant Name>

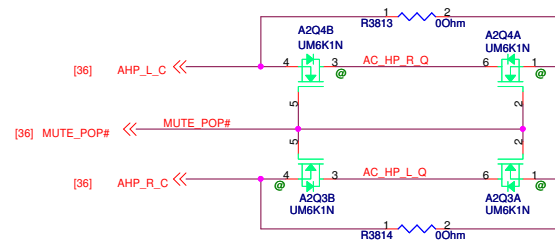
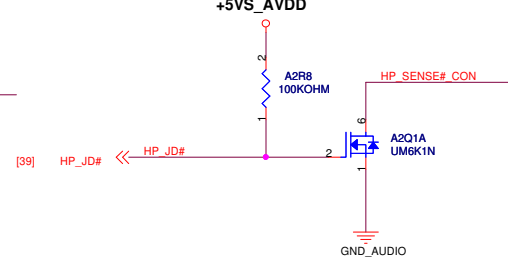
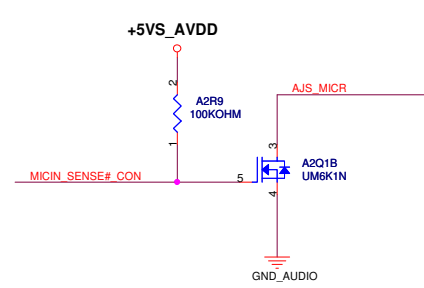
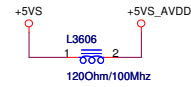
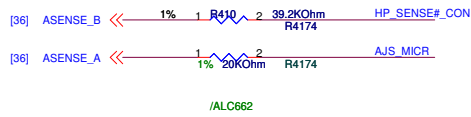
<b>ASUS</b>		<b>Title : 10</b>
<b>ASUSTeK COMPUTER INC</b>		<b>Engineer:</b>
Size Custom	Project Name	Rev 1.0
Date: Friday, February 13, 2009		Sheet 34 of 91



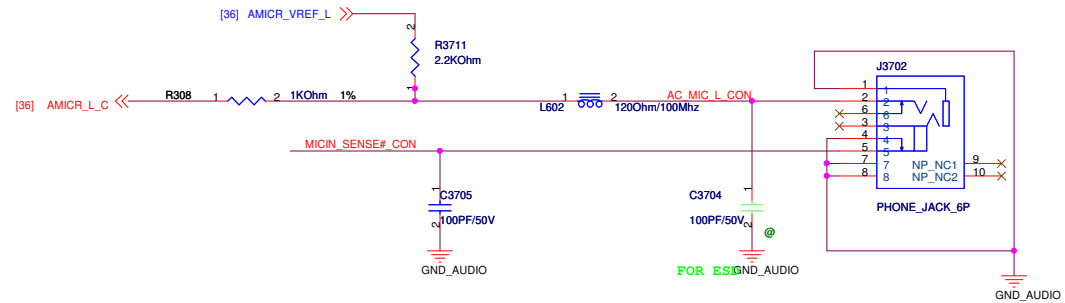
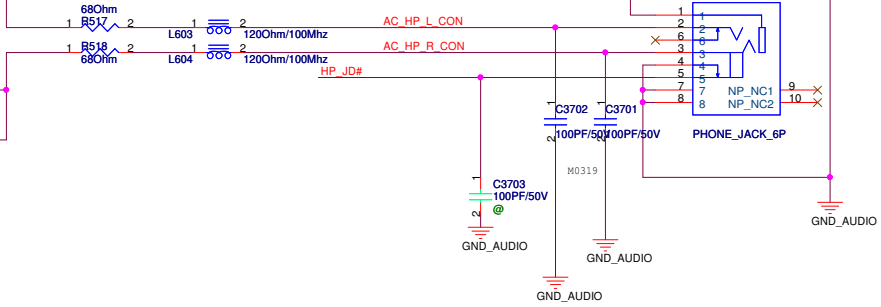
<Variant Name>

		Title : <b>MDC</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Vincent Chung</i>	
Size	Project Name		Rev
Custom	<b>G71V</b>		1.0
Date: <i>Friday, February 13, 2009</i>		Sheet	35 of 91



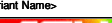


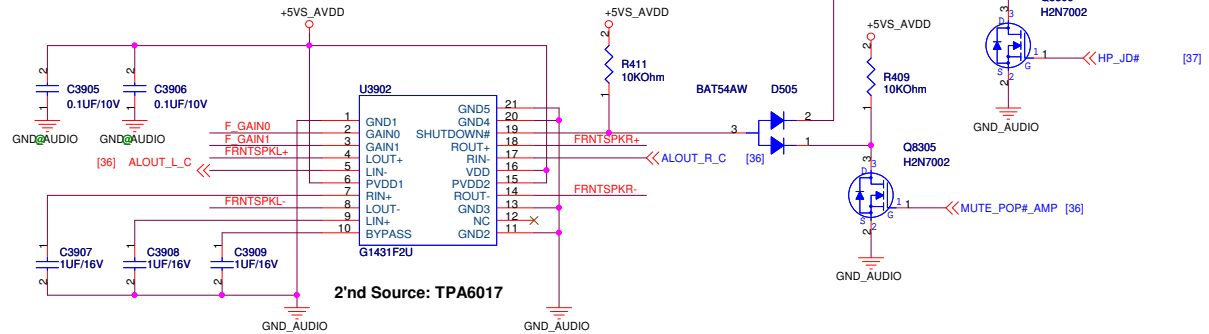
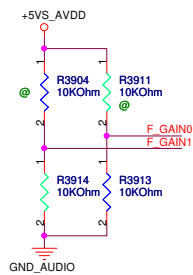
## HP CONN



## External MIC CONN

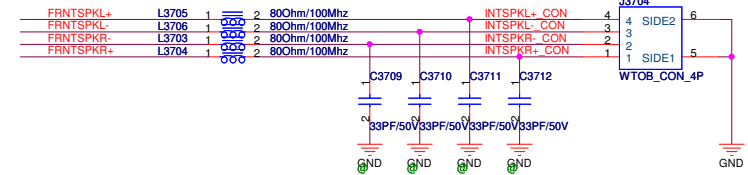
Title : AUD_Amp & Jack		
Engineer:		
Size	Project Name	Rev
Custom		1.0
Date:	Friday, February 13, 2009	Sheet 37 of 91

		<b>Title :</b> AUD_FM2010	
<b>ASUSTek COMPUTER INC. NB1</b>		<b>Engineer:</b> John Hung	
Size Custom	Project Name  N2Sv	Rev 1.0	
Date: Friday, February 13, 2009		Sheet 38	of 91



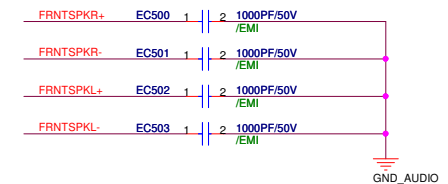
2'nd Source: TPA6017

## SPEAKER CONNECTOR (2W)



GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB


## 2.0G-G71G-EMI



<Variant Name>

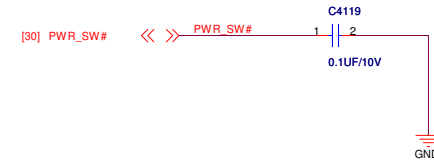
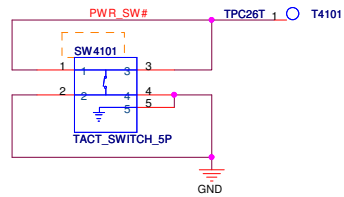
<b>ASUS</b>		<b>Title : AUD_Woofers &amp; Front</b>	
		<b>Engineer:</b>	
Size	Project Name		Rev
Custom			1.0
Date:	Friday, February 13, 2009	Sheet	39 of 91

<Variant Name>

		<b>Title :</b> CB_R5C833
<b>Engineer:</b>		
Size Custom	Project Name	Rev 1.0
Date: Friday, February 13, 2009	Sheet	40 of 91

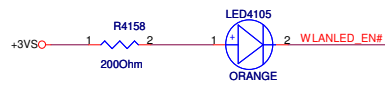


## SWITCH BUTTON

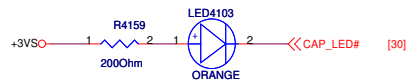


## LED

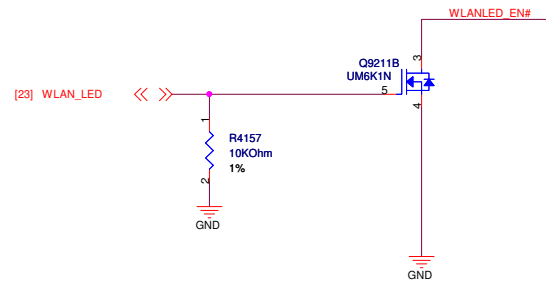
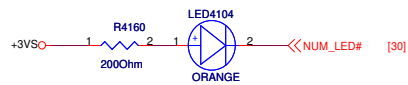
### For WireLess LED



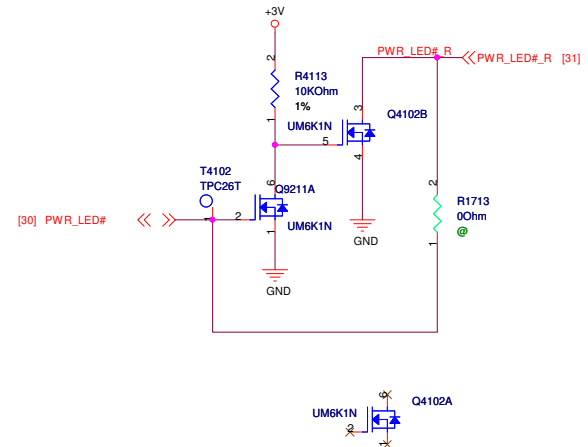
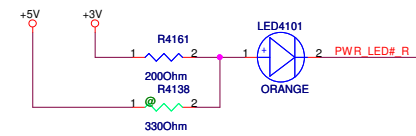
### for Cap. Lock



### for Num Lock



### For POWER LED

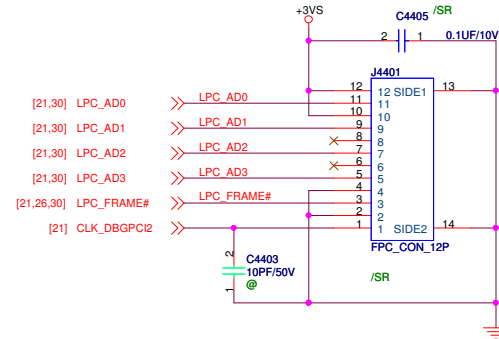



<Variant Name>

<b>ASUS</b>		Title : CB_R5C833	
ASUSTeK COMPUTER INC. NB1		Engineer:	
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009	Sheet	41	of 91

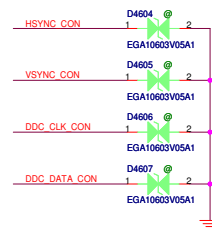
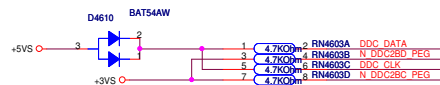
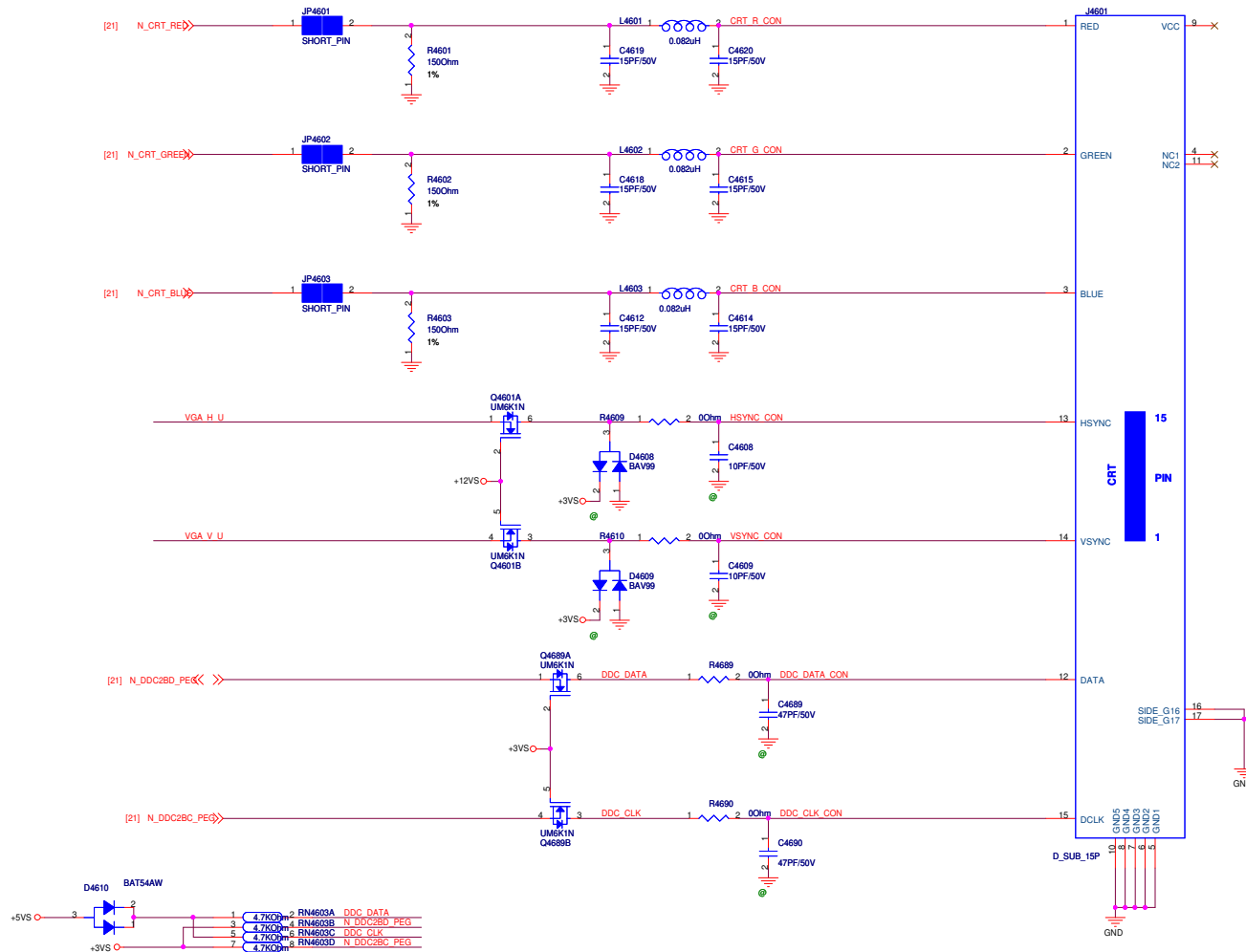




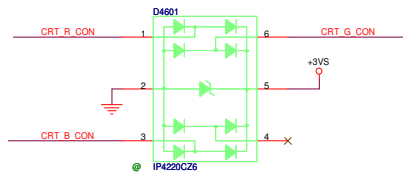



<Variant Name>		
 <b>Title : DEBUG</b>		
<b>Engineer:</b>		
Size Custom	Project Name	Rev 1.0
Date: Friday, February 13, 2009	Sheet 44 of 91	






PLACE ESD Diodes near VGA port




<Variant Name>			
		Title : CRT	
Engineer:			
Size	Project Name		Rev
C			1.1
Date: Friday, February 13, 2009		Sheet 46 of	91



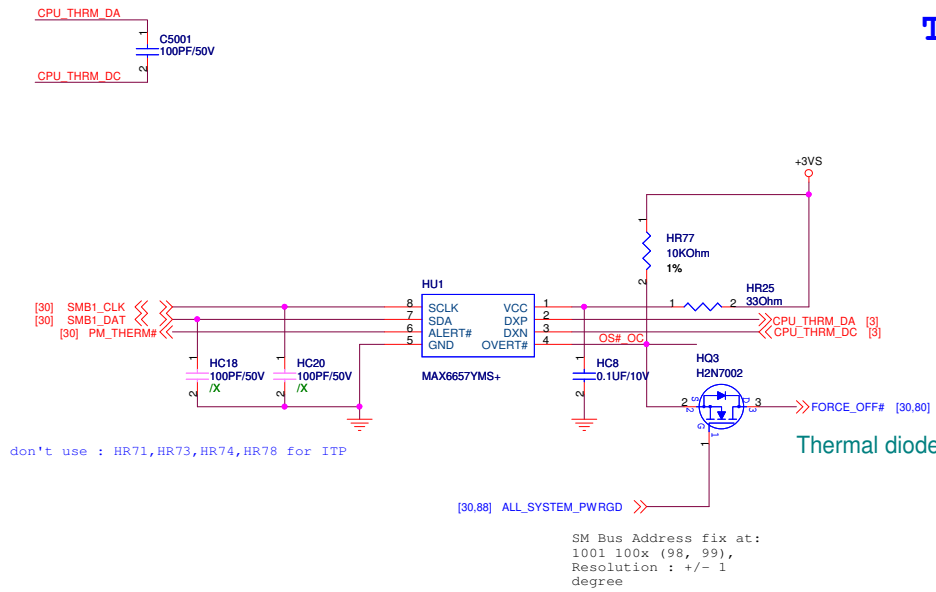
<Variant Name>

		<b>Title:</b> <b>WDS &amp; Inverter CON</b>	
<b>Engineer:</b>			
Size <a href="#">Custom</a>	Project Name		Rev <b>1.0</b>
Date: <b>Friday, February 13, 2009</b>	Sheet	<b>48</b> of	<b>91</b>

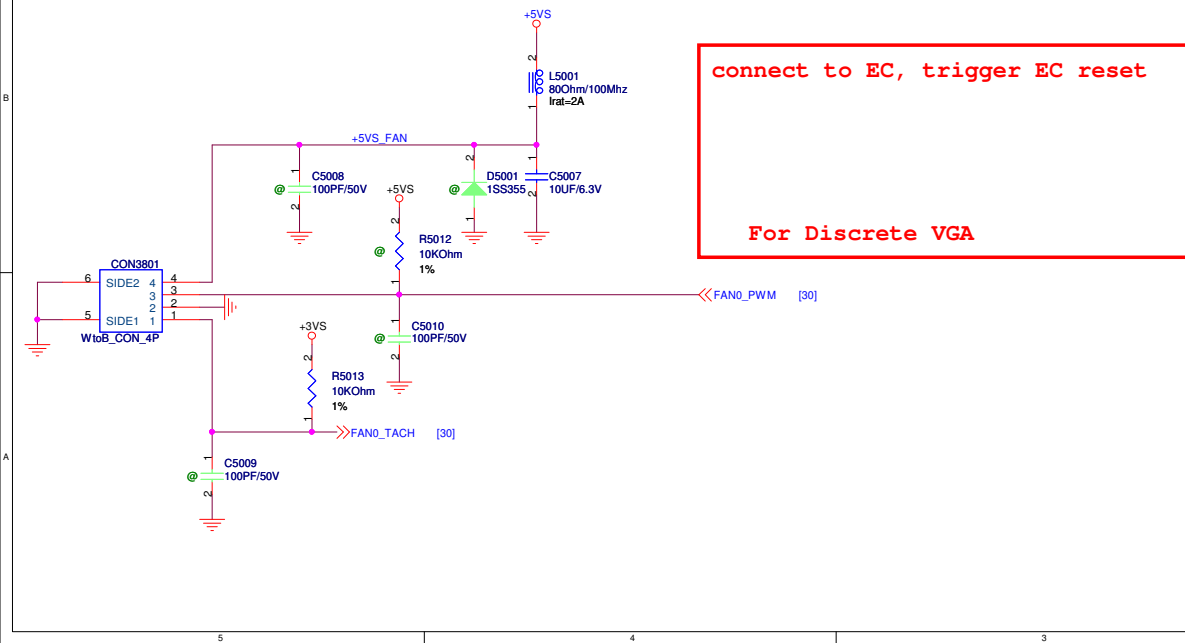


5	4	3	2	1
D				D
C				C
B				B
A				A
				<div> <div>&lt;Variant Name&gt;</div> <div> <div>  <div>Title :</div> </div> <div> <div>Engineer:</div> <div> <div>Size</div> <div>Project Name</div> <div>Rev</div> </div> </div> </div> <div> <div>Date: Friday, February 13, 2009</div> <div>Sheet 49 of 91</div> </div> </div>
5	4	3	2	1

## Thermal Sensor



## DC FAN Control

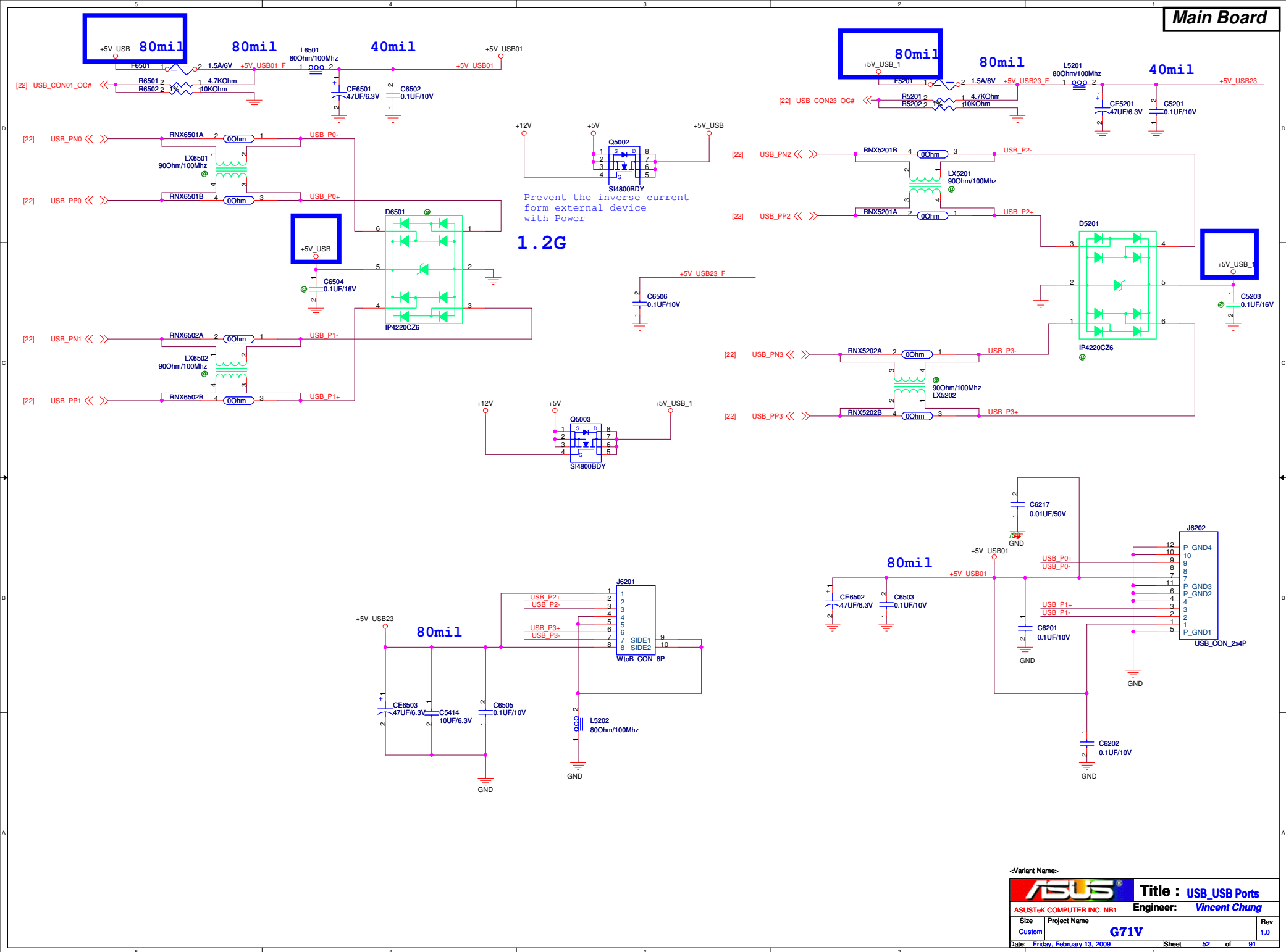


<Variant Name>

<b>ASUS</b>		<b>Title : Thermal &amp; Fan</b>	
Size		Engineer:	
Custom	Project Name	Rev	
Date: Friday, February 13, 2009	Sheet 50 of 91	1.1	

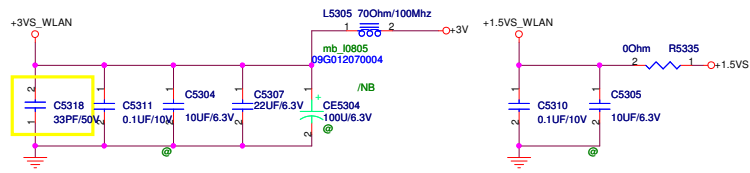
<Variant Name>

		<b>Title</b> <b>Sata HDD &amp; Swap Bay</b>	
<b>Engineer:</b>			
Size <i>Custom</i>	Project Name		Rev <i>1.0</i>
Date: <i>Friday, February 13, 2009</i>	Sheet	<i>51</i>	of <i>91</i>

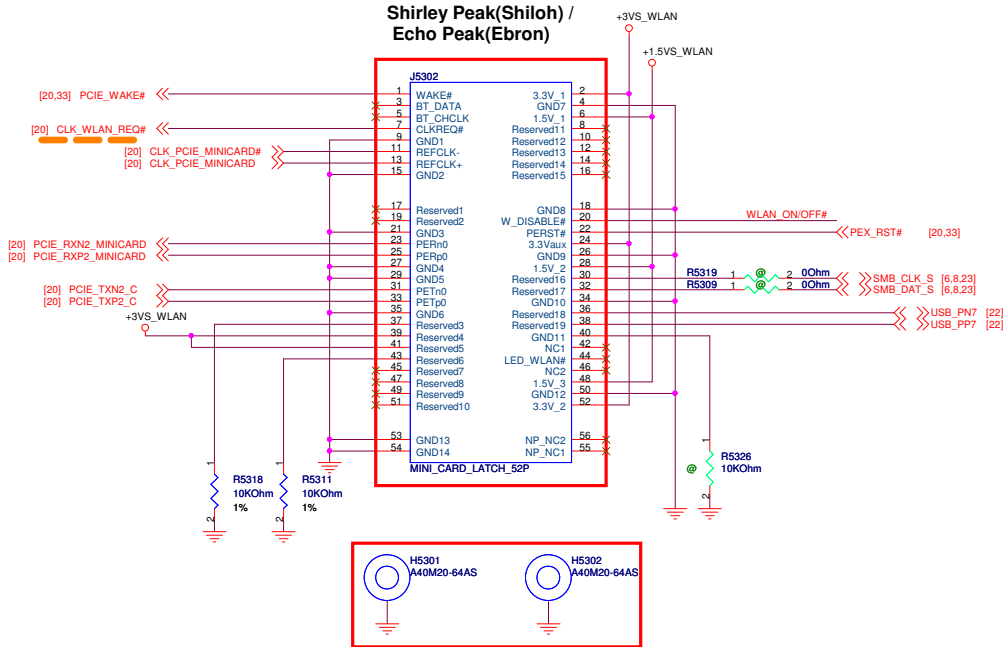


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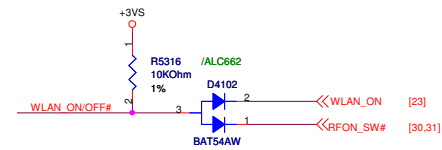
<b>ASUS</b>		<b>Title : USB_USB Ports</b>	
ASUSTeK COMPUTER INC. NBI		Engineer: Vincent Chung	
Size	Project Name	Rev	
Custom	G71V	1.0	
Date: Friday, February 13, 2009		Sheet	52 of 91



# Shirley Peak(Shiloh) / Echo Peak(Ebron)

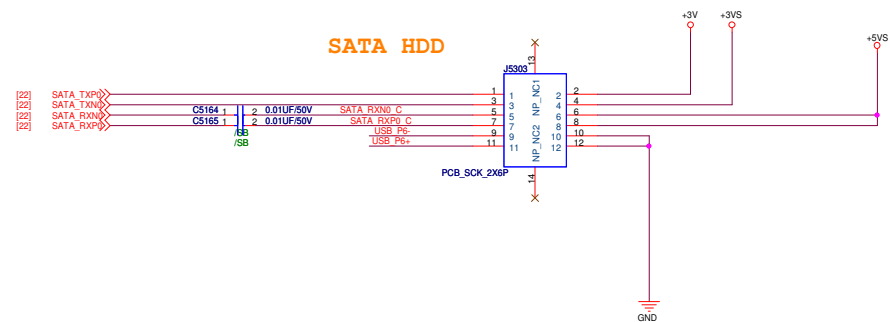
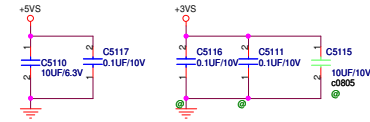


N2




<Variant Name>

<b>ASUS</b>		<b>Title :Minicard card &amp; Nut</b>	
Engineer:			
Size	Project Name	Rev	
Custom		1.0	
Date: Friday, February 13, 2009		Sheet 53 of 91	



5	4	3	2	1	
D					D
C					C
B					B
A					A
5	4	3	2	1	

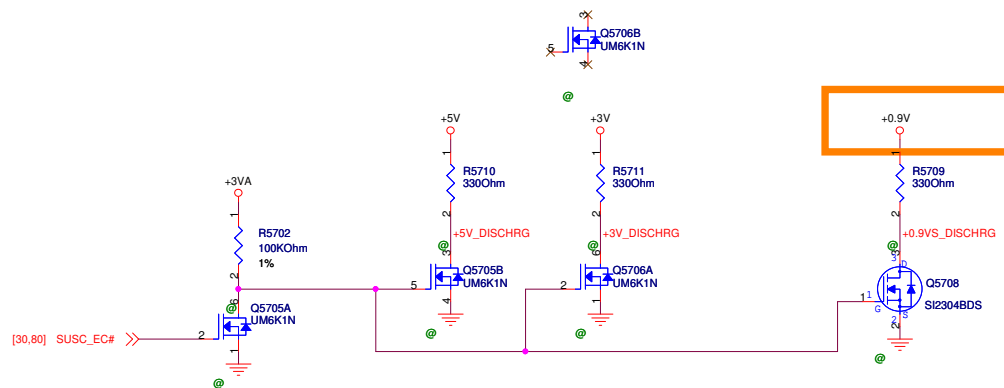
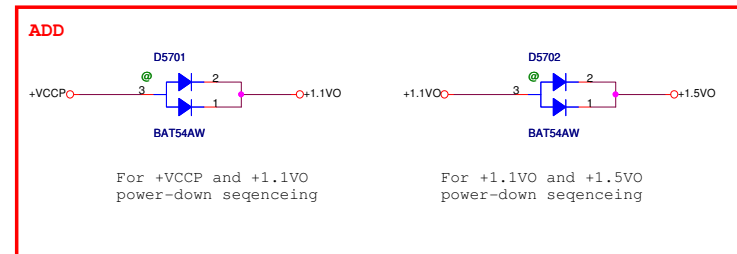
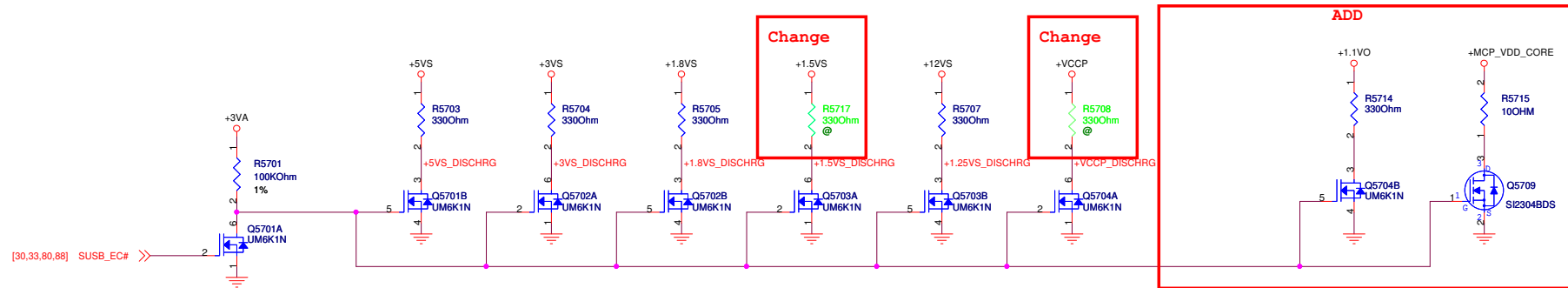
<Variant Name>

		<b>Title :</b>	
<b>Engineer:</b>			
Size	Project Name		Rev
A			1.0
Date: <a href="#">Friday, February 13, 2009</a>		Sheet	55 of 91

<Variant Name>

		<b>Title :</b> <i>LED_Indicator</i>	
<b>ASUSTek COMPUTER INC. NB1</b>		<b>Engineer:</b> <i>Vincent Chung</i>	
Size <i>Custom</i>	Project Name <b>G71V</b>	Rev <b>1.0</b>	
<b>Date:</b> <i>Friday, February 13, 2009</i>		<b>Sheet</b> <i>56</i> <b>of</b> <i>91</i>	






&lt;Variant Name&gt;

<b>ASUS</b>		<b>Title : DSG_Discharge</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>G71G</b>	1.0	
Date: Friday, February 13, 2009		Sheet	57 of 91

<Variant Name>

		<b>Title :</b>	
		<b>Engineer:</b>	
Size Custom	Project Name		Rev 1.0
Date: Friday, February 13, 2009	Sheet	58 of	91

D

C

B

A

**<Variant Name>**



**Title :**

ASUSTeK COMPUTER INC. NB6

**Engineer:**

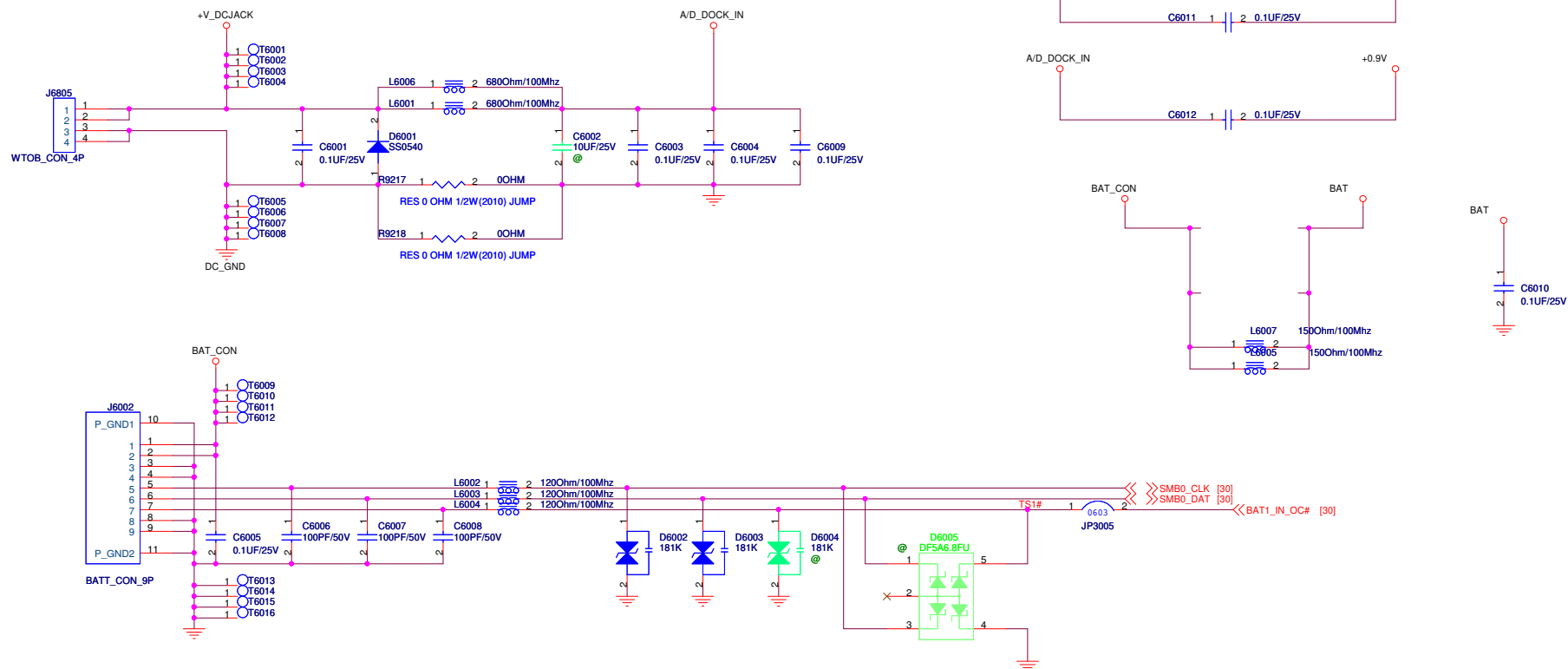
Size  
A

Project Name
--------------

Rev
1.0


Date: Friday, February 13, 2009

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<Variant Name>



Title :

ASUSTeK COMPUTER INC. NB1Engineer: John Hung

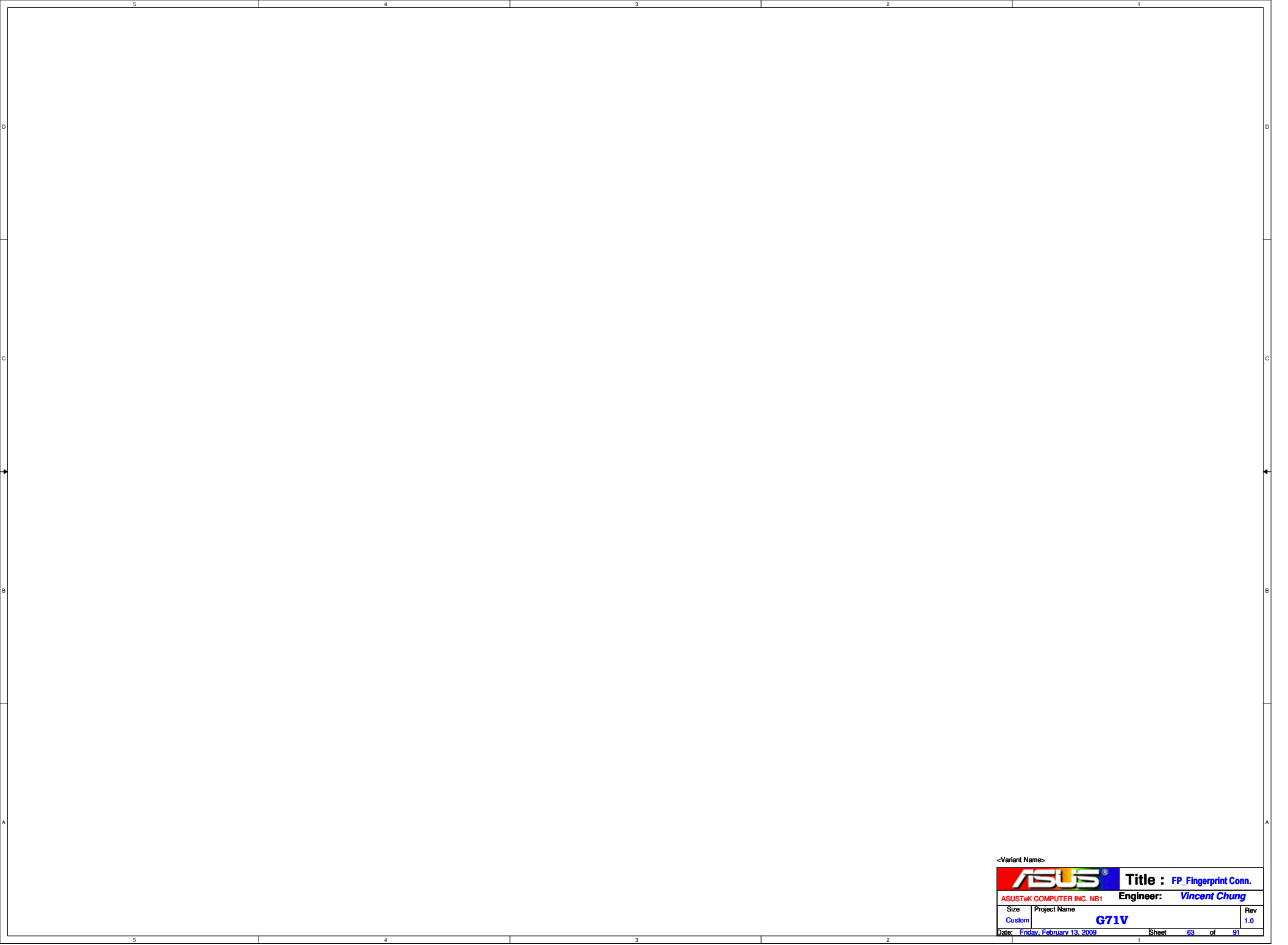
Size  
Custom

Project Name

Date: Friday, February 13, 2009

Rev  
1.0

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<Variant Name>



Title : FP\_Fingerprint Conn.

ASUSTeK COMPUTER INC. NB1


Engineer: Vincent Chung

Size	Project Name	Rev
Custom	G71V	1.0

Date: Friday, February 13, 2009

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<Variant Name>

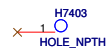
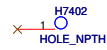
		<b>Title :</b> <i>TUN_TV Tuner</i>	
<b>ASUSTek COMPUTER INC. NB1</b>		<b>Engineer:</b> <i>John Hung</i>	
<b>Size</b> <i>Custom</i>	<b>Project Name</b> <i>N2Sv</i>	<b>Rev</b> <i>1.0</i>	
<b>Date:</b> <i>Friday, February 13, 2009</i>		<b>Sheet</b>	<i>64</i> of <i>91</i>



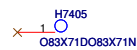
### Hole-A



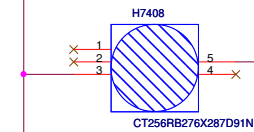
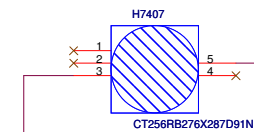
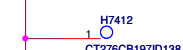
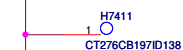
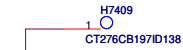
### Hole-B



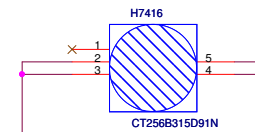
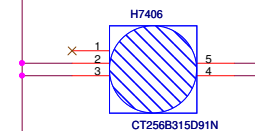
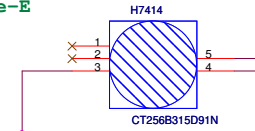
### Hole-C



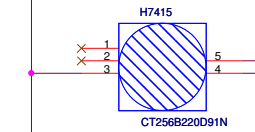
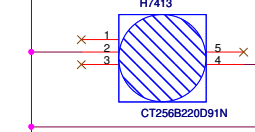
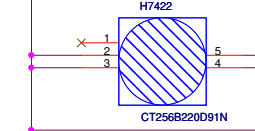
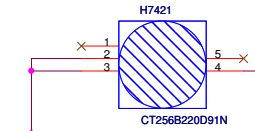
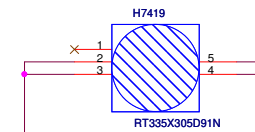
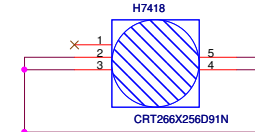
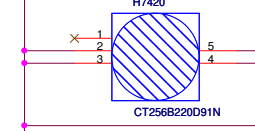
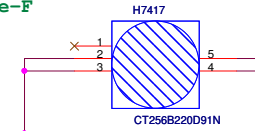
### Hole-D



### Hole-E



### Hole-F

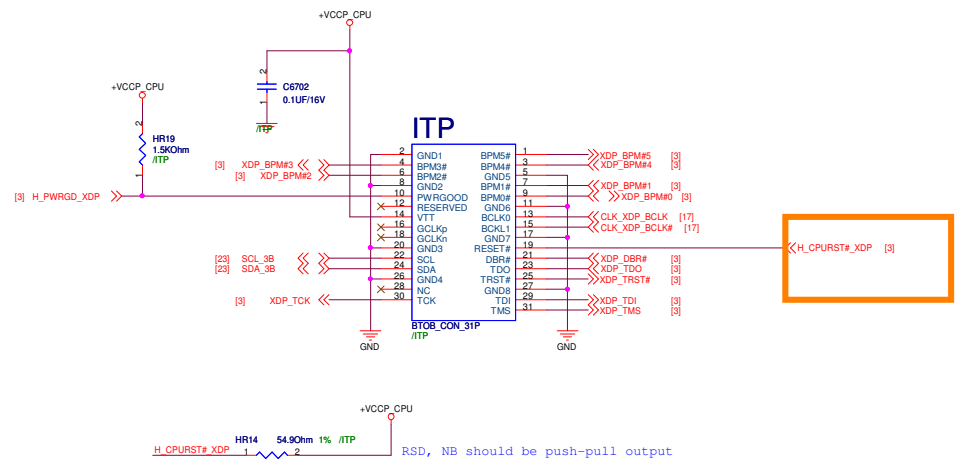


<Variant Name>

<b>ASUS</b>		<b>Title :ME_Conn &amp; Screw Holes</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Vincent Chung</b>	
Size	Project Name	Rev	
Custom	<b>G71V</b>	1.0	
Date: Friday, February 13, 2009		Sheet	65 of 91

<Variant Name>	
ASUS® Title : E-SATA	
Engineer:	
Size Custom	Project Name  Rev 1.0
Date: Friday, February 13, 2009	Sheet 66 of 91

Place Beside CPU




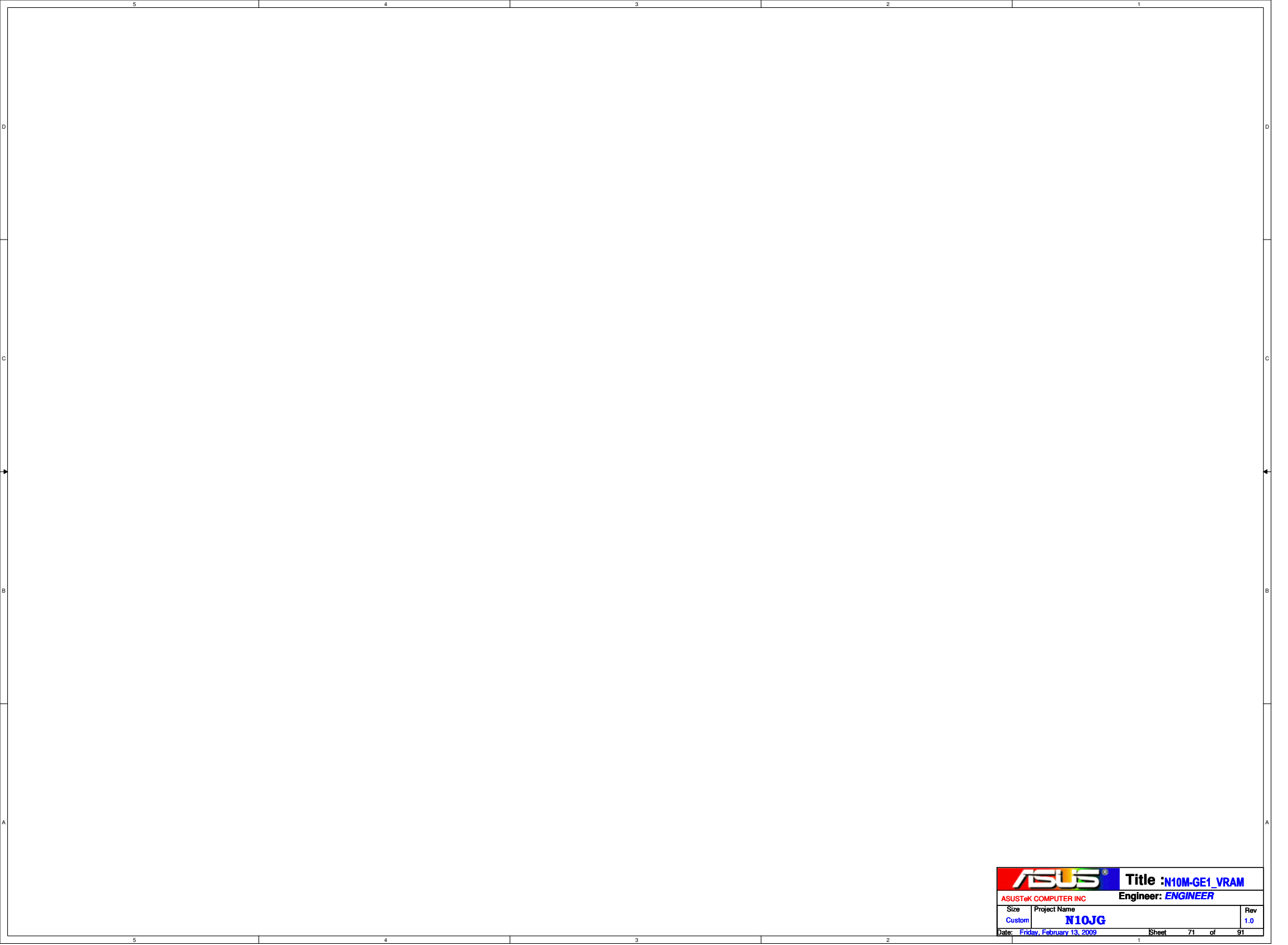
IN CPU page





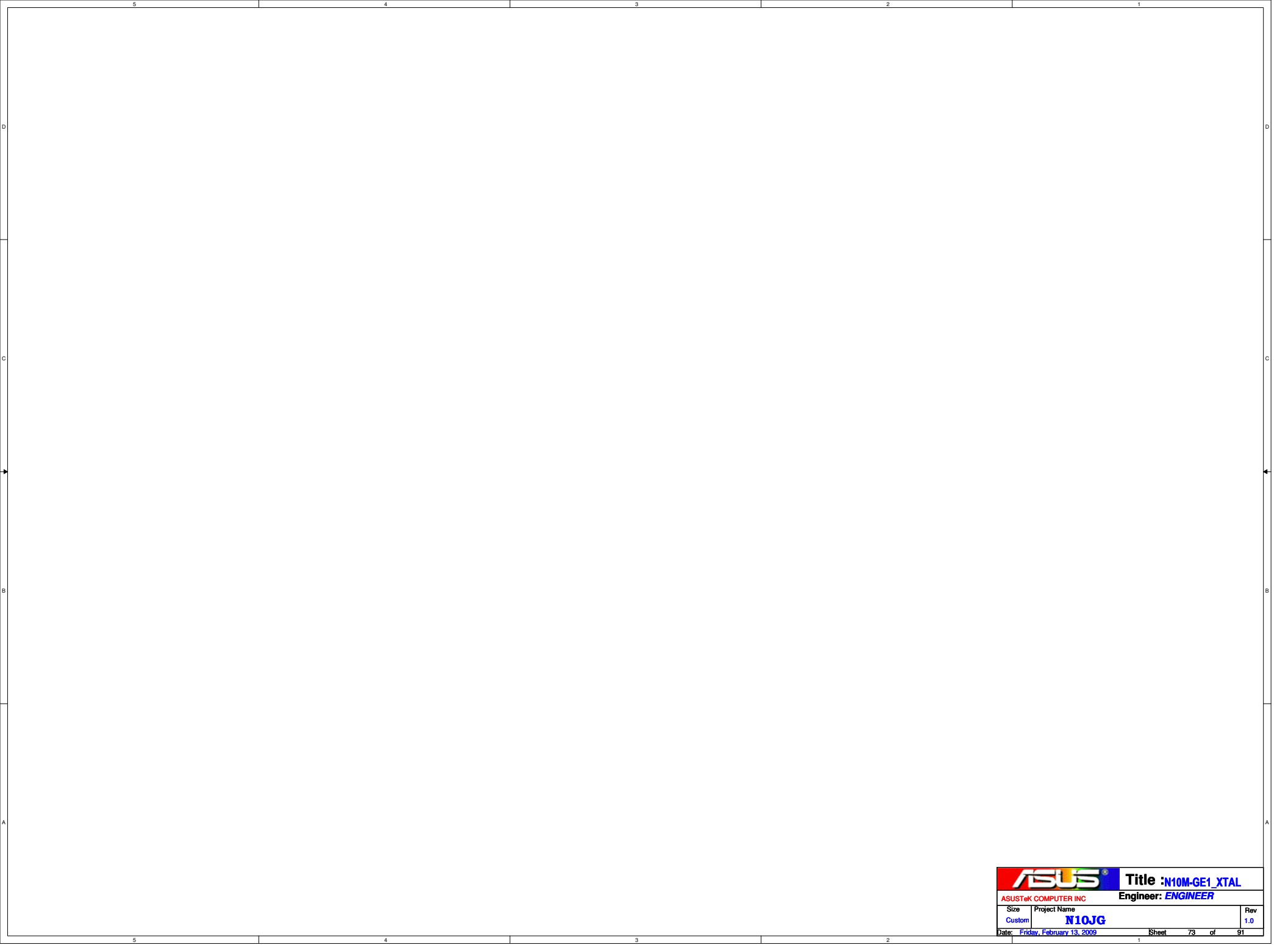


		<b>Title :</b> N10M-GE1_FB	
ASUSTeK COMPUTER INC		<b>Engineer:</b> ENGINEER	
Size Custom	Project Name N10JG		Rev 1.0
Date: Friday, February 13, 2009		Sheet	70 of 91




		<b>Title :</b> N10M-GE1_DISPLAY	
<b>ASUSTek COMPUTER INC</b>		<b>Engineer:</b> ENGINEER	
Size Custom	Project Name <b>N10JG</b>		Rev 1.0
Date: Friday, February 13, 2009		Sheet 72 of 91	






		<b>Title :</b> N10M-GE1_XTAL	
ASUSTeK COMPUTER INC		Engineer: <i>ENGINEER</i>	
Size	Project Name		Rev
Custom	N10JG		1.0
Date: Friday, February 13, 2009		Sheet	73 of 91

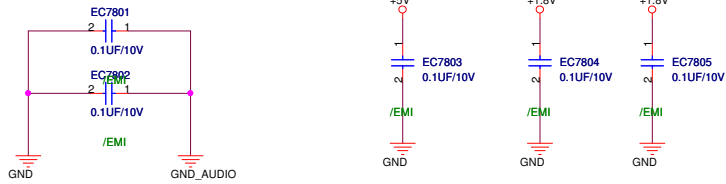


		Title : <b>N10M-GE1_ROM</b>	
ASUSTeK COMPUTER INC		Engineer: <b>ENGINEER</b>	
Size Custom	Project Name <b>N10JG</b>		Rev <b>1.0</b>
Date: <b>Friday, February 13, 2009</b>		Sheet	74 of 91

<Variant Name>

		Title : LED & Touchpad	
ASUSTeK COMPUTER INC. NB1		Engineer: Vincent Chung	
Size	Project Name		Rev
Custom	G71V		1.1
Date: Friday, February 13, 2009		Sheet	75 of 91

<Variant Name>			
		Title :Fingerprint & Touchpad	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Wenchi_Shen</i>	
Size Custom	Project Name <b>M70Sv</b>		Rev 1.1
Date: <i>Friday, February 13, 2009</i>		Sheet	76 of 91



54321

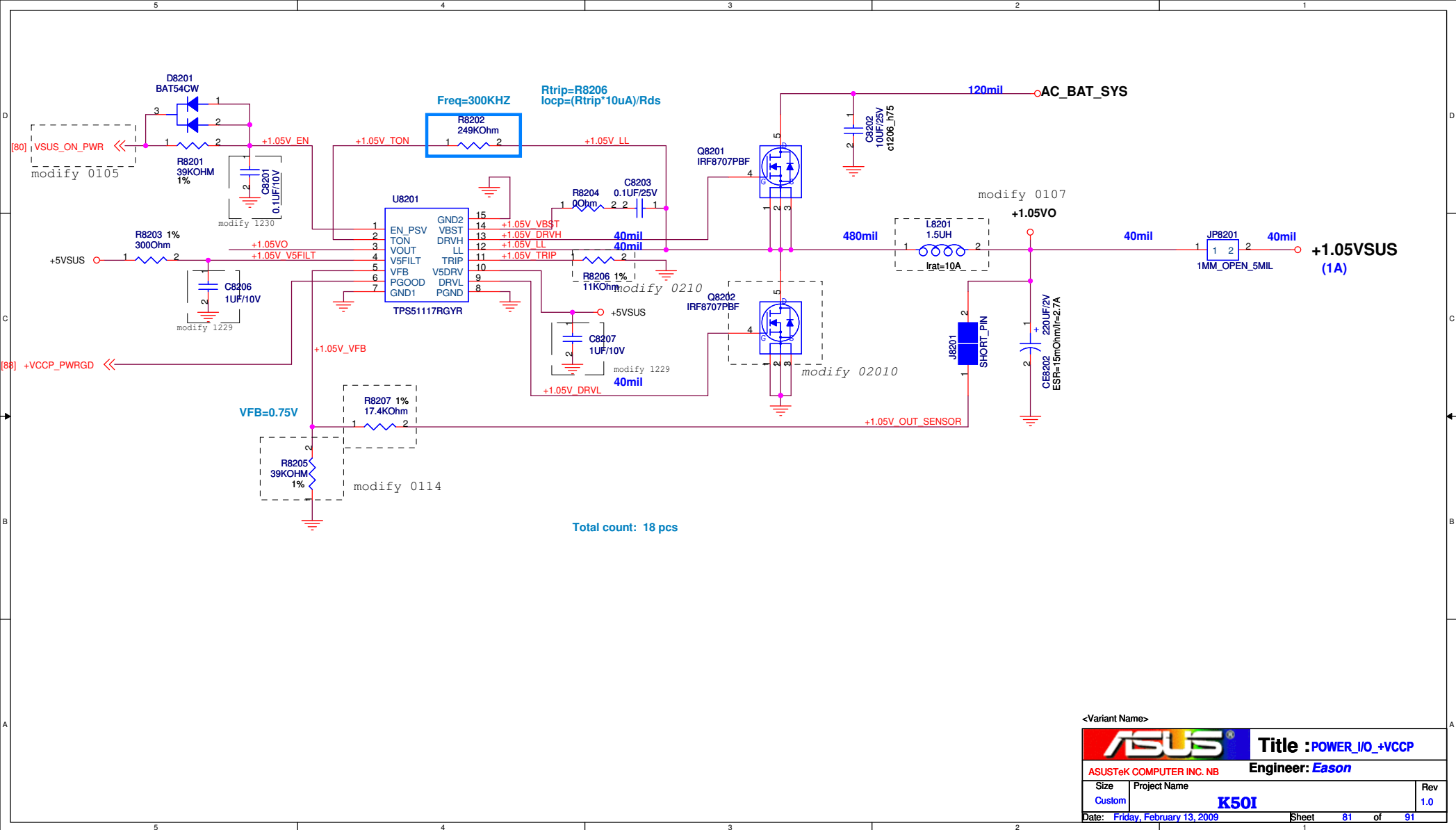
History1.0G:@1.1G power modify : \$1.2G: %1.1G EE modify :

- 200805201.2G
- Page 521. ADD USB+5V gate Q5002
- Page 562. ADD R5626,R5609
- Page 43. DEL R0412
- Page 544. ADD C5402,C5403 5p for SMBus in GPIO controller ; GPRN10 change to 10K ohm
- Page 845. Controlle +5V with SUSC#\_PWR
- Page 826. Change +VCCP to 1.2V default for CPU O.C. ability improve
- 200807012.0G
- Page 561. TP-LED v.s. TP-disable LED reverse
- Page 452. Inverter CN pin 19 reserve 0 phm to GND ,never stuff for single-lamp inverter
- Page 463. Battery in P/H change to +3VA
- Page 804. CPU load-line modify to 2.1 mini-ohm (R8036 由 10.5K改成 9.31K 1%)





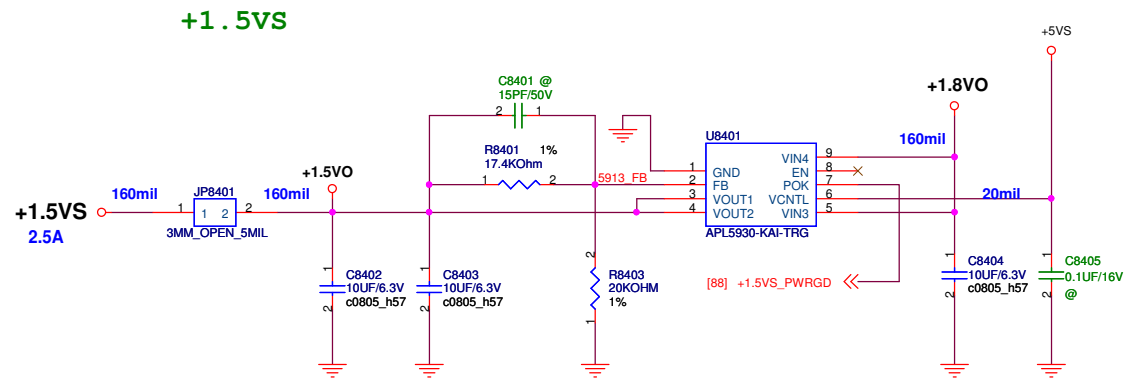




<Variant Name>

<b>ASUS</b>		<b>Title :POWER_I/O_+VCCP</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <b>Eason</b>	
Size Custom	Project Name <b>K50I</b>		Rev 1.0
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Total count: 6 pcs


<Variant Name>		
		Title : INS29491694
ASUSTeK COMPUTER INC. NB		Engineer: Eason
Size B	Project Name <b>K50I</b>	Rev 1.0
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BATTERY IN DETECT

<Variant Name>

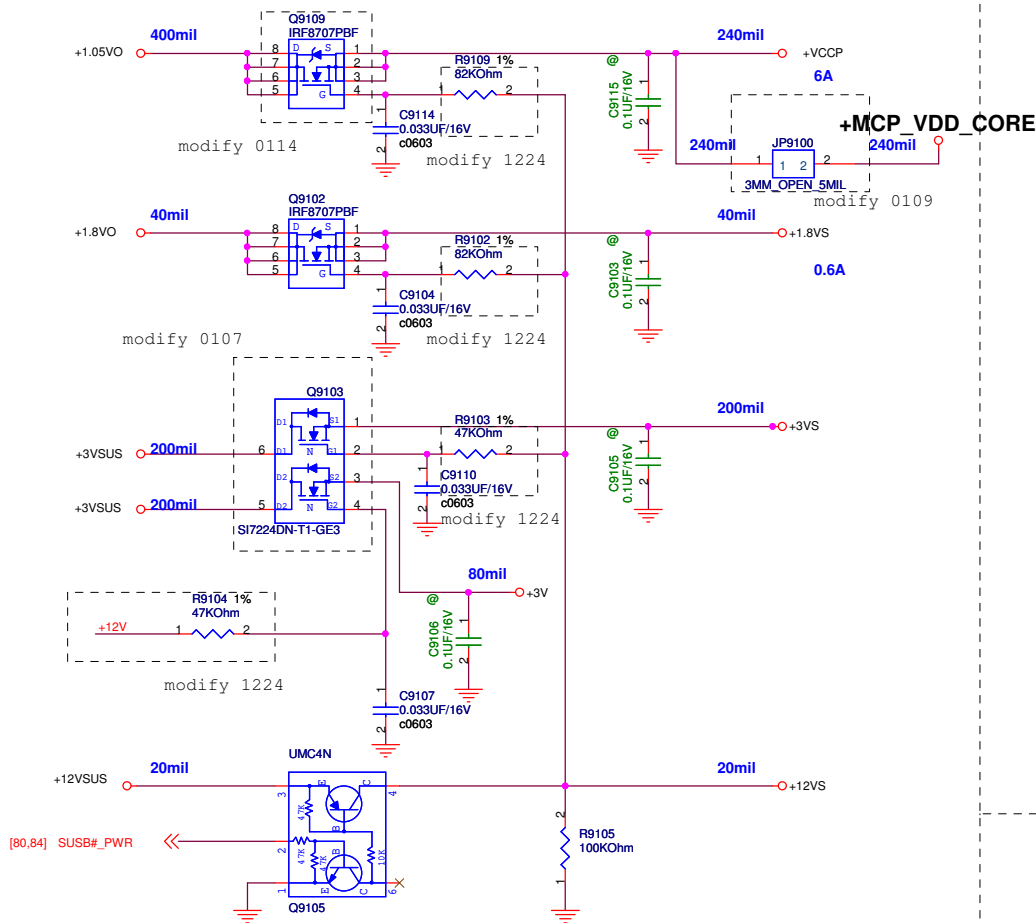


Title :POWER\_DETECT

ASUSTeK COMPUTER INC. NBEngineer: Eason

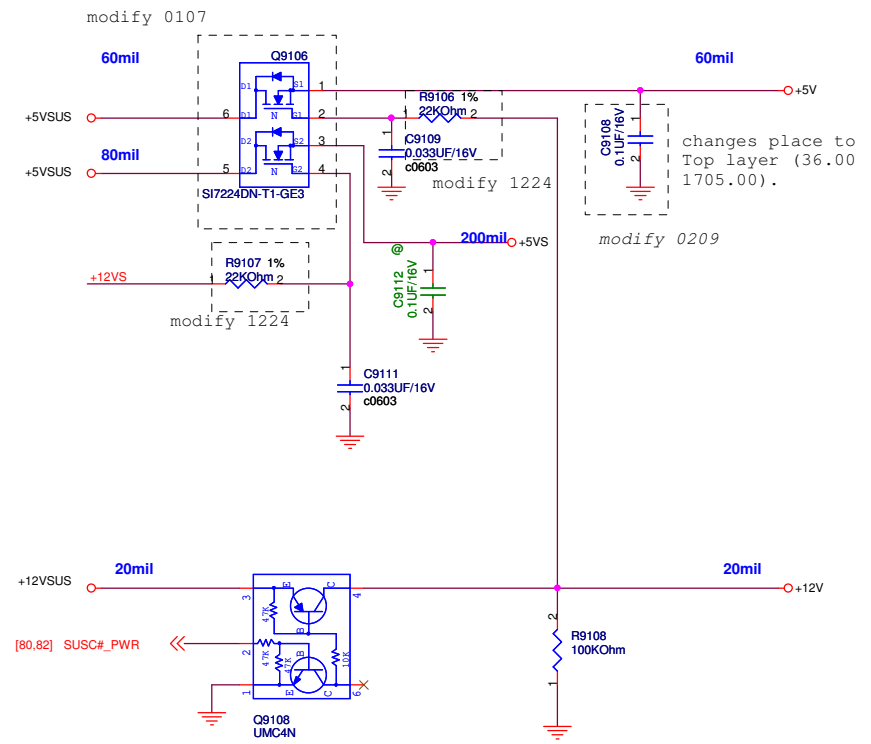
Size	Project Name	Rev
Custom	K50I	1.0
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# SUSB#\_PWR POWER



Total count: 19 pcs

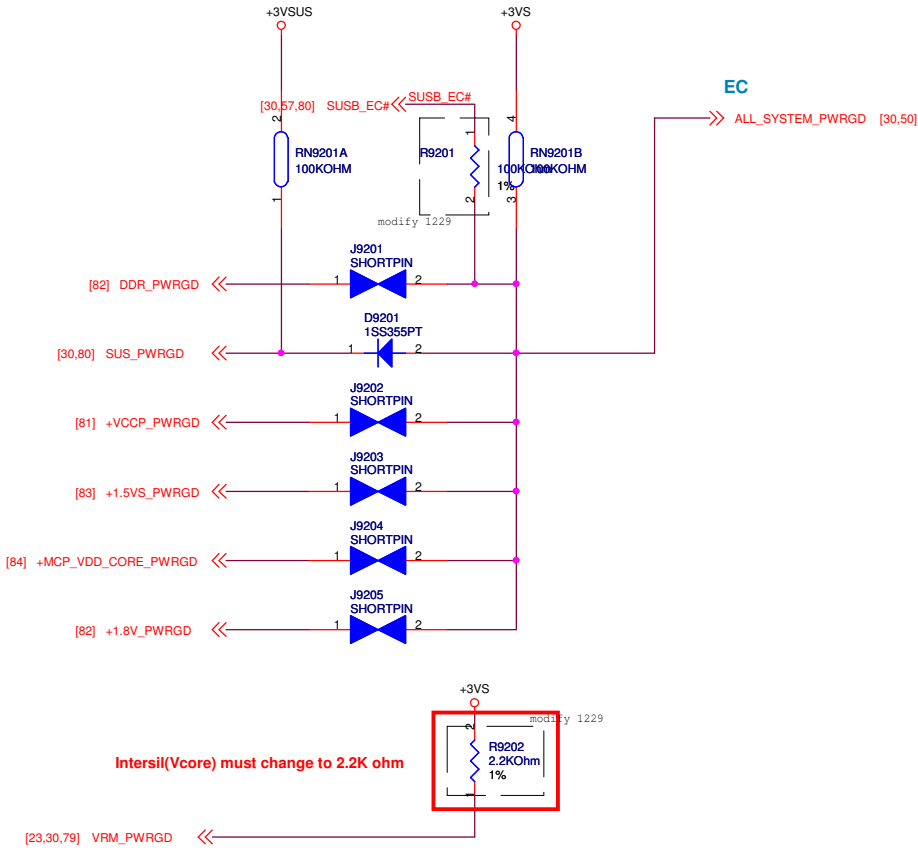
# SUSC#\_PWR POWER



<Variant Name>

<b>ASUS</b>		<b>Title : POWER_LOAD SWITCH</b>	
ASUSTek COMPUTER INC. NB		Engineer: <b>Eason</b>	
Size B	Project Name <b>K50I</b>		Rev 1.0
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POWER GOOD DETECTOR



<Variant Name>		Title : POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Eason	
Size B	Project Name K50I	Rev 1.0	
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