Schematic Page Description :

Quanta Computer Inc.		
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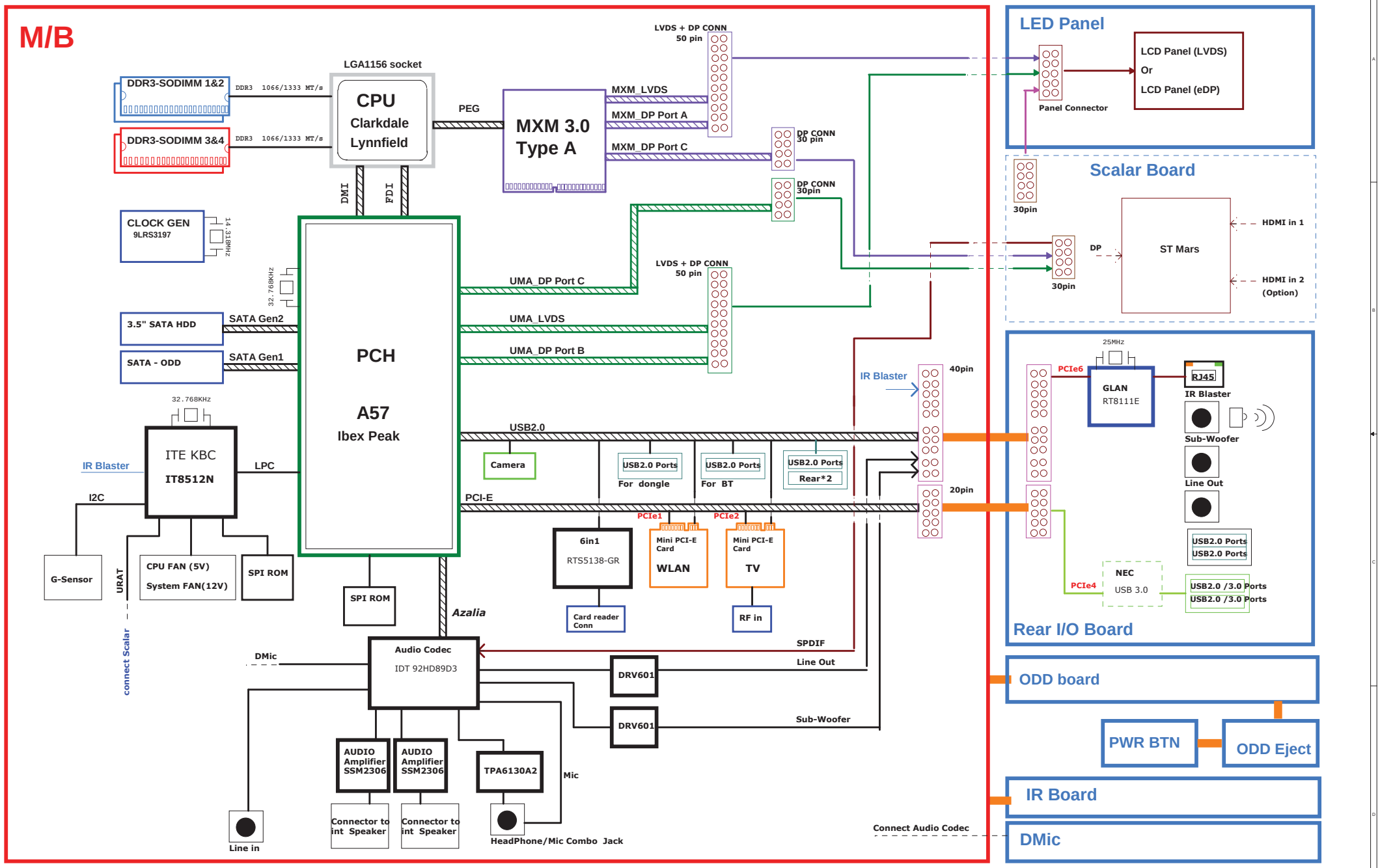
F01 System Block Diagram



Quanta Computer Inc.
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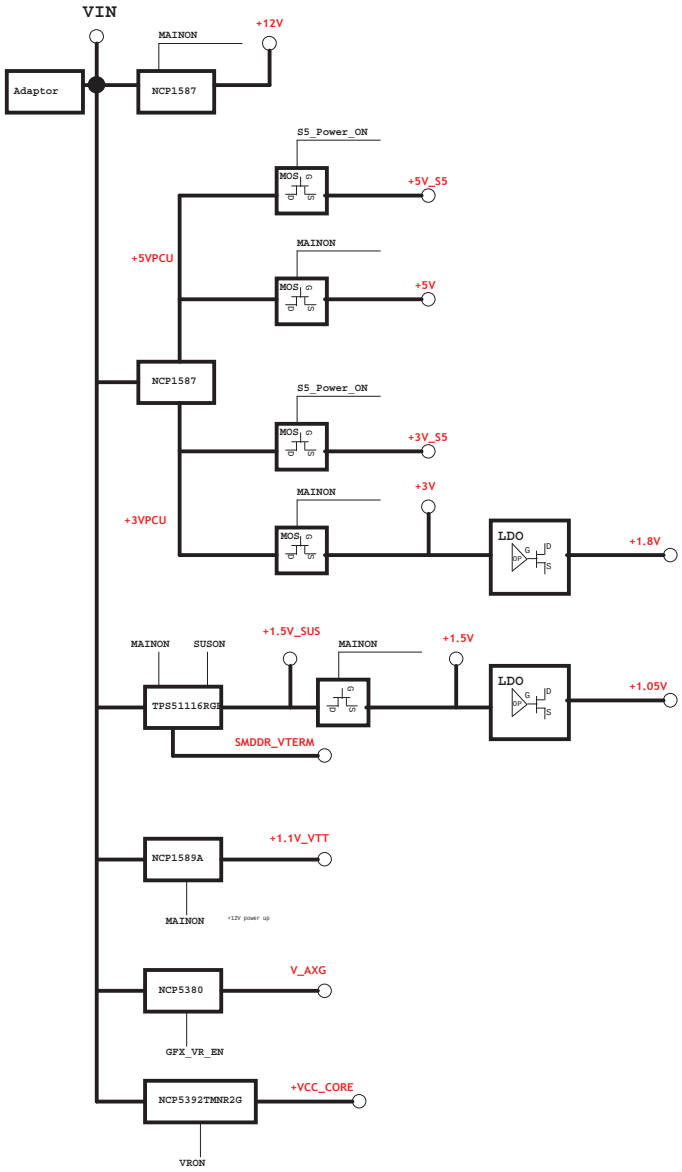
Power Rail	Destination	Voltage	S0 Current
+VCC_CORE	Lynnfield :	0.65V~1.4V	90A(TDC)
	Default for initial power up	1.1V	
V_AXG			
+1.1V_VTT	Lynnfield : Memory controller & shared cache	1.045V~1.1V~1.155V	30A(TDC)
	Ibex Peak : DMI	1.1V	0.065A
	Ibex Peak : CPU_IO	1.05V~1.1V~1.16V	0.001A
+1.8V	Lynnfield : Internal processor PLL	1.71V~1.8V~1.89V	1.1A
	Ibex Peak : Internal PLL & VRMs	1.71V~1.8V~1.89V	0.196A
	Ibex Peak : Dual channel NAND I/F	1.71V~1.8V~1.89V	0.156A
+1.5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V~1.5V~1.575V	6A
SMDDR_VTERM	DDRIII Terminator:	0.75V	2A
+1.05V	Ibex Peak : VccCore	0.998V~1.05V~1.1V	1.629A
	Ibex Peak : Vcc core I/O buffer	0.998V~1.05V~1.1V	3.251A
	Ibex Peak : DMI buffer voltage	0.998V~1.05V~1.1V	0.065A
	Ibex Peak : Display PLL A power	0.998V~1.05V~1.1V	0.075A
	Ibex Peak : Display PLL B power	0.998V~1.05V~1.1V	0.075A
+1.5V	Mini PCIE : +1.5V(WLAN)		
+3V	Ibex Peak : I/O buffer voltage	3.14V~3.3V~3.47V	0.357A
	Ibex Peak : Display DAC Analog power	3.14V~3.3V~3.47V	0.069A
	CH7308 : LVDD		
	ALC662 : DVDD		
	Mini PCIE : +3.3V(WLAN)		
	CAREMA		
+5V	Ibex Peak : Core well Ref. voltage	4.75V~5V~5.25V	0.001A
	SATA ODD		
	SATA HDD(2.5" x SSD)		
	ALC662S : AVDD		
	Touch Screen		
	LCD Panel		
	USB: x 12 ports	5V	6A
+12V			
+3V_S5	Ibex Peak : Intel Management Engine	3.14V~3.3V~3.47V	0.086A
	Ibex Peak : Suspend well I/O Buffer	3.14V~3.3V~3.47V	0.168A
	Ibex Peak : HD Audio controller Suspend Voltage	3.14V~3.3V~3.47V	0.006A
	LAN 82578DM : VDD		
	CLK Gen.CK505 : VDD		
	EC(IT8512) : VSTBY		
	SPI FLASH ROM		
+5V_S5	Ibex Peak : Suspend well Ref. Voltage	4.75V~5V~5.25V	0.001A
	INVERTER : Vin		
	FAN_CPU		
+3VPCU			
+5VPCU			
15VPCU			
VIN			



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Power Map
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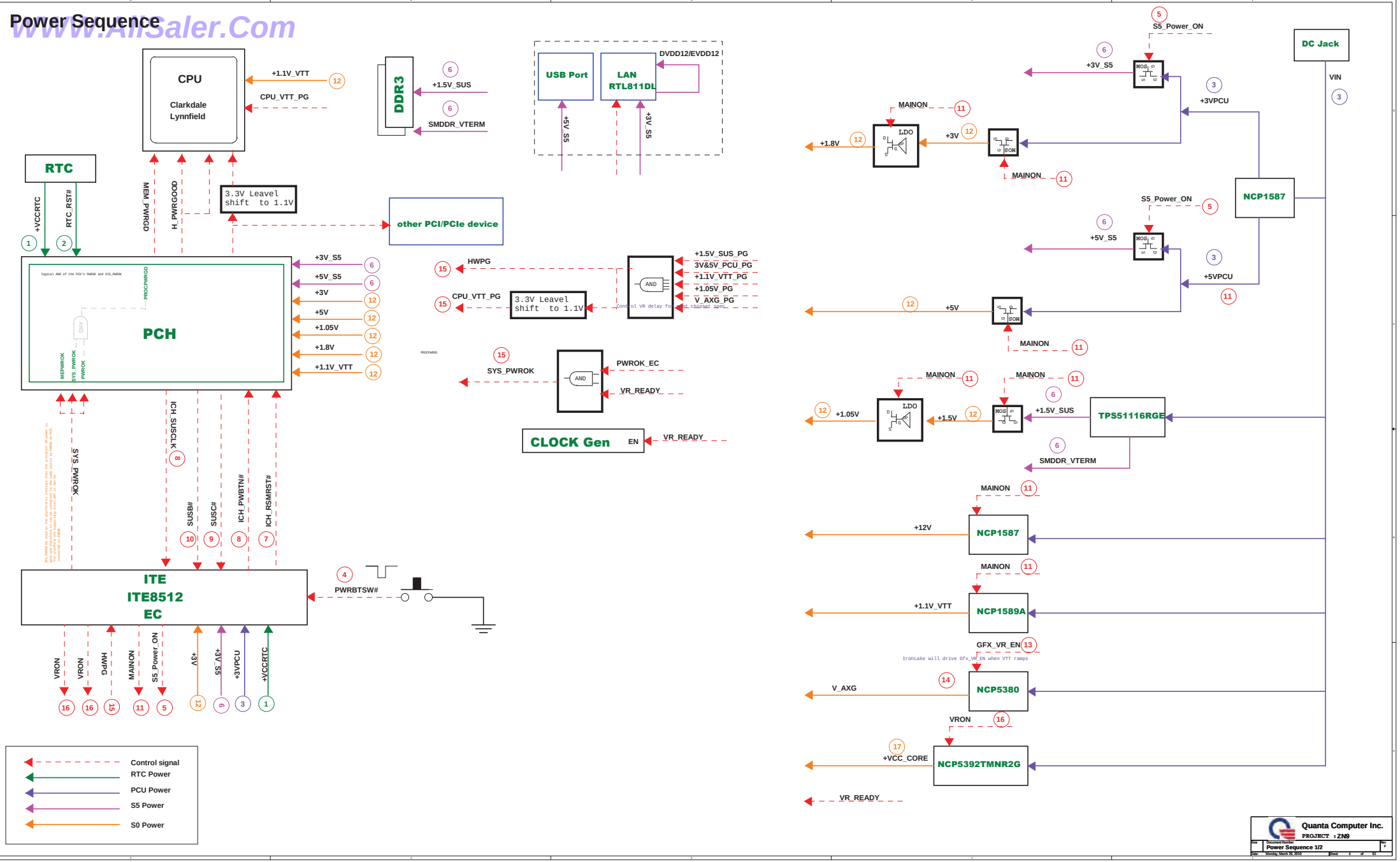
Power Sequence



Quanta Computer Inc.
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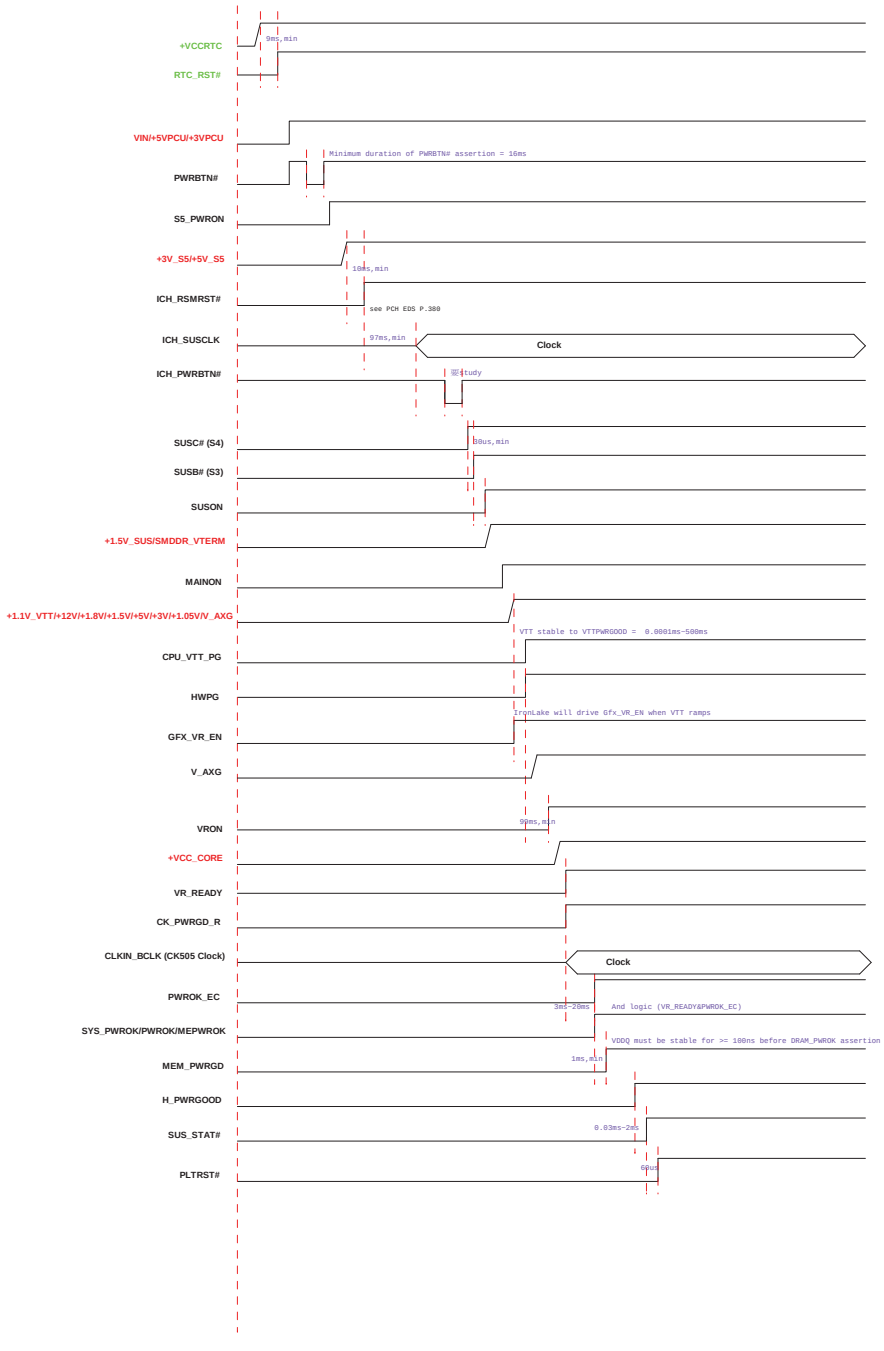
Power Sequence 1/2

POWER SEQUENCE

Voltage Rails

Power	Voltage	S0	S3	S4	S5	PCU	G3	Ctl Signal	
+VCCRTC	3V	ON	ON	ON	ON	ON	ON		
VIN	19.5V	ON	ON	ON	ON	ON	OFF	Adaptor in	
+5VPCU	5V	ON	ON	ON	ON	ON	OFF	Adaptor in	
+3VPCU	3.3V	ON	ON	ON	ON	ON	OFF	Adaptor in	EC
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	S5_PWRON	PCH SUS,
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	S5_PWRON	Sys Management, PCH Resume Well, Intel HD Audio, USB, WLAN,
+5V_S3	5V	ON	ON	OFF	OFF	OFF	OFF	S3_5V_EN	DDR3 Memory
+1.5V_SUS	1.5V	ON	ON	OFF	OFF	OFF	OFF	SUSON	DDR3 Memory
SMDDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	OFF	SUSON	
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	SATA, PCI REF
+3V	3.3V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	PCI Express*, SATA, HV CMOS,CRT, Band Gap voltages, Intel HD Audio
+1.5V	1.5V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	mini PCIe, Intel HD Audio
+1.05V	1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	PCH core, PCH PLL voltages, PCH CLK Buffer, SATA, USB, PCH fuse,Display Link, Display Port, PCIe
+1.8V	1.8V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	LVDSIO, SFR, FLASH
+1.1V_VTT	1.1V / 1.05V	ON	OFF	OFF	OFF	OFF	OFF	MAINON	CPU VTT, FDI,PEG, DMI, VCCTTADDR, PCH DMI,PCH V_CPU_IO
V_AXG	???V	ON	OFF	OFF	OFF	OFF	OFF	GFX_VR_EN	mini PCIe, Intel HD Audio
+VCC_CORE	???V	ON	OFF	OFF	OFF	OFF	OFF	VRON	CPU Core

Power	Voltage	S0	S3	S4	S5	PCU	G3	
VIN_MXM								
+5V_MXM								
+3V_MXM								
USBVCC2								
3VPCU_EC								
LCDVCC								
CCD_PWR								
VIN_LCD								
VDDA_CODEC								



Quanta Computer Inc.
PROJECT : ZH9
Power Sequence 2/2
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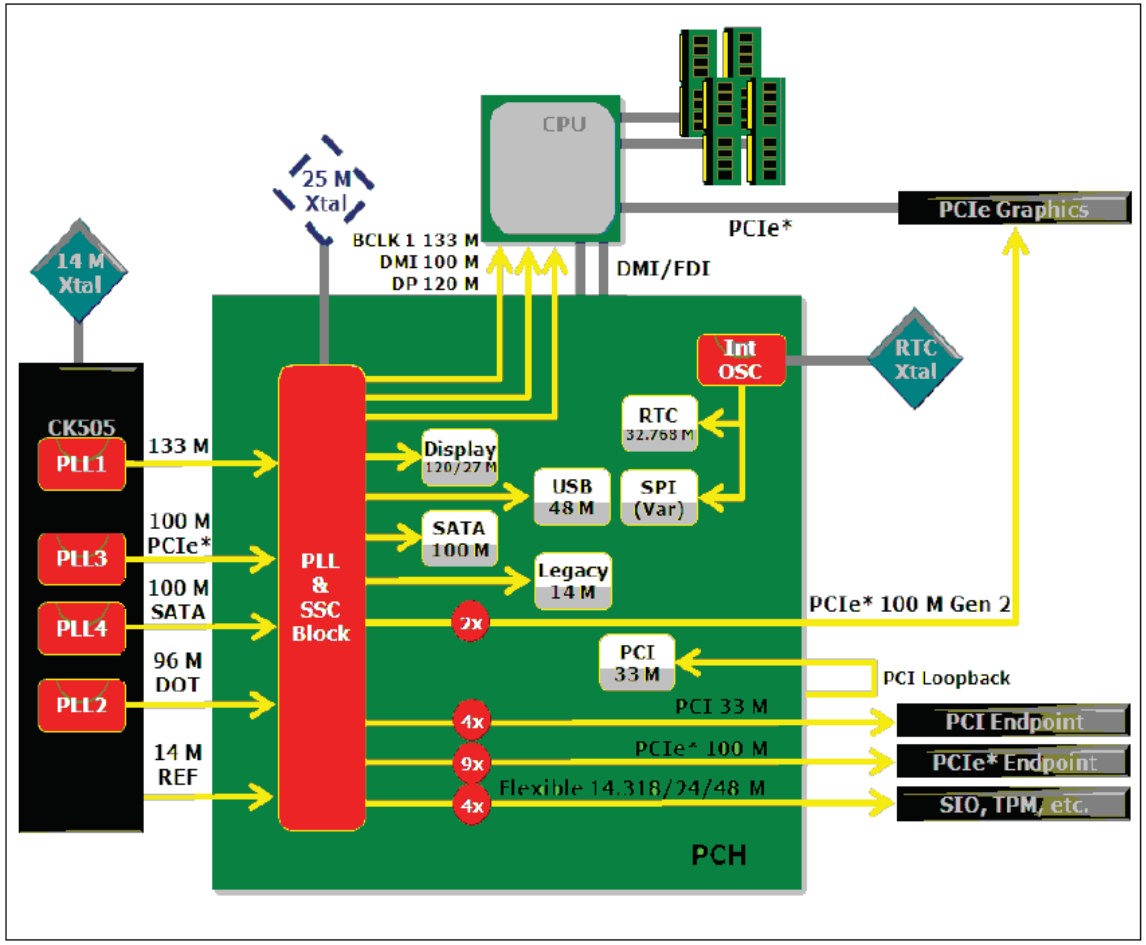

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Size	Document Number	Rev
	IBEX PEAK-M 1/6	F

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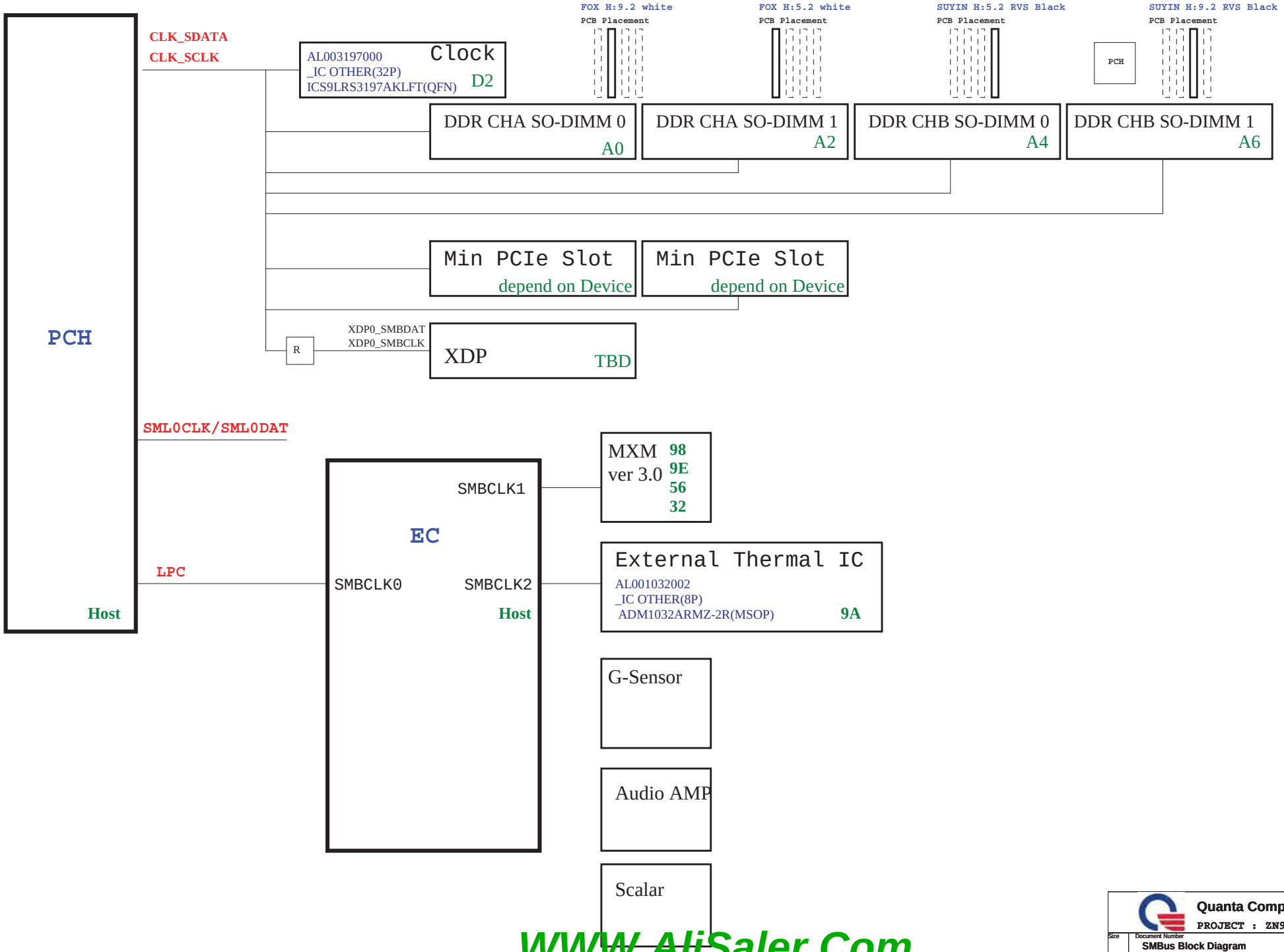
ZN7 SMbus Block Diagram



Quanta Computer Inc.
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Size	Document Number	Rev
	SMBus Block Diagram	F

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NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		INITAL : HIGH / ACTIVE : LOW
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		I		
		I		

NAME	GPIO/PIN	I/O	DESCRIPTION	ACTIVE
		I		
		B		
		I		
		I		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		O		
		O		
		O		
		O		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		I		
		O		
		O		
		O		
		I		
		I		

Quanta Computer Inc.
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Size	Document Number	Rev
	GPIO List	F

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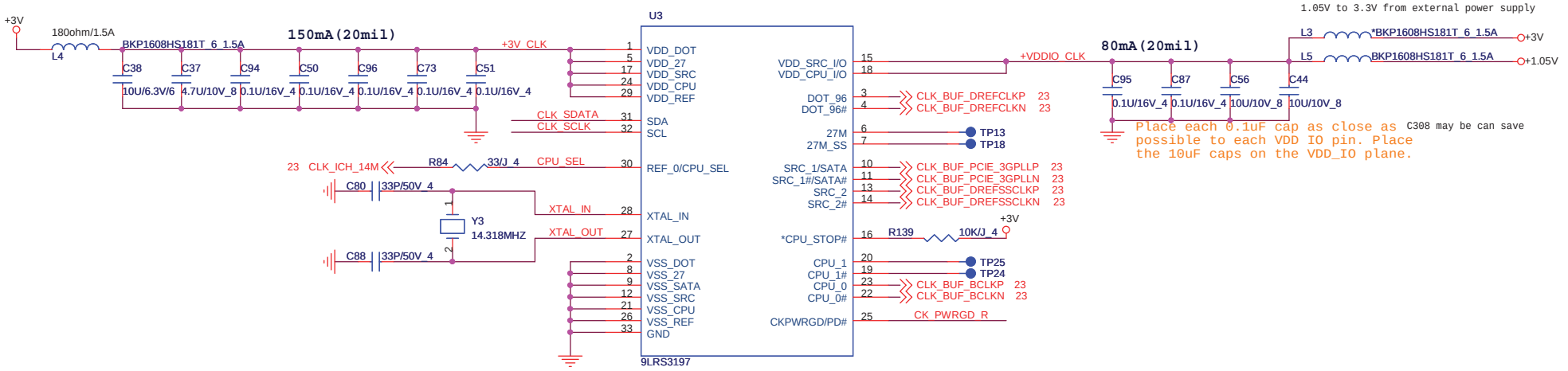
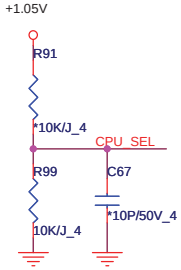
Clock Generator

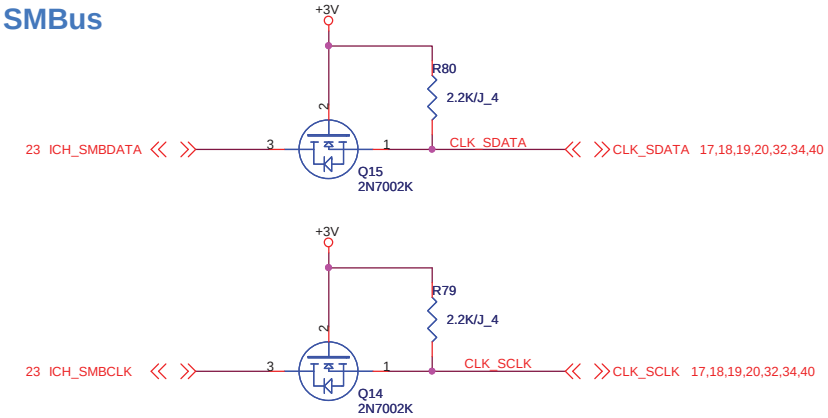


CPU_CLK select

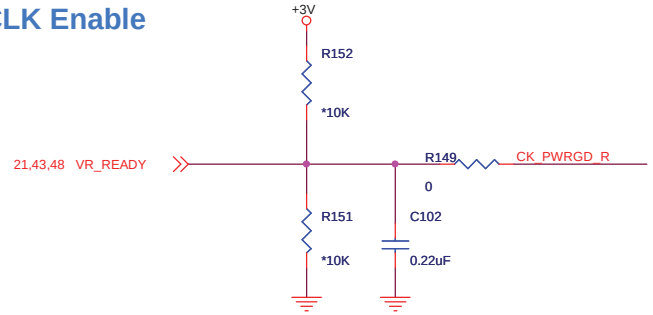


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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Size	Document Number	Rev
	Clock Generator	F
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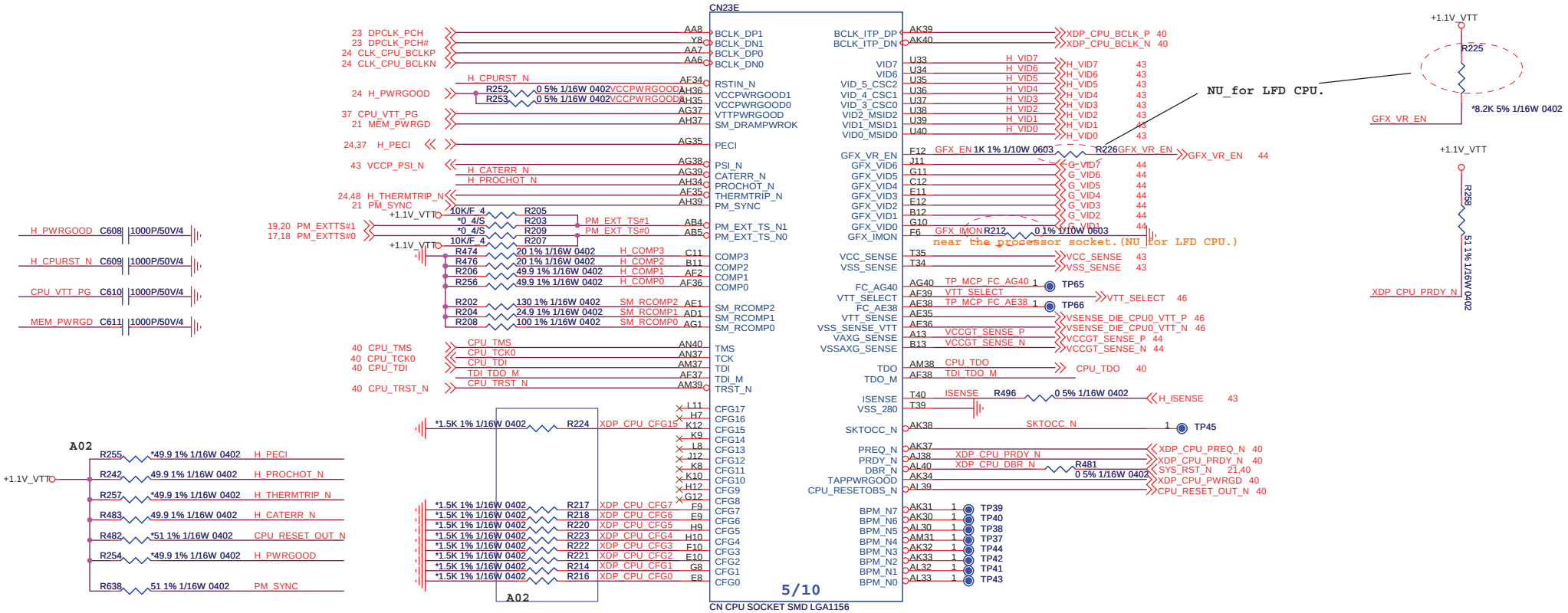
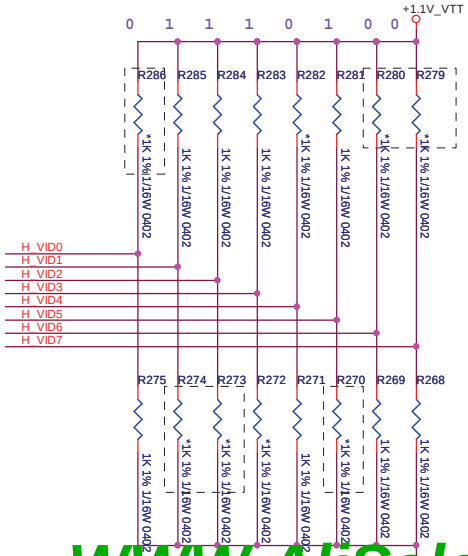


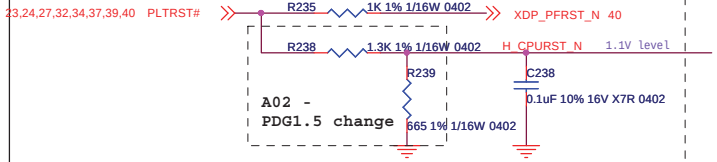
CFG	H	L	Notes
0			H:1x16, L:2x8
1	RSVD		
2	RSVD		
3	NORM	RSVD	LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		

CFG 0-6 all internal PULL-UP

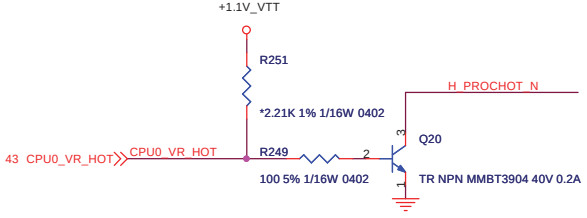
VID[7:0] : 00101110 =>1.325V@VCC,Max
2009B FMB processors supported



Need to be placed close to processor
to minimize ESD risk



CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU



Quanta Computer Inc.			
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Size	Document Number		Rev
	MCP (CLK/CTRL/MISC)		F
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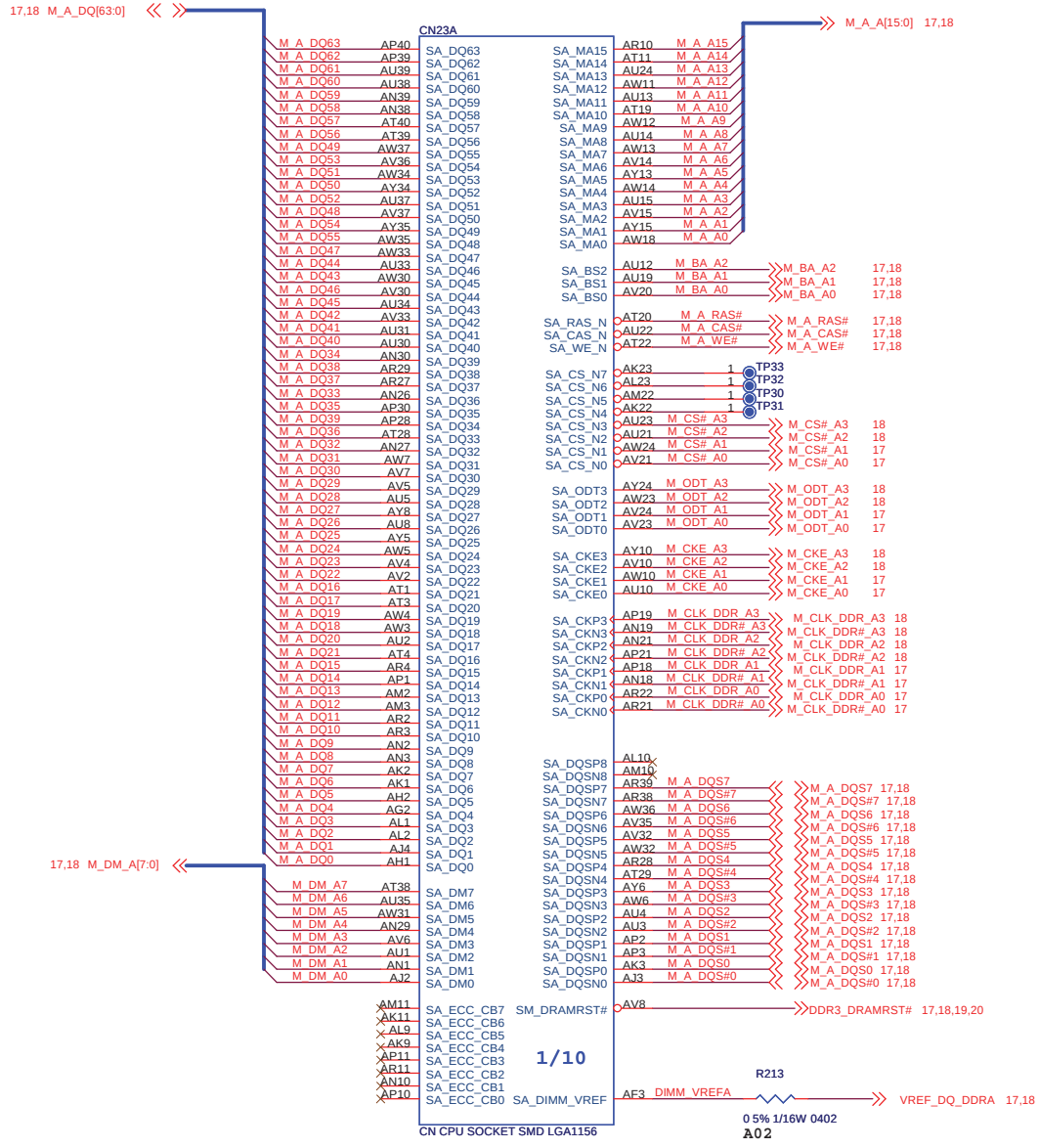

Quanta Computer Inc.

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Size	Document Number	Rev
	MCP (DDR3 CHANNEL A)	F

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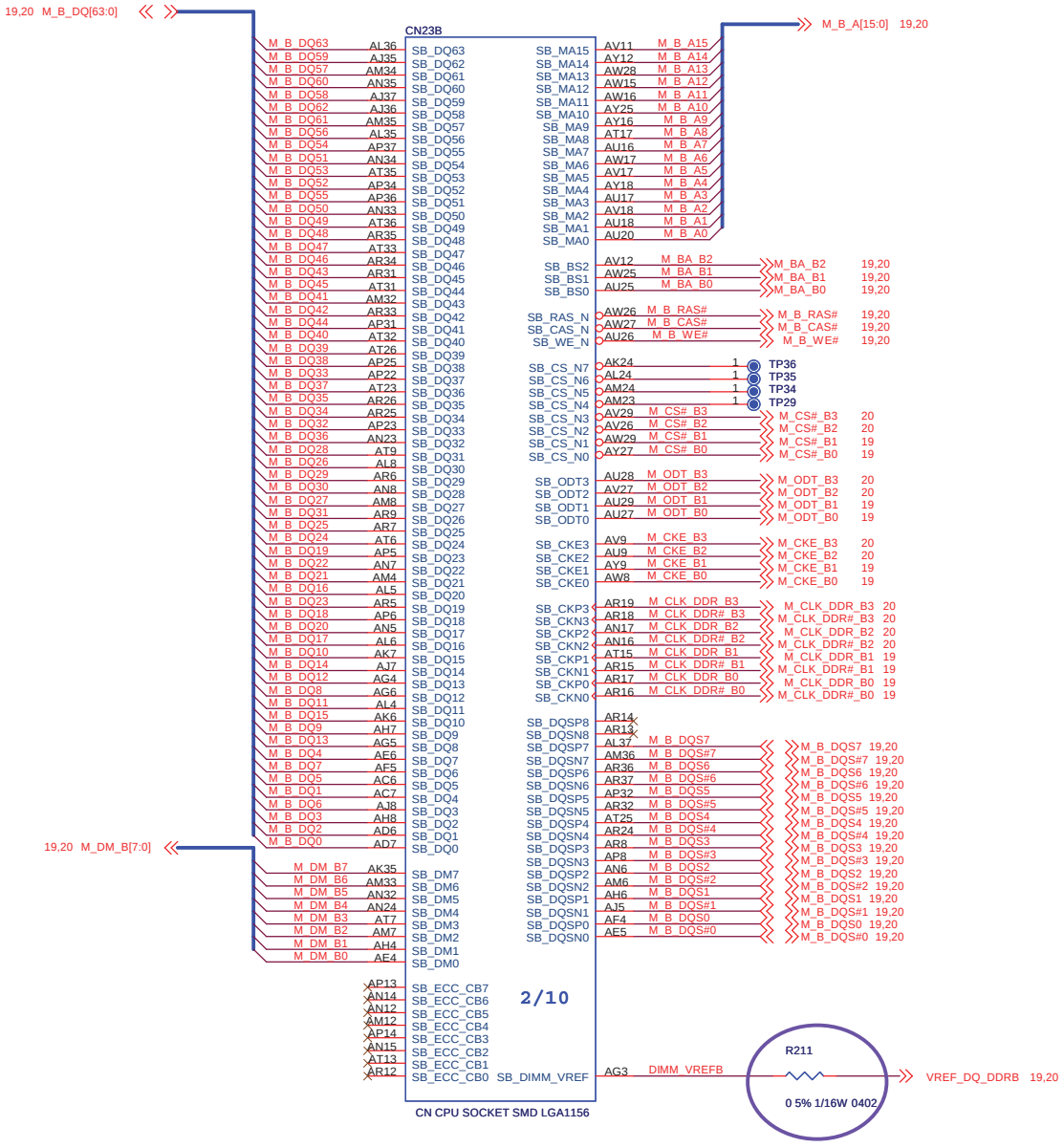

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Size	Document Number	Rev
	MCP (DDR3 CHANNEL B)	F

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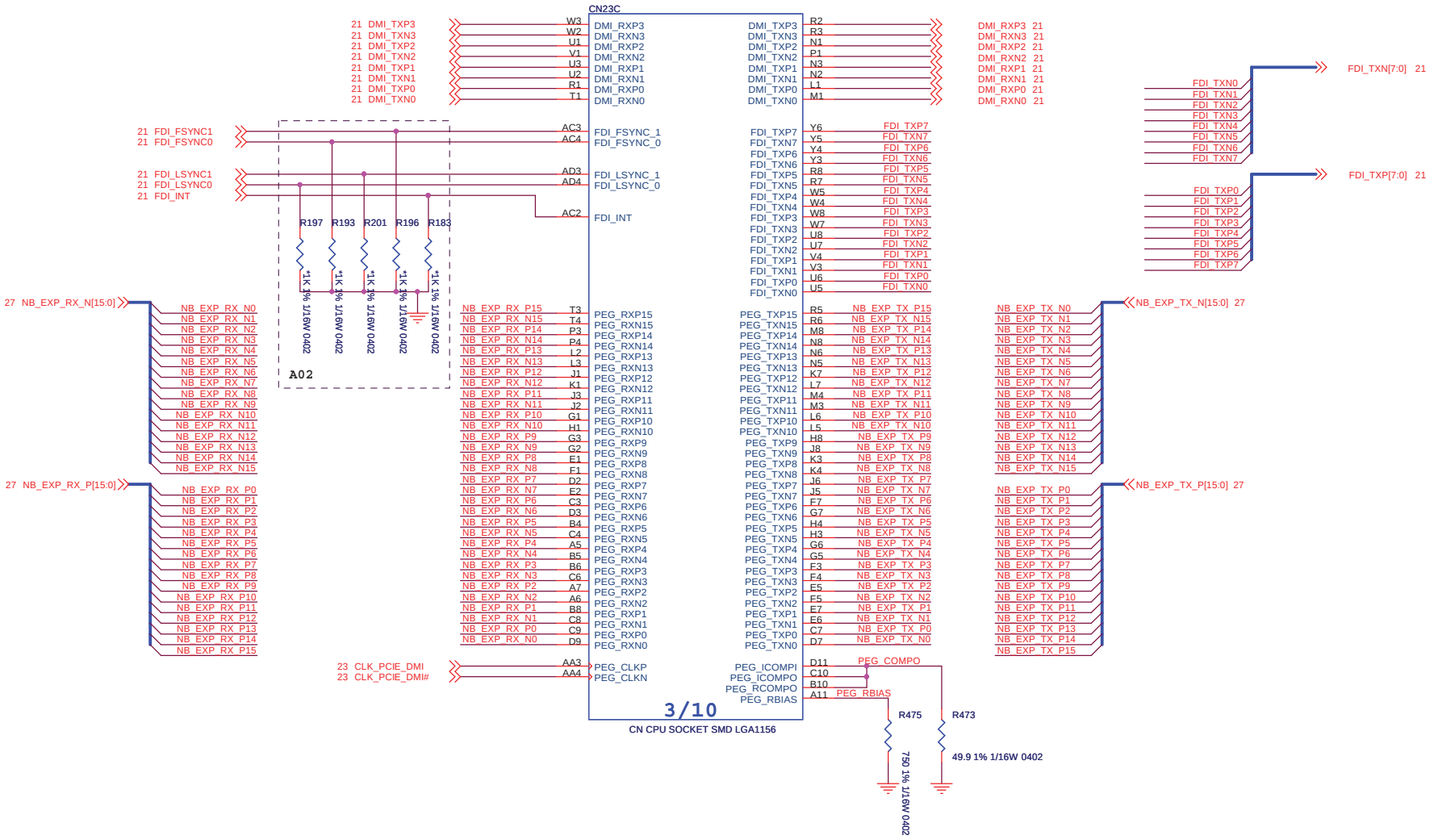

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Size	Document Number	Rev
	MCP (PCIE/DMI)	F
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Size	Document Number	Rev
	MCP (VCCP)	F

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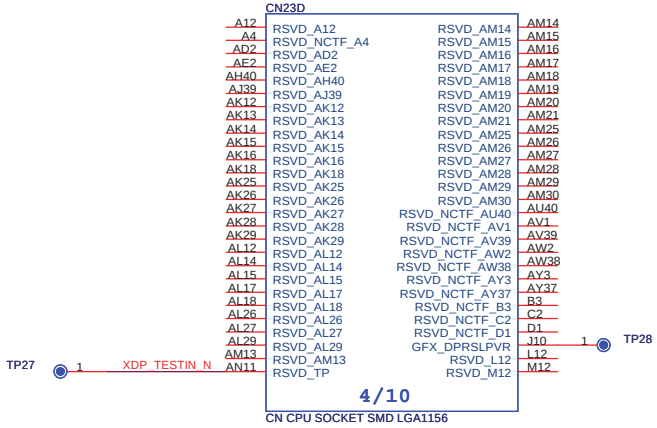

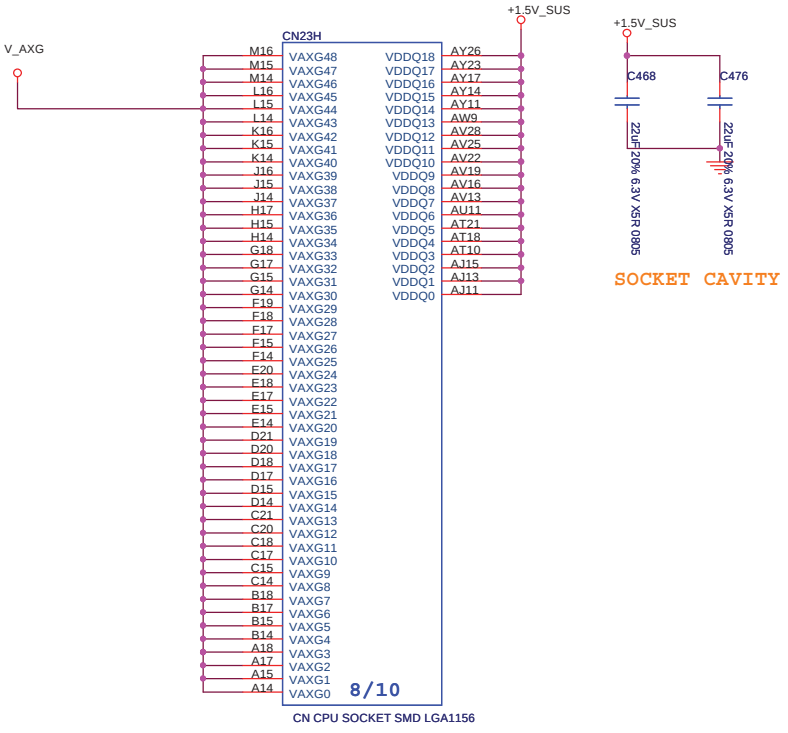

Quanta Computer Inc.
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Size	Document Number	Rev
	MCP (MISC/VCC)	F
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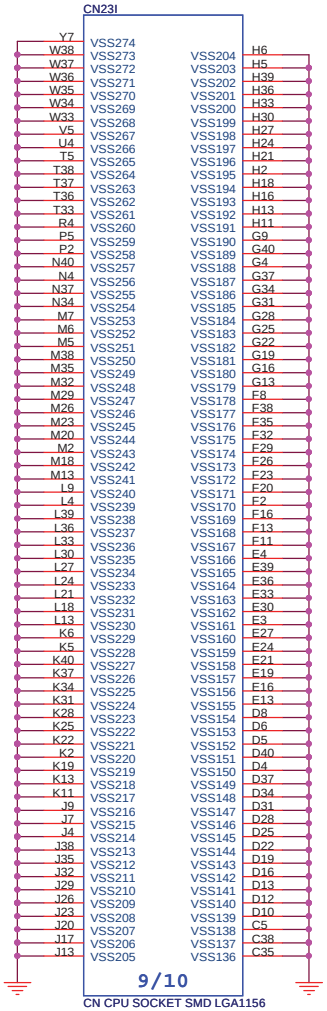

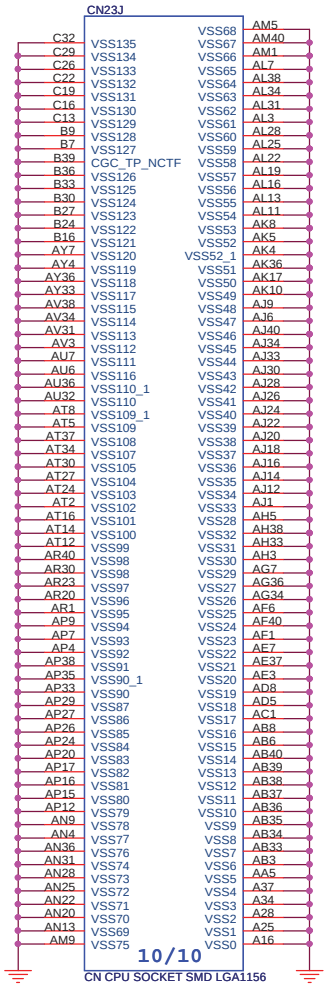

Quanta Computer Inc.

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Size	Document Number	Rev
	MCP (GND)	F

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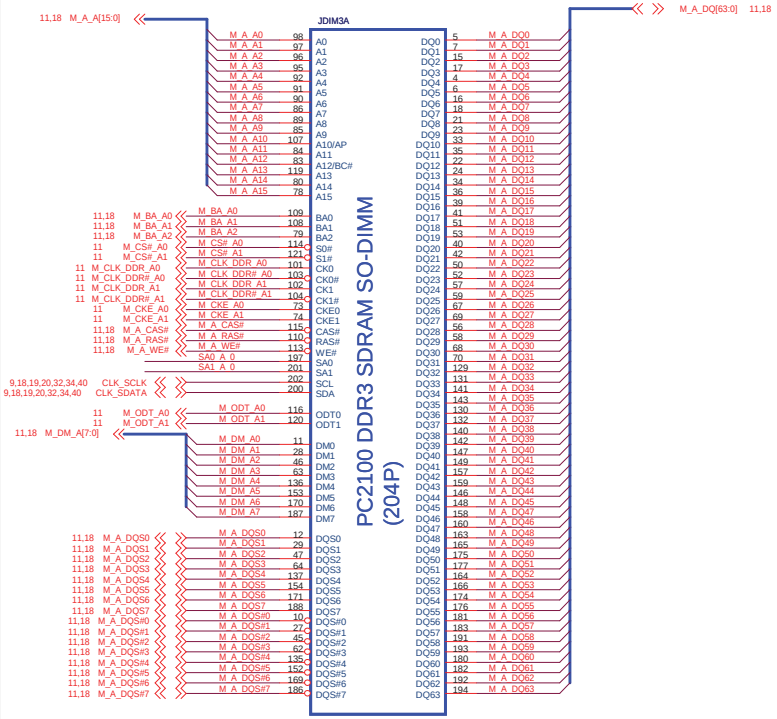
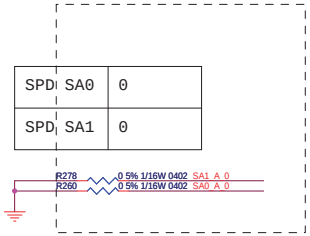
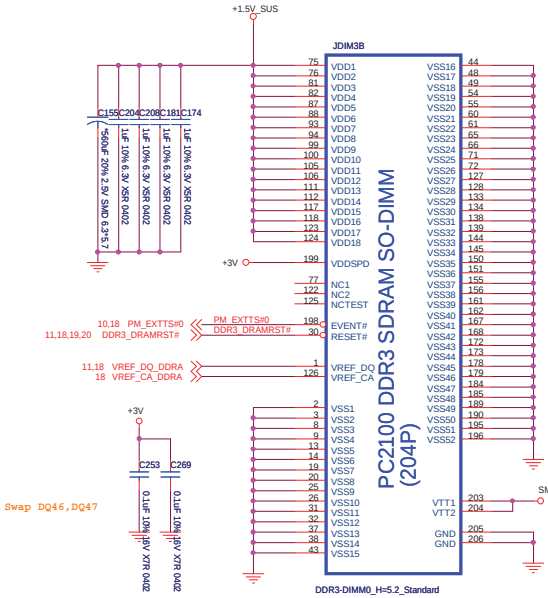
CHANNEL A DIMM 0

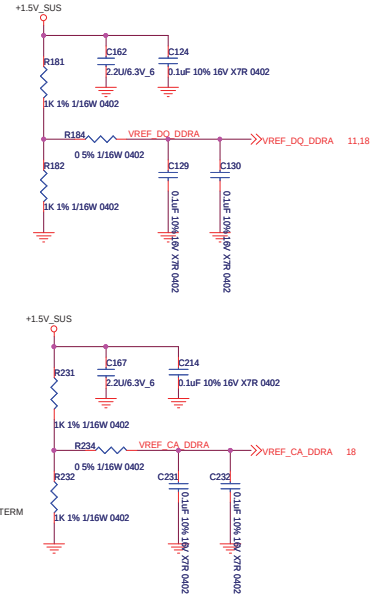


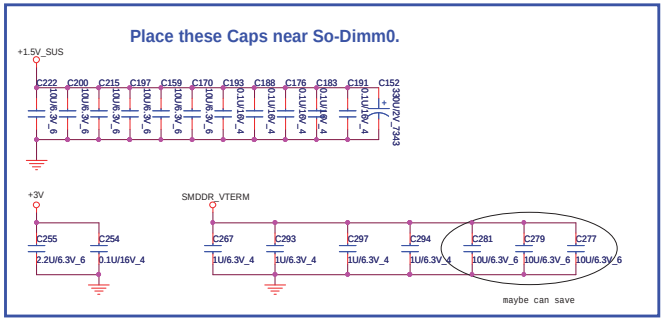


PCH

FOX H:9.2 white
PCB Placement







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Size	Document Number	Rev
	DDR3 CHA DIMM 0	F

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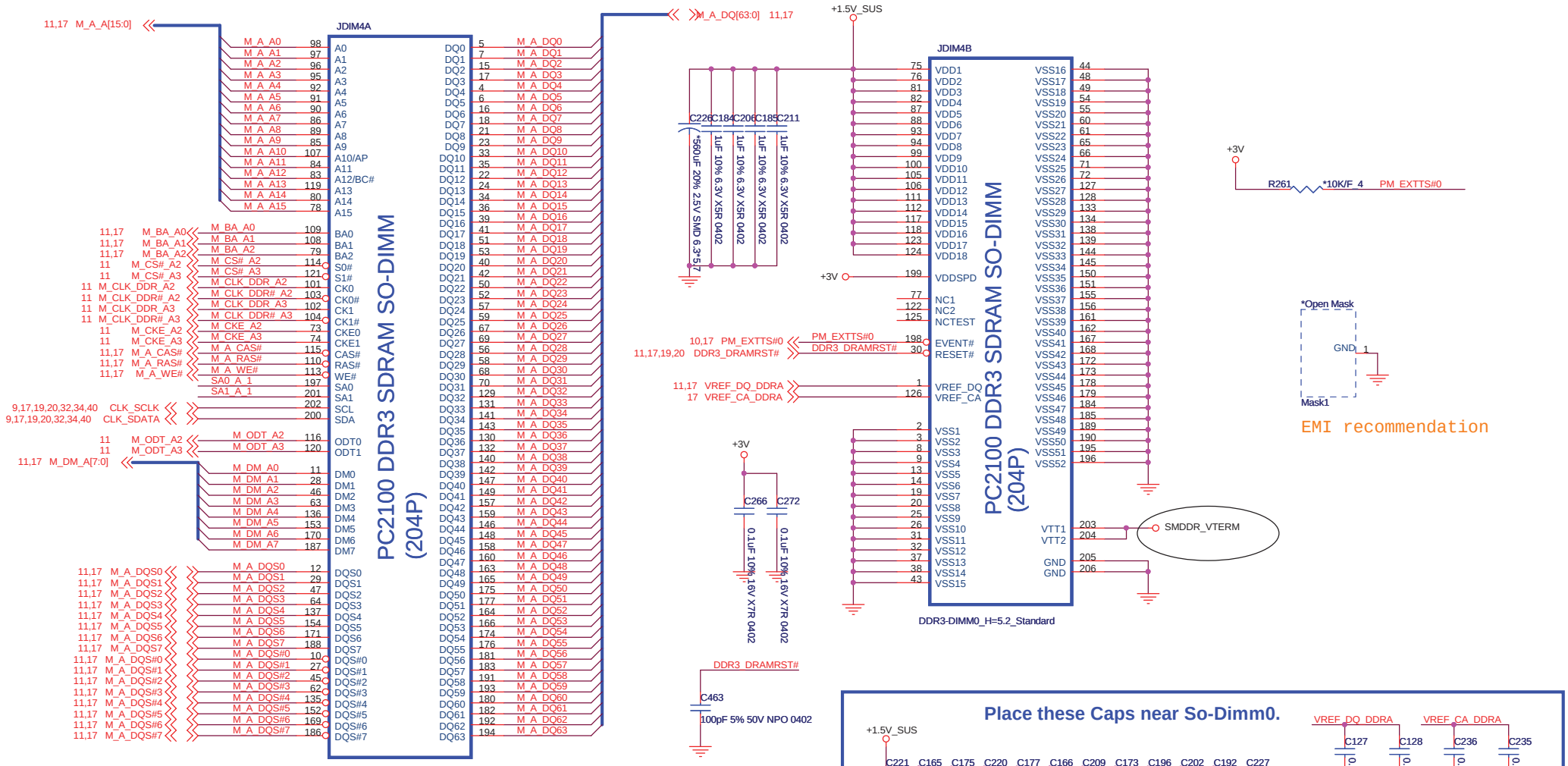
CHANNEL A DIMM 1



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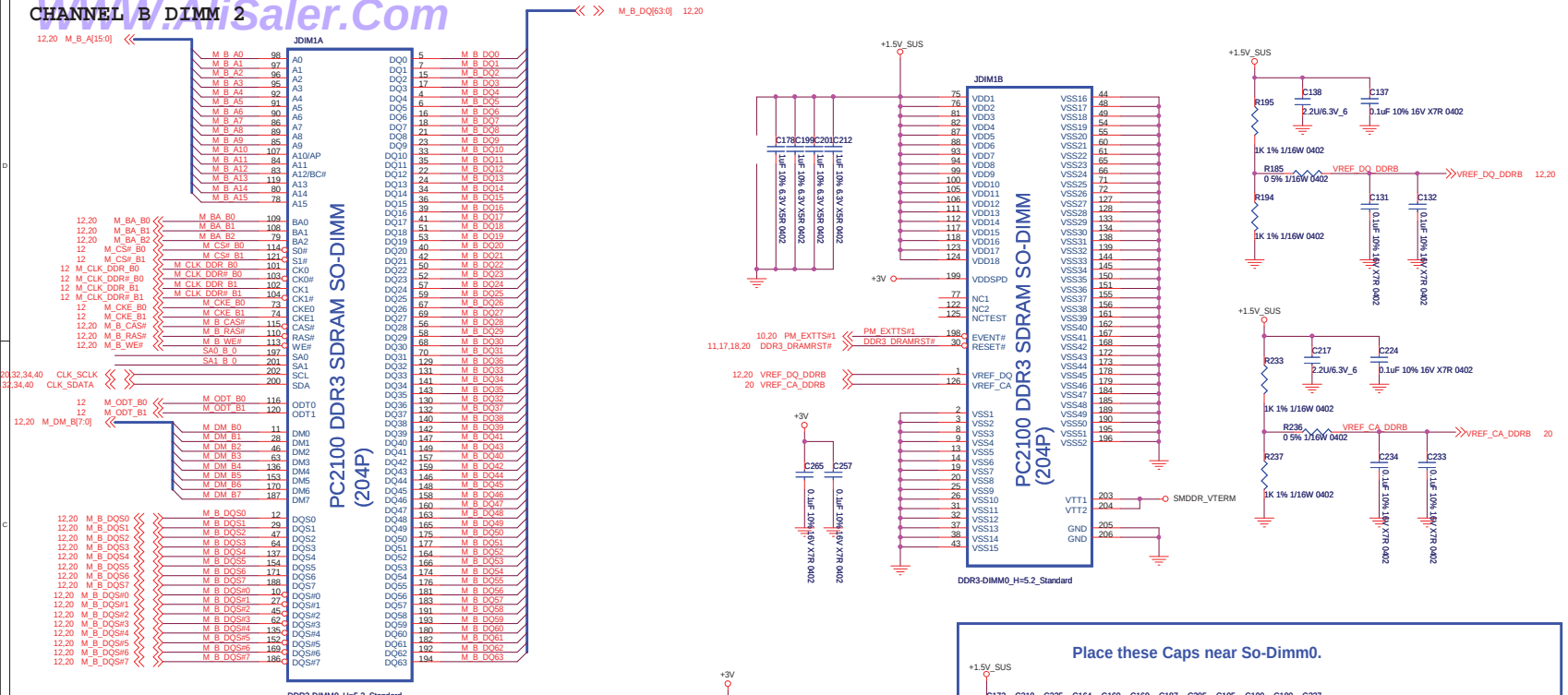
CHANNEL B DIMM 2



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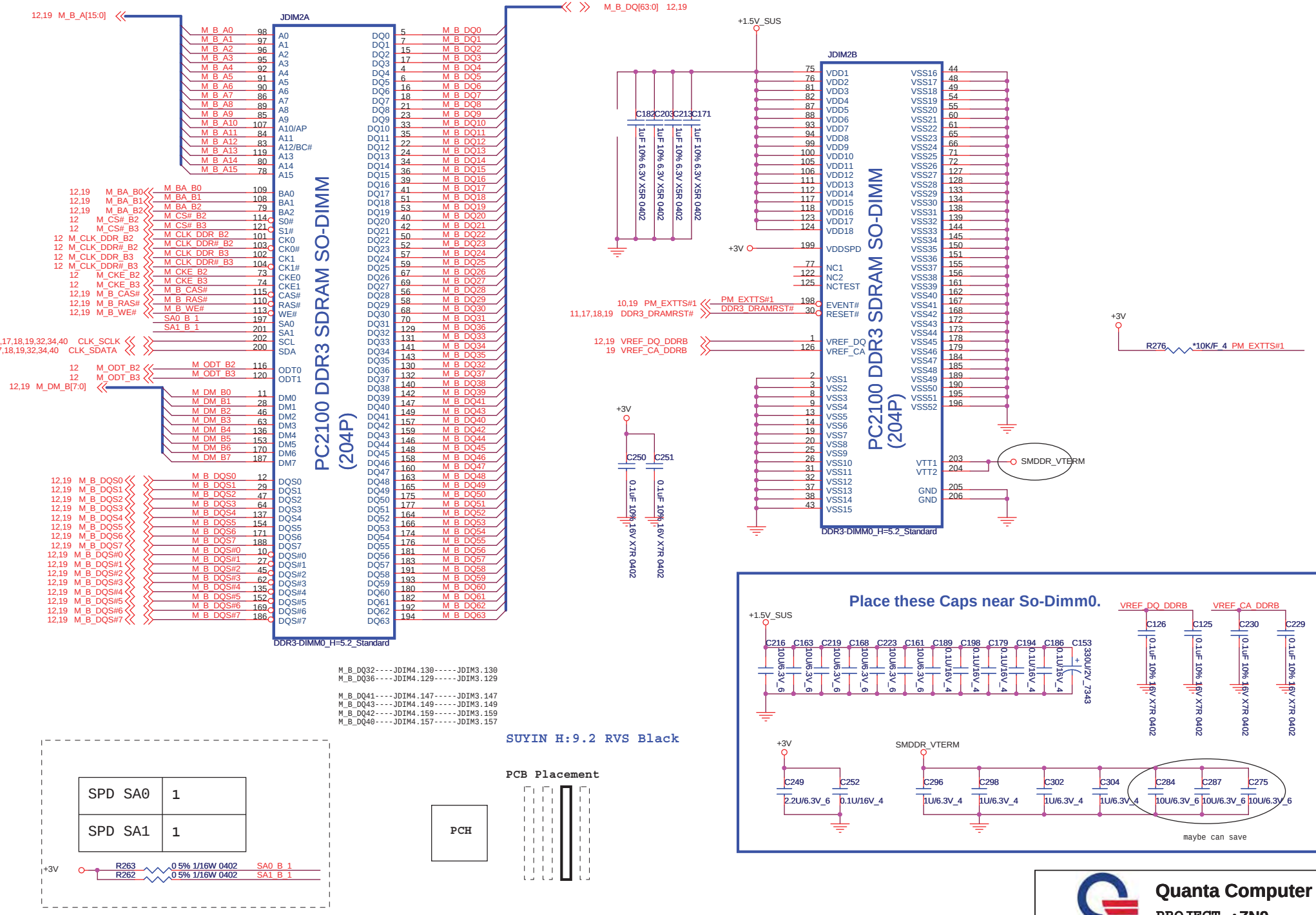
CHANNEL B DIMM 3



SPD SA0	1
SPD SA1	1

+3V R263 0 5% 1/16W 0402 SA0_B_1
R262 0 5% 1/16W 0402 SA1_B_1

SUYIN H:9.2 RVS Black

PCB Placement

PCH

Quanta Computer Inc.

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	DDR3 CHB DIMM 1	F

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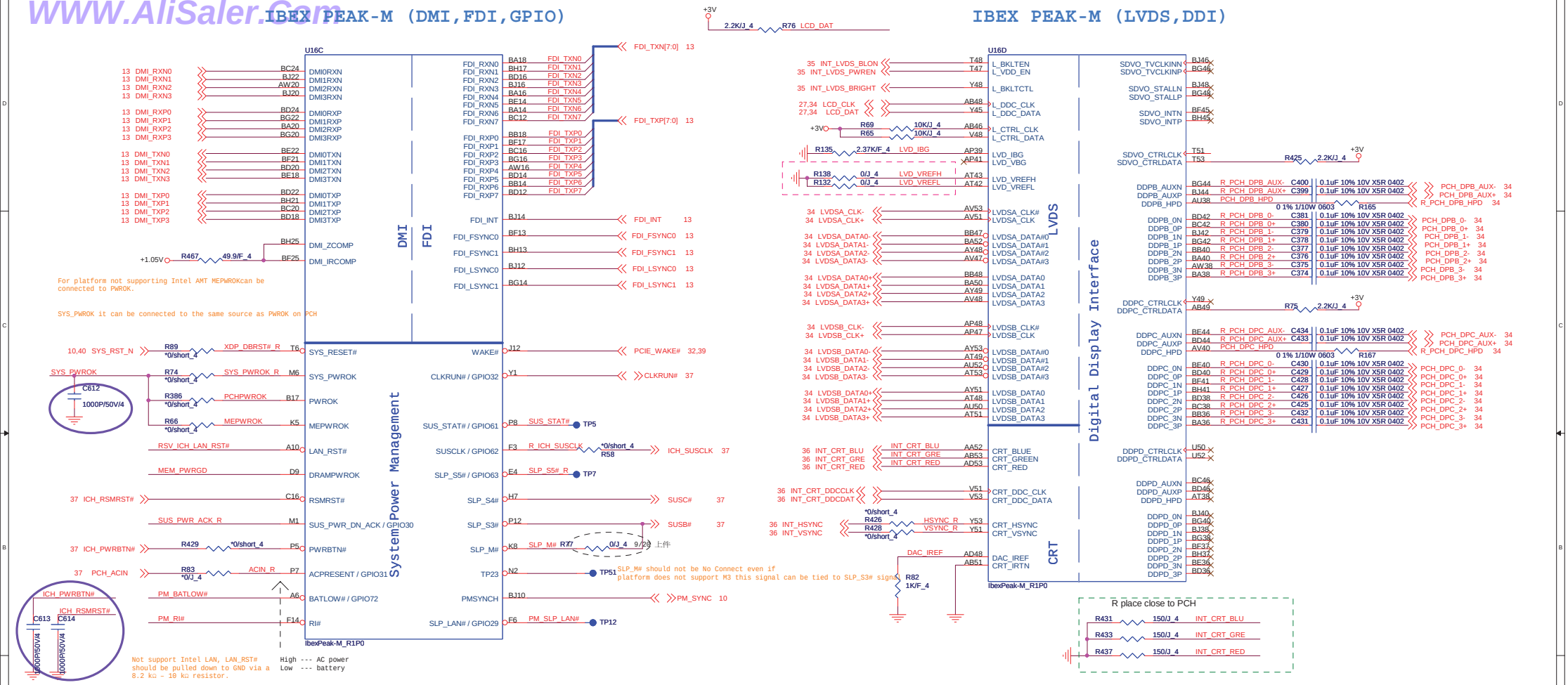
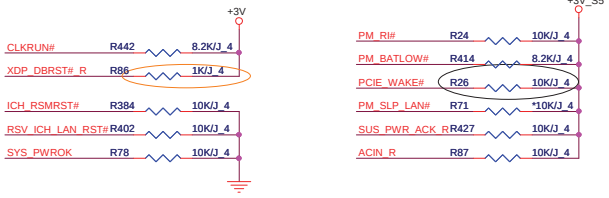
IBEX PEAK-M (DMI,FDI,GPIO)

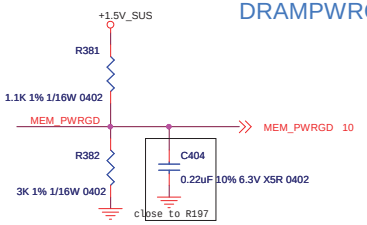
IBEX PEAK-M (LVDS,DDI)



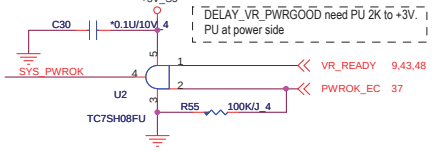
PCH Pull-high/low



DRAMPWROK



System PWR_OK



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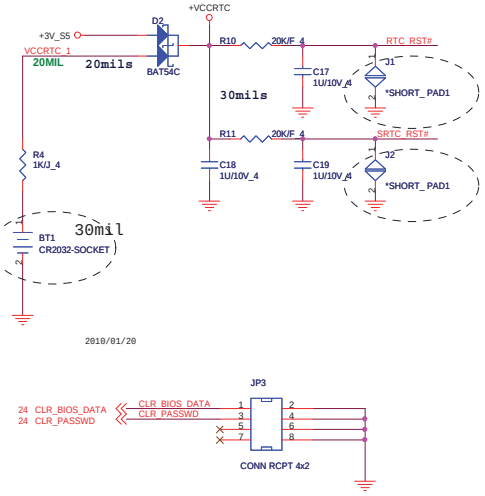
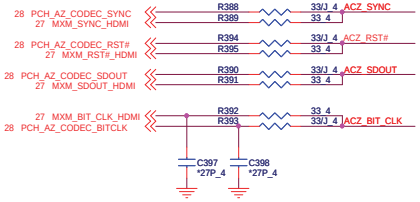
RTC Circuitry

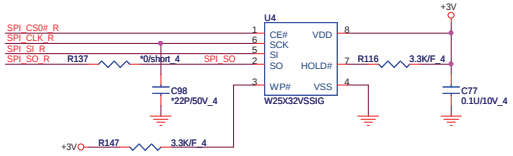


HDA Bus

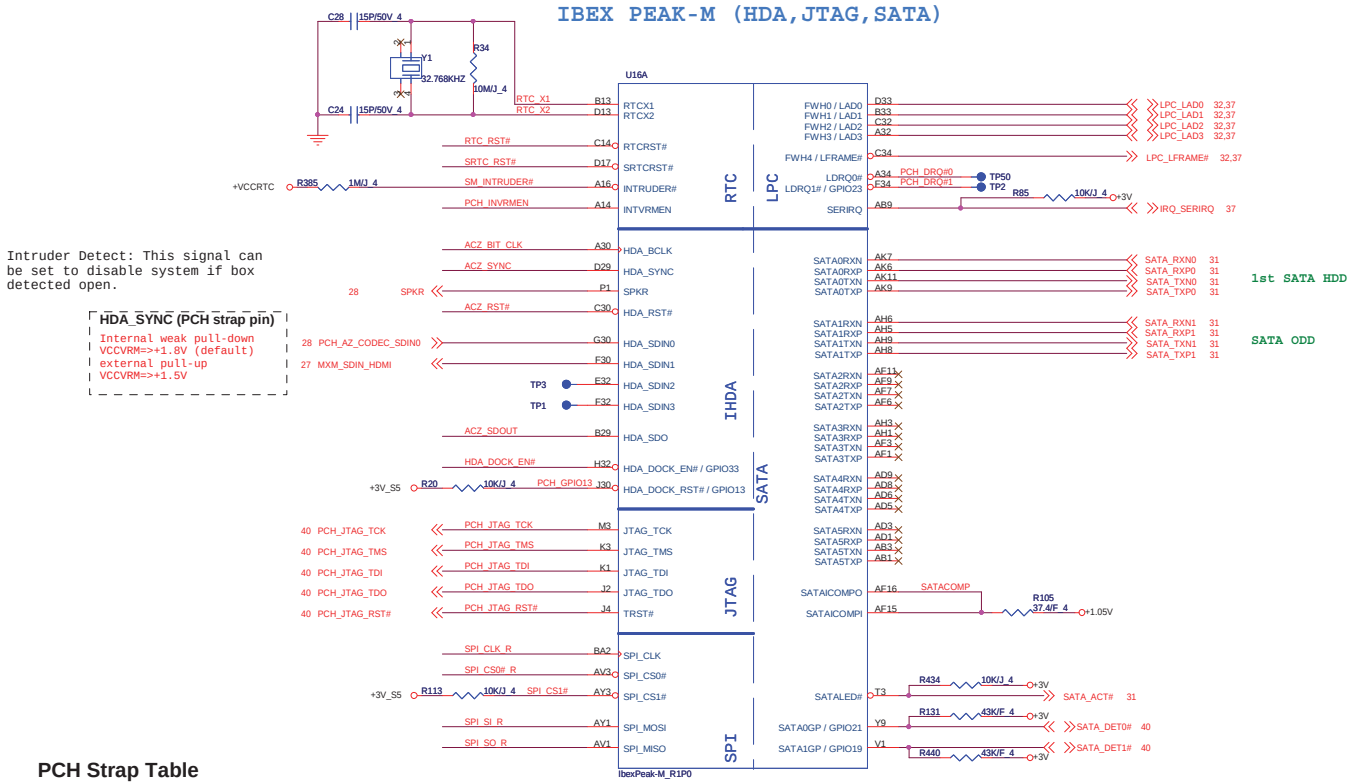


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



IBEX PEAK-M (HDA,JTAG,SATA)



Intruder Detect: This signal can be set to disable system if box detected open.

HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZN7 note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R432 *10K/J_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R410 *10K/J_4 PCI_GNT3# 23
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC R383 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V R49 *1K/J_4 R54 *1K/J_4 R48 *1K/J_4 R53 *1K/J_4 PCI_GNT0# 23 PCI_GNT1# 23
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R457 *1K/J_4 NV_ALE NV_ALE 23
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R156 *1K/J_4 NV_CLE NV_CLE 23
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R18 *1K/J_4 R17 *10K/J_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R456 *1K/J_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R63 10K/J_4 RSV_GPIO8 24
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R100 1K/J_4 CR_WAKE# 24

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Size | Document Number: PCH (SATA/RTC/HDA/LPC) | Rev F
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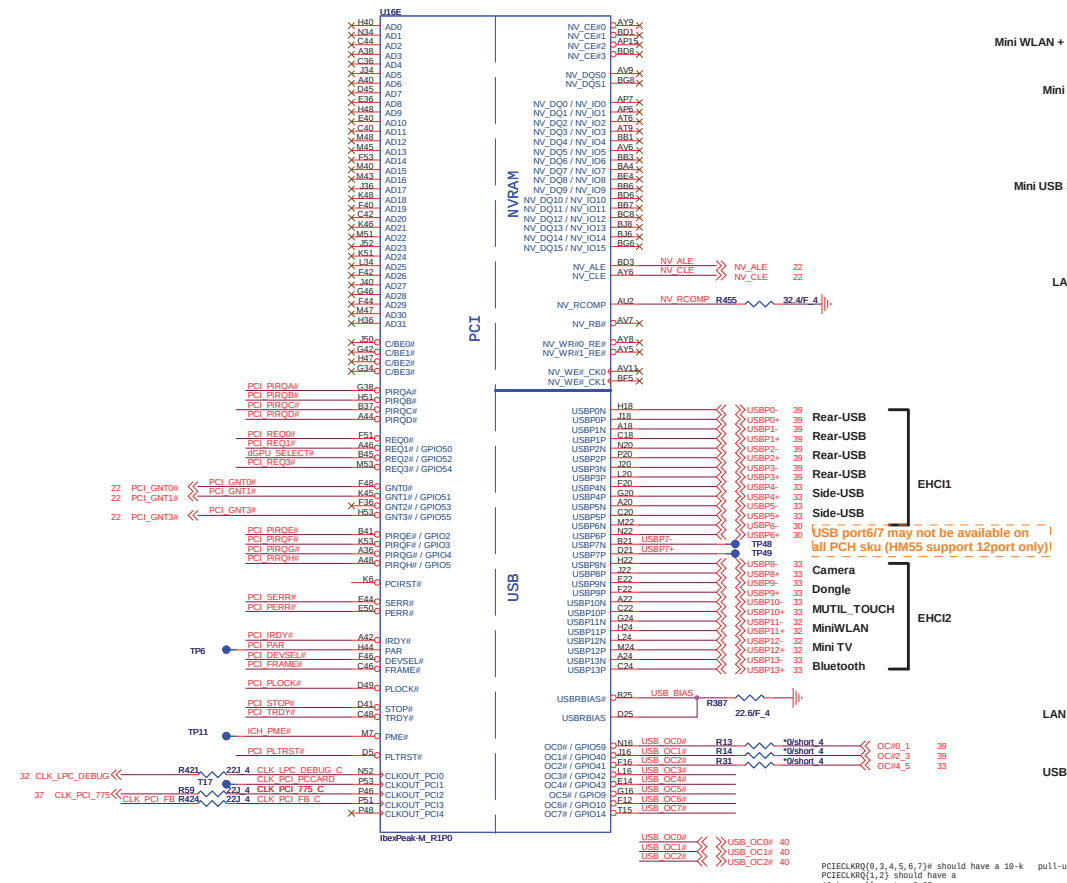
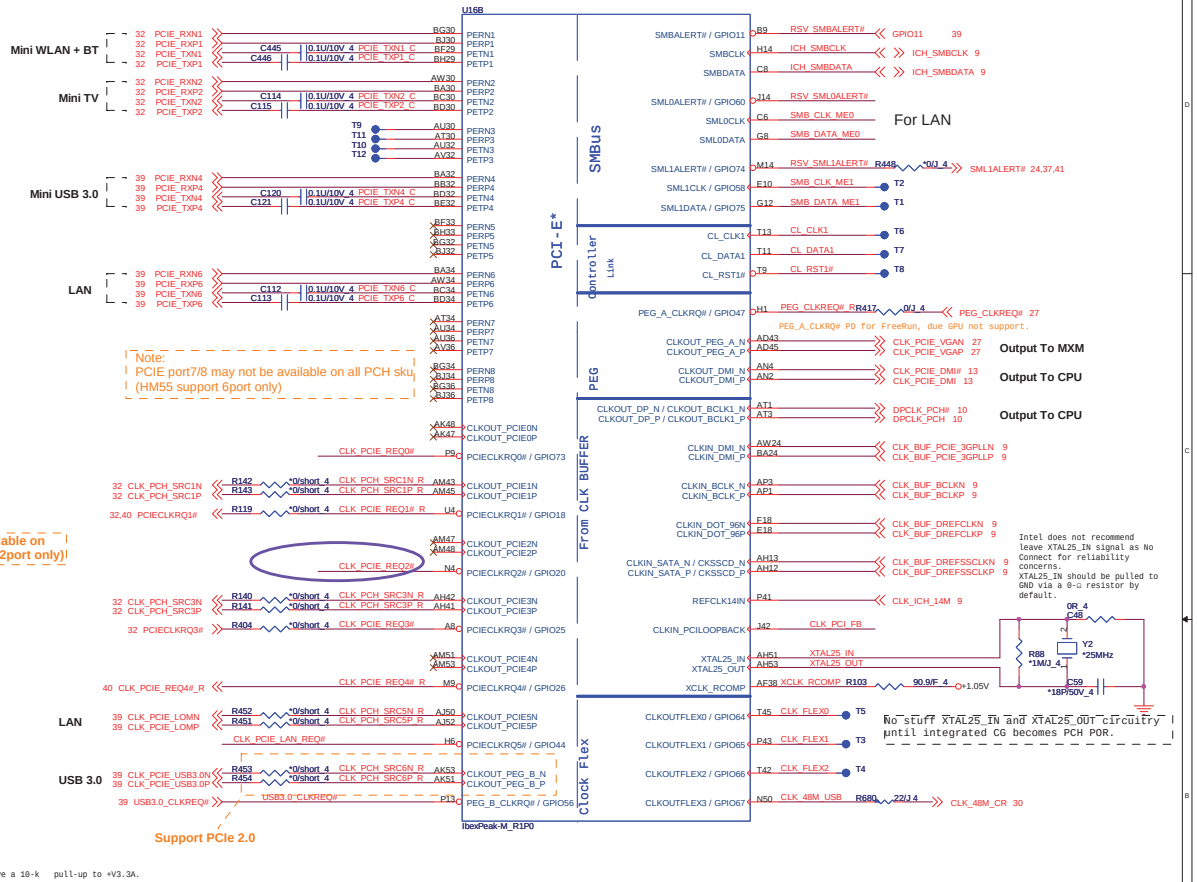
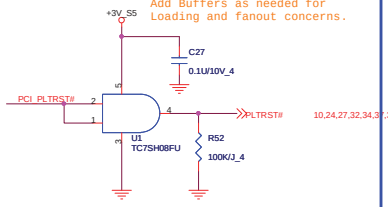
IBEX PEAK-M (PCI,USB,NVRAM)



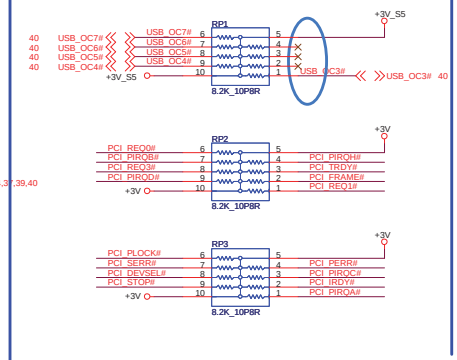
IBEX PEAK-M (PCI-E,SMBUS,CLK)



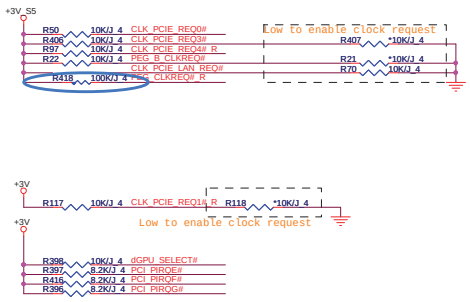
PLTRST#



PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

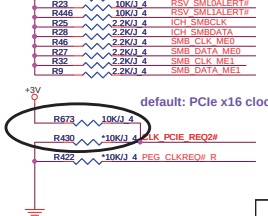
Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

01/13 stuff the R673 to pull high to +3V; un-stuff the R430

SMBus/Pull-up



PCIECLKRQ(0,3,4,5,6,7)# should have a 10-k pull-up to +V3.3A.
PCIECLKRQ(1,2) should have a 10-k pull-up to +3.3S

No stuff XTAL25_IN and XTAL25_OUT circuitry until integrated CG becomes PCH POR.

Intel does not recommend leave XTAL25_IN signal as No Connect for reliability concerns. XTAL25_IN should be pulled to GND via a 0~Ω resistor by default.

Quanta Computer Inc.			
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	PCH (PCIE/USB/CLK/NV)		F
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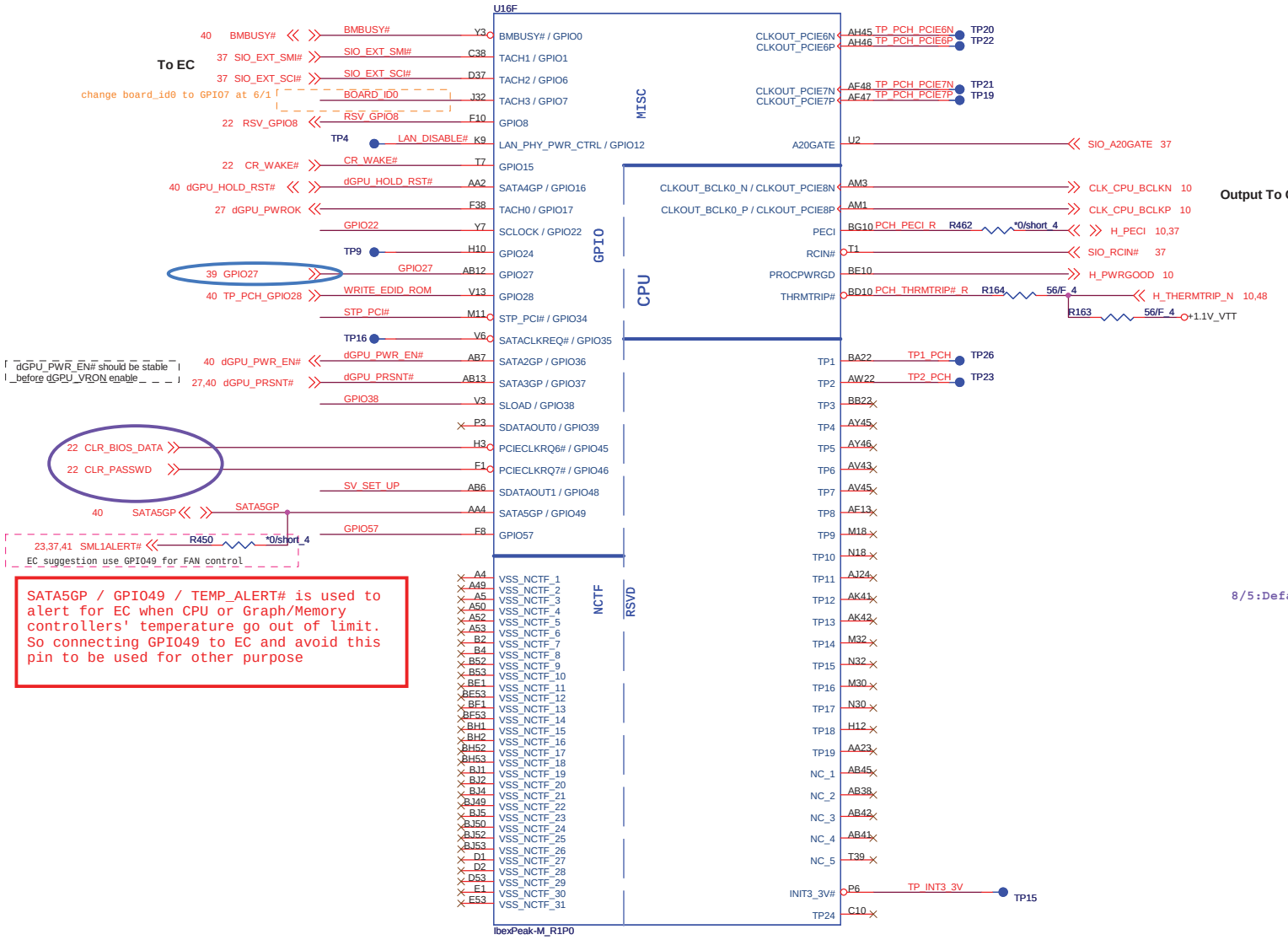
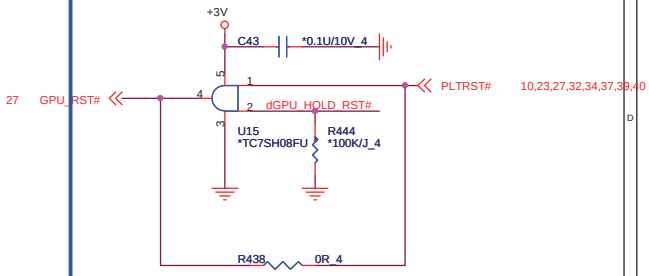
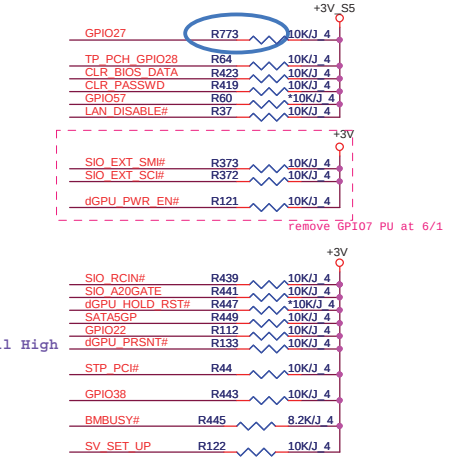
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPU RST#



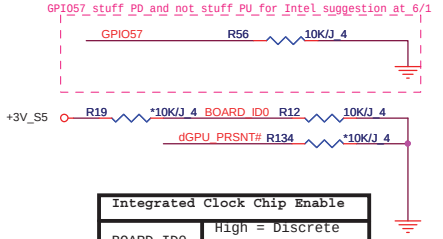
GPIO Pull-up/Pull-down



8/5:Default Pull High

SV_SET_UP	1-X High = Strong (Default)

GPIO57 stuff PD and not stuff PU for Intel suggestion at 6/1



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

Quanta Computer Inc.
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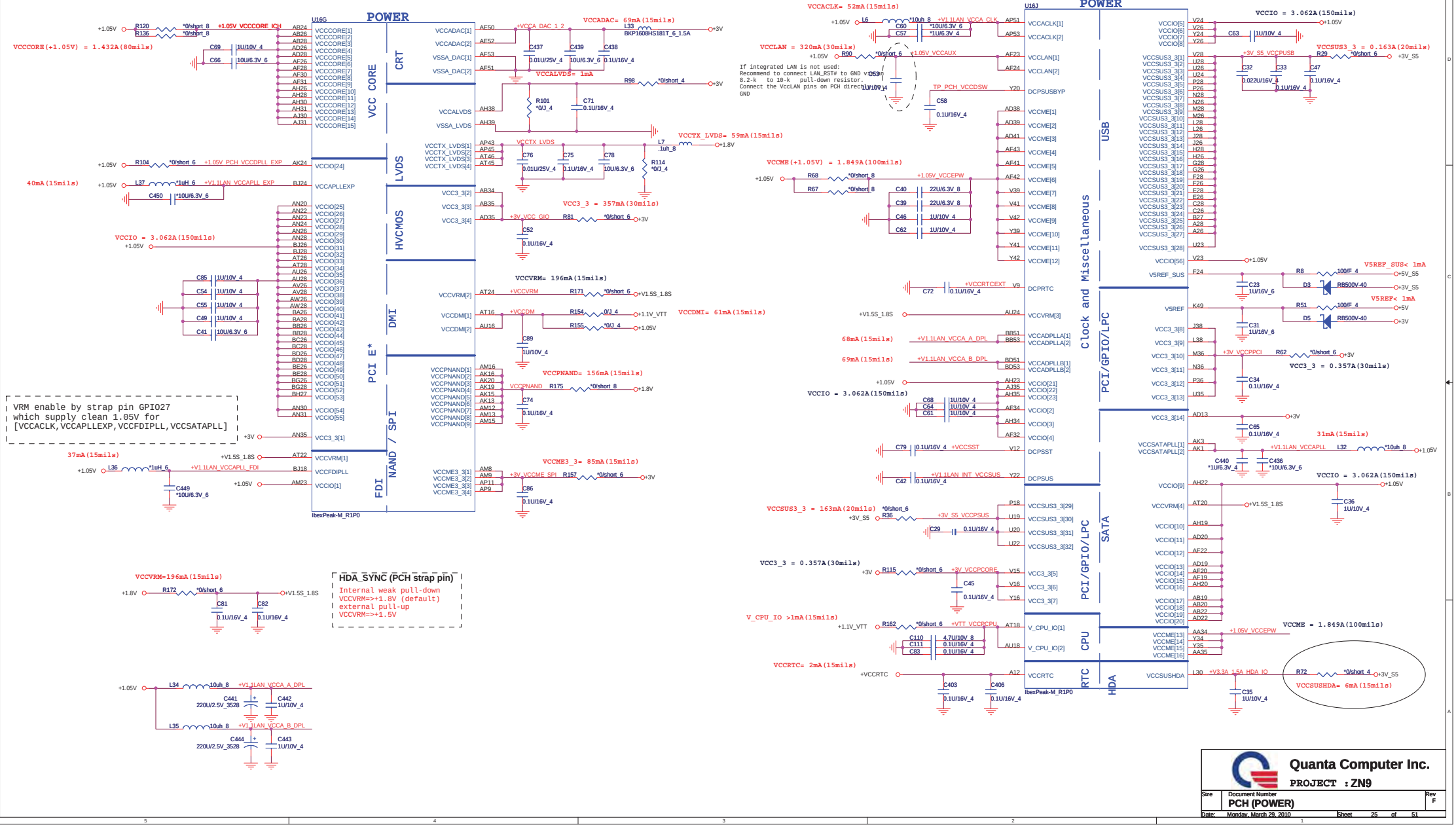
IBEX PEAK-M (POWER)



Quanta Computer Inc.
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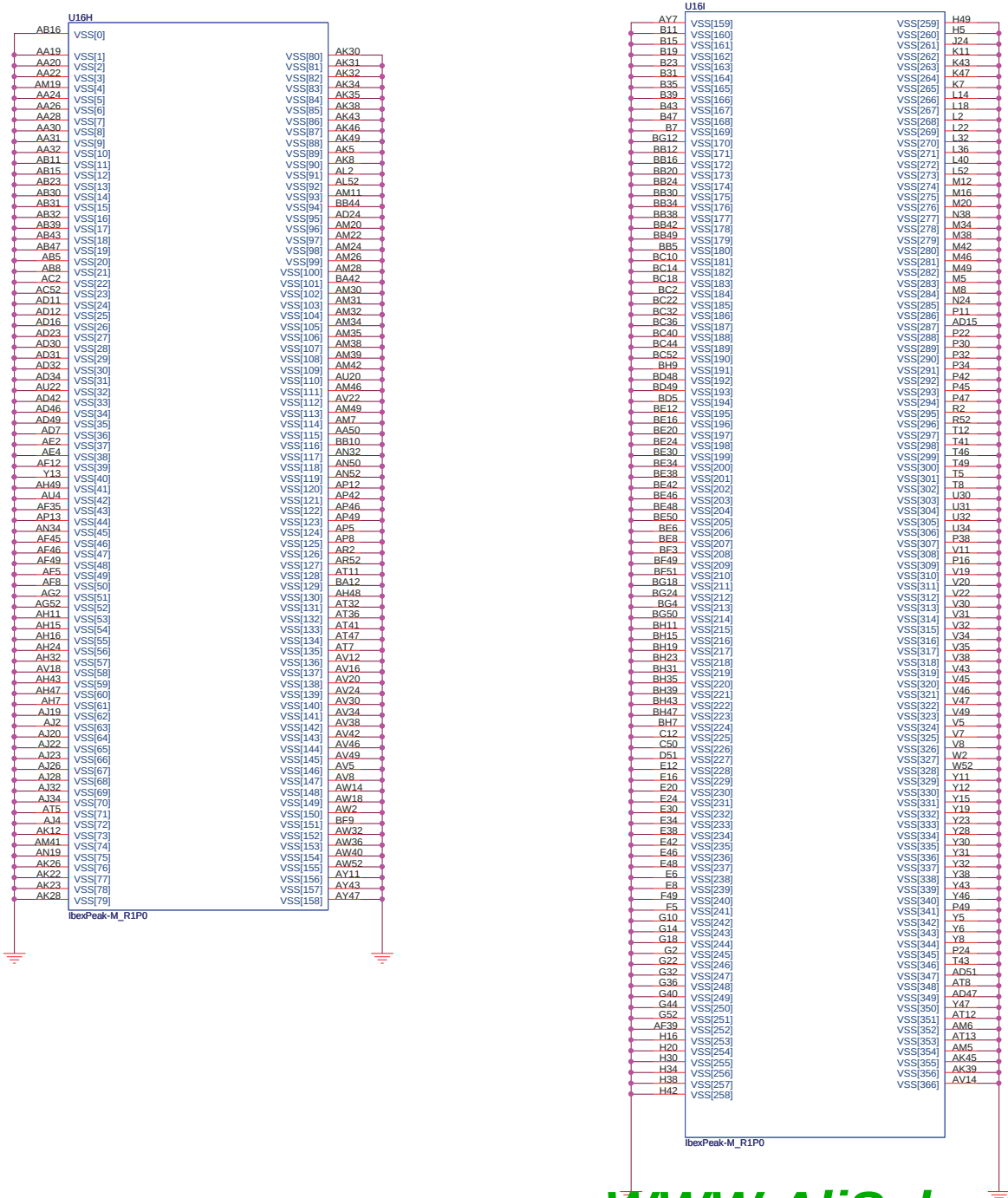
IBEX PEAK-M (GND)



Quanta Computer Inc.

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MXM Module

7~20V
Check Footprint and P/N

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	N/A	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

7/28: add decoupling capacitors for AMD recommendation

02/05 Change CN24 P/N to DFHSW4FR014

7/28: pull-up resistor for AMD recommendation. (AMD:10K ohm pull-up resistor)

02/03 Exchange the MXM DP link from DP-B to DP-C

Thermo SMBus

MXM VIN Power switch

MXM 3V/5V Power switch

MXM DP(Port C) CONN for Scalar Board

3Amp

LVDS+DP(Port A) CONN for MXM

To low power status mode

To EC

For CRT Debug

01/13 Change the CON5 P.25 Netname from "8028_RST" to "PLTRST#"
01/27 Change the Scalar Board CON5 P.6 from 12V to 3V
02/01 Stuff the D4 for ESD test
02/05 Change the CON5(DP CONN) from right angle type to vertical type (DFHD30MS760)
02/05 Change the CON5(DP CONN) P1,P3,P5 connector +5V power rail for fix scalar power sequence

02/05 Change CON2 P/N to DFWF50MR004

Quanta Computer Inc.	
PROJECT : ZN9	
Size	Document Number: MXM 3.0
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CODEC

92HD89D3

IC AUDIO CODEC 92HD89D3

Analog

Digital

12/8 AC5/AC6 change to 00ohms by IDT demanded

1/20 AC17/AC19 from 1u to 10u solved the THD issue.

1/20 AC20/AC21 from 1u to 100u solved the THD issue.

1/20 AC14/AC16/AC18 from 1u to 10u solved the THD issue.

1/20 AC22/AC23 from 1u to 100u solved the THD issue.

AC7/AC8 place near U20 Pin9

C568/C567 place near U20 Pin1,3

12/8. AR21 need move to close the MIC by IDT demanded

12/8 resistors change to null by IDT demanded

VOUT = 1.25 (1+R1/R2)

R1 4.8375V 28.7K R2 10K

2nd source : G923-330T1U

AL000923003

12/8. AU2 current too small, when use we need to find other by IDT demanded

11/30. change net name HPL and HPR to HPL1 and HPR1

AC41 should near AU3

AC57 should near AU6

01/27 HP request to change the AU3/AU6 from DRV603 return to DRV601

BUZZER

BZ 3.6V 90DB 8.5*8.5MM DNGJ4B20001

MMBT3904 40V 0.2A

MUTE

Check

EC

PCH CODEC_RST

LINE IN/Mic Reserved Jack

11/25 cancel BAT54C*2 by IDT demanded

02/01 stuff the AD3,AD4,AD5 for ESD TEST

02/05 Change CN39/CN40 P/N from DFTJ07FR017 to DFTJ07FR033

HeadPhone/Mic Combo Jack

11/25 add filter by IDT demanded

1/26 change 22ohm to 16ohm for meet 2Vrms output.

11/25 value change 100P to 0.01u by IDT demanded

02/01 stuff the AD7,AD8,AD9,AD10 for ESD TEST

AC97/ALC SCHEMATIC (AFTER PLUG IN)

AC97 ALC SCHEMATIC (BEFORE PLUG IN)

Quanta Computer Inc.	
PROJECT : ZN9	
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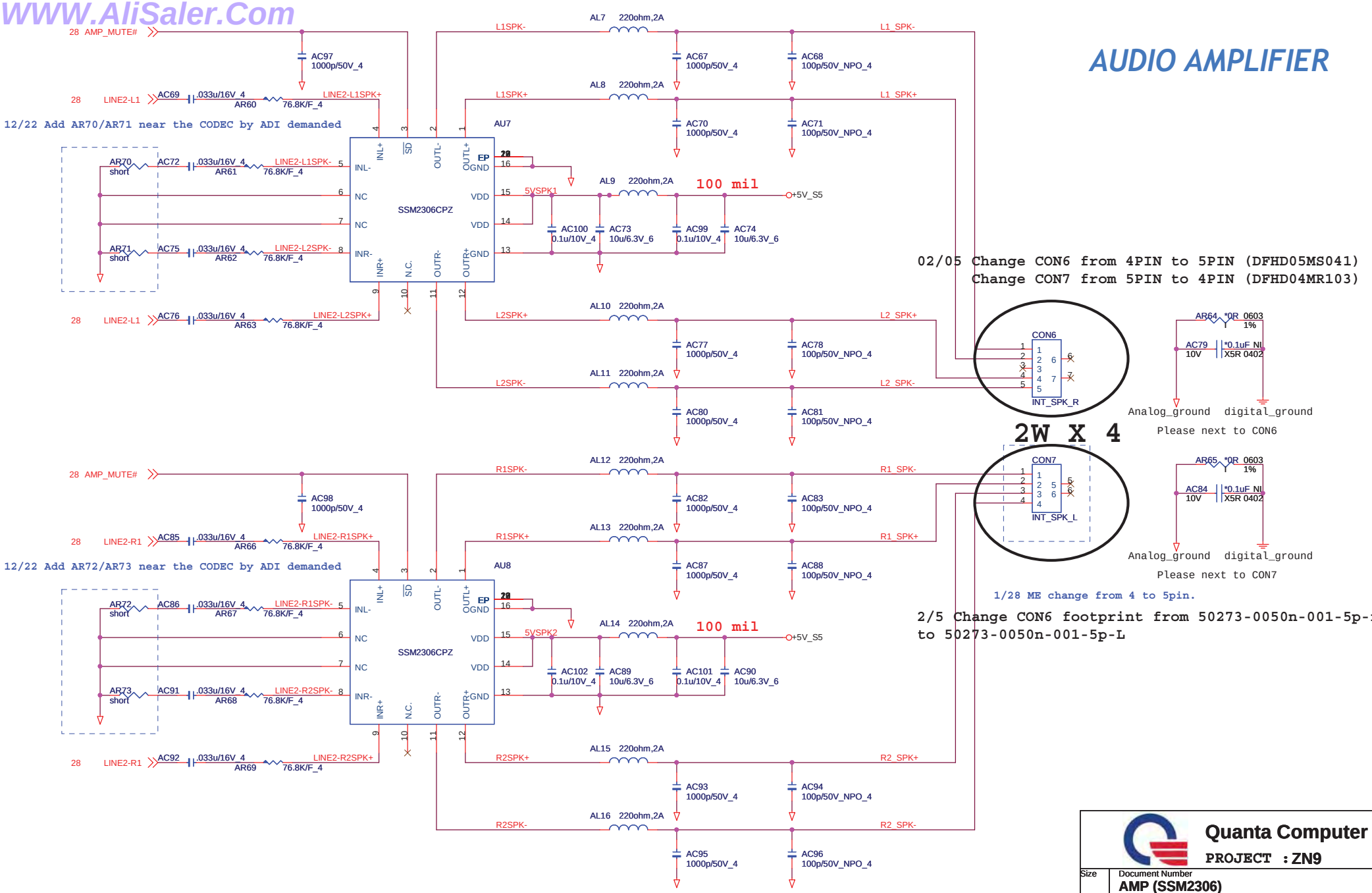
AUDIO AMPLIFIER



Quanta Computer Inc.		
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Size	Document Number: AMP (SSM2306)	Rev F
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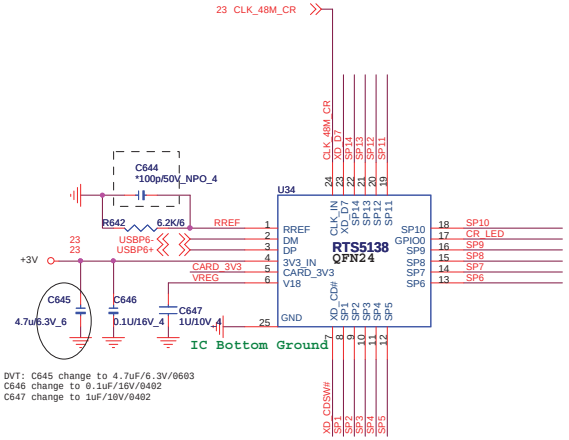
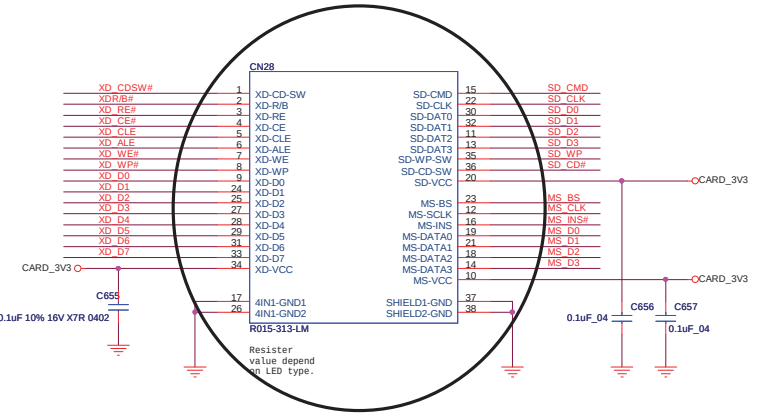
6 IN 1 CARD READER

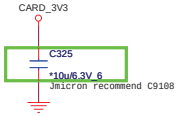


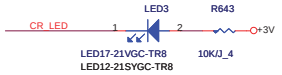
DVT: C645 change to 4.7uF/6.3V/0603
C646 change to 0.1uF/16V/0402
C647 change to 1uF/10V/0402



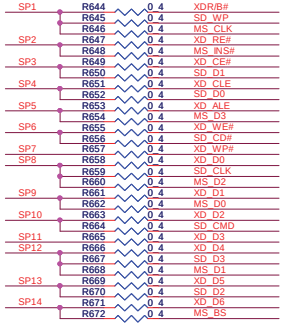
02/08 Change CN28 P/N to DFHS38FR002

As close as possible to CCN28 Pin38





HPspec: It illuminates when a card is inserted into the connector and flashes with read/write activity.



Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	

Quanta Computer Inc.
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	JMB380 CR &1394	F
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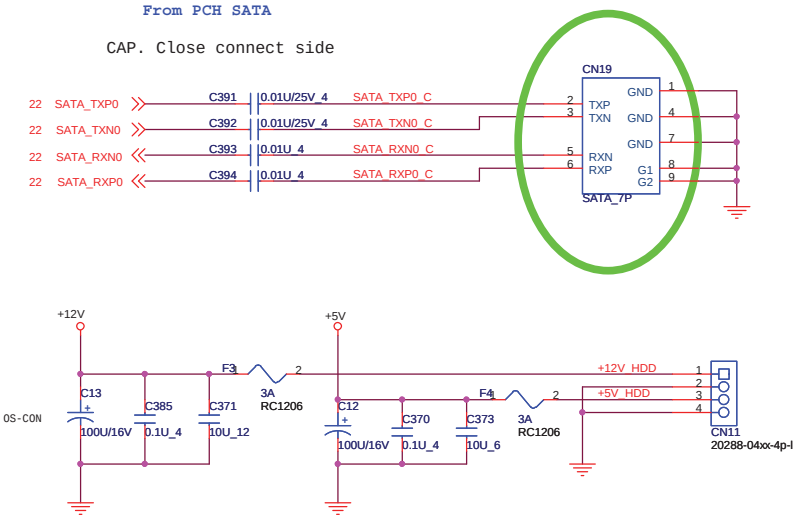
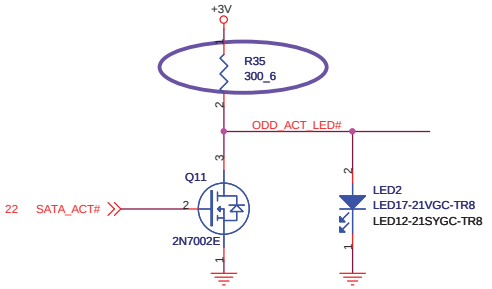
1st 2.5"/3/5" SATA HDD

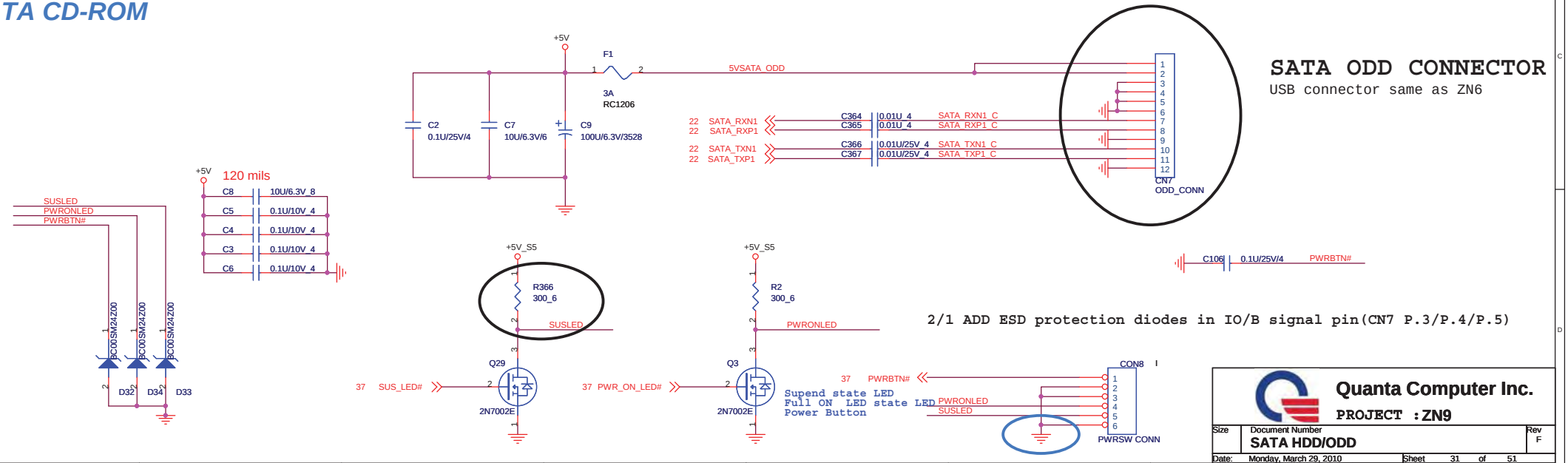
SATA HDD CONNECTOR



SATA HDD CONNECTOR



SATA CD-ROM



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	SATA HDD/ODD	F
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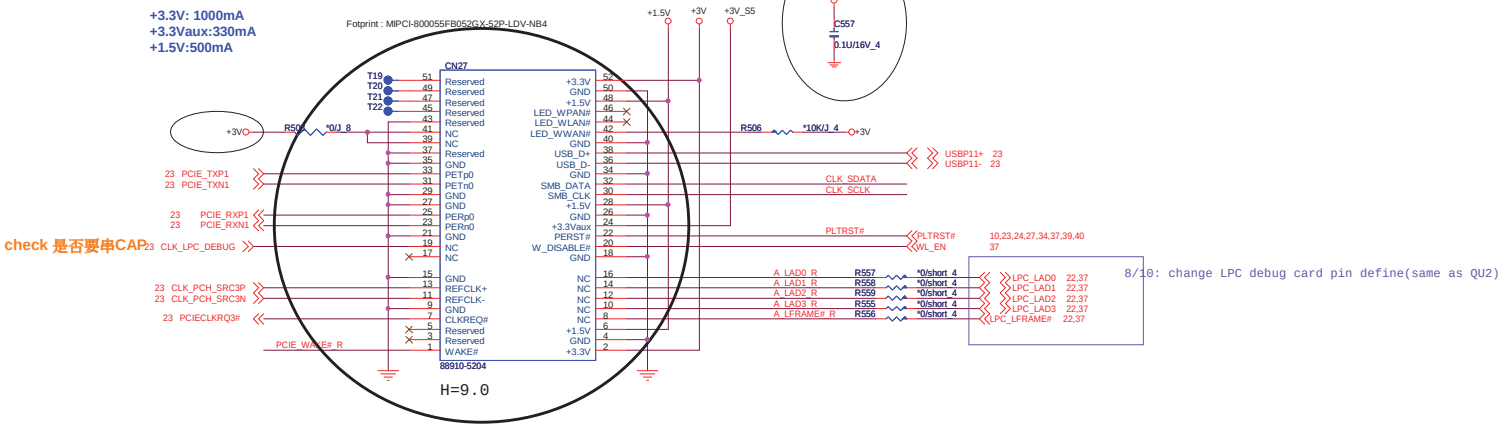
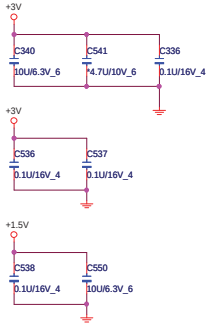
Wireless + BT and Port 80 Debug

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4

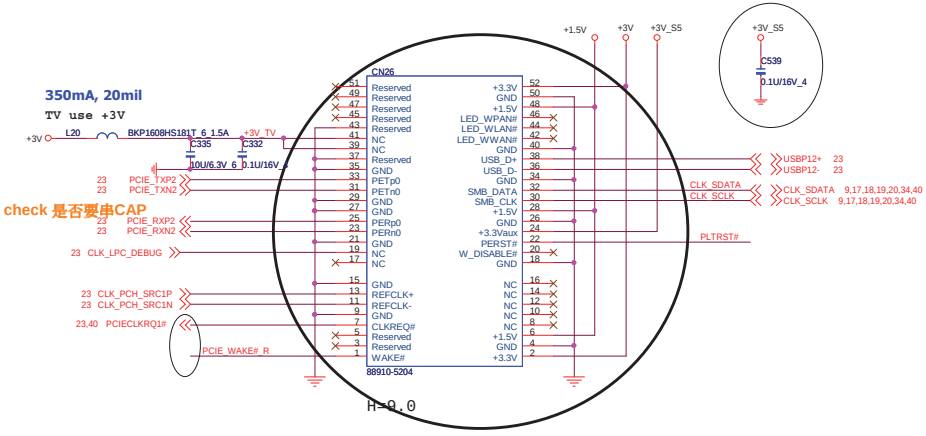


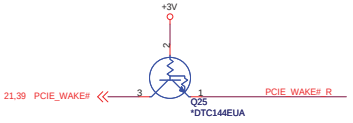


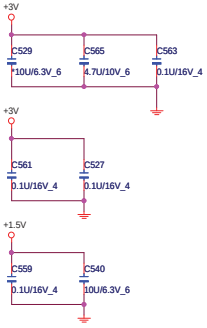
02/05 Change CN26/CN27 P/N to DFHD52MS035

TV

350mA, 20mil
TV use +3V







Quanta Computer Inc.
PROJECT : ZN9

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	MINI PCIE (WLAN/TV)	F

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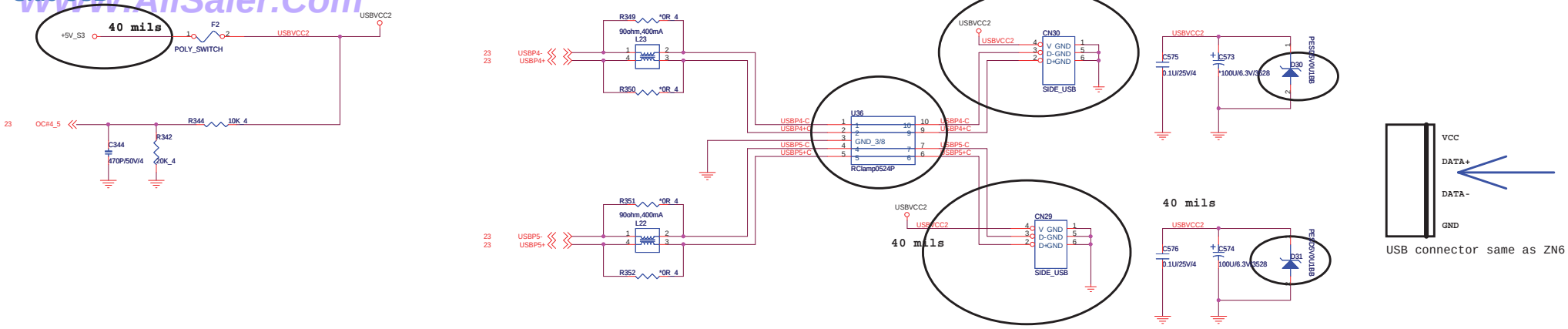
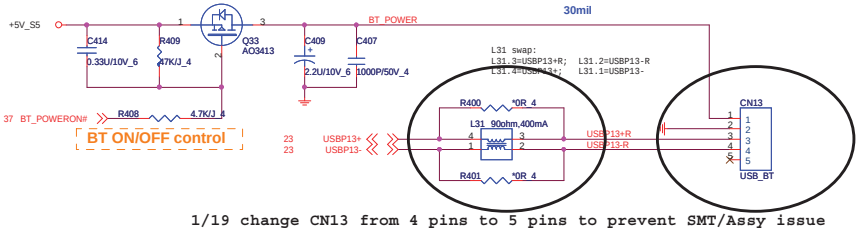
Side USB



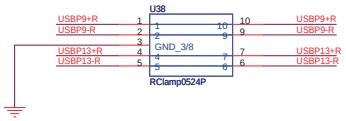
USB connector same as ZN6

02/01 Stuff the U36 and D30,D31(and change the P/N and footprint) for ESD test

BLUETOOTH CONNECTOR

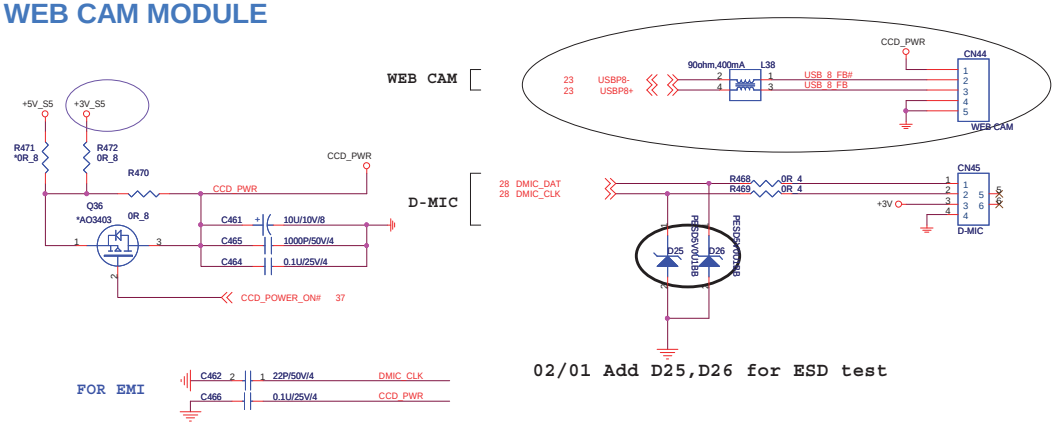


1/19 change CN13 from 4 pins to 5 pins to prevent SMT/Assy issue
Check Vendor p/n and change the footprint



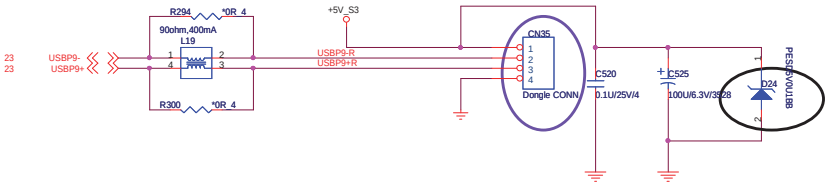
02/02 Add the U38(USD protection diodes) for ESD test
Delete the U19 because U38 will replace U19 ESD function

WEB CAM MODULE



02/01 Add D25,D26 for ESD test

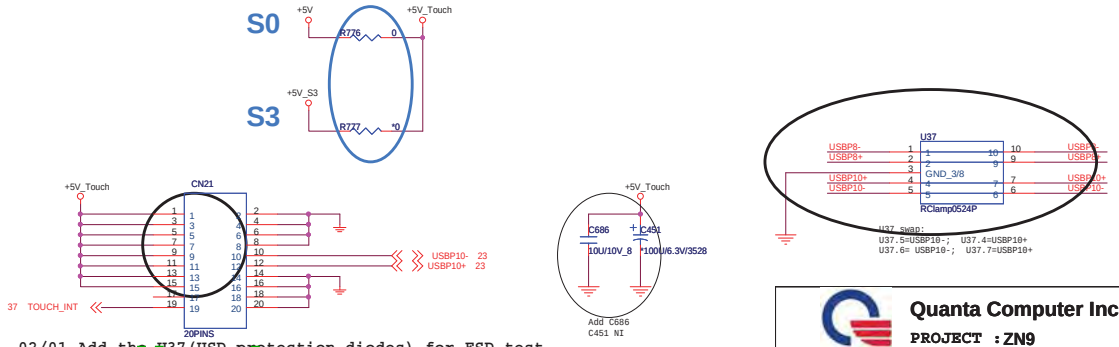
For dongle



2/1 Stuff the D24 (and change the P/N and footprint) for ESD test

MULTI-TOUCH

HP spec:USB header for touch controller must be able to support 3.0 A.



02/01 Add the U37(USD protection diodes) for ESD test

Quanta Computer Inc.
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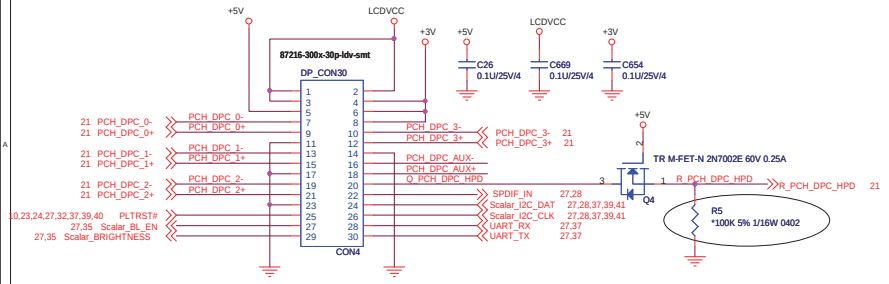
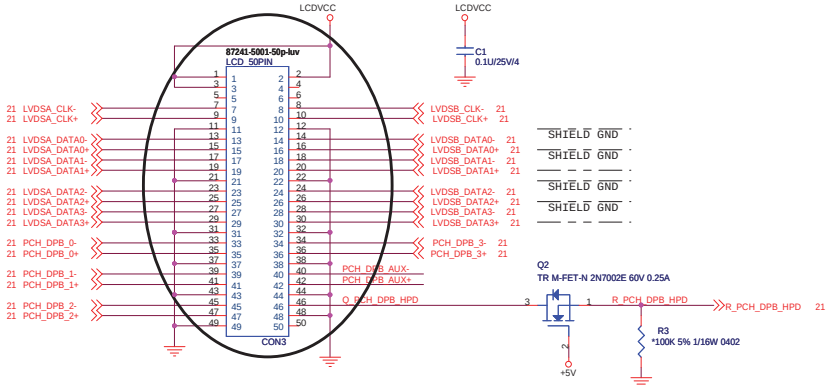
UMA DP CONN for scalar Board



01/13 Change the Netname from "8028_RST" to "PLTRST#"
01/27 Change the Scalar Board CON5 P.6 from 12V to 3V
02/05 Change the CON4(DP CONN) from right angle type to vertical type (DFHD30MS760)
02/05 Change the CON4(DP CONN) P1,P3,P5 connector +5V power rail for fix scalar power sequence

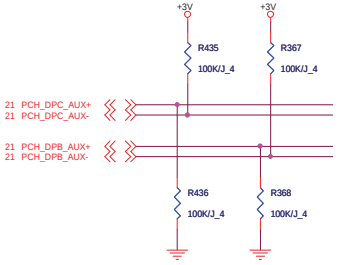
SHIELD GND
SHIELD GND
SHIELD GND
SHIELD GND

LVDS+DP CONN for UMA



DP I/P and ctrl signal from MB

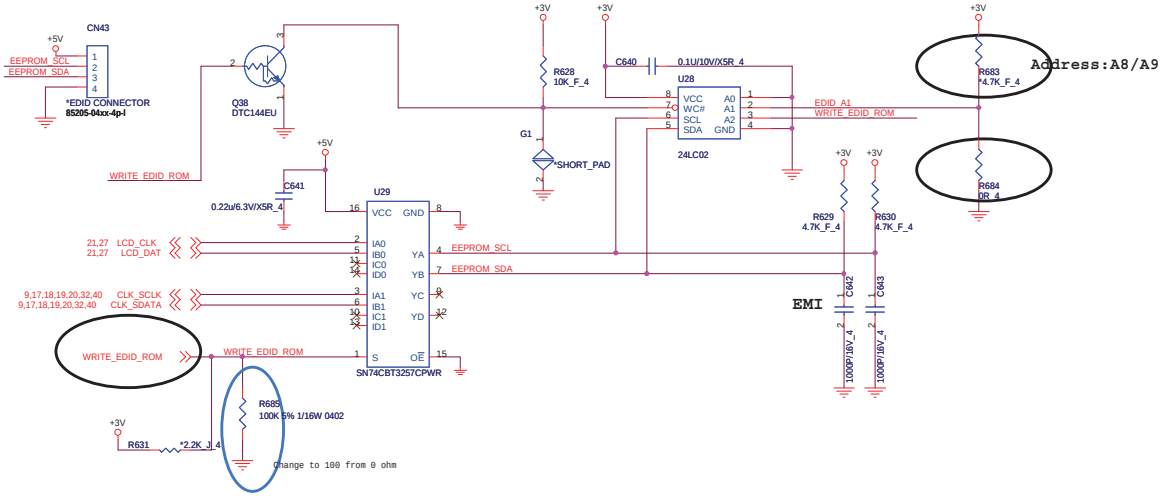
02/05 Change CON3 P/N to DFWF50MR004



EEPROM IIC Selection

PANEL EDID DATA

02/02 un-stuff the R683 and Stuff the R684



02/02 un-stuff the R631 and Stuff the R685

Quanta Computer Inc.
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	Panel (DP/LVDS)	F
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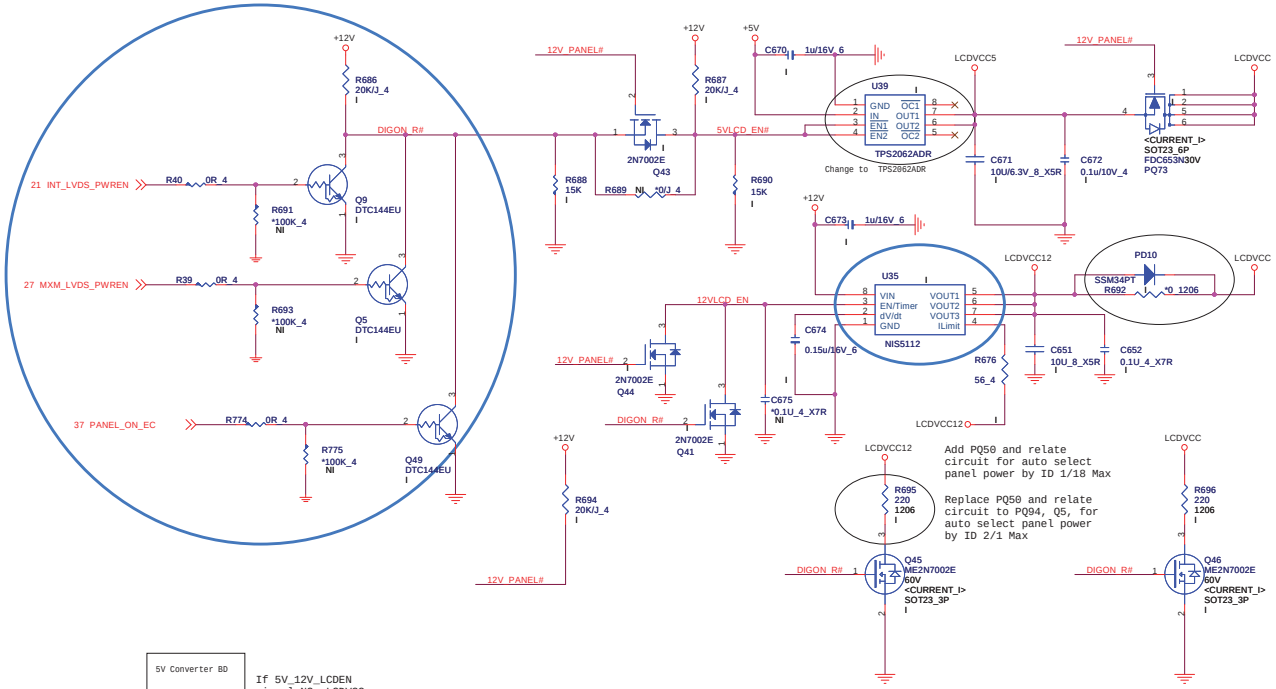
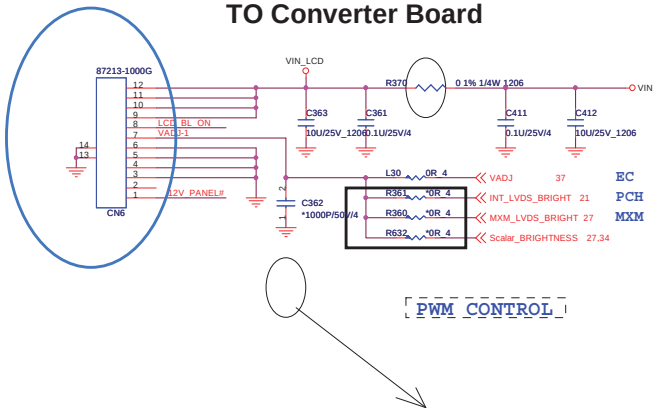
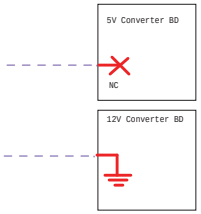
PANEL VCC CONTROL



TO Converter Board

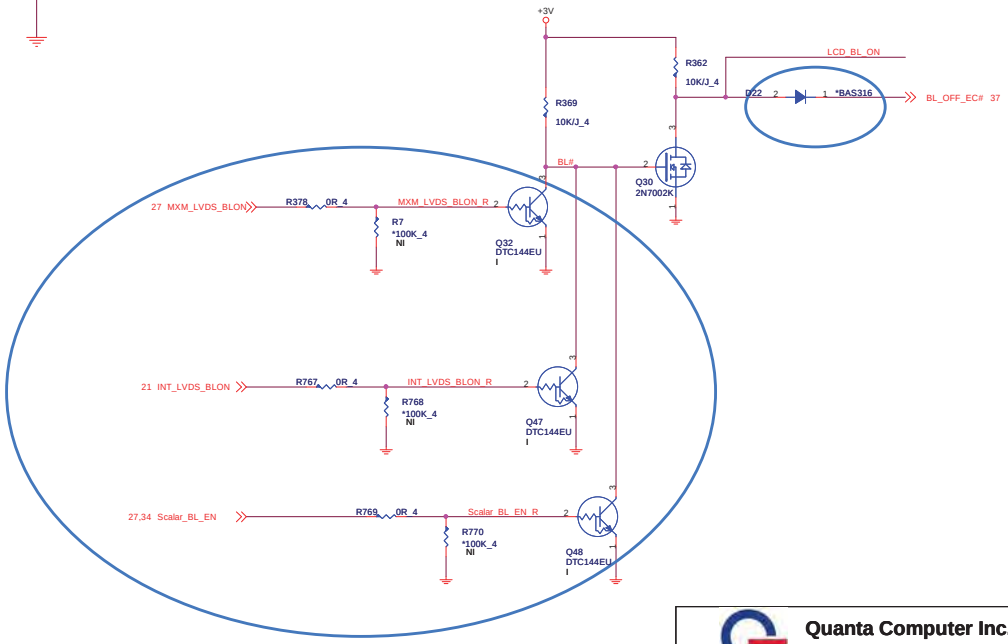


Add on scalar control signal for Cayman ver.
02/05 un-stuff the R360,R361,R632



If 5V_12V_LCDEN signal NC, LCDVCC will output 5V for panel power

If 5V_12V_LCDEN signal connect to GND, LCDVCC will output 12V for panel power



	Scalar_BL_EN	INT_LVDS_BLON	MXM_LVDS_BLON
Clarkdale - UMA LVDS	0V	3.336V	0V
Clarkdale+MXM -MXM LVDS	0V	0V	3.29V
Lynnfield+MXM - MXM LVDS	0V	0V	3.289V
Clarkdale+MXM + Scalar - Scalar LVDS	3.183V	0V	0V
Lynnfield +MXM + Scalar - Scalar LVDS output	3.177V	0V	0V

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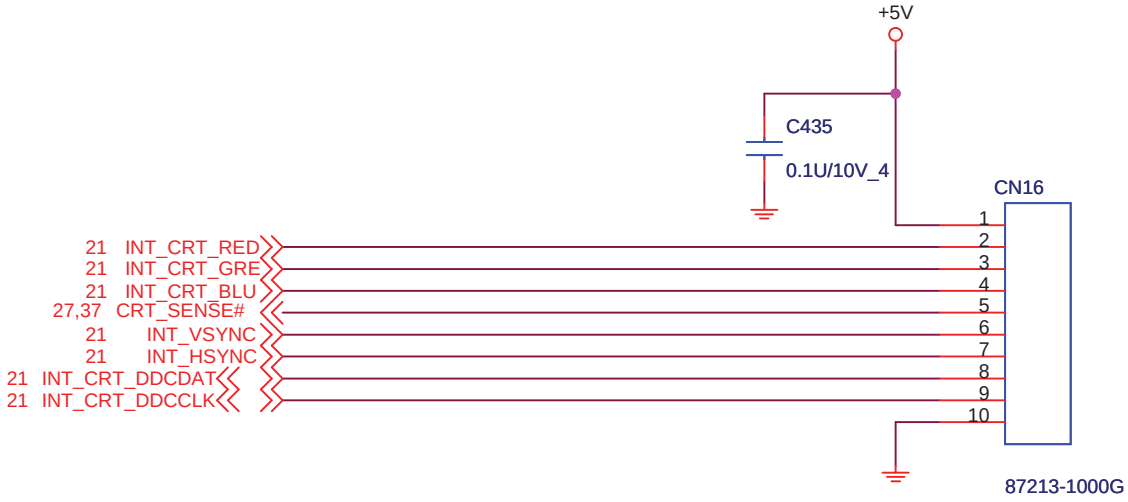
CRT for Debug



Quanta Computer Inc.

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EC

Layout Note:
Place all capacitors close to IT8512.

3VPCU_EC

+3VPCU

L9 120ohm,300mA

C109 0.1U/25V/4 C90 0.1U/25V/4 C136 0.1U/25V/4 C116 0.1U/25V/4 C91 0.1U/25V/4 C119 0.1U/25V/4

(For PLL Power)

L10 120ohm,300mA +3VPCU

C135 1000P/50V/4 C134 0.1U/25V/4

L8 120ohm,300mA +3VPCU

C105 0.1U/25V/4

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

+VCCRTC

3VPCU_EC

+3V

C84 *10P/50V/4 R148 *22/J_4 CLK_PCI_775

+3VPCU R460 *10K/J_4 LPCRST#

C101 0.1U/25V/4

U5 IT8512

BL_OFF_EC# 35
PANEL_ON_EC 35
MXMPWR_EN 27

HWPG PWROK_EC 21

ICH_RSMRST# 21
VRON 43
MAINON 45,46,47,49,50
S5_Power_On 50

R634 0R_4 CIR_TX1 39
R635 0R_4 CIR_RX1 39

SUSON 45,50

PWRBTN# R158 10K_4
H_PECI R160 4.7K_4
HWPG R110 *10K_4
EC_ACIN R170 10K_4
BL_OFF_EC# R162 10K_4
WL_EN R159 *10K_4
CRT_SENSE# R191 *10K_4
THERM_CLK_EC R174 4.7K_4
THERM_DAT_EC R173 4.7K_4
MXM_SMCLK12 R166 2.2K/J_4
MXM_SMDATA12 R161 2.2K/J_4

+5V_S3
TOUCH_INT R765 10K_4

HWPG
SUSC#
C103 *39P/50V/4 C70 *39P/50V/4

22,32 LPC_LAD0
22,32 LPC_LAD1
22,32 LPC_LAD2
22,32 LPC_LAD3
LPCRST#
23 CLK_PCI_775
22,32 LPC_LFRAME#
LPCPD#
LAD0 LAD1 LAD2 LAD3 LPCRST#/WUI4/GPD2 LPCCLK LFRAME#

10,23,24,27,32,34,39,40 PLTRST# R461 *0/short_4

+3VPCU R459 *10K 5% 1/16W 0402

24 SIO_A20GATE
22 IRQ_SERIRQ
24 SIO_EXT_SMI#
24 SIO_EXT_SCI#
24 SIO_RCIN#
PCURST#
D13 1SS355
D11 1SS355
D10 1SS355
D12 1SS355
T13

LPC

GA20/GPB5 SERIRQ ECSMI#/GPD4 ECSCI#/GPD3 WRST# KBRST#/GPB6 PWUREQ#/BBO/GPC7

GPIO

SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2 SMCLK2/WUI22/GPF6 SMDAT2/WUI23/GPF7

MXM_SMCLK12 27
MXM_SMDATA12 27
H_PECI 10,24

T23

SM BUS

PS2CLK0/TMB0/GPF0 PS2DAT0/TMB1/GPF1 PS2CLK2/WUI20/GPF4 PS2DAT2/WUI21/GPF5

SML1ALERT# 23,24,41
GS_INT# 39
MXM_PWR_LEVEL# 27

PS/2

THERM_CLK_EC 27,28,34,39,41
THERM_DAT_EC 27,28,34,39,41
HP_AMP_I2C_CLK 27,28,34,39,41
HP_AMP_I2C_DAT 27,28,34,39,41
Scalar_I2C_CLK 27,28,34,39,41
Scalar_I2C_DAT 27,28,34,39,41
GS_SCL 27,28,34,39,41
GS_SDA 27,28,34,39,41

+3V R111 10K/J_4 HWPG

HWPG

45,49 +1.5V_SUS_PG D9 BAS316
44 V_AXG_PG D8 *BAS316
46 +1.1V_VTT_PG D7 BAS316
49 +1.05V_PG D6 BAS316

+3V R677 10K/J_4 Q39 2N7002K

+1.1V_VTT R678 4.7 <PKG> <PKG-BOM> Q42 2N7002K

CPU_VTT_PG 10
1.1V leavel

<HP-BOM> R679 *12K/F_4

39 CIR_RX0 CIR_RX0 T14

CIR

CRX0/GPC0 CTX0/TMA0/GPB2

PWM

PWM0/GPA0 VADJ 35
PWM1/GPA1 BT_POWERON# 33
PWM2/GPA2 FAN1# 41
PWM3/GPA3 FAN2# 41
PWM4/GPA4 PWR_ON_LED# 31
PWM5/GPA5 SUS_LED# 31
PWM7/GPA7 WL_EN 32
TACH0/GPD6 FAN1SIG 41
TACH1/TMA1/GPD7 FAN2SIG 41
TMR0/WUI2/GPC4 volume+# 39
TMR1/WUI3/GPC6 volumeL-# 39

27,34 UART_TX
27,34 UART_RX
R636 0R_4 UARTTX
R637 0R_4 UARTRX

UART port

DAC4/DCD0#/GPJ4 DSR0#/GPG6 GINT/CTS0#/GPD5 PS2DAT1/RTS0#/GPF3 DAC5/RIG0#/GPJ5 PS2CLK1/DTR0#/GPF2 TXD/SOUT0/GPB1 RXD/SIN0/GPB0

IT8512NX

WAKE UP

PWRSW/GPE4 PWRBTN# 31
RI1#/WUI0/GPD0 SUSB# 21
RI2#/WUI1/GPD1 SUSC# 21
WUI5/GPE5 EC_ACIN 112
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7 PCH_ACIN 21

Input only

+3VPCU R126 470K_4 PCURST# C92 0.1U/25V/4

8512_SCK
8512_SCE#
8512_SI
8512_SO
FSCK FSCE# FMOSI FMISO

EXTERNAL SERIAL FLASH

8Mbit , SPI

39 Mute_BTN#
39 IR_ACTIVE_LED
BIOS_WP#
33 TOUCH_INT
28 EC_AMP_MUTE#
KSO16/SMOSI/GPC3 KSO17/SMISO/GPC5 PWM6/SSCK/GPA6 SSCE#/GPG2 SBUSY/GPG1/ID7 GPG0

SPI Device

MID1
MID2
MID3
CIR_ED1 39
CRT_SENSE# 37,39
3VA5V_PCU_PG 48
ADP-ID 42

A/D D/A

ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/WUI28/GPI4 ADC5/WUI29/GPI5 ADC6/WUI30/GPI6 ADC7/WUI31/GPI7

CCD_POWER_ON# 33
S3_5V_EN 39,48
ICH_PWRBTN# 21
CLKRUN# 21

DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3

4.7K 5% 1/16W 0402 R187 +3VPCU

CK32KE PMUX2
CK32K PMUX1

*0/J_6 R150 ICH_SUSCLK 21

Y4 32.768KHZ C97 18P/50V/4 C93 18P/50V/4

CLOCK

KBMX

KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15

KSI0/ST8# KSI1/APFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7

VSS VSS VSS VSS VSS VSS AVSS VCORE

R186 0R_4 C100 0.1U

+3VPCU
R180 10K_4 R178 10K_4

8512_SCE#
8512_SCK R176 47R_4
8512_SI R179 47R_4
8512_SO R177 15R_4
BIOS_WP#

U6 MX25L1605A
U7 *MX25L1605A

C122 0.1U/25V/4

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

For Debug use

88502-2401-24P-L CON1

CP5 CP2 CP4 CP3 CP6 CP1 220P X 4_4

0402 size

RP14 RP13 RP15 *10KX8

RP13,RP14,RP15 change to un-stuff

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

	MID3	MID2	MID1
EVT PCBA	0	0	0
	0	0	1
	0	1	0
	0	1	1

+3VPCU R198 *10K_4 R199 *10K_4 R200 *10K_4

MID1 R188 0R_4
MID2 R189 0R_4
MID3 R190 0R_4

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Cancel Braidwood function

Quanta Computer Inc.		
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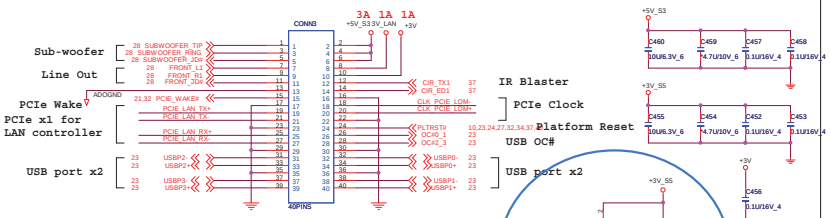
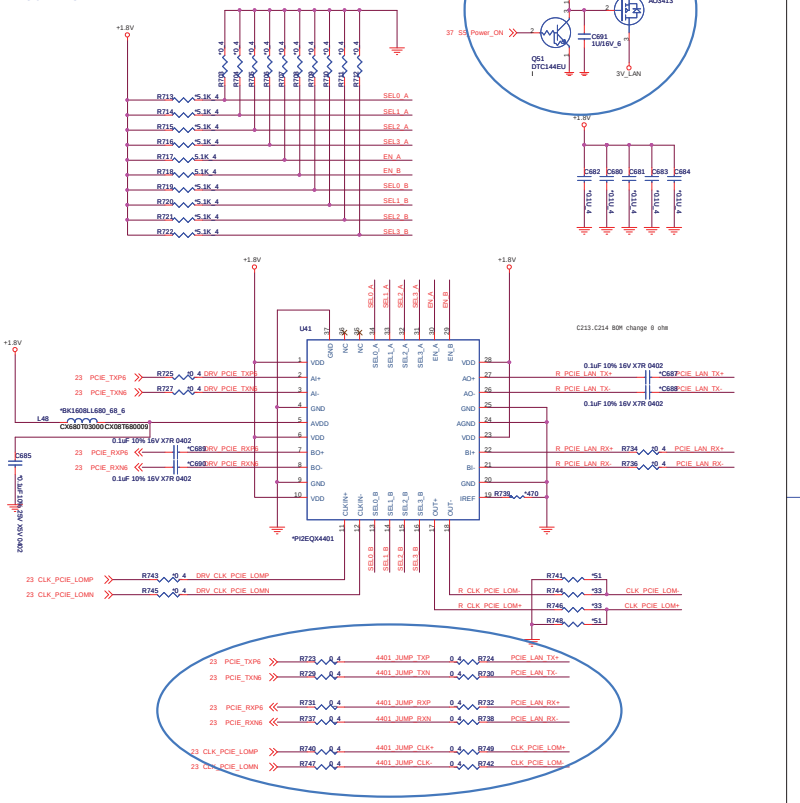
40 pin I/O Connector

02/01 ADD ESD protection diodes in IO/B signal pin(CONN3 P.1/P.3/P.5/P.7/P.9)

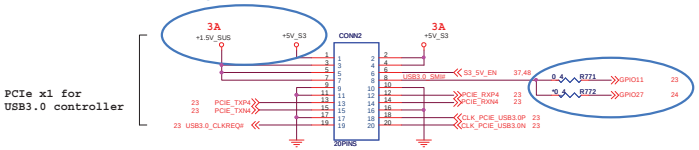


LAN Redriver

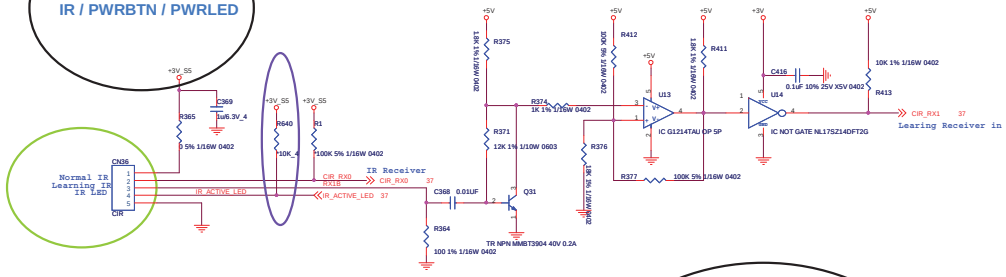


20 pin for USB3.0 Controller

20 pin I/O Connector

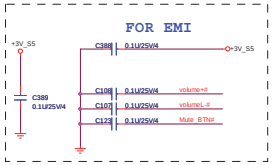


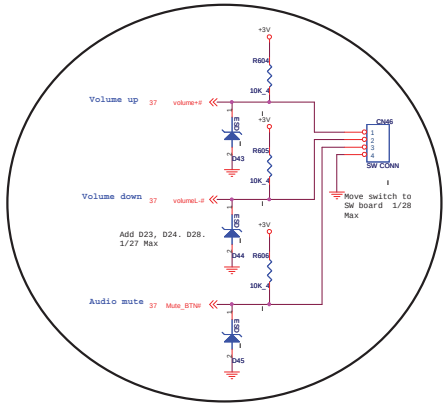
Eject Button
IR / PWRBTN / PWRLED



The aqua-white (470 +/- 5 nm) color is used to indicate the system is powered on and in the S0 state. The amber (590 +/- 5 nm) color is used to indicate the system is in one of the standby states (S3, S4, S5).

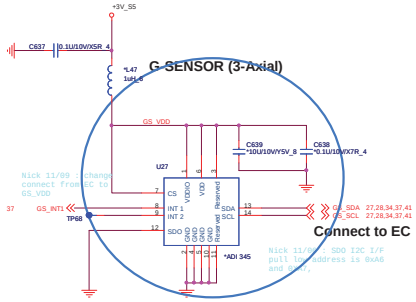
PWRBTN# must pull up to PCU power well

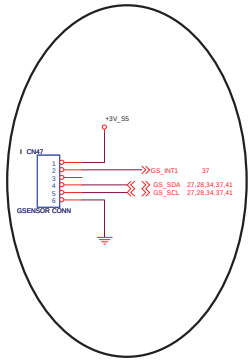




02/03 delete the R607/R609/SW1/SW2/SW3
Add ESD*3 and CN?
Volume Control function change to Daughter/B)

G-Sensor





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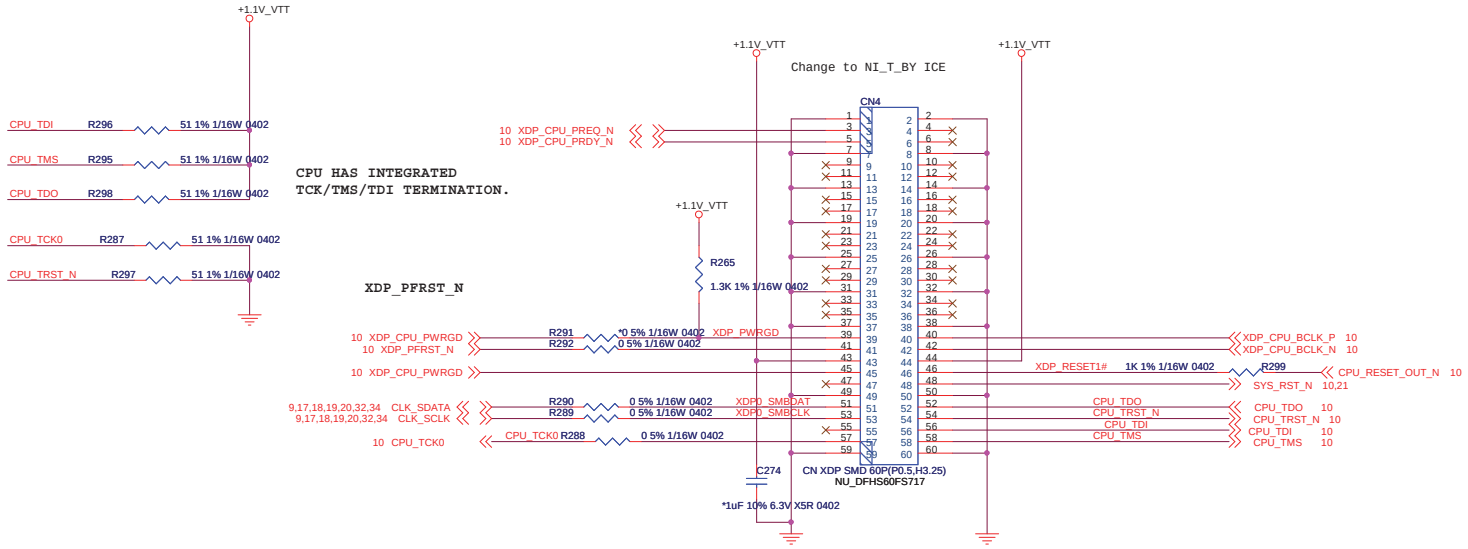
CPU XDP Connector

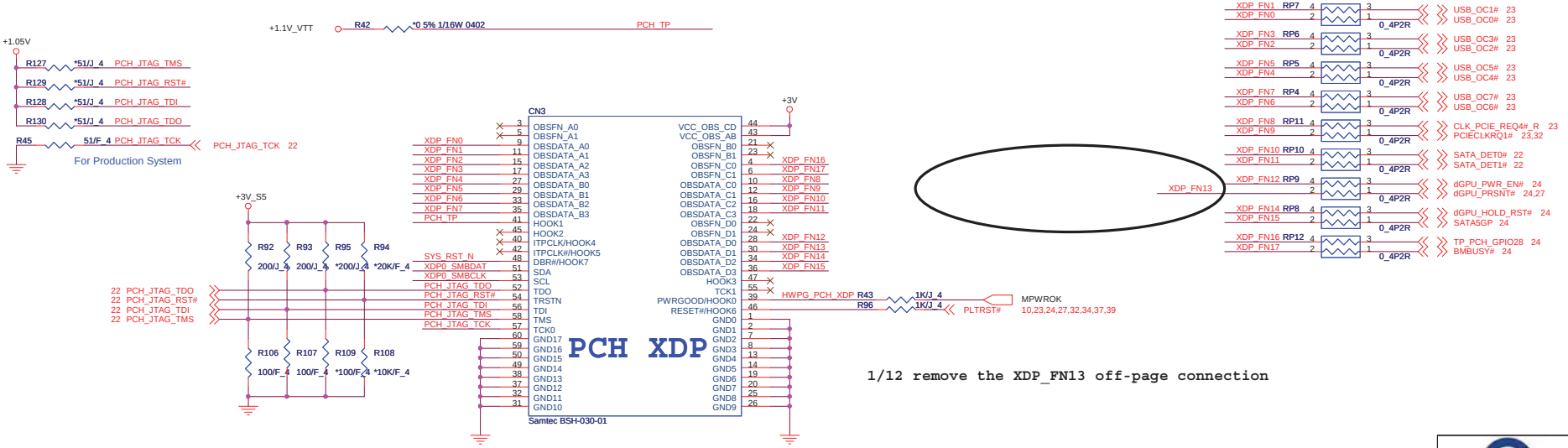
XDP0 - CPU

bsh-060-01-l-d-60p-ldv
bsh-060-01-l-d-60p-ldv



CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

PCH XDP Connector



1/12 remove the XDP_FN13 off-page connection

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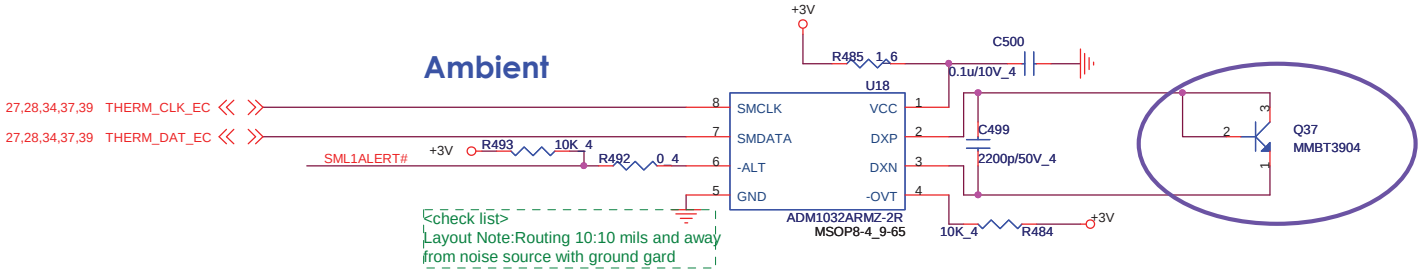
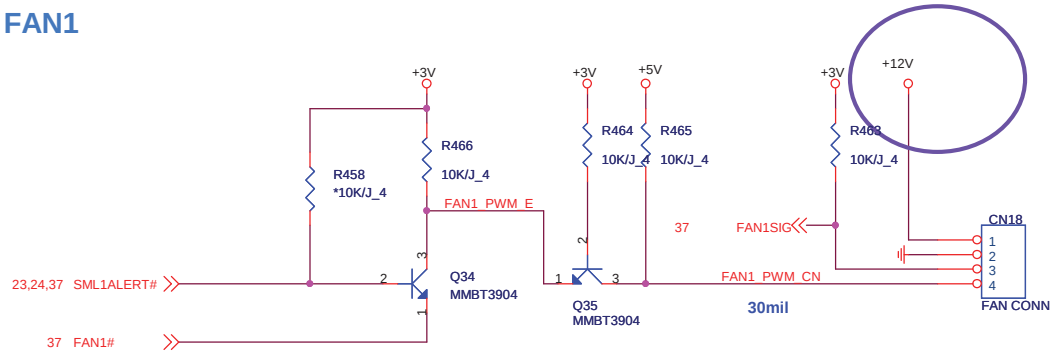
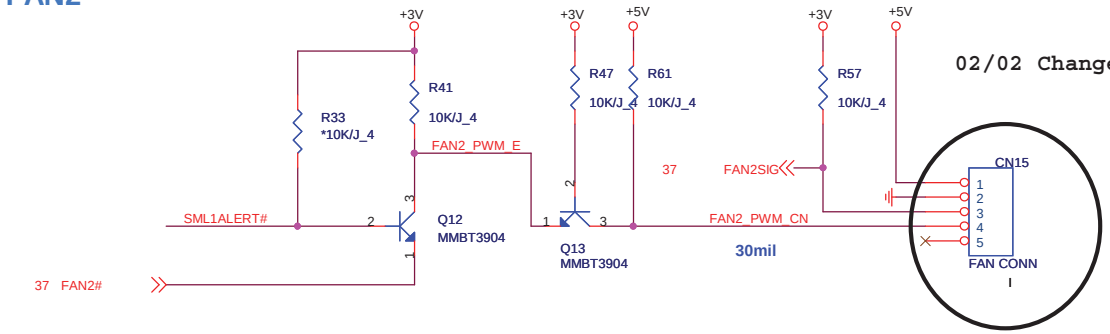
Ambient



FAN1



FAN2



02/02 Change CN15 from 4 pins to 5 pins to prevent SMT/Assy issue

Quanta Computer Inc.

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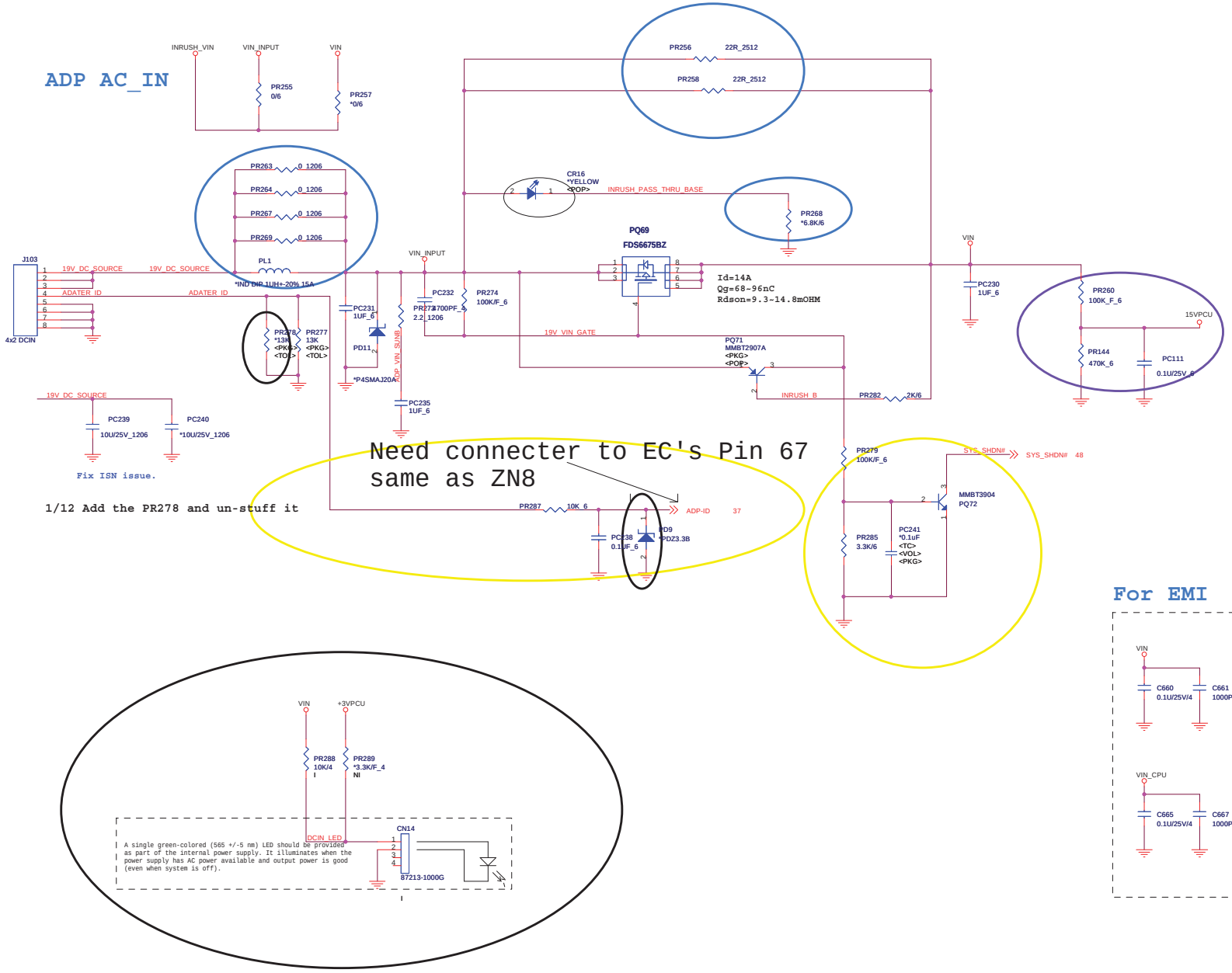
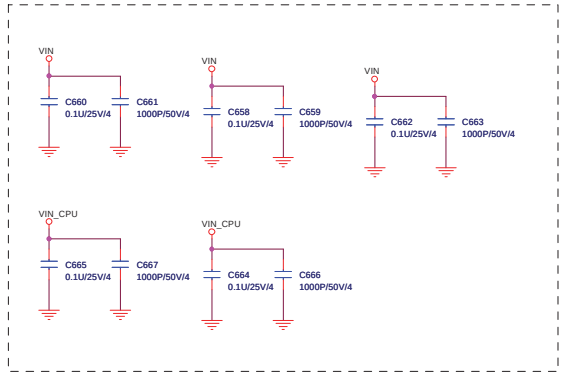
ADP AC_IN



For EMI



1/12 un-stuff PD9 for power request

Quanta Computer Inc.		
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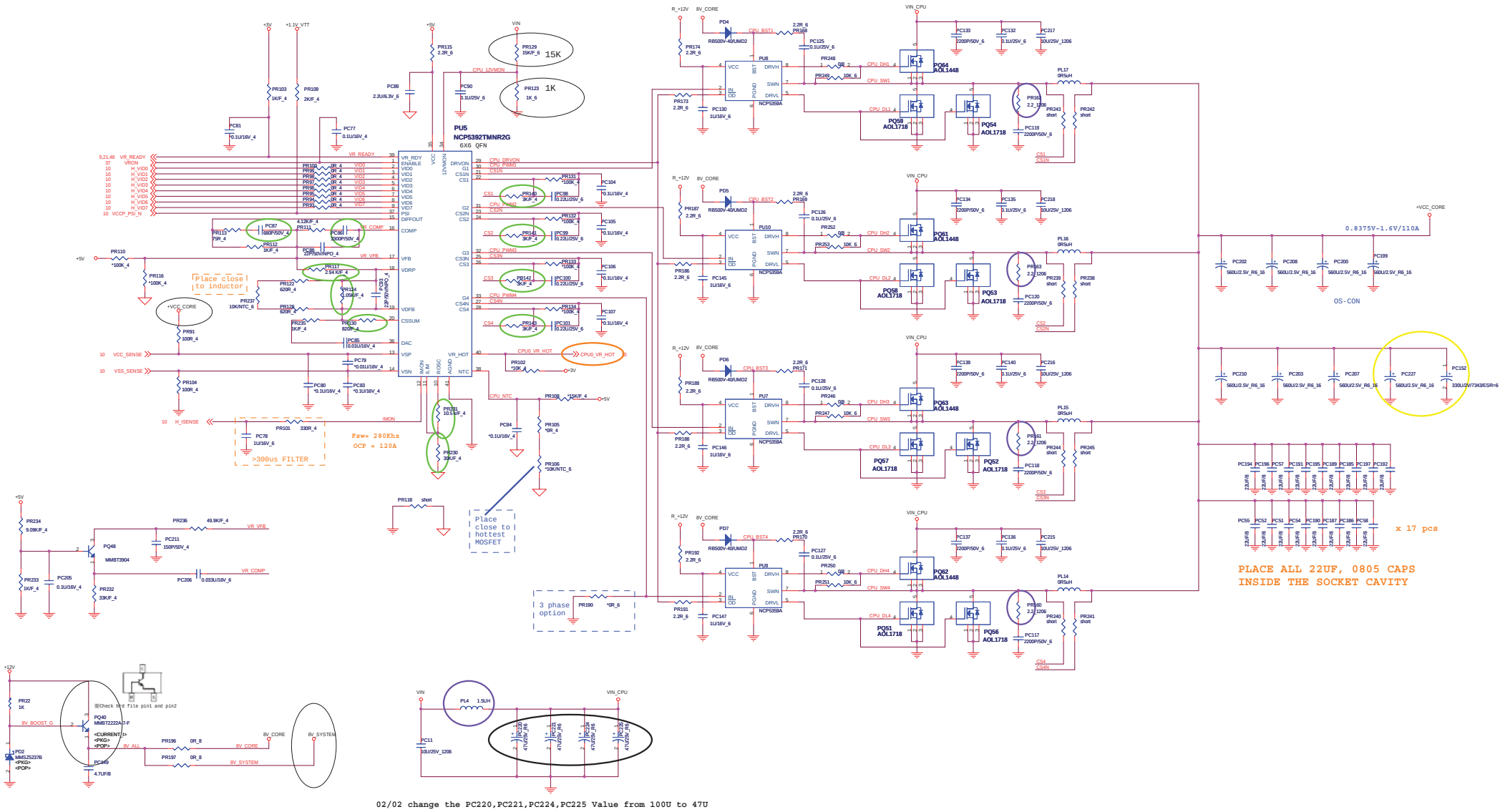
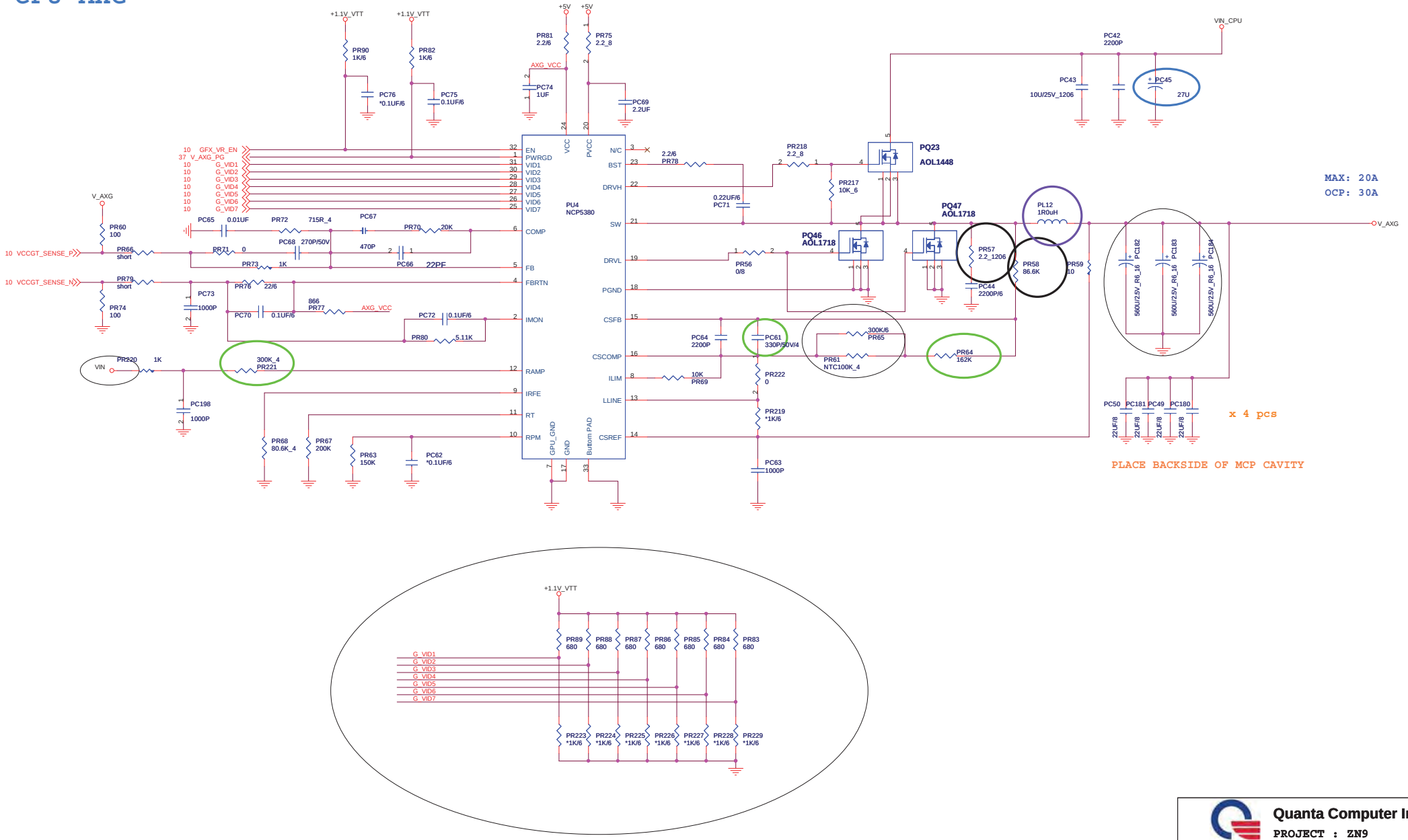


Quanta Computer Inc.
PROJECT : ZN9
CPU VCC_CORE (NCP5392)

CPU AXG



Quanta Computer Inc.

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	VAXG (NCP5380A)	F

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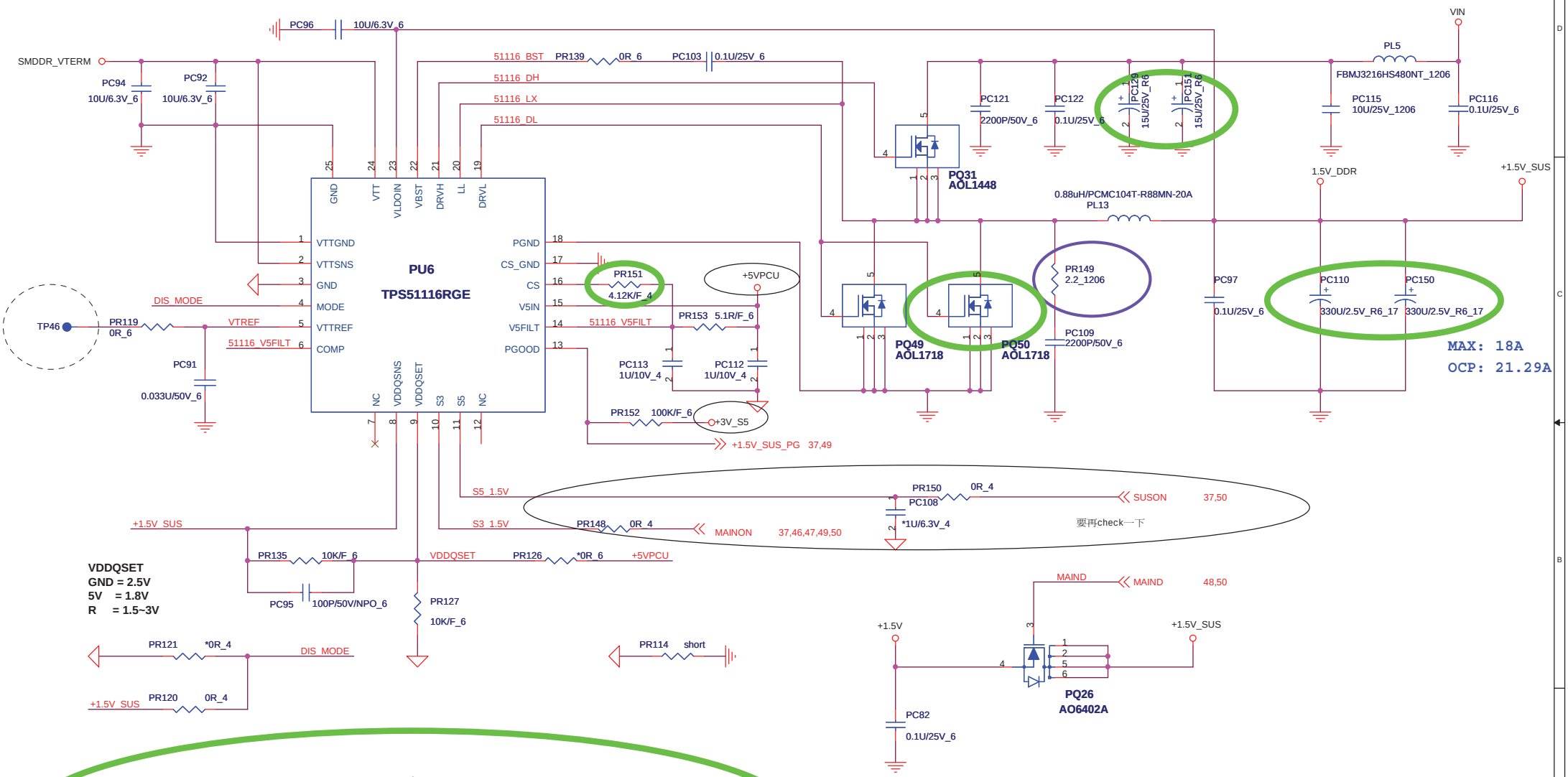
DDR3 1.5V(TPS51116)



del_IL=(19V-1.5V)*1.5V/(0.88u*400K*19V)=3.92A

(10uAxPR26/Rdson)+del_IL/2=Iocp

(10uA*4.1K/2.15m)+del_IL/2=21.029A

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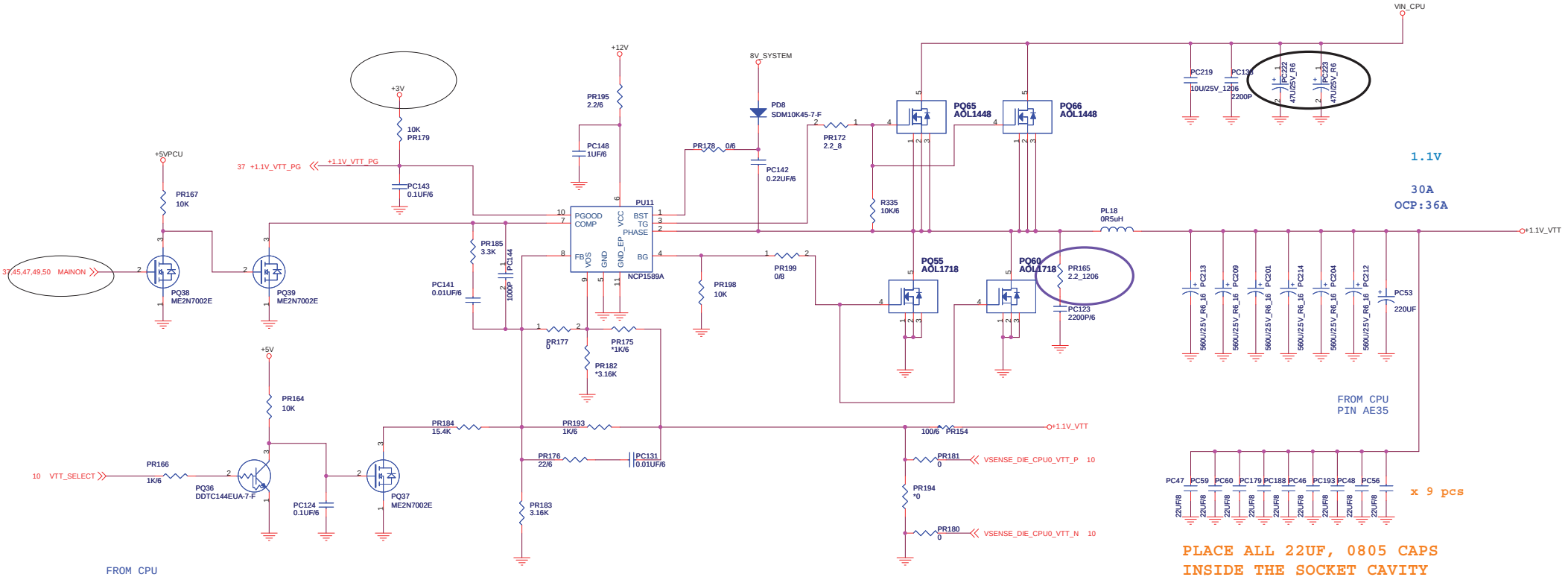
+1.1V_VTT

02/02 change the PC222,PC223 Value from 100U to 47U



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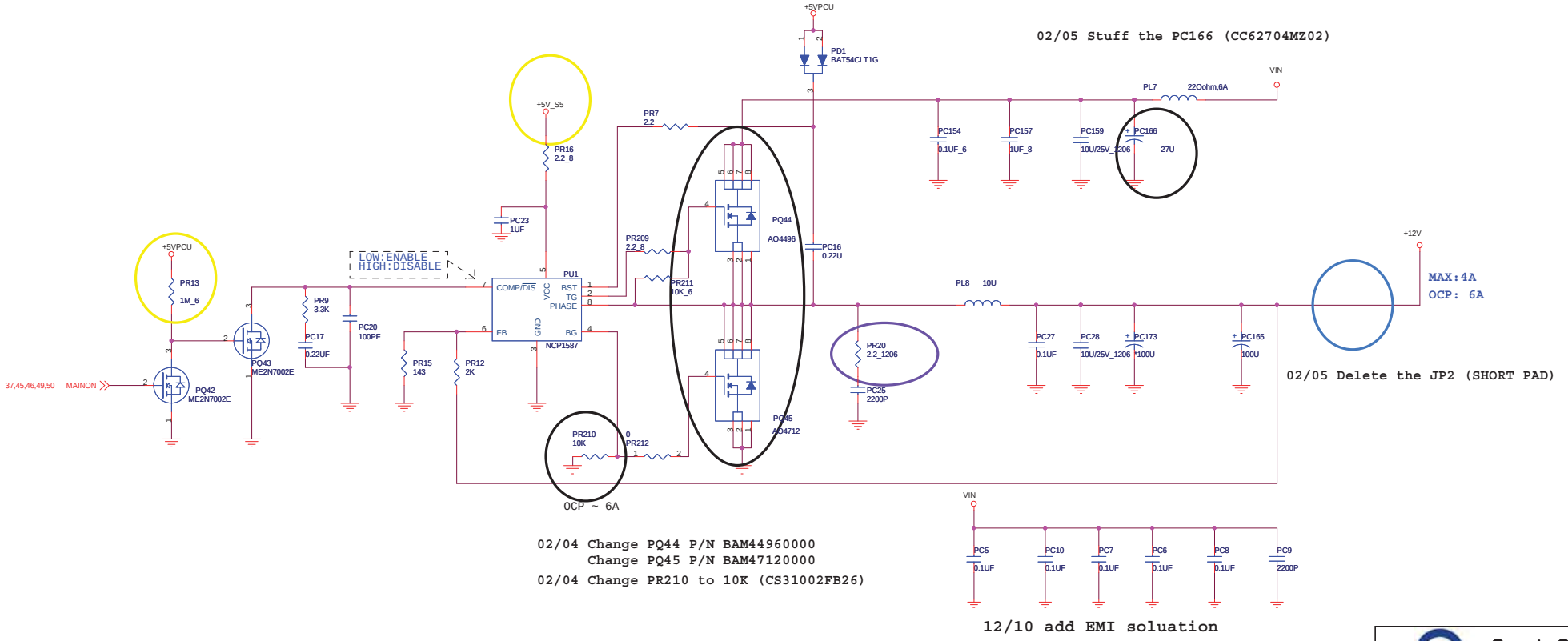
19V to 12V Power CKT



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	+12V/ HDD(NCP1587)	F

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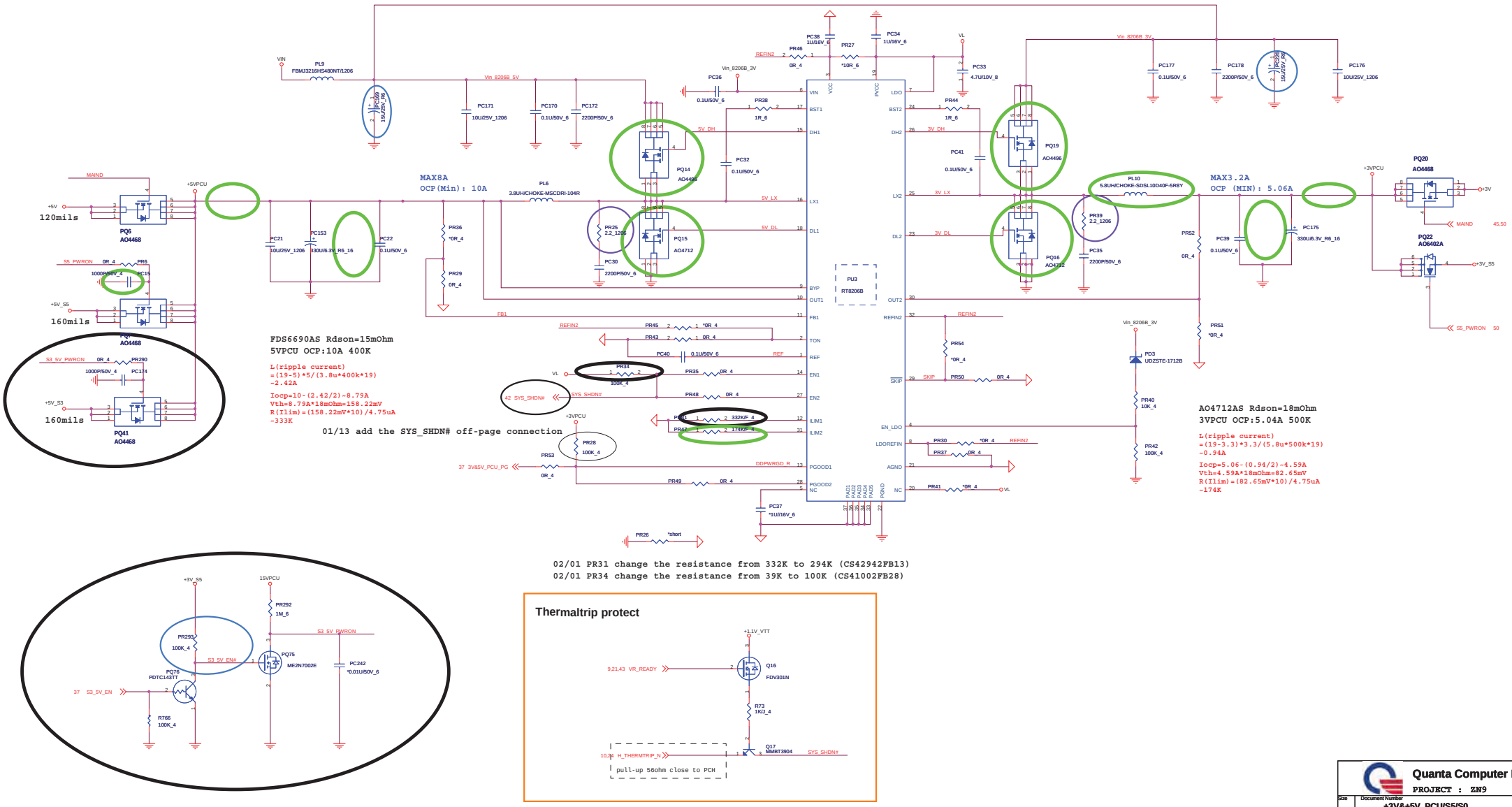
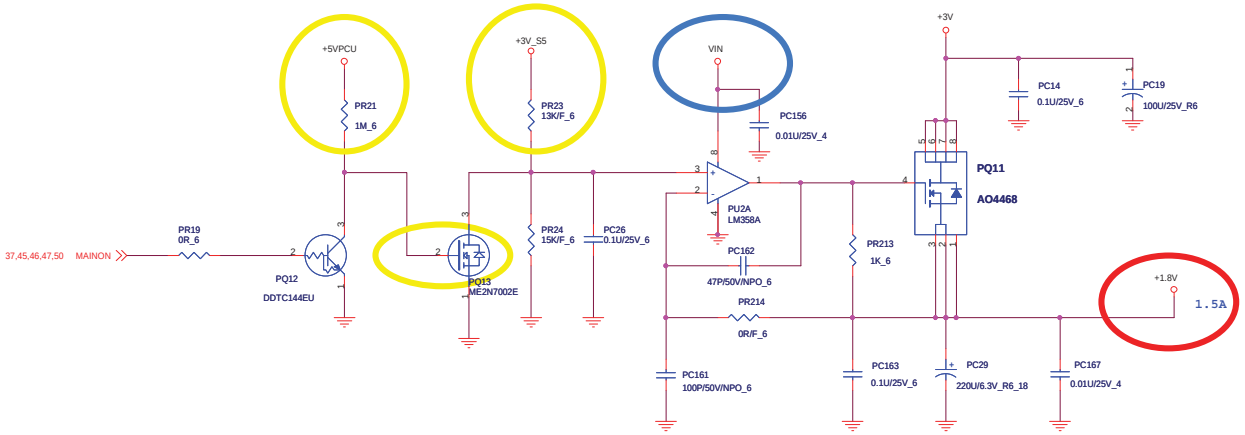
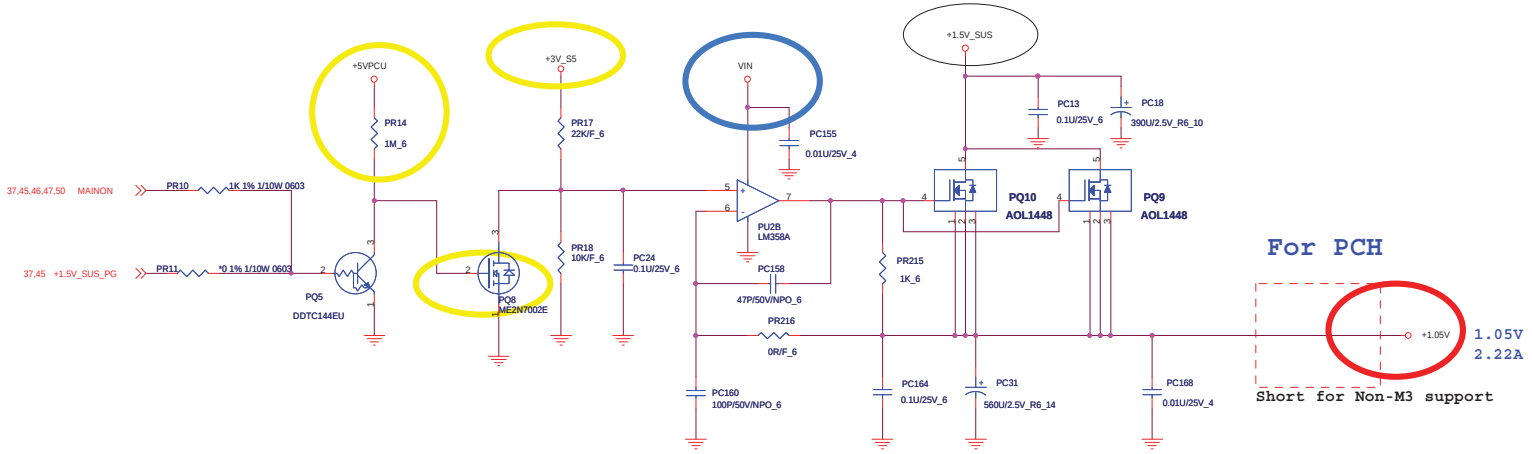
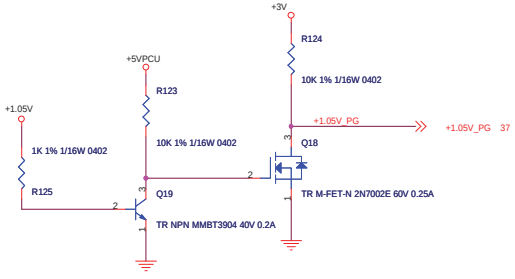
3VPCU & 5VPCU
+3V_S5 & +5V_S5
+3V & +5V



+1.8V & +1.05V







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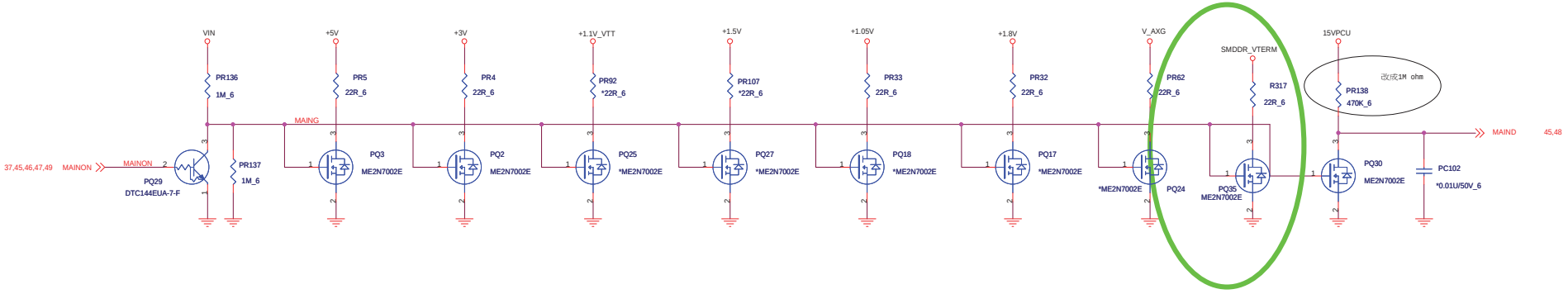

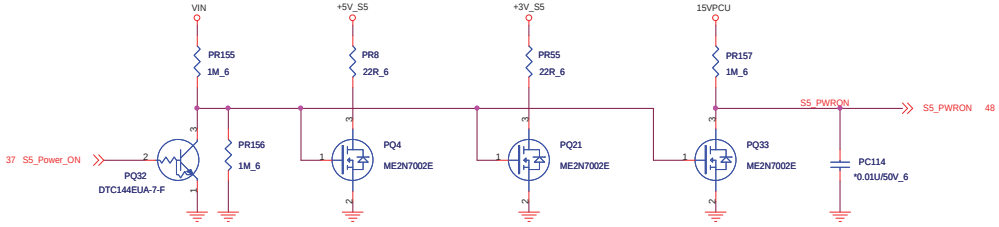

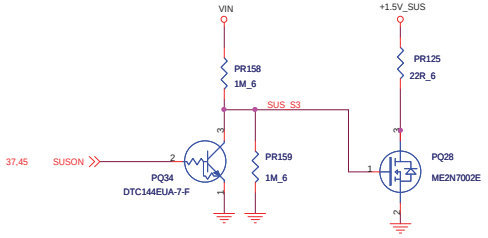

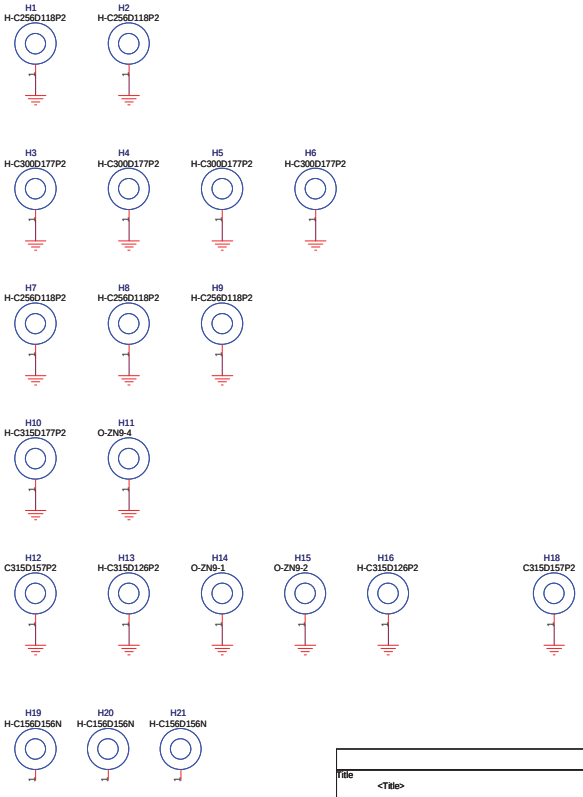

02/05 delete the H22 location

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	Change list
EVT1.5	1.Remove Vcore output 0 ohm resister --- PR144,PR145,PR146,PR147 (p.43) 2.PSI signal change pull high to +1.1V_VTT (p.43) 3.Remove PC111 (p.45) 4.PR135 value change to 10k ohm (p.45) 5.3.3V and 5V PWM High/low side MOSFET chgne to AOL1448 --- PQ14,PQ15,PQ16,PQ19 (p.45) 6.PC169 (p.45) 7.Add one CAP (p.45) 8.PR23 value change to 13k ohm (p.45) 9.PR17 value change to 22k ohm (p.45) 10. Change Choke PL8 ---> 10UH ---> CYDIU44NC1B Footprint= CHOKE-MSCDR1-10AR PL4 ---> 1.5UH ---> CV-1580MCDS Footprint =choke-sp005306-3r3m-2 PL17,PL16,PL15,PL14 ---> 0.5UH ---HDC<50*6MB00 Footprintechoke-acl1809k-r50m-2p 11.CN8 change to DC jack 12.Add PC227,PC228 for 3.3V and 5V power 13.PR248,PR252,PR246,PR250 chage 0805 footprint 14.PR162,PR1163,PR161,PR160,PR149,PR25,PR39 change 1206 footprint 15. PR218 value change to 6.8k ohm (p.45) 16.cancel Case open fucion ---- DEL R555,R556,R554,Q39,Q40,CN31,D23 17.ODD eject signal pull high --- R146 18.Q37 change to MMBT3904 19.FAN speed control change to PWM type 20.Change I/O board design (a) 80 pin board to board connector change to 40+20 pin wire to board connector ----> DEL CONN1, ADD CONN2,CONN3 (b) DEL CN8 , ADD CN38,CN37,CN39 (c) 21.USB dongle change to wire to connector 22.LPC 80port change connect to wireleses miniPCIe card 23.CN6 change to vertical type 24.ODD change to vertical type 25.DEL SPI BIOS debug connector --- CN20 26.DEL C154,C228 27.Add G-Sensor function 28. Add ID pin function for Adaptor circuitry
EVT2.0	1. DEL Braidwood function 2. Scalar Board connector change to 30pin and add I2C/ URAT and 3.3V power 3. Vcore power inductor chang P/N to DC<503M000 4. Add EEPROM for Panel EDID 5. Add one 3 pin connector for HP logo light module 6. Aduio codec IC change to ALH8903F00 7. Headphone AMP IC change to TPA6138A2 8. Speaker AMP IC change to S3MC30CFZ 9. SA/SB_DIMM_VREF 0 ohm resistor stuffed by default 10. PM_SYNC pull up 51.1 ohm to VTT
EVT2.5 E01	1.R542 change to 6.2K ohm for fix card reader can't work issue 2.DDR data bit swaping for DDR traces routing smoothly 3.Change rear I/O connector pindefine and move USB connector close to PCH 4.Add fuse for HDD power 5.Modify Smart ID circuit 6.D-MIC and Webcam separate into two connector (Wa-Cam: 5 pin , D-MIC: 4 pin)
EVT2.5 E02	1.Change side I/O USB connector for mechanical drawing design 2.Change SATA pin define 3.Add 12V/5V switch circuit for panel power (option2 and option4)

	Change list
DVT F01	1. P23--- 01/13 stuff the R573 to pull high to +3V; un-stuff the R430 2. P27--- 01/13 Change the CON5 P.25 Netname from "BD28_RST" to "PLTRST#" 3. P27--- 01/27 Change the Scalar Board CON5 P.5 from 12V power to 3V power 4. P27--- 02/01 Stuff the D4 for ESD test 5. P28,P29---Exchange the design circuit by Hank. 5.1---(01/27 HP request to change the AUD/AUS from DRV603 return to DRV801) 5.2---(02/01 stuff the AD3,4A4,AD5,AD7,AD8,AD9,AD10 for ESD TEST) 6. P31--- 02/01 ADD ESD protection diodes in ID/B signal pin(CN7 P.3/P.4/P.5) 7. P33--- 02/01 Stuff the U36 and D30,D31and change the P/N and footprint) for ESD test 8. P33--- 01/19 Change CN13 from 4 pins to 5 pins to prevent SMT/Assy issue 9. P33--- 02/01 stuff the D24 (and change the P/N and footprint) for ESD test 10. P33--- 02/01 Add D25,D26 for ESD test 11. P33--- 02/01 Add the U37(USB protection diodes) for ESD test 12. P39--- 02/01 ADD ESD protection diodes in ID/B signal pin(CONN3 P.1/P.3/P.5/P.7/P.9) 13. P40--- 01/12 remove the RDF_PAI3 off-page connection 14. P40--- 01/13 add the NET(SYS_SHDN#) off-page connection 15. P40--- 02/01 PR31 change the resistance from 332K to 294K (C5429J2FB13) 16. P40--- 02/01 PR34 change the resistance from 30K to 105K (C5419G2FE20) 17. P22---02/02 Delete the CN2 (Battery socket) and add XDT1 CONN for Battery+Wire cable used 18. P23--- 02/02 Add the U38(USB protection diodes) for ESD test (CN35 USB dongle PIN define check) 19. P41--- 02/02 Change CN33 from 4 pins to 5 pins to prevent SMT/Assy issue 20. P45--- 02/02 Change the PC220,PC223,PC224,PC225 Value from 100U to 47U 21. P45--- 02/02 Change the PC227,PC228 Value from 100U to 47U 22. P36---02/02 Un-stuff the R631 and Stuff the R630 23. P36---02/02 Un-stuff the R632 and Stuff the R659 24. P27---02/02 Delete the CN2(Battery socket) and add XDT1 CONN for Battery+Wire cable used 25. P27---02/03 Exchange the MXM DP output from DP-B to DP-C 26. P27---02/03 Add the U38(USB protection diodes) for ESD test,Delete the U38 because U38 will replace U19 ESD function 27. P33---02/03 Add the U38(USB protection diodes) for ESD test 28. P39---02/03 Delete the R607/R608/R609/SW1/SW2/SW3 Add ESD*3 and CN7--Volume Control function change to Daughter/B 29. P27--- 02/04 Change the CON5 (DP CONN) from right angle type to vertical type (DFHD39MS759) 02/04 Change the CON5 (DP CONN) P1,P3,P5 connector +5V power rail for fix scalar power sequence 30. P34--- 02/04 Change the CON4 (DP CONN) from right angle type to vertical type (DFHD39MS759) 02/04 Change the CON4 (DP CONN) P1,P3,P5 connector +5V power rail for fix scalar power sequence 31. P35--- 02/04 Un-stuff the R360,R361,R632 32. P47--- 02/04 Change PQ44 P/N BAM4960000 Change PQ45 P/N BAM4720000 Change PR210 to 10K (CS31002FB26) Stuff the PC166 (CCG2704M202) Delete the JP2 (SHORT PAD) 33. P27---02/05 Change CON2 (LVDS Conn) P/N to DFWF50MB004 34. P27---02/05 Change CN24 (MXM Conn) P/N to DFHS94FB014 35. P28---02/05 Change CN39/CN40 (Audio Jack) P/N from DFTJ07FR017 to DFTJ07FR023 36. P29---02/05 Change CON6 from 4PIN to 5PIN (DFHD05MS041) Change CON7 from 5PIN to 4PIN (DFHD04MR103) 37. P29---02/05 Change CON6 footprint from 50273-0050n-001-5p-r to 50273-0050n-001-5p-L 38. P30---02/05 Change CN28 (Card reader) P/N to DFHC38FR002 39. P32---02/05 Change CN26/CN27 (Mini PCIE Conn) P/N to DFHDS2MS035 40. P34---02/05 Change CON3 (LVDS Conn) P/N to DFWF50MB004 41. P35---02/05 ADD the U35 P/N ALH0511Z000 (new create) 42. P50---02/05 delete the H22 location 43. P30---02/08 Change CARD READER P/N to DFHS38FR002
DVT F02	43. Change AC LED circuit 43. Change AC LED circuit DVT: C645 change to 4.7uF/6.3V/0603 C646 change to 0.1uF/16V/0402 C647 change to 1uF/10V/0402 L31 swap: L31.3=USBP13+R; L31.2=USBP13-R L31.4=USBP13+; L31.1=USBP13- L19 swap:: L19.3=USBP9-R; L19.2=USBP9+R L19.4=USBP9-; L19.1USBP9+ U37 swap: U37.5=USBP10-; U37.4=USBP10+ U37.6= USBP10-; U37.7=USBP10+ change scalar board pin define Add C686 C451 NI R26 change to 10K ohm RP13,RP14,RP15 change to un-stuff
	U35 change P/N

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Title: Timing Diagram

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