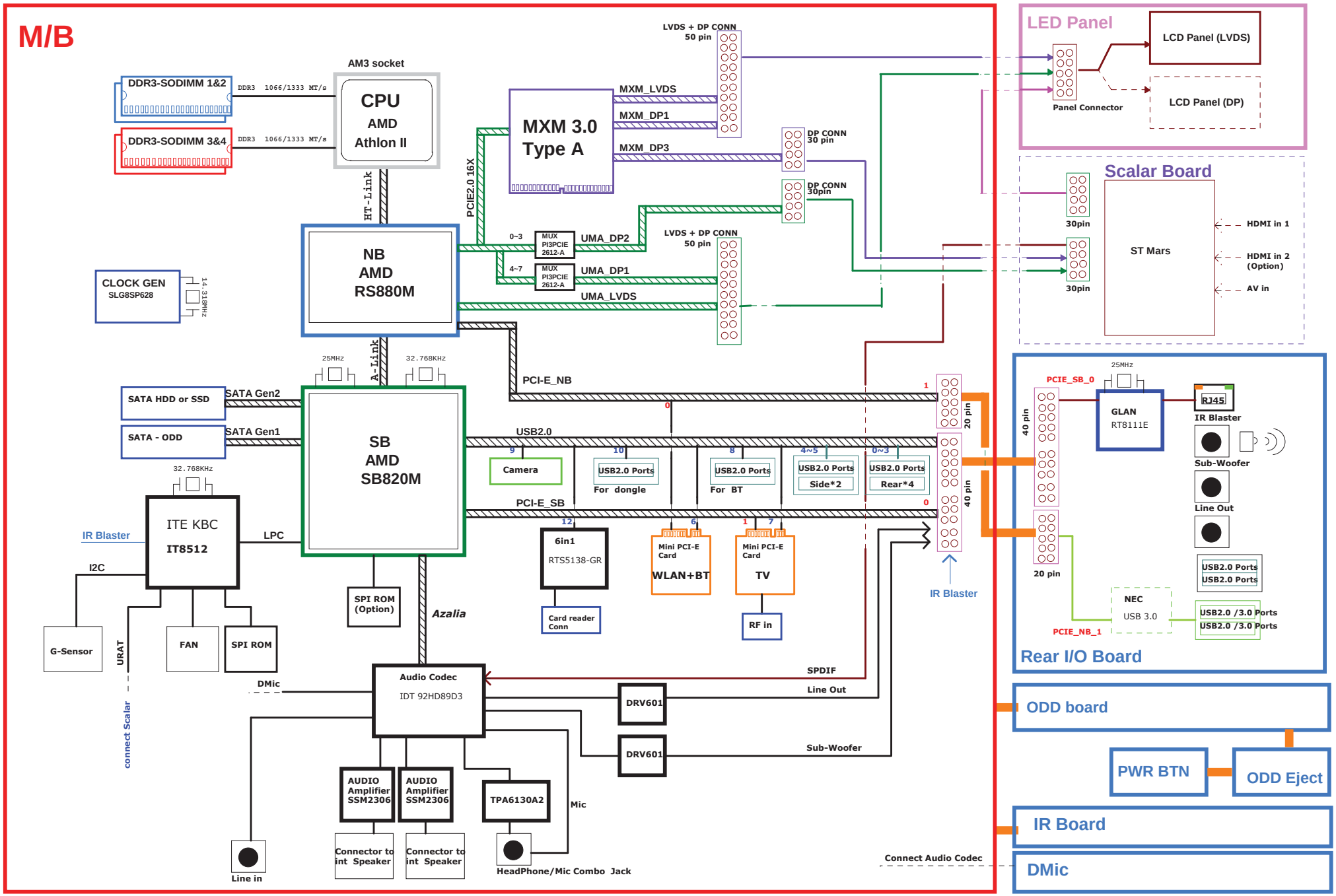
M3 System Block Diagram



Quanta Computer Inc.
PROJECT : ZN8
Size | Document Number: System Block Diagram | Rev A
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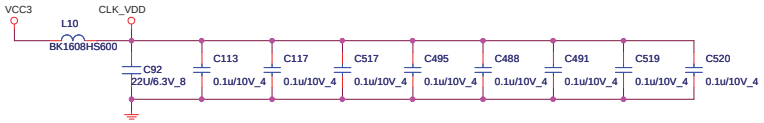
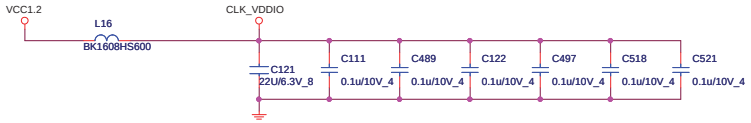
CLK_GEN_SLG8SP628





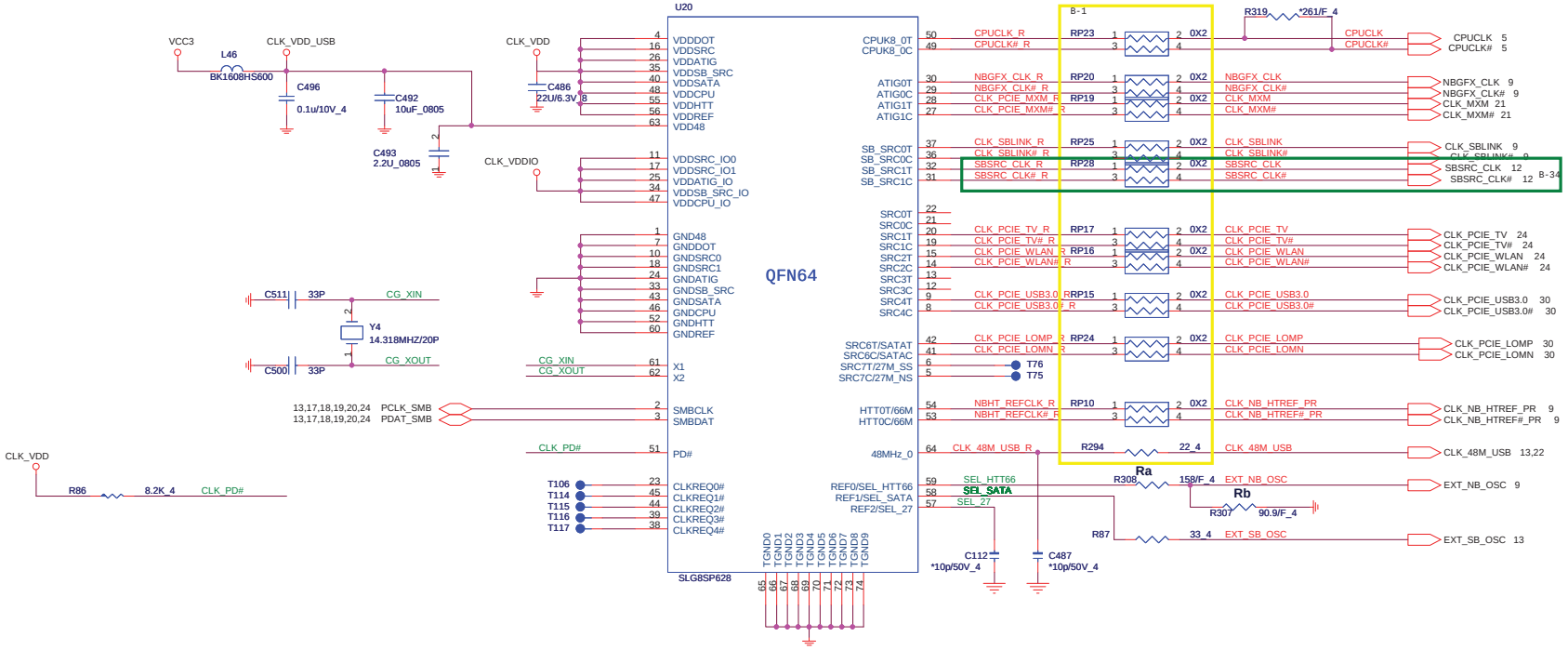
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

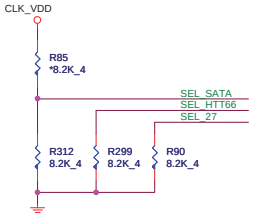
Place within 0.5" of CLKGEN

ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000





To CPU **200 Mhz**

To NB **RS880M for VGA**

To NB **100 Mhz**

To SB

To LAN Controller

To Mini PCIE Slot(TV)

To Mini PCIE Slot(WLAN) **100 Mhz**

To 6 in 1 Controller

To USB 3.0

To NB HT BUS **100 Mhz**

To SB USB **48 Mhz**

To NB

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

CLOCK INPUT TABLE

CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

Quanta Computer Inc.

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Size	Document Number	Rev
	Clock Generator	1A

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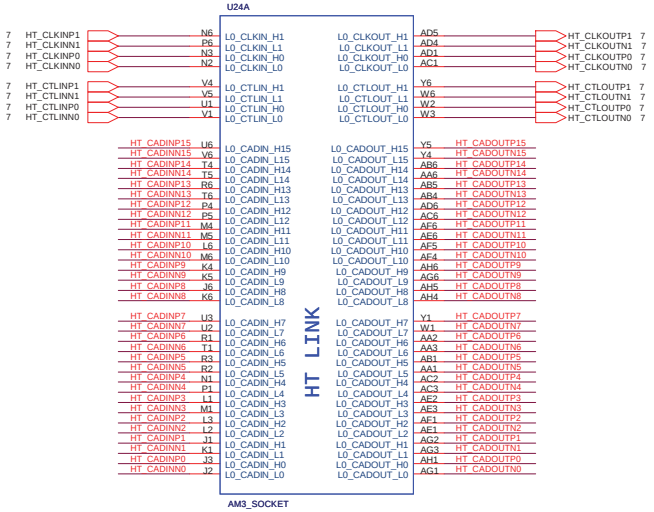
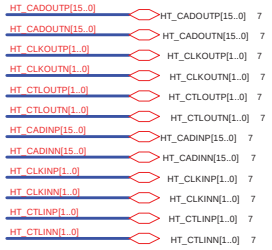
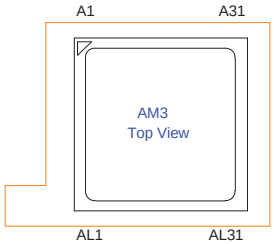
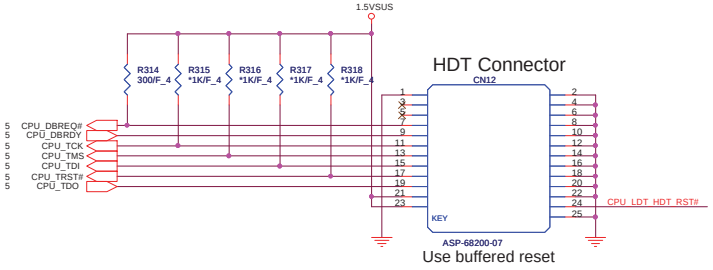
CPU HyperTransport and Debug



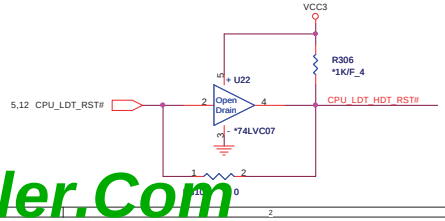






Use buffered reset

HDT Header



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PROJECT : ZN8		
Size	Document Number: CPU HyperTransport and Debug	Rev: 1A
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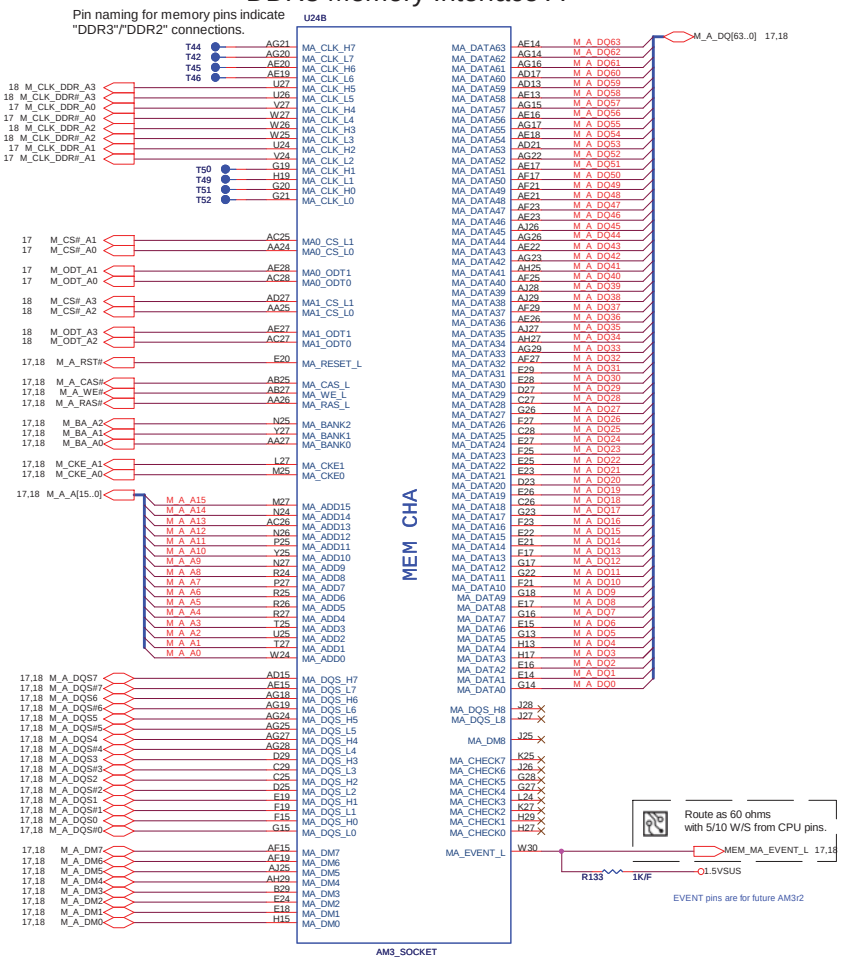
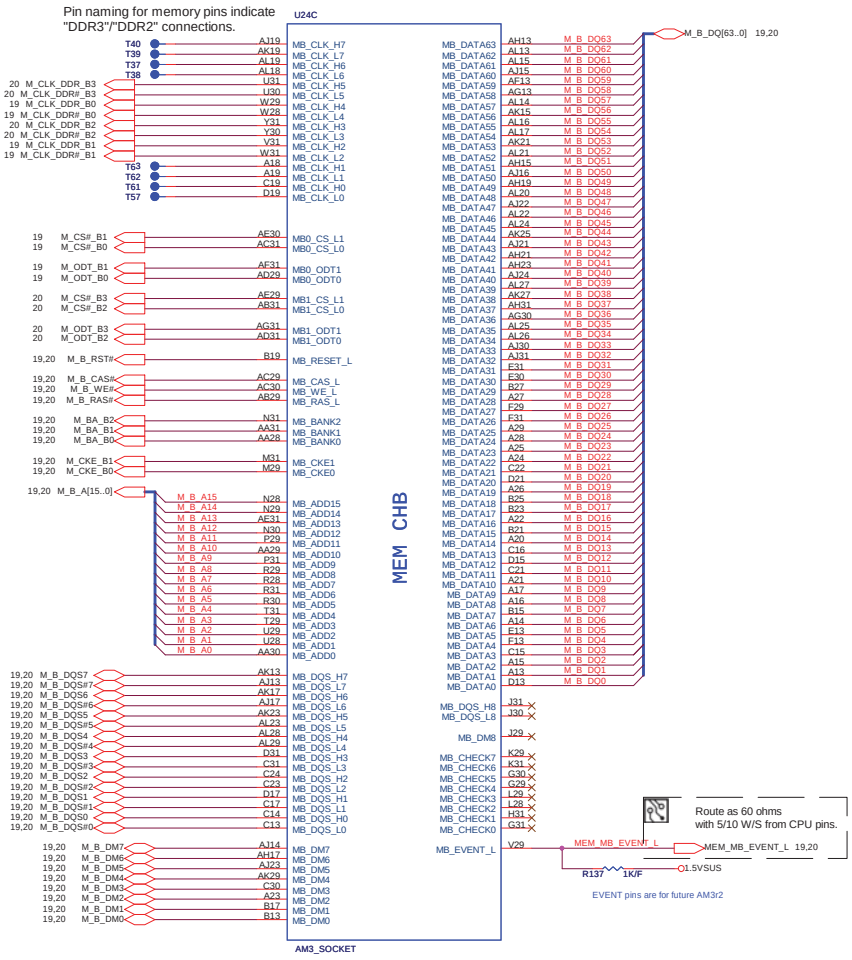
CPU Memory

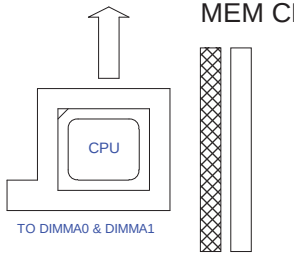
DDR3 Memory Interface A



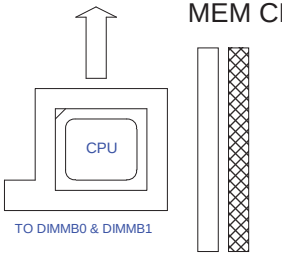
DDR3 Memory Interface B



MEM CHA



MEM CHB



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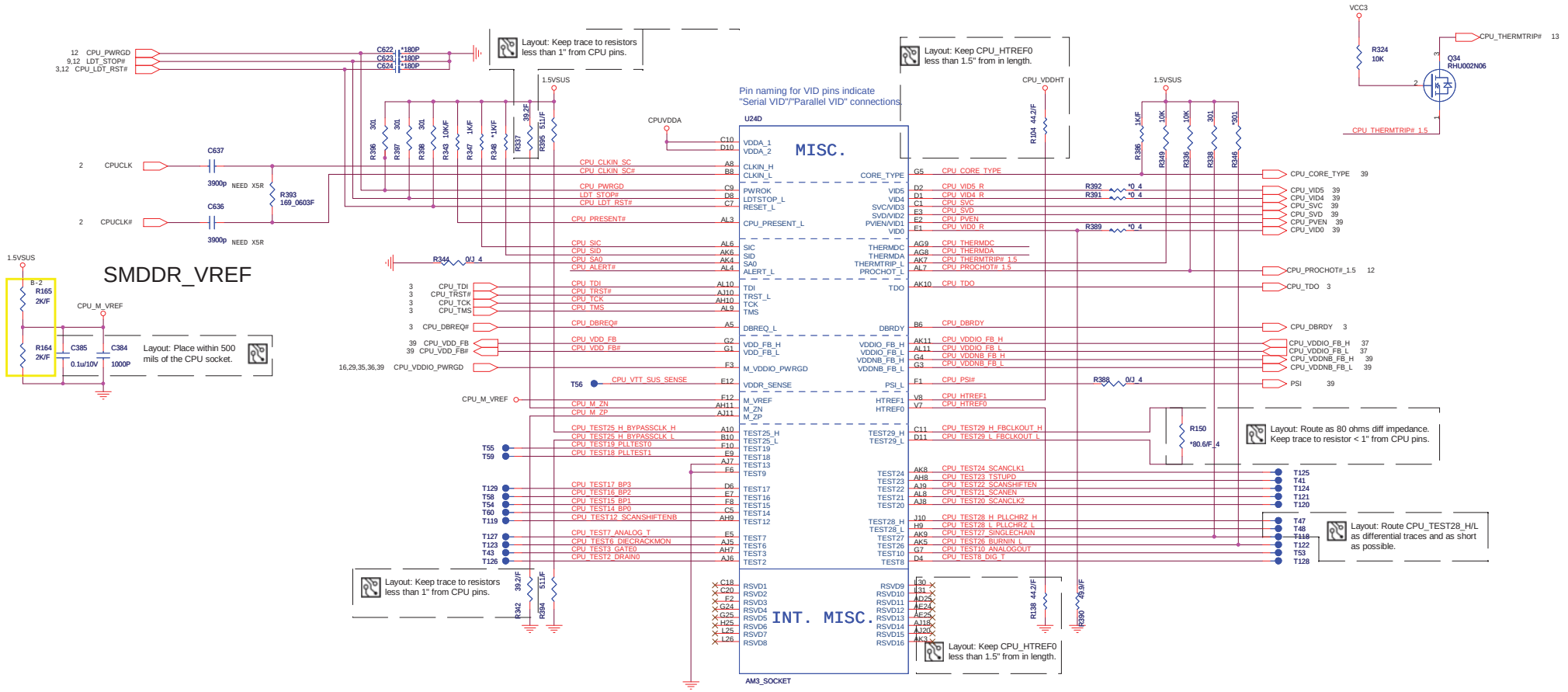
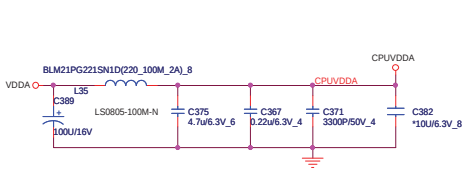
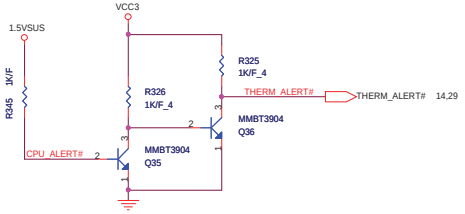
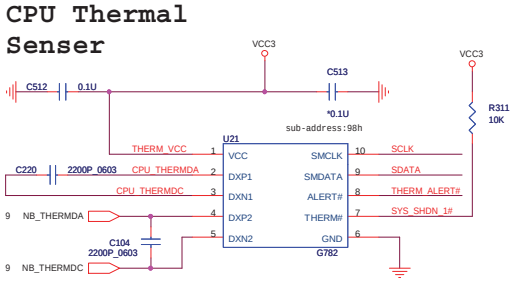
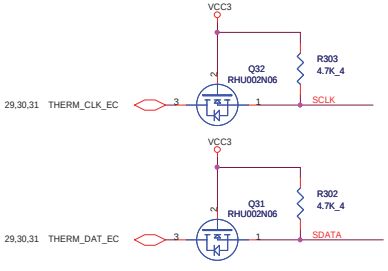
CPU Control and Miscellaneous

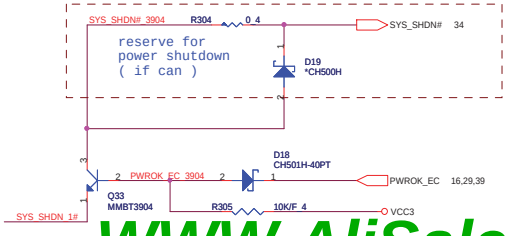












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PROJECT : ZN8		
Size	Document Number: CPU Control & Misc	Rev: 1A
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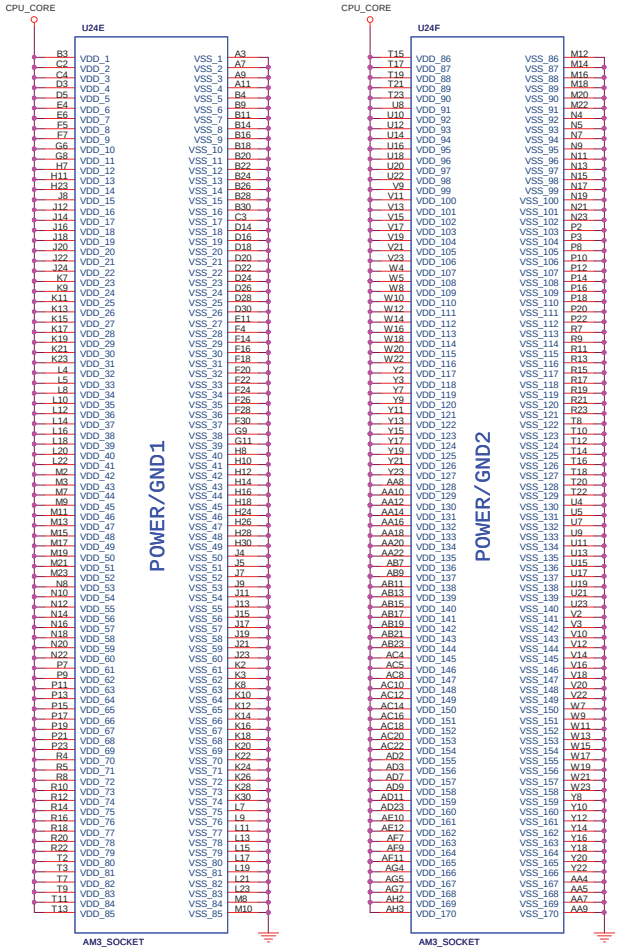
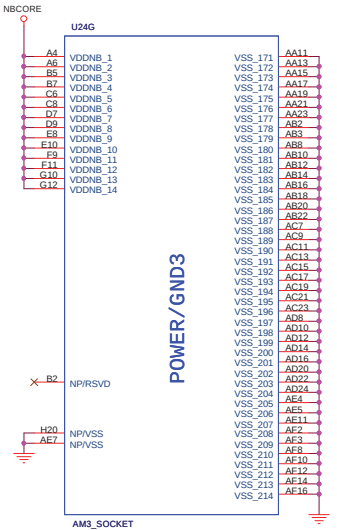
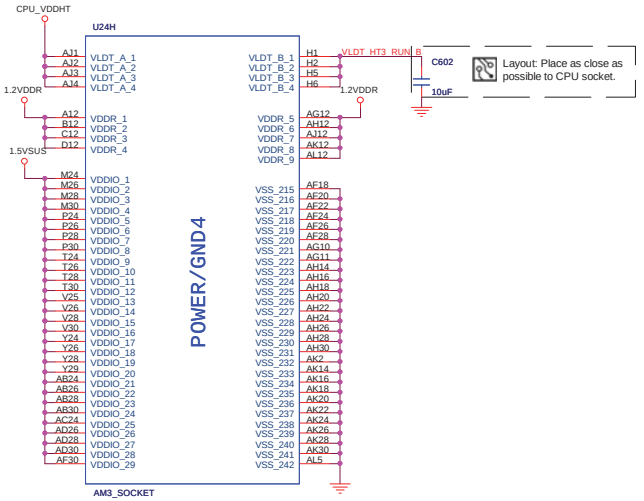
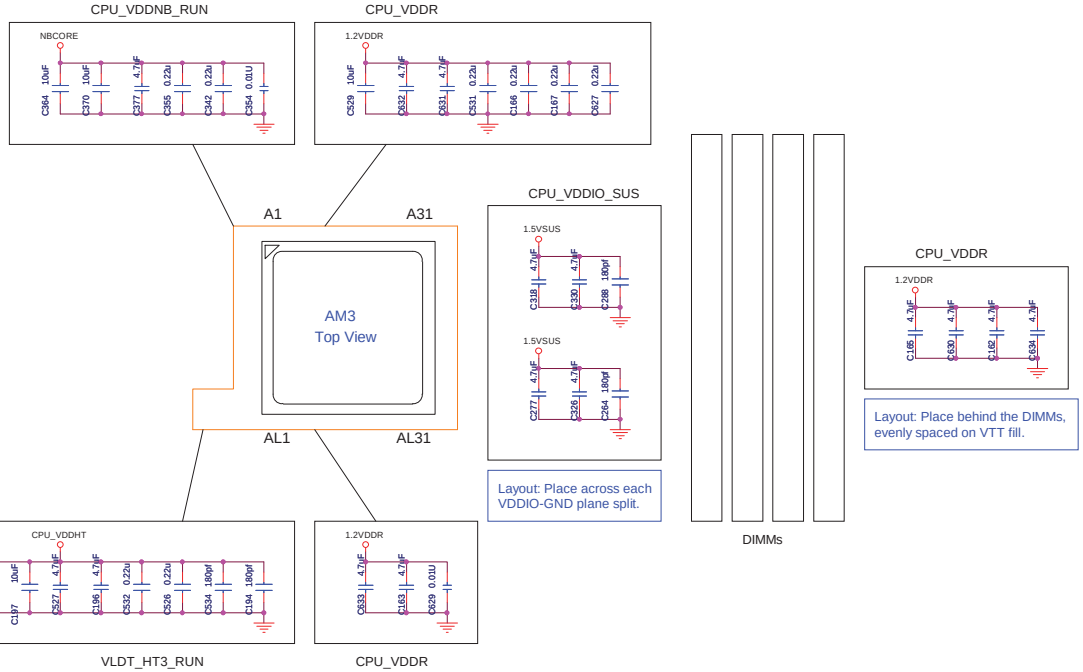
Processor Power and Ground

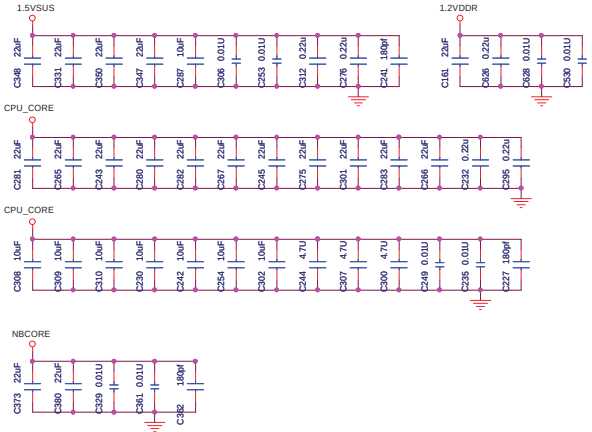








Bottom Side Decoupling



Quanta Computer Inc.
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	CPU Power & GND	1A
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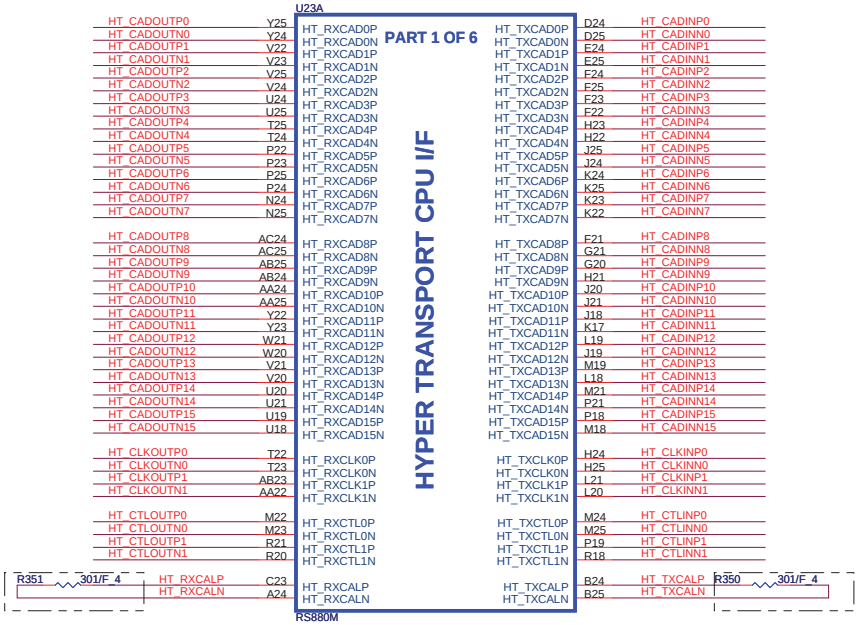

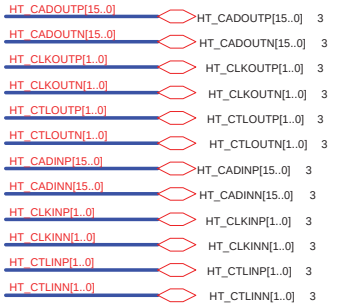

signals	RS880M
HT_TXCALP	R430 301 ohm 1%
HT_TXCALN	
HT_RXCALP	R434 301 ohm 1%
HT_RXCALN	

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Size	Document Number	Rev
	RS880M-HT Link I/F	1A

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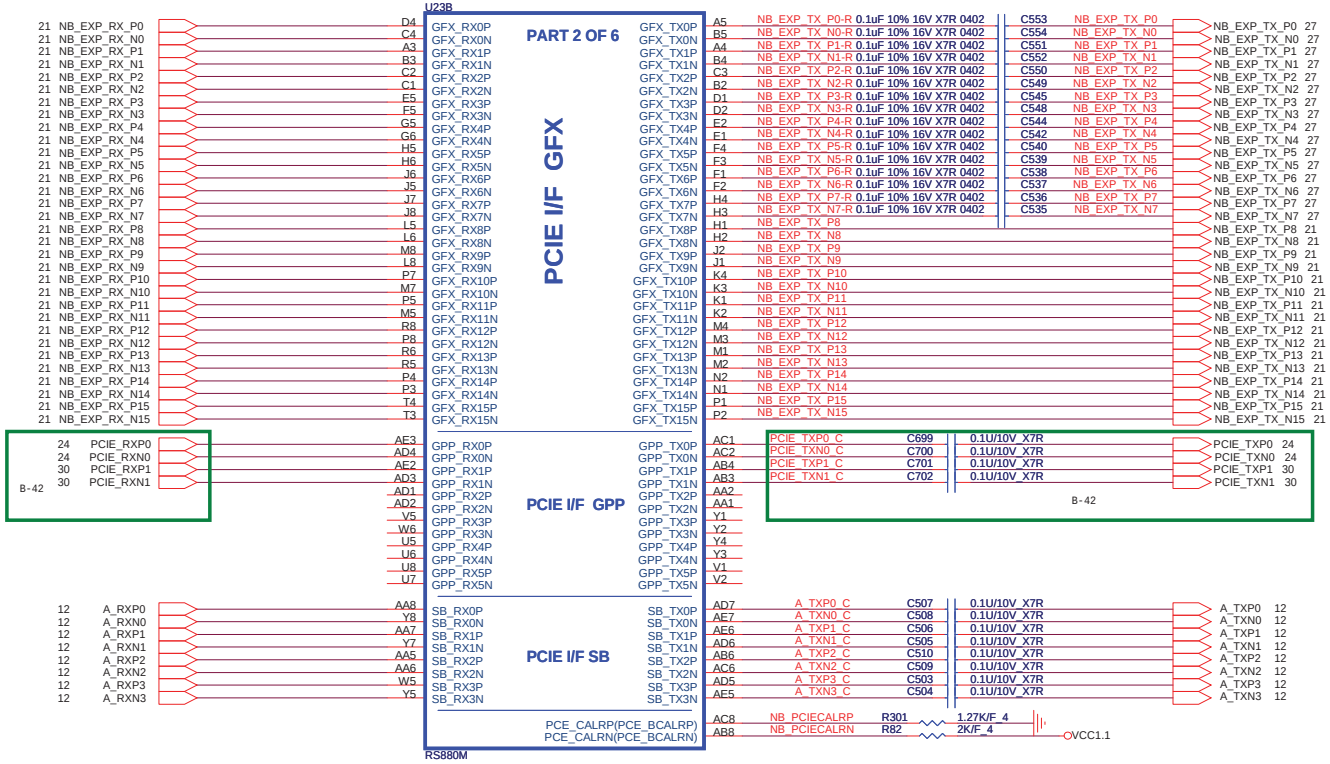

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	RS880M-PCIE I/F	1A

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Enables Debug Bus acess
through memory I/O pads and GPIO.
0 : Enable RS880M , Default
1 : Disable RS880M
(RX881 use DAC_VSYNC)

INT_CRT_VSYNC_NB — R357 3K/J_4 — VCC3
R352 *3K/J_4

Indicates if memory Side port
is available or not
0: Reserved
1: Required setting. Select with a pull-up
resistor on the strap
(RX881 use DAC_HSYNC)

INT_CRT_HSYNC_NB — R356 3K/J_4 — VCC3

U23C — RS880M — PART 3 OF 6

CRT/TVOUT
AVDD1(NC) AVDD2(NC) AVDDDI(NC) AVSSDI(NC) AVDDQ(NC) AVSSQ(NC)
C_Pr(DFT_GPIO5) Y(DFT_GPIO2) COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0) REDb(NC) GREEN(DFT_GPIO1) GREENb(NC) BLUE(DFT_GPIO3) BLUEb(NC)
DAC_HSYNC(PWM_GPIO4) DAC_VSYNC(PWM_GPIO6) DAC_SCL(PCE_RCALRN) DAC_SDA(PCE_TCALRN)
DAC_RSET(PWM_GPIO1)
TXOUT_L0P(NC) TXOUT_L0N(NC) TXOUT_L1P(NC) TXOUT_L1N(NC) TXOUT_L2P(NC) TXOUT_L2N(DBG_GPIO0) TXOUT_L3P(NC) TXOUT_L3N(DBG_GPIO2)
TXOUT_U0P(NC) TXOUT_U0N(NC) TXOUT_U1P(PCIE_RESET_GPIO3) TXOUT_U1N(PCIE_RESET_GPIO2) TXOUT_U2P(NC) TXOUT_U2N(NC) TXOUT_U3P(PCIE_RESET_GPIO5) TXOUT_U3N(NC)
TXCLK_LP(DBG_GPIO1) TXCLK_LN(DBG_GPIO3) TXCLK_UP(PCIE_RESET_GPIO4) TXCLK_UN(PCIE_RESET_GPIO1)

PLL PWR
PLLVDD(NC) PLLVDD18(NC) PLLVSS(NC)
VDDA18HTPLL
VDDA18PCIEPLL1 VDDA18PCIEPLL2

LVTM
VDDLTP18(NC) VSSLTP18(NC)
VDDLT18_1(NC) VDDLT18_2(NC) VDDLT33_1(NC) VDDLT33_2(NC)
VSSLT1(VSS) VSSLT2(VSS) VSSLT3(VSS) VSSLT4(VSS) VSSLT5(VSS) VSSLT6(VSS) VSSLT7(VSS)

PM
SYSRESETb POWERGOOD LDTSTOPb ALLOW_LDTSTOP

CLOCKs
HT_REFCLKP HT_REFCLKN
REFCLK_P/OSCIN(OSCIN) REFCLK_N(PWM_GPIO3)
GFX_REFCLKP GFX_REFCLKN
GPP_REFCLKP GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP) GPPSB_REFCLKN(SB_REFCLKN)
LVDS_DIGON(PCE_TCALRP) LVDS_BLON(PCE_RCALRP) LVDS_ENA_BL(PWM_GPIO2)

MIS.
I2C_CLK I2C_DATA DDC_CLK0/AUX0P(NC) DDC_DATA0/AUX0N(NC) DDC_CLK1/AUX1P(NC) DDC_DATA1/AUX1N(NC)
STRP_DATA
RSVD
AUX_CAL(NC)
TMDS_HPD(NC) HPD(NC)
SUS_STAT#(PWM_GPIO5)
THERMALDIODE_P THERMALDIODE_N
TESTMODE

140ohm CS11402FB19

28 INT_CRT_RED — R364 *0/short_4 — INT_CRT_RED_R — G18
28 INT_CRT_GREEN — R353 140/F_4 — R365 *0/short_4 — INT_CRT_GRE_R — G17 / G18
28 INT_CRT_BLU — R354 150/F_4 — R366 *0/short_4 — INT_CRT_BLU_R — F18 / F19
R355 150/F_4 — F19
10,28 INT_CRT_HSYNC — R361 *0/short_4 — INT_CRT_HSYNC_NB — A11
10,28 INT_CRT_VSYNC — R362 *0/short_4 — INT_CRT_VSYNC_NB — B11
28 INT_CRT_DDCDAT — R371 *0/short_4 — INT_CRT_DDCDAT_NB — F8
28 INT_CRT_DDCCLK — R370 *0/short_4 — INT_CRT_DDCCLK_NB — E8
R115 715/F_6 — DAC_RSET_NB — G14

+3V_AVDD_NB — F12 / E12
+1.8V_AVDDDI_NB — F14 / G15
+1.8V_AVDDQ_NB — H15 / H14
+1.1V_PLLVDD — A12
+1.8V_PLLVDD18 — D14 / B12
20mA +1.8V_VDDA18HTPLL — H17
120mA +1.8V_VDDA18PCIEPLL — D7 / E7

B-66
12 A_RST#_SB
16 NB_PWRGD
R111 0_2
NB_RST# IN — D8
NB_PWRGD — A10
NB_LDT_STOP# — C10
NB_ALLOW_LDTSTOP — C12

2 CLK_NB_HTREF_PR — C25
2 CLK_NB_HTREF#_PR — C24
2 EXT_NB_OSC — RP27 4 3 0_4P2R_4 1 2 B-3 — NB_REFCLK_N — R313 *4.7K — E11 / F11
2 NBGFX_CLK — T2
2 NBGFX_CLK# — R309 *4.7K — T1
B-36
2 CLK_SBLINK — V4
2 CLK_SBLINK# — V3
B-4 21,26 LCD_CLK — B9
21,26 LCD_DAT — A9
26 DP_AUX0P — A8
26 DP_AUX0N — B8
26 DP_AUX1P — B7
26 DP_AUX1N — A7
STRP_DATA — B10
T36 — G11
R358 150R — RS880_AUX_CAL — C8

VCC1.1 — B-35 — R373 150/F_4 — R375 150/F_4 — for EXT Gen

For A11 version
R335 *49.9/F_4 — CLK_SBLINK
R333 *49.9/F_4 — CLK_SBLINK#

VCC3 — R360 4.7K/J_4 — R359 4.7K/J_4 — EDID_CLK — EDID_DATA

VCC3 — R374 *2K/F — STRP_DATA — R372 *2K/F

DDR3 based CPU : Level shifted to 1.8 V on the
Northbridge side using an open-drain buffer and
pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor
on the Northbridge side.

VCC1.8 — R119 1K/F_4 — NB_LDT_STOP#
VCC1.8 — U8 Open Drain - 74LVC07
5,12 LDT_STOP#
12 ALLOW_LDTSTOP — R120 *0/short_4 — NB_ALLOW_LDTSTOP
R121 1K/F_4 — VCC1.8

ALLOW_LDTSTOP	OC
LDT_STOP#	3.3V Input

* Although defined as 3.3V I/Os, a 1.8V signaling level is supported on LDT_STOP#/ALLOW_LDTSTOP given that Vih is 1.4V.
3.3V to 1.8V level translation is not required.

VCC3 — L33 BLM18PG181SN1D(180,1.5A)_6 — +3V_AVDD_NB — C238 2.2U/6.3V_6
AVDD-DAC Analog

VCC1.1 — BLM18PG181SN1D(180,1.5A)_6 — L28 — +1.1V_PLLVDD — C222 2.2U/6.3V_6
PLLVDD - Graphics PLL

VCC1.8 — L32 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_VDDLTP18_NB — C234 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL

VCC1.8 — L31 BLM21PG221SN1D(220,100M,2A)_8 — +1.8V_VDDLT_18_NB — C202 4.7U/6.3V_6 — C221 2.2U/6.3V_6 — C200 0.1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital

VCC1.8 — PLLVDD18 - Graphics PLL — L29 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_PLLVDD18 — C233 10U/6.3V_8 — C203 0.1U/10V_4

VCC1.8 — R117 0/J_6 — +1.8V_AVDDDI_NB — C223 0.1U/10V_4
AVDDI-DAC Digital
BLM18PG181SN1D(180,1.5A)_6 — L30 — +1.8V_AVDDQ_NB — C224 0.1U/10V_4
AVDDQ-DAC Bandgap Reference

VCC1.8 — VDDA18PCIEPLL -PCIE PLL — L27 BLM18PG221SN1D _6 — 20mils width — +1.8V_VDDA18PCIEPLL — C198 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL — L17 BLM18PG221SN1D _6 — 20mils width — +1.8V_VDDA18HTPLL — C193 2.2U/6.3V_6

A13 +1.8V_VDDLTP18_NB — B13
A15 +1.8V_VDDLT_18_NB — B15
A14 — B14
C14 D15 C16 C18 C20 E20 C22

A22 B22 A21 B21 B20 A20 A19 B19 — LVDS_TX_L0P 26 / L0N 26 / L1P 26 / L1N 26 / L2P 26 / L2N 26 / L3P 26 / L3N 26
B18 A18 A17 B17 D20 D21 D18 D19 — LVDS_TX_U0P 26 / U0N 26 / U1P 26 / U1N 26 / U2P 26 / U2N 26 / U3P 26 / U3N 26
B16 A16 D16 D17 — LVDS_TXCLK_LP 26 / LN 26 / UP 26 / UN 26

E9 F7 G12 — R107 *0/short_4 — R112 *0/short_4 — R113 *0/short_4 — INT_LVDS_PWREN 27 / INT_LVDS_BRIGHT 27 / INT_LVDS_BLON 27
R108 4.7K — R106 4.7K — R109 4.7K

D9 D10 — DP2_HPD 26 / DP_HPD 26
D12 — R127 *0/short_4 — SUS_STAT# 13 / SUS_STAT#_R 10
AE8 NB_THERMDA — NB_THERMDA 5
AD8 NB_THERMDC — NB_THERMDC 5
D13 TEST_EN — R122 1.8K/F_4

RS880M DEBUG PIN MAPPING

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL

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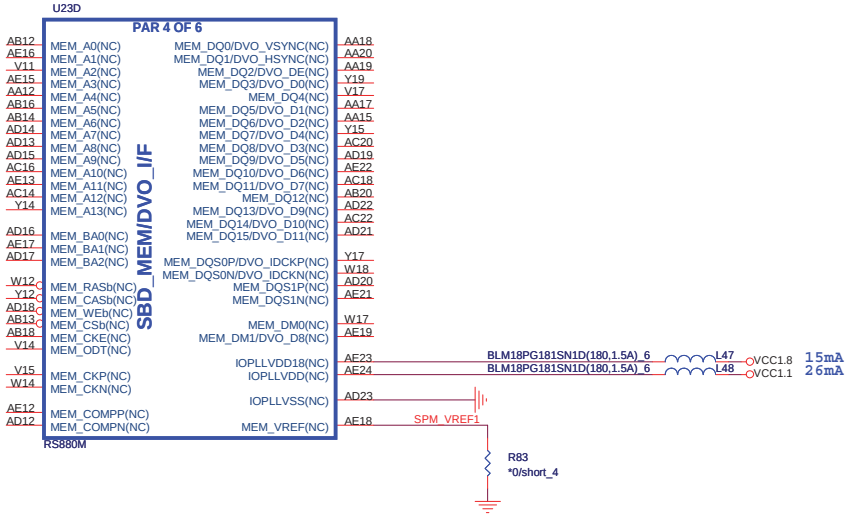
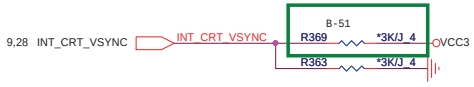
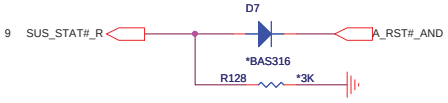




STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

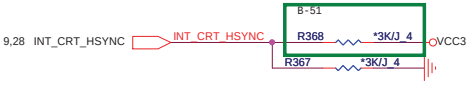
RS880M	
1 Disable	
0 Enable	



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

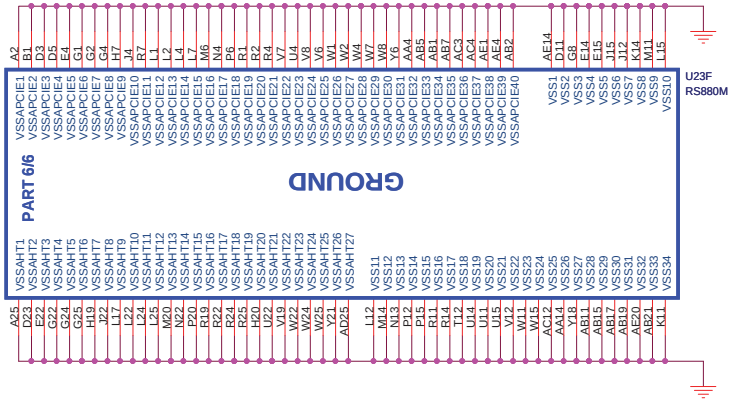
Quanta Computer Inc.
PROJECT : ZN8

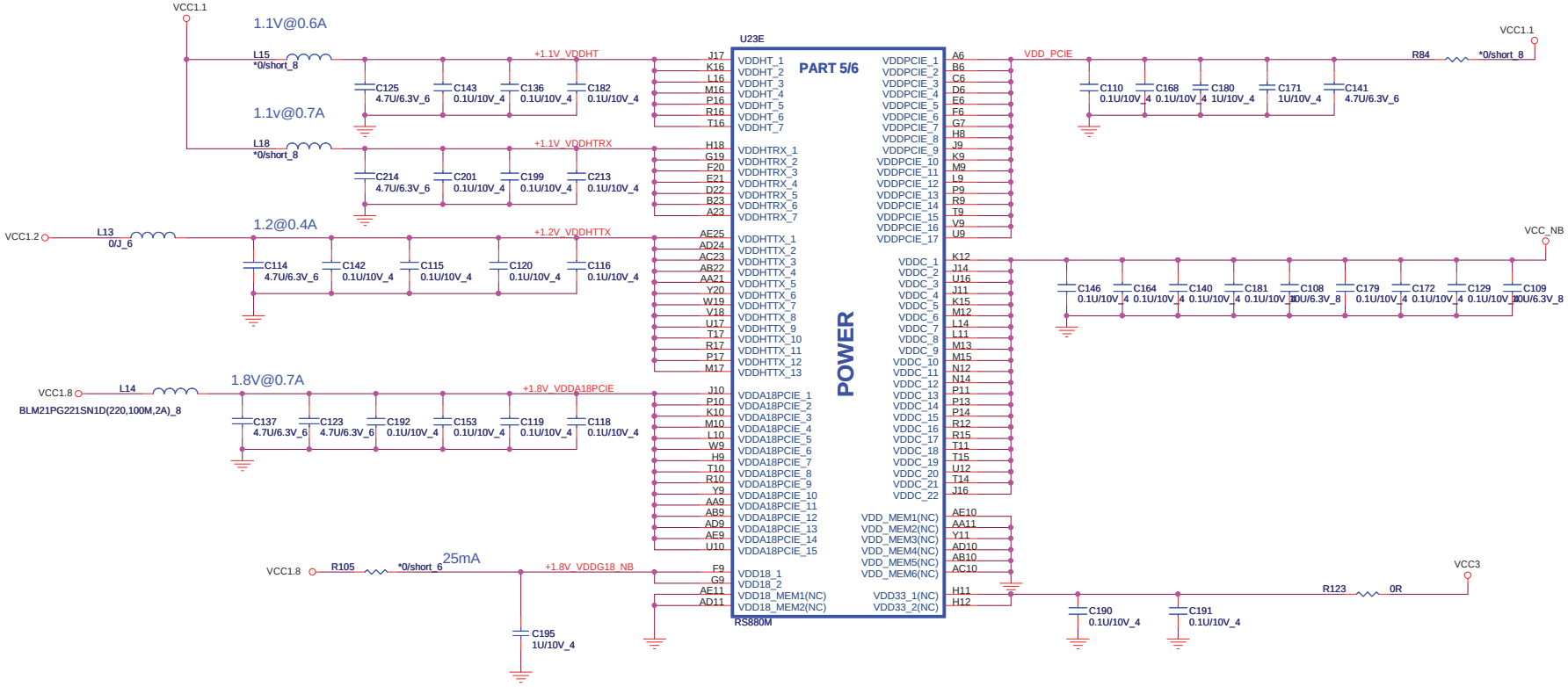
Size	Document Number	Rev
	RS880M-Spmem/Straps	1A

Date: Monday, March 22, 2010 Sheet 10 of 40

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC



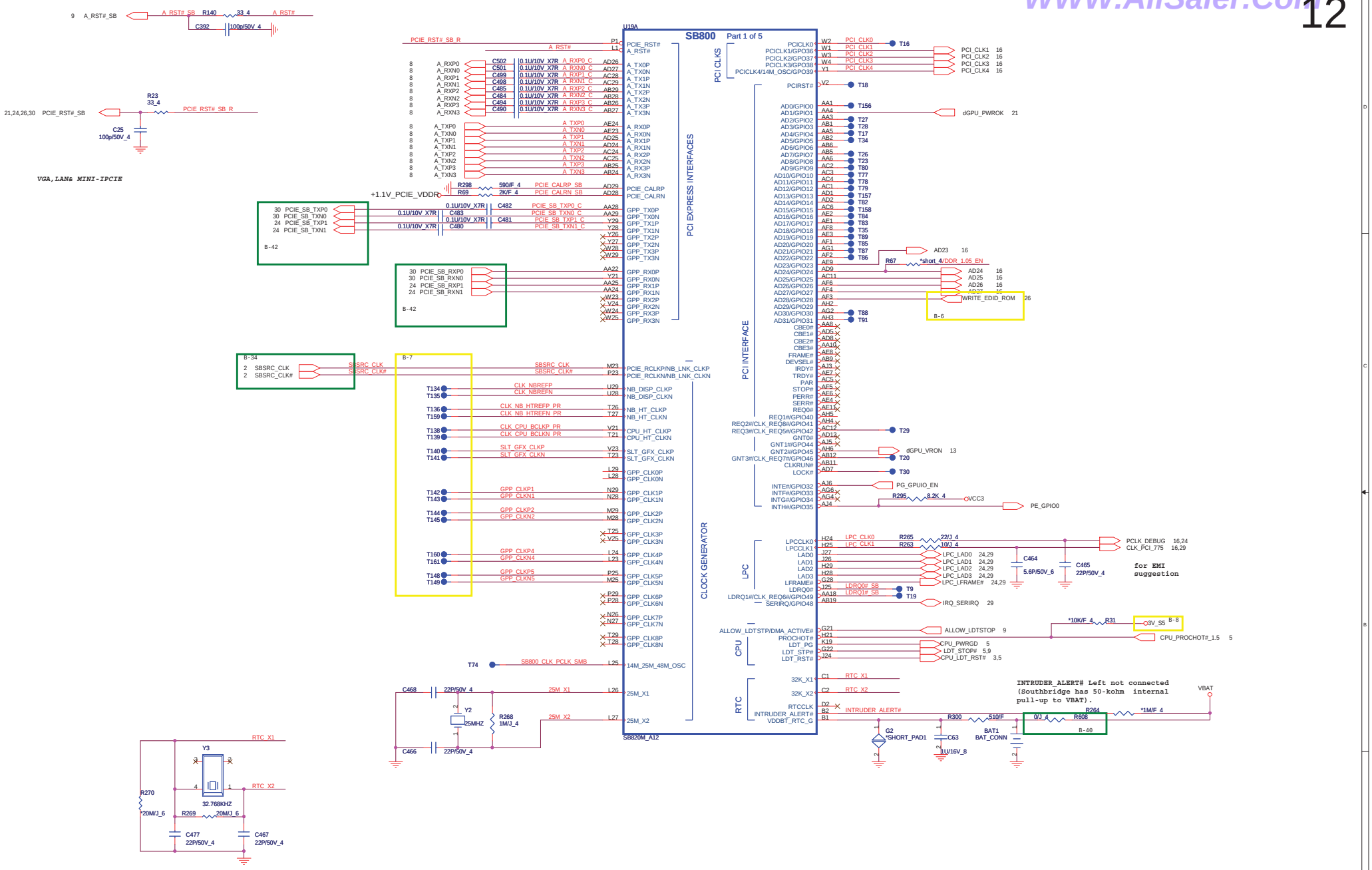


H1
FANSINK

SK2
RX740, RS720, RS780, Socket
DNI

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	RS880M-Power	1A
Date: Monday, March 22, 2010	Sheet 11 of 40	



Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	SB820-PCIE/PCI/CPU/LPC 1/4		1A
Date: Monday, March 22, 2010		Sheet 12 of 40	

NC only ,Can't be install

R41 *2.2K/J_4 SB_TEST0
R37 *2.2K/J_4 SB_TEST1
R51 *2.2K/J_4 SB_TEST2

R609 *2.2K/J_4 PCIE_WAKE#

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

SCL0/SDATA0 is 3V tolerance Clock gen/Robson/TV AMD datasheet define it tuner /DDR2/DDR2 thermal/Accelerometer

R73 2.2K/J_4 PCLK_SMB
R74 2.2K/J_4 PDAT_SMB

SCL1/SDATA1 is 3V/S5 tolerance AMD datasheet define it

R36 2.2K/J_4 SB_SMBCLK1
R47 2.2K/J_4 SB_SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance AMD datasheet define it

R33 2.2K/J_4 SB_SCLK2
R32 2.2K/J_4 SB_SDATA2
R186 *2.2K/J_4 DNBSWON#

R52 *4.7K/J_4 SUS_STAT#

U19D

SB800 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC
USB_RCOMP

USB 1.1 USB MISC

USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N

USB 2.0

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

GPIO

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

USB OC

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

HD AUDIO

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

GBE LAN

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

EMBEDDED CTRL

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226

SB820M_A12

MULTI-TOUCH
Dongle
USB
CAMERA
BLUETOOTH
TV MINI
CARD
WLAN MINI
CARD
Side
USB
Side
USB
USB
board
USB
board
USB
board
USB
board

R80 100K/F_6
D5 RB501V-40
D4 *SW@RB501V-40
C107 0.1u/10V_4

>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)

HD audio interface is +3VS5 voltage

R56 *10K/F_4
R422 *10K/F_4
R144 *10K/F_4
R272 *10K/F_4
R59 *10K/F_4
R276 10K/F_4
R63 10K/F_4
R58 10K/F_4
R65 10K/F_4
R64 10K/F_4

CN1
C23 10/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG
SB JTAG

R257 22_4
R44 11.8K/F_6
R266 10K/F_4
R267 10K/F_4

R610 *0_4
R611 22K
C703 4.7U/6.3V_6

R57 *0/short_4

R273 33/J_4
R249 33_4C478 *10P/50V_4
R277 33/J_4
R247 33_4C479 *10P/50V_4
R271 33/J_4
R248 33_4C75 10P/50V_4
R281 33/J_4
R250 33_4

If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/4	1A
Date: Monday, March 22, 2010	Sheet 13 of 40	

SATA PORT 0,1,2,3
can support AHCI
mode

SATA1

SATA ODD

U19B

SB800
Part 2 of 5

SERIAL ATA

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800-? 1% resistor to GND. P/N:CS18062FB00(806 Ohm) SB800 A12: TBD-? 1% resistor to GND. (1K ohm)
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

FLASH

HW MONITOR

SPI ROM

SB820M_A12

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

8Mbit , SPI

*MX25L1605A

CONN RCPT 4x2

	ID4	ID3	ID2	ID1	ID0
0				UMA	14"
1				Discrete	15"

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	SB820-SATA/IDE/HWM/SPI 3/4	1A

Date: Monday, March 22, 2010 Sheet 14 of 40

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

SB820 without GBE: Connected to GND plane.

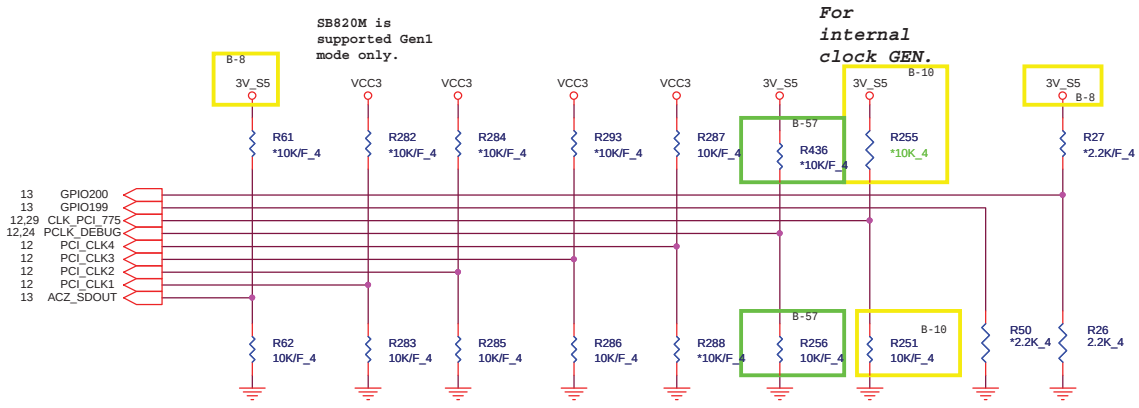
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

For support USB wakeup-->3V_S5

Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	SB820-PWR/DECOUPLING 4/4		1A
Date: Monday, March 22, 2010		Sheet 15 of 40	

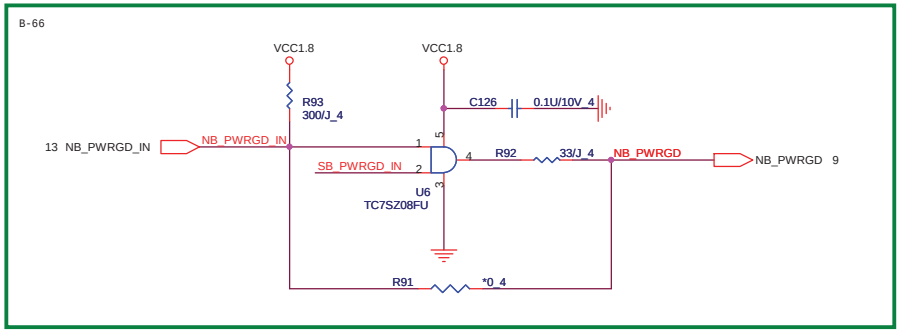
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



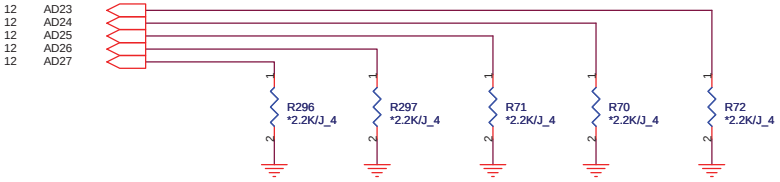
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K



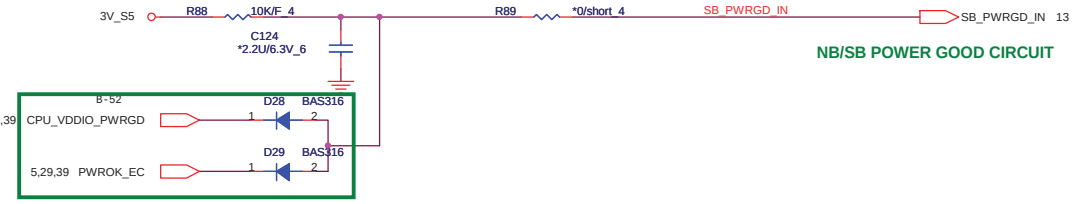
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



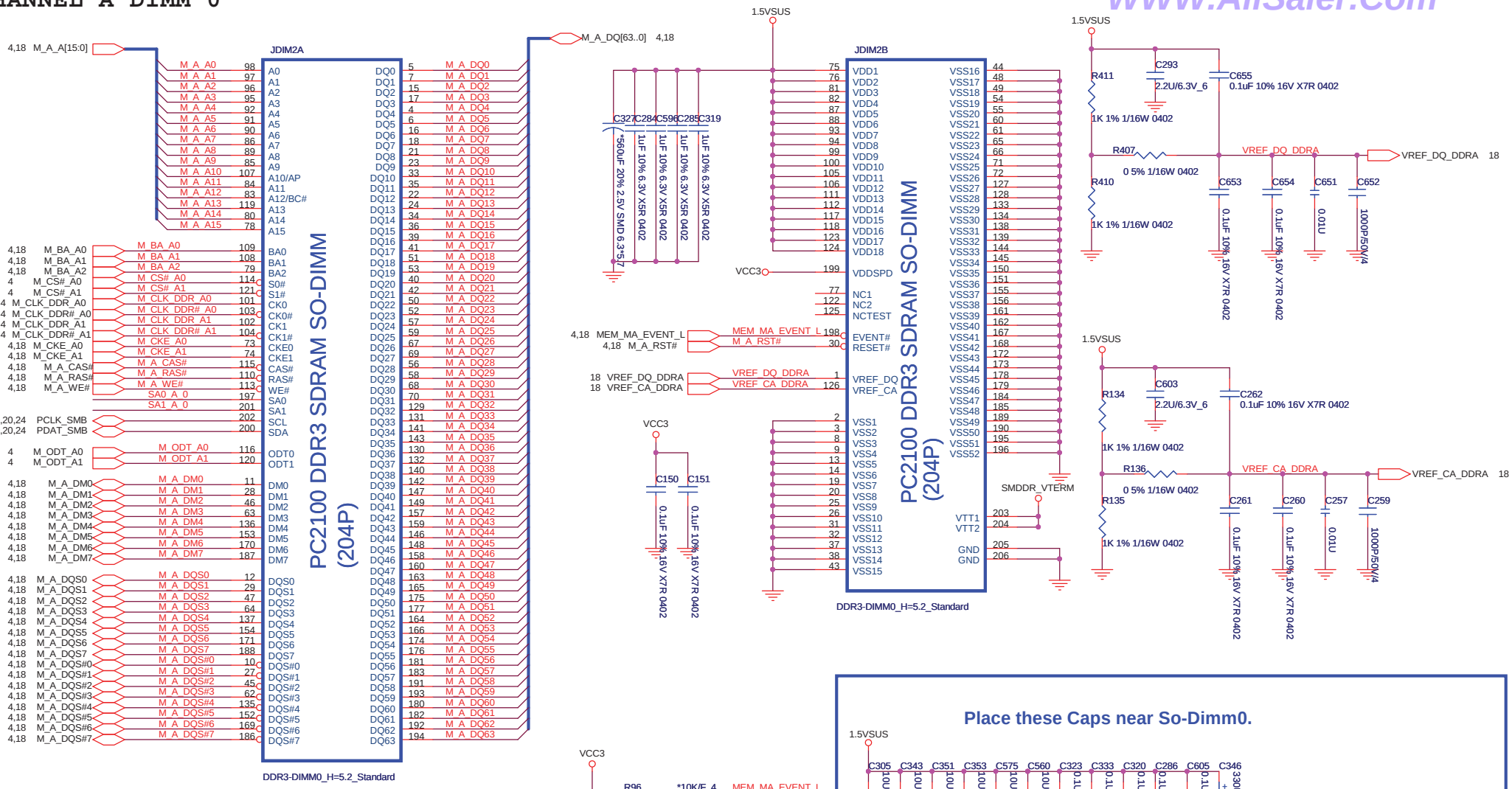
NB/SB POWER GOOD CIRCUIT

Quanta Computer Inc.
PROJECT : ZN8

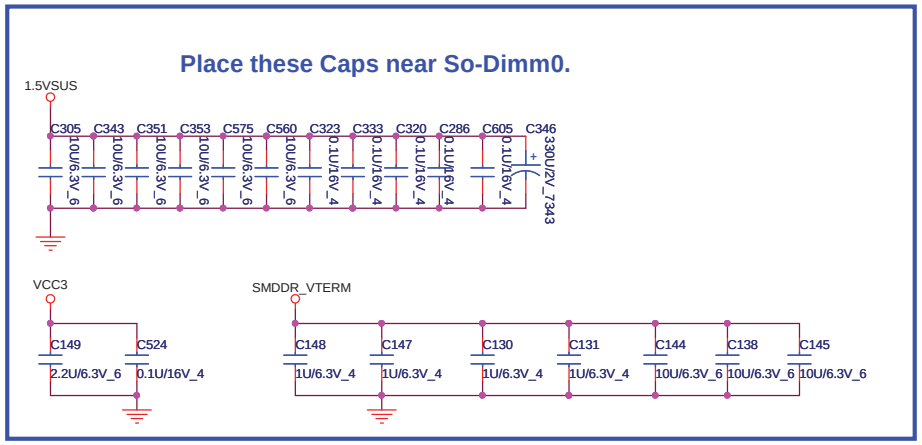
Size	Document Number	Rev
	SB820-STRAPS/PWRGD	1A

Date: Monday, March 22, 2010 Sheet 16 of 40

CHANNEL A DIMM 0



Place these Caps near So-Dimm0.



FOX H:9.2 white

PCB Placement

SPD SA0	0
SPD SA1	0

R98 0 5% 1/16W 0402 SA1_A_0
R99 0 5% 1/16W 0402 SA0_A_0

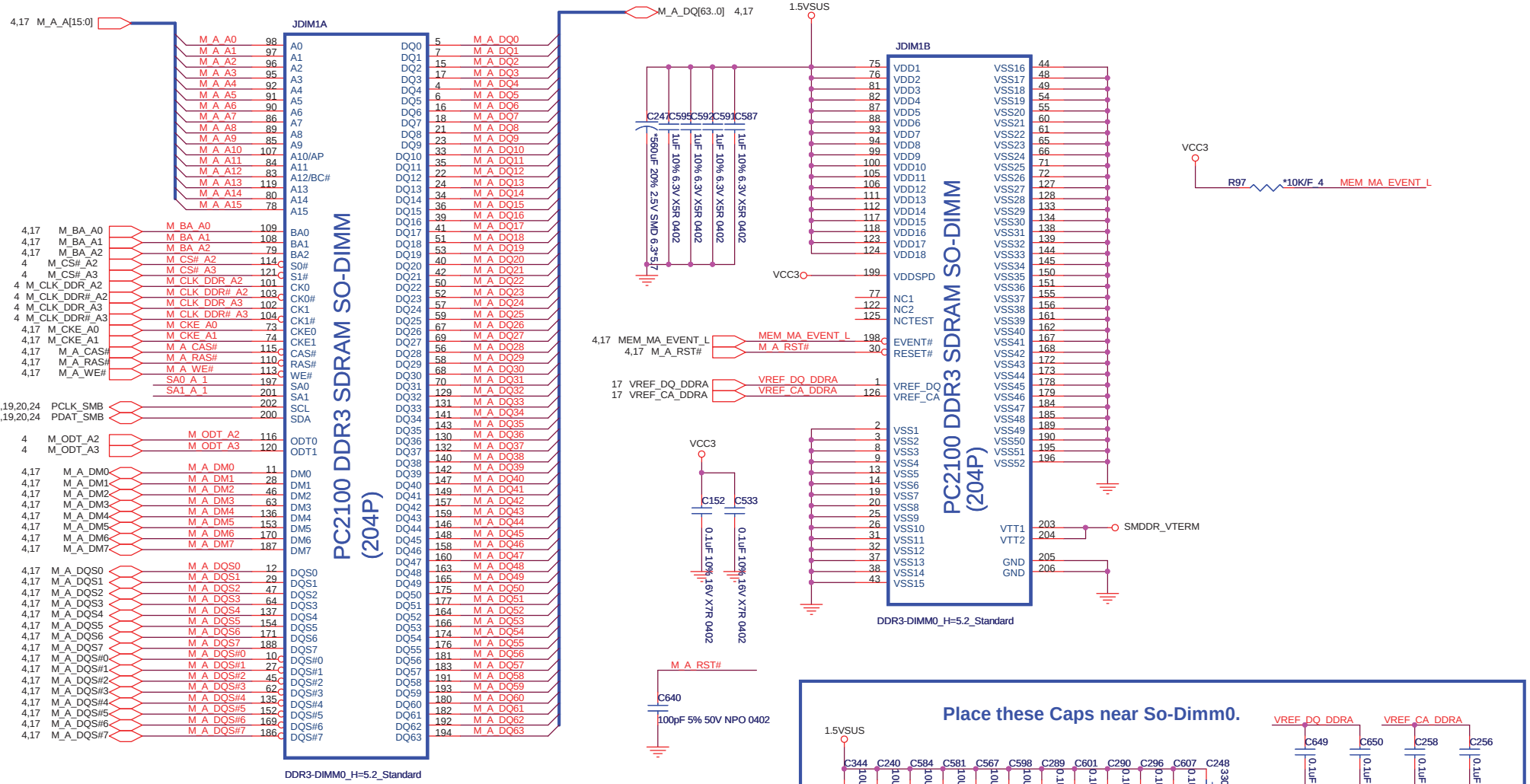
AM3

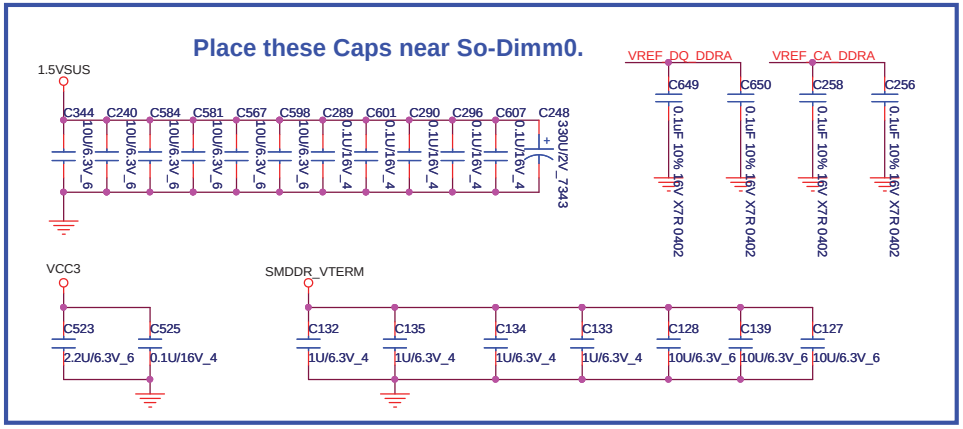
Quanta Computer Inc.

PROJECT : ZN8

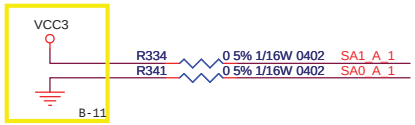
Size	Document Number	Rev
	DDR3 CHA DIMM 0	1A
Date: Monday, March 22, 2010	Sheet 17 of 40	

CHANNEL A DIMM 1



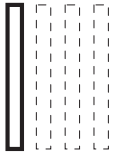


SPD SA0	1
SPD SA1	0



AM3

FOX H:5.2 white
PCB Placement



Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	DDR3 CHA DIMM1	1A
Date: Monday, March 22, 2010	Sheet 18 of 40	

CHANNEL B DIMM 0

JDIM4A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=5.2_Standard

JDIM4B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=5.2_Standard

M_B_DQ[63:0] 4,20

4,20 M_B_A[15:0]

M_B_A0 98
M_B_A1 97
M_B_A2 96
M_B_A3 95
M_B_A4 92
M_B_A5 91
M_B_A6 90
M_B_A7 86
M_B_A8 89
M_B_A9 85
M_B_A10 107
M_B_A11 84
M_B_A12 83
M_B_A13 119
M_B_A14 80
M_B_A15 78

4,20 M_BA_B0 M_BA_B0 109
4,20 M_BA_B1 M_BA_B1 108
4,20 M_BA_B2 M_BA_B2 79
4 M_CS#_B0 M_CS#_B0 114
4 M_CS#_B1 M_CS#_B1 121
4 M_CLK_DDR_B0 M_CLK_DDR_B0 101
4 M_CLK_DDR#_B0 M_CLK_DDR#_B0 103
4 M_CLK_DDR_B1 M_CLK_DDR_B1 102
4 M_CLK_DDR#_B1 M_CLK_DDR#_B1 104
4,20 M_CKE_B0 M_CKE_B0 73
4,20 M_CKE_B1 M_CKE_B1 74
4,20 M_B_CAS# M_B_CAS# 115
4,20 M_B_RAS# M_B_RAS# 110
4,20 M_B_WE# M_B_WE# 113
SA0_B_0 197
SA1_B_0 201
2,13,17,18,20,24 PCLK_SMB 202
2,13,17,18,20,24 PDAT_SMB 200
4 M_ODT_B0 M_ODT_B0 116
4 M_ODT_B1 M_ODT_B1 120

4,20 M_B_DM0 M_B_DM0 11
4,20 M_B_DM1 M_B_DM1 28
4,20 M_B_DM2 M_B_DM2 46
4,20 M_B_DM3 M_B_DM3 63
4,20 M_B_DM4 M_B_DM4 136
4,20 M_B_DM5 M_B_DM5 153
4,20 M_B_DM6 M_B_DM6 170
4,20 M_B_DM7 M_B_DM7 187

4,20 M_B_DQS0 M_B_DQS0 12
4,20 M_B_DQS1 M_B_DQS1 29
4,20 M_B_DQS2 M_B_DQS2 47
4,20 M_B_DQS3 M_B_DQS3 64
4,20 M_B_DQS4 M_B_DQS4 137
4,20 M_B_DQS5 M_B_DQS5 154
4,20 M_B_DQS6 M_B_DQS6 171
4,20 M_B_DQS7 M_B_DQS7 188
4,20 M_B_DQS#0 M_B_DQS#0 10
4,20 M_B_DQS#1 M_B_DQS#1 27
4,20 M_B_DQS#2 M_B_DQS#2 45
4,20 M_B_DQS#3 M_B_DQS#3 62
4,20 M_B_DQS#4 M_B_DQS#4 135
4,20 M_B_DQS#5 M_B_DQS#5 152
4,20 M_B_DQS#6 M_B_DQS#6 169
4,20 M_B_DQS#7 M_B_DQS#7 186

M_B_DQ0 5
M_B_DQ1 7
M_B_DQ2 15
M_B_DQ3 17
M_B_DQ4 4
M_B_DQ5 6
M_B_DQ6 16
M_B_DQ7 18
M_B_DQ8 21
M_B_DQ9 23
M_B_DQ10 33
M_B_DQ11 35
M_B_DQ12 22
M_B_DQ13 24
M_B_DQ14 34
M_B_DQ15 36
M_B_DQ16 39
M_B_DQ17 41
M_B_DQ18 51
M_B_DQ19 53
M_B_DQ20 40
M_B_DQ21 42
M_B_DQ22 50
M_B_DQ23 52
M_B_DQ24 57
M_B_DQ25 59
M_B_DQ26 67
M_B_DQ27 69
M_B_DQ28 56
M_B_DQ29 58
M_B_DQ30 68
M_B_DQ31 70
M_B_DQ36 129
M_B_DQ33 131
M_B_DQ34 141
M_B_DQ35 143
M_B_DQ32 130
M_B_DQ37 132
M_B_DQ38 140
M_B_DQ39 142
M_B_DQ41 147
M_B_DQ43 149
M_B_DQ40 157
M_B_DQ42 159
M_B_DQ44 146
M_B_DQ45 148
M_B_DQ46 158
M_B_DQ47 160
M_B_DQ48 163
M_B_DQ49 165
M_B_DQ50 175
M_B_DQ51 177
M_B_DQ52 164
M_B_DQ53 166
M_B_DQ54 174
M_B_DQ55 176
M_B_DQ56 181
M_B_DQ57 183
M_B_DQ58 191
M_B_DQ59 193
M_B_DQ60 180
M_B_DQ61 182
M_B_DQ62 192
M_B_DQ63 194

M_B_DQ32----JDIM4.130-----JDIM3.130
M_B_DQ36----JDIM4.129-----JDIM3.129

M_B_DQ41----JDIM4.147-----JDIM3.147
M_B_DQ43----JDIM4.149-----JDIM3.149
M_B_DQ42----JDIM4.159-----JDIM3.159
M_B_DQ40----JDIM4.157-----JDIM3.157

1.5VSUS

C340 *560UF 20% 2.5V SMD 6.3*5.7
C562 1uF 10% 6.3V X5R 0402
C564 1uF 10% 6.3V X5R 0402
C583 1uF 10% 6.3V X5R 0402
C568 1uF 10% 6.3V X5R 0402

VCC3

4,20 MEM_MB_EVENT_L
4,20 M_B_RST#
MEM_MB_EVENT_L
M_B_RST#

20 VREF_DQ_DDRB
20 VREF_CA_DDRB

SMDDR_VTERM

VCC3

C170 0.1uF 10% 16V X7R 0402
C169 0.1uF 10% 16V X7R 0402

R102 *10K/F_4 MEM_MB_EVENT_L

1.5VSUS

R171 1K 1% 1/16W 0402
C269 2.2U/6.3V_6
C398 0.1uF 10% 16V X7R 0402
R173 0 5% 1/16W 0402
VREF_DQ_DDRB
VREF_DQ_DDRB 20
R172 1K 1% 1/16W 0402
C402 0.1uF 10% 16V X7R 0402
C399 0.1uF 10% 16V X7R 0402
C400 0.01U
C401 1000P/50V/4

1.5VSUS

R118 1K 1% 1/16W 0402
C339 2.2U/6.3V_6
C252 0.1uF 10% 16V X7R 0402
R126 0 5% 1/16W 0402
VREF_CA_DDRB
VREF_CA_DDRB 20
R124 1K 1% 1/16W 0402
C255 0.1uF 10% 16V X7R 0402
C251 0.1uF 10% 16V X7R 0402
C236 0.01U
C228 1000P/50V/4

Place these Caps near So-Dimm0.

1.5VSUS

C338 10U/6.3V_6
C594 10U/6.3V_6
C317 10U/6.3V_6
C336 10U/6.3V_6
C279 10U/6.3V_6
C274 10U/6.3V_6
C571 0.1U/16V_4
C303 0.1U/16V_4
C590 0.1U/16V_4
C561 0.1U/16V_4
C573 0.1U/16V_4
C349 330U/2V_7343

VCC3

C178 2.2U/6.3V_6
C176 0.1U/16V_4

SMDDR_VTERM

C154 1U/6.3V_4
C187 1U/6.3V_4
C188 1U/6.3V_4
C156 1U/6.3V_4
C183 10U/6.3V_6
C184 10U/6.3V_6
C155 10U/6.3V_6

SPD SA0	0
SPD SA1	1

VCC3
R101 0 5% 1/16W 0402 SA0_B_0
R100 0 5% 1/16W 0402 SA1_B_0
B-11

AM3

SUYIN H:5.2 RVS Black

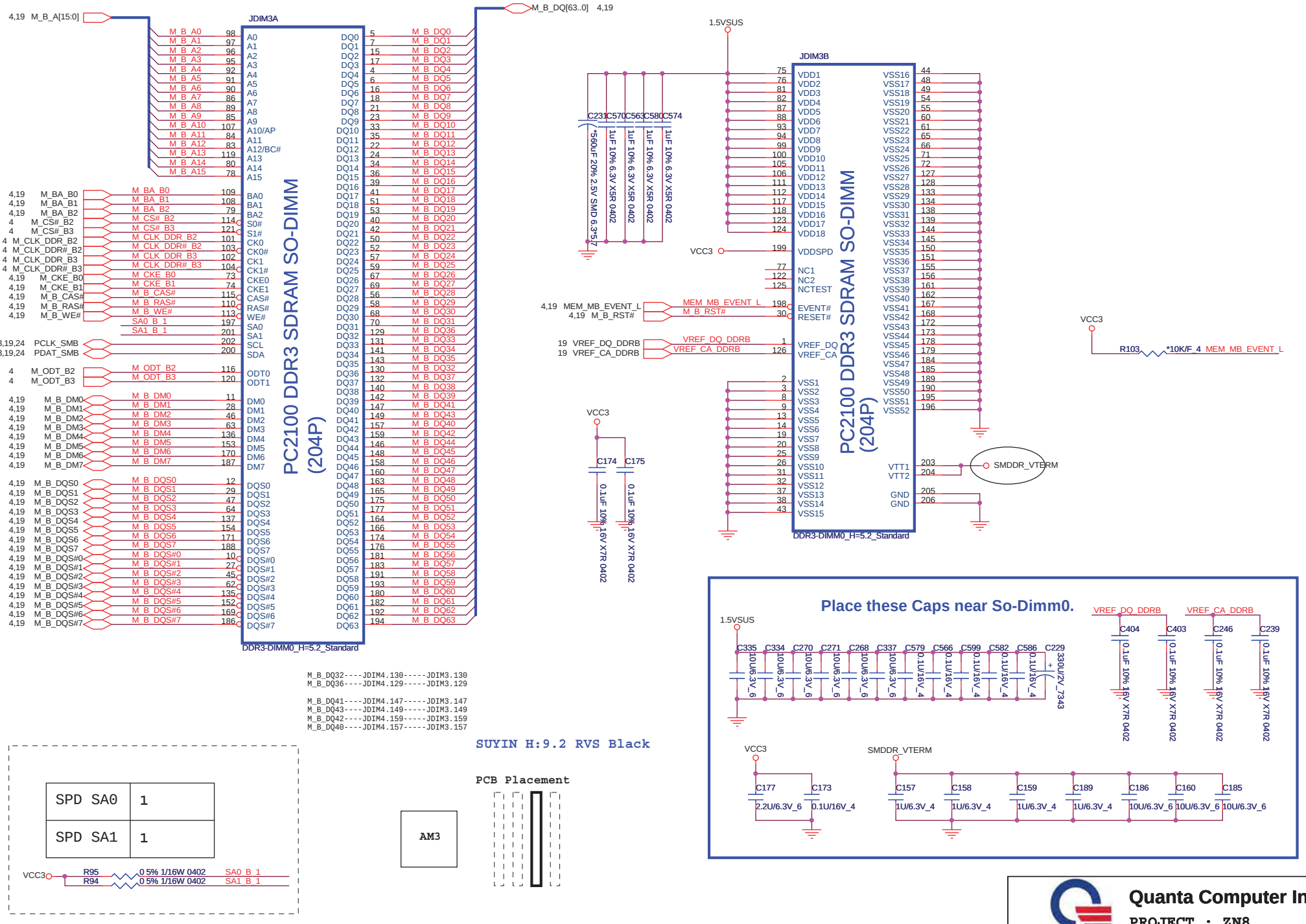
PCB Placement

Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	DDR3 CHB DIMM 0	1A
Date: Monday, March 22, 2010	Sheet 19 of 40	

CHANNEL B DIMM 1



M_B_DQ32----JDIM4.130-----JDIM3.130
M_B_DQ36----JDIM4.129-----JDIM3.129

M_B_DQ41----JDIM4.147-----JDIM3.147
M_B_DQ43----JDIM4.149-----JDIM3.149
M_B_DQ42----JDIM4.159-----JDIM3.159
M_B_DQ40----JDIM4.157-----JDIM3.157

SUYIN H:9.2 RVS Black

PCB Placement

AM3

SPD SA0	1
SPD SA1	1

VCC3 R95 0 5% 1/16W 0402 SA0_B_1
R94 0 5% 1/16W 0402 SA1_B_1

Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	DDR3 CHB DIMM1	1A
Date: Monday, March 22, 2010	Sheet 20 of 40	

MXM Module

6/25 Change CN22 pin define and footprint at C test.

VIN_MXM 7~20V

10Amp

2.5Amp

1Amp

7/28: add decoupling capacitors for AMD recommendation

CN17A

MXM3_2.0 CONNECTOR

MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	N/A	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A

dGPU_PRSNT#	Sku
Low	MXM
High	WO/ MXM

dGPU_PRSNT# 13,27,29

PEX_Swing adjust

CN17B

LVDS: Upper-CH, Lower-CH

Display Port: DP-A, DP-B, DP-C, DP-D

CRT

PWM

THERM

MXM3_2.0 CONNECTOR

Thermo SMBus

Q24 2N7002D

Q23 2N7002D

MXM VIN Power switch

10Amp

MXM 3V/5V Power switch

1Amp

2.5Amp

To low power status mode

1 : FULL POWER
0 : LOW POWER

To EC

For CRT Debug

MXM DP CONN for Scalar Board

DP_CON30

CON2

LVDS+DP CONN for MXM

87241-5001-50p-luv
LCD_50CN

CON4

Q8 TR M-FET-N 2N7002E 60V 0.25A

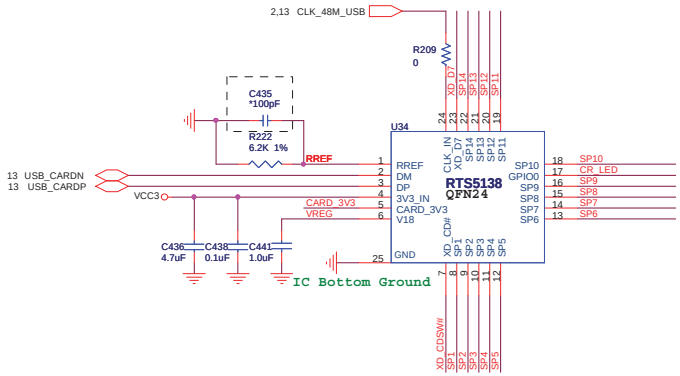
Q11 TR M-FET-N 2N7002E 60V 0.25A

Quanta Computer Inc.

PROJECT : ZN8

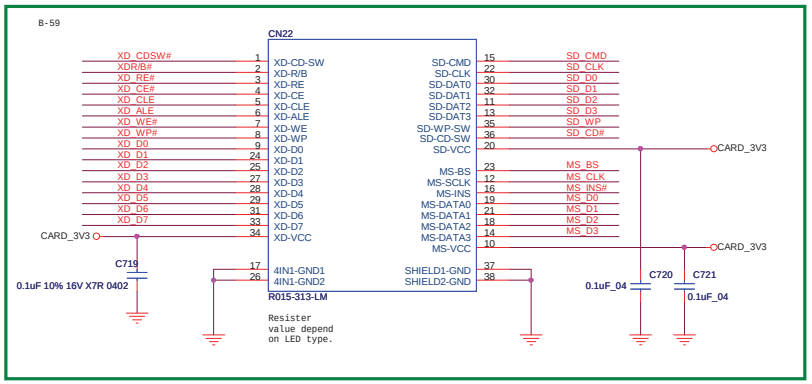
Size	Document Number	Rev
	MXM 3.0	1A

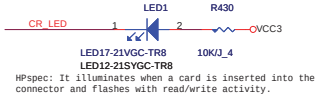
Date: Monday, March 22, 2010 Sheet 21 of 40

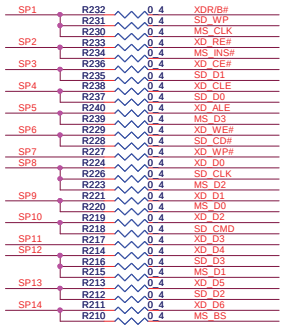


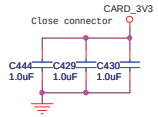
Share Pin

Share Pin	XD	MS	SD
SP1	XDR/B#	MS_CLK	SD_WP
SP2	XD_RE#	MS_INS#	
SP3	XD_CE#		SD_D1
SP4	XD_CLE	MS_D7	SD_D0
SP5	XD_ALE	MS_D3	SD_D7
SP6	XD_WE#		SD_CD#
SP7	XD_WP	MS_D6	SD_D6
SP8	XD_D0	MS_D2	SD_CLK
SP9	XD_D1	MS_D0	SD_D5
SP10	XD_D2		SD_CMD
SP11	XD_D3	MS_D4	SD_D4
SP12	XD_D4	MS_D1	SD_D3
SP13	XD_D5	MS_D5	SD_D2
SP14	XD_D6	MS_BS	









Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	RTS5138	1A

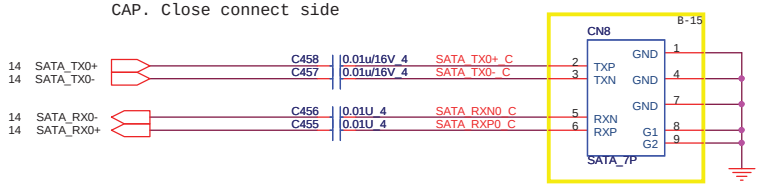
Date: Monday, March 22, 2010 Sheet 22 of 40

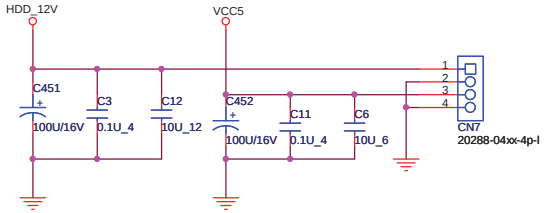
1st 2.5"/3/5" SATA HDD

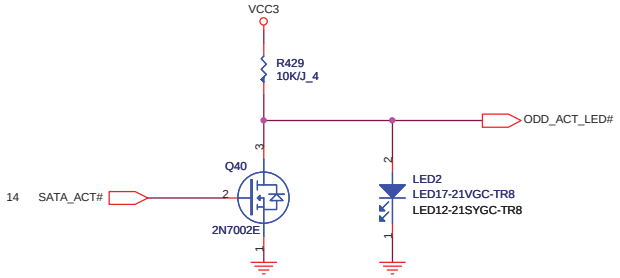
From PCH SATA

SATA HDD CONNECTOR

CAP. Close connect side





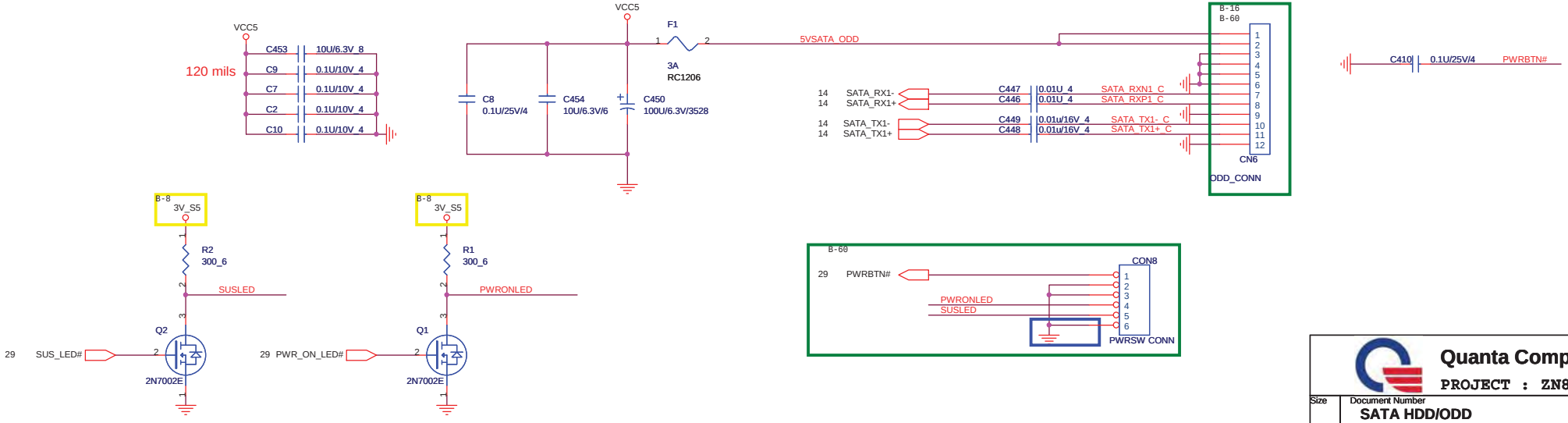


SATA CD-ROM

To SATA-HDD conn

SATA ODD CONNECTOR

USB connector same as ZN6



Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	SATA HDD/ODD	1A

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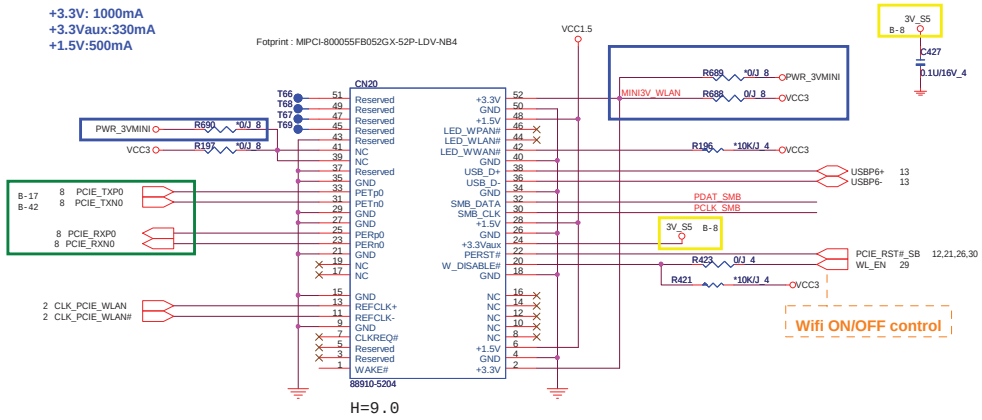
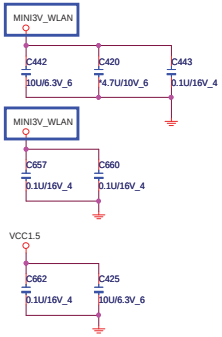
Wireless + BT

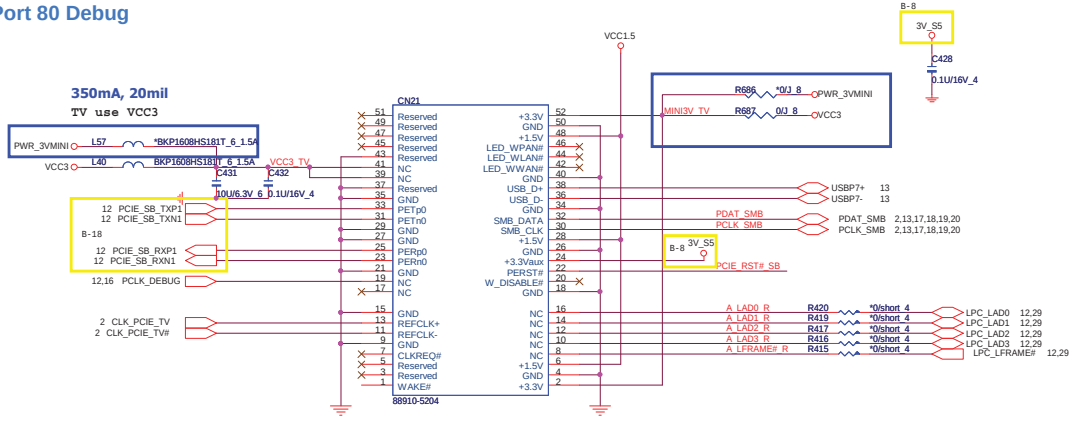
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

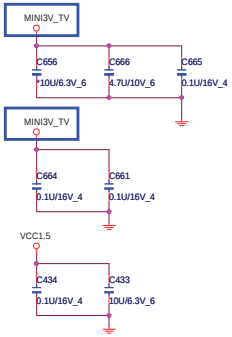




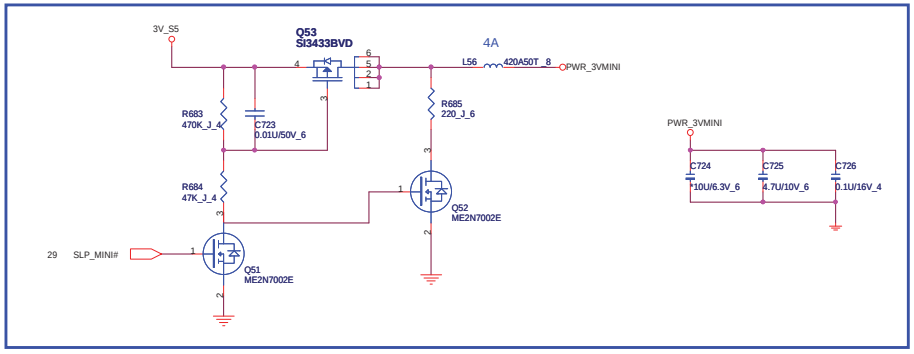
H=9.0

TV and Port 80 Debug





H=9.0



Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	MINI PCIE (WLAN/TV)	1A
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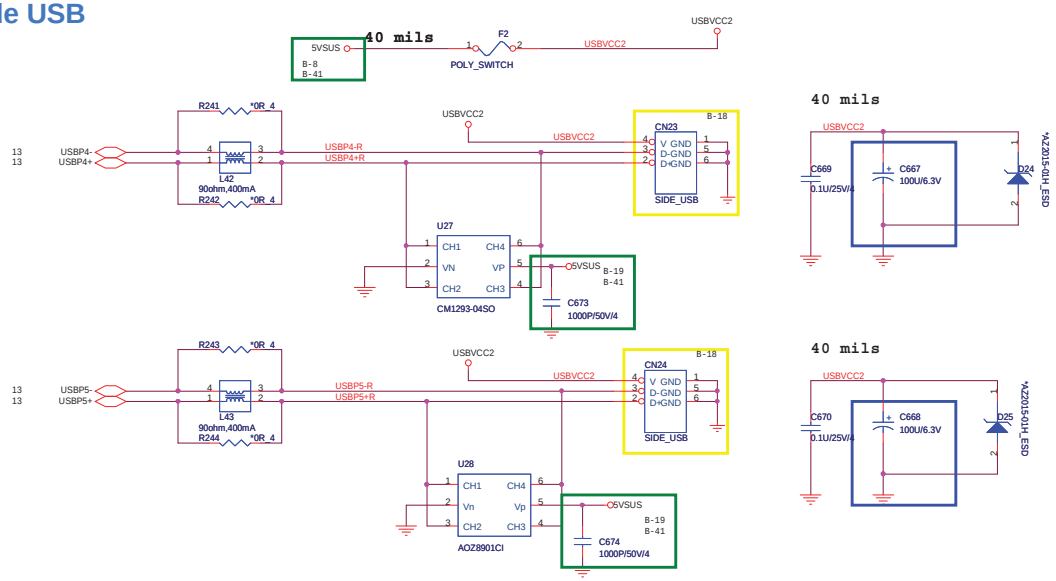
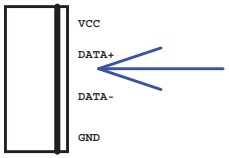
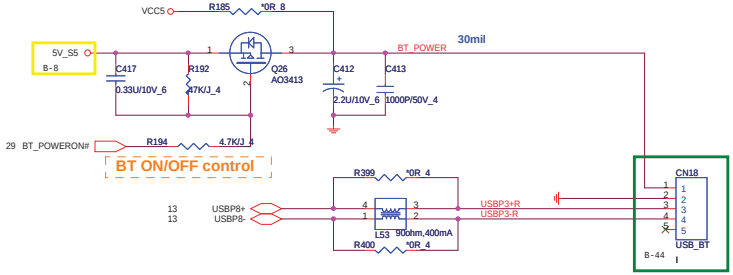
Side USB



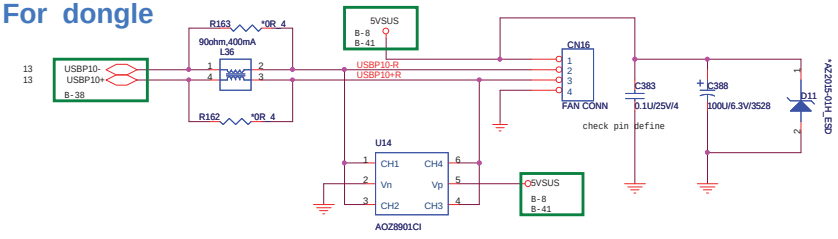


USB connector same as ZN6

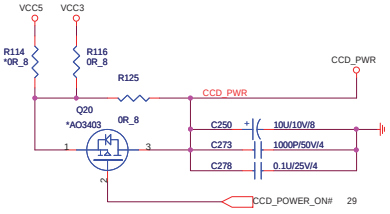
BLUETOOTH CONNECTOR



For dongle

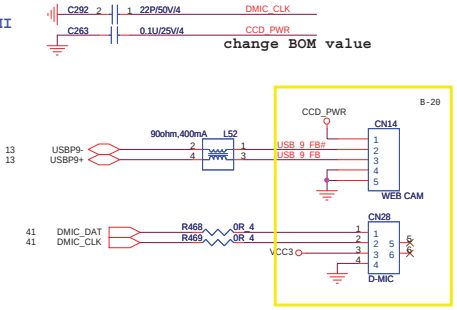


WEB CAM MODULE



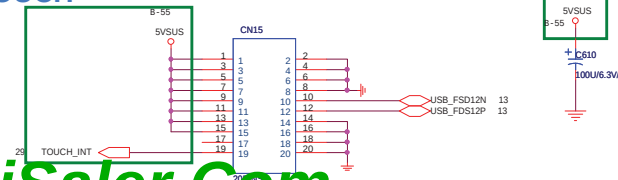
TO WEB CAM MODULE

FOR EMI



MULTI-TOUCH

HP spec:USB header for touch controller must be able to support 3.0 A.



Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	USB/CCD/BT/MT	1A

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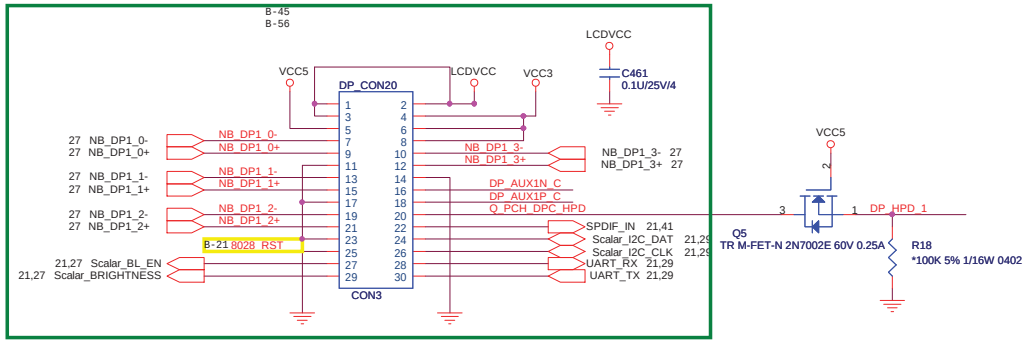
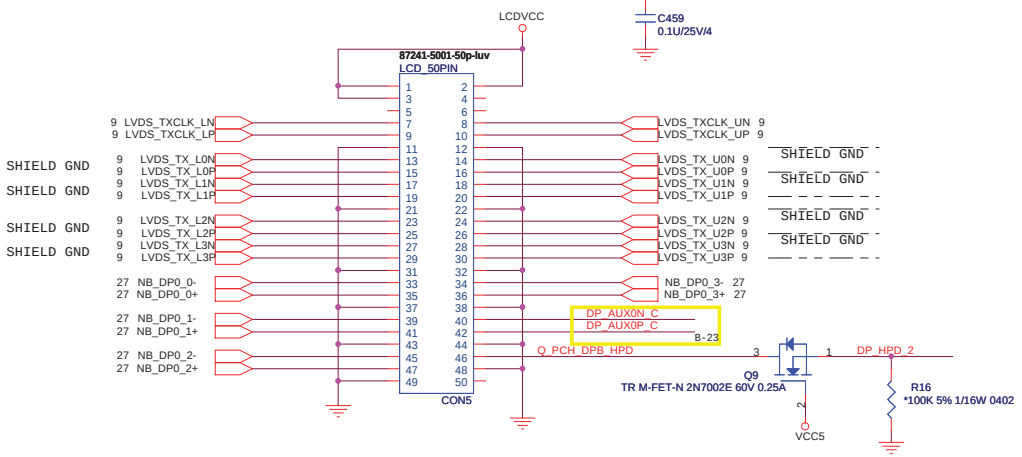
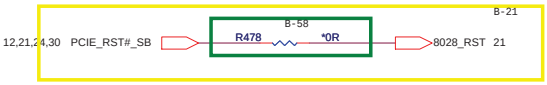
UMA DP CONN for scalar Board



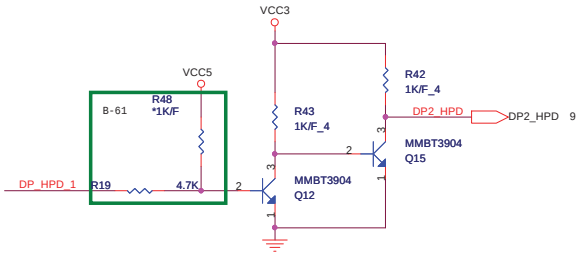
LVDS+DP CONN for UMA

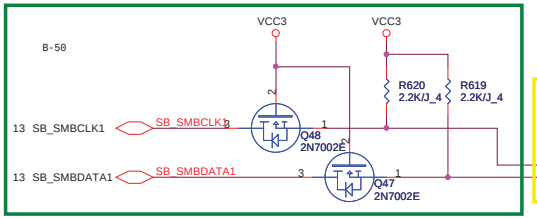


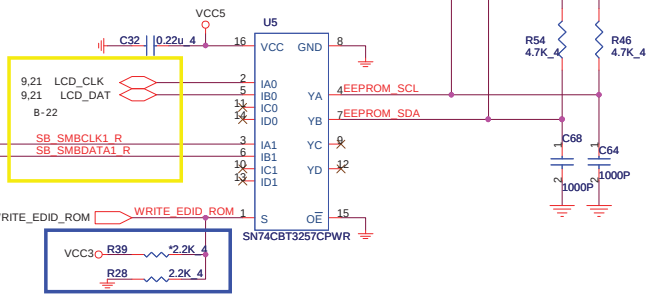


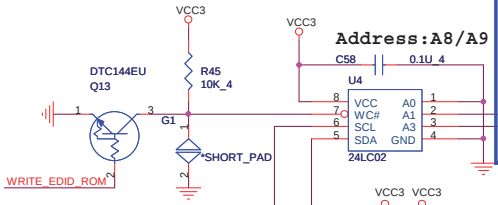
EEPROM IIC Selection

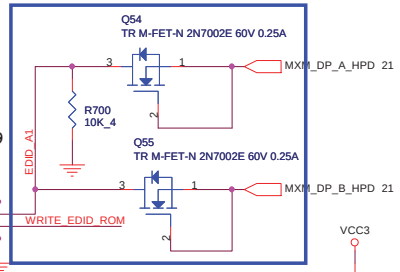
PANEL EDID DATA

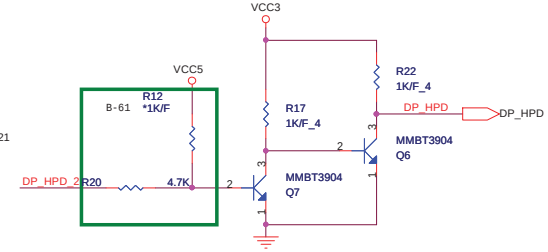


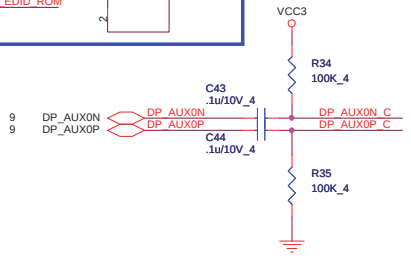


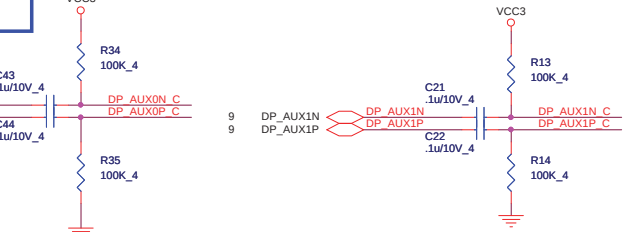


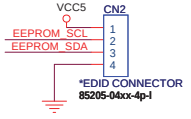


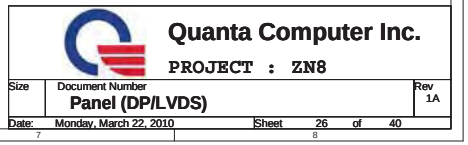




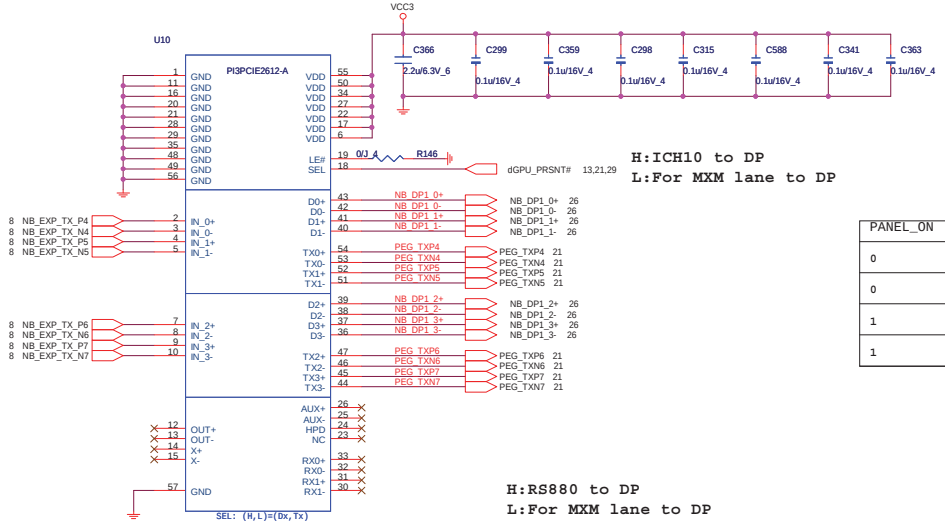


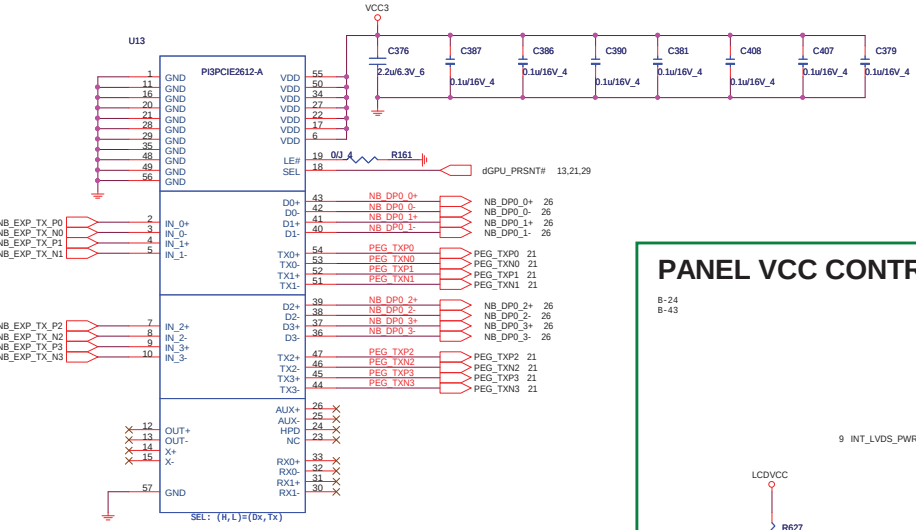




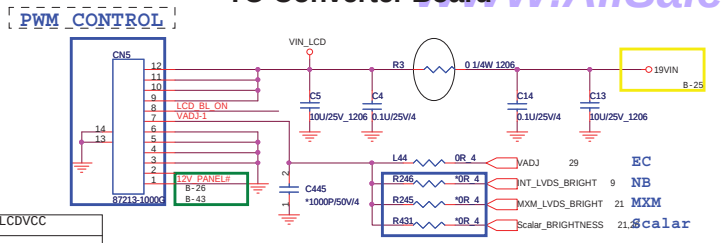


TO Converter Board

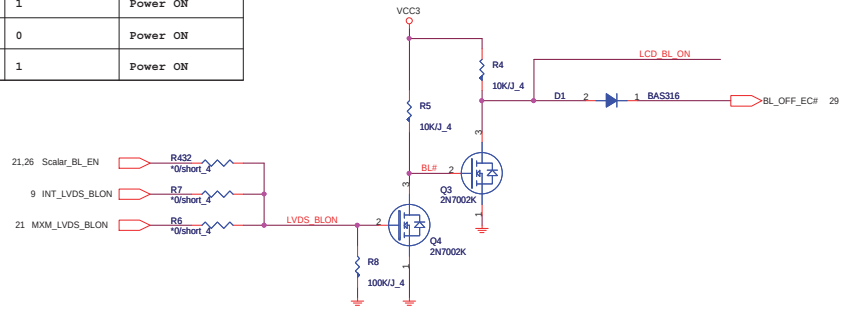


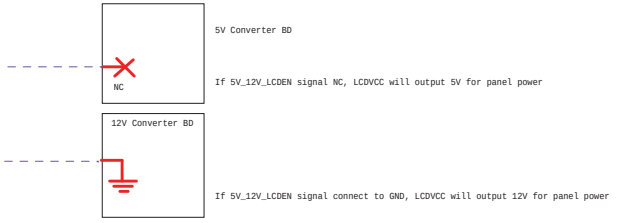


PWM_CONTROL



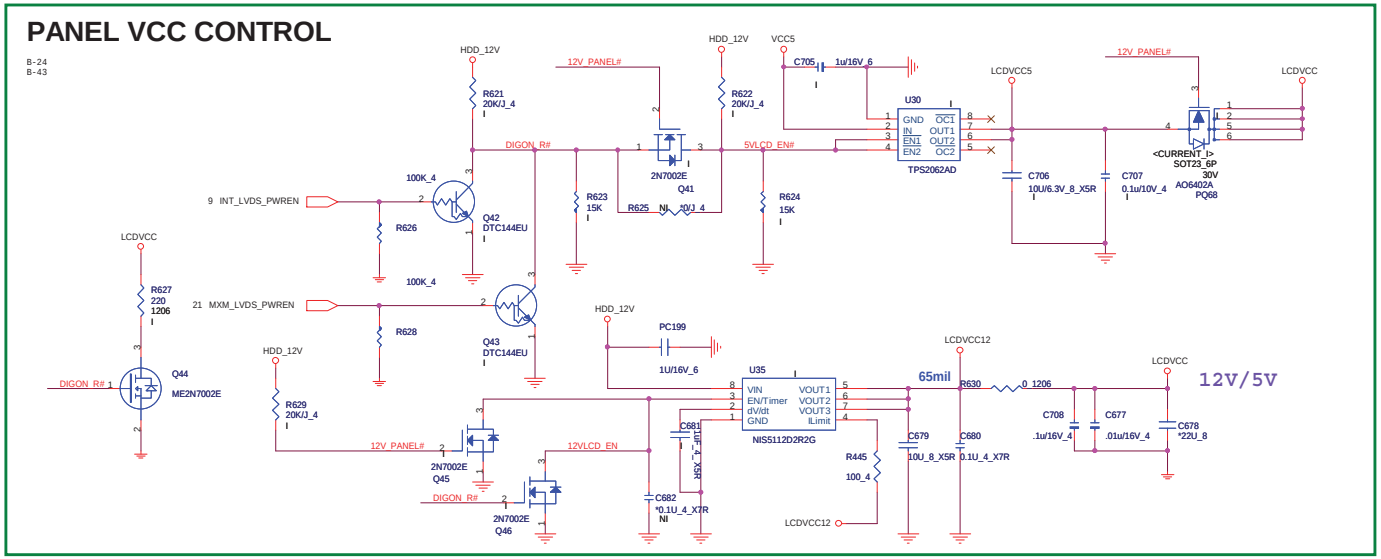
PANEL_ON	PANEL_ON_EC	LCDVCC
0	0	Power OFF
0	1	Power ON
1	0	Power ON
1	1	Power ON





Option 2
a.5V panel --- remove Q41,C675,R438,R441,D26
b.12V panel --- remove Q41,R442,D26
Option 4
remove R441,R442

PANEL VCC CONTROL



Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	Panel (Control)	1A
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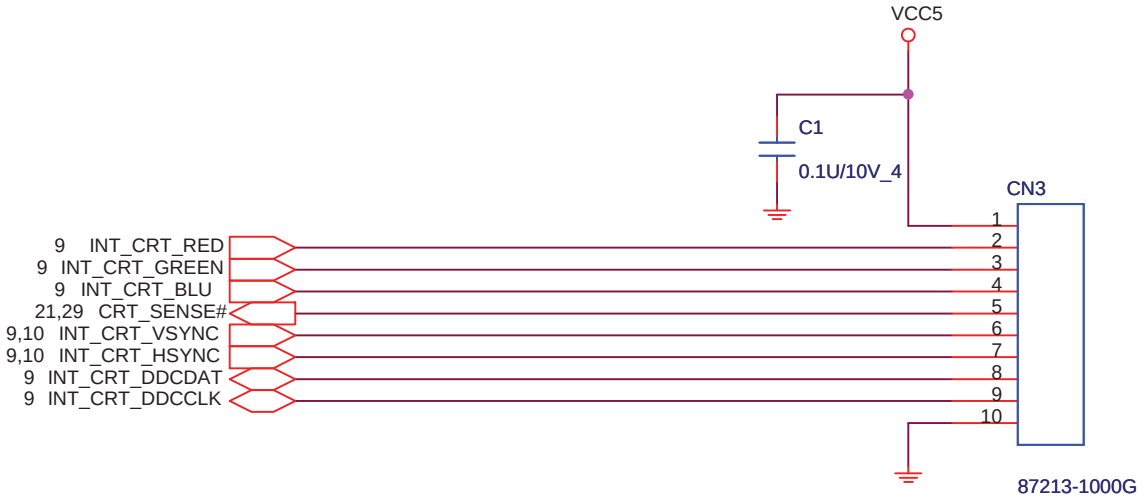
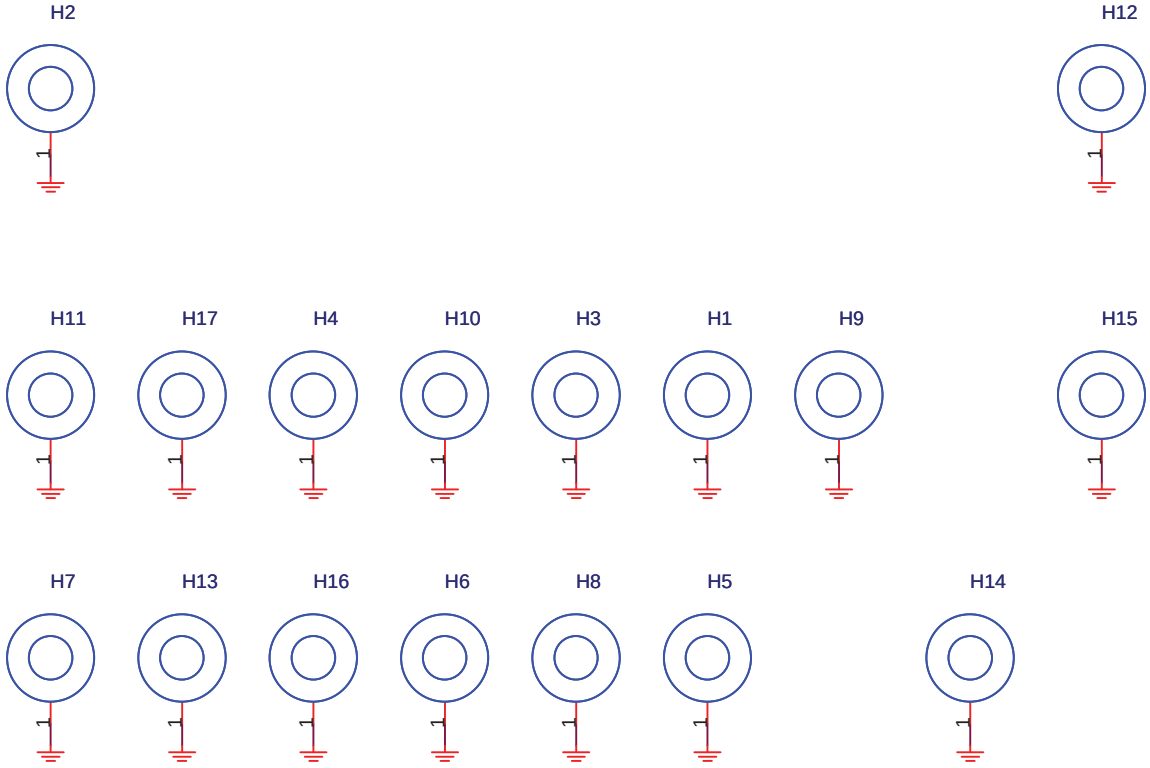
CRT for Debug





Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: CRT	Rev: 1A
Date: Monday, March 22, 2010	Sheet 28 of 40	

EC

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

(For PLL Power)

IT8512NX

LPC
GPIO
SM BUS
PS/2
For PS2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI Device
KBMX
A/D D/A
CLOCK
CIR

HWPG

8Mbit , SPI

Input only

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

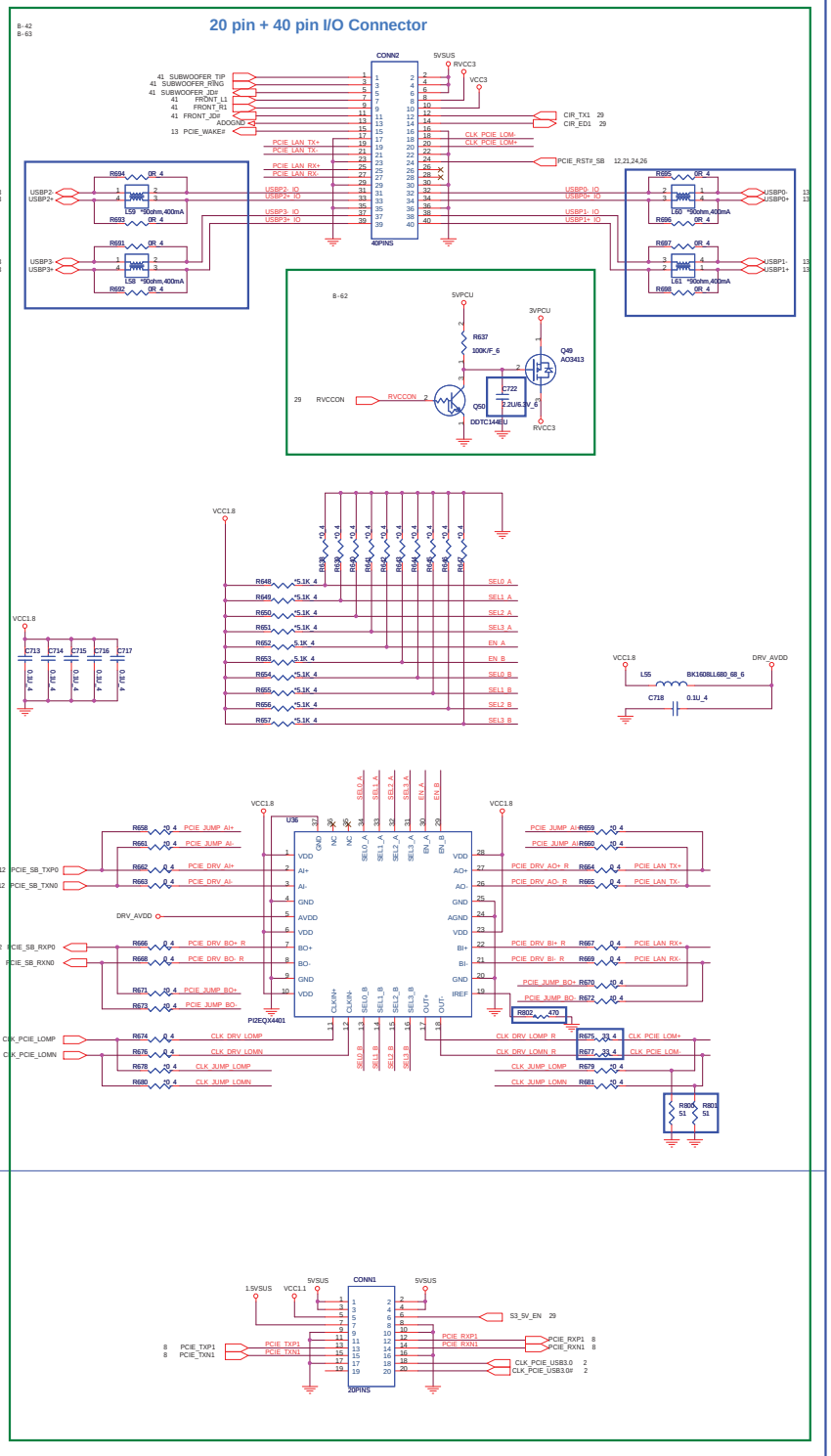
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

For Debug use

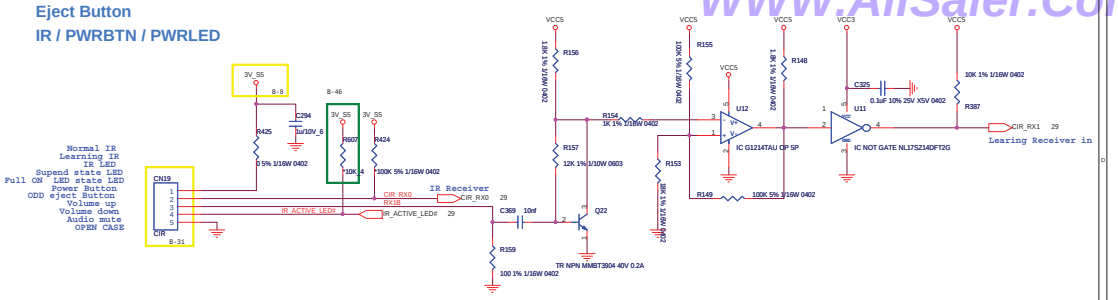
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	EC ITE 8512N/FLASH		1A
Date: Monday, March 22, 2010		Sheet 29 of 40	

20 pin + 40 pin I/O Connector

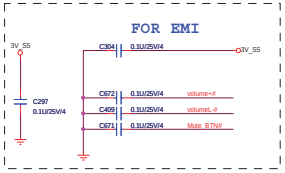


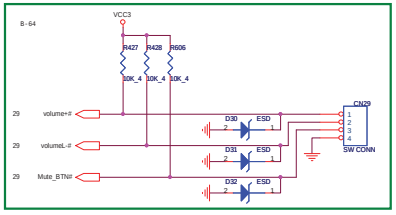
Eject Button
IR / PWRBTN / PWRLED



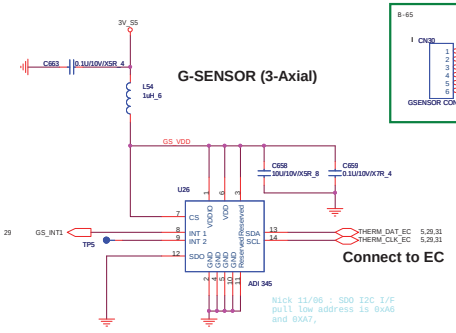
The aqua-white (470 +/- 5 nm) color is used to indicate the system is powered on and in the S0 state. The amber (590 +/- 5 nm) color is used to indicate the system is in one of the standby states (S3, S4, S5).

PWRBTN# must pull up to PCU power well



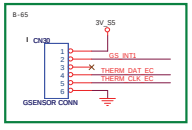


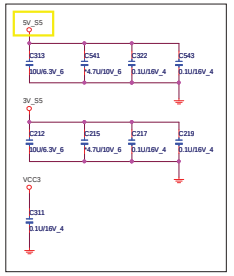
G-SENSOR (3-Axial)



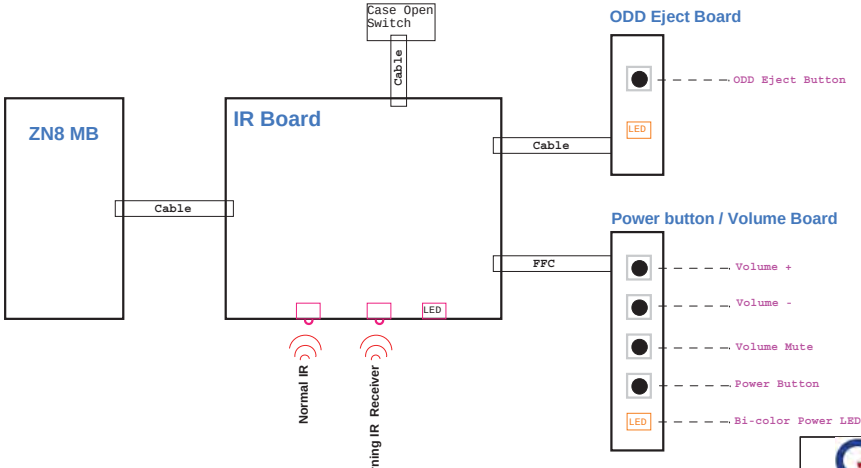
Connect to EC

Nick 11/06 : SDO I2C I/F pull low address is 0xA6 and 0XA7,



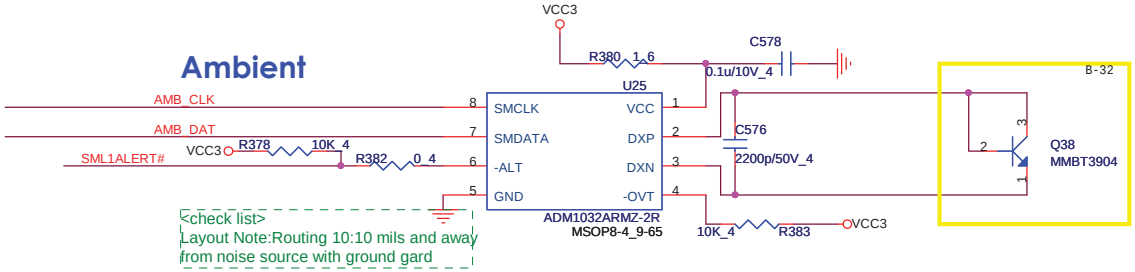


ZN8 MB / IR Board / ODD Eject Board / Power button / Volume Board

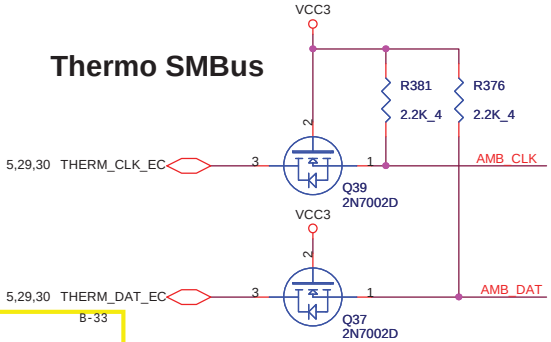


Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	I/O Board Connector		1A
Date: Tuesday, March 23, 2010		Sheet 30 of 40	

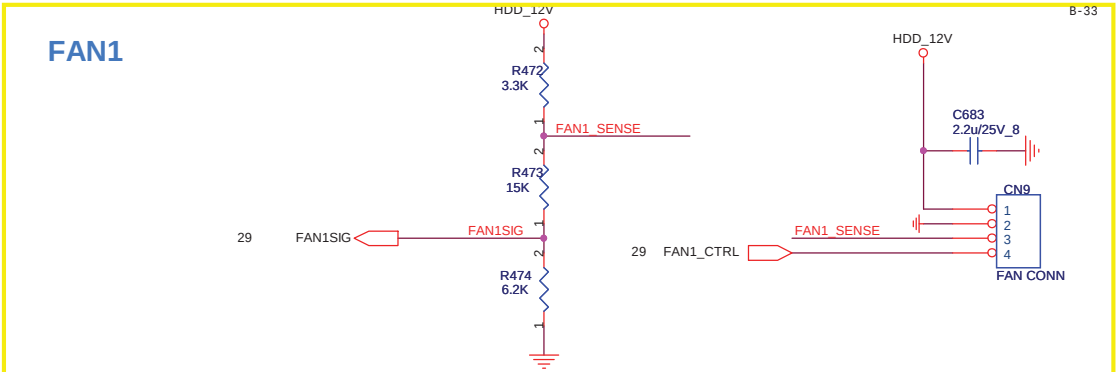
Ambient



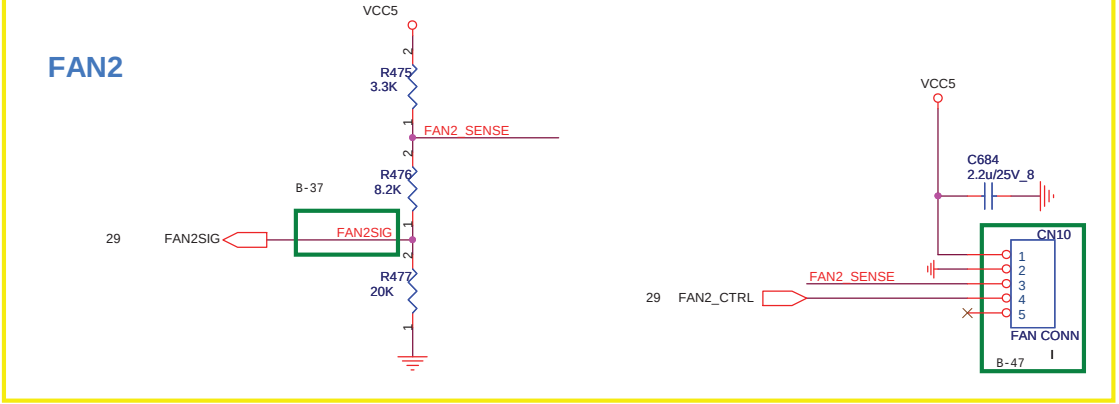
Thermo SMBus



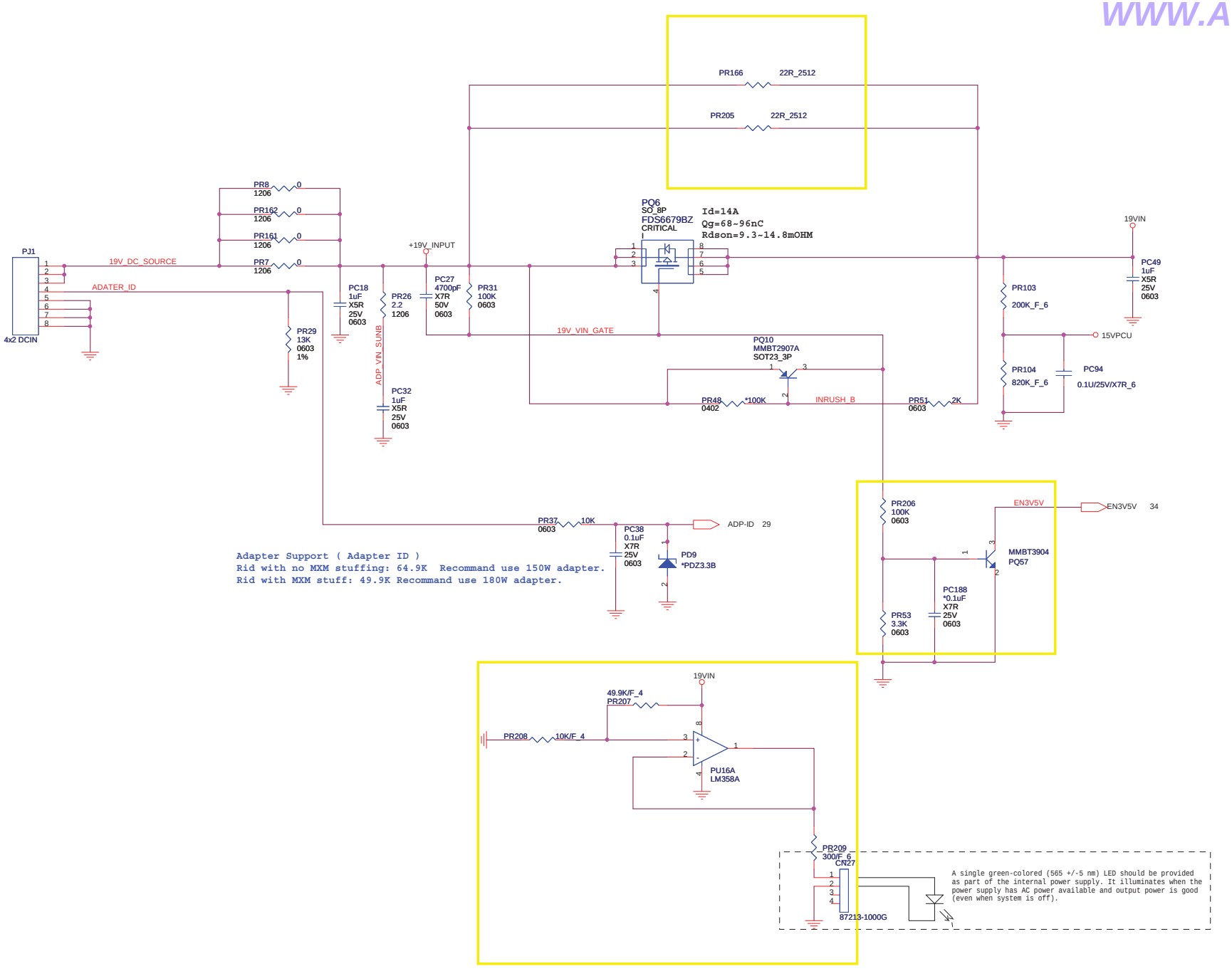
FAN1



FAN2



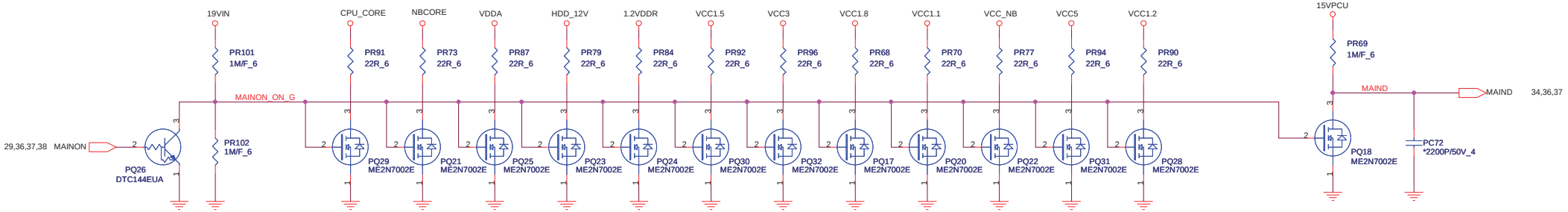
Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: FAN/Thermal Protection	Rev: 1A
Date: Monday, March 22, 2010	Sheet 31 of 40	

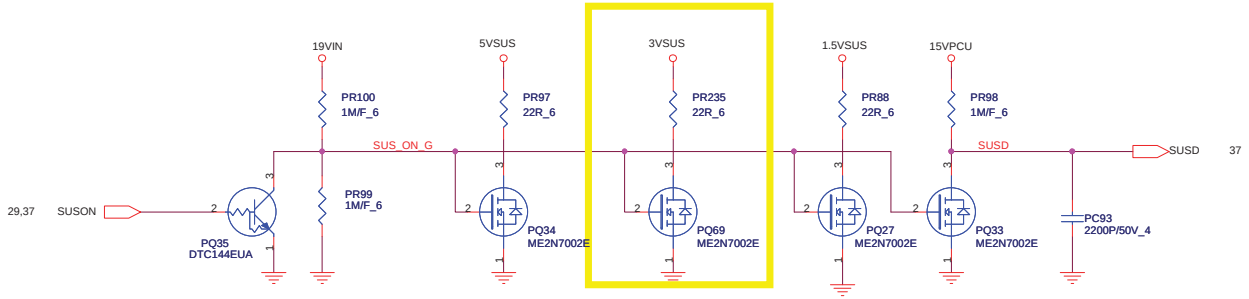


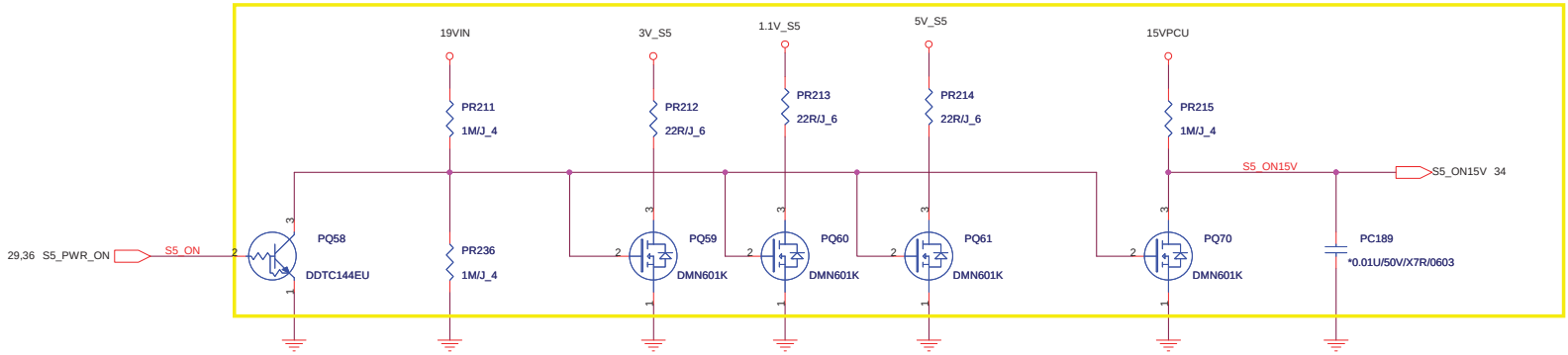
Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	ACIN	1A
Date: Monday, March 22, 2010	Sheet 32 of 43	







Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	DISCHG & MOS SW	1A

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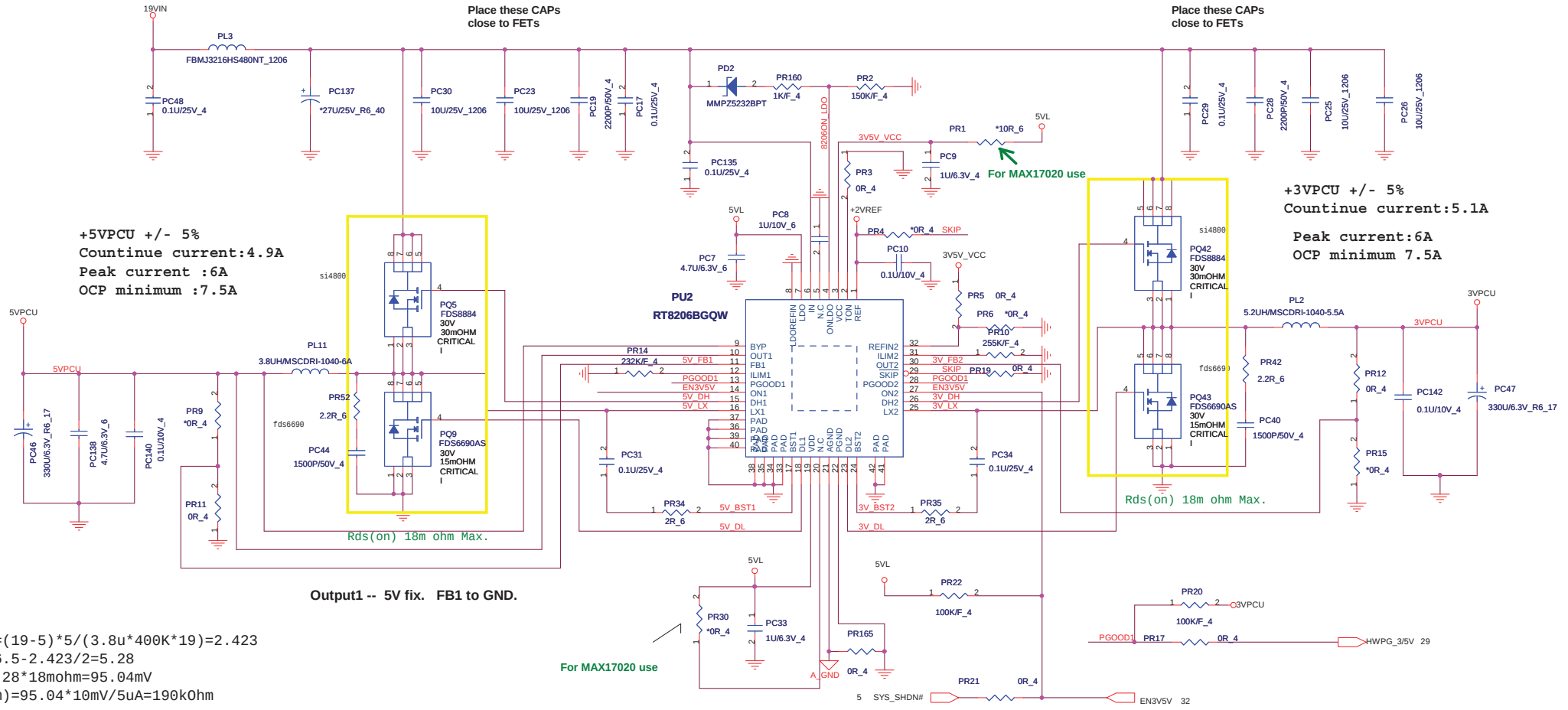
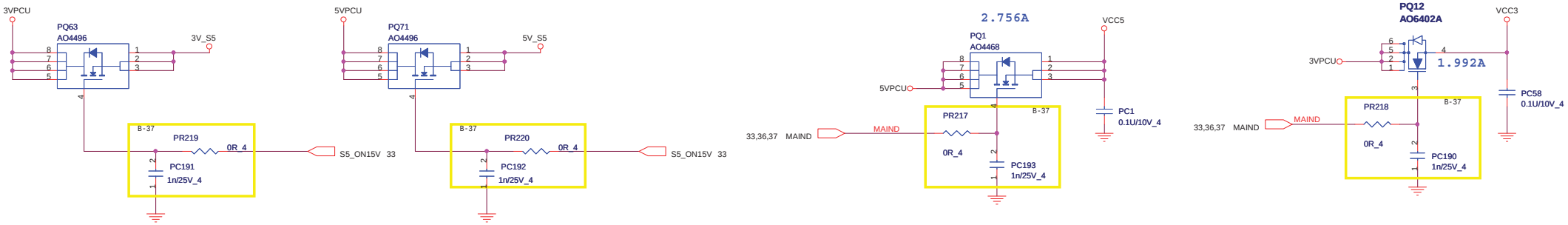
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



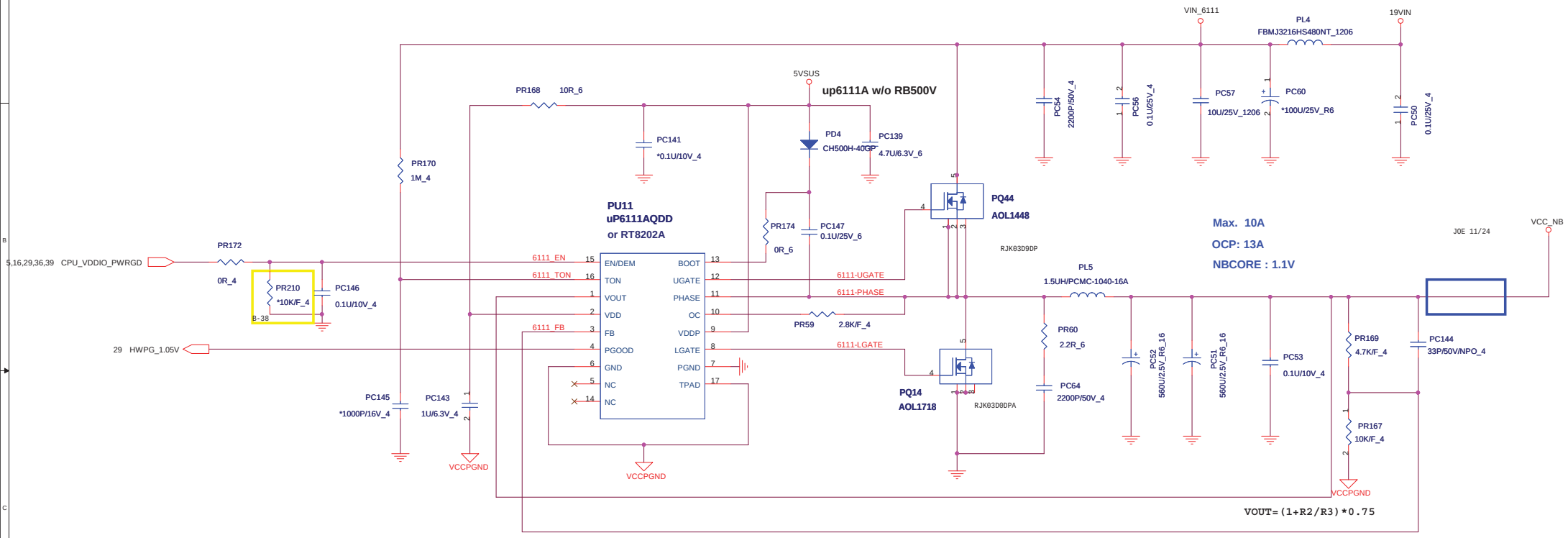
del I=(19-5)*5/(3.8u*400K*19)=2.423
Iocp=6.5-2.423/2=5.28
Vth=5.28*18mohm=95.04mV
R(Ilim)=95.04*10mV/5uA=190kOhm



Design common circuit for ,
RT8206B or Max17020 or TPS51427

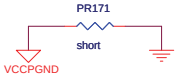
Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	+5V/+3V (RT8206B)	1A
Date: Monday, March 22, 2010	Sheet 34 of 43	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)



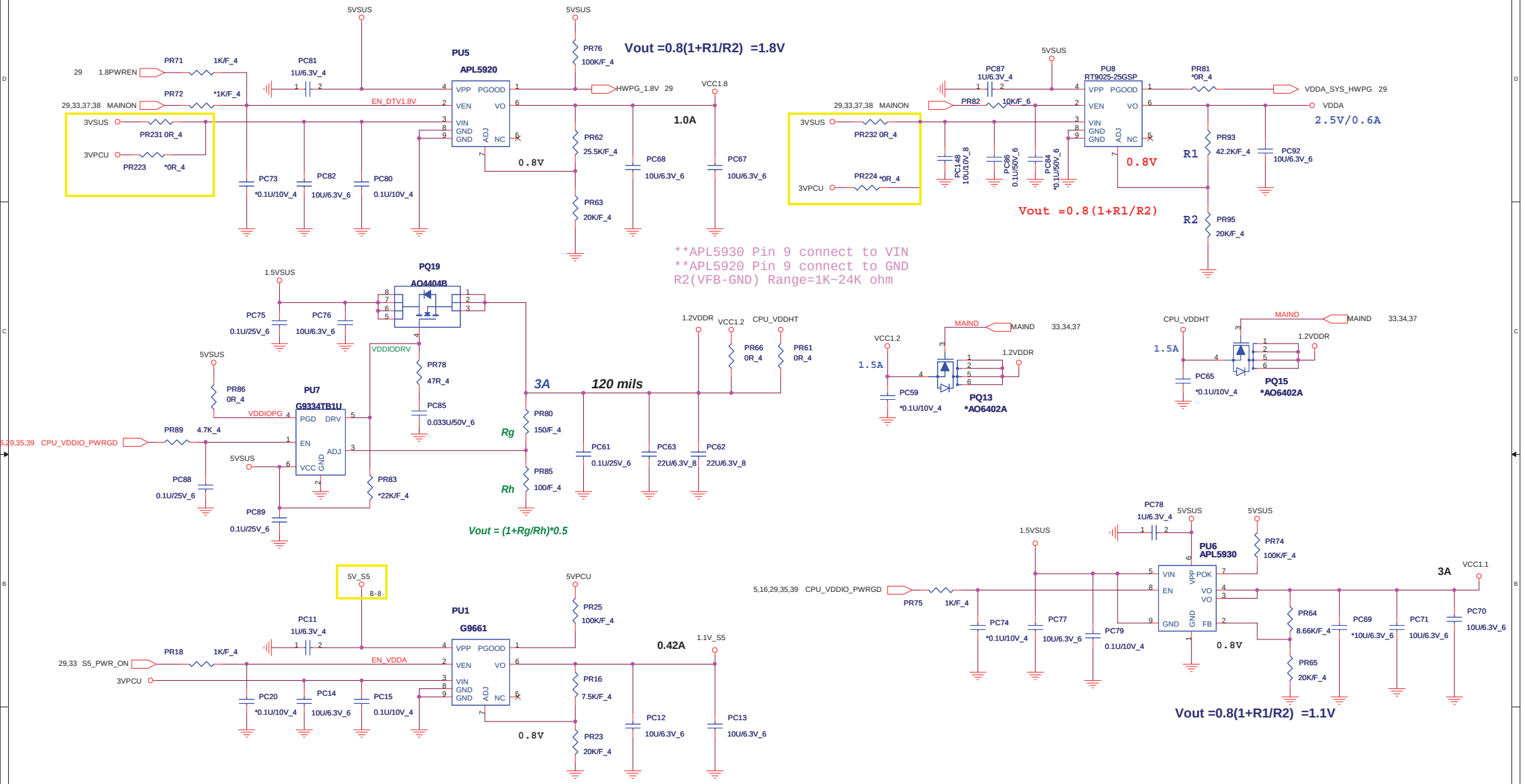
AO4712 Rds=4.3m Ohm Max./4.5V

Rds * OCP = RILIM * 20uA

13A OCP --- R_OC = 2.8K

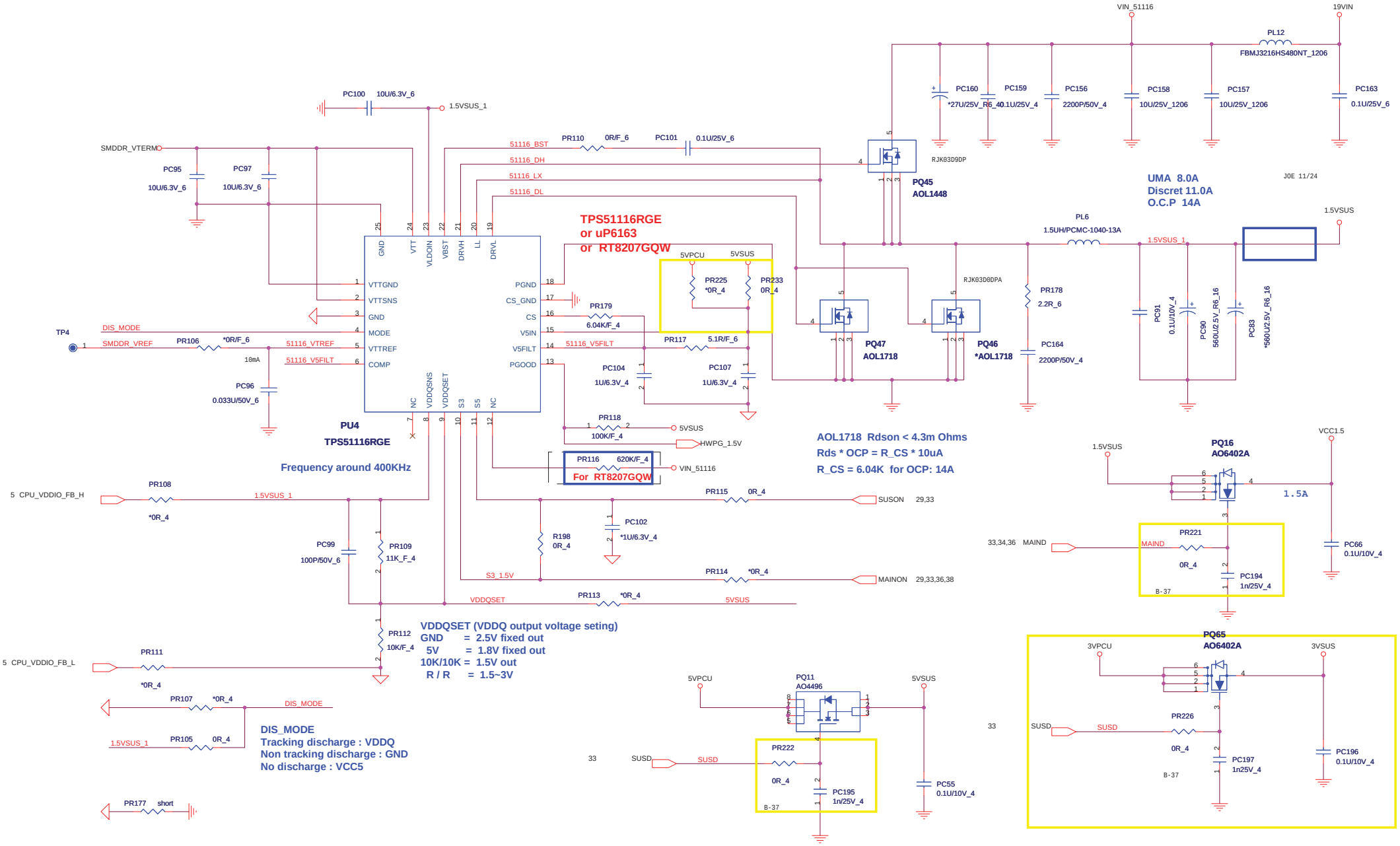
Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: NBCORE_1.1V(uP6111)	Rev: 1A
Date: Monday, March 22, 2010	Sheet 35 of 43	

VCC1.1V, 1.2VDDR, VCC1.8V,VDDA,1.1V_S5

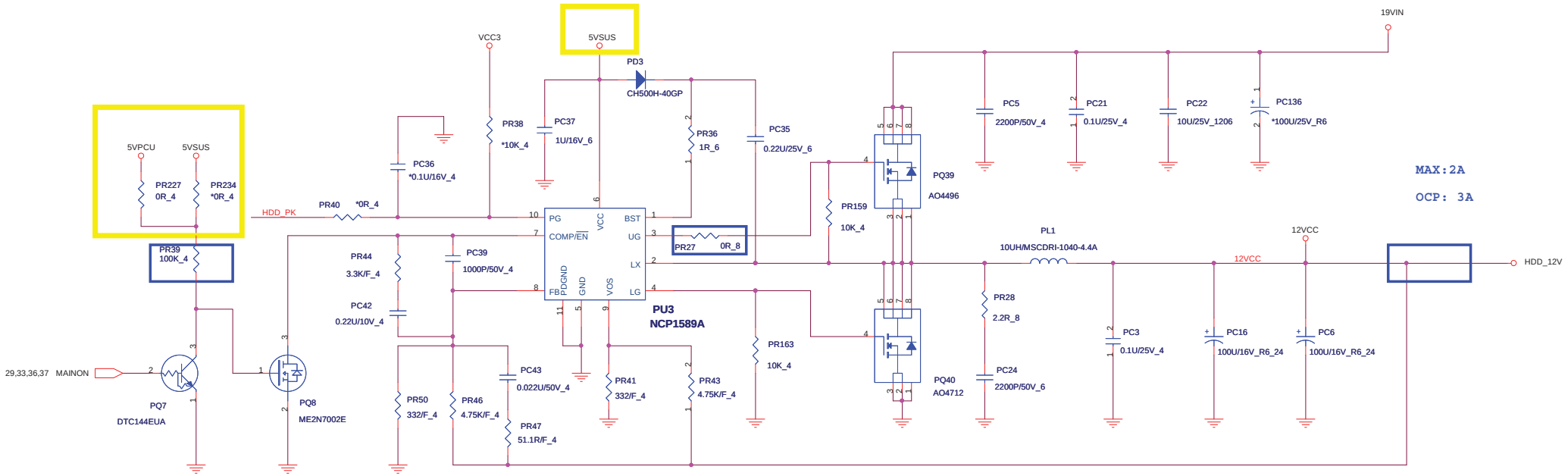


Quanta Computer Inc.			
PROJECT : ZN8			
Size	Document Number		Rev
	VCC1.1,VDD1.8,2.5V(LDO)		1A
Date: Monday, March 22, 2010	Sheet 36 of 43		

DDRIII-- 1.5VSUS

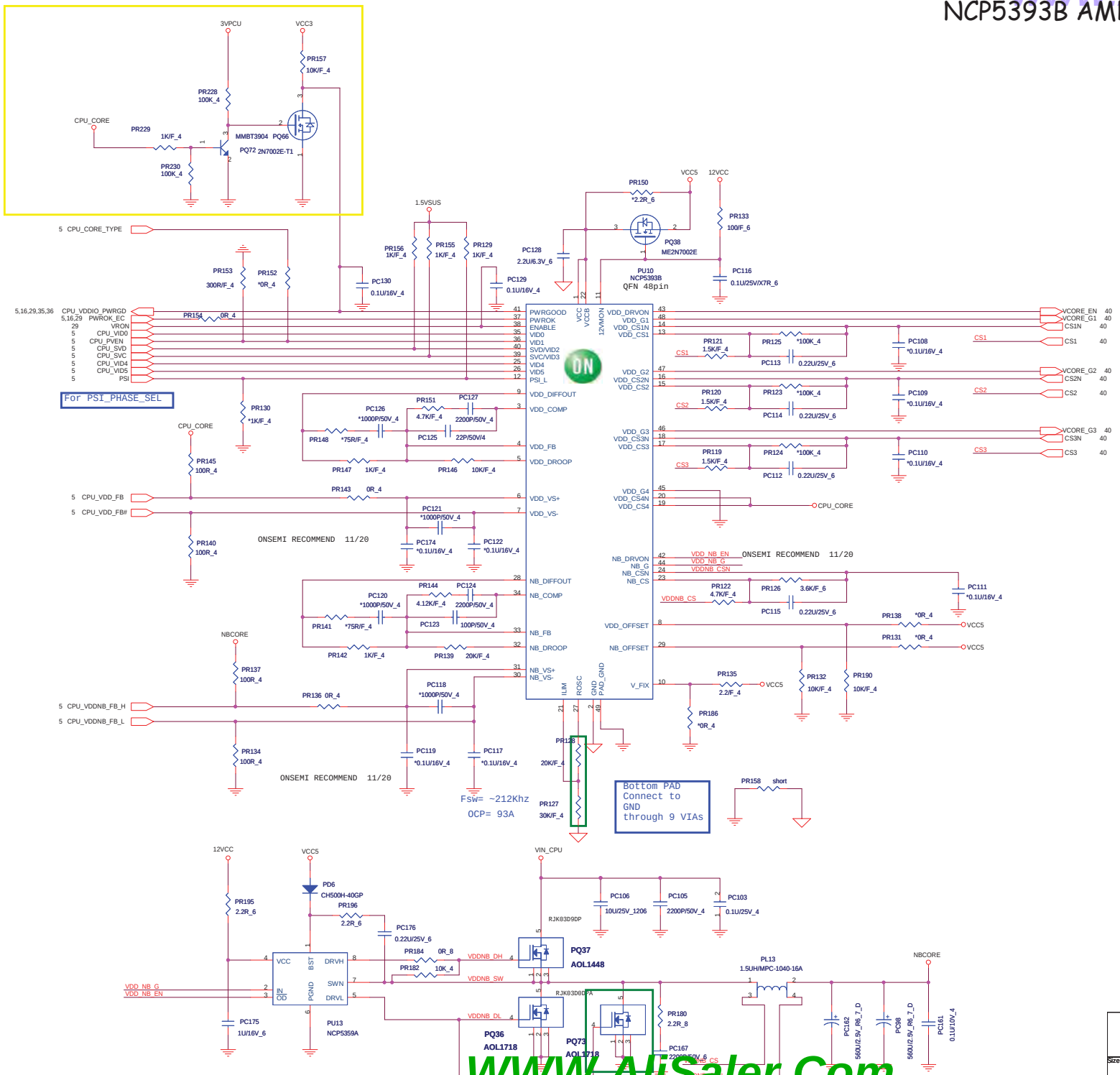


Quanta Computer Inc.	
PROJECT : ZN8	
Size	Document Number: DDR(TPS51116) — Rev: 1A
Date: Tuesday, March 23, 2010	Sheet 37 of 43



Quanta Computer Inc.		
PROJECT : ZN8		
Size	Document Number: HDD12V	Rev: 1A
Date: Monday, March 22, 2010	Sheet 38 of 43	

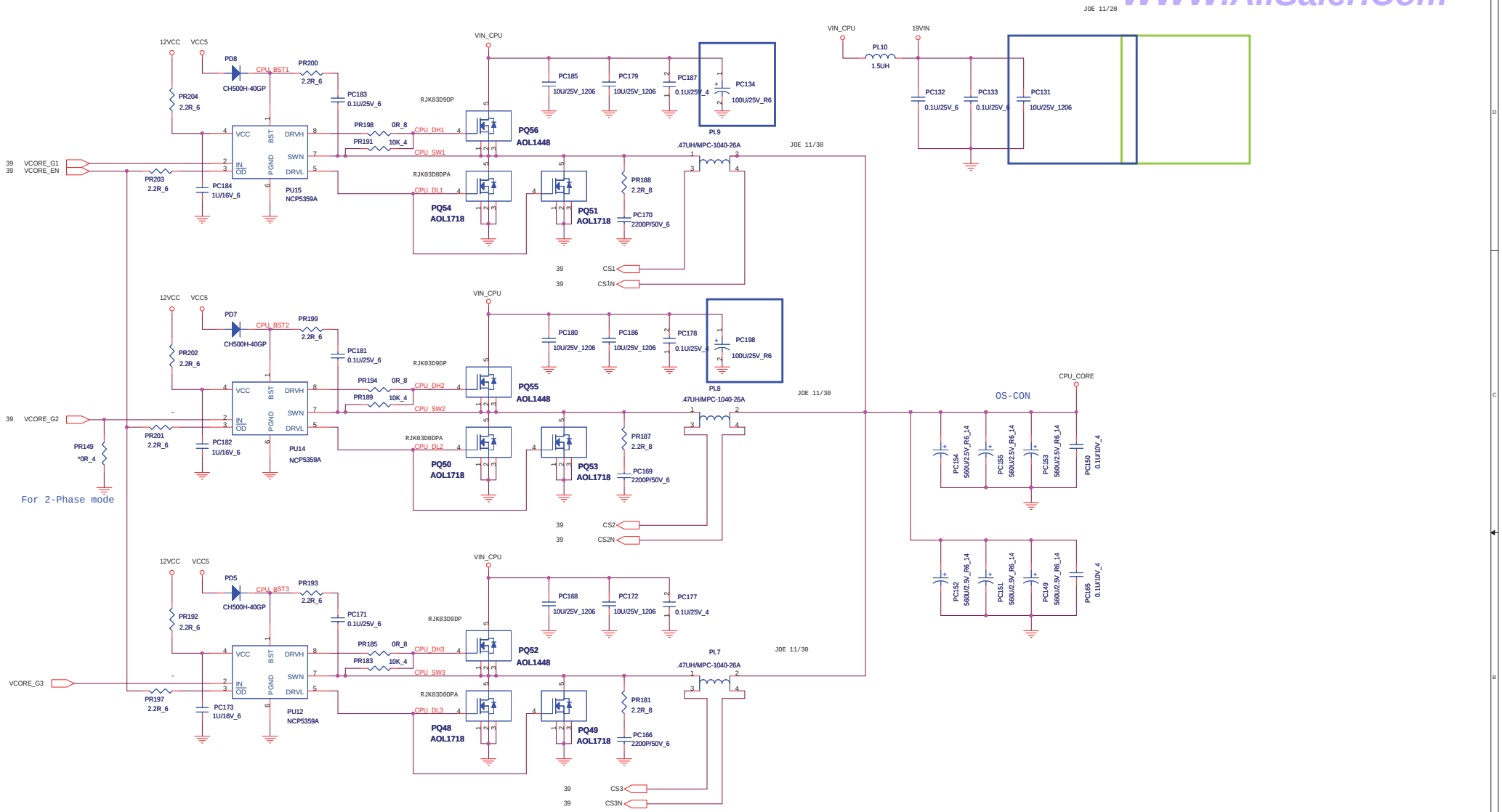
NCP5393B AMD AM3 POWER CKT



Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	AMD AM3 CPUCORE(NCP5293)	1A
Date: Monday, March 22, 2010	Sheet 39 of 43	



Quanta Computer Inc.
PROJECT : ZN8

Size	Document Number	Rev
	CPU DRIVER	1A
Date: Monday, March 22, 2010	Sheet 40 of 43	

CODEC

Near sense pin

12/8 AC90/AC93 change to 0ohms by IDT demanded

2/3 AC17/AC19 from 1u to 10u solved the THD issue.

2/3 AC20/AC21 from 1u to 100u solved the THD issue.

AC19/AC21 place near AU7 Pin9

2/3 AC14/AC16/AC18 from 1u to 10u solved the THD issue.

2/3 AC22/AC23 from 1u to 100u solved the THD issue.

AC92/AC23 place near AU7 Pin1,3

12/8. AR59 need move close to the MIC by IDT demanded

12/8 resistors change to null by IDT demanded

Please next to Codec

VOUT = 1.25 (1+R1/R2)

R1	R2
4.8375V	28.7K
	10K

2nd source : G923-330T1U

AL000923003

12/8. AU3 current too small, when use we need to find other by IDT demanded

AC17 should near AU2

AC12 should near AU1

Place near AU4

11/30. change net name HPL and HPR to HPL1 and HPR1

11/25 cancel BAT54C*2 by IDT demanded

11/25 add filter by IDT demanded

2/3 change 22ohm to 16ohm for meet 2Vrms output.

11/25 value change from 100P to 0.01u by IDT demanded

LINE IN/Mic Reserved Jack

Normal Close

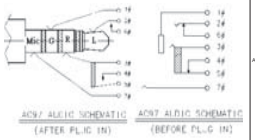
HeadPhone/Mic Combo Jack

Normal Close

MUTE

Check

BUZZER



Quanta Computer Inc.

PROJECT : ZN8

Size: | Document Number: HD Audio Codec(92HD89D3) | Rev: A

Date: Monday, March 22, 2010 | Sheet 41 of 43

AUDIO AMPLIFIER

41 AMP_MUTE#

AC60 1000p/50V_4

41 LINE2-L1 — AC62 .033u/16V_4 — AR47 76.8K/F_4 — LINE2-L1SPK+

12/22 Add AR70/AR71 near the CODEC by ADI demanded

AR70 short — AC31 .033u/16V_4 — AR25 76.8K/F_4 — LINE2-L1SPK-

AR71 short — AC30 .033u/16V_4 — AR24 76.8K/F_4 — LINE2-L2SPK-

41 LINE2-L1 — AC61 .033u/16V_4 — AR46 76.8K/F_4 — LINE2-L2SPK+

AU5 SSM2306CPZ

INL+ SD OUTL- OUTL+ EP GND

INL- VDD

NC VDD

NC GND

INR- INR+ N.C. OUTR- OUTR+

5VSPK1

AC59 0.1u/10V_4 AC54 10u/6.3V_6 AC3 0.1u/10V_4 AC2 10u/6.3V_6

AL1 220ohm,2A 100 mil 5VPCU

L1SPK- AL13 220ohm,2A L1_SPK-

AC58 1000p/50V_4 AC53 100p/50V_NPO_4

L1SPK+ AL12 220ohm,2A L1_SPK+

AC57 1000p/50V_4 AC52 100p/50V_NPO_4

L2SPK+ AL11 220ohm,2A L2_SPK+

AC56 1000p/50V_4 AC51 100p/50V_NPO_4

L2SPK- AL10 220ohm,2A L2_SPK-

AC55 1000p/50V_4 AC50 100p/50V_NPO_4

2/3 ME change from 4 to 5pin.

CON6 INT_SPK_R

2W X 4

AR1 *0R 0603 1%

AC1 10V *0.1uF NL X5R 0402

Analog_ground digital_ground

Please next to CON6

41 AMP_MUTE#

AC73 1000p/50V_4

41 LINE2-R1 — AC75 .033u/16V_4 — AR48 76.8K/F_4 — LINE2-R1SPK+

12/22 Add AR72/AR73 near the CODEC by ADI demanded

AR72 short — AC29 .033u/16V_4 — AR23 76.8K/F_4 — LINE2-R1SPK-

AR73 short — AC28 .033u/16V_4 — AR22 76.8K/F_4 — LINE2-R2SPK-

41 LINE2-R1 — AC74 .033u/16V_4 — AR49 76.8K/F_4 — LINE2-R2SPK+

AU6 SSM2306CPZ

INL+ SD OUTL- OUTL+ EP GND

INL- VDD

NC VDD

NC GND

INR- INR+ N.C. OUTR- OUTR+

5VSPK2

AC72 0.1u/10V_4 AC67 10u/6.3V_6 AC6 0.1u/10V_4 AC5 10u/6.3V_6

AL2 220ohm,2A 100 mil 5VPCU

R1SPK- AL17 220ohm,2A R1_SPK-

AC71 1000p/50V_4 AC66 100p/50V_NPO_4

R1SPK+ AL16 220ohm,2A R1_SPK+

AC70 1000p/50V_4 AC65 100p/50V_NPO_4

R2SPK+ AL15 220ohm,2A R2_SPK+

AC69 1000p/50V_4 AC64 100p/50V_NPO_4

R2SPK- AL14 220ohm,2A R2_SPK-

AC68 1000p/50V_4 AC63 100p/50V_NPO_4

CON7 INT_SPK_L

AR3 *0R 0603 1%

AC7 10V *0.1uF NL X5R 0402

Analog_ground digital_ground

Please next to CON7

Quanta Computer Inc.

PROJECT : ZN8

Size	Document Number	Rev
	AMP (SSM2306)	1A
Date: Monday, March 22, 2010	Sheet 42 of 43	

B-1 : CLK source change to CLK GEN from SB
B-2 : Change resistor footprint type
B-3 : Remove resistor for CLK GEN source
B-4 : Linking for EDID read
B-5 : For LAN and USB3.0 PCIE signal
B-6 : For EDID writing control
B-7 : Change CLK source from SB to CLK GEN
B-8 : Separate system S5 power from 3VPCU
B-9 : Mount R80 and D5 for ROM control
B-10 : Change SB strap setting
B-11 : Correct DIMM setting
B-12 : Linking for EDID read
B-13 : Correct 19V power rail net name
B-14 : Correct CLK_MINI_CK connection
B-15 : Change LPC connector type
B-16 : Change ODD connector type
B-17 : Change mini PCIE controller form NB to SB
B-18 : Change mini PCIE controller form NB to SB
B-19 : Add cpapacitor for noise filtration
B-20 : Separate DMIC and camera connector
B-21 : Correct scalar board reset signal
B-22 : Modify panel EDID read / write function
B-23 : Modify display port AUX channel connection
B-24 : Add panel power 12V/5V switch function
B-25 : Correct 19V power rail net name
B-26 : Panel power 12V/5V power selection
B-27 : Link HP amp I2C to EC for GAIN control
B-28 : PWM driving for FAN control
B-29 : CPU_CORE PWRD assertion for EC
B-30 : Adjust I/O port pin define
B-31 : Change CIR connector type
B-32 : Correct DIMM thermal detect function
B-33 : Modify FAN circuit for 12V FAN
B-34: CLK_SRCRCP_P0 / CLK_SRCRCN_P0 link to CLK GEN SRCRC_CLK_R / SRCRC_CLK#_R
B-35: Change R373,R375 to 150 ohm from 4.7K
B-36: De-pop R313,R289
B-37: Fix FAN net name issue
B-38: Fix USB overcle issue
B-39: Change ODD SB from prot 0 to port C
B-40: Fix VBAT issue
B-41:Change USB power to 5VSUS
B-42: Change PCIEx1 Lane to fix Lan issue
B-43: Modified Panel power circuit
B-44: Change CN15(BT) from 4pin to 5pin
B-45: Change CON2, CON3 pin definition
B-46: Reserve PU Res. for IR con pin4.
B-47: Change FAN2(CN16) from 4pin to 5pin
B-48: Connector PCIE_WAKE to IO_BD for WOL
B-49: Remove CN11 Logo_light# circuit
B-50: Change U5 SMBUS from main to resume
B-51: De-pop R356,R359
B-52: Change D6 to D28,D29
B-53: Add ICH_RSMRST# RC delay circuit
B-54: Reserve SB_SPI for debug
B-55: Change MT touch power to 5VSUS
B-56: Change scalar BD conn. power.
B-57: Disable SB EC strap
B-58: De-pop R478 to fix scalar BD reset issue
B-59: Change carder connector type(CN22)
B-60: isolate power btn from CN6 to CON8
B-61: Change R19,R20 to 4.7K and de-pop R12,R48 for MPD issue
B-62: Add RVCC3 power control circuit
B-63: Add re-driver IC for PCIE LAN and USB3.0
B-64: Add CN23 for vol+/vol-/mute function
B-65: Add CN19 for E-SECUTY
B-66: Add NB_PWRGD control circuit for spike issue

PAGE 32

1.del DCIN1 · PR176 · PR175 · PR173 · PR24 · PQ4 · PQ2 · PR32 · PR24 · PR49 · PD1 · PC41 · PR33 · PR164 · CR1 · PR13 · PQ41 · PQ3 · PR55 · PR56 · PC45 · PR54 · PR45 · PR57 · PC4 · PC2

2 - ADD PR206/100kohm · PC188/0.1uF · PQ57/MMBT3904 · PR207/49.9kohm · PR37/10kohm · PU16A/LM358 · PR166/22ohm · PD9/PDZ3.3B · PR209/300ohm

3 - change PR29 FROM 64.9k ohm TO 13kohm

PAGE 35

1 - change PR172 FROM 1k ohm TO 0 ohm

2 - ADD PR7/10kohm · PC51/560uF/2.5V

PAGE 36

1 - change PU8 VEN FROM CPU_VDDIO_PWRGD TO MAINON

PAGE 37

1 - change VCC1.5V TO VCC1.5

2 - add pq65, pr226,pc197,pc196 for 3vsus

PAGE 39

1 - change PU10 PWRGOOD FROM CPU_CORE TO VCC3

2 - add mosfet in VDDNB

3 - add pr229,pr230,pr228,pr157,pq67,p166 for pwrgood

Quanta Computer Inc.
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