UMA (11.6")

Intel Brasswell-M Platform Block Diagram

+3VS5/+5VS5 PG.29

MOIC PG.31

CPU Core PG.32,33

DDR3L PG.30

Charger PG.28

DDR3L Memory down*4pcs PG.14 — 1600MT/s Channel A

DDR3L Memory down*4pcs PG.15 — 1600MT/s Channel B

Intel Brasswell L

Power : 4.5 (Watt)

Package : BGA1170

Size : 25 X 27 (mm)

PG.2~13

eDP (2 lane) → EDP panel PG.18

DP Port0 → HDMI PG.18

eMMC 4.51 → eMMC 32G/64G

USB 3.0 → USB3.0 Ports X1 PG.23

USB 2.0 → USB2.0 Ports X1 PG.23

PCI-E x2 → Card Reader RTS5239-GR PG.17

PCI-E x2 → WLAN BT COMBO NGFF M2 PG.24

USB 2.0 → WLAN BT COMBO NGFF M2 PG.24

USB 2.0 → Webcam PG.18

USB 2.0 → WWAN NGFF M2 PG.20

LPC → KBC IT8987 PG.25 → KB PG.21, TP PG.21, ROM PG.5

Fast SPI

Azalia → AUDIO CODEC ALC 3227 PG.19

Without amp for eMMC sku

Hp → Headphone amplifier HPA022642RTJR Daughter board → Combo Jack Daughter board

MIC

Speaker PG.19

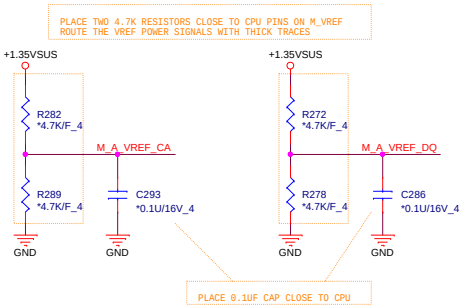
NB5

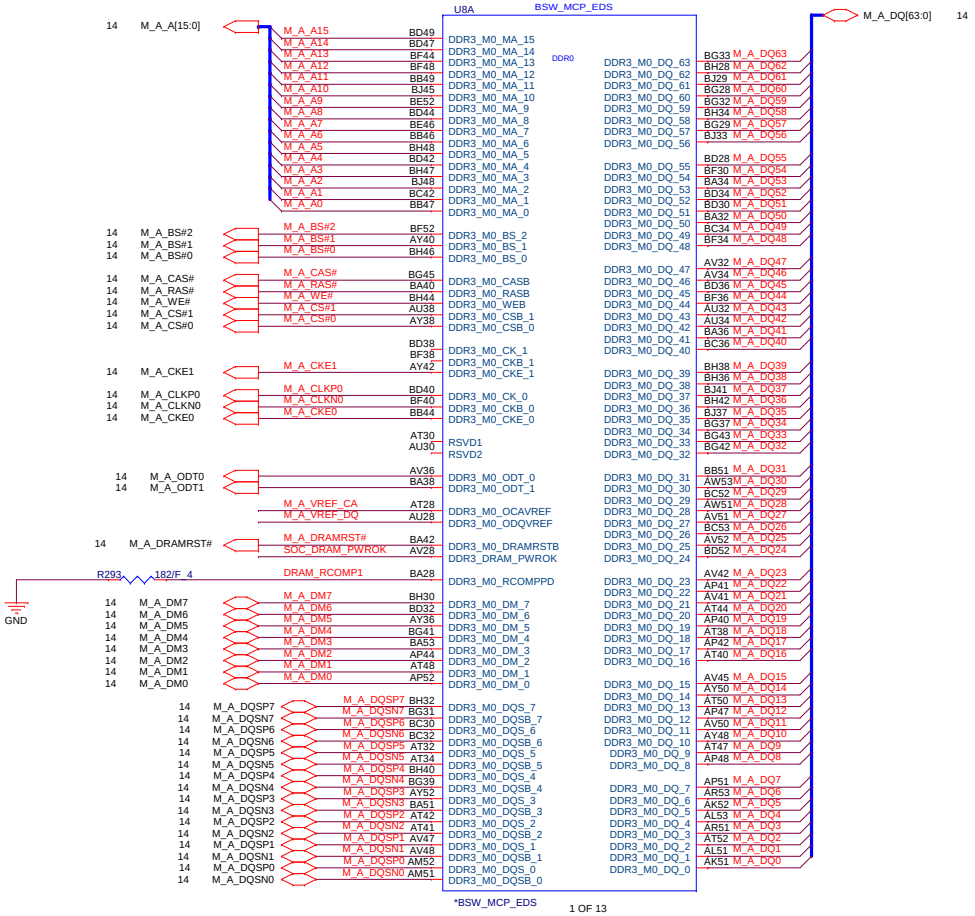
PROJECT : Y0H

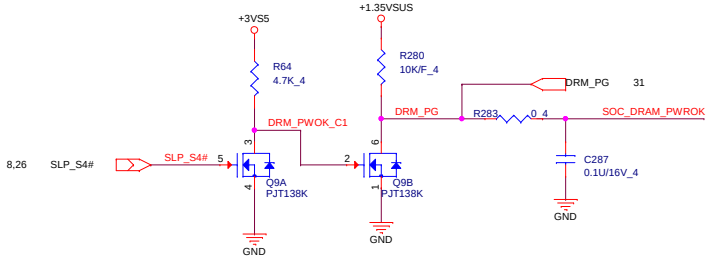
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

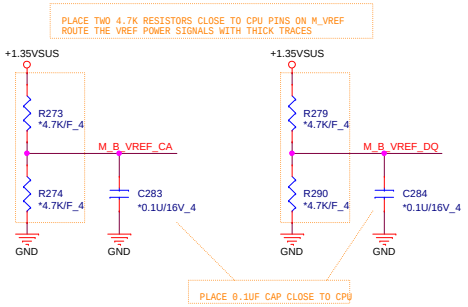
Date: Monday, July 06, 2015 Sheet 1 of 38

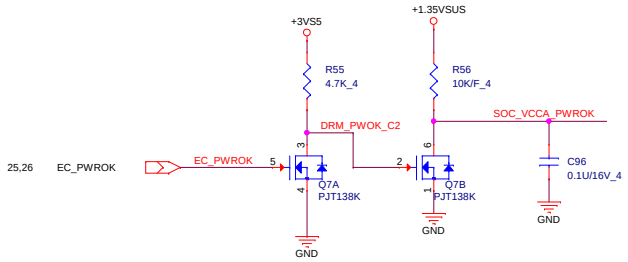


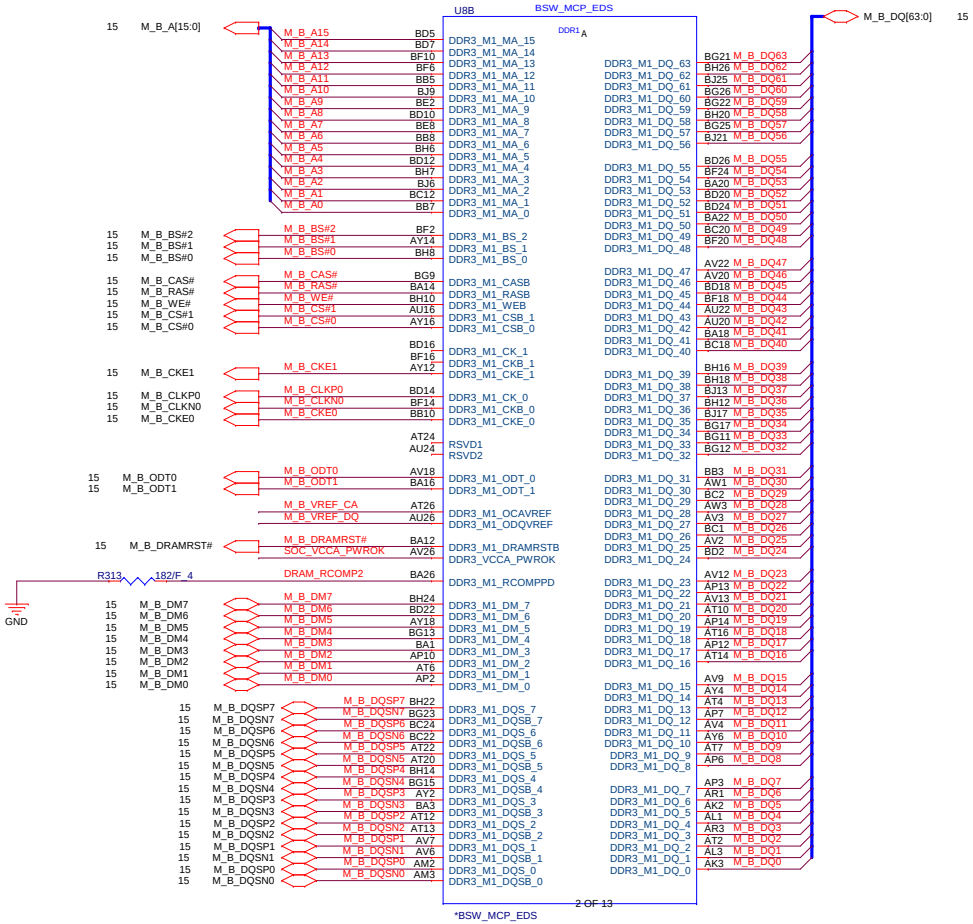




NB5	PROJECT : Y0H Quanta Computer Inc.		
	Size	Document Number Valley 1/9 (DDRA)	Rev 1A
	Date: Monday, July 06, 2015	Sheet 2 of 38	







NB5	PROJECT : Y0H Quanta Computer Inc.		
	Size	Document Number Valley 2/9 (DDRB)	Rev 1A
	Date: Monday, July 06, 2015	Sheet 3 of 38	

+1.8VS5

R93 2.2K_4 SDVO_DATA
R98 2.2K_4 SDVO_CLK
R97 *10K/F_4 HDMI_HPD_DC#
R108_1 2 *100K_4 DDI1_BKLT_EN
R104_1 2 *100K_4 DDI1_BKLT_CTRL_R
R102_1 2 *100K_4 EDP_PANEL_EN

SI: remove R97 as Intel suggestion

2/10 Chqnge P/N
from BAM70020002 to BAM01380016

7/1 Delete R50

+1.8V

DDI1_BKLT_CTRL_R

R52 4.7K_4 +3V

PCH_DPST_PWM 18

DMN53D0L-7 Q5

R51 100K_4

R53 *0_4

GND

U8C BSW_MCP_EDS

DDI0

18 IN_D2 D50 DDI0_TXP_0
18 IN_D2# C51 DDI0_TXN_0
18 IN_D1 H49 DDI0_TXP_1
18 IN_D1# H50 DDI0_TXN_1
18 IN_D0 F53 DDI0_TXP_2
18 IN_D0# F52 DDI0_TXN_2
18 IN_CLK G53 DDI0_TXP_3
18 IN_CLK# G52 DDI0_TXN_3
H47 DDI0_AUXP
H46 DDI0_AUXN
18 HDMI_HPD_DC# W51 HV_DDI0_HPD
18 SDVO_CLK Y51 HV_DDI0_DDC_SCL
18 SDVO_DATA Y52 HV_DDI0_DDC_SDA
V52 PANEL0_BKLTEN
V51 PANEL0_BKLTCTL
W53 PANEL0_VDDEN
R411 402/F_4 SOC_DDIO_RCOMP F38 SOC_DDIO_RCOMP
SOC_DDIO_RCOMP_P G38 DDI0_PLLOBS_P
DDI0_PLLOBS

DDI1

18 INT_EDP_TXP0 INT_EDP_TXP0 J51 DDI1_TXP_0
18 INT_EDP_TXN0 INT_EDP_TXN0 H51 DDI1_TXN_0
18 INT_EDP_TXP1 INT_EDP_TXP1 K51 DDI1_TXP_1
18 INT_EDP_TXN1 INT_EDP_TXN1 K52 DDI1_TXN_1
L53 DDI1_TXP_2
L51 DDI1_TXN_2
M52 DDI1_TXP_3
M51 DDI1_TXN_3
18 INT_EDP_AUXP INT_EDP_AUXP M42 DDI1_AUXP
18 INT_EDP_AUXN INT_EDP_AUXN K42 DDI1_AUXN
DDI1_EDP_HPD_R R51 HV_DDI1_HPD
26 DDI1_BKLT_EN DDI1_BKLT_EN P51 PANEL1_BKLTEN
DDI1_BKLT_CTRL_R P62 PANEL1_BKLTCTL
26 EDP_PANEL_EN EDP_PANEL_EN R53 PANEL1_VDDEN
SOC_DDI1_RCOMP F47 DDI1_PLLOBS_P
R393 402/F_4 SOC_DDI1_RCOMP_P F49 DDI1_PLLOBS

Add DP to VGA port 0617

DDI2

19 DDI2_TX0_P DDI2_TX0_P F40 DDI2_TXP_0
19 DDI2_TX0_N DDI2_TX0_N G40 DDI2_TXN_0
19 DDI2_TX1_P DDI2_TX1_P J40 DDI2_TXP_1
19 DDI2_TX1_N DDI2_TX1_N K40 DDI2_TXN_1
F42 DDI2_TXP_2
G42 DDI2_TXN_2
D44 DDI2_TXP_3
F44 DDI2_TXN_3
19 INT_DDI2_AUXP INT_DDI2_AUXP D48 DDI2_AUXP
19 INT_DDI2_AUXN INT_DDI2_AUXN C49 DDI2_AUXN
DDI2_HPD_CON_R U51 HV_DDI2_HPD
23 UART2_TXD T51 HV_DDI2_DDC_SCL
23 UART2_RXD T52 HV_DDI2_DDC_SDA

NC's

B53 RSVD6
A52 RSVD3
E52 RSVD9
D52 RSVD8
B50 RSVD5
B49 RSVD4
E53 RSVD10
C53 RSVD7
A51 RSVD2
A49 RSVD1
G44 RSVD11

MCSI and Camera Interface

M44 RSVD15
K44 RSVD12
K48 RSVD14
K47 RSVD13
T44 MCSI_1_CLKP
T45 MCSI_1_CLKN
Y47 MCSI_1_DP_0
Y48 MCSI_1_DN_0
V45 MCSI_1_DP_1
V47 MCSI_1_DN_1
V50 MCSI_1_DP_2
V48 MCSI_1_DN_2
T41 MCSI_1_DP_3
T42 MCSI_1_DN_3
P50 MCSI_2_CLKP
P48 MCSI_2_CLKN
P47 MCSI_2_DP_0
P45 MCSI_2_DN_0
M48 MCSI_2_DP_1
M47 MCSI_2_DN_1
T50 RSVD17
T48 RSVD16
P44 MCSI_COMP

GP_CAMERASB

AB41 GP_CAMERASB00
AB45 GP_CAMERASB01
AB44 GP_CAMERASB02
AC53 GP_CAMERASB03
AB51 GP_CAMERASB04
AB52 GP_CAMERASB05
AA51 GP_CAMERASB06
AB40 GP_CAMERASB07
Y44 GP_CAMERASB08
Y42 GP_CAMERASB09
Y41 GP_CAMERASB10
V40 GP_CAMERASB11

7/1 Delete test point

R368 150/F_4

GND

CAM08 CAM08 12 OBSFN_C0 TP33
CAM09 CAM09 12
CAM11 CAM11 12

SDMMC1

M7 SDMMC1_CLK
P6 SDMMC1_CMD
M6 SDMMC1_D0
M4 SDMMC1_D1
P9 SDMMC1_D2
P7 SDMMC1_D3_CD_B
T6 MMC1_D4_SD_WE
T7 MMC1_D5
T10 MMC1_D6
T12 MMC1_D7
T13 MMC1_RCLK
P13 SDMMC1_RCOMP

SDMMC4_CLK 16
SDMMC4_CMD 16
SDMMC4_DAT0 16
SDMMC4_DAT1 16
SDMMC4_DAT2 16
SDMMC4_DAT3 16
SDMMC4_DAT4 16
SDMMC4_DAT5 16
SDMMC4_DAT6 16
SDMMC4_DAT7 16
SDMMC4_RCLK 16
EMMC_RCOMP

R392 100/F_4

GND

SDMMC2

K10 SDMMC2_CLK
K9 SDMMC2_CMD
M12 SDMMC2_D0
M10 SDMMC2_D1
K7 SDMMC2_D2
K6 SDMMC2_D3_CD_B

SDMMC3

F2 SDMMC3_CLK
D2 SDMMC3_CMD
K3 SDMMC3_CD_B
J1 SDMMC3_D0
J3 SDMMC3_D1
H3 SDMMC3_D2
G2 SDMMC3_D3
K2 VSDIO_1P8_EN
L3 VSDIO_PWR_EN#
P12 SDMMC3_1P8_EN
SDMMC3_PWR_EN_B
SDMMC3_RCOMP

R385 80.6/F_4

GND

3 OF 13

*BSW_MCP_EDS

RT2136 output high
SOC active Low

+1.8VS5

R58 10K/F_4

DDI1_EDP_HPD_R

Q6 2N7002K(DMN601K-7)

EDP_HPD_C R59 0_4 ULT_EDP_HPD 18

R61 100K_4

GND GND

2/24 ADD PU to +1.8VS5

+1.8VS5 R165 10K_4 UART2_TXD
R166 10K_4 UART2_RXD

+1.8VS5

R1095 10K/F_4

DDI2_HPD_CON_R

Q34 2N7002K(DMN601K-7)

VGA_HPD_C R1096 0_4 DDI2_HPD_CON 19

R1072 100K_4

GND GND

+1.8VS5

VSDIO_1P8_EN R395 2 *100K_4
VSDIO_PWR_EN# R397 *10K_4

VSDIO_1P8_EN R389 2 *100K_4
VSDIO_PWR_EN# R398 *10K_4

GND

5,35 +1.8V

PROJECT : Y0H
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	Valley 3/9 (Display)	1A

Date: Monday, July 06, 2015 Sheet 4 of 38

HDD

HDD sku only

+1.8V

24 SATA_LED# — Q11 DMN53D0L-7 — SATA_LED_R_N

DMN53D0L-7 Q13

24 ACC_LED# — GND

ACC_LED_R#

C103 *22P/50V_4 No_stuff C119

GND — BIT_CLK_AUDIO

23 SATA_TXP0
23 SATA_TXN0
23 SATA_RXP0
23 SATA_RXN0

26 SOC_KBC_SCI

+1.8V — R71 10K_4 — R67 20/F_4 — SATA_LED_R_N

TP2

+1.8V — R74 10K_4 — SATA_DEVSLP_SOC

R387 402/F_4

+1.8VS5 — R434 100K/F_4 — R364 2.2K_4

22 ACCEL_INTH#

20 ACZ_RST#_AUDIO — R340 75/F_4
20 BIT_CLK_AUDIO — R79 75/F_2
20 ACZ_SDIN0
20 ACZ_SYNC_AUDIO — R331 75/F_4
20 ACZ_SDOUT_AUDIO — R346 75/F_4

20 ACZ_SPKR

7/1 Delete test point

BSW_MCP_EDS U8D

SATA_TXP0	C31	SATA_TXP0	
SATA_TXN0	B30	SATA_TXN0	
SATA_RXP0	N28	SATA_RXP0	
SATA_RXN0	M28	SATA_RXN0	
	C29	SATA_TXP1	
	A29	SATA_TXN1	
	J28	SATA_RXP1	
	K28	SATA_RXN1	
SATA_LED_R_N	AH3	SATA_LEDN	
SATA_GP0	AH2	SATA_GP0	
	AG3	SATA_GP1	SATA
SATA0_DEVSLP_SOC	AG1	SATA_GP2	
SATA_DEVSLP_SOC	AF3	SATA_GP3	
SATA_RCOMP_DP	N30	SATA_OBSP	
SATA_RCOMP_DN	M30	SATA_OBSN	
SOC_SPI_CLK_R	W3	FST_SPI_CLK	
SOC_SPI_CS#_R	V4	FST_SPI_CS0_B	
ACC_LED_R#	V6	FST_SPI_CS1_B	
ACCEL_INTH#	V7	FST_SPI_CS2_B	
SOC_SPI_MOSI_R	V2	FST_SPI_D0	FAST SPI
SOC_SPI_MISO_R	V3	FST_SPI_D1	
SOC_SPI_WP#	U1	FST_SPI_D2	
SOC_SPI_HOLD#	U3	FST_SPI_D3	
ACZ_RST#	AF13	MF_HDA_RSTB	
	AD6	MF_HDA_SDI1	
ACZ_BCLK	AD9	MF_HDA_CLK	
ACZ_SDIN0	AD7	MF_HDA_SDI0	
ACZ_SYNC	AF12	MF_HDA_SYNC	
ACZ_SDOUT	AF14	MF_HDA_SDO	
	AB9	MF_HDA_DOCKENB	
	AB7	MF_HDA_DOCKRSTB	
	H4	SPKR	AUDIO
	AK9	GP_SSP_2_CLK	
	AK10	GP_SSP_2_FS	
	AK12	GP_SSP_2_TXD	
	AK13	GP_SSP_2_RXD	

4 OF 13

*BSW_MCP_EDS

	C24	PCIE_TXP0	PCIE_TXP0_CR_L	C128 0.1U/16V_4	PCIE_TXP0_CARD 17
	B24	PCIE_TXN0	PCIE_TXN0_CR_L	C127 0.1U/16V_4	PCIE_TXN0_CARD 17
	G20	PCIE_RXP0			PCIE_RXP0_CARD 17
	J20	PCIE_RXN0			PCIE_RXN0_CARD 17
	A25	PCIE_TXP1			
	C25	PCIE_TXN1			
	D20	PCIE_RXP1			
	F20	PCIE_RXN1			
	B26	PCIE_TXP2	PCIE_TXP2_NGFF_C	C528 0.1U/16V_4	PCIE_TXP2_NGFF 24
	C26	PCIE_TXN2	PCIE_TXN2_NGFF_C	C529 0.1U/16V_4	PCIE_TXN2_NGFF 24
	D22	PCIE_RXP2			PCIE_RXP2_NGFF 24
	F22	PCIE_RXN2			PCIE_RXN2_NGFF 24
	A27	PCIE_TXP3	PCIE_TXP3_WLAN_C	C130 0.22U/16V_4	PCIE_TXP3_WLAN 24
	C27	PCIE_TXN3	PCIE_TXN3_WLAN_C	C129 0.22U/16V_4	PCIE_TXN3_WLAN 24
	G24	PCIE_RXP3			PCIE_RXP3_WLAN 24
	J24	PCIE_RXN3			PCIE_RXN3_WLAN 24
	AM10	PCIE_CLKREQ0B			CLK_PCIE_REQ2# 17
	AM12	PCIE_CLKREQ1B	PCIE_CLKREQ1#		
	AK14	PCIE_CLKREQ2B	PCIE_CLKREQ_NGFF#		PCIE_CLKREQ_NGFF# 24
	AM14	PCIE_CLKREQ3B	PCIE_CLKREQ_WLAN#		PCIE_CLKREQ_WLAN# 24
	A21	CLK_DIFF_P_0			CLK_PCIE_CRP 17
	C21	CLK_DIFF_N_0			CLK_PCIE_CRN 17
	C19	CLK_DIFF_P_1			
	B20	CLK_DIFF_N_1			
CLK_PCIE_NGFFP	C18	CLK_DIFF_P_2			CLK_PCIE_NGFFP 24
CLK_PCIE_NGFFN	B18	CLK_DIFF_N_2			CLK_PCIE_NGFFN 24
CLK_PCIE_WLANP	C17	CLK_DIFF_P_3			CLK_PCIE_WLANP 24
CLK_PCIE_WLANN	A17	CLK_DIFF_N_3			CLK_PCIE_WLANN 24
	C16	RSVD20			
	B16	RSVD21			
SOC_PCIE_COMP	D26	PCIE_OBSP			
SOC_PCIE_COMN	F26	PCIE_OBSN	R420 402/F_4		
	V14	SPI1_CLK			
	Y13	SPI1_CS0_B			
	Y12	SPI1_CS1_B			
	V13	SPI1_MISO			
	V12	SPI1_MOSI			

Card reader

WIFI

WIFI

+1.8VS5

CLK_PCIE_REQ2# R277 10K_4
PCIE_CLKREQ1# R275 10K_4
PCIE_CLKREQ_NGFF# R296 10K_4
PCIE_CLKREQ_WLAN# R271 10K_4

Vender	Size	P/N
Winbond	8MB	AKE5EZN0N01 (W25Q64FWSSIQ)
GigaDevice	8MB	AKE5EG-0Q00 (GD25LQ64CSIGR)
	8MB	AKE5EFN0Q00 (EN25S64-104HIP)
Socket (208mil)		DFHS08FS023 (Firstly Stuff)

+3VS5 +1.8VS5

R426 *0_4 R422 0_4

SOC_SPI_CLK_R2 — C411 10P/50V_4 — GND

EMI

R464 3.3K/F_4 R448 3.3K/F_4 C404 0.1U/16V_4 GND

SOC_SPI_WP# R470 0_4

SOC_SPI_HOLD# R450 0_4

SPI NOR FLASH

U9

SPI_VCC 8 VCC
SPI_3P 3 WP#
SPI_7P 7 SPI_HOLD
SPI_SI 5
SPI_SO 2
CS# 1
SPI_SCK 6
GND 4

SPI_FLASH
soic8-7_9-1_27
AKE5EZN0N00
IC FLASH (8P) W25Q64FWSSIQ (SOIC)
20150101: SI build change to AKE5EZN0N01

GND

SOC_SPI_MOSI_R2 R478 10_4 SOC_SPI_MOSI_R
SOC_SPI_MISO_R2 R457 10_4 SOC_SPI_MISO_R
SOC_SPI_CS#_R2 R444 33_4 SOC_SPI_CS#_R
SOC_SPI_CLK_R2 R468 10_4 SOC_SPI_CLK_R

3/9 Del net: EC_SPI_WP# / EC_SPI_HOLD# ; location: R107,R116
To EC for share ROM

To EC for share ROM
3/9 Del net: SOC_SPI_CLK / SOC_SPI_CS# / SOC_SPI_MISO / SOC_SPI_MOSI; location: R448,R480,R479,R462

To EC for SHPI

R475 *0_4 SHPI_SPI_CLK 25
R443 *0_4 SHPI_SPI_CS# 25
R456 *0_4 SHPI_SPI_MISO 25
R479 *0_4 SHPI_SPI_MOSI 25
SOC_SPI_WP# R469 *0_4 SHPI_SPI_WP# 25
SOC_SPI_HOLD# R451 *0_4 SHPI_SPI_HOLD# 25

From CPU

SPI_VCC R447 *3.3K/F_4 SOC_SPI_CS#_R2

SOC_SPI_MOSI_R2 TP54
SOC_SPI_MISO_R2 TP53
SOC_SPI_CS#_R2 TP50
SOC_SPI_CLK_R2 TP51
SPI_3P TP55
SPI_7P TP45

For EMI

*10P/50V_4 C416 SOC_SPI_CLK_R2

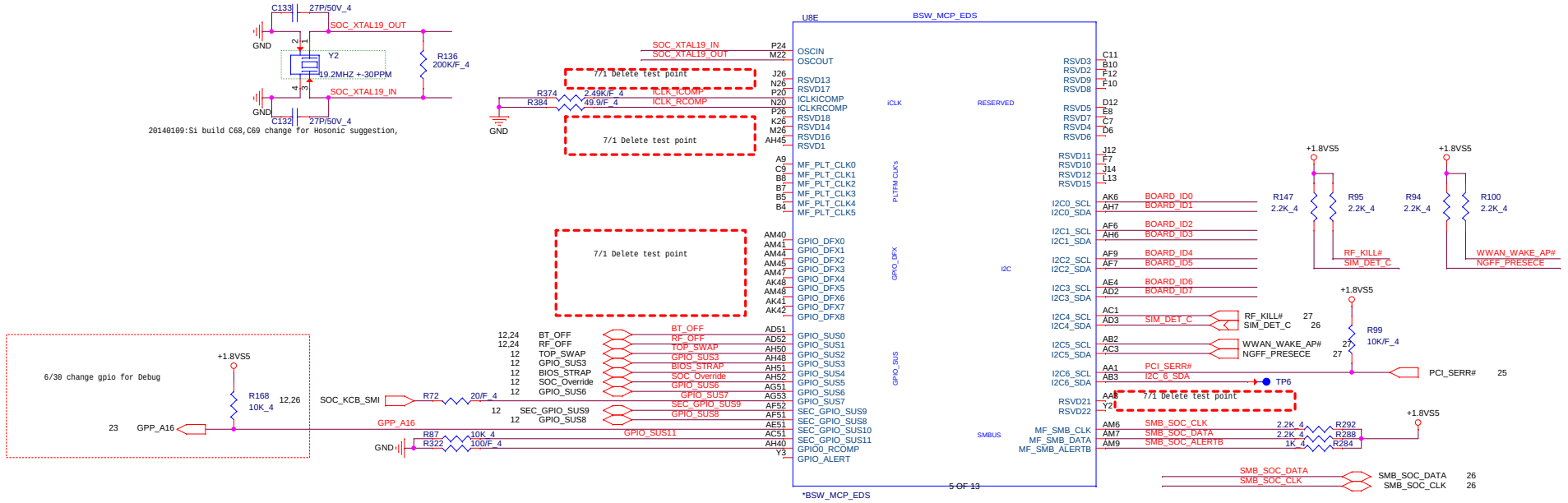
4,35 +1.8V

NB5

PROJECT : Y0H
Quanta Computer Inc.

Size	Document Number	Rev
	Valley 4/9 (SD/PCIE/SATA)	1A

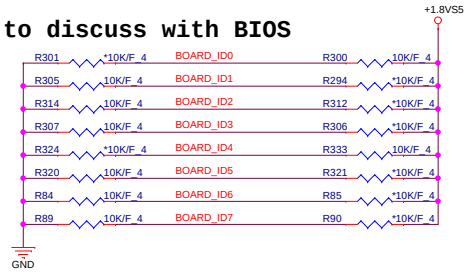
Date: Monday, July 06, 2015 Sheet 5 of 38



BOARD ID SETTING

	Reserve (Default = 000)			Size	Reserved			Storage
Model	BOARD_ID7	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Samsung	0	1	0	2G=0	0	0	0	0 : emmc
Mircon	0	0	1	4G=1	0	0	0	1 : HDD
Hynix	0	0	0	0	0	0	0	

Need to discuss with BIOS



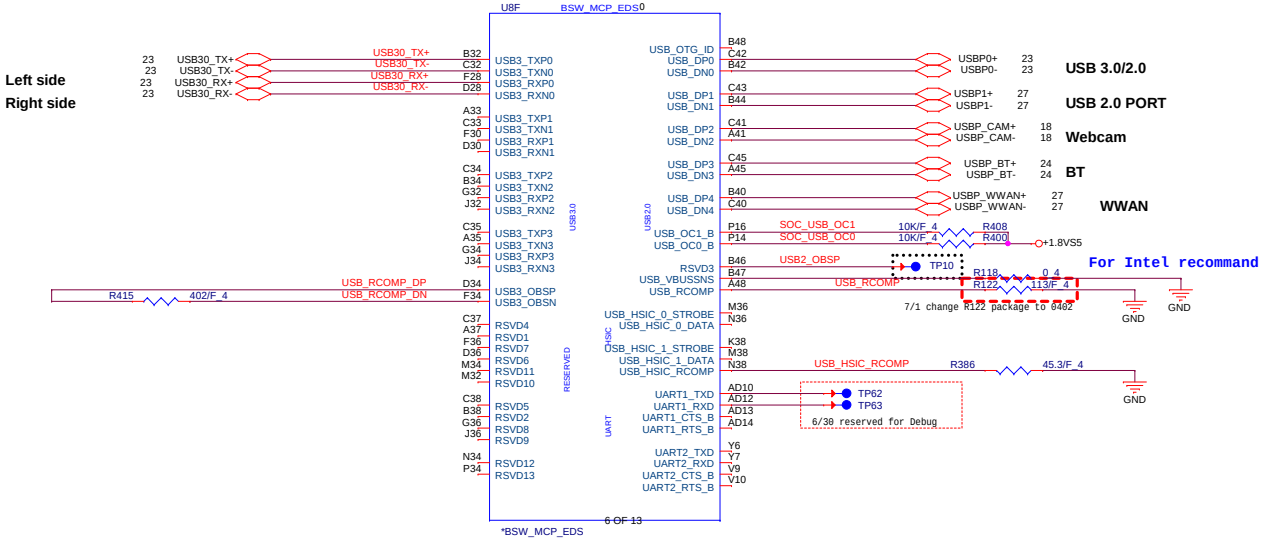
NB5

PROJECT : Y0H

Quanta Computer Inc.

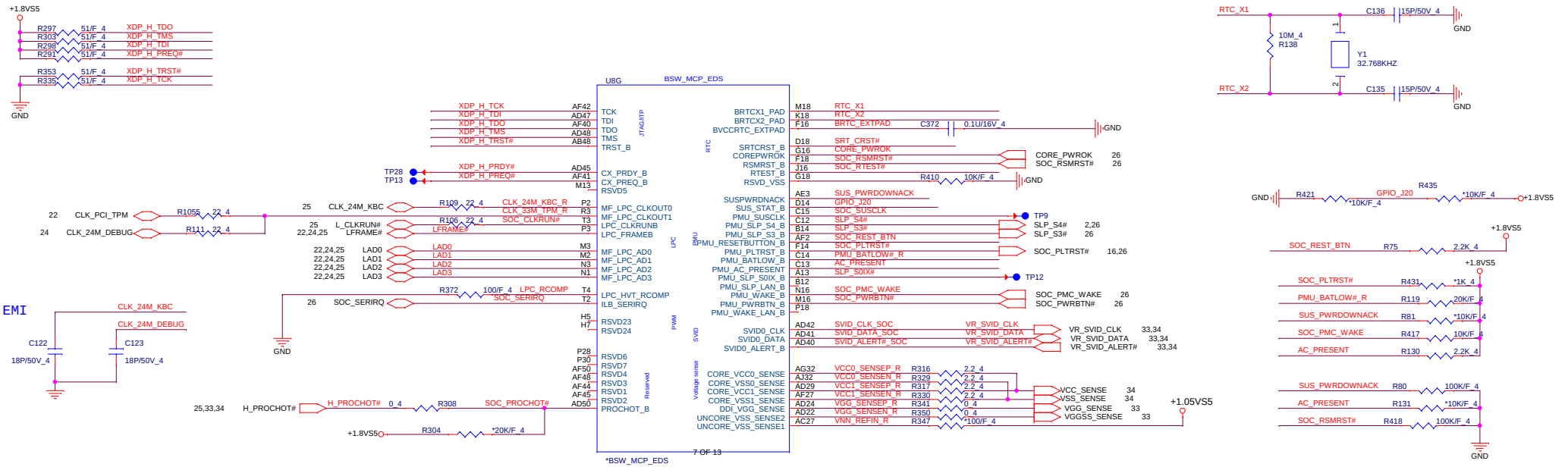
Size	Document Number	Rev
	Valley 5/9 (SPI/GPIO/CLK)	1A

Date: Monday, July 06, 2015 Sheet 6 of 38



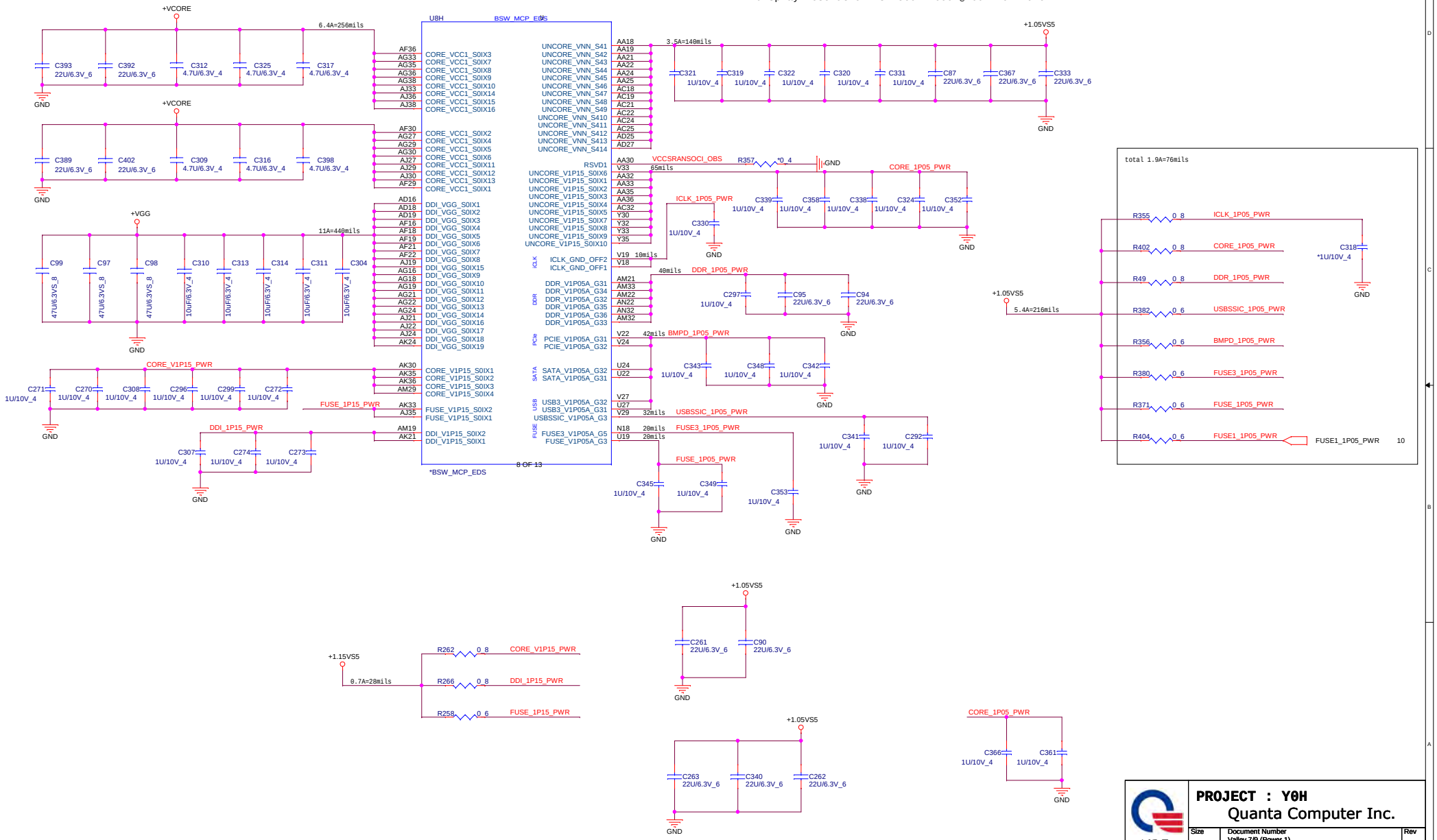
PROJECT : Y0H Quanta Computer Inc.			
NB5	Size	Document Number Valley 6/9 (USB/LPC/I2C)	Rev 1A
	Date: Monday, July 06, 2015	Sheet 7 of 38	

RTC Clock 32.768KHz

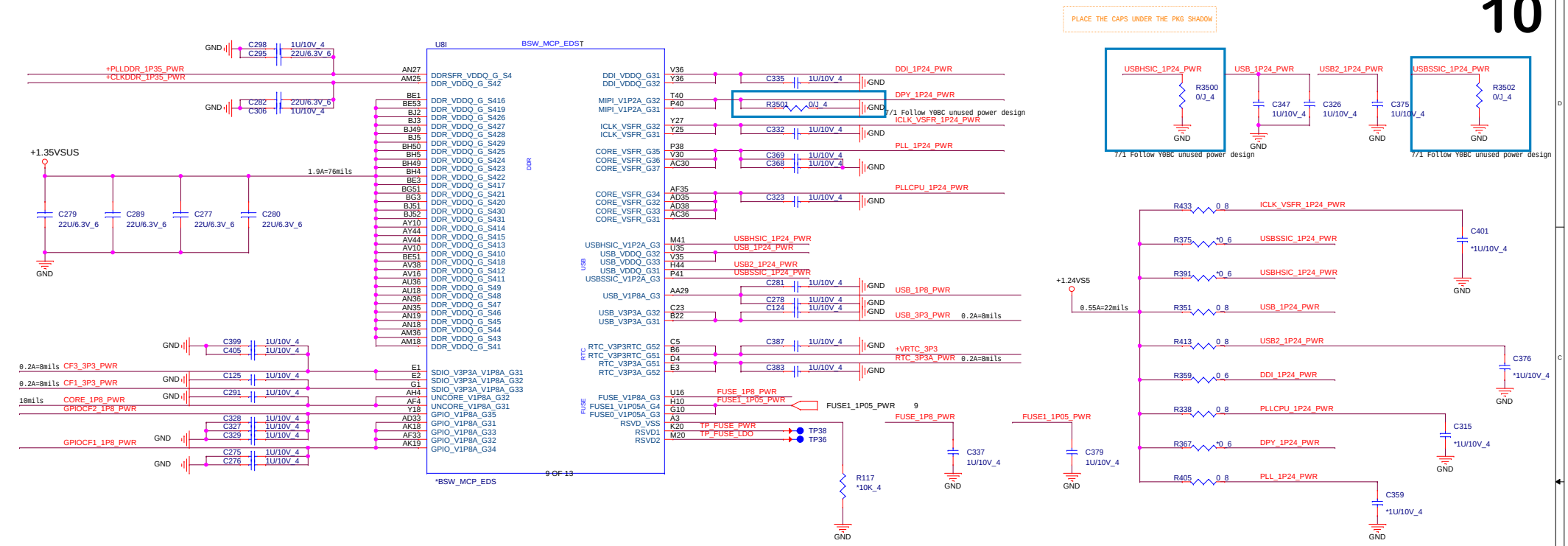


NB5	PROJECT : Y0H Quanta Computer Inc.	
	Size: Document Number: Valley 6/9 (USB/LPC/I2C)	Rev: 1A
	Date: Monday, July 06, 2015	Sheet 8 of 38

VNN can optionally be merged with V1P05A
if display resolution is 2560 x1600 @ 60Hz or lower.



PROJECT :	Y0H
Quanta Computer Inc.	
NB5	
Size	Document Number: Valley 7/9 (Power 1)
Rev	1A
Date: Monday, July 06, 2015	Sheet 9 of 38

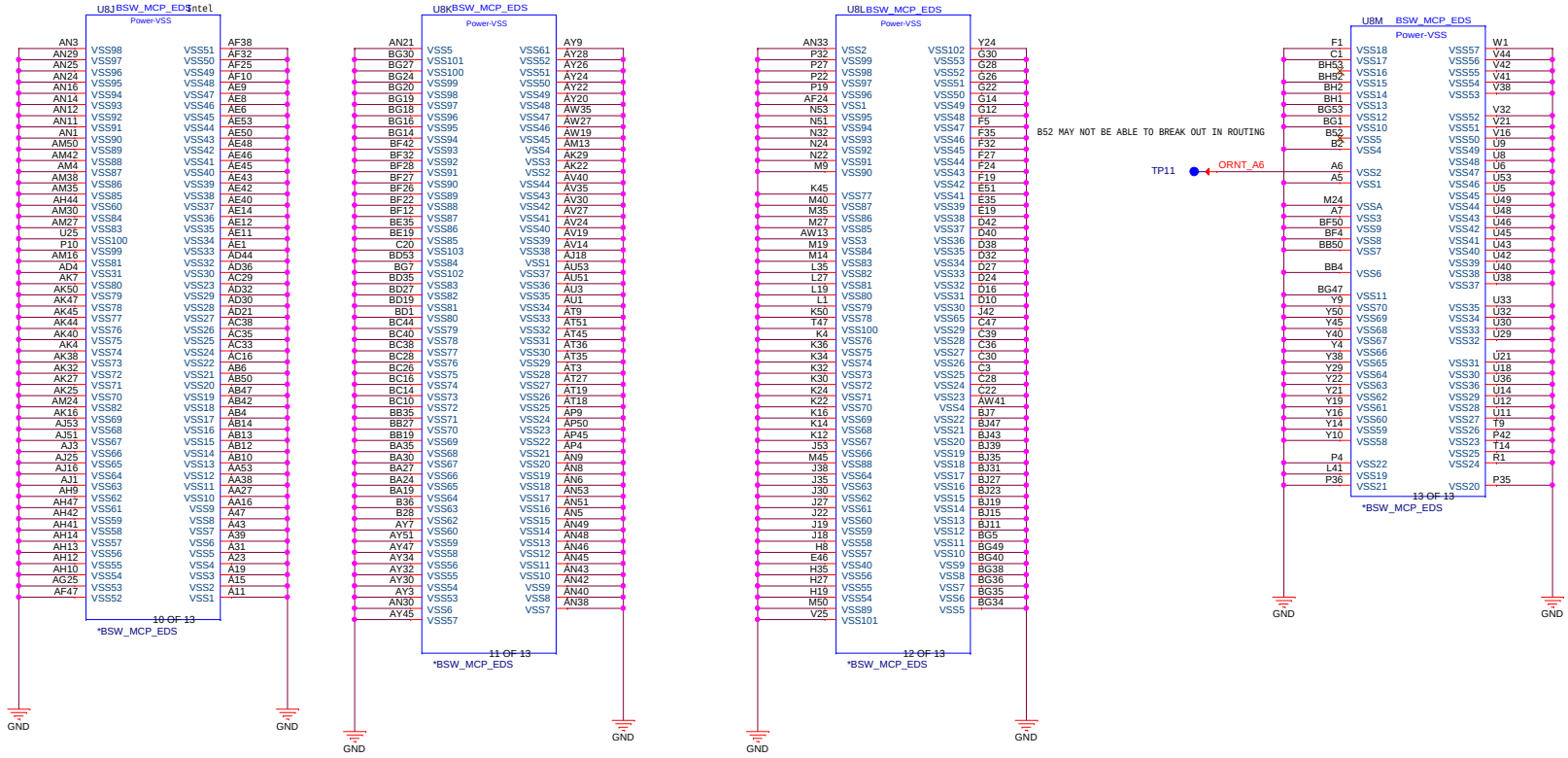


VSDIO VOLTAGE SETTING (CF3_3P3_PWR)		
SDMMC3_PWR_EN_N	SDMMC3_1P8_EN	VSDIO (V)
1	0	0V
1	1	0V
0	0	3.3V
0	1	1.8V

PROJECT : Y0H
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	Valley 8/9 (Power 2)	1A
Date: Monday, July 06, 2015	Sheet 10 of 38	

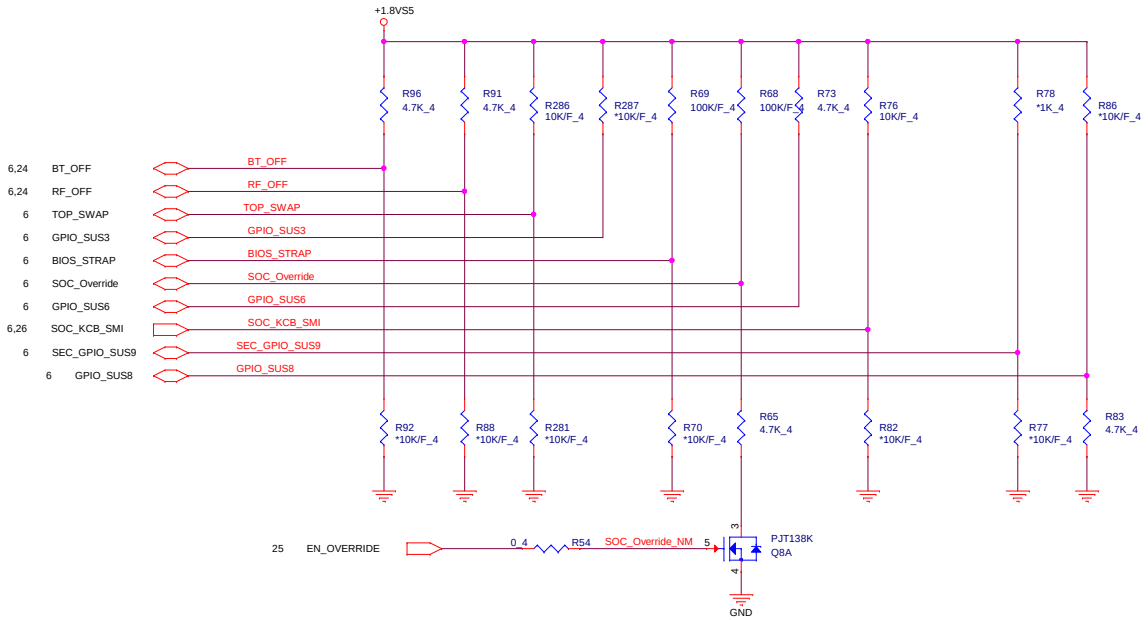


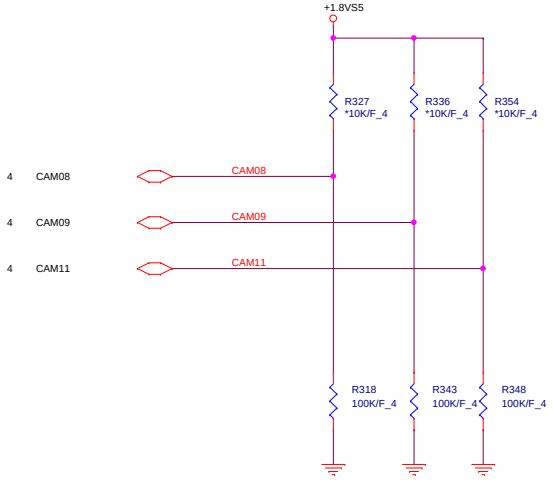
PROJECT : Y0H

Quanta Computer Inc.

NB5

Size	Document Number	Rev
	Valley 9/9 (GND)	1A
Date: Monday, July 06, 2015	Sheet 11 of 38	





	CAM08	CAM09	CAM11
PULL HIGH	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
PULL LOW	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT

REQUIRED STRAPS

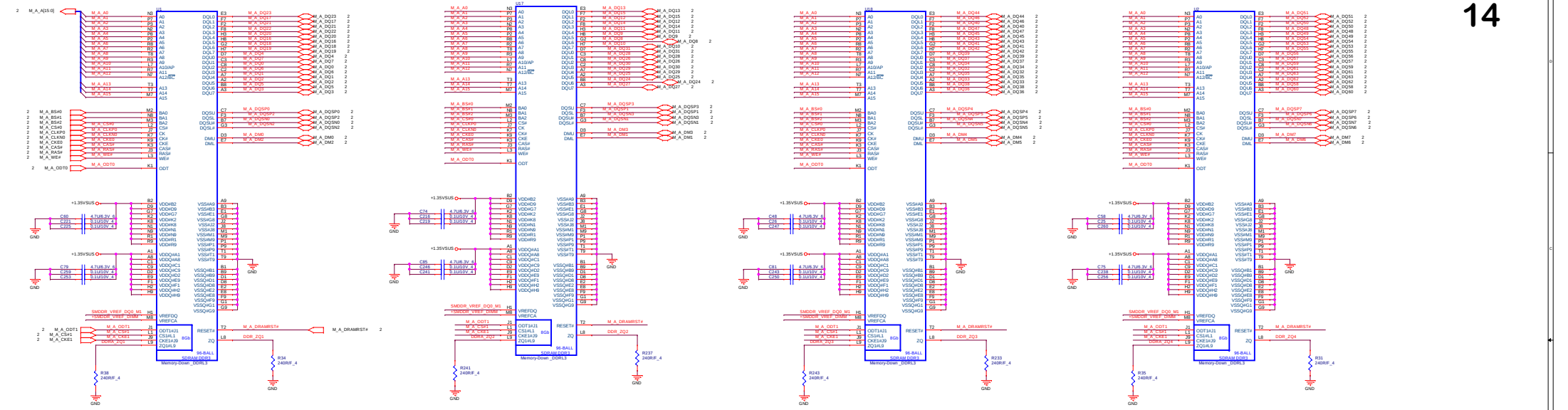
	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
PULL HIGH	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V
PULL LOW	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override DEFAULT			Supply is 1.25V DEFAULT

NB5

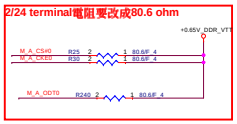
PROJECT : Y0H
Quanta Computer Inc.

Size	Document Number	Rev
	Valley 9/9 (GND)	1A

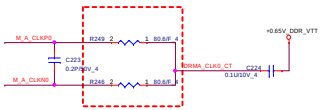
Date: Monday, July 06, 2015 Sheet 12 of 38



2/24 terminal電阻要改成80.6 ohm

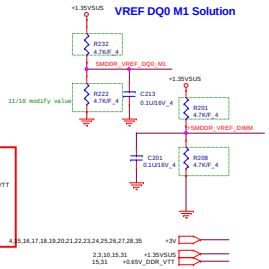


7/1 terminal電阻要改成80.6 ohm

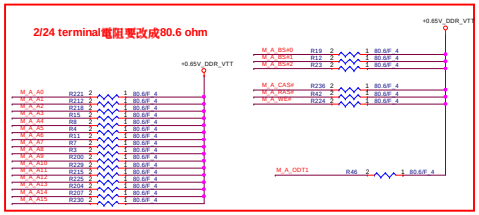


2/24 terminal電阻要改成80.6 ohm

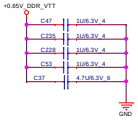
VREF DQ0 M1 Solution



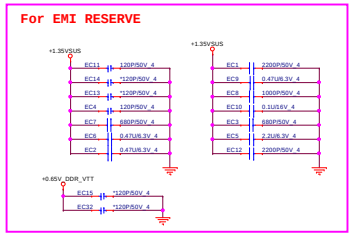
2/24 terminal電阻要改成80.6 ohm



DDR3L				
TOPBS PN	QBCON	Vender PN	Description	
AKD5JGETW07	AKD5JGETW08	H5TC4G63AFR-PBA	IC SDRAM (96P) H5TC4G63AFR-PBA	Hynix (default)
AKD5PGST508	AKD5PGST509	K4B4G1646Q-HYK0	IC SDRAM (96P) K4B4G1646Q-HYK0	Samsung
	AKD5PGSTL19	MT41K256M16LY-107:N	IC SDRAM(96P)MT41K256M16LY-107:N	Micron
AKD5PGSTW14	AKD5PGSTW15	H5TC4G63CFR-PBA	IC SDRAM (96P) H5TC4G63CFR-PBA	Hynix (NEW Die)

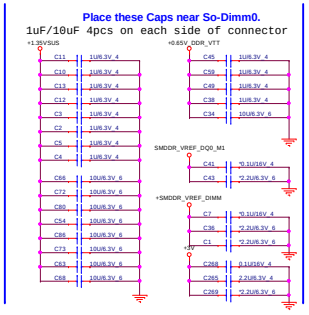


For EMI RESERVE



Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



PROJECT : Y0H

Quanta Computer Inc.

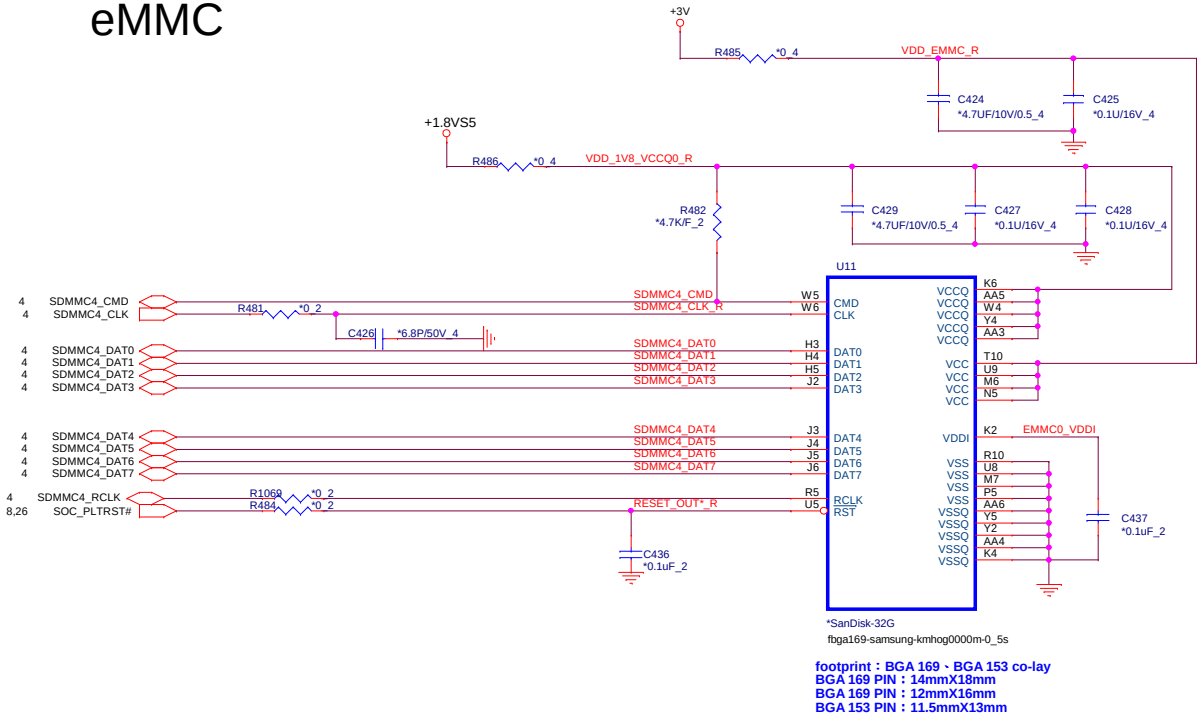
NB5

Size | Document Number: DDR3 DIMM0-STD(4.0th) | Rev: 1a

Date: Monday, July 06, 2015 | Sheet 14 of 38


2/24 terminal電阻要改成80.6 ohm
7/1 terminal電阻要改成80.6 ohm
VREF DQ1 M1 Solution
Local Thermal Sensor
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
Local Thermal Sensor
DDR3 Thermal Sensor
Main:AL0014120003 EMC1412-1-ACZL-TR(98h)
2nd:AL0004310014 TMP431ADGKR(98h)
PROJECT : Y0H
Quanta Computer Inc.
NB5
DDR3 DIMM1-STD(4.0H)
Monday, July 06, 2015
Sheet 15 of 38

eMMC



footprint：BGA 169、BGA 153 co-lay
BGA 169 PIN：14mmX18mm
BGA 169 PIN：12mmX16mm
BGA 153 PIN：11.5mmX13mm

Default

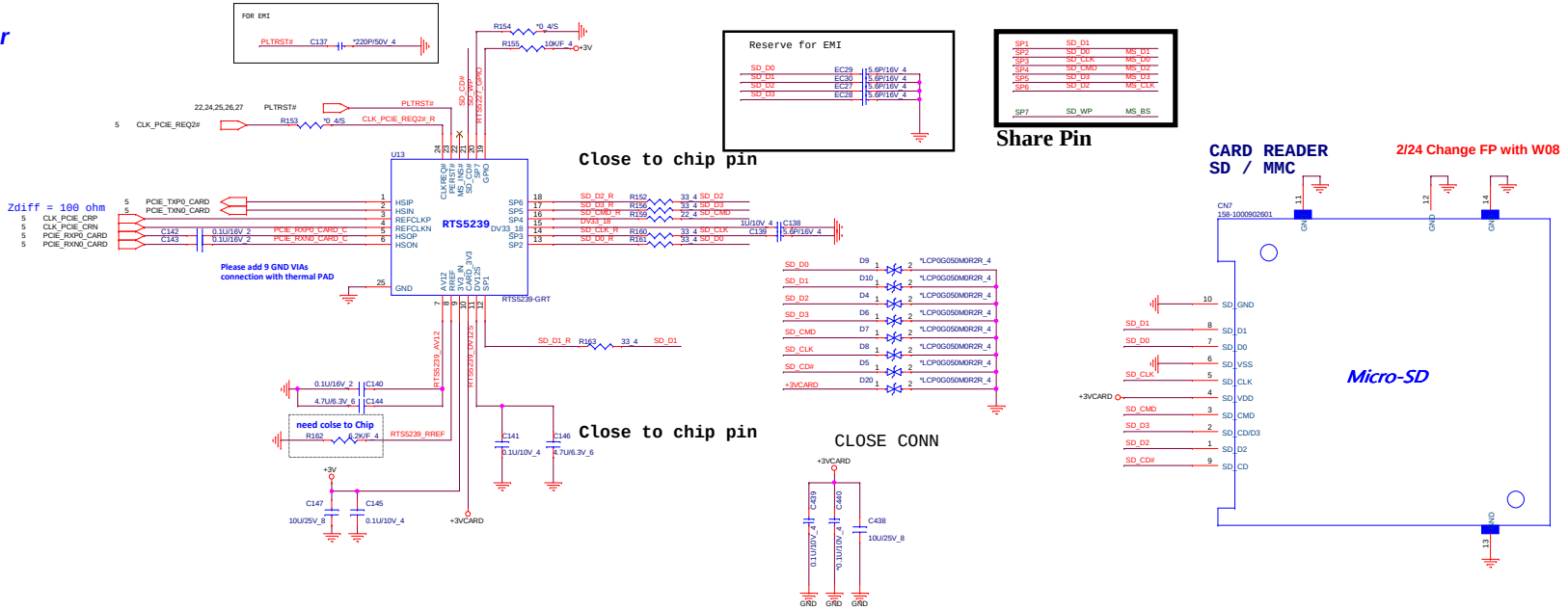
iNAND (eMMC) V4.51

TOPBSQ	QBCON	Description	SIZE	Vender
AKE3SZ-TW01	AKE3SZ-TW02	IC FLASH(153P)H26M64103EMR(FBGA)	32G	Hynix
	AKE5SZ0T512	IC FLASH(153)KLMBG4GEND-B031(FBGA)	32G	samaung
AKE3SFUT000	AKE3SFUT001	IC FLASH(153P)SDIN9DW4-32G(FBGA)	32G	SanDisk
AKE3TG-TW01	AKE3TG-TW02	IC FLASH(153P)H26M78103CCR(FBGA)	64G	Hynix
	AKE3TZPT520	IC FLASH(153)KLMCG8GEND-B031(FBGA)	64G	samaung
AKE3TFUT101	AKE3TFUT102	IC FLASH(153P)SDIN9DW4-64G(FBGA)	64G	SanDisk

eMMC setting		Location				
Vender	SIZE	R526 *10K_4	R528 *10K_4	R527 *10K_4	R529 *10K_4	R530 *10K_4
Hynix	32G	1	O	O	O	O
samaung	32G	1	1	O	O	O
SanDisk	32G	1	1	1	O	O
Hynix	64G	1	1	1	1	O
samaung	64G	O	1	1	1	1
SanDisk	64G	O	O	1	1	1
Hynix	128G	O	O	O	1	1
samaung	128G	O	O	O	O	1
SanDisk	128G	O	O	O	O	O
		1	1	1	1	1

Memory setting		Location				
Vender	SIZE	R521 *10K_4	R522 *10K_4	R523 *10K_4	R524 *10K_4	R525 *10K_4
Hynix	2G	1	O	O	O	O
samaung	2G	1	1	O	O	O
Micron	2G	1	1	1	O	O
Hynix	4G	1	1	1	1	O
samaung	4G	O	1	1	1	1
Micron	4G	O	O	1	1	1
		O	O	O	1	1
		O	O	O	O	1
		O	O	O	O	O
		1	1	1	1	1

CardReader



NB5	PROJECT : Y0H Quanta Computer Inc.	
Size	Document Number TOPAZ_S3_Main	Rev 1A
Date: Monday, July 06, 2015	Sheet 17of 38	

LID Switch

R250 can't change to shortpad

SI...Change LVDS_BLCON1 to PN_BLON ...12/13

100mA

For EDP Only: stuff Cap
For LVDS only stuff Resister

For eDP

R6110 close to U6100
for eDP,stuff

for eDP,stuff U2 & L8

for LVDS,stuff C29 & R23

EMI Solution

3/10 Del location: R578,R584

Close to HDMI connector

Close to Q16

FOLLOW W03

for EMI request

HDMI SMBus Isolation

Close to HDMI connector

PJT138K

HDMI CONN

LVDS Conn.

GS12401-1011-9H
51519-03001-v01-30p-l

DFFC30FR150

L9
MCM2012B900GBE

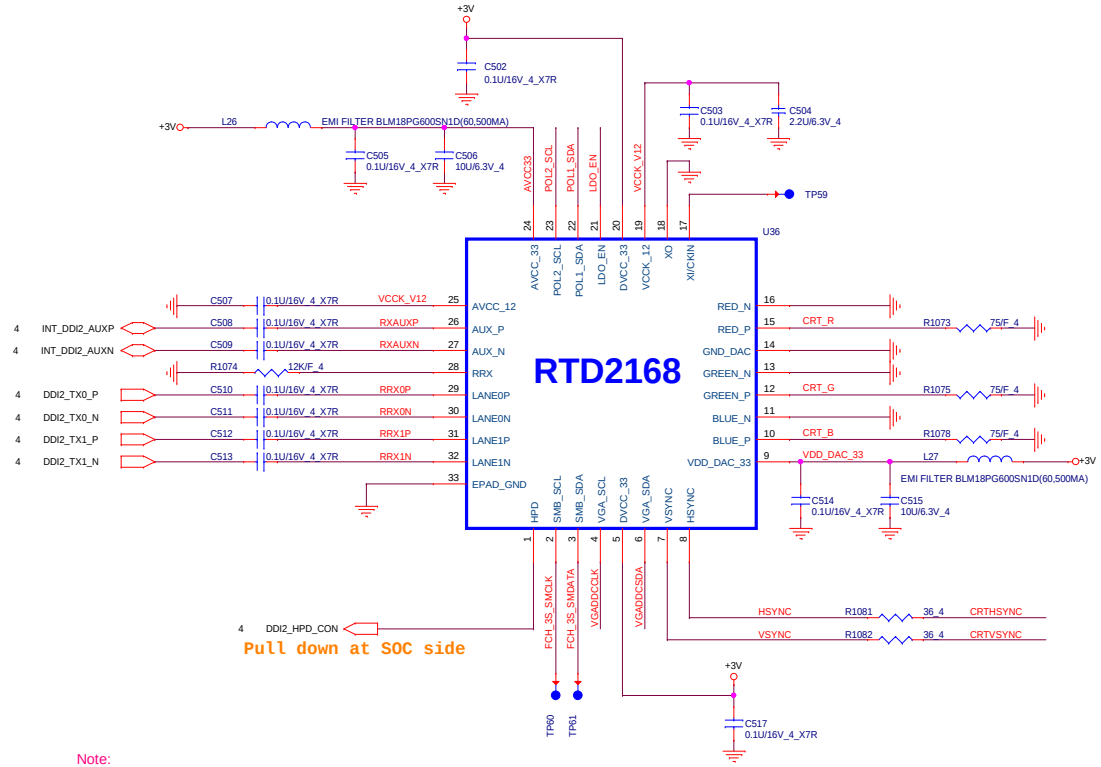
For EDP Only,close CN6100

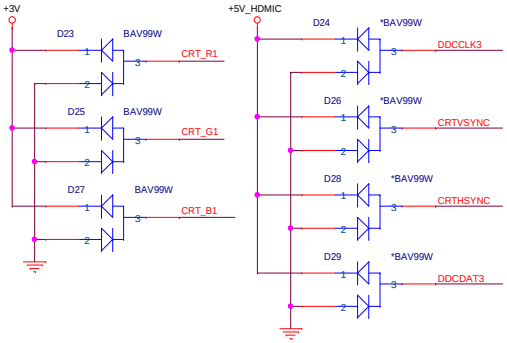
For EDP Only: Reserve

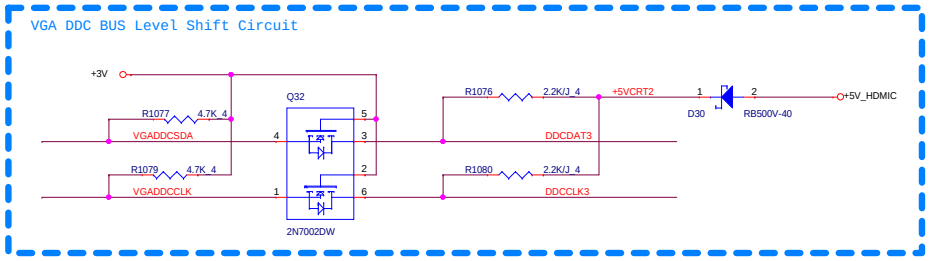
40 mils

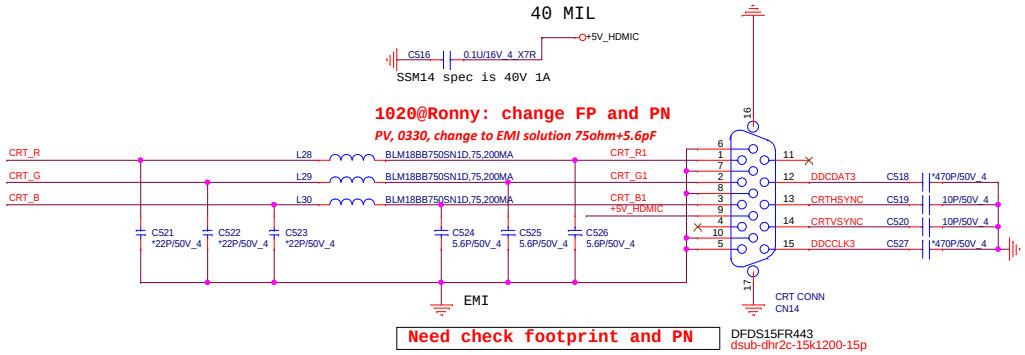
SSM14 spec is 40V 1A

PROJECT : Y0H			
Quanta Computer Inc.			
NB5	Size: Custom	Document Number: LCD CONN/LID/CAM/D-MIC	Rev: 1A
	Date: Monday, July 06, 2015	Sheet 18 of 38	





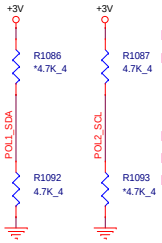




Note:
1- C1,C3,C6,C8,C9,C11,C12,C19,C20
Should be close to chip
2- C12 shold be X5R material
3- R1 should be 12K ohm with +/-1%
4- R8, R9, R10 should be 75 ohm with +/-1%

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

EEPROM MODE

In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

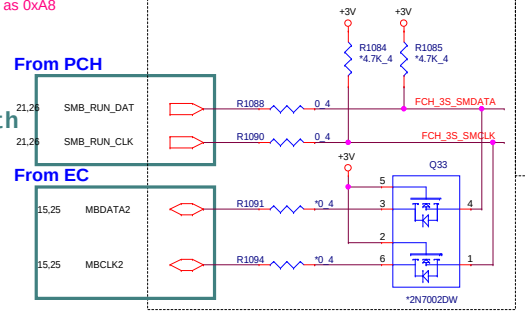
1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

DB:check with SMBUS

CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address: 0x64/0x65 and 0x68/0x69



Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

NB5

PROJECT : S400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 – DP2VGA_converter	1A
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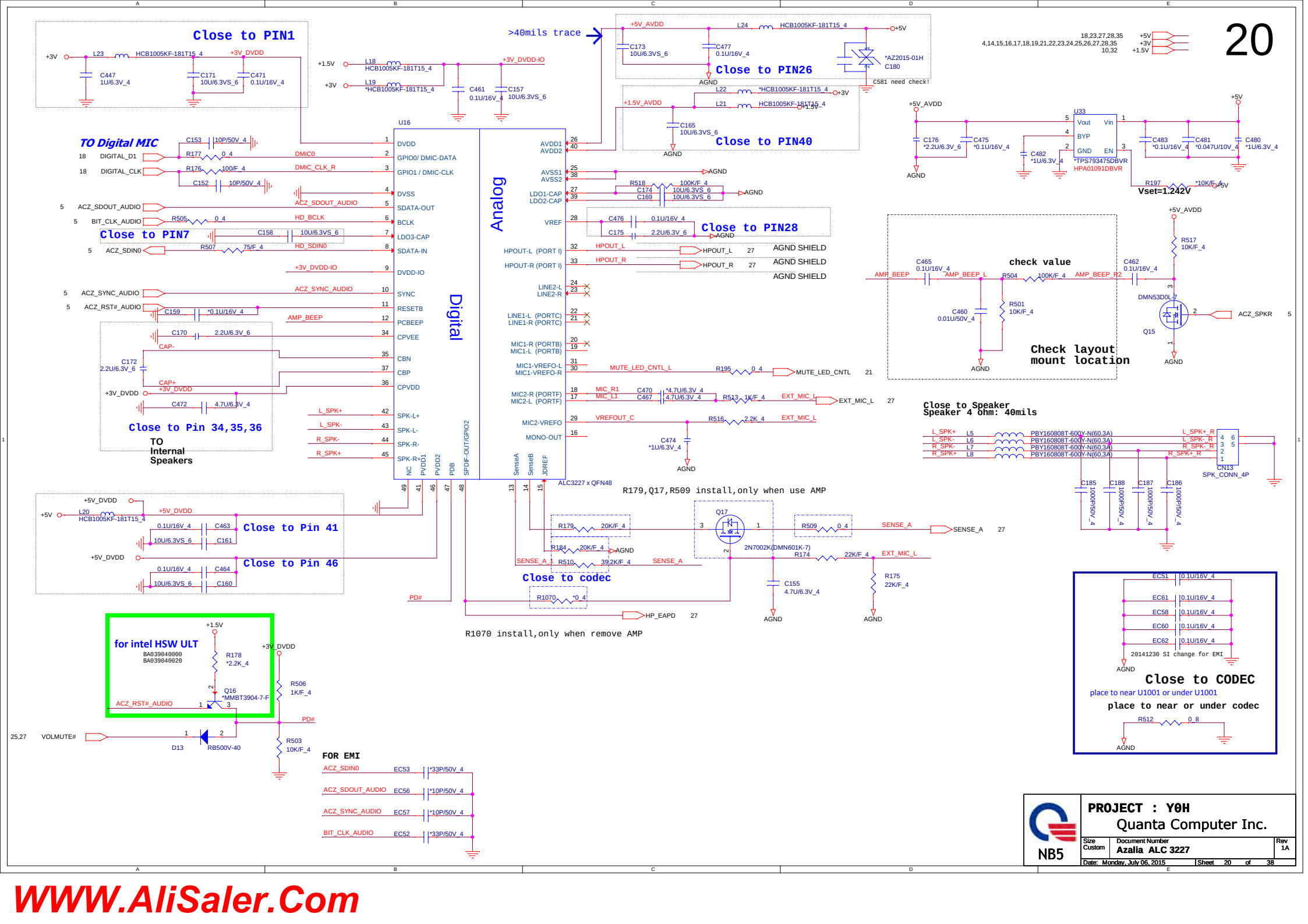
20
Close to PIN1
>40mils trace
Close to PIN26
Close to PIN40
Close to PIN28
Close to PIN7
TO Digital MIC
Close to Pin 34,35,36
TO
Internal
Speakers
Close to Pin 41
Close to Pin 46
Close to codec
Close to Speaker
Speaker 4 ohm: 40mils
check value
Check layout
mount location
Vset=1.242V
R179,Q17,R509 install,only when use AMP
R1070 install,only when remove AMP
for intel HSW ULT
FOR EMI
Close to CODEC
place to near U1001 or under U1001
place to near or under codec
U16
Analog
Digital
ALC3227 x QFN48
AGND SHIELD
PROJECT : Y0H
Quanta Computer Inc.
NB5
Azalia ALC 3227
Rev 1A
Date: Monday, July 06, 2015
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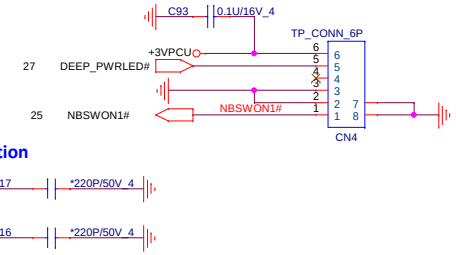
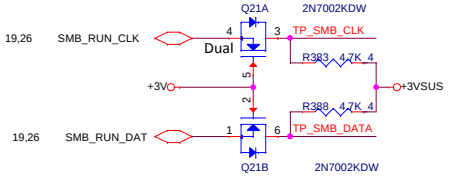
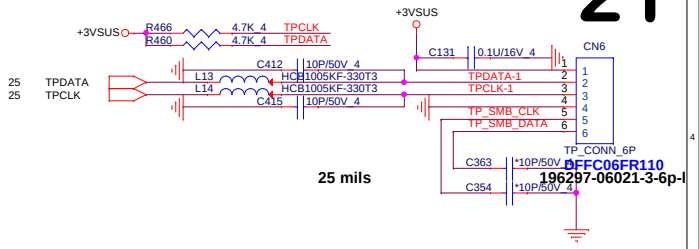
WWW.AliSaler.Com

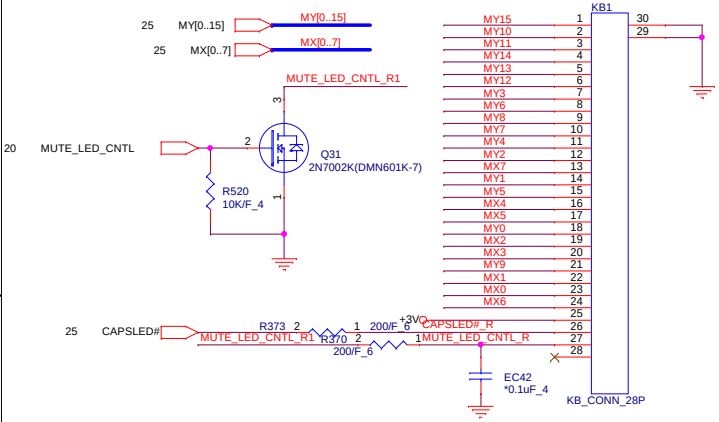
Touch Pad Connector

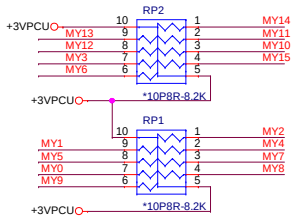




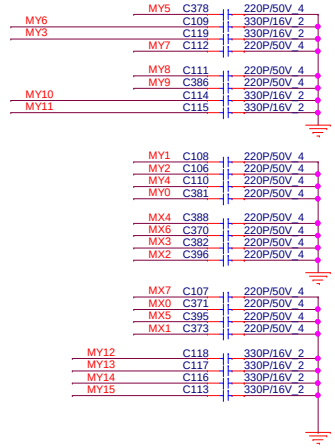


KEYBOARD Con.





KEYBOARD PULL-UP



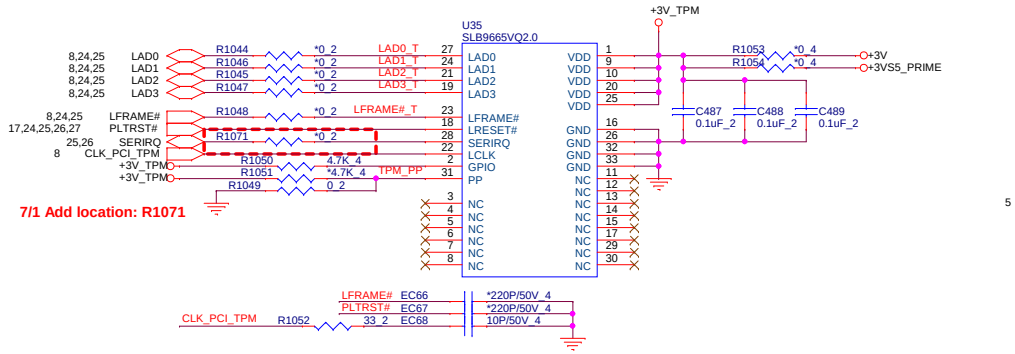
4,14,15,16,17,18,19,20,22,23,24,25,26,27,28,35 +3V
18,20,23,27,28,35 +5V
8,10,23,24,25,26,27,29,30 +3VPCU

NB5

PROJECT : Y0H
Quanta Computer Inc.

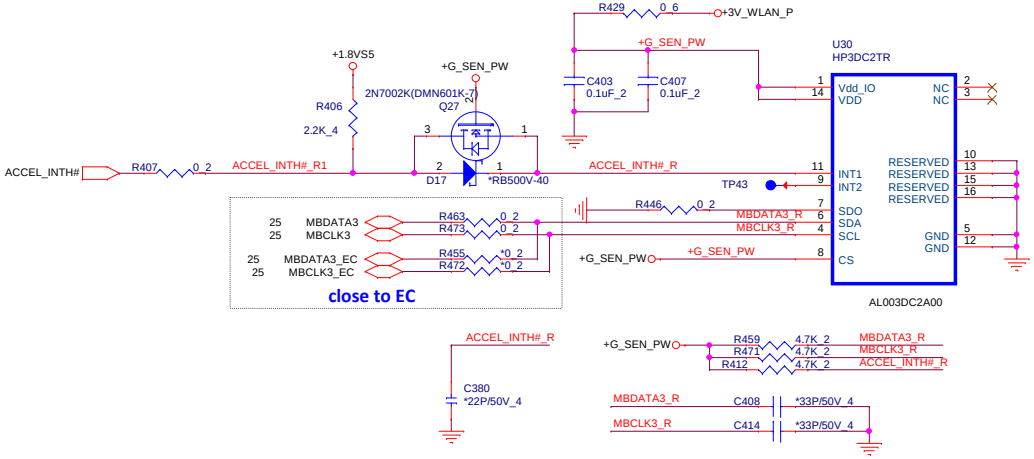
Size	Document Number	Rev
	TPM/TP/FAN/LED	1A
Date: Monday, July 06, 2015	Sheet 21 of 38	

TPM (2.0)



Accelerometer Sensor

G-Sensor Power need check



Touch screen

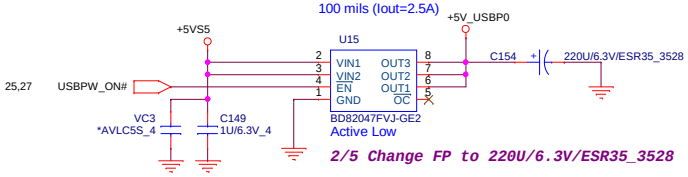
Green CLK Circuitry

23,27,28,30,31,32,33,34,35 +5VS5
8,10,21,23,24,25,26,27,29,30 +3VPCU

4,14,15,16,17,18,19,20,21,23,24,25,26,27,28,35 +3V
18,20,23,27,28,35 +5V

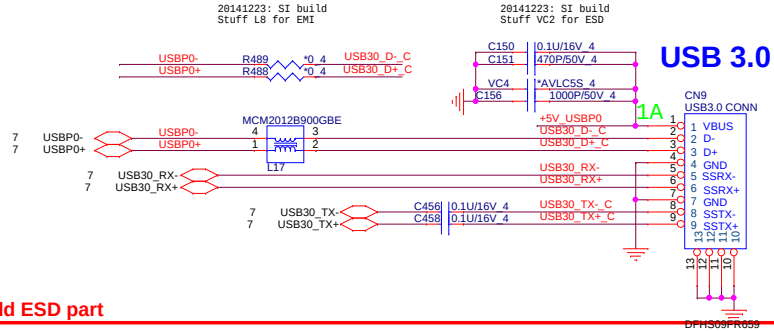
NB5	PROJECT : Y0H Quanta Computer Inc.	
Size	Document Number USB3.0/GCLK/TS/FR	Rev 1A
Date: Monday, July 06, 2015	Sheet 22 of 38	

USB 2.0/3.0 Combo

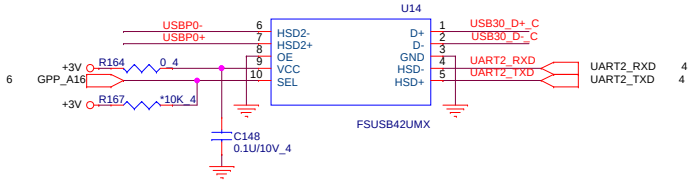


2/5 Change FP to 220U/6.3V/ESR35_3528

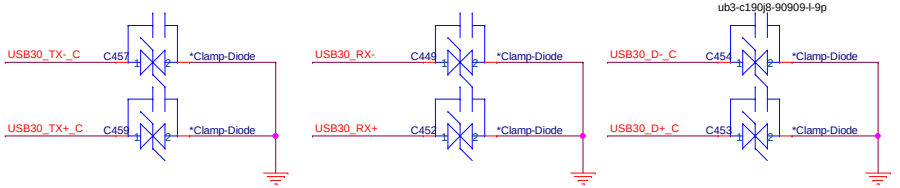
USB 3.0



UART for DEBUG

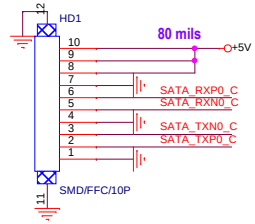


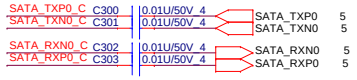
2/25 Add ESD part

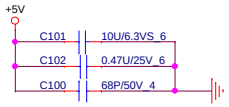


HDD

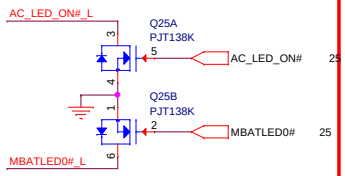
3/24 Change pin define as Napa





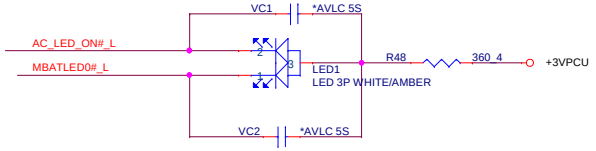


2/26 add LED MOS



PWR LED

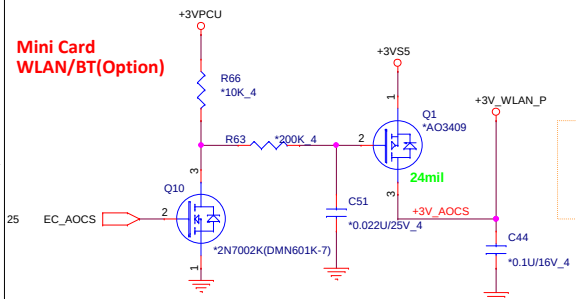
2/10 need check with EC

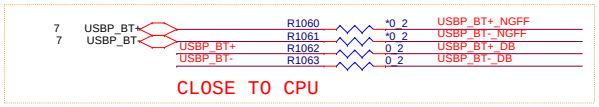


14,15,16,17,18,19,20,21,22,24,25,26,27,28,35 +3V
18,20,27,28,35 +5V
8,10,21,24,25,26,27,29,30 +3VPCU

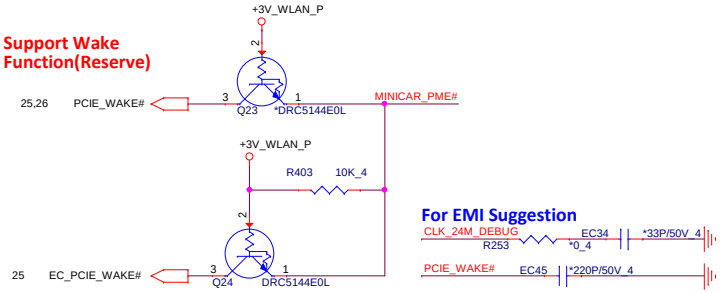
NB5	PROJECT : Y0H Quanta Computer Inc.	
Size	Document Number RTS5141 CARD READER	Rev 1A
Date: Monday, July 06, 2015	Sheet 23 of 38	

Mini Card WLAN/BT(Option)

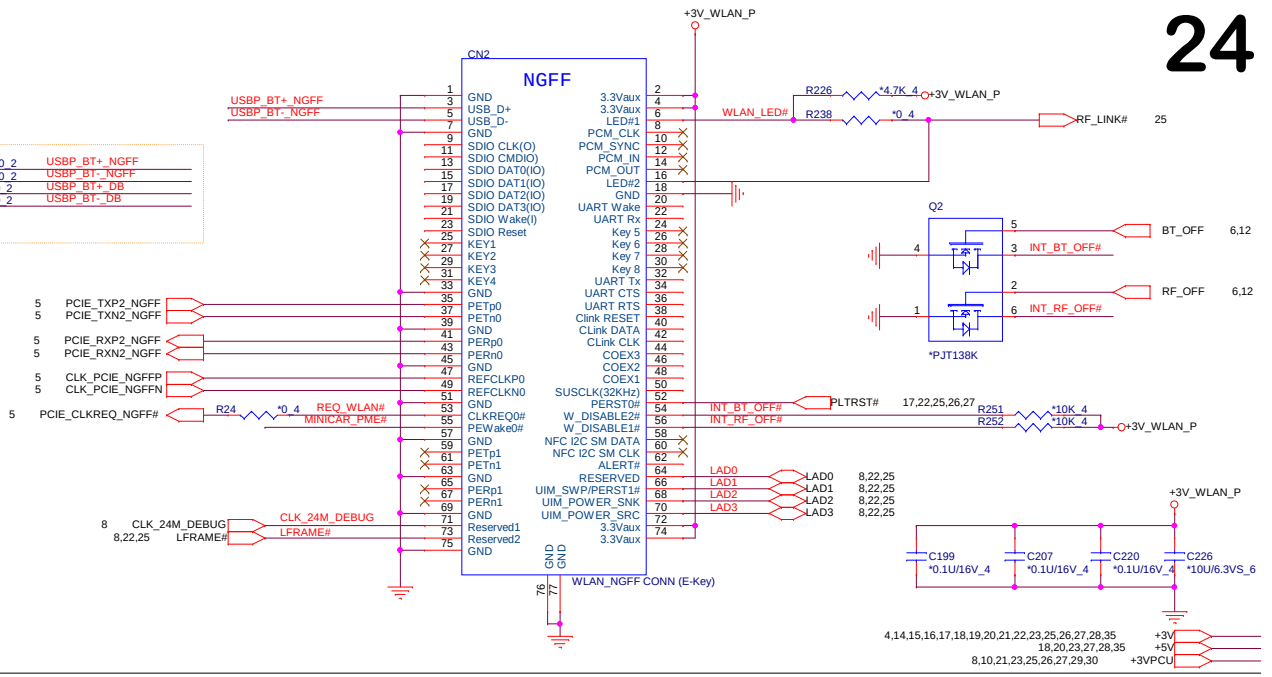




Support Wake Function(Reserve)

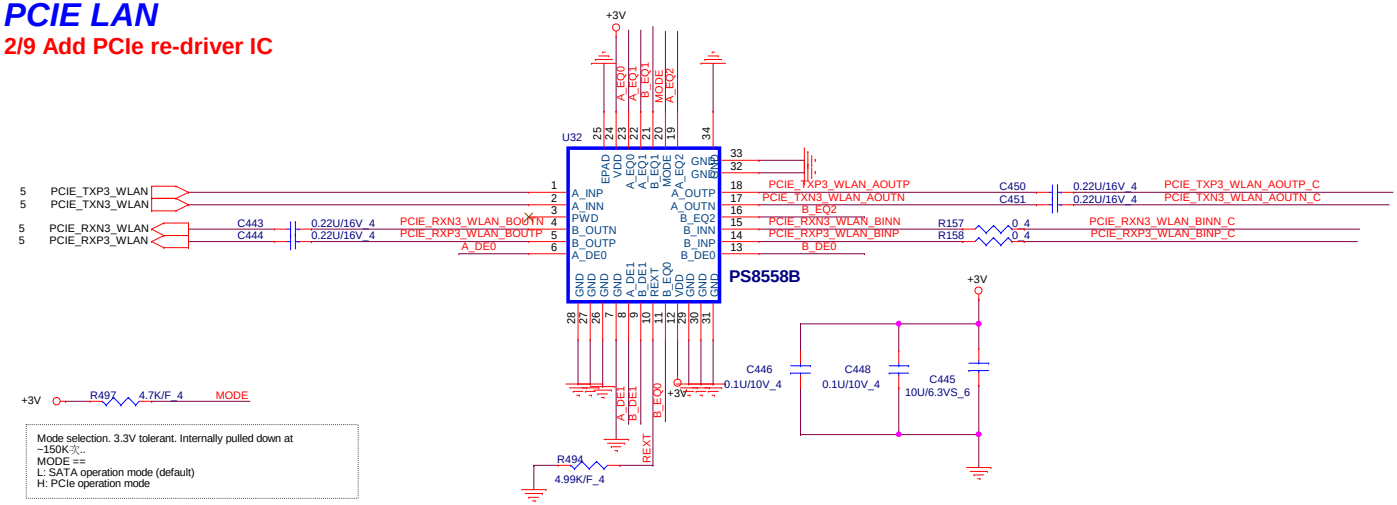


For EMI Suggestion



PCIE LAN

2/9 Add PCIe re-driver IC



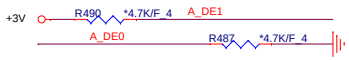
Mode selection. 3.3V tolerant. Internally pulled down at ~150K次..
MODE ==
L: SATA operation mode (default)
H: PCIe operation mode

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K
[A_EQ2,A_EQ1,A_EQ0] ==

LLL:	13.3dB(default)
LHL:	10.1dB
HLL:	14.7dB
HHL:	16.5dB
LLH:	14dB
LHH:	8dB
HLH:	11.9dB
HHH:	15.6dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K
[B_EQ2,B_EQ1,B_EQ0] ==

LLL:	13.3dB(default)
LHL:	10.1dB
HLL:	14.7dB
HHL:	16.5dB
LLH:	14dB
LHH:	8dB
HLH:	11.9dB
HHH:	15.6dB

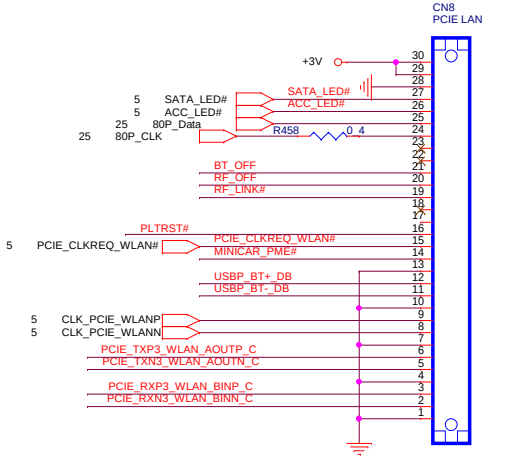


Programmable output de-emphasis level setting for channel A .
A_DE0: internally pulled up at ~150K; A_DE1 internally pulled down at ~150K
[A_DE1,A_DE0] ==

LL:	-2dB
HL:	-7.5dB
LH:	-3.5dB (default)
HH:	-6dB

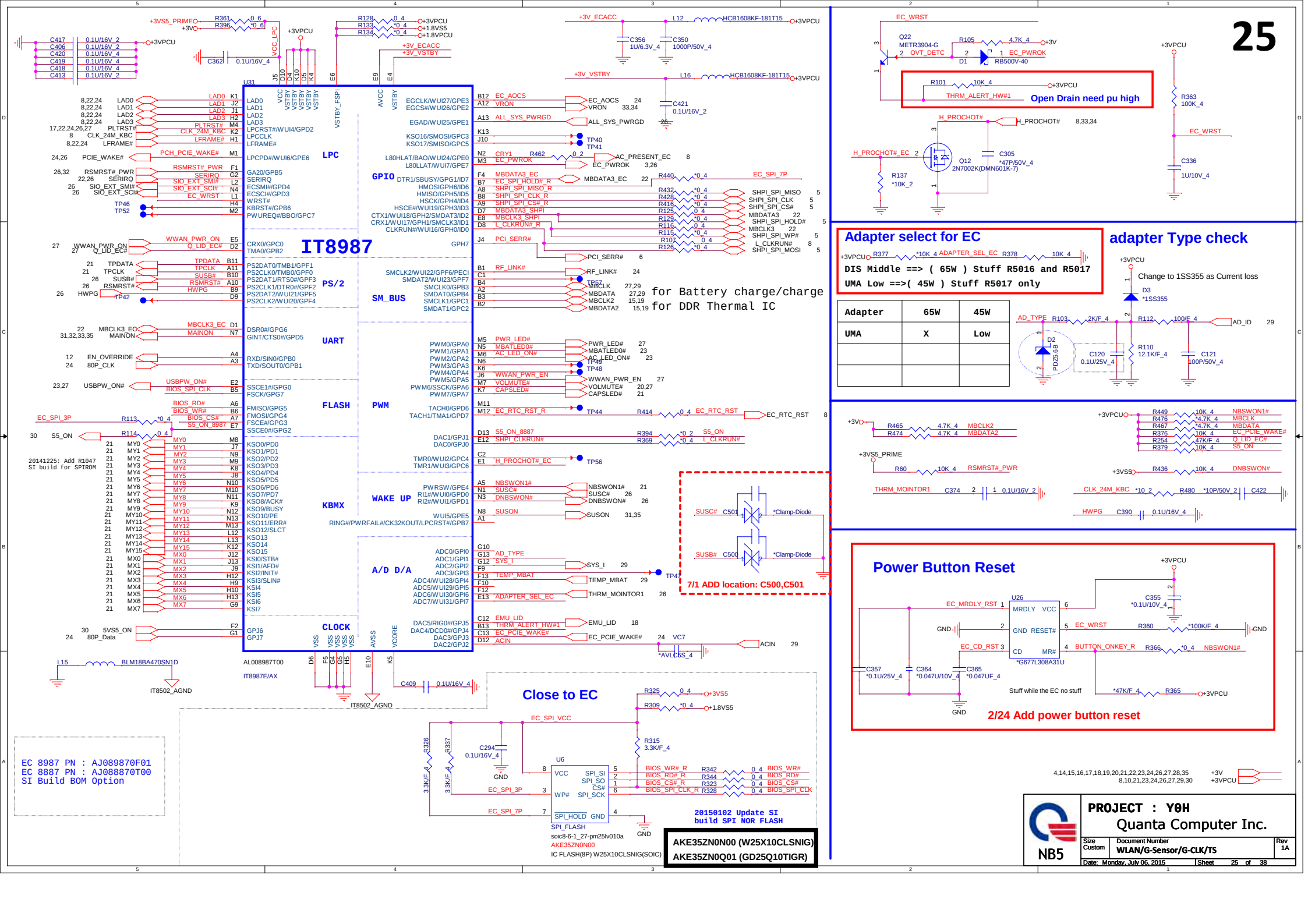
Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K; B_DE1 internally pulled down at ~150K
[B_DE1,B_DE0] ==

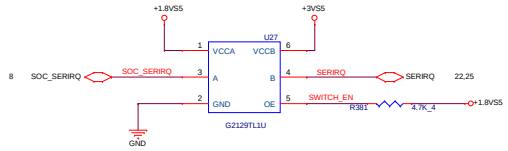
LL:	-2dB
HL:	-7.5dB
LH:	-3.5dB (default)
HH:	-6dB

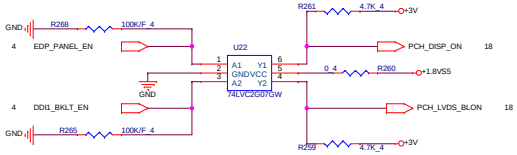


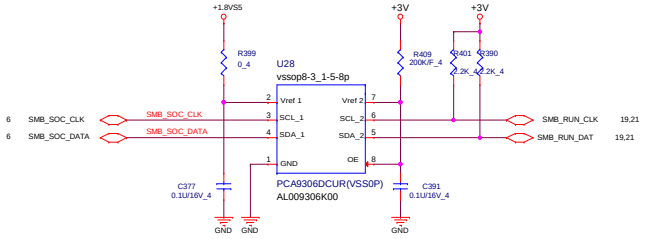
NB5	PROJECT : Y0H Quanta Computer Inc.	
Size	Document Number WLAN	Rev 1A
Date: Wednesday, July 08, 2015	Sheet 24 of 38	

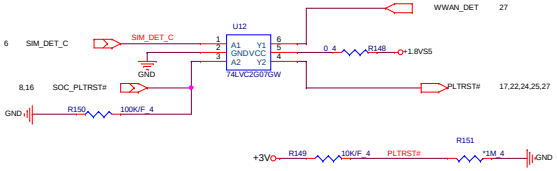
Chip power down. 3.3V tolerant. Internally pulled down at ~150K.
PWD ==
L: Normal operation (default)
H: Chip power down

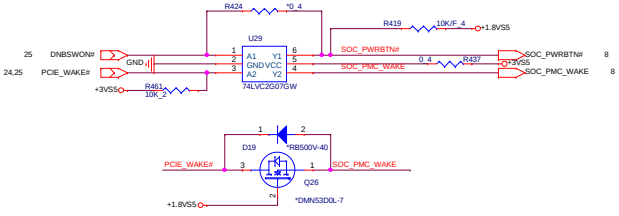

IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
for Battery charge/charge
for DDR Thermal IC
Close to EC
Open Drain need pu high
Adapter select for EC
DIS Middle ==> (65W) Stuff R5016 and R5017
UMA Low ==>(45W) Stuff R5017 only
Adapter | 65W | 45W
UMA | X | Low
adapter Type check
Change to 1SS355 as Current loss
Power Button Reset
2/24 Add power button reset
7/1 ADD location: C500,C501
20141225: Add R1047 SI build for SPIROM
EC 8987 PN : AJ089870F01
EC 8887 PN : AJ088870T00
SI Build BOM Option
20150102 Update SI build SPI NOR FLASH
AKE35ZN0N00 (W25X10CLSNIG)
AKE35ZN0Q01 (GD25Q10TIGR)
PROJECT : Y0H
Quanta Computer Inc.
NB5
WLAN/G-Sensor/G-CLK/TS
Date: Monday, July 06, 2015
Sheet 25 of 38

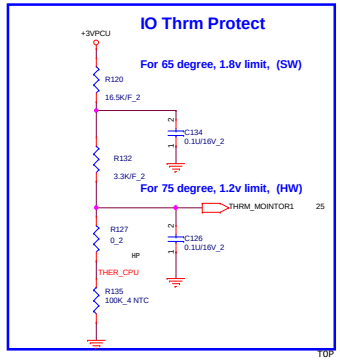


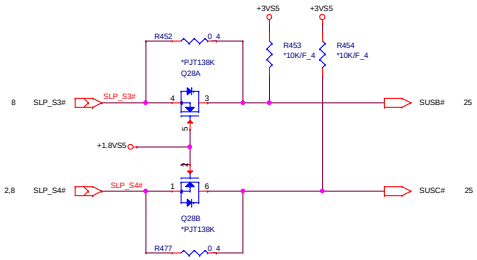


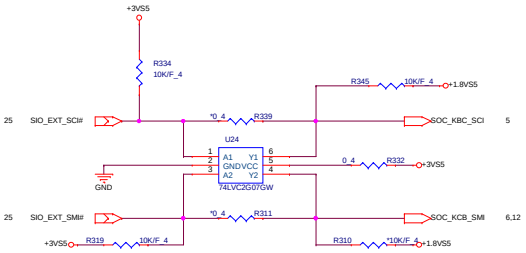


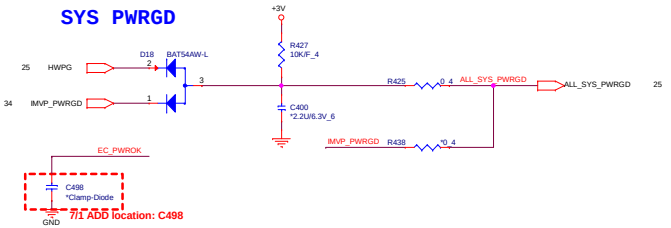


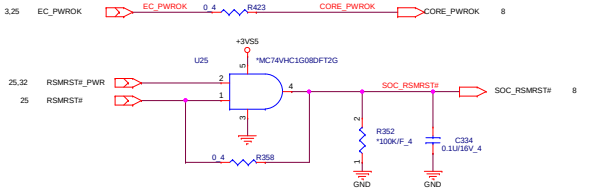


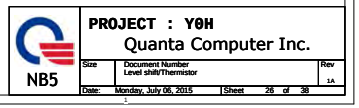






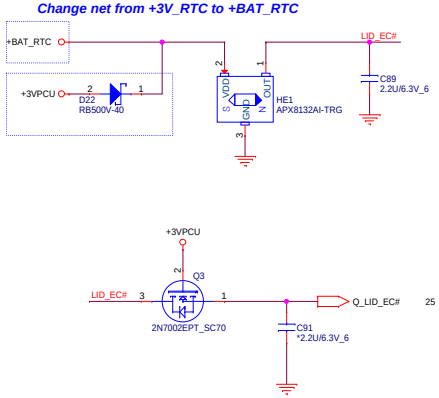




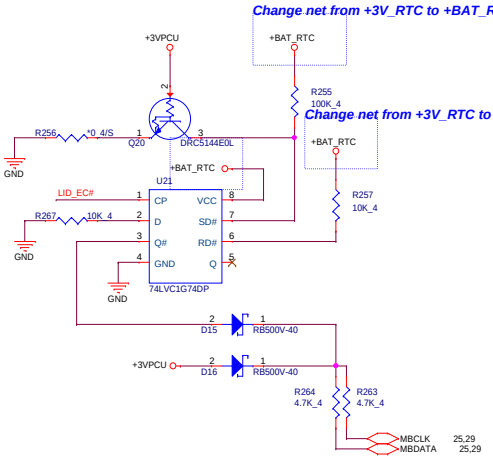


LID

Change net from +3V_RTC to +BAT_RTC



Change net from +3V_RTC to +BAT_RTC



Change net from +3V_RTC to +BAT_RTC

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

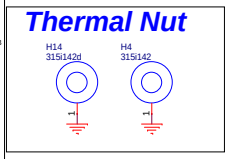
Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

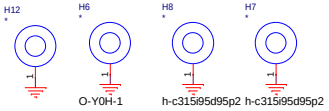
[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

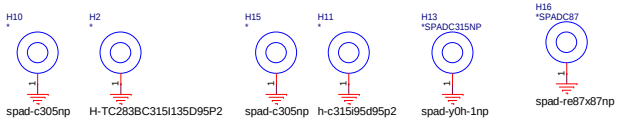
Daughter Board

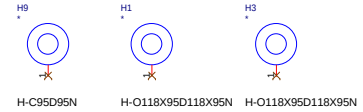
HOLE

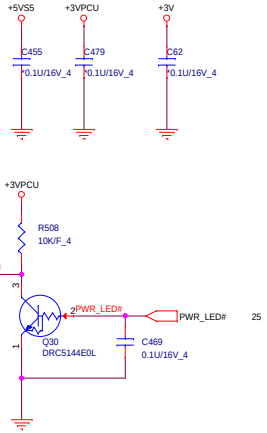
Thermal Nut

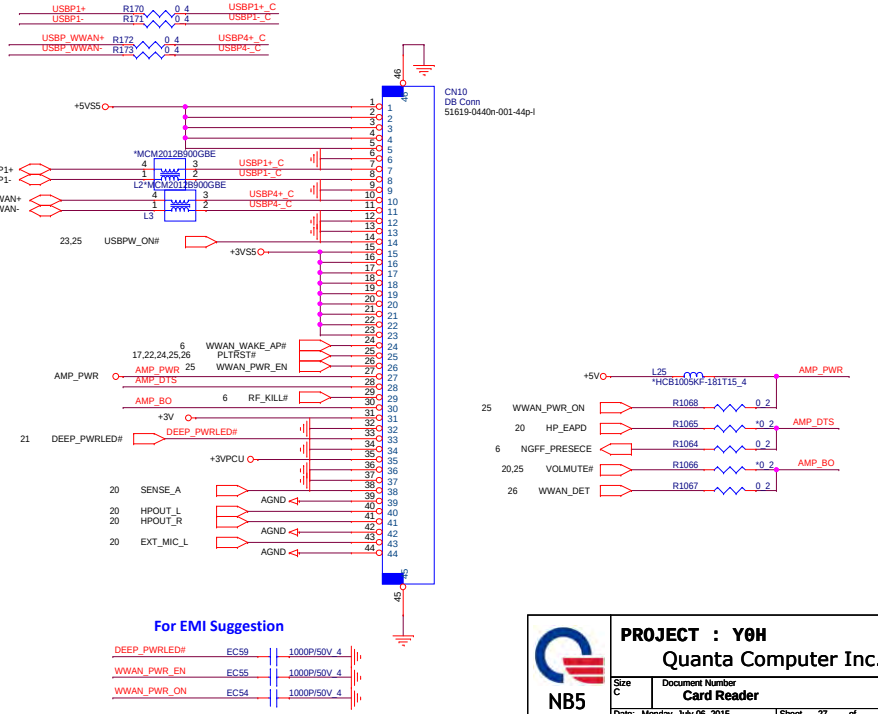












For EMI Suggestion

PROJECT : Y0H
Quanta Computer Inc.

Size	Document Number	Rev
C	Card Reader	1A

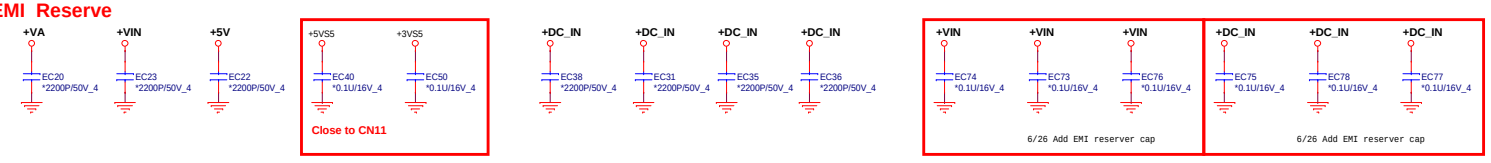
NB5

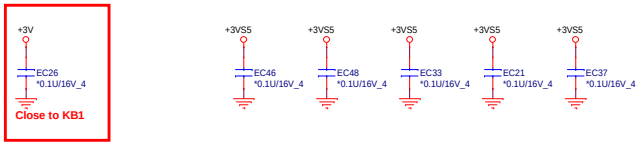
Date: Monday, July 06, 2015 | Sheet 27 of 38

I/O port definition

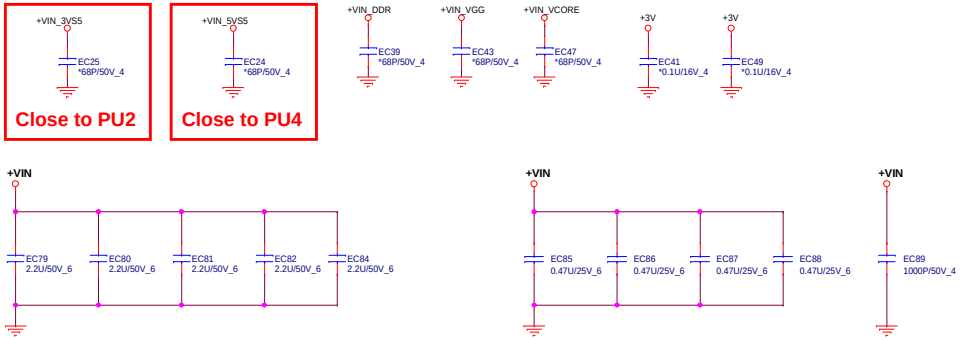
	Brasswell-M	Note
SATA Port0	HDD	
SATA Port1	ODD	
PCIE Port0	Card reader	
PCIE Port1		
PCIE Port2		
PCIE Port3	WIFI	
USB3.0 Port0	USB 2.0/3.0 Combo	
USB3.0 Port1		
USB3.0 Port2		
USB3.0 Port3		
USB2.0 Port0	USB 2.0/3.0 Combo	
USB2.0 Port1	USB 2.0	
USB2.0 Port2	Webcam	
USB2.0 Port3	BT	
USB2.0 Port4	WWAN	

EMI Reserve

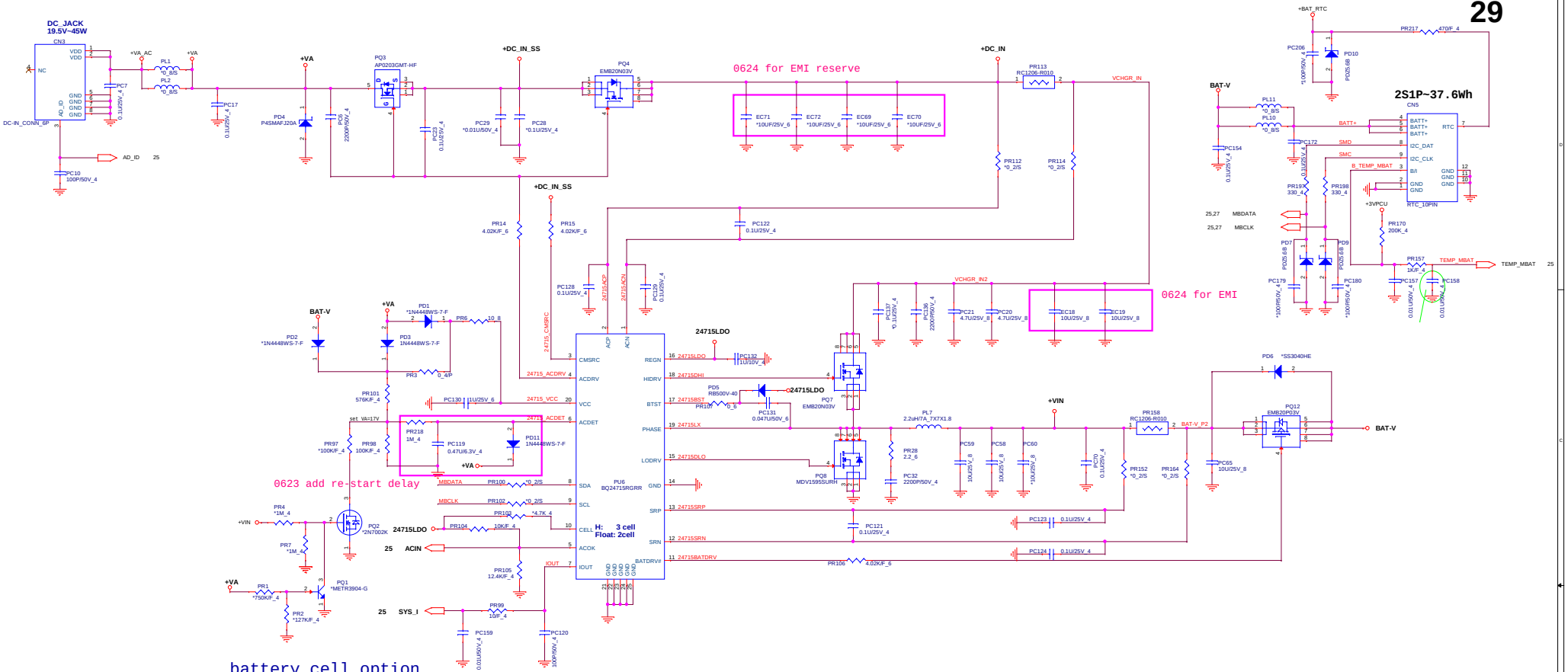




RF Reserve



NB5	PROJECT : Y0H Quanta Computer Inc.	
	Size:	Document Number: USB20 HUB GL850G-50 — Rev: 1A
	Date: Monday, July 06, 2015	Sheet 28 of 38

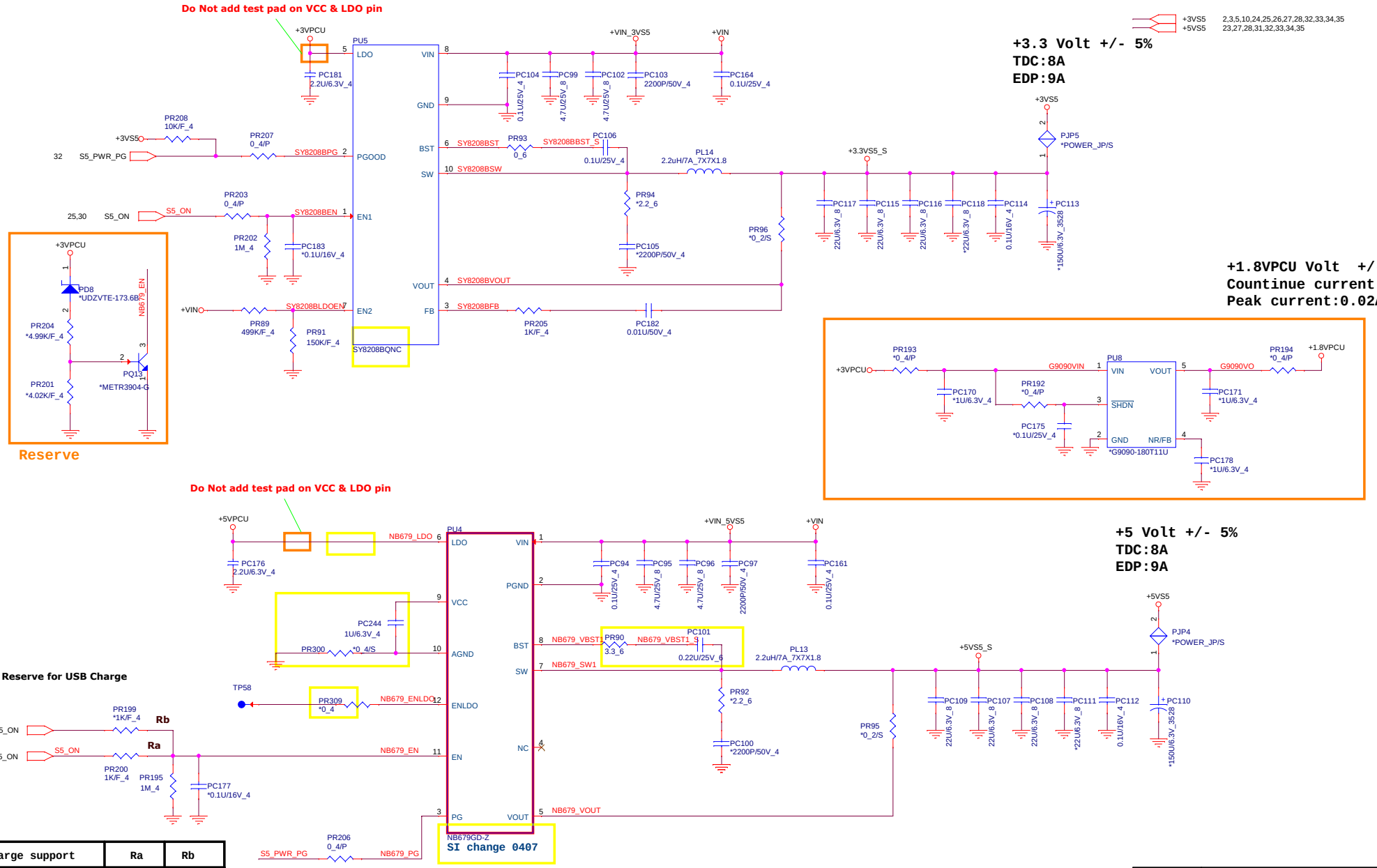


battery cell option

	2-cell	3-cell
PR26	un-stuff	stuff

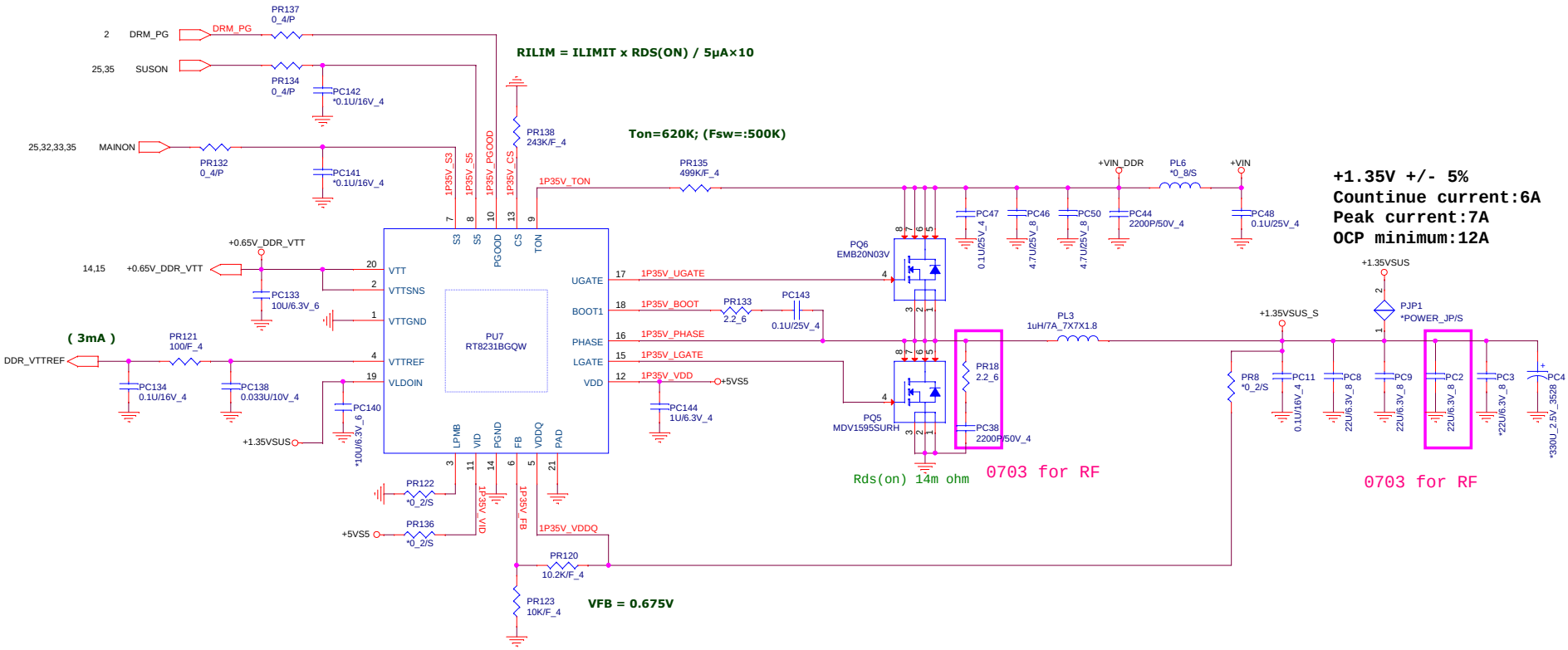
PROJECT : Y0H
Quanta Computer Inc.
NB5
Size: Custom
Document Number: Charger(BQ24715)
Rev: 1A
Date: Monday, July 06, 2015
Sheet 29 of 38

DC/DC +3VS5/+5VS5

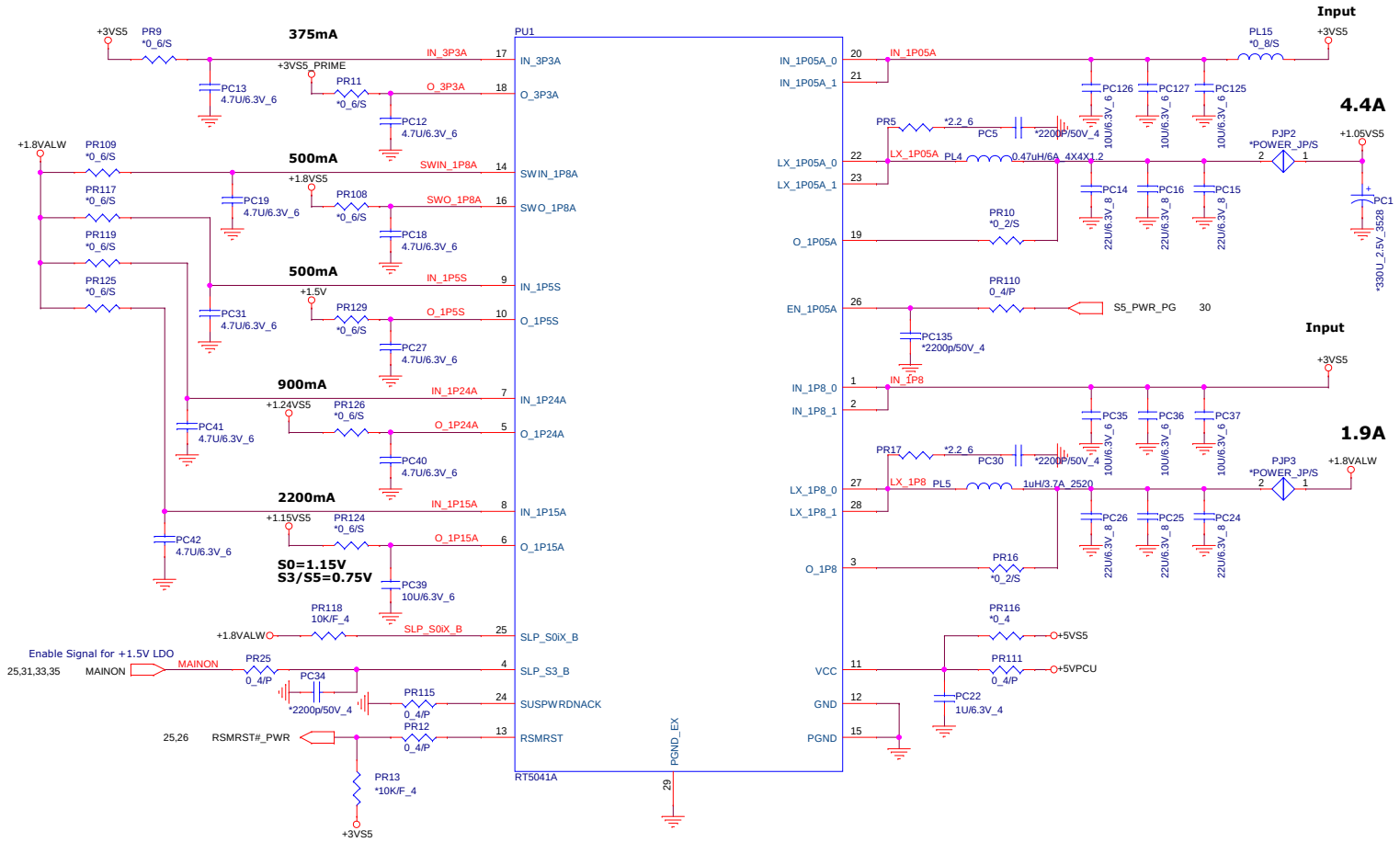


USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

NB5	PROJECT : Y0H Quanta Computer Inc.	
Size Custom	Document Number 3/5VPCU(SY8208B/SY8208C)	Rev 1A
Date: Monday, July 06, 2015	Sheet 30 of 38	



PROJECT :	Y0H
	Quanta Computer Inc.
Size	Document Number: DDR3 (RT8231B)/1.8VS5
Rev	1A
Date:	Monday, July 06, 2015
Sheet	31 of 38
NB5	



+3VS5 2,3,5,10,24,25,26,27,28,30,33,34,35
+1.8VALW 35
+1.8VS5 4,5,6,7,8,10,12,16,18,22,25,26,33
+3VS5_PRIME 10,22,25
+1.5V 10,20
+1.24VS5 10
+1.15VS5 9,32
+5VPCU 30,32
+1.05VS5 8,9,33,34
+1.15VS5 9,32
+5VPCU 30,32
+1.8V 4,5,35

NB5

PROJECT : Y0H
Quanta Computer Inc.

Size	Document Number	Rev
	1.05VS5/1.8VS5/1.24VS5	1A

Date: Monday, July 06, 2015 Sheet 32 of 38

+3VS5 2,3,5,10,24,25,26,27,28,30,32,34,35
+1.05VS5 8,9,32,34
+5VS5 23,27,28,30,31,32,34,35
+VGG 9
+1.8VS5 4,5,6,7,8,10,12,16,18,22,25,26,32
+VIN 18,28,29,30,31,34

Close to CPU

+VGG Volt +/- 5%
Imax:13A
OCP:16.64A
LL=0
VBOOT=1V

0625 For IC performace

Fsw=:600KHz

Rds(on) 4.2m ohm

0625 move back to power side

For Acoustic

Place close with VCORE Inductor B=4250

14A for ICCMAX=1V

Vref=0.6V

0625 For IC performace

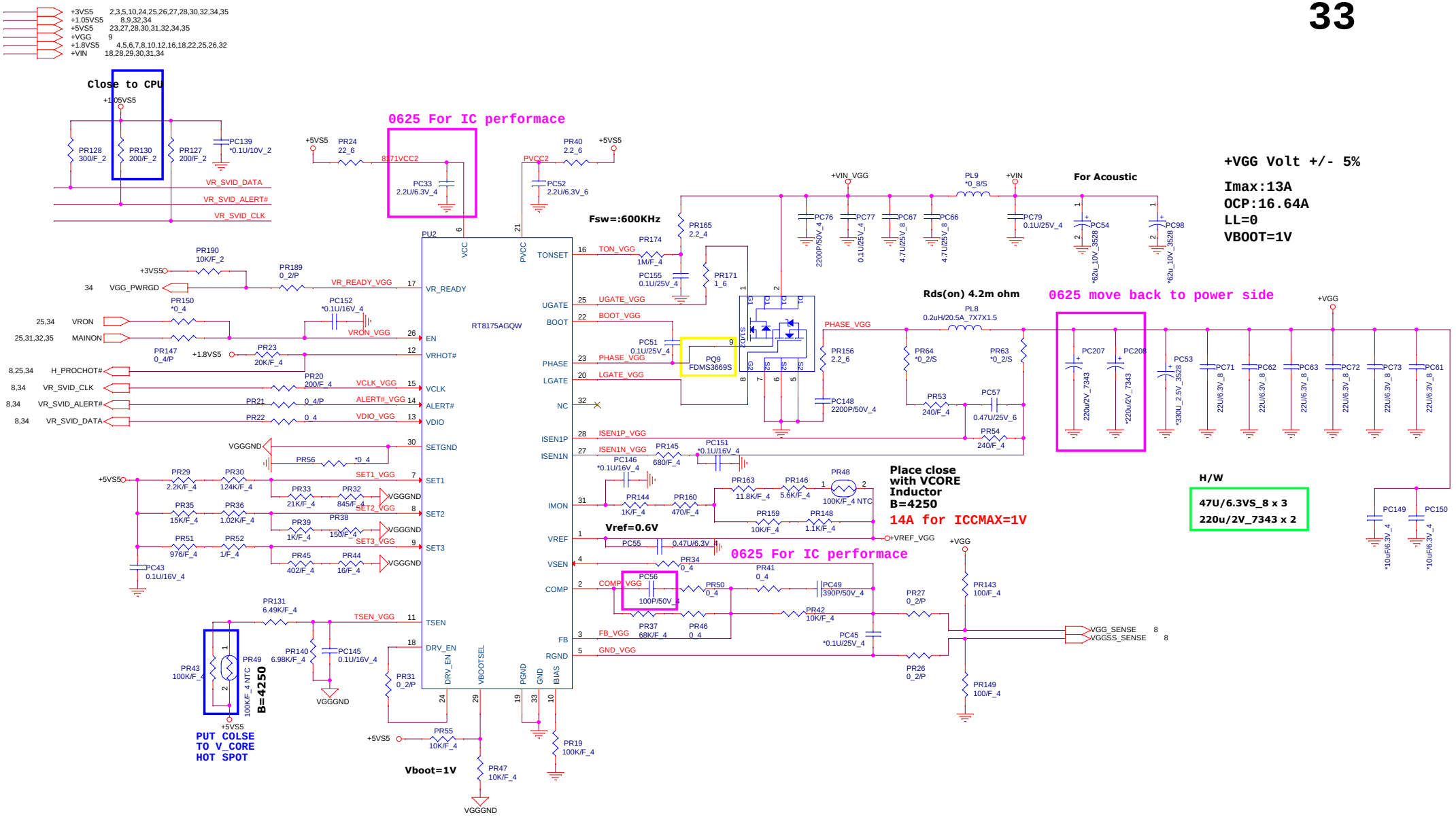
H/W
47U/6.3VS_8 x 3
220u/2V_7343 x 2

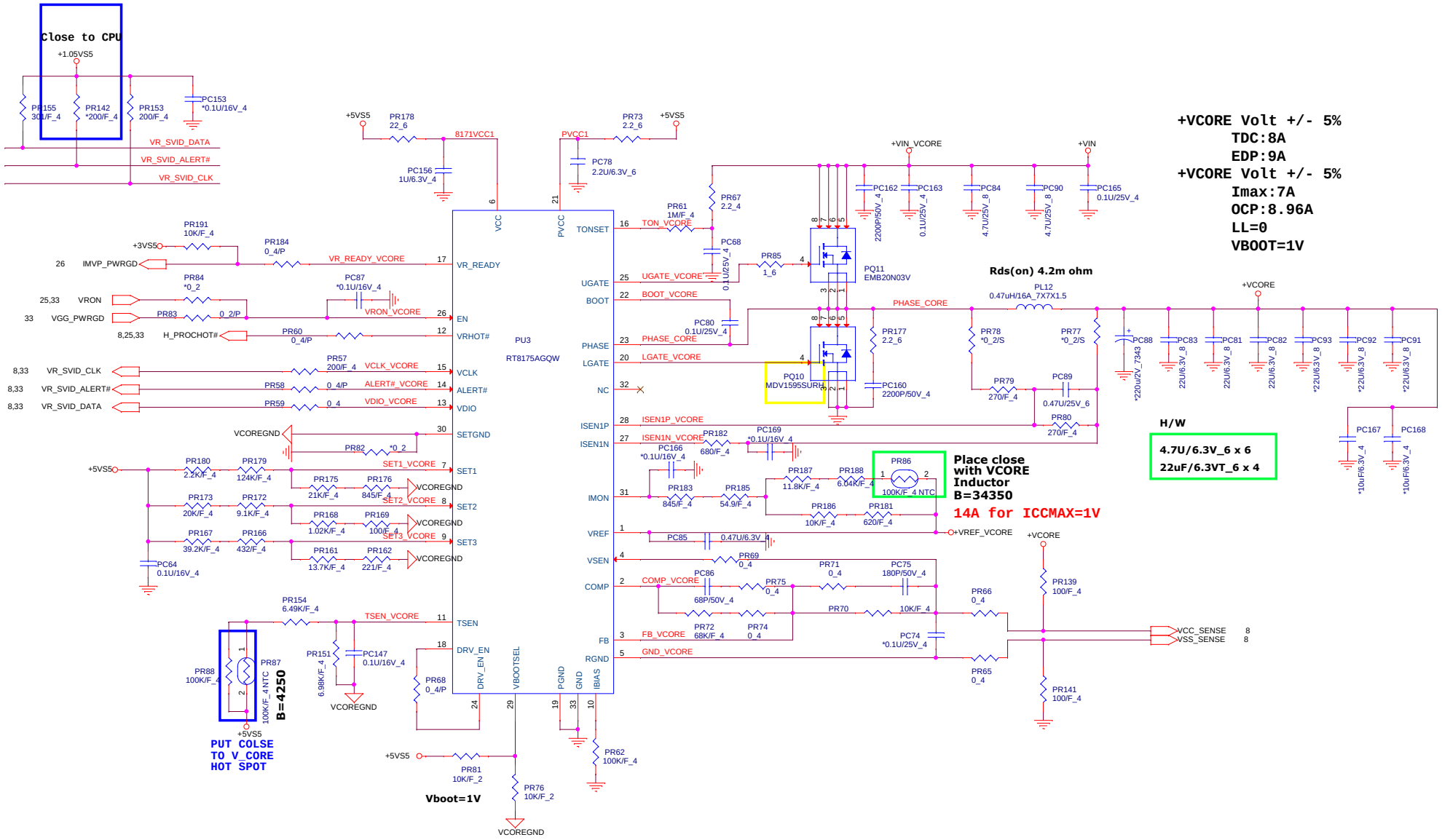
PUT COLSE TO V_CORE HOT SPOT

B=4250

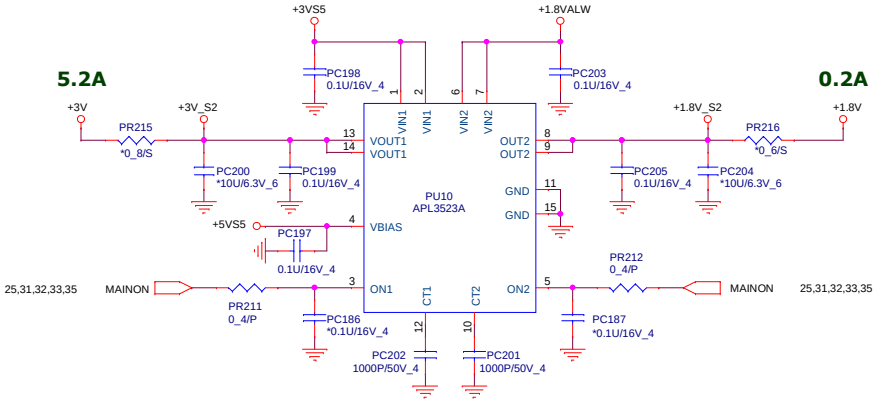
Vboot=1V

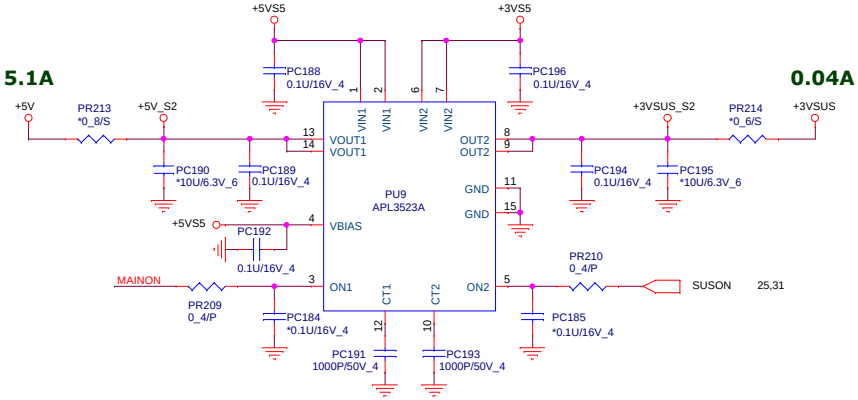
RT8175AGQW





NB5	PROJECT : Y0H Quanta Computer Inc.	
	Size: Document Number: +VCC CORE (RT8171A)	Rev: 1A
	Date: Monday, July 06, 2015	Sheet 34 of 38





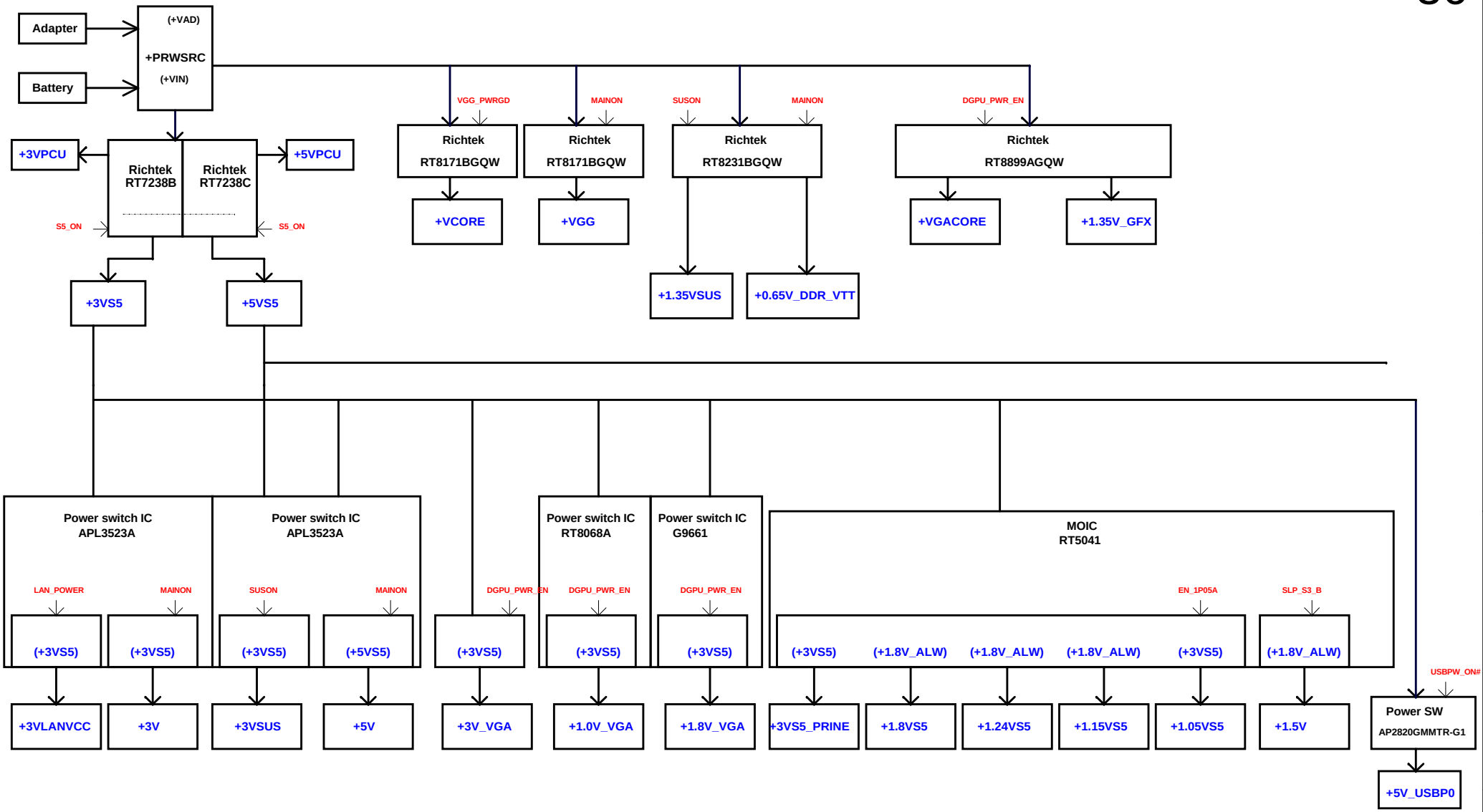
4,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28 +3V
18,20,23,27,28 +5V
2,3,5,10,24,25,26,27,28,30,32,33,34 +3VS5
23,27,28,30,31,32,33,34 +5VS5
21 +3VSUS

NB5

PROJECT : Y0H

Quanta Computer Inc.

Size	Document Number	Rev
	Dis-charge IC (G5934RZ1U)	1A
Date: Monday, July 06, 2015	Sheet 35 of 38	

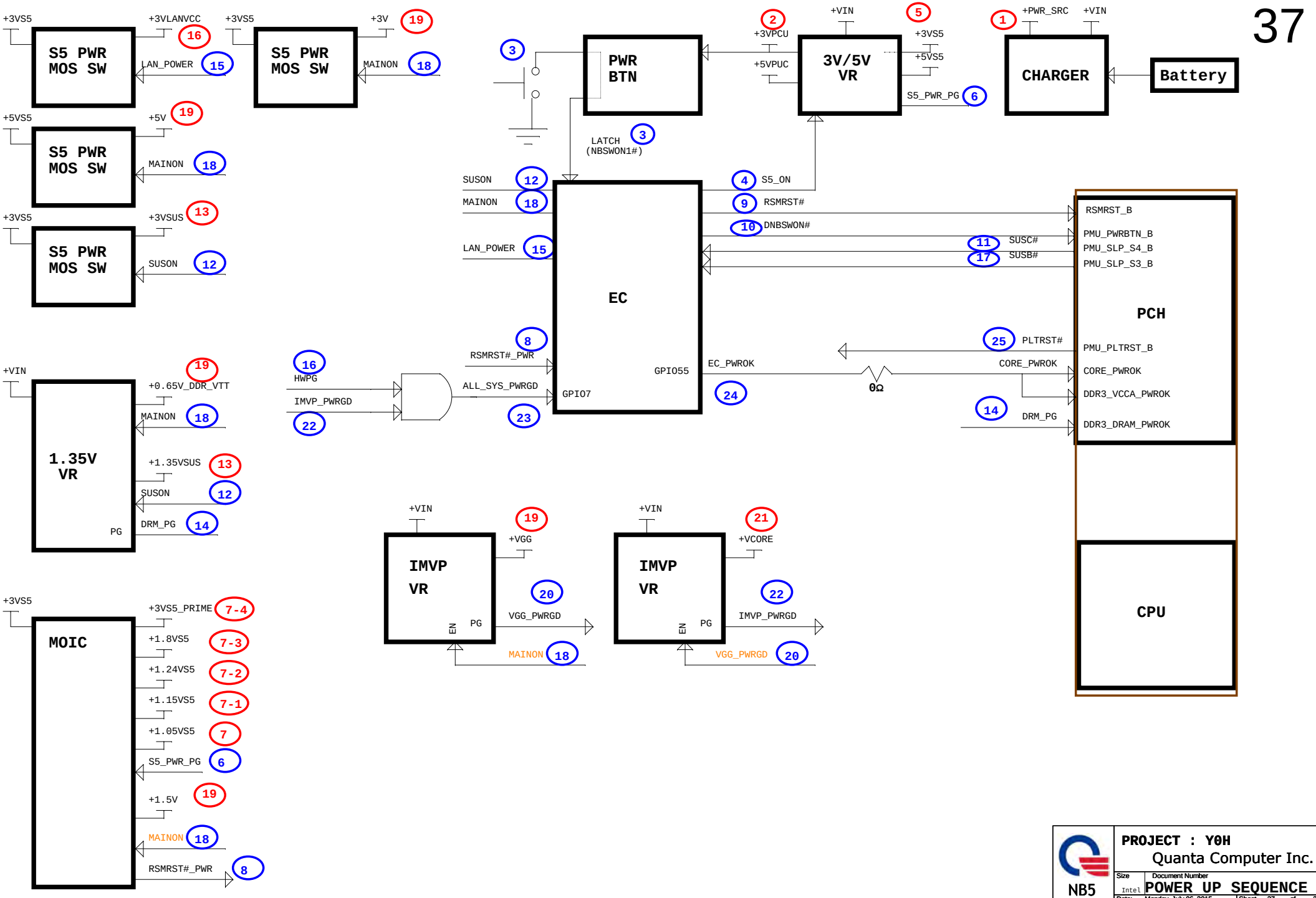


NB5

PROJECT : Y0H
Quanta Computer Inc.

Size	Document Number	Rev
	Power Block Diagram	1A

Date: Monday, July 06, 2015 Sheet 36 of 38



NB5	PROJECT : Y0H Quanta Computer Inc.		
	Size: Intel	Document Number: POWER UP SEQUENCE	Rev: 1A
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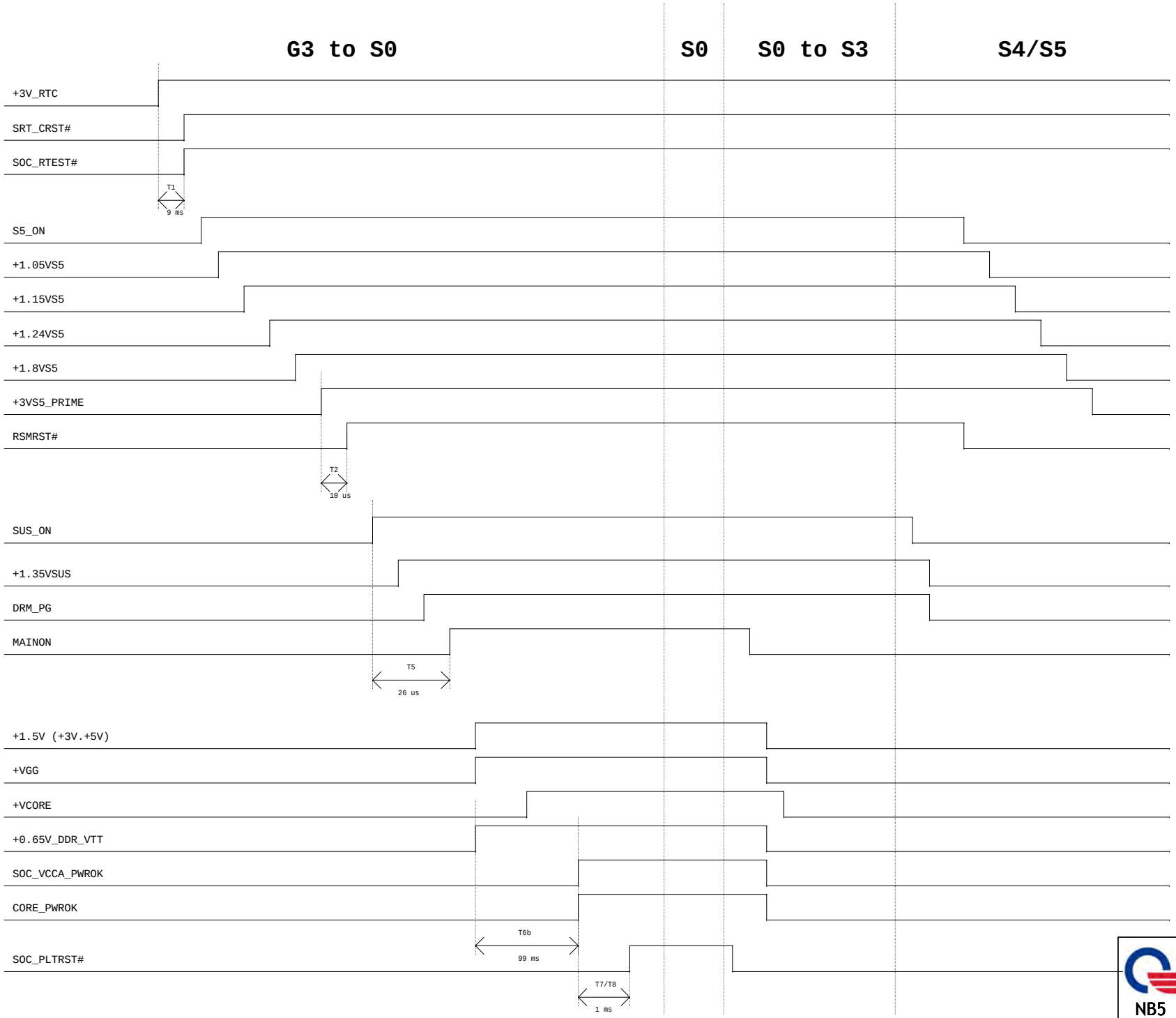

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