

Compal confidential

Schematics Document

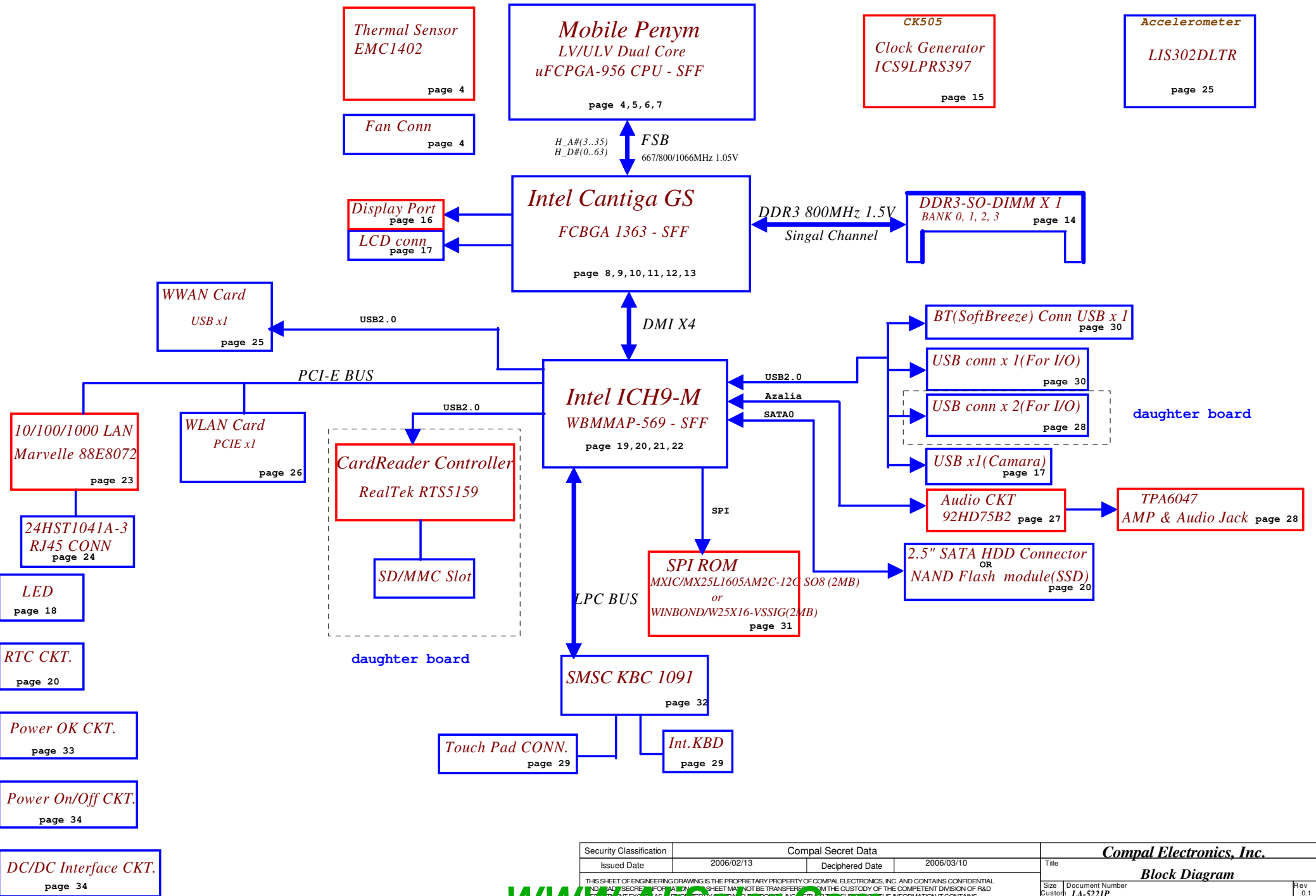
Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

Fossil

2009-02-03

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Fossil

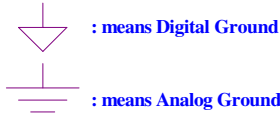


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Voltage Rails (O MEANS ON X MEANS OFF)

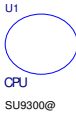
<div>power plane</div> <div>State</div>	+B +3VL	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

ULV723@ mean CPU ULV723 (U1) for L01
SU9300@ mean CPU SU9300 (U1) for L02



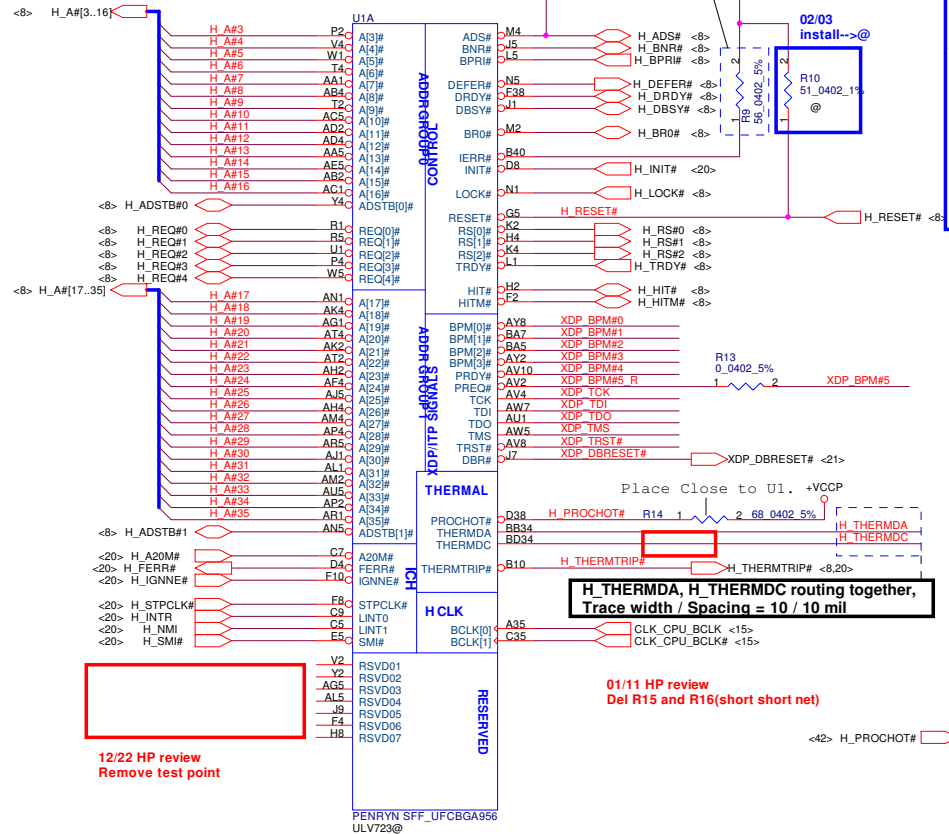
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

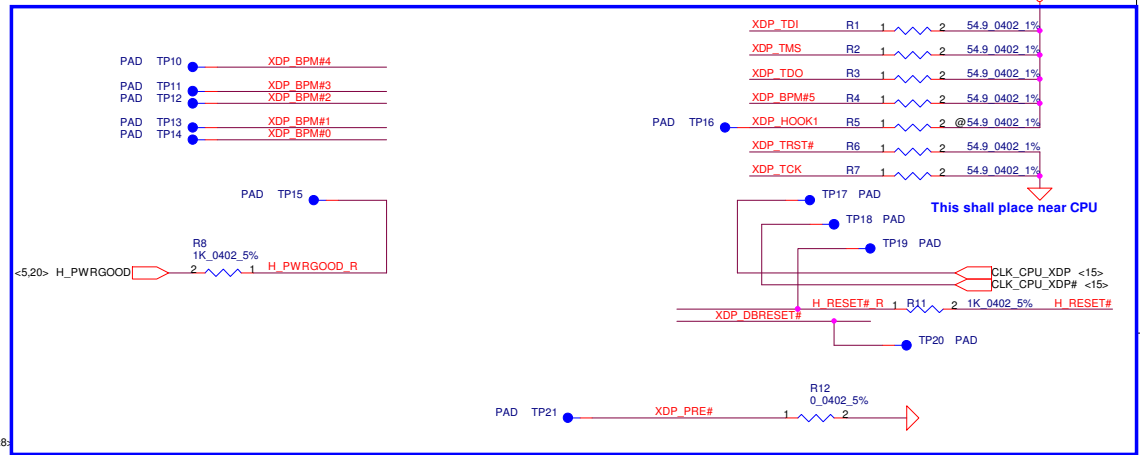
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

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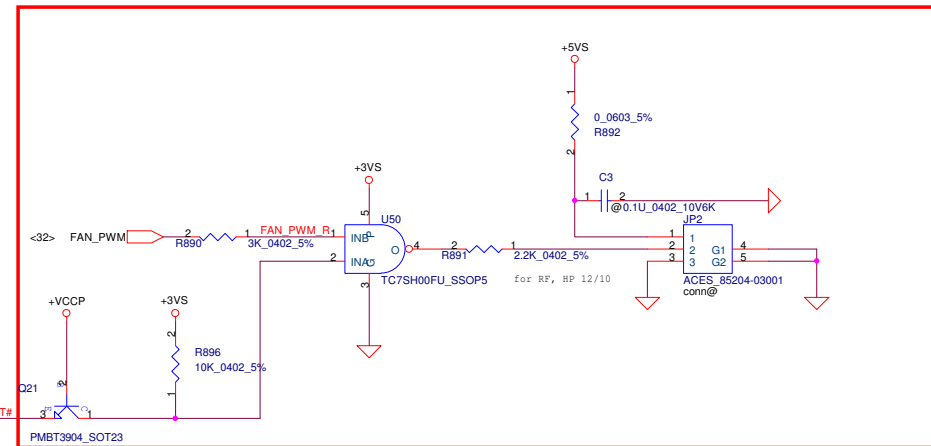


XDP Connector

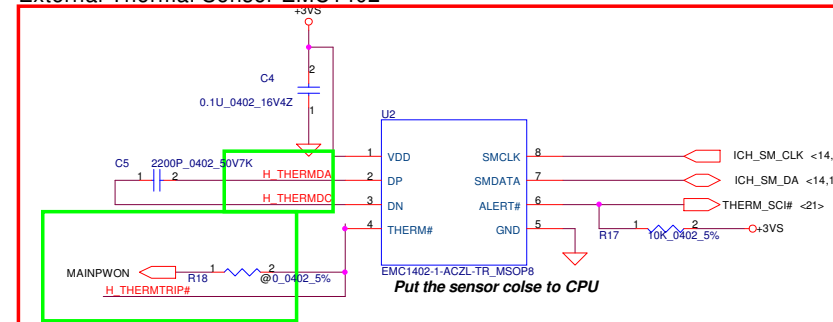


PWM Fan Control circuit

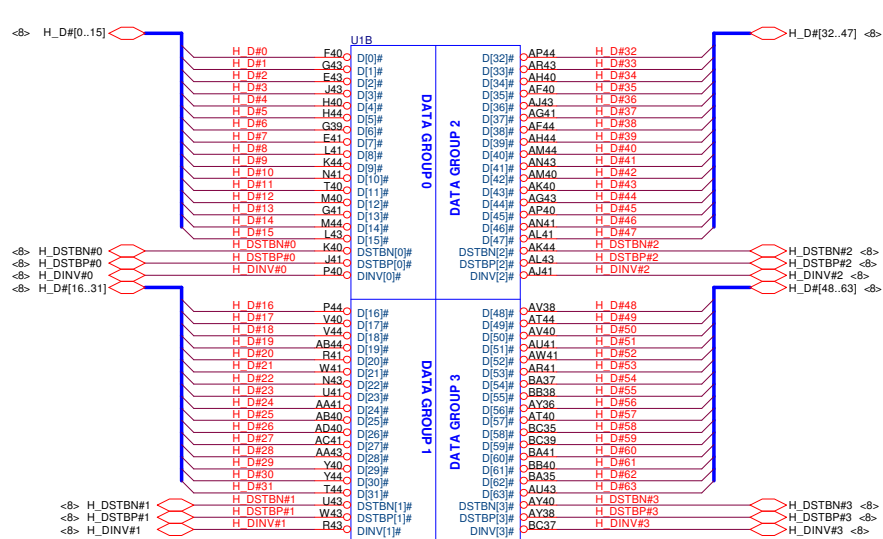
12/22 Follow consumer design



External Thermal Sensor EMC1402



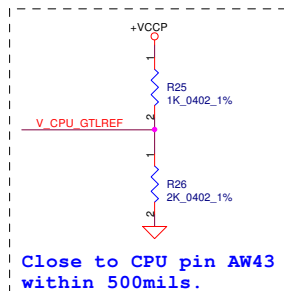
Security Classification	Compal Secret Data	Title	Compal Electronics, Inc.		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Penryn(1/3)-AGTL+/ITP-XDP	
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12/17 HP review
Remove test point

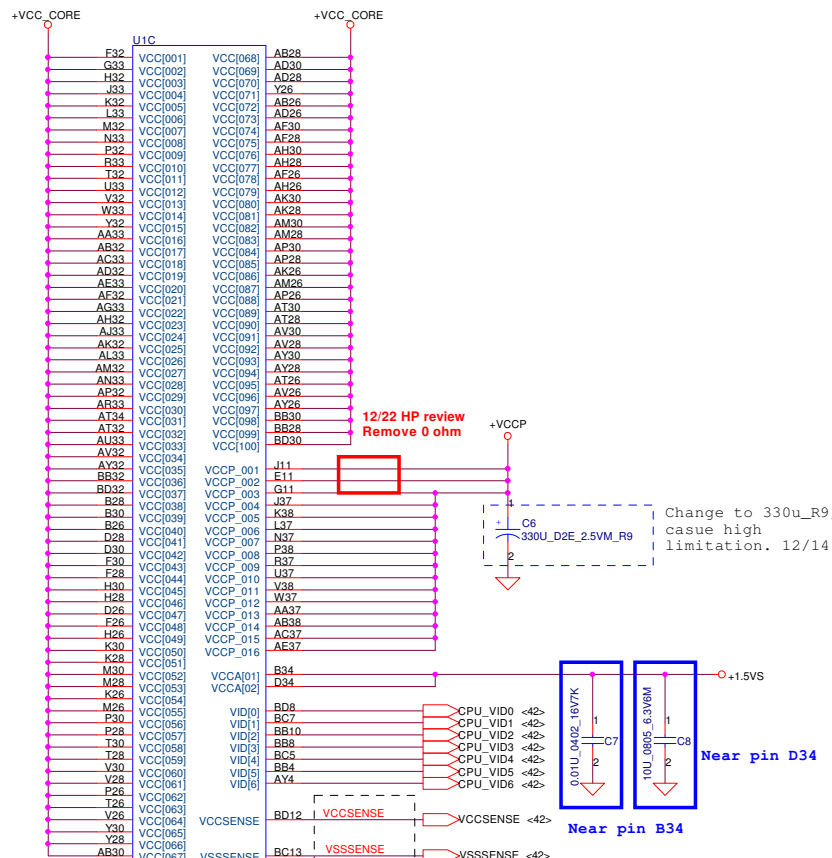
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

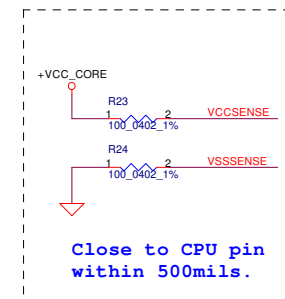


12/22 HP review
Remove test point

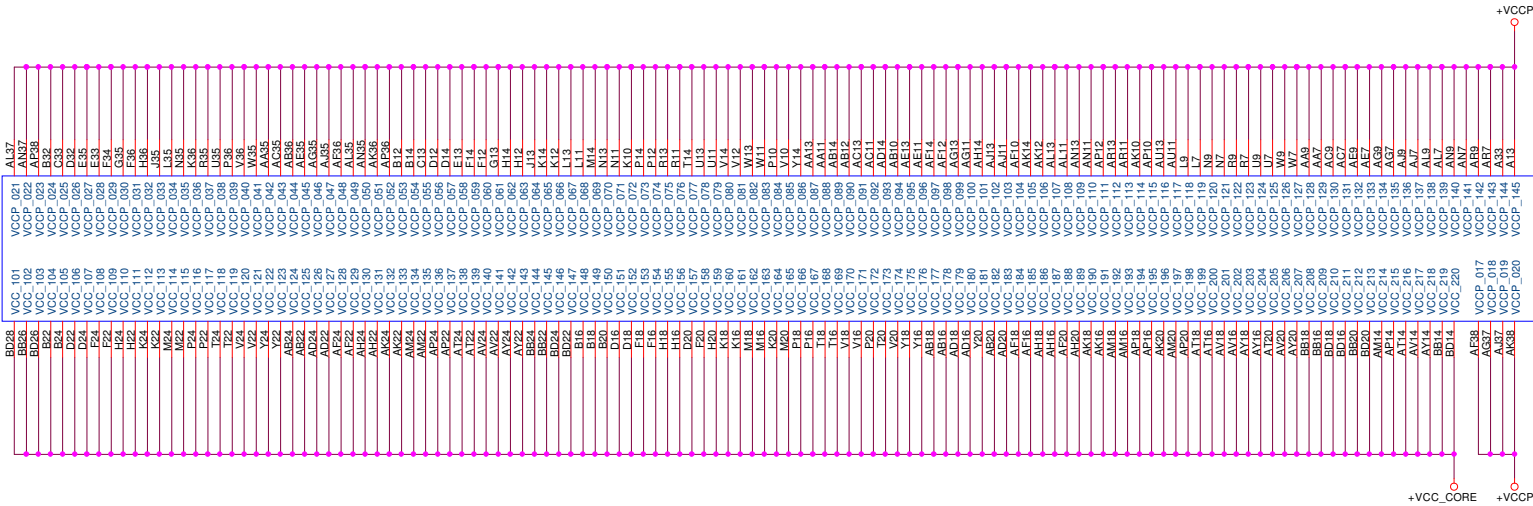
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



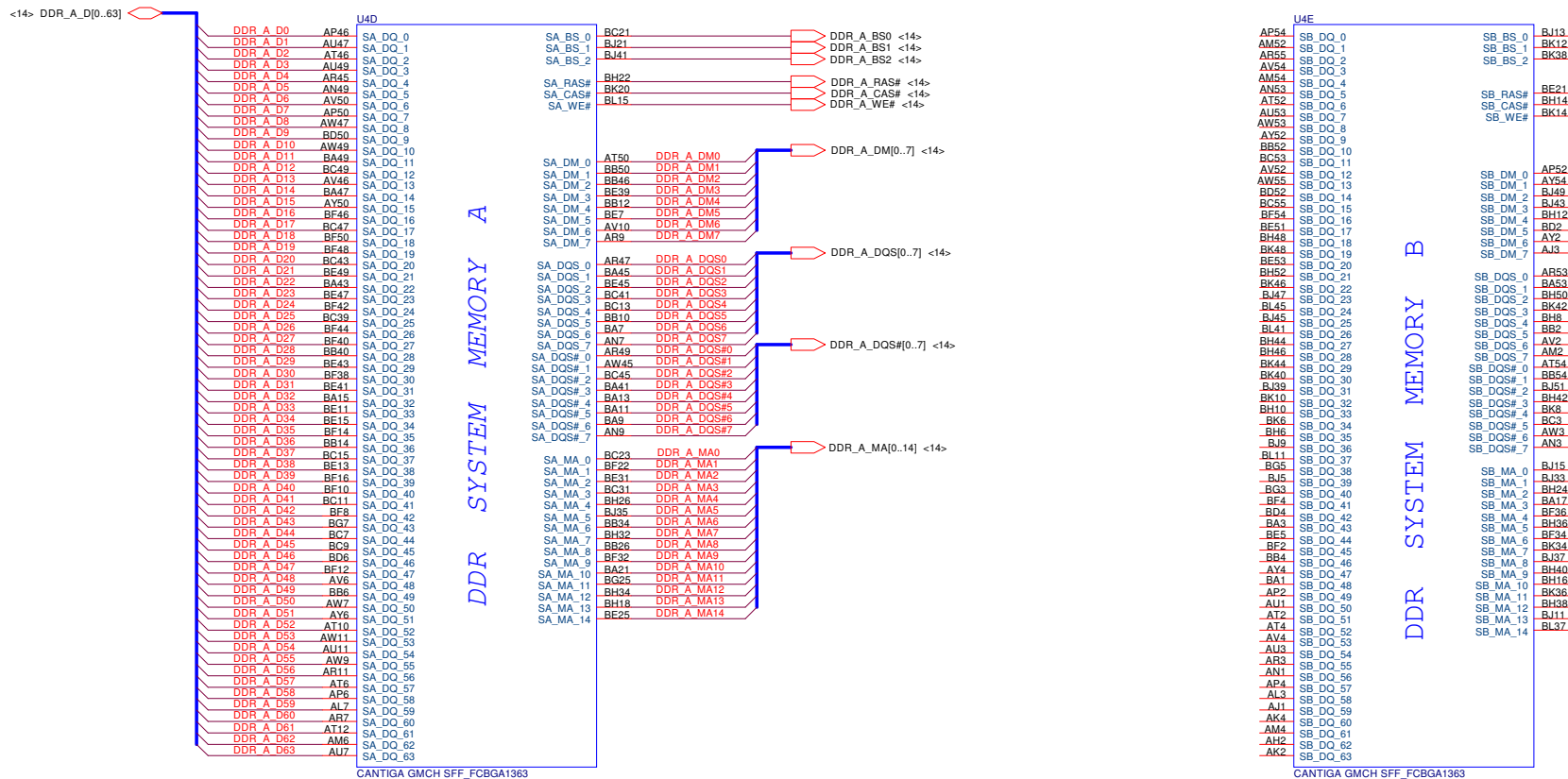
ULV723@



U1F
PENRYN SFF_UFCBGA956

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U1D	U1E
B42	VSS1001
F44	VSS1002
D42	VSS1003
F42	VSS1004
H42	VSS1005
K42	VSS1006
M42	VSS1007
P42	VSS1008
T42	VSS1009
V42	VSS1010
Y42	VSS1011
AB42	VSS1012
AD42	VSS1013
AF42	VSS1014
AH42	VSS1015
AK42	VSS1016
AM42	VSS1017
AP42	VSS1018
AT42	VSS1019
AV44	VSS1020
AY44	VSS1021
BA43	VSS1022
BB42	VSS1023
CB42	VSS1024
CC42	VSS1025
CD42	VSS1026
CE42	VSS1027
CF42	VSS1028
CG42	VSS1029
CH42	VSS1030
CI42	VSS1031
CJ42	VSS1032
CK42	VSS1033
CL42	VSS1034
CM42	VSS1035
CN42	VSS1036
CO42	VSS1037
CP42	VSS1038
CQ42	VSS1039
CR42	VSS1040
CS42	VSS1041
CT42	VSS1042
CU42	VSS1043
CV42	VSS1044
CW42	VSS1045
CX42	VSS1046
CY42	VSS1047
CA42	VSS1048
CB42	VSS1049
CC42	VSS1050
CD42	VSS1051
CE42	VSS1052
CF42	VSS1053
CG42	VSS1054
CH42	VSS1055
CI42	VSS1056
CJ42	VSS1057
CK42	VSS1058
CL42	VSS1059
CM42	VSS1060
CN42	VSS1061
CO42	VSS1062
CP42	VSS1063
CQ42	VSS1064
CR42	VSS1065
CS42	VSS1066
CT42	VSS1067
CU42	VSS1068
CV42	VSS1069
CW42	VSS1070
CX42	VSS1071
CY42	VSS1072
CA42	VSS1073
CB42	VSS1074
CC42	VSS1075
CD42	VSS1076
CE42	VSS1077
CF42	VSS1078
CG42	VSS1079
CH42	VSS1080
CI42	VSS1081
CJ42	VSS1082
CK42	VSS1083
CL42	VSS1084
CM42	VSS1085
CN42	VSS1086
CO42	VSS1087
CP42	VSS1088
CQ42	VSS1089
CR42	VSS1090
CS42	VSS1091
CT42	VSS1092
CU42	VSS1093
CV42	VSS1094
CW42	VSS1095
CX42	VSS1096
CY42	VSS1097
CA42	VSS1098
CB42	VSS1099
CC42	VSS1100
CD42	VSS1101
CE42	VSS1102
CF42	VSS1103
CG42	VSS1104
CH42	VSS1105
CI42	VSS1106
CJ42	VSS1107
CK42	VSS1108
CL42	VSS1109
CM42	VSS1110
CN42	VSS1111
CO42	VSS1112
CP42	VSS1113
CQ42	VSS1114
CR42	VSS1115
CS42	VSS1116
CT42	VSS1117
CU42	VSS1118
CV42	VSS1119
CW42	VSS1120
CX42	VSS1121
CY42	VSS1122
CA42	VSS1123
CB42	VSS1124
CC42	VSS1125
CD42	VSS1126
CE42	VSS1127
CF42	VSS1128
CG42	VSS1129
CH42	VSS1130
CI42	VSS1131
CJ42	VSS1132
CK42	VSS1133
CL42	VSS1134
CM42	VSS1135
CN42	VSS1136
CO42	VSS1137
CP42	VSS1138
CQ42	VSS1139
CR42	VSS1140
CS42	VSS1141
CT42	VSS1142
CU42	VSS1143
CV42	VSS1144
CW42	VSS1145
CX42	VSS1146
CY42	VSS1147
CA42	VSS1148
CB42	VSS1149
CC42	VSS1150
CD42	VSS1151
CE42	VSS1152
CF42	VSS1153
CG42	VSS1154
CH42	VSS1155
CI42	VSS1156
CJ42	VSS1157
CK42	VSS1158
CL42	VSS1159
CM42	VSS1160
CN42	VSS1161
CO42	VSS1162
CP42	VSS1163
CQ42	VSS1164
CR42	VSS1165
CS42	VSS1166
CT42	VSS1167
CU42	VSS1168
CV42	VSS1169
CW42	VSS1170
CX42	VSS1171
CY42	VSS1172
CA42	VSS1173
CB42	VSS1174
CC42	VSS1175
CD42	VSS1176
CE42	VSS1177
CF42	VSS1178
CG42	VSS1179
CH42	VSS1180
CI42	VSS1181
CJ42	VSS1182
CK42	VSS1183
CL42	VSS1184
CM42	VSS1185
CN42	VSS1186
CO42	VSS1187
CP42	VSS1188
CQ42	VSS1189
CR42	VSS1190
CS42	VSS1191
CT42	VSS1192
CU42	VSS1193
CV42	VSS1194
CW42	VSS1195
CX42	VSS1196
CY42	VSS1197
CA42	VSS1198
CB42	VSS1199
CC42	VSS1200
CD42	VSS1201
CE42	VSS1202
CF42	VSS1203
CG42	VSS1204
CH42	VSS1205
CI42	VSS1206
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CL42	VSS1209
CM42	VSS1210
CN42	VSS1211
CO42	VSS1212
CP42	VSS1213
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CS42	VSS1216
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CA42	VSS1223
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CG42	VSS1229
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CI42	VSS1231
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CK42	VSS1233
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CP42	VSS1238
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CR42	VSS1240
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CV42	VSS1244
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CX42	VSS1296
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CD42	VSS1351
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CL42	VSS1434
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CN42	VSS1436
CO42	VSS1437
CP42	VSS1438
CQ42	VSS1439
CR42	VSS1440
CS42	VSS1441
CT42	VSS1442
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CX42	VSS1446
CY42	VSS1447
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CB42	VSS1449
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CD42	VSS1451
CE42	VSS1452
CF42	VSS1453
CG42	VSS1454
CH42	VSS1455
CI42	VSS1456
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CM42	VSS1460
CN42	VSS1461
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CQ42	VSS1464
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CB42	VSS1474
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CD42	VSS1476
CE42	VSS1477
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CG42	VSS1479
CH42	VSS1480
CI42	VSS1481
CJ42	VSS1482
CK42	VSS1483
CL42	VSS1484
CM42	VSS1485
CN42	VSS1486
CO42	VSS1487
CP42	VSS1488
CQ42	VSS1489
CR42	VSS1490
CS42	VSS1491
CT42	VSS1492
CU42	VSS1493
CV42	VSS1494
CW42	VSS1495
CX42	VSS1496
CY42	VSS1497
CA42	VSS1498
CB42	VSS1499
CC42	VSS1500
CD42	VSS1501
CE42	VSS1502
CF42	VSS1503
CG42	VSS1504
CH42	VSS1505
CI42	VSS1506
CJ42	VSS1507
CK42	VSS1508
CL42	VSS1509
CM42	VSS1510
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CP42	VSS1513
CQ42	VSS1514
CR42	VSS1515
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CT42	VSS1517
CU42	VSS1518
CV42	VSS1519
CW42	VSS1520
CX42	VSS1521
CY42	VSS1522
CA42	VSS1523
CB42	VSS1524
CC42	VSS1525
CD42	VSS1526
CE42	VSS1527
CF42	VSS1528
CG42	VSS1529
CH42	VSS1530
CI42	VSS1531
CJ42	VSS1532
CK42	VSS1533
CL42	VSS1534
CM42	VSS1535

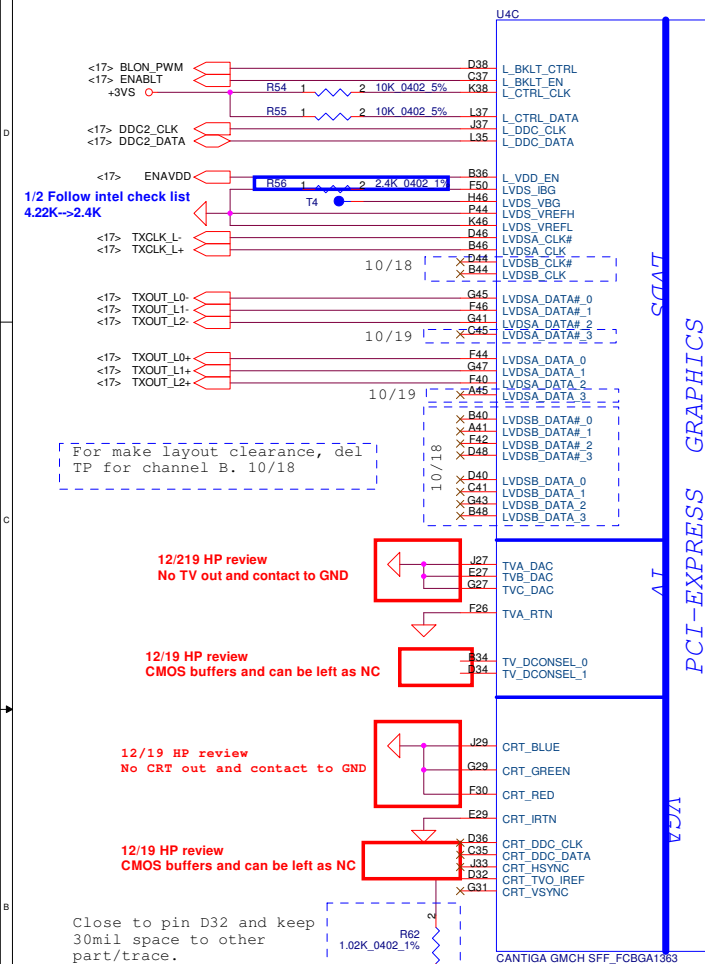


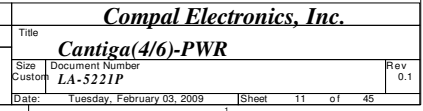
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Place R53 <500mils to U4 pin U45&T44.

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

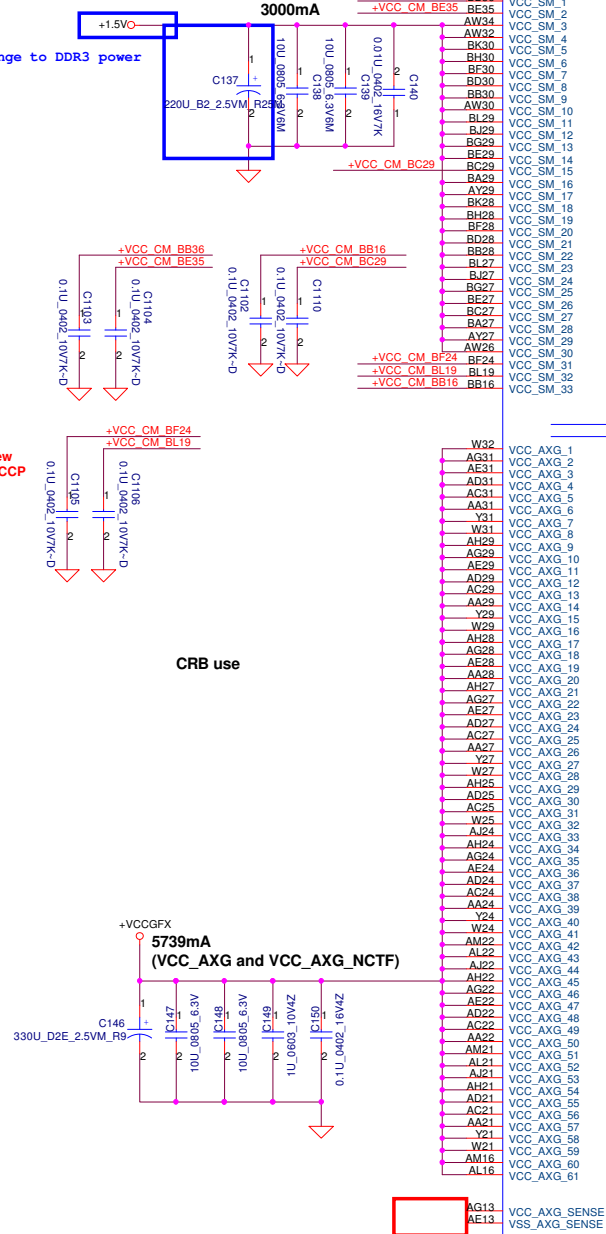
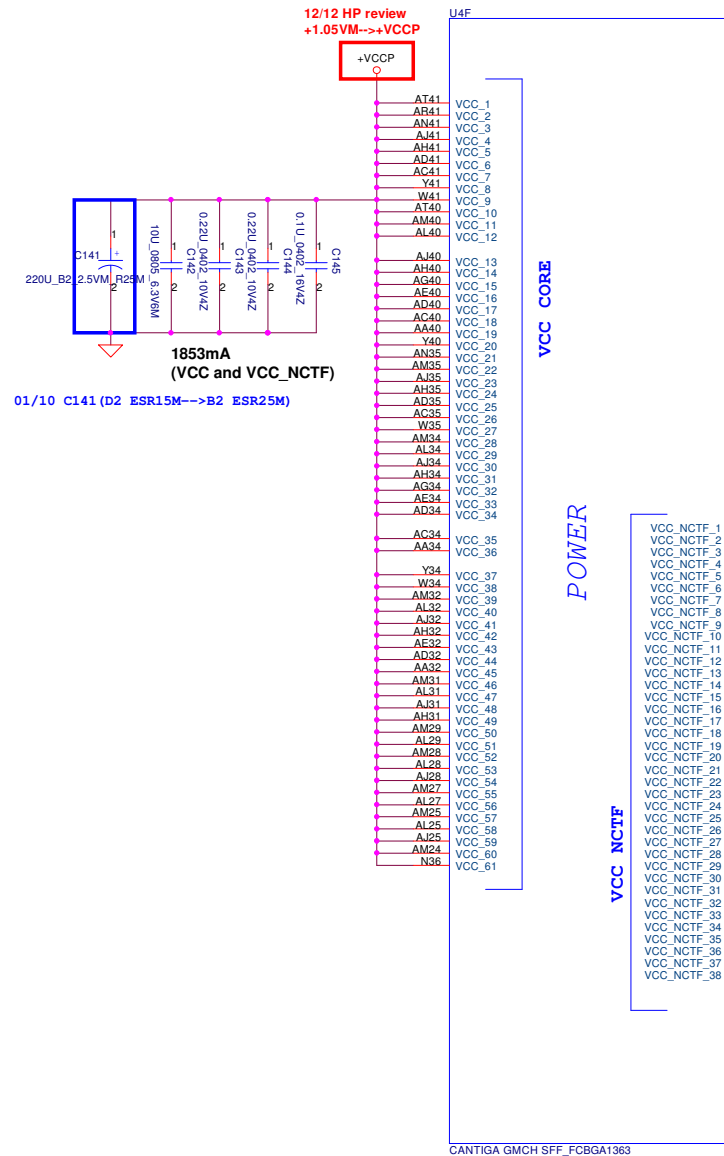




Extnal Graphic: 1210.34mA
Integrated Graphic: 1930.4mA

01/10 C137 (330u D2 ESR9M-->220u B2 ESR25M)

02/02 Change to DDR3 power



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				Document Number	0.1
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BA55	VSS_1	C43
AN55	VSS_2	A43
AJ55	VSS_3	BD42
US5	VSS_4	H42
AE55	VSS_5	BG41
AA55	VSS_6	AY41
U55	VSS_7	AU41
N55	VSS_8	AM41
BD54	VSS_9	AL41
BG53	VSS_10	AE41
AJ53	VSS_11	AA41
AE53	VSS_12	R41
AA53	VSS_13	M41
U53	VSS_14	E41
N53	VSS_15	BD40
J53	VSS_16	AU40
G53	VSS_17	AP40
E53	VSS_18	AN40
K52	VSS_19	W40
BG51	VSS_20	T40
BA51	VSS_21	R40
AW51	VSS_22	K40
AL51	VSS_23	H40
AR51	VSS_24	BL39
AN51	VSS_25	BG39
AL51	VSS_26	BA39
AJ51	VSS_27	E39
AE51	VSS_28	C39
AC51	VSS_29	A29
AA51	VSS_30	BD38
W51	VSS_31	AU38
U51	VSS_32	H38
R51	VSS_33	BG37
N51	VSS_34	AL37
L51	VSS_35	M37
J51	VSS_36	E37
G51	VSS_37	BD36
C51	VSS_38	AW36
BD50	VSS_39	H56
AM50	VSS_40	BL35
K50	VSS_41	BG35
BG49	VSS_42	AY35
E49	VSS_43	AU35
C49	VSS_44	AL35
BD48	VSS_45	AG35
BB48	VSS_46	AE35
AY48	VSS_47	AA35
AT48	VSS_48	Y35
AP48	VSS_49	M35
AM48	VSS_50	E35
AJ48	VSS_51	A35
AH48	VSS_52	BD34
AF48	VSS_53	AU34
AD48	VSS_54	AN34
AB48	VSS_55	H34
Y48	VSS_56	BL33
V48	VSS_57	BG33
T48	VSS_58	AY33
P48	VSS_59	E33
M48	VSS_60	BD32
K48	VSS_61	AU32
H48	VSS_62	AN32
BL47	VSS_63	AG32
BG47	VSS_64	AC32
E47	VSS_65	Y32
C47	VSS_66	H32
A47	VSS_67	B32
BD46	VSS_68	BJ31
AY46	VSS_69	BG31
AM46	VSS_70	AY31
AK46	VSS_71	AN31
AH46	VSS_72	M31
BG45	VSS_73	E31
AE45	VSS_74	N30
AC45	VSS_75	H30
W45	VSS_76	AN29
AA45	VSS_77	AJ29
W45	VSS_78	M29
R45	VSS_79	A29
N45	VSS_80	AW28
E45	VSS_81	AN28
BD44	VSS_82	AD28
BB44	VSS_83	AC28
AV44	VSS_84	Y28
AK44	VSS_85	W28
AH44	VSS_86	H28
AF44	VSS_87	F28
AD44	VSS_88	AN27
K44	VSS_89	AJ27
H44	VSS_90	M27
BL43	VSS_91	BF26
BG43	VSS_92	BD26
AY43	VSS_93	N26
AR43	VSS_94	H26
W43	VSS_95	BJ25
R43	VSS_96	AY25
M43	VSS_97	AU25
E43	VSS_98	
	VSS_99	

VSS

CANTIGA GMCH SFF_FCBGA1363

12/12 FOR NO CRACK DETECT FUNCTION

AN25	VSS_199	AM8
AG25	VSS_200	AK8
AE25	VSS_201	AH8
AA25	VSS_202	AF8
Y25	VSS_203	AD8
E25	VSS_204	AB8
A25	VSS_205	Y8
BD24	VSS_206	V8
AE41	VSS_207	P8
AL24	VSS_208	M8
H24	VSS_209	K8
BG23	VSS_210	H8
E41	VSS_211	E7
E23	VSS_212	VSS_313
BD22	VSS_213	VSS_314
BB22	VSS_214	VSS_315
AN22	VSS_215	VSS_316
Y22	VSS_216	VSS_317
W22	VSS_217	VSS_318
H22	VSS_218	VSS_319
BL21	VSS_219	VSS_320
BG21	VSS_220	VSS_321
AY21	VSS_221	VSS_322
AN21	VSS_222	VSS_323
AG21	VSS_223	VSS_324
AE21	VSS_224	VSS_325
M21	VSS_225	VSS_326
E21	VSS_226	VSS_327
A21	VSS_227	VSS_328
BD20	VSS_228	VSS_329
H20	VSS_229	VSS_330
BG19	VSS_230	VSS_331
AY19	VSS_231	VSS_332
M19	VSS_232	VSS_333
E19	VSS_233	VSS_334
BD18	VSS_234	VSS_335
N18	VSS_235	VSS_336
H18	VSS_236	VSS_337
BG17	VSS_237	VSS_338
AY17	VSS_238	VSS_339
M17	VSS_239	VSS_340
E17	VSS_240	VSS_341
A17	VSS_241	VSS_342
BD16	VSS_242	VSS_343
AG16	VSS_243	VSS_344
AE16	VSS_244	VSS_345
Y16	VSS_245	VSS_346
W16	VSS_246	VSS_347
H16	VSS_247	VSS_348
BG15	VSS_248	VSS_349
AY15	VSS_249	VSS_350
M15	VSS_250	VSS_351
E15	VSS_251	VSS_352
A15	VSS_252	VSS_353
BD14	VSS_253	VSS_354
H14	VSS_254	VSS_355
BG13	VSS_255	VSS_356
AY13	VSS_256	VSS_357
M13	VSS_257	VSS_358
E13	VSS_258	VSS_359
A13	VSS_259	VSS_360
BD13	VSS_260	VSS_361
H13	VSS_261	VSS_362
BG12	VSS_262	
AY12	VSS_263	
M12	VSS_264	
E12	VSS_265	
A12	VSS_266	
BD12	VSS_267	
H12	VSS_268	
BG11	VSS_269	
AY11	VSS_270	
M11	VSS_271	
E11	VSS_272	
A11	VSS_273	
BD11	VSS_274	
H11	VSS_275	
BG10	VSS_276	
AY10	VSS_277	
M10	VSS_278	
E10	VSS_279	
A10	VSS_280	
BD10	VSS_281	
H10	VSS_282	
BG9	VSS_283	
AY9	VSS_284	
M9	VSS_285	
E9	VSS_286	
A9	VSS_287	
BD8	VSS_288	
H8	VSS_289	
BG7	VSS_290	
AY7	VSS_291	
M7	VSS_292	
E7	VSS_293	
A7	VSS_294	
BD7	VSS_295	
H7	VSS_296	
BG6	VSS_297	
AY6	VSS_298	
M6	VSS_299	
E6	VSS_299	

VSS

VSS NCTF

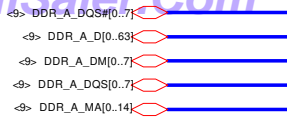
VSS SCB

VSS_NCTF_1	BL55
VSS_NCTF_2	BL1
VSS_NCTF_3	AS5
VSS_NCTF_4	D1
VSS_NCTF_5	B55
VSS_NCTF_6	B2
VSS_NCTF_7	A4
VSS_NCTF_8	
VSS_NCTF_9	
VSS_NCTF_10	
VSS_NCTF_11	
VSS_NCTF_12	
VSS_NCTF_13	
VSS_NCTF_14	
VSS_NCTF_15	
VSS_NCTF_16	
VSS_NCTF_17	
VSS_NCTF_18	
VSS_NCTF_19	
VSS_NCTF_20	
VSS_NCTF_21	
VSS_NCTF_22	
VSS_NCTF_23	

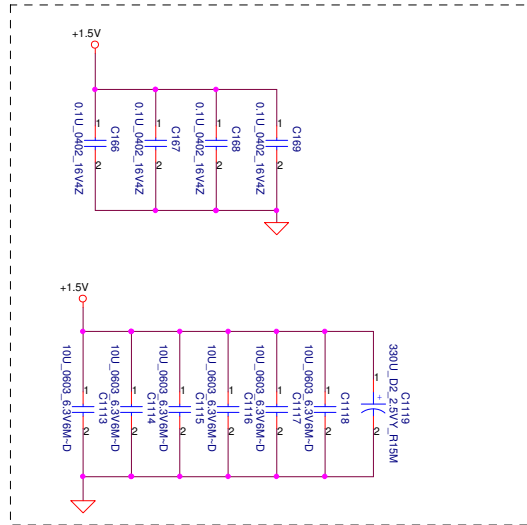
12/12 FOR NO CRACK DETECT FUNCTION

CANTIGA GMCH SFF_FCBGA1363

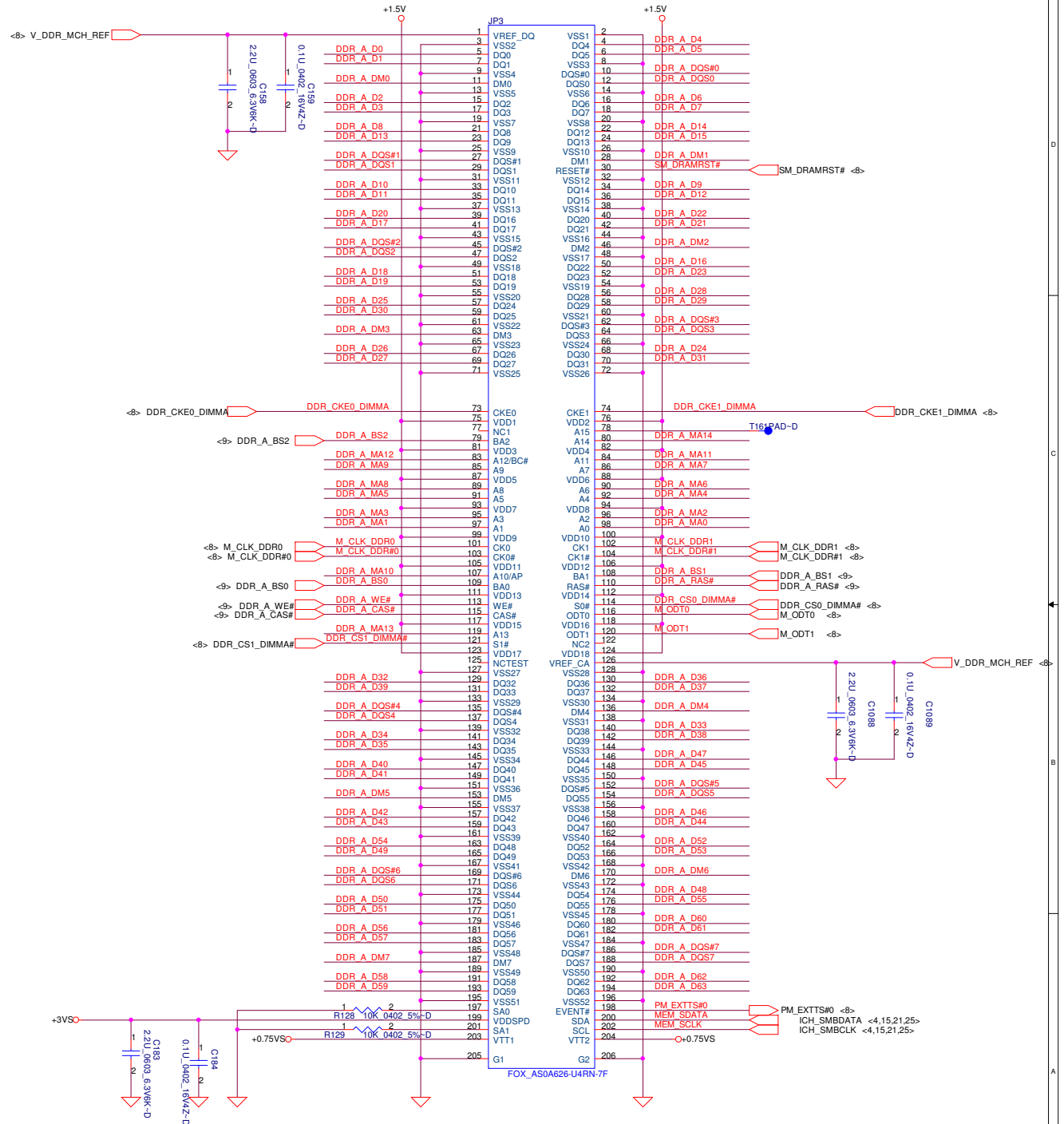
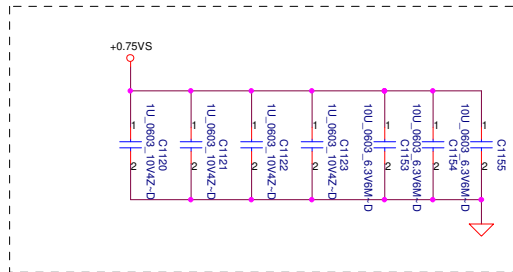
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Layout Note:
Place near JP3



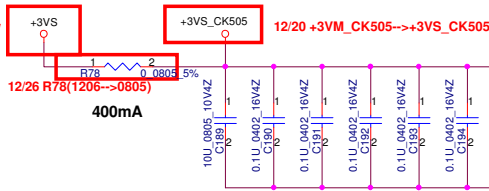
Layout Note:
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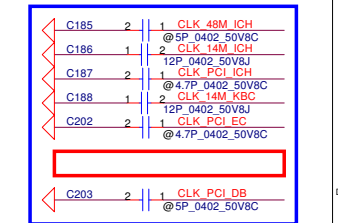
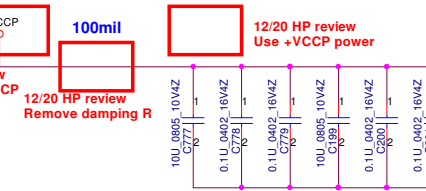
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FSLC	FSLB	FSLA	CPU	FSB	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3

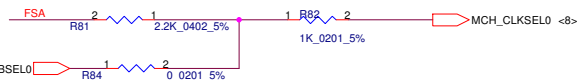
12/17 HP review
+3VM-->+3VS



12/17 HP review
+1.05VM-->+VCCP



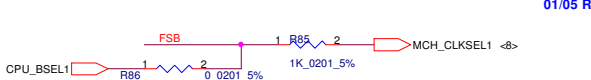
12/20 HP review
Remove reserved pull +VCCP R



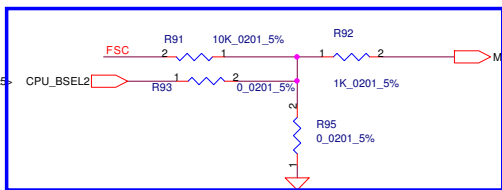
12/20 HP review
Remove reserved pull low R



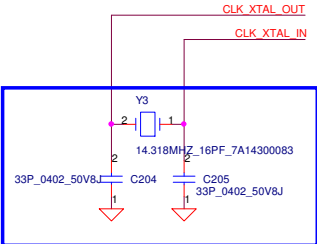
12/20 HP review
Remove reserved pull +VCCP R



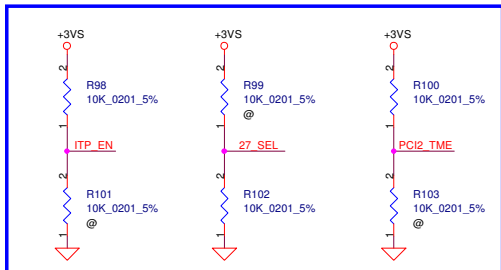
12/20 HP review
Remove reserved pull low R



12/31 Use 0201 size

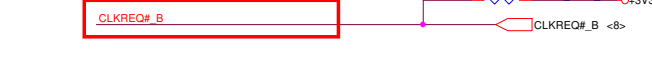


12/31 Y3 sue 5032 size and confirm C204 C205 c value



12/31 Use 0201 size

12/17 HP review
Remove damping R



12/20
+3VM_CK505-->+3VS_CK505

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

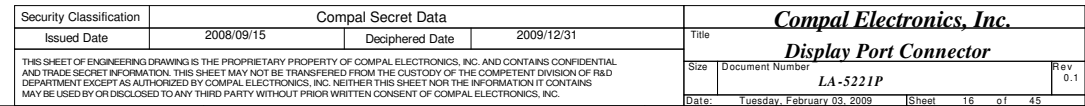
12/20 HP review
Use +VCCP power

12/20 HP review
Use +VCCP power

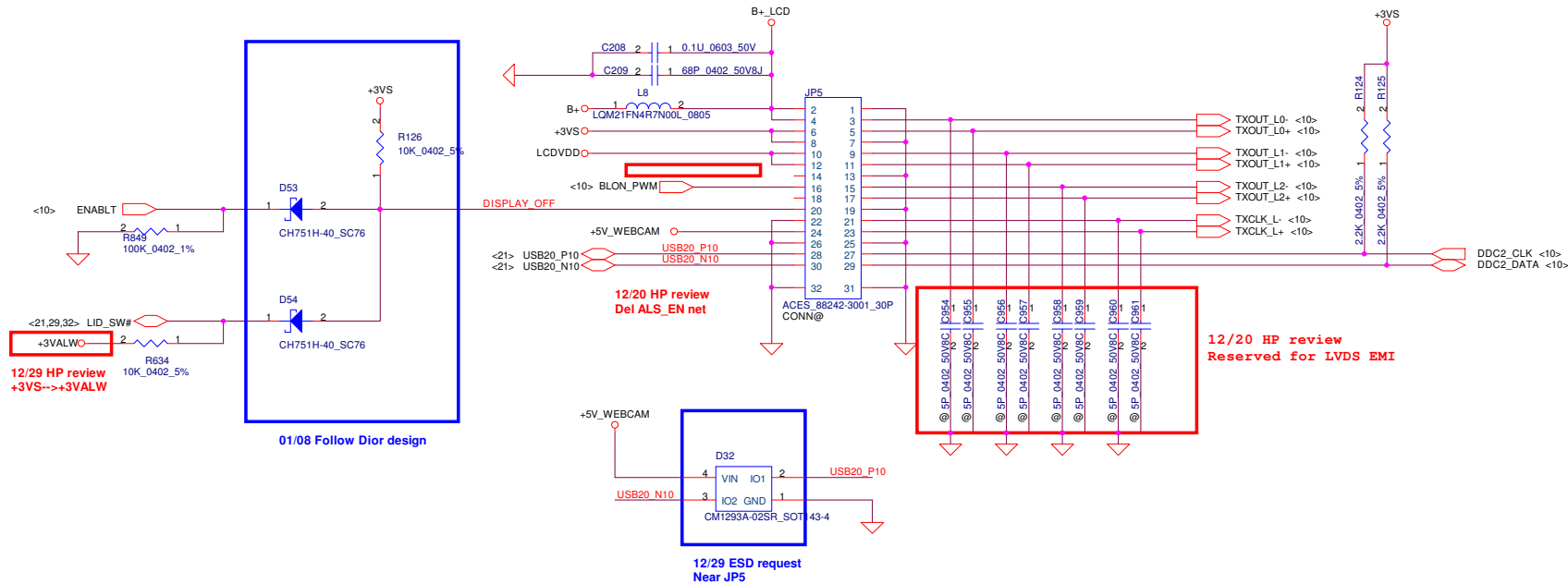
12/20 HP review
Use +VCCP power

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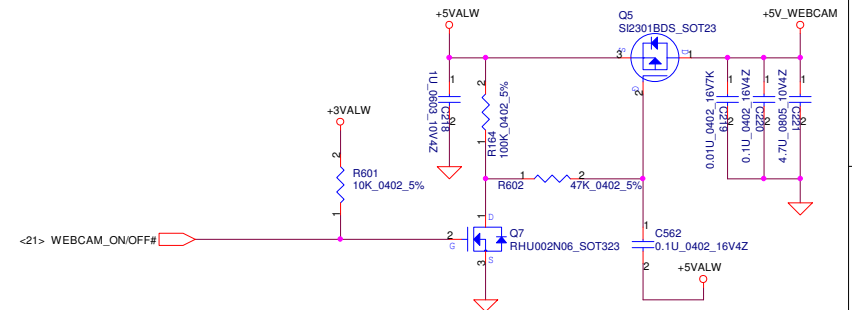
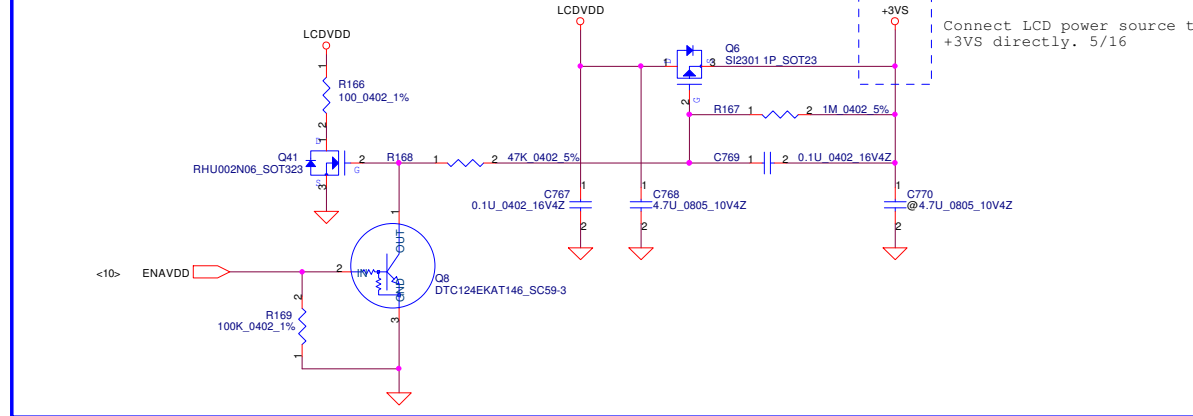
Compal Electronics, Inc.			
CLOCK GENERATOR			
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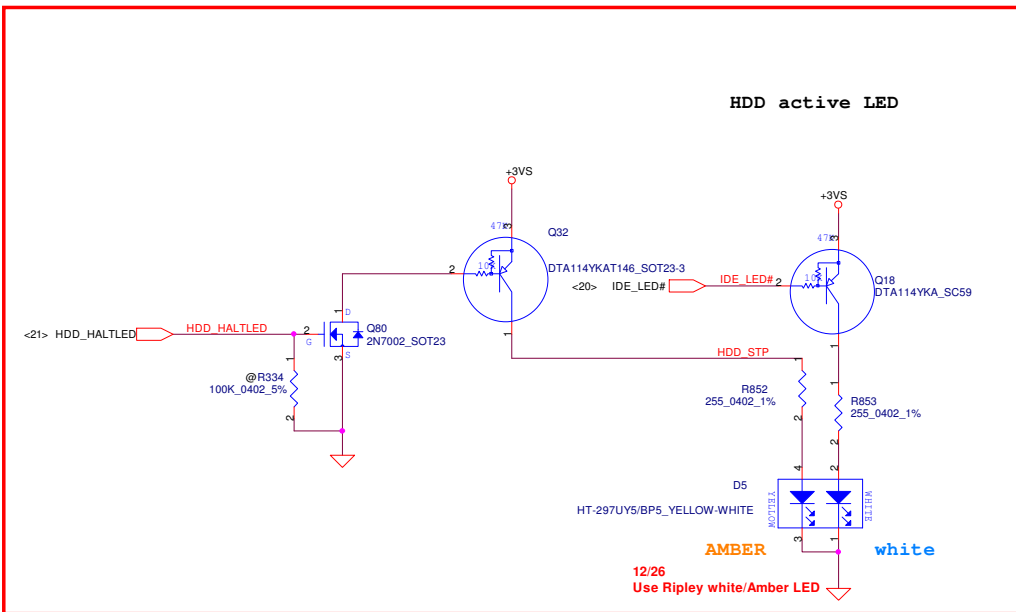
LED/PANEL BD. CONN.



LCD POWER CIRCUIT

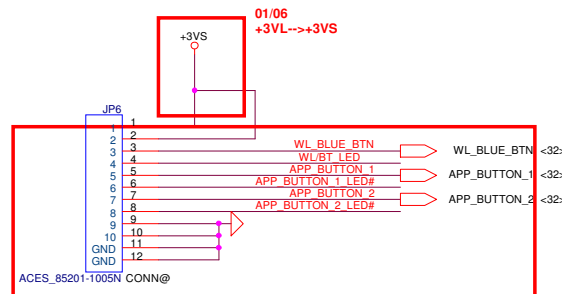


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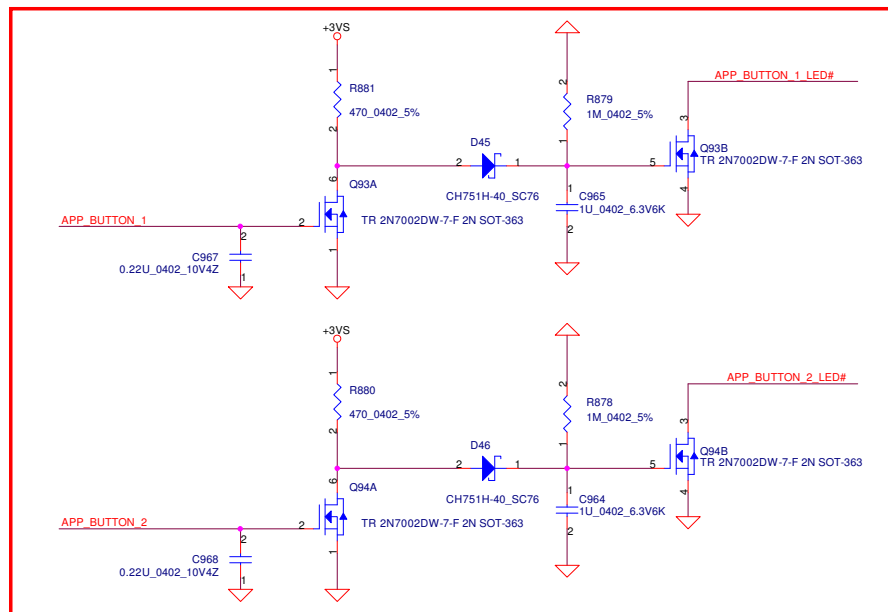
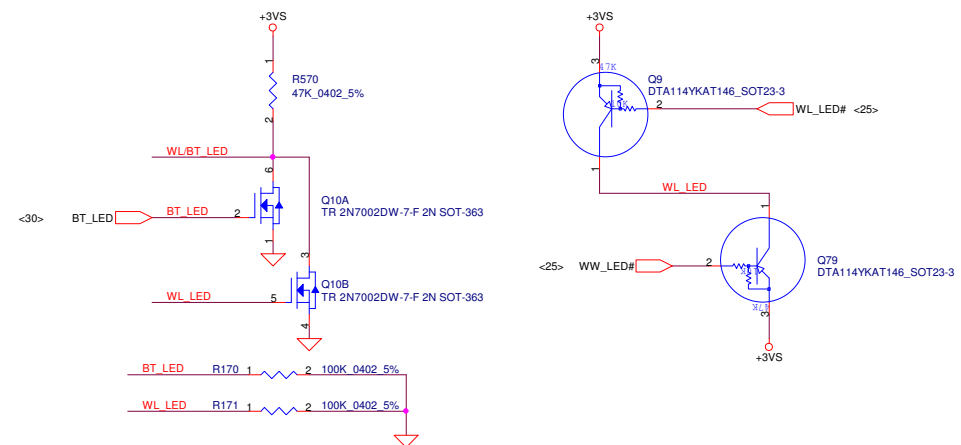


12/26
Modify HD LED control(follow skyy)

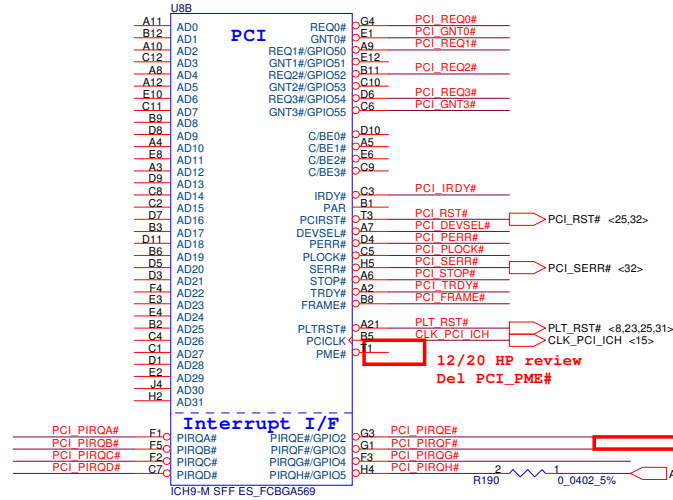
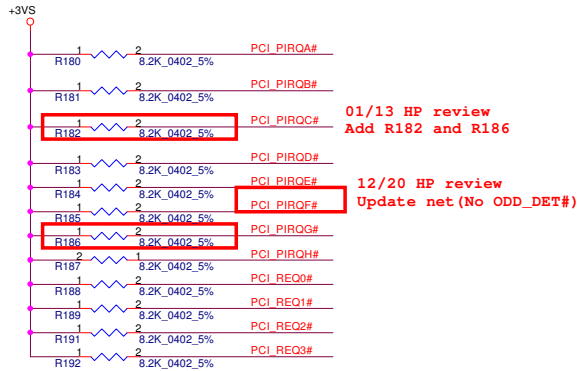
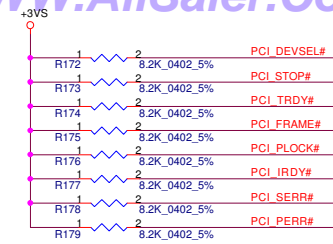
To LED small board



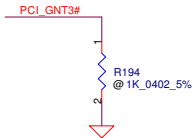
01/06
Confirm LED GPIO ok



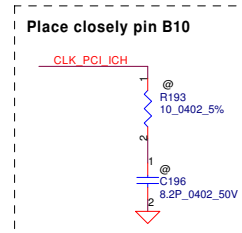
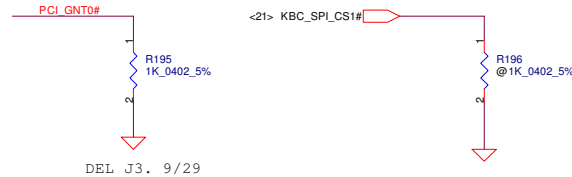
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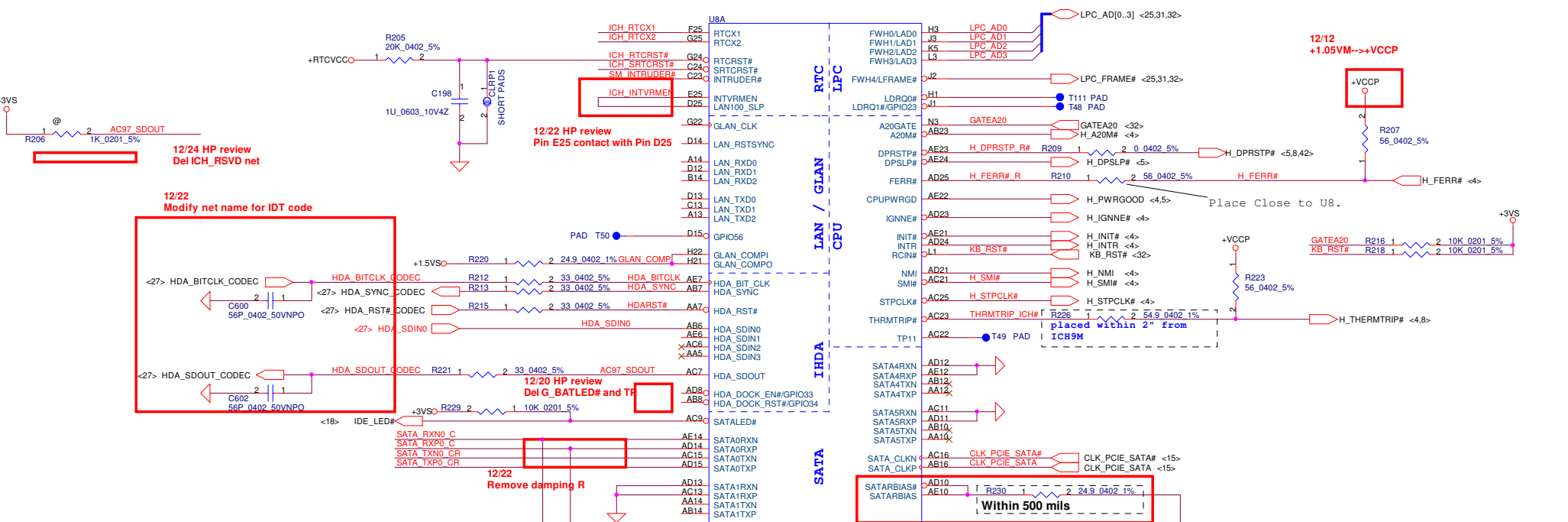
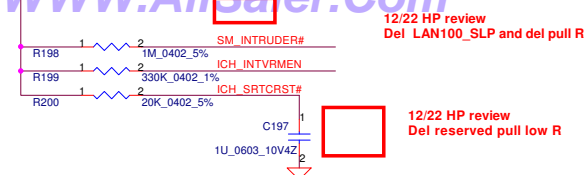


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

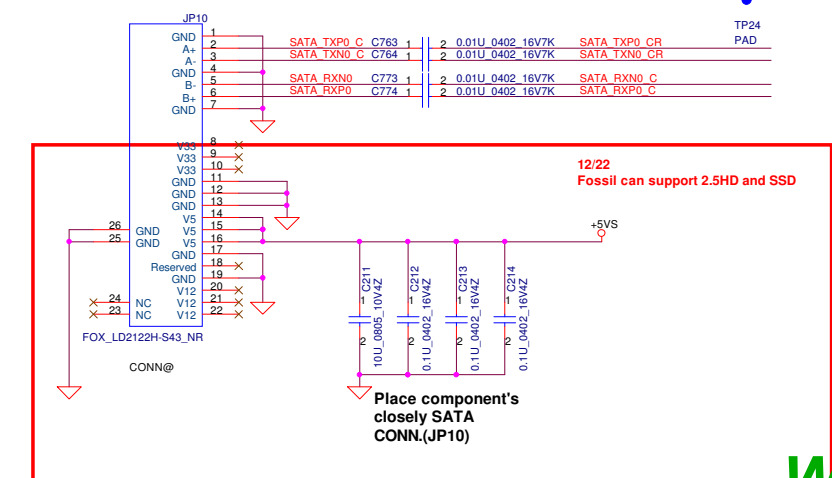


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

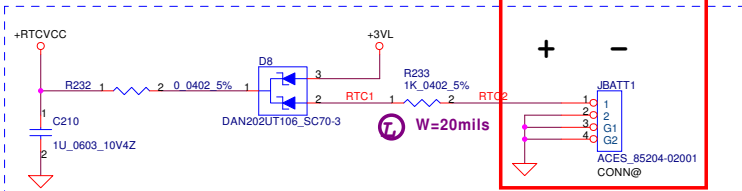
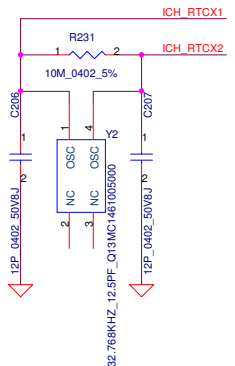




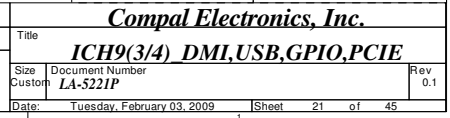
2.5' SATA HDD Connector

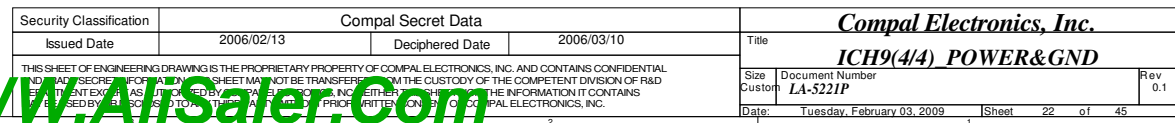


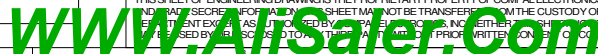
01/13 Add test point



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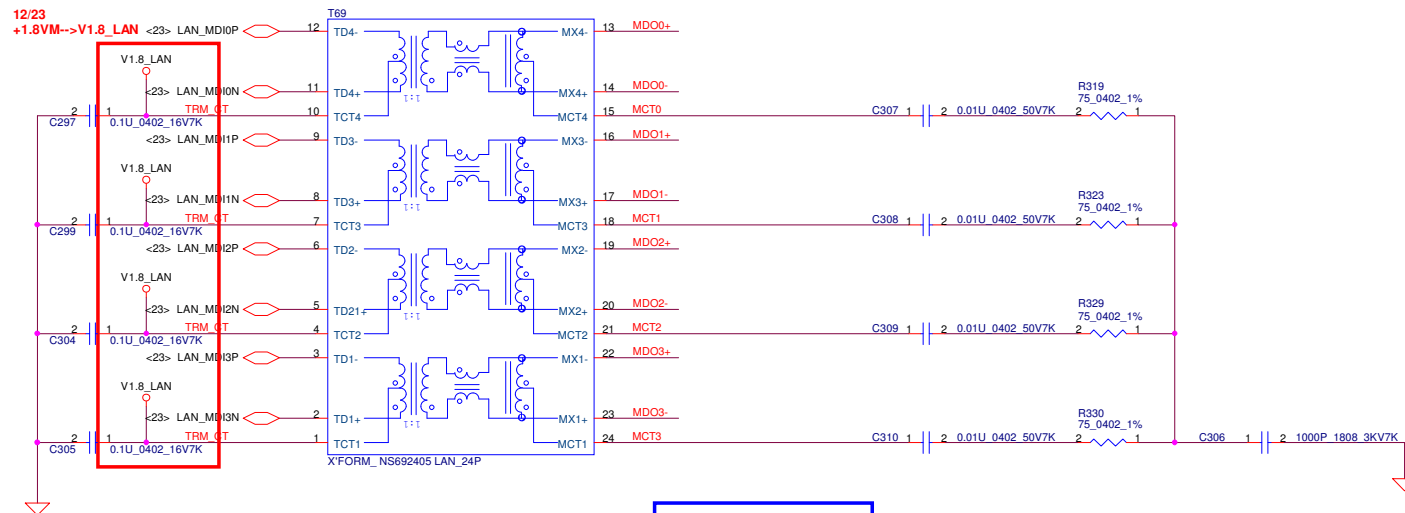
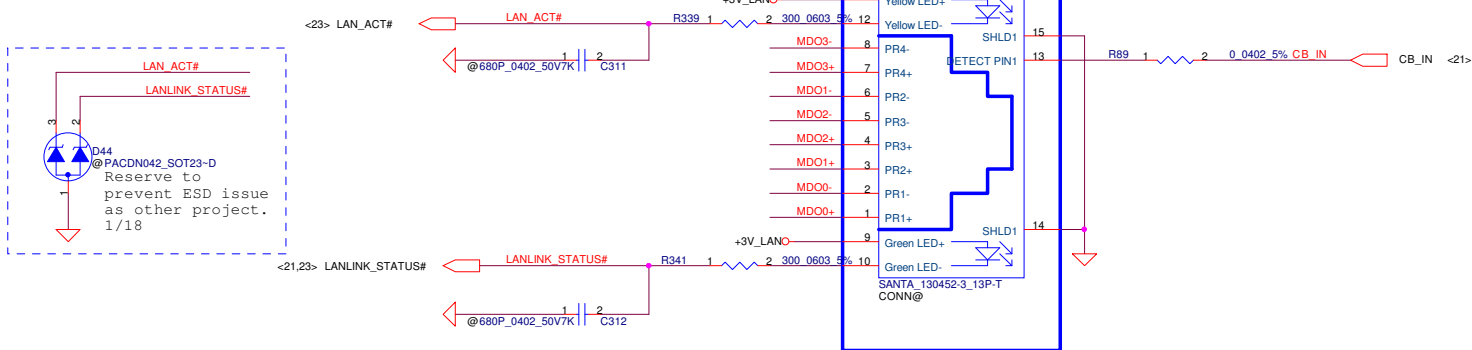




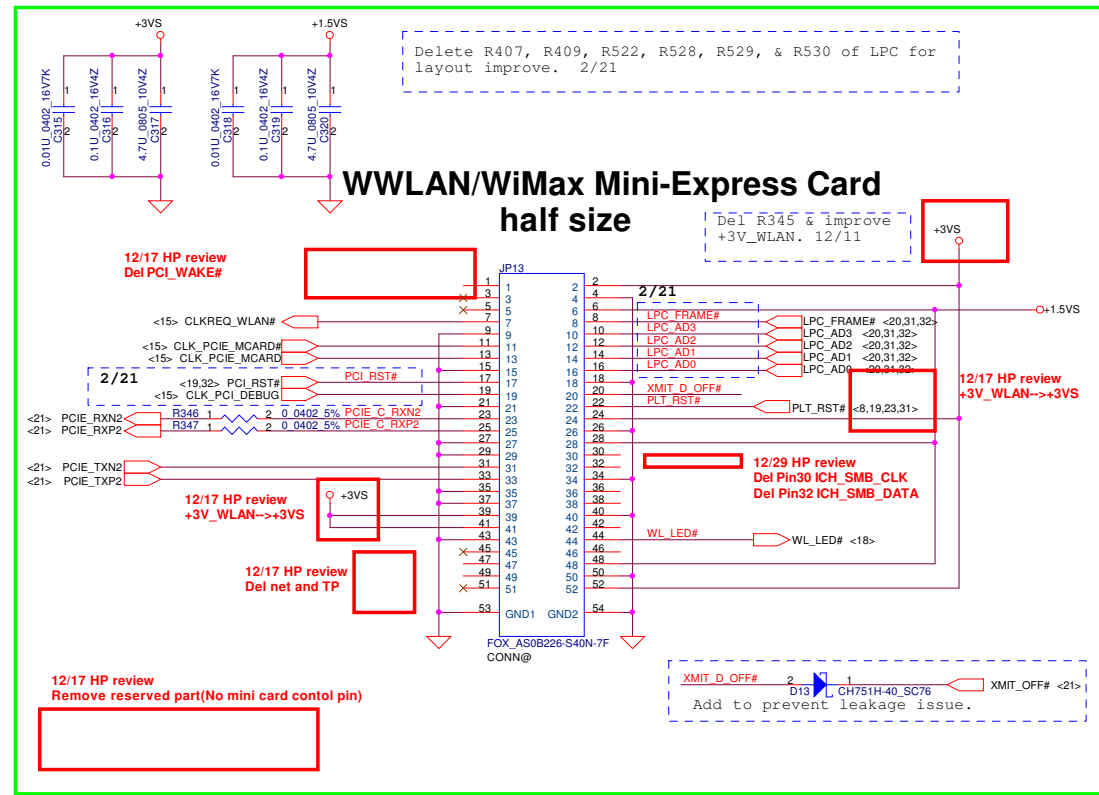


12/15 No support Docking

Delete all termination cause they are already inside BOAZMAN. 9/28

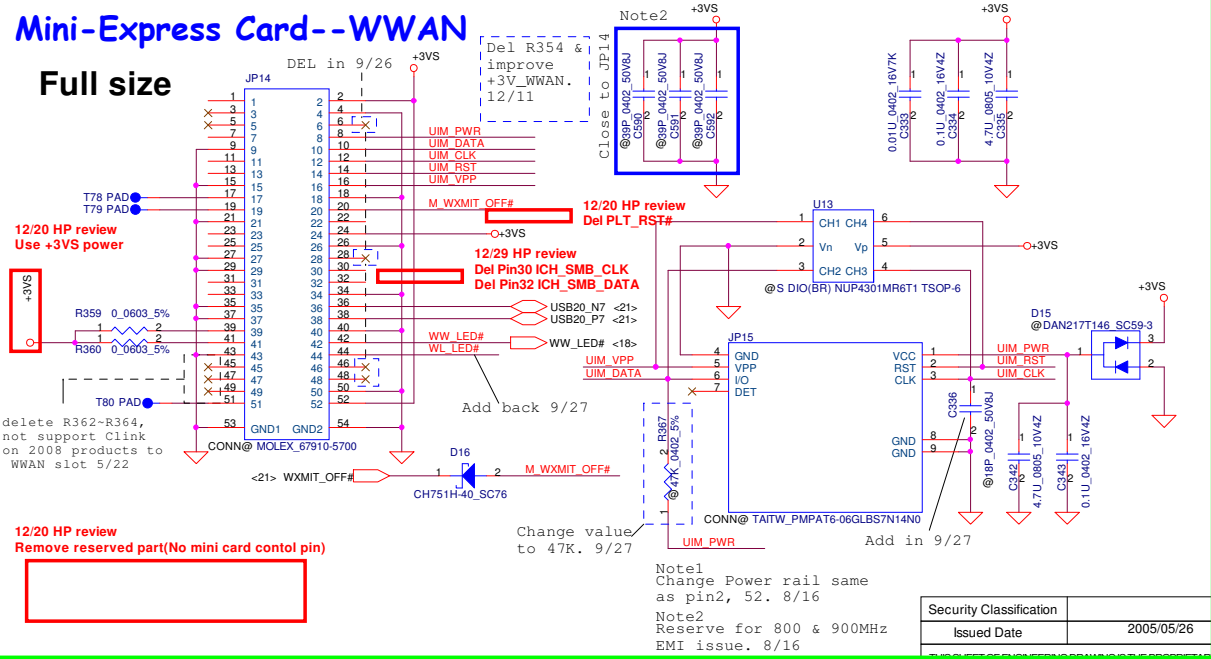
12/29 HP review
Del Q23 Q2401/13
Update JP7 footprint

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Mini-Express Card--WWAN

Full size



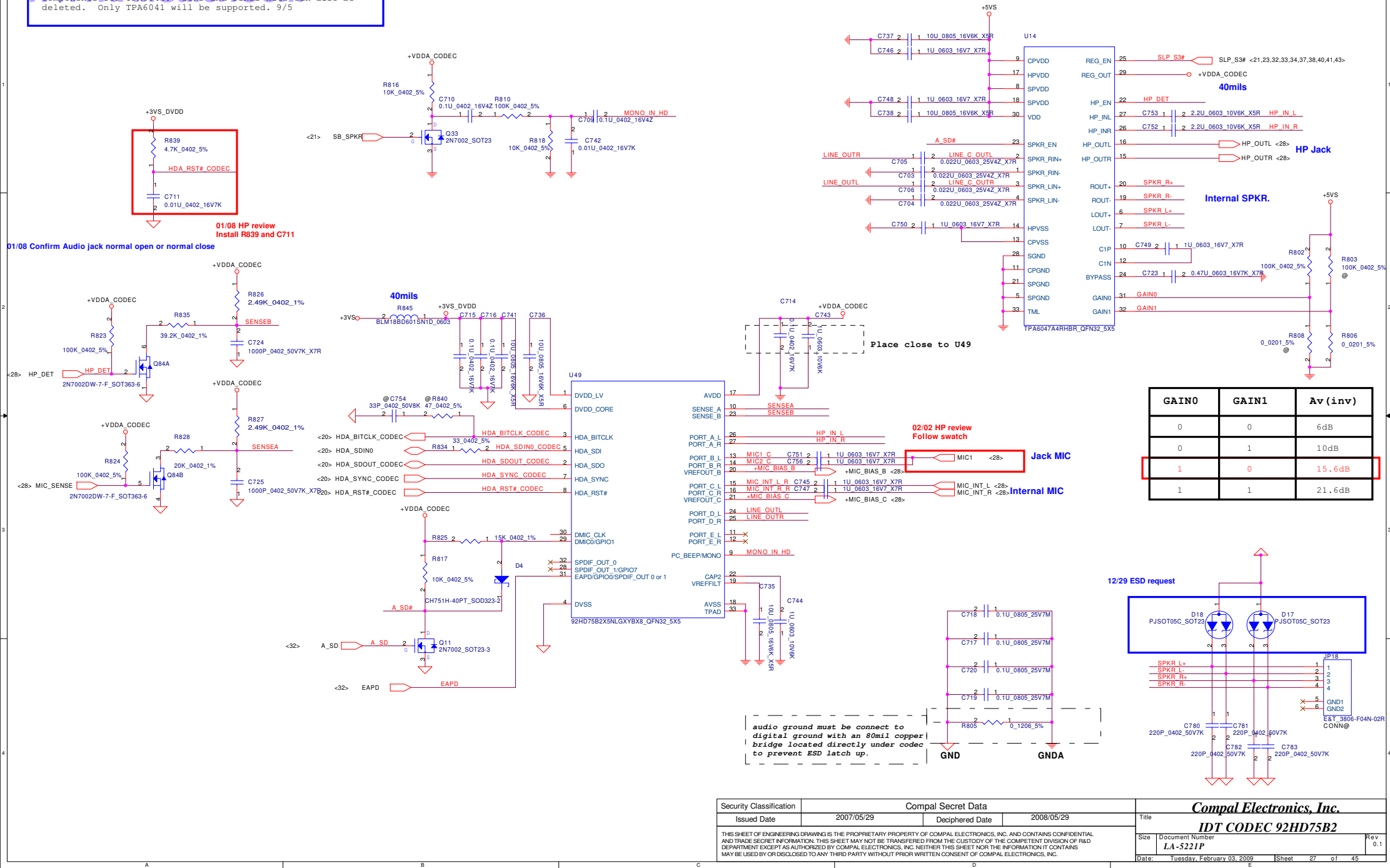
12/17 Remove to small board

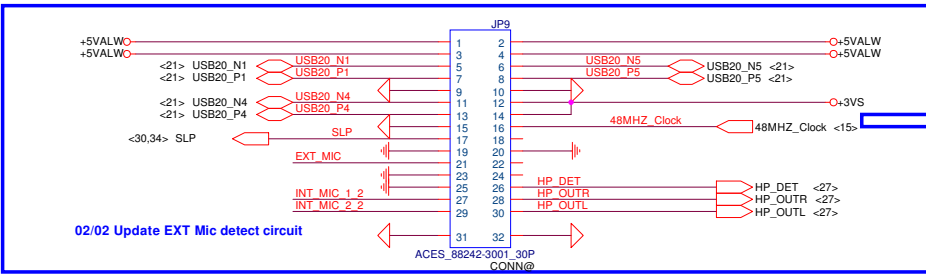
Title			
Card reader board			
Size	Document Number		Rev
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TPA6044 no longer needed, so delete BOM options & co-layout components for TPA6044. SGND and SGND1 nets can also be deleted. Only TPA6041 will be supported. 9/5

AMP. FOR INTERNAL SPEAKER

11/25

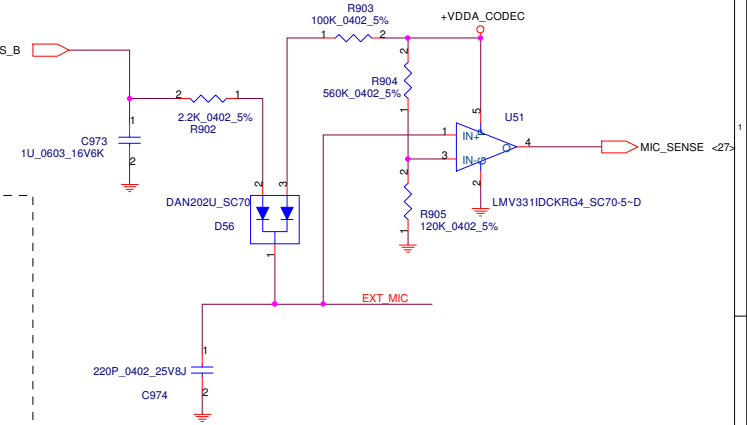
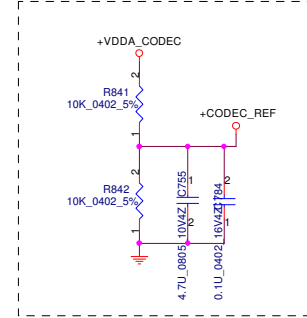




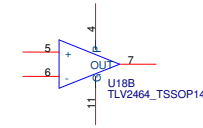
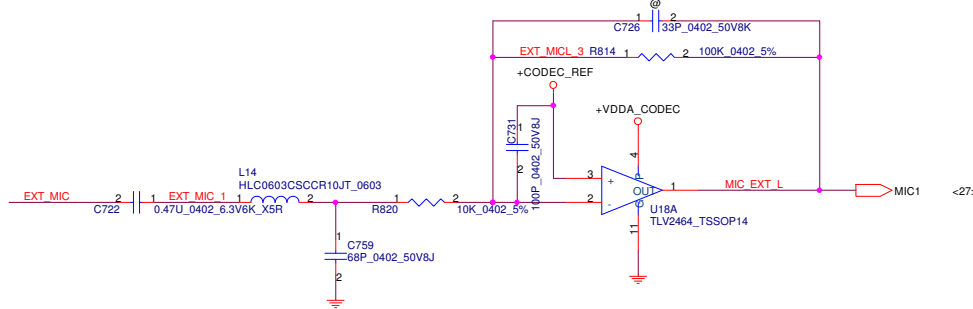
USB I/O connx2, Audio JACK
Card reader transfer conn

12/26 Reserved for card reader

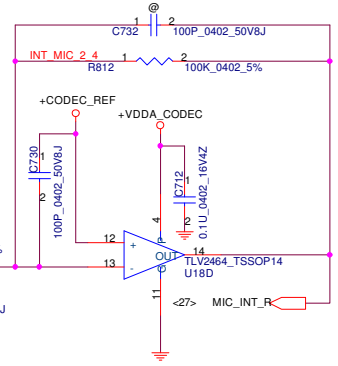
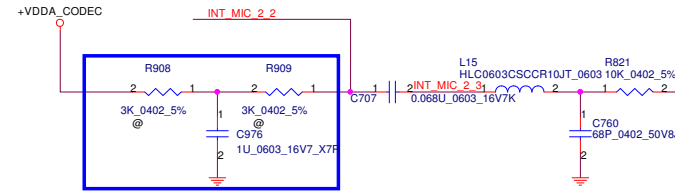
Place close to U18



AMP. FOR EXTERNAL MICROPHONE



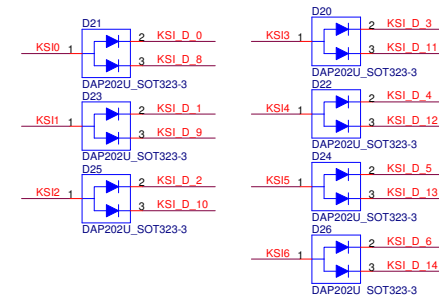
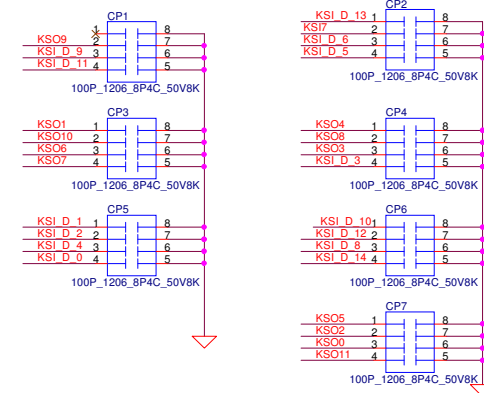
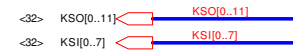
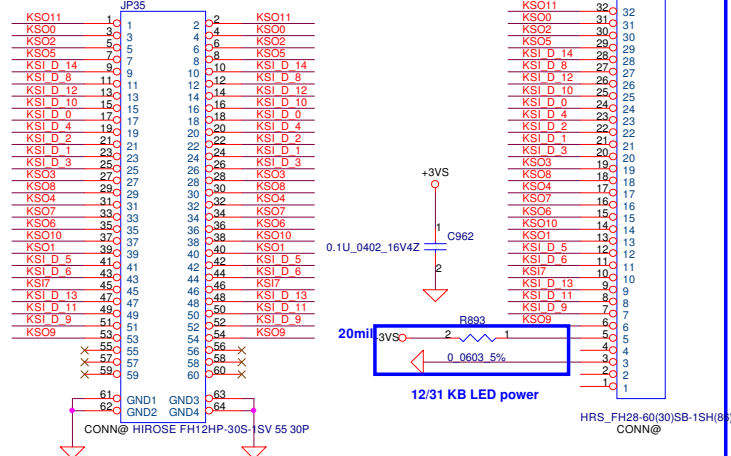
AMP. FOR INTERNAL MICROPHONE



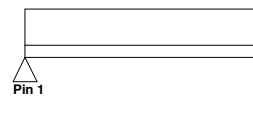
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				Size	Document Number	Rev
/W.A.S.A.I.S.A						

INT_KBD_CONN.

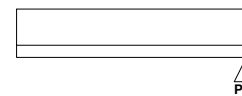
01/09 Co layout for DB phase



Dior KB up contact

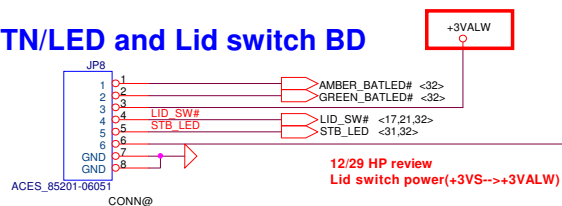


DB use

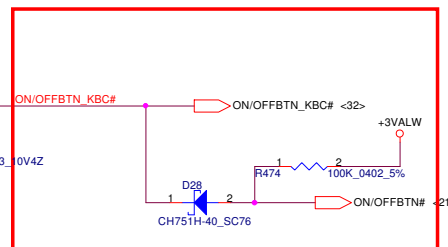


**Pin1 reserve , so net name is reserve
for Fossil down contact**

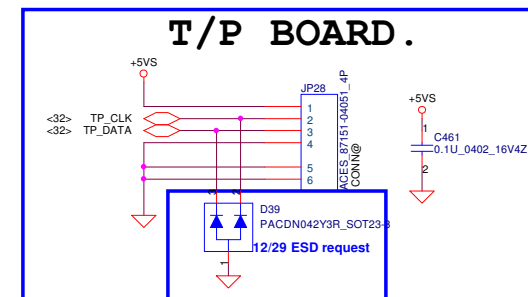
Power BTN/LED and Lid switch BD



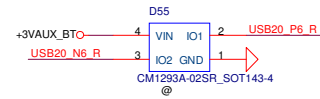
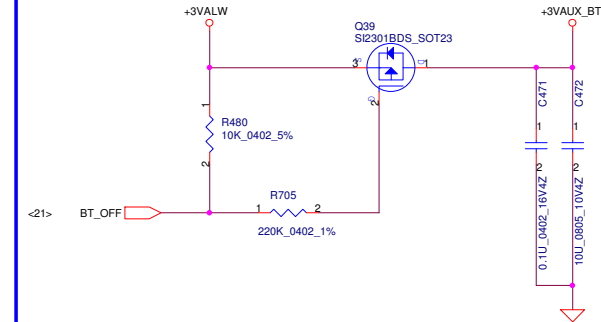
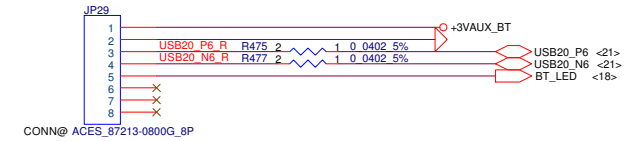
PS:GND use DC in jack GND



12/20 HP review
Modify ON/OFFBTN# circuit



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**BT (SoftBreeze) Connector**

12/16 change to small board

2A normal with 3.5A Max(1ms)

4A

01/15 Del R356 R887

USB_VCCC

12/16 HP review
S4_STATE#-->SLP

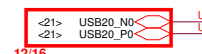
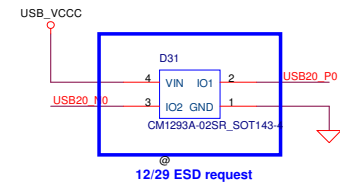
01/08 Update USB power and footprint

USB CONNECTOR 3

12/29 Use B2 size

160mils

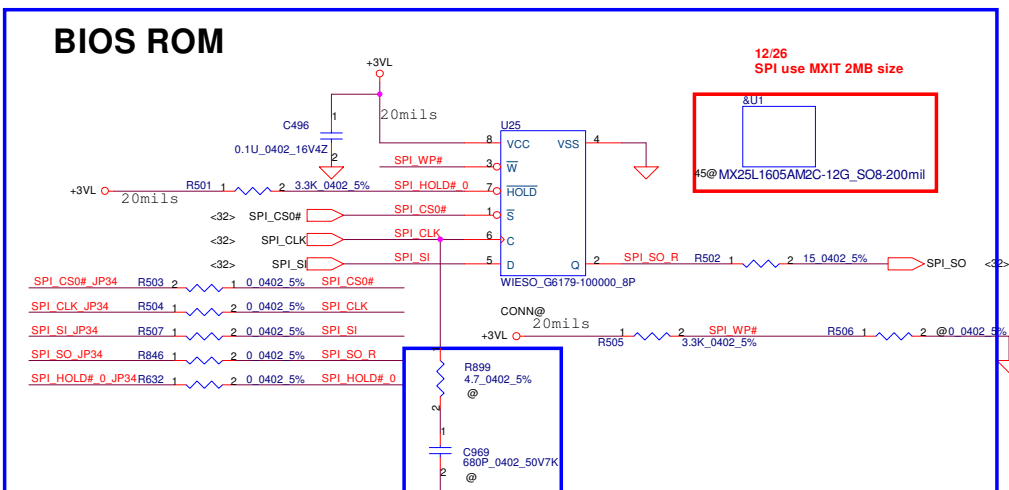
01/15 Pin7 and Pin8 contact to GND

12/16
USB port 0 for debug on M/B

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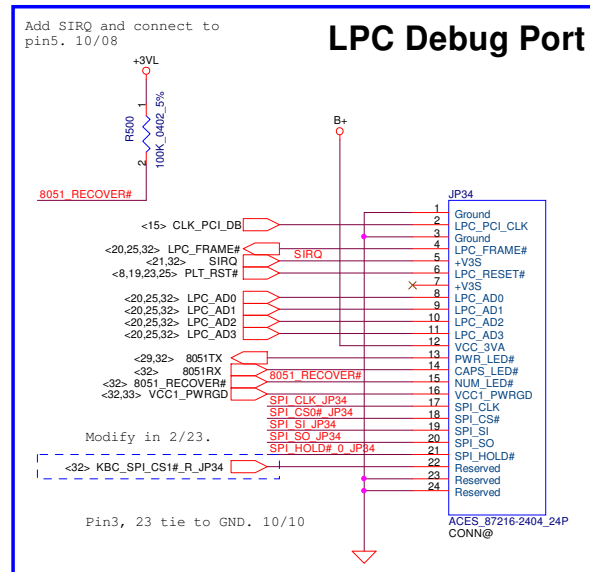
01/23
U25 is conn
&U1 is SPI ROM

BIOS ROM

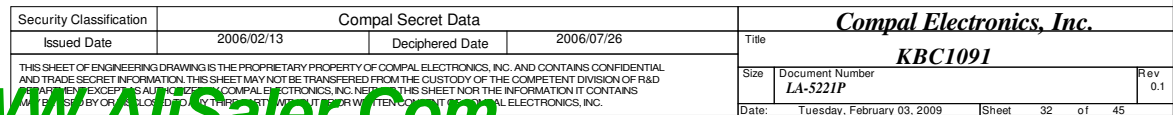


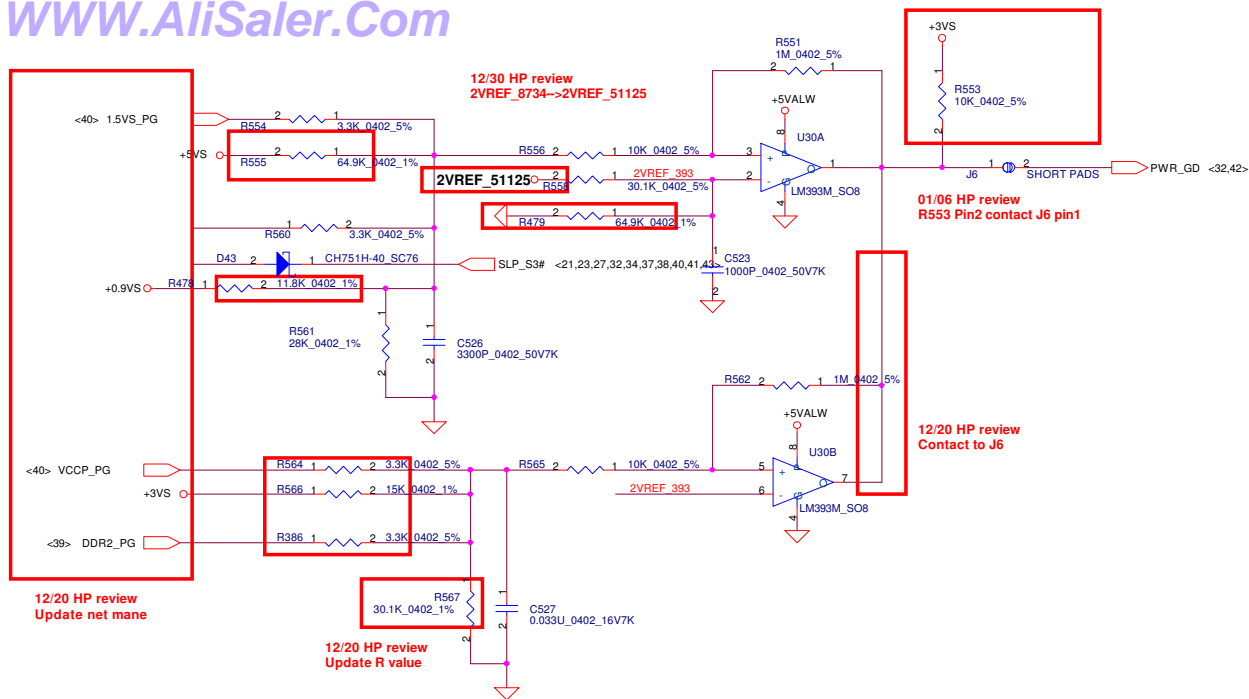
01/13
Reserved for ESD

LPC Debug Port

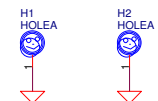


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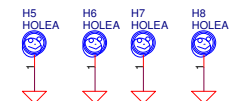




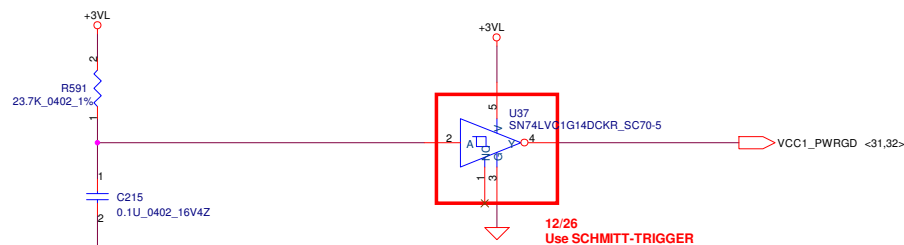
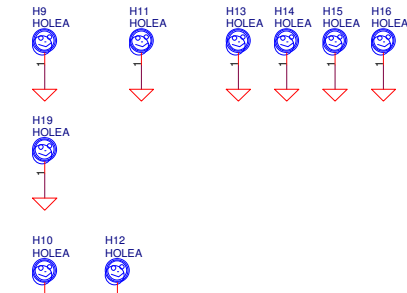
WWAN Card STANDOFF



CPU support



WWLAN Card STANDOFF



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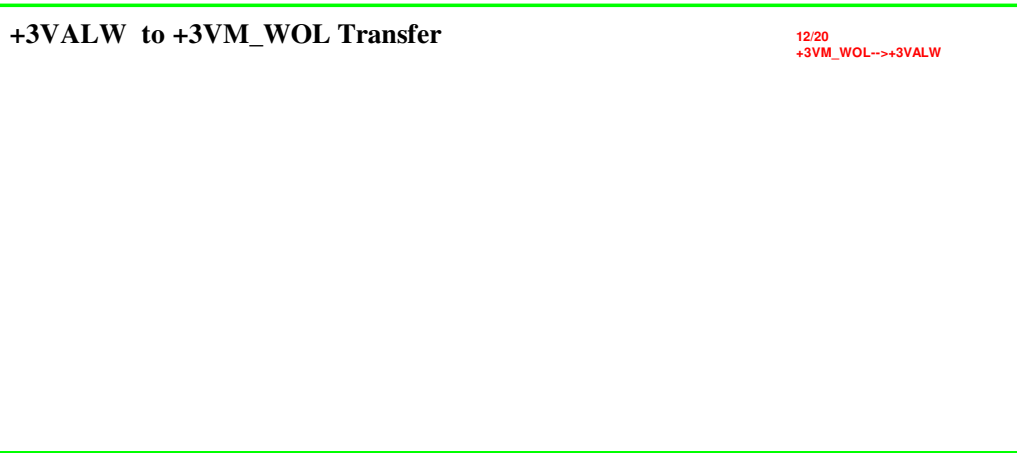
+1.05VM to +VCCP Transfer

12/12
+1.05VN-->+VCCP

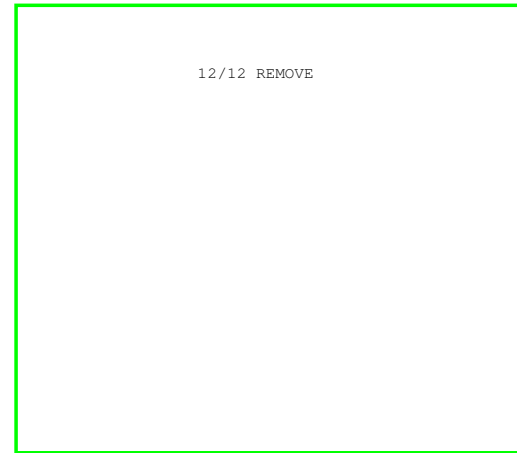


+3VALW to +3VM_WOL Transfer

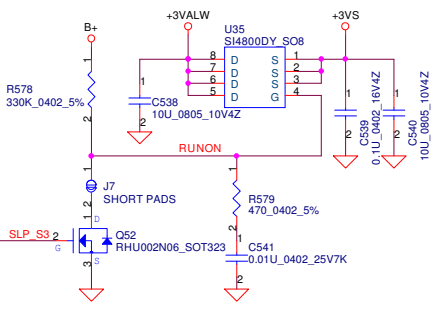
12/20
+3VM_WOL-->+3VALW



12/12 REMOVE

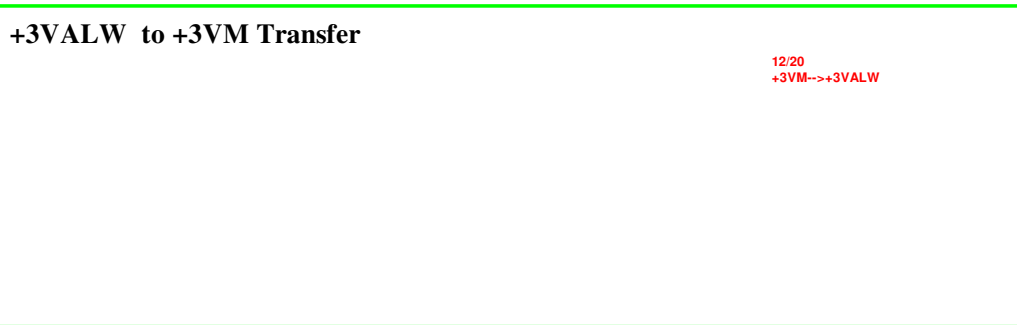


+3VALW to +3VS Transfer

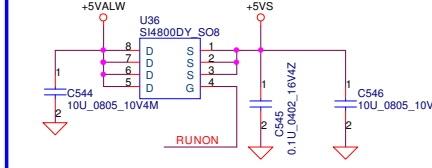


+3VALW to +3VM Transfer

12/20
+3VM-->+3VALW

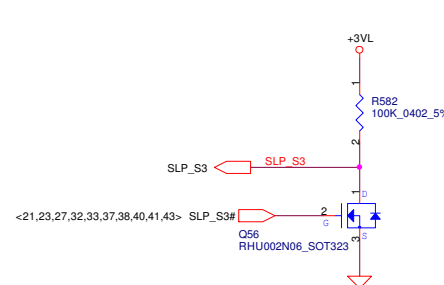
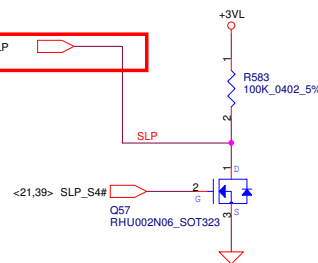
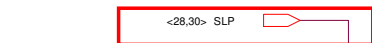


+5VALW to +5VS Transfer

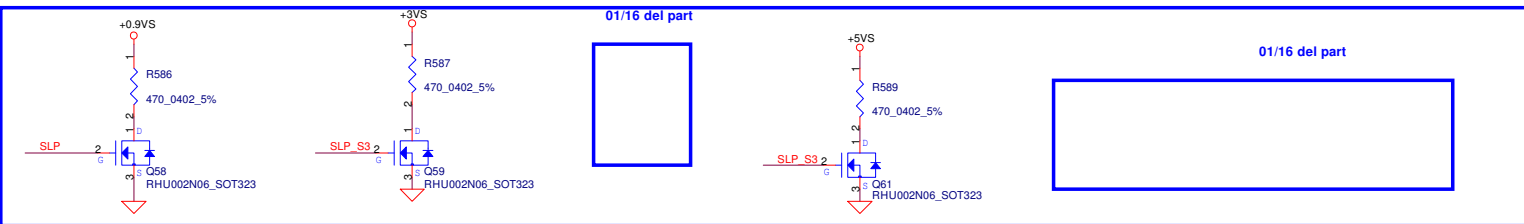


12/20 HP review
SLP control

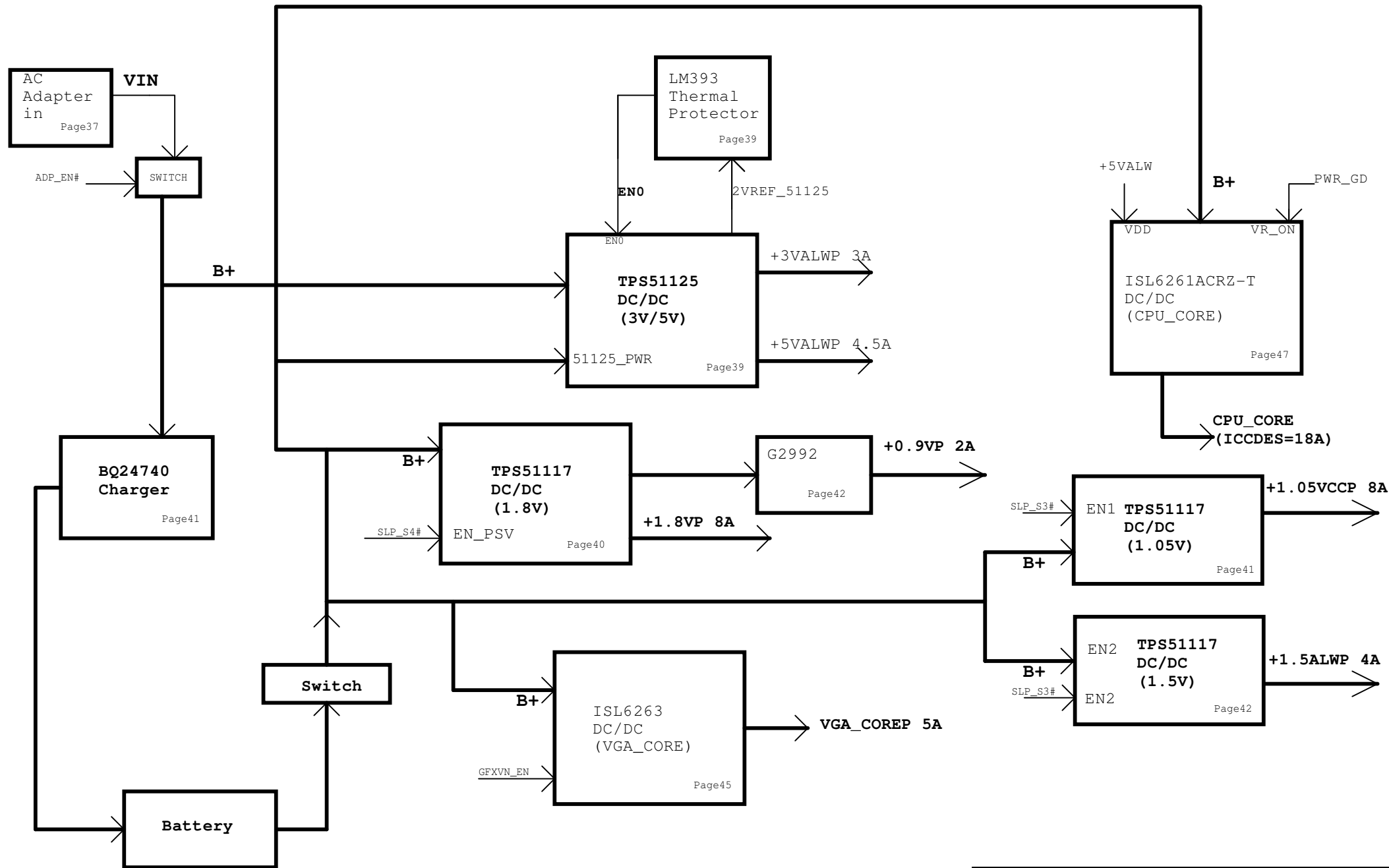
01/16 del part



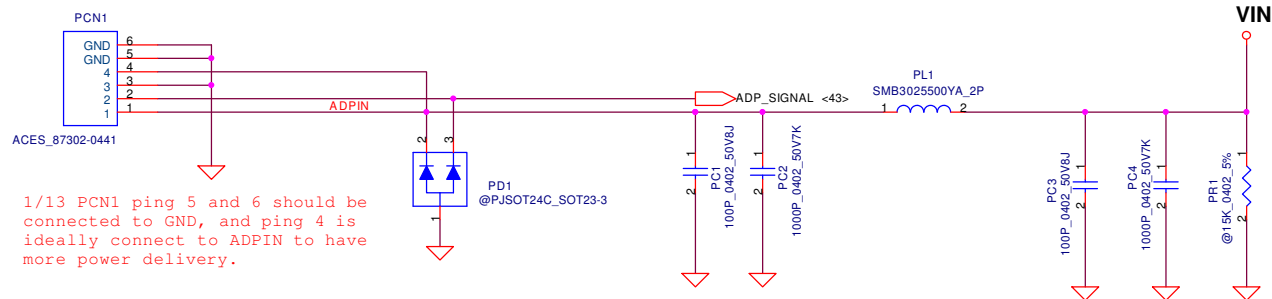
Discharge circuit-1



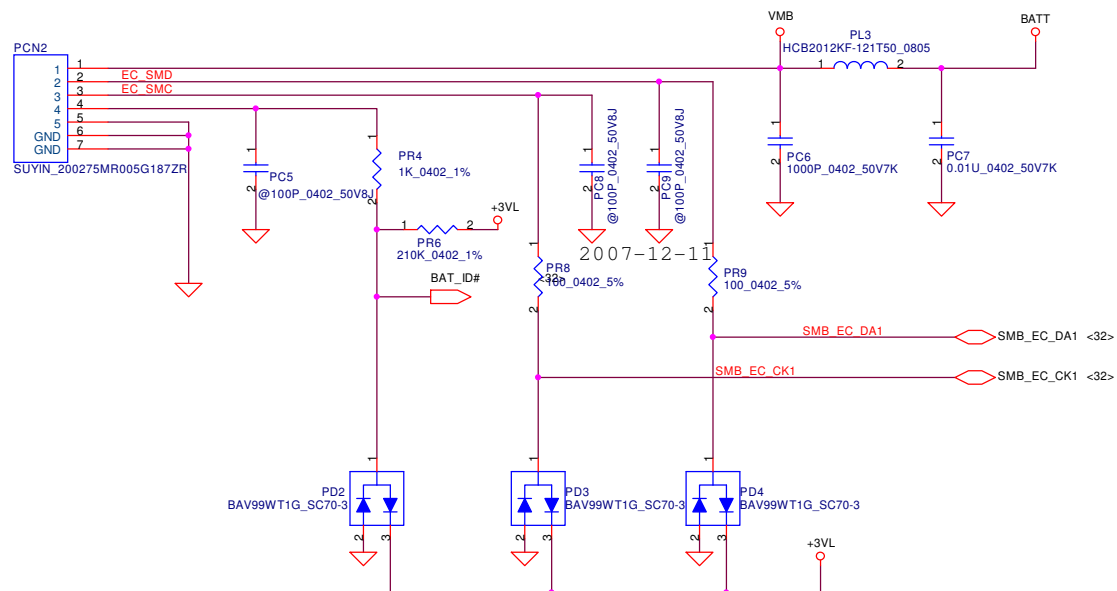
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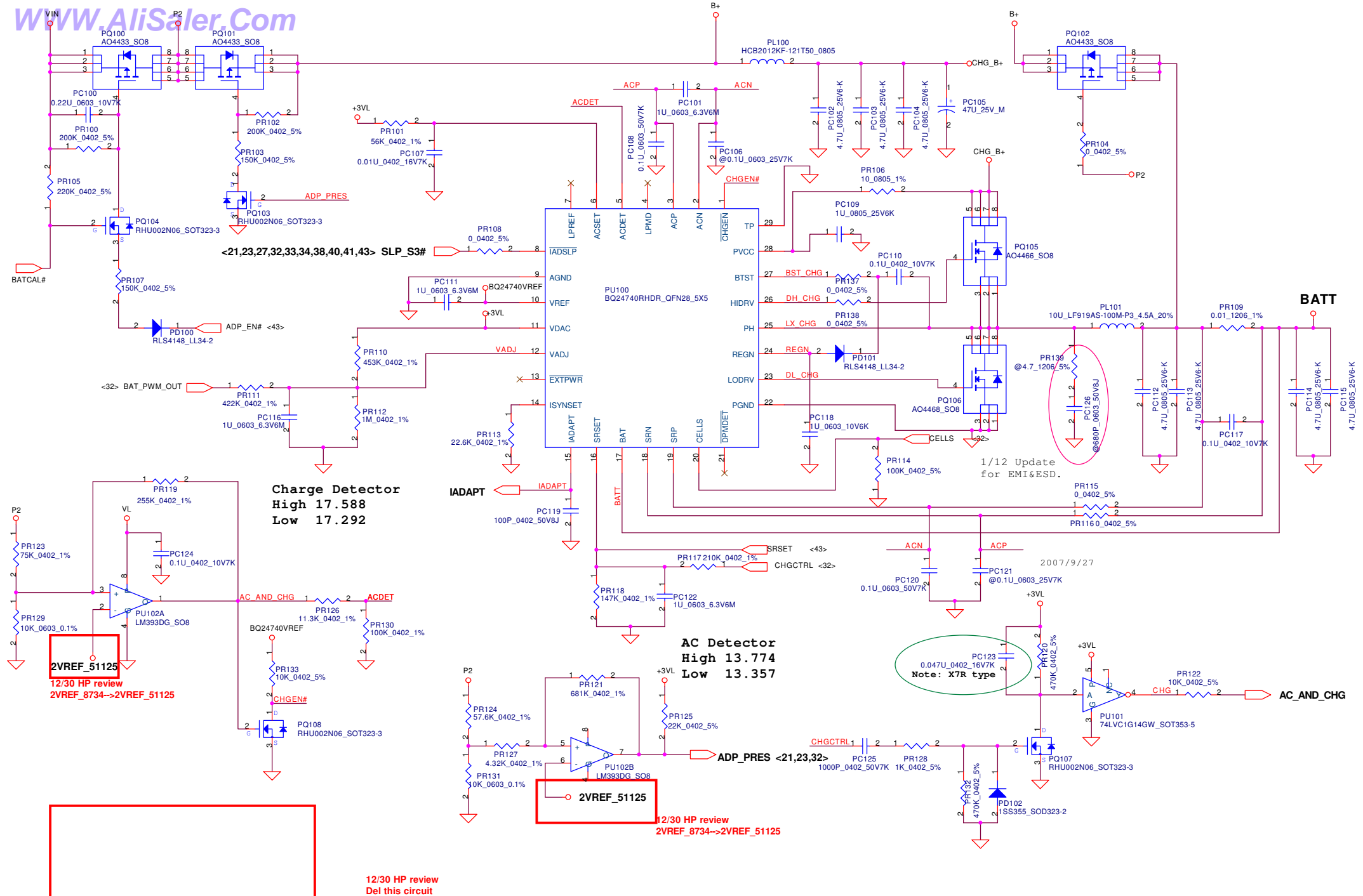
Title		
POWER BLOCK DIAGRAM		
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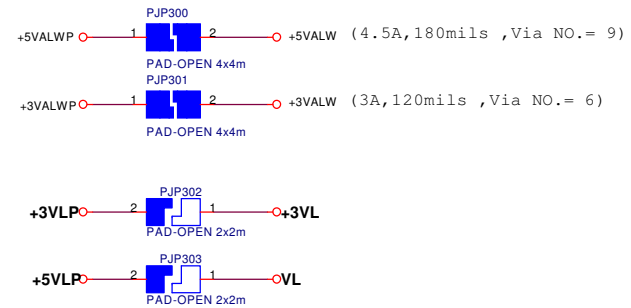
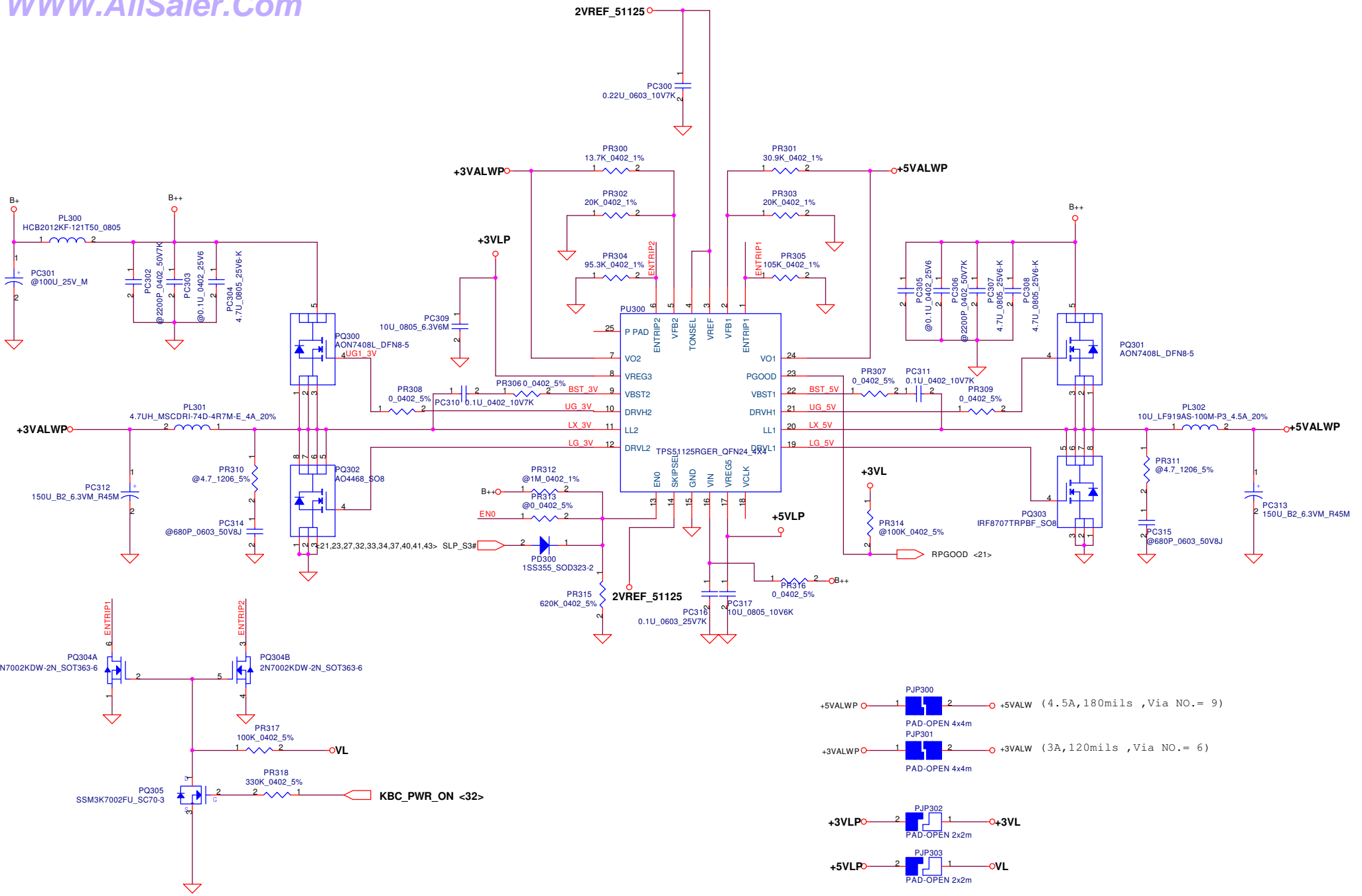
PH1 under CPU botten side :
 CPU thermal protection at 90 \pm 3 degree C
 Recovery at 47 \pm 3 degree C



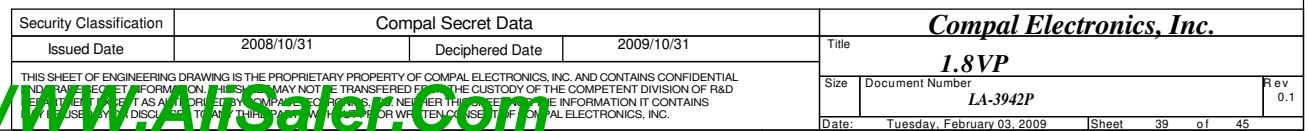
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								Size		Document Number		Rev	
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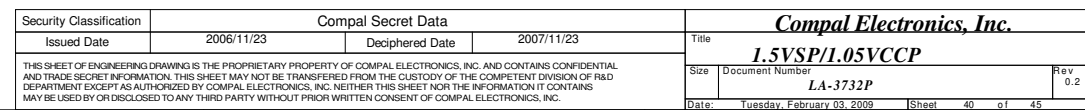


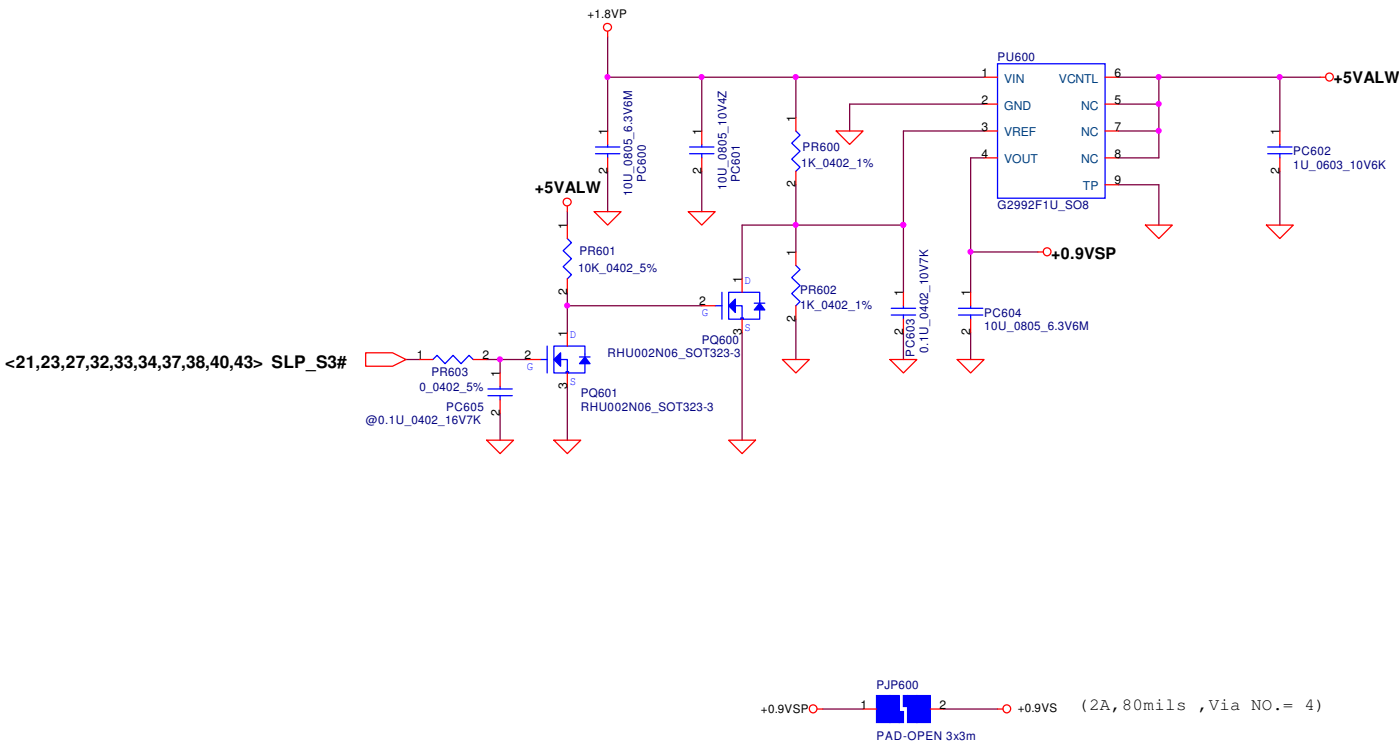
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Size	Document Number	Rev		LA-3941P	
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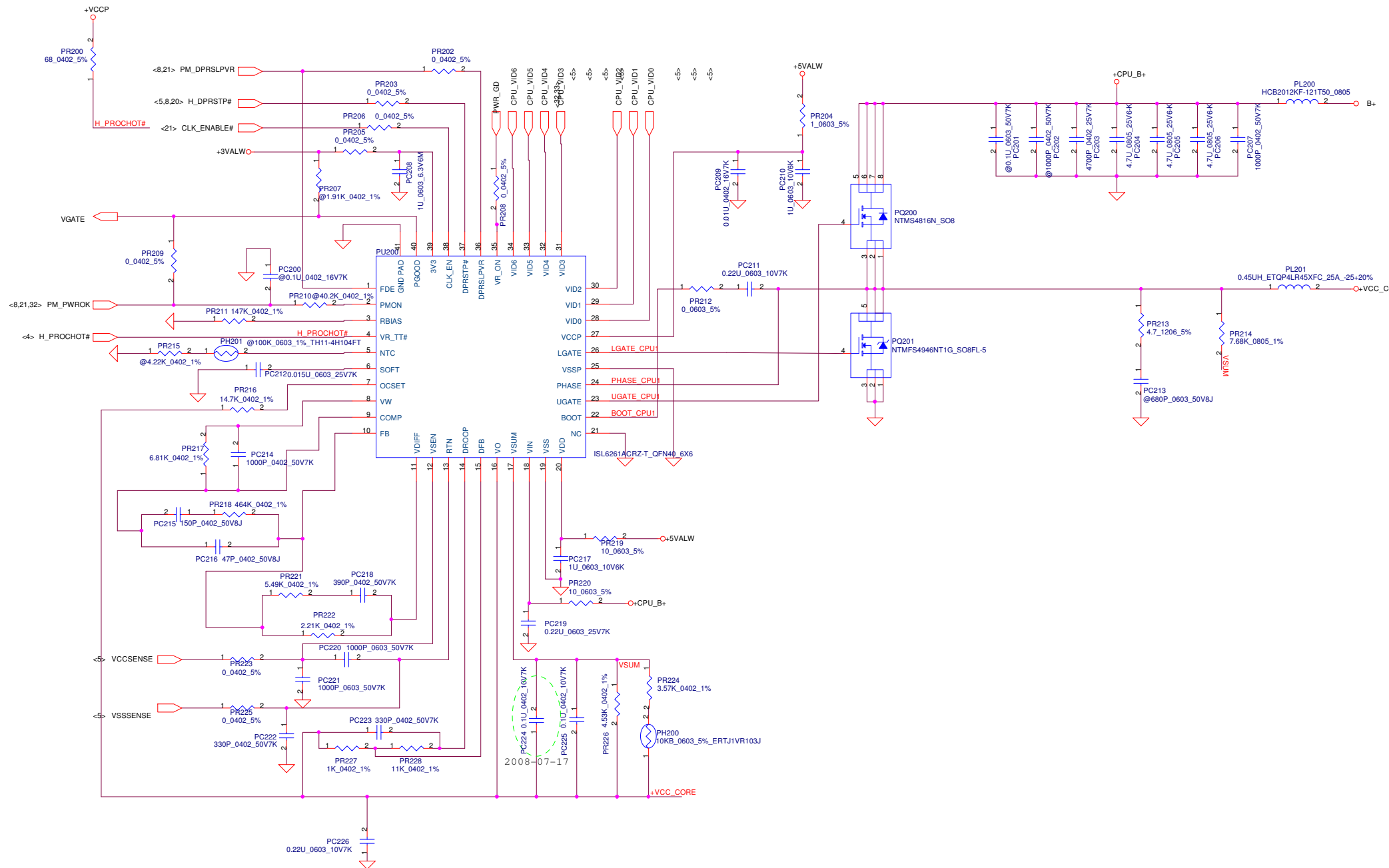
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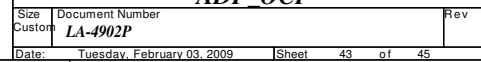


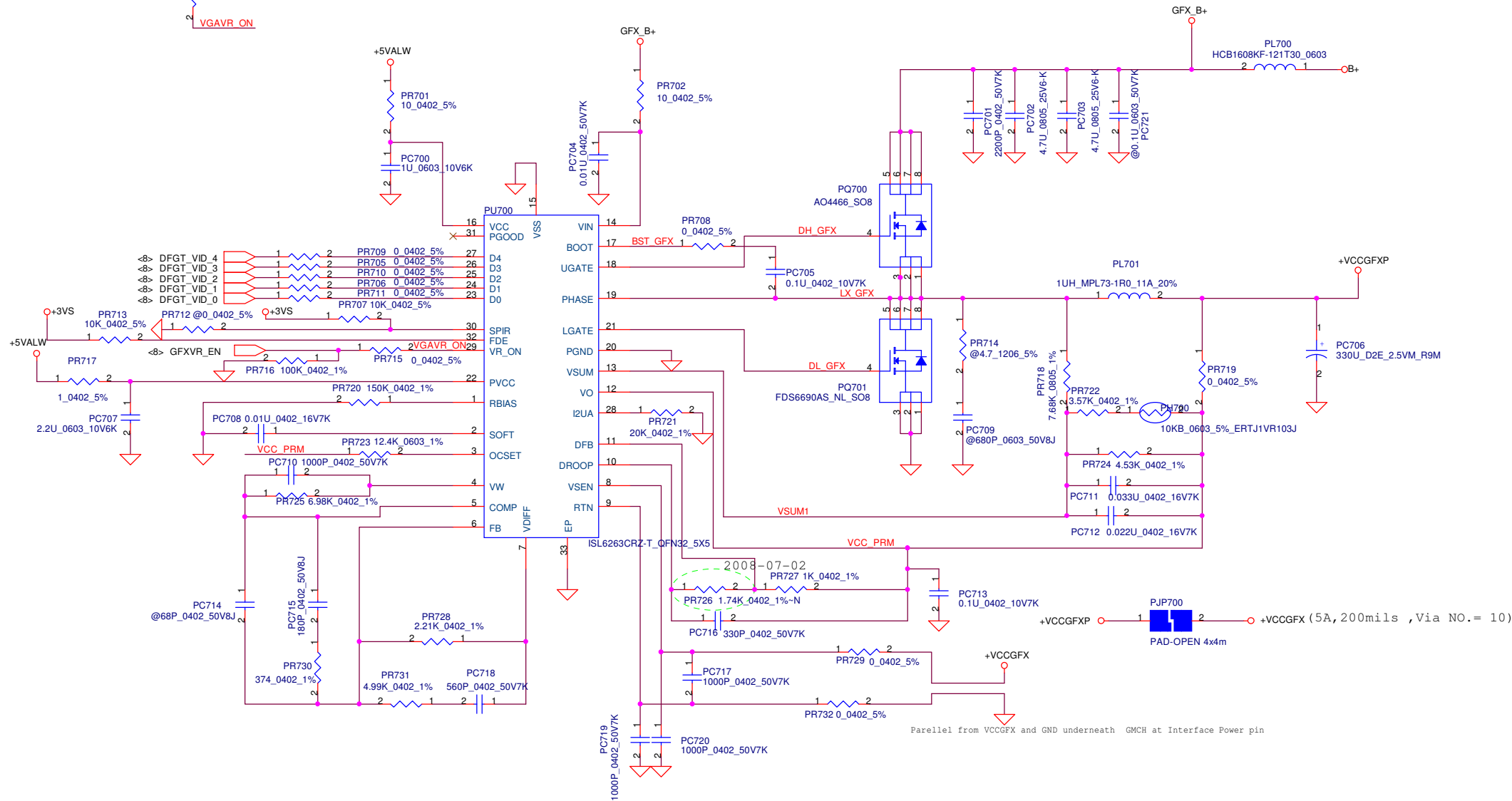


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