Wistron Confidential

MV1

2010/1/21 REV :MV-01

<Core Design>

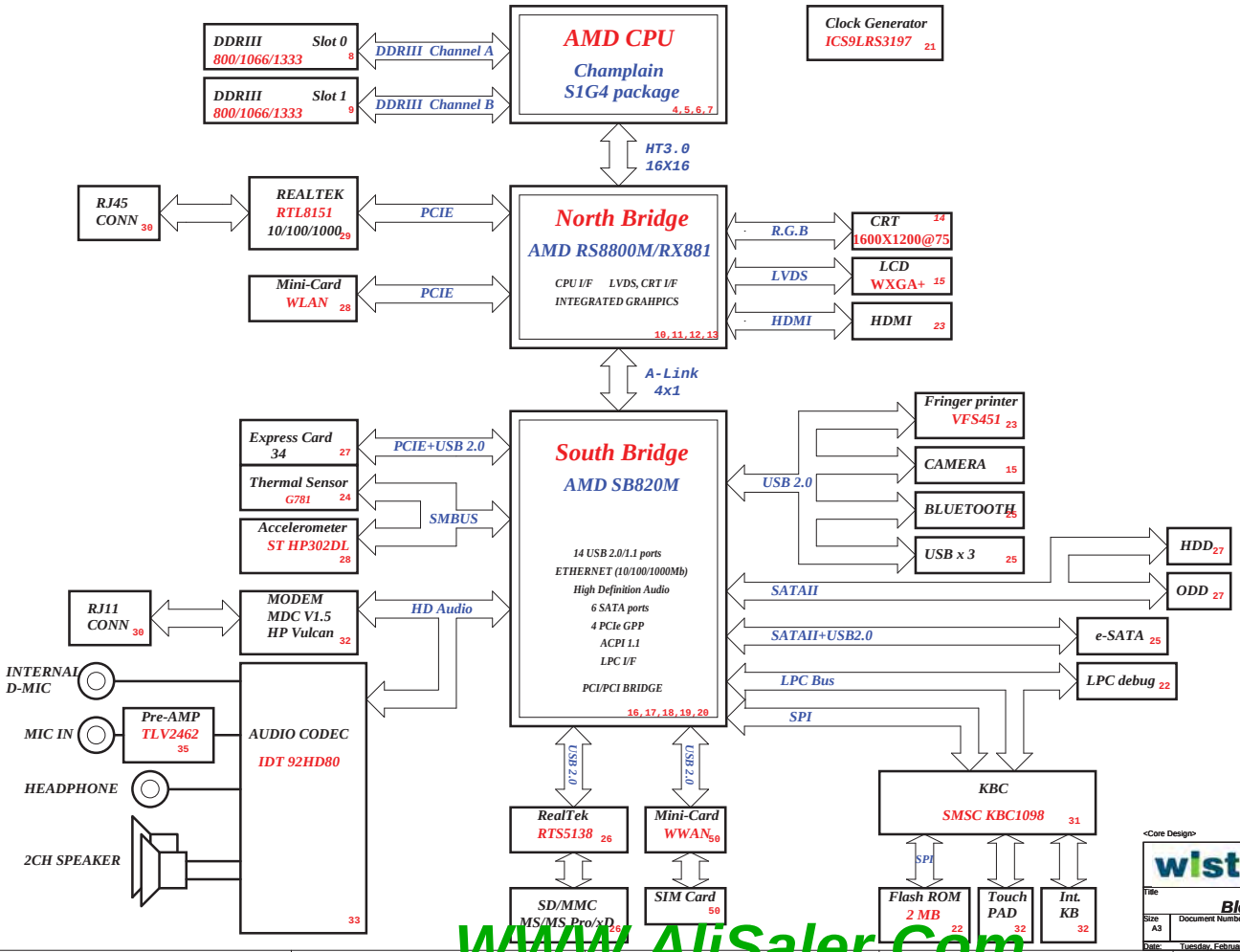
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Cover

Size	Document Number	Rev
A3	PATEK	-1

Date: Thursday, January 21, 2010 Sheet 1 of 50

Patek UMA Block Diagram



SYSTEM DC/DC RT8205A	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +VL +3VALW +3VL 39

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
+5VALW	+1.1VALW 41

SYSTEM DC/DC G972	
INPUTS	OUTPUTS
+3VS	+1.8VS 38

SYSTEM DC/DC G9091/RT9205	
INPUTS	OUTPUTS
+3VS	+2.5VS_LDO_CPU
+1.5VS	+1.05VS 37

SYSTEM DC/DC RT8207	
INPUTS	OUTPUTS
+5VALW	+1.5V +0.75V 40

MAXIM CHARGER BQ24740	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 43

CPU DC/DC ISL6265/RT8209B	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE +VDDNB 36
+5VALW	+NB_VDDC 46

PCB 6 LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Block Diagram

Size	Document Number	Rev
A3	PATEK	-1

Date: Tuesday, February 09, 2010 Sheet 2 of 50

RS880M strapping

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC)
0 : Enable *1 : Disable

RS880: Enables Side port memory (RS880 use HSYNC)

*0 : Enable 1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

PCIE routing

Page 10

LANE 0	LAN
LANE 3	NEW CARD
LANE 4	WLAN

USB table

Page 19

Pair	Device
USB-FSD1 FPR	
USB-9 Bluetooth	
USB-8 WLAN	
USB-7 WWAN	
USB-6 USB Card Reader	
USB-5 Right Side	
USB-4 USB Camera	
USB-3 Right Side	
USB-2 Left Side (e-SATA combo)	
USB-1 New Card	
USB-0 Left Side (S/W Debug port)	

SB820M strapping

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK_KBC (LPCCLK0)	LPC_CLK_DB (LPCCLK1)	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	SB-TSI
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SB_SMB_CLK1 SB_SMB_DAT1	SB820M	X	X	X	X	X	X	X
SB_SMB_CLK0 SB_SMB_DAT0	SB820M	X	V	V	V	V	X	X
CPU_SIC_SB700 CPU_SID_SB700	CPU	X	X	X	X	X	X	V

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: NOTES

Size: A3 | Document Number: PATEK | Rev: -1

Date: Thursday, January 21, 2010 | Sheet 3 of 50

CPU VLDT MAX 1.5A

LAYOUT: PLACE CLOSE TO CPU ALONG HT POWER SHAPE

1207

1028

CPU1A

SEC 1 OF 6 LDT

S1G3 & S1G4 not support LDT_REQ#

<Core Design>

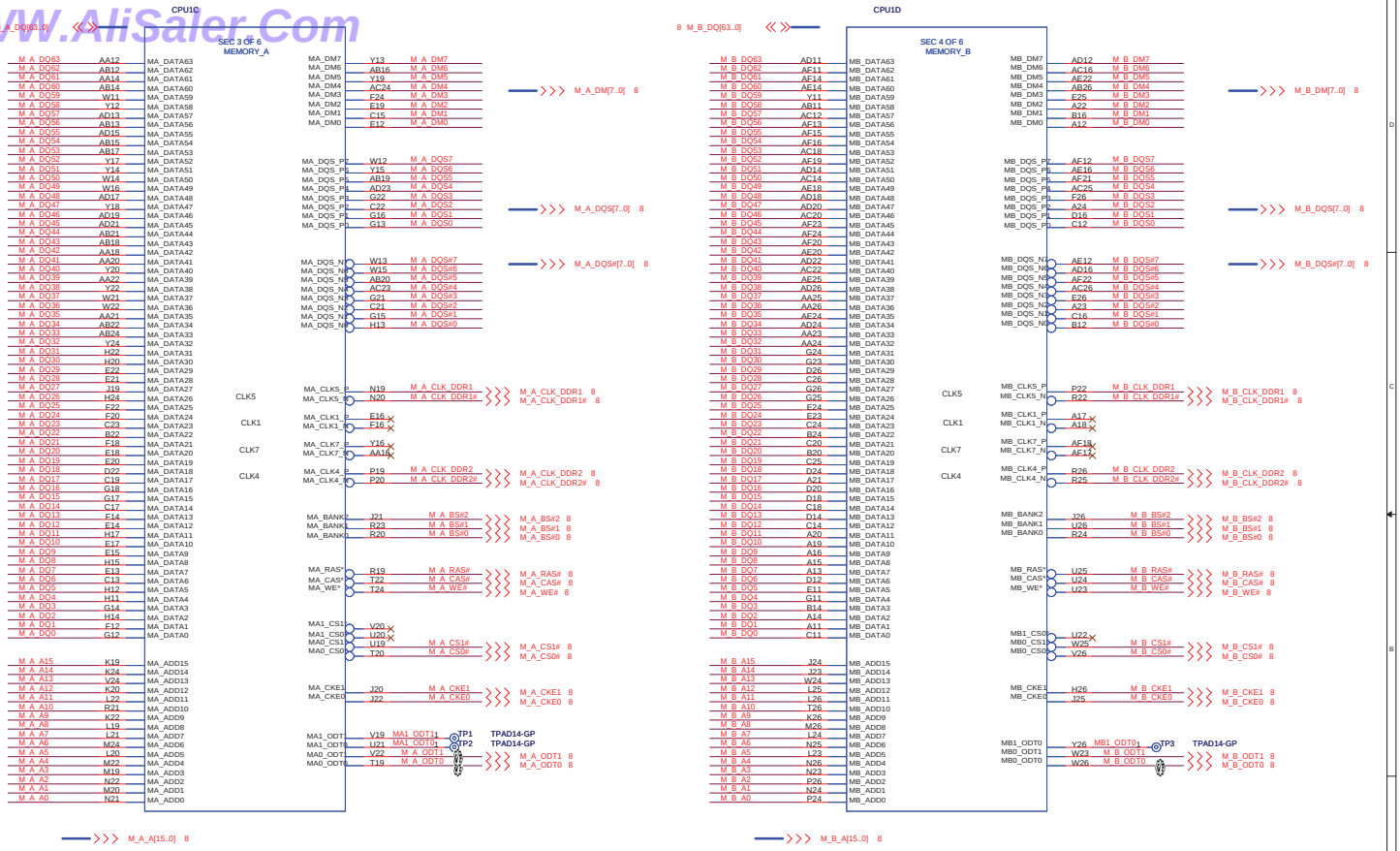
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU(1/4) HT

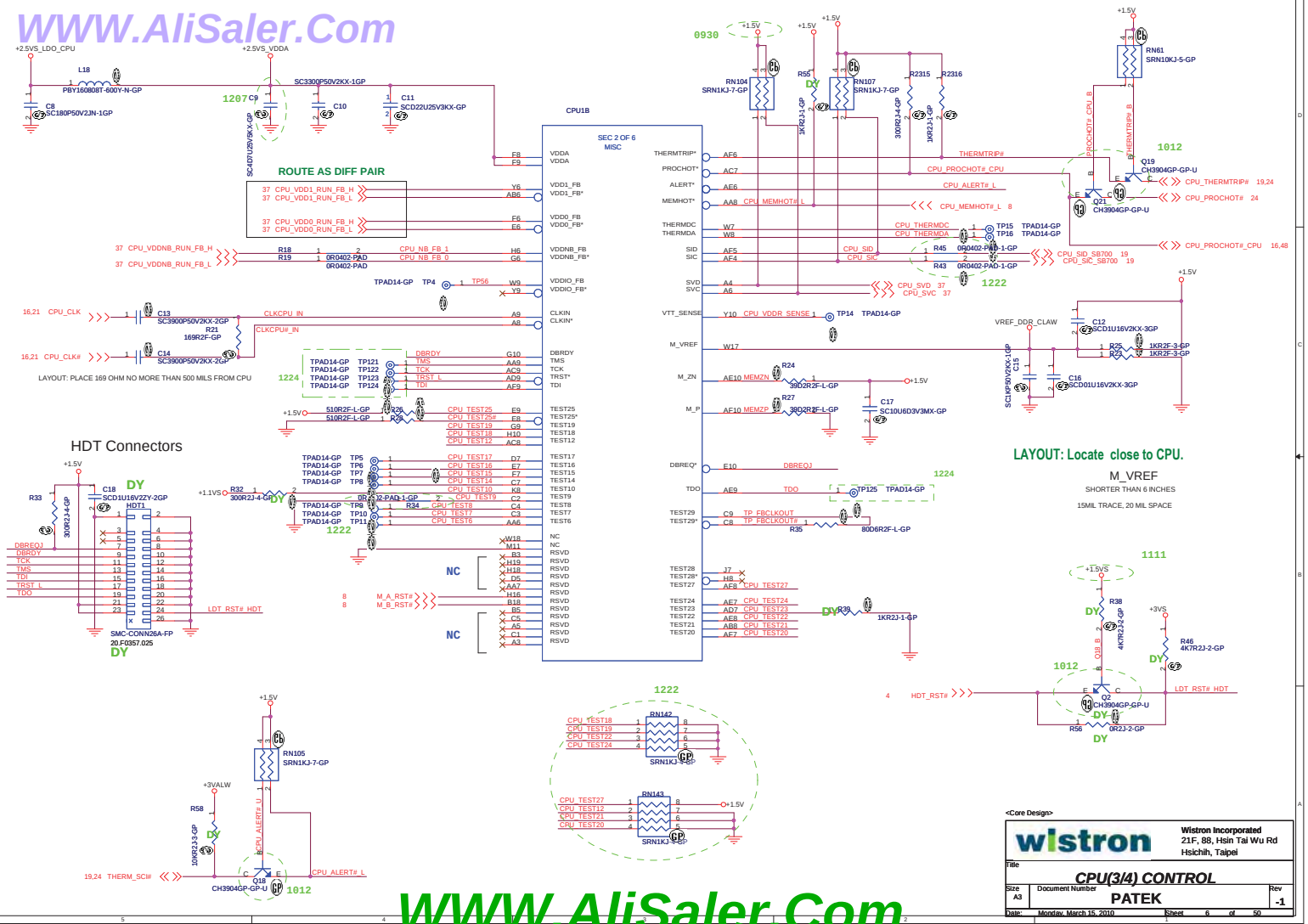
Size: A3 | Document Number: PATEK | Rev: -1

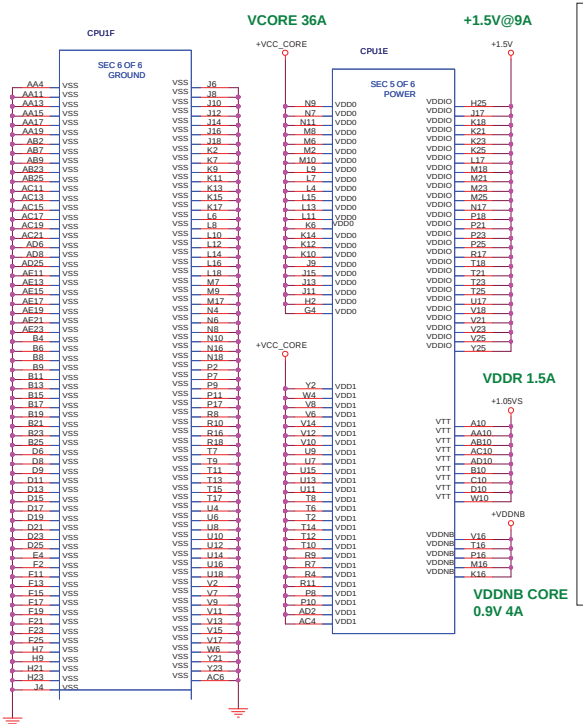
Date: Monday, March 15, 2010 | Sheet 4 of 50



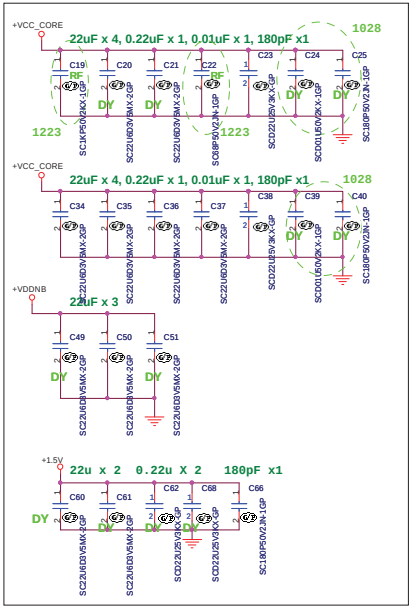
<Core Design>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	CPU(2/4) DDR III	
Size A3	Document Number PATEK	Rev -1
Date: Monday, March 15, 2010	Sheet 5 of 50	



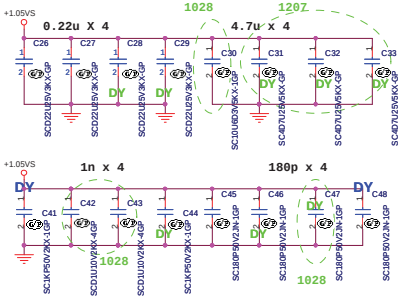


LAYOUT: PLACE UNDER CPU ON BACK



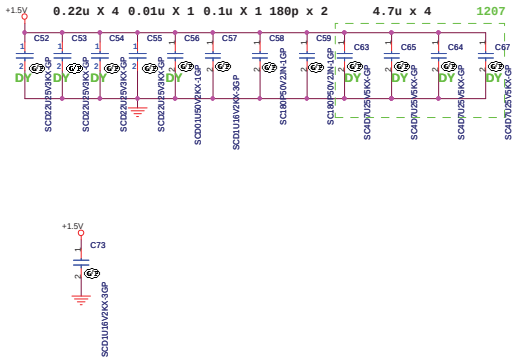
CPU MEMORY VTT

LAYOUT: PLACE CLOSE TO CPU socket



CPU VDDIO

LAYOUT: PLACE CLOSE TO CPU BETWEEN CPU AND MEMORY

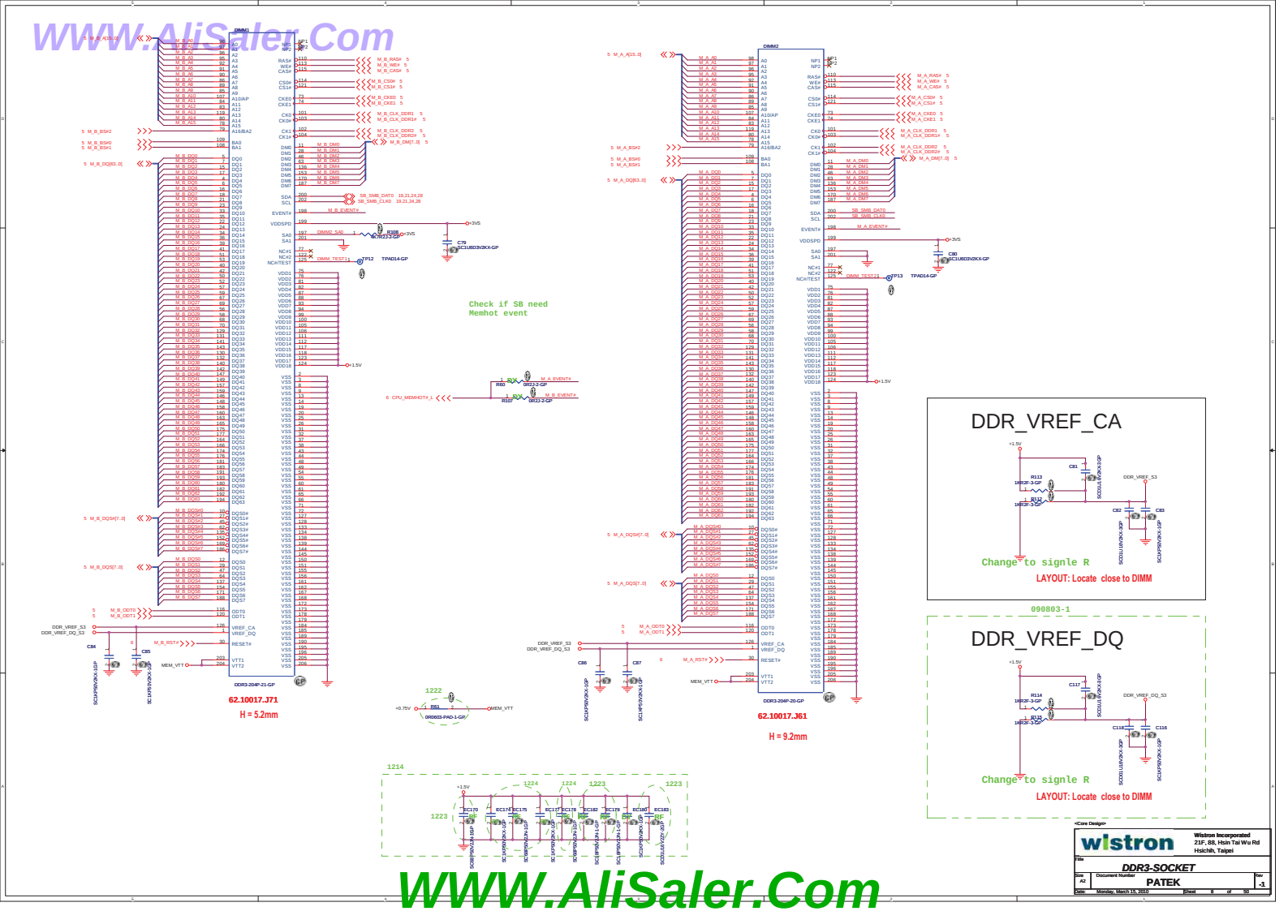


<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU(4/4) POWER

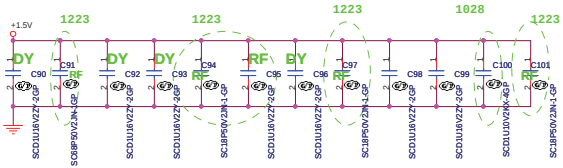
Size: A3 | Document Number: PATEK | Rev: -1

Date: Thursday, January 21, 2010 | Sheet 7 of 50

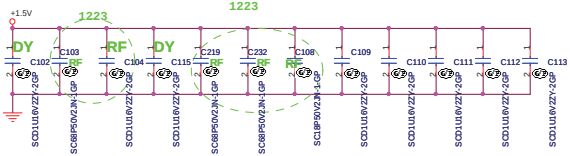


DE-COUPLING FOR CHANNEL A SODIMM

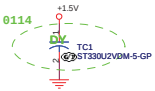
DE-COUPLING FOR CHANNEL B SODIMM



DE-COUPLING FOR CHANNEL A SODIMM (ONE CAP PER POWER PIN)



DE-COUPLING FOR CHANNEL B SODIMM (ONE CAP PER POWER PIN)



<Core Design>

wistron

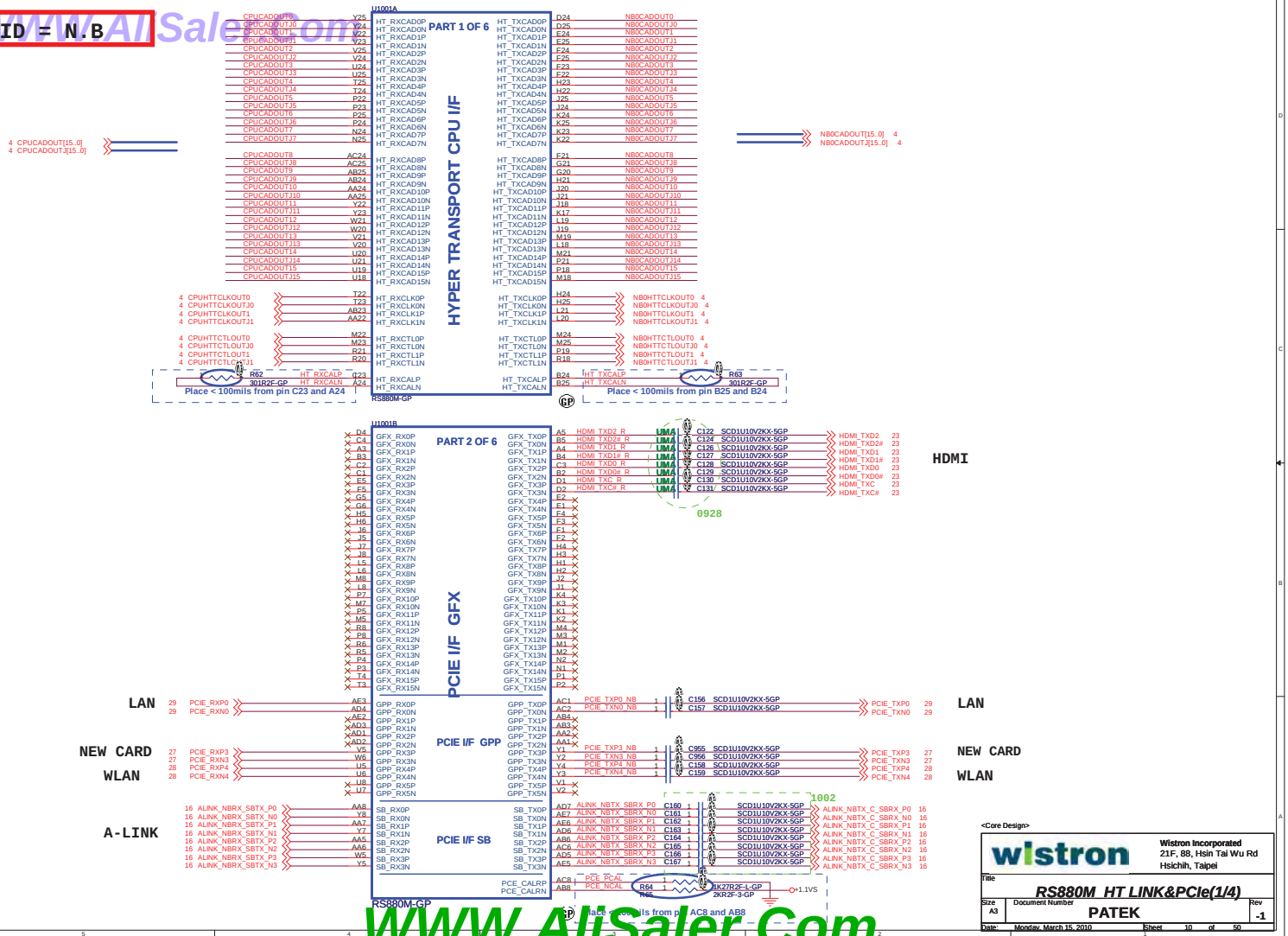
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DDR3-RESISTOR/CAP

Size: A3 | Document Number: PATEK | Rev: -1

Date: Thursday, January 21, 2010 | Sheet 9 of 50

SSID = N.B



STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable

RS880: Enables Side port memory (RS880 use HSYNC)
0 : Enable * 1 : Disable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

Close to NB ball

ENABLE External CLK GEN

	GPIO MODE	
STRP_DATA	0	1
NB_VDDC	1.1V	0.95V

RS880M-GP

RX881 NC

090709-1

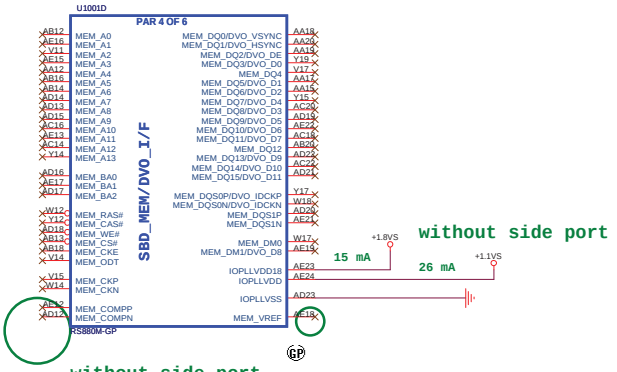
<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M_LVDS&CRT(2/4)

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 11 of 50



<Core Design>

wistron

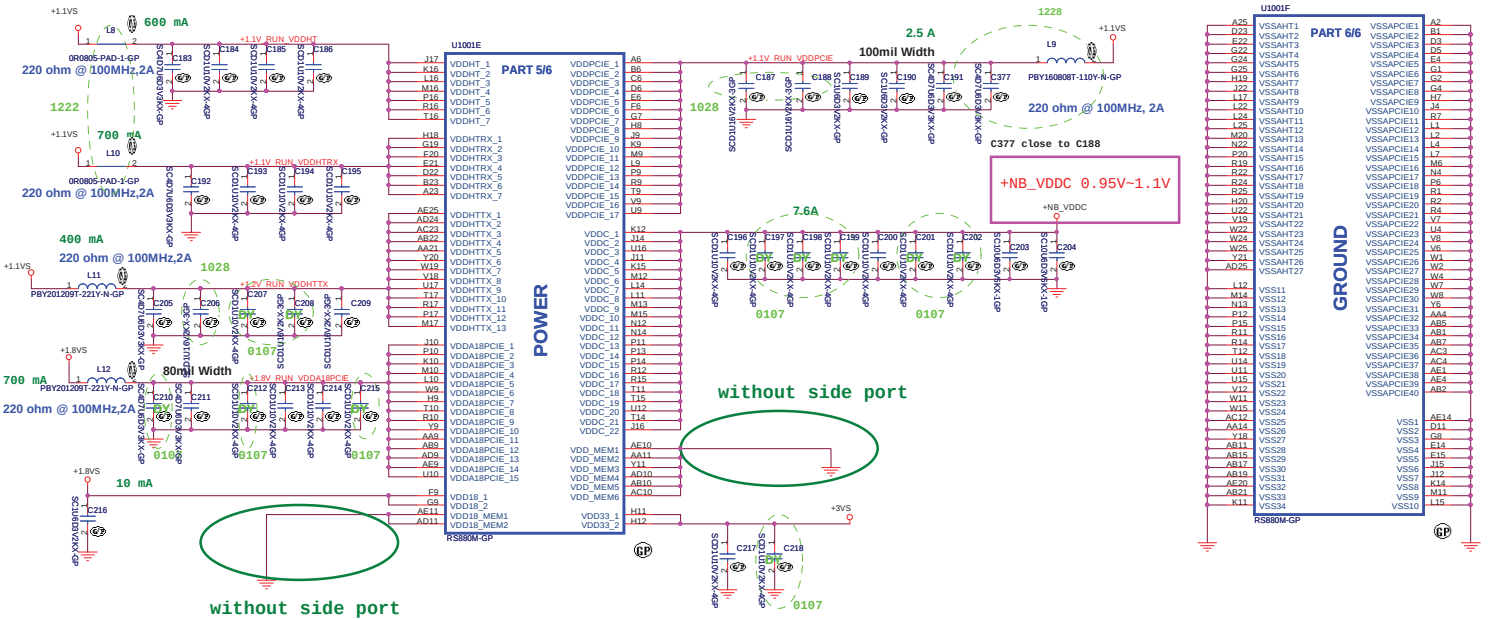
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M Side Port(3/4)

Size: A3 | Document Number: PATEK | Rev: -1

Date: Thursday, January 21, 2010 | Sheet 12 of 50

SSID = N.B



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M PWR&GND(4/4)

Size: A3 | Document Number: PATEK | Rev: -1

Date: Thursday, January 21, 2010 | Sheet 13 of 50

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

1026

11 VGA_RED
11 VGA_GREEN
11 VGA_BLUE

L13 NBQ160808T-470Y-N-GP
L14 NBQ160808T-470Y-N-GP
L15 NBQ160808T-470Y-N-GP

CRT_R
CRT_G
CRT_B

R100 10R2F-1-GP
R101 150R2F-1-GP
R102 140R2F-GP

C221 C222 C223 C224 C225 C226
SC10P50V2JN-4GP

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

+5VS_CRT

1221
EC253 SC1U6D3V2KX-GP
C1193 EMI
C220 SCD1U16V2ZY-2GP

Q87 DMP2305U-7-GP
F1 FUSE-1D1A6V-4GP-U
+5VS_CRT_FUSE
69.50007.691
1203

R1248 10KR2J-3-GP
R1249 10KR2J-3-GP
CRTVDD_EN

CRT1
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND
D-SUB-15-27-GP-U2
20.20847.015
1018

DDC_CRT_DAT
DDC_CRT_CLK
CRT_R
CRT_G
CRT_B
JVGA_VS
JVGA_HS

Q88 2N7002E-1-GP
SB_PWRGD 19,31
C1194 SCD1U16V2ZY-2GP

C230 DY
C229 DY
C227 DY
C228 DY
SC2P50V2JN-4GP
SC3P50V2JN-3GP

AFTE14P-GP AFTP82 CRT_R
AFTE14P-GP AFTP85 CRT_G
AFTE14P-GP AFTP86 CRT_B
AFTE14P-GP AFTP87 GND
AFTE14P-GP AFTP88 +5VS_CRT

+5VS_CRT
RN11 SRN4K7J-8-GP
DDC_CRT_CLK 11
DDC_CRT_DAT 11

DDC_CRT_DAT& DDC_CRT_CLK
The signal is 5V-tolerant on RS880M.

+5VS_CRT
1010
C231 SCD1U16V2KX-3GP

11 VGA_HSYNC
11 VGA_VSYNC

U3 74AHCT1G125GW-1-GP
U4 74AHCT1G125GW-1-GP
OE# VCC A GND Y

HSYNC_5
VSYNC_5

RN12 SRN33J-5-GP-U
JVGA_HS
JVGA_VS

Hsync & Vsync level shift

ESD
close to connector

+5VS_CRT
CRT_R
D3 BAV99-8-GP

D5 BAV99S-GP
DDC_CRT_CLK
DDC_CRT_DAT

D6 BAV99S-GP
CRT_B
CRT_G

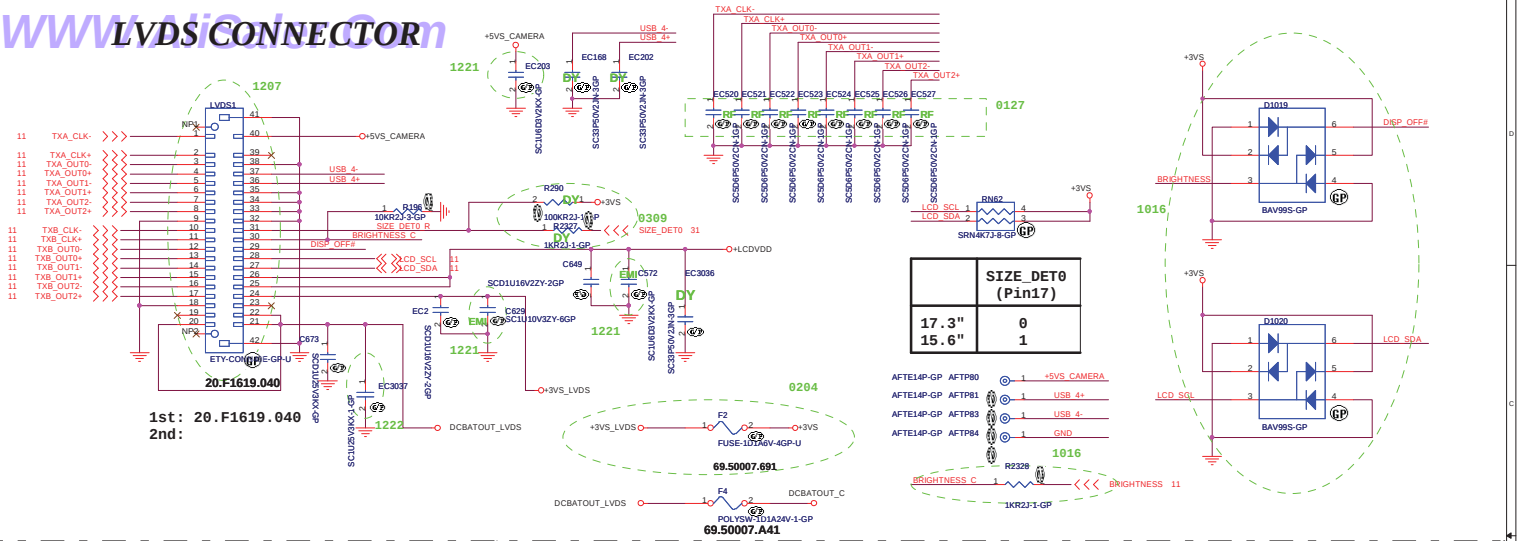
D4 BAV99S-GP
JVGA_HS
JVGA_VS

<Core Design>

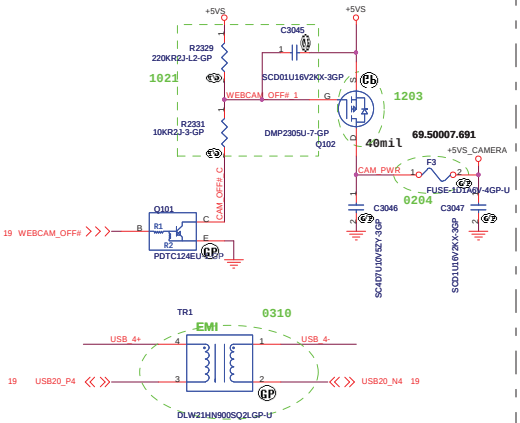
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CRT CONNECTOR
Size: A3
Document Number: PATEK
Rev: -1
Date: Monday, March 15, 2010
Sheet 14 of 50

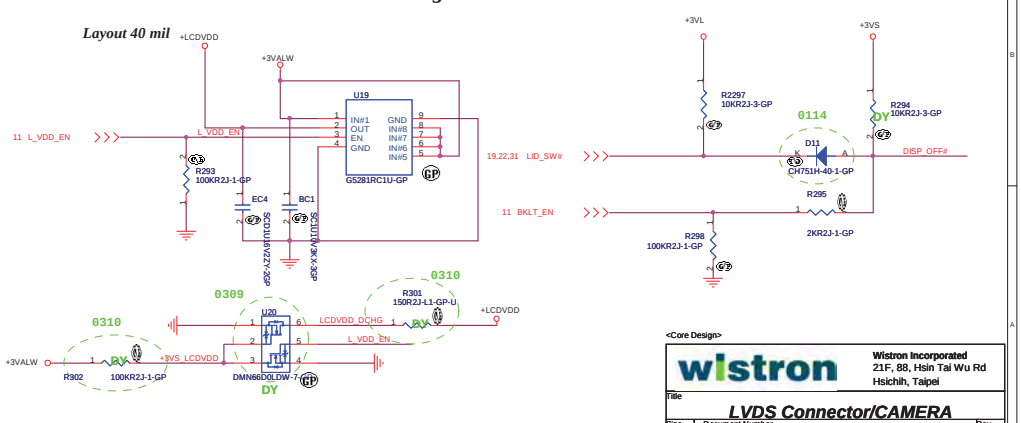
LVDS CONNECTOR



Camera Power&Interface



LCD Power&Discharge

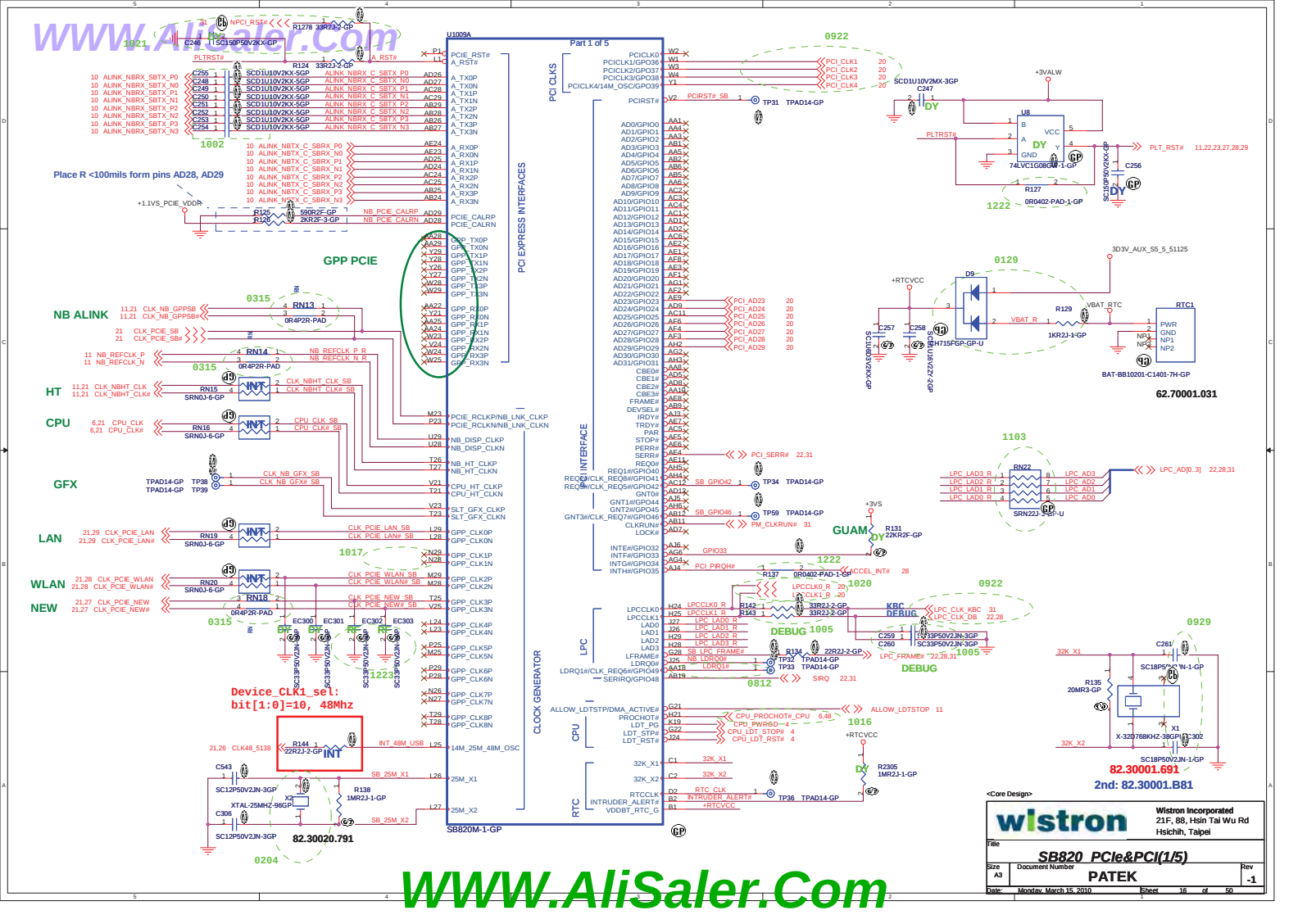


<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LVDS Connector/CAMERA

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 15 of 50



<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SB820 PCIe&PCI(1/5)

Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 16 of 50

SSID = S.B

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700

SATA HDD

SATA ODD

ESATA

Very Close to SB820

U1009B

Part 2 of 5

SB820M-1-GP

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SB820 SATA&IDE(2/5)

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 17 of 50

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

U1009C
Part 3 of 5

POWER

131mA
71mA
GPIOD not used
43mA
600mA
93mA
567mA
658mA
TBDmA
510mA
TBDmA
32mA
113mA
TBDmA
197mA
47mA
62mA
17mA
5mA
GBE PHY not used
Close to SB820
20mil Width
Close to SB820
20mil Width
42R 4A
42R 4A
42R 4A
Decoupled along with the
VDDAN_33_USB_S power rail.
Separate ferrite bead or
additional capacitors are not required

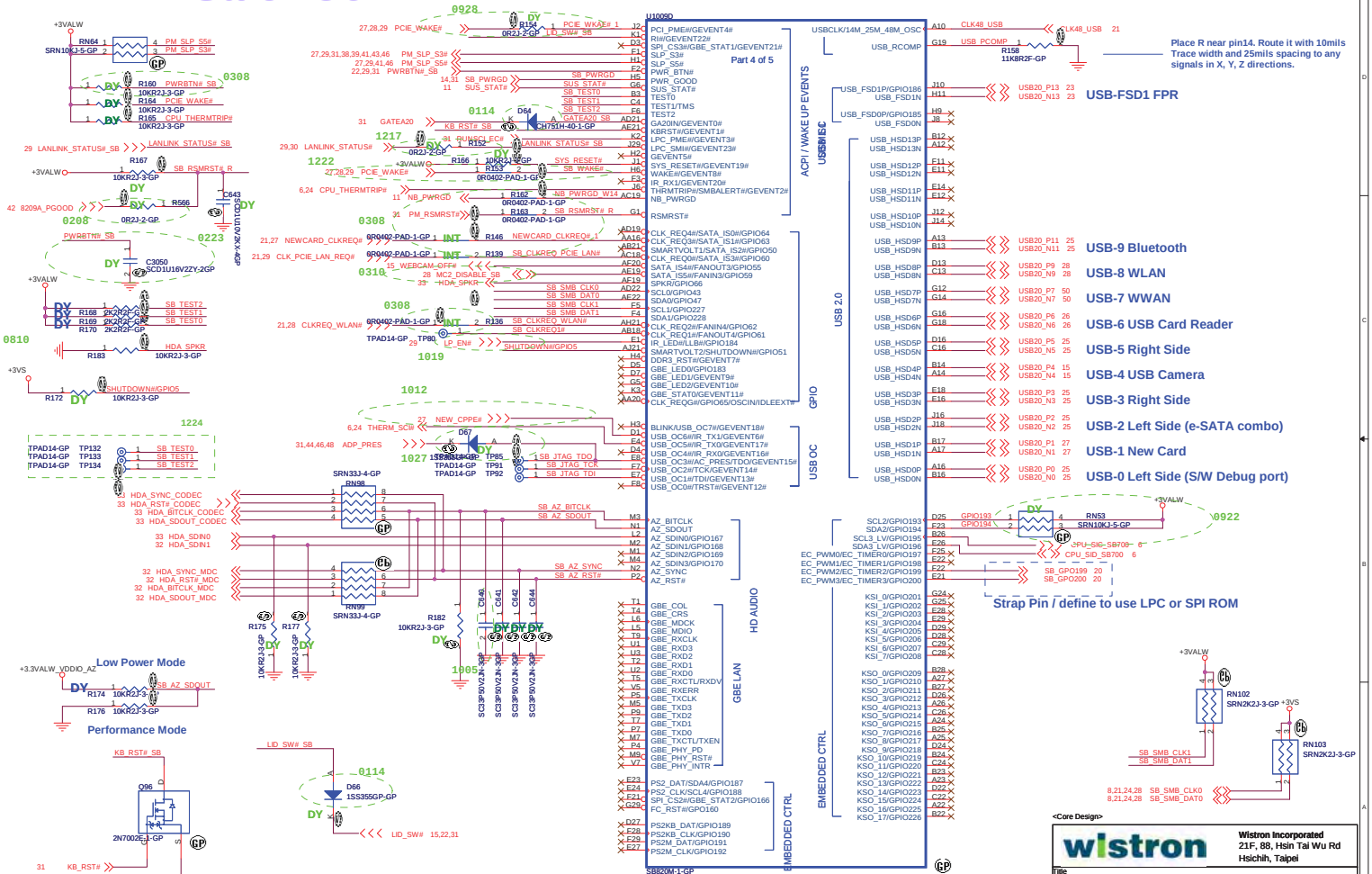
U1009E
Part 5 of 5
GROUND

<Core Design>

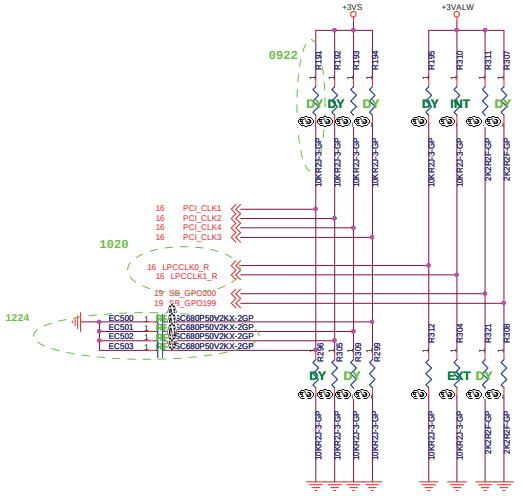
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SB820 PWR&GND(3/5)
Size: A3
Document Number: PATEK
Rev: -1
Date: Monday, March 08, 2010
Sheet 18 of 50

SSID = S.B



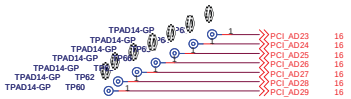
REQUIRED STRAPS



USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPCCLK0_R	LPCCLK1_R	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

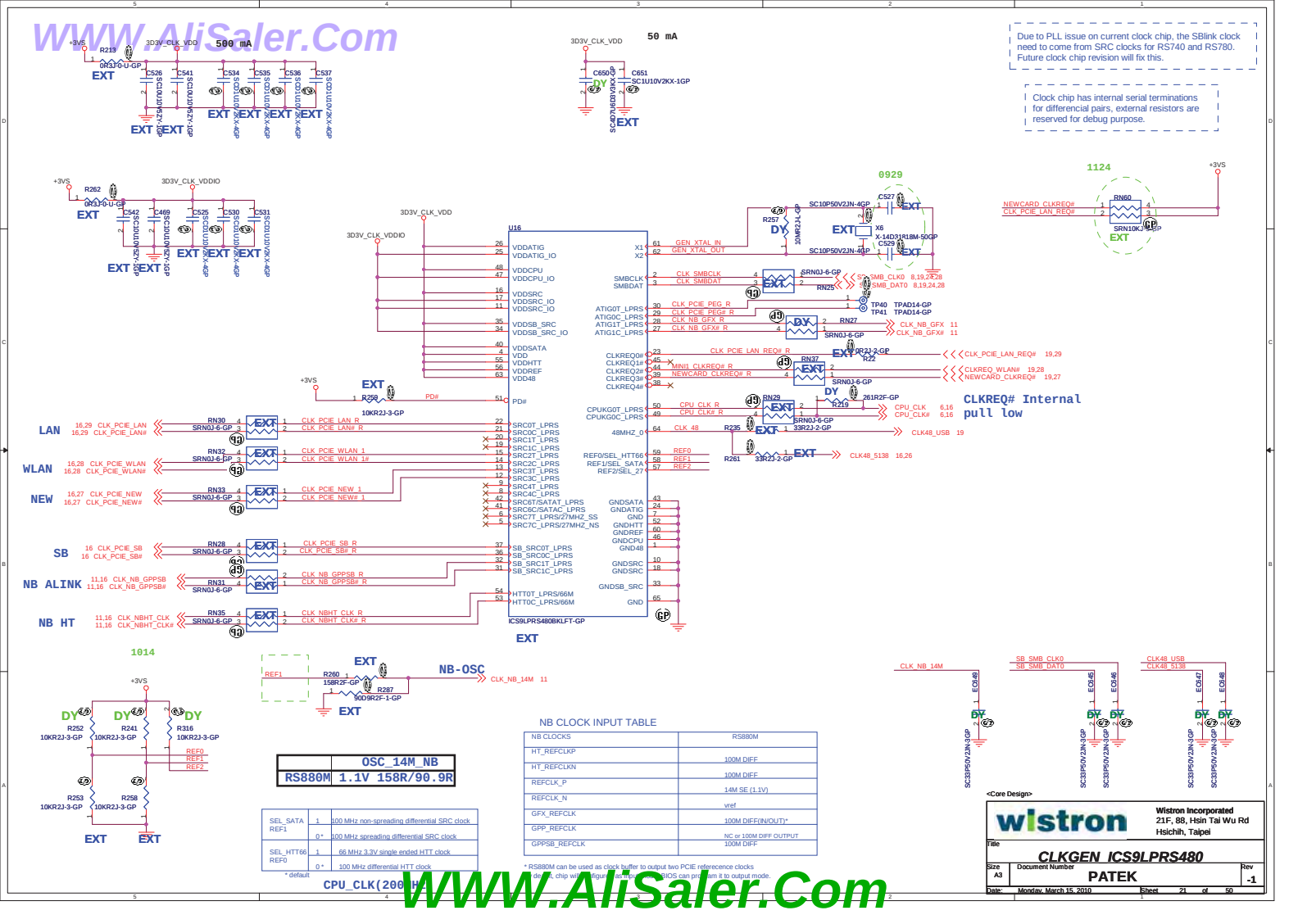
Title: SB820 STRAPPING(5/5)

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 20 of 50

Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

* RS880M can be used as clock buffer to output two PCIE refereccence clocks

SEL_SATA REF1		
	1	100 MHz non-spreading differential SRC clock
	0 *	100 MHz spreading differential SRC clock
SEL_HTT66 REF0	1	66 MHz 3.3V single ended HTT clock
	0 *	100 MHz differential HTT clock

* default

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

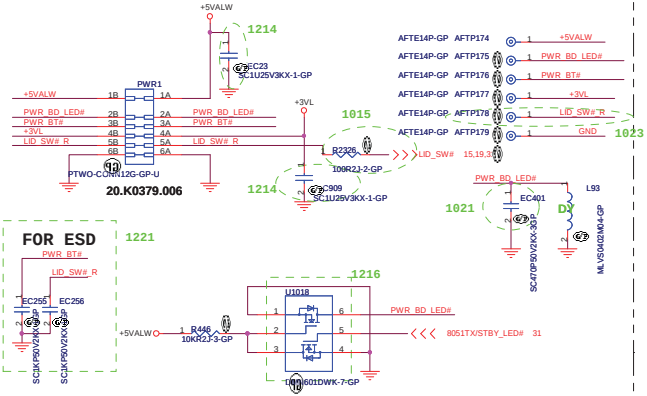
Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: PATEK | Rev: -1

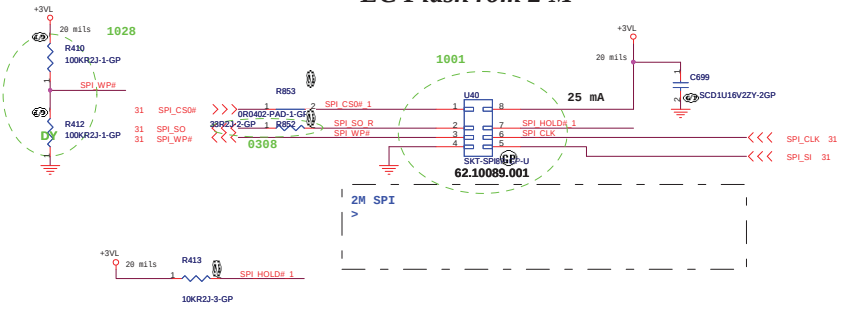
Date: Monday, March 15, 2010 | Sheet 21 of 50

POWER SW CONN.

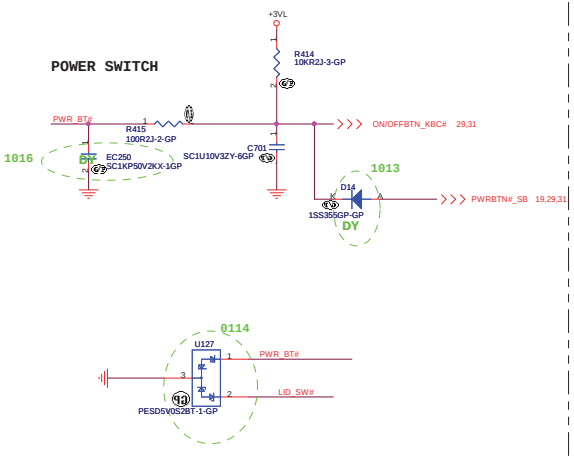
COVER SWITCH



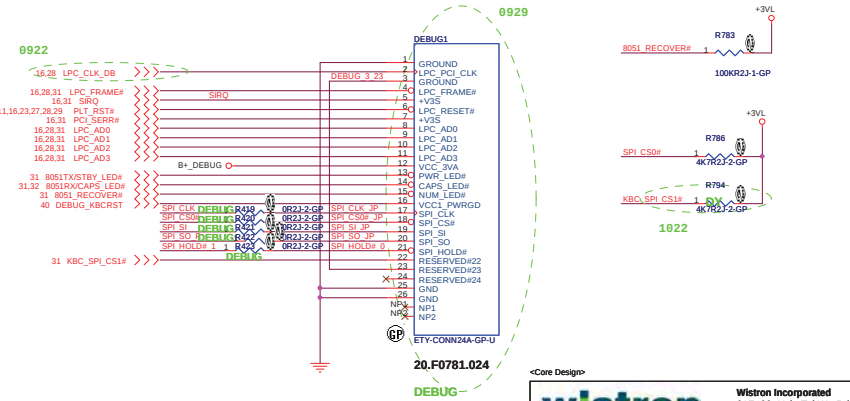
EC Flash rom 2 M



Power SW Circuit



24 PIN LPC DEBUG CONN.



<Core Design>

wistron

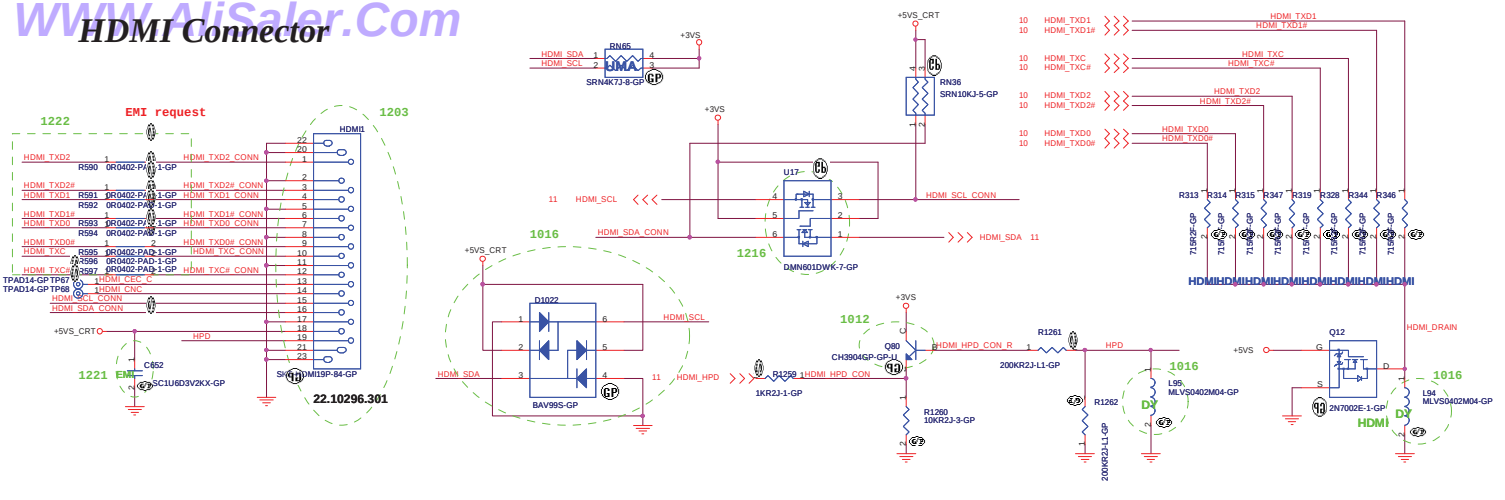
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BTN/ROM/DEBUG

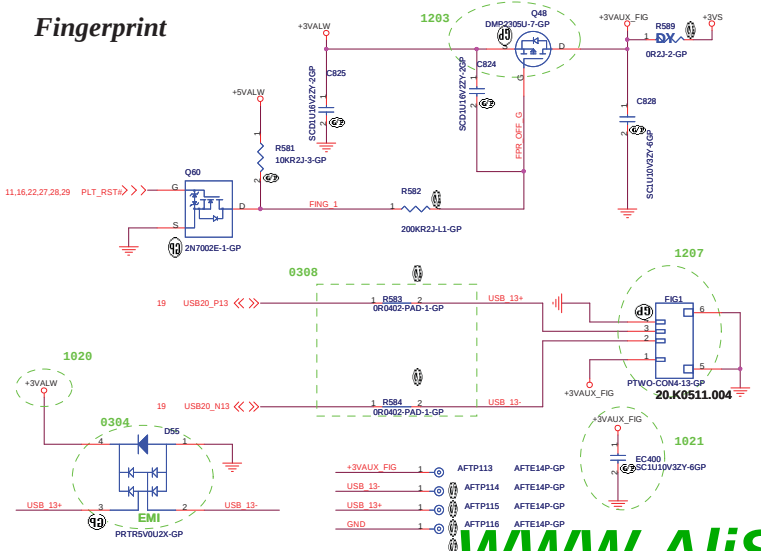
Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 22 of 50

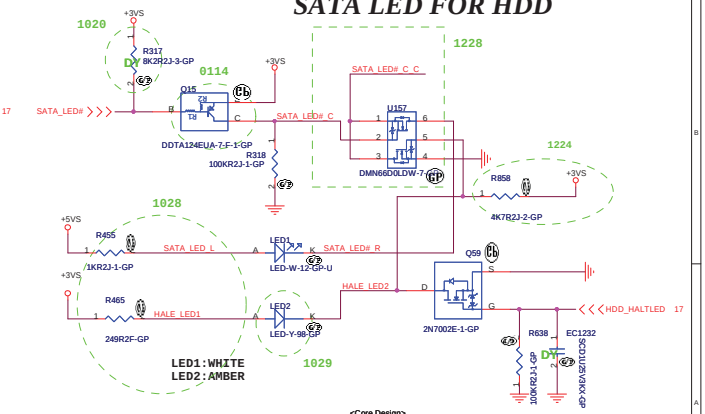
HDMI Connector



Fingerprint



SATA LED FOR HDD



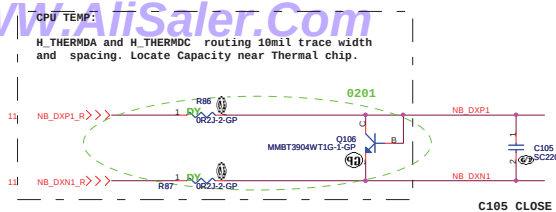
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDMI/FPR/SATA LED

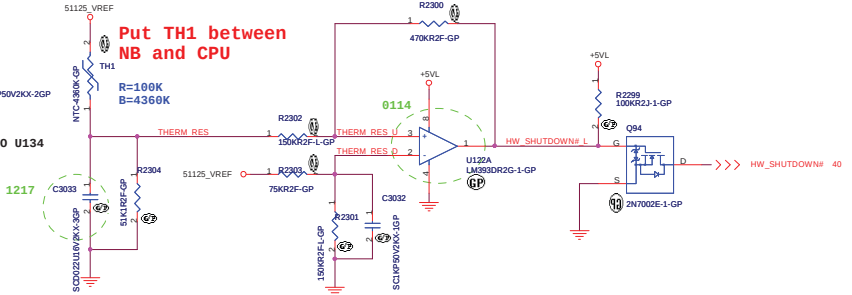
Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 23 of 50

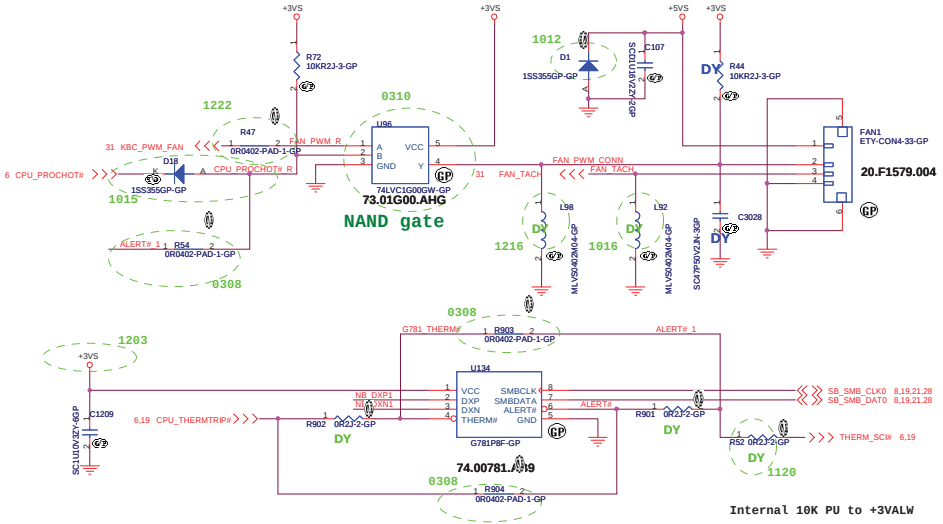
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal chip.

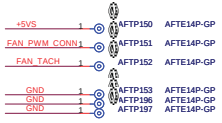


C105 CLOSE TO U134



4 WIRE PWM Fan Control Circuit





<Core Design>

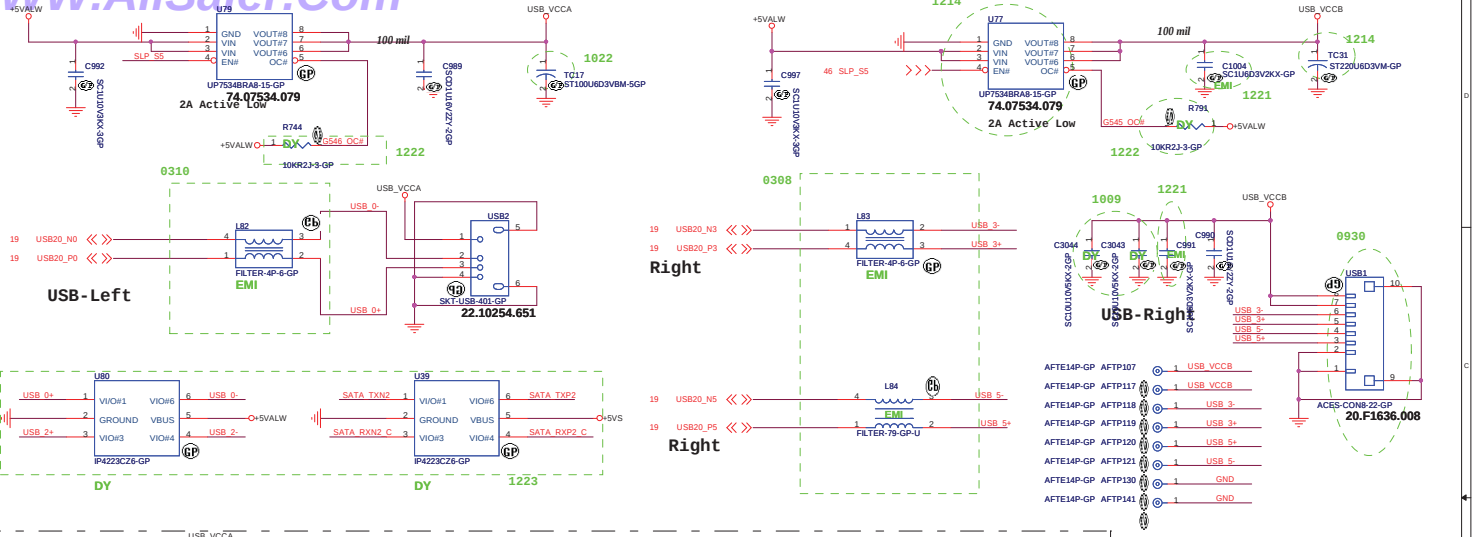
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: G781 THERMAL

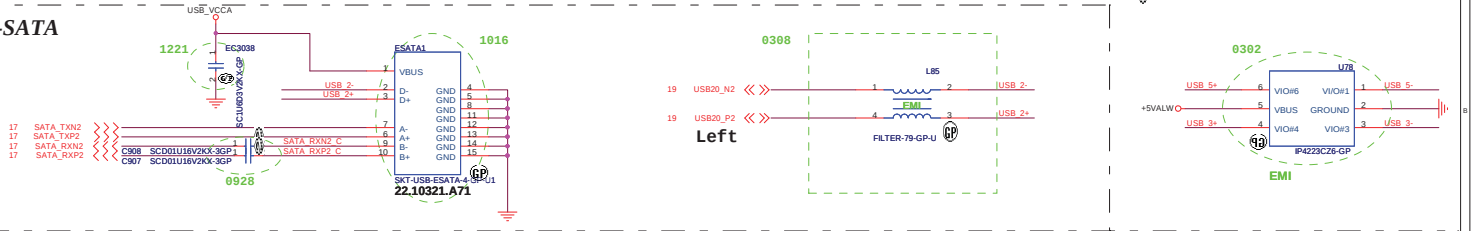
Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 24 of 50

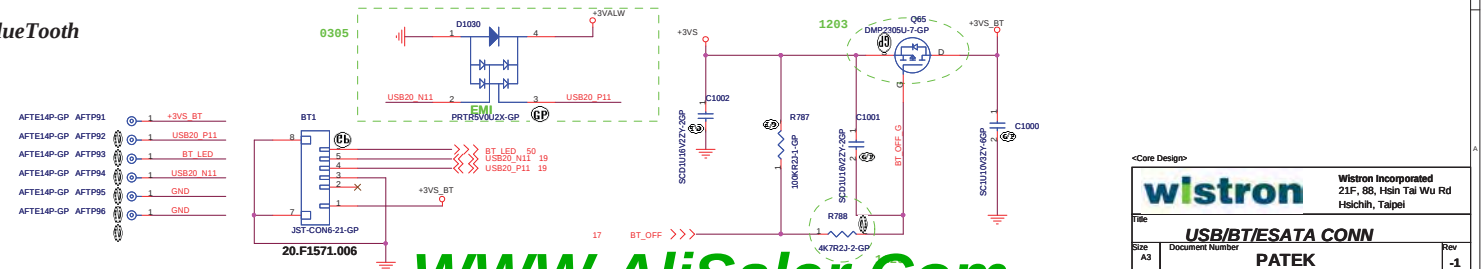
USB & E-SATA POWER



E-SATA



BlueTooth



<Core Design>

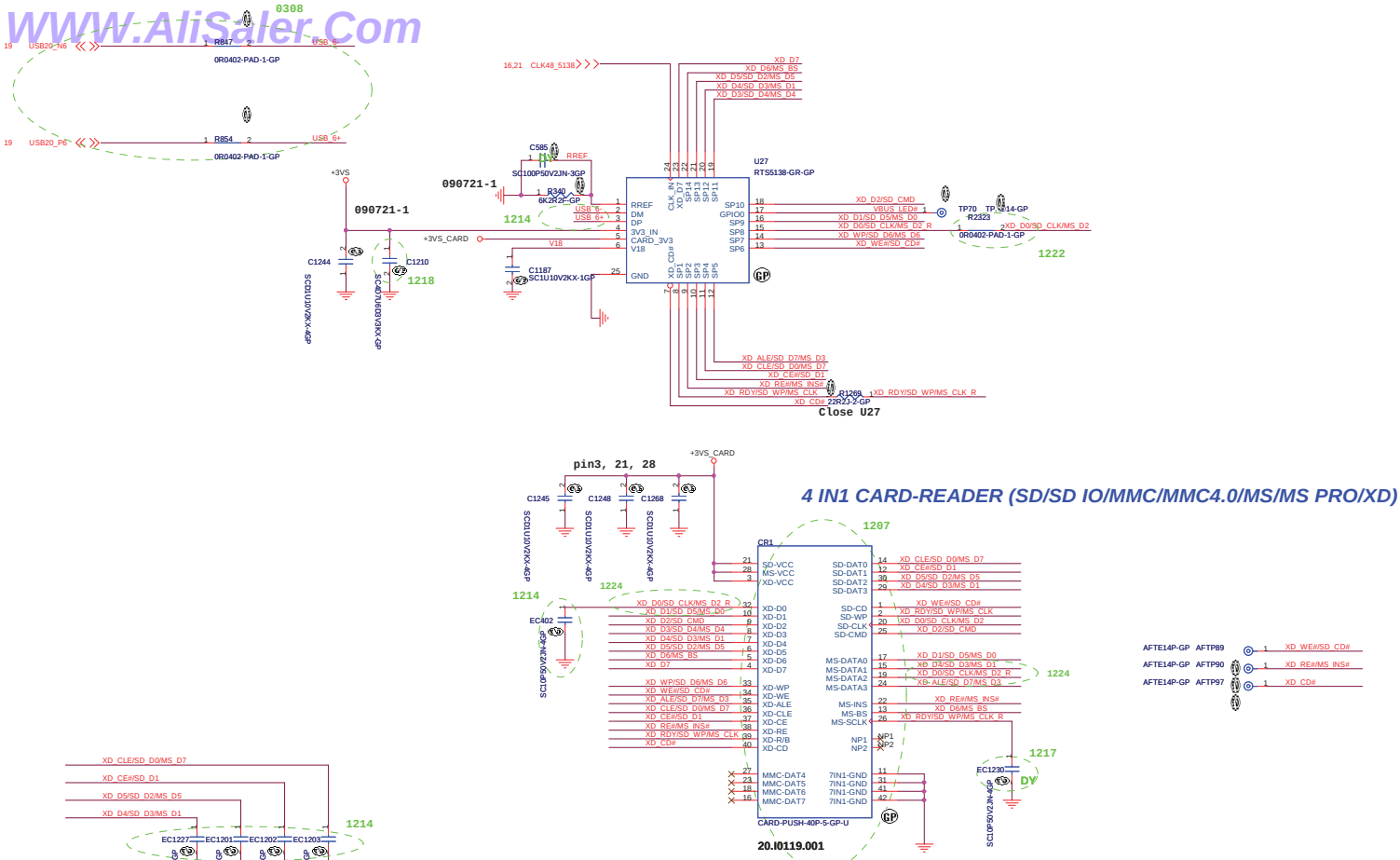
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB/BT/ESATA CONN

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 25 of 50



<Core Design>

wistron

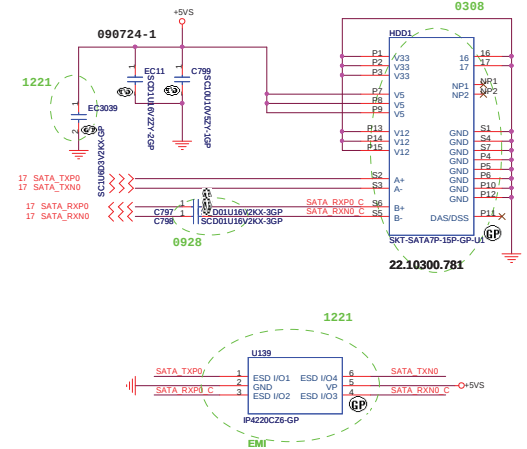
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CardReader RTS5138

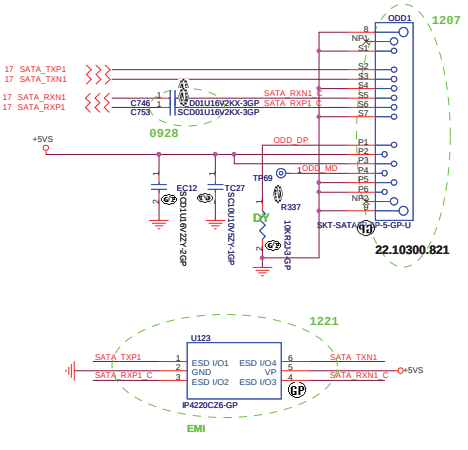
Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 26 of 50

SATA HD Connector

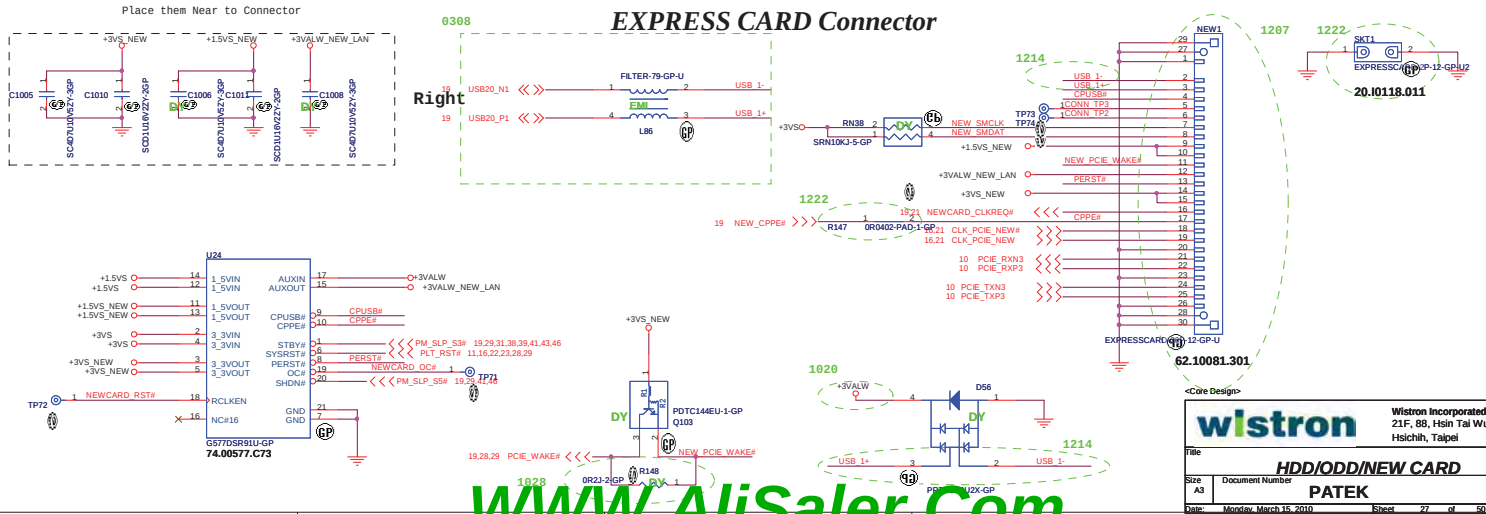


ODD Connector



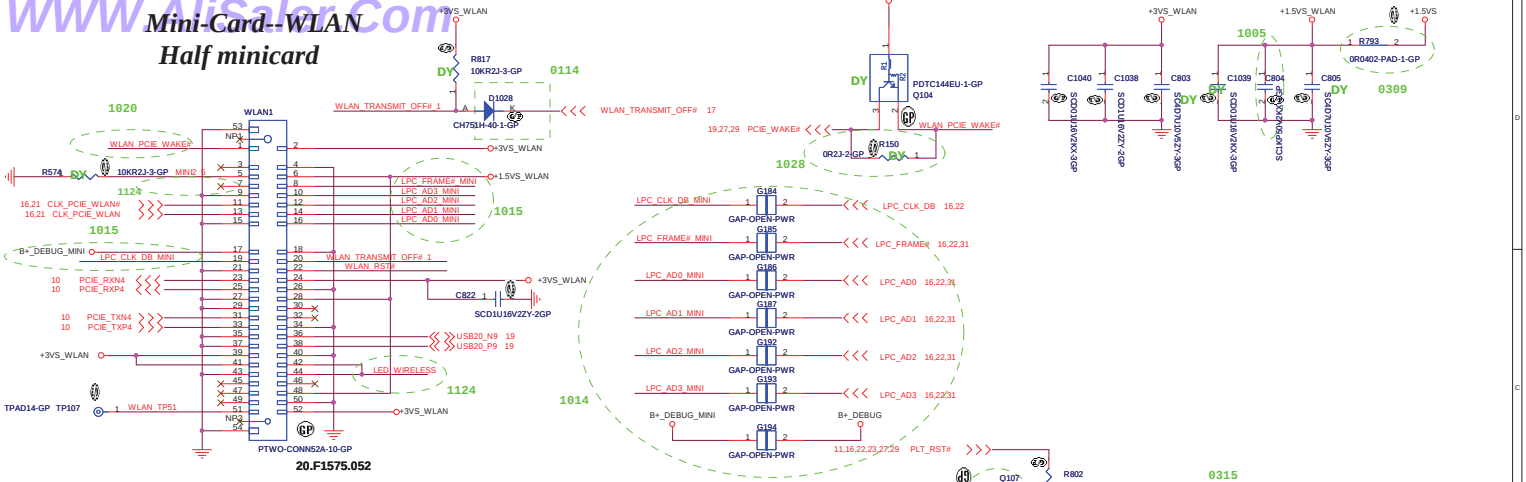
Place them Near to Connector

EXPRESS CARD Connector

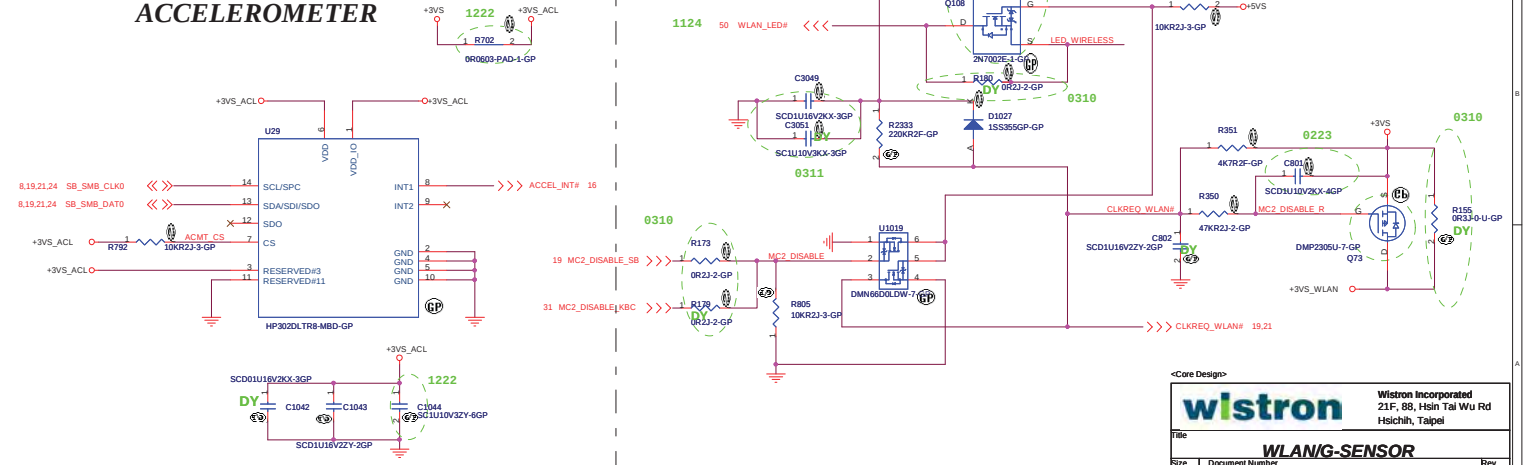


Wistron Incorporated	21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	HDD/ODD/NEW CARD
Size	A3
Document Number	PATEK
Rev	-1
Date:	Monday, March 15, 2010
Sheet	27 of 50

Mini-Card--WLAN
Half minicard



ACCELEROMETER



<Core Design>

wistron

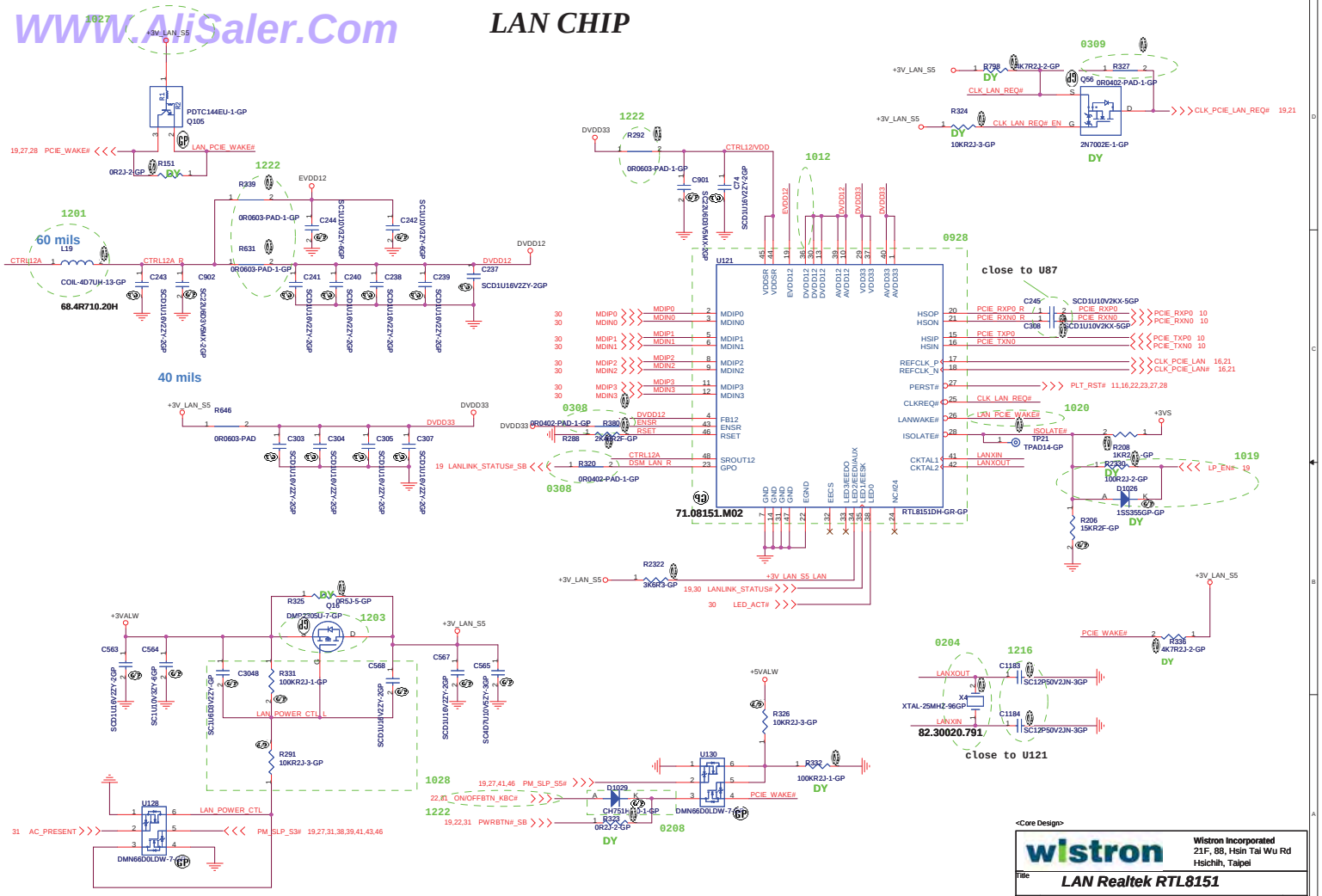
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: WLAN/G-SENSOR

Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 28 of 50

LAN CHIP



<Core Design>

wistron

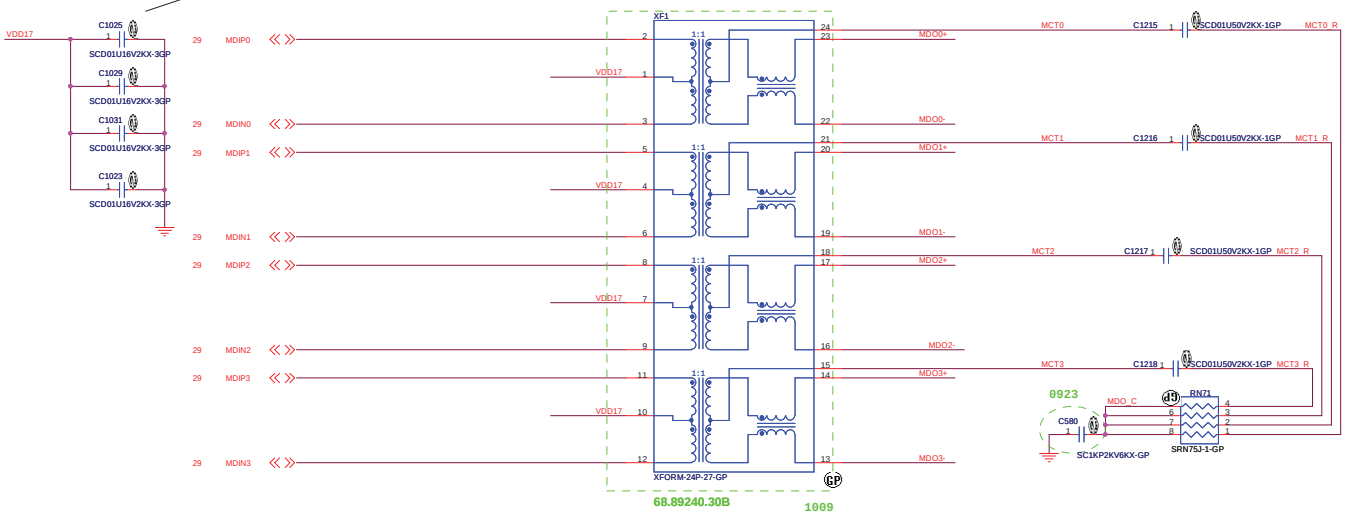
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LAN Realtek RTL8151

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 29 of 50

Transformer



LAN Conn

<Core Design>

wistron

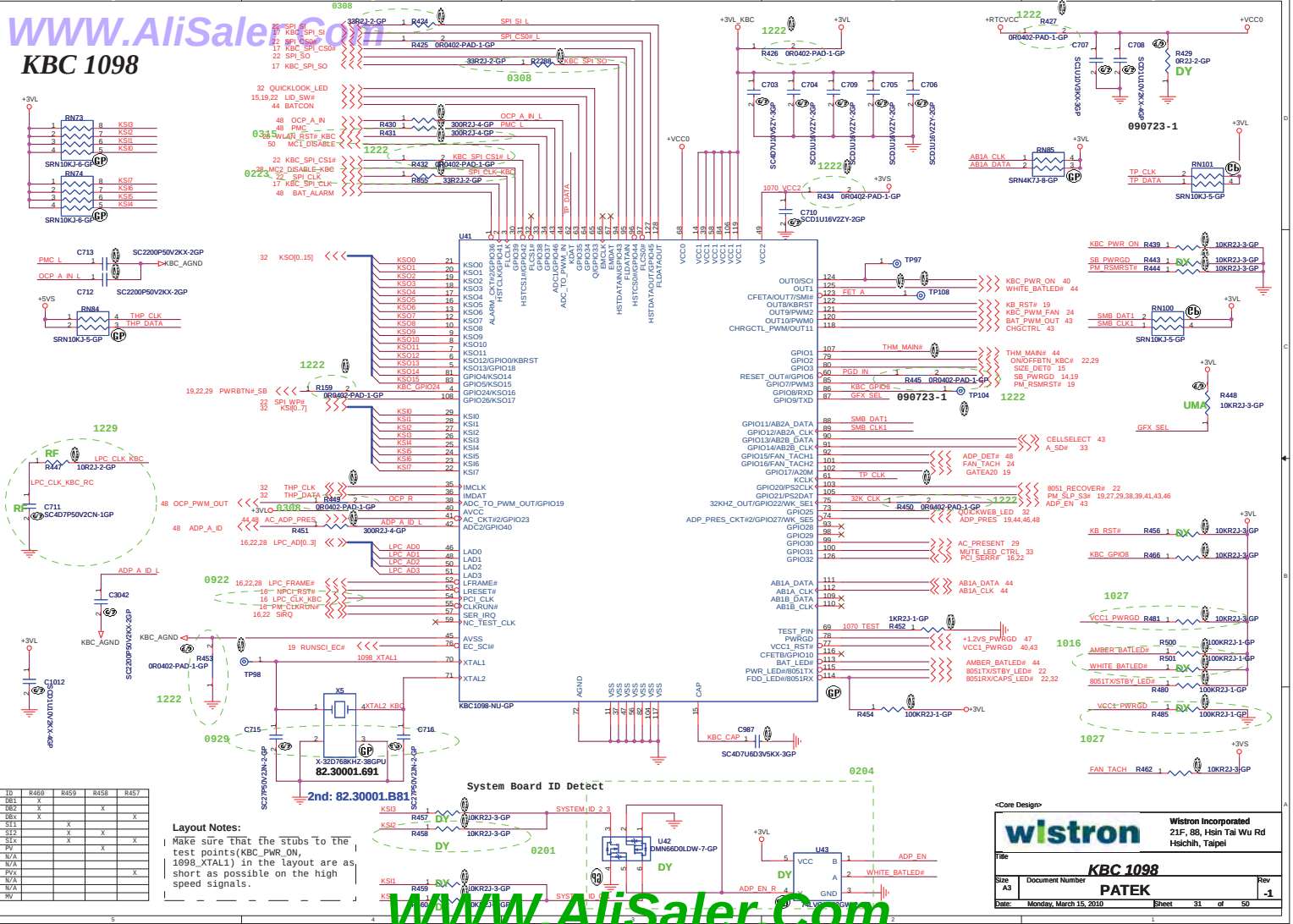
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Magnetic & RJ45

Size: A3 | Document Number: PATEK | Rev: -1

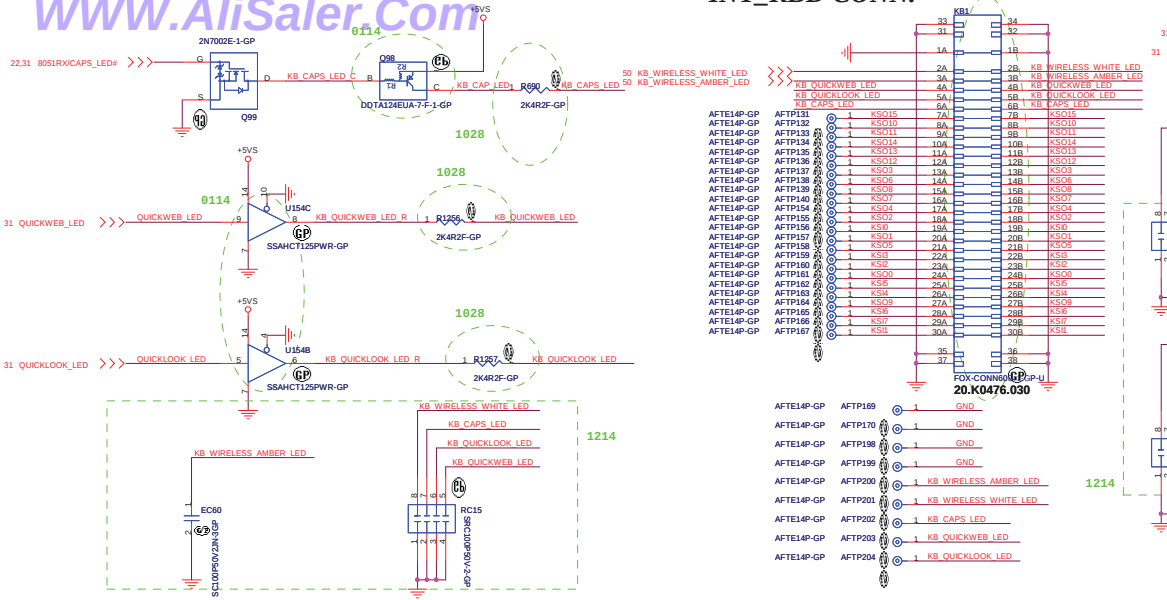
Date: Monday, March 15, 2010 | Sheet 30 of 50

KBC 1098

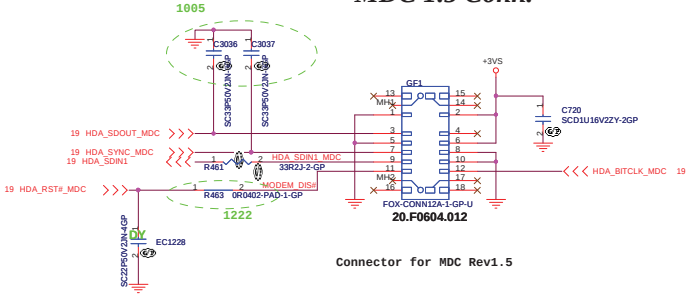


ID	R460	R459	R458	R457
DB1	X			
DB2	X		X	
DBx	X			X
SI1		X		
SI2		X	X	
SIx		X		X
PV			X	
N/A				
N/A				
PVx				X
N/A				
N/A				
MV				

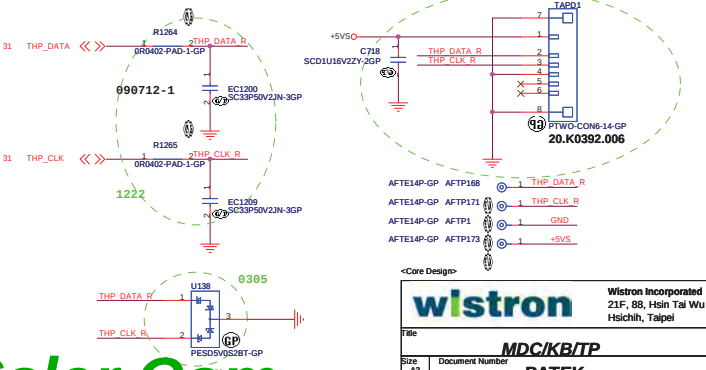
INT_KBD CONN.



MODEM
MDC 1.5 Conn.



Touch_Pad CONN.



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: MDC/KB/TP

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 32 of 50

AUDIO CODEC(92HD80)

close to U30

Port Arrangement
Port A---> Ext Mic
Port B---> HP
Port C---> FREE
Port D---> SPKR
Port E---> FREE
Port F---> FREE

1216 1214 1222 0114 0928 0309 1021

71.92H80.M01

92HD80B1X5NLGXYD2-1-GP

Close to Pin13

Close to Pin14

Place close to Codec chip

audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

<Core Design>

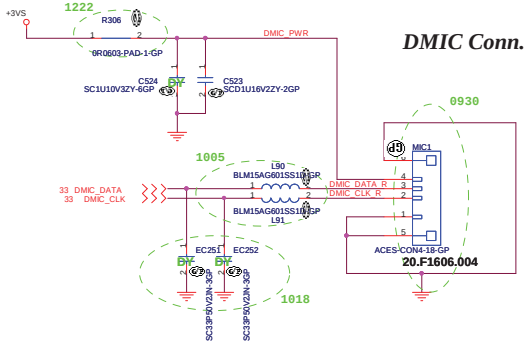
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO 92HD80 / OP AMP

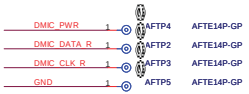
Size: A3 | Document Number: PATEK | Rev: -1

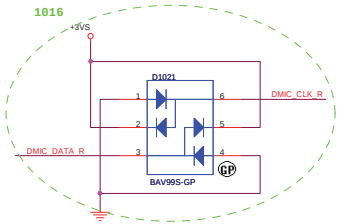
Date: Monday, March 15, 2010 | Sheet 33 of 50

Dual Internal Digital MIC

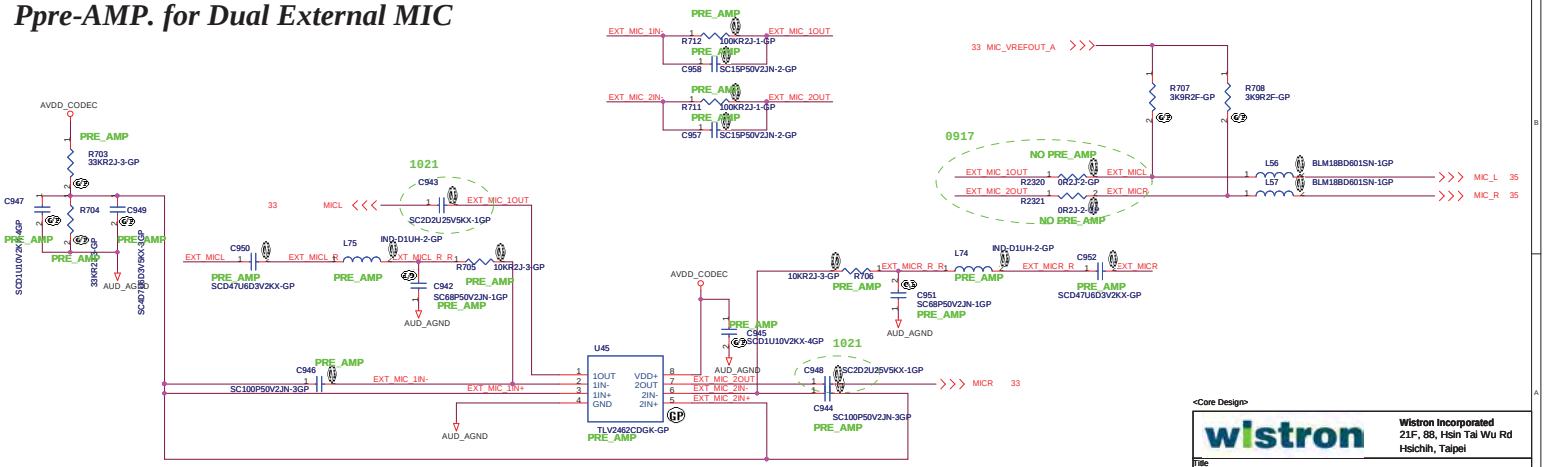


DMIC Conn.





Ppre-AMP. for Dual External MIC



<Core Design>

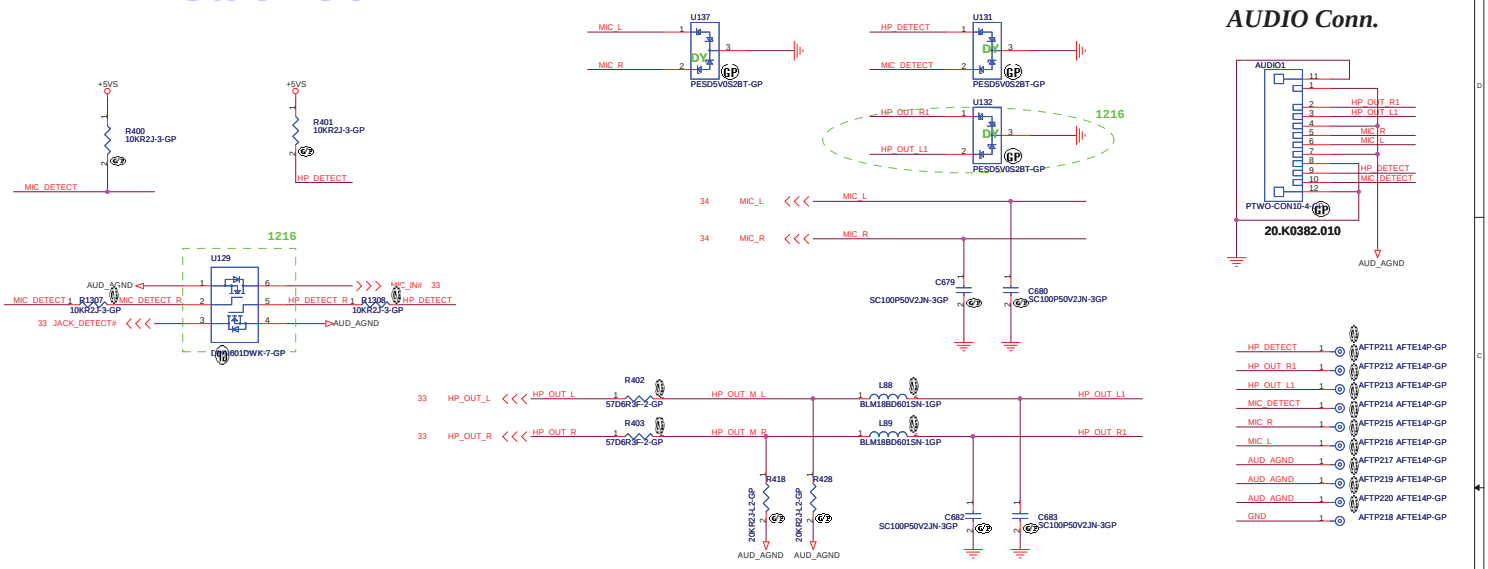
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO Pre-AMP / D MIC

Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 34 of 50



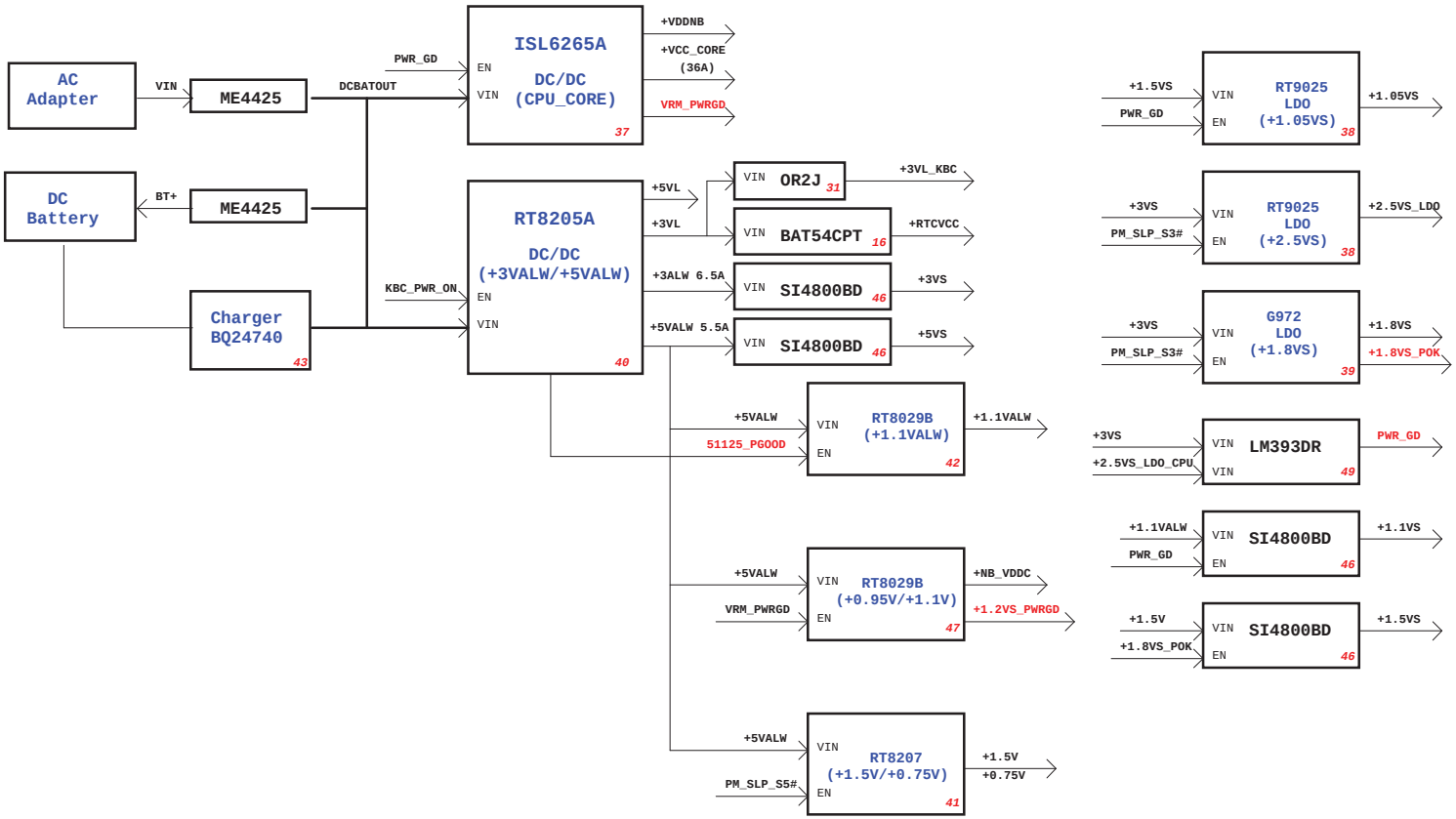
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO JACK

Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 35 of 50

Patek UMA Power Block Diagram



<Core Design>

wistron

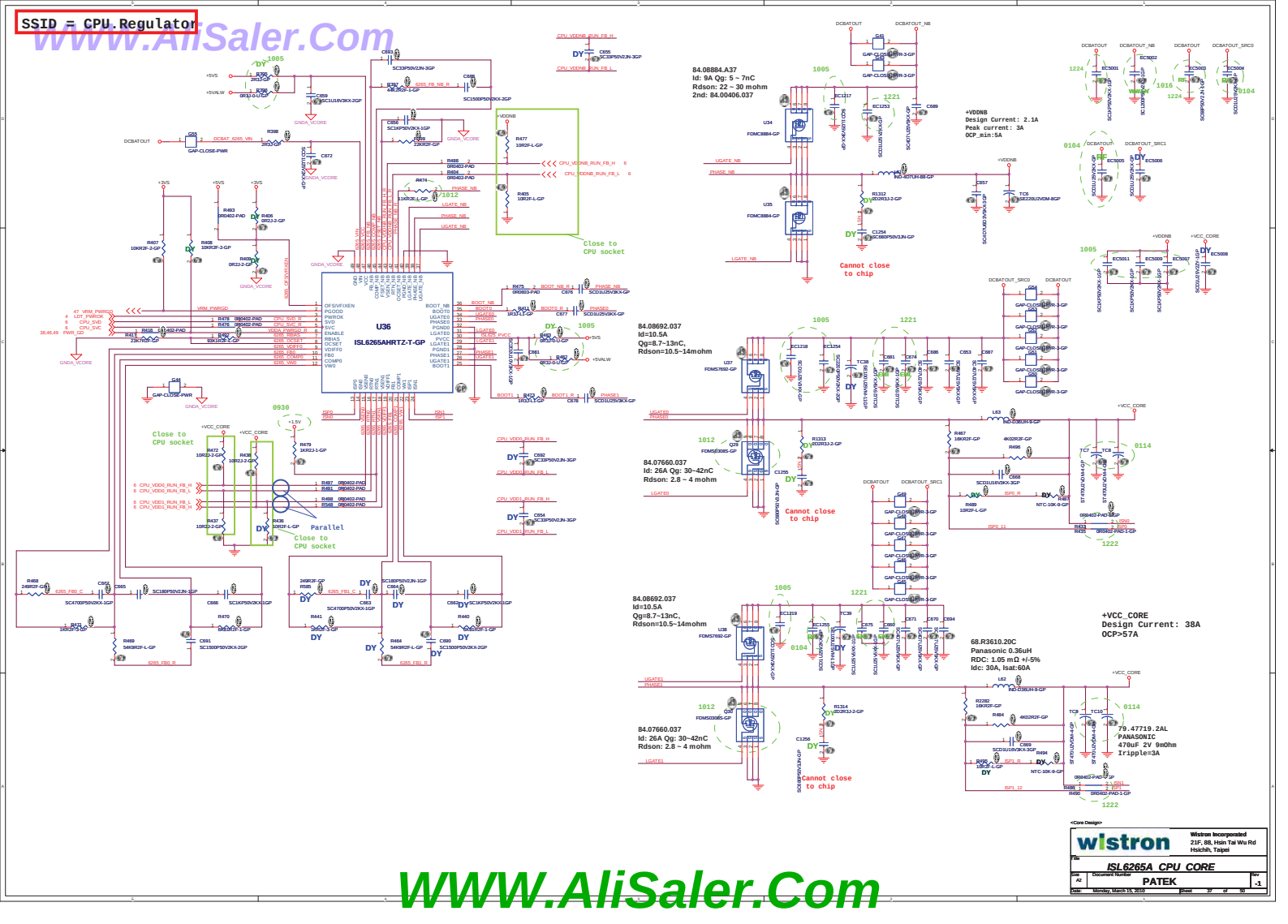
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

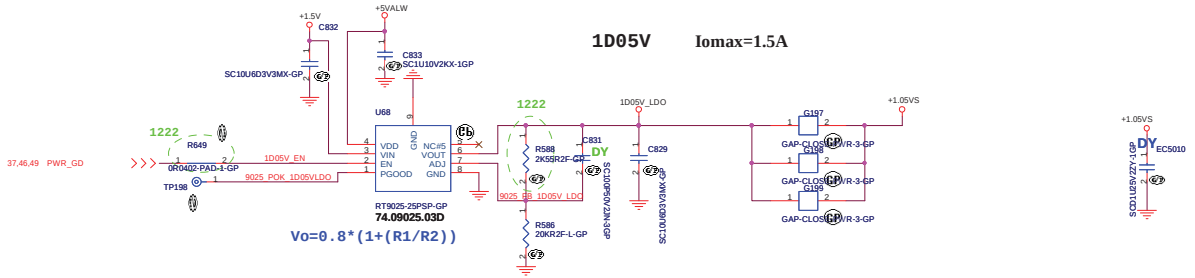
Title: Power Block Diagram

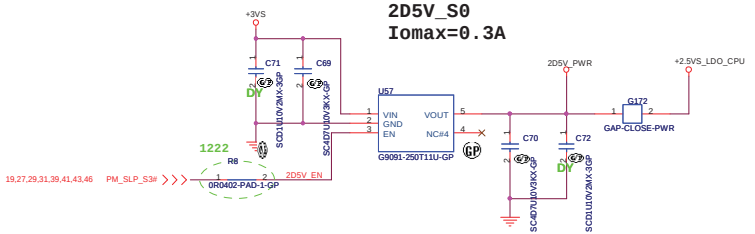
Size	Document Number	Rev
A3	PATEK	-1

Date: Thursday, January 21, 2010 Sheet 36 of 50

SSID = CPU.Regulator







<Core Design>

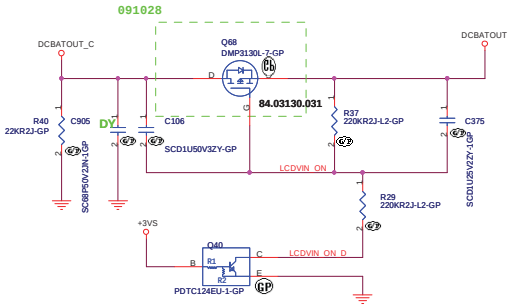
wistron

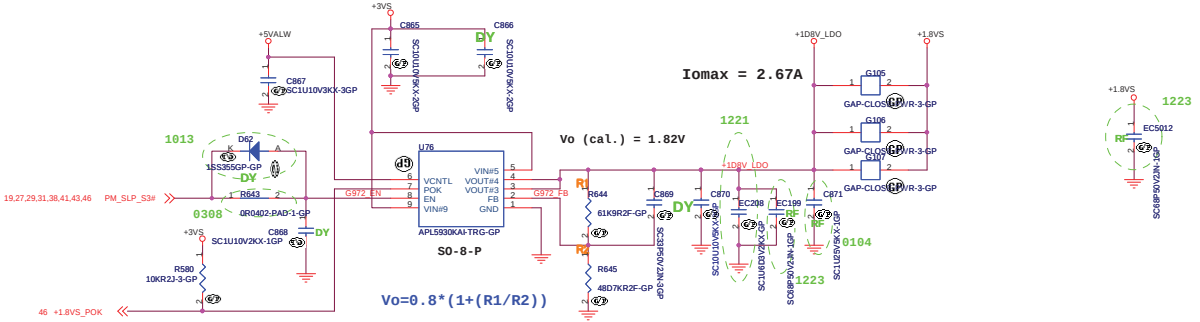
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RT8209B +1.05VS / +2.5VS

Size: A3 | Document Number: PATEK | Rev: -1

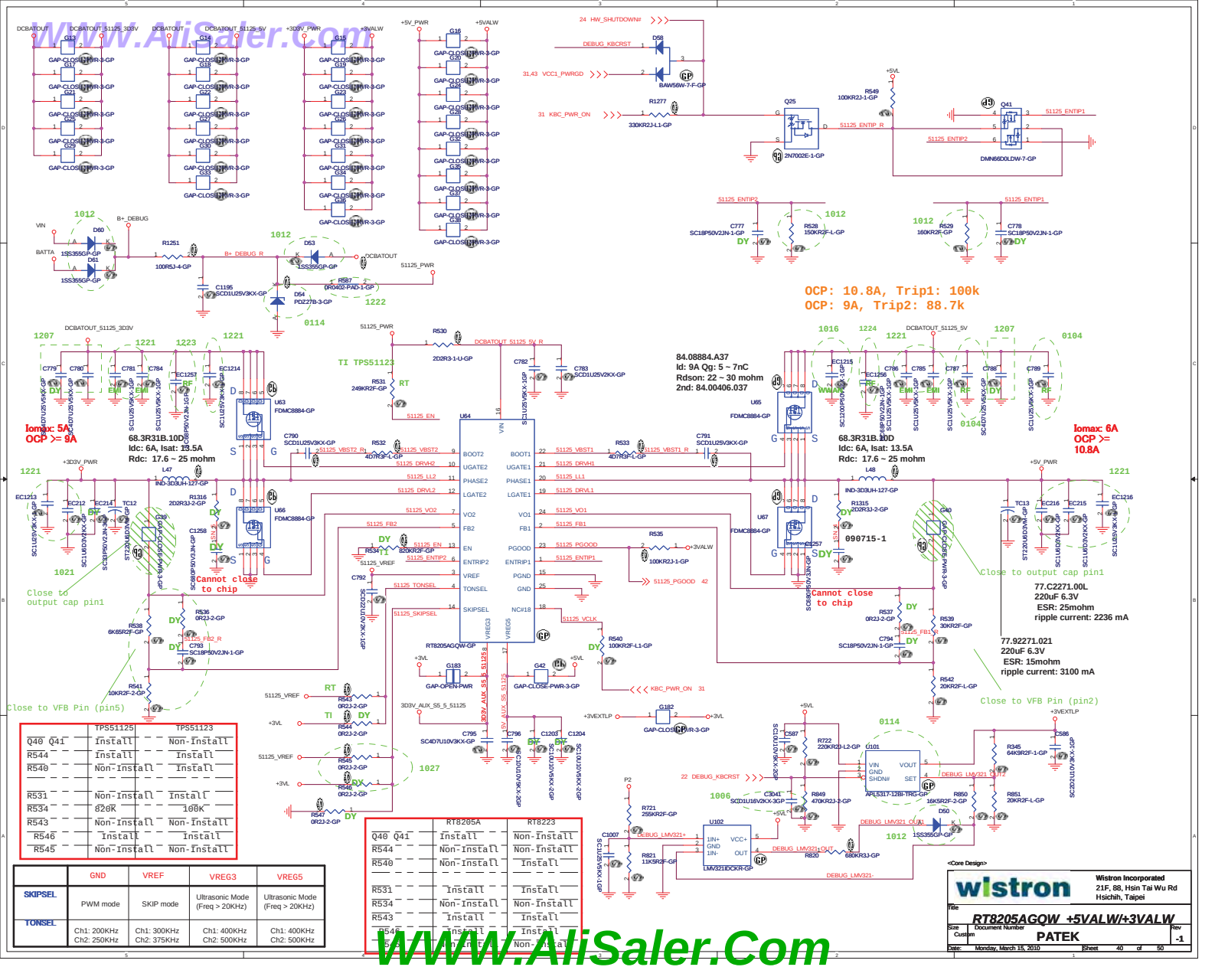
Date: Monday, March 15, 2010 | Sheet 38 of 50





<Core Design>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: G972 +1.8VS		
Size: A3	Document Number: PATEK	Rev: -1
Date: Monday, March 15, 2010	Sheet 39 of 50	



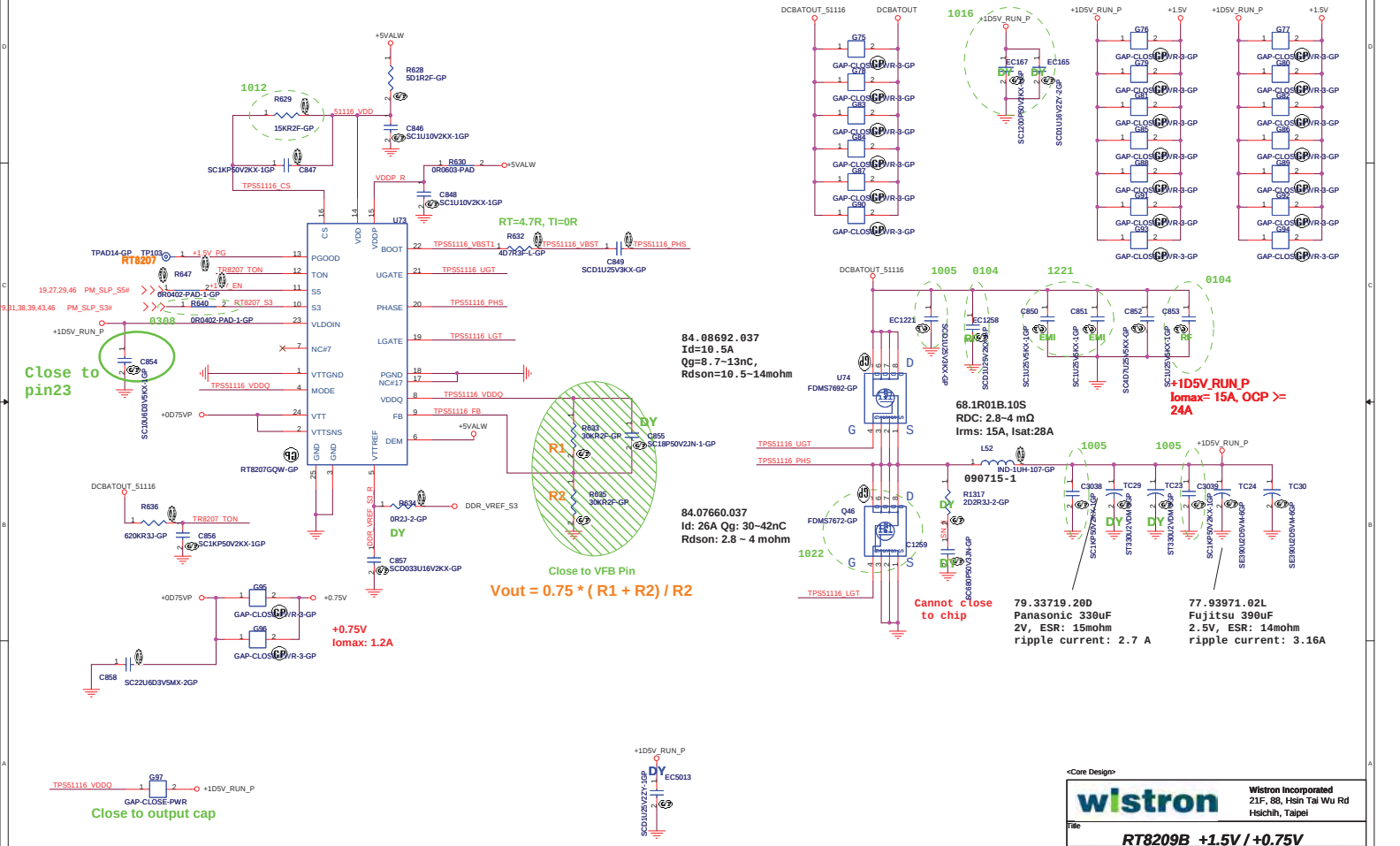
	TPS51125	TPS51123
Q40 Q41	Install	Non-Install
R544	Install	Install
R540	Non-Install	Install
R531	Non-Install	Install
R534	820R	100K
R543	Non-Install	Non-Install
R546	Install	Install
R545	Non-Install	Non-Install

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R544	Non-Install	Non-Install
R540	Non-Install	Install
R531	Install	Install
R534	Non-Install	Non-Install
R543	Install	Install
R546	Install	Install
R545	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz

Wistron Incorporated	21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	RT8205AGQW +5VALW/+3VALW
Size: Custom	Document Number: PATEK
Rev	-1
Date: Monday, March 15, 2010	Sheet 40 of 50

RT8207 for 1D5V and 0D75V



<Core Design>

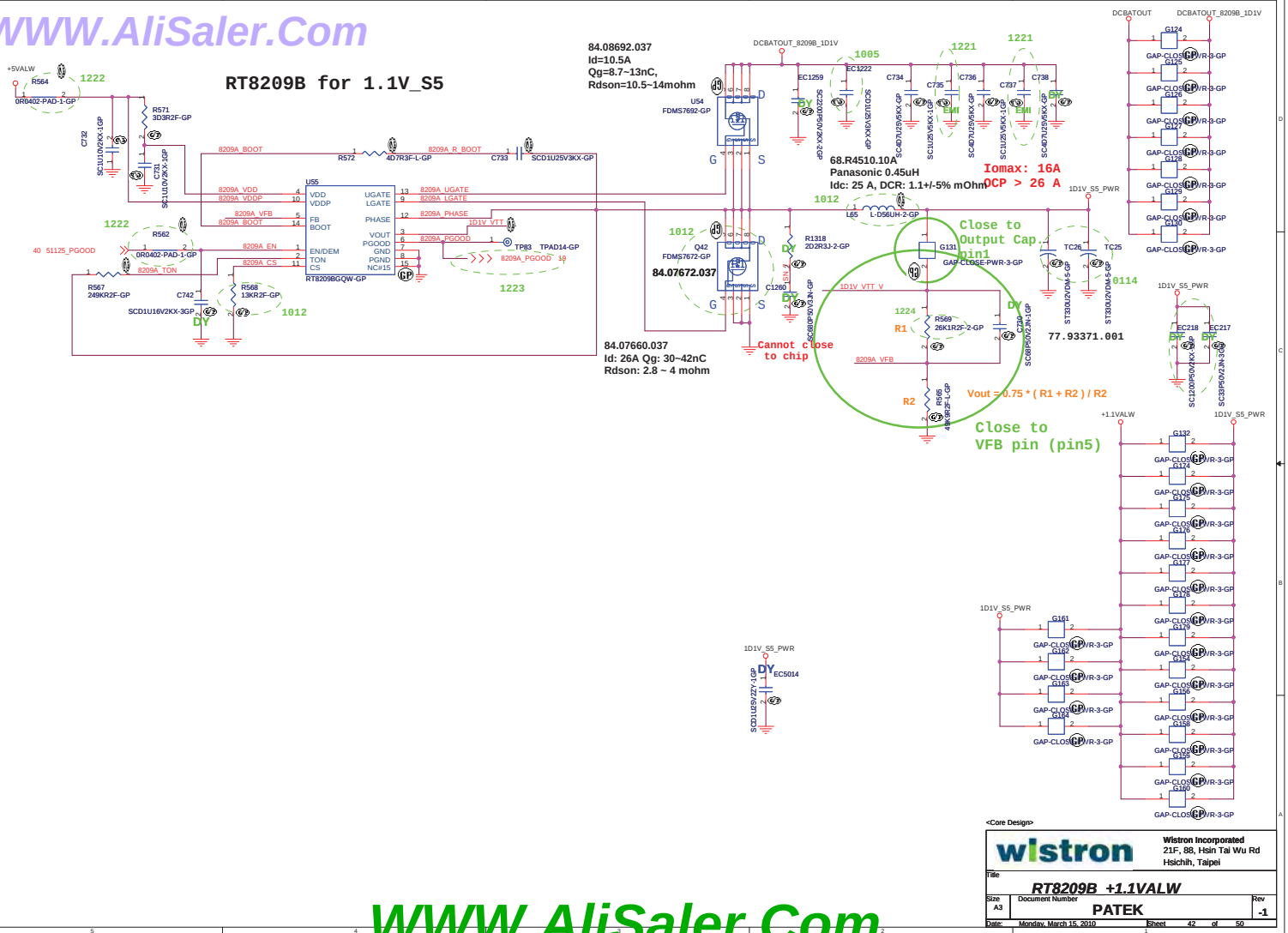
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RT8209B +1.5V / +0.75V

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 41 of 50

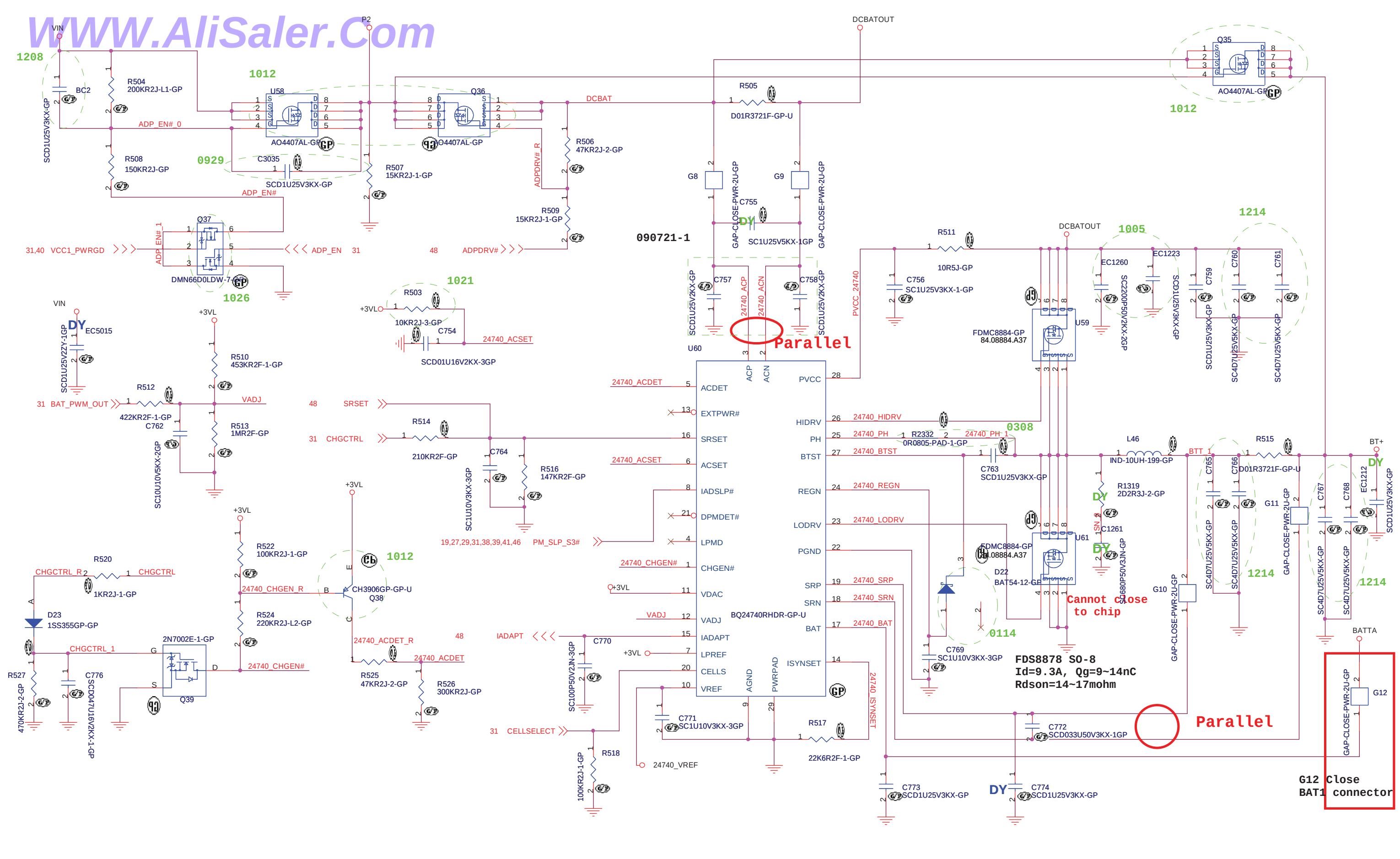


wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RT8209B +1.1VALW

Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 42 of 50



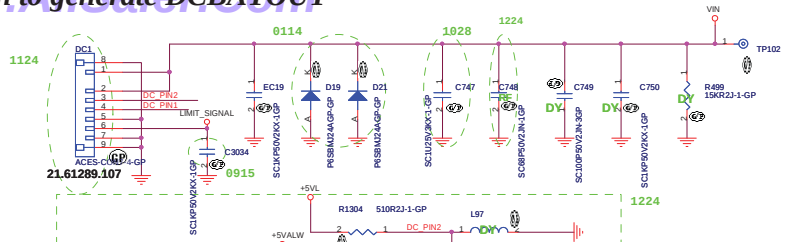
<Core Design>

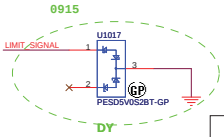
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title		
CHARGER BQ24740		
Size: A3	Document Number: PATEK	Rev: -1
Date: Monday, March 15, 2010	Sheet 43 of 50	

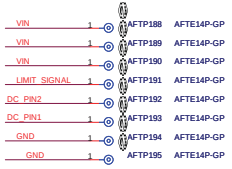
Adaptor in to generate DCBATOUT



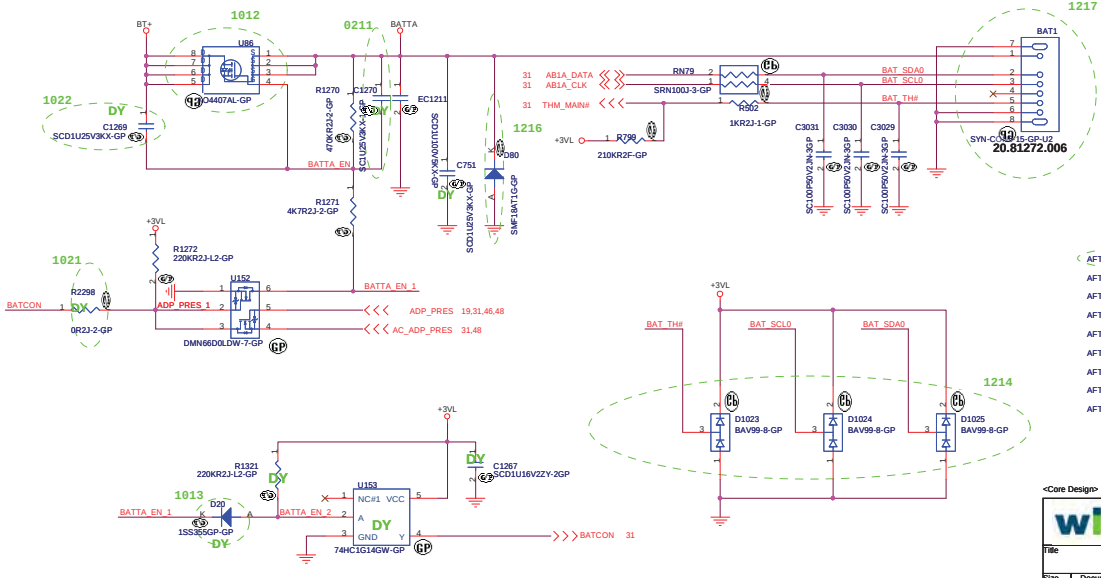


	AMBER ON	WHITE ON	ALL OFF
AMBER	-	+	-
WHITE	+	-	-

White LED:
PIN1 (+)
PIN2 (-)
Amber LED:
PIN1 (-)
PIN2 (+)



BATTERY CONNECTOR



<Core Design>

wistron

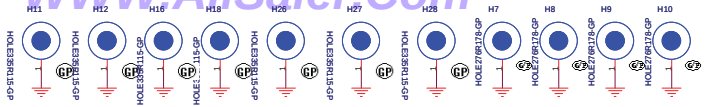
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AD & BATT CONN.

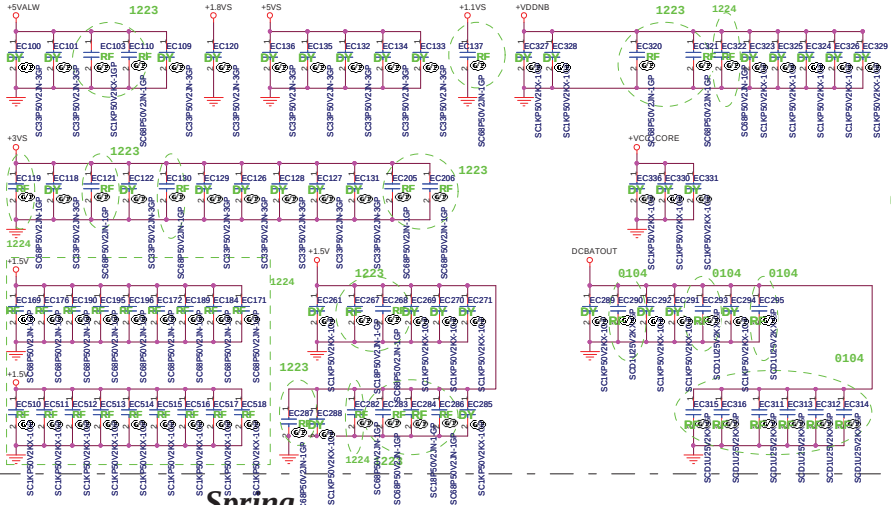
Size: Custom | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 44 of 50

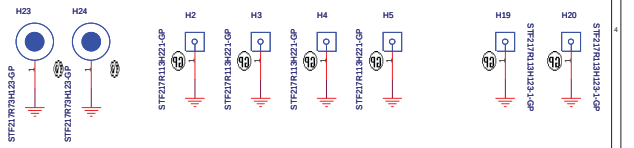
HOLE



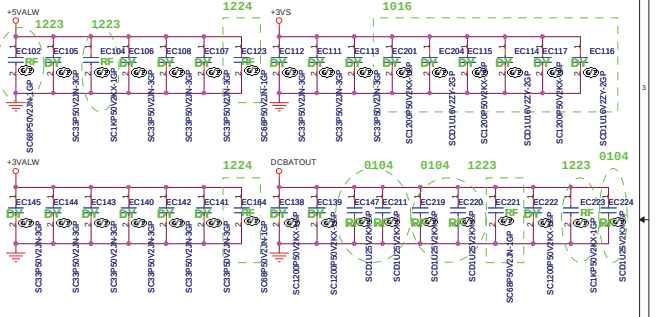
Bottom Side for RF



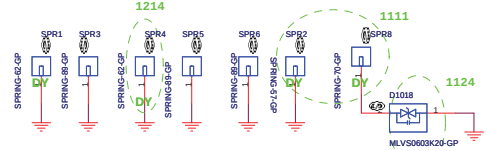
Stand Off



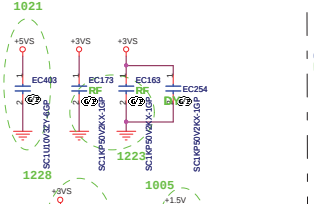
Top Side for RF



Spring

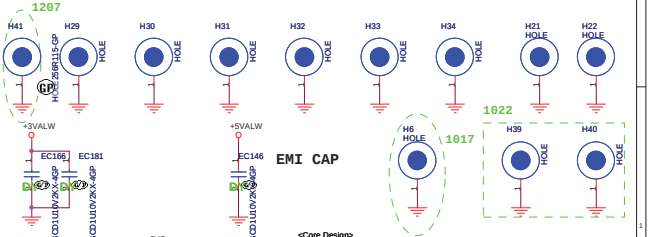


EMI CAP



Ground PAD

P/N: ZZ.0HOLE.XXX



EMI CAP

<Core Design>

wistron

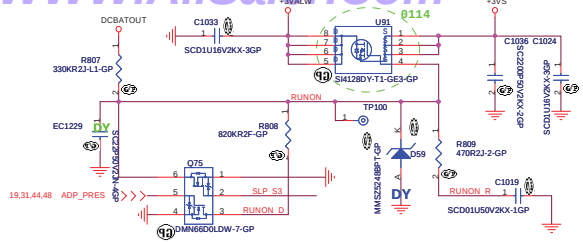
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HOLE

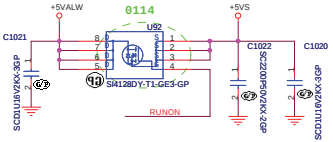
Size: A3 | Document Number: PATEK | Rev: -1

Date: Thursday, March 11, 2010 | Sheet 45 of 50

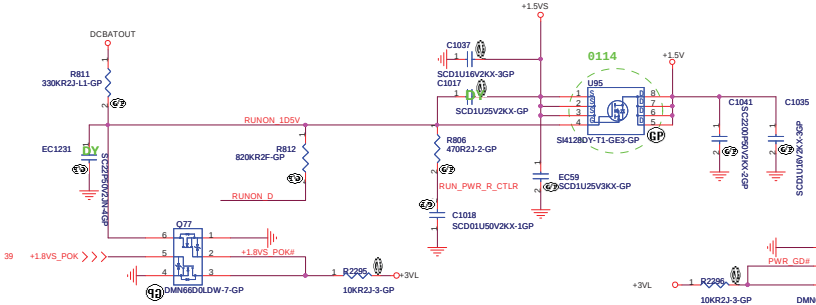
+3VALW to +3VS Transfer



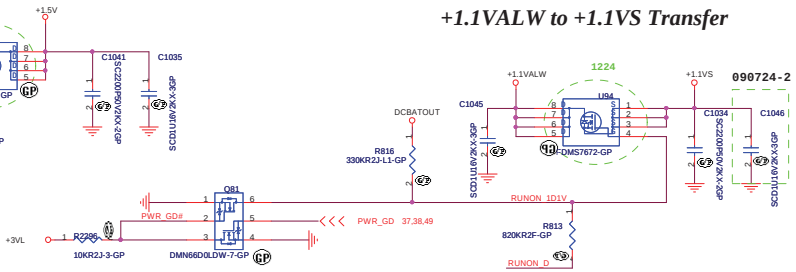
+5VALW to +5VS Transfer



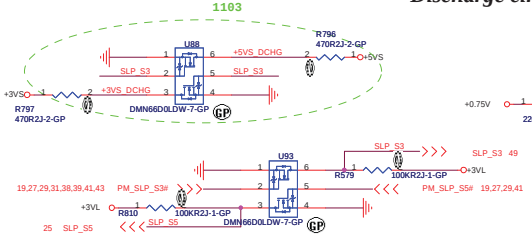
+1.5V to +1.5VS Transfer

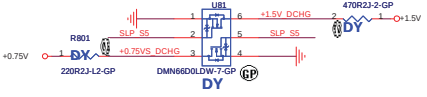


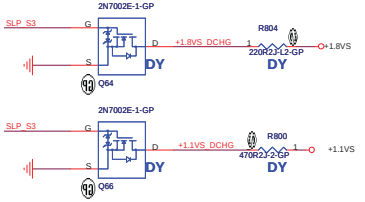
+1.1VALW to +1.1VS Transfer



Discharge circuit-1







<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DC/DC

Size	Document Number	Rev
A3	PATEK	-1

Date: Monday, March 15, 2010 Sheet 46 of 50

RT8209B for 1D1V&0D95V

84.08884.A01
Id: 9A Qg: 5 ~ 7nC
Rdson: 22 ~ 30 mohm

Iomax: 8A
OCP> 12A

Vout = 0.75 * (R1 + R2) / R2

68.1R51A.10K
Irms: 10A, Isat: 18A
Rdc: 8.6 ~ 14 mohm

80.2271V.12L
NEC 220uF
2.5V, ESR: 15mohm
ripple current: 2.38 A

77.92271.021
Fujitsu 220uF
6.3V, ESR: 15mohm
ripple current: 3.1A

Close to Output Cap pin1

Cannot close to chip

Close to VFB pin (pin5)

1D1V_NB = (1 + R1 / Rb) X 0.75

+VCC_NB_CORE	R1	RBot	STRP_DATA	ideal voltage
0.95v	10k	R2 37.4k	HIGH	0.95
1.1v	10k	R2 37.4k // R3 49.9k	LOW	1.1

GAP close if only PowerPlay not supported

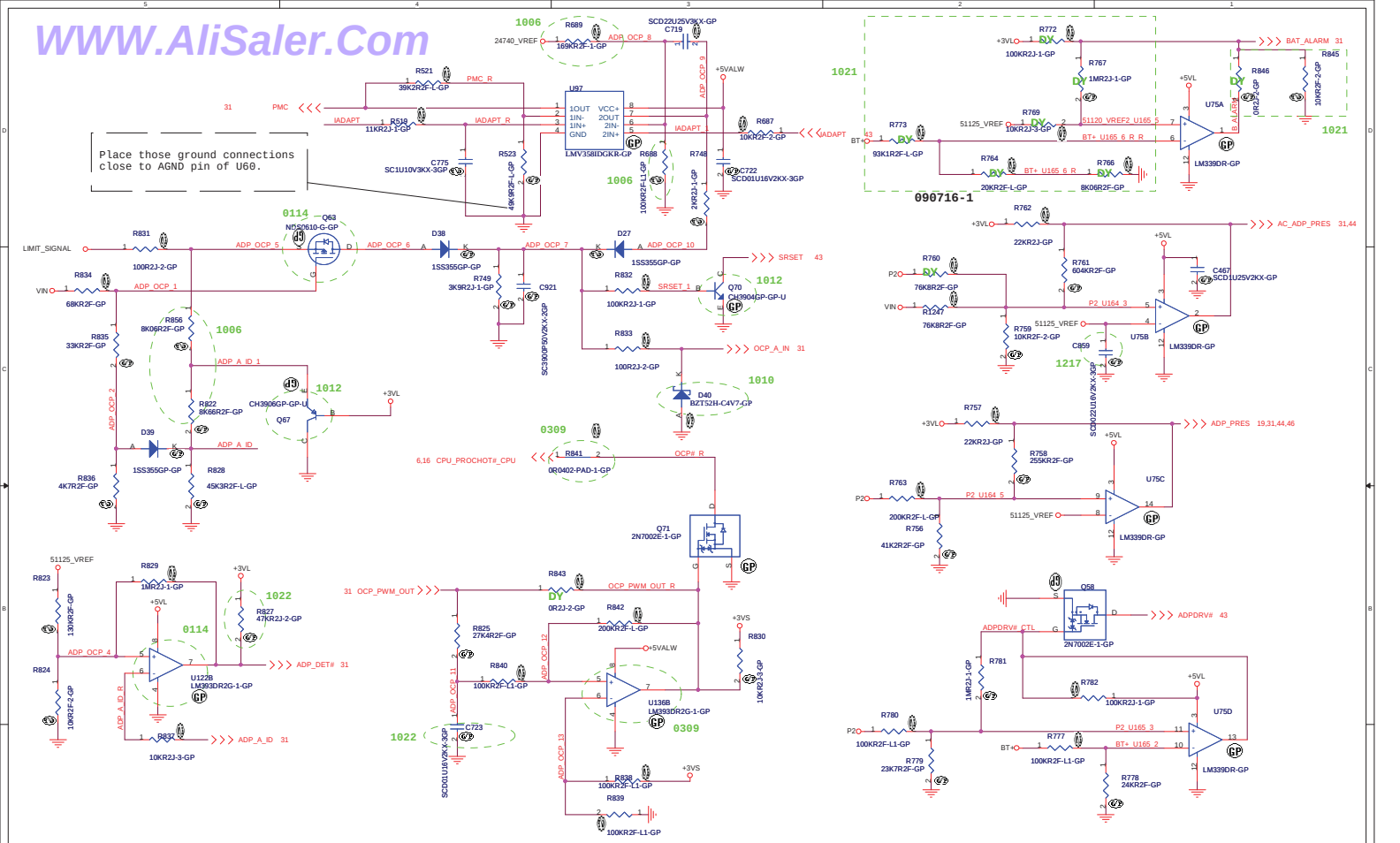
<Core Design>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: POWERPLAY +1.1VS/+0.95VS

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 47 of 50



NOTE:

When AC_ADP_PRES=0 -->1
Vin*(R759//R761)/ [(R759//R761)+R1247]=51125_VREF
Vin=17.6145V

When AC_ADP_PRES=1 --> 0
[(Vin-51125_VREF)/R1247]+[(+3VL-51125_VREF)/(R761+R762)]=51125_VREF/R759
Vin=17.212554V

When ADP_PRES=0->1
P2*(R756//R758)/ [(R756//R758)+R763]=51125_VREF
P2=13.325V

When ADP_PRES=1->0
[(P2-51125_VREF)/R756]+[(+3VL-51125_VREF)/(R757+R758)]=51125_VREF/R756
P2=10.894V

<Core Design>

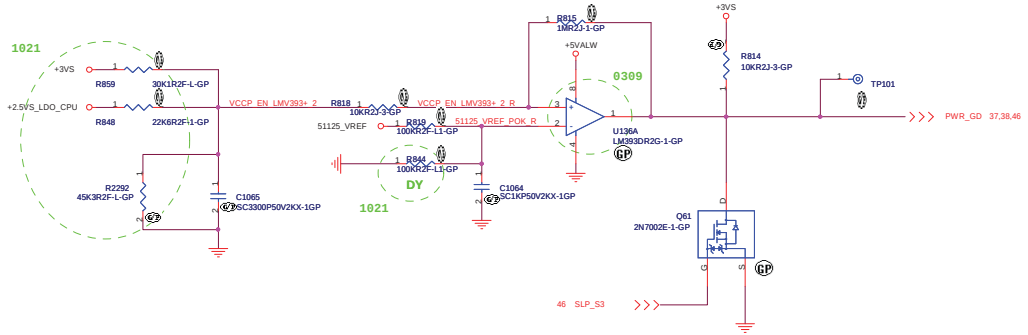
wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: ADP OCP

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 48 of 50



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: POK CKT

Size: A3 | Document Number: PATEK | Rev: -1

Date: Monday, March 15, 2010 | Sheet 49 of 50

Mini-Card--WWAN
Full minicard