


Wistron Confidential

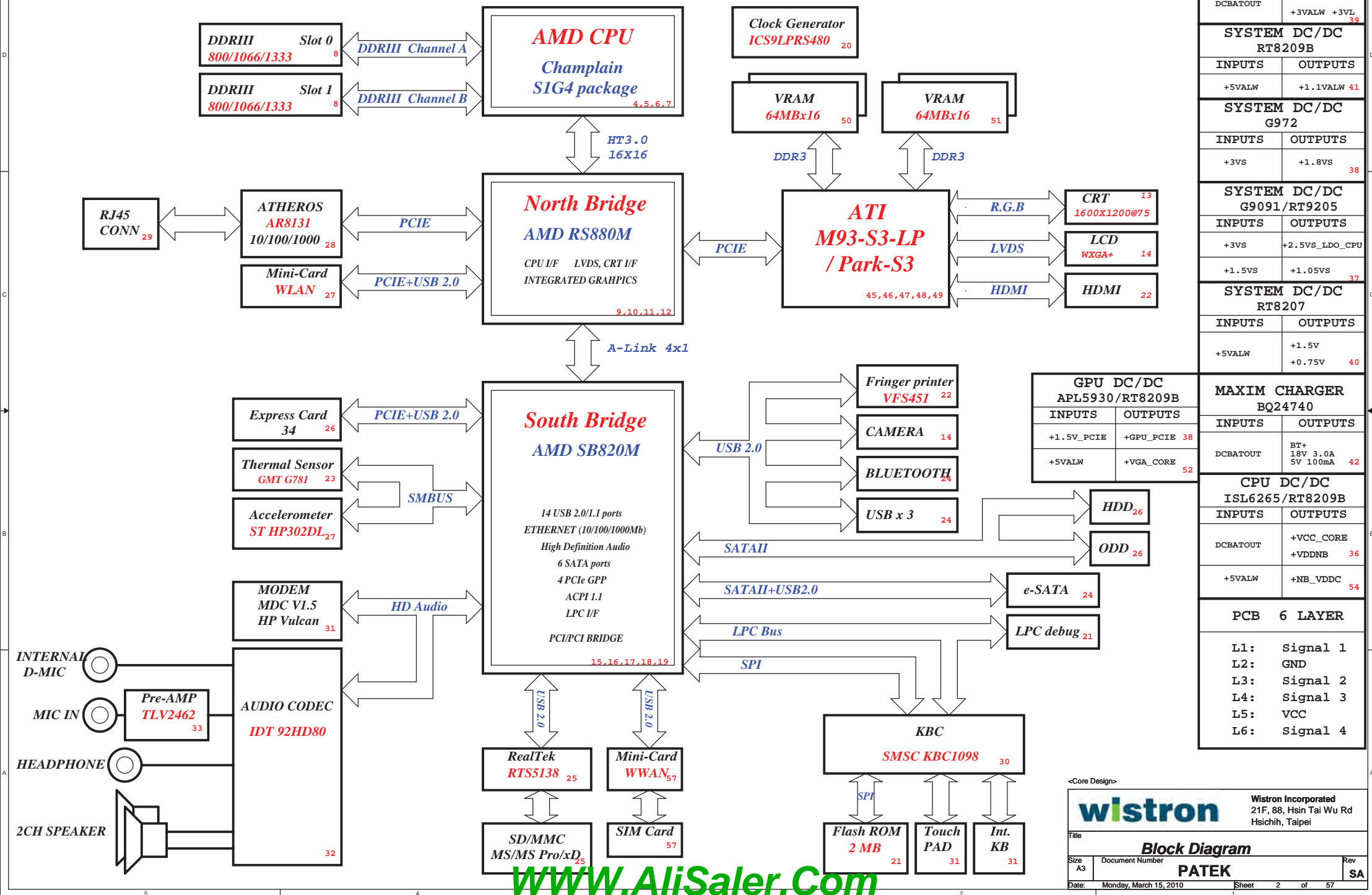
PV1

2009/12/28

REV :PV-01

<Core Design>	
	
Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	
Cover	
Size	Document Number
A3	PATEK
Date:	Monday, March 15, 2010
Sheet	1 of 57
Rev	SA

Patek DIS Block Diagram



RS880M strapping

STRAP_DEBUG_BUS_GPIO_ENABLEb Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC) 0 : Enable * 1 : Disable
RS880: Enables Side port memory (RS880 use HSYNC) 0 : Enable * 1 : Disable
SUS_STAT# Selects Loading of STRAPS From EEPROM *1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

SB820M strapping

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK_KBC (LPCCLK0)	LPC_CLK_DB (LPCCLK1)	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	L, H = LPC ROM L, L = FWH ROM

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	SB-TSI
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SB_SMB_CLK1 SB_SMB_DAT1	SB820M	X	X	X	X	X	X	X
SB_SMB_CLK0 SB_SMB_DAT0	SB820M	X	V	V	V	V	X	X
CPU_SIC_SB700 CPU_SID_SB700	CPU	X	X	X	X	X	X	V

PCIE routing

Page 9


LANE 0	LAN
LANE 3	NEW CARD
LANE 4	WLAN

USB table

Page 18

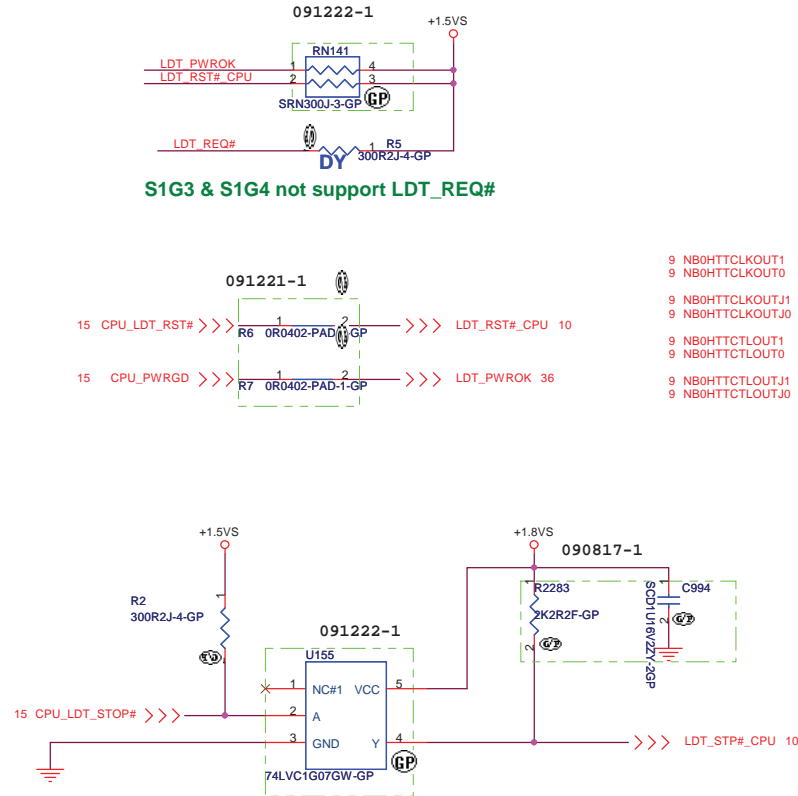
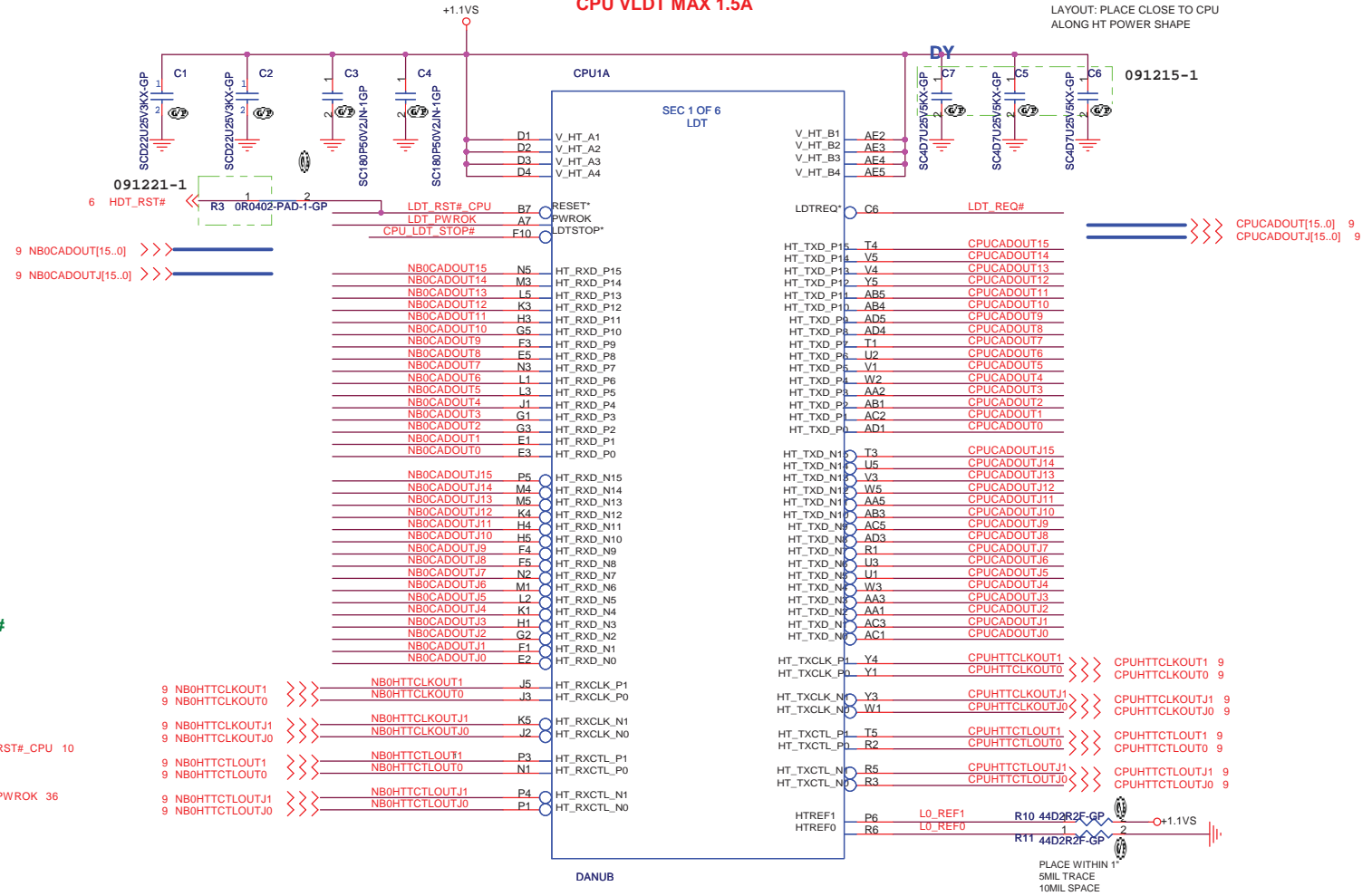
Pair	Device
	USB-FSD1 FPR
	USB-9 Bluetooth
	USB-8 WLAN
	USB-7 WWAN
	USB-6 USB Card Reader
	USB-5 Right Side
	USB-4 USB Camera
	USB-3 Right Side
	USB-2 Left Side (e-SATA combo)
	USB-1 New Card
	USB-0 Left Side (S/W Debug port)

<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
NOTES			
Size A3	Document Number	PATEK	Rev SA
Date:	Monday, March 15, 2010	Sheet	3 of 57



LAYOUT: PLACE CLOSE TO CPU
ALONG HT POWER SHAPE



<Core Design>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	CPU(1/4) HT
-------	--------------------

Size A3	Document Number PATEK
------------	---------------------------------

Date: Monday, March 15, 2010

Sheet 4 of 57

Rev	
SA	

8 M_A_DQ[63..0]

<<>>

SEC 3 OF 6
MEMORY_A

M A DQ63	AA12	MA_DATA63
M A DQ62	AB12	MA_DATA62
M A DQ61	AB14	MA_DATA61
M A DQ60	AB14	MA_DATA60
M A DQ59	WV11	MA_DATA59
M A DQ58	Y12	MA_DATA58
M A DQ57	AD13	MA_DATA57
M A DQ56	AB13	MA_DATA56
M A DQ55	AD15	MA_DATA55
M A DQ54	AB15	MA_DATA54
M A DQ53	AB17	MA_DATA53
M A DQ52	Y17	MA_DATA52
M A DQ51	Y14	MA_DATA51
M A DQ50	WV16	MA_DATA50
M A DQ49	WV16	MA_DATA49
M A DQ48	AD17	MA_DATA48
M A DQ47	Y18	MA_DATA47
M A DQ46	AD19	MA_DATA46
M A DQ45	AD21	MA_DATA45
M A DQ44	AB21	MA_DATA44
M A DQ43	AB18	MA_DATA43
M A DQ42	AA18	MA_DATA42
M A DQ41	Y20	MA_DATA41
M A DQ40	Y20	MA_DATA40
M A DQ39	AA22	MA_DATA39
M A DQ38	Y22	MA_DATA38
M A DQ37	WV21	MA_DATA37
M A DQ36	WV22	MA_DATA36
M A DQ35	AA21	MA_DATA35
M A DQ34	AB22	MA_DATA34
M A DQ33	AB24	MA_DATA33
M A DQ32	Y24	MA_DATA32
M A DQ31	H22	MA_DATA31
M A DQ30	H20	MA_DATA30
M A DQ29	E22	MA_DATA29
M A DQ28	E21	MA_DATA28
M A DQ27	J19	MA_DATA27
M A DQ26	H24	MA_DATA26
M A DQ25	F22	MA_DATA25
M A DQ24	G20	MA_DATA24
M A DQ23	C23	MA_DATA23
M A DQ22	B22	MA_DATA22
M A DQ21	E18	MA_DATA21
M A DQ20	E18	MA_DATA20
M A DQ19	E20	MA_DATA19
M A DQ18	D22	MA_DATA18
M A DQ17	C19	MA_DATA17
M A DQ16	G18	MA_DATA16
M A DQ15	C17	MA_DATA15
M A DQ14	C17	MA_DATA14
M A DQ13	F14	MA_DATA13
M A DQ12	E14	MA_DATA12
M A DQ11	H17	MA_DATA11
M A DQ10	E17	MA_DATA10
M A DQ9	E15	MA_DATA9
M A DQ8	H15	MA_DATA8
M A DQ7	E13	MA_DATA7
M A DQ6	C13	MA_DATA6
M A DQ5	H12	MA_DATA5
M A DQ4	H11	MA_DATA4
M A DQ3	G14	MA_DATA3
M A DQ2	H14	MA_DATA2
M A DQ1	E12	MA_DATA1
M A DQ0	G12	MA_DATA0

M A A15	K19	MA_ADD15
M A A14	K24	MA_ADD14
M A A13	Y24	MA_ADD13
M A A12	V20	MA_ADD12
M A A11	L22	MA_ADD11
M A A10	R21	MA_ADD10
M A A9	K22	MA_ADD9
M A A8	L19	MA_ADD8
M A A7	L21	MA_ADD7
M A A6	M24	MA_ADD6
M A A5	L20	MA_ADD5
M A A4	M22	MA_ADD4
M A A3	M19	MA_ADD3
M A A2	N22	MA_ADD2
M A A1	M20	MA_ADD1
M A A0	N21	MA_ADD0

MA_DM7	Y13	M A DM7
MA_DM6	AB16	M A DM6
MA_DM5	Y19	M A DM5
MA_DM4	AC24	M A DM4
MA_DM3	F24	M A DM3
MA_DM2	E19	M A DM2
MA_DM1	C15	M A DM1
MA_DM0	E12	M A DM0

MA_DQS_PZ	W12	M A DQS7
MA_DQS_PR	Y15	M A DQS6
MA_DQS_PS	AB19	M A DQS5
MA_DQS_PL	AD23	M A DQS4
MA_DQS_PL	G22	M A DQS3
MA_DQS_PL	C22	M A DQS2
MA_DQS_PL	G16	M A DQS1
MA_DQS_PL	G13	M A DQS0

MA_DQS_N	W13	M A DQS#7
MA_DQS_N	W15	M A DQS#6
MA_DQS_N	AB20	M A DQS#5
MA_DQS_N	AC23	M A DQS#4
MA_DQS_N	G21	M A DQS#3
MA_DQS_N	C21	M A DQS#2
MA_DQS_N	G15	M A DQS#1
MA_DQS_N	H13	M A DQS#0

090803-1

MA_CLK5_P	N19	M A CLK DDR1	>>>	M_A_CLK_DDR1# 8
MA_CLK5_N	N20	M A CLK DDR1#	>>>	M_A_CLK_DDR1# 8
MA_CLK1_P	E16			
MA_CLK1_N	F16			
MA_CLK7_P	Y16			
MA_CLK7_N	AA16			
MA_CLK4_P	P19	M A CLK DDR2	>>>	M_A_CLK_DDR2# 8
MA_CLK4_N	P20	M A CLK DDR2#	>>>	M_A_CLK_DDR2# 8

MA_BANK2	J21	M A BS#2	>>>	M_A_BS#2 8
MA_BANK1	R23	M A BS#1	>>>	M_A_BS#1 8
MA_BANK0	R20	M A BS#0	>>>	M_A_BS#0 8

MA_RAS*	R19	M A RAS#	>>>	M_A_RAS# 8
MA_CAS*	T22	M A CAS#	>>>	M_A_CAS# 8
MA_WE*	T24	M A WE#	>>>	M_A_WE# 8

MA1_CS1	V20			
MA1_CS0	U20			
MA0_CS1	U19	M A CS1#	>>>	M_A_CS1# 8
MA0_CS0	T20	M A CS0#	>>>	M_A_CS0# 8

MA_CKE1	J20	M A CKE1	>>>	M_A_CKE1 8
MA_CKE0	J22	M A CKE0	>>>	M_A_CKE0 8

MA1_ODT0	V19	MA1_ODT1	TP1	TPAD14-GP
MA1_ODT0	U21	MA1_ODT0	P2	TPAD14-GP
MA0_ODT0	V22	M A ODT1		
MA0_ODT0	T19	M A ODT0		

>>> M_A_A[15..0] 8

DANUB

8 M_B_DQ[63..0]

<<>>

CPU1D

SEC 4 OF 6
MEMORY_B

M B DQ63	AD11	MB_DATA63
M B DQ62	AE11	MB_DATA62
M B DQ61	AE14	MB_DATA61
M B DQ60	AE14	MB_DATA60
M B DQ59	Y11	MB_DATA59
M B DQ58	AB11	MB_DATA58
M B DQ57	AC12	MB_DATA57
M B DQ56	AE13	MB_DATA56
M B DQ55	AE15	MB_DATA55
M B DQ54	AE16	MB_DATA54
M B DQ53	AC18	MB_DATA53
M B DQ52	AE19	MB_DATA52
M B DQ51	AD14	MB_DATA51
M B DQ50	AC14	MB_DATA50
M B DQ49	AE18	MB_DATA49
M B DQ48	AE18	MB_DATA48
M B DQ47	AD20	MB_DATA47
M B DQ46	AC20	MB_DATA46
M B DQ45	AE23	MB_DATA45
M B DQ44	AE24	MB_DATA44
M B DQ43	AE20	MB_DATA43
M B DQ42	AE20	MB_DATA42
M B DQ41	AD22	MB_DATA41
M B DQ40	AC22	MB_DATA40
M B DQ39	AE25	MB_DATA39
M B DQ38	AD26	MB_DATA38
M B DQ37	AA25	MB_DATA37
M B DQ36	AA26	MB_DATA36
M B DQ35	AE24	MB_DATA35
M B DQ34	AD24	MB_DATA34
M B DQ33	AA23	MB_DATA33
M B DQ32	AA24	MB_DATA32
M B DQ31	G24	MB_DATA31
M B DQ30	G23	MB_DATA30
M B DQ29	G26	MB_DATA29
M B DQ28	C26	MB_DATA28
M B DQ27	G26	MB_DATA27
M B DQ26	G25	MB_DATA26
M B DQ25	E24	MB_DATA25
M B DQ24	E23	MB_DATA24
M B DQ23	C24	MB_DATA23
M B DQ22	B24	MB_DATA22
M B DQ21	C20	MB_DATA21
M B DQ20	B20	MB_DATA20
M B DQ19	C25	MB_DATA19
M B DQ18	D24	MB_DATA18
M B DQ17	A21	MB_DATA17
M B DQ16	D20	MB_DATA16
M B DQ15	D19	MB_DATA15
M B DQ14	C18	MB_DATA14
M B DQ13	D14	MB_DATA13
M B DQ12	C14	MB_DATA12
M B DQ11	A20	MB_DATA11
M B DQ10	A19	MB_DATA10
M B DQ9	A16	MB_DATA9
M B DQ8	A15	MB_DATA8
M B DQ7	A13	MB_DATA7
M B DQ6	D12	MB_DATA6
M B DQ5	E11	MB_DATA5
M B DQ4	G11	MB_DATA4
M B DQ3	B14	MB_DATA3
M B DQ2	A14	MB_DATA2
M B DQ1	A11	MB_DATA1
M B DQ0	C11	MB_DATA0

M B DQ52	AE19	MB_DATA52
M B DQ51	AD14	MB_DATA51
M B DQ50	AC14	MB_DATA50
M B DQ49	AE18	MB_DATA49
M B DQ48	AE18	MB_DATA48
M B DQ47	AD20	MB_DATA47
M B DQ46	AC20	MB_DATA46
M B DQ45	AE23	MB_DATA45
M B DQ44	AE24	MB_DATA44
M B DQ43	AE20	MB_DATA43
M B DQ42	AE20	MB_DATA42
M B DQ41	AD22	MB_DATA41
M B DQ40	AC22	MB_DATA40
M B DQ39	AE25	MB_DATA39
M B DQ38	AD26	MB_DATA38
M B DQ37	AA25	MB_DATA37
M B DQ36	AA26	MB_DATA36
M B DQ35	AE24	MB_DATA35
M B DQ34	AD24	MB_DATA34
M B DQ33	AA23	MB_DATA33
M B DQ32	AA24	MB_DATA32
M B DQ31	G24	MB_DATA31
M B DQ30	G23	MB_DATA30
M B DQ29	G26	MB_DATA29
M B DQ28	C26	MB_DATA28
M B DQ27	G26	MB_DATA27
M B DQ26	G25	MB_DATA26
M B DQ25	E24	MB_DATA25
M B DQ24	E23	MB_DATA24
M B DQ23	C24	MB_DATA23
M B DQ22	B24	MB_DATA22
M B DQ21	C20	MB_DATA21
M B DQ20	B20	MB_DATA20
M B DQ19	C25	MB_DATA19
M B DQ18	D24	MB_DATA18
M B DQ17	A21	MB_DATA17
M B DQ16	D20	MB_DATA16
M B DQ15	D19	MB_DATA15
M B DQ14	C18	MB_DATA14
M B DQ13	D14	MB_DATA13
M B DQ12	C14	MB_DATA12
M B DQ11	A20	MB_DATA11
M B DQ10	A19	MB_DATA10
M B DQ9	A16	MB_DATA9
M B DQ8	A15	MB_DATA8
M B DQ7	A13	MB_DATA7
M B DQ6	D12	MB_DATA6
M B DQ5	E11	MB_DATA5
M B DQ4	G11	MB_DATA4
M B DQ3	B14	MB_DATA3
M B DQ2	A14	MB_DATA2
M B DQ1	A11	MB_DATA1
M B DQ0	C11	MB_DATA0

M B DQ52	AE19	MB_DATA52
M B DQ51	AD14	MB_DATA51
M B DQ50	AC14	MB_DATA50
M B DQ49	AE18	MB_DATA49
M B DQ48	AE18	MB_DATA48
M B DQ47	AD20	MB_DATA47
M B DQ46	AC20	MB_DATA46
M B DQ45	AE23	MB_DATA45
M B DQ44	AE24	MB_DATA44
M B DQ43	AE20	MB_DATA43
M B DQ42	AE20	MB_DATA42
M B DQ41	AD22	MB_DATA41
M B DQ40	AC22	MB_DATA40
M B DQ39	AE25	MB_DATA39
M B DQ38	AD26	MB_DATA38
M B DQ37	AA25	MB_DATA37
M B DQ36	AA26	MB_DATA36
M B DQ35	AE24	MB_DATA35
M B DQ34	AD24	MB_DATA34
M B DQ33	AA23	MB_DATA33
M B DQ32	AA24	MB_DATA32
M B DQ31	G24	MB_DATA31
M B DQ30	G23	MB_DATA30
M B DQ29	G26	MB_DATA29
M B DQ28	C26	MB_DATA28
M B DQ27	G26	MB_DATA27
M B DQ26	G25	MB_DATA26
M B DQ25	E24	MB_DATA25
M B DQ24	E23	MB_DATA24
M B DQ23	C24	MB_DATA23
M B DQ22	B24	MB_DATA22
M B DQ21	C20	MB_DATA21
M B DQ20	B20	MB_DATA20
M B DQ19	C25	MB_DATA19
M B DQ18	D24	MB_DATA18
M B DQ17	A21	MB_DATA17
M B DQ16	D20	MB_DATA16
M B DQ15	D19	MB_DATA15
M B DQ14	C18	MB_DATA14
M B DQ13	D14	MB_DATA13
M B DQ12	C14	MB_DATA12
M B DQ11	A20	MB_DATA11
M B DQ10	A19	MB_DATA10
M B DQ9	A16	MB_DATA9
M B DQ8	A15	MB_DATA8
M B DQ7	A13	MB_DATA7
M B DQ6	D12	MB_DATA6
M B DQ5	E11	MB_DATA5
M B DQ4	G11	MB_DATA4
M B DQ3	B14	MB_DATA3
M B DQ2	A14	MB_DATA2
M B DQ1	A11	MB_DATA1
M B DQ0	C11	MB_DATA0

M B DQ52	AE19	MB_DATA52
M B DQ51	AD14	MB_DATA51
M B DQ50	AC14	MB_DATA50
M B DQ49	AE18	MB_DATA49
M B DQ48	AE18	MB_DATA48
M B DQ47	AD20	MB_DATA47
M B DQ46	AC20	MB_DATA46
M B DQ45	AE23	MB_DATA45
M B DQ44	AE24	MB_DATA44
M B DQ43	AE20	MB_DATA43
M B DQ42	AE20	MB_DATA42
M B DQ41	AD22	MB_DATA41
M B DQ40	AC22	MB_DATA40
M B DQ39	AE25	MB_DATA39
M B DQ38	AD26	MB_DATA38
M B DQ37	AA25	MB_DATA37
M B DQ36	AA26	MB_DATA36
M B DQ35	AE24	MB_DATA35
M B DQ34	AD24	MB_DATA34
M B DQ33	AA23	MB_DATA33
M B DQ32	AA24	MB_DATA32
M B DQ31	G24	MB_DATA31
M B DQ30	G23	MB_DATA30
M B DQ29	G26	MB_DATA29
M B DQ28	C26	MB_DATA28
M B DQ27	G26	MB_DATA27
M B DQ26	G25	MB_DATA26
M B DQ25	E24	MB_DATA25
M B DQ24	E23	MB_DATA24
M B DQ23	C24	MB_DATA23
M B DQ22	B24	MB_DATA22
M B DQ21	C20	MB_DATA21
M B DQ20	B20	MB_DATA20
M B DQ19	C25	MB_DATA19
M B DQ18	D24	MB_DATA18
M B DQ17	A21	MB_DATA17
M B DQ16	D20	MB_DATA16
M B DQ15	D19	MB_DATA15
M B DQ14	C18	MB_DATA14
M B DQ13	D14	MB_DATA13
M B DQ12	C14	MB_DATA12
M B DQ11	A20	MB_DATA11
M B DQ10	A19	MB_DATA10
M B DQ9	A16	MB_DATA9
M B DQ8	A15	MB_DATA8
M B DQ7	A13	MB_DATA7
M B DQ6	D12	MB_DATA6
M B DQ5	E11	MB_DATA5
M B DQ4	G11	MB_DATA4
M B DQ3	B14	MB_DATA3
M B DQ2	A14	MB_DATA2
M B DQ1	A11	MB_DATA1
M B DQ0	C11	MB_DATA0

M B DQ41	AD22
M B DQ40	AC22
M B DQ39	AE25
M B DQ38	AD26
M B DQ37	AA25
M B DQ36	AA26
M B DQ35	AE24
M B DQ34	AD24



	1
--	---

3	2	1
---	---	---



2	1
---	---



	1
--	---

2	1
---	---



	1
--	---

	1
--	---

[illegible]

	1
--	---

	1
--	---

	1
--	---

	1
--	---

1

--	--

	1
--	---

1	
---	--

1	
---	--

--	--



SSID = N.B

4 CPUCADOUT[15..0]
4 CPUCADOUTJ[15..0]



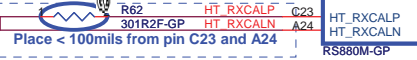
CPUCADOUT0	Y25
CPUCADOUT1	Y24
CPUCADOUT2	V23
CPUCADOUT3	V25
CPUCADOUT4	V24
CPUCADOUT5	U24
CPUCADOUT6	U25
CPUCADOUT7	T25
CPUCADOUT8	T24
CPUCADOUT9	P22
CPUCADOUT10	P23
CPUCADOUT11	P25
CPUCADOUT12	P24
CPUCADOUT13	N24
CPUCADOUT14	N25
CPUCADOUT15	AC24
CPUCADOUT16	AC25
CPUCADOUT17	AB25
CPUCADOUT18	AB24
CPUCADOUT19	AA24
CPUCADOUT20	AA25
CPUCADOUT21	Y22
CPUCADOUT22	Y23
CPUCADOUT23	W21
CPUCADOUT24	W20
CPUCADOUT25	V21
CPUCADOUT26	V20
CPUCADOUT27	U20
CPUCADOUT28	U21
CPUCADOUT29	U19
CPUCADOUT30	U18

4 CPUHTTCLKOUT0
4 CPUHTTCLKOUTJ0
4 CPUHTTCLKOUT1
4 CPUHTTCLKOUTJ1

T22	HT_RXCLK0P
T23	HT_RXCLK0N
AB23	HT_RXCLK1P
AA22	HT_RXCLK1N

4 CPUHTTCTLOUT0
4 CPUHTTCTLOUTJ0
4 CPUHTTCTLOUT1
4 CPUHTTCTLOUTJ1

M22	HT_RXCTL0P
R21	HT_RXCTL0N
R20	HT_RXCTL1P
	HT_RXCTL1N

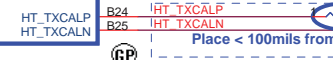


U1001A
PART 1 OF 6
HYPER TRANSPORT CPU I/F

HT_TXCAD0P	D24
HT_TXCAD0N	D25
HT_TXCAD1P	E24
HT_TXCAD1N	E25
HT_TXCAD2P	F24
HT_TXCAD2N	F25
HT_TXCAD3P	F22
HT_TXCAD3N	F23
HT_TXCAD4P	H22
HT_TXCAD4N	H25
HT_TXCAD5P	J25
HT_TXCAD5N	J24
HT_TXCAD6P	K24
HT_TXCAD6N	K25
HT_TXCAD7P	K22
HT_TXCAD7N	K23
HT_TXCAD8P	F21
HT_TXCAD8N	G21
HT_TXCAD9P	G20
HT_TXCAD9N	H21
HT_TXCAD10P	J21
HT_TXCAD10N	J18
HT_TXCAD11P	K17
HT_TXCAD11N	L19
HT_TXCAD12P	J19
HT_TXCAD12N	M19
HT_TXCAD13P	L18
HT_TXCAD13N	M21
HT_TXCAD14P	P21
HT_TXCAD14N	P18
HT_TXCAD15P	M18
HT_TXCAD15N	

HT_TXCLK0P
HT_TXCLK0N
HT_TXCLK1P
HT_TXCLK1N

HT_TXCTL0P
HT_TXCTL0N
HT_TXCTL1P
HT_TXCTL1N



NB0CADOUT0	D24
NB0CADOUT1	E24
NB0CADOUT2	F24
NB0CADOUT3	F22
NB0CADOUT4	H22
NB0CADOUT5	J25
NB0CADOUT6	K24
NB0CADOUT7	K22
NB0CADOUT8	F21
NB0CADOUT9	G21
NB0CADOUT10	H21
NB0CADOUT11	J21
NB0CADOUT12	J18
NB0CADOUT13	M19
NB0CADOUT14	L18
NB0CADOUT15	M21
NB0CADOUT16	P21
NB0CADOUT17	P18
NB0CADOUT18	M18
NB0CADOUT19	

NB0HTTCLKOUT0
NB0HTTCLKOUTJ0
NB0HTTCLKOUT1
NB0HTTCLKOUTJ1

NB0HTTCTLOUT0
NB0HTTCTLOUTJ0
NB0HTTCTLOUT1
NB0HTTCTLOUTJ1



LAN REVERSE

45 PEG_RXN[15..0]
45 PEG_RXP[15..0]

LAN

NEW CARD

WLAN

A-LINK

PEG_RXP15	D4
PEG_RXN15	C4
PEG_RXP14	A3
PEG_RXN14	B3
PEG_RXP13	C2
PEG_RXN13	C1
PEG_RXP12	E5
PEG_RXN12	F5
PEG_RXP11	F5
PEG_RXN11	G6
PEG_RXP10	H5
PEG_RXN10	H6
PEG_RXP9	J6
PEG_RXN9	J5
PEG_RXP8	J7
PEG_RXN8	J8
PEG_RXP7	L5
PEG_RXN7	L6
PEG_RXP6	M8
PEG_RXN6	L8
PEG_RXP5	P7
PEG_RXN5	M7
PEG_RXP4	P5
PEG_RXN4	M5
PEG_RXP3	R8
PEG_RXN3	P8
PEG_RXP2	R6
PEG_RXN2	R5
PEG_RXP1	P4
PEG_RXN1	P3
PEG_RXP0	T4
PEG_RXN0	T3

U1001B
PART 2 OF 6
PCIE I/F GFX

GFX_RX0P	A5
GFX_RX0N	B5
GFX_RX1P	A4
GFX_RX1N	B4
GFX_RX2P	C3
GFX_RX2N	B2
GFX_RX3P	D1
GFX_RX3N	D2
GFX_RX4P	E2
GFX_RX4N	E1
GFX_RX5P	F4
GFX_RX5N	F3
GFX_RX6P	F1
GFX_RX6N	F2
GFX_RX7P	H4
GFX_RX7N	H3
GFX_RX8P	H1
GFX_RX8N	H2
GFX_RX9P	J2
GFX_RX9N	J1
GFX_RX10P	K4
GFX_RX10N	K3
GFX_RX11P	K1
GFX_RX11N	K2
GFX_RX12P	M4
GFX_RX12N	M3
GFX_RX13P	M1
GFX_RX13N	M2
GFX_RX14P	N1
GFX_RX14N	N2
GFX_RX15P	P1
GFX_RX15N	P2

GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
GPP_RX4P
GPP_RX4N
GPP_RX5P
GPP_RX5N

GPP_RX6P
GPP_RX6N
GPP_RX7P
GPP_RX7N
GPP_RX8P
GPP_RX8N
GPP_RX9P
GPP_RX9N
GPP_RX10P
GPP_RX10N
GPP_RX11P
GPP_RX11N
GPP_RX12P
GPP_RX12N
GPP_RX13P
GPP_RX13N
GPP_RX14P
GPP_RX14N
GPP_RX15P
GPP_RX15N

GPP_RX16P
GPP_RX16N
GPP_RX17P
GPP_RX17N
GPP_RX18P
GPP_RX18N
GPP_RX19P
GPP_RX19N
GPP_RX20P
GPP_RX20N
GPP_RX21P
GPP_RX21N
GPP_RX22P
GPP_RX22N
GPP_RX23P
GPP_RX23N
GPP_RX24P
GPP_RX24N
GPP_RX25P
GPP_RX25N

GPP_RX26P
GPP_RX26N
GPP_RX27P
GPP_RX27N
GPP_RX28P
GPP_RX28N
GPP_RX29P
GPP_RX29N
GPP_RX30P
GPP_RX30N
GPP_RX31P
GPP_RX31N
GPP_RX32P
GPP_RX32N
GPP_RX33P
GPP_RX33N
GPP_RX34P
GPP_RX34N
GPP_RX35P
GPP_RX35N

GPP_RX36P
GPP_RX36N
GPP_RX37P
GPP_RX37N
GPP_RX38P
GPP_RX38N
GPP_RX39P
GPP_RX39N
GPP_RX40P
GPP_RX40N
GPP_RX41P
GPP_RX41N
GPP_RX42P
GPP_RX42N
GPP_RX43P
GPP_RX43N
GPP_RX44P
GPP_RX44N
GPP_RX45P
GPP_RX45N

GPP_RX46P
GPP_RX46N
GPP_RX47P
GPP_RX47N
GPP_RX48P
GPP_RX48N
GPP_RX49P
GPP_RX49N
GPP_RX50P
GPP_RX50N
GPP_RX51P
GPP_RX51N
GPP_RX52P
GPP_RX52N
GPP_RX53P
GPP_RX53N
GPP_RX54P
GPP_RX54N
GPP_RX55P
GPP_RX55N

GPP_RX56P
GPP_RX56N
GPP_RX57P
GPP_RX57N
GPP_RX58P
GPP_RX58N
GPP_RX59P
GPP_RX59N
GPP_RX60P
GPP_RX60N
GPP_RX61P
GPP_RX61N
GPP_RX62P
GPP_RX62N
GPP_RX63P
GPP_RX63N
GPP_RX64P
GPP_RX64N
GPP_RX65P
GPP_RX65N

GPP_RX66P
GPP_RX66N
GPP_RX67P
GPP_RX67N
GPP_RX68P
GPP_RX68N
GPP_RX69P
GPP_RX69N
GPP_RX70P
GPP_RX70N
GPP_RX71P
GPP_RX71N
GPP_RX72P
GPP_RX72N
GPP_RX73P
GPP_RX73N
GPP_RX74P
GPP_RX74N
GPP_RX75P
GPP_RX75N

GPP_RX76P
GPP_RX76N
GPP_RX77P
GPP_RX77N
GPP_RX78P
GPP_RX78N
GPP_RX79P
GPP_RX79N
GPP_RX80P
GPP_RX80N
GPP_RX81P
GPP_RX81N
GPP_RX82P
GPP_RX82N
GPP_RX83P
GPP_RX83N
GPP_RX84P
GPP_RX84N
GPP_RX85P
GPP_RX85N

GPP_RX86P
GPP_RX86N
GPP_RX87P
GPP_RX87N
GPP_RX88P
GPP_RX88N
GPP_RX89P
GPP_RX89N
GPP_RX90P
GPP_RX90N
GPP_RX91P
GPP_RX91N
GPP_RX92P
GPP_RX92N
GPP_RX93P
GPP_RX93N
GPP_RX94P
GPP_RX94N
GPP_RX95P
GPP_RX95N

GPP_RX96P
GPP_RX96N
GPP_RX97P
GPP_RX97N
GPP_RX98P
GPP_RX98N
GPP_RX99P
GPP_RX99N
GPP_RX100P
GPP_RX100N
GPP_RX101P
GPP_RX101N
GPP_RX102P
GPP_RX102N
GPP_RX103P
GPP_RX103N
GPP_RX104P
GPP_RX104N
GPP_RX105P
GPP_RX105N

GPP_RX106P
GPP_RX106N
GPP_RX107P
GPP_RX107N
GPP_RX108P
GPP_RX108N
GPP_RX109P
GPP_RX109N
GPP_RX110P
GPP_RX110N
GPP_RX111P
GPP_RX111N
GPP_RX112P
GPP_RX112N
GPP_RX113P
GPP_RX113N
GPP_RX114P
GPP_RX114N
GPP_RX115P
GPP_RX115N

GPP_RX116P
GPP_RX116N
GPP_RX117P
GPP_RX117N
GPP_RX118P
GPP_RX118N
GPP_RX119P
GPP_RX119N
GPP_RX120P
GPP_RX120N
GPP_RX121P
GPP_RX121N
GPP_RX122P
GPP_RX122N
GPP_RX123P
GPP_RX123N
GPP_RX124P
GPP_RX124N
GPP_RX125P
GPP_RX125N

SCD1U10V2KX-5GP	PEG_TXP15
SCD1U10V2KX-5GP	PEG_TXN15
SCD1U10V2KX-5GP	PEG_TXP14
SCD1U10V2KX-5GP	PEG_TXN14
SCD1U10V2KX-5GP	PEG_TXP13
SCD1U10V2KX-5GP	PEG_TXN13
SCD1U10V2KX-5GP	PEG_TXP12
SCD1U10V2KX-5GP	PEG_TXN12
SCD1U10V2KX-5GP	PEG_TXP11
SCD1U10V2KX-5GP	PEG_TXN11
SCD1U10V2KX-5GP	PEG_TXP10
SCD1U10V2KX-5GP	PEG_TXN10
SCD1U10V2KX-5GP	PEG_TXP9
SCD1U10V2KX-5GP	PEG_TXN9
SCD1U10V2KX-5GP	PEG_TXP8
SCD1U10V2KX-5GP	PEG_TXN8
SCD1U10V2KX-5GP	PEG_TXP7
SCD1U10V2KX-5GP	PEG_TXN7
SCD1U10V2KX-5GP	PEG_TXP6
SCD1U10V2KX-5GP	PEG_TXN6
SCD1U10V2KX-5GP	PEG_TXP5
SCD1U10V2KX-5GP	PEG_TXN5
SCD1U10V2KX-5GP	PEG_TXP4
SCD1U10V2KX-5GP	PEG_TXN4
SCD1U10V2KX-5GP	PEG_TXP3
SCD1U10V2KX-5GP	PEG_TXN3
SCD1U10V2KX-5GP	PEG_TXP2
SCD1U10V2KX-5GP	PEG_TXN2
SCD1U10V2KX-5GP	PEG_TXP1
SCD1U10V2KX-5GP	PEG_TXN1
SCD1U10V2KX-5GP	PEG_TXP0
SCD1U10V2KX-5GP	PEG_TXN0

PCIE_TXP0 NB
PCIE_TXN0 NB

PCIE_TXP1 NB
PCIE_TXN1 NB
PCIE_TXP2 NB
PCIE_TXN2 NB
PCIE_TXP3 NB
PCIE_TXN3 NB
PCIE_TXP4 NB
PCIE_TXN4 NB
PCIE_TXP5 NB
PCIE_TXN5 NB
PCIE_TXP6 NB
PCIE_TXN6 NB
PCIE_TXP7 NB
PCIE_TXN7 NB
PCIE_TXP8 NB
PCIE_TXN8 NB
PCIE_TXP9 NB
PCIE_TXN9 NB
PCIE_TXP10 NB
PCIE_TXN10 NB
PCIE_TXP11 NB
PCIE_TXN11 NB
PCIE_TXP12 NB
PCIE_TXN12 NB
PCIE_TXP13 NB
PCIE_TXN13 NB
PCIE_TXP14 NB
PCIE_TXN14 NB
PCIE_TXP15 NB
PCIE_TXN15 NB

PCIE_TXP16 NB
PCIE_TXN16 NB
PCIE_TXP17 NB
PCIE_TXN17 NB
PCIE_TXP18 NB
PCIE_TXN18 NB
PCIE_TXP19 NB
PCIE_TXN19 NB
PCIE_TXP20 NB
PCIE_TXN20 NB
PCIE_TXP21 NB
PCIE_TXN21 NB
PCIE_TXP22 NB
PCIE_TXN22 NB
PCIE_TXP23 NB
PCIE_TXN23 NB
PCIE_TXP24 NB
PCIE_TXN24 NB
PCIE_TXP25 NB
PCIE_TXN25 NB

PCIE_TXP26 NB
PCIE_TXN26 NB
PCIE_TXP27 NB
PCIE_TXN27 NB
PCIE_TXP28 NB
PCIE_TXN28 NB
PCIE_TXP29 NB
PCIE_TXN29 NB
PCIE_TXP30 NB
PCIE_TXN30 NB
PCIE_TXP31 NB
PCIE_TXN31 NB
PCIE_TXP32 NB
PCIE_TXN32 NB
PCIE_TXP33 NB
PCIE_TXN33 NB
PCIE_TXP34 NB
PCIE_TXN34 NB
PCIE_TXP35 NB
PCIE_TXN35 NB

PCIE_TXP36 NB
PCIE_TXN36 NB
PCIE_TXP37 NB
PCIE_TXN37 NB
PCIE_TXP38 NB
PCIE_TXN38 NB
PCIE_TXP39 NB
PCIE_TXN39 NB
PCIE_TXP40 NB
PCIE_TXN40 NB
PCIE_TXP41 NB
PCIE_TXN41 NB
PCIE_TXP42 NB
PCIE_TXN42 NB
PCIE_TXP43 NB
PCIE_TXN43 NB
PCIE_TXP44 NB
PCIE_TXN44 NB
PCIE_TXP45 NB
PCIE_TXN45 NB

PCIE_TXP46 NB
PCIE_TXN46 NB
PCIE_TXP47 NB
PCIE_TXN47 NB
PCIE_TXP48 NB
PCIE_TXN48 NB
PCIE_TXP49 NB
PCIE_TXN49 NB
PCIE_TXP50 NB
PCIE_TXN50 NB
PCIE_TXP51 NB
PCIE_TXN51 NB
PCIE_TXP52 NB
PCIE_TXN52 NB
PCIE_TXP53 NB
PCIE_TXN53 NB
PCIE_TXP54 NB
PCIE_TXN54 NB
PCIE_TXP55 NB
PCIE_TXN55 NB

PCIE_TXP56 NB
PCIE_TXN56 NB
PCIE_TXP57 NB
PCIE_TXN57 NB
PCIE_TXP58 NB
PCIE_TXN58 NB
PCIE_TXP59 NB
PCIE_TXN59 NB
PCIE_TXP60 NB
PCIE_TXN60 NB
PCIE_TXP61 NB
PCIE_TXN61 NB
PCIE_TXP62 NB
PCIE_TXN62 NB
PCIE_TXP63 NB
PCIE_TXN63 NB
PCIE_TXP64 NB
PCIE_TXN64 NB
PCIE_TXP65 NB
PCIE_TXN65 NB

PCIE_TXP66 NB
PCIE_TXN66 NB
PCIE_TXP67 NB
PCIE_TXN67 NB
PCIE_TXP68 NB
PCIE_TXN68 NB
PCIE_TXP69 NB
PCIE_TXN69 NB
PCIE_TXP70 NB
PCIE_TXN70 NB
PCIE_TXP71 NB
PCIE_TXN71 NB
PCIE_TXP72 NB
PCIE_TXN72 NB
PCIE_TXP73 NB
PCIE_TXN73 NB
PCIE_TXP74 NB
PCIE_TXN74 NB
PCIE_TXP75 NB
PCIE_TXN75 NB

PCIE_TXP76 NB
PCIE_TXN76 NB
PCIE_TXP77 NB
PCIE_TXN77 NB
PCIE_TXP78 NB
PCIE_TXN78 NB
PCIE_TXP79 NB
PCIE_TXN79 NB
PCIE_TXP80 NB
PCIE_TXN80 NB
PCIE_TXP81 NB
PCIE_TXN81 NB
PCIE_TXP82 NB
PCIE_TXN82 NB
PCIE_TXP83 NB
PCIE_TXN83 NB
PCIE_TXP84 NB
PCIE_TXN84 NB
PCIE_TXP85 NB
PCIE_TXN85 NB

PCIE_TXP86 NB
PCIE_TXN86 NB
PCIE_TXP87 NB
PCIE_TXN87 NB
PCIE_TXP88 NB
PCIE_TXN88 NB
PCIE_TXP89 NB
PCIE_TXN89 NB
PCIE_TXP90 NB
PCIE_TXN90 NB
PCIE_TXP91 NB
PCIE_TXN91 NB
PCIE_TXP92 NB
PCIE_TXN92 NB
PCIE_TXP93 NB
PCIE_TXN93 NB
PCIE_TXP94 NB
PCIE_TXN94 NB
PCIE_TXP95 NB
PCIE_TXN95 NB

PCIE_TXP96 NB
PCIE_TXN96 NB
PCIE_TXP97 NB
PCIE_TXN97 NB
PCIE_TXP98 NB
PCIE_TXN98 NB
PCIE_TXP99 NB
PCIE_TXN99 NB
PCIE_TXP100 NB
PCIE_TXN100 NB
PCIE_TXP101 NB
PCIE_TXN101 NB
PCIE_TXP102 NB
PCIE_TXN102 NB
PCIE_TXP103 NB
PCIE_TXN103 NB
PCIE_TXP104 NB
PCIE_TXN104 NB
PCIE_TXP105 NB
PCIE_TXN105 NB

PCIE_TXP106 NB
PCIE_TXN106 NB
PCIE_TXP107 NB
PCIE_TXN107 NB
PCIE_TXP108 NB
PCIE_TXN108 NB
PCIE_TXP109 NB
PCIE_TXN109 NB
PCIE_TXP110 NB
PCIE_TXN110 NB
PCIE_TXP111 NB
PCIE_TXN111 NB
PCIE_TXP112 NB
PCIE_TXN112 NB
PCIE_TXP113 NB
PCIE_TXN113 NB
PCIE_TXP114 NB
PCIE_TXN114 NB
PCIE_TXP115 NB
PCIE_TXN115 NB

PCIE_TXP116 NB
PCIE_TXN116 NB
PCIE_TXP117 NB
PCIE_TXN117 NB
PCIE_TXP118 NB
PCIE_TXN118 NB
PCIE_TXP119 NB
PCIE_TXN119 NB
PCIE_TXP120 NB
PCIE_TXN120 NB
PCIE_TXP121 NB
PCIE_TXN121 NB
PCIE_TXP122 NB
PCIE_TXN122 NB
PCIE_TXP123 NB
PCIE_TXN123 NB
PCIE_TXP124 NB
PCIE_TXN124 NB
PCIE_TXP125 NB
PCIE_TXN125 NB

LAN REVERSE

PEG_TXP1[15..0]
PEG_TXN1[15..0]

LAN

NEW CARD

WLAN

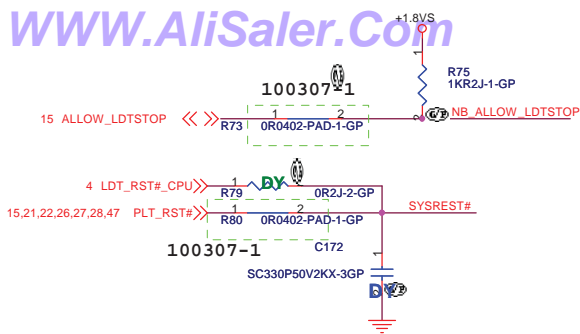
A-LINK

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

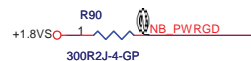
File: **RS880M HT LINK&PCIE(1/4)**

Size: A3 Document Number: **PATEK** Rev: SA

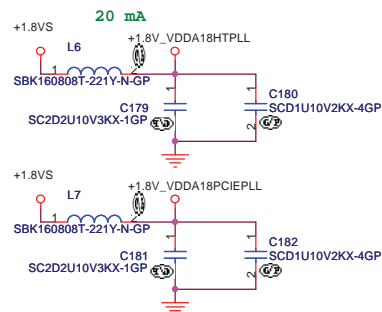
Date: Monday, March 15, 2010 Sheet: 9 of 57



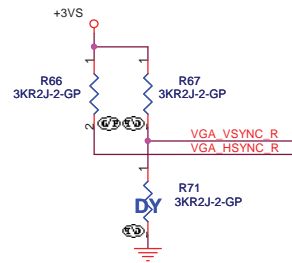
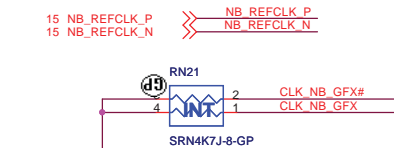
Close to NB ball



ENABLE External CLK GEN



	GPIO MODE	
STRP_DATA	0	1
NB_VDDC	1.1V	0.95V



PART 3 OF 6

CRT/TVOUT

PWR
LVTM

CLO

MIS.

RS880M-GF

STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable      * 1 : Disable
```

RS880: Enables Side port memory (RS880 use HSYNC)

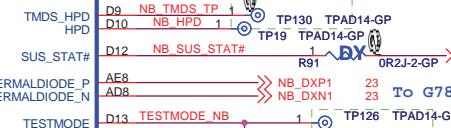
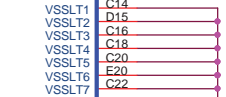
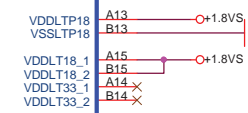
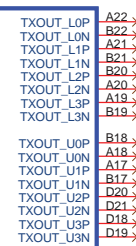
0 : Enable 1 : Disable

SUS_STAT#

```

*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
    or use default values if not connected

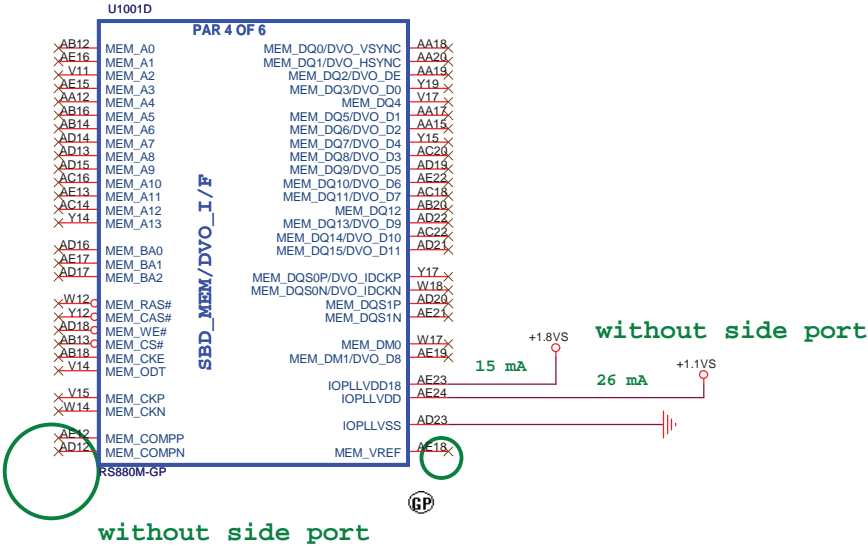
```



<Core Design>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

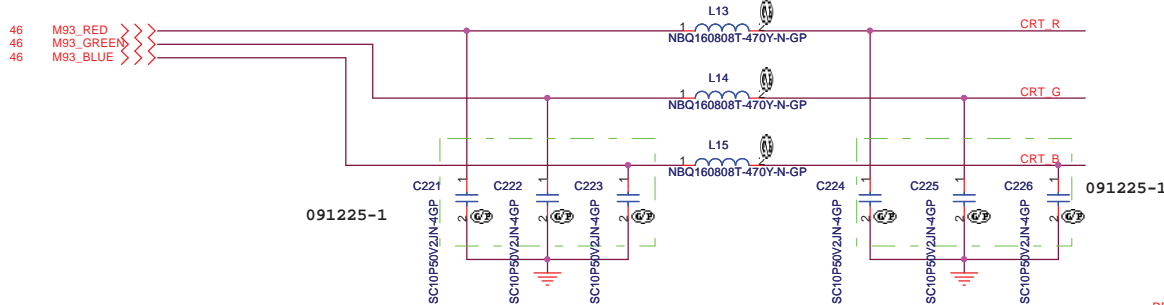
Title			
RS880M LVDS&CRT(2/4)			
Size A3	Document Number		Rev
	PATEK		SA
Date:	Monday, March 15, 2010	Sheet	10 of 57





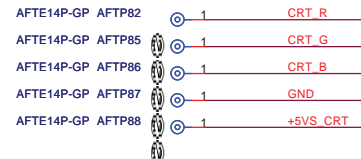
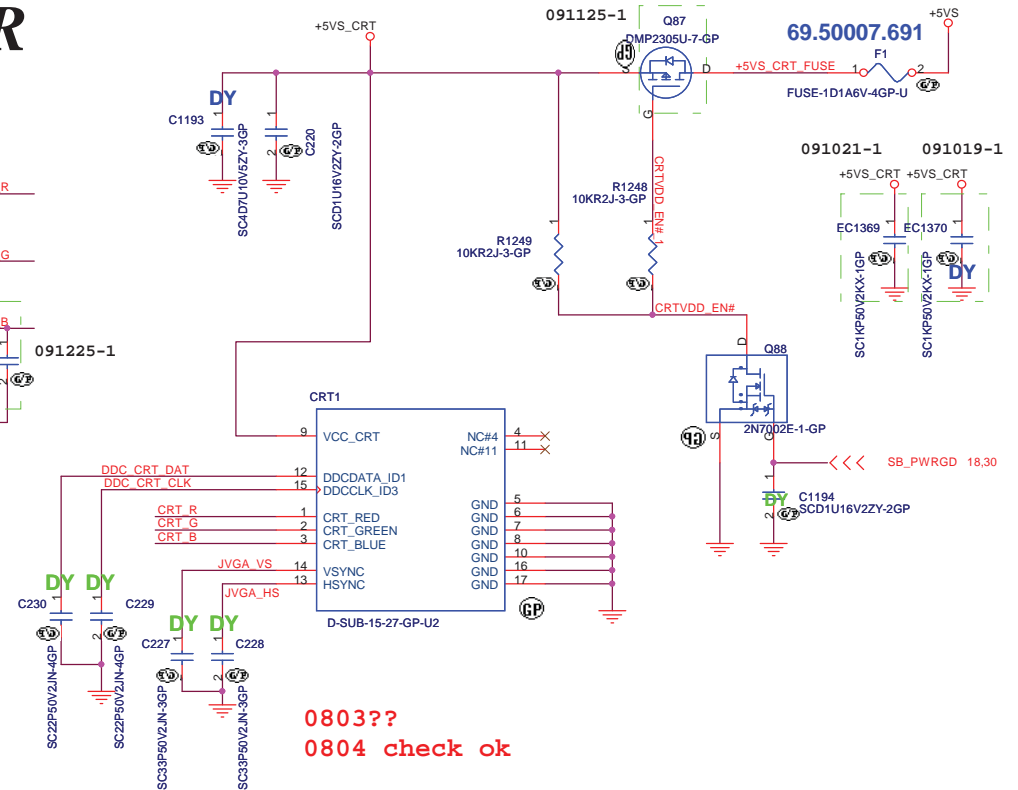
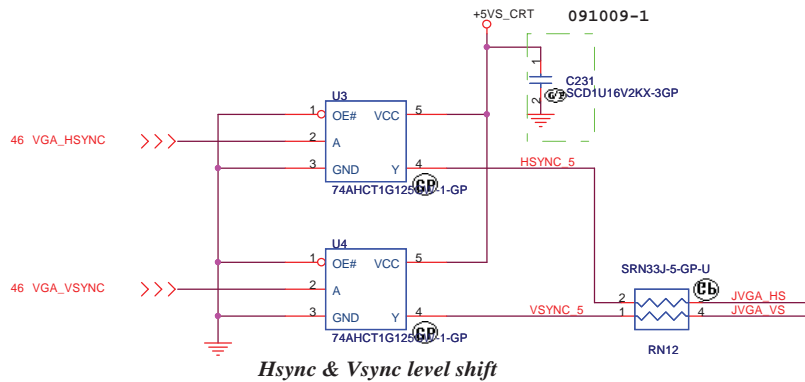
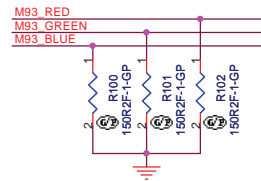
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

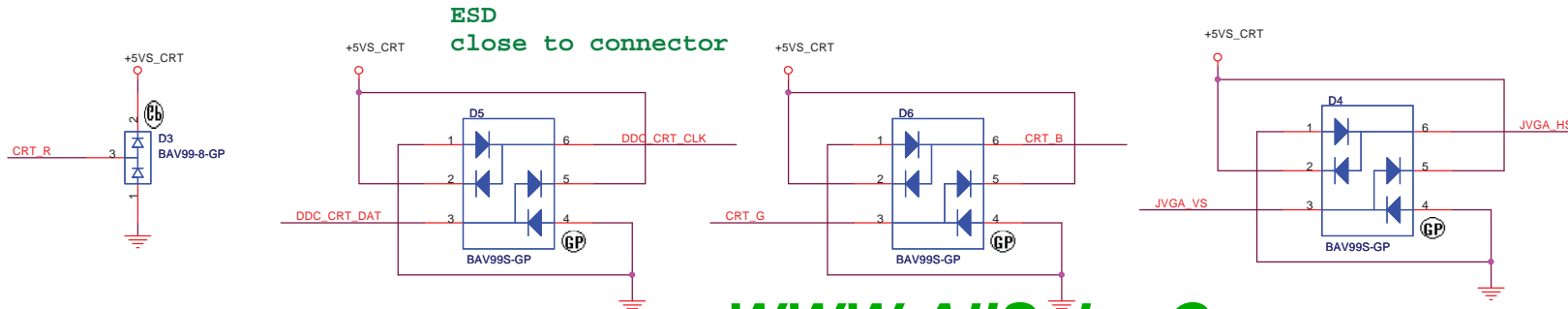


Layout Note:


* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



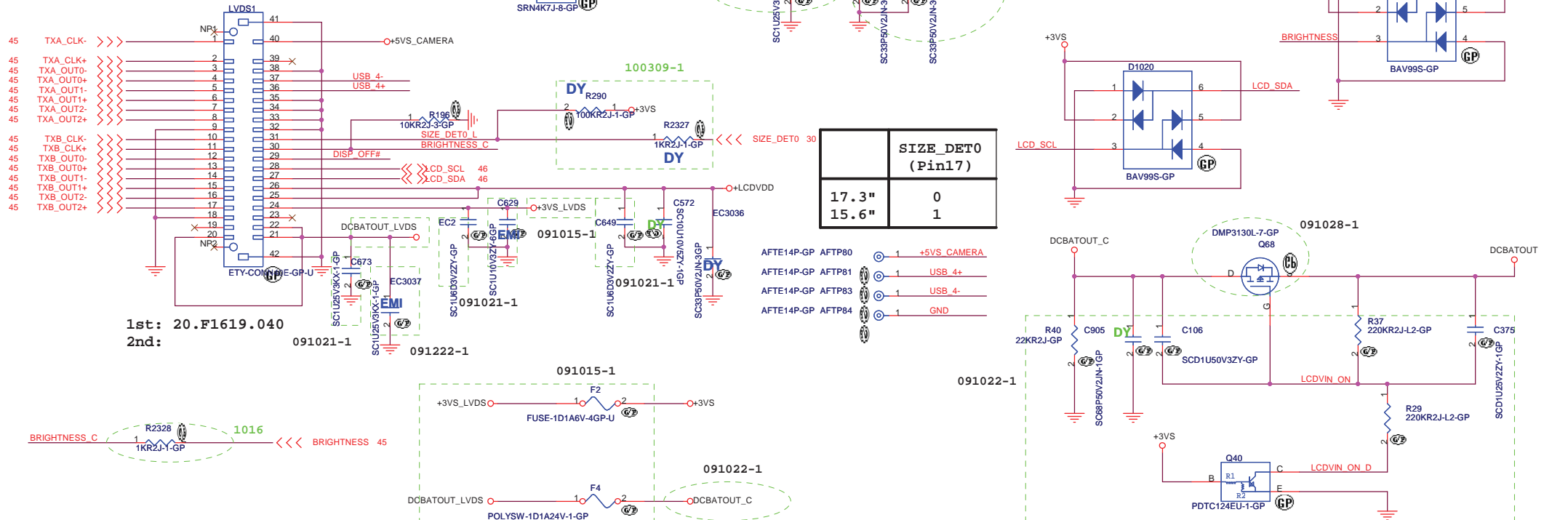
DDC_CRT_DAT& DDC_CRT_CLK
The signal is 5V-tolerant on RS880M.



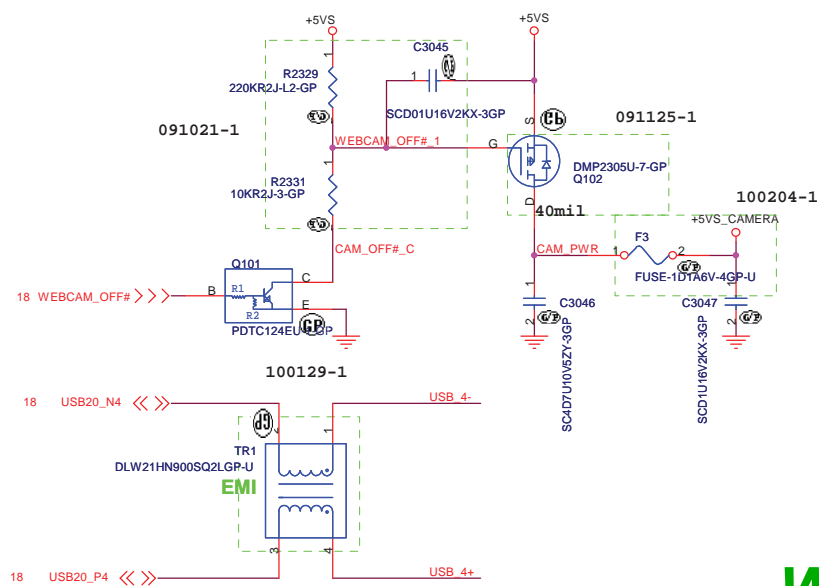
<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CRT CONNECTOR			
Size A3	Document Number PATEK		Rev SA
Date:	Monday, March 15, 2010	Sheet	13 of 57

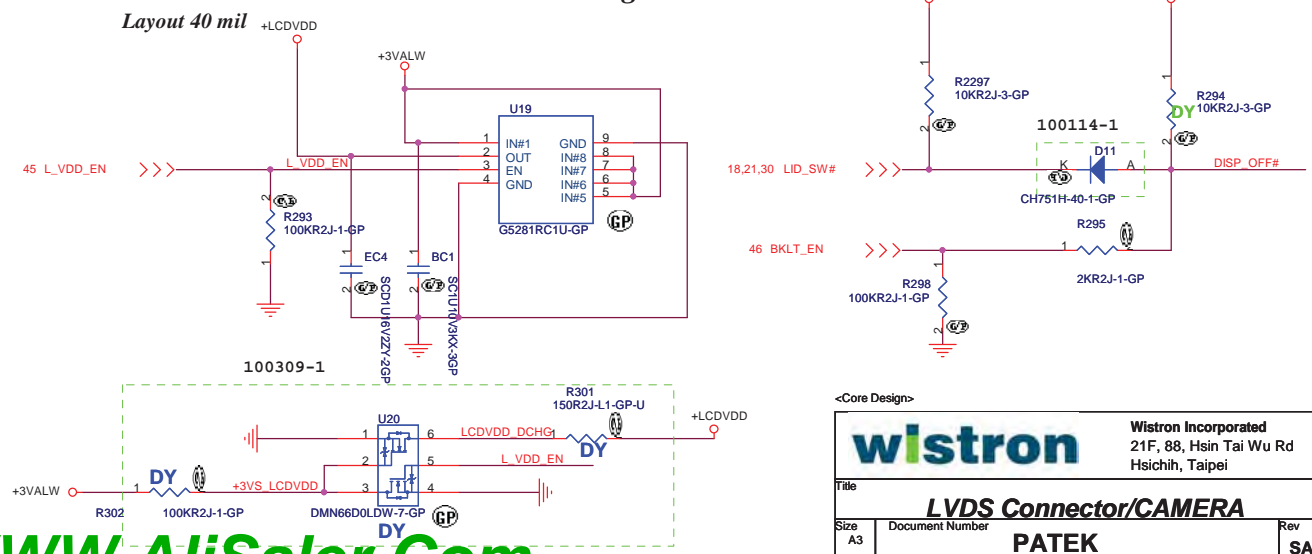
LVDS CONNECTOR

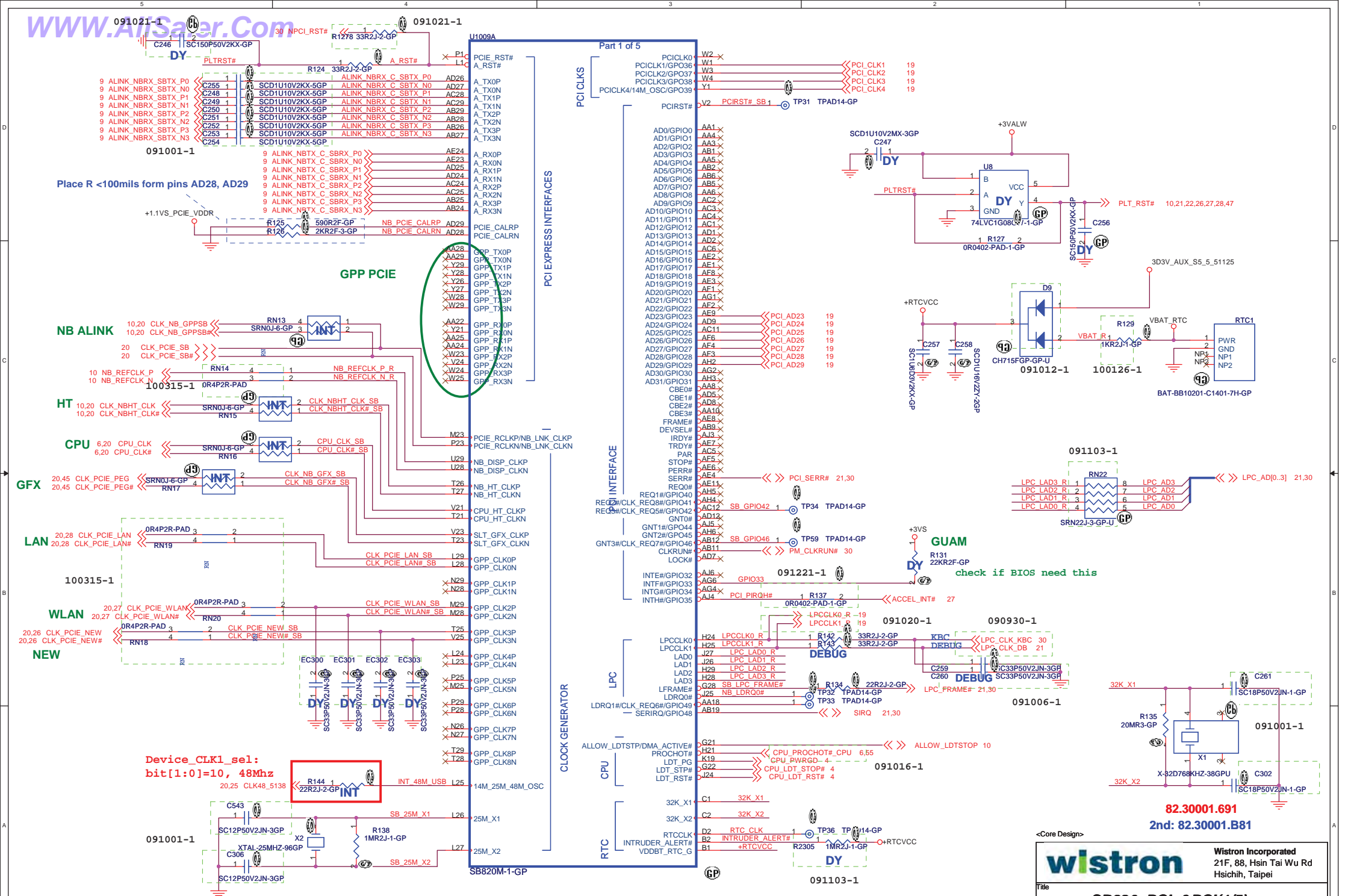


Camera Power&Interface



LCD Power&Discharge





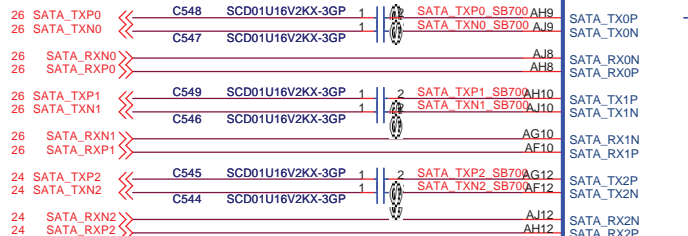
SSID = S.B

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

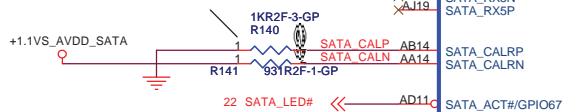
SATA HDD

SATA ODD

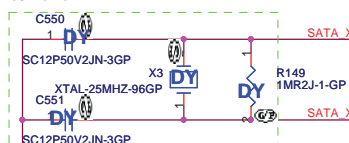
ESATA



Very Close to SB820

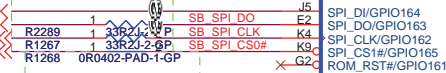


091020-1



100307-1

30 KBC_SPI_SO
30 KBC_SPI_SI
30 KBC_SPI_CLK
30 KBC_SPI_CS0#



091221-1

SB820M-1-GP

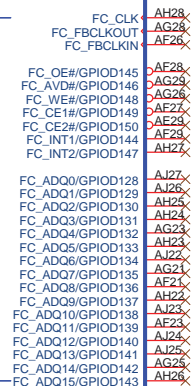
Part 2 of 5

SERIAL ATA

HW MONITOR

SPI ROM

FLASH



NC#G27
NC2#Y2

GP

091027-1

091221-1

<<< WLAN_TRANSMIT_OFF# 27

>>> BT_OFF 24

<<< WWAN_TRANSMIT_OFF# 57

close to R171

R171 10KR2J-3-GP

R2325 0R0402-PAD-1-GP

G+3VS

C3040 SC33P50V2JN-3GP

091019-1

10KR2J-3-GP

R2291 0R2J-2-GP

R2317 10KR2J-3-GP

R2290 0R0402-PAD-1-GP

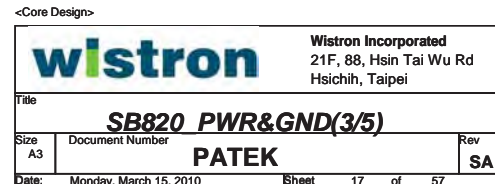
R2319 0R2J-2-GP

>>> HDD_HALTED 22

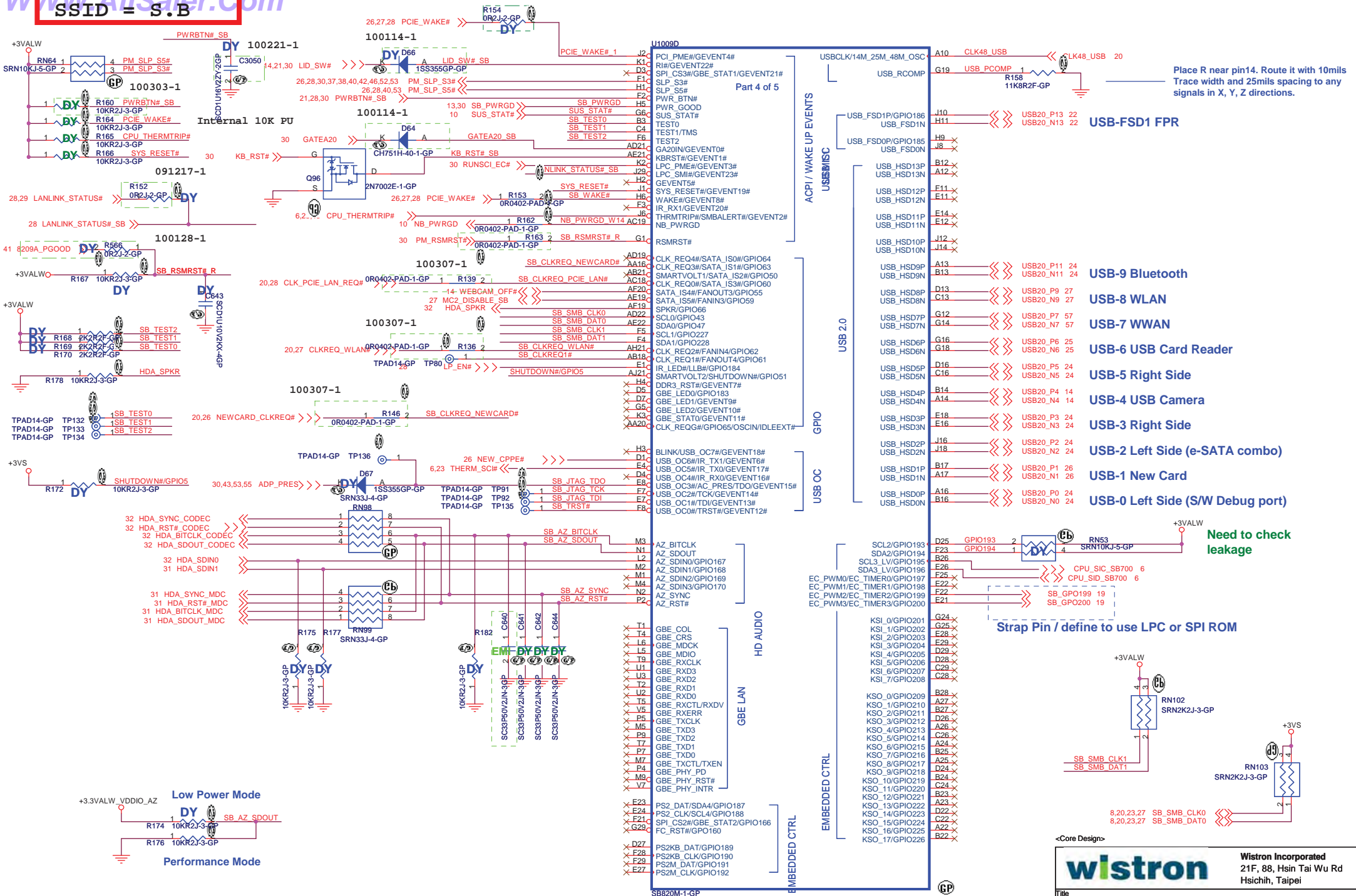
091217-1

<Core Design>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
SB820 SATA&IDE(2/5)			
Size	Document Number	Rev	
A3	PATEK	SA	
Date	Monday, March 15, 2010	Sheet	16 of 57



SSID = S.B



Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

USB-FSD1 FPR

USB-9 Bluetooth

USB-8 WLAN

USB-7 WWAN

USB-6 USB Card Reader

USB-5 Right Side

USB-4 USB Camera

USB-3 Right Side

USB-2 Left Side (e-SATA combo)

USB-1 New Card

USB-0 Left Side (S/W Debug port)

Need to check leakage

Strap Pin / define to use LPC or SPI ROM

<Core Design>

wistron

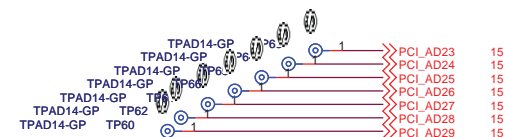
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **SB820 USB&GPIO(4/5)**

Size: A3	Document Number: PATEK	Rev: SA
Date: Monday, March 15, 2010	Sheet: 18	of 57

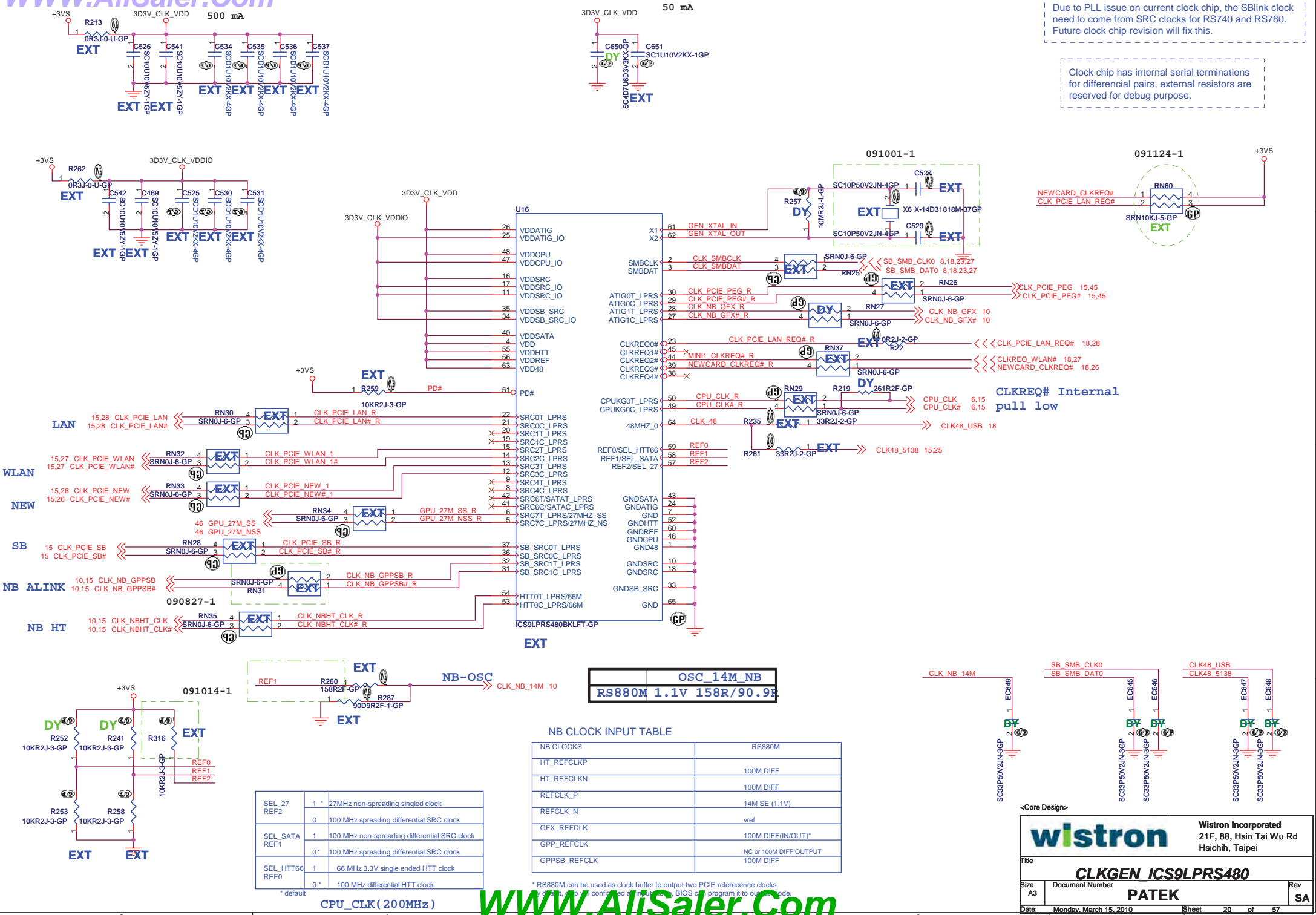


DEBUG STRAPS



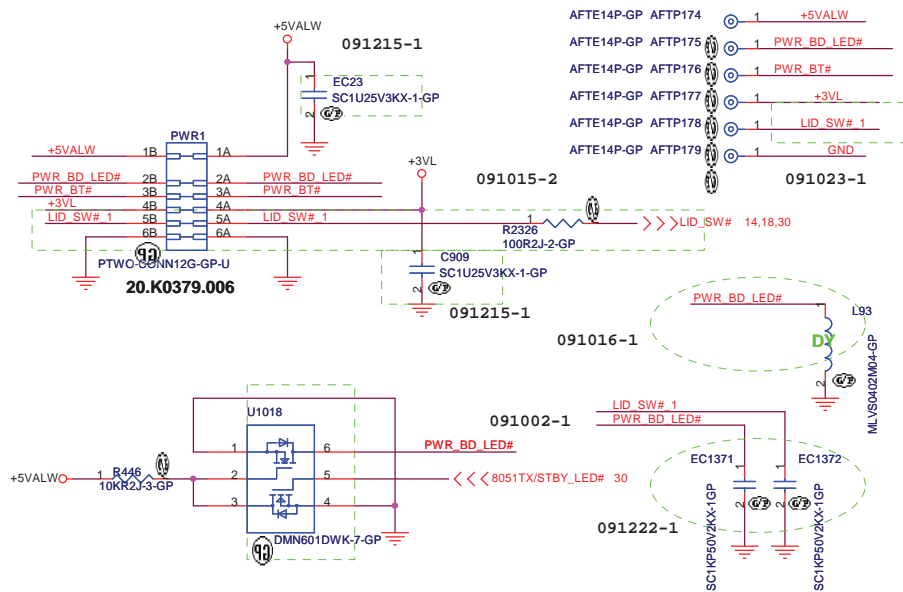
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

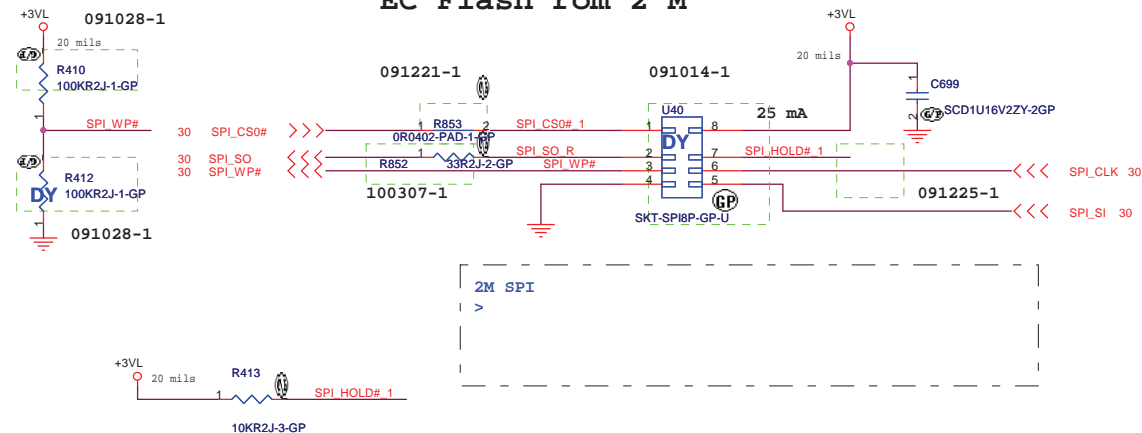


POWER SW CONN.

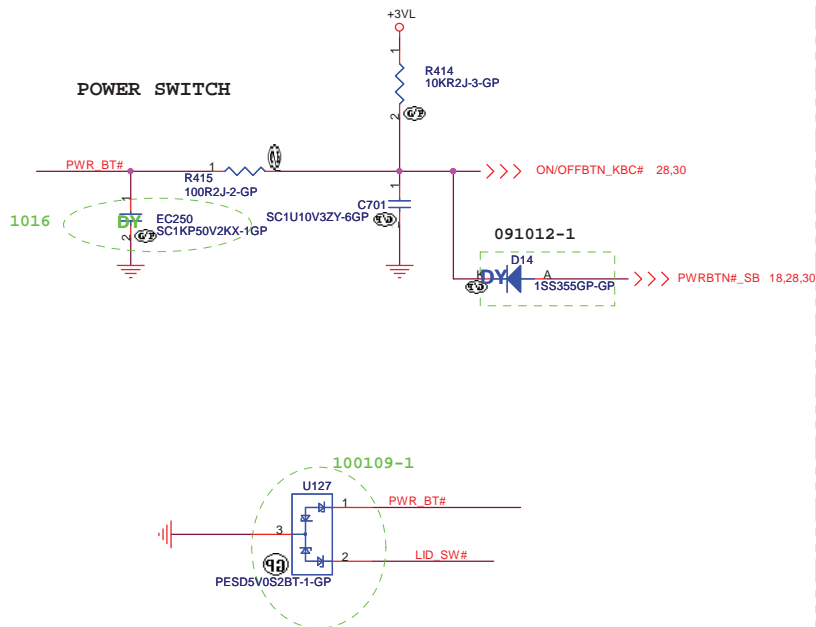
COVER SWITCH



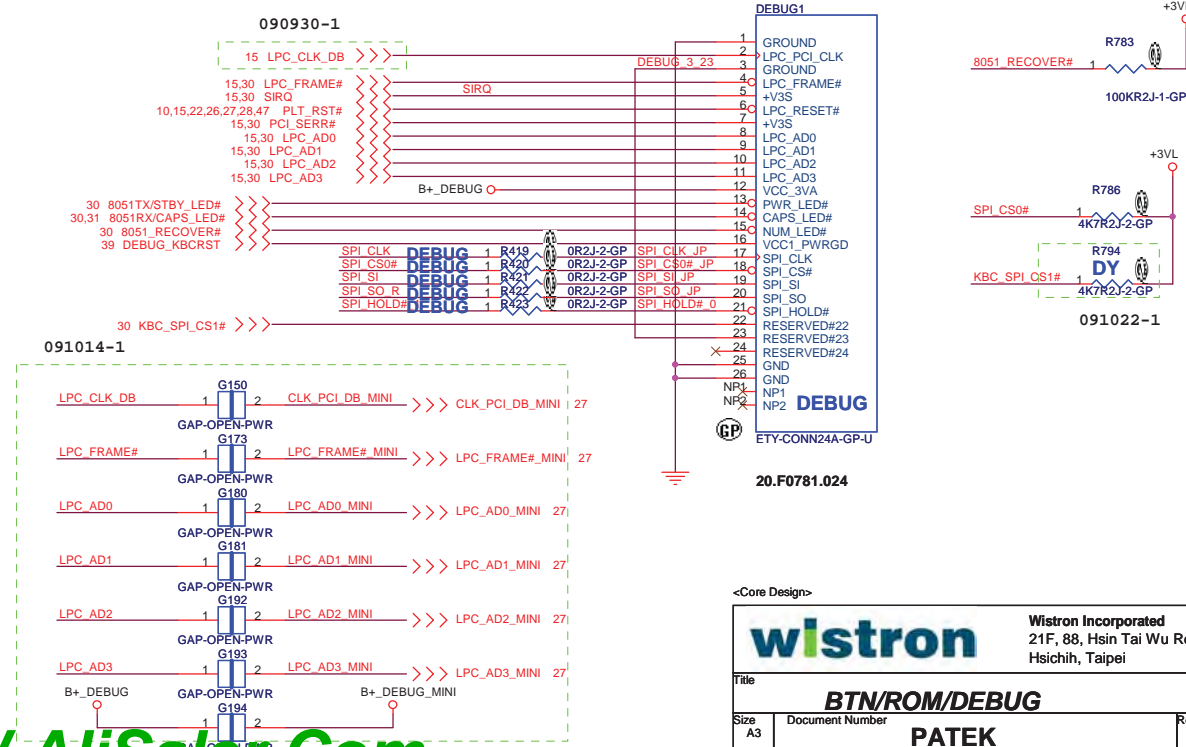
EC Flash rom 2 M

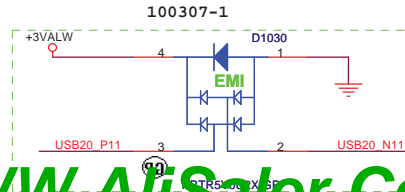
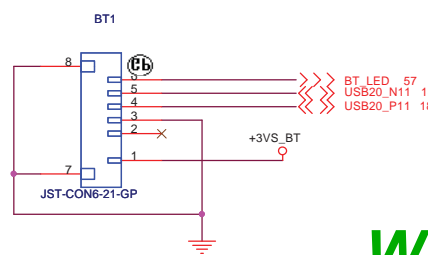
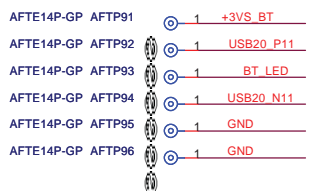
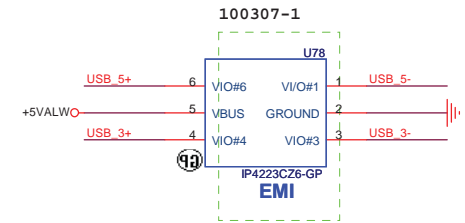
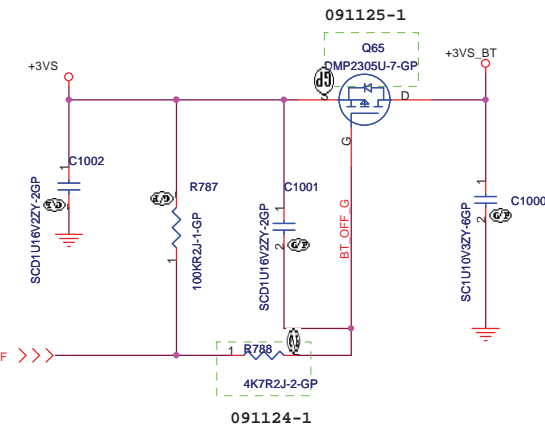
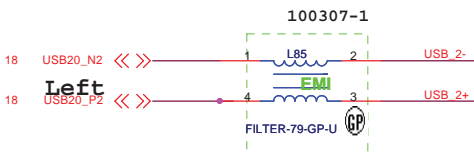
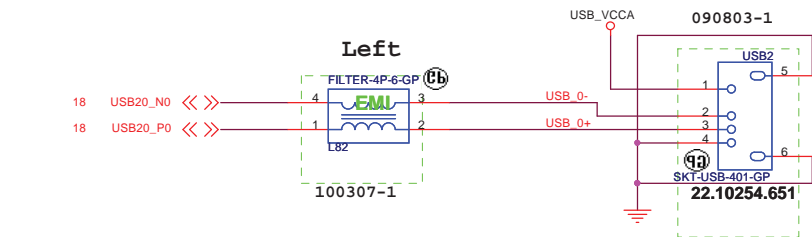
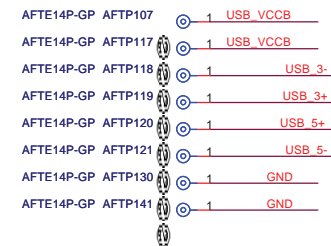
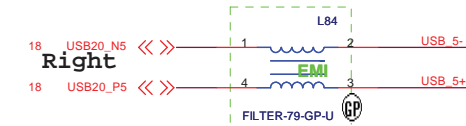
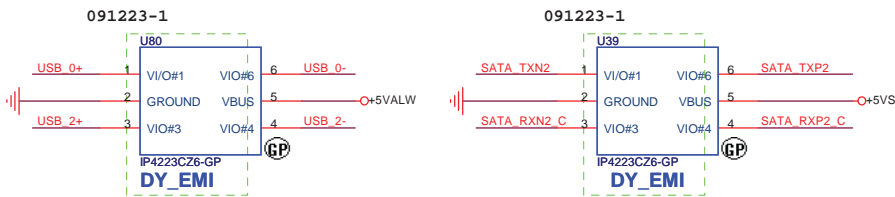
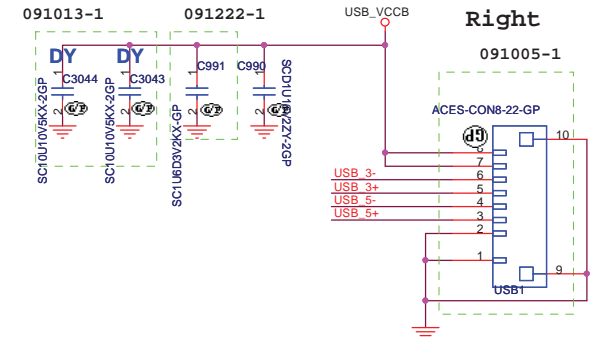
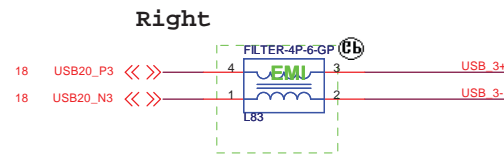
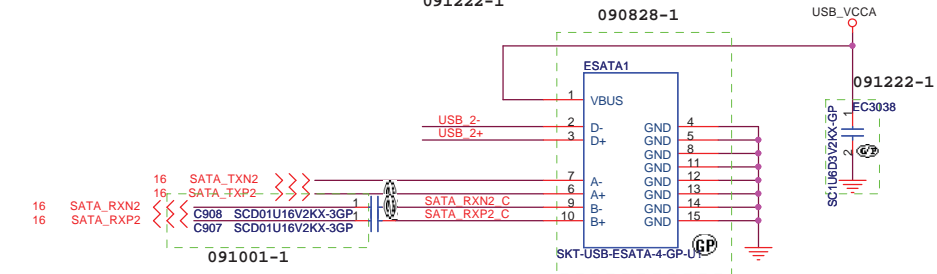
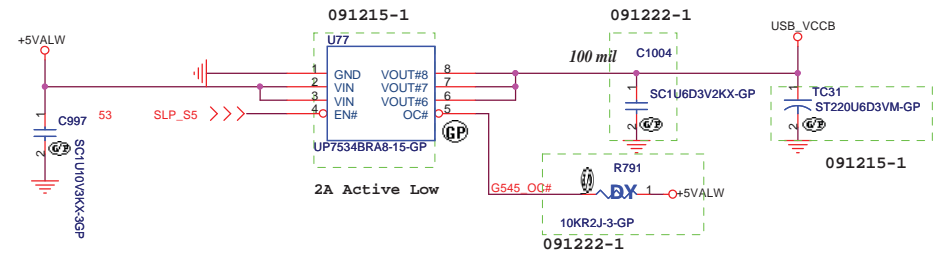
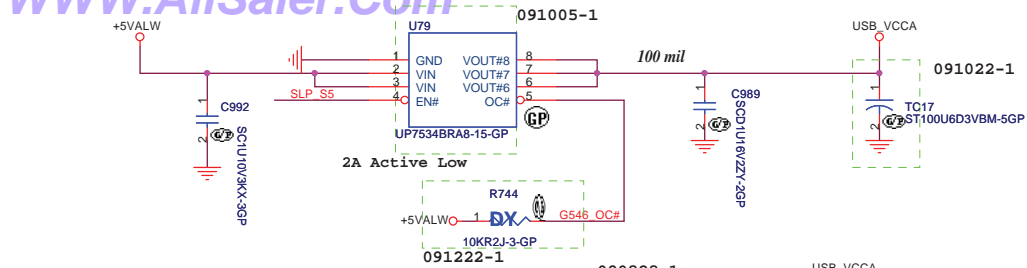


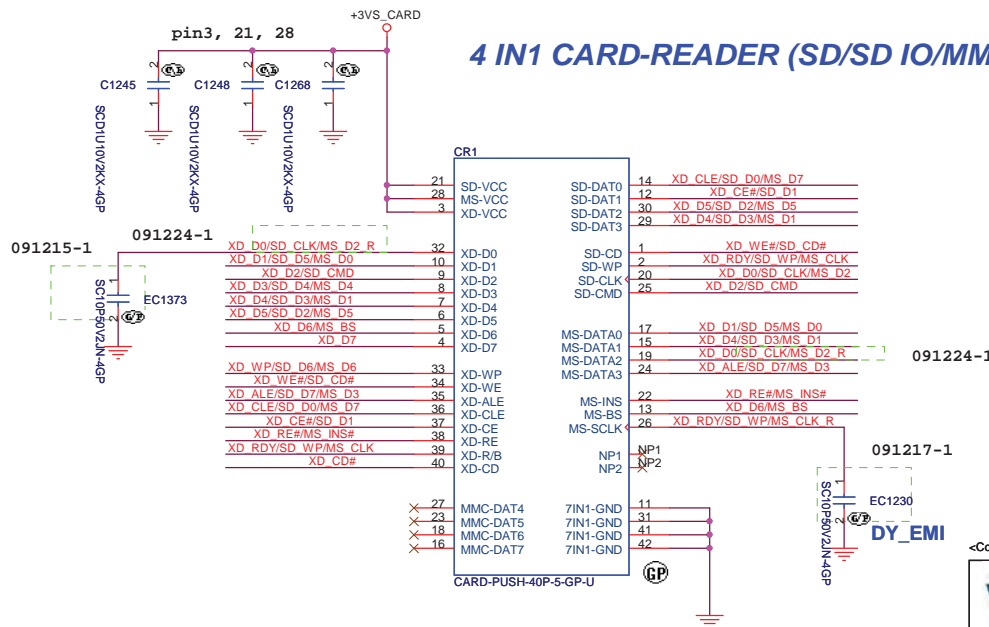
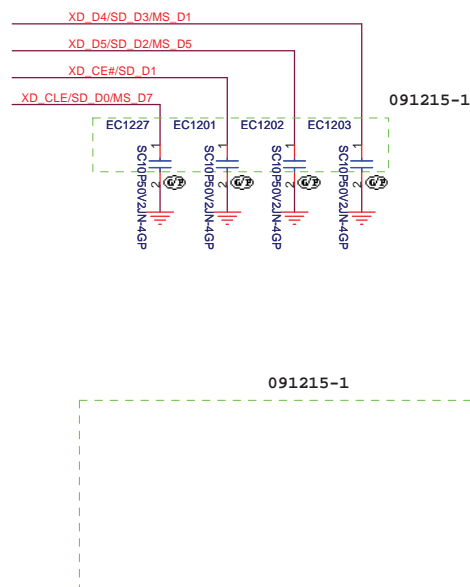
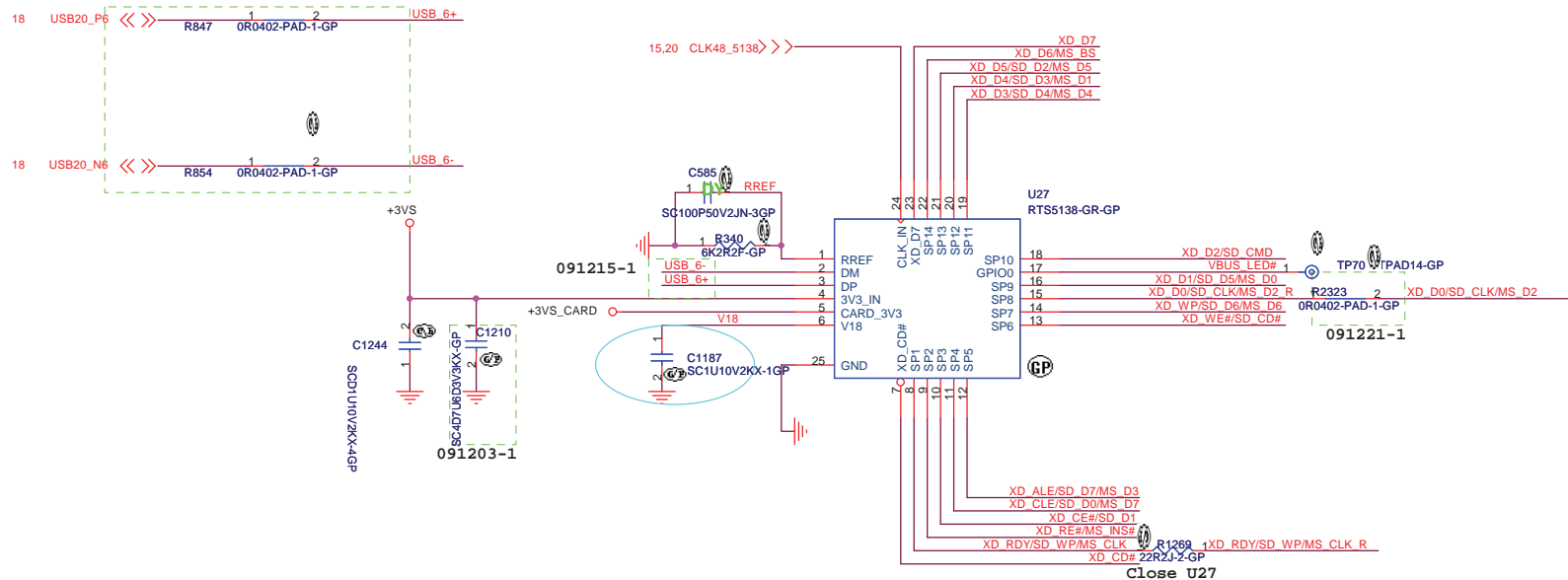
Power SW Circuit

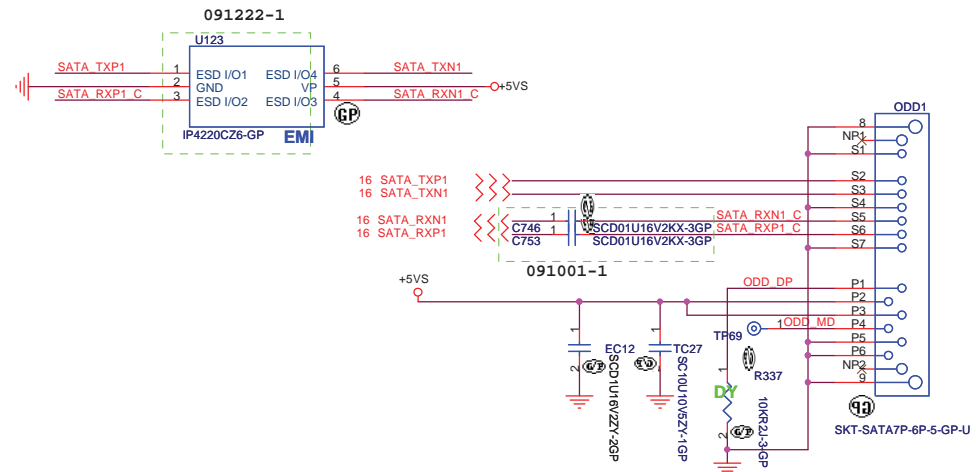
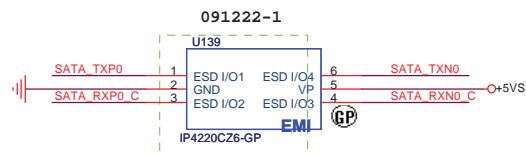


24 PIN LPC DEBUG CONN.

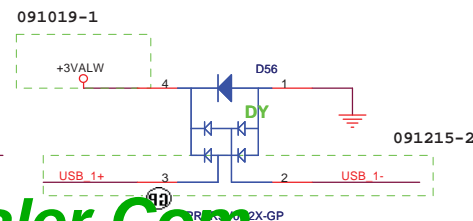
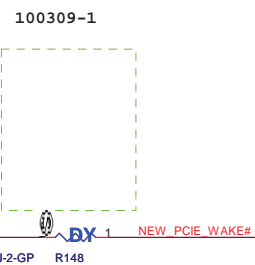
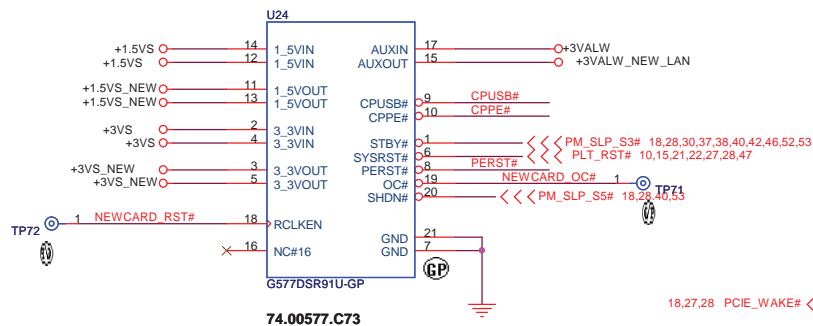
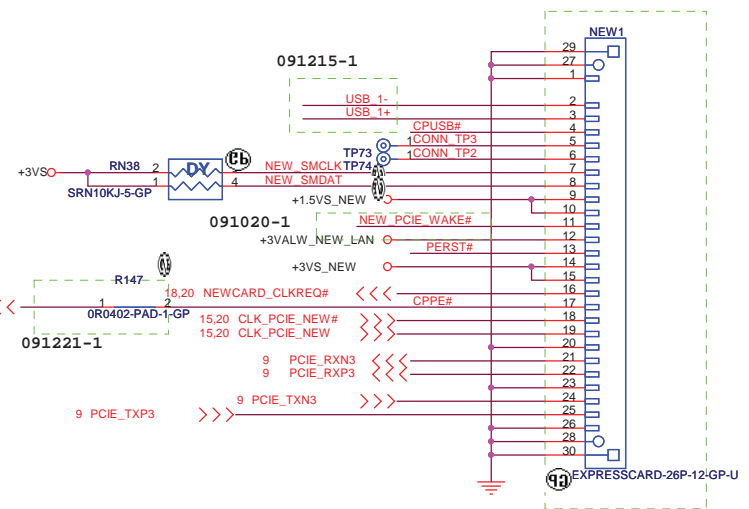
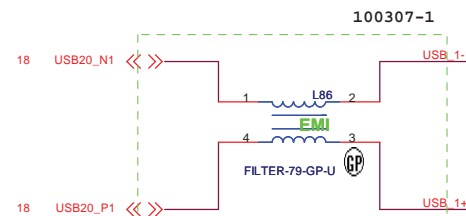
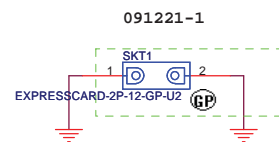








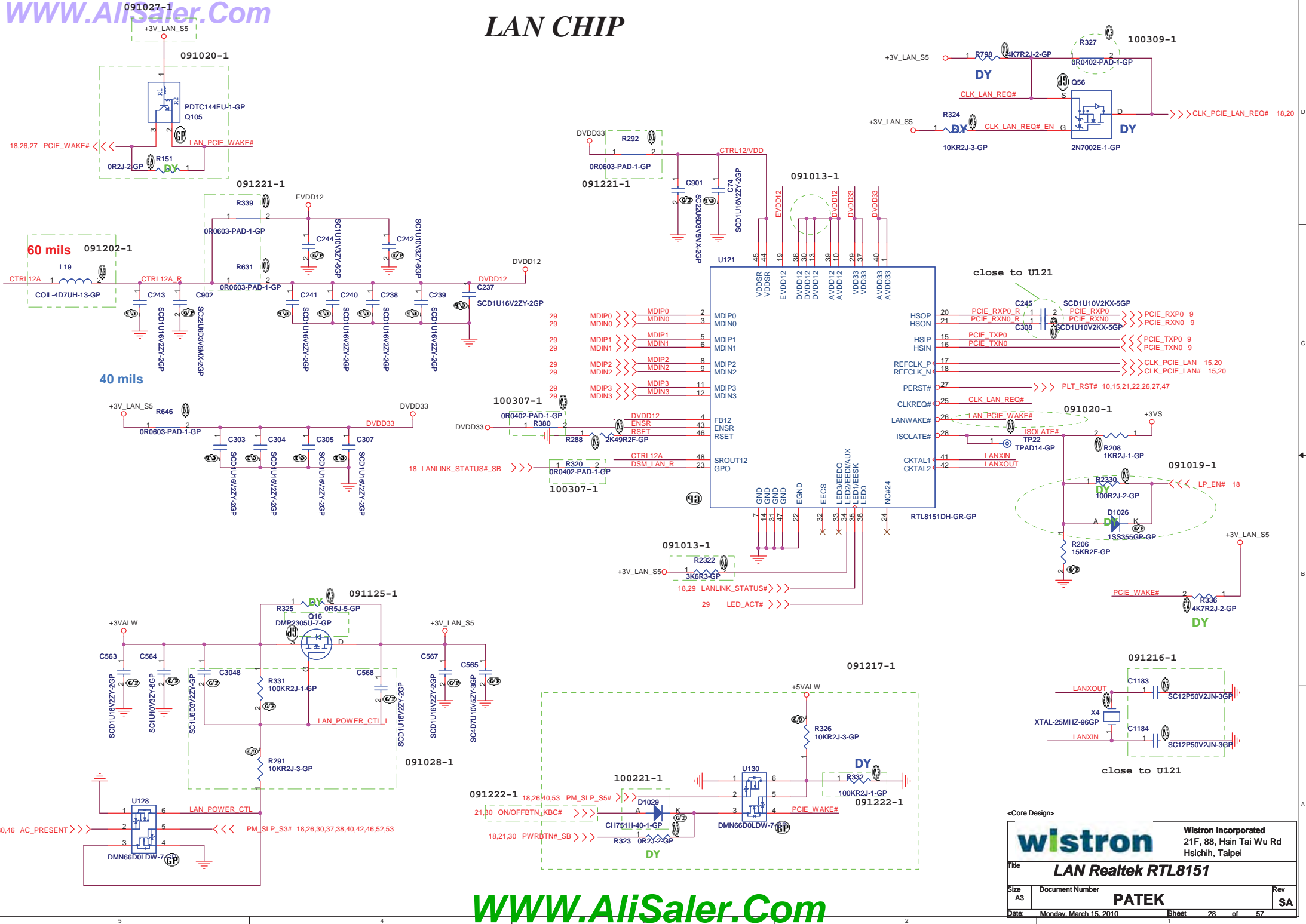
091014-1

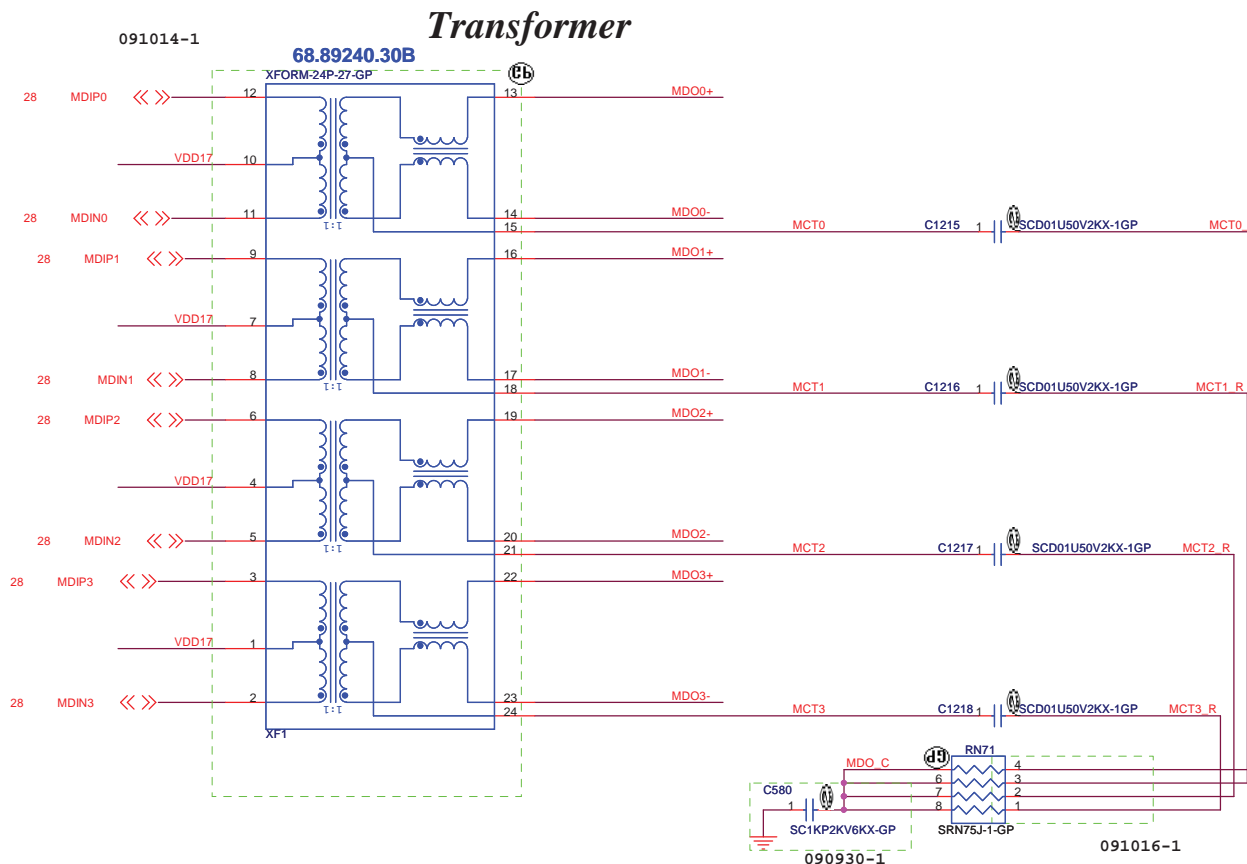
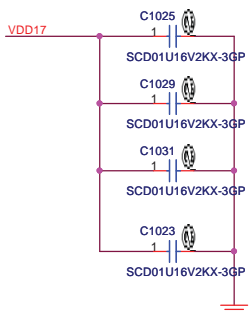


Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

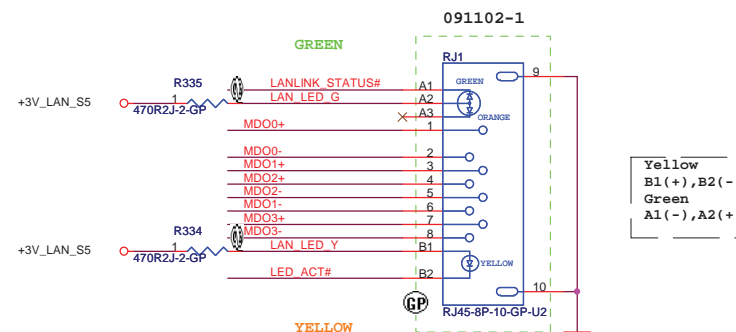
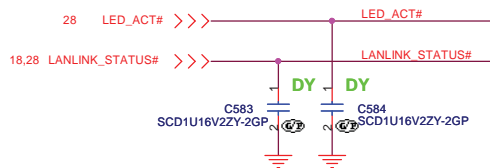
Sheet 26 of

LAN CHIP



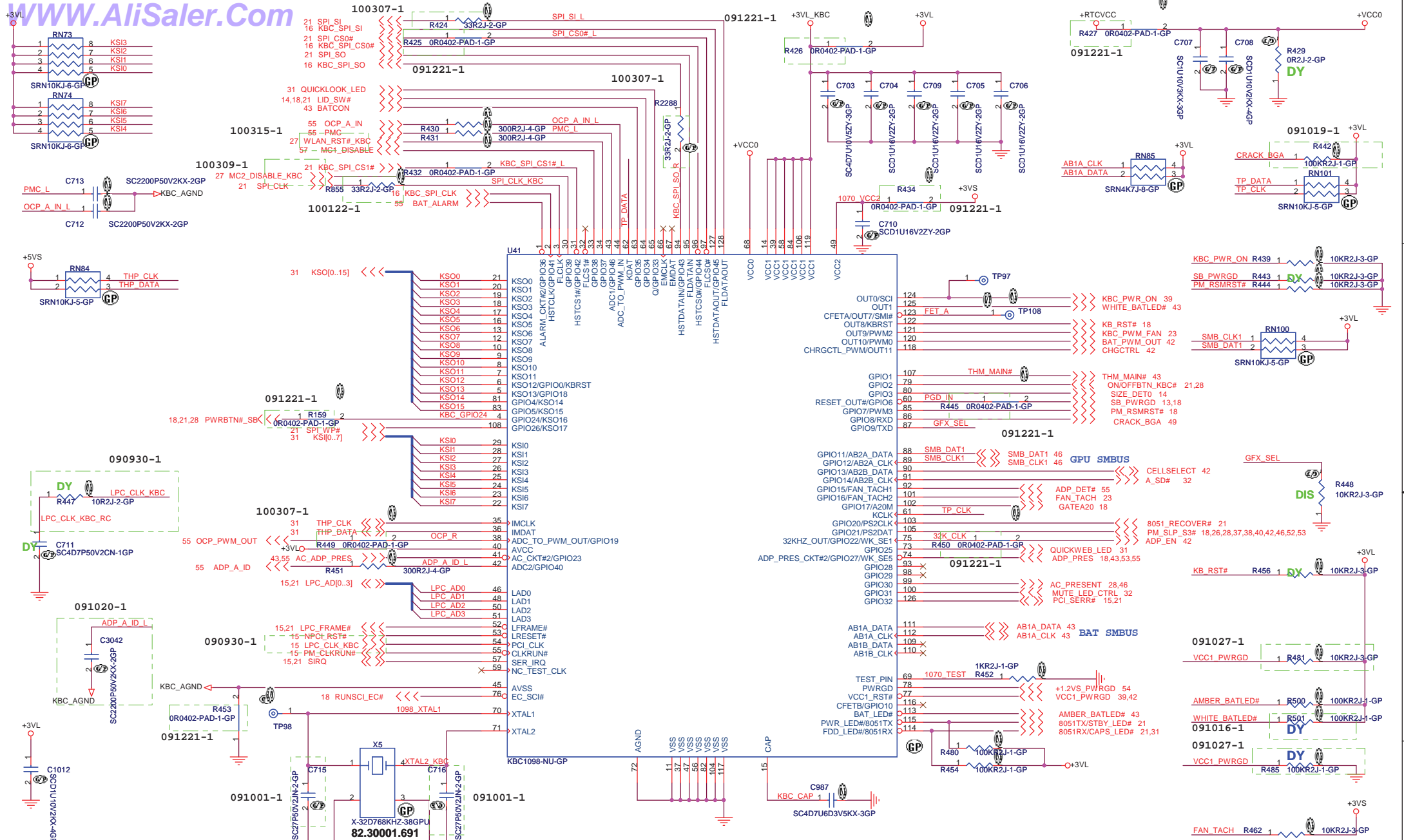


LAN Conn



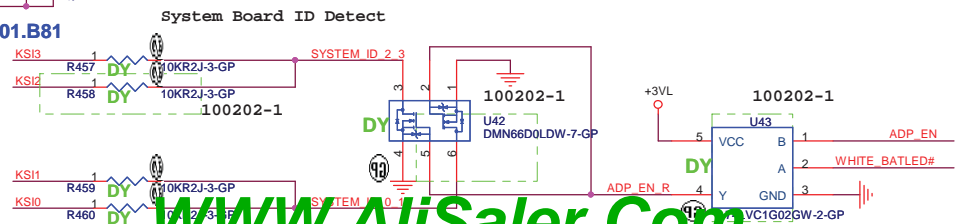
<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
Magnetic & RJ45			
Size A3	Document Number	PATEK	Rev SC
Date:	Monday, March 15, 2010	Sheet	29 of 57



ID	R460	R459	R458	R457
DB1	X			
DB2	X			
DBx	X			
SI1		X		
SI2		X		
SIx		X		
PV			X	
N/A				
N/A				
PVx			X	
N/A				
N/A				
MV				

Layout Notes:
Make sure that the stubs to the test points (KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.

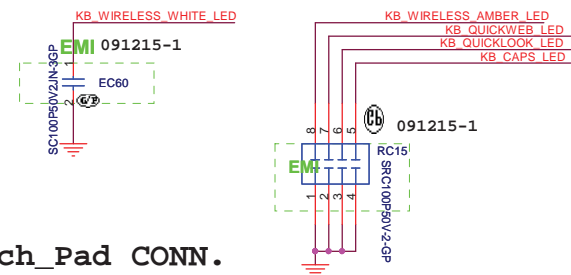
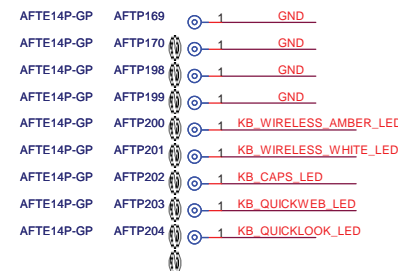
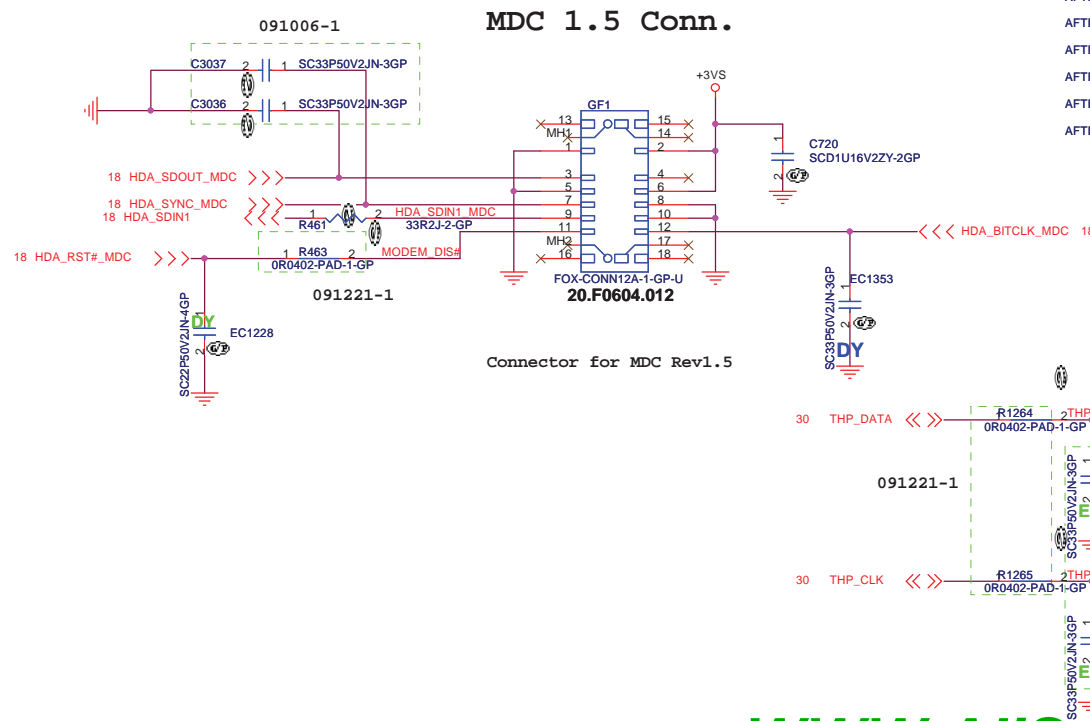
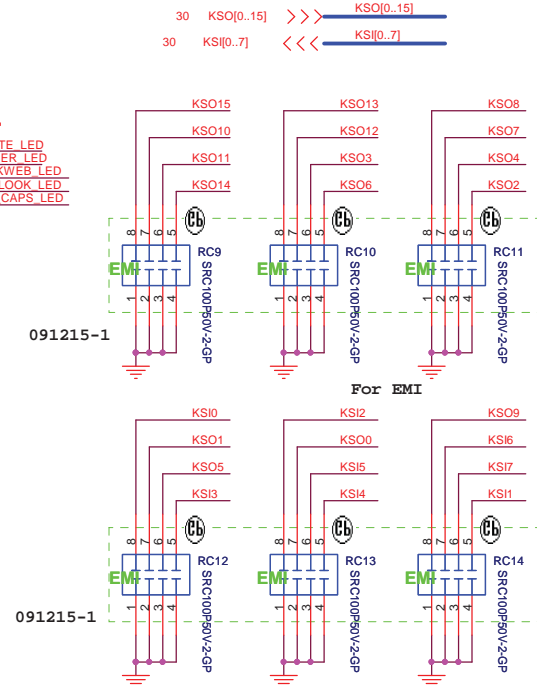
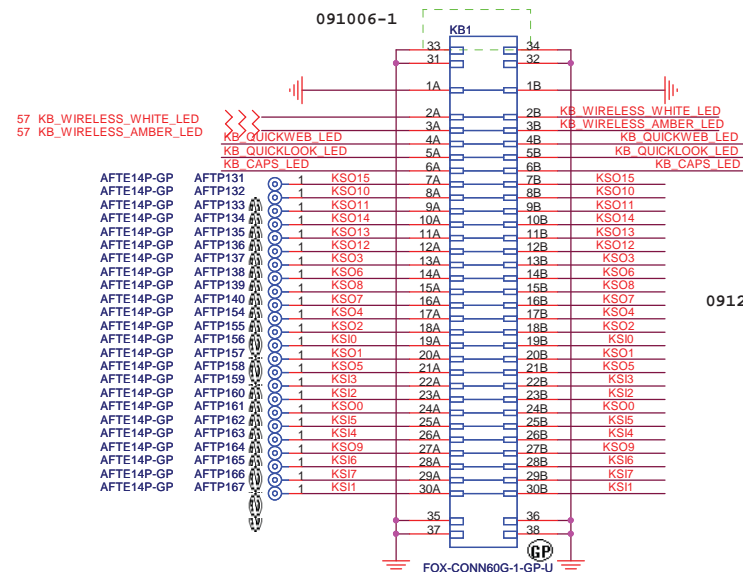
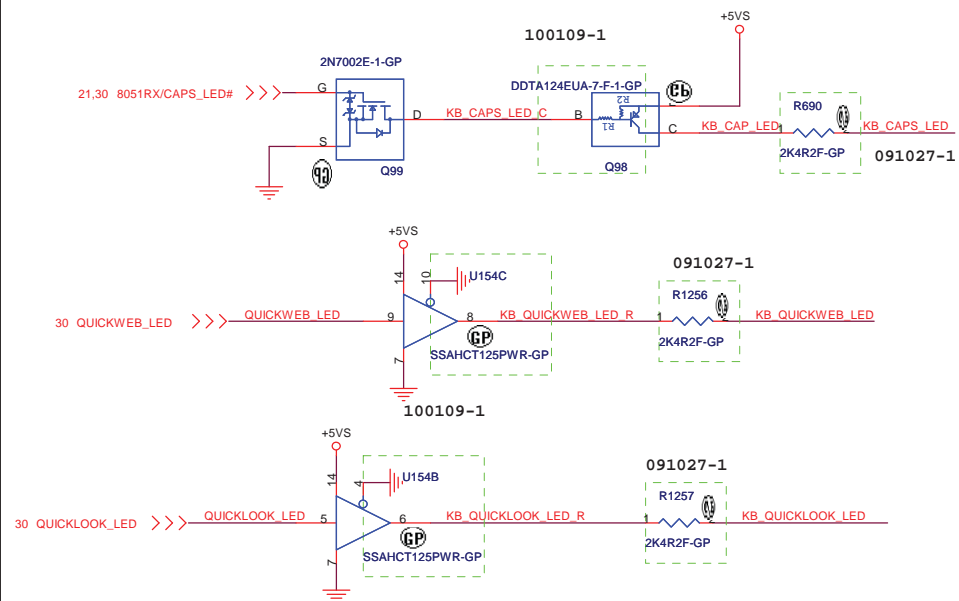


Wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

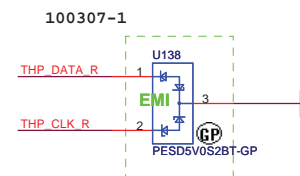
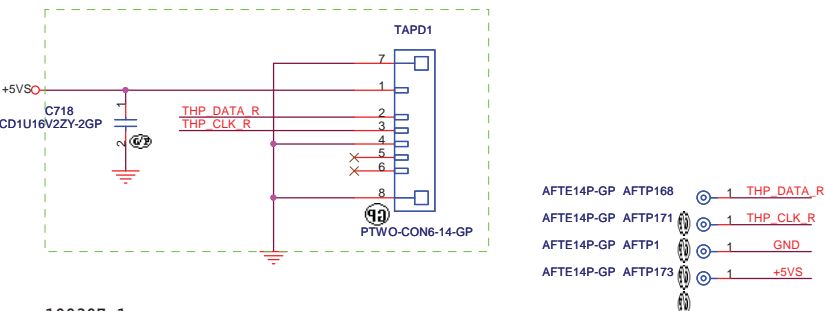
KBC 1098

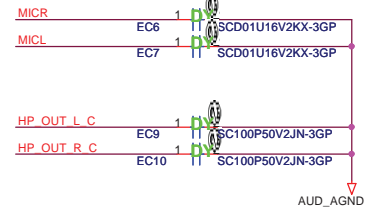
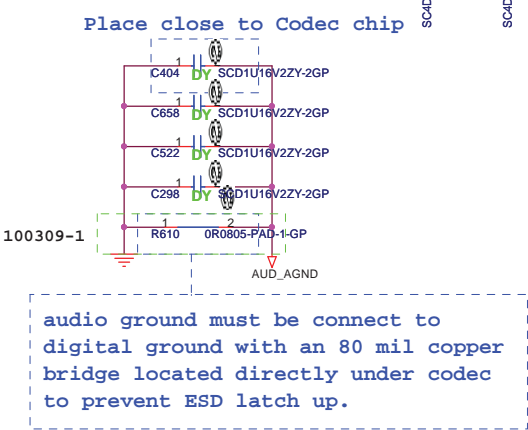
Size A3 Document Number **PATEK** Rev SA

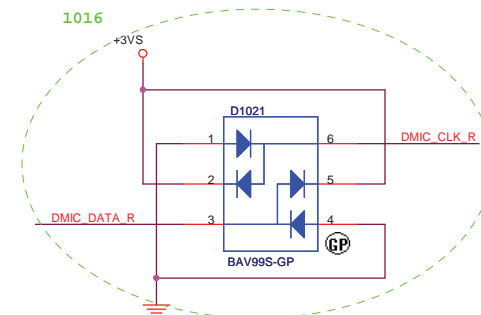
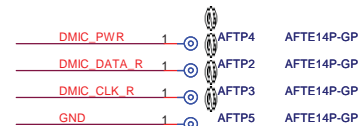
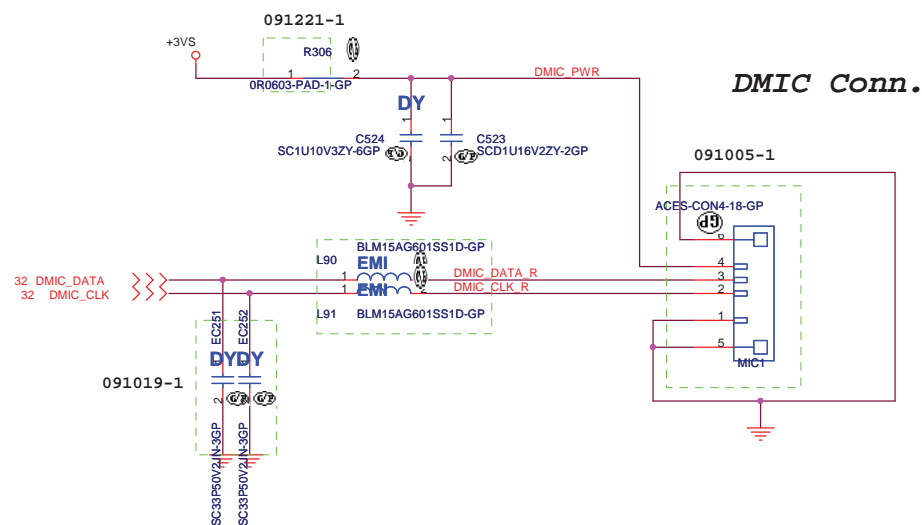
Date: Monday, March 15, 2010 Sheet 30 of 57



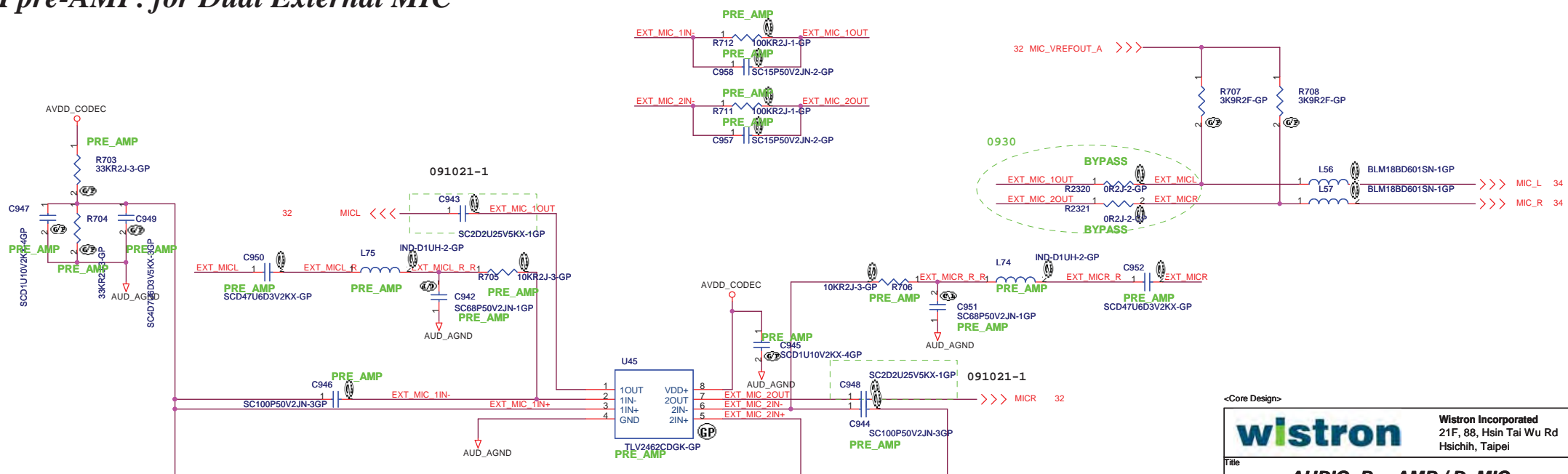
Touch_Pad CONN.
091015-1

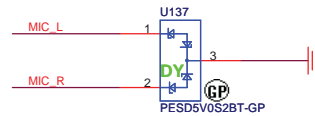


[illegible]

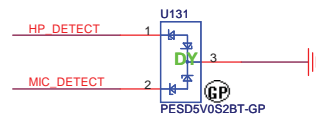
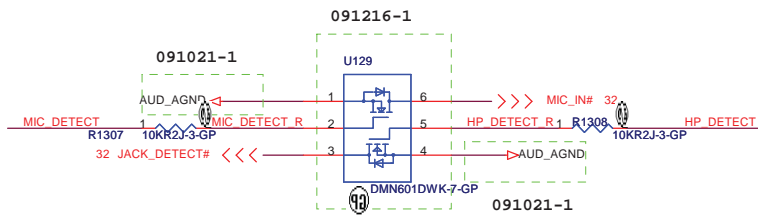
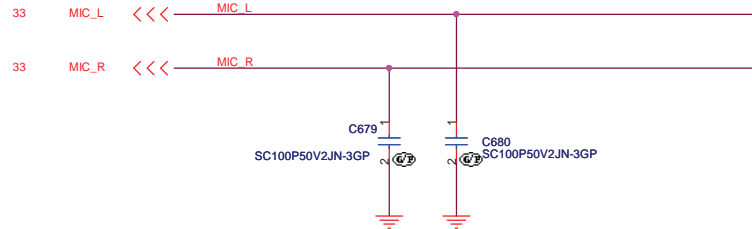


Ppre-AMP. for Dual External MIC

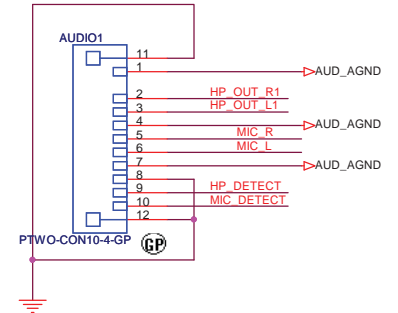




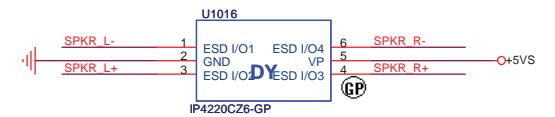
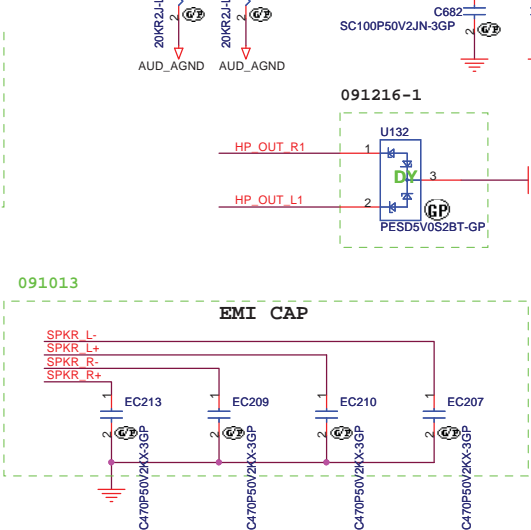
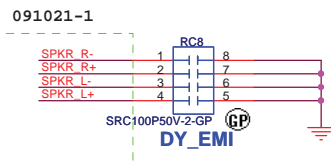
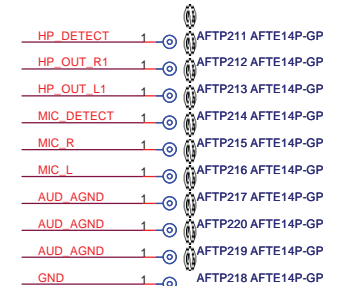
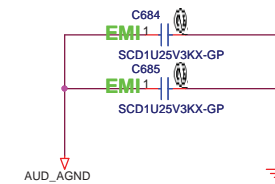
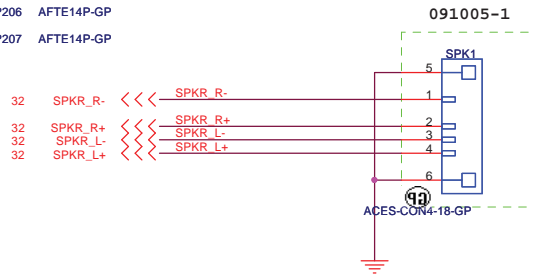
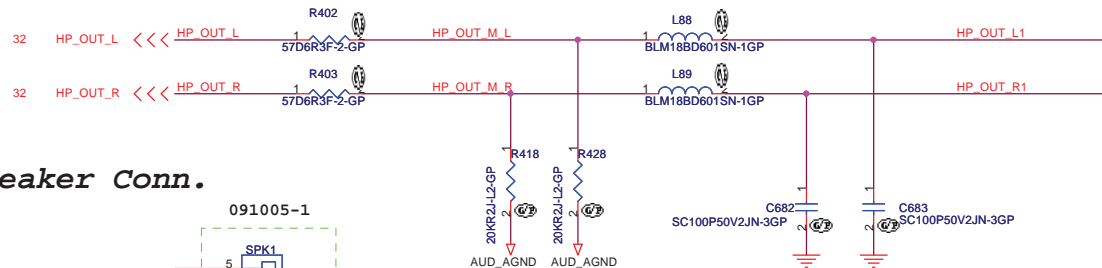
MIC IN



LINE OUT



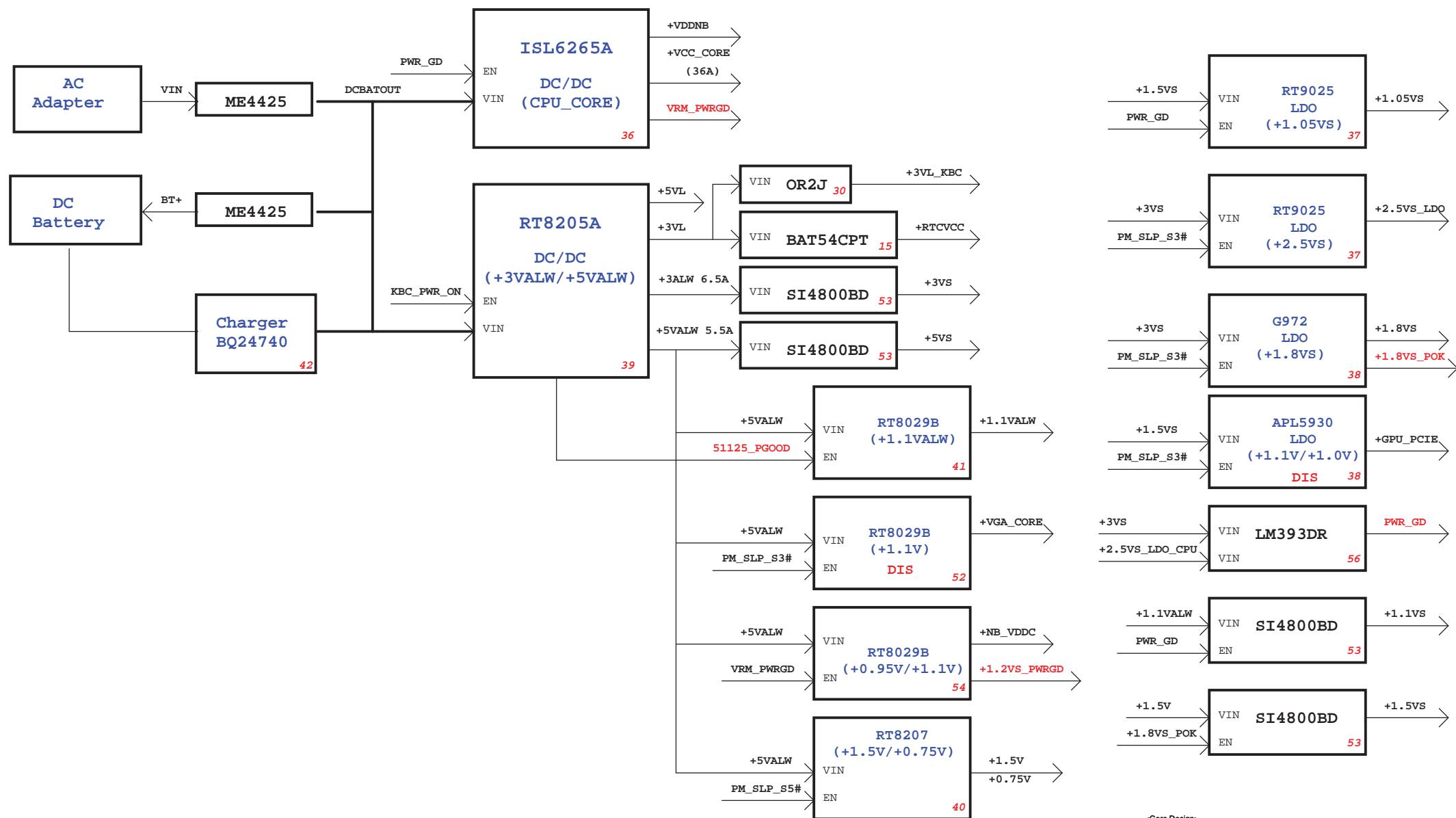
Speaker Conn.

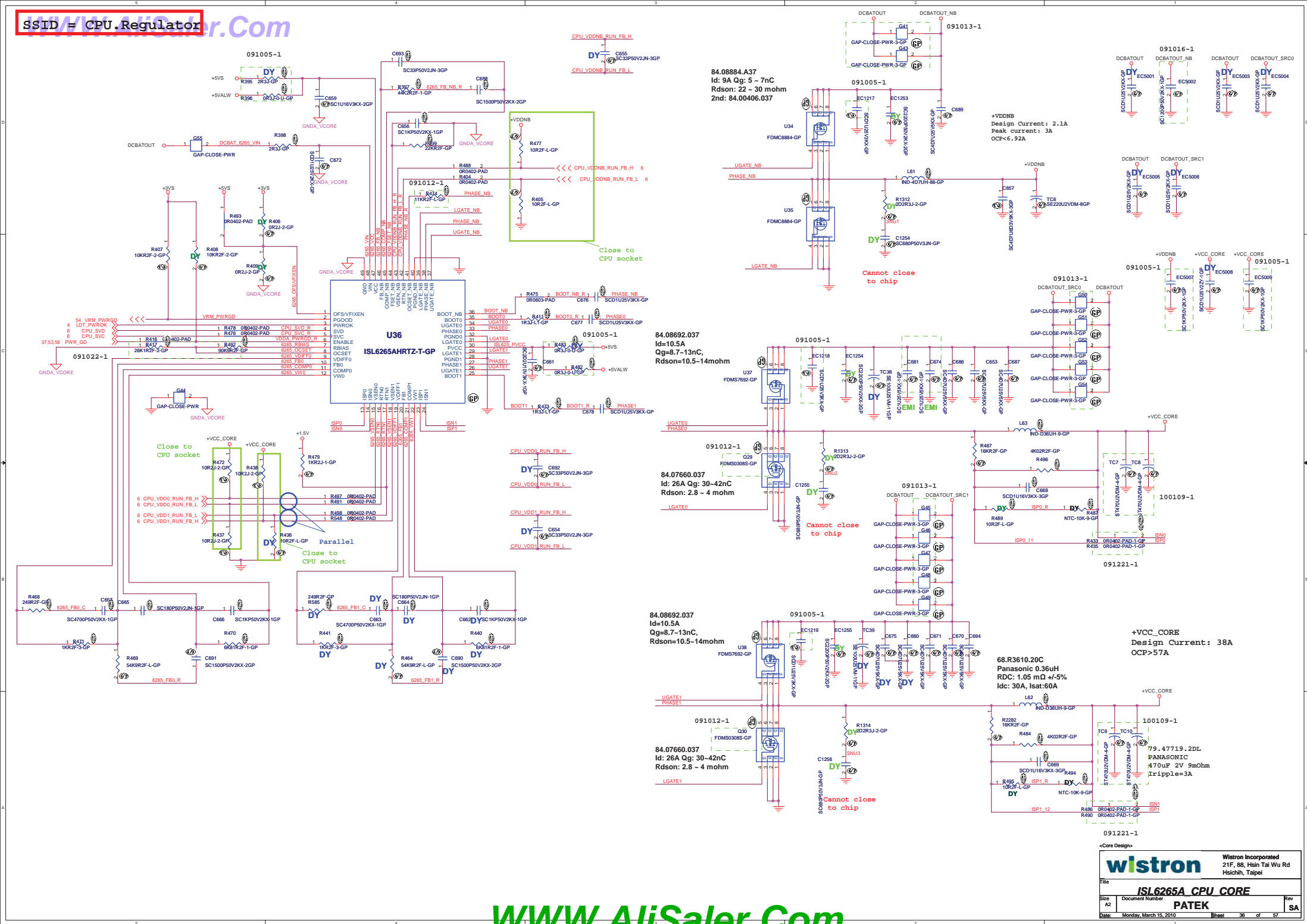


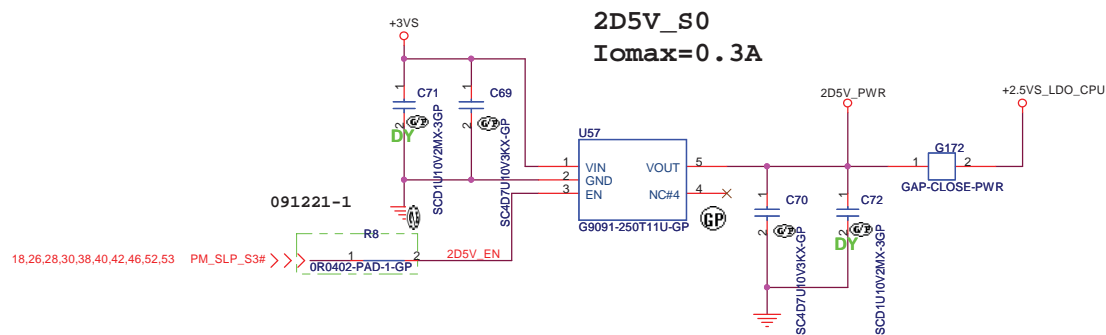
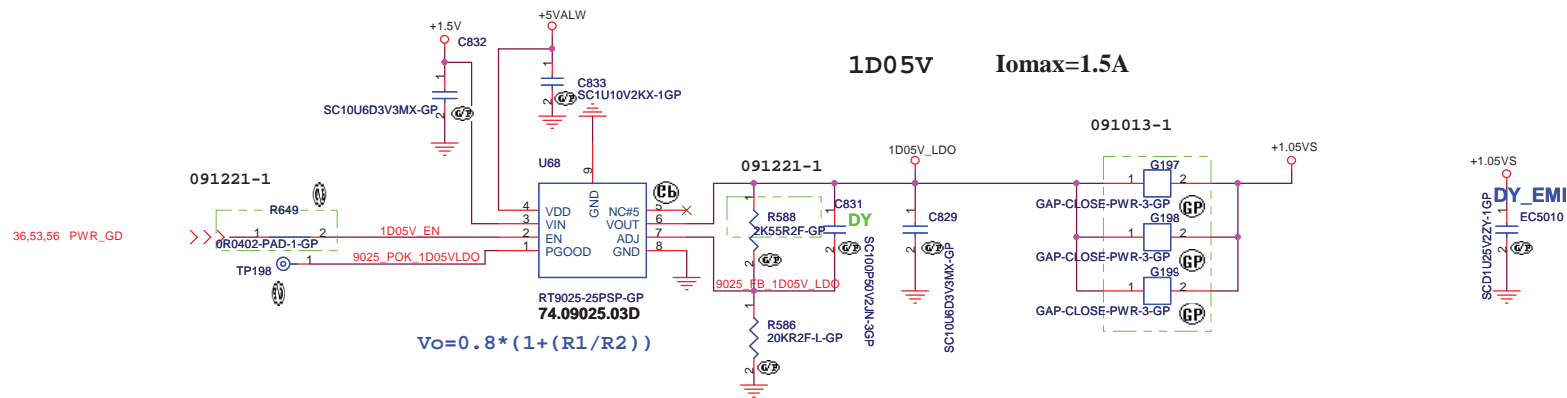
<Core Design>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title AUDIO JACK			
Size A3	Document Number PATEK		Rev SA
Date: Monday, March 15, 2010	Sheet 34	of 57	

Patek DIS POWER Block Diagram







<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

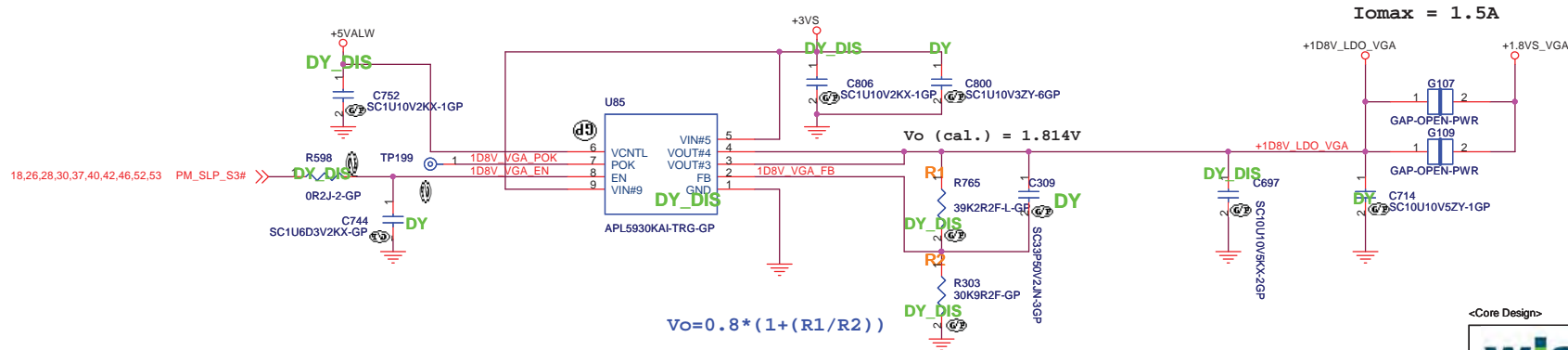
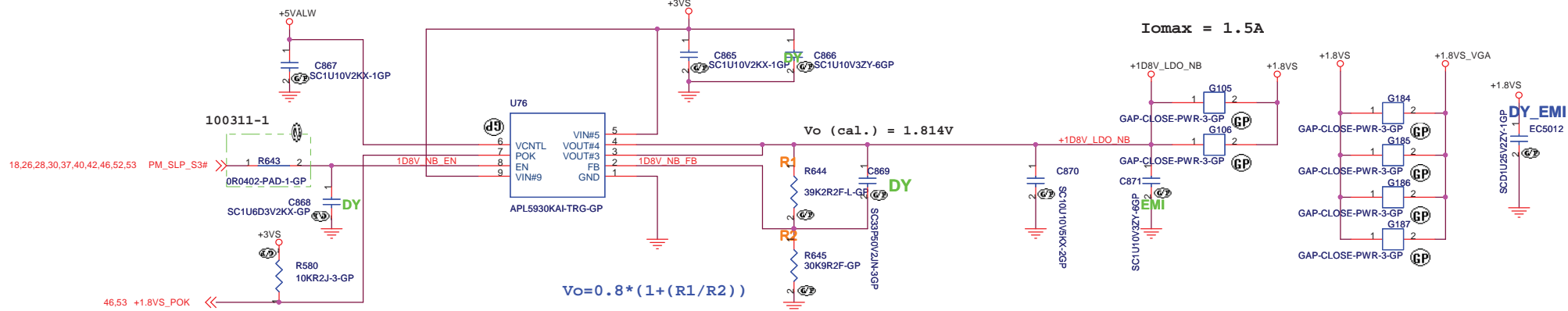
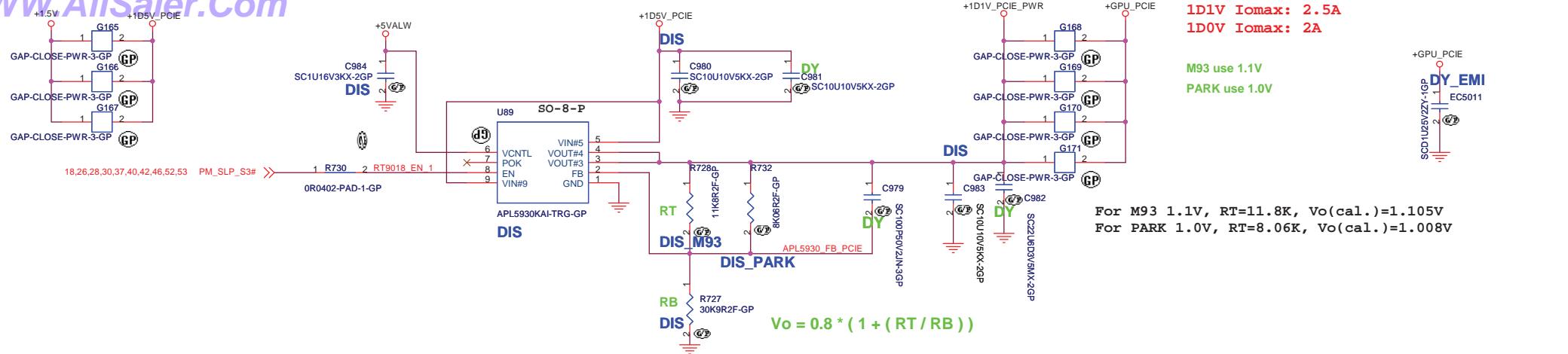
Title
RT8209B +1.05VS / +2.5VS

Size A3 Document Number
PATEK

Date: Monday, March 15, 2010

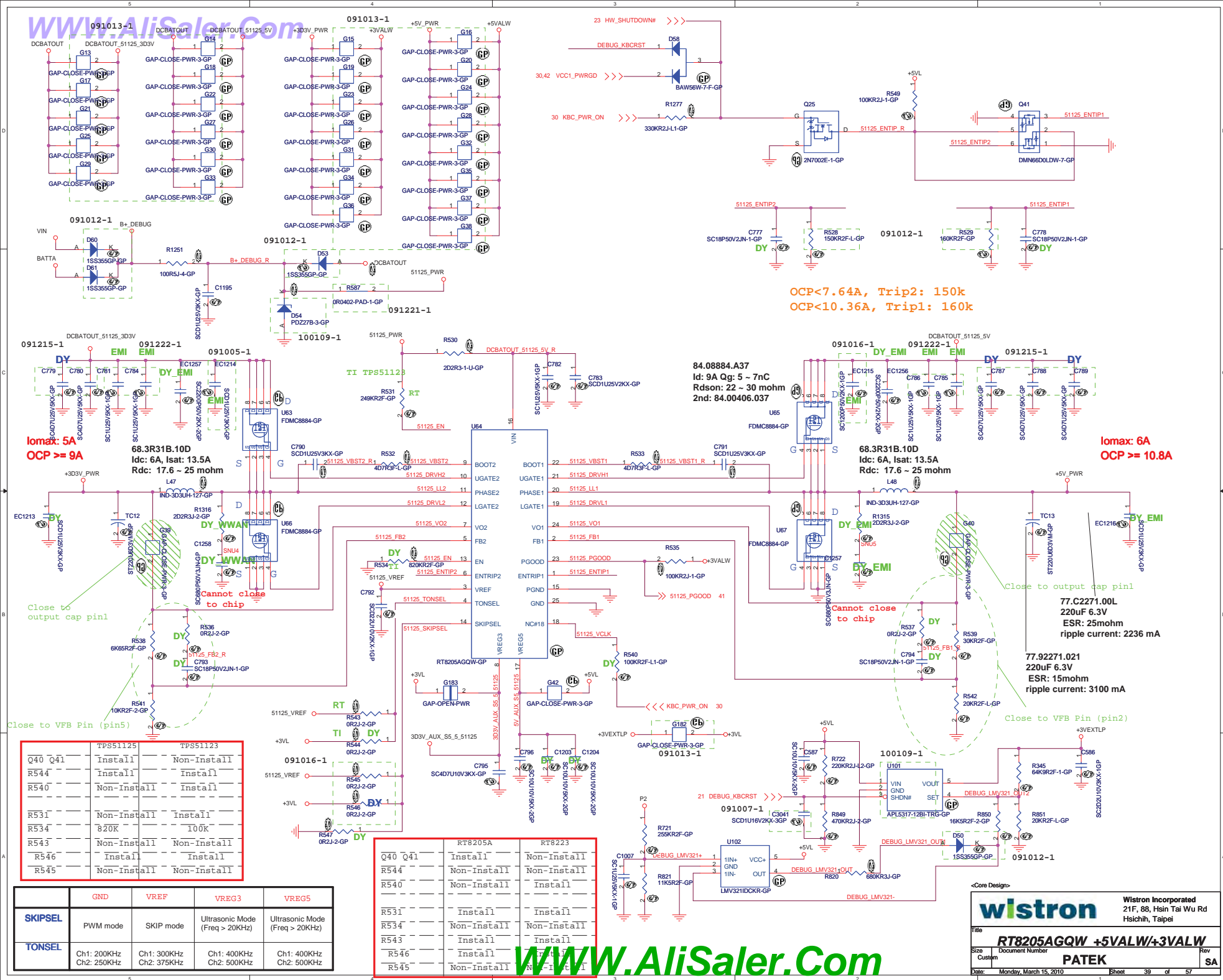
Sheet 37 of 57

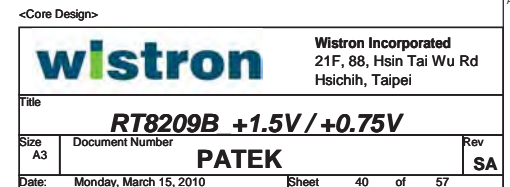
Rev
SA



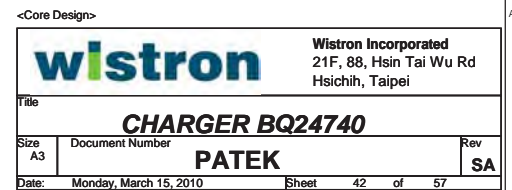
<Core Design>

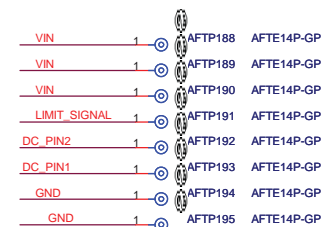
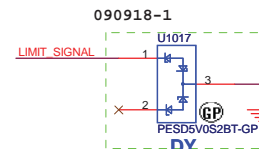
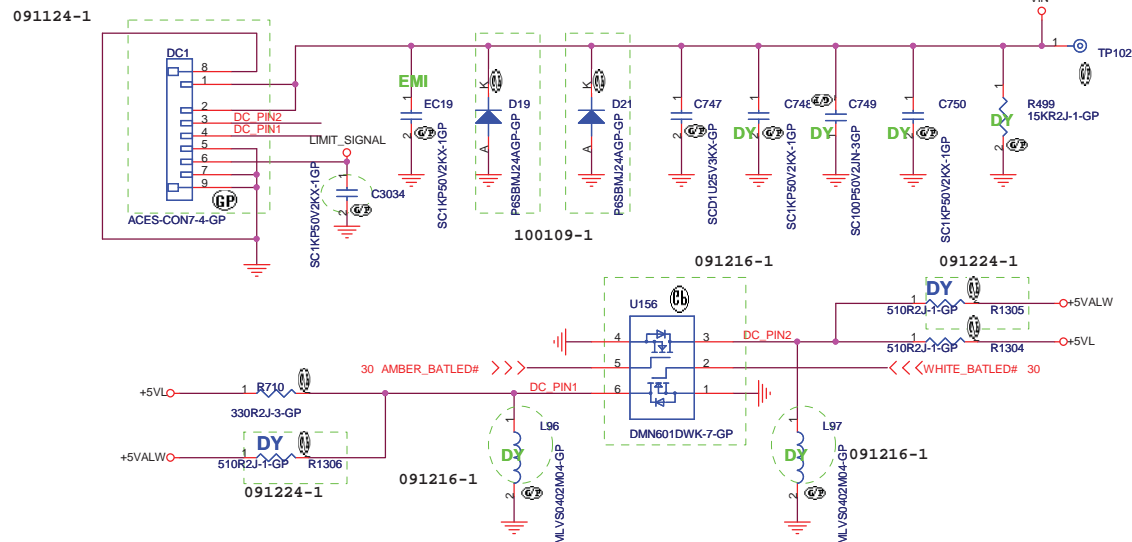
		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		G972 +1.8VS / PARK +1.0VS	
Size	Document Number	PATEK	Rev
A3			SA
Date:	Monday, March 15, 2010	Sheet	38 of 57





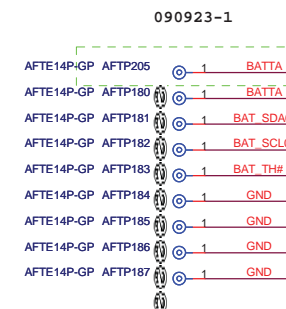
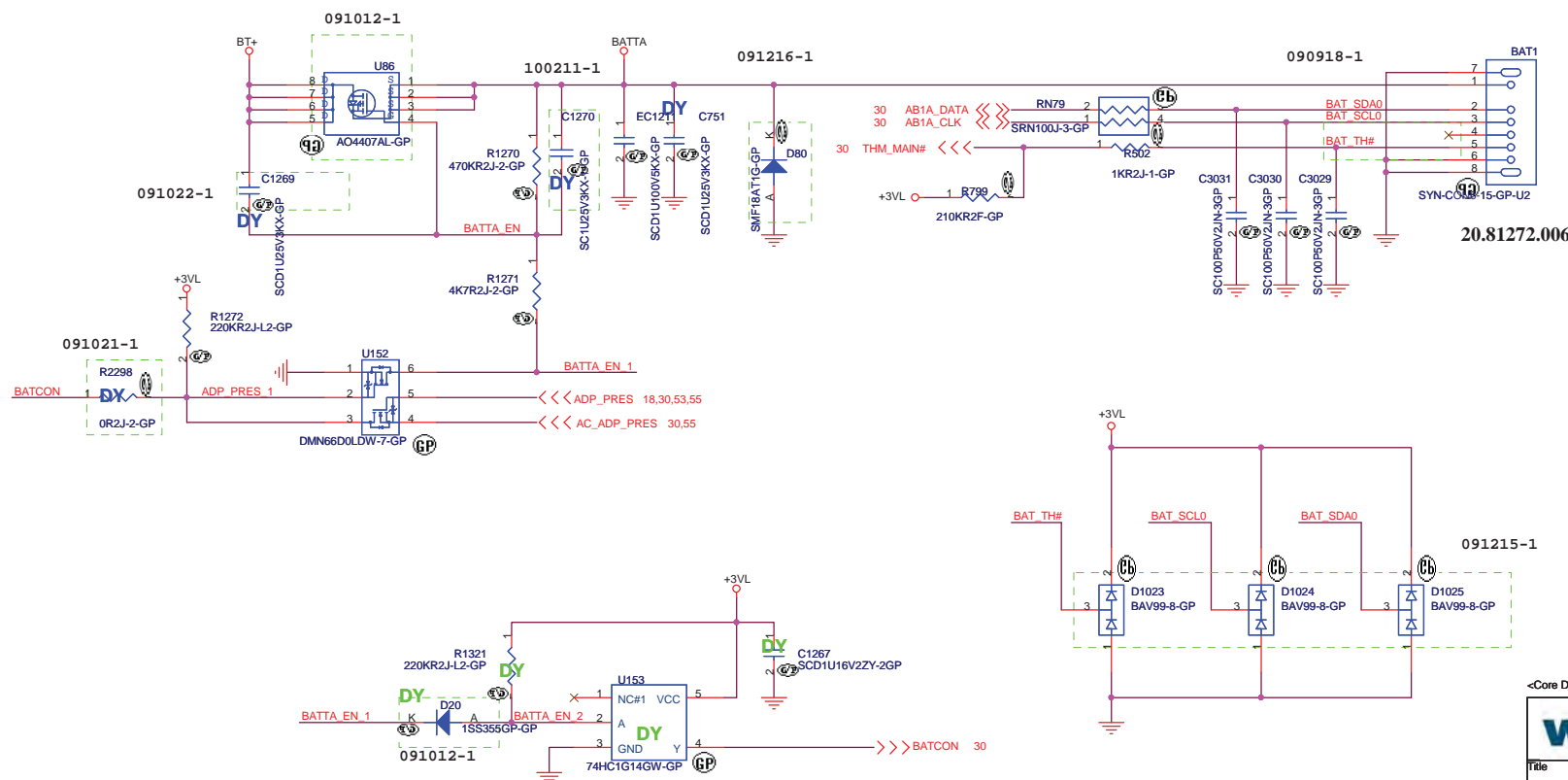






White LED:
PIN1 (-)
PIN2 (+)
Amber LED:
PIN1 (+)
PIN2 (-)

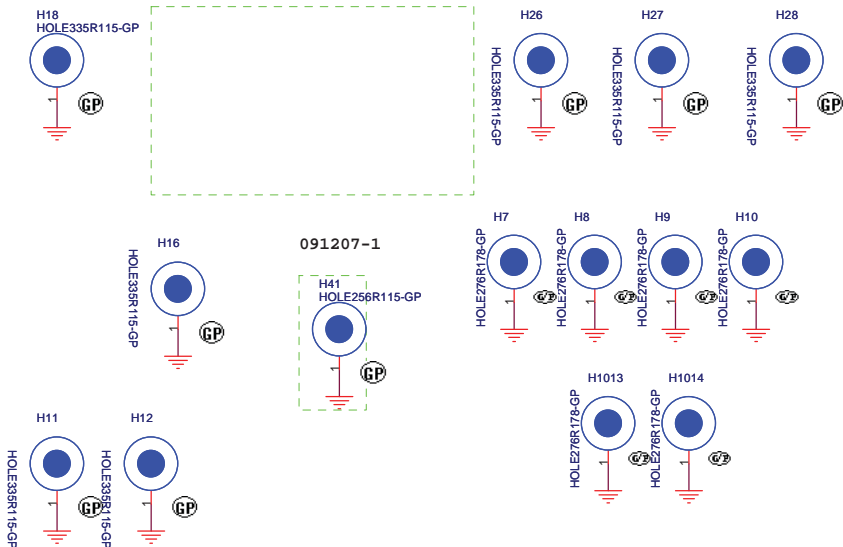
BATTERY CONNECTOR



<Core Design>

HOLE

091016-1



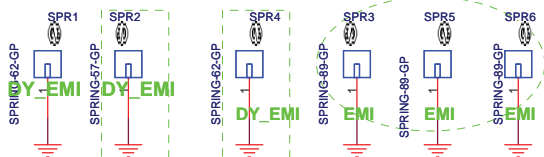
091207-1

Spring

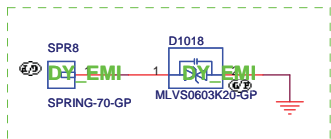
091107-1

091208-1

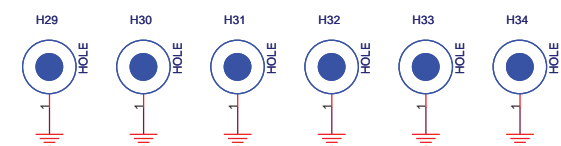
091016-1



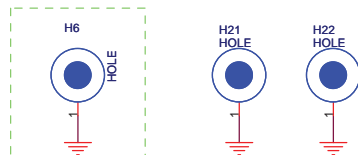
091109-1



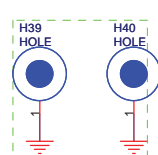
Ground PAD



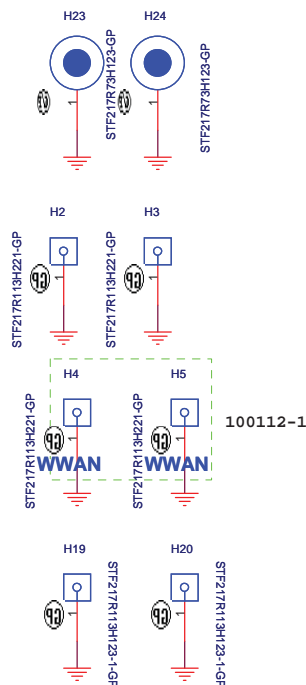
091016-1



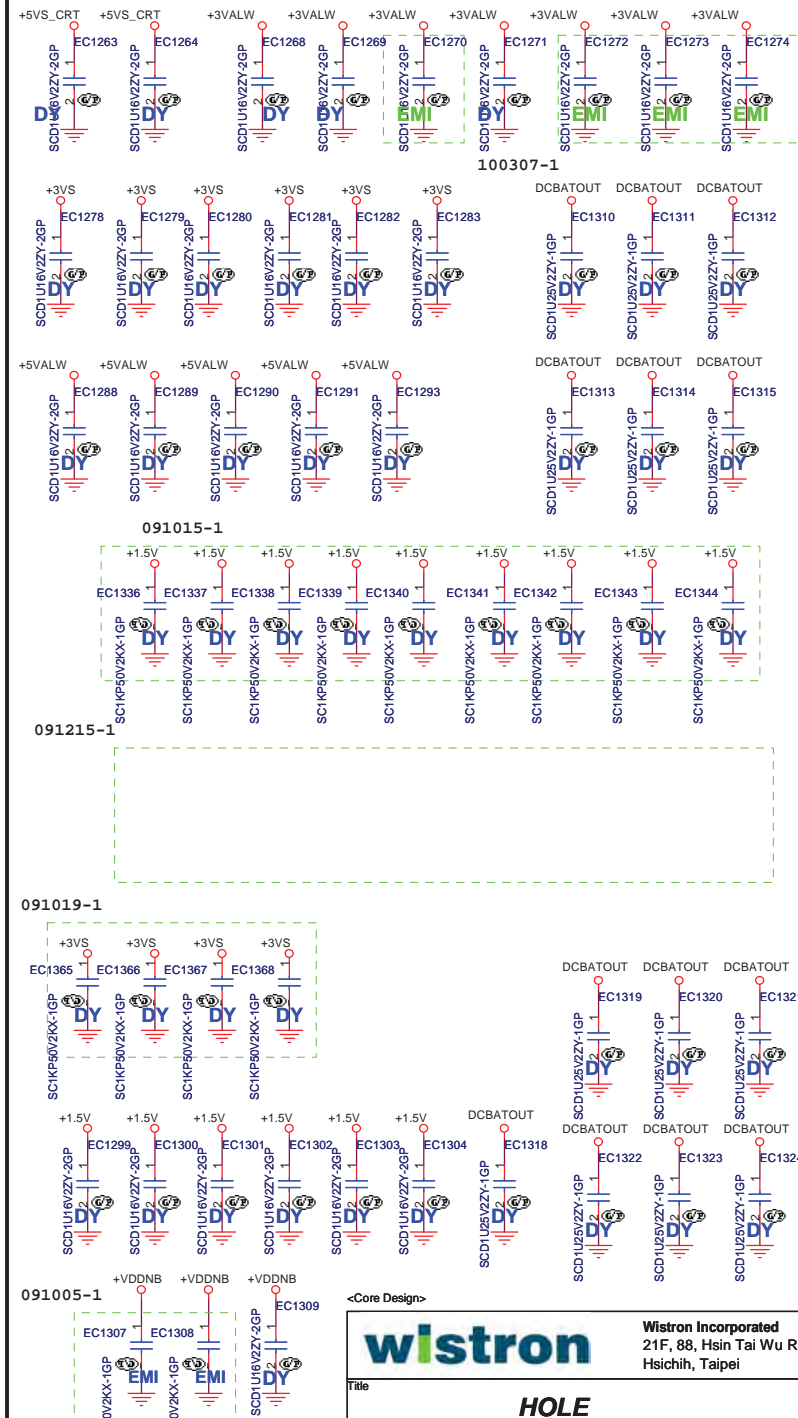
091022-1



StandOff

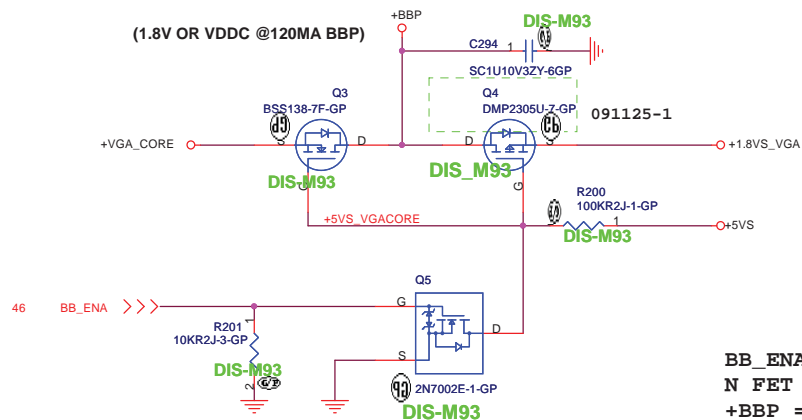
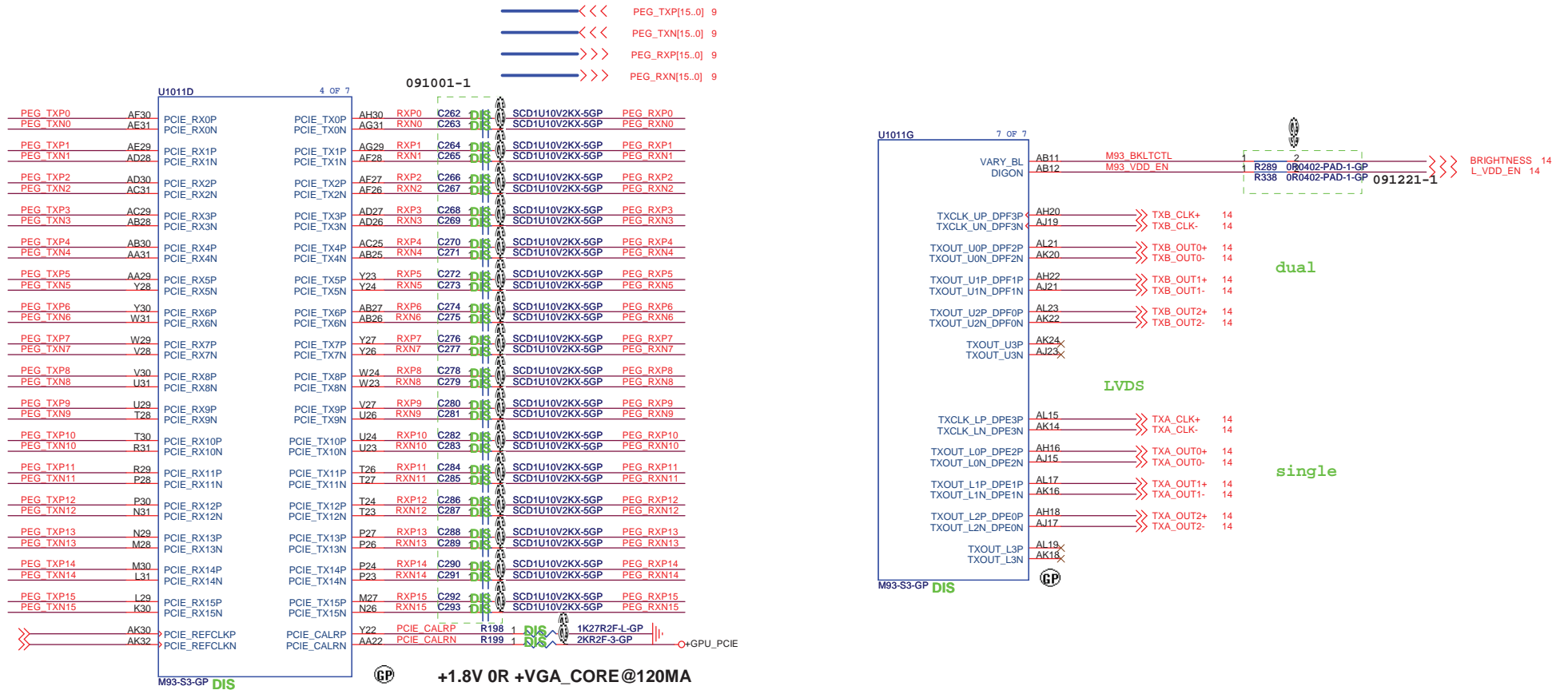


EMI CAP



wistron			Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: HOLE				
Size: A3	Document Number: PATEK			Rev: SA
Date: Monday, March 15, 2010	Sheet: 44	of 57		

M93 GPU(1/5)



BB_ENA = 0V FOR BACK BIASING DISABLED
N FET Q5 = OFF, P FET Q4 = OFF, N FET Q3 = ON
+BBP = VDD_CORE

BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET Q5 = ON, P FET Q4 = ON, N FET Q3 = OFF
+BBP = +1.8V

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

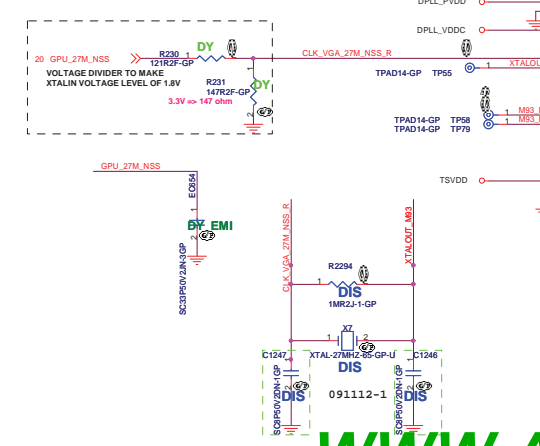
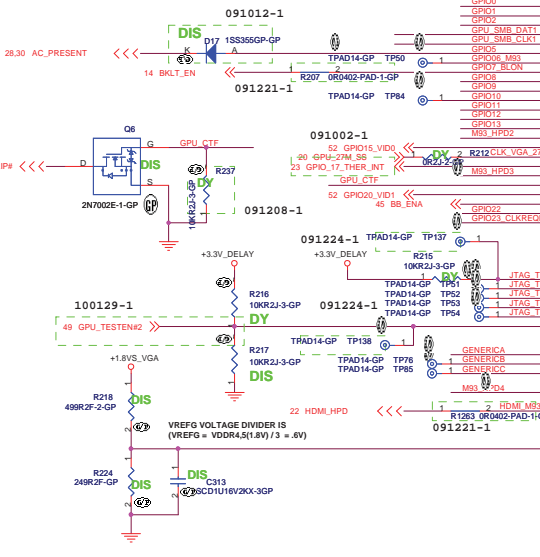
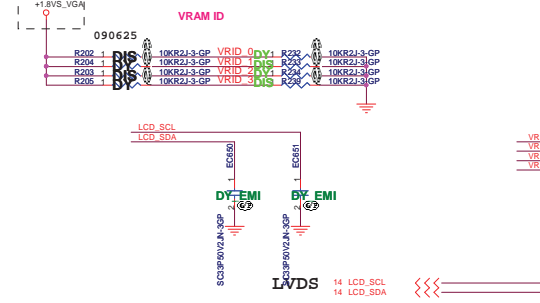
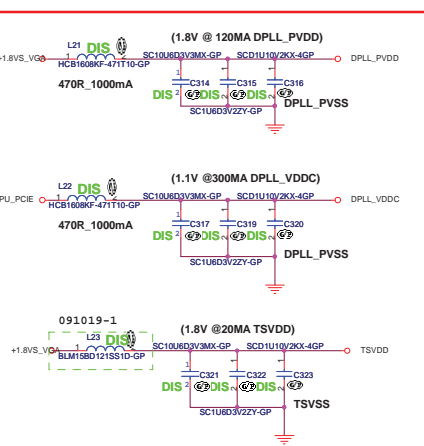
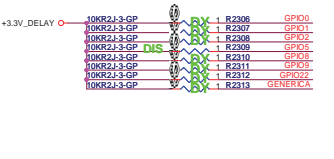
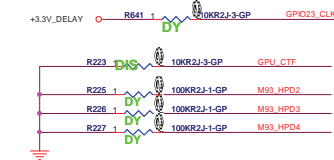
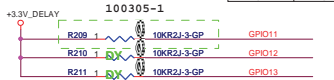
Title			
VGA-PCIE/LVDS(1/5)			
Size	Document Number	Rev	
A3	PATEK	SA	
Date:	Monday, March 15, 2010	Sheet	45 of 57

CONFIGURATION STRAPS			
ALLOW FOR PULLUP/PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	PCI FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS ENABLED	X
BF_GEN2_EN_A	GPIO2	PCI GEN2 ENABLED	X
RSVD	GPIO8	VGA ENABLED	0
BF_VGA_DIS	GPIO9	PCI GEN2 ENABLED	0
RSVD	GPIO21	VGA ENABLED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM ID CFG(2)	GPIO(13:1)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V25VNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC	AUD[1] AUD[0]	0
AUD[1]	HSYNC	0:0 No audio function	0
AUD[0]	VSNC	0:1 Audio for DisplayPort and HDMI if dongle is detected	XX
		1:0 Audio for DisplayPort only	
		1:1 Audio for both DisplayPort and HDMI	

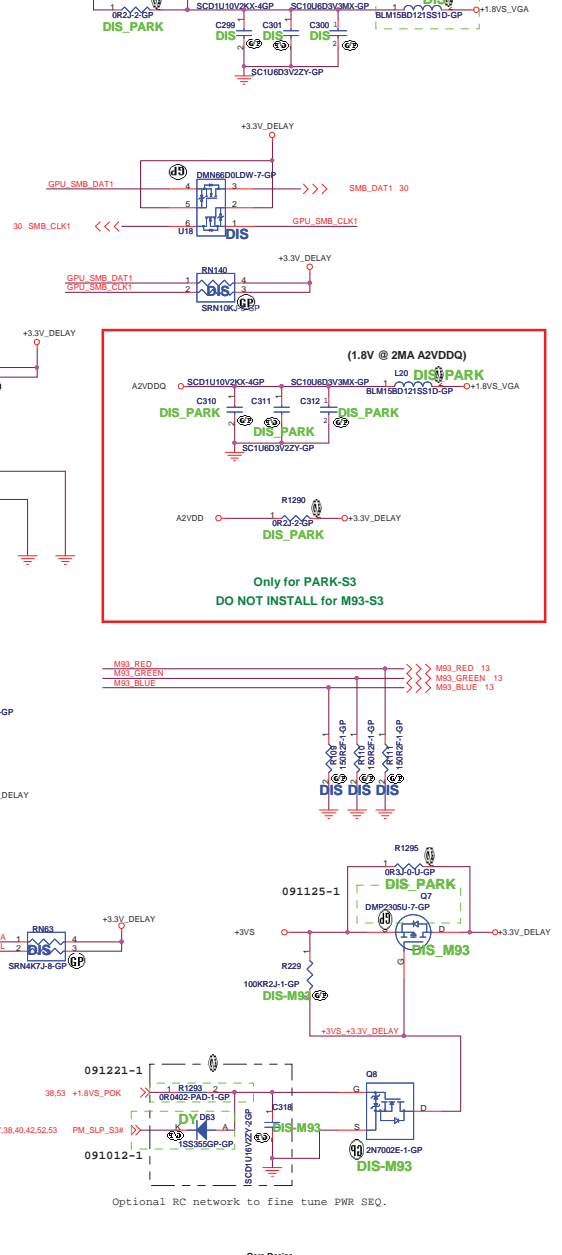
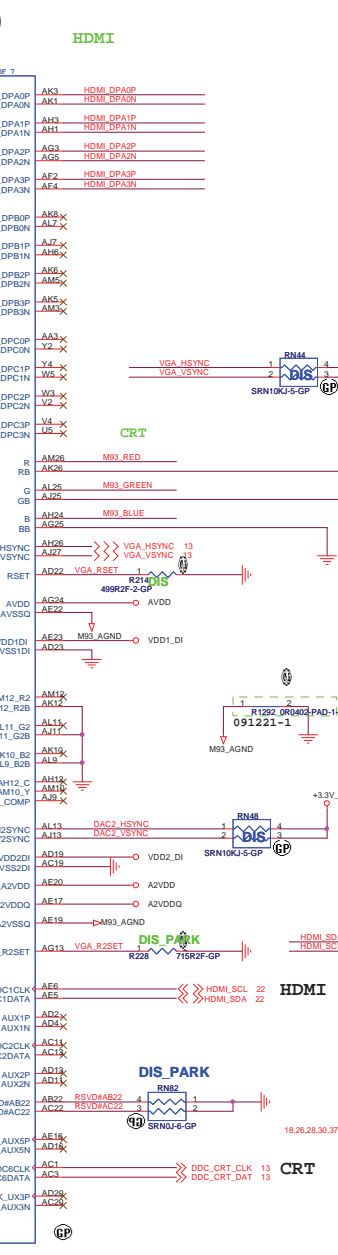
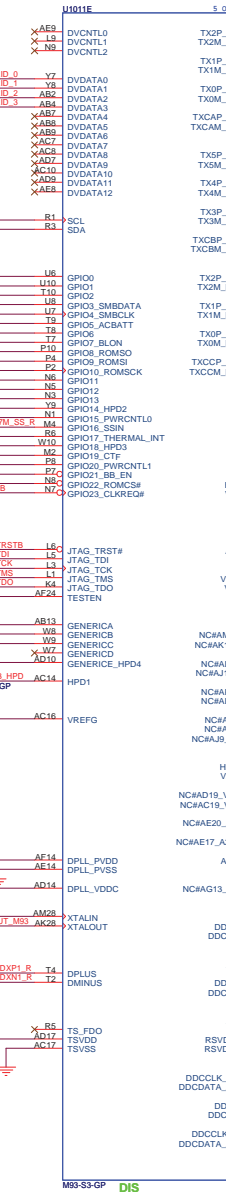
Aperture Config.	M93S3	Strapping Resistor	64MB	128MB	256MB
CONFIG0	GPIO_11	R209	0	0	1
CONFIG1	GPIO_12	R210	1	0	0
CONFIG2	GPIO_13	R211	0	0	0

M93 LP: VDDC=0.9/1.1V

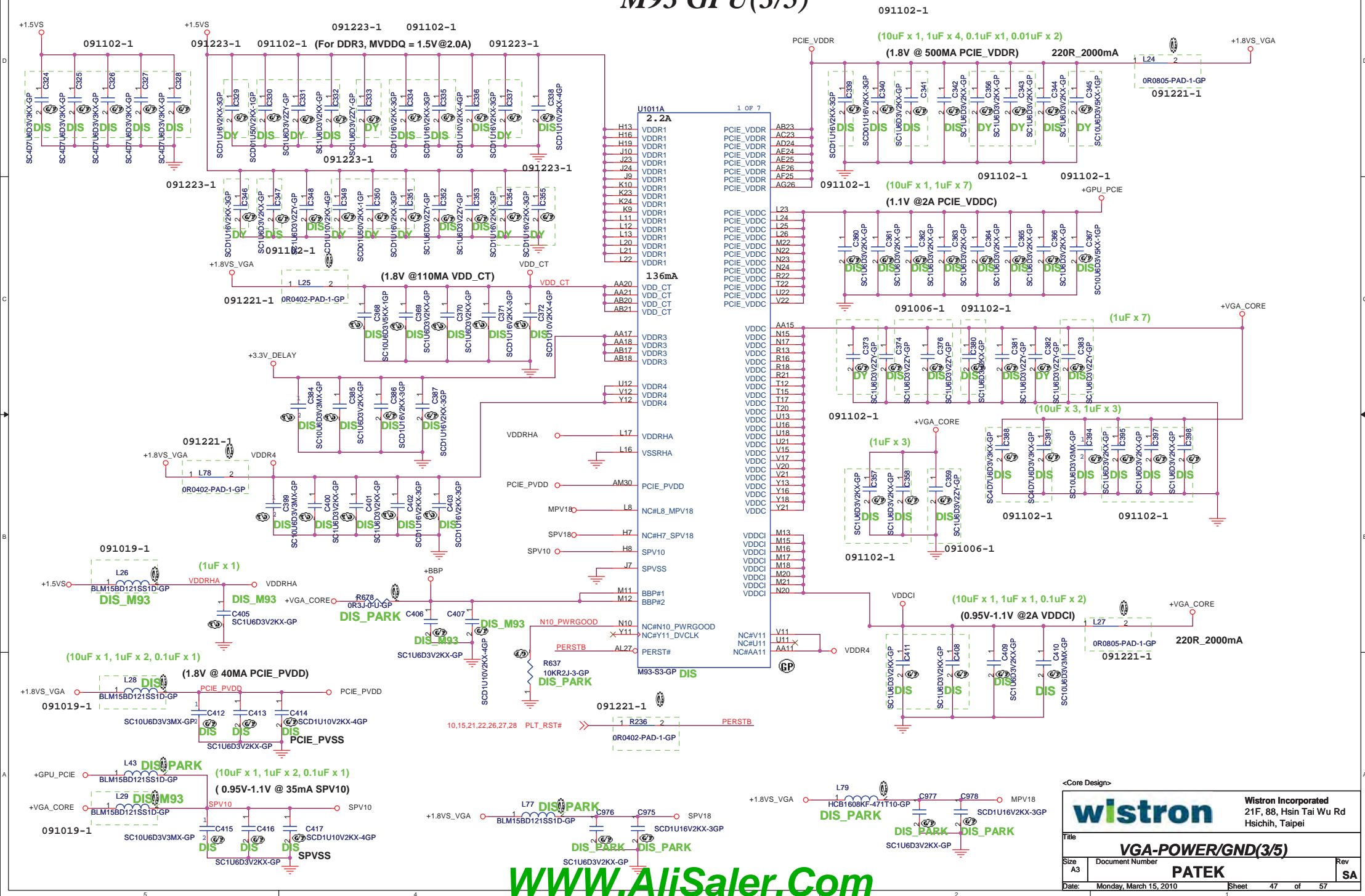
VDD1	VDD0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V



M93 GPU(2/5)

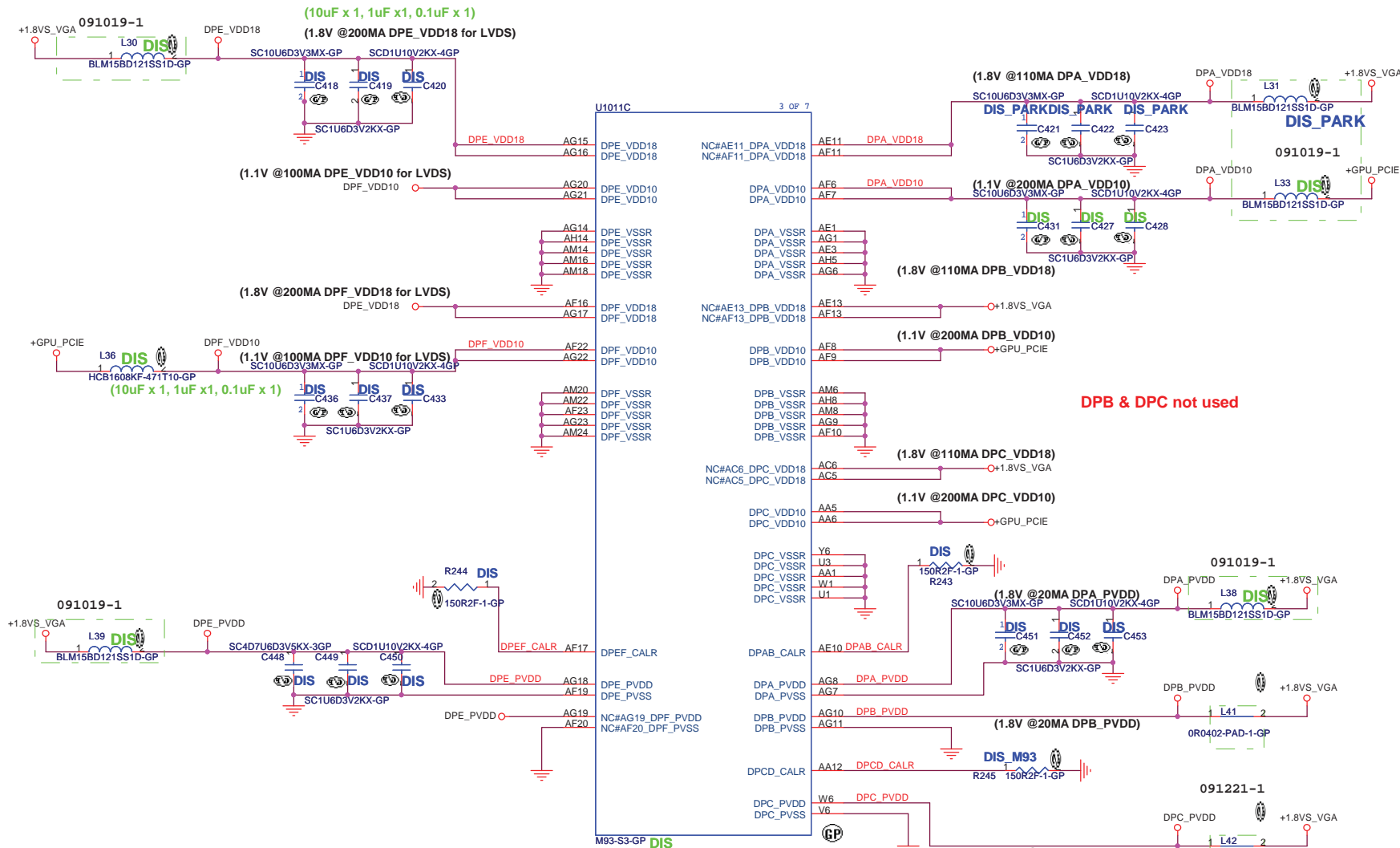


M93 GPU(3/5)



M93 GPU(4/5)

When space is not enough
Consider that use one bead to share



NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEADfor one rail of each pair if signal integrity for DP lanes are OK.
We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove DecouplingCapacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need at least 500mA Bead to support join rails.

DPB & DPC not used

<Core Design>



Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

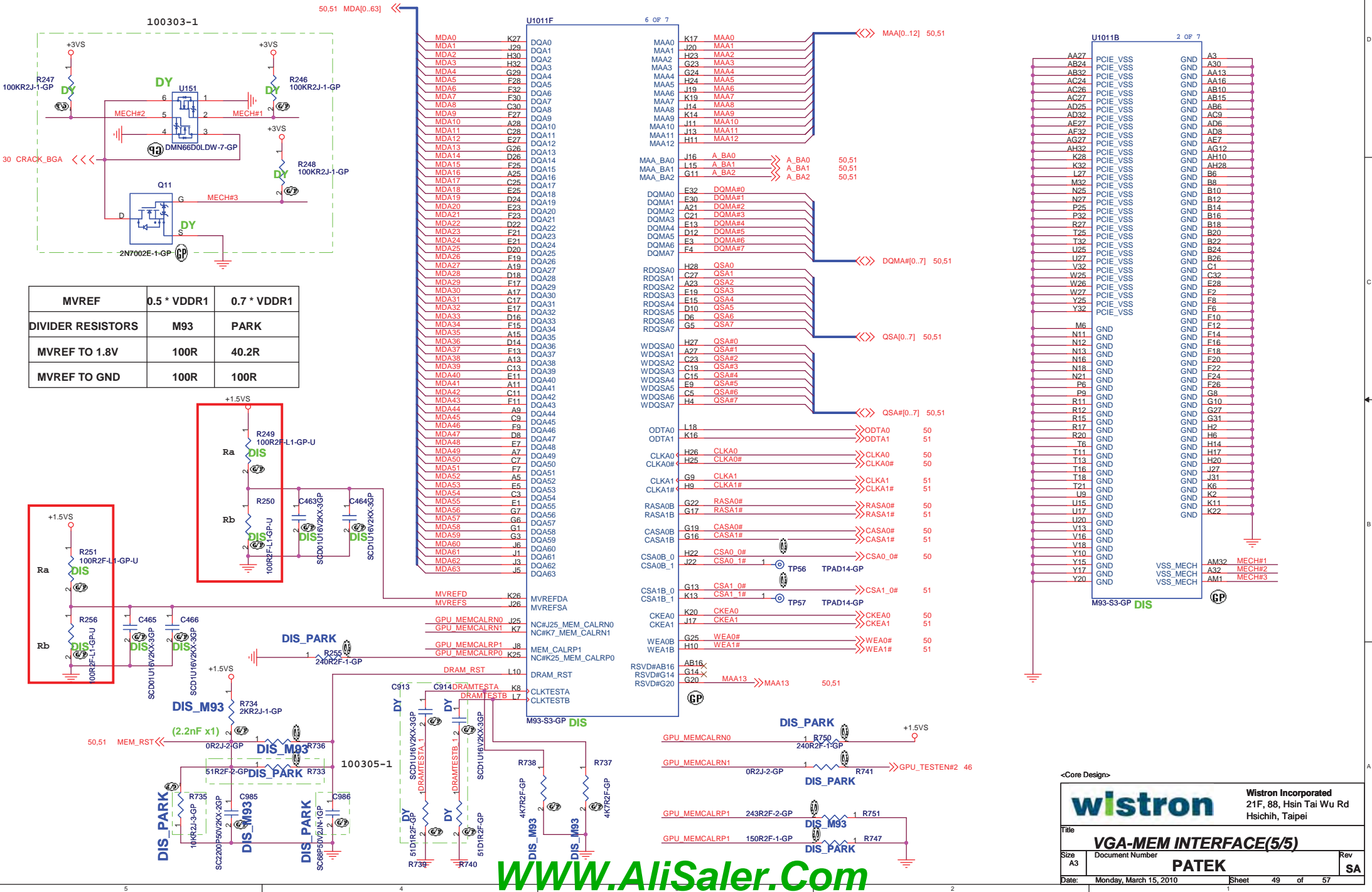
Title	VGA-POWER/GND(4/5)
-------	---------------------------

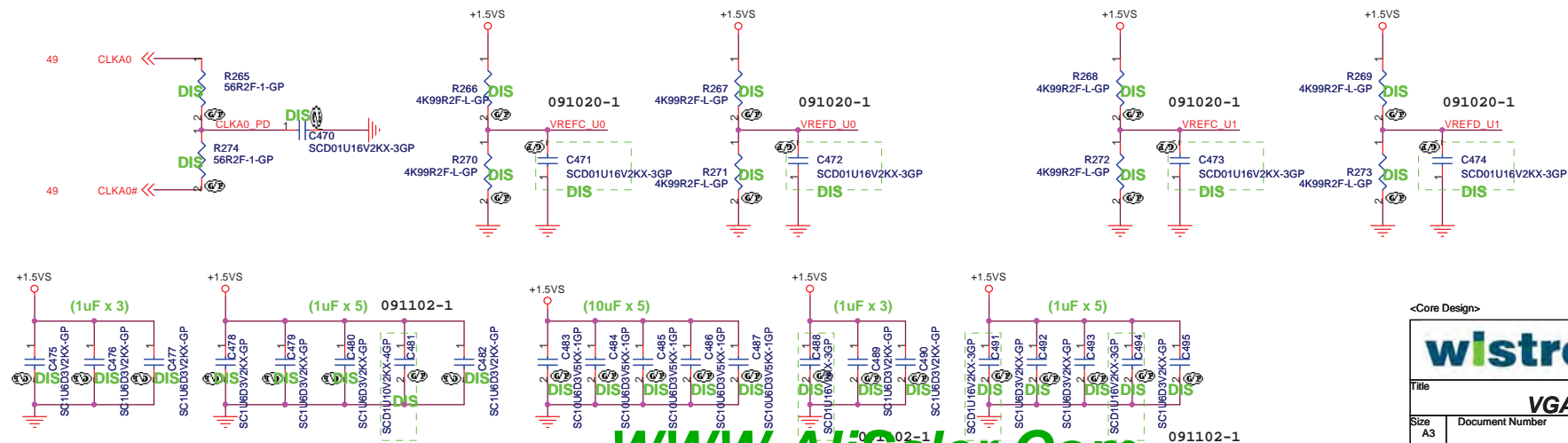
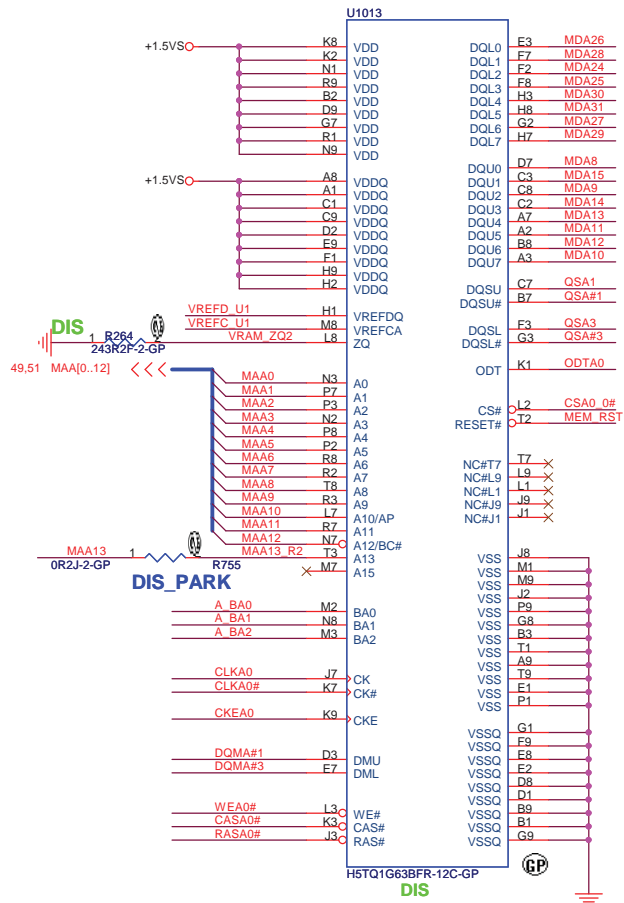
Size A3	Document Number PATEK
------------	---------------------------------

Rev	
SA	

Date: Monday, March 15, 2010 Sheet 48 of 57

GPU(5/5)





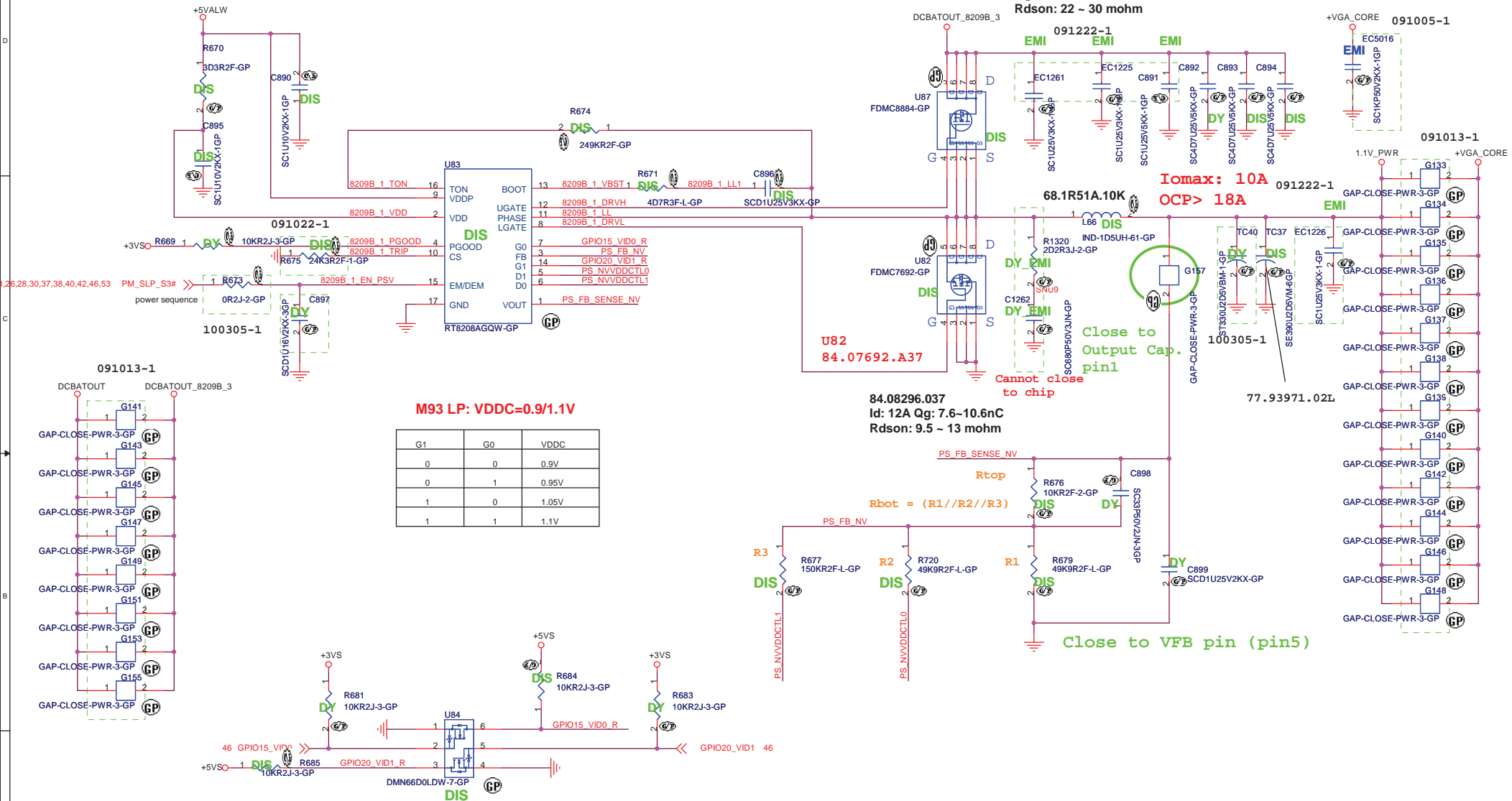


Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

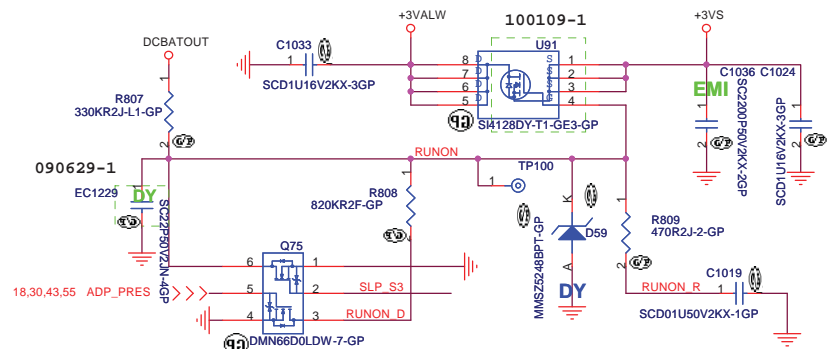
Title			
VGA-MEMORY			
Size	Document Number	Rev	
A3	PATEK	SA	
Date:	Monday, March 15, 2010	Sheet	51 of 57

RT8209B for +VGA_CORE

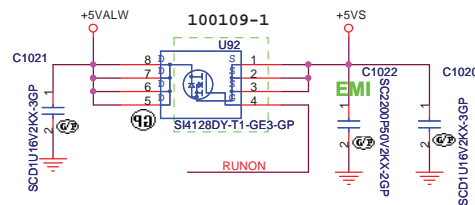
84.08884.A37
Id: 7.2A
Qg: 5 ~ 7nC
Rdson: 22 ~ 30 mohm



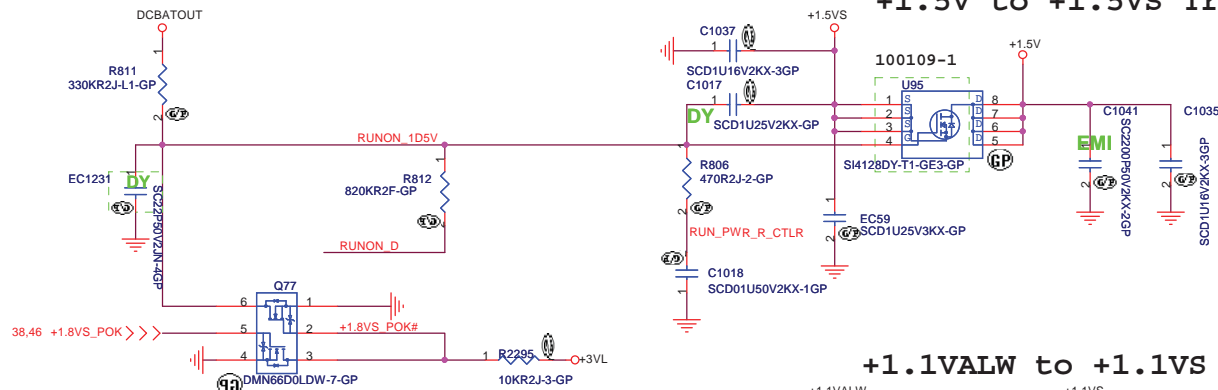
+3VALW to +3VS Transfer



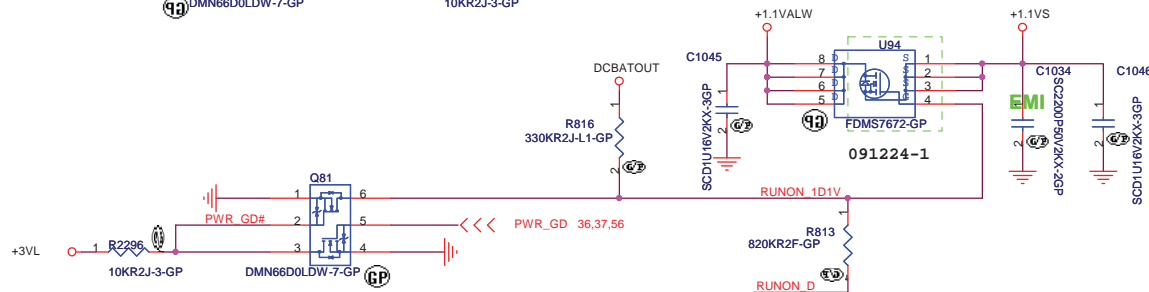
+5VALW to +5VS Transfer



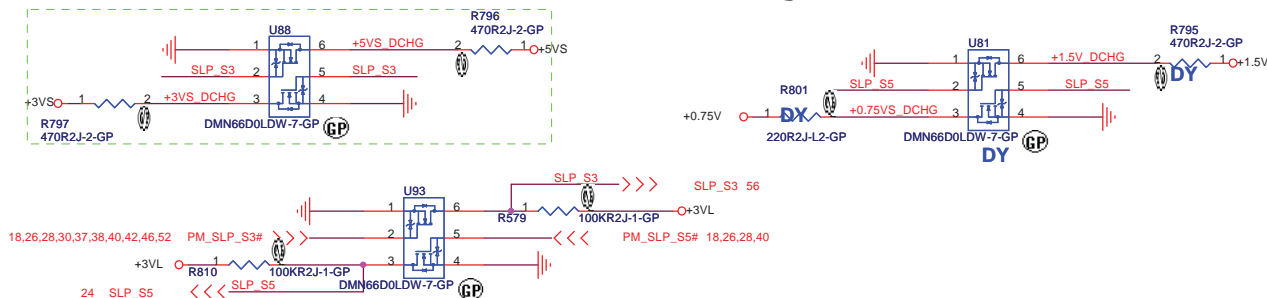
+1.5V to +1.5VS Transfer



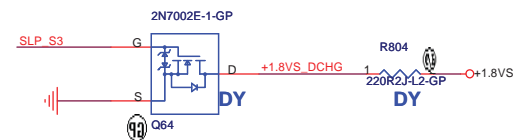
+1.1VALW to +1.1VS Transfer



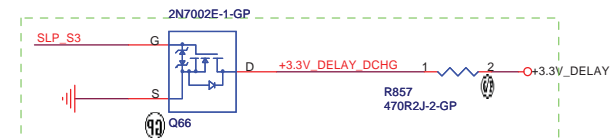
Discharge circuit-1




090724-1



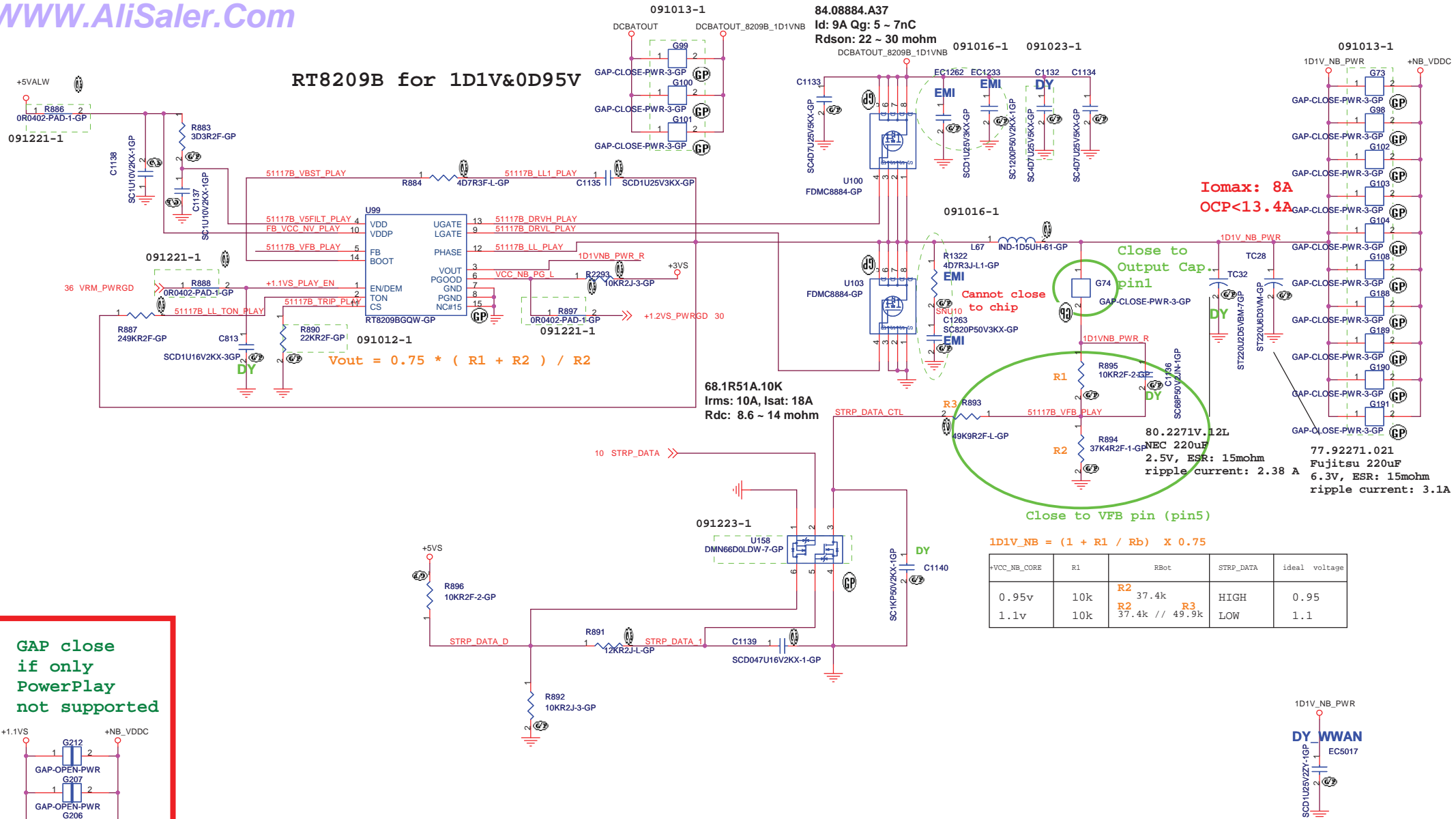
091215-2



<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
DC/DC			
Size A3	Document Number PATEK		Rev SA
Date:	Monday, March 15, 2010	Sheet 53	of 57

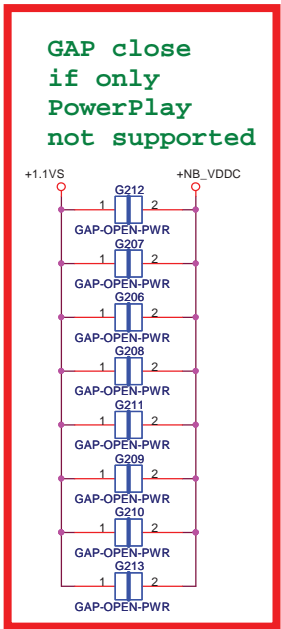
RT8209B for 1D1V&0D95V

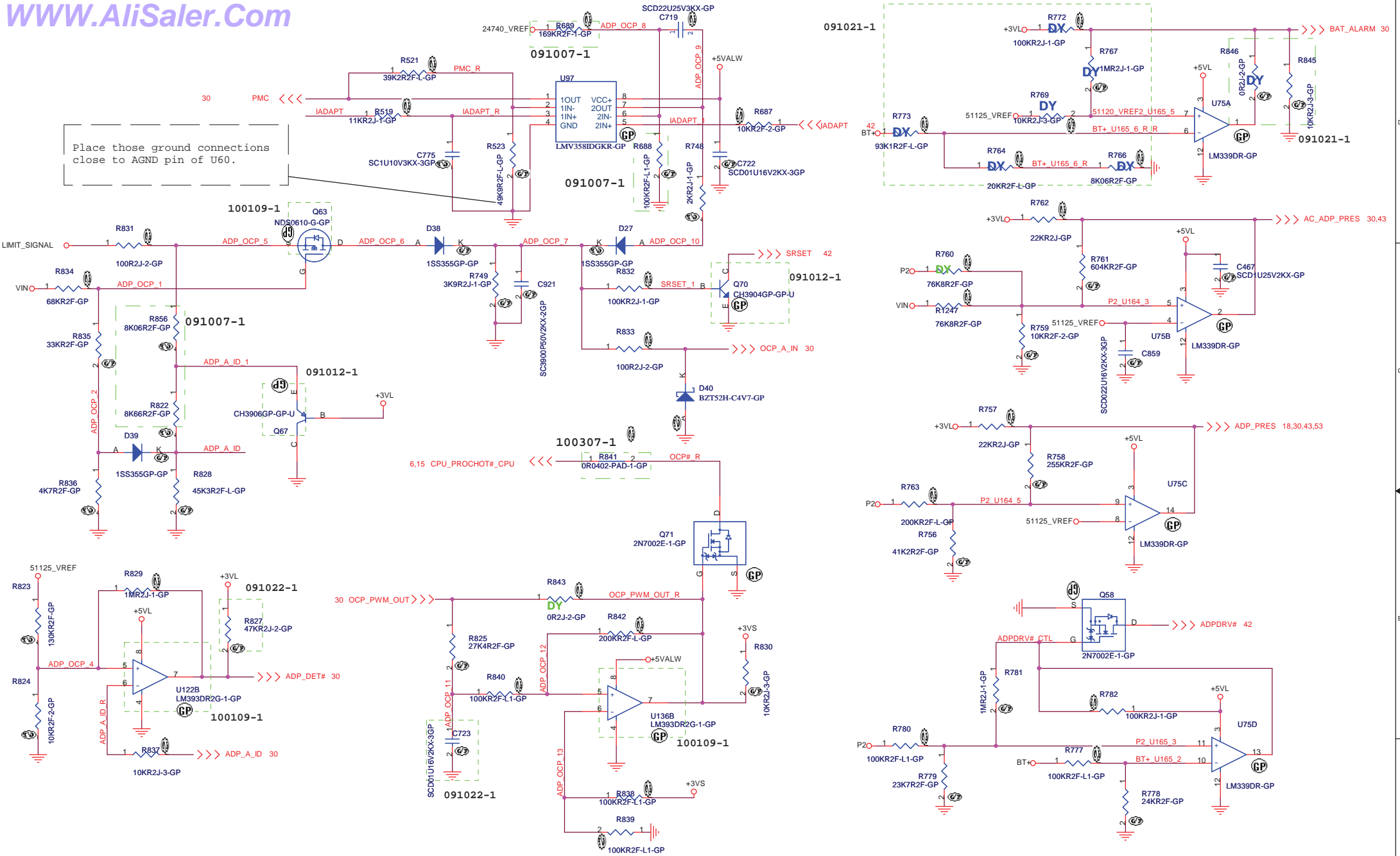


$$V_{out} = 0.75 * (R1 + R2) / R2$$

$$1D1V_NB = (1 + R1 / Rb) * 0.75$$

+VCC_NB_CORE	R1	Rb	STRP_DATA	ideal voltage
0.95v	10k	R2 37.4k	HIGH	0.95
1.1v	10k	R2 37.4k // R3 49.9k	LOW	1.1





NOTE:


When AC_ADAP_PRES=0 --> 1
 $V_{in} = (R_{759} / R_{761}) / [(R_{759} / R_{761}) + R_{1247}] \times 51125_VREF$
 $V_{in} = 17.6145V$

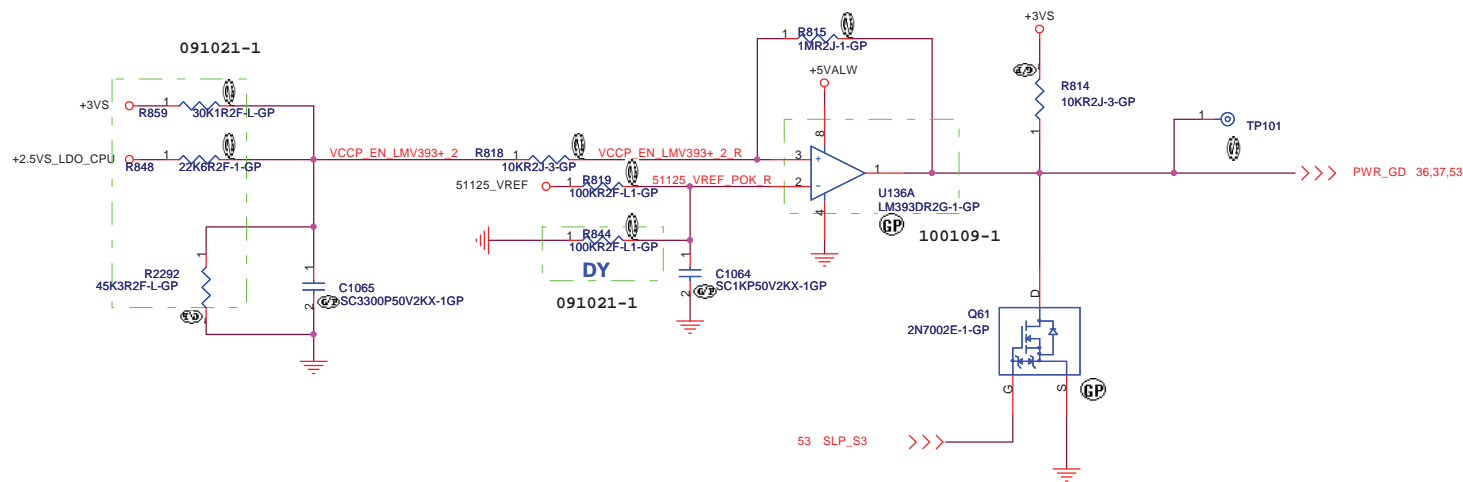
When AC_ADAP_PRES=1 --> 0
 $[(V_{in} - 51125_VREF) / R_{1247}] + [(+3VL - 51125_VREF) / (R_{761} + R_{762})] = 51125_VREF / R_{759}$
 $V_{in} = 17.212554V$

When ADP_PRES=0->1
 $P2 \times (R_{756} / R_{758}) / [(R_{756} / R_{758}) + R_{763}] = 51125_VREF$
 $P2 = 13.325V$

When ADP_PRES=1->0
 $[(P2 - 51125_VREF) / R_{756}] + [(+3VL - 51125_VREF) / (R_{757} + R_{758})] = 51125_VREF / R_{756}$
 $P2 = 10.894V$

<Core Design>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
ADP OCP			
Size A3	Document Number PATEK		Rev SC
Date:	Monday, March 15, 2010	Sheet	55 of 57



<Core Design>

wistron		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title POK CKT			
Size A3	Document Number PATEK		Rev SA
Date:	Monday, March 15, 2010	Sheet 56 of 57	

