

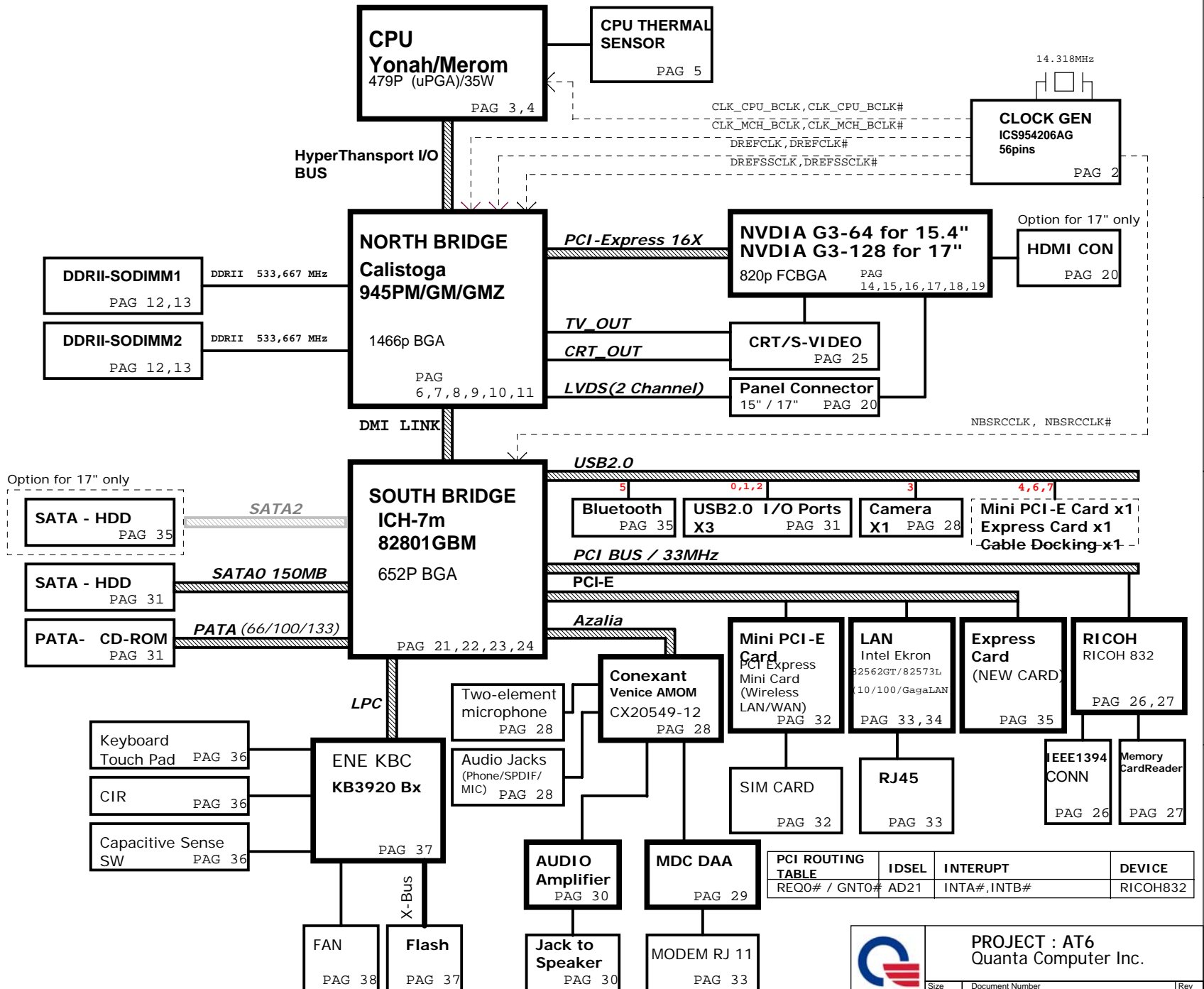
AT6 BLOCK DIAGRAM

PCB STACK UP

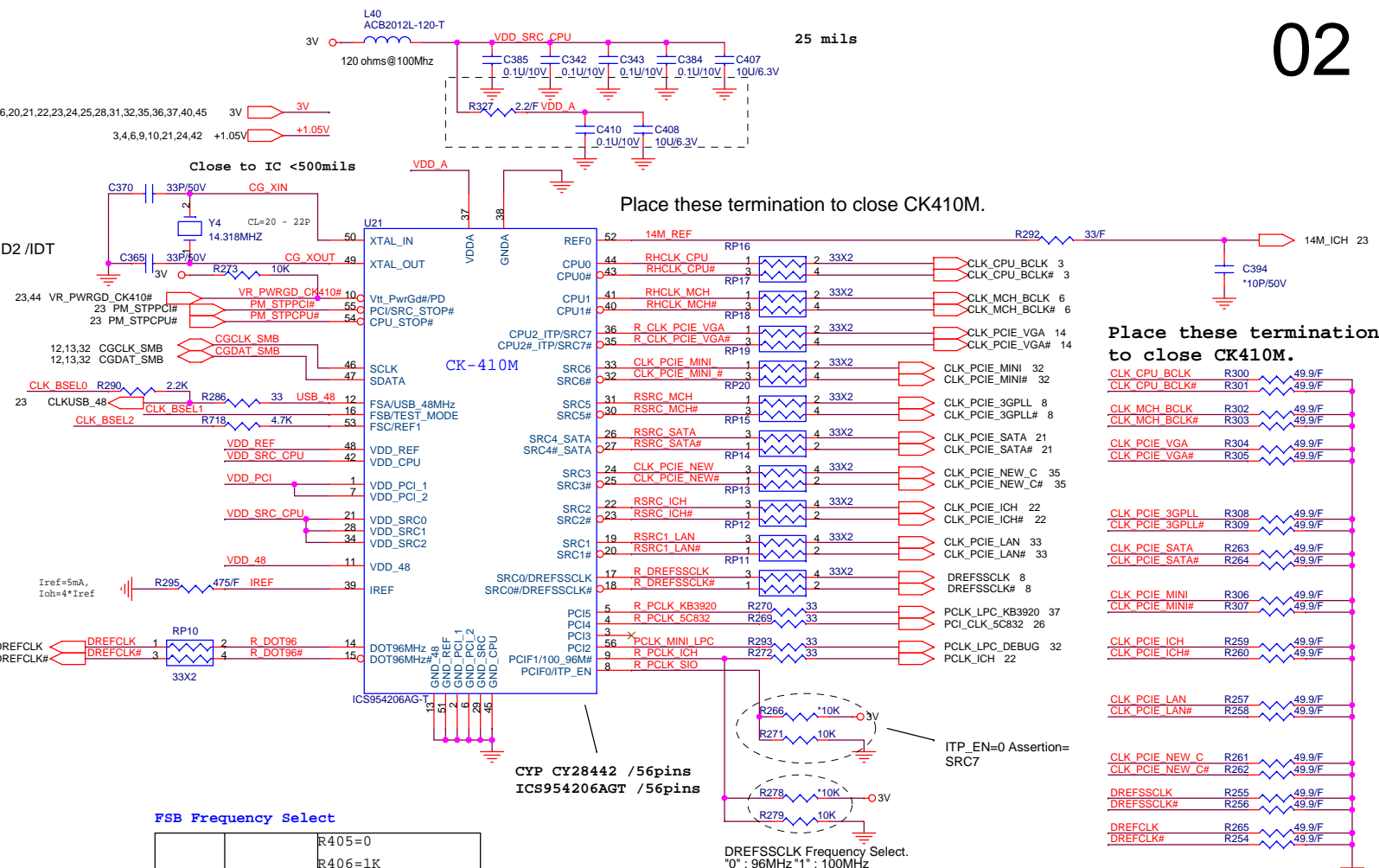
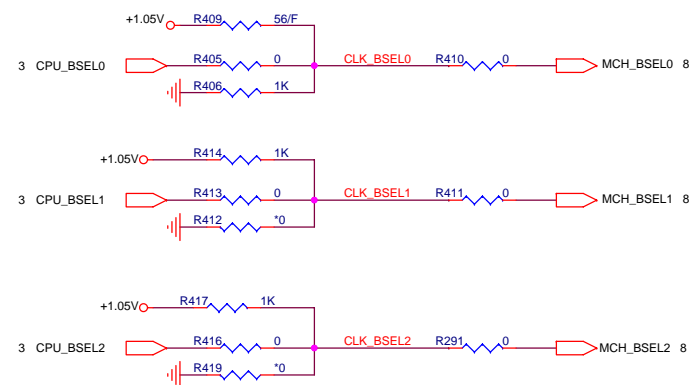
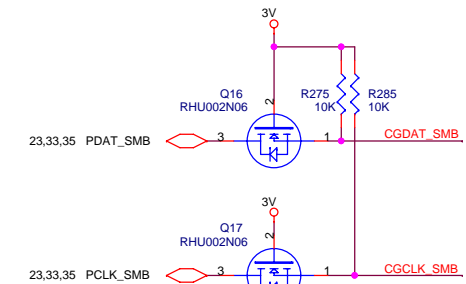
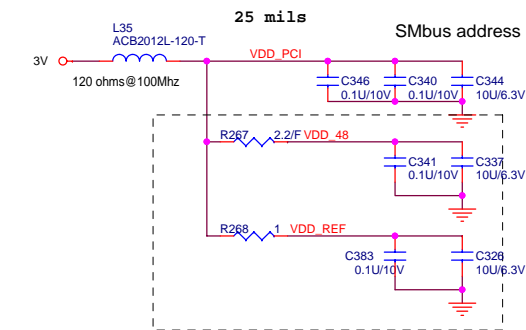
LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking
TV_OUT
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr
PAG 38

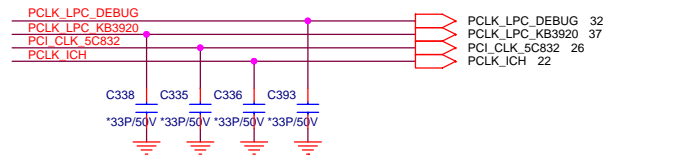
SYSTEM CHARGER(MAX8724)
PAG 39
SYSTEM POWER MAX8743A
PAG 40
DDR II SMDR_VTERM 1.8V/1.8VSUS(MAX8632)
PAG 41
VCCP +1.5V AND GMCH 1.05V(MAX8743)
PAG 42
VGACORE(1.025V)MAX1992
PAG 43
CPU CORE MAX8771
PAG 44

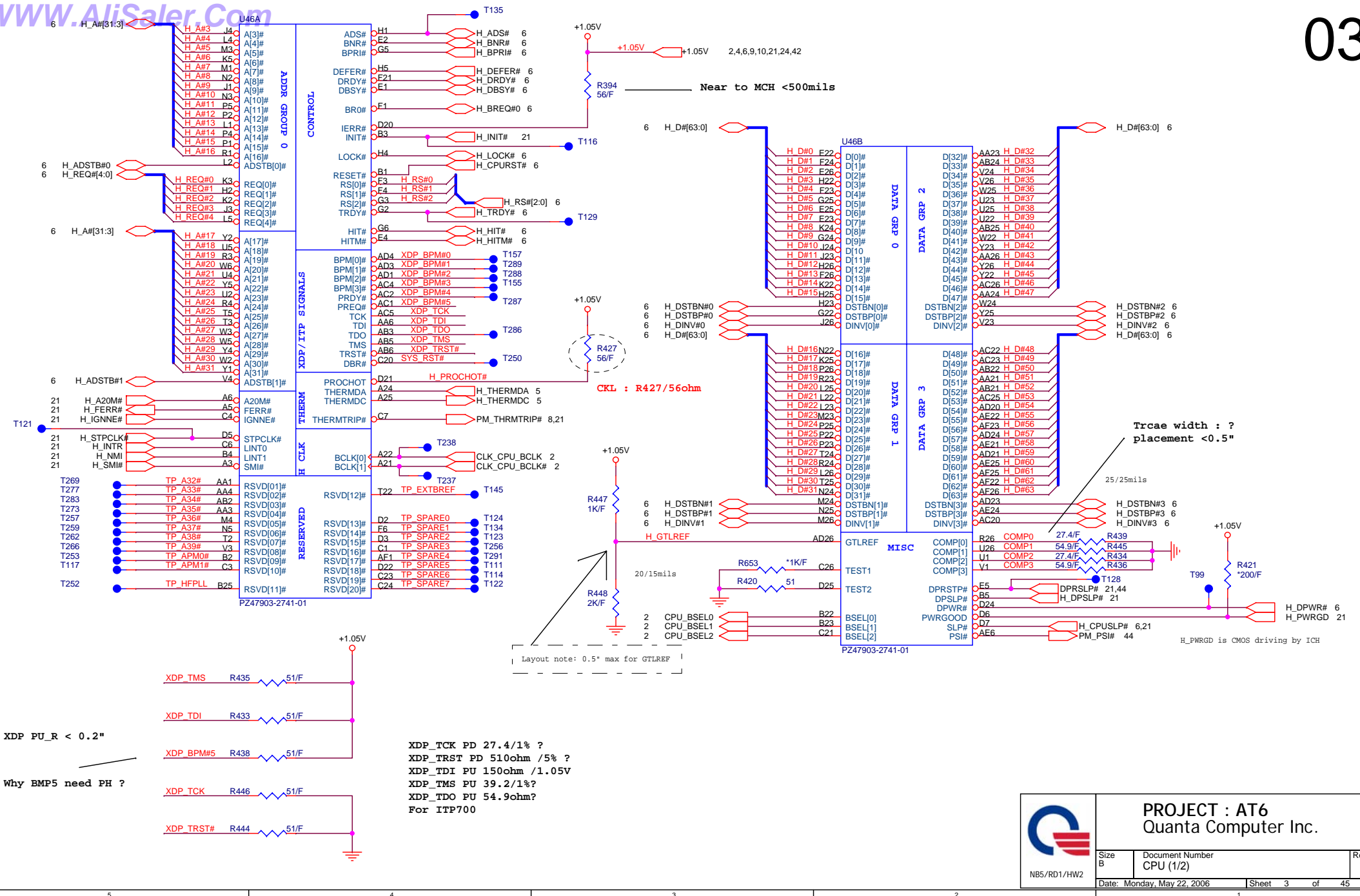


FSC	FSB	FSA	CPU	SRC	PCI	DOT
1	0	1	100	100	33	96
0	0	1	133	100	33	96
0	1	1	166	100	33	96
0	1	0	200	100	33	96
0	0	0	266	100	33	96
1	0	0	333	100	33	96
1	1	0	400	100	33	96
1	1	1	200	100	33	96

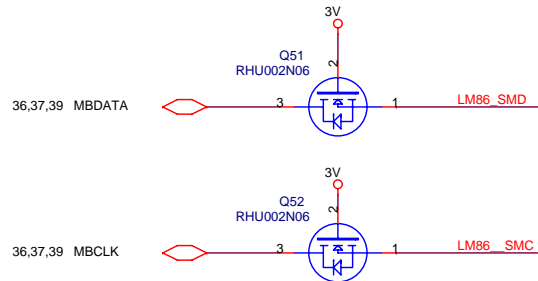
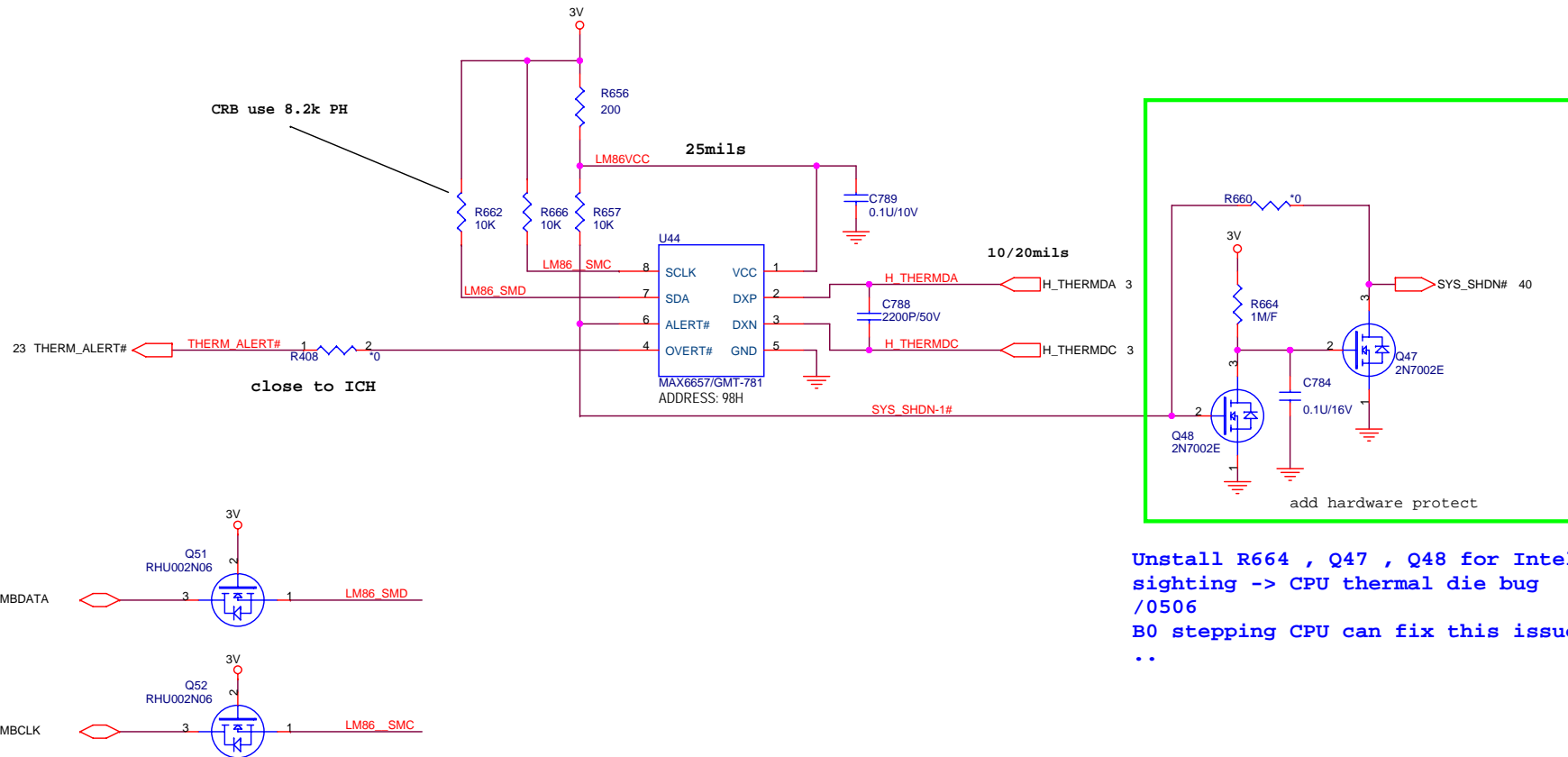


FSB Frequency Select		
FSB Freq (Mhz)	CPU DRIVEN (default)	R405=0
		R406=1K
		R413=0
		R414=1K
		R416=0
		R417=1K
	533	R405=NO STUFF
		R409=56/F
		R413=NO STUFF
		R412=0
		R416=NO STUFF
		R419=0
	667	R405=NO STUFF
		R409=56/F
		R413=NO STUFF
		R414=1K
		R416=NO STUFF
		R419=0



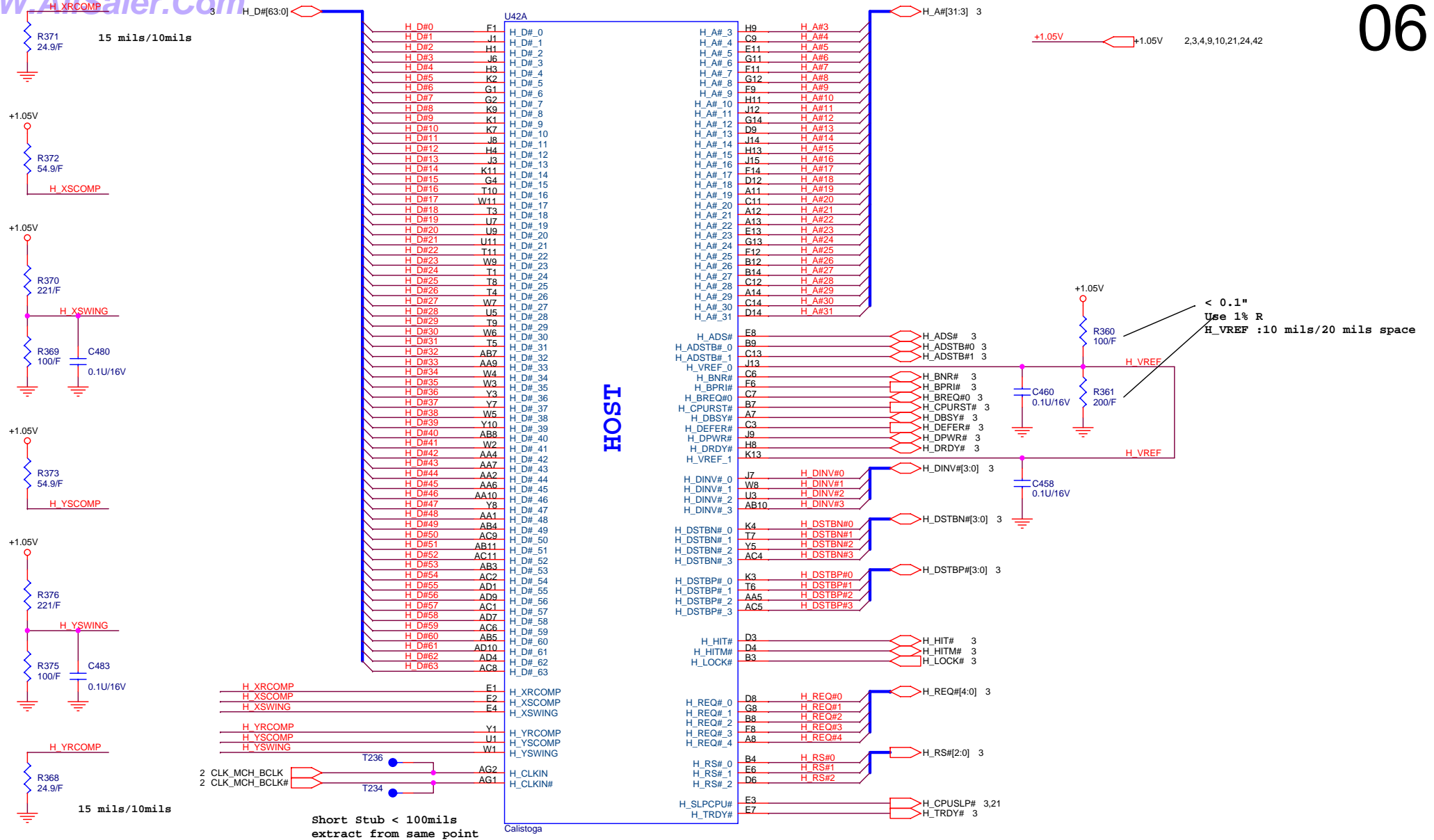






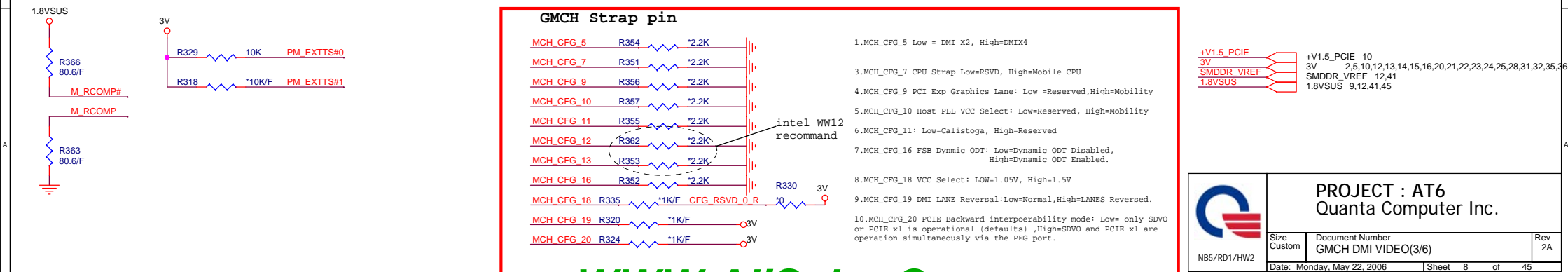
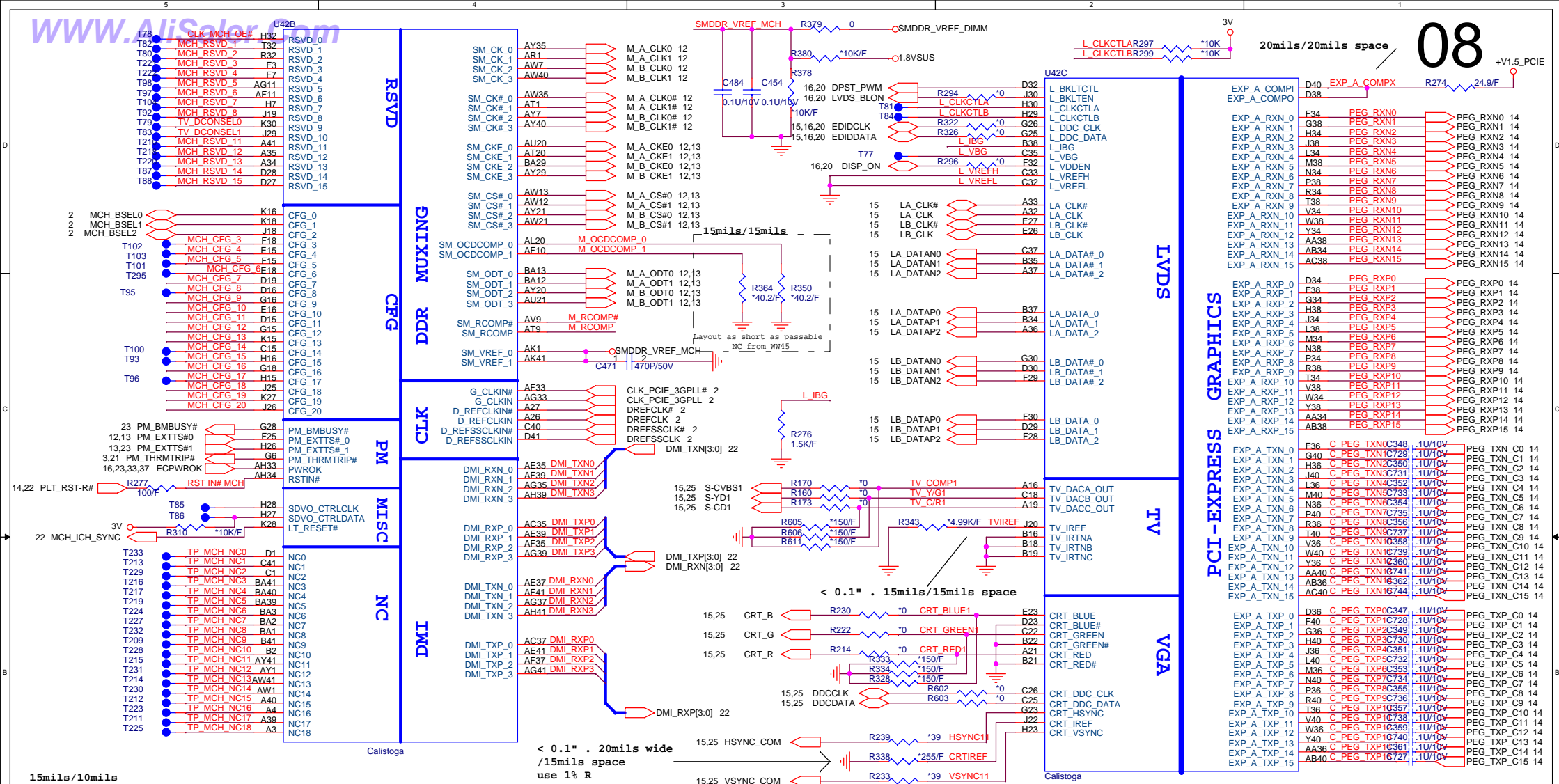
PROJECT : AT6
Quanta Computer Inc.

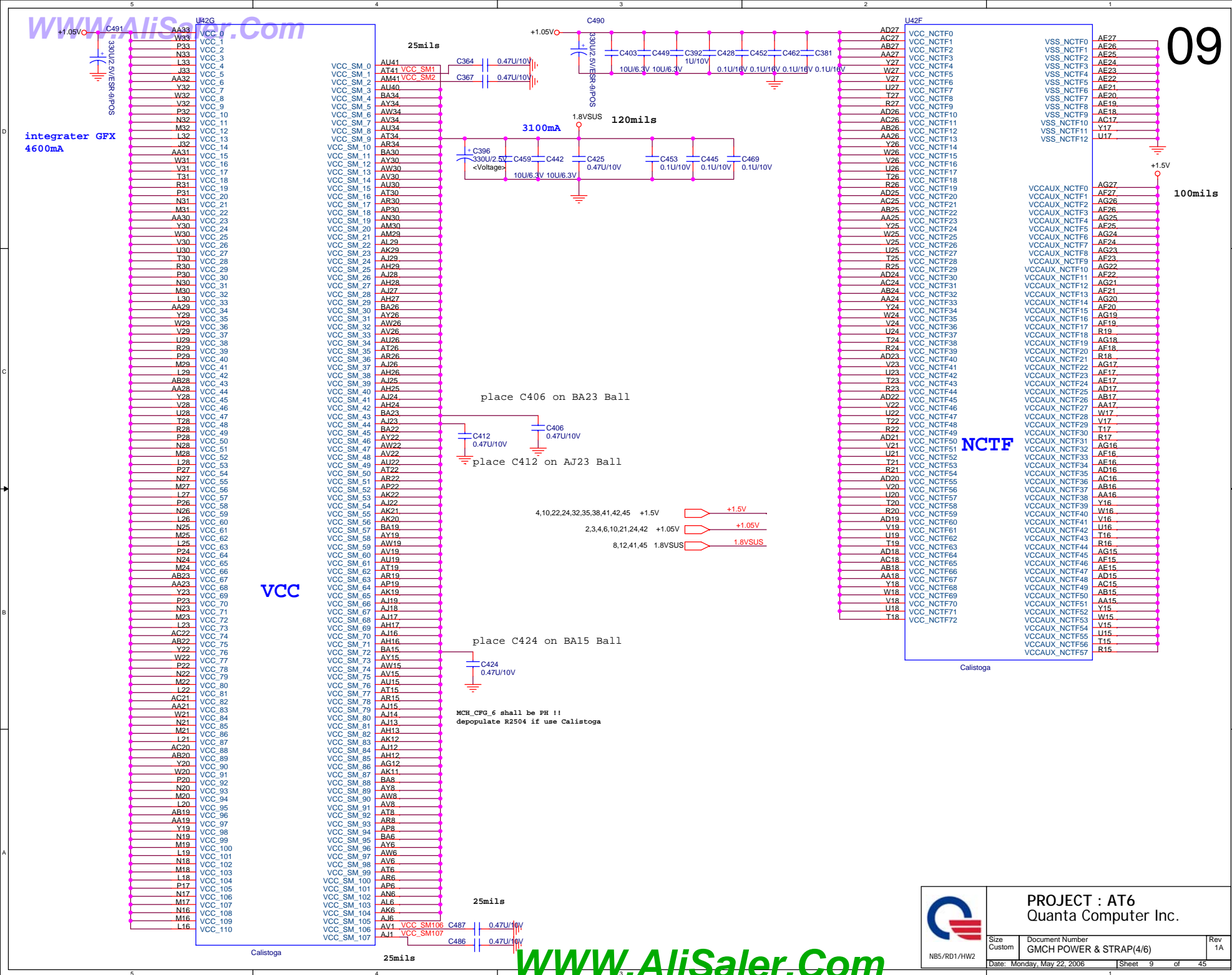
Size B	Document Number THERMAL LM86	Rev 2A
Date: Monday, May 22, 2006	Sheet 5 of 45	

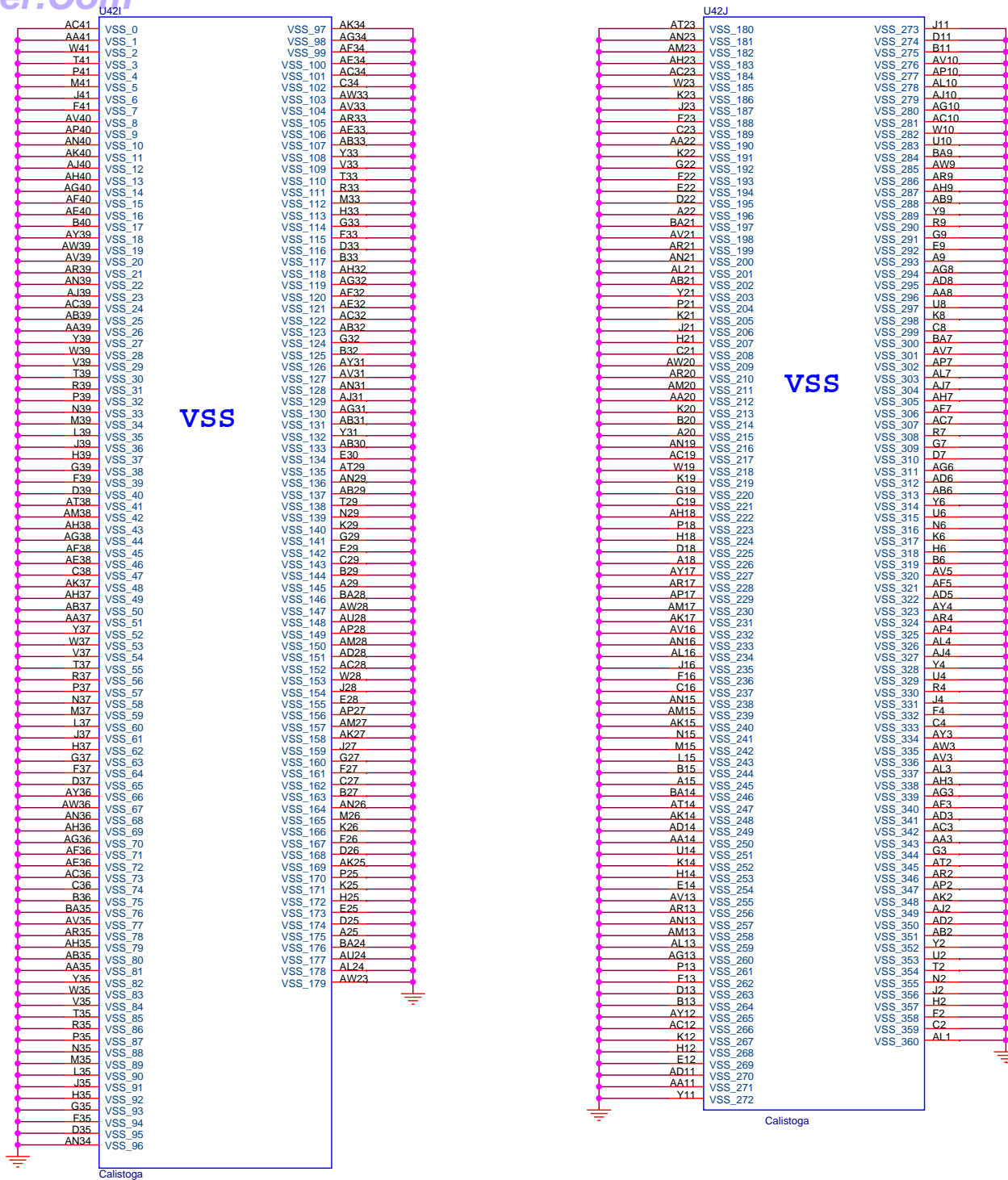


PROJECT : AT6 Quanta Computer Inc.		
Size B	Document Number GMCH HOST(1/6)	Rev 1A
Date: Monday, May 22, 2006 Sheet 6 of 45		









CGCLK_SMB
CGDAT_SMB
M_A_CKE[0..1]
M_A_CS[0..1]
M_A_RAS#
M_A_CAS#
M_A_WE#

CGCLK_SMB 2,13,32
CGDAT_SMB 2,13,32
M_A_CKE[0..1] 8,13
M_A_CS[0..1] 8,13
M_A_RAS# 7,13
M_A_CAS# 7,13
M_A_WE# 7,13

M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS[0..2]
M_A_ODT[0..1]

M_A_CLK0 8
M_A_CLK0# 8
M_A_CLK1 8
M_A_CLK1# 8
M_A_BS[0..2] 7,13
M_A_ODT[0..1] 8,13

M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DSQ[0..7]
M_A_DSQ[0..7]
M_A_A[13..0]

M_A_DQM[0..7] 7
M_A_DQ[0..63] 7
M_A_DSQ[0..7] 7
M_A_DSQ[0..7] 7
M_A_A[13..0] 7,13

M_B_CKE[0..1]
M_B_CS[0..1]
M_B_RAS#
M_B_CAS#
M_B_WE#

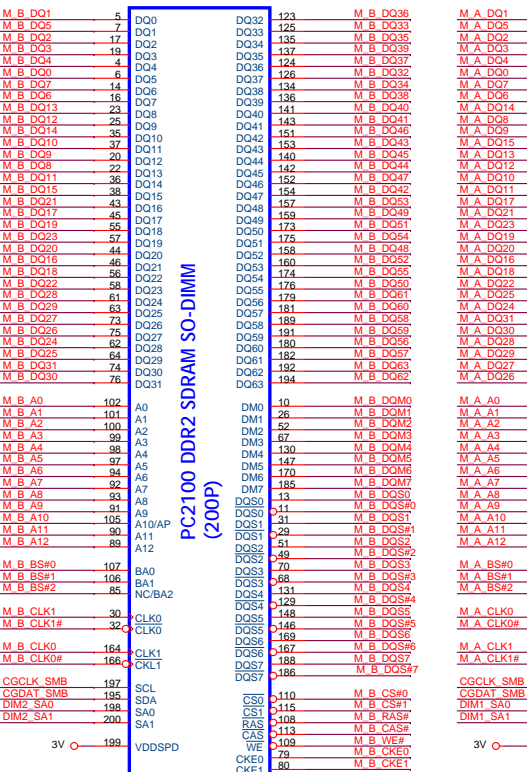
M_B_CKE[0..1] 8,13
M_B_CS[0..1] 8,13
M_B_RAS# 7,13
M_B_CAS# 7,13
M_B_WE# 7,13

M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS[0..2]
M_B_ODT[0..1]

M_B_CLK0 8
M_B_CLK0# 8
M_B_CLK1 8
M_B_CLK1# 8
M_B_BS[0..2] 7,13
M_B_ODT[0..1] 8,13

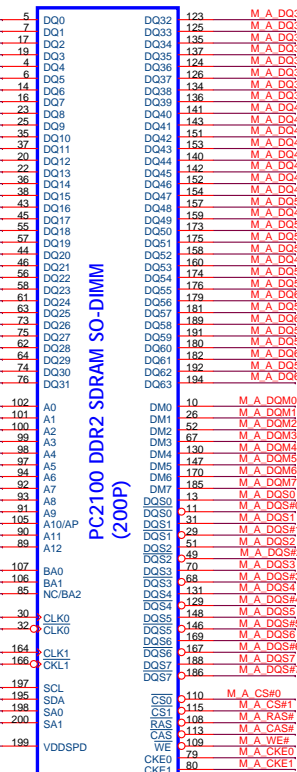
M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DSQ[0..7]
M_B_DSQ[0..7]
M_B_A[13..0]

M_B_DQM[0..7] 7
M_B_DQ[0..63] 7
M_B_DSQ[0..7] 7
M_B_DSQ[0..7] 7
M_B_A[13..0] 7,13



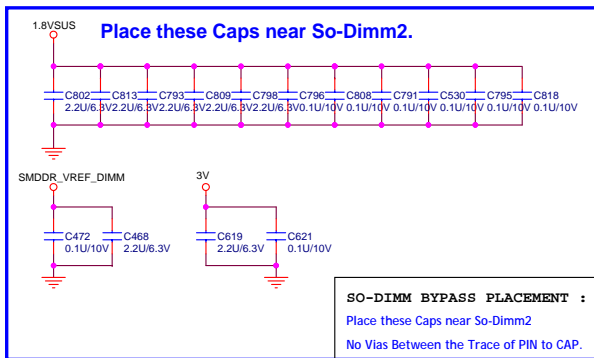
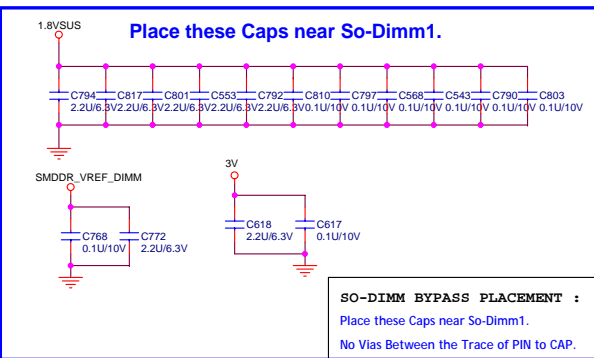
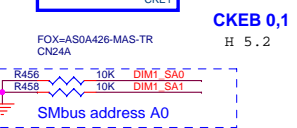
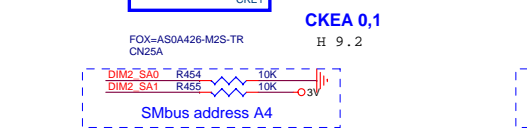
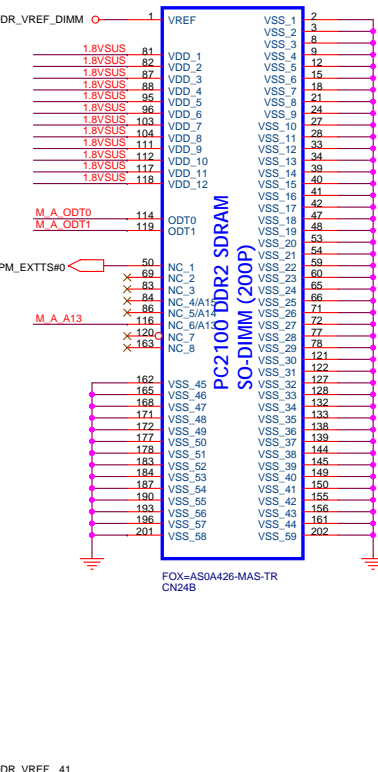
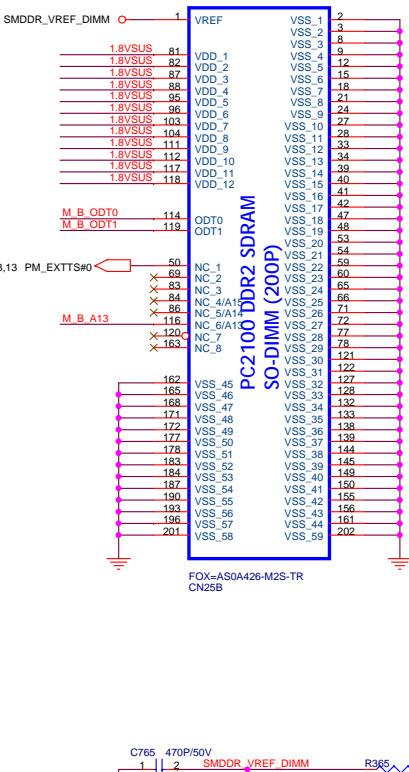
CKEA 0,1

H 9.2

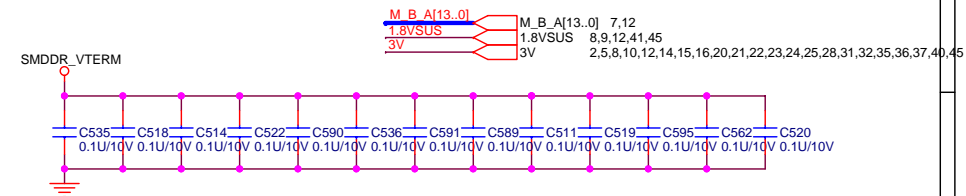
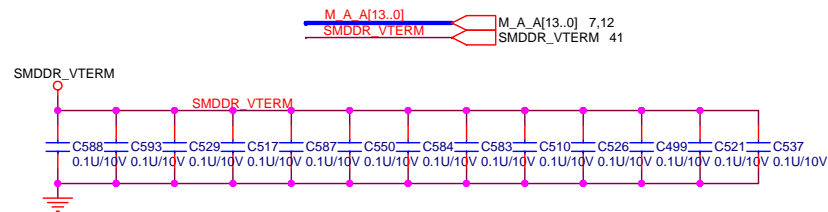


CKEB 0,1

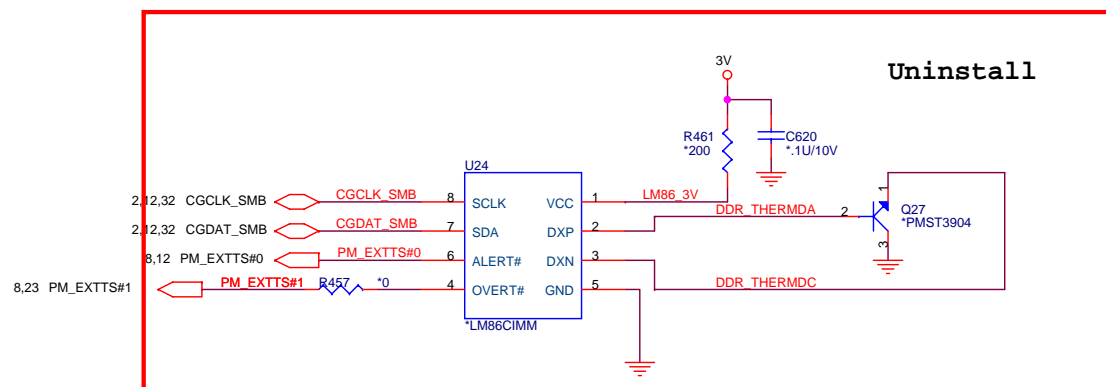
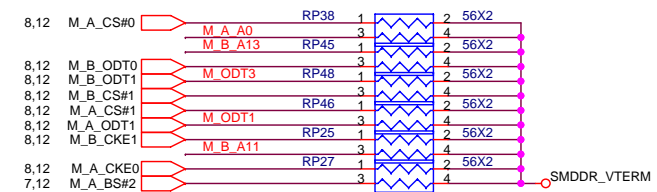
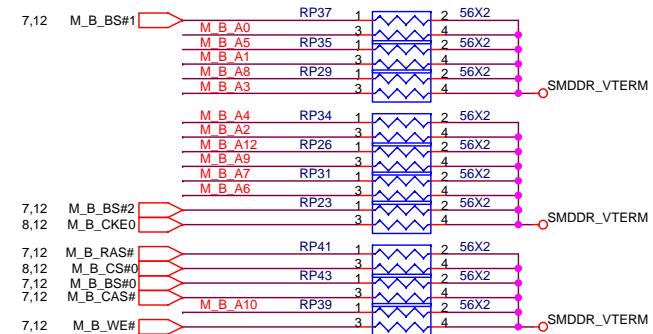
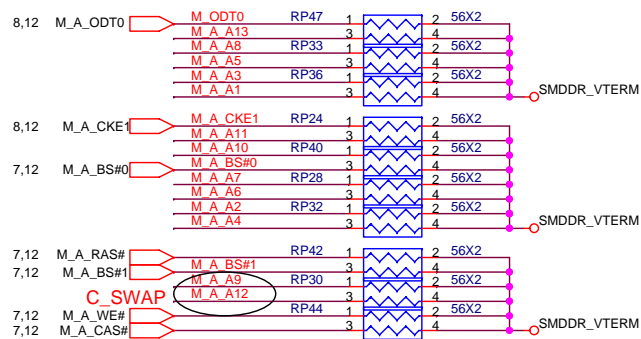
H 5.2



DDR II B CHANNEL

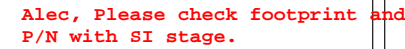


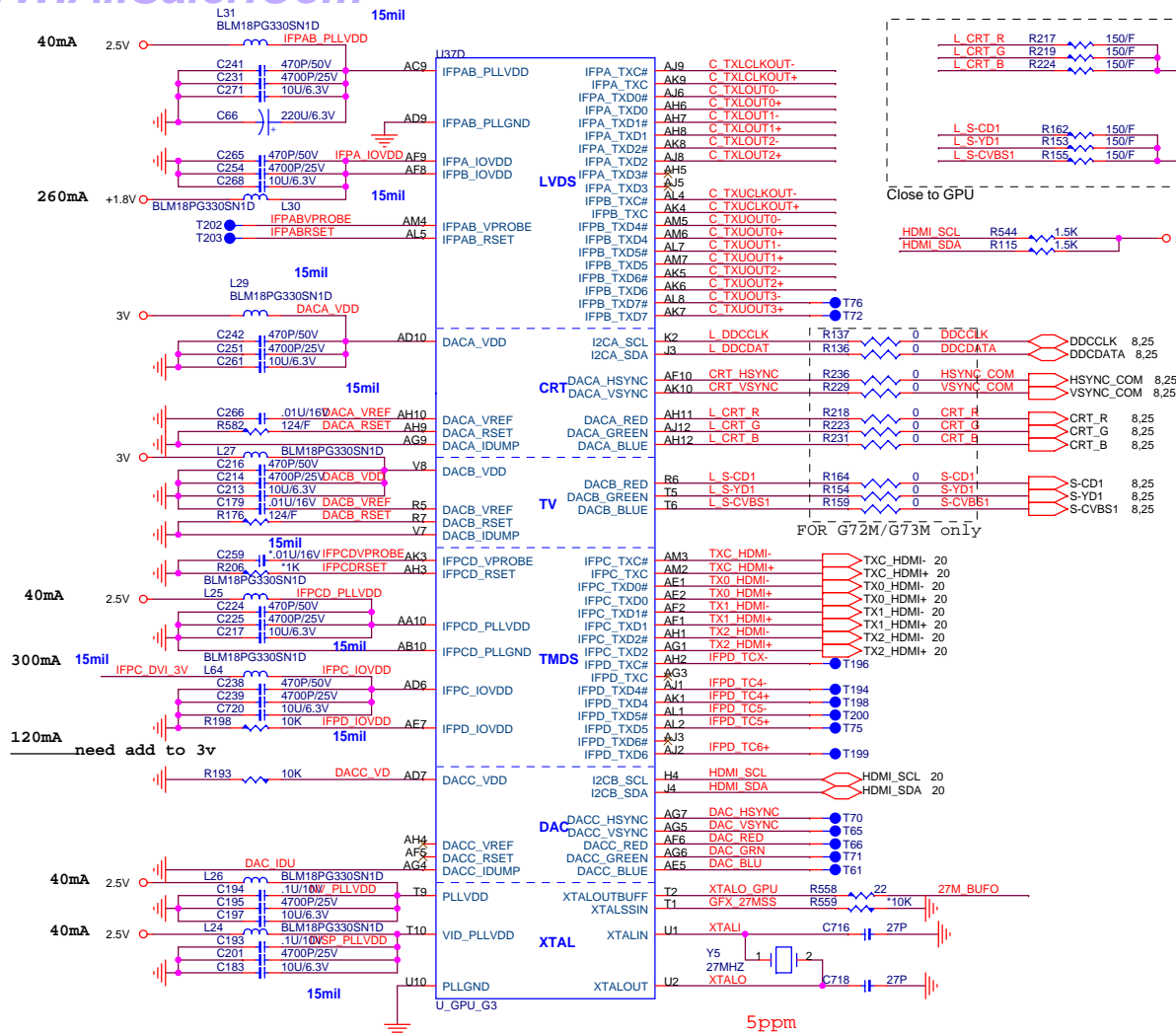
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



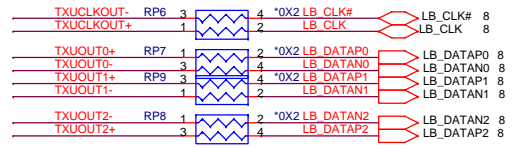
PROJECT : AT6
Quanta Computer Inc.

Size B	Document Number DDRII RES.ARRAY	Rev 1A
Date: Monday, May 22, 2006	Sheet 13 of 45	

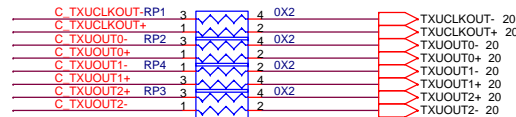
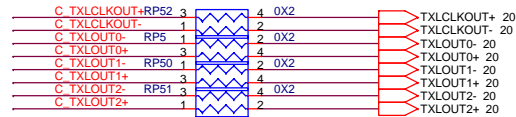




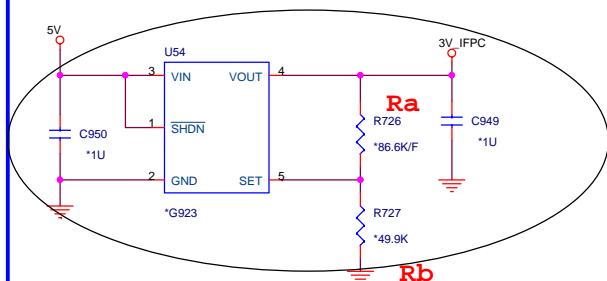
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA

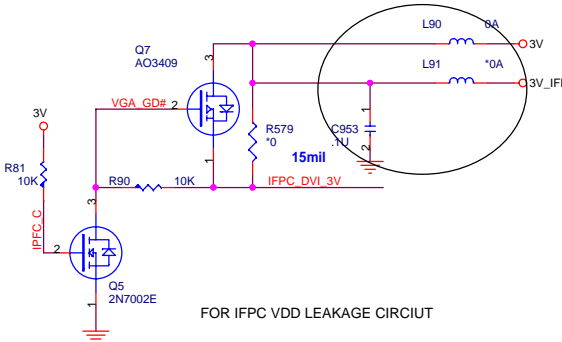


C_For HDMI Nvidia's PUN issue

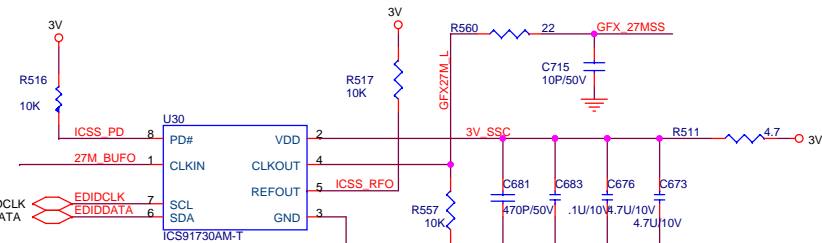


$$V_{out} = 1.25 \left(1 + \frac{R_a}{R_b} \right)$$

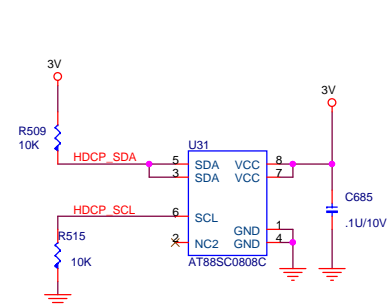
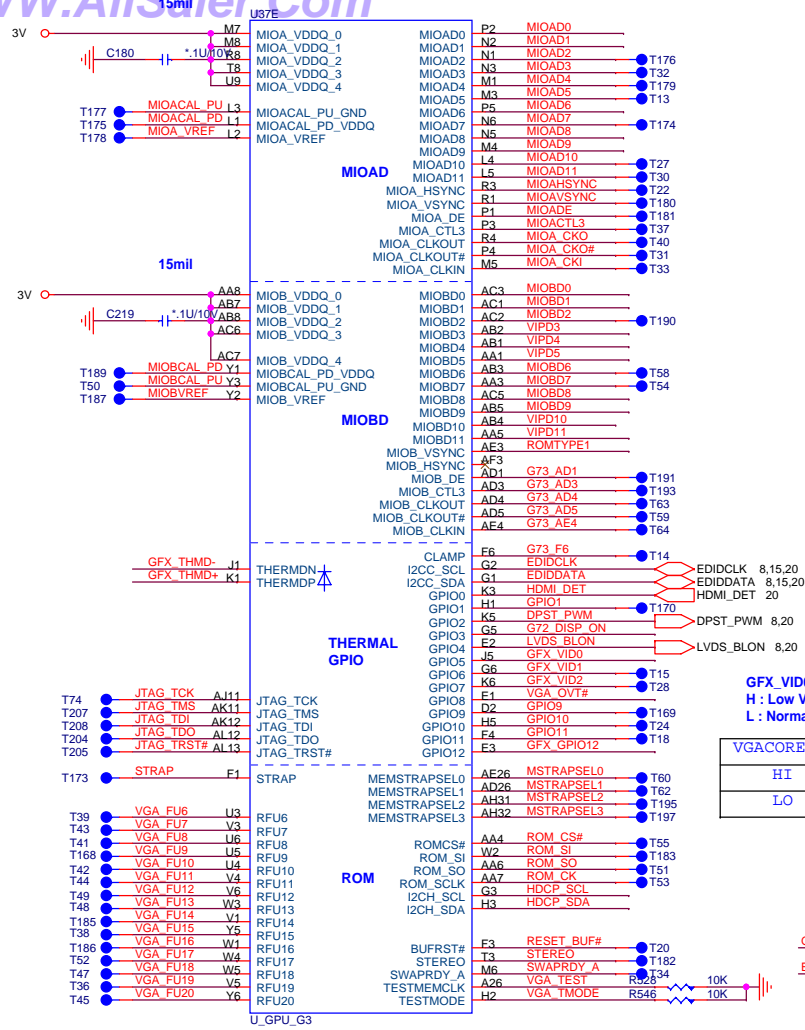
C_For HDMI Nvidia's PUN issue



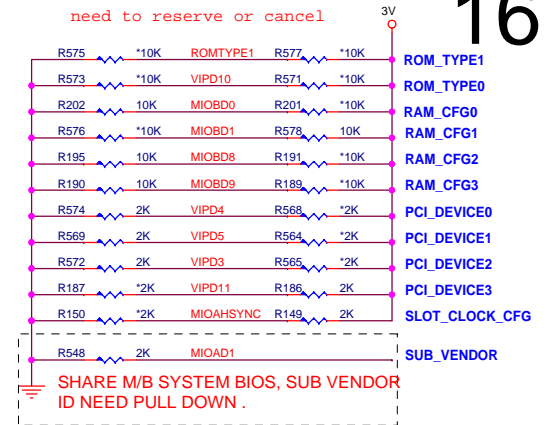
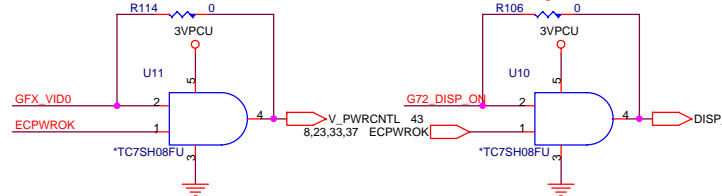
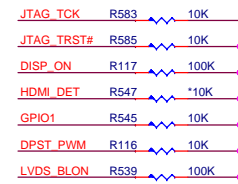
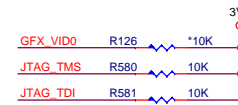
SPREAD SPECTRUM



I2C ADDRESS: 0xD4H



PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved

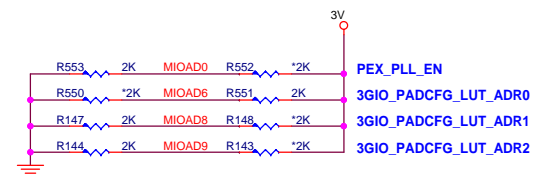
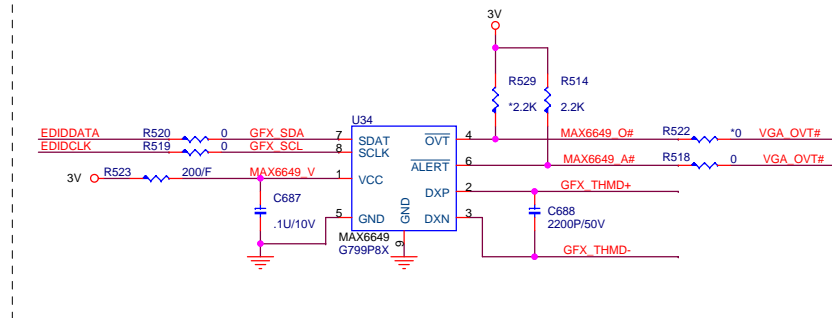
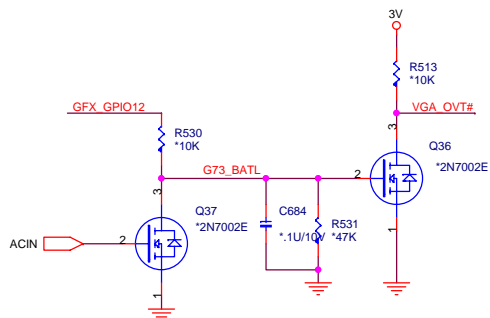


G72M VRAM Configuration Table

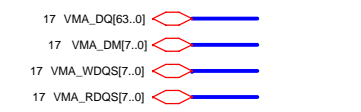
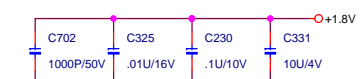
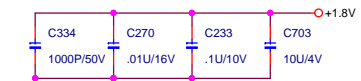
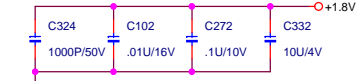
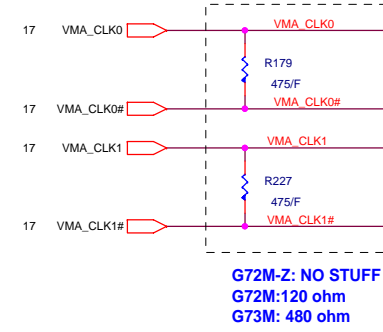
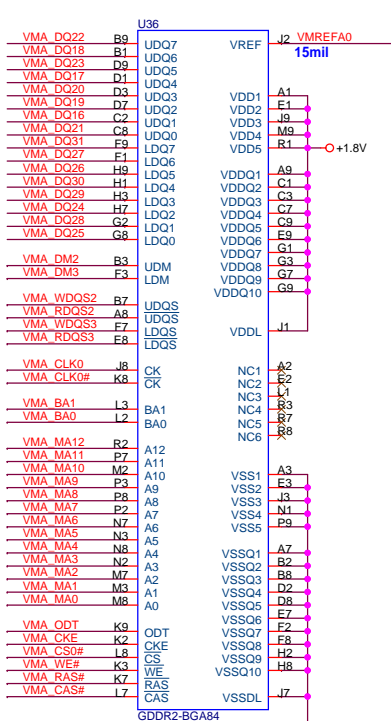
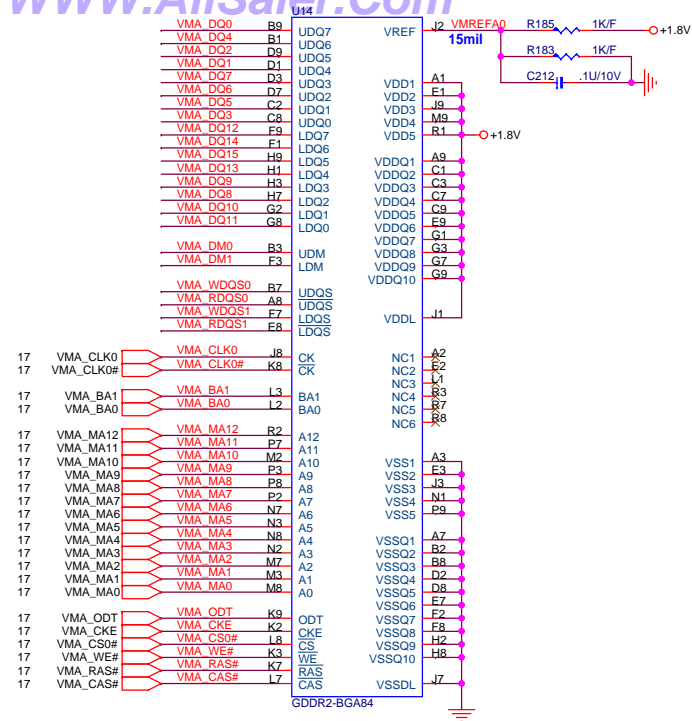
RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix

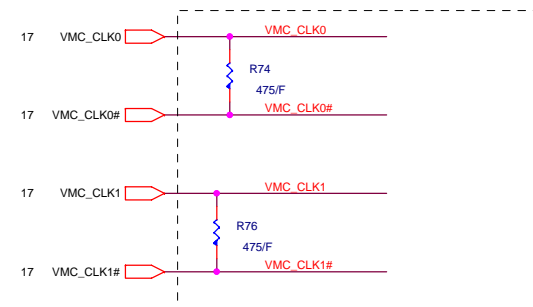
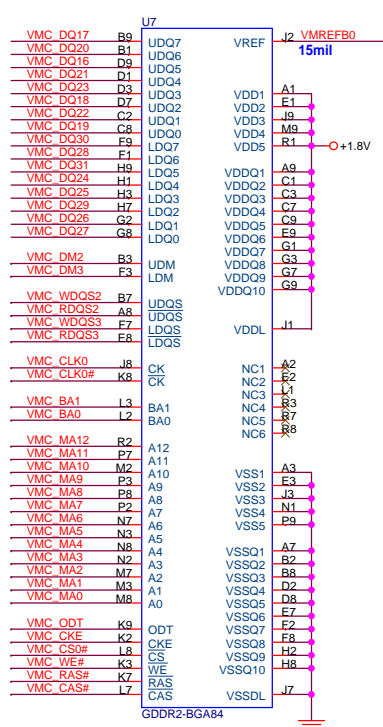
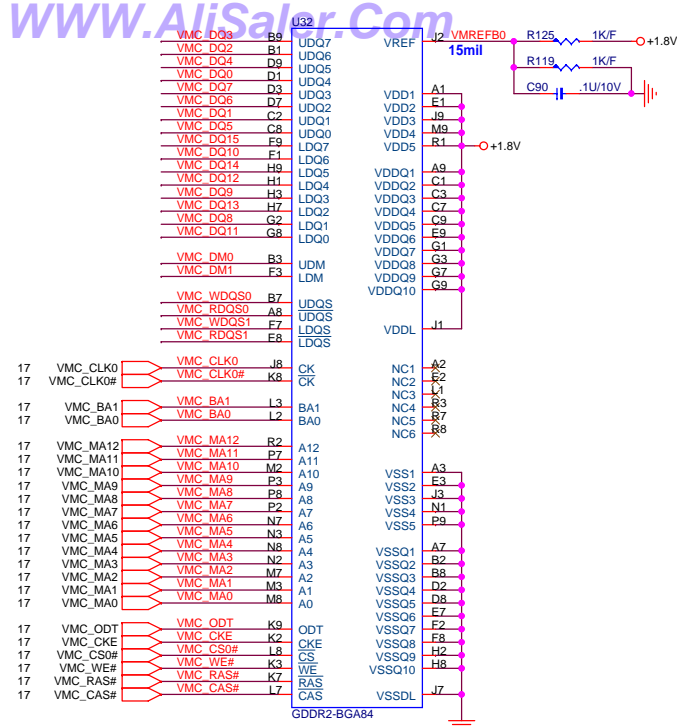




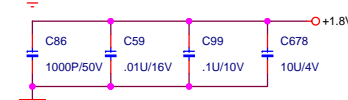
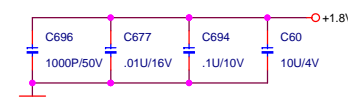
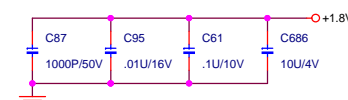
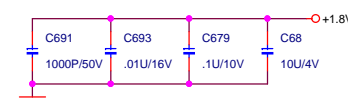


256Mb : AKD5JGAT*05

512Mb : AKD59G-T*01



G72M-Z:NO STUFF
G72M:120 ohm
G73M: 480 ohm



17 VMC_DQ[63..0]

17 VMC_DM[7..0]

17 VMC_WDQS[7..0]

17 VMC_RDQS[7..0]

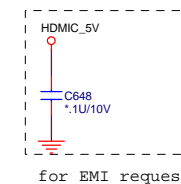
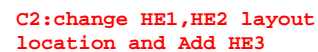
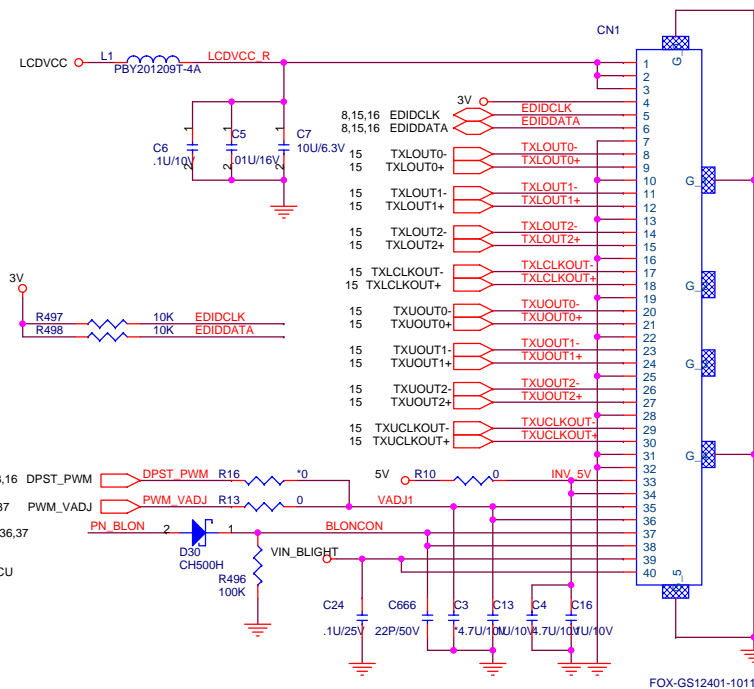
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01



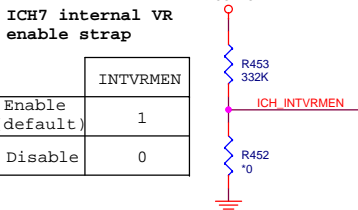
NB5/RD1/HW2

PROJECT : AT6
Quanta Computer Inc.

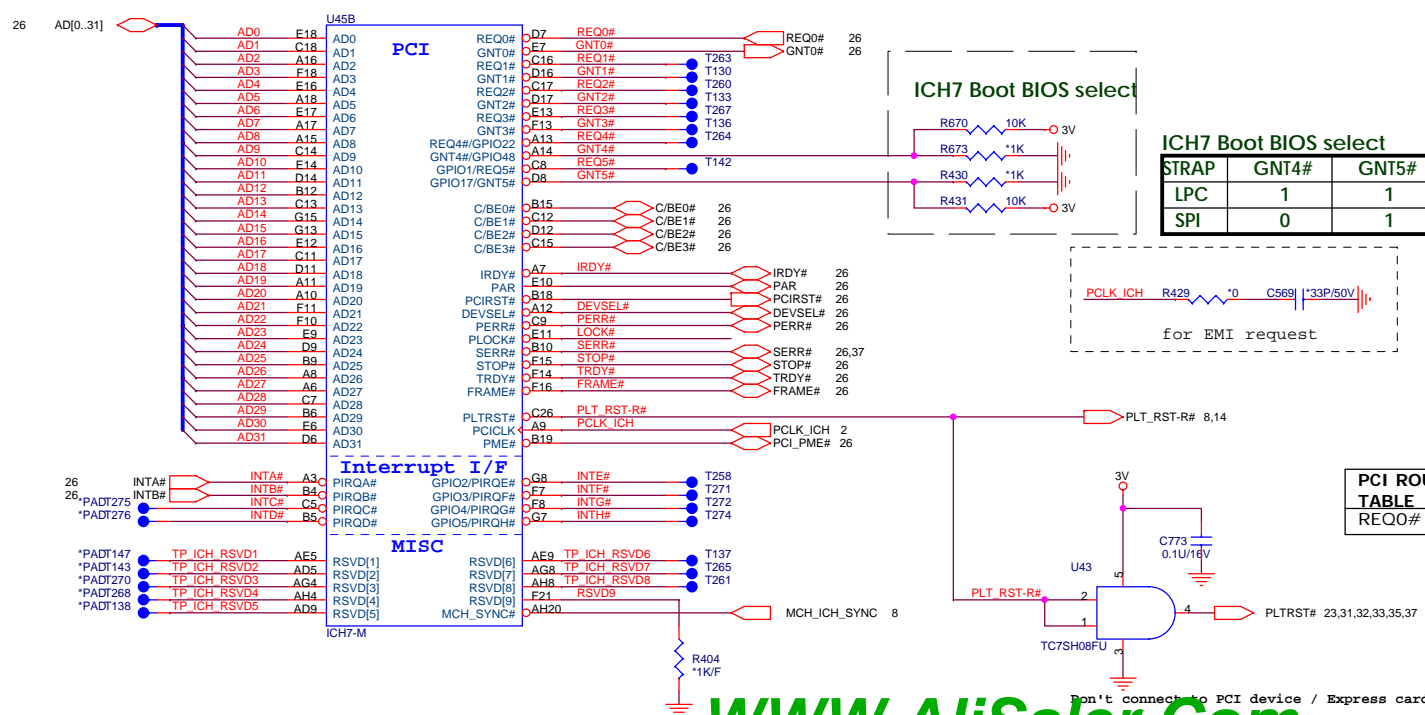
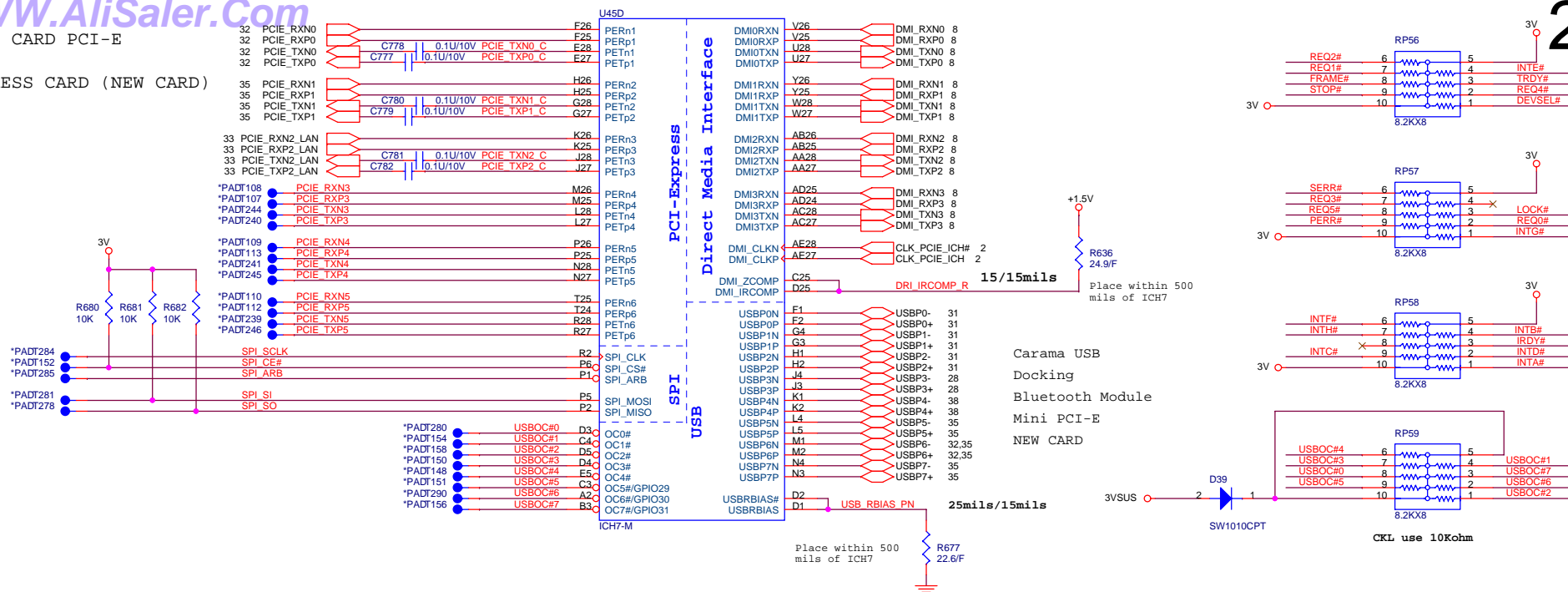
Size Custom	Document Number NVG73M VREM-2(GDDR2 BGA84)	Rev 1A
Date: Monday, May 22, 2006		Sheet 19 of 45



LAYOUT must support connectors from JAE, Molex and Acon.



EXPRESS CARD (NEW CARD)



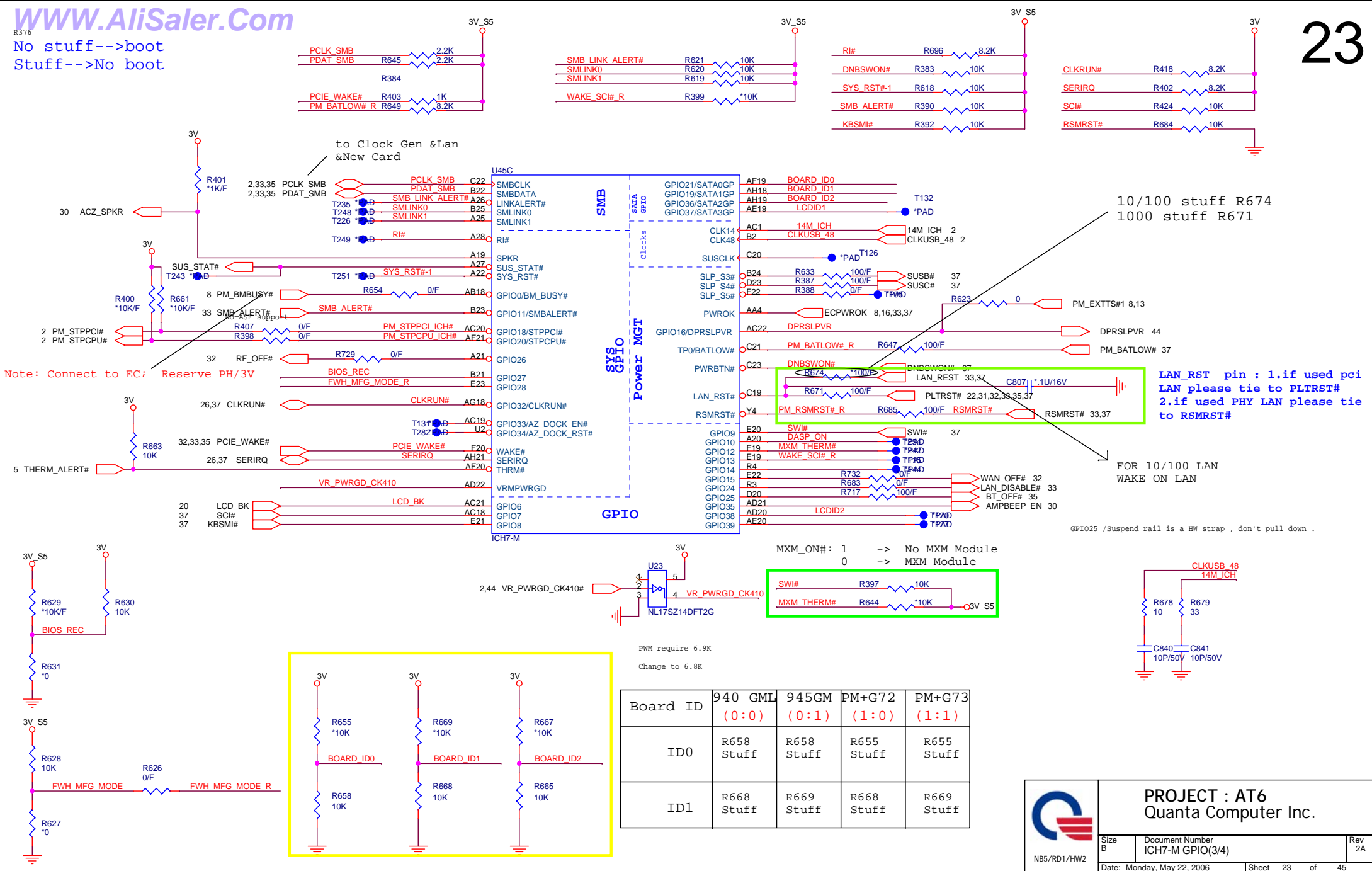
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH83C

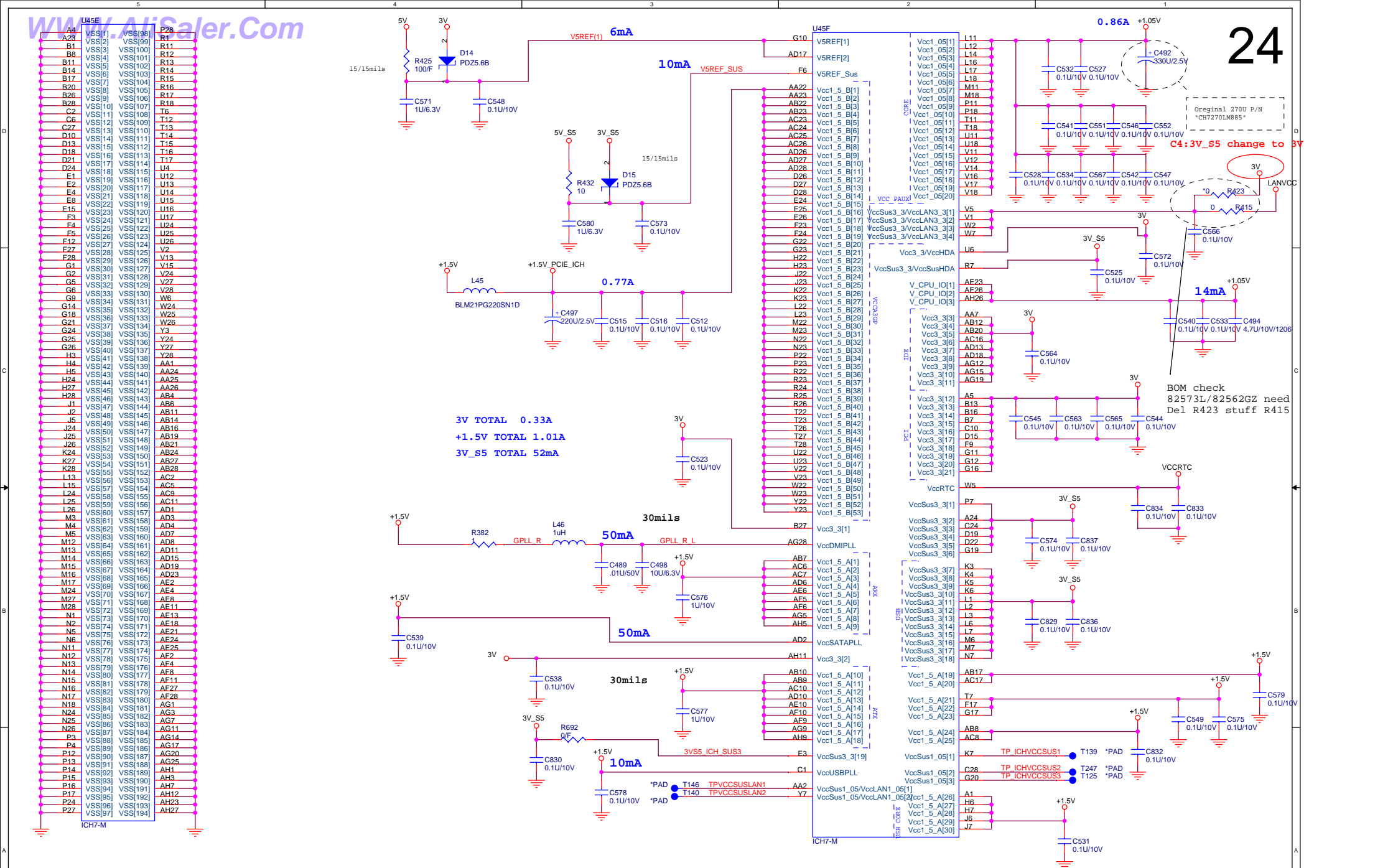


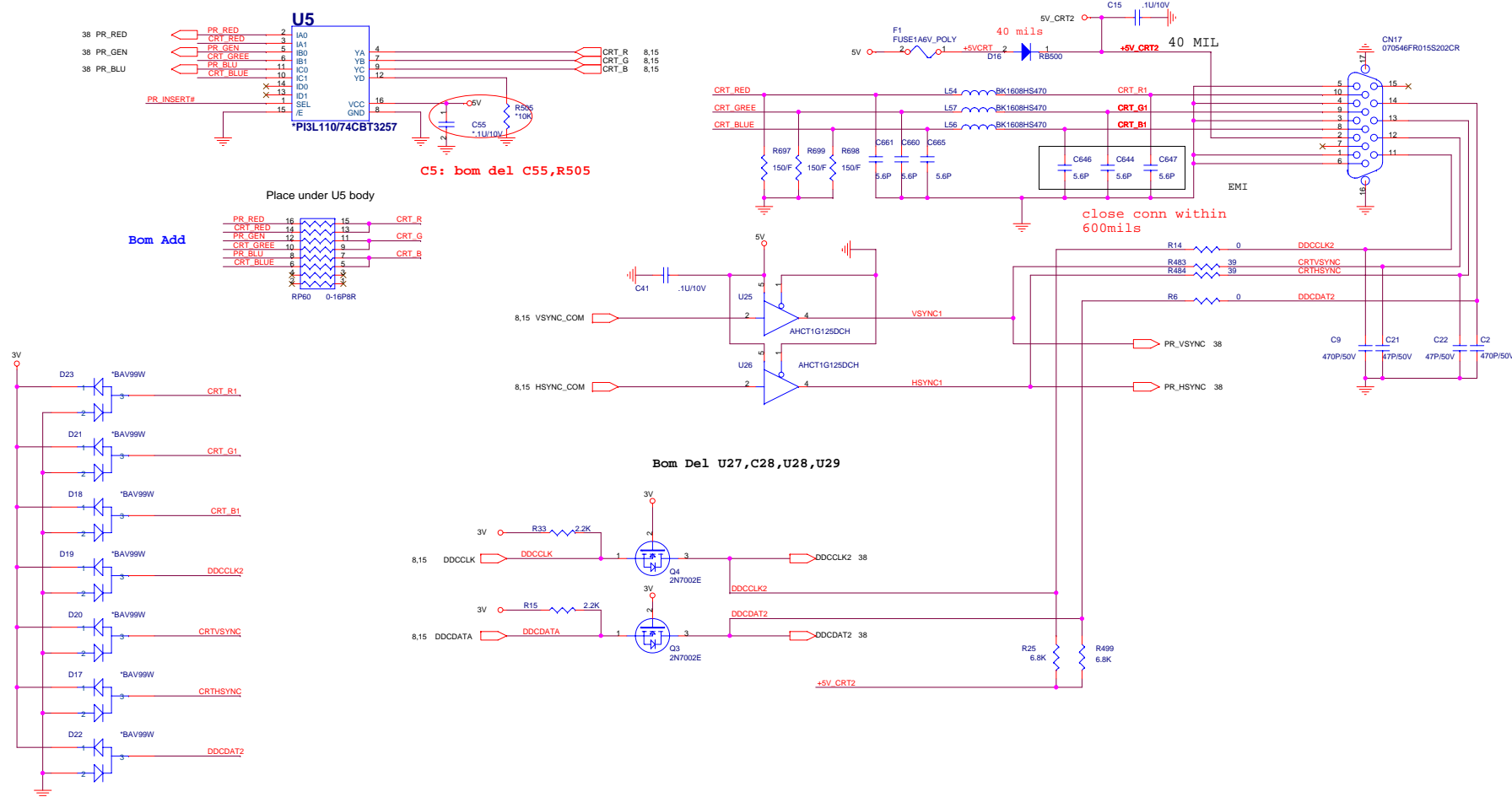
PROJECT : AT6
Quanta Computer Inc.

Size Custom	Document Number ICH7-M M PCI E(2/4)	R
Date: Monday, May 22, 2006	Sheet 22 of 45	

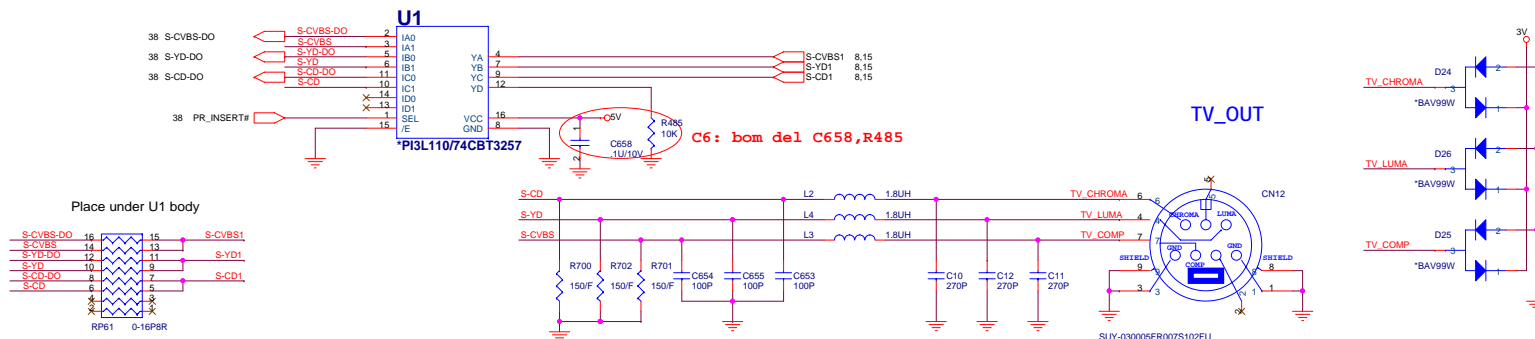
No stuff-->boot
Stuff-->No boot

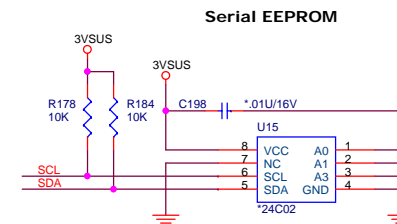
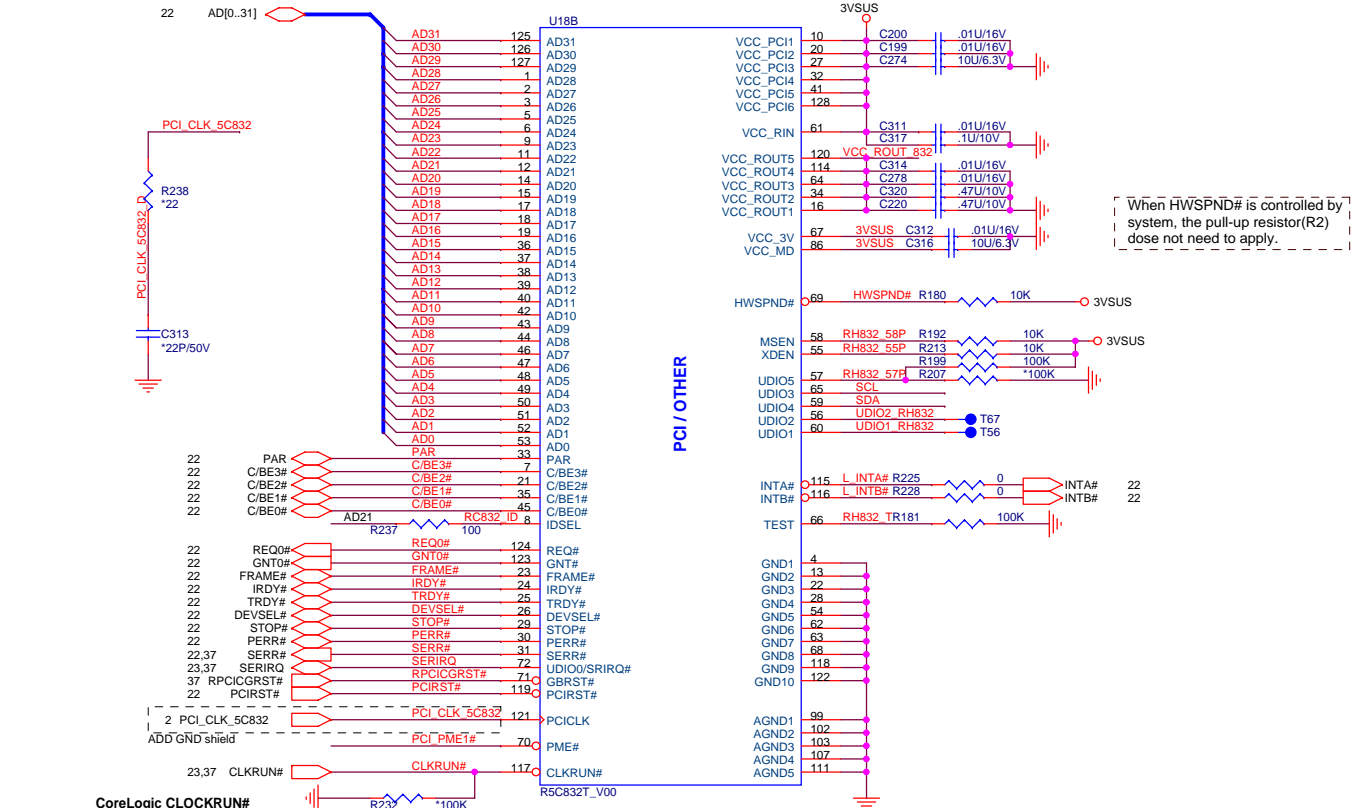






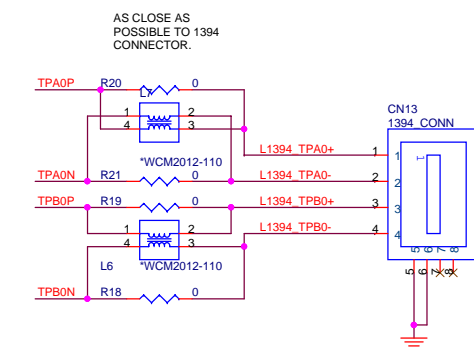
TV_SWITCH



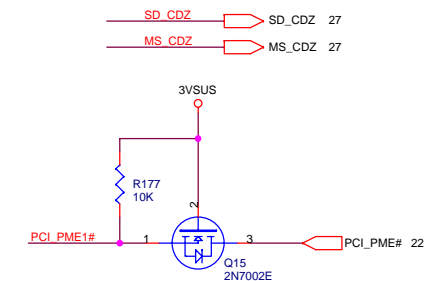


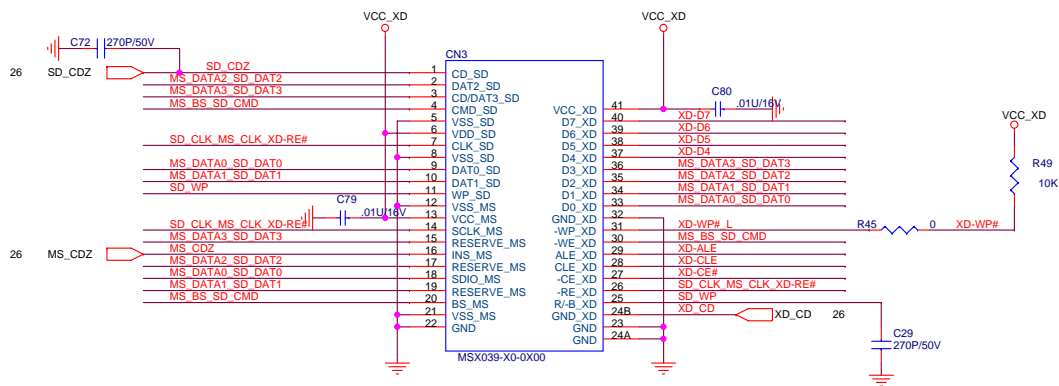
* NOT Use EEPROM :
R199 : installed
R207,U15,C198 : NOT installed

* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed

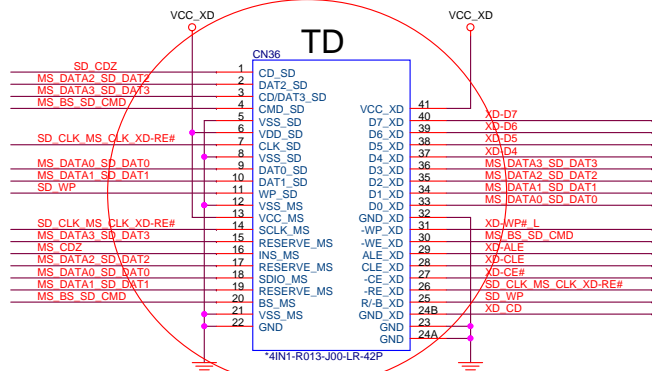


*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically And layout with shields.
Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

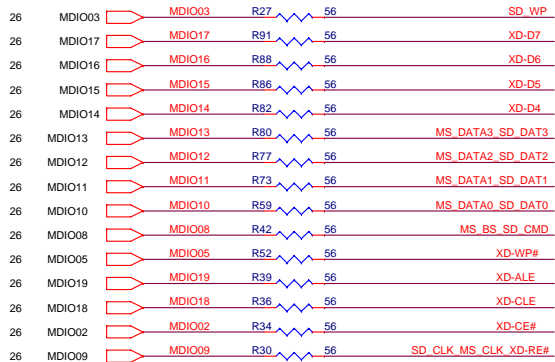




C7: change CN36 footprint

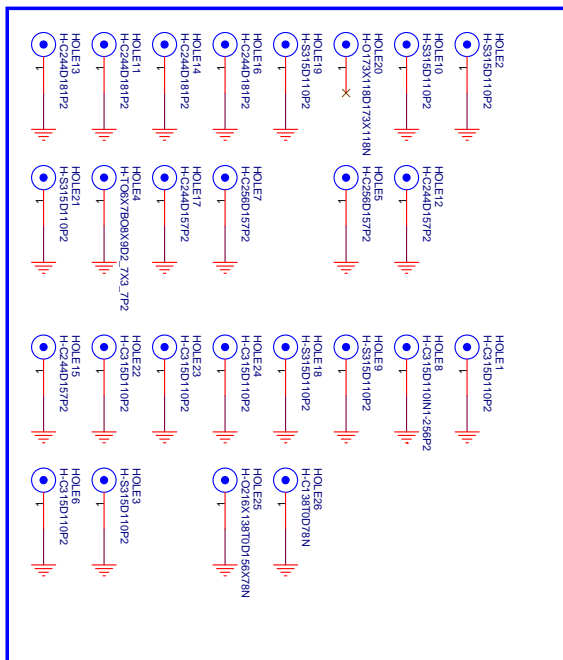


bom create 2'nd source

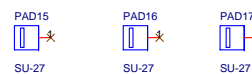
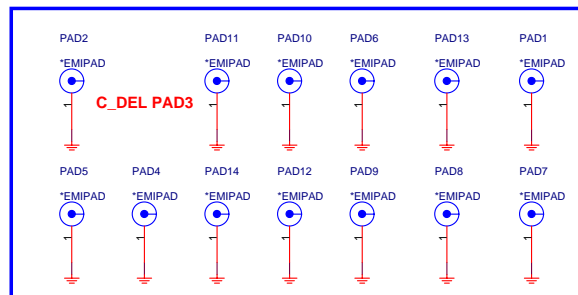


C_Delete reserve circuit for card reader power.

SCREW HOLE

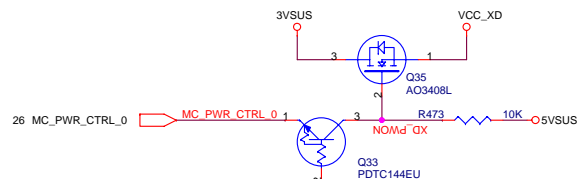
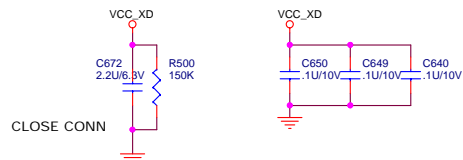


EMI PAD



moden cable sprig

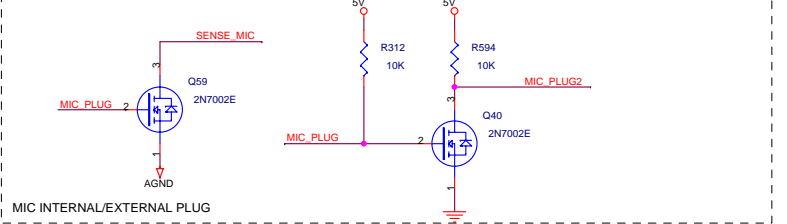
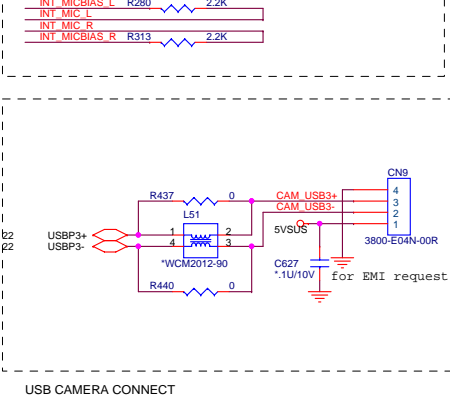
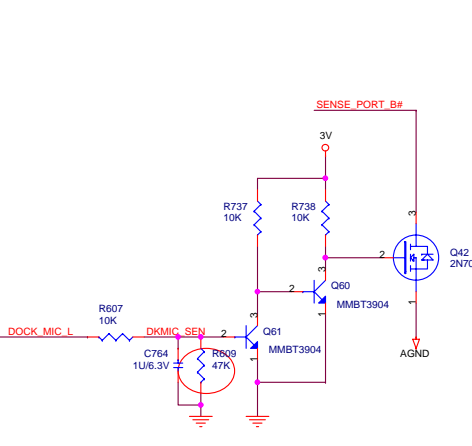
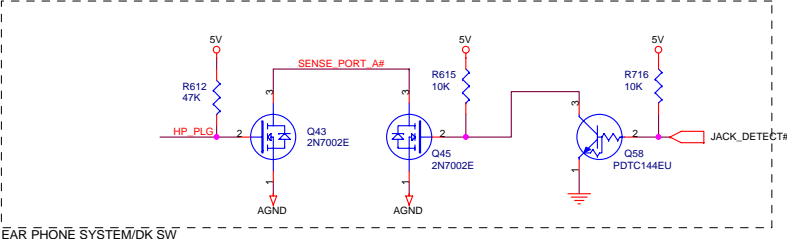
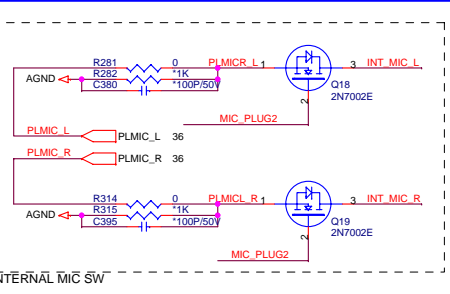
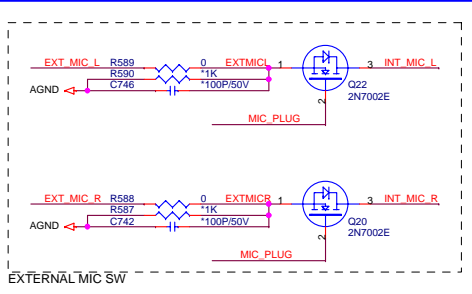
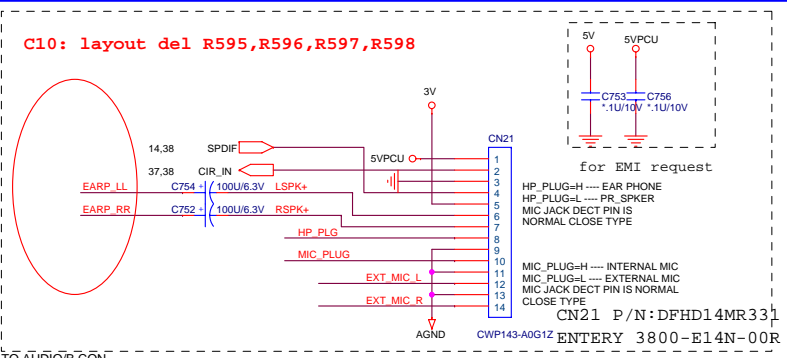
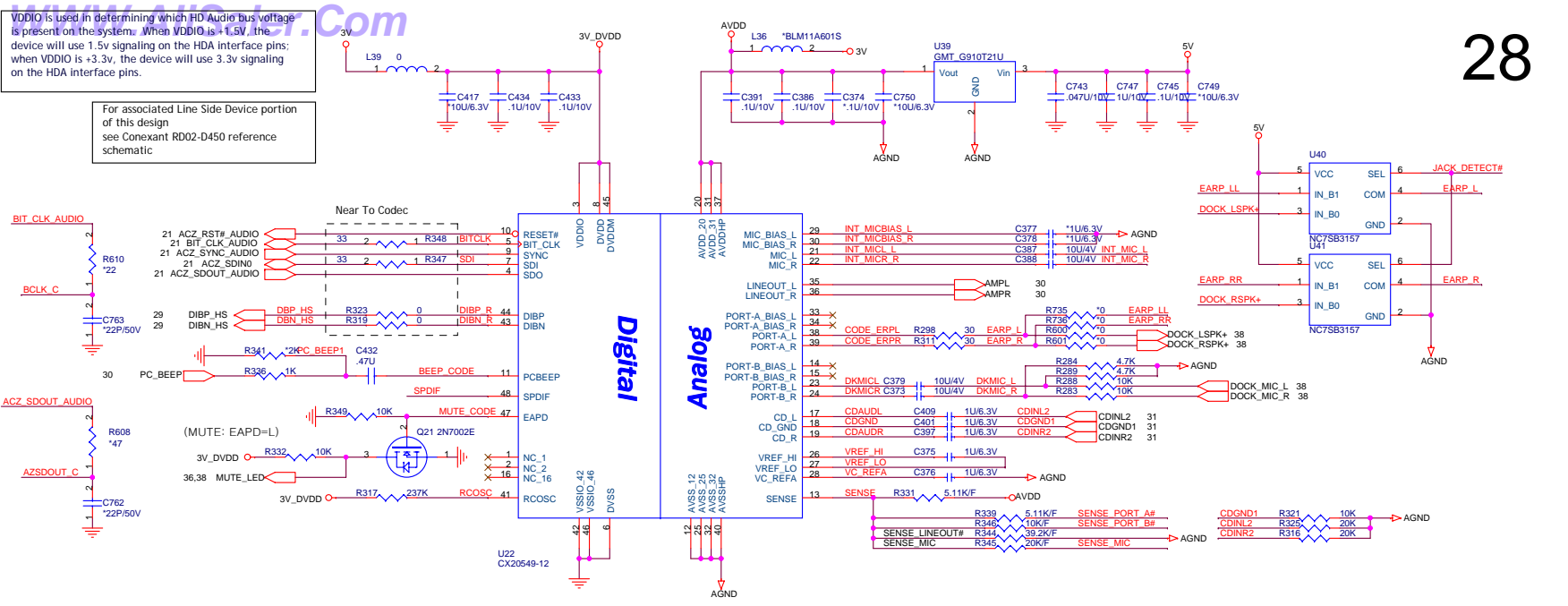
C8: Add lock bluetools cable sprig



PROJECT : AT6 Quanta Computer Inc.		
Size Custom	Document Number CARD READER/HOLE	Rev 1A
Date: Monday, May 22, 2006		
Sheet 27 of 45		

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5V signaling on the HDA interface pins; when VDDIO is +3.3V, the device will use 3.3V signaling on the HDA interface pins.

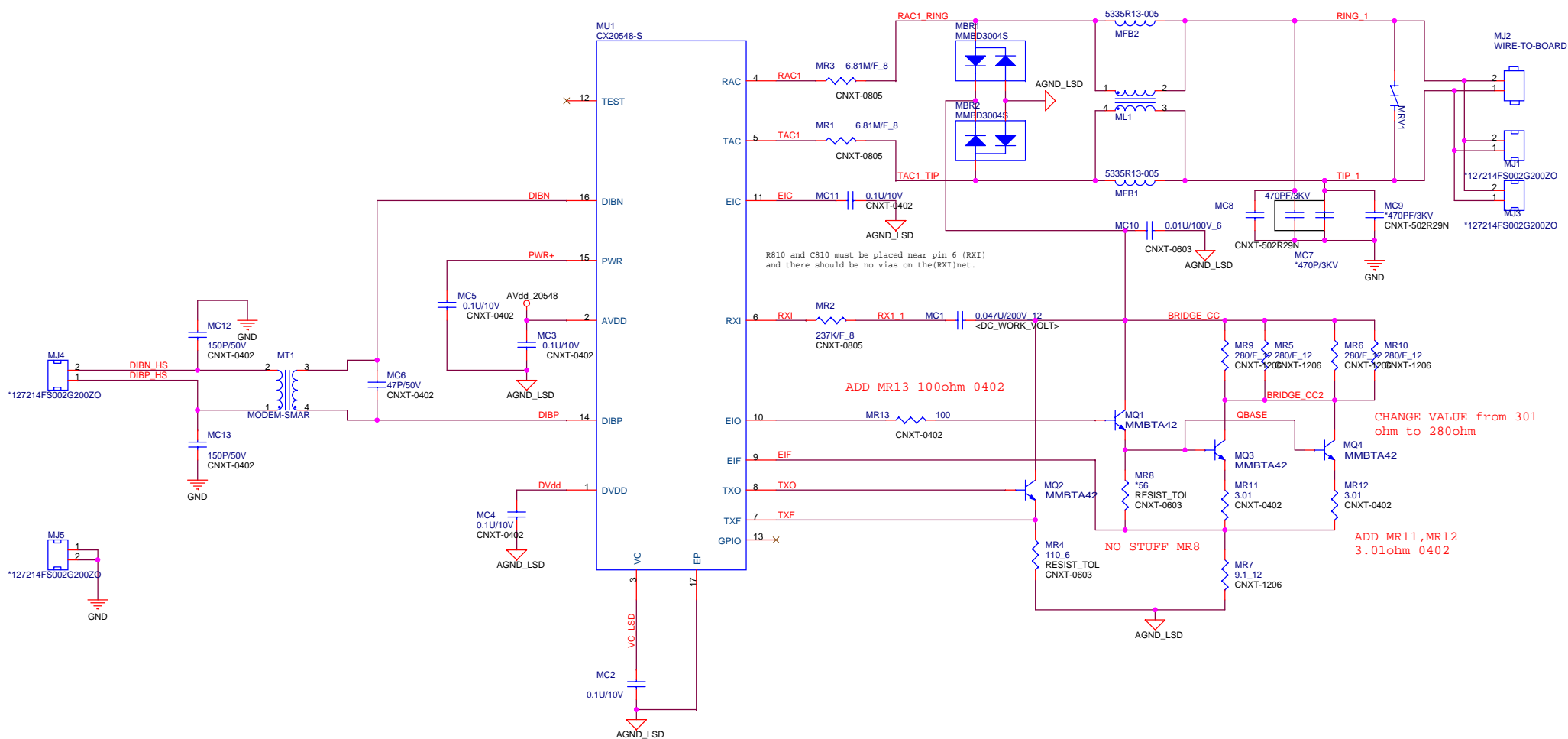
For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

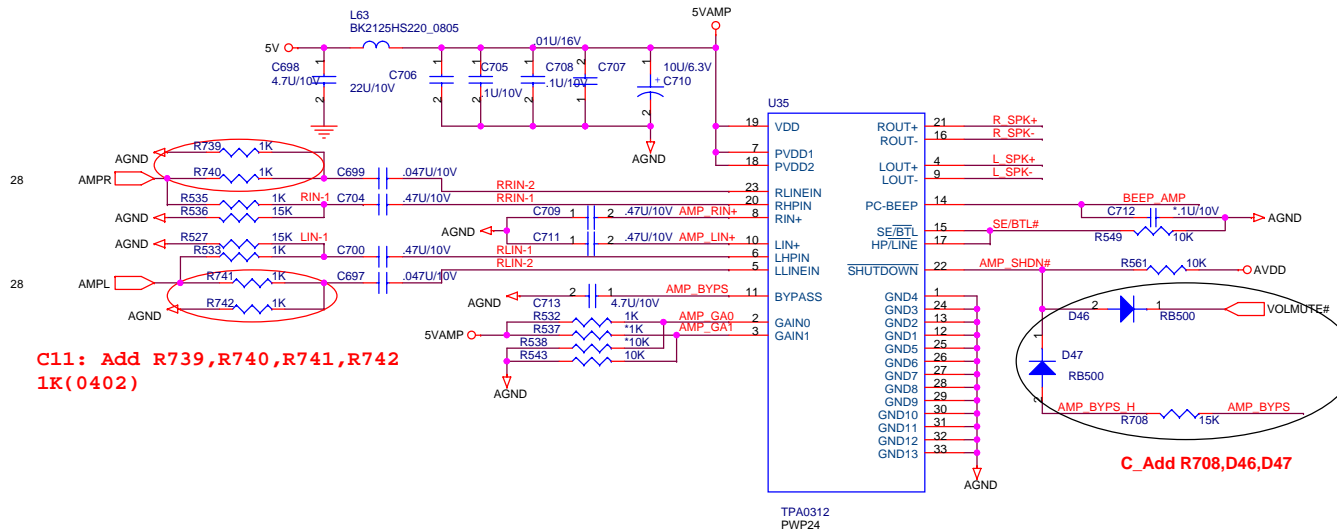


Revision History

REV	Description	Date
0	Initial Release	April 26, 2005

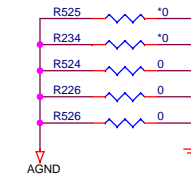
28 DIBN_HS
28 DIBP_HS





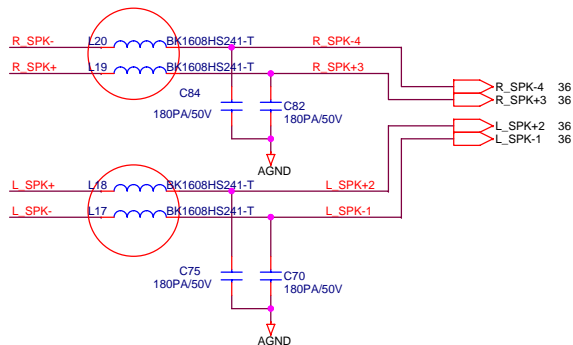
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



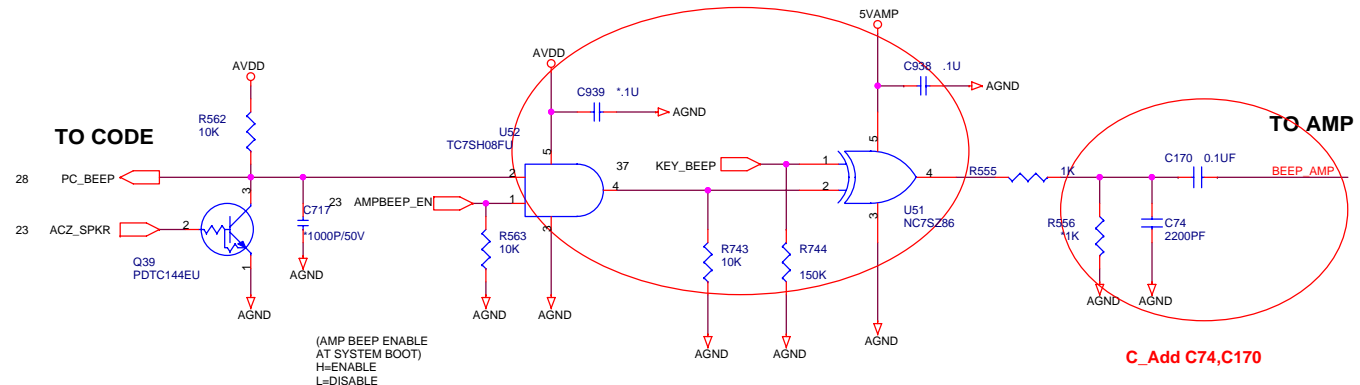
INT. SPEAKER

C12: change L17,L18,L19,L20 value to 240 Ohm



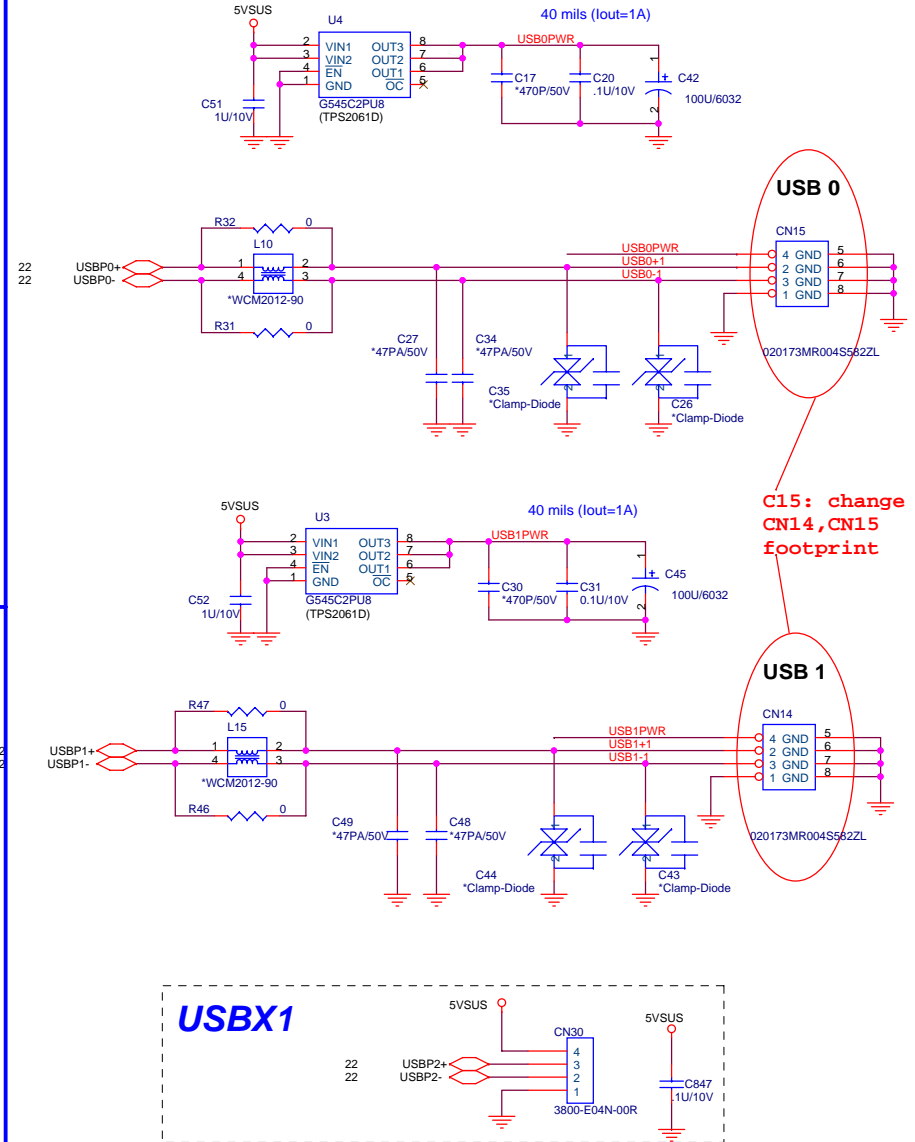
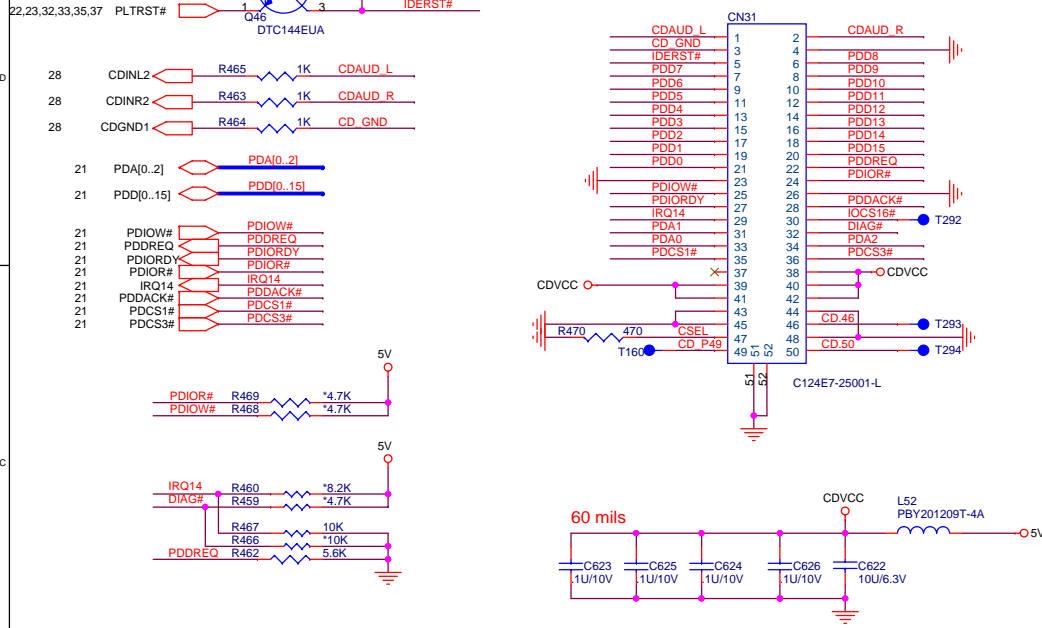
PCSPK BEEP

C13: Del Q57,R715,R554,C714 Add C938,U51,R774,R743,U52,C939,R563

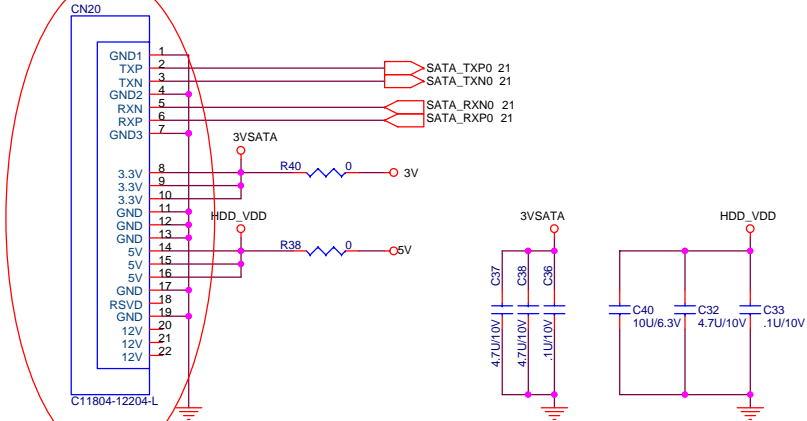


CD-ROM

USB2



SATA_1 CONNECTOR



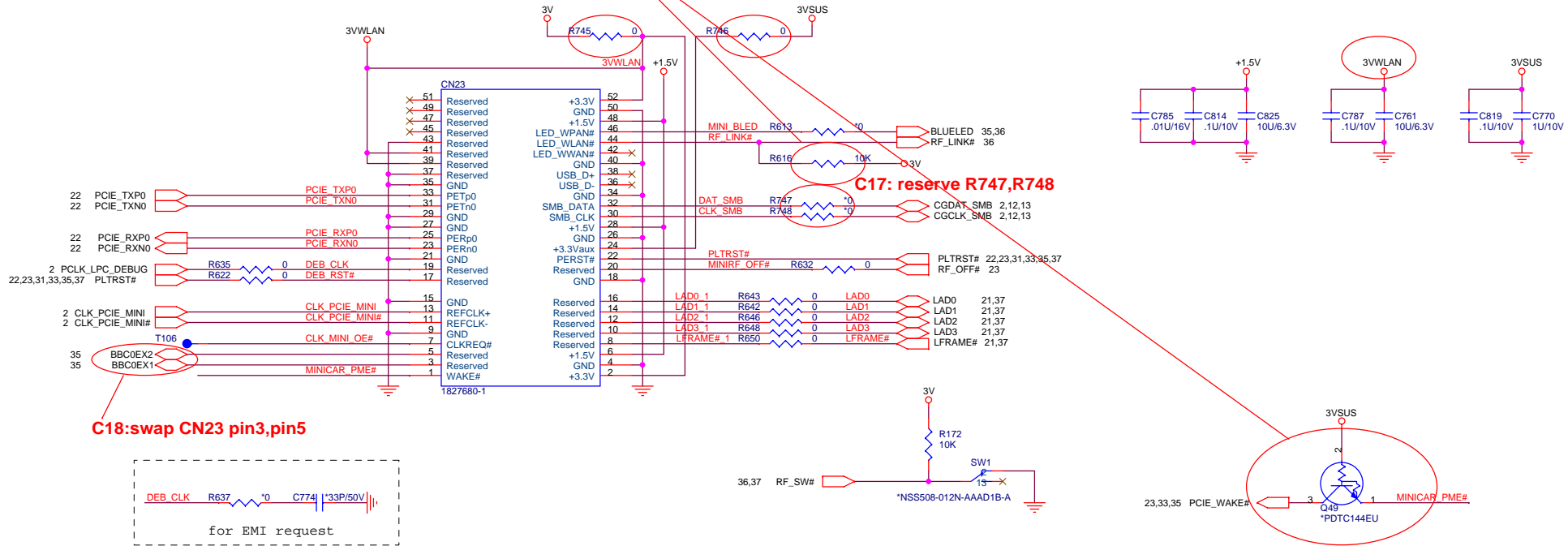
C14: change CN20 footprint

C15: change CN14, CN15 footprint

Mini PCI-E Card 1 WLAN

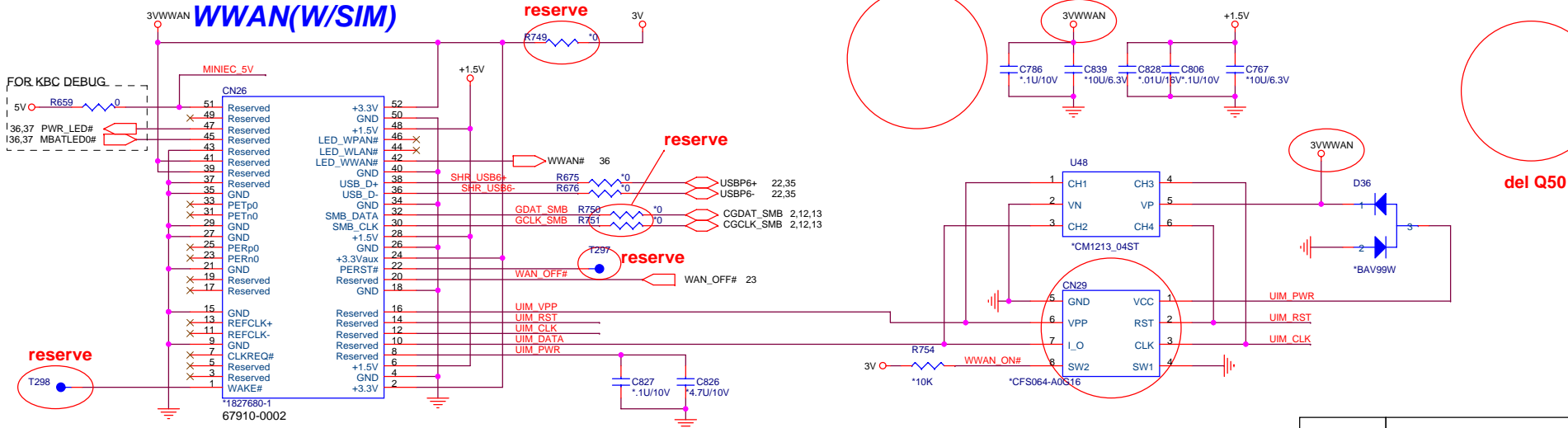
C16: Add Bom R745(RC1206) R746(RC0603) and R616
Del Q49

32



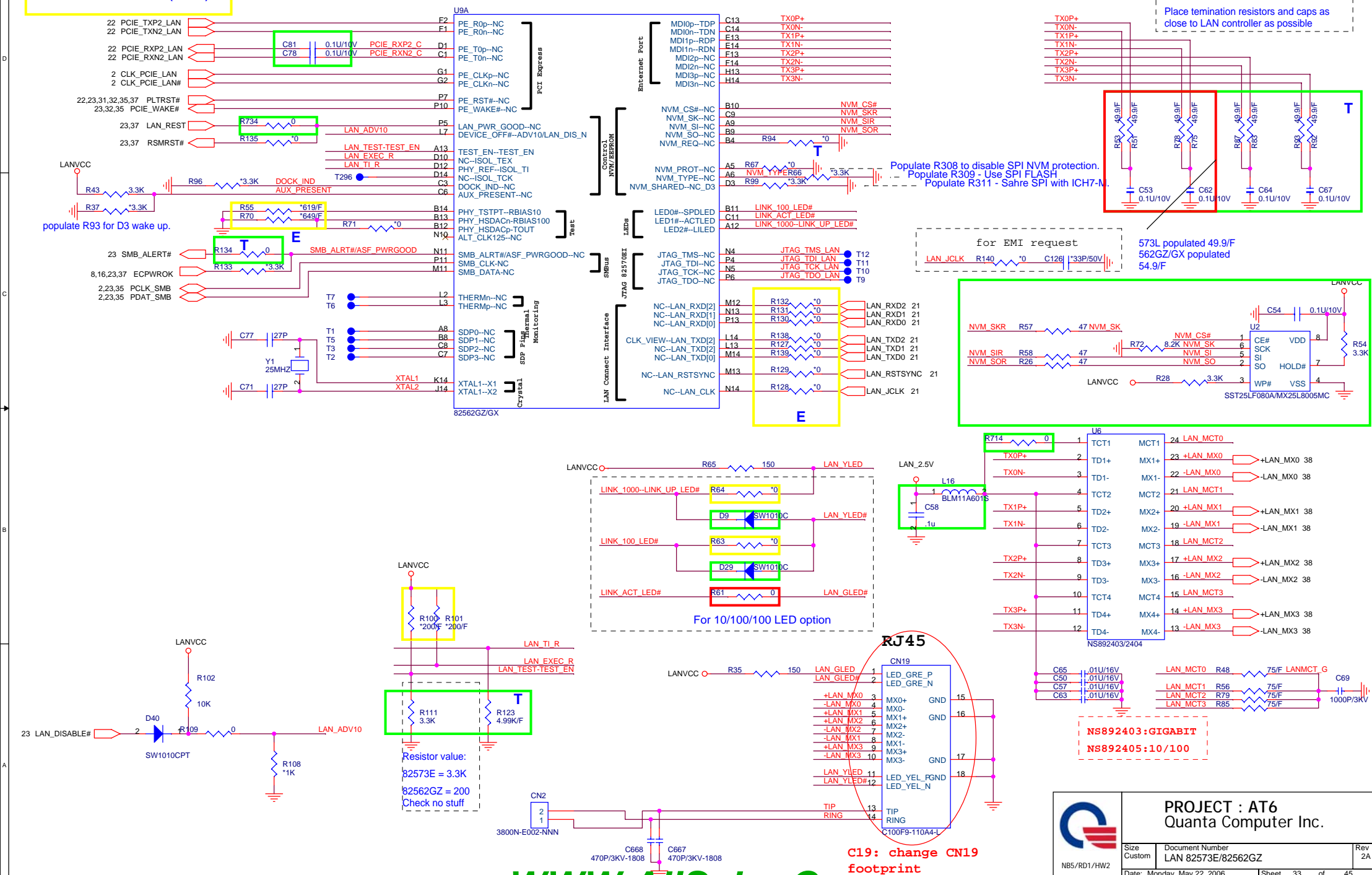
Mini PCI-E Card 2 WWAN(W/SIM)

del C771, C822



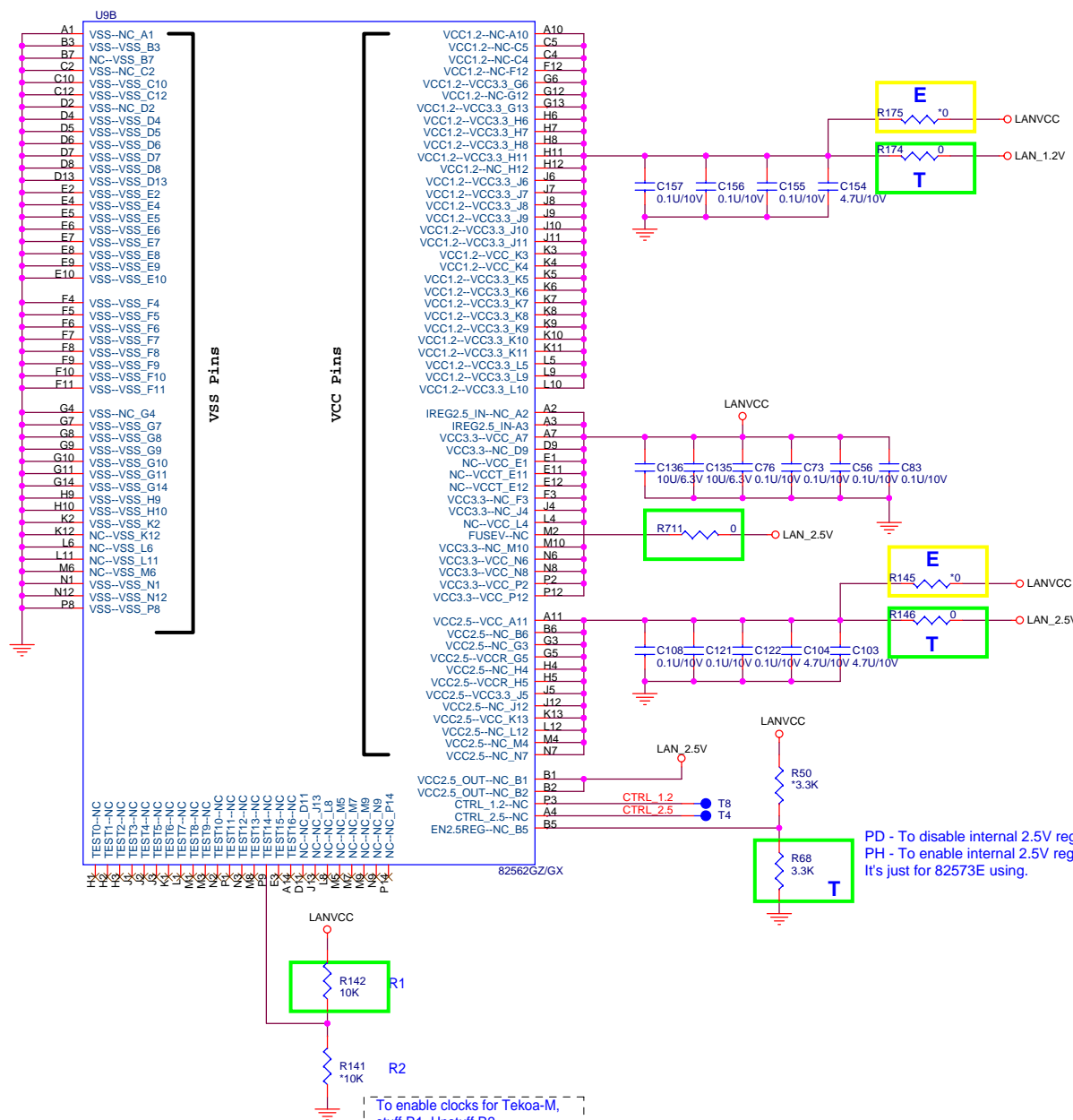
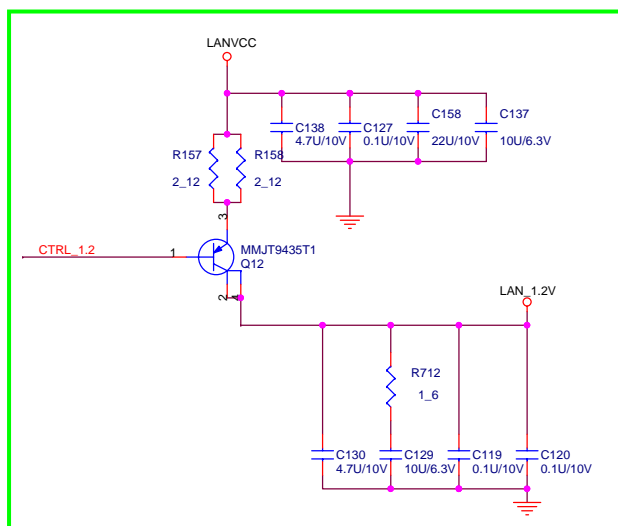
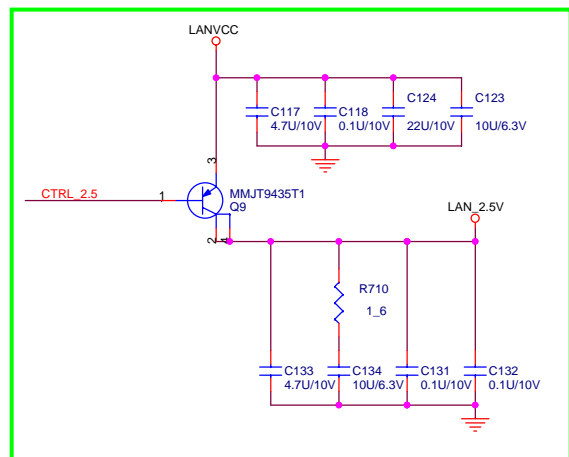
C. Change to P-TWO footprint.
SDCARD-CSF064-A0G16-1-8P

PROJECT : AT6 Quanta Computer Inc.		
Size Custom	Document Number MINI CARD X2	Rev 1A
Date: Monday, May 22, 2006	Sheet 32 of 45	

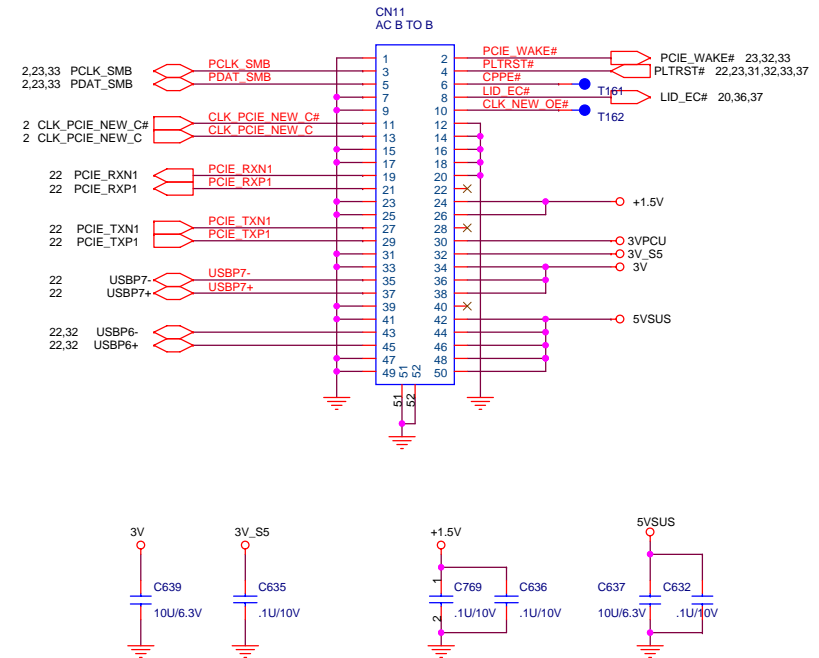
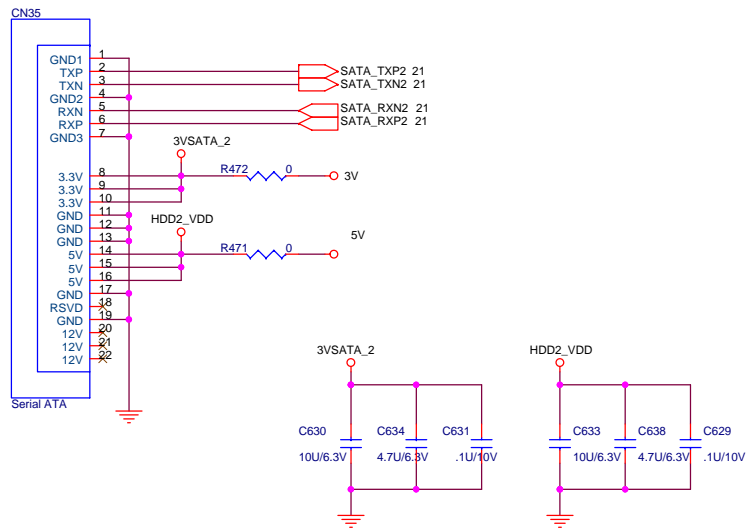


T : Stuffed for 82573L(10/100/1000)

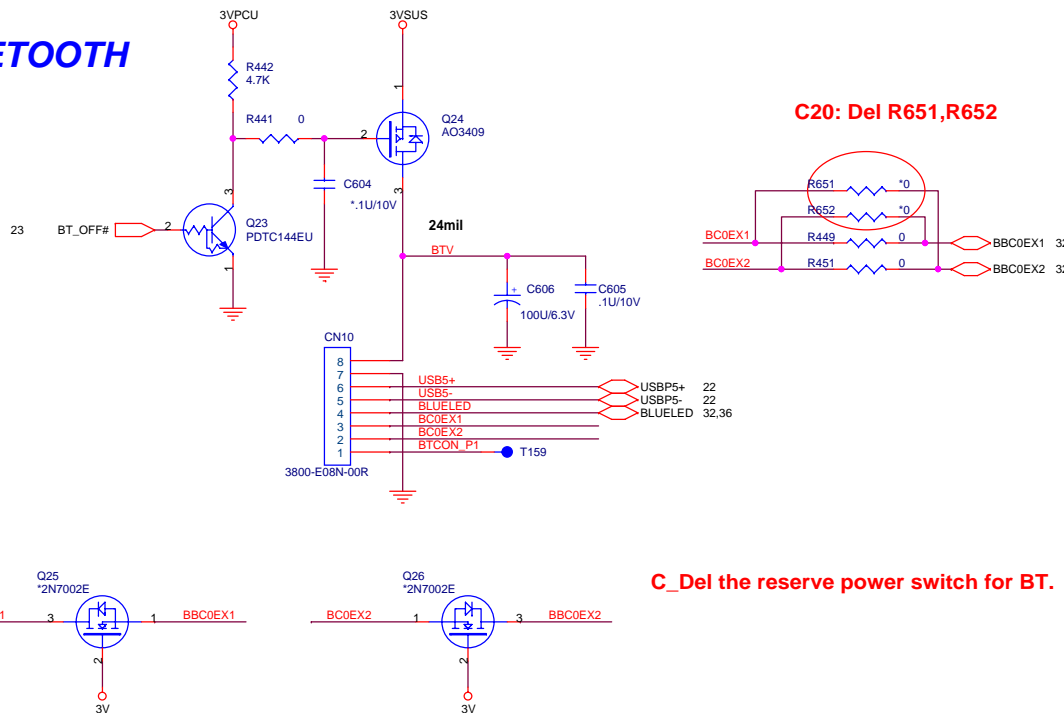
E : Stuffed for 8256GZ/GX(10/100)



PD - To disable internal 2.5V regulator.
PH - To enable internal 2.5V regulator.
It's just for 82573E using.

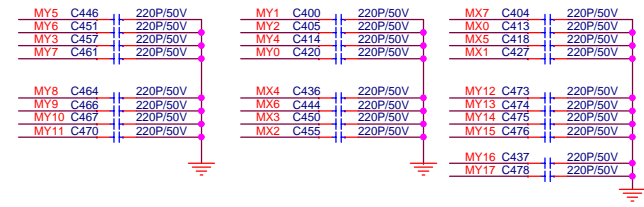
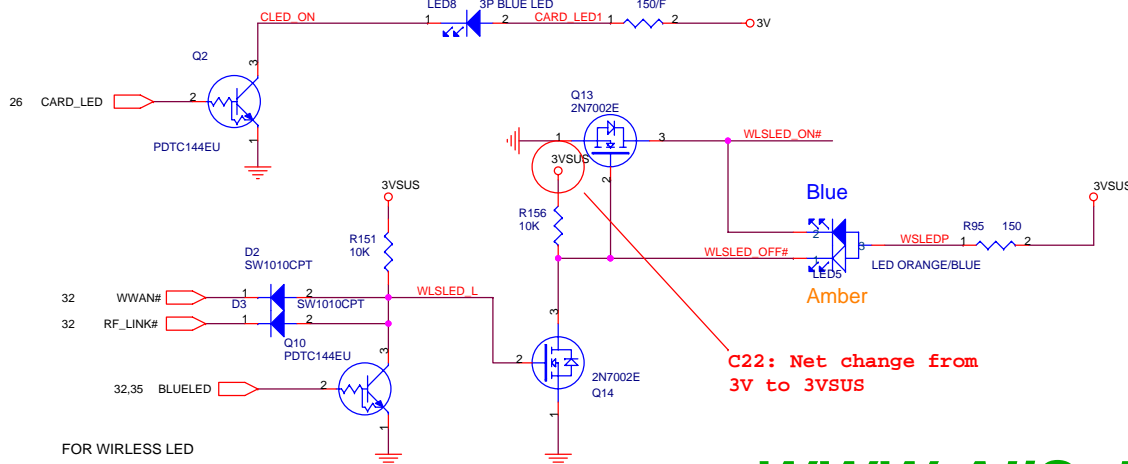
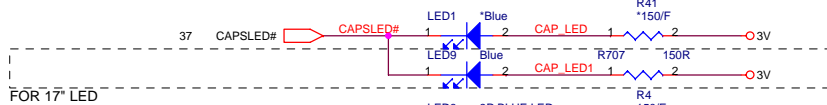
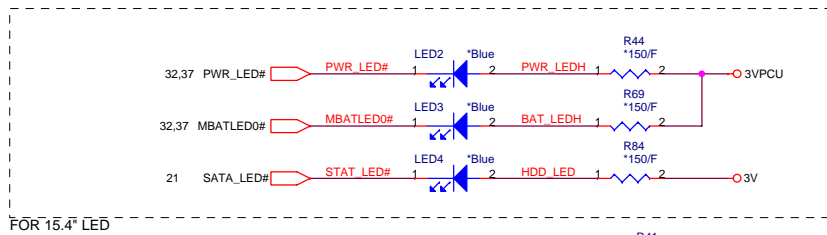
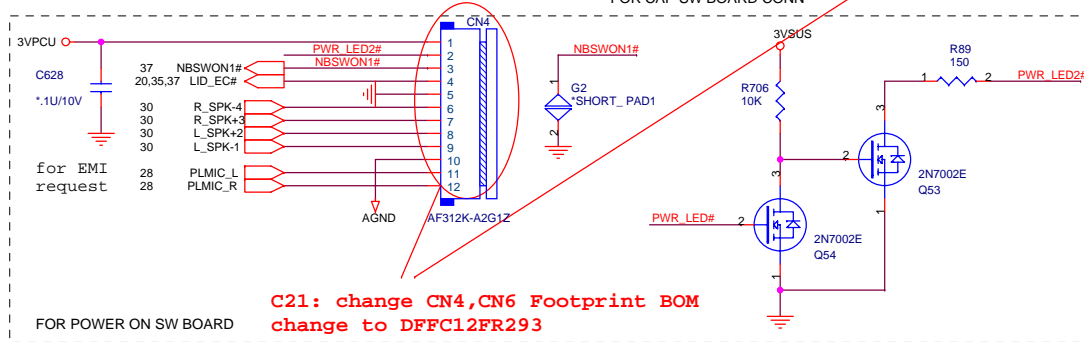
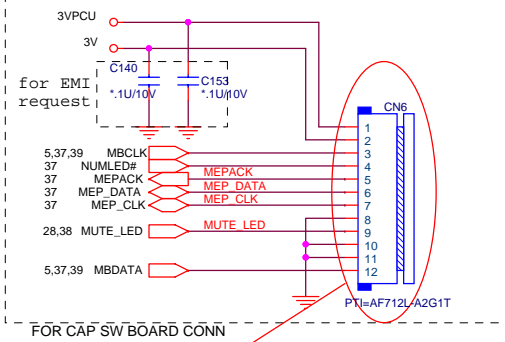
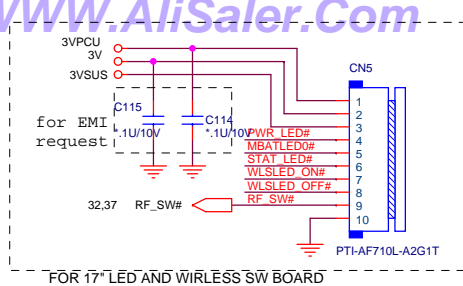


BLUETOOTH

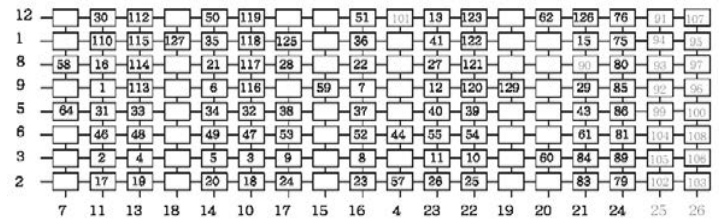
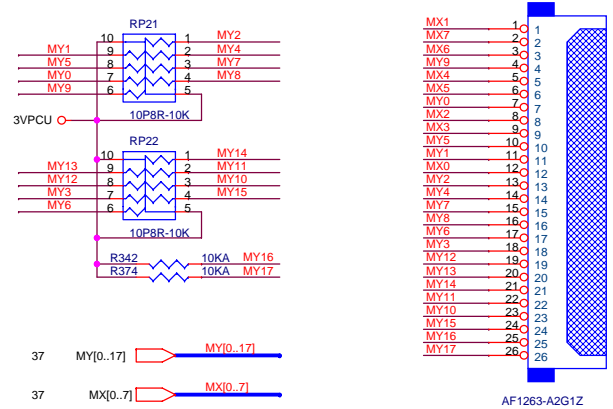


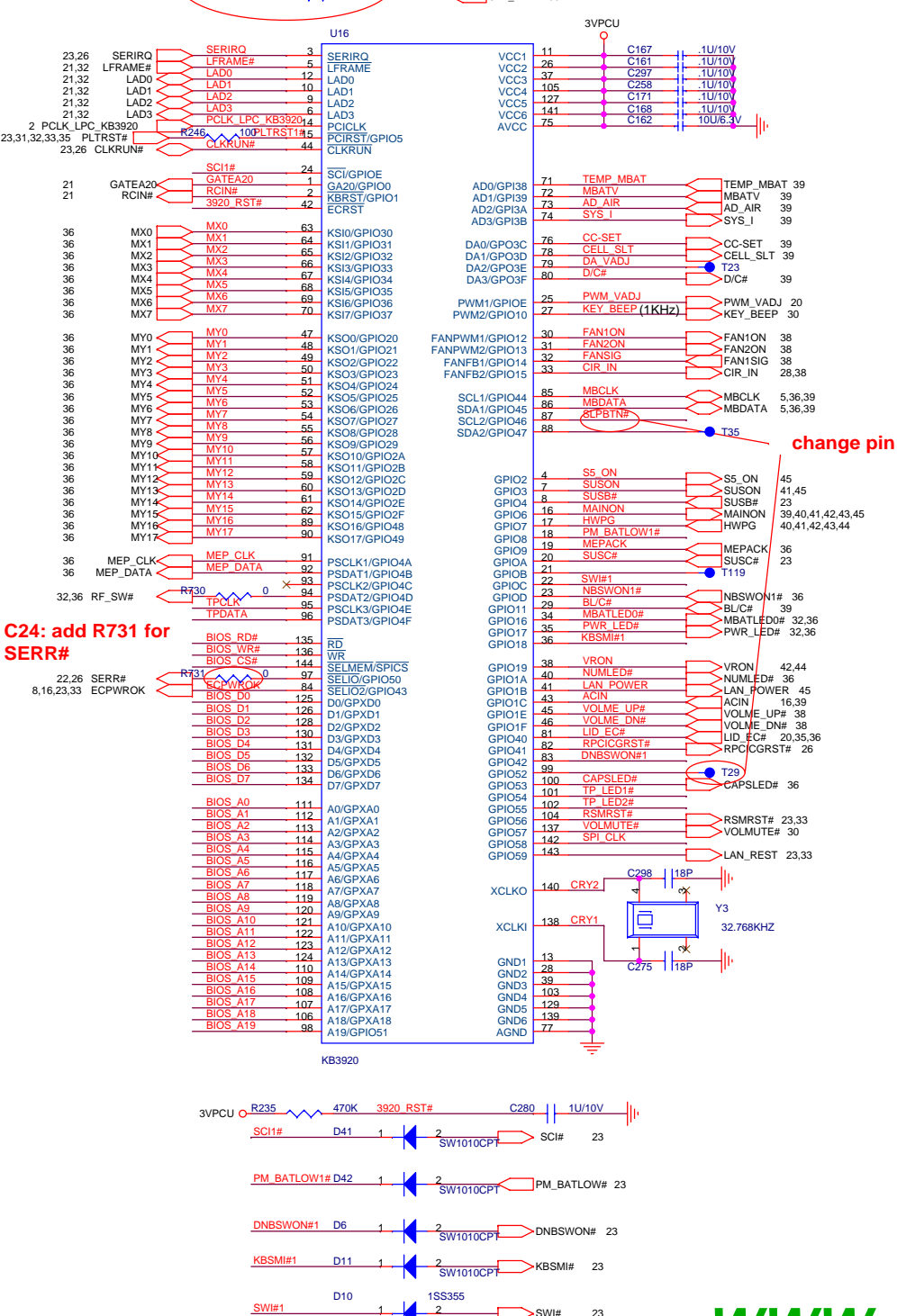
PROJECT : AT6
Quantia Computer Inc.

Size Custom	Document Number NEW CARD/BT	Rev 1A
Date: Monday, May 22, 2006	Sheet 35 of 45	



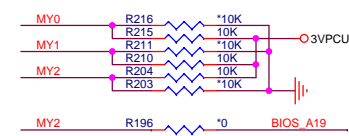
KEYBOARD PULL-UP



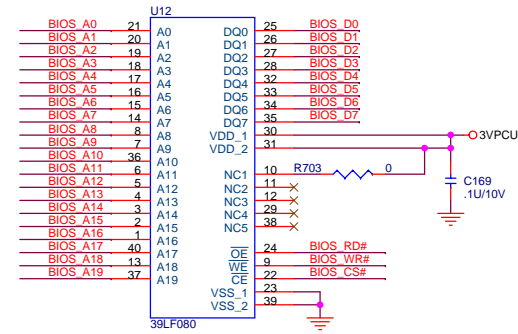


STRAP PIN

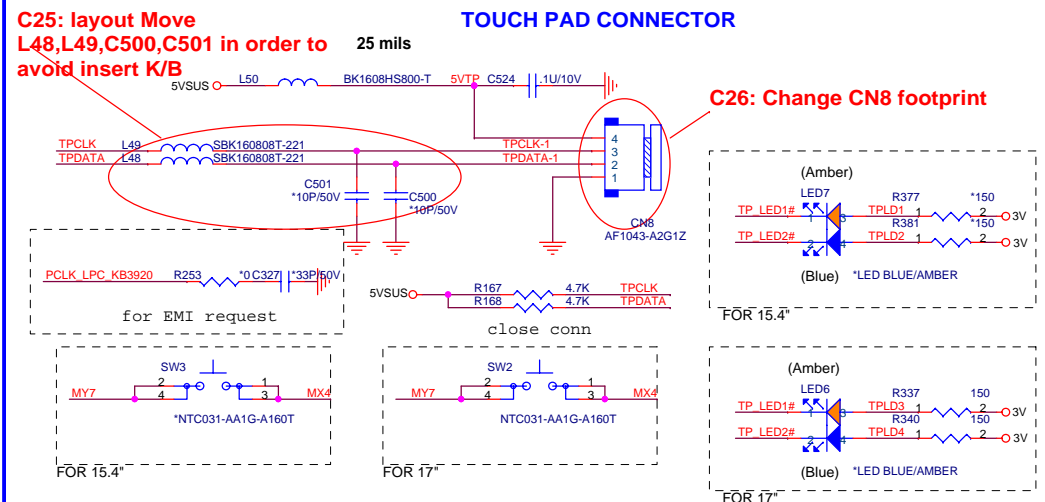
MY0	47	TP_TEST: Clock Test Mode Low: Test Mode HIGH: 32kHz clock in normal running
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



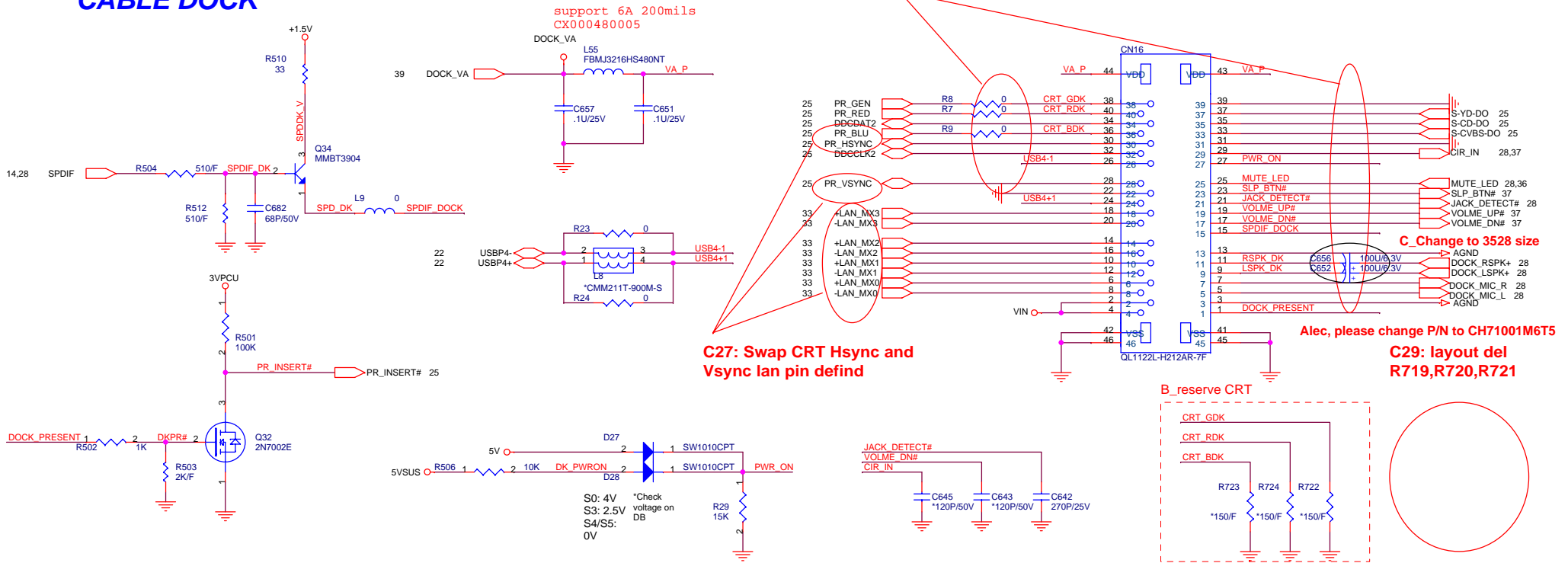
BIOS 1M FLASH ROM



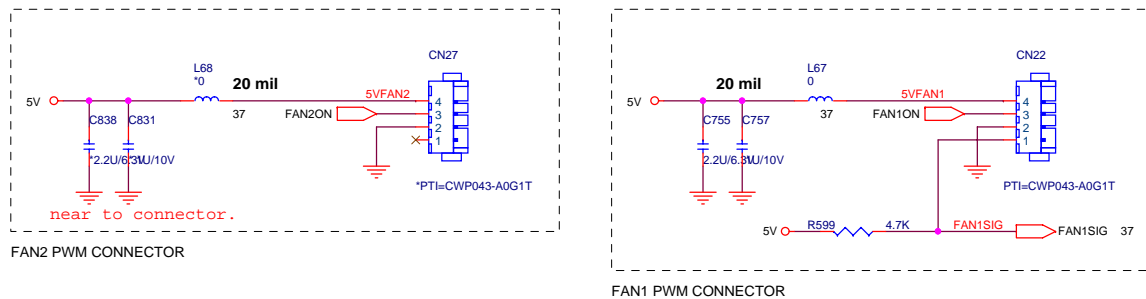
TOUCH PAD CONNECTOR



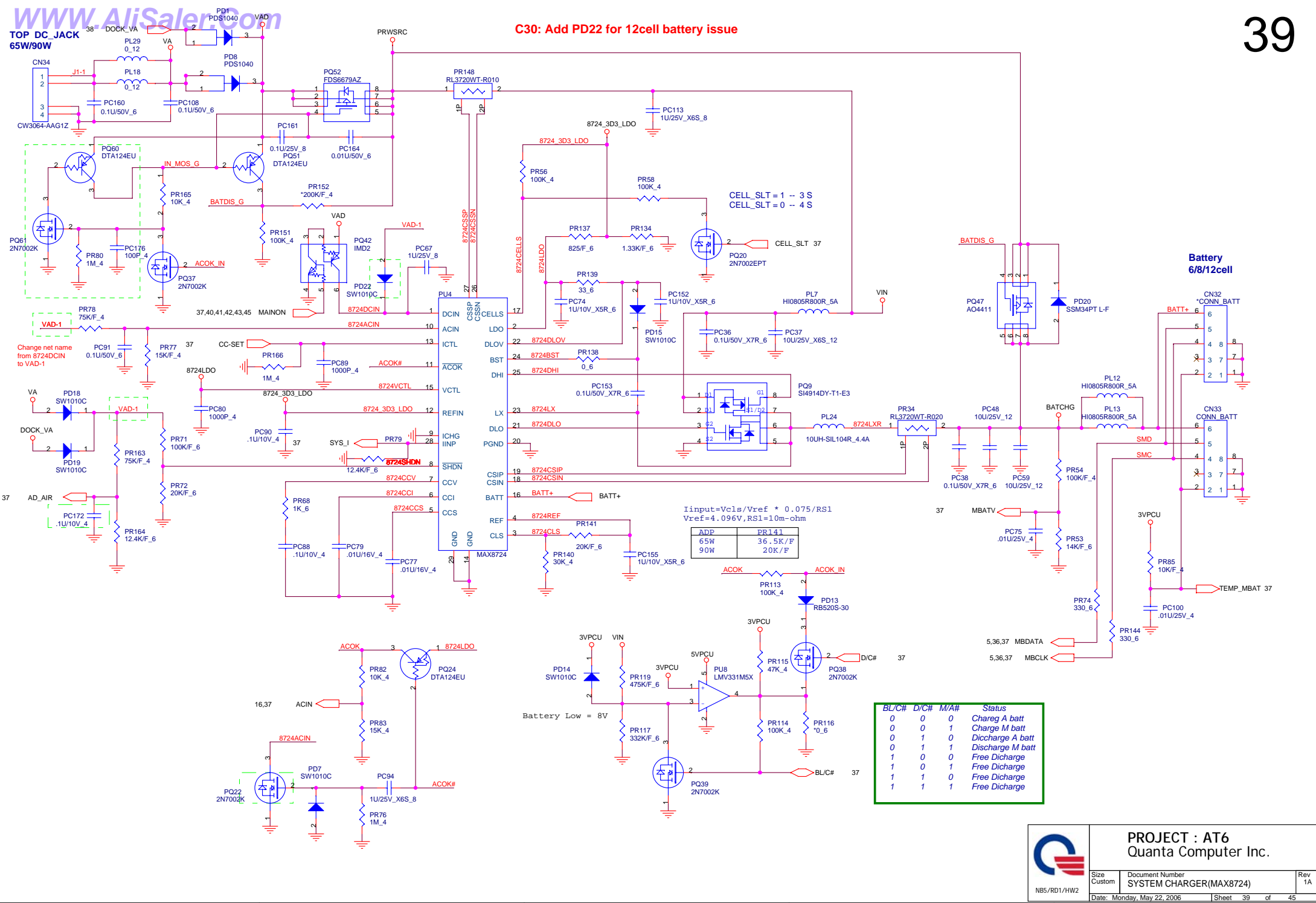
CABLE DOCK



FAN



C30: Add PD22 for 12cell battery issue



BL/C#	D/C#	M/A#	Status
0	0	0	Charge A batt
0	0	1	Charge M batt
0	1	0	Discharge A batt
0	1	1	Discharge M batt
1	0	0	Free Discharge
1	0	1	Free Discharge
1	1	0	Free Discharge
1	1	1	Free Discharge

PROJECT : AT6
Quanta Computer Inc.

Size Custom

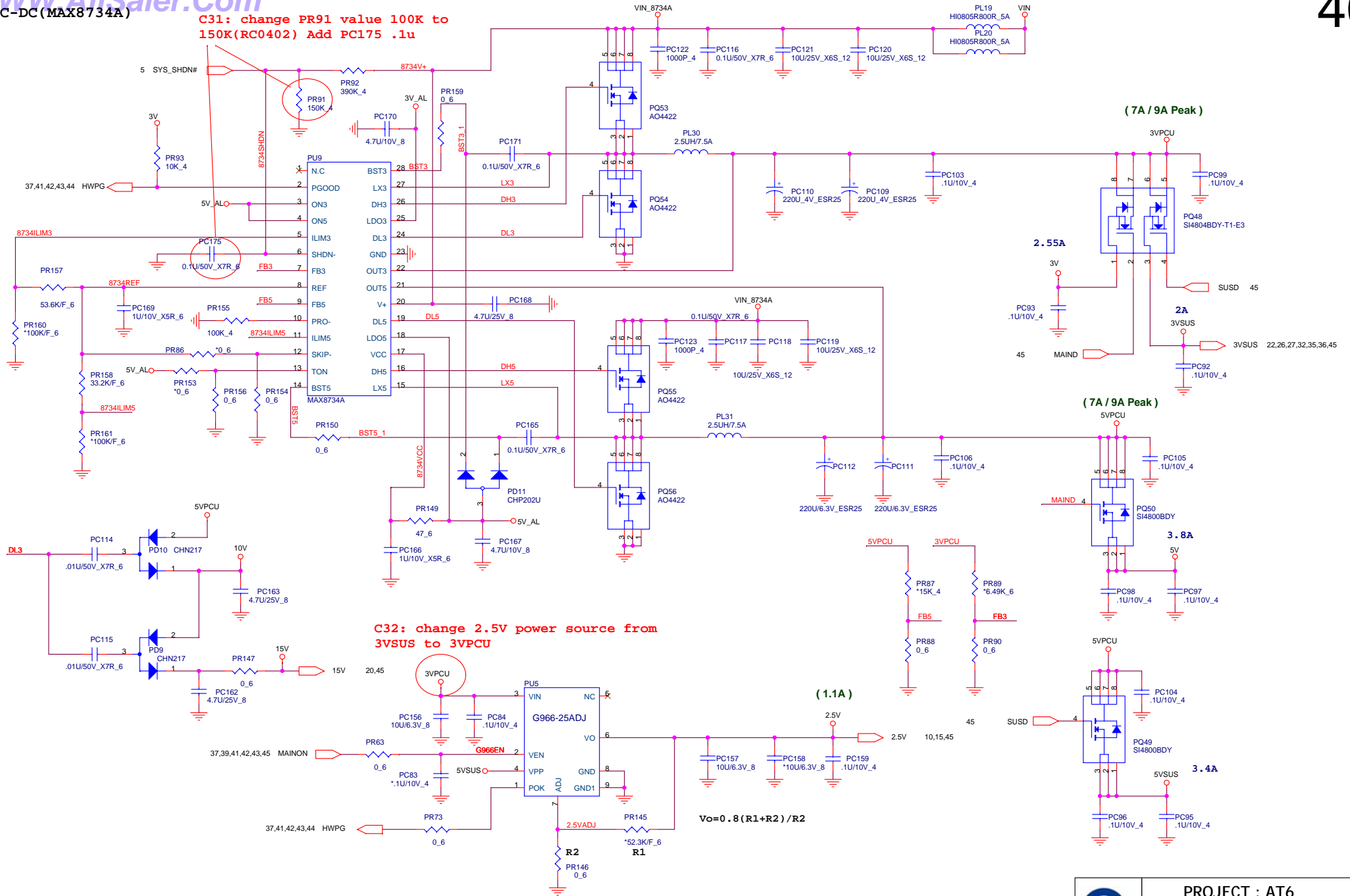
Document Number
SYSTEM CHARGER(MAX8724)

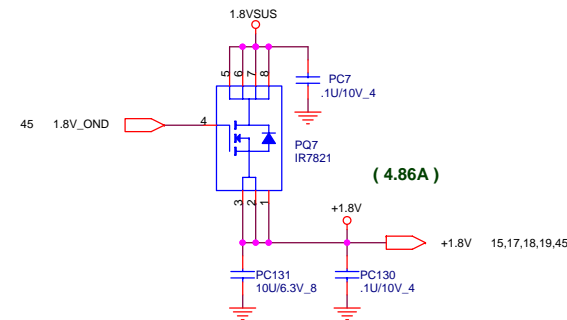
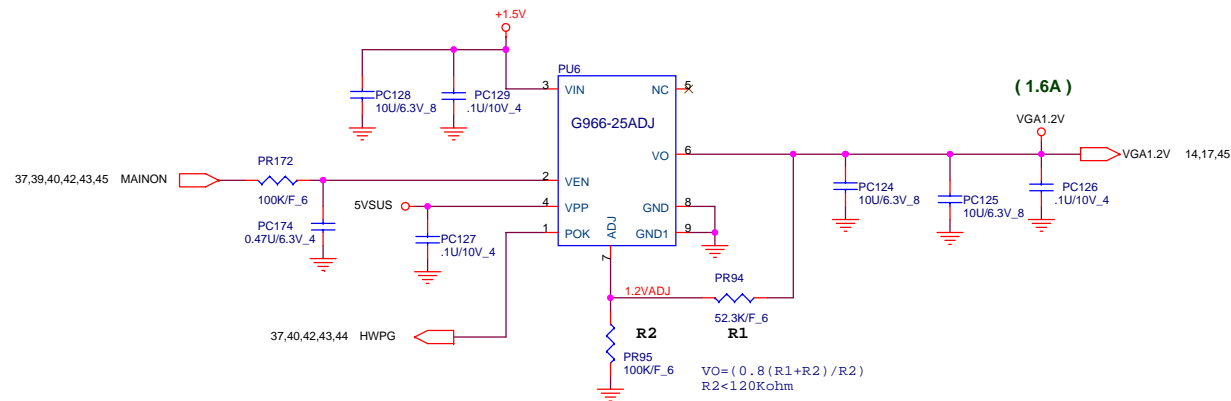
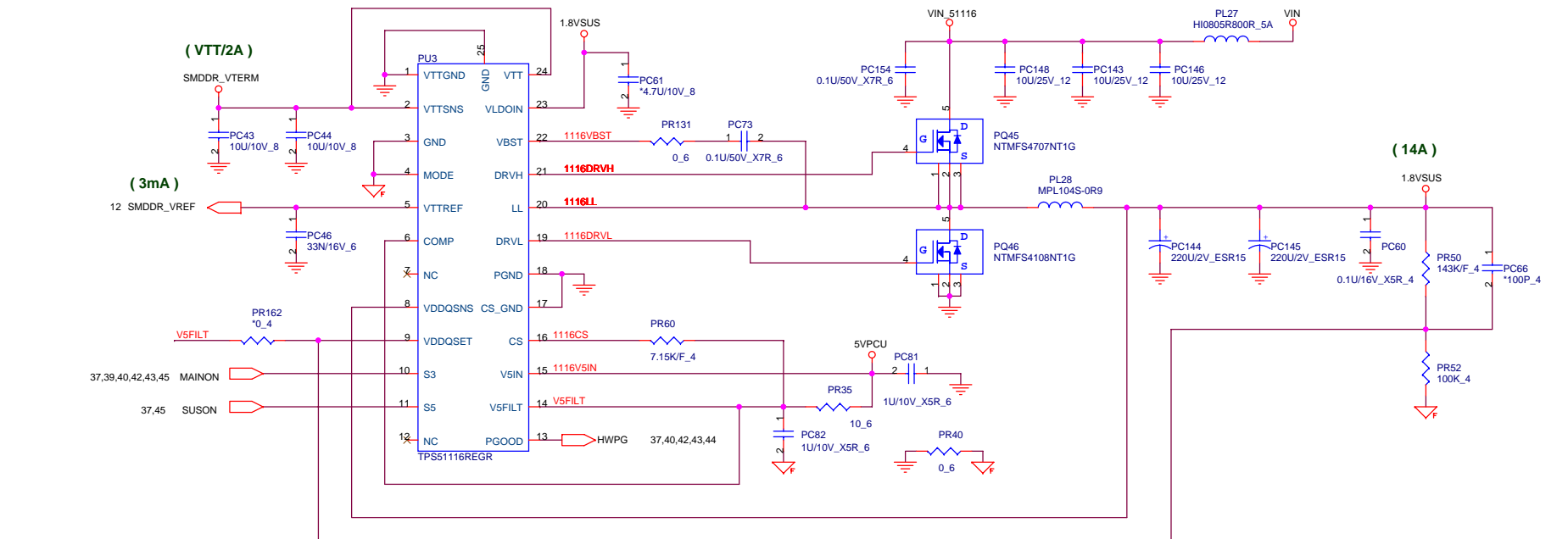
Date: Monday, May 22, 2006

Rev 1A

Sheet 39 of 45

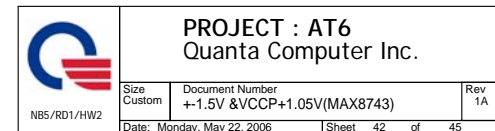
C31: change PR91 value 100K to 150K(RC0402) Add PC175 .1u

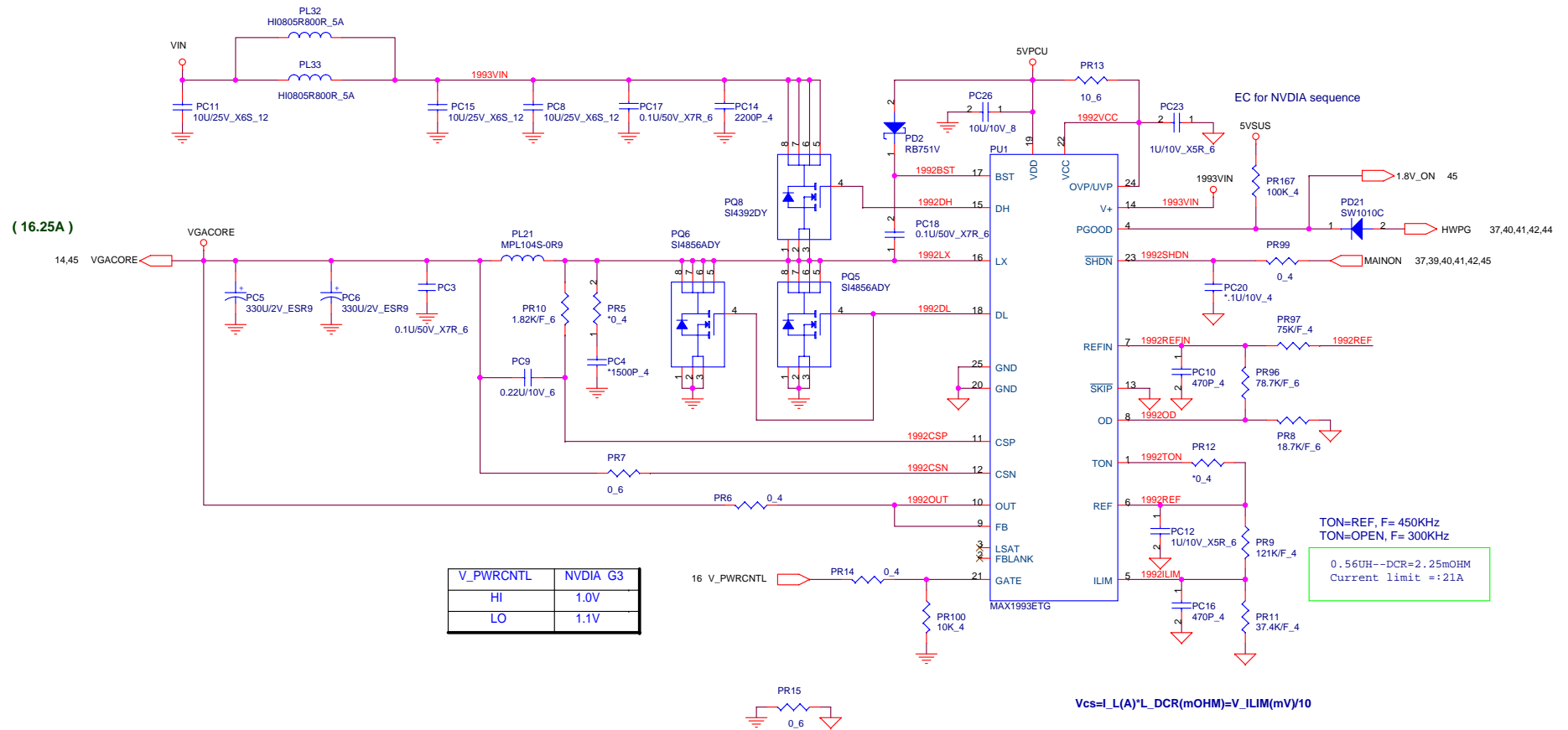


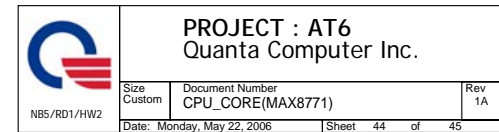


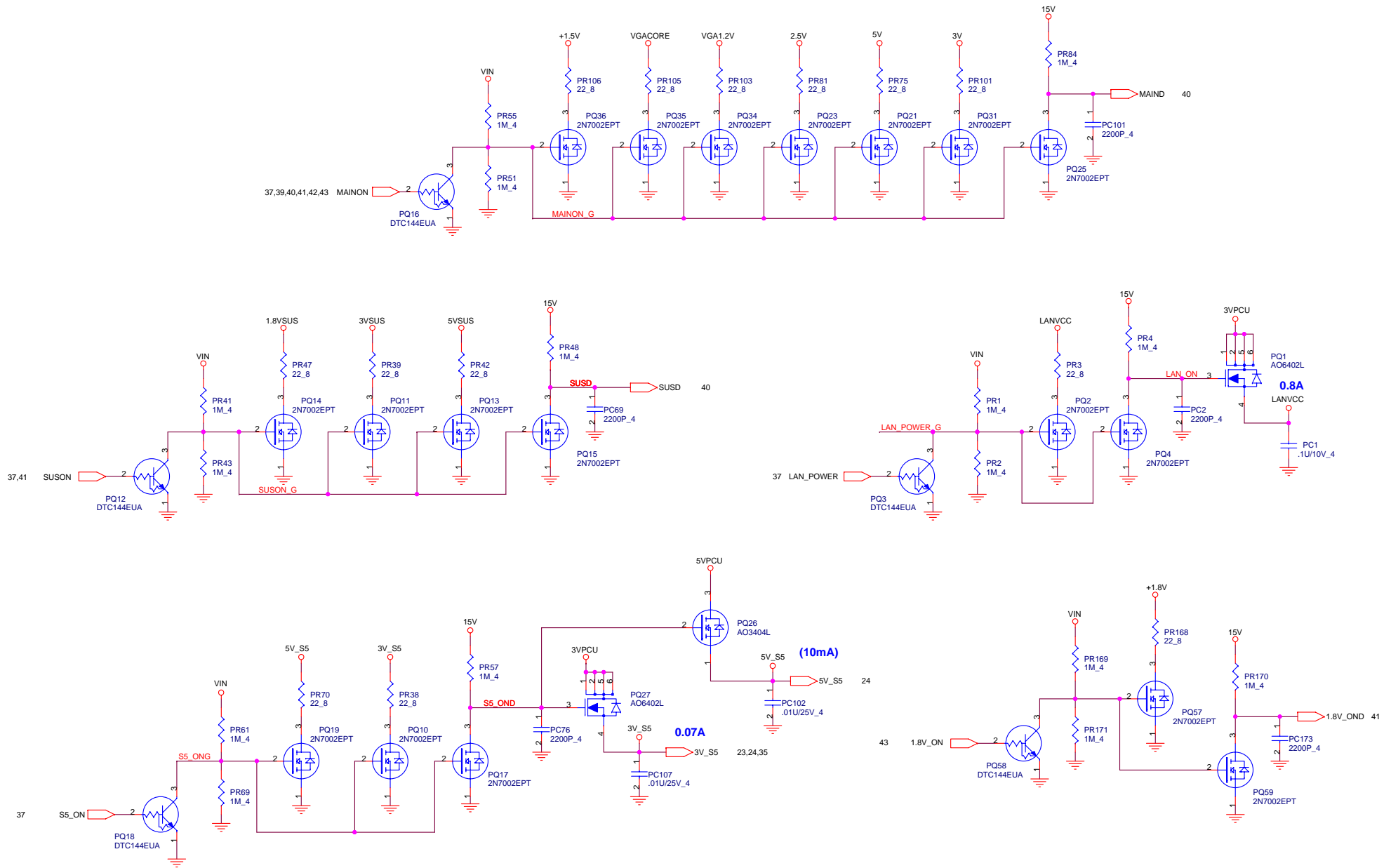
PROJECT : AT6
Quanta Computer Inc.


Size Custom	Document Number DDRII 1.8VSUS/SMDDR_VTERM	Rev 2A
Date: Monday, May 22, 2006	Sheet 41 of 45	









		PROJECT : AT6 Quanta Computer Inc.	
		Size Custom Document Number DISCHARGE	Rev 2A
NB5/RD1/HW2		Date: Monday, May 22, 2006	Sheet 45 of 45