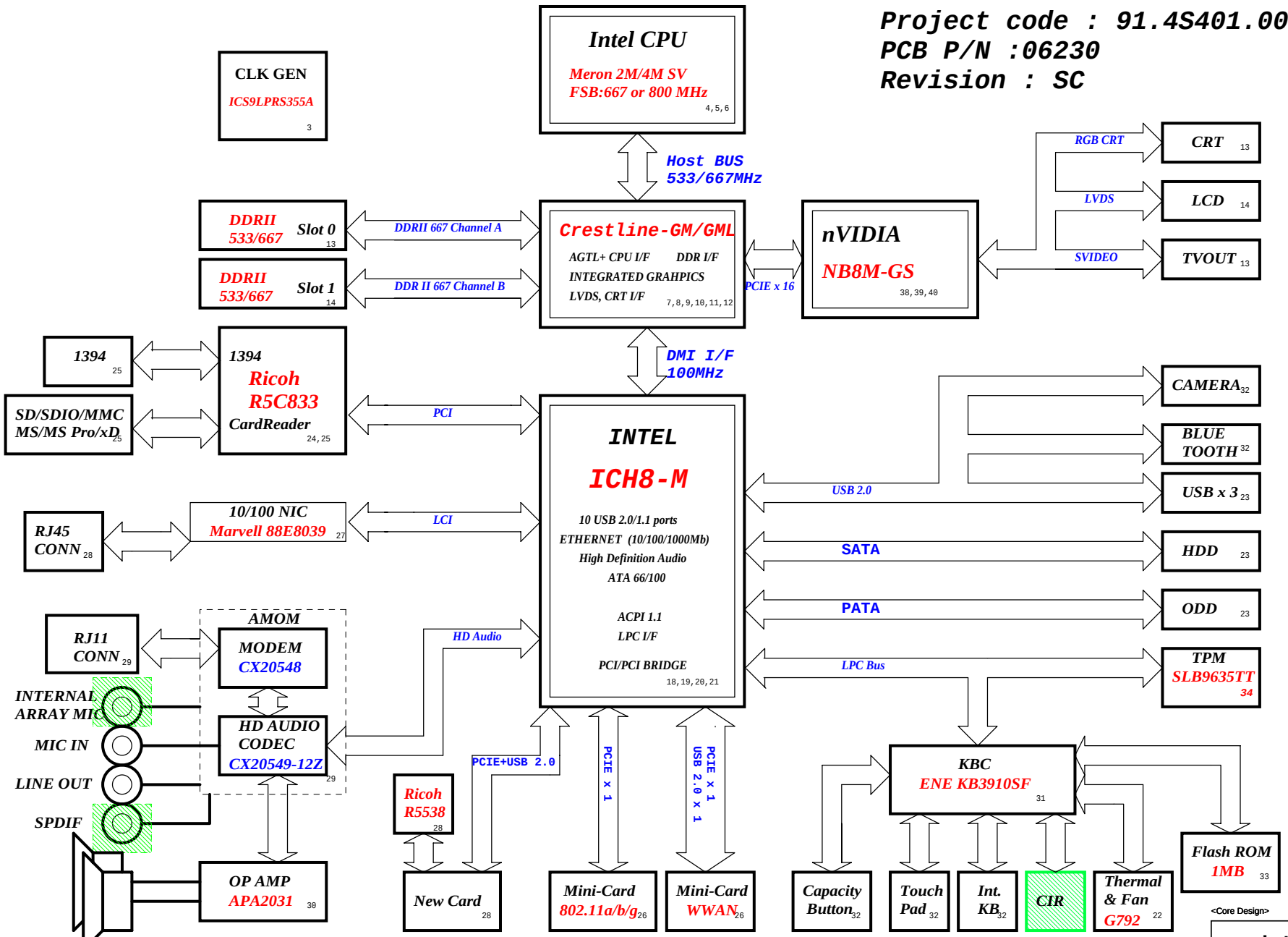
Pamirs-Discrete Block Diagram

Project code : 91.4S401.001
PCB P/N :06230
Revision : SC



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC FAN5234	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0 11A

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: VCC
L7: Signal 4
L8: Signal 5
L9: GND
L10: Signal 5

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size	Document Number	Rev
A3	Pamirs-Discrete	SC

Date: Monday, December 18, 2006 Sheet 1 of 47

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable; high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule; High=No Reboot

8.2K PULL HIGH

19,21 +RTCVCC → +RTCVCC
4,5,6,7,9,10,11,19,21,37,47 1D05V_S0 → 1D05V_S0
3,7,10,21,38 1D25V_S0 → 1D25V_S0
27 1D2V_LAN_S5 → 1D2V_LAN_S5
28 1D5V_NEW_S0 → 1D5V_NEW_S0
5,10,17,19,20,21,26,28,38,47 1D5V_S0 → 1D5V_S0
7,10,11,13,14,34,37,38 1D8V_S3 → 1D8V_S3
27,28 2D5V_LAN_S5 → 2D5V_LAN_S5
29,30 3D3V_AUD_S0 → 3D3V_AUD_S0
19,31,32,33,36,39,46 3D3V_AUX_S5 → 3D3V_AUX_S5
27,28 3D3V_LAN_S5 → 3D3V_LAN_S5
3,4,7,10,11,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36,40,41,42,43,47 3D3V_S0 → 3D3V_S0
17,18,20,21,22,26,27,28,29,31,34,36,39,47 3D3V_S5 → 3D3V_S5
22,26,29,31,34,36 5V_AUX_S5 → 5V_AUX_S5
16,23,32,33,34,36,37,38 5V_S3 → 5V_S3
15,16,17,20,21,22,23,29,30,31,32,33,34,35,47 5V_S0 → 5V_S0
16,21,34,37,40 5V_S5 → 5V_S5
17,39,46,47 AD+ → AD+
16,17,34,35,36,37,39,40,47 DCBATOUT → DCBATOUT
13,14,38 DDR_VREF_S0 → DDR_VREF_S0
7,13,14,38 DDR_VREF_S3 → DDR_VREF_S3
22,31,33,39 KBC_3D3V_AUX → KBC_3D3V_AUX
16 LCDVDD_S0 → LCDVDD_S0
5,6,35 VCC_CORE_S0 → VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
SI_[illegible]	[illegible]

<Core Design>

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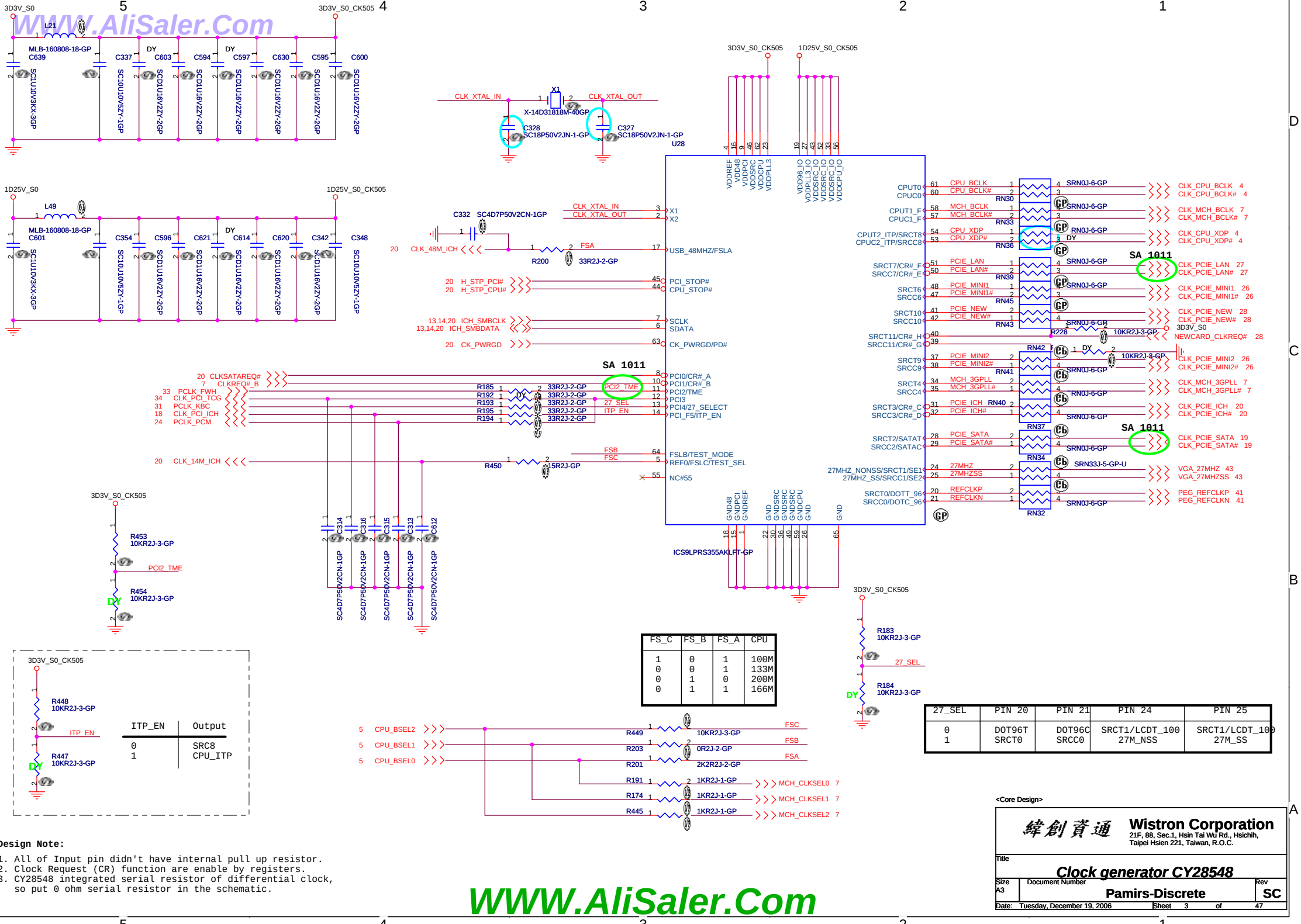

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

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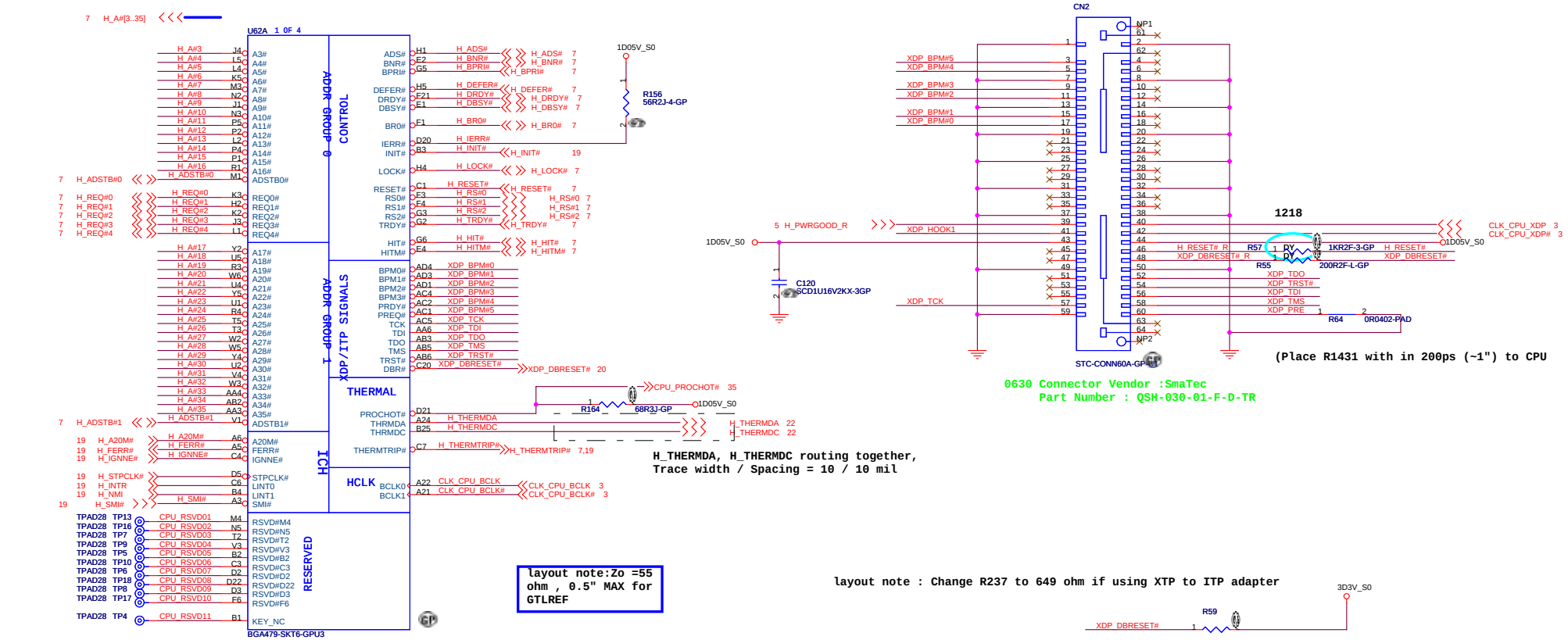
Title: Clock generator CY28548

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

Date: Tuesday, December 19, 2006 | Sheet 3 of 47

XDP Connector



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Meron(1/3)-AGTL+/XDP

Size: Custom | Document Number: Pamirs-Discrete | Rev: SC

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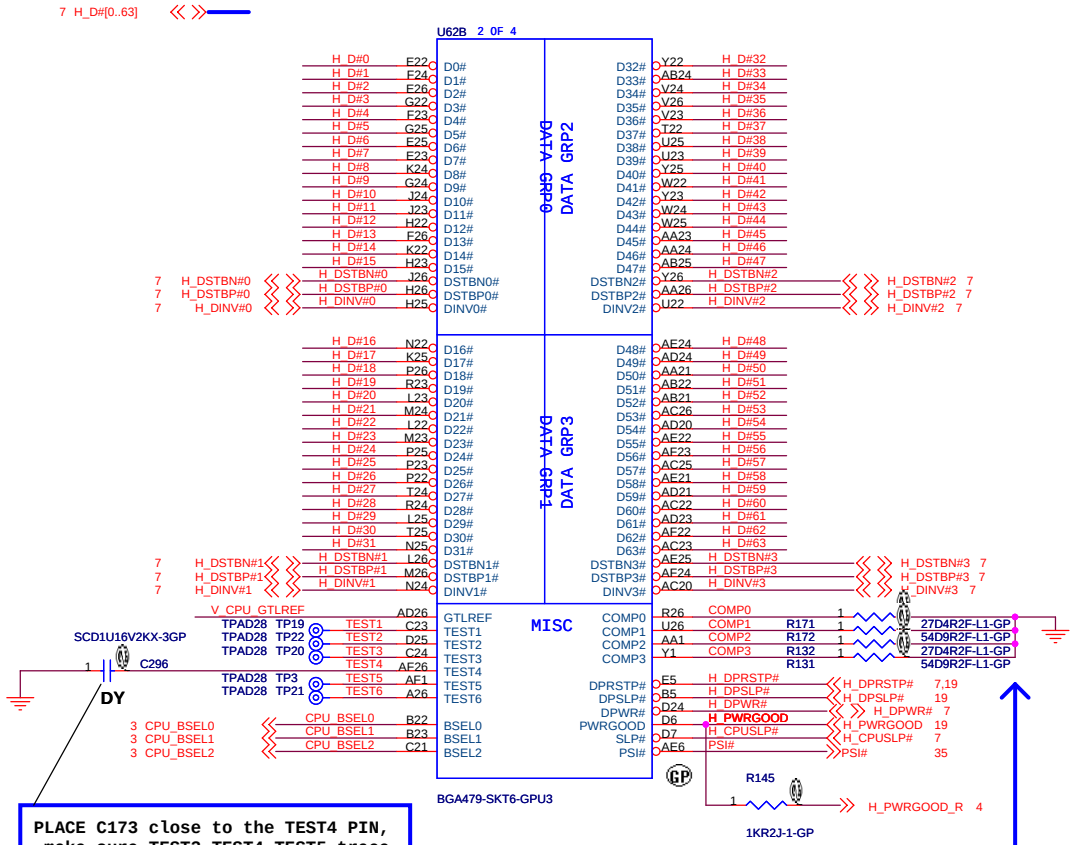
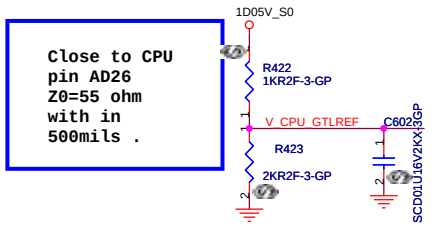


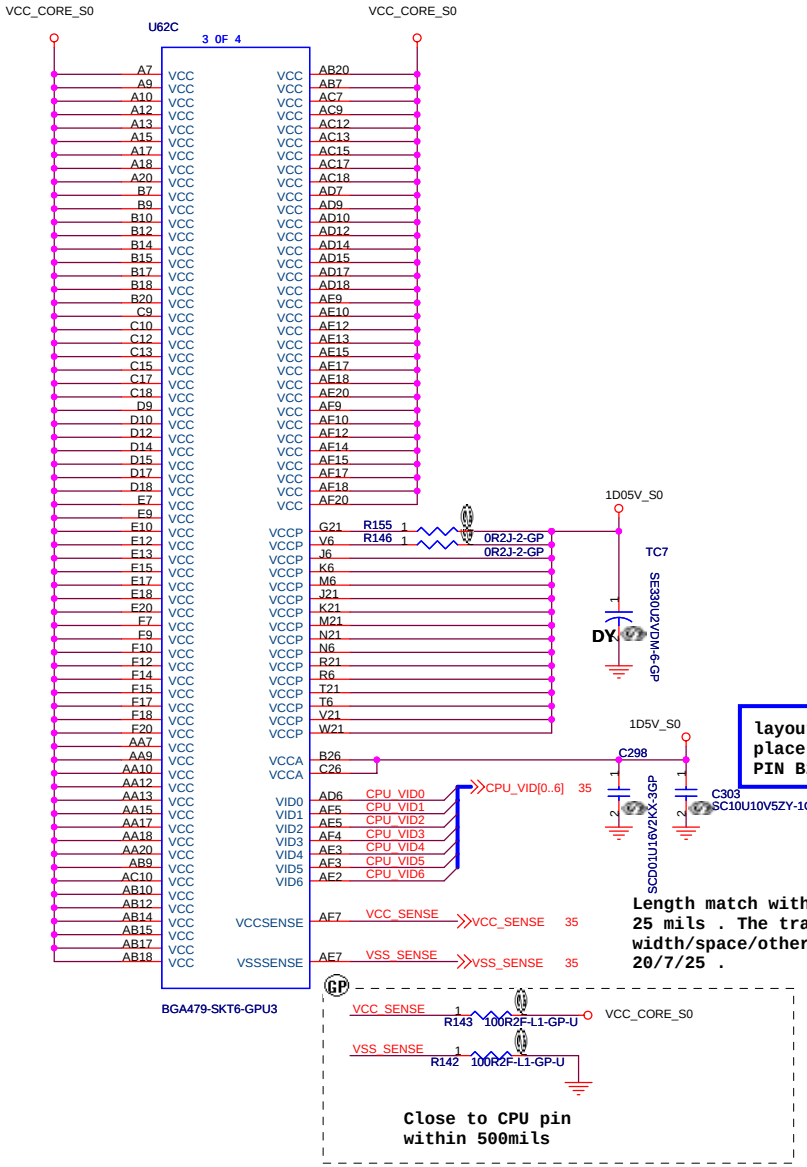
PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal . COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0



Close to CPU pin AD26 Z0=55 ohm with in 500mils .



layout note: place C3 near PIN B26

Length match within 25 mils . The trace width/space/other is 20/7/25 .

Close to CPU pin within 500mils

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Title: Meron(2/3)-AGTL+/PWR

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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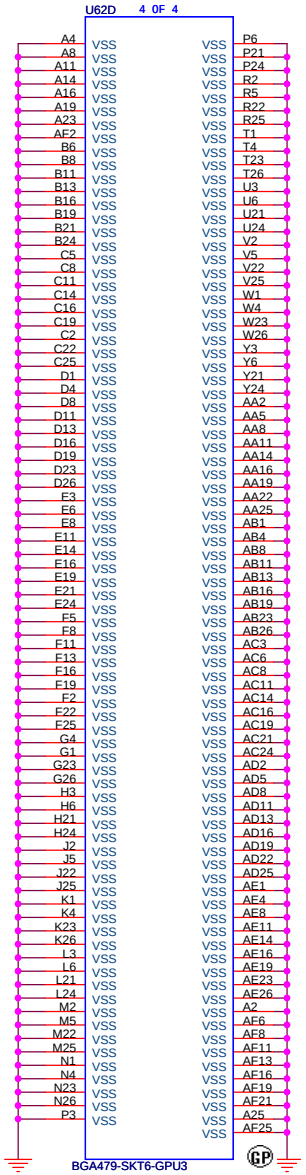
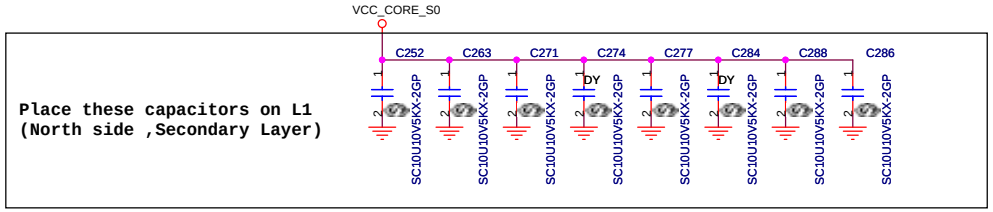
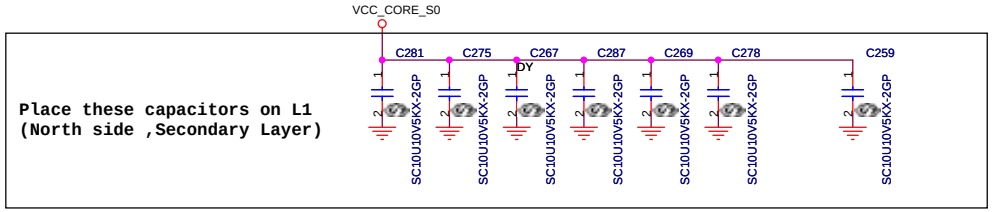
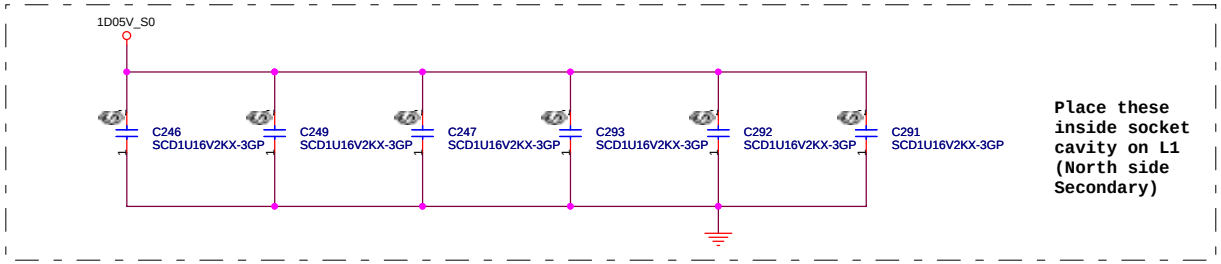






Mid Frequencd Decoupling



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Meron(3/3)-GND&Bypass

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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FOR Calero: 80.6 ohm
Crestline: 20 ohm

U23A 1 OF 10 — HOST

U23B 2 OF 10 — RSVD, DDR MUXING, CLK, DMI, CFG, GRAPHICS VID, PM, ME, NC, MISC

CRESTLINE-GP-U

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

From Astro demo schematic

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

Layout Note :
Place C151 within 100 mils of NB

Layout Note :
Place C153 near pin B3 of NB

SA 0928

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Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size: Custom | Document Number: Pamirs-Discrete | Rev: SA

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DDR_A_D[0..63] 13
DDR_A_BS[0..2] 13
DDR_A_DM[0..7] 13
DDR_A_DQS[0..7] 13
DDR_A_DQS#[0..7] 13
DDR_A_MA[0..13] 13

U23D 4 OF 10

DDR SYSTEM MEMORRY A

DDR_A_D0	AR43	SA_DQ0	SA_BS0	BB19	DDR_A_BS0
DDR_A_D1	AW44	SA_DQ1	SA_BS1	BK19	DDR_A_BS1
DDR_A_D2	BA45	SA_DQ2	SA_BS2	BF29	DDR_A_BS2
DDR_A_D3	AY46	SA_DQ3			
DDR_A_D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR_A_CAS#
DDR_A_D5	AR45	SA_DQ5			
DDR_A_D6	AT42	SA_DQ6	SA_DM0	AT45	DDR_A_DM0
DDR_A_D7	AW47	SA_DQ7	SA_DM1	BD44	DDR_A_DM1
DDR_A_D8	BB45	SA_DQ8	SA_DM2	BD42	DDR_A_DM2
DDR_A_D9	BF48	SA_DQ9	SA_DM3	AW38	DDR_A_DM3
DDR_A_D10	BG47	SA_DQ10	SA_DM4	AW13	DDR_A_DM4
DDR_A_D11	BJ45	SA_DQ11	SA_DM5	BG8	DDR_A_DM5
DDR_A_D12	BB47	SA_DQ12	SA_DM6	AY5	DDR_A_DM6
DDR_A_D13	BG50	SA_DQ13	SA_DM7	AN6	DDR_A_DM7
DDR_A_D14	BH49	SA_DQ14			
DDR_A_D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR_A_DQS0
DDR_A_D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR_A_DQS1
DDR_A_D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR_A_DQS2
DDR_A_D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR_A_DQS3
DDR_A_D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR_A_DQS4
DDR_A_D20	BF44	SA_DQ20	SA_DQS5	BH6	DDR_A_DQS5
DDR_A_D21	BH45	SA_DQ21	SA_DQS6	BB2	DDR_A_DQS6
DDR_A_D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR_A_DQS7
DDR_A_D23	BF40	SA_DQ23	SA_DQS#0	AT47	DDR_A_DQS#0
DDR_A_D24	AR40	SA_DQ24	SA_DQS#1	BD47	DDR_A_DQS#1
DDR_A_D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR_A_DQS#2
DDR_A_D26	AT39	SA_DQ26	SA_DQS#3	BA37	DDR_A_DQS#3
DDR_A_D27	AW36	SA_DQ27	SA_DQS#4	BA16	DDR_A_DQS#4
DDR_A_D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR_A_DQS#5
DDR_A_D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR_A_DQS#6
DDR_A_D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR_A_DQS#7
DDR_A_D31	AT38	SA_DQ31			
DDR_A_D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR_A_MA0
DDR_A_D33	AT13	SA_DQ33	SA_MA1	BD20	DDR_A_MA1
DDR_A_D34	AW11	SA_DQ34	SA_MA2	BK27	DDR_A_MA2
DDR_A_D35	AV11	SA_DQ35	SA_MA3	BH28	DDR_A_MA3
DDR_A_D36	AU15	SA_DQ36	SA_MA4	BL24	DDR_A_MA4
DDR_A_D37	AT11	SA_DQ37	SA_MA5	BK28	DDR_A_MA5
DDR_A_D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR_A_MA6
DDR_A_D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR_A_MA7
DDR_A_D40	BE10	SA_DQ40	SA_MA8	BL28	DDR_A_MA8
DDR_A_D41	BD10	SA_DQ41	SA_MA9	BA28	DDR_A_MA9
DDR_A_D42	BD8	SA_DQ42	SA_MA10	BC19	DDR_A_MA10
DDR_A_D43	AY9	SA_DQ43	SA_MA11	BE28	DDR_A_MA11
DDR_A_D44	BG10	SA_DQ44	SA_MA12	BG30	DDR_A_MA12
DDR_A_D45	AW9	SA_DQ45	SA_MA13	BJ16	DDR_A_MA13
DDR_A_D46	BD7	SA_DQ46			
DDR_A_D47	BB9	SA_DQ47			
DDR_A_D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR_A_RAS#
DDR_A_D49	AY7	SA_DQ49	SA_RCVEN#	AY20	SA_RCVEN#
DDR_A_D50	AT5	SA_DQ50			
DDR_A_D51	AT7	SA_DQ51	SA_WE#	BA19	DDR_A_WE#
DDR_A_D52	AY6	SA_DQ52			
DDR_A_D53	BB7	SA_DQ53			
DDR_A_D54	AR5	SA_DQ54			
DDR_A_D55	AR8	SA_DQ55			
DDR_A_D56	AR9	SA_DQ56			
DDR_A_D57	AN3	SA_DQ57			
DDR_A_D58	AM8	SA_DQ58			
DDR_A_D59	AN10	SA_DQ59			
DDR_A_D60	AT9	SA_DQ60			
DDR_A_D61	AN9	SA_DQ61			
DDR_A_D62	AM9	SA_DQ62			
DDR_A_D63	AN11	SA_DQ63			

TP58

DDR_A_CAS# 13
DDR_A_RAS# 13
DDR_A_WE# 13

CRESTLINE-GP-U

DDR_B_D[0..63] 14
DDR_B_BS[0..2] 14
DDR_B_DM[0..7] 14
DDR_B_DQS[0..7] 14
DDR_B_DQS#[0..7] 14
DDR_B_MA[0..13] 14

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DDR SYSTEM MEMORY B

DDR_B_D0	AP49	SB_DQ0	SB_BS0	AY17	DDR_B_BS0
DDR_B_D1	AR51	SB_DQ1	SB_BS1	BG18	DDR_B_BS1
DDR_B_D2	AW50	SB_DQ2	SB_BS2	BG36	DDR_B_BS2
DDR_B_D3	AW51	SB_DQ3			
DDR_B_D4	AN51	SB_DQ4	SB_CAS#	BE17	DDR_B_CAS#
DDR_B_D5	AN50	SB_DQ5			
DDR_B_D6	AV50	SB_DQ6	SB_DM0	AR50	DDR_B_DM0
DDR_B_D7	AV49	SB_DQ7	SB_DM1	BD49	DDR_B_DM1
DDR_B_D8	BA50	SB_DQ8	SB_DM2	BK45	DDR_B_DM2
DDR_B_D9	BB50	SB_DQ9	SB_DM3	BL39	DDR_B_DM3
DDR_B_D10	BA49	SB_DQ10	SB_DM4	BH12	DDR_B_DM4
DDR_B_D11	BE50	SB_DQ11	SB_DM5	BJ7	DDR_B_DM5
DDR_B_D12	BA51	SB_DQ12	SB_DM6	BF3	DDR_B_DM6
DDR_B_D13	AY49	SB_DQ13	SB_DM7	AW2	DDR_B_DM7
DDR_B_D14	BF50	SB_DQ14			
DDR_B_D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR_B_DQS0
DDR_B_D16	BJ50	SB_DQ16	SB_DQS1	BD50	DDR_B_DQS1
DDR_B_D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR_B_DQS2
DDR_B_D18	BJ43	SB_DQ18	SB_DQS3	BK39	DDR_B_DQS3
DDR_B_D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR_B_DQS4
DDR_B_D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR_B_DQS5
DDR_B_D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR_B_DQS6
DDR_B_D22	BK43	SB_DQ22	SB_DQS7	AV2	DDR_B_DQS7
DDR_B_D23	BK42	SB_DQ23	SB_DQS#0	AU50	DDR_B_DQS#0
DDR_B_D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR_B_DQS#1
DDR_B_D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR_B_DQS#2
DDR_B_D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR_B_DQS#3
DDR_B_D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR_B_DQS#4
DDR_B_D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR_B_DQS#5
DDR_B_D29	BJ40	SB_DQ29	SB_DQS#6	BF2	DDR_B_DQS#6
DDR_B_D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR_B_DQS#7
DDR_B_D31	BK37	SB_DQ31			
DDR_B_D32	BK13	SB_DQ32	SB_MA0	BC18	DDR_B_MA0
DDR_B_D33	BE11	SB_DQ33	SB_MA1	BG28	DDR_B_MA1
DDR_B_D34	BK11	SB_DQ34	SB_MA2	BG25	DDR_B_MA2
DDR_B_D35	BC11	SB_DQ35	SB_MA3	AW17	DDR_B_MA3
DDR_B_D36	BC13	SB_DQ36	SB_MA4	BF25	DDR_B_MA4
DDR_B_D37	BE12	SB_DQ37	SB_MA5	BE25	DDR_B_MA5
DDR_B_D38	BC12	SB_DQ38	SB_MA6	BA29	DDR_B_MA6
DDR_B_D39	BG12	SB_DQ39	SB_MA7	BC28	DDR_B_MA7
DDR_B_D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR_B_MA8
DDR_B_D41	BL9	SB_DQ41	SB_MA9	BD37	DDR_B_MA9
DDR_B_D42	BK5	SB_DQ42	SB_MA10	BG17	DDR_B_MA10
DDR_B_D43	BL5	SB_DQ43	SB_MA11	BF37	DDR_B_MA11
DDR_B_D44	BK9	SB_DQ44	SB_MA12	BA39	DDR_B_MA12
DDR_B_D45	BK10	SB_DQ45	SB_MA13	BG13	DDR_B_MA13
DDR_B_D46	BJ8	SB_DQ46			
DDR_B_D47	BJ6	SB_DQ47	SB_RAS#	AV16	DDR_B_RAS#
DDR_B_D48	BF4	SB_DQ48	SB_RCVEN#	AY18	SB_RCVEN#
DDR_B_D49	BH5	SB_DQ49			
DDR_B_D50	BG1	SB_DQ50	SB_WE#	BC17	DDR_B_WE#
DDR_B_D51	BC2	SB_DQ51			
DDR_B_D52	BK3	SB_DQ52			
DDR_B_D53	BE4	SB_DQ53			
DDR_B_D54	BD3	SB_DQ54			
DDR_B_D55	BJ2	SB_DQ55			
DDR_B_D56	BA3	SB_DQ56			
DDR_B_D57	BB3	SB_DQ57			
DDR_B_D58	AR1	SB_DQ58			
DDR_B_D59	AT3	SB_DQ59			
DDR_B_D60	AY2	SB_DQ60			
DDR_B_D61	AY3	SB_DQ61			
DDR_B_D62	AU2	SB_DQ62			
DDR_B_D63	AT2	SB_DQ63			

TP59

DDR_B_RAS# 14
DDR_B_CAS# 14
DDR_B_WE# 14

CRESTLINE-GP-U

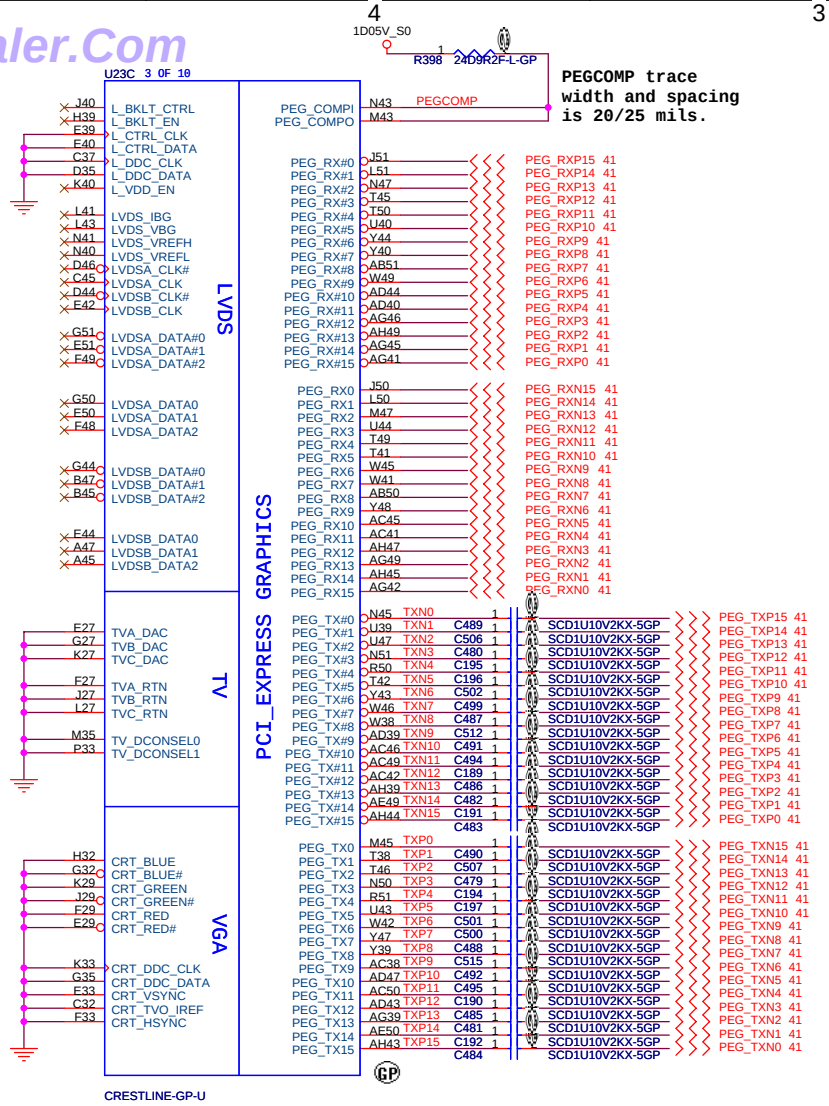
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(2/6)-DDR2 A/B CH

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Wednesday, October 18, 2006 Sheet 8 of 47



Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

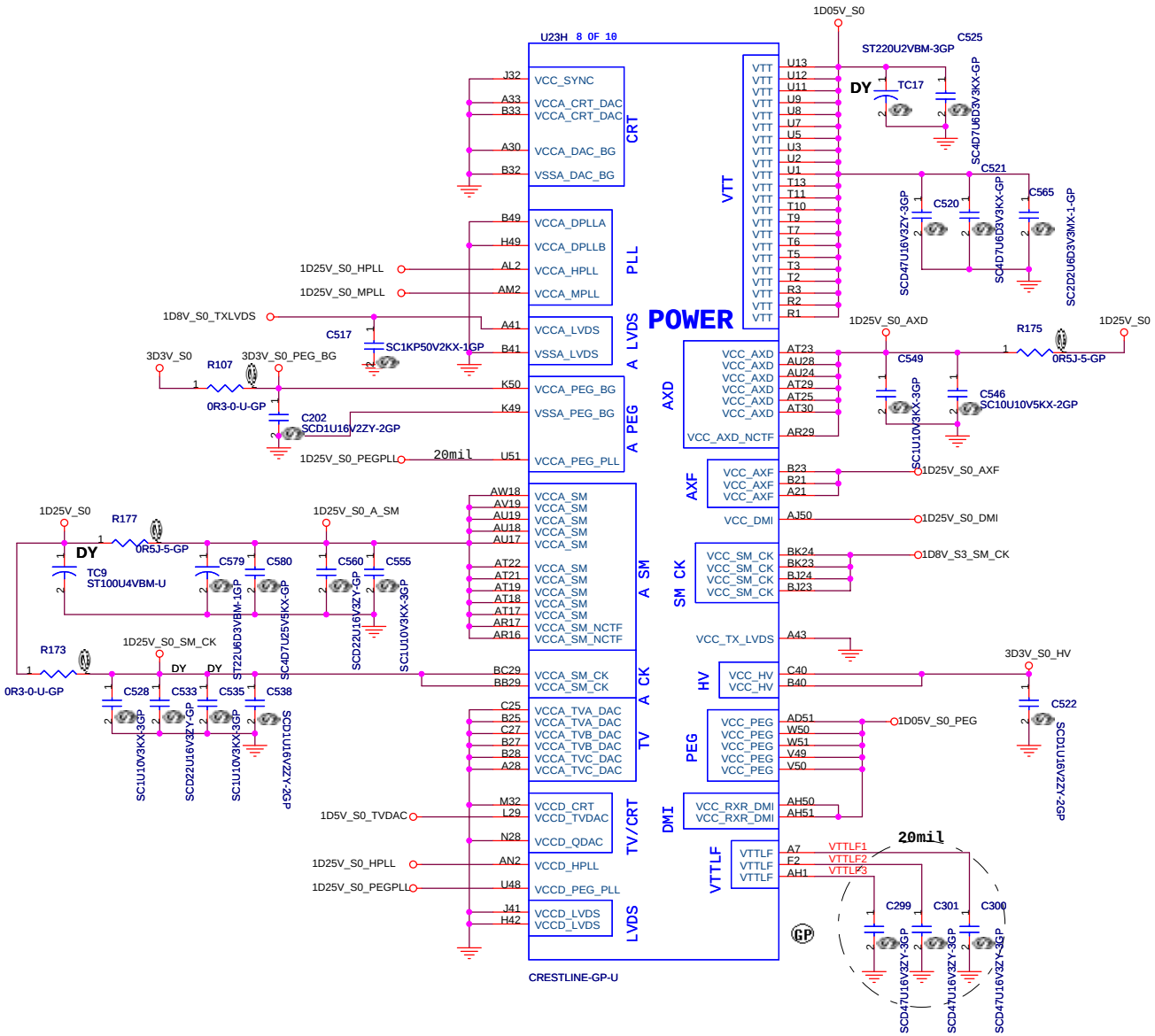
<Core Design>

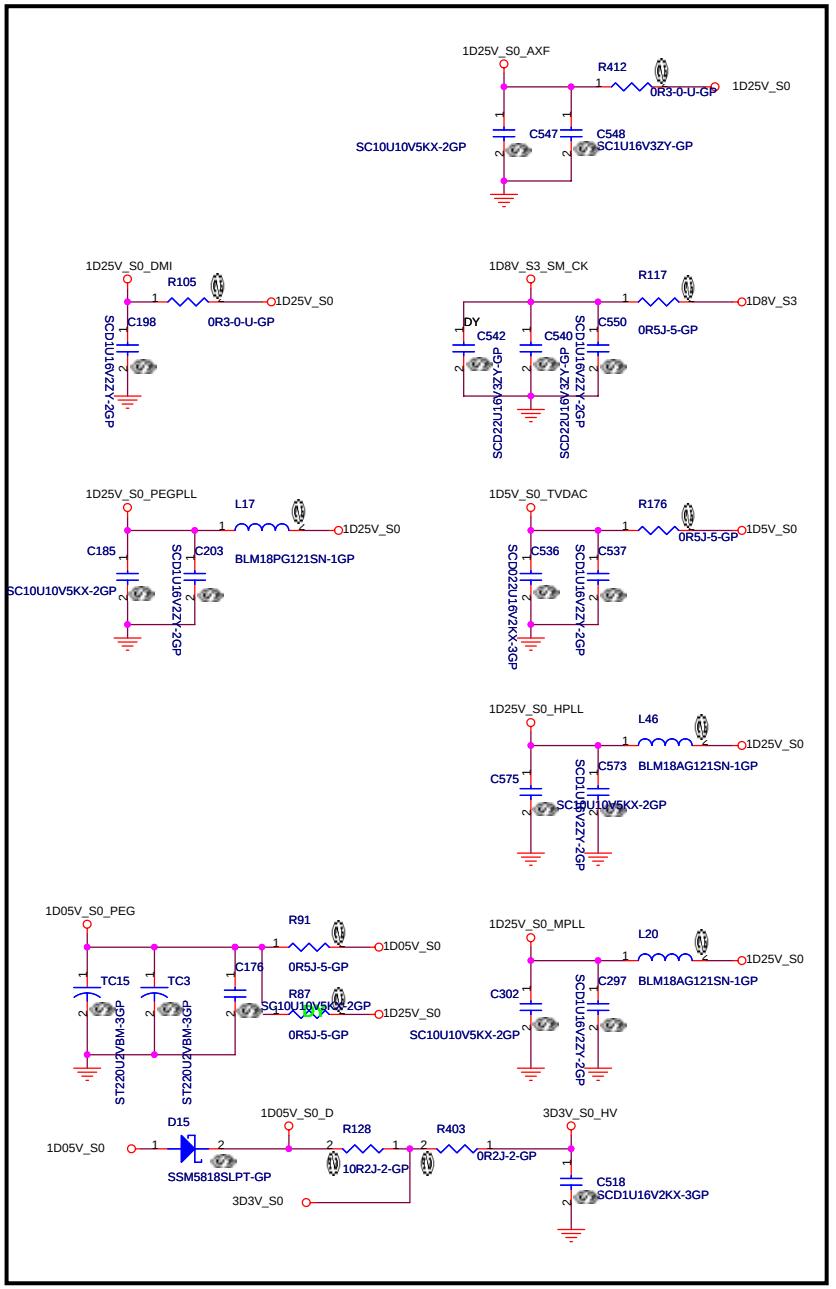
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(3/6)-VGA/LVDS/TV

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Monday, December 18, 2006 | Sheet 9 of 47





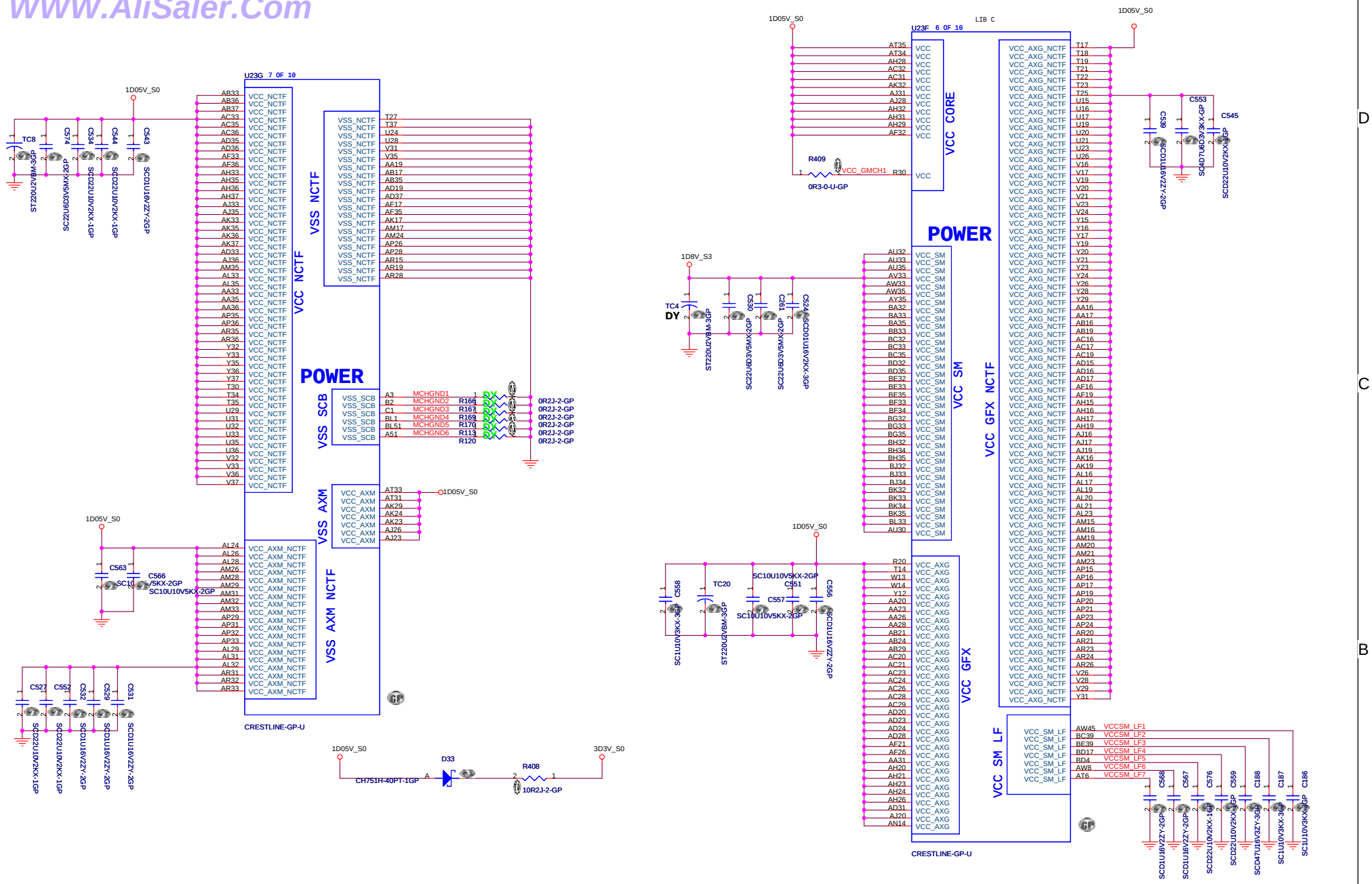
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(4/6)-PWR

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Thursday, December 14, 2006 Sheet 10 of 47



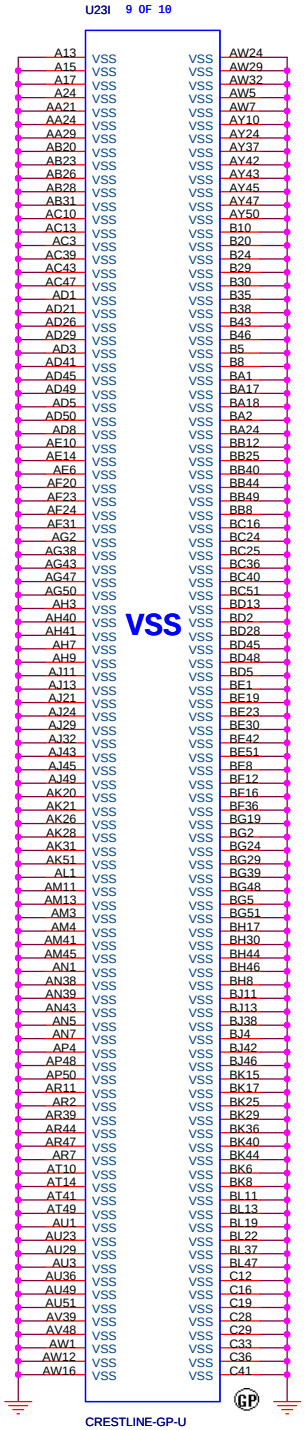
<Core Design>

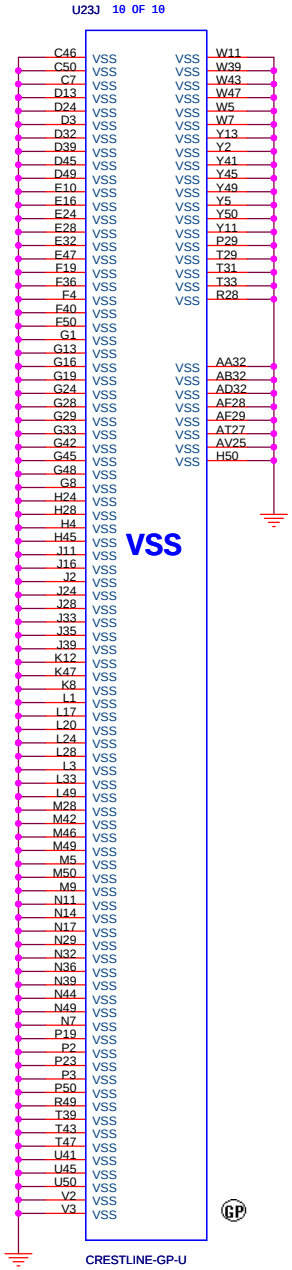
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(5/6)-PWR/GND

Size	Document Number	Rev
Custom	Pamirs-Discrete	SA

Date: Monday, December 18, 2006 Sheet 11 of 47





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(6/6)-PWR/GND

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Wednesday, October 18, 2006 Sheet 12 of 47

8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]
8 DDR_A_BS[0..2]

Layout Note:
Place near DM1

1D8V_S3
C213 SC22U16V5Y-2GP
C238 SC22U16V5Y-2GP
DY C251 SC22U16V5Y-2GP
DY C262 SC22U16V5Y-2GP
C272 SC22U16V5Y-2GP
DY C217 SC22U16V5Y-2GP
C242 SCD1U16V2Y-2GP
C231 SCD1U16V2Y-2GP
C224 SCD1U16V2Y-2GP
TC5 330U2VM-2GP

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DDR_VREF_S0
DY C503 SCD1U16V2Y-2GP
C498 SCD1U16V2Y-2GP
DY C511 SCD1U16V2Y-2GP
C509 SCD1U16V2Y-2GP
DY C516 SCD1U16V2Y-2GP
C514 SCD1U16V2Y-2GP
C523 SCD1U16V2Y-2GP
DY C519 SCD1U16V2Y-2GP
C204 SCD1U16V2Y-2GP
C241 SCD1U16V2Y-2GP
C216 SCD1U16V2Y-2GP
C227 SCD1U16V2Y-2GP
C255 SCD1U16V2Y-2GP

DDR_VREF_S0
RN13 SRN56J-4-GP: DDR_A_MA8, DDR_A_MA5
RN8 SRN56J-4-GP: DDR_A_BS2, DDR_CKE0_DIMMA
RN17 SRN56J-4-GP: DDR_A_MA3, DDR_A_MA1
RN55 SRN56J-4-GP: DDR_A_MA7, DDR_A_MA6
RN58 SRN56J-4-GP: DDR_A_RAS#, DDR_CS0_DIMMA#
RN11 SRN56J-4-GP: DDR_A_MA12, DDR_A_MA9
RN20 SRN56J-4-GP: DDR_A_MA10, DDR_A_BS0
RN56 SRN56J-4-GP: DDR_A_MA4, DDR_A_MA2
RN23 SRN56J-4-GP: DDR_A_WE#, DDR_CS1_DIMMA#
RN57 SRN56J-4-GP: DDR_A_MA0, DDR_A_BS1
RN26 SRN56J-4-GP: M_ODT1, DDR_A_CAS#
RN59 SRN56J-4-GP: M_ODT0, DDR_A_MA13
RN53 SRN56J-4-GP: DDR_CKE1_DIMMA
RN54 SRN56J-4-GP: DDR_A_MA14, DDR_A_MA11

Layout Note:
Place these resistors closely DM1,all trace length Max=1.5"

DM2
DDR_A_MA0 102 A0
DDR_A_MA1 101 A1
DDR_A_MA2 100 A2
DDR_A_MA3 99 A3
DDR_A_MA4 98 A4
DDR_A_MA5 97 A5
DDR_A_MA6 94 A6
DDR_A_MA7 92 A7
DDR_A_MA8 93 A8
DDR_A_MA9 91 A9
DDR_A_MA10 105 A10/AP
DDR_A_MA11 90 A11
DDR_A_MA12 89 A12
DDR_A_MA13 116 A13
DDR_A_MA14 86 A14
84 A15
DDR_A_BS2 85 A16/BA2
DDR_A_BS0 107 BA0
DDR_A_BS1 106 BA1
DDR_A_D0 5 DQ0
DDR_A_D1 7 DQ1
DDR_A_D2 17 DQ2
DDR_A_D3 19 DQ3
DDR_A_D4 4 DQ4
DDR_A_D5 6 DQ5
DDR_A_D6 14 DQ6
DDR_A_D7 16 DQ7
DDR_A_D8 23 DQ8
DDR_A_D9 25 DQ9
DDR_A_D10 35 DQ10
DDR_A_D11 37 DQ11
DDR_A_D12 20 DQ12
DDR_A_D13 22 DQ13
DDR_A_D14 36 DQ14
DDR_A_D15 38 DQ15
DDR_A_D16 43 DQ16
DDR_A_D17 45 DQ17
DDR_A_D18 55 DQ18
DDR_A_D19 57 DQ19
DDR_A_D20 44 DQ20
DDR_A_D21 46 DQ21
DDR_A_D22 56 DQ22
DDR_A_D23 58 DQ23
DDR_A_D24 61 DQ24
DDR_A_D25 63 DQ25
DDR_A_D26 73 DQ26
DDR_A_D27 75 DQ27
DDR_A_D28 62 DQ28
DDR_A_D29 64 DQ29
DDR_A_D30 74 DQ30
DDR_A_D31 76 DQ31
DDR_A_D32 123 DQ32
DDR_A_D33 125 DQ33
DDR_A_D34 135 DQ34
DDR_A_D35 137 DQ35
DDR_A_D36 124 DQ36
DDR_A_D37 126 DQ37
DDR_A_D38 134 DQ38
DDR_A_D39 136 DQ39
DDR_A_D40 141 DQ40
DDR_A_D41 143 DQ41
DDR_A_D42 151 DQ42
DDR_A_D43 153 DQ43
DDR_A_D44 140 DQ44
DDR_A_D45 142 DQ45
DDR_A_D46 152 DQ46
DDR_A_D47 154 DQ47
DDR_A_D48 157 DQ48
DDR_A_D49 159 DQ49
DDR_A_D50 173 DQ50
DDR_A_D51 175 DQ51
DDR_A_D52 158 DQ52
DDR_A_D53 160 DQ53
DDR_A_D54 174 DQ54
DDR_A_D55 176 DQ55
DDR_A_D56 179 DQ56
DDR_A_D57 181 DQ57
DDR_A_D58 189 DQ58
DDR_A_D59 191 DQ59
DDR_A_D60 180 DQ60
DDR_A_D61 182 DQ61
DDR_A_D62 192 DQ62
DDR_A_D63 194 DQ63
DDR_A_DQS#0 11 DQS0#
DDR_A_DQS#1 29 DQS1#
DDR_A_DQS#2 49 DQS2#
DDR_A_DQS#3 68 DQS3#
DDR_A_DQS#4 129 DQS4#
DDR_A_DQS#5 146 DQS5#
DDR_A_DQS#6 167 DQS6#
DDR_A_DQS#7 186 DQS7#
DDR_A_DQS0 13 DQS0
DDR_A_DQS1 31 DQS1
DDR_A_DQS2 51 DQS2
DDR_A_DQS3 70 DQS3
DDR_A_DQS4 131 DQS4
DDR_A_DQS5 148 DQS5
DDR_A_DQS6 169 DQS6
DDR_A_DQS7 188 DQS7
M_ODT0 114 OTD0
M_ODT1 119 OTD1
VREF 1 VREF
GND 202 GND
MH1 MH1
RAS# 108 DDR_A_RAS# — DDR_A_RAS# 8
WE# 109 DDR_A_WE# — DDR_A_WE# 8
CAS# 113 DDR_A_CAS# — DDR_A_CAS# 8
CS0# 110 DDR_CS0_DIMMA# — DDR_CS0_DIMMA# 7
CS1# 115 DDR_CS1_DIMMA# — DDR_CS1_DIMMA# 7
CKE0 79 DDR_CKE0_DIMMA — DDR_CKE0_DIMMA 7
CKE1 80 DDR_CKE1_DIMMA — DDR_CKE1_DIMMA 7
CK0 30 M_CLK_DDR0 — M_CLK_DDR0 7
CK0# 32 M_CLK_DDR#0 — M_CLK_DDR#0 7
CK1 164 M_CLK_DDR1 — M_CLK_DDR1 7
CK1# 166 M_CLK_DDR#1 — M_CLK_DDR#1 7
DM0 10 DDR_A_DM0
DM1 26 DDR_A_DM1
DM2 52 DDR_A_DM2
DM3 67 DDR_A_DM3
DM4 130 DDR_A_DM4
DM5 147 DDR_A_DM5
DM6 170 DDR_A_DM6
DM7 185 DDR_A_DM7
SDA 195 ICH_SMBDATA — ICH_SMBDATA 3,14,20
SCL 197 ICH_SMBCLK — ICH_SMBCLK 3,14,20
VDDSPD 199 — SCD1U16V2ZY-2GP — 3D3V_S0
SA0 198 R416 1 — 2 10KR2J-3-GP
SA1 200 R417 1 — 2 10KR2J-3-GP
50 PM_EXTTS#0 7
C569 SCD1U16V2ZY-2GP
C571 SC2D2U6D3V3KX-GP
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
1D8V_S3
VDD 81 82 87 88 95 96 103 104 111 112 117 118
VSS 3 8 9 12 15 18 21 24 27 28 33 34 39 40 41 42 47 48 53 54 59 60 65 66 71 72 77 78 121 122 127 128 132 133 138 139 144 145 149 150 155 156 161 162 165 168 171 172 177 178 183 184 187 190 193 196 201
MH2
DDR2-200P-20-GP-U

DDR_VREF_S3
7 M_ODT0
7 M_ODT1
SC2D2U16V5ZY-2GP
C76 SCD1U16V2ZY-2GP
C82

<Core Design>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **DDRII-SODIMM SLOT1**
Size: Custom | Document Number: Pamirs-Discrete | Rev: SA
Date: Wednesday, October 18, 2006 | Sheet 13 of 47

8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]
8 DDR_B_BS[0..2]

Layout Note:
Place near DM2

1D8V_S3
DY
C541 SCD2U16V2ZY-2GP
C508 SCD2U16V2ZY-2GP
C244 SCD2U16V2ZY-2GP
C497 SCD2U16V2ZY-2GP
C232 SCD2U16V2ZY-2GP
C513 SCD1U16V2ZY-2GP
C170 SCD1U16V2ZY-2GP
C221 SCD1U16V2ZY-2GP
C264 SCD1U16V2ZY-2GP

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DDR_VREF_S0
DY
C245 SCD1U16V2ZY-2GP
C256 SCD1U16V2ZY-2GP
C184 SCD1U16V2ZY-2GP
C207 SCD1U16V2ZY-2GP
C234 SCD1U16V2ZY-2GP
C265 SCD1U16V2ZY-2GP
C226 SCD1U16V2ZY-2GP
C235 SCD1U16V2ZY-2GP
C243 SCD1U16V2ZY-2GP
C237 SCD1U16V2ZY-2GP
C215 SCD1U16V2ZY-2GP
C183 SCD1U16V2ZY-2GP
C225 SCD1U16V2ZY-2GP

DDR_VREF_S0
RN18 SRN56J-4-GP: DDR_B_MA3, DDR_B_MA1
RN10 SRN56J-4-GP: DDR_B_MA12, DDR_B_MA9
RN21 SRN56J-4-GP: DDR_B_MA10, DDR_B_BS0
RN7 SRN56J-4-GP: DDR_CKE3_DIMMB, DDR_B_MA11
RN19 SRN56J-4-GP: DDR_B_MA0, DDR_B_BS1
RN14 SRN56J-4-GP: DDR_B_MA5, DDR_B_MA8
RN22 SRN56J-4-GP: DDR_CS2_DIMMB#, DDR_B_RAS#
RN12 SRN56J-4-GP: DDR_B_MA7, DDR_B_MA6
RN24 SRN56J-4-GP: DDR_B_WE#, DDR_B_CAS#
RN16 SRN56J-4-GP: DDR_B_MA4, DDR_B_MA2
RN27 SRN56J-4-GP: DDR_CS3_DIMMB#, M_ODT3
RN25 SRN56J-4-GP: M_ODT2, DDR_B_MA13
RN9 SRN56J-4-GP: DDR_B_MA14
RN6 SRN56J-4-GP: DDR_B_BS2, DDR_CKE2_DIMMB
SRN56J-4-GP

Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"

DM1
7 DDR_B_MA14
DDR_B_MA0 102, DDR_B_MA1 101, DDR_B_MA2 100, DDR_B_MA3 99, DDR_B_MA4 98, DDR_B_MA5 97, DDR_B_MA6 94, DDR_B_MA7 92, DDR_B_MA8 93, DDR_B_MA9 91, DDR_B_MA10 105, DDR_B_MA11 90, DDR_B_MA12 89, DDR_B_MA13 116, DDR_B_MA14 86
DDR_B_BS2 84, 85
DDR_B_BS0 107, DDR_B_BS1 106
DDR_B_D0 5, DDR_B_D1 7, DDR_B_D2 17, DDR_B_D3 19, DDR_B_D4 4, DDR_B_D5 6, DDR_B_D6 14, DDR_B_D7 16, DDR_B_D8 23, DDR_B_D9 25, DDR_B_D10 35, DDR_B_D11 37, DDR_B_D12 20, DDR_B_D13 22, DDR_B_D14 36, DDR_B_D15 38, DDR_B_D16 43, DDR_B_D17 45, DDR_B_D18 55, DDR_B_D19 57, DDR_B_D20 44, DDR_B_D21 46, DDR_B_D22 56, DDR_B_D23 58, DDR_B_D24 61, DDR_B_D25 63, DDR_B_D26 73, DDR_B_D27 75, DDR_B_D28 62, DDR_B_D29 64, DDR_B_D30 74, DDR_B_D31 76, DDR_B_D32 123, DDR_B_D33 125, DDR_B_D34 135, DDR_B_D35 137, DDR_B_D36 124, DDR_B_D37 126, DDR_B_D38 134, DDR_B_D39 136, DDR_B_D40 141, DDR_B_D41 143, DDR_B_D42 151, DDR_B_D43 153, DDR_B_D44 140, DDR_B_D45 142, DDR_B_D46 152, DDR_B_D47 154, DDR_B_D48 157, DDR_B_D49 159, DDR_B_D50 173, DDR_B_D51 175, DDR_B_D52 158, DDR_B_D53 160, DDR_B_D54 174, DDR_B_D55 176, DDR_B_D56 179, DDR_B_D57 181, DDR_B_D58 189, DDR_B_D59 191, DDR_B_D60 180, DDR_B_D61 182, DDR_B_D62 192, DDR_B_D63 194
DDR_B_DQS#0 11, DDR_B_DQS#1 29, DDR_B_DQS#2 49, DDR_B_DQS#3 68, DDR_B_DQS#4 129, DDR_B_DQS#5 146, DDR_B_DQS#6 167, DDR_B_DQS#7 186
DDR_B_DQS0 13, DDR_B_DQS1 31, DDR_B_DQS2 51, DDR_B_DQS3 70, DDR_B_DQS4 131, DDR_B_DQS5 148, DDR_B_DQS6 169, DDR_B_DQS7 188
M_ODT2 114, M_ODT3 119
VREF 1, VREF 2
GND 202
MH1
A0 102, A1 101, A2 100, A3 99, A4 98, A5 97, A6 94, A7 92, A8 93, A9 91, A10/AP 105, A11 90, A12 89, A13 116, A14 86, A15 84, A16/BA2 85
BA0 107, BA1 106
DQ0 5, DQ1 7, DQ2 17, DQ3 19, DQ4 4, DQ5 6, DQ6 14, DQ7 16, DQ8 23, DQ9 25, DQ10 35, DQ11 37, DQ12 20, DQ13 22, DQ14 36, DQ15 38, DQ16 43, DQ17 45, DQ18 55, DQ19 57, DQ20 44, DQ21 46, DQ22 56, DQ23 58, DQ24 61, DQ25 63, DQ26 73, DQ27 75, DQ28 62, DQ29 64, DQ30 74, DQ31 76, DQ32 123, DQ33 125, DQ34 135, DQ35 137, DQ36 124, DQ37 126, DQ38 134, DQ39 136, DQ40 141, DQ41 143, DQ42 151, DQ43 153, DQ44 140, DQ45 142, DQ46 152, DQ47 154, DQ48 157, DQ49 159, DQ50 173, DQ51 175, DQ52 158, DQ53 160, DQ54 174, DQ55 176, DQ56 179, DQ57 181, DQ58 189, DQ59 191, DQ60 180, DQ61 182, DQ62 192, DQ63 194
DQS0# 11, DQS1# 29, DQS2# 49, DQS3# 68, DQS4# 129, DQS5# 146, DQS6# 167, DQS7# 186
DQS0 13, DQS1 31, DQS2 51, DQS3 70, DQS4 131, DQS5 148, DQS6 169, DQS7 188
OTD0 114, OTD1 119
DDR2-200P-21-GP-U

RAS# 108 ← DDR_B_RAS#
WE# 109 ← DDR_B_WE#
CAS# 113 ← DDR_B_CAS#
CS0# 110 ← DDR_CS2_DIMMB#
CS1# 115 ← DDR_CS3_DIMMB#
CKE0 79 ← DDR_CKE2_DIMMB
CKE1 80 ← DDR_CKE3_DIMMB
CK0 30 ← M_CLK_DDR2
CK0# 32 ← M_CLK_DDR#2
CK1 164 ← M_CLK_DDR3
CK1# 166 ← M_CLK_DDR#3
DM0 10 ← DDR_B_DM0
DM1 26 ← DDR_B_DM1
DM2 52 ← DDR_B_DM2
DM3 67 ← DDR_B_DM3
DM4 130 ← DDR_B_DM4
DM5 147 ← DDR_B_DM5
DM6 170 ← DDR_B_DM6
DM7 185 ← DDR_B_DM7
SDA 195 ↔ ICH_SMBDATA 3,13,20
SCL 197 ↔ ICH_SMBCLK 3,13,20
VDDSPD 199 — SCD1U16V2ZY-2GP — 3D3V_S0
SA0 198 — R420 10KR2J-3-GP — 3D3V_S0
SA1 200 — R421 10KR2J-3-GP
C577 SC2D2U6D3V3KX-GP
C578
NC#50 50 → PM_EXTTS#1 7
NC#69 69
NC#83 83
NC#120 120
NC#163/TEST 163
1D8V_S3
VDD 81, 82, 87, 88, 95, 96, 103, 104, 111, 112, 117, 118
VSS 3, 8, 9, 12, 15, 18, 21, 24, 27, 28, 33, 34, 39, 40, 41, 42, 47, 48, 53, 54, 59, 60, 65, 66, 71, 72, 77, 78, 121, 122, 127, 128, 132, 133, 138, 139, 144, 145, 149, 150, 155, 156, 161, 162, 165, 168, 171, 172, 177, 178, 183, 184, 187, 190, 193, 196
GND 201
MH2

DDR_VREF_S3
7 M_ODT2
7 M_ODT3
DDR_VREF_S3
SC2D2U16V5ZY-2GP
C71 SCD1U16V2ZY-2GP
C77

<Core Design>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDRII-SODIMM SLOT2**
Size: Custom | Document Number: Pamirs-Discrete | Rev: SA
Date: Wednesday, October 18, 2006 | Sheet 14 of 47

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

42 VGA_RED
42 VGA_GREEN
42 VGA_BLUE

L8 BLM18BB470SN1-GP
L2 BLM18BB470SN1-GP
L1 BLM18BB470SN1-GP

CRT_R 17
CRT_G 17
CRT_B 17

R23 150R2F-1-GP
R20 150R2F-1-GP
R19 150R2F-1-GP

C35 SC10P50V2JN-4GP
C29 SC10P50V2JN-4GP
C22 SC10P50V2JN-4GP
C32 SC10P50V2JN-4GP
C26 SC10P50V2JN-4GP
C21 SC10P50V2JN-4GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_CRT_S0
C13 SCD01U16V2KX-3GP
F1 FUSE-1D1A6V-8GP
5V_S0
D4 CH751H-40PT-1GP
5V_CRT1_S0
RN1 SRN2K2J-1-GP

CRT1 20.20424.015
CRT_R
CRT_G
CRT_B
DDC_DATA_CON
JVGA_HS
JVGA_VS
DDC_CLK_CON

C15 SC33P50V2JN-3GP DY
C20 SC33P50V2JN-3GP DY
C11 SC22P50V2JN-4GP
C9 SC22P50V2JN-4GP

DDC_DATA_CON
DDC_CLK_CON
D11 BAV99W-1-GP DY
D12 BAV99W-1-GP DY

5V_CRT1_S0
U3 PACDN009MR-GP-U DY
GMCH_HSYNC
GMCH_VSYNC
CRT_R
CRT_G
CRT_B

5V_S0
BAV99W-1-GP
C464 SCD1U16V2ZY-2GP
PR_INSERT 17

17,42 GMCH_HSYNC
17,42 GMCH_VSYNC
U6A TSAHCT125PW-GP
U6B TSAHCT125PW-GP
HSYNC_5
VSYNC_5
RN4 SRN33J-5-GP-U
JVGA_HS
JVGA_VS

3D3V_S0
RN2 SRN2K2J-1-GP
U1 2N7002DW-1-GP
42 VGA_DDCDATA
17 DDC_CLK_CON
DDC_DATA_CON 17
VGA_DDCCLK 42

TV OUT CONN

connector

42 VGA_TV_CRMA
L32 BLM18BB470SN1-GP
C432 SC10P50V2JN-4GP
C431 SC10P50V2JN-4GP
R1 150R2F-1-GP
TV_CRMA 17

42 VGA_TV_COMP
L33 BLM18BB470SN1-GP
C434 SC10P50V2JN-4GP
C433 SC10P50V2JN-4GP
R3 150R2F-1-GP
TV_COMP 17

42 VGA_TV_LUMA
L34 BLM18BB470SN1-GP
C438 SC10P50V2JN-4GP
C437 SC10P50V2JN-4GP
R2 150R2F-1-GP
TV_LUMA 17

Place this 2 resistors close to the TV-out connector

TV1 MINDIN7-16-GP-U
TV_LUMA
TV_CRMA
TV_COMP
LUMA
CRMA
COMP
NC#2
NC#5
GND

D1 BAV99W-1-GP DY
VGA_TV_COMP
C1 SCD1U16V2ZY-2GP DY

D3 BAV99W-1-GP DY
VGA_TV_LUMA
C3 SCD1U16V2ZY-2GP DY

D2 BAV99W-1-GP DY
VGA_TV_CRMA
C2 SCD1U16V2ZY-2GP DY

3D3V_S0

5V @ ext. CRT side

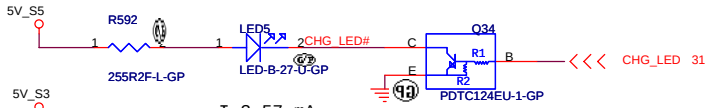
<Core Design>

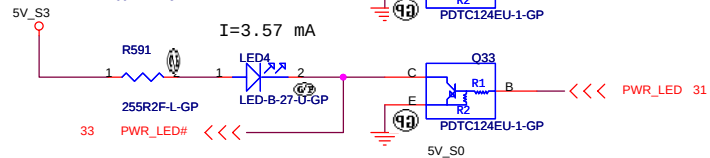
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

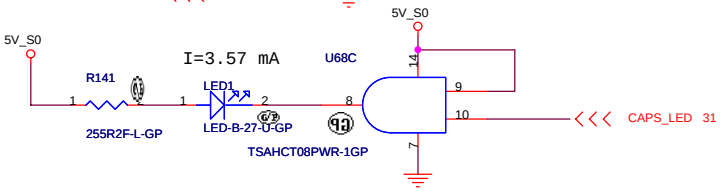
Title: CRT/TV Connector
Size: A3
Document Number: Pamirs-Discrete
Rev: SA
Date: Friday, November 24, 2006
Sheet 15 of 47

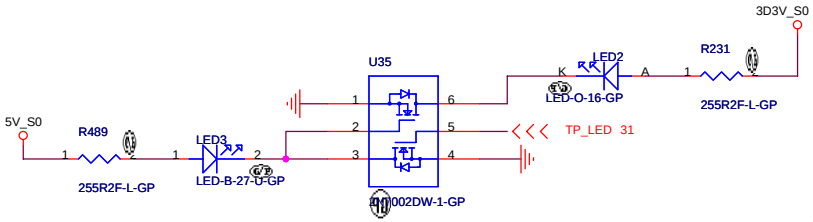
LED / INVERTER INTERFACE

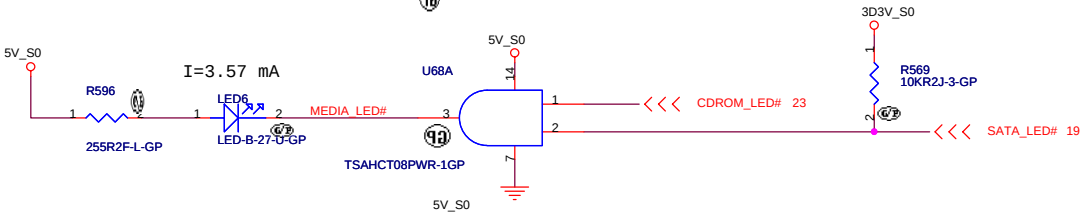
LCD/INV CONN

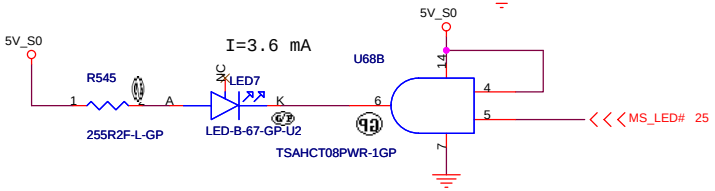


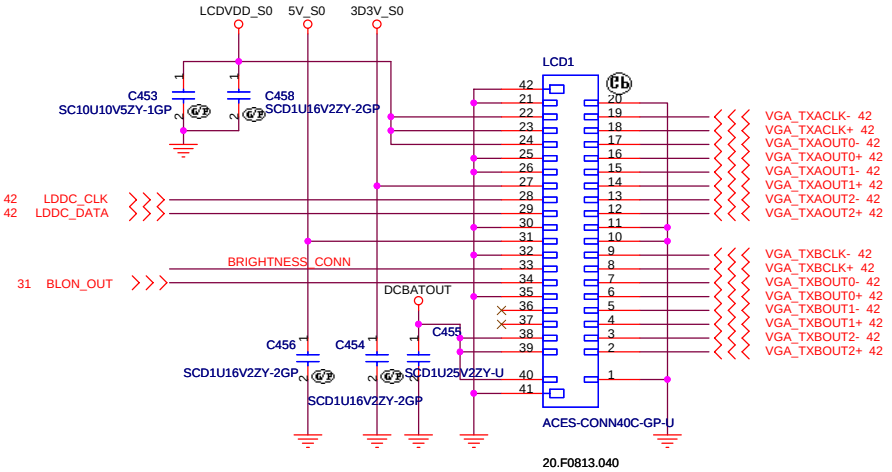


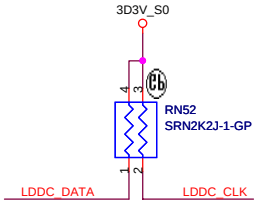


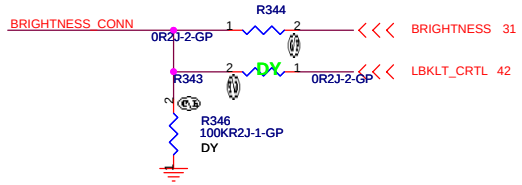


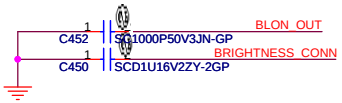


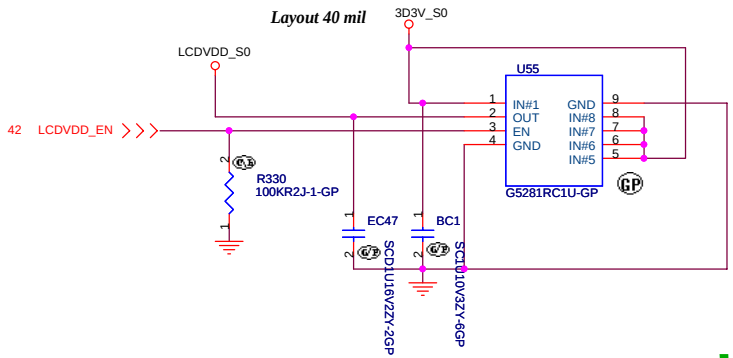


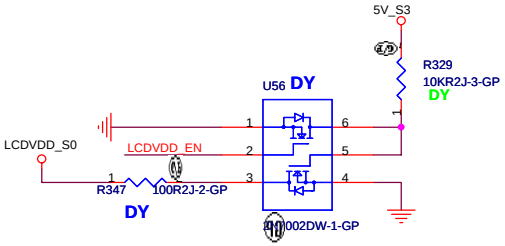












<Core Design>

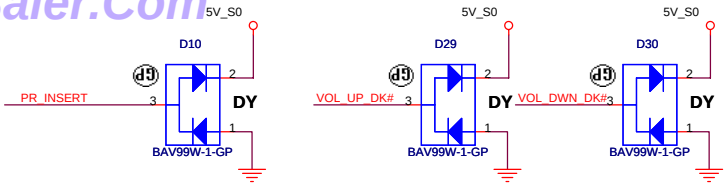
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

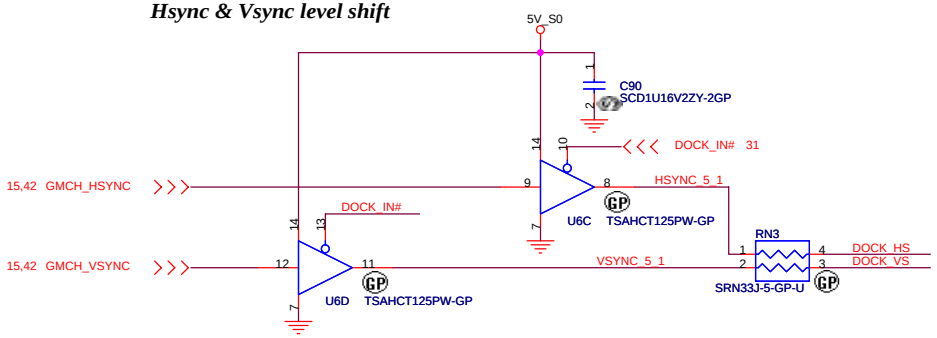
Size: Custom | Document Number: Pamirs-Discrete | Rev: SA

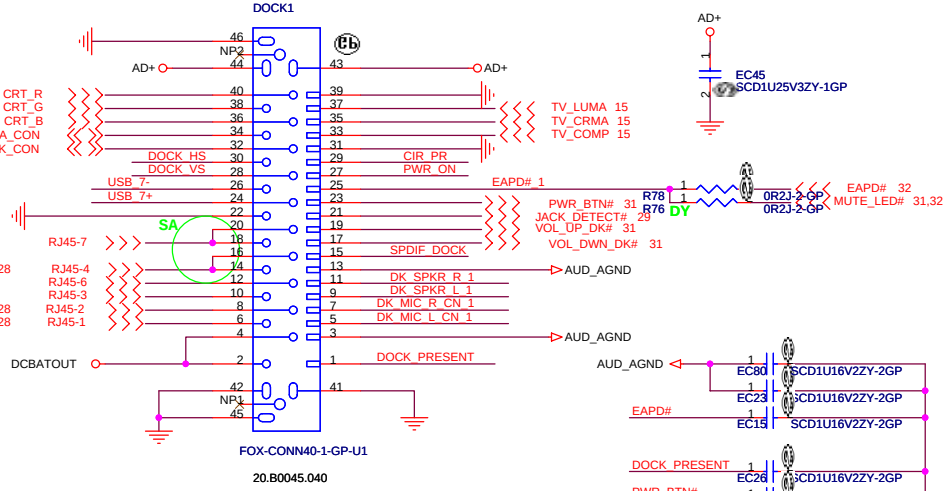
Date: Tuesday, December 19, 2006 | Sheet 16 of 47

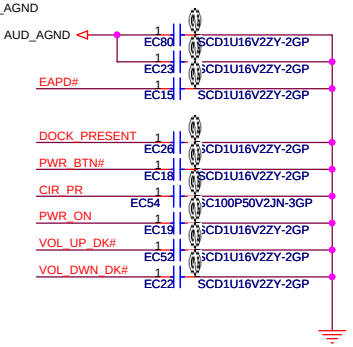
Docking Connector

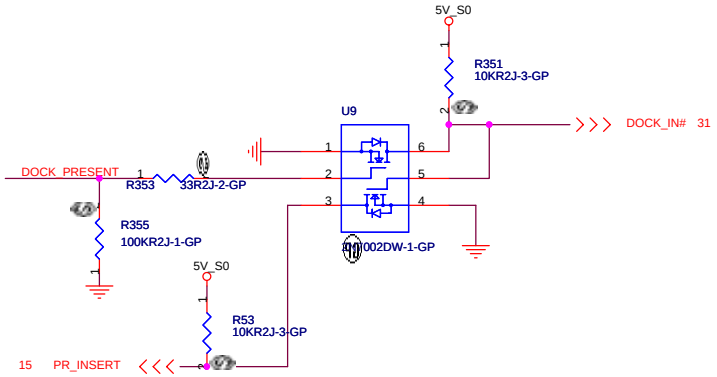


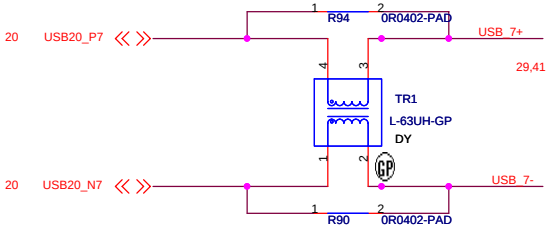
Hsync & Vsync level shift

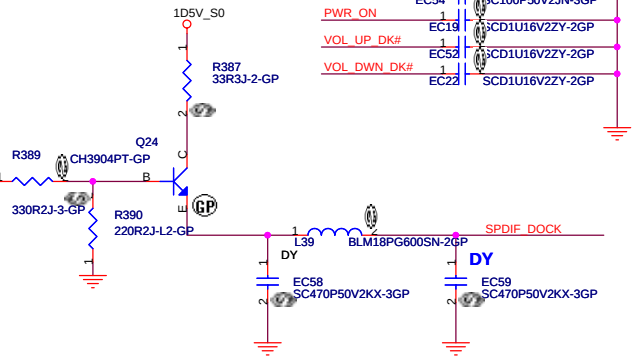


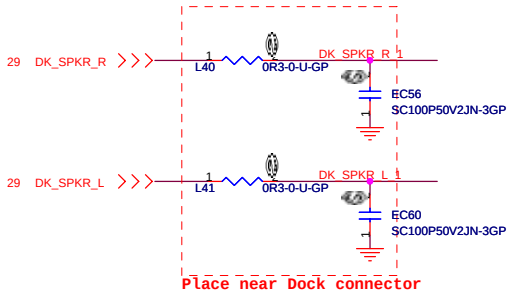


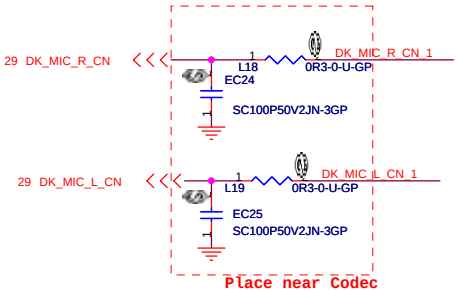


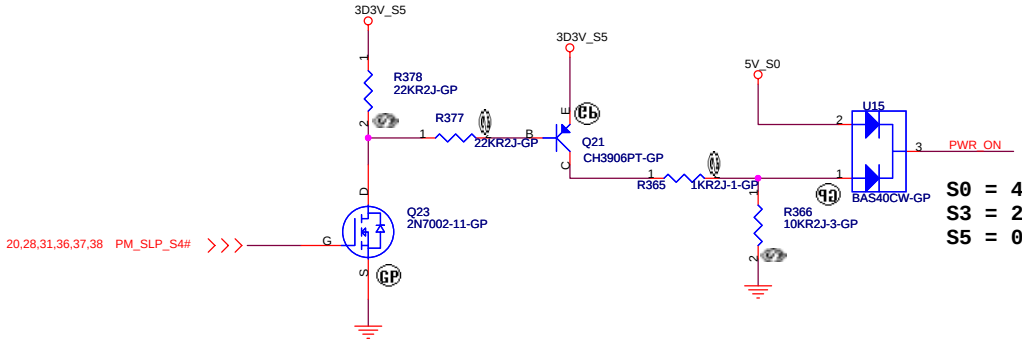








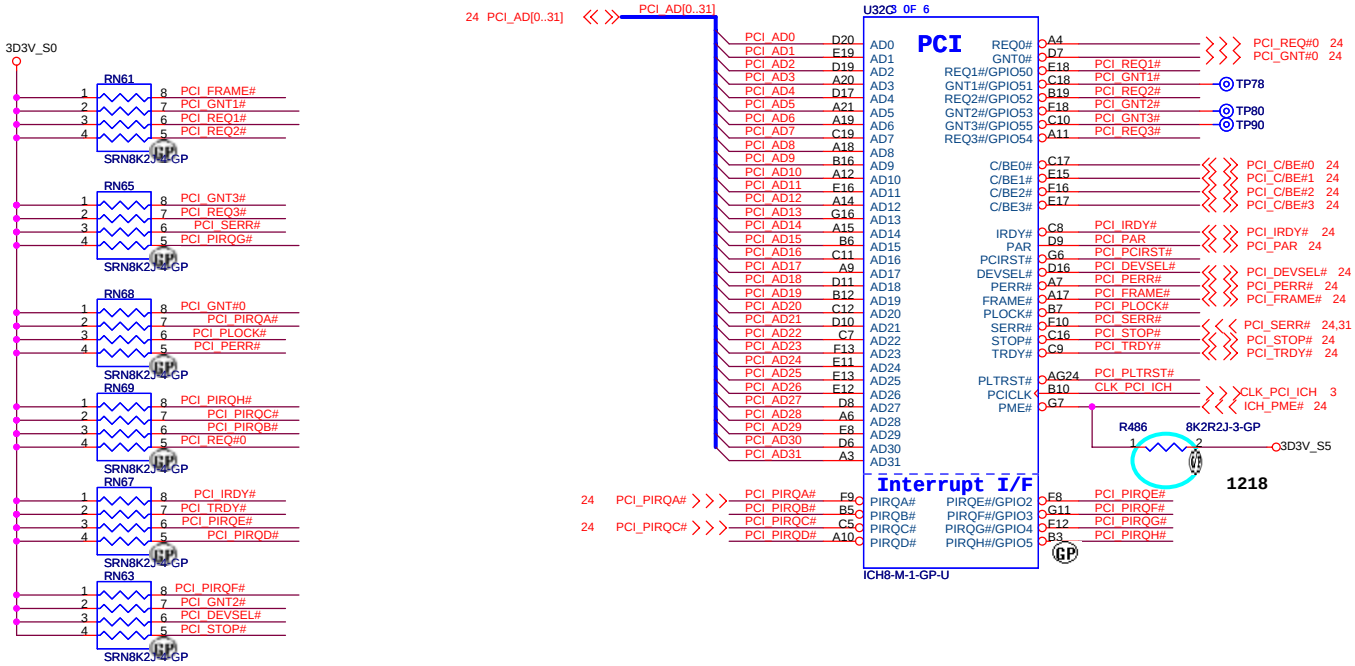


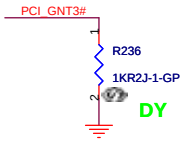



```
S0 = 4V
S3 = 2.5V
S5 = 0V
```

<Core Design>

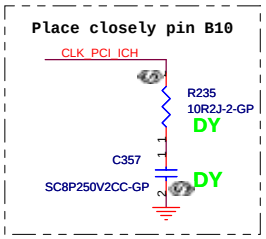
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Board to board conn/ Docking***
Size A3	Document Number: Pamirs-Discrete — Rev: SA
Date: Friday, November 24, 2006	Sheet 17 of 47

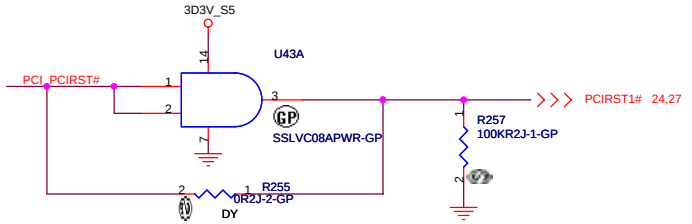


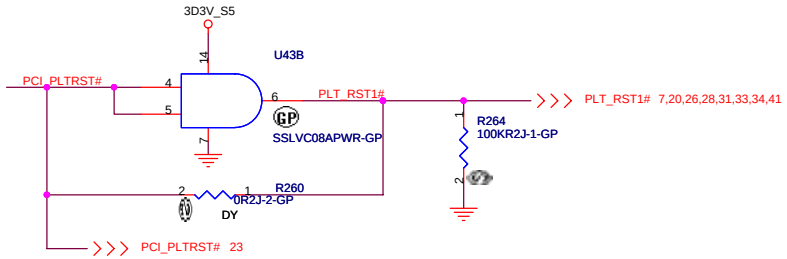


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *





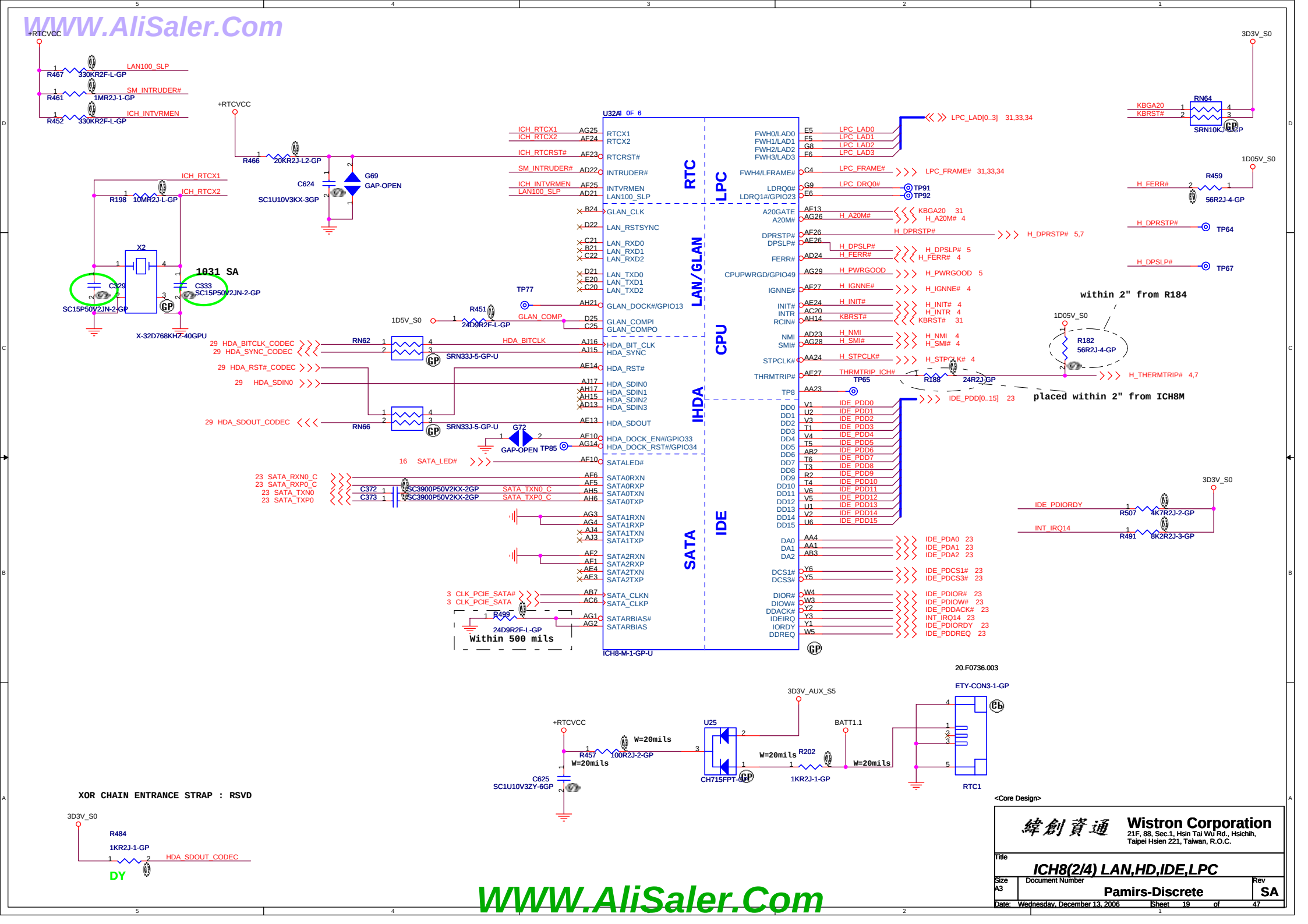


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Monday, December 18, 2006 | Sheet 18 of 47



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(2/4) LAN,HD,IDE,LPC

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Wednesday, December 13, 2006 | Sheet 19 of 47

Place closely pin G5

CLK_48M_ICH
R245 10R2J-2-GP DY
C371 SC4D7P50V2CN-1GP DY

Place closely pin AG9

CLK_14M_ICH
R493 10R2J-2-GP DY
C671 SC4D7P50V2CN-1GP DY

U32D 4 OF 6

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1
SATA GPIO: SATA0GP/GPIO21, SATA1GP/GPIO19, SATA2GP/GPIO36, GPIO37
CLOCKS: CLK14, CLK48, SUSCLK
SYSGPIO: RI#, SUS_STAT#/LPCPD#, SYS_RESET#, BMBUSY#/GPIO0, SMBALERT#/GPIO11, STP_PCI#, STP_CPU#, CLKRUN#, WAKE#, SERIRQ, THRM#, VRMPWRGD, TP7
POWER MGT: S4_STATE#/GPIO26, PWROK, DPRSLPVR/GPIO16, BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, CK_PWRGD, CLPWROK, SLP_M#, CL_CLK0, CL_CLK1, CL_DATA0, CL_DATA1, CL_VREF0, CL_VREF1, CL_RST#
GPIO: TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, GPIO12, TACH0/GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48
Controller Link: CLGPIO0/GPIO24, CLGPIO1/GPIO10, CLGPIO2/GPIO14, CLGPIO3/GPIO9
MISC: SPKR, MCH_SYNC#, TP3
ICH8-M-1-GP-U

Low--> default
High--> No boot

1016 SA

32K suspend clock output

U32B 2 OF 6

PCI-Express: PERN1/PERP1/PETN1/PETP1, PERN2/PERP2/PETN2/PETP2, PERN3/PERP3/PETN3/PETP3, PERN4/PERP4/PETN4/PETP4, PERN5/PERP5/PETN5/PETP5, PERN6/GLAN_RXN/PERP6/GLAN_RXP/PETN6/GLAN_TXN/PETP6/GLAN_TXP
Direct Media Interface: DMI0RXN/DMI0RXP/DMI0TXN/DMI0TXP, DMI1RXN/DMI1RXP/DMI1TXN/DMI1TXP, DMI2RXN/DMI2RXP/DMI2TXN/DMI2TXP, DMI3RXN/DMI3RXP/DMI3TXN/DMI3TXP, DMI_CLKN/DMI_CLKP, DMI_ZCOMP, DMI_IRCOMP
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO
USB: OC0#, OC1#/GPIO40, OC2#/GPIO41, OC3#/GPIO42, OC4#/GPIO43, OC5#/GPIO29, OC6#/GPIO30, OC7#/GPIO31, OC8#, OC9#, USBP0N/USBP0P, USBP1N/USBP1P, USBP2N/USBP2P, USBP3N/USBP3P, USBP4N/USBP4P, USBP5N/USBP5P, USBP6N/USBP6P, USBP7N/USBP7P, USBP8N/USBP8P, USBP9N/USBP9P, USBRBIAS#/USBRBIAS
ICH8-M-1-GP-U

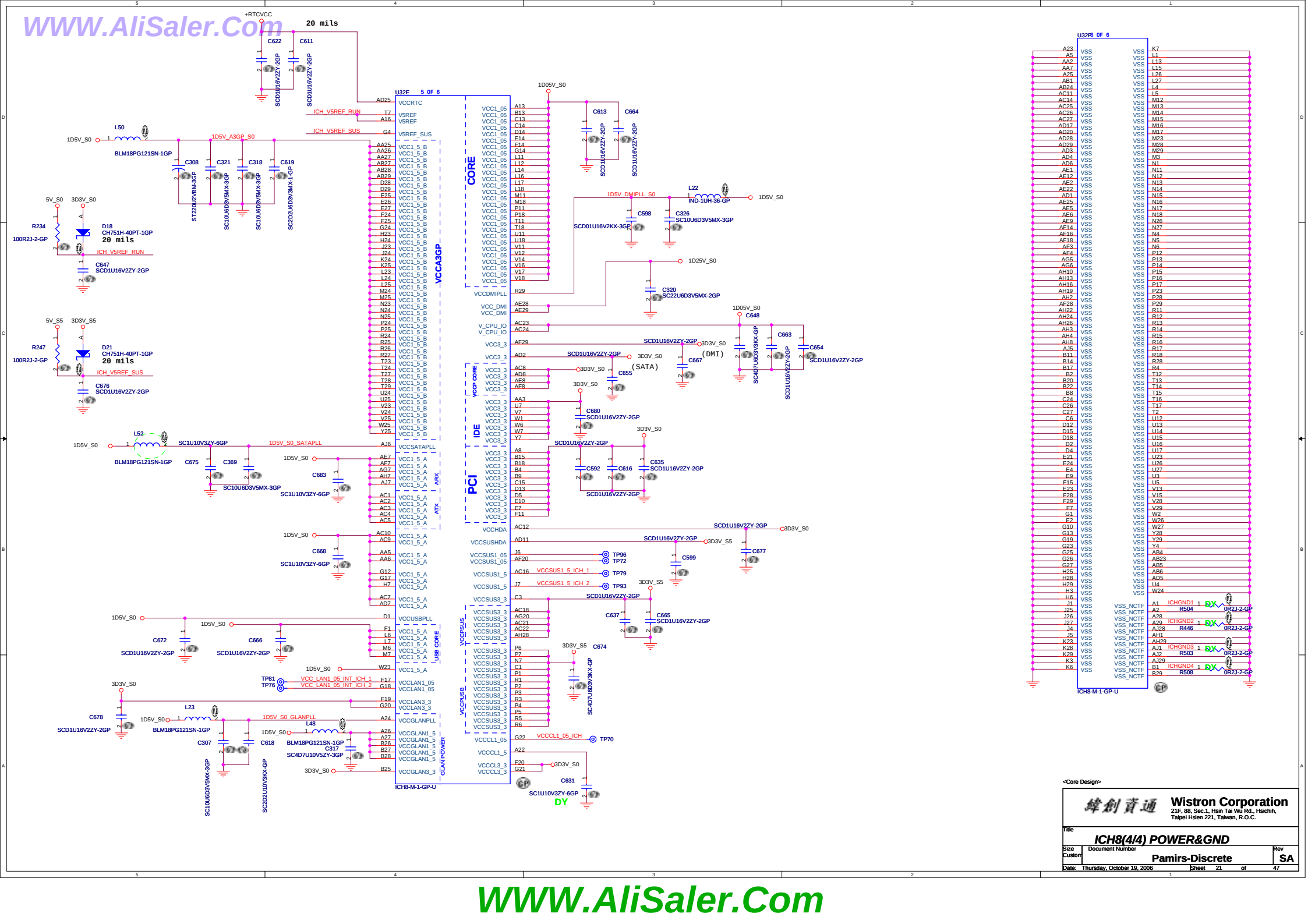
USB1
New Card
USB2
USB3
CAMERA
BT
MINICARD 1
DOCK

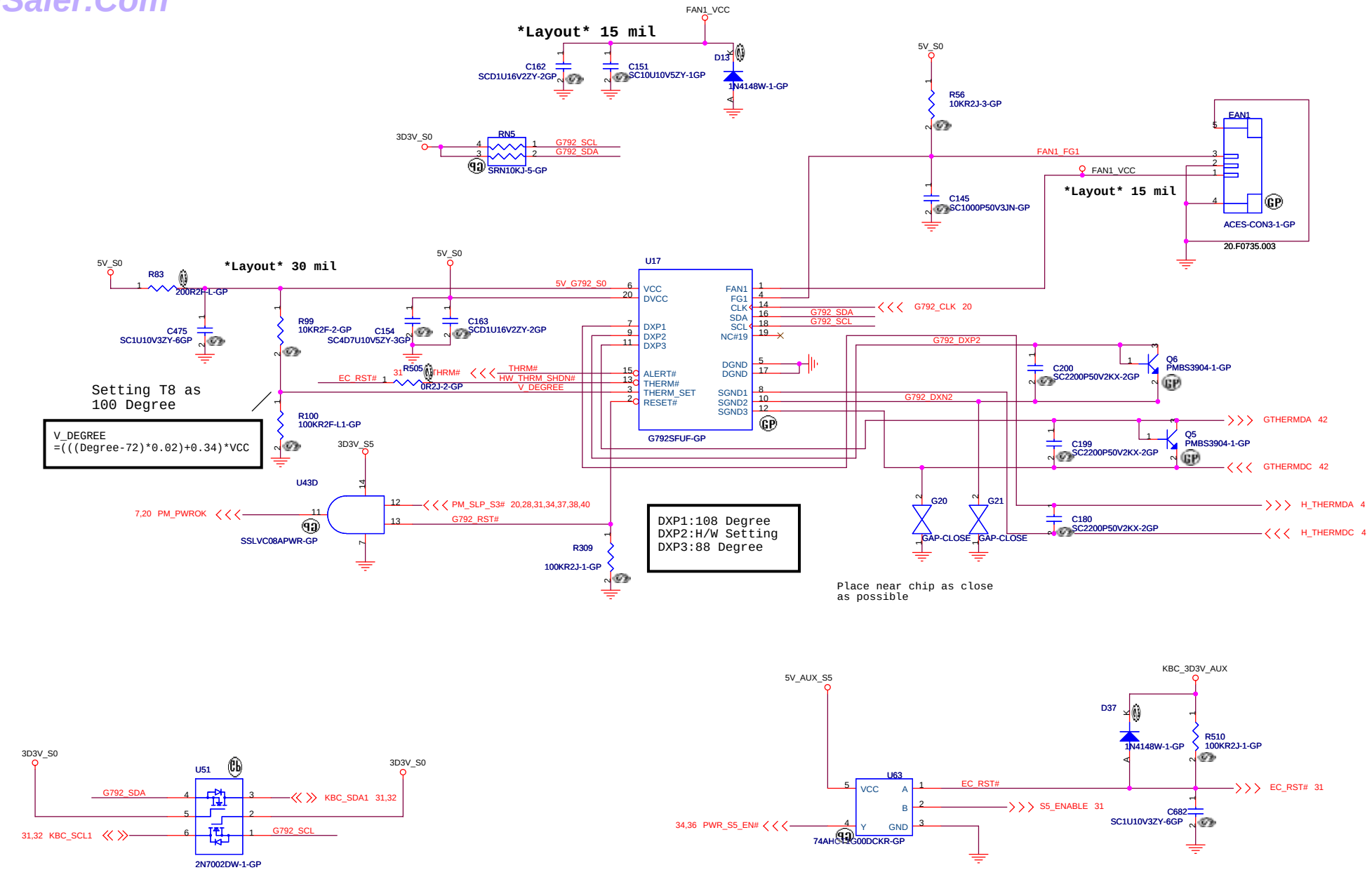
Within 500 mils

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(3/4) PM,USB,GPIO
Size: Custom
Document Number: Pamirs-Discrete
Rev: SA
Date: Monday, December 18, 2006
Sheet 20 of 47





<Core Design>

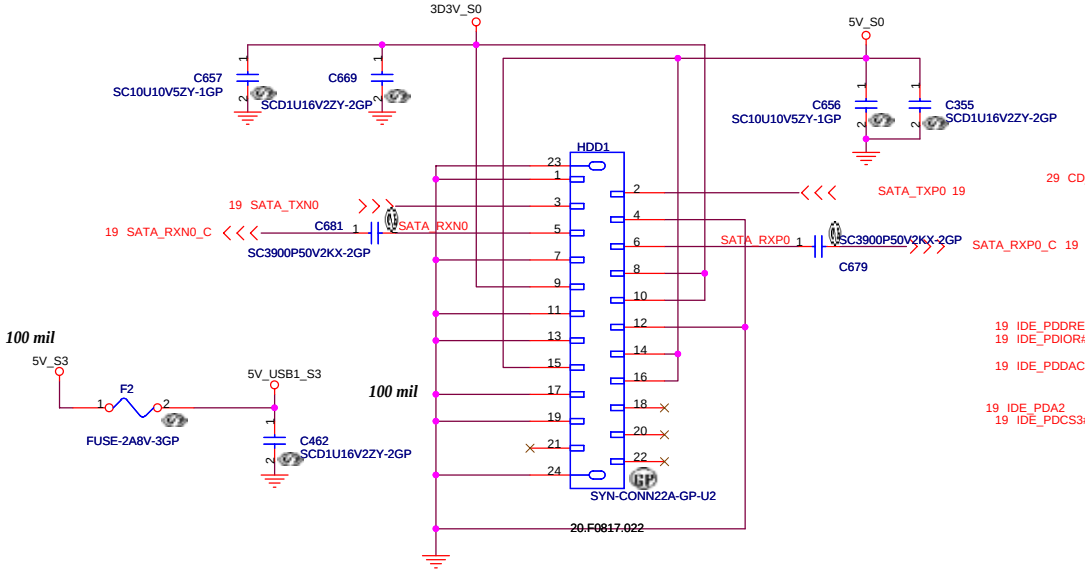
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

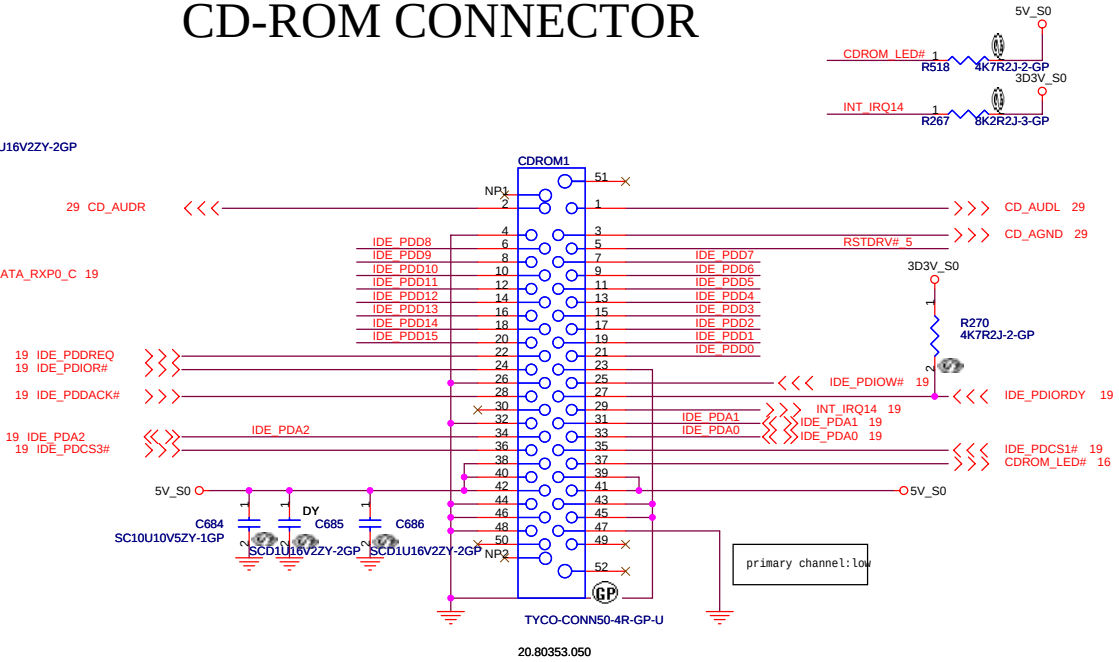
Size	Document Number	Rev
Custom	Pamirs-Discrete	SA

Date: Monday, October 23, 2006 Sheet 22 of 47

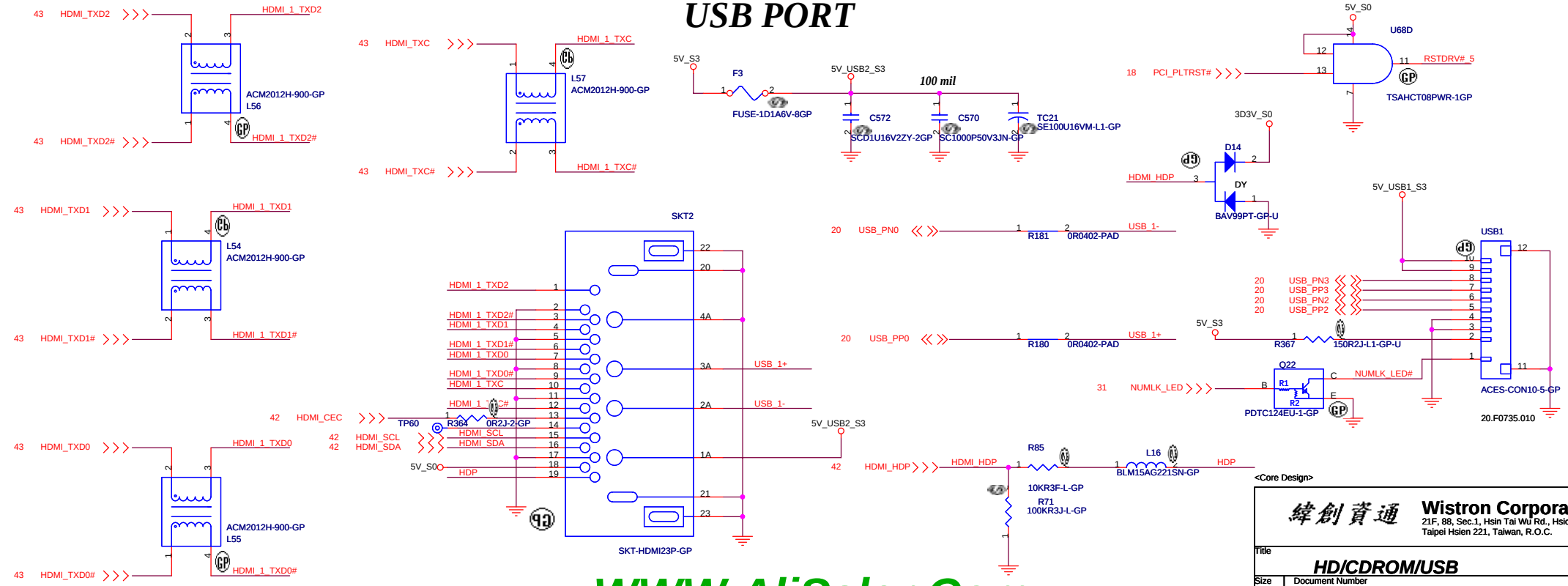
SATA HD Connector



CD-ROM CONNECTOR



USB PORT



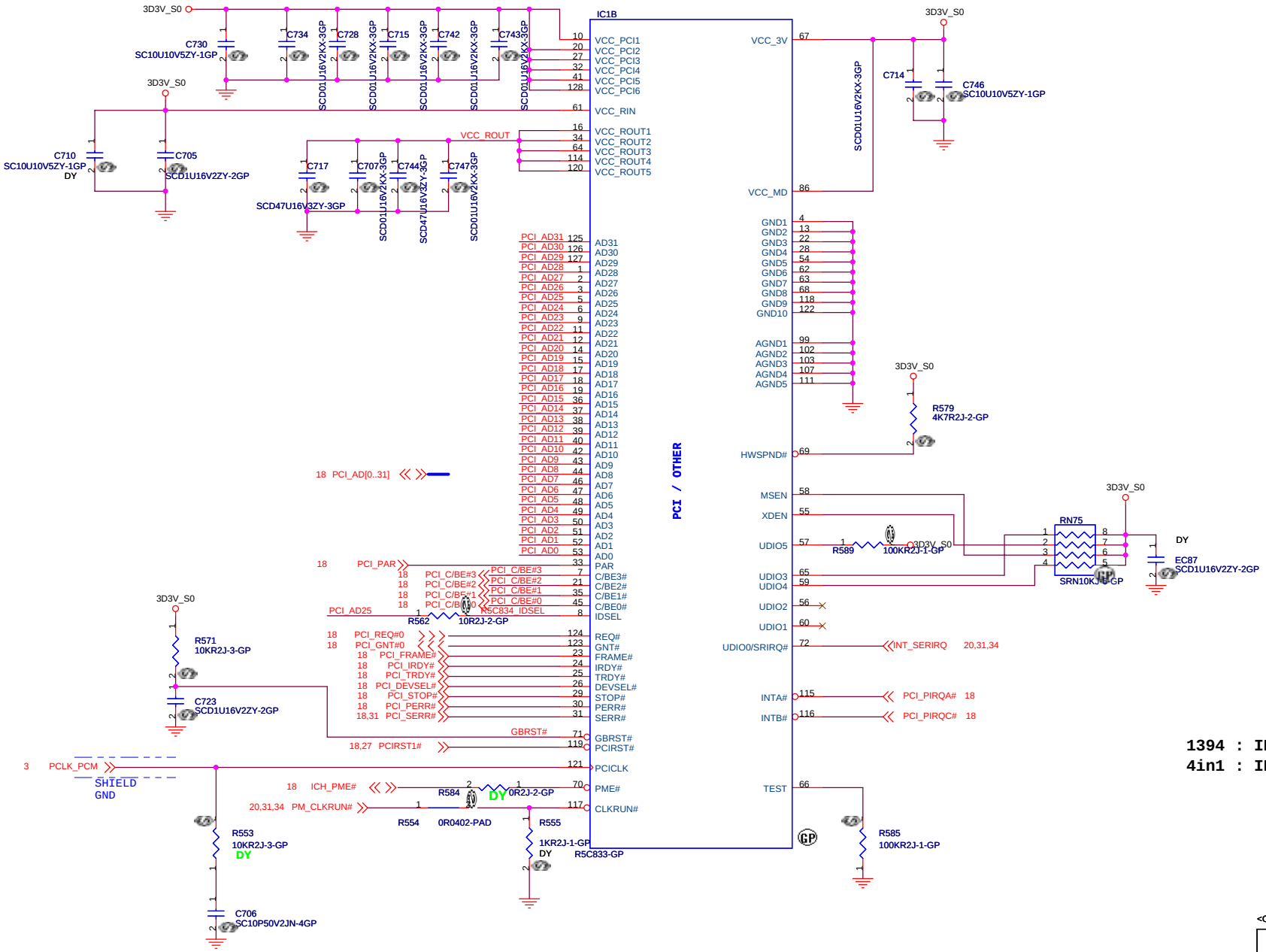
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HD/CDROM/USB

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Tuesday, December 12, 2006 Sheet 23 of 47



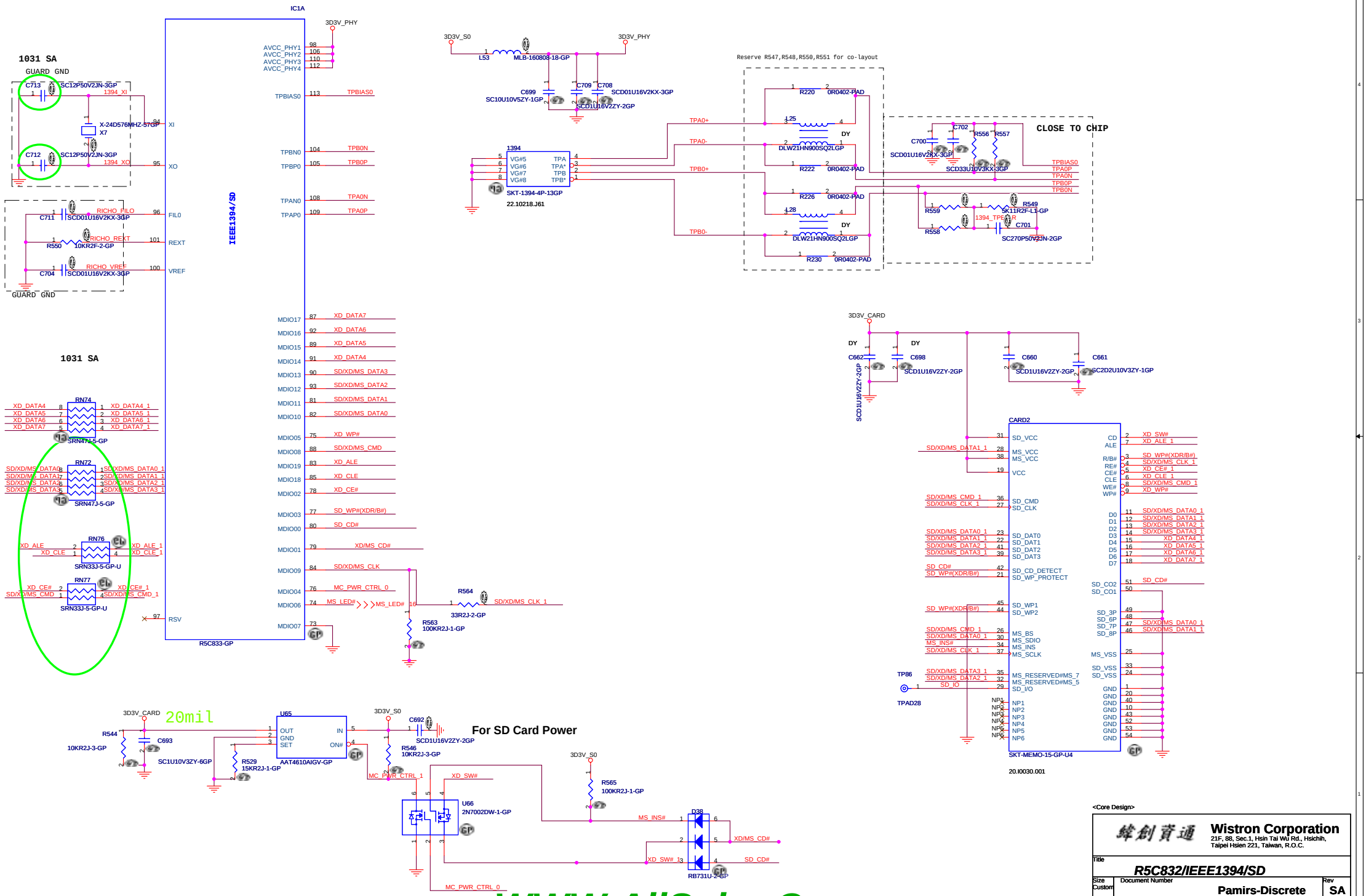
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Wednesday, December 06, 2006 Sheet 24 of 47



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

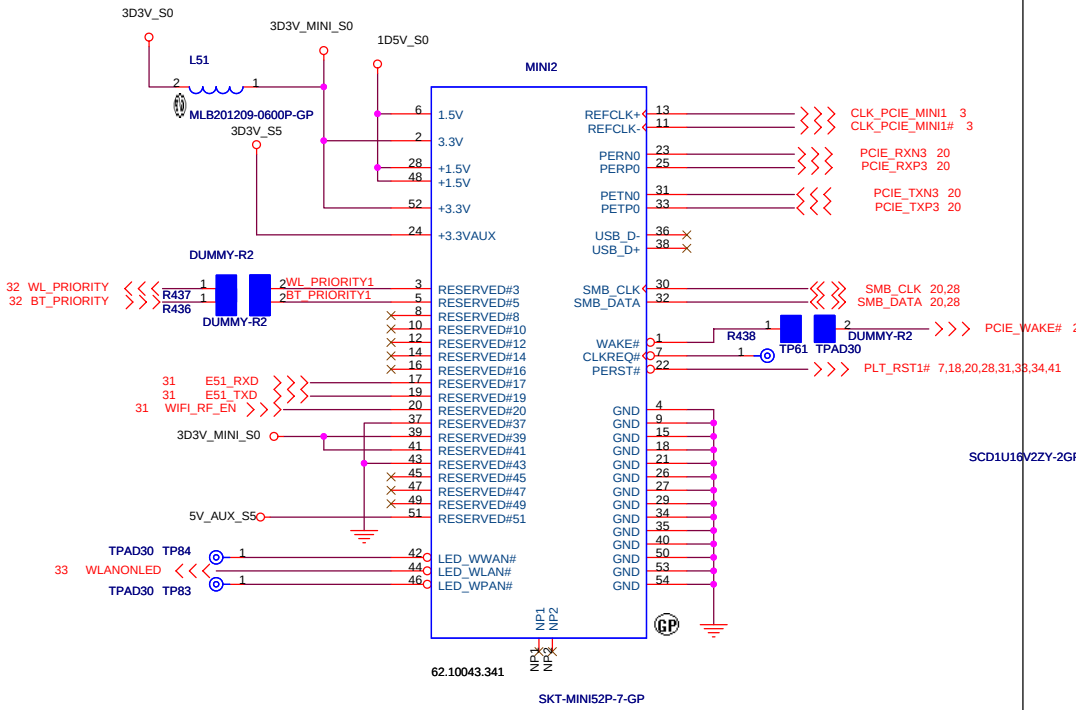
Title: R5C832/IEEE1394/SD

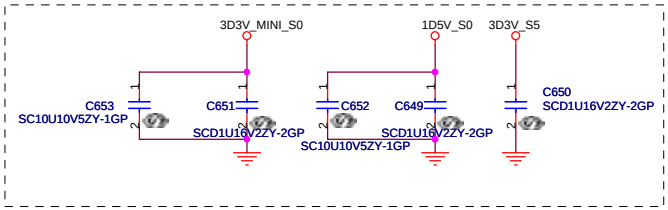
Size: Custom | Document Number: Pamirs-Discrete | Rev: SA

Date: Friday, December 15, 2006 | Sheet 25 of 47

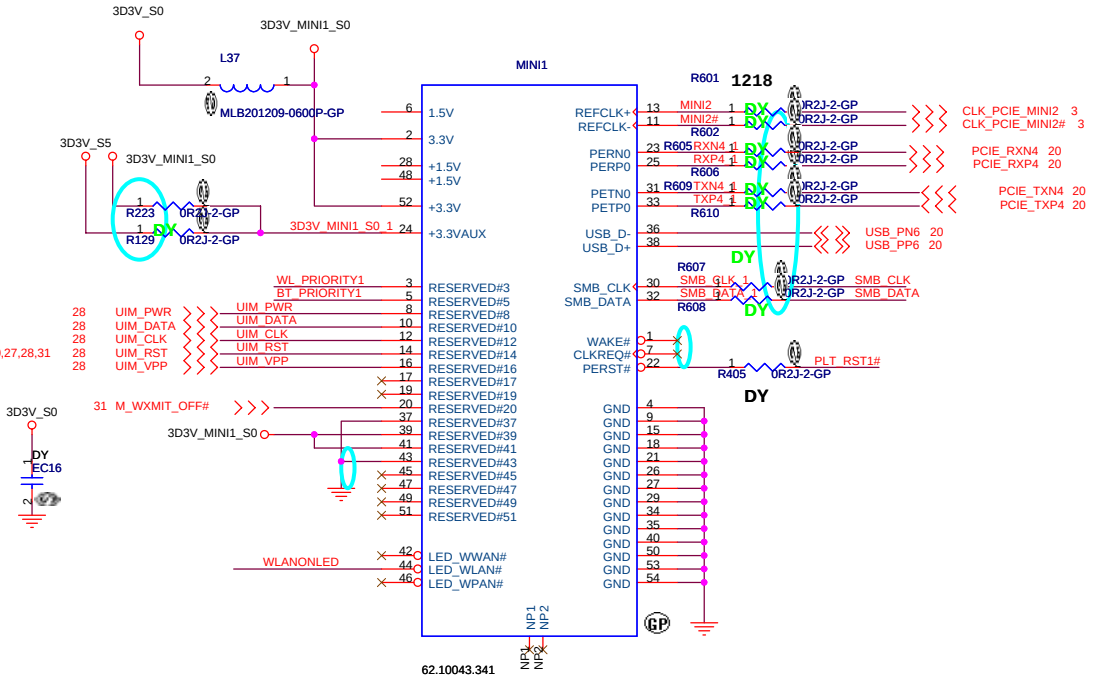
Mini Card Connector 2

Wireless card





Mini Card Connector 1 WWAN



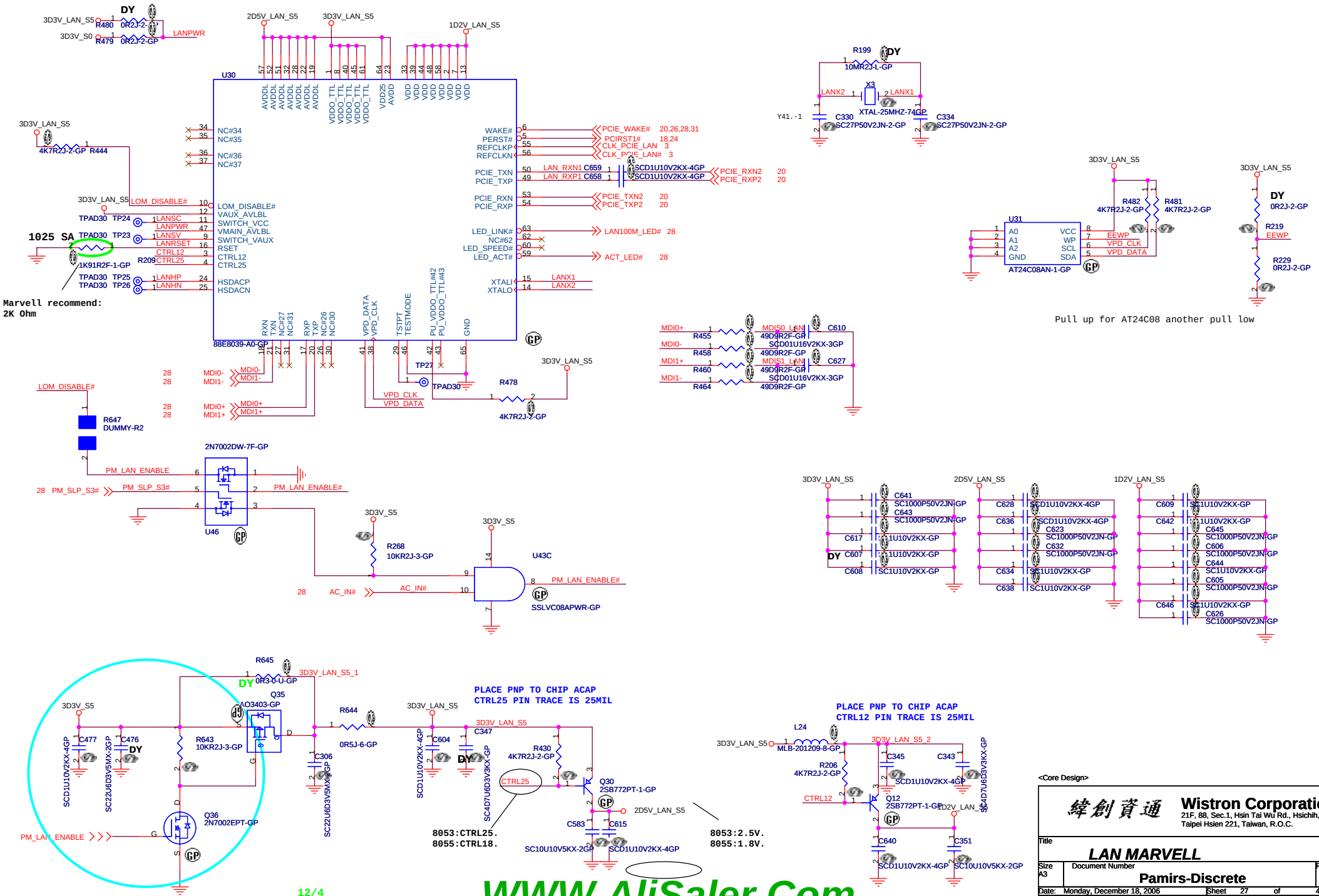
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Tuesday, December 19, 2006 Sheet 26 of 47



<Core Design>

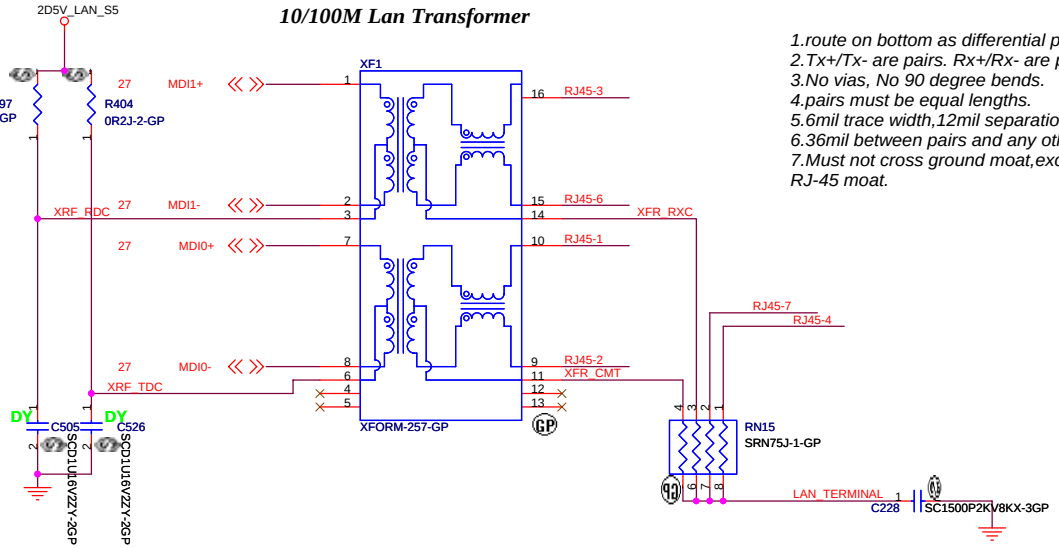
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN MARVELL

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

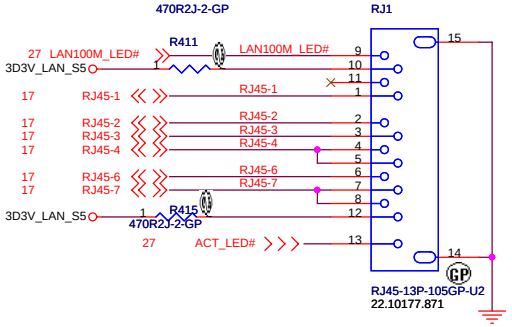
Date: Monday, December 18, 2006 Sheet 27 of 47

10/100M Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

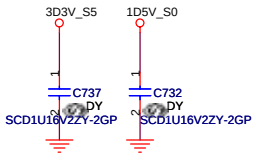
PIN09 : GREEN
PIN11 : ORANGE
PIN13 : YELLOW



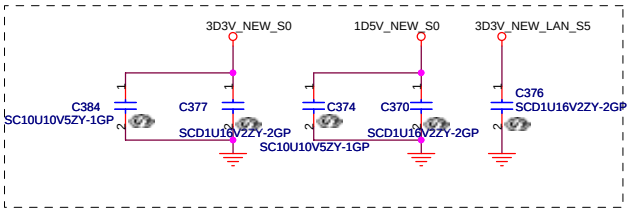
Green : Link up
Blinking : TX/RX activity

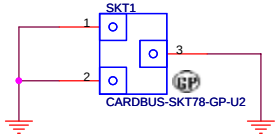
NEWCARD Connector

Place them Near to Chip

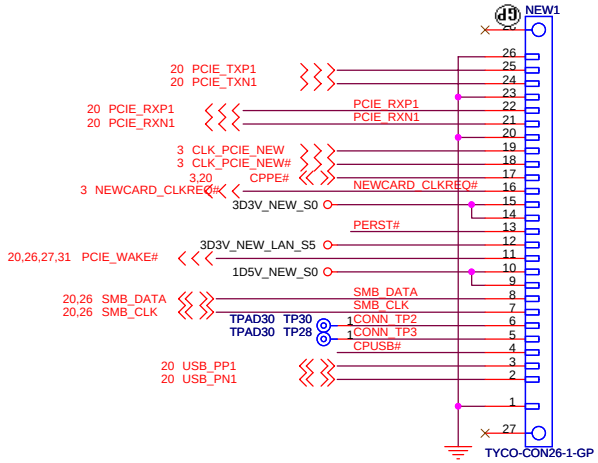


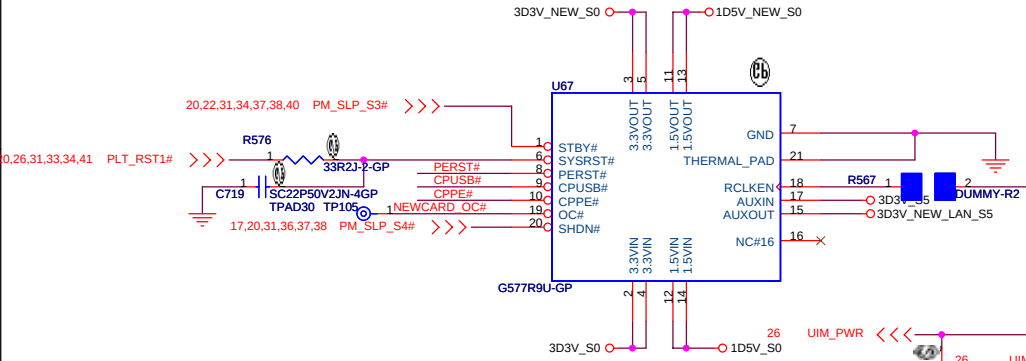
Place them Near to Connector

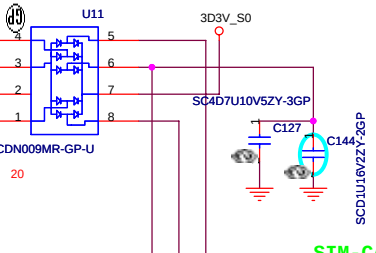




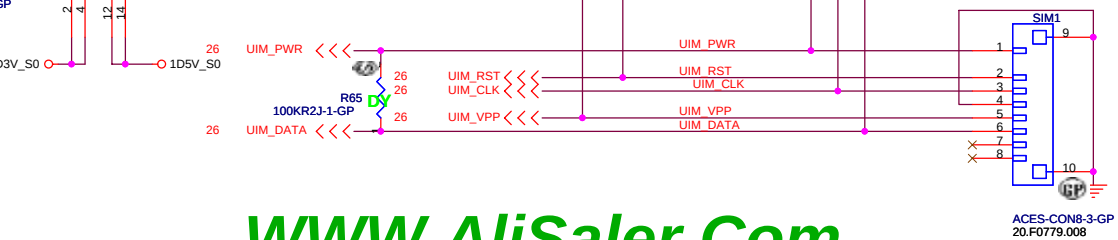
For Newcard socket

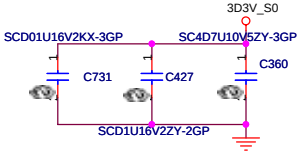






SIM-CARD





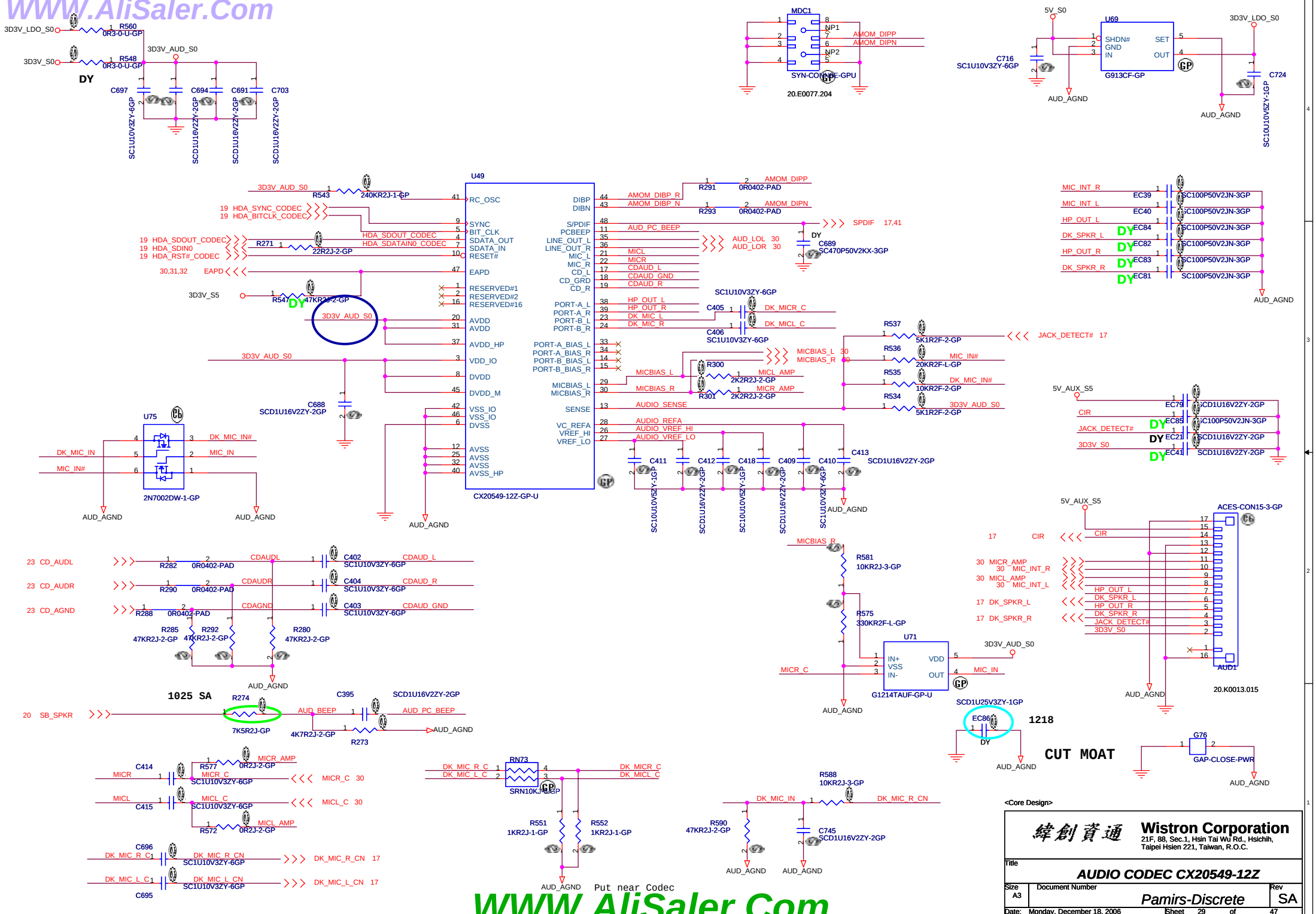
<Core Design>

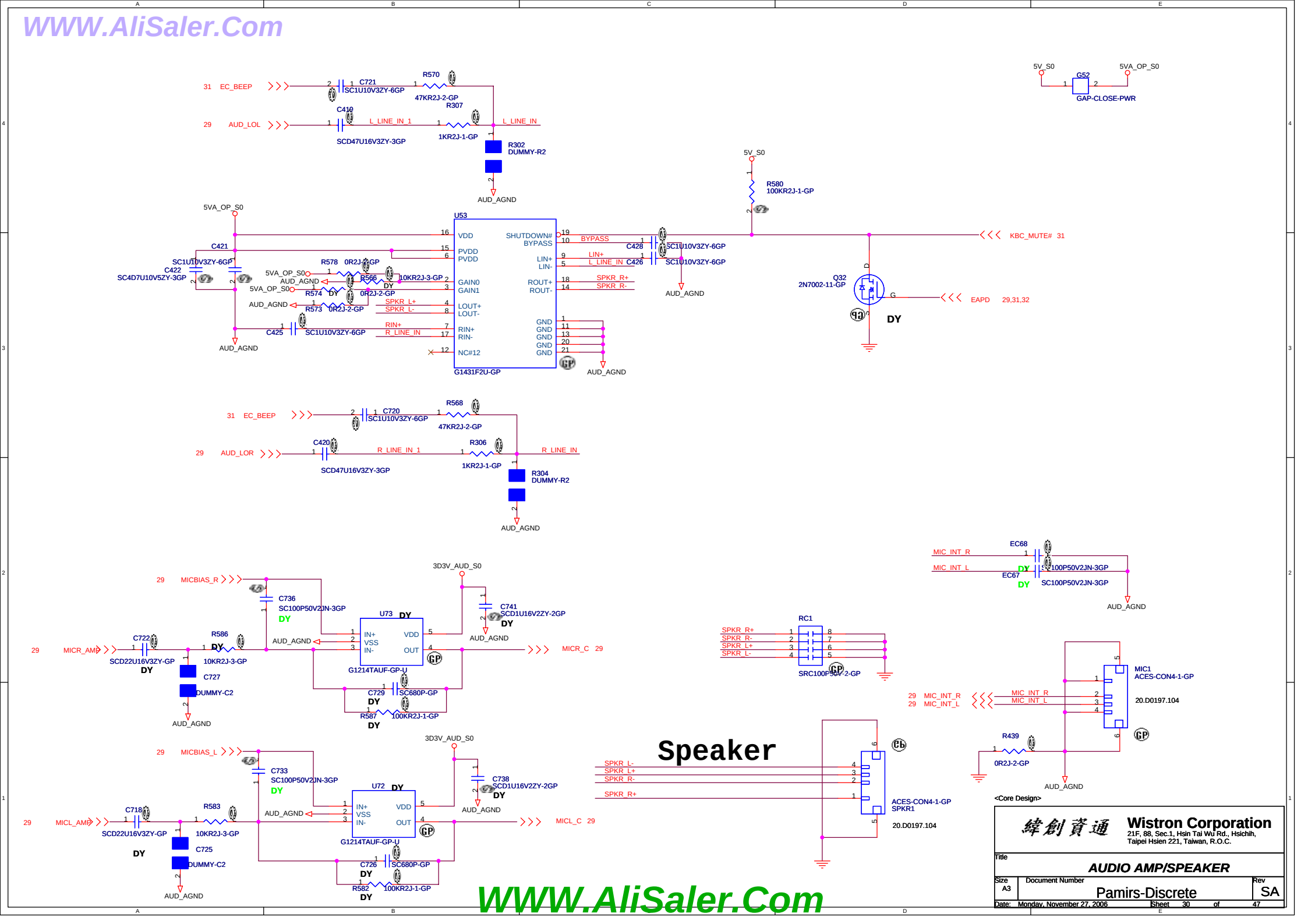
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN connector/NEW CARD/SIM

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Tuesday, December 12, 2006 Sheet 28 of 47



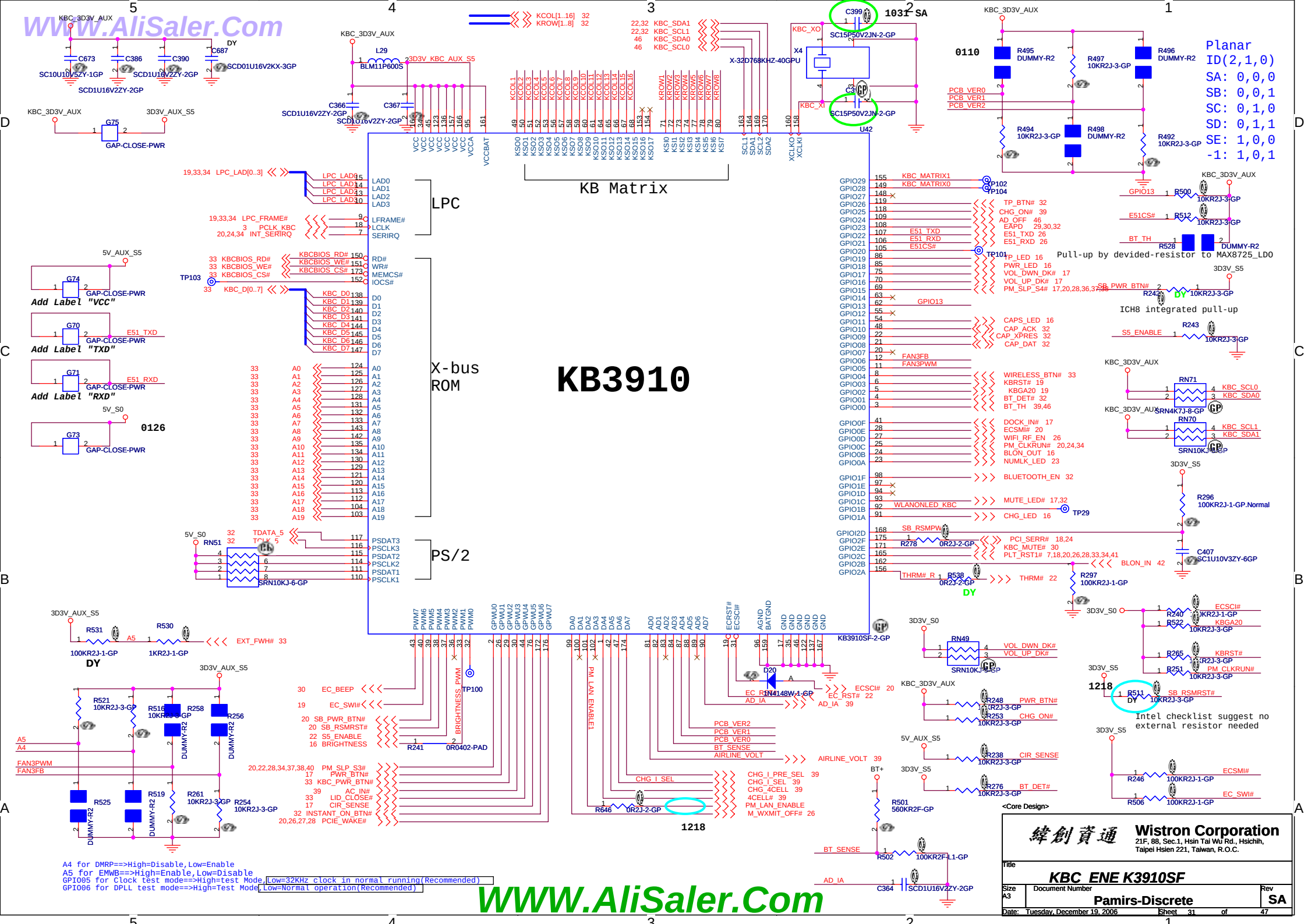


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO AMP/SPEAKER***

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Monday, November 27, 2006 Sheet 30 of 47



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	KBC_ENE K3910SF
Size A3	Document Number: Pamirs-Discrete
Rev	SA
Date: Tuesday, December 19, 2006	Sheet 31 of 47

CAMERA

Blue thumb

Internal KeyBoard Connector

31 KROW[1..8]
31 KCOL[1..16]

KB1
ACES-CON24-2-GP
20.K0220.024

Keyboard matrix (from vendor)

	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1

TouchPad Connector

TPAD1
FOX-CON4-12-GP
SA 1011

TOUCH-PAD SWITCH

SW1
SW-TACT-68-GP-U
62.40009.451

CAPACITY BUTTON

CAP1
ACES-CON12-4-GP
20.K0228.012

BT1
ACES-CON8-4-GP
20.F0772.008

Close to CN8

CAM1
ACES-CON5-1GP
20.D0197.105

MAX 150mA

for EMI

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KeyBoard-CONN
Size: A3
Document Number: Pamirs-Discrete
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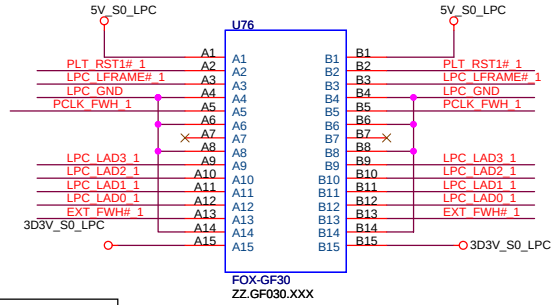
Date: Monday, December 18, 2006
Sheet 32 of 47

TOP VIEW

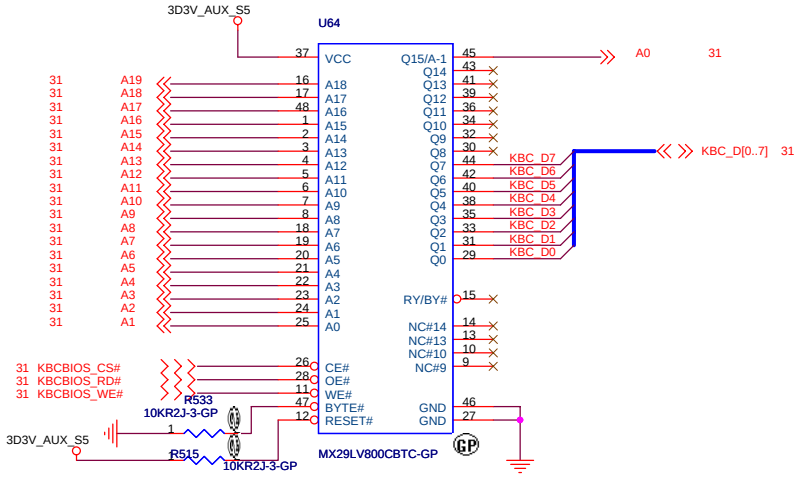
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

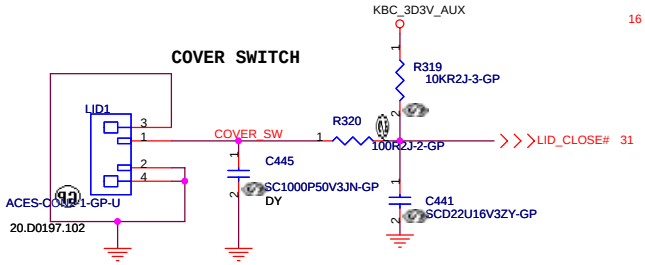
(BOTTOM VIEW)

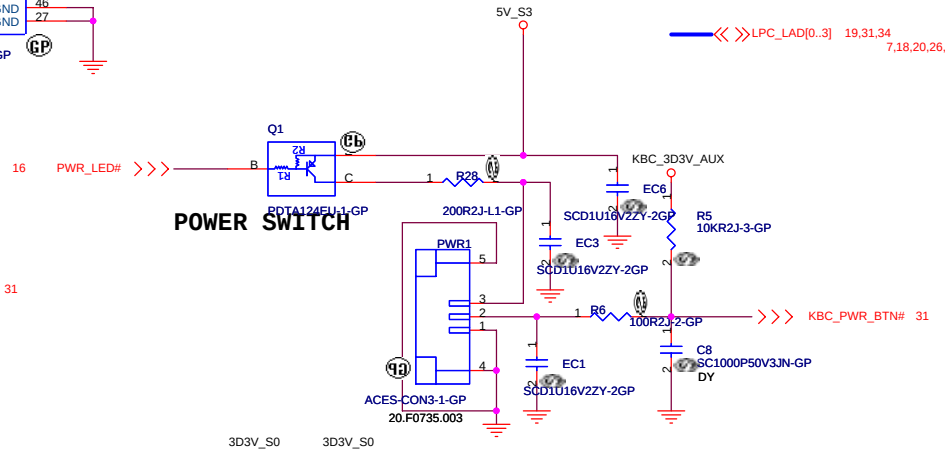
GOLDEN FINGER FOR DEBUG BOARD

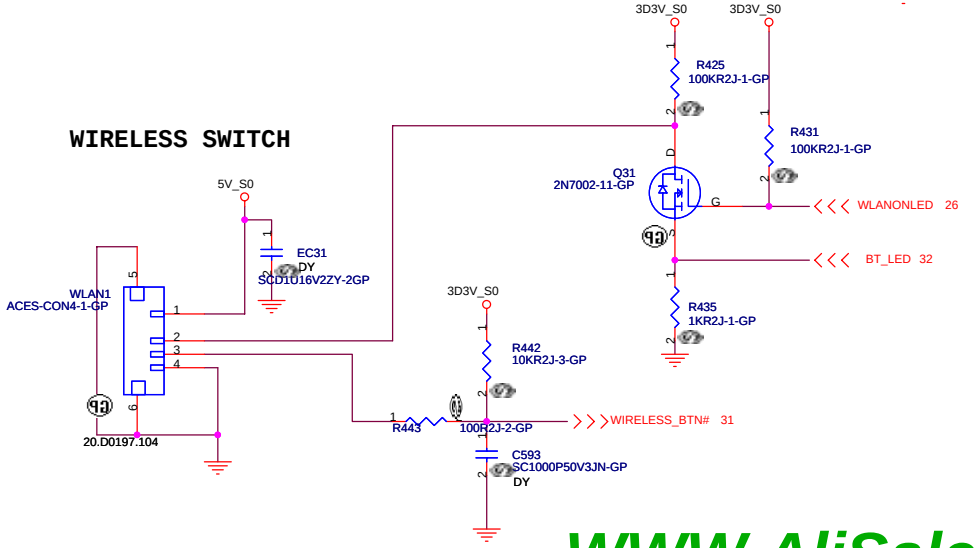


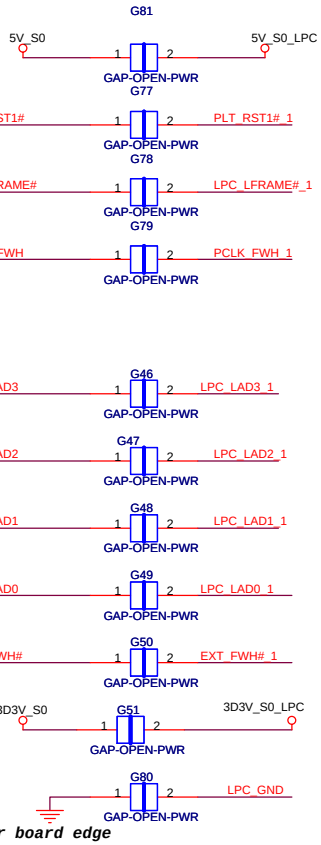
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46









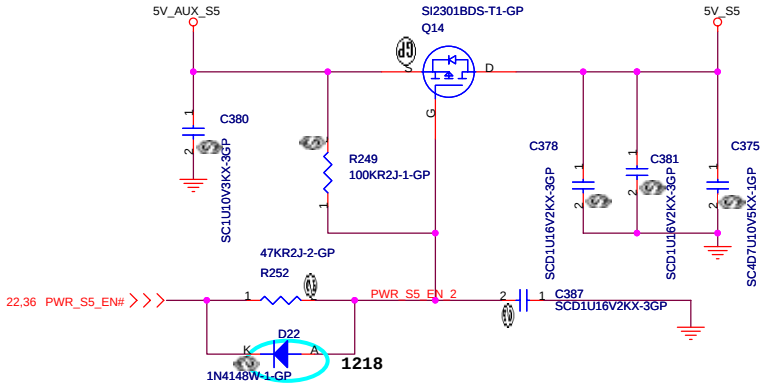


Put near board edge

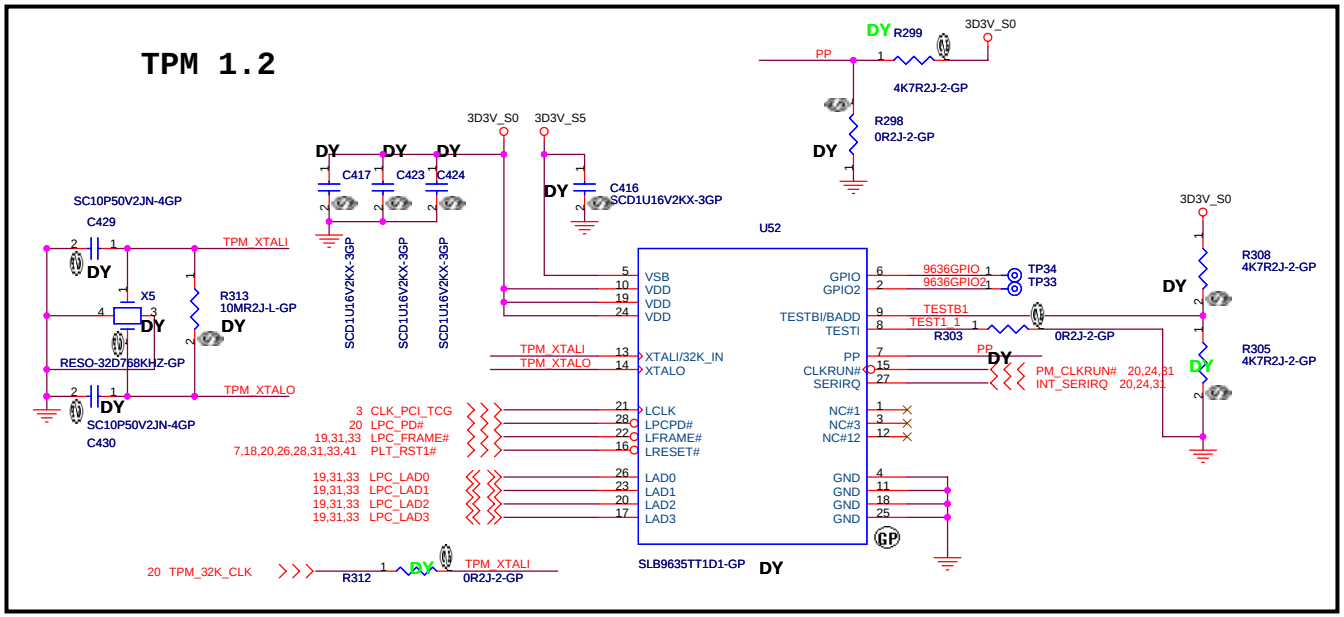
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **FWH and Debug**		
Size: A3	Document Number: **Pamirs-Discrete**	Rev: **SA**
Date: Thursday, November 02, 2006	Sheet 33 of 47	

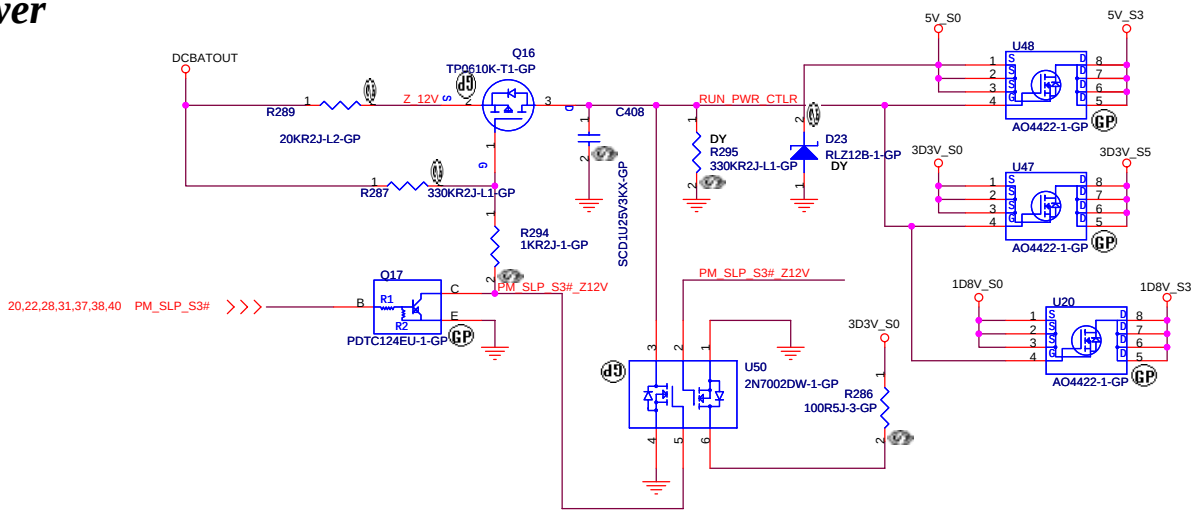
5V_AUX_S5 TO 5V_S5



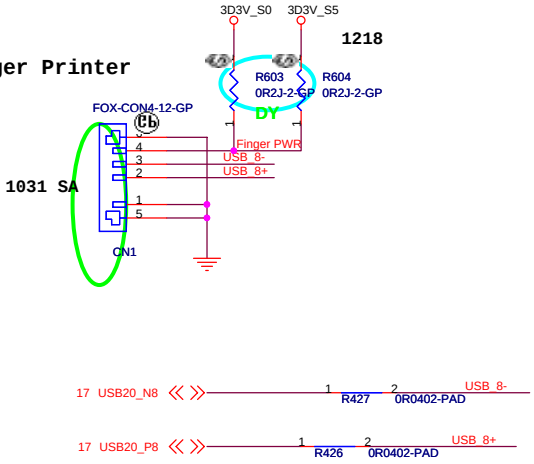
TPM 1.2



Run Power



Finger Printer



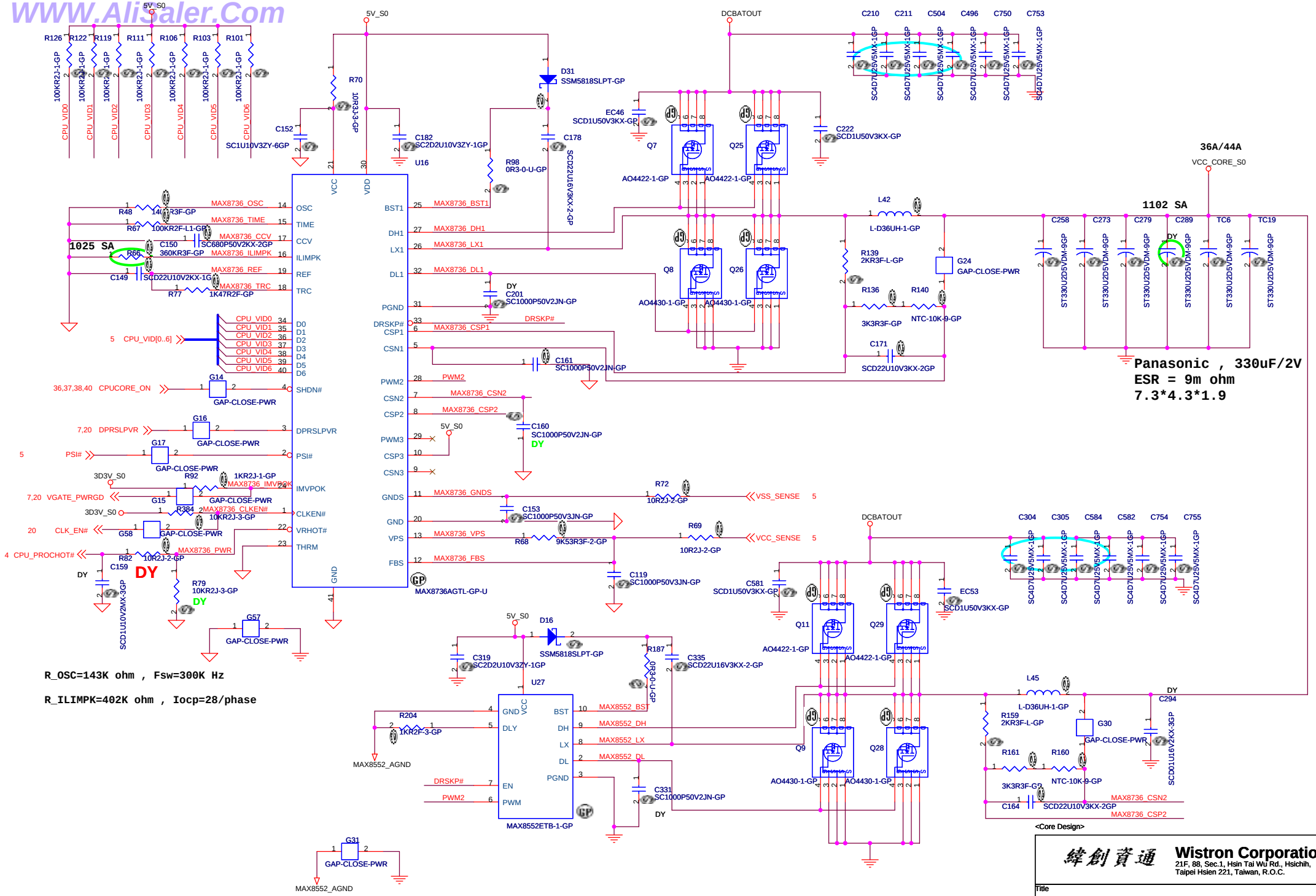
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWRPLANE&RESETLOGIC

Size	Document Number	Rev
A3	Pamirs-Discrete	SA

Date: Monday, December 18, 2006 Sheet 34 of 47



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC-DC VCCCPUCORE
Size	A3
Document Number	Pamirs-Discrete
Rev	SA
Date:	Wednesday, December 13, 2006
Sheet	35 of 47

0707 Change 5V_S5 to 5V_S3
0718 Change 3D3V_AUX_S5 to 3D3V_S5

U44 TPS51120RHBR-GPU1 74.51120.073

8/10

8/10

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

GS 10*10*4 4D7uH
DCR<25mohm, Isat=6A

5V Iomax=5A
OCP>10A

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

NEC 220uF ,V size
ESR=25mohm
Iripple=2.2A

3D3V Iomax=4A
OCP>8A

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

GS 10*10*4 4D7uH
DCR<25mohm, Isat=6A

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

NEC 220uF ,V size
ESR=25mohm
Iripple=2.2A

Vout=1V*(R1+R2)/R2

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_S3/3D3V_S5

Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Friday, December 08, 2006 | Sheet 36 of 47

Iocp=7.0 2 = 14A*
Rds,on=17m ohm
*Vcs1=Iocp*Rds,on=238mV*
VILIM=Vcs1/0.1=2.38V

*Iocp=7.0*2 = 14A*
Rds,on=17m ohm
*Vcs2=Iocp*Rds,on=28mV*
VILIM2=Vcs2/0.1=2.38V

1D8V / 7.0A
OCP>=14A

1D05V_S0/5A
OCP>=10A

NEC
Irms=7.5A(Isat=10.4A)
DCR=13mohm
12*12*5.5
1102 SA

Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

Panasonic 220uF/2D5V
ESR=15m ohm
Iripple=2.7 A

Panasonic 220uF/2V
ESR=15m ohm
Iripple=2.7 A

Vout=Vfb*(1+(R1/R2))
Where Vfb=1.0V,R2=10Kohm

Voutsetting=1.820V

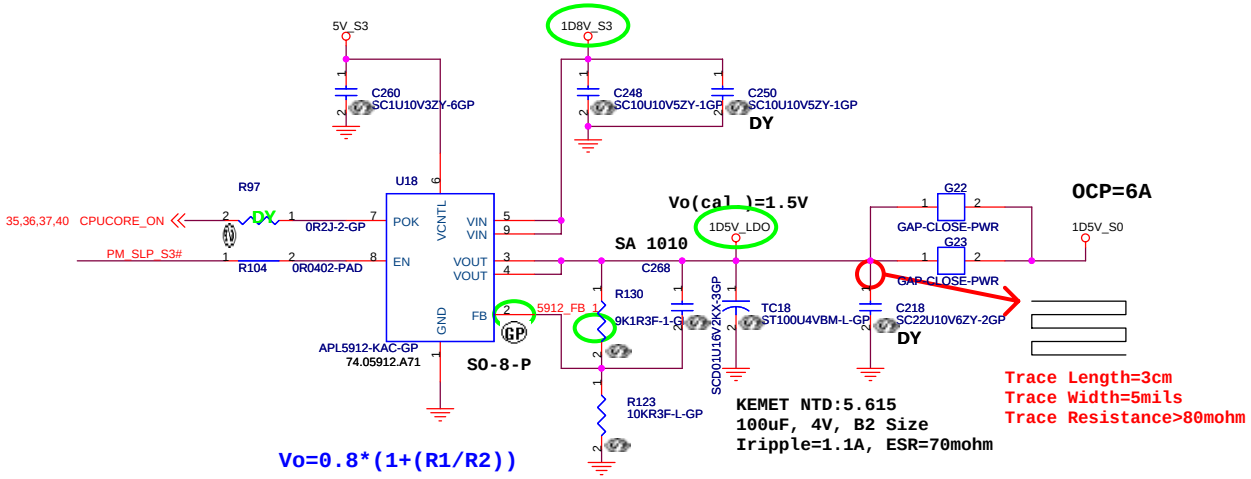
Voutsetting=1.0511V

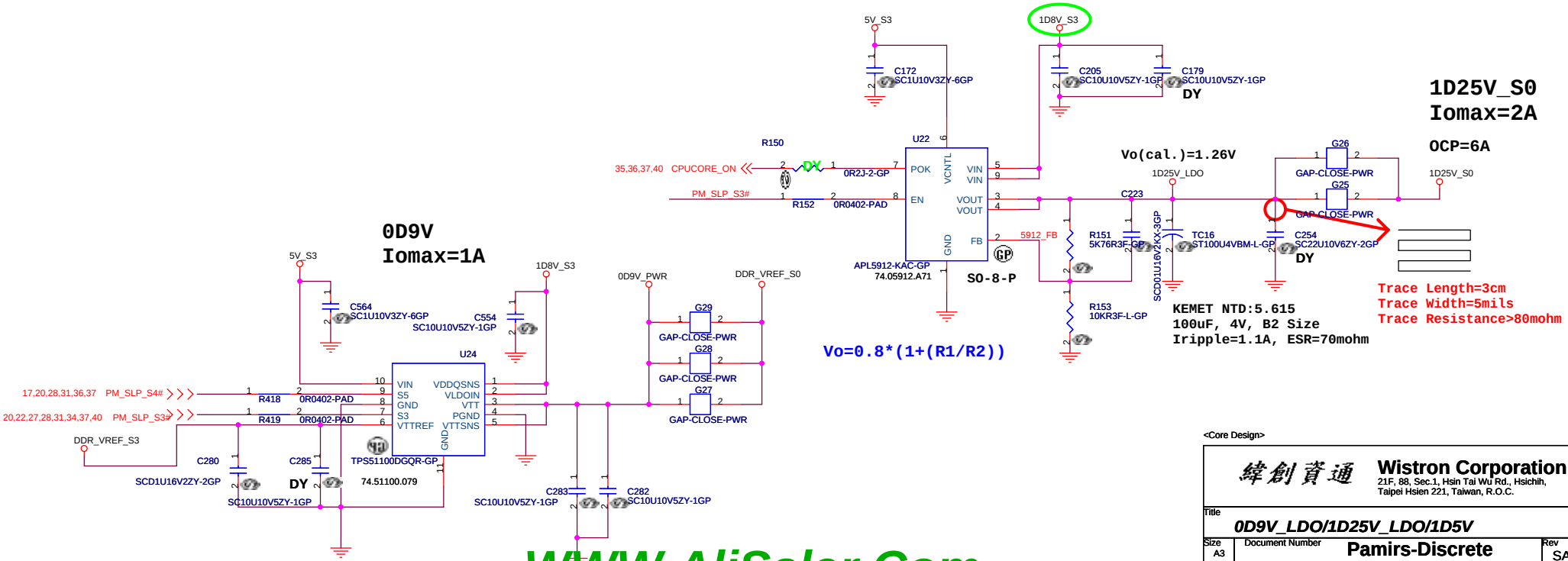
Ton	Frequency (Out1)KHz	Frequency (Out2)KHz
AGND	620	460
REF	485	355
OPEN	345	255
VCC	235	170

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_S3/1D05V_S0
Size: A3
Document Number: Pamirs-Discrete
Rev: SA
Date: Monday, December 18, 2006
Sheet 37 of 47





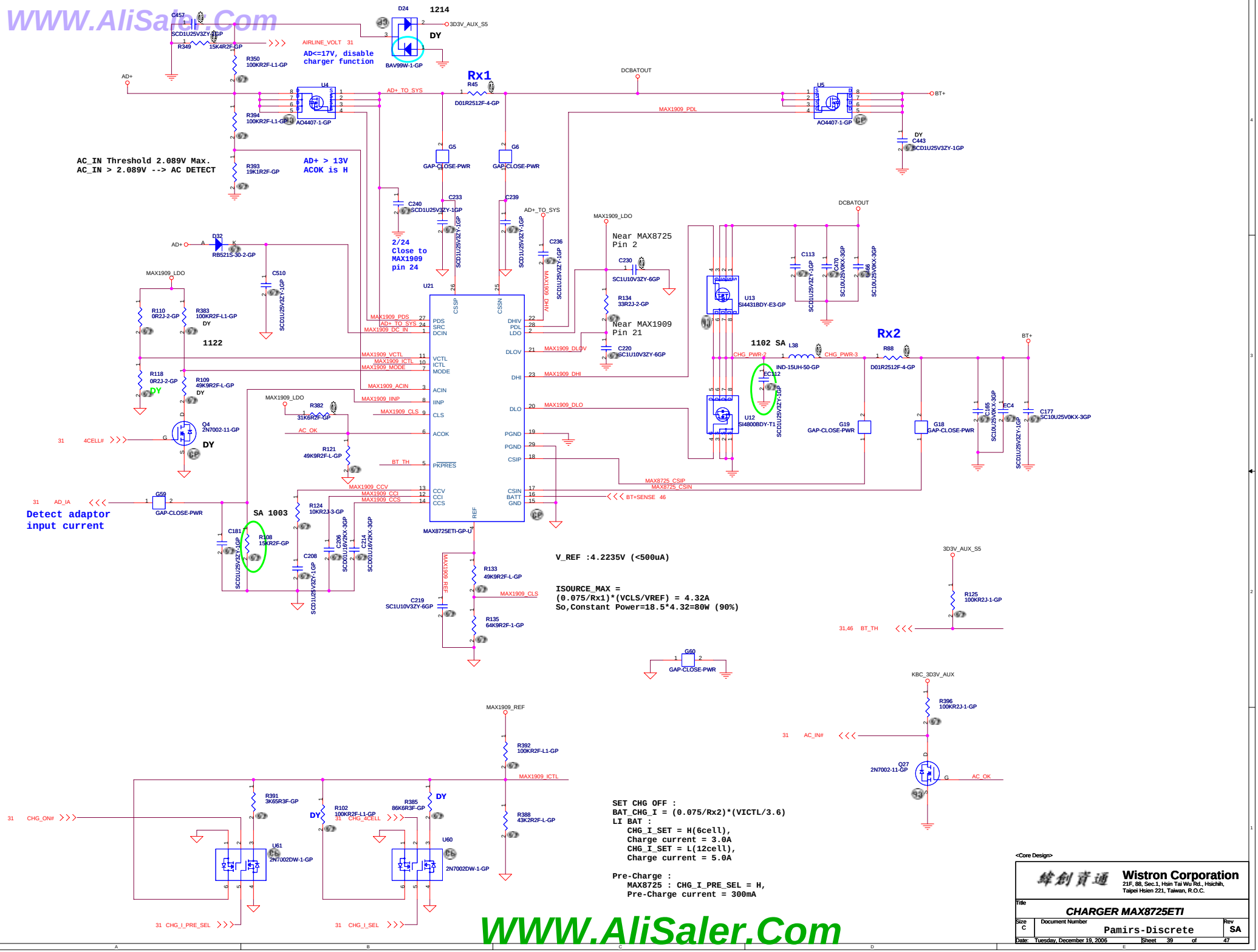
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

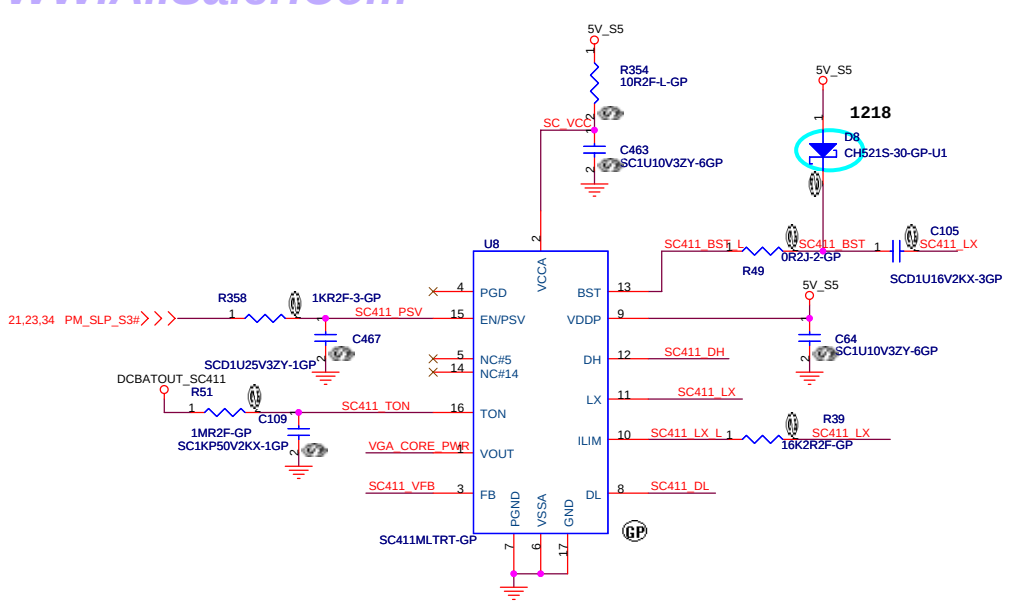
Title: 0D9V_LDO/1D25V_LDO/1D5V

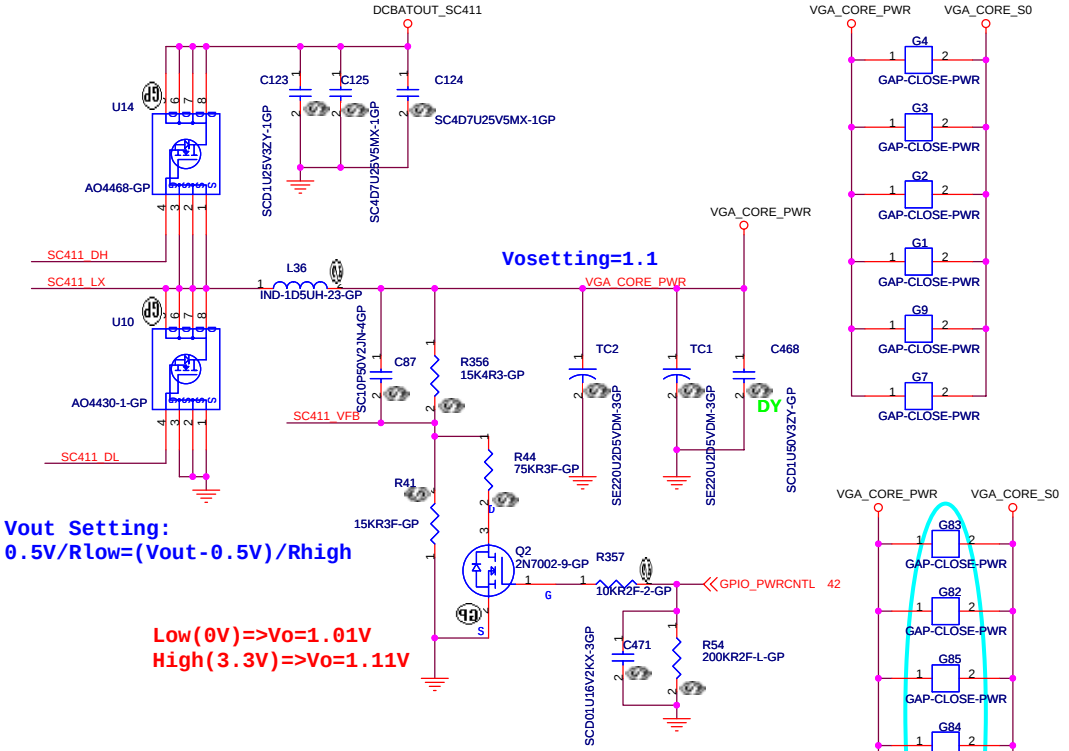
Size: A3 | Document Number: Pamirs-Discrete | Rev: SA

Date: Tuesday, November 07, 2006 | Sheet 38 of 47



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CHARGER MAX8725ETI
Size: C
Document Number: Pamirs-Discrete
Rev: SA
Date: Tuesday, December 19, 2006
Sheet 39 of 47

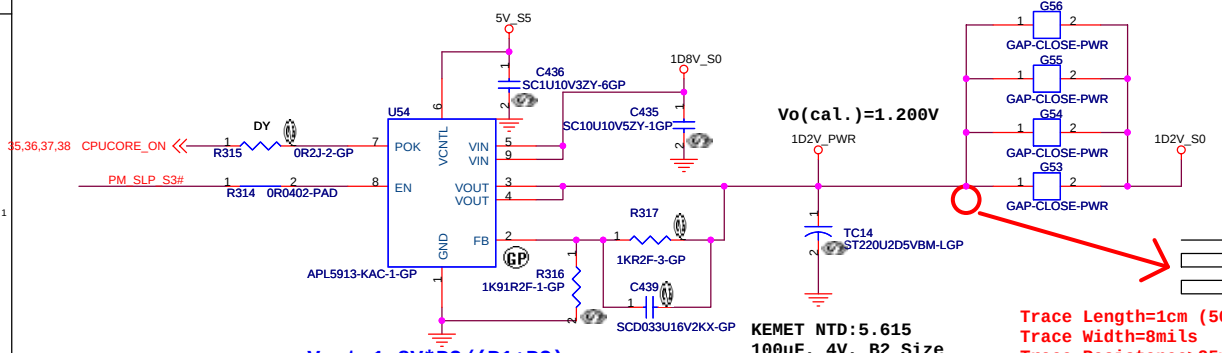




Vout Setting:
0.5V/Rlow=(Vout-0.5V)/Rhigh

Low(0V)=>Vo=1.01V
High(3.3V)=>Vo=1.11V

1D2V_S0
Iomax=3A



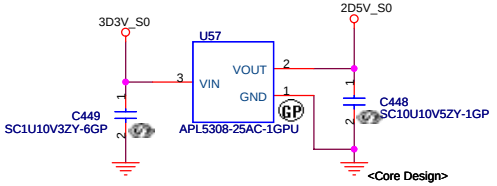
Vout=1.8V*R2/(R1+R2)

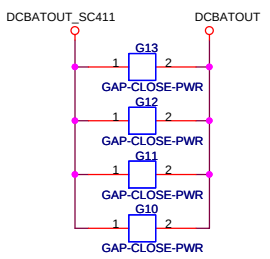
SO-8-P

KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

Trace Length=1cm (500mils)
Trace Width=8mils
Trace Resistance>25mohm

2D5V_S0
Iomax=300mA





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Title	**VGA CORE 1V**	
Size A3	Document Number **Pamirs-Discrete**	Rev **SA**
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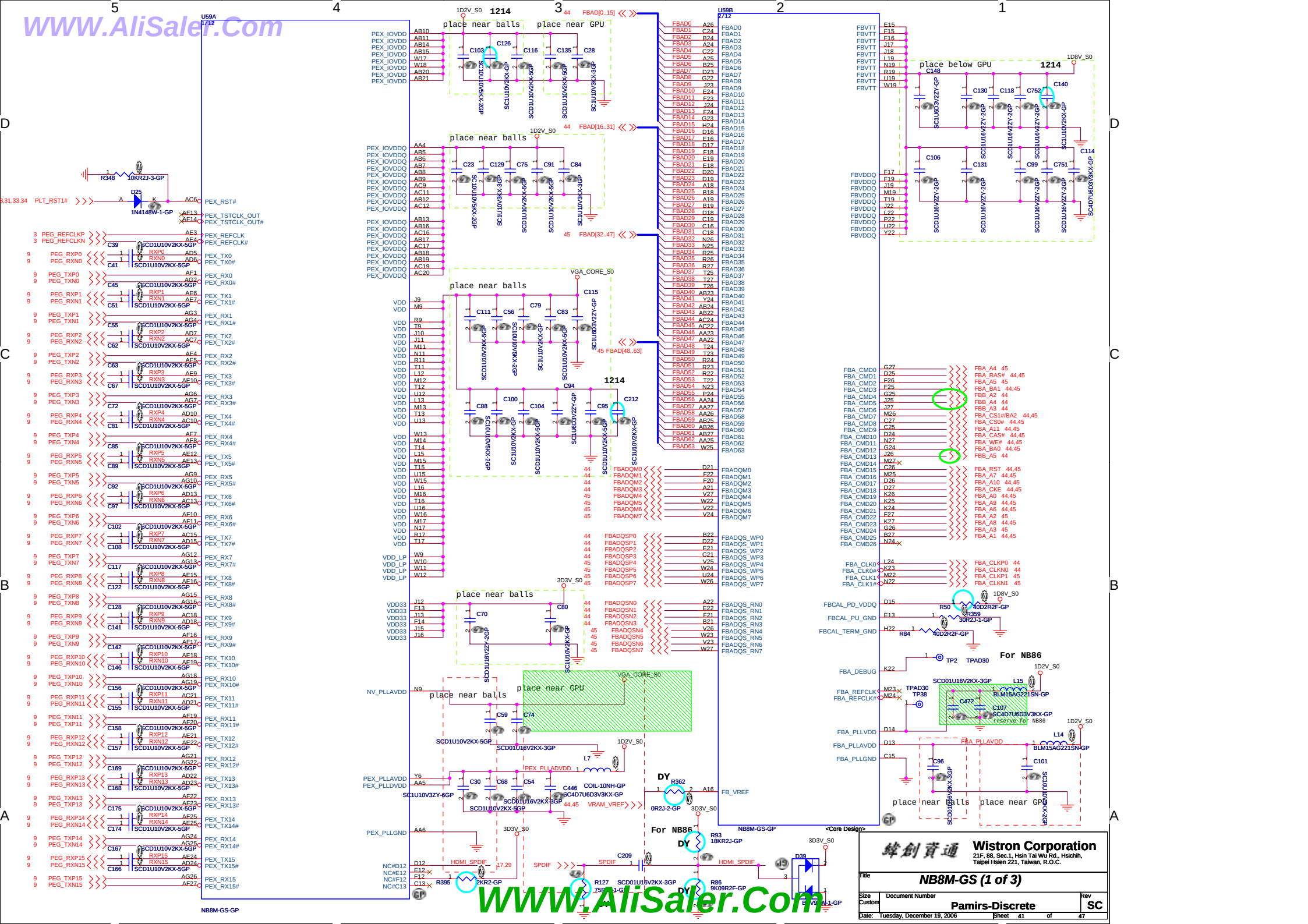

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Size: Custom | Document Number: Pamirs-Discrete | Rev: SC

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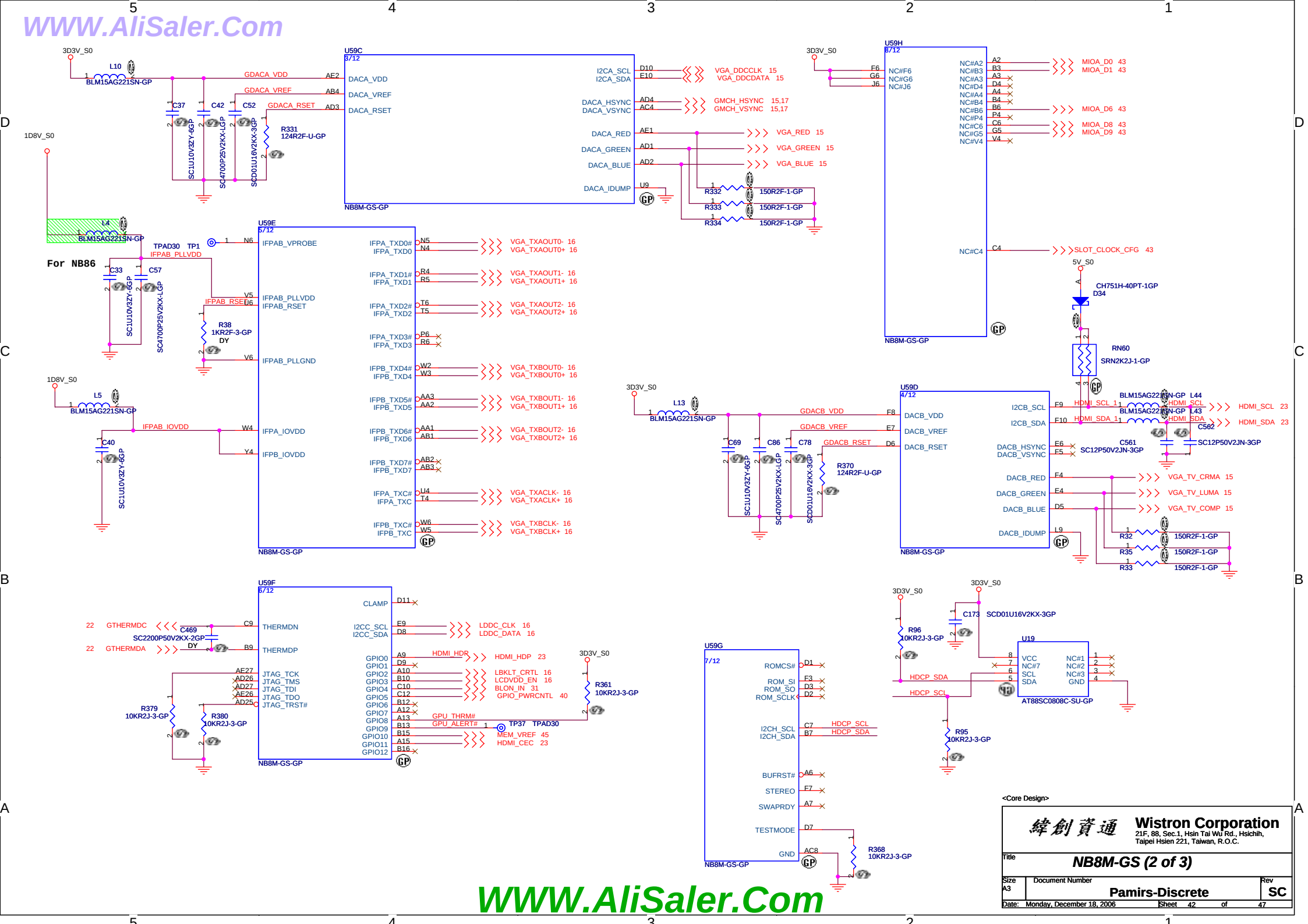

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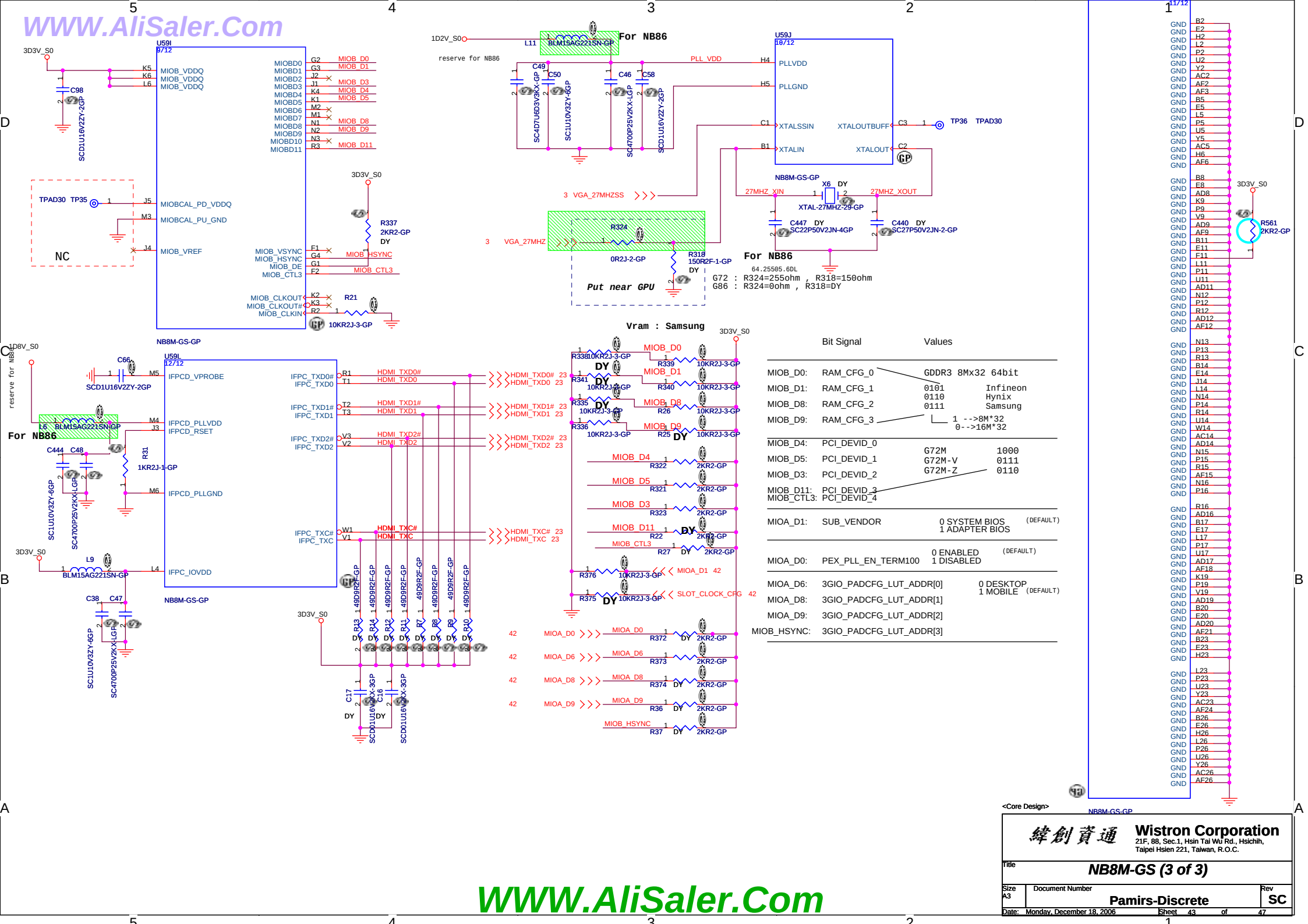

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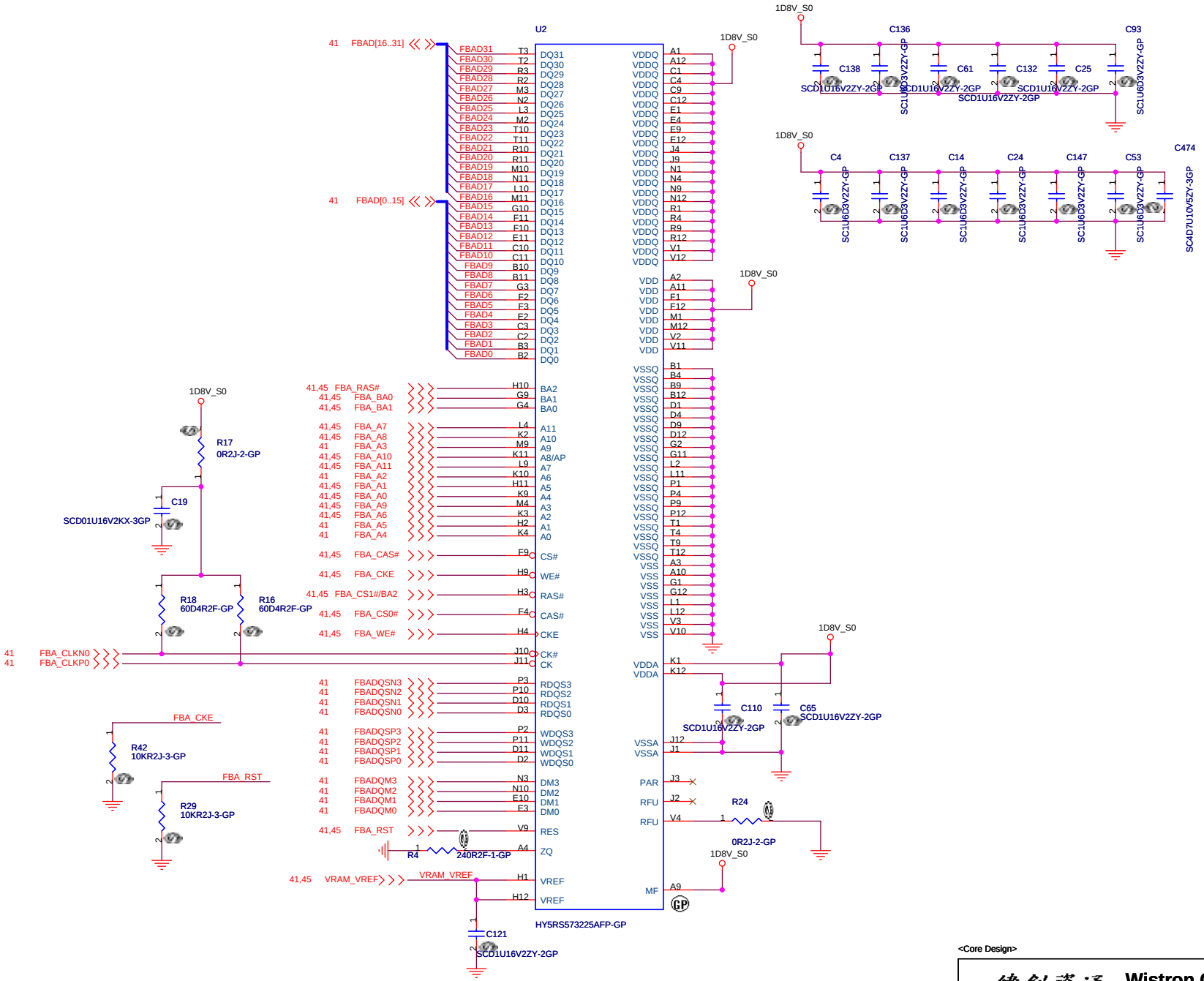

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Title	***VRAM1***
Size A3	Document Number **Pamirs-Discrete** Rev **SC**
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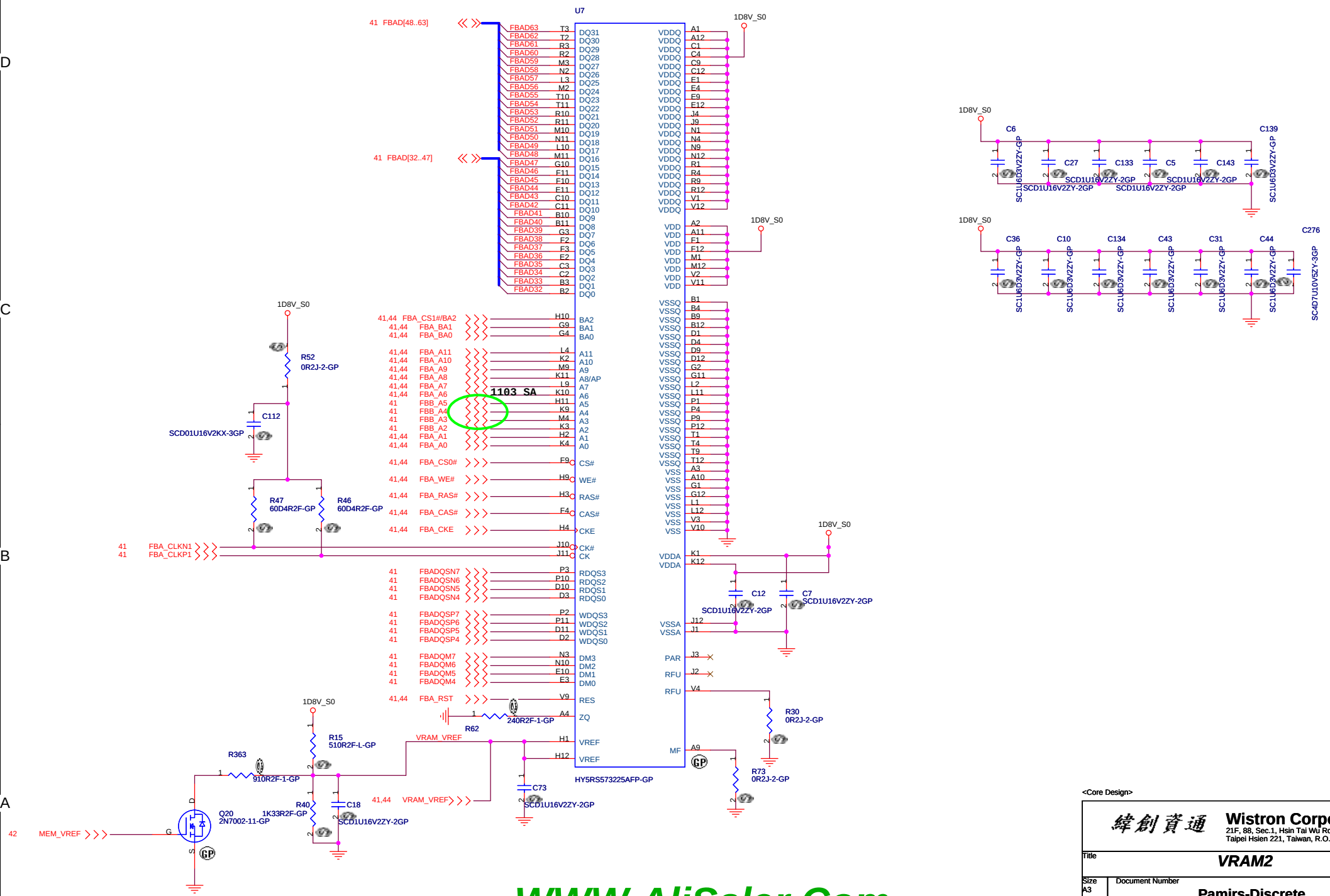

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Title: VRAM2

Size: A3 | Document Number: Pamirs-Discrete | Rev: SC

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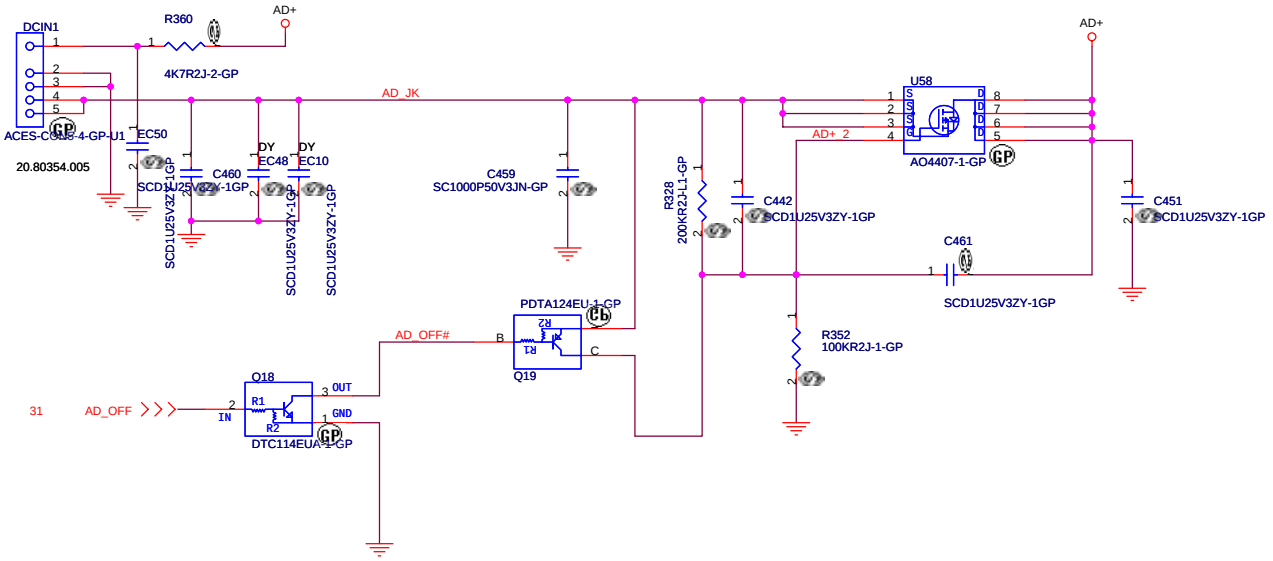
Adaptor in to generate DCBATOUT



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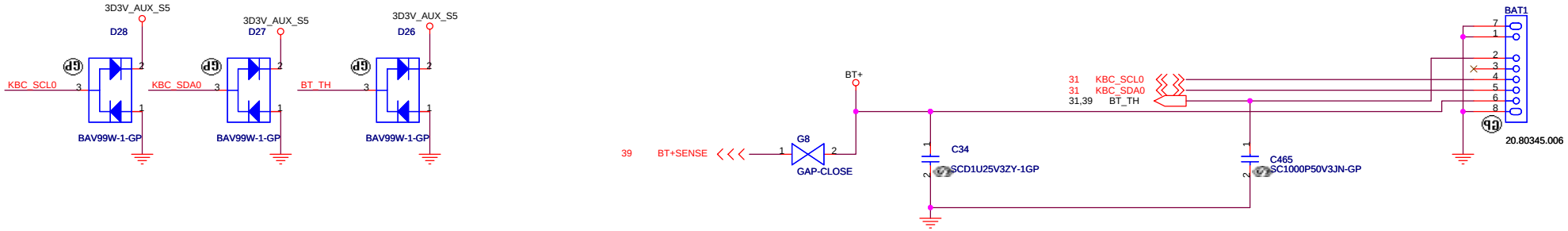

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Title	AD/BATT CONN	
Size A3	Document Number Pamirs-Discrete	Rev SC
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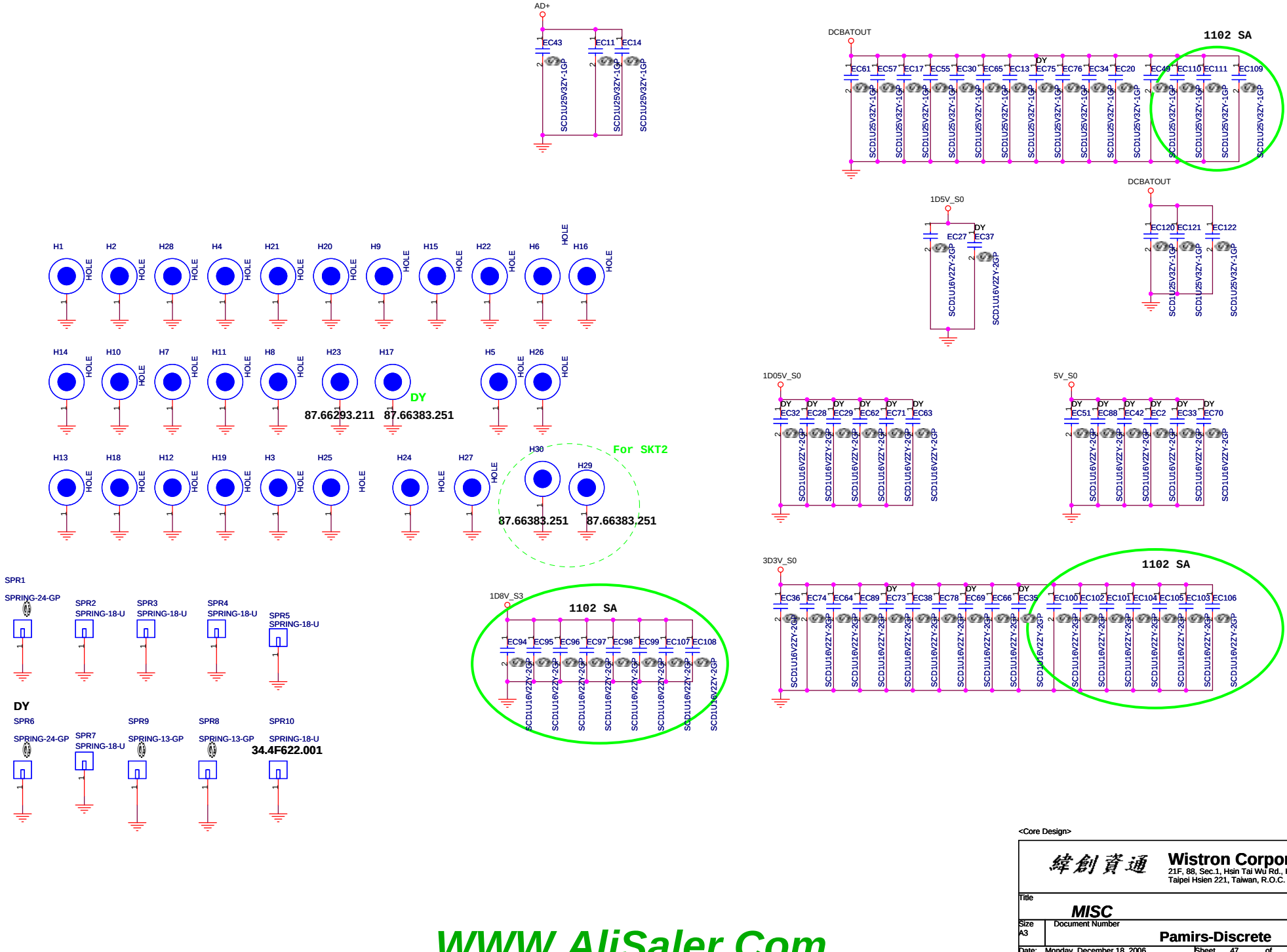

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Title: MISC

Size	Document Number	Rev
A3	Pamirs-Discrete	SC

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