Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M core logic

2008-05-22
REV：0.3

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.		
Title: Cover Sheet		
Size: Custom	Document Number: Montevina Consumer UMA	Rev: 0.3
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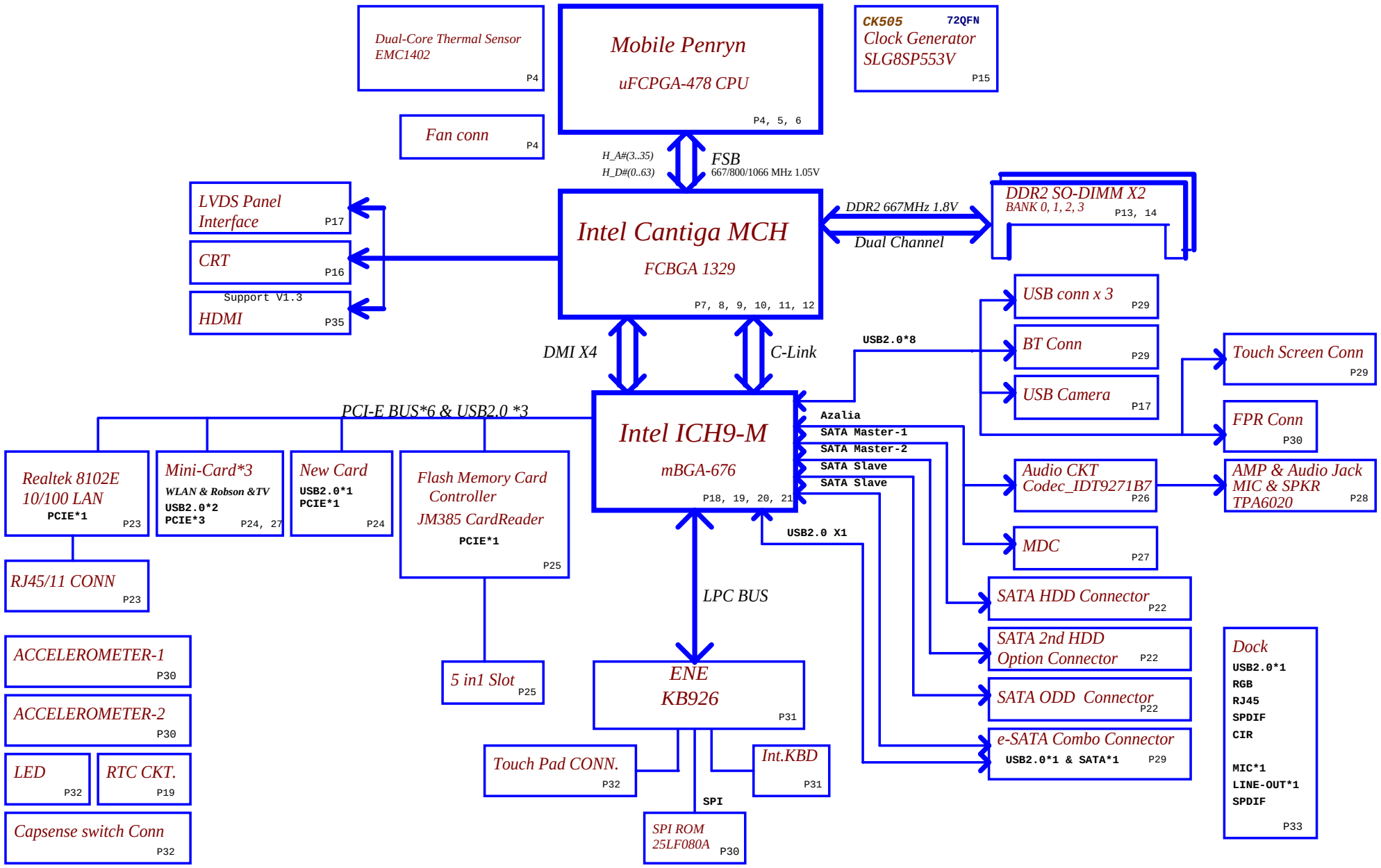
Montevina Consumer UMA



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Title: Block Diagram

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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

USB assignment :	PCIe assignment :
USB-0 Right side port	PCIe-1 WLAN
USB-1 Right side port	PCIe-2 Robson
USB-2 Left side port (combo with ESATA)	PCIe-3 TV-tuner
USB-3 Dock	PCIe-4 LAN
USB-4 USB Camera	PCIe-5 Card reader
USB-5 WLAN	PCIe-6 New card
USB-6 Bluetooth	
USB-7 Finger Printer	
USB-8 TV-tuner	
USB-9 New card	
USB-10 Left side port	
USB-11 Touch screen	

Symbol Note :

: means Digital Ground

: means Analog Ground

45@ : stuff when 45 level assembly.
@ : just reserve , no stuff.
DEBUG@ : reserve for debug only.

SMBUS Control Table

	SOURCE	INVERTER	Battery	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK Gen.	MINI CARD	LCD	Cap.board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V CY
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
ESB_CLK ESB_DAT	KB926	X	X	X	X	X	X	X	X	V ENE
DDC2_CLK DDC2_DAT	North Bridge	X	X	X	X	X	X	X	V	X
ICH_SMBCLK ICH_SMBDATA	South Bridge	X	X	X	X	V	V	V	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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Title: Notes List

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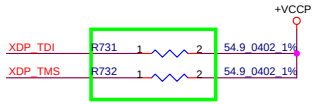
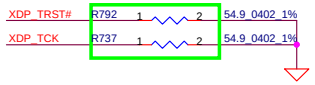
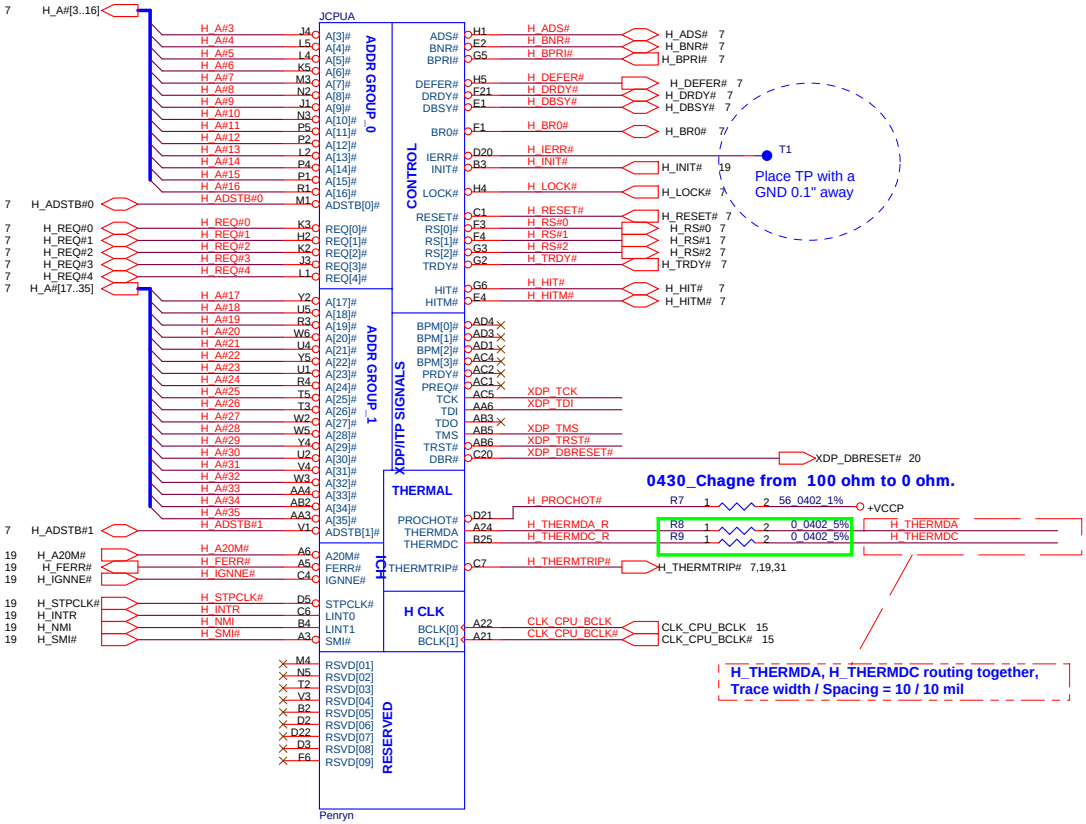
ITP-XDP Connector

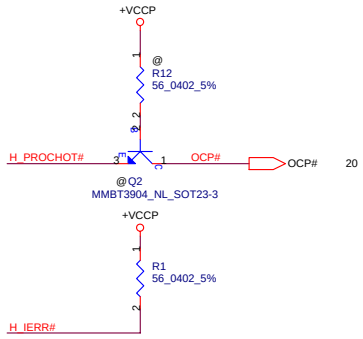
0512_Remove XDP debug port.

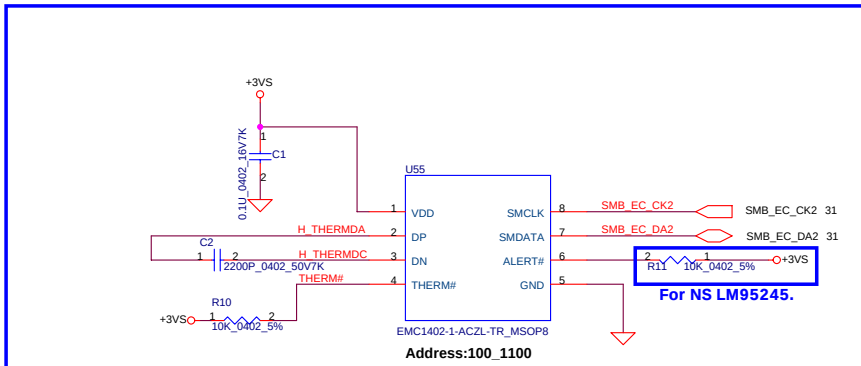


0512_Change value to 54.9 ohm if remove XDP port.

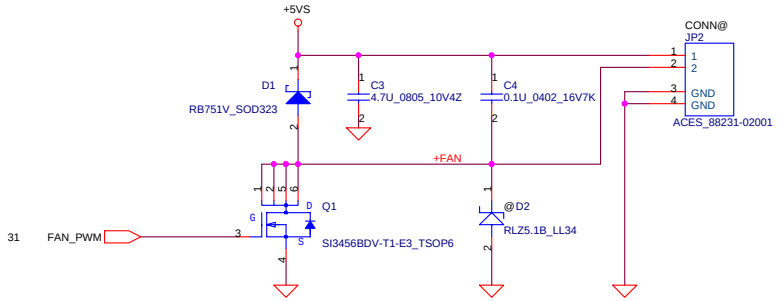








PWM Fan Control circuit



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Title: Penryn(1/3)-AGTL+/ITP-XDP

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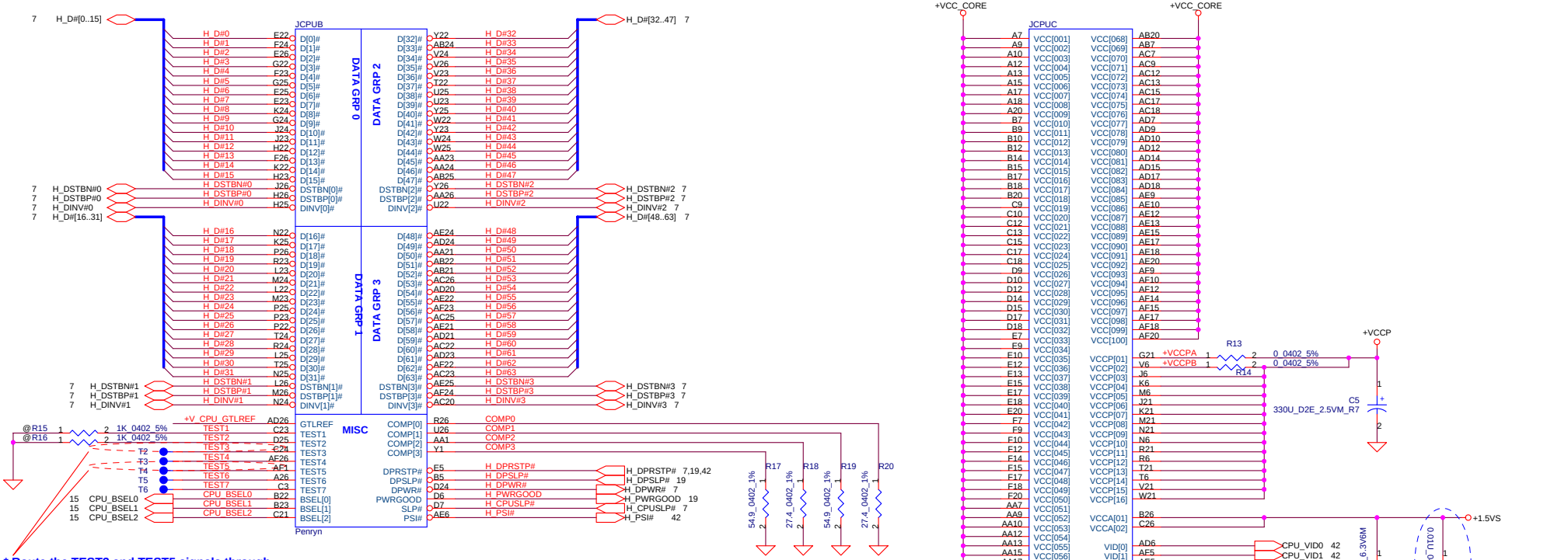
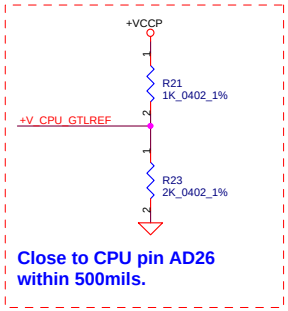


*** Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.**

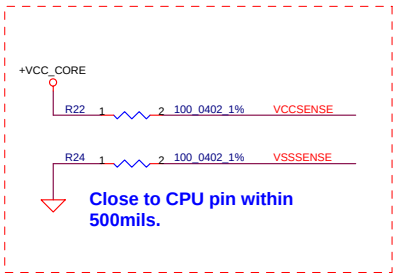
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.

Length match within 25 mils.
The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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Title: **Compal Electronics, Inc.**
Penryn(2/3)-AGTL+/ITP-XDP

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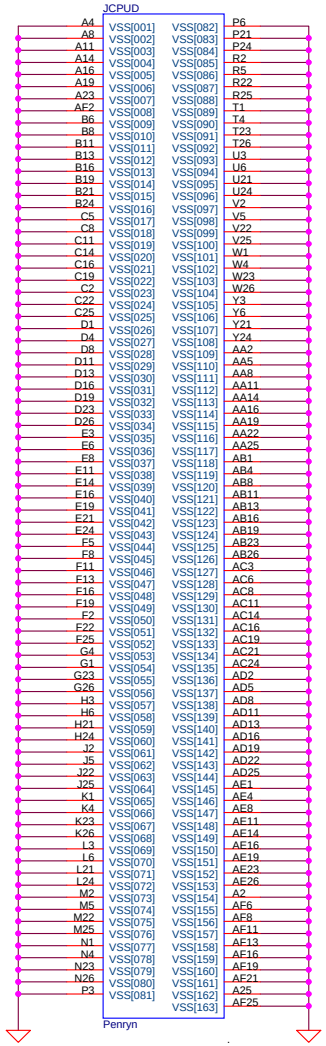
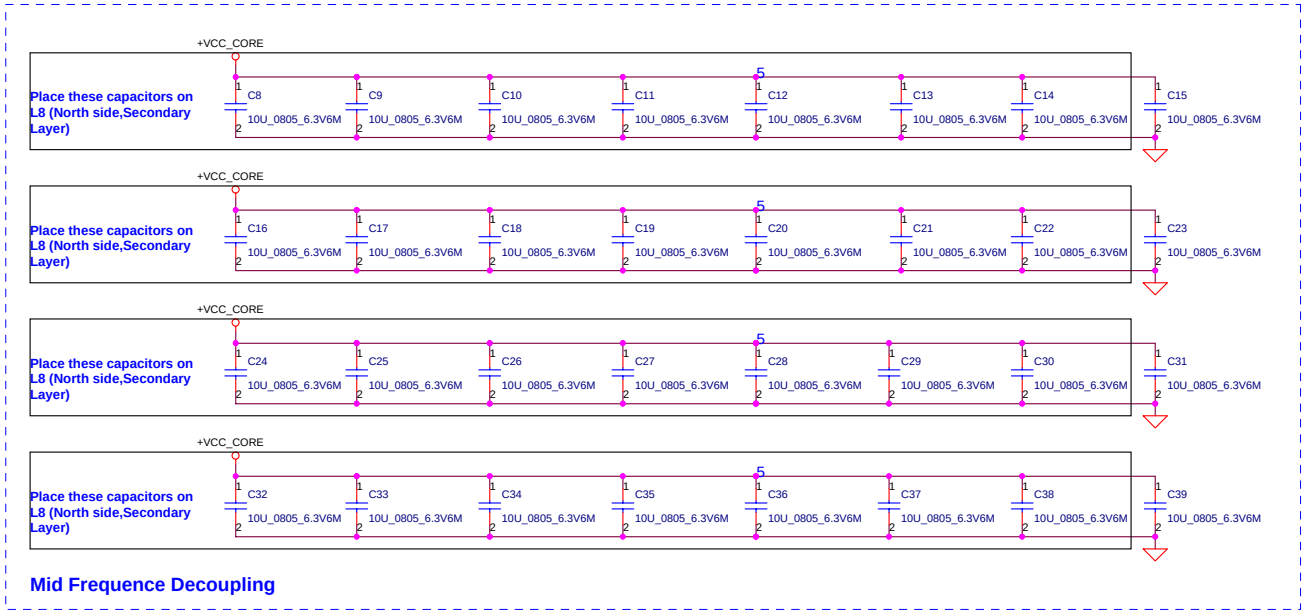
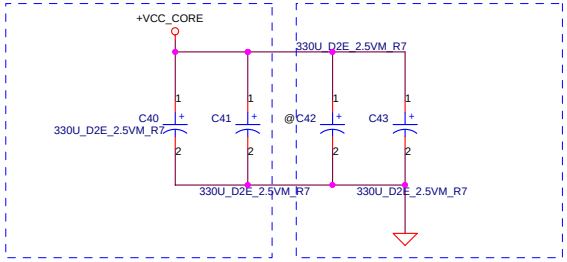
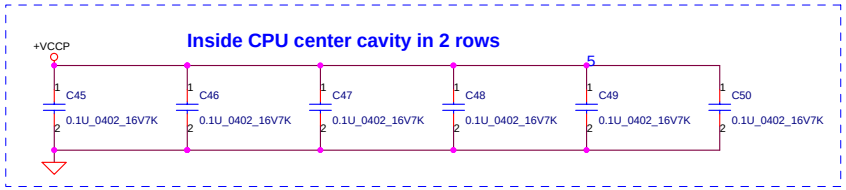




Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF





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	Penryn(3/3)-AGTL+/ITP-XDP		
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U57A — HOST — CANTIGA ES_FCBGA1329

U57B — RSVD / DDR CLK/ CONTROL/COMPENSATION / CLK / CFG / DMI / GRAPHICS VID / PM / ME / NC / MISC / HDA — CANTIGA ES_FCBGA1329

Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.

+V_DDR_MCH_REF generated by DC-DC

Follow Design Guide For Cantiga: 80.6ohm

*R37*Follow Intel feedback

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Title: Cantiga(1/6)-AGTL/DMI/DDR

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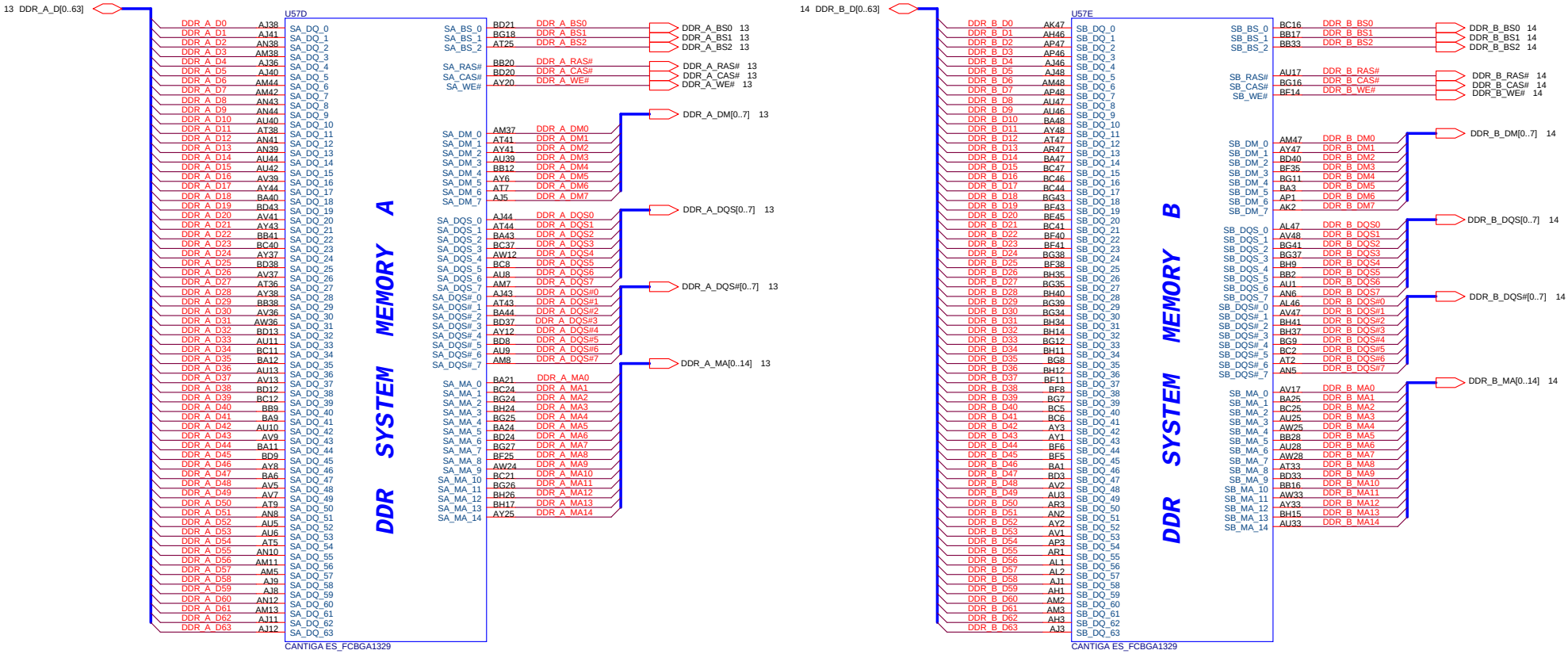

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Title: Cantiga(2/6)-DDR2 A/B CH

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Reserve for Intel DPST function.

@R2222 0_0402_5%

17,31 INV_PWM — NB_PWM — L32

ENBKL_NB — G32

+3VS — R51 10K_0402_5% — M32

R52 10K_0402_5% — M33

17 DDC2_CLK — DDC2_CLK — K33

17 DDC2_DATA — DDC2_DATA — J33

17 ENAVDD — ENAVDD — M29

R53 2.37K_0402_1% — C44

Follow Intel DG & Checklist

17 LVDS_ACLK- — LVDS_ACLK- — C41

17 LVDS_ACLK+ — LVDS_ACLK+ — C40

17 LVDS_BCLK- — LVDS_BCLK- — B37

17 LVDS_BCLK+ — LVDS_BCLK+ — A37

17 LVDS_A0- — LVDS_A0- — H47

17 LVDS_A1- — LVDS_A1- — E46

17 LVDS_A2- — LVDS_A2- — G40

A40

17 LVDS_A0+ — LVDS_A0+ — H48

17 LVDS_A1+ — LVDS_A1+ — D45

17 LVDS_A2+ — LVDS_A2+ — F40

B40

17 LVDS_B0- — LVDS_B0- — A41

17 LVDS_B1- — LVDS_B1- — H38

17 LVDS_B2- — LVDS_B2- — G37

J37

17 LVDS_B0+ — LVDS_B0+ — B42

17 LVDS_B1+ — LVDS_B1+ — G38

17 LVDS_B2+ — LVDS_B2+ — F37

K37

T85 TV_COMPS

T86 TV_LUMA

T87 TV_CRMA

Follow Intel DG & Checklist

R672 75_0402_1% R673 75_0402_1% R674 75_0402_1%

+3VS — @R675 2.2K_0402_5% — R2141 0_0402_5% — C31

E25 TVA_DAC

H25 TVB_DAC

K25 TVC_DAC

H24 TV_RTN

E32 TV_DCONSEL_0 TV_DCONSEL_1

16 M_BLUE — M_BLUE — E28

16 M_GREEN — M_GREEN — G28

16 M_RED — M_RED — J28

Follow Intel DG & Checklist

R54 150_0402_1% R55 150_0402_1% R56 150_0402_1%

G29 CRT_IRTN

16 3VDDCCL — 3VDDCCL — H32

16 3VDDCDA — 3VDDCDA — J32

16 CRT_HSYNC — CRT_HSYNC R57 30.1_0402_1% HSYNC — J29

16 CRT_VSYNC — CRT_VSYNC R58 30.1_0402_1% VSYNC — L29

R60 1.02K_0402_1%

CANTIGA ES_FCBGA1329

U57C

L_BKLT_CTRL L32

L_BKLT_EN G32

L_CTRL_CLK M32

L_CTRL_DATA M33

L_DDC_CLK K33

L_DDC_DATA J33

L_VDD_EN M29

LVDS_IBG C44

LVDS_VBG B43

LVDS_VREFH E37

LVDS_VREFL E38

LVDSA_CLK# C41

LVDSA_CLK C40

LVDSB_CLK# B37

LVDSB_CLK A37

LVDSA_DATA#_0 H47

LVDSA_DATA#_1 E46

LVDSA_DATA#_2 G40

LVDSA_DATA#_3 A40

LVDSA_DATA_0 H48

LVDSA_DATA_1 D45

LVDSA_DATA_2 F40

LVDSA_DATA_3 B40

LVDSB_DATA#_0 A41

LVDSB_DATA#_1 H38

LVDSB_DATA#_2 G37

LVDSB_DATA#_3 J37

LVDSB_DATA_0 B42

LVDSB_DATA_1 G38

LVDSB_DATA_2 F37

LVDSB_DATA_3 K37

CRT_DDC_CLK H32

CRT_DDC_DATA J32

CRT_HSYNC J29

CRT_TVO_IREF E29

CRT_VSYNC L29

LVDS

TV

VGA

PCI-EXPRESS GRAPHICS

PEG_COMPI T37

PEG_COMPO T36

R50 49.9_0402_1% +VCC_PEG

PEGCOMP trace width and spacing is 20/25 mils.

PEG_RX#_0 H44

PEG_RX#_1 J46

PEG_RX#_2 L44

PEG_RX#_3 L40

PEG_RX#_4 N41

PEG_RX#_5 P48

PEG_RX#_6 N44

PEG_RX#_7 T43

PEG_RX#_8 U43

PEG_RX#_9 Y43

PEG_RX#_10 Y48

PEG_RX#_11 Y36

PEG_RX#_12 AA43

PEG_RX#_13 AD37

PEG_RX#_14 AC47

PEG_RX#_15 AD39

Reserve for Intel DPST function.

31 ENBKL — R42 0_0402_5% — ENBKL_NB

17,31 BKOFF# — @R43 0_0402_5%

R2140 100K_0402_5%

PEG_RX_0 H43

PEG_RX_1 J44

PEG_RX_2 L43

PEG_RX_3 L41 — TMDS_B_HPD# — TMDS_B_HPD# 35

PEG_RX_4 N40

PEG_RX_5 P47

PEG_RX_6 N43

PEG_RX_7 T42

PEG_RX_8 U42

PEG_RX_9 Y42

PEG_RX_10 W47

PEG_RX_11 Y37

PEG_RX_12 AA42

PEG_RX_13 AD36

PEG_RX_14 AC48

PEG_RX_15 AD40

PEG_TX#_0 J41 — TMDS_BDATA2# C1060 0.1U_0402_16V7K — TMDS_B_DATA2# 35

PEG_TX#_1 M46 — TMDS_BDATA1# C1061 0.1U_0402_16V7K — TMDS_B_DATA1# 35

PEG_TX#_2 M47 — TMDS_BDATA0# C1062 0.1U_0402_16V7K — TMDS_B_DATA0# 35

PEG_TX#_3 M40 — TMDS_BCLK# C1063 0.1U_0402_16V7K — TMDS_B_CLK# 35

PEG_TX#_4 M42

PEG_TX#_5 R48

PEG_TX#_6 N38

PEG_TX#_7 T40

PEG_TX#_8 U37

PEG_TX#_9 U40

PEG_TX#_10 Y40

PEG_TX#_11 AA46

PEG_TX#_12 AA37

PEG_TX#_13 AA40

PEG_TX#_14 AD43

PEG_TX#_15 AC46

PEG_TX_0 J42 — TMDS_BDATA2 C1064 0.1U_0402_16V7K — TMDS_B_DATA2 35

PEG_TX_1 L46 — TMDS_BDATA1 C1065 0.1U_0402_16V7K — TMDS_B_DATA1 35

PEG_TX_2 M48 — TMDS_BDATA0 C1066 0.1U_0402_16V7K — TMDS_B_DATA0 35

PEG_TX_3 M39 — TMDS_BCLK C1067 0.1U_0402_16V7K — TMDS_B_CLK 35

PEG_TX_4 M43

PEG_TX_5 R47

PEG_TX_6 N37

PEG_TX_7 T39

PEG_TX_8 U36

PEG_TX_9 U39

PEG_TX_10 Y39

PEG_TX_11 Y46

PEG_TX_12 AA36

PEG_TX_13 AA39

PEG_TX_14 AD42

PEG_TX_15 AD46

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

0430_Remove C1018~C1025 (Reserve for WWAN issue)

Solve 3G WWAN issue

+3VS — @R59 4.02K_0402_1% — CFG5 — @R63 2.21K_0402_1%

+3VS — @R64 4.02K_0402_1% — CFG19

+3VS — @R67 4.02K_0402_1% — CFG20

0505_Double confirm Strapping setting.

CFG6 @R73 2.21K_0402_1%

CFG7 @R65 2.21K_0402_1%

CFG9 @R68 2.21K_0402_1%

CFG10 @R71 2.21K_0402_1%

CFG12 @R77 2.21K_0402_1%

CFG13 @R66 2.21K_0402_1%

CFG16 @R70 2.21K_0402_1%

Useless Strapping

CFG8 @R105 2.21K_0402_1%

CFG11 @R101 2.21K_0402_1%

CFG14 @R104 2.21K_0402_1%

CFG15 @R76 2.21K_0402_1%

CFG17 @R75 2.21K_0402_1%

CFG18 @R100 2.21K_0402_1%

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Title: Cantiga(3/6)-VGA/LVDS/TV

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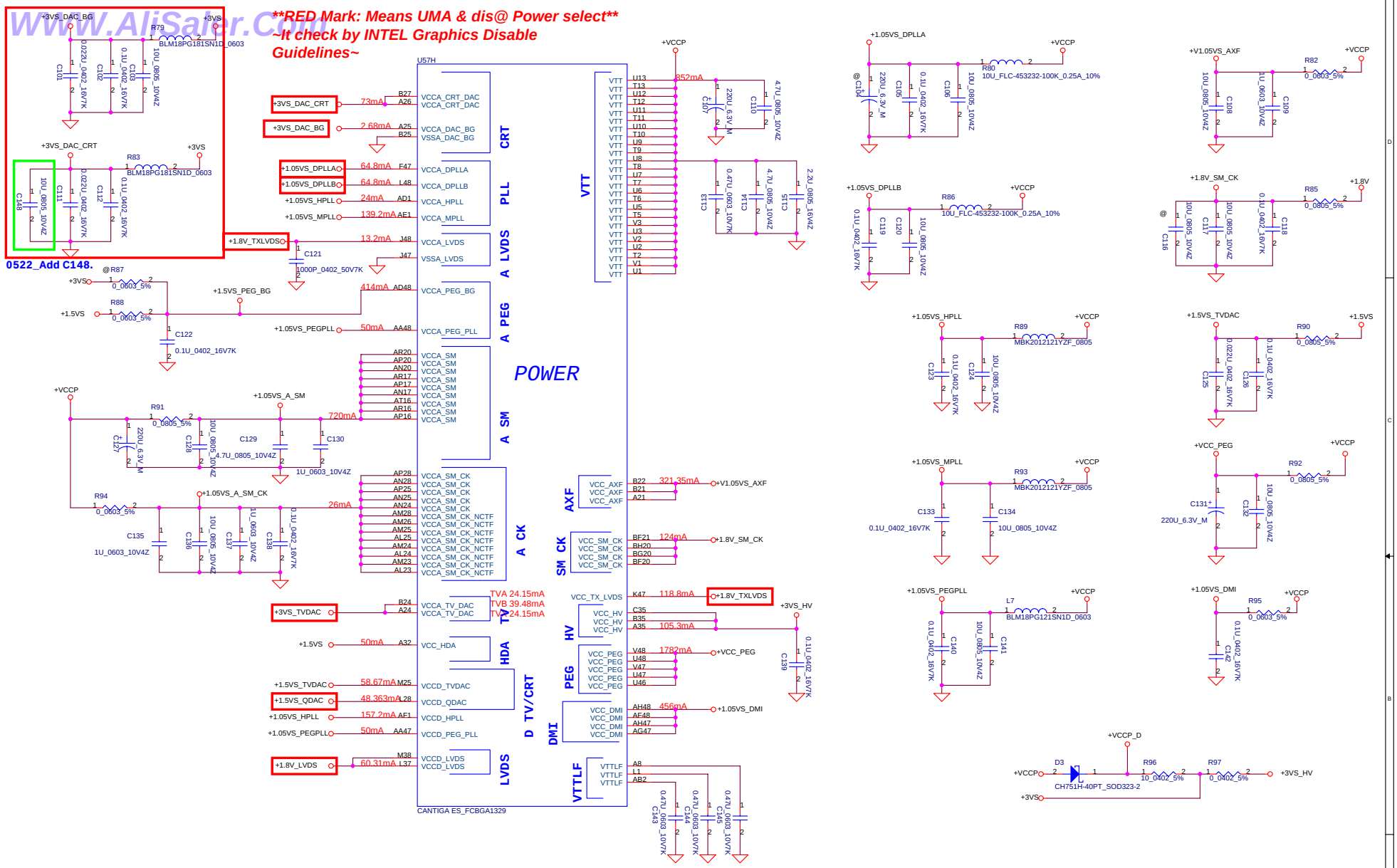
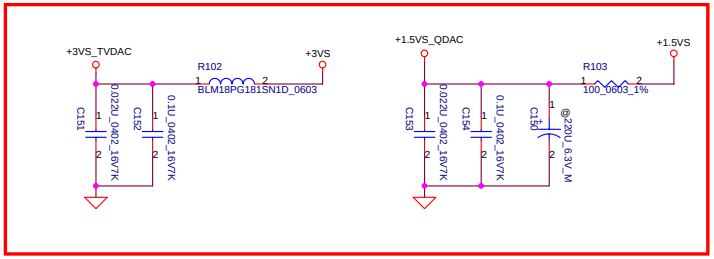
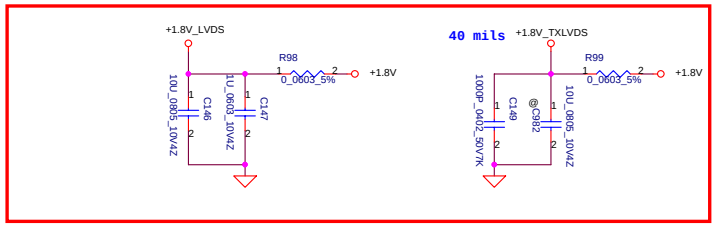
RED Mark: Means UMA & dis@ Power select
~It check by INTEL Graphics Disable Guidelines~

0522_Add C148.







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Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	Cantiga(4/6)-PWR
Size: Custom	Document Number: Montevina Consumer Discrete
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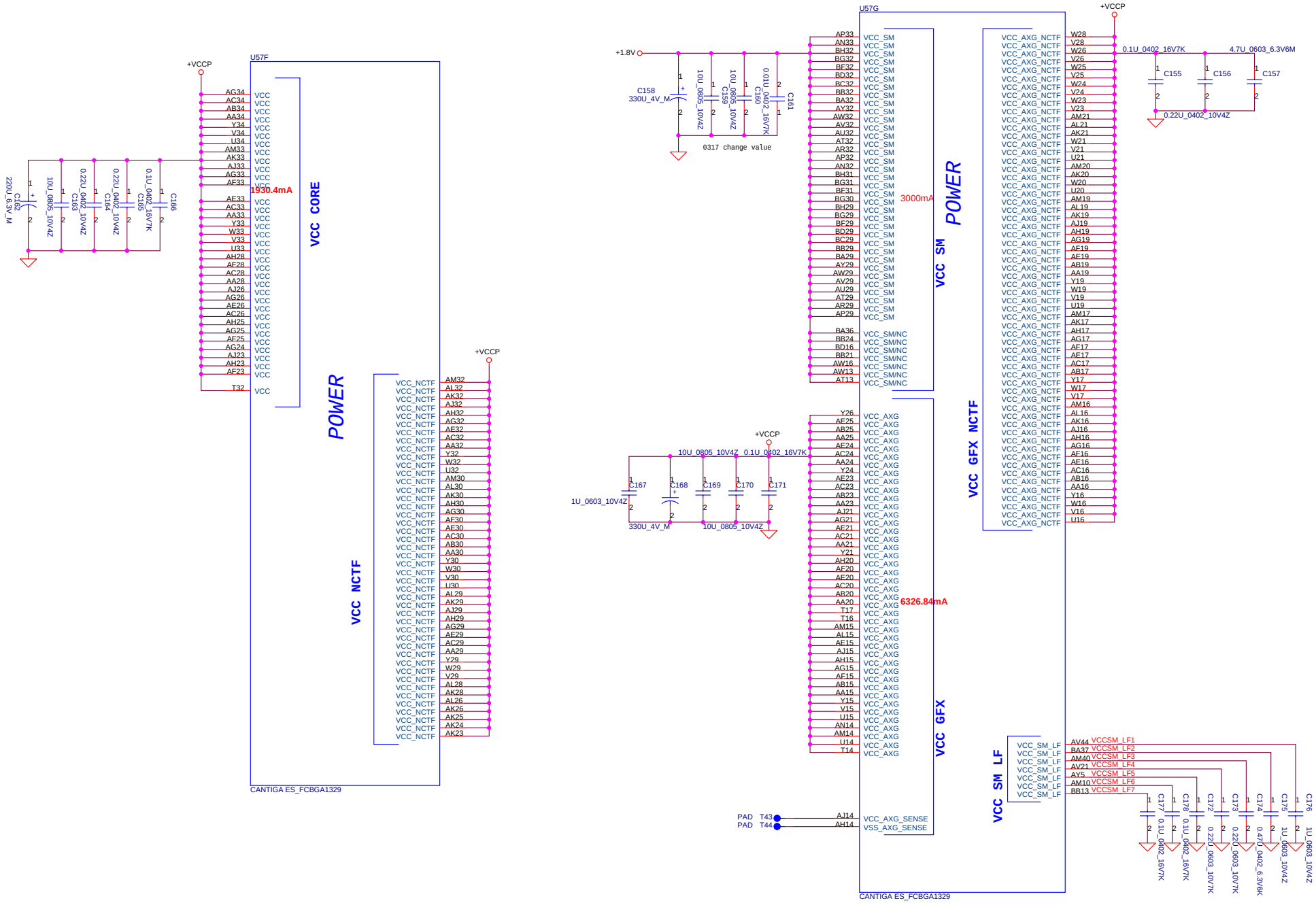

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Compal Electronics, Inc.			
Title: Cantiga(5/6)-PWR/GND			
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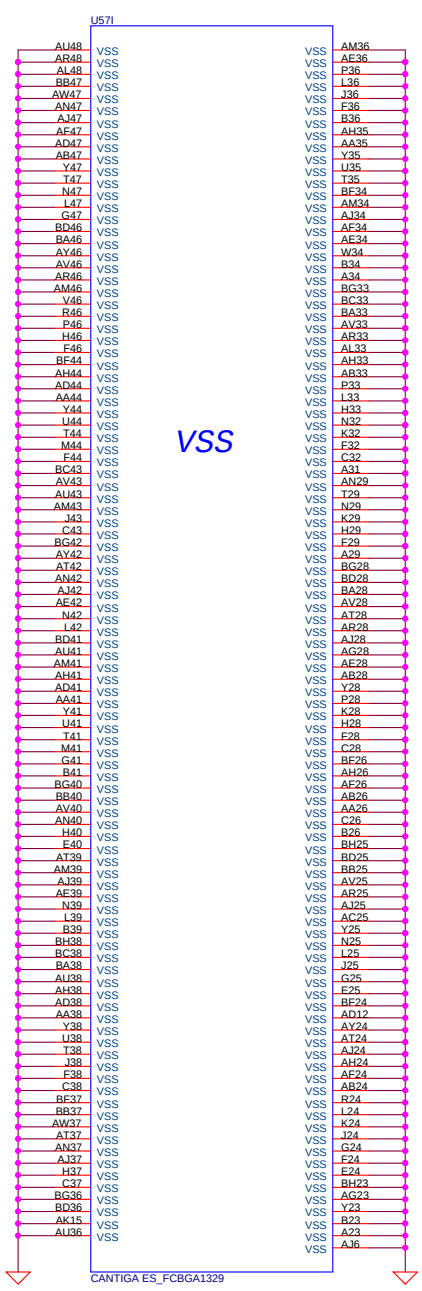

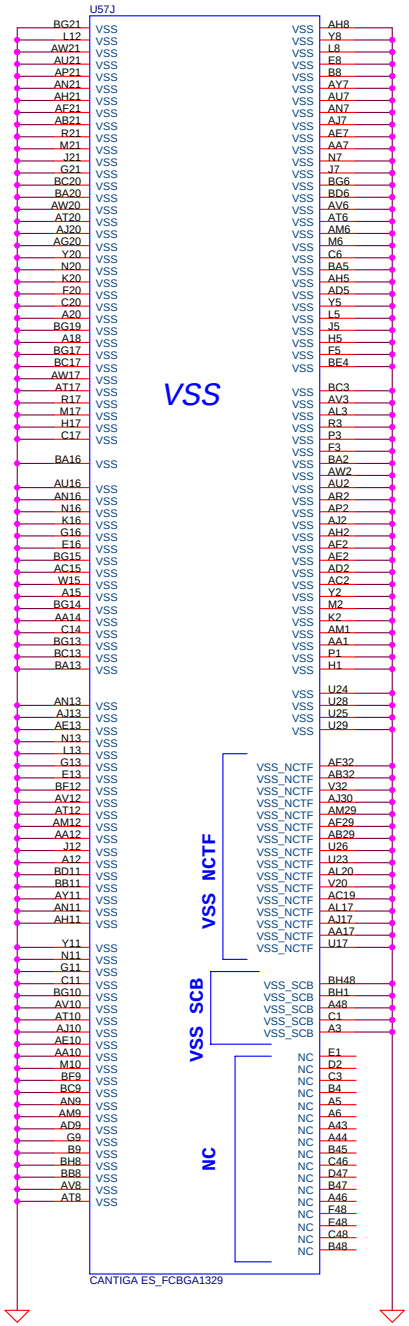

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Title	Cantiga(6/6)-PWR/GND
Size: Custom	Document Number: Montevina Consumer Discrete
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8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..14]

Layout Note:
Place near JDIMM1

+1.8V
2.2U_0805_16V4Z: C182, C183, C184, C185, C186
0.1U_0402_16V7K: C187, C188, C189, C190
330U_4V_M: C181

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

+0.9V
0.1U_0402_16V7K: C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203

Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"

+0.9V
56_0404_4P2R_5%
RP1: DDR_A_MA5, DDR_A_MA8 / RP2: DDR_CKE0_DIMMA, DDR_A_BS2
RP3: DDR_A_MA1, DDR_A_MA3 / RP4: DDR_A_MA7, DDR_A_MA6
RP5: DDR_A_RAS#, DDR_CS0_DIMMA# / RP6: DDR_A_MA9, DDR_A_MA12
RP7: DDR_A_BS0, DDR_A_MA10 / RP8: DDR_A_MA4, DDR_A_MA2
RP9: DDR_A_CAS#, DDR_A_WE# / RP10: DDR_A_MA0, DDR_A_BS1
RP11: DDR_CS1_DIMMA#, M_ODT1 / RP12: M_ODT0, DDR_A_MA13
RP13: DDR_A_MA11, DDR_CKE1_DIMMA, DDR_A_MA14
R108 56_0402_5%

+1.8V
+V_DDR_MCH_REF
JDIMM1 CONN@

	VREF	1	2	VSS	
DDR_A_D4	VSS	3	4	DQ4	DDR_A_D6
DDR_A_D1	DQ0	5	6	DQ5	DDR_A_D0
	DQ1	7	8	VSS	
DDR_A_DQS#0	VSS	9	10	DM0	DDR_A_DM0
DDR_A_DQS0	DQS0#	11	12	VSS	
	DQS0	13	14	DQ6	DDR_A_D5
DDR_A_D2	VSS	15	16	DQ7	DDR_A_D7
DDR_A_D3	DQ2	17	18	VSS	
	DQ3	19	20	DQ12	DDR_A_D13
DDR_A_D8	VSS	21	22	DQ13	DDR_A_D12
DDR_A_D14	DQ8	23	24	VSS	
	DQ9	25	26	DM1	DDR_A_DM1
DDR_A_DQS#1	VSS	27	28	VSS	
DDR_A_DQS1	DQS1#	29	30	CK0	M_CLK_DDR0 (M_CLK_DDR0 7)
	DQS1	31	32	CK0#	M_CLK_DDR#0 (M_CLK_DDR#0 7)
DDR_A_D9	VSS	33	34	VSS	
DDR_A_D15	DQ10	35	36	DQ14	DDR_A_D11
	DQ11	37	38	DQ15	DDR_A_D10
	VSS	39	40	VSS	
		41	42		
DDR_A_D16	VSS	43	44	DQ20	DDR_A_D20
DDR_A_D17	DQ16	45	46	DQ21	DDR_A_D21
	DQ17	47	48	VSS	
DDR_A_DQS#2	VSS	49	50	NC	PM_EXTTS#0 7
DDR_A_DQS2	DQS2#	51	52	DM2	DDR_A_DM2
	DQS2	53	54	VSS	
DDR_A_D18	VSS	55	56	DQ22	DDR_A_D23
DDR_A_D19	DQ18	57	58	DQ23	DDR_A_D22
	DQ19	59	60	VSS	
DDR_A_D29	VSS	61	62	DQ28	DDR_A_D28
DDR_A_D24	DQ24	63	64	DQ29	DDR_A_D25
	DQ25	65	66	VSS	
DDR_A_DM3	VSS	67	68	DQS3#	DDR_A_DQS#3
	DM3	69	70	DQS3	DDR_A_DQS3
	NC	71	72	VSS	
DDR_A_D26	VSS	73	74	DQ30	DDR_A_D31
DDR_A_D27	DQ26	75	76	DQ31	DDR_A_D30
	DQ27	77	78	VSS	
7 DDR_CKE0_DIMMA	CKE0	79	80	NC/CKE1	DDR_CKE1_DIMMA (DDR_CKE1_DIMMA 7)
	VDD	81	82	VDD	
8 DDR_A_BS2	BA2	83	84	NC/A15	
DDR_A_BS2	VDD	85	86	NC/A14	DDR_A_MA14
	A12	87	88	VDD	
DDR_A_MA12	A9	89	90	A11	DDR_A_MA11
DDR_A_MA9	A8	91	92	A7	DDR_A_MA7
DDR_A_MA8	VDD	93	94	A6	DDR_A_MA6
	A5	95	96	VDD	
DDR_A_MA5	A3	97	98	A4	DDR_A_MA4
DDR_A_MA3	A2	99	100	A0	DDR_A_MA2
DDR_A_MA1	A1	101	102	VDD	DDR_A_MA0
	VDD	103	104	BA1	DDR_A_BS1
DDR_A_MA10	A10/AP	105	106	RAS#	DDR_A_RAS# (DDR_A_RAS# 8)
8 DDR_A_BS0 DDR_A_BS0	BA0	107	108	S0#	DDR_CS0_DIMMA# (DDR_CS0_DIMMA# 7)
8 DDR_A_WE# DDR_A_WE#	WE#	109	110	VDD	
	VDD	111	112	ODT0	M_ODT0 (M_ODT0 7)
8 DDR_A_CAS# DDR_A_CAS#	CAS#	113	114	NC/A13	DDR_A_MA13
7 DDR_CS1_DIMMA# DDR_CS1_DIMMA#	NC/S1#	115	116	VDD	
7 M_ODT1 M_ODT1	VDD	117	118	NC	
	NC/ODT1	119	120	VSS	
	VSS	121	122	DQ36	DDR_A_D39
DDR_A_D37	DQ32	123	124	DQ37	DDR_A_D38
DDR_A_D36	DQ33	125	126	VSS	
	VSS	127	128	DM4	DDR_A_DM4
DDR_A_DQS#4	DQS4#	129	130	VSS	
DDR_A_DQS4	DQS4	131	132	DQ38	DDR_A_D34
	VSS	133	134	DQ39	DDR_A_D33
DDR_A_D35	DQ34	135	136	VSS	
DDR_A_D32	DQ35	137	138	DQ44	DDR_A_D45
	VSS	139	140	DQ45	DDR_A_D43
DDR_A_D40	DQ40	141	142	VSS	
DDR_A_D44	DQ41	143	144	DQS5#	DDR_A_DQS#5
	VSS	145	146	DQS5	DDR_A_DQS5
DDR_A_DM5	DM5	147	148	VSS	
	VSS	149	150	DQ46	DDR_A_D47
DDR_A_D41	DQ42	151	152	DQ47	DDR_A_D42
DDR_A_D46	DQ43	153	154	VSS	
	VSS	155	156	DQ52	DDR_A_D52
DDR_A_D49	DQ48	157	158	DQ53	DDR_A_D53
DDR_A_D48	DQ49	159	160	VSS	
	VSS	161	162	CK1	M_CLK_DDR1 (M_CLK_DDR1 7)
	NC,TEST	163	164	CK1#	M_CLK_DDR#1 (M_CLK_DDR#1 7)
DDR_A_DQS#6	VSS	165	166	VSS	
DDR_A_DQS6	DQS6#	167	168	DM6	DDR_A_DM6
	DQS6	169	170	VSS	
DDR_A_D54	VSS	171	172	DQ54	DDR_A_D51
DDR_A_D50	DQ50	173	174	DQ55	DDR_A_D55
	DQ51	175	176	VSS	
DDR_A_D61	VSS	177	178	DQ60	DDR_A_D57
DDR_A_D60	DQ56	179	180	DQ61	DDR_A_D56
	DQ57	181	182	VSS	
DDR_A_DM7	VSS	183	184	DQS7#	DDR_A_DQS#7
	DM7	185	186	DQS7	DDR_A_DQS7
DDR_A_D59	VSS	187	188	VSS	
DDR_A_D58	DQ58	189	190	DQ62	DDR_A_D62
	DQ59	191	192	DQ63	DDR_A_D63
	VSS	193	194	VSS	
14,15,30 CLK_SMBDATA CLK_SMBDATA	SDA	195	196	SAO	
14,15,30 CLK_SMBCLK CLK_SMBCLK	SCL	197	198	SA1	
+3VS	VDDSPD	199	200		
	G1	201	202	G2	

FOX_AS0A426-N4RN-7F-D

C179: 2.2U_0805_16V4Z
C180: 0.1U_0402_16V7K
C204: 2.2U_0603_6.3V4Z
C205: 0.1U_0402_16V7K
R106: 10K_0402_5%
R107: 10K_0402_5%

SO-DIMM A

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.
Title: DDRII-SODIMM SLOT1
Size: Custom
Document Number: Montevina Consumer Discrete
Rev: 0.3
Date: Friday, May 23, 2008
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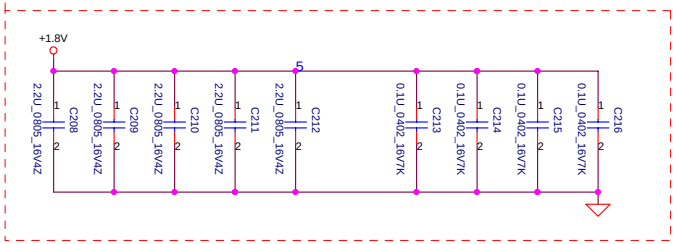
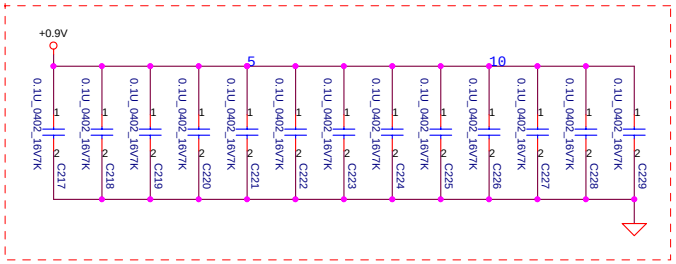
8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..14]

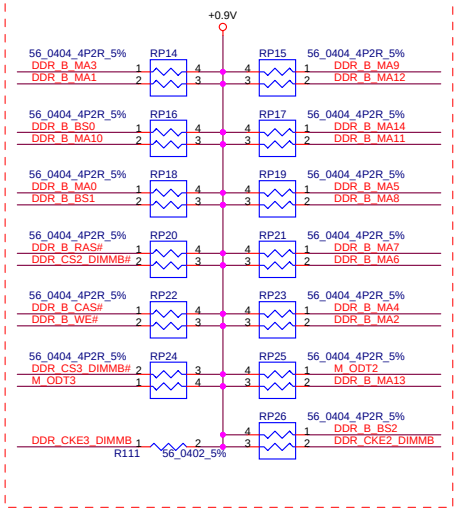
Layout Note:
Place near JDIMM2

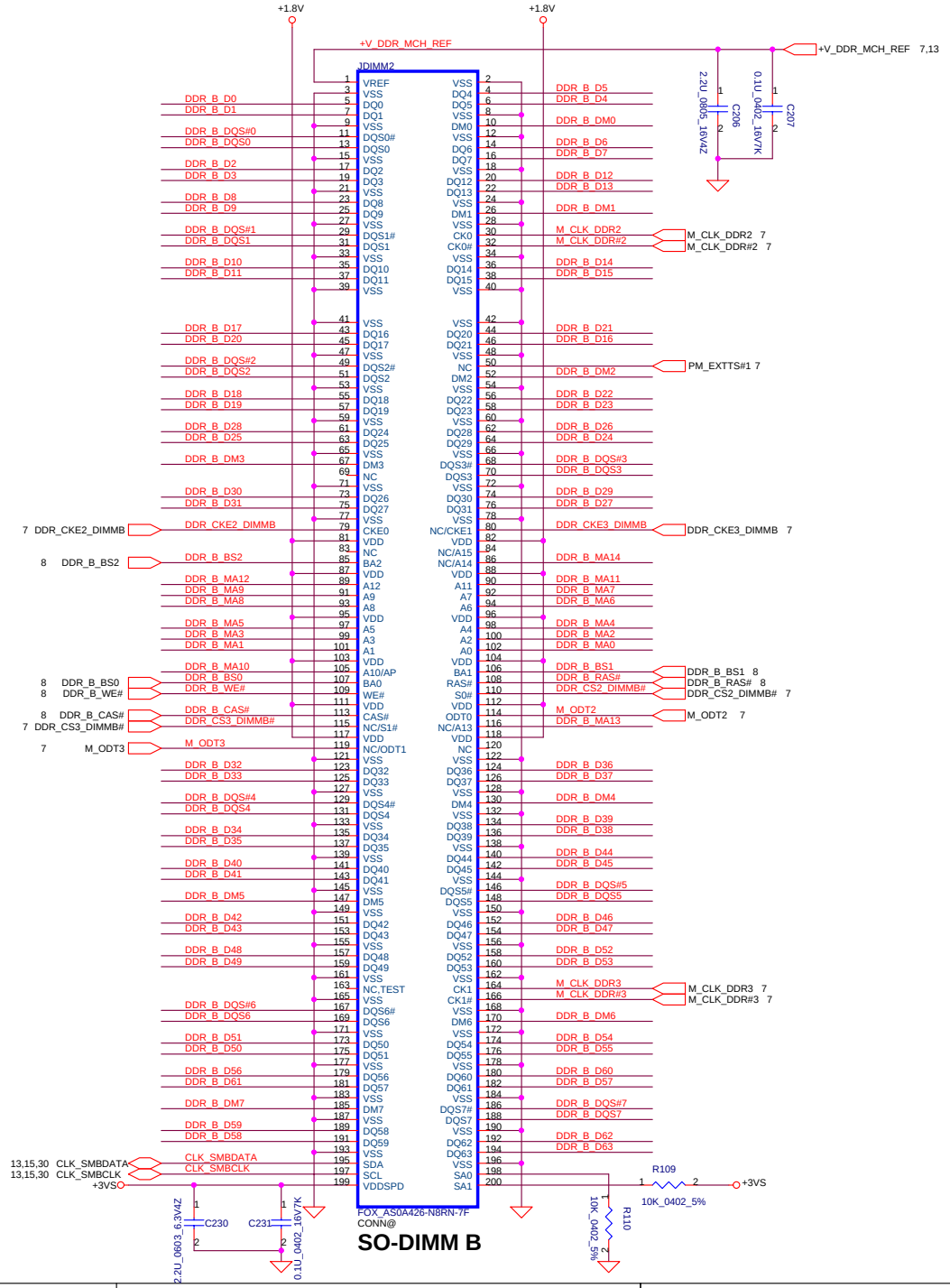


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"





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Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT2

Size | Document Number: Montevina Consumer Discrete | Rev: 0.3

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Routing the trace at least 10mil

Place close to U51

0512_Delete clock for XDP debug port.

0512_Reserve R126.

No USB CardReader anymore

0507_Reserve R714.

ITP_EN	0 = SRC8/SRC8# (SRC8@) 1 = ITP/ITP# (XDP@)
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

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Issued Date	2006/02/13	Deciphered Date	2006/03/10

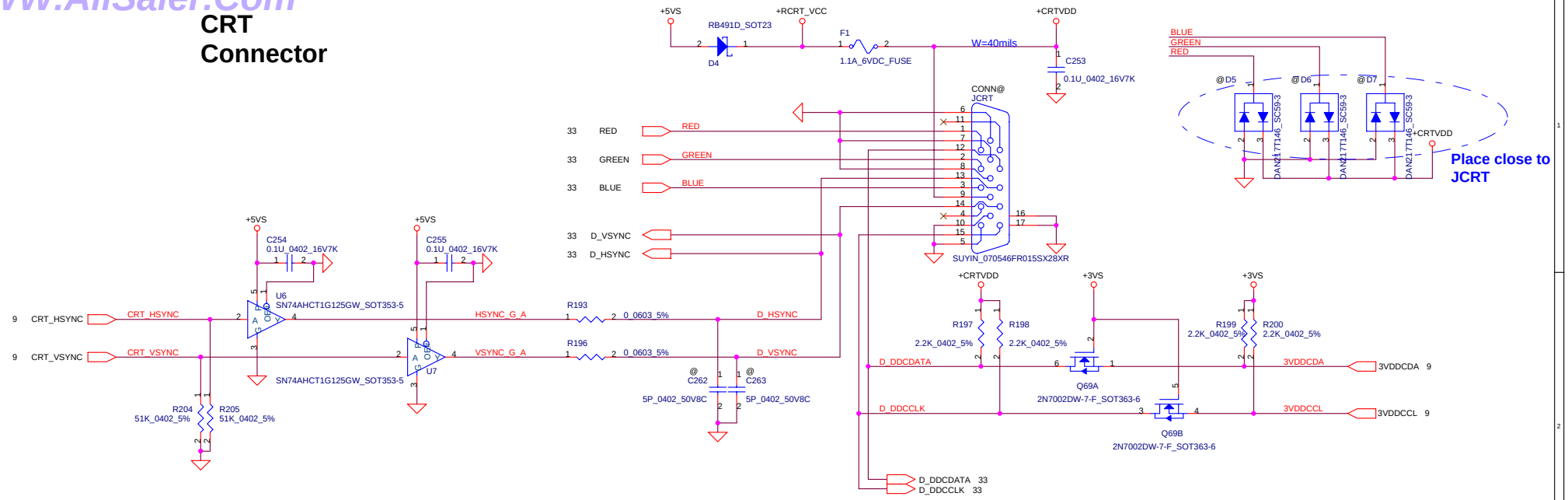
Compal Electronics, Inc.

Title: Clock Generator CK505

Size: | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 15 of 44

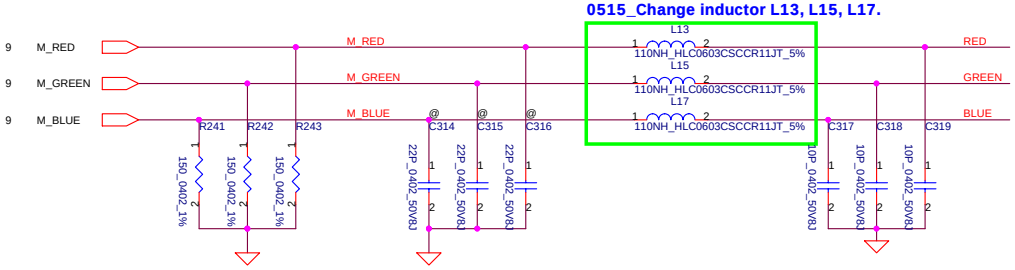
CRT Connector



CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

0515_Change inductor L13, L15, L17.



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

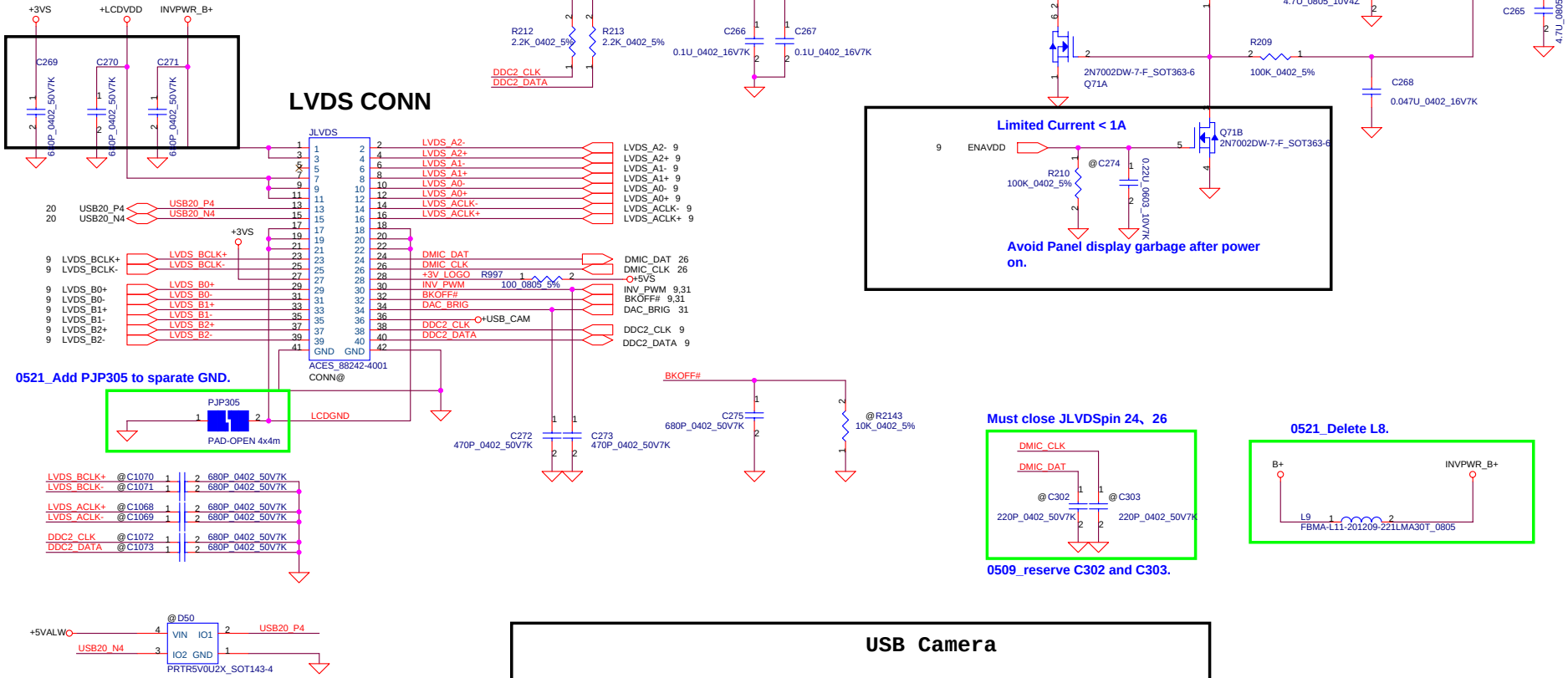
Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 16 of 44

LVDS CONN



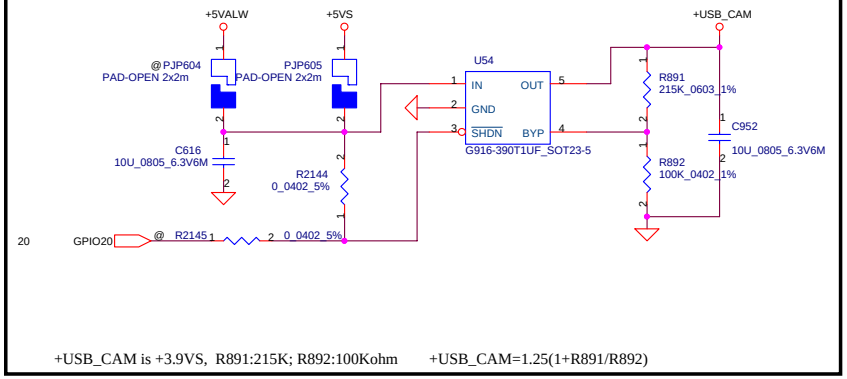
0521_Add PJP305 to sparate GND.

Must close JLVDSpin 24、26

0509_reserve C302 and C303.

0521_Delete L8.

USB Camera



+USB_CAM is +3.9VS, R891:215K; R892:100Kohm +USB_CAM=1.25(1+R891/R892)

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: LCD CONN.

Size: Document Number: Montevina Consumer UMA Rev: 0.3

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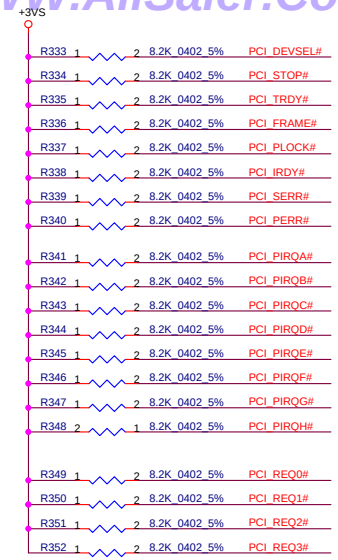
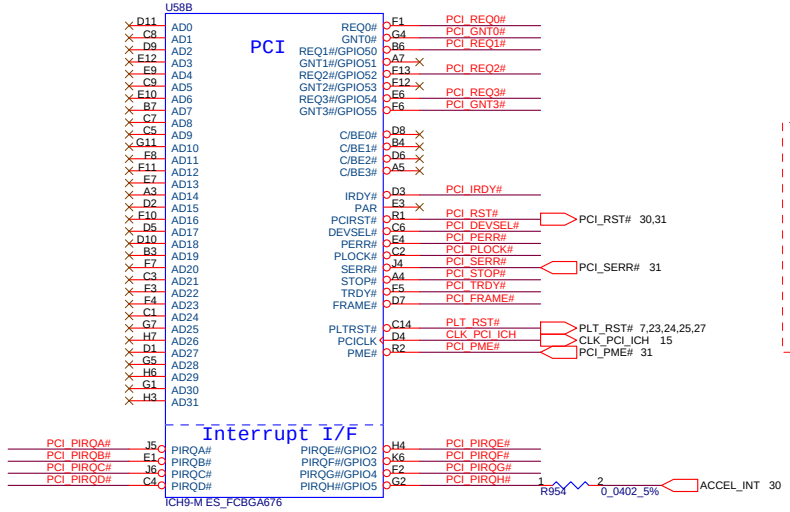
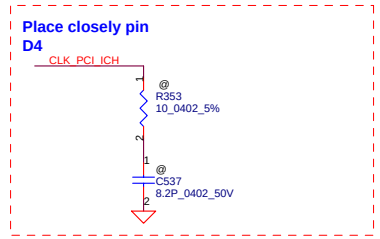
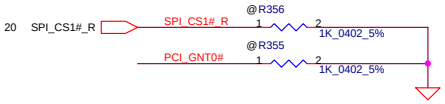






A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

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Compal Electronics, Inc.			
Title	ICH9(1/4)-PCI/INT		
Size	Document Number		Rev
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Date:	Friday, May 23, 2008	Sheet 18 of 44	

ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

0510_Follow Intel check list.

0506_Add R49.

HDD

2nd HDD

ODD

eSATA

Within 500 mils

placed within 2" from ICH9M

within 2" from R374

Place near ICH9

For HDA_BITCLK_NB crossmoat issue

XOR CHAIN ENTRANCE STRAP:RSVD

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

ICH9-M ES_FCBGA676

PCS3P732Z11BXG-08-CR_TDFN8_2X2

32.768KHZ_12.5P_MC-146

DAN202U_SC70

ACES_85205-02001

CR2032 RTC BATTERY

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 19 of 44

0512_Reserve R1041.

0520_Reserve R424.

R424
Low -->default
High -->No boot

0512_Delete HDCP SPI interface.

Place closely pin AF3

Place closely pin H1

WLAN

Robson

TV tuner

LAN

5 in 1 Card reader

New Card

Within 500 mils

Within 500 mils

Board ID

Discrete-->H
UMA-->L

17" platform-->H
14" platform-->L

USB-0 Right side
USB-1 Right side
USB-2 eSATA & USB Combo
USB-3 Dock
USB-4 USB Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Fingerprint
USB-8 MiniCard(TV tuner)
USB-9 New Card
USB-10 Left Side
USB-11 Touch Screen

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

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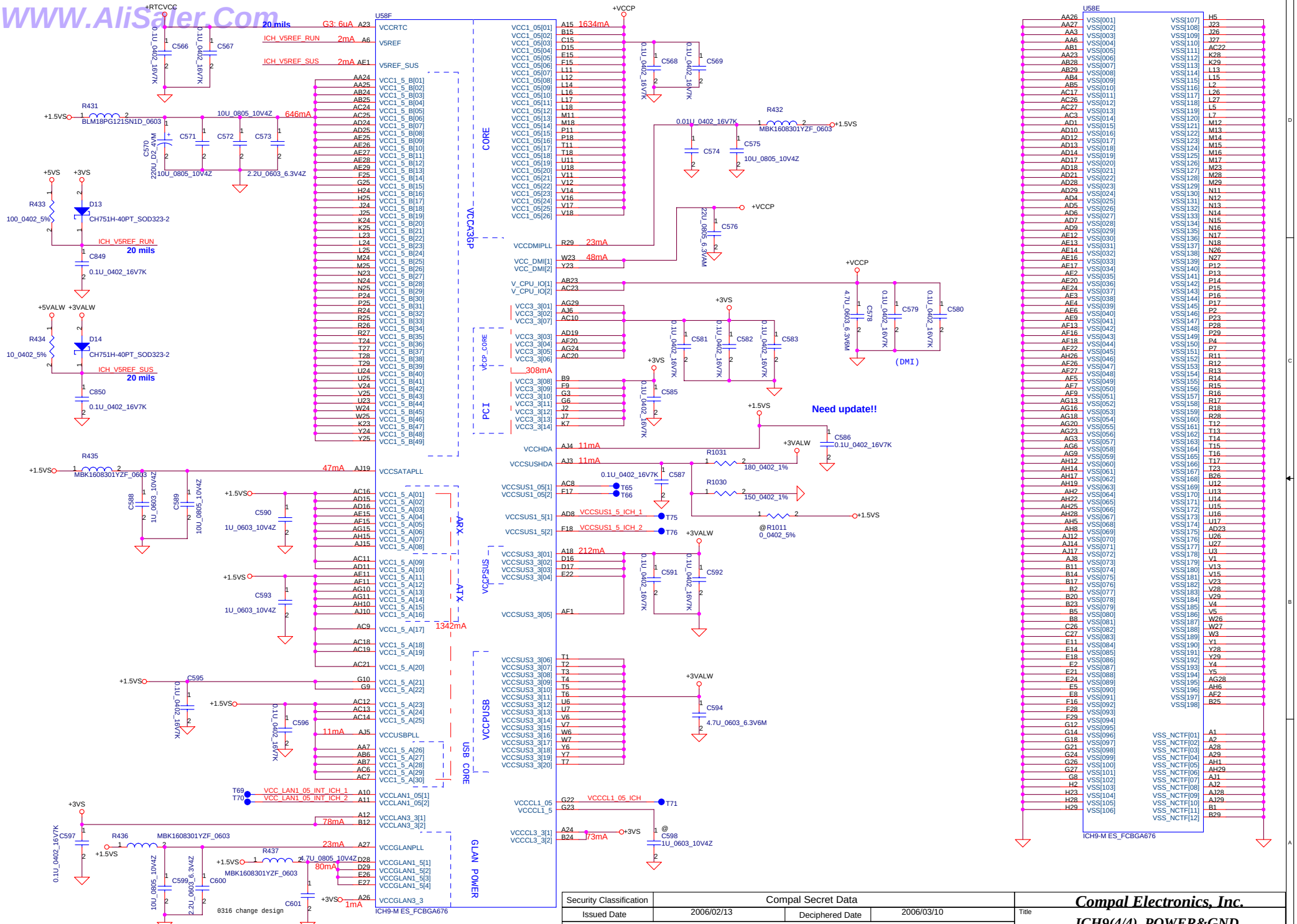
Compal Electronics, Inc.

Title: ICH9(3/4)_DMI,USB,GPIO,PCIE

Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 20 of 44



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

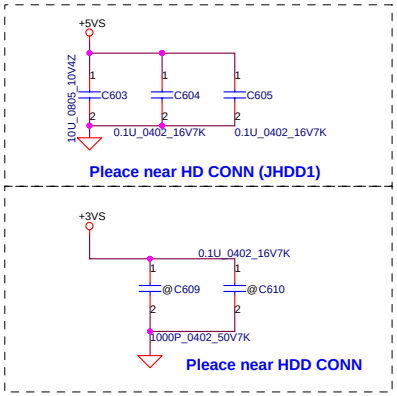
Compal Electronics, Inc.

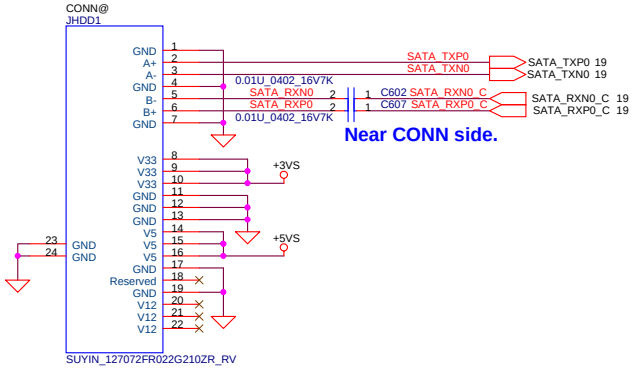
Title: ICH9(4/4)_POWER&GND

Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

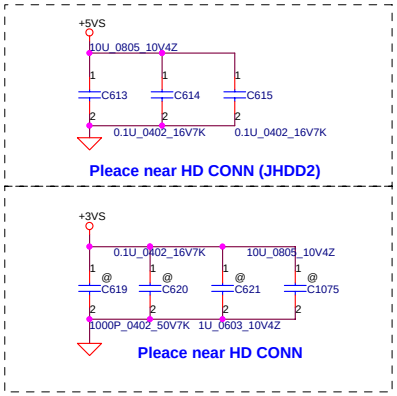
Date: Friday, May 23, 2008 | Sheet 21 of 44

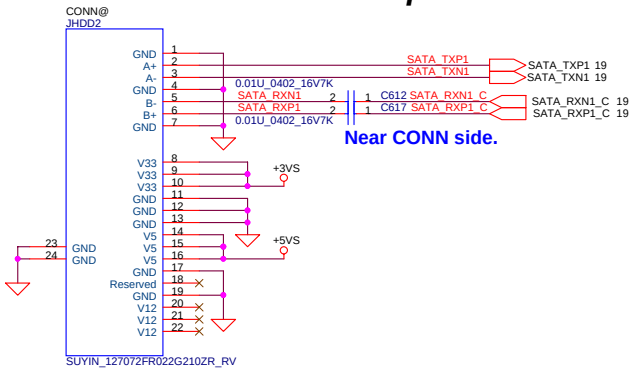
HDD Connector



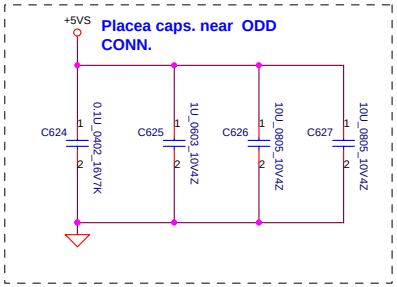


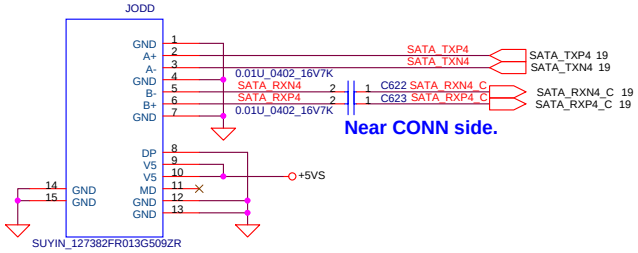
2nd HDD Connector-option





CD-ROM Connector





ZZZ1

PCB-MB

PCB 03W LA-4081P REV0 M/B UMA

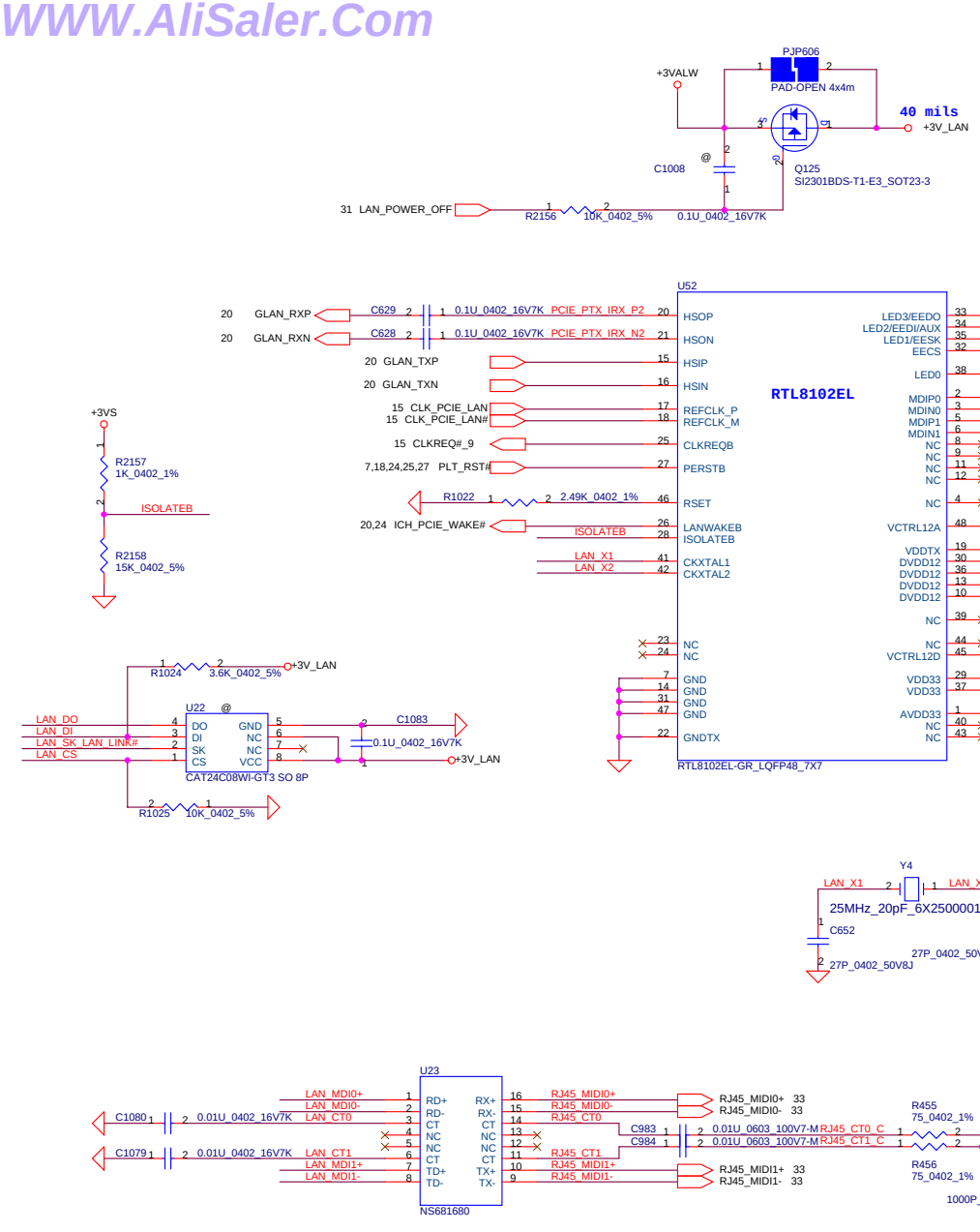
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

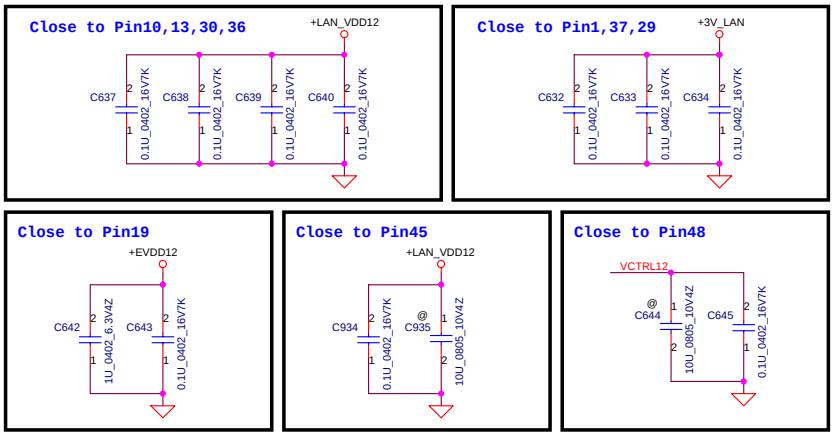
Compal Electronics, Inc.

Title: HDD & CDROM

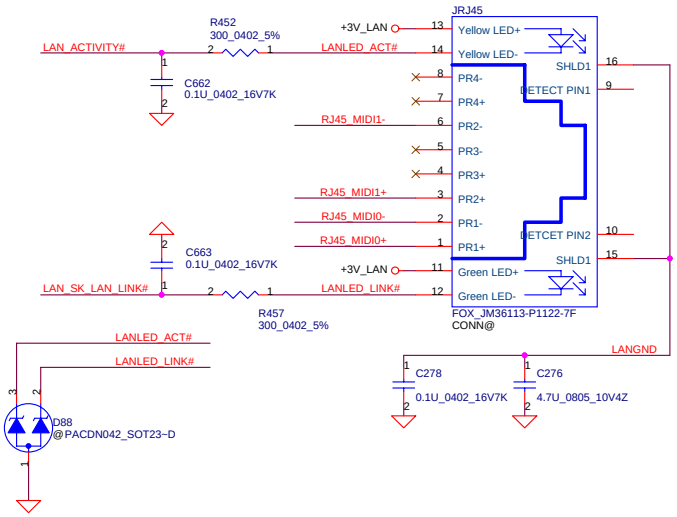
Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 22 of 44





LAN Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2007/06/30

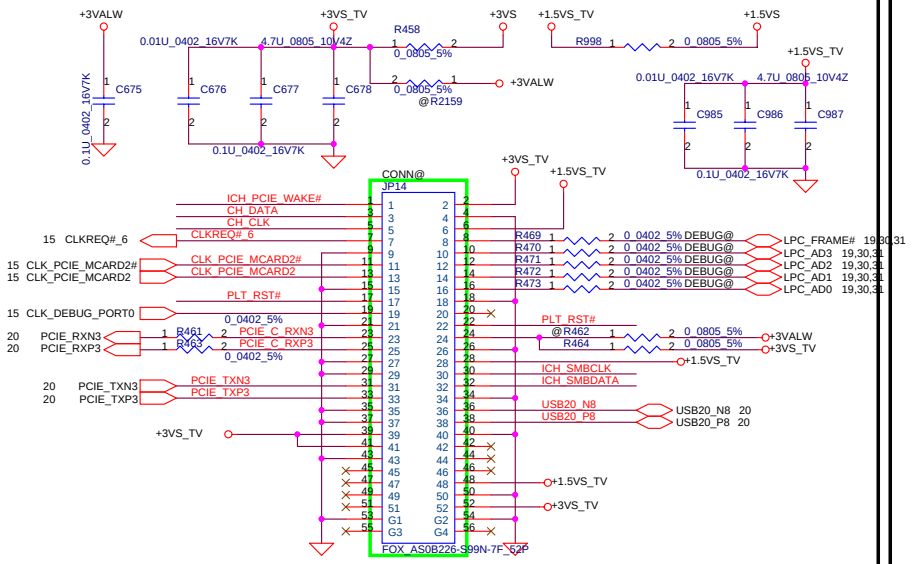
Compal Electronics, Inc.

Title: 88E8042 10/100 LAN

Size: Custom | Document Number: LA-4081P | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 23 of 44

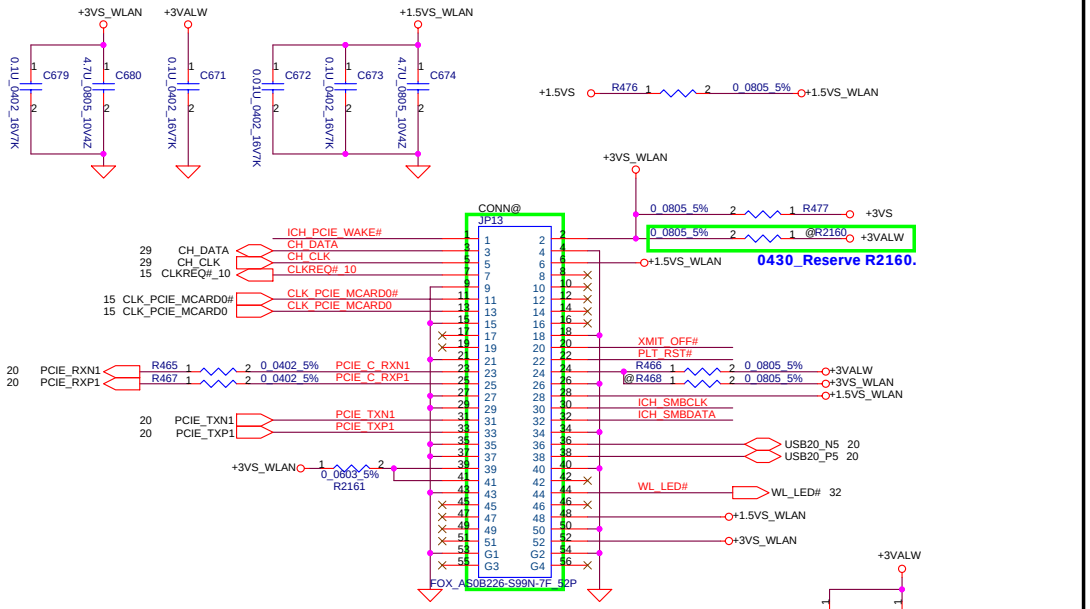
Mini Card 0--TV tuner



Follow 17" DIS.

Power Rail	Voltage Tolerance	Primary Power		Auxiliary Power
		Peak (Max) mA	Normal (Max) mA	Normal (Max) mA
+3.3V	+/- 9%	1000	750	
3.3Vaux	+/- 9%	330	250	250 (Wake Enable) 5 (Wake Disable)
+1.5V	+/- 5%	500	375	N/A

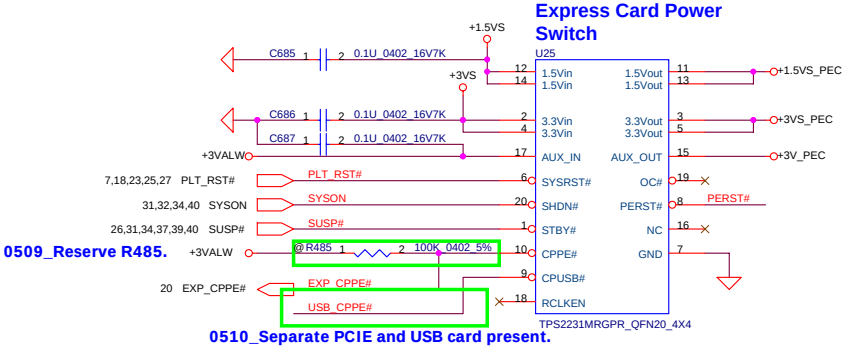
Mini Card 2---WLAN



Follow 17" DIS.

New Card

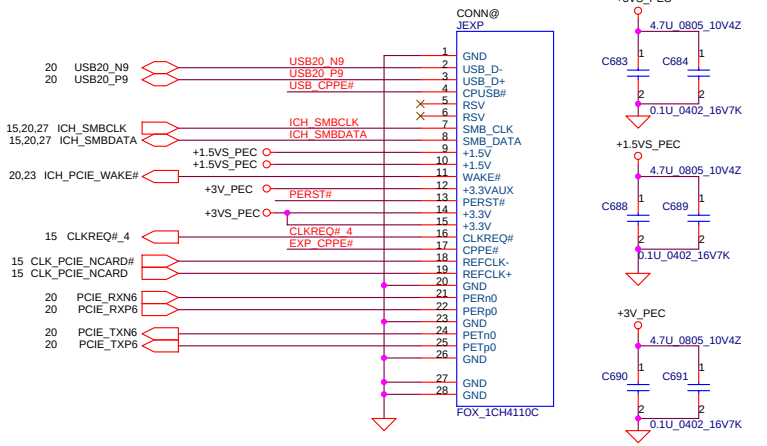
Express Card Power Switch



0509_Reserve R485.

0510_Separate PCIE and USB card present.

Near to Express Card slot.

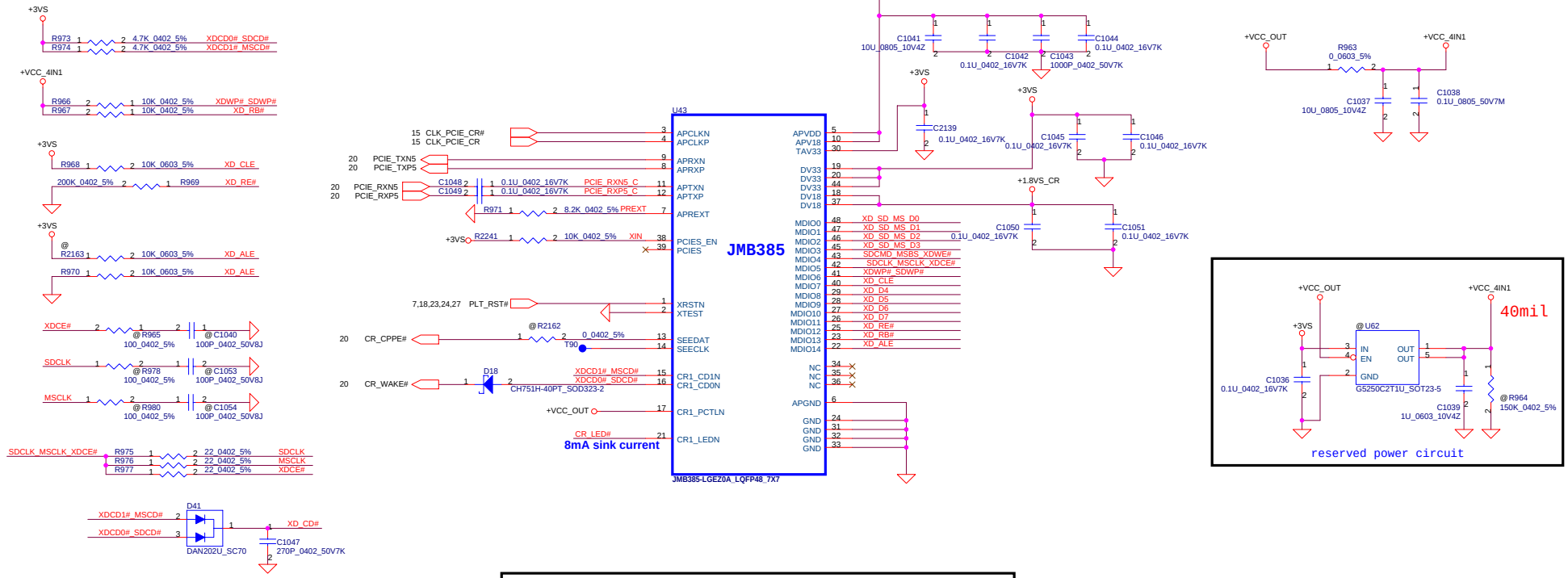


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

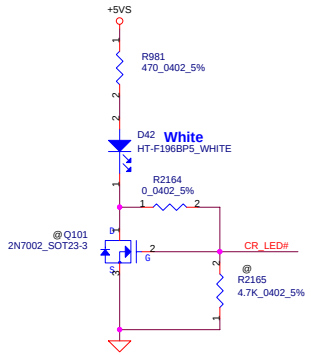
Follow 17" DIS.

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Title	*Compal Electronics, Inc.* *WLAN, WWAN, New Card*
Size	Document Number: *Montevina Consumer Discrete* — Rev: 0.3
Date: Friday, May 23, 2008	Sheet 24 of 44

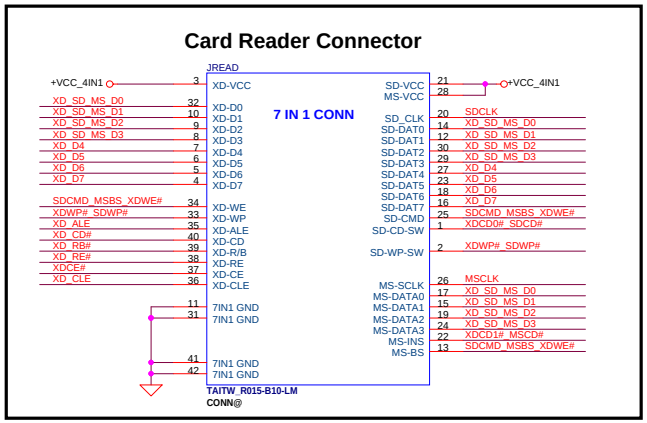


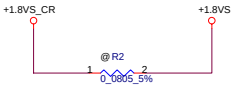
White LED: VF=3V, IF = 5mA, Res = 56ohm



01/03 Change Cardreader LED control

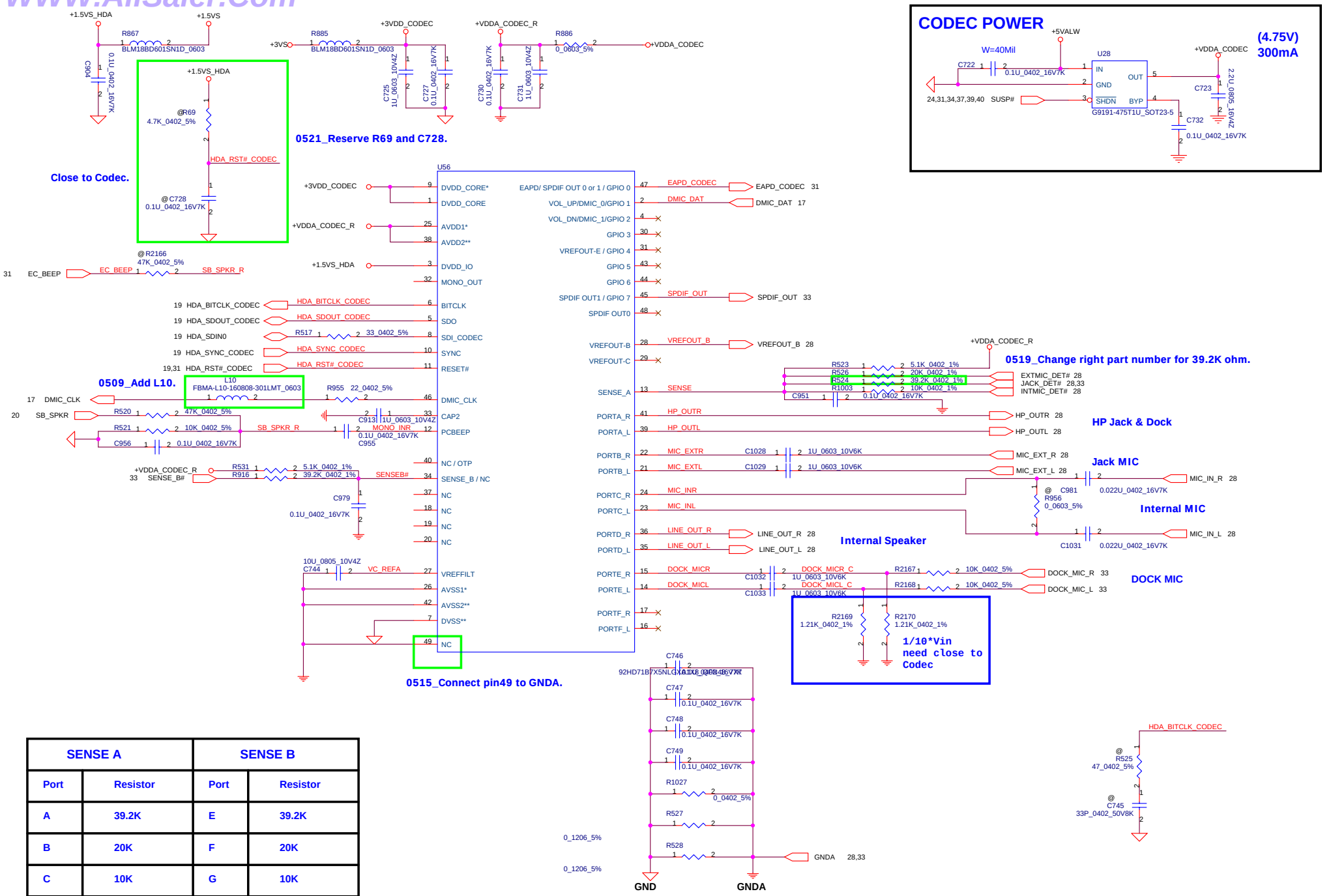
02/13 Direct driver LED





Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

Compal Electronics, Inc.			
Title: USB CardReader&CONN			
Size: Custom	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Friday, May 23, 2008	Sheet 25 of 44		

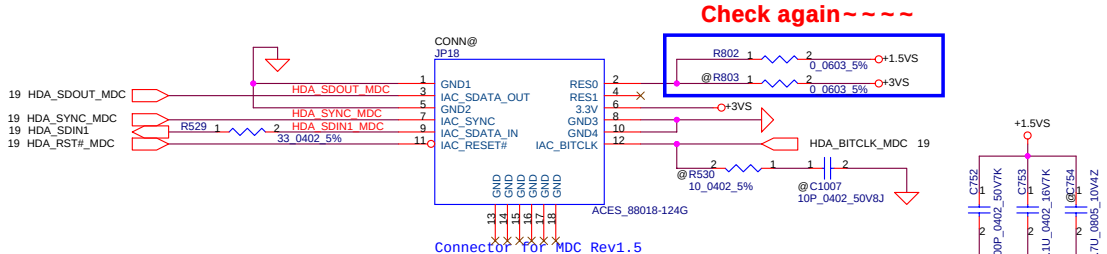


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

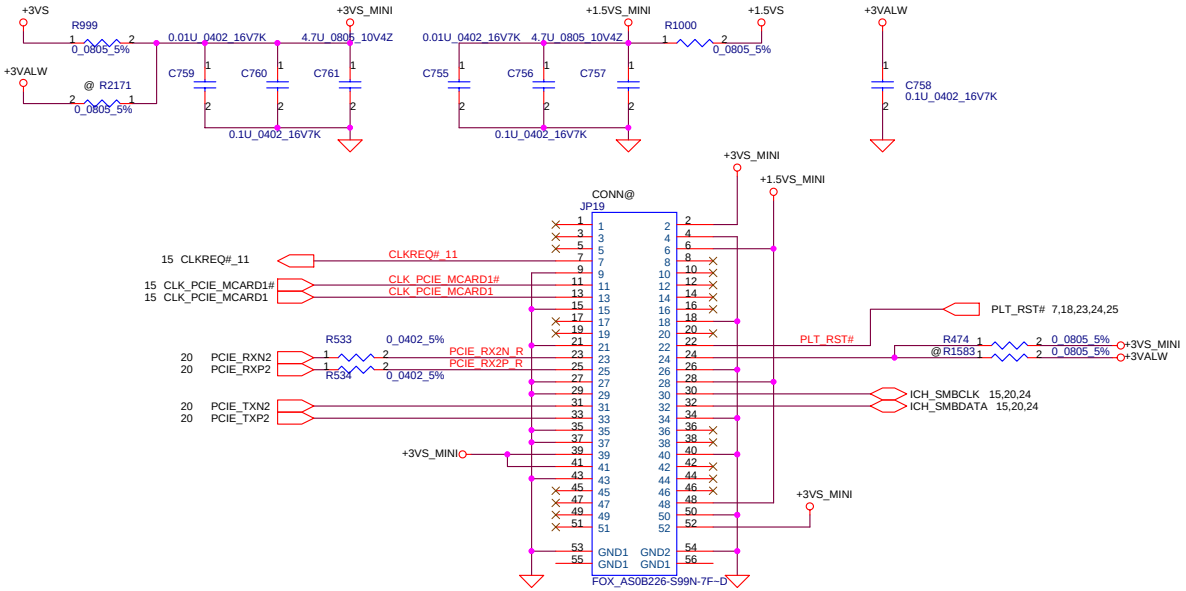
Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2006/07/26

Title	Codec_IDT9271B7		
Size: Custom	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Monday, May 26, 2008	Sheet 26 of 44		

MDC 1.5 Conn.

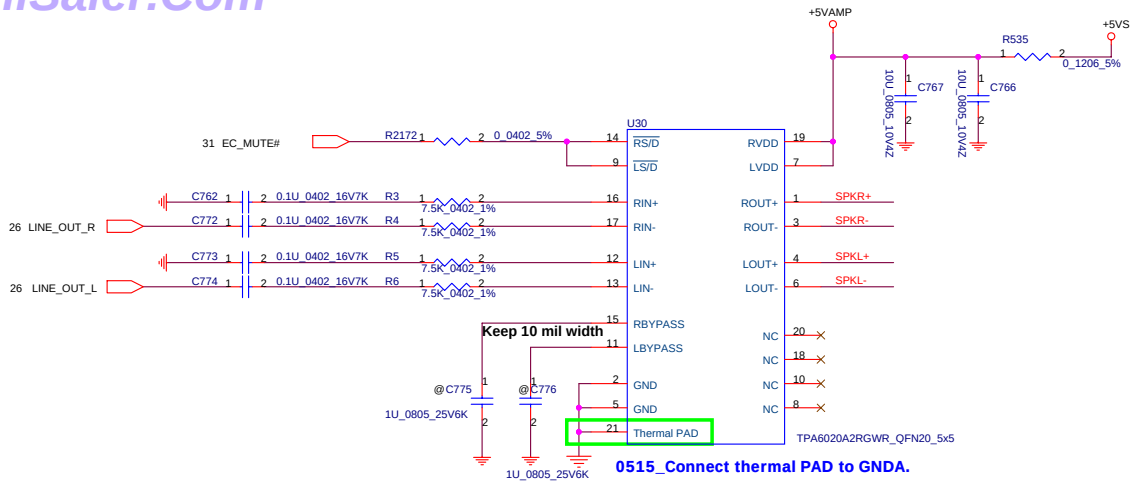


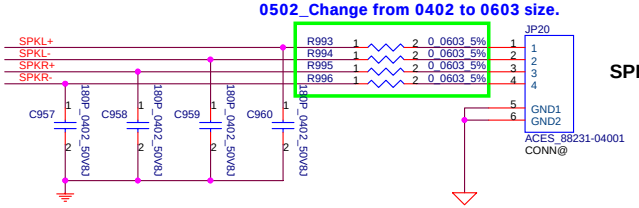
Mini Card 1---Robson



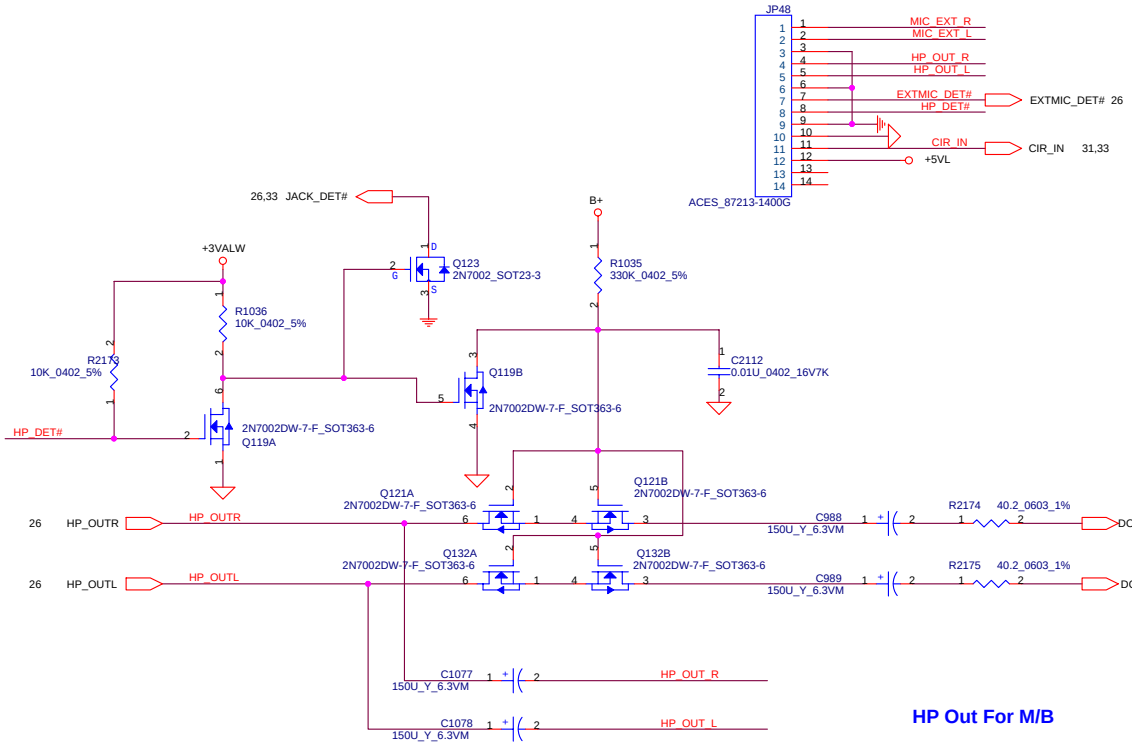
Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: MDC 1.5 & Robson			
Size:	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Friday, May 23, 2008	Sheet 27 of 44		



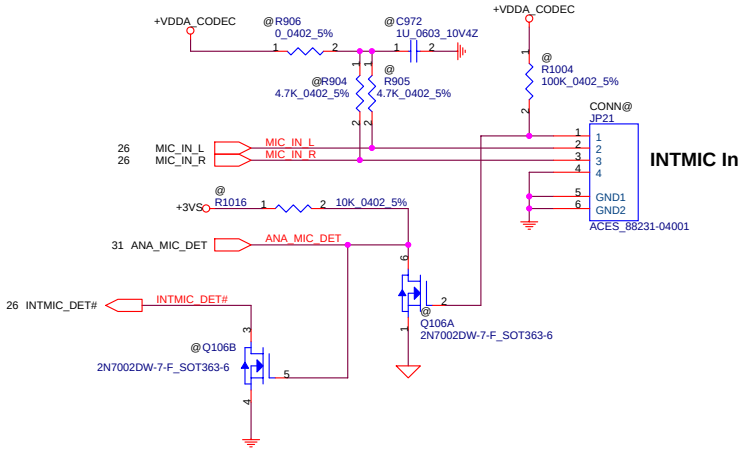


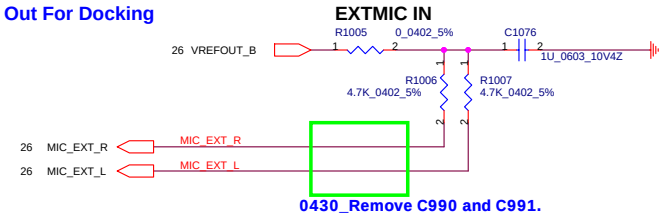
Audio & USB board conn



HP Out For Docking

HP Out For M/B

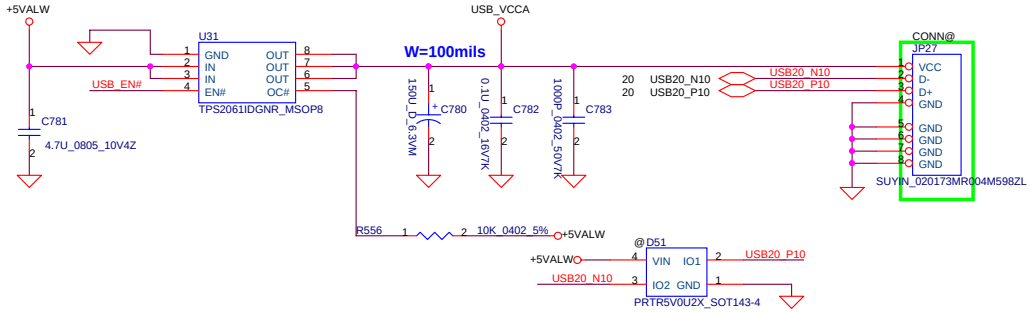




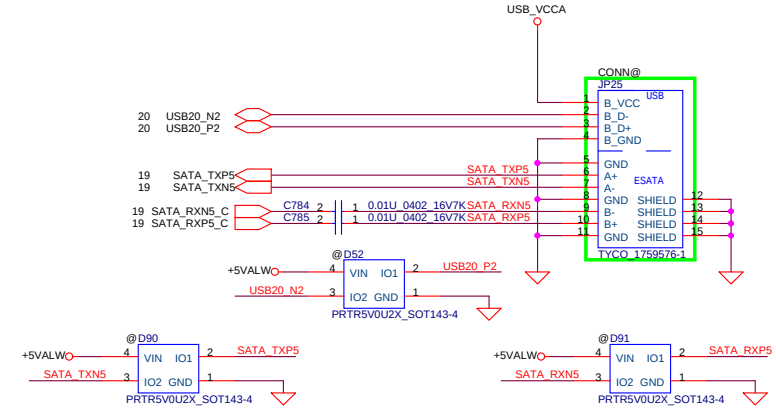
Security Classification	Compal Secret Data		
Issued Date	2006/10/26	Deciphered Date	2006/07/26

Title	AMP & Audio Jack		
Size: Custom	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Monday, May 26, 2008	Sheet 28 of 44		

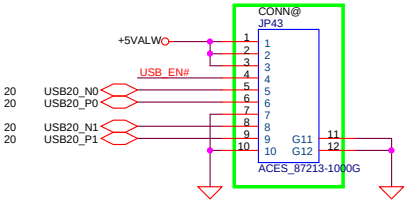
Left side USB CONNECTOR



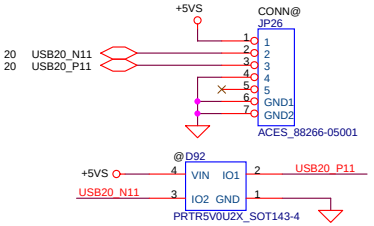
Left side eSATA/USB combination Connector



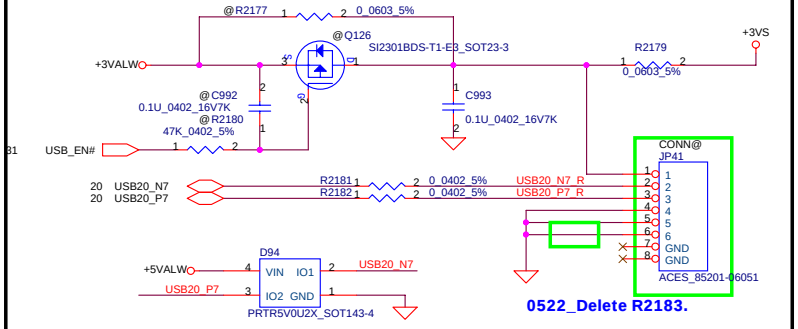
USB cable connector for Right side



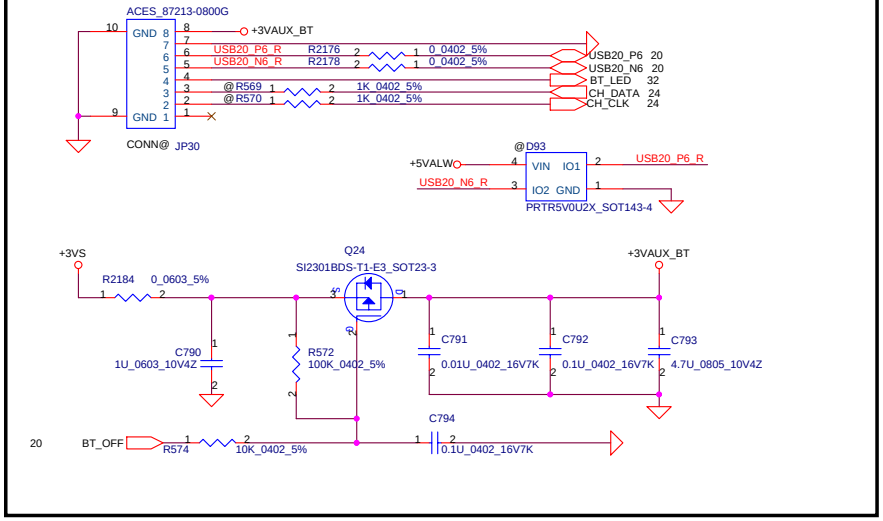
Touch screen connector



Finger printer



BT Connector



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: USB, BT, eSATA

Size: Document Number: Montevina Consumer Discrete — Rev: 0.3

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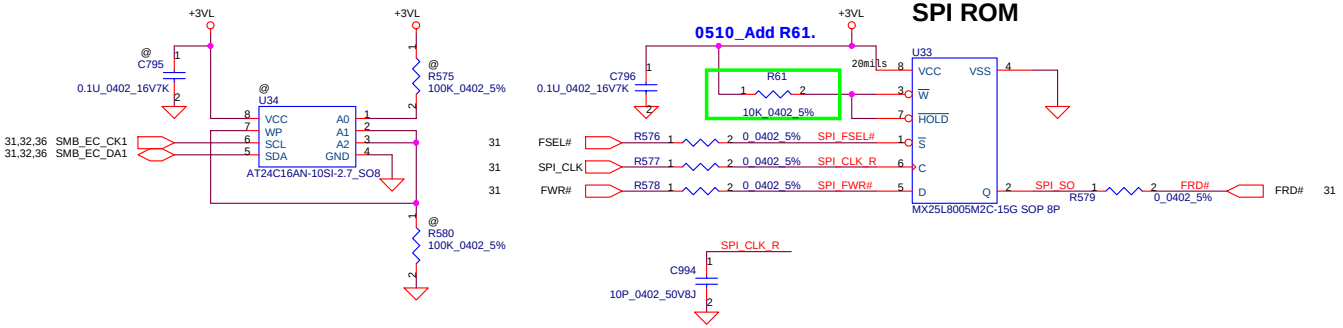
SPI ROM

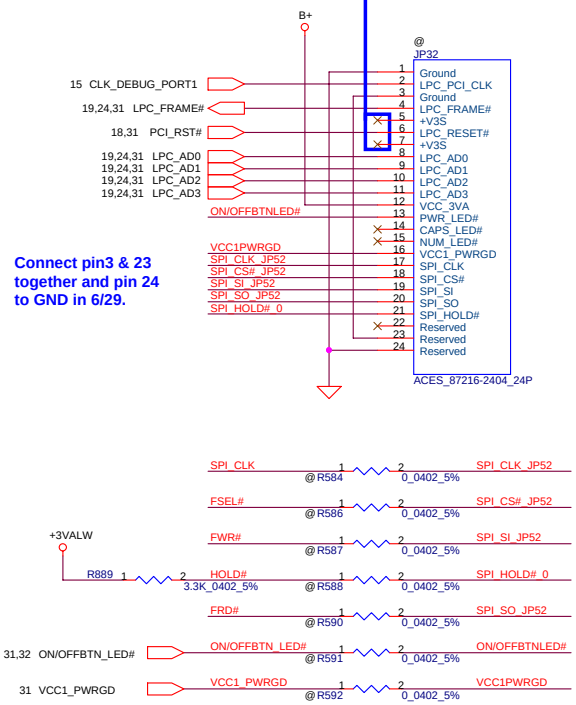
0510_Add R61.



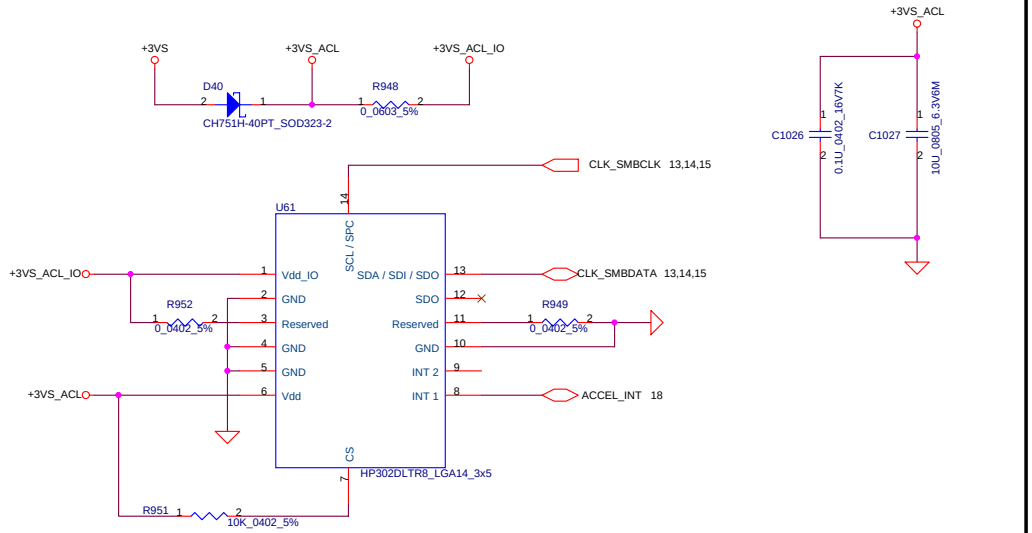
LPC debug port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13

Connect pin3 & 23 together and pin 24 to GND in 6/29.

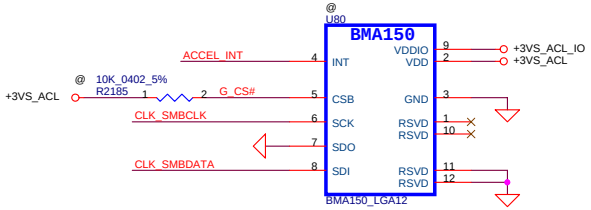


Acceleromter-1



Acceleromter-2

U61 & U80 must be close



HDCP ROM

0512_Remove HDCP SPI ROM.

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: BIOS ROM

Size | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 30 of 44

0512_Remove C1009.

0430_Change from 100K ohm to 8.2K ohm.

0502_Change from +3VALW to +3VL.

0430_Change from +3VL to +3VALW.

17" INT_KBD CONN.(TYPE "D" KB)

CONN@ JP34

For C0 Revision

For EMI

0430_Reverse D54.

EC DEBUG port

U37 KB926QFC0_LQFP128_14X14

Security Classification	Compal Secret Data
Issued Date	2006/10/26
Deciphered Date	2006/07/26
Title	EC KB926/KB Conn.
Size	Document Number: Montevina Consumer Discrete
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Date:	Friday, May 23, 2008
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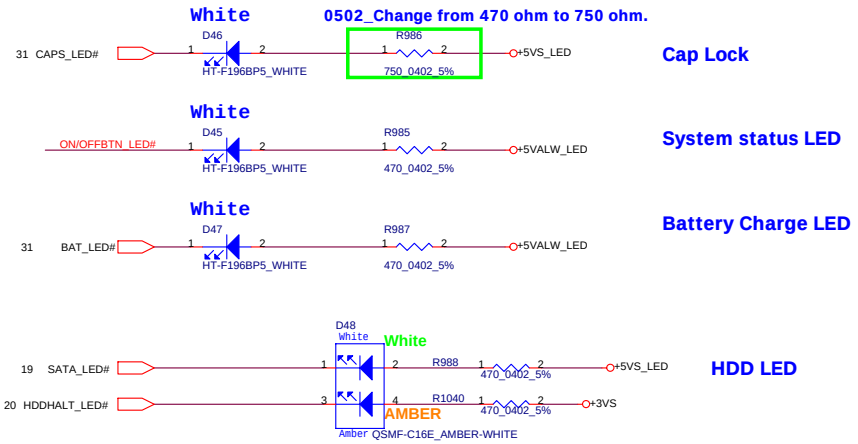
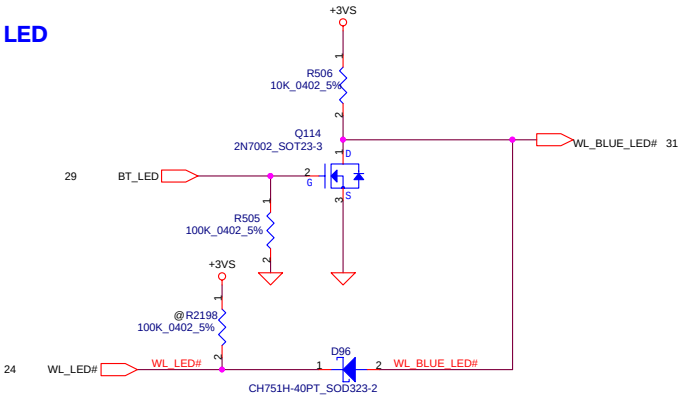
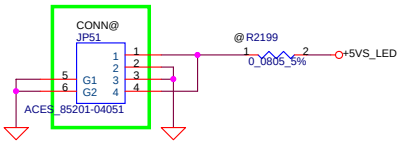
LED



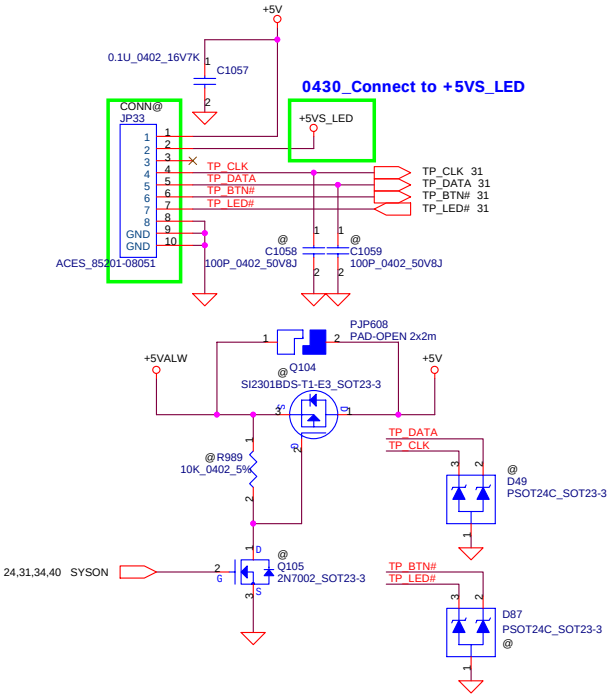
Mini-PCIE Card LED



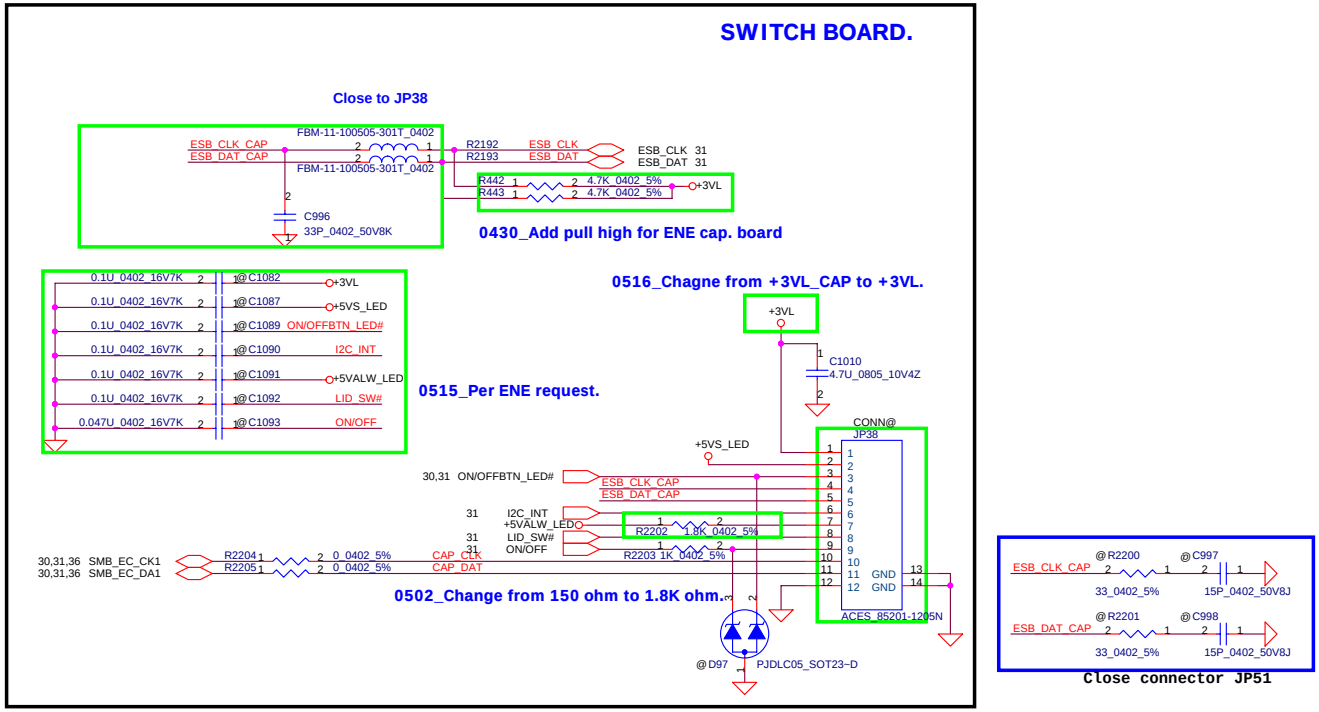
K/B backlight



T/P Board (Inculde T/P_ON/OFF)



SWITCH BOARD.

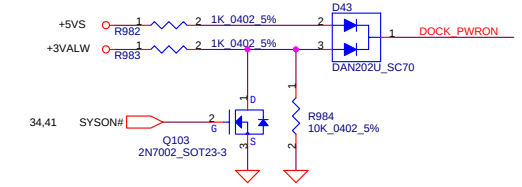


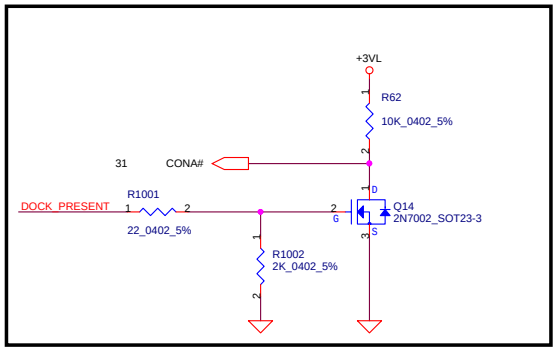
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

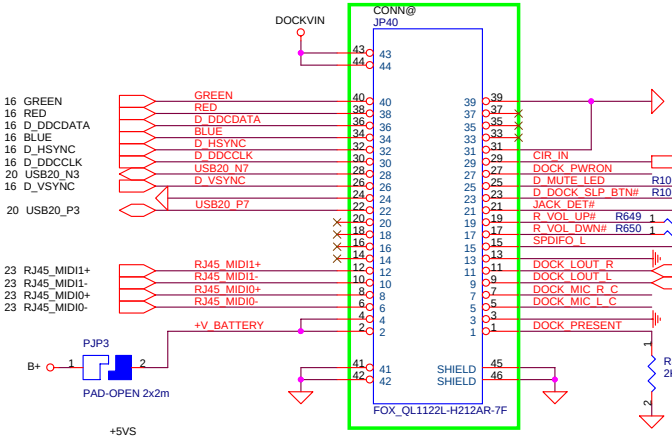
Title	Compal Electronics, Inc.		
	KBD, ON/OFF, SW, CIR		
Size	Document Number		Rev
	Montevina Consumer Discrete		0.3
Date:	Monday, May 26, 2008	Sheet	32 of 44

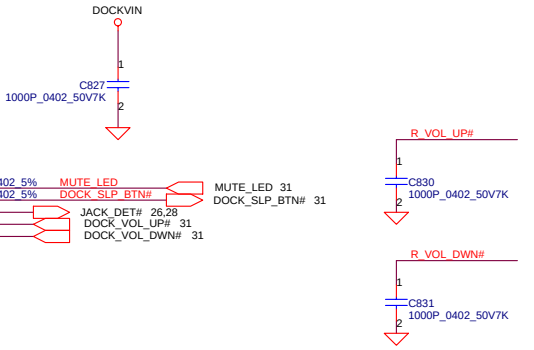
Atlas/ Saturn Dock

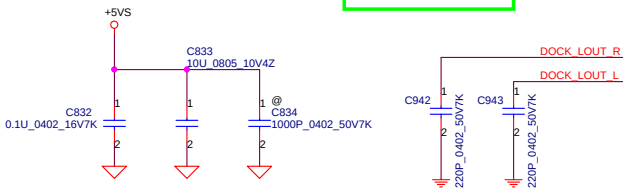
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

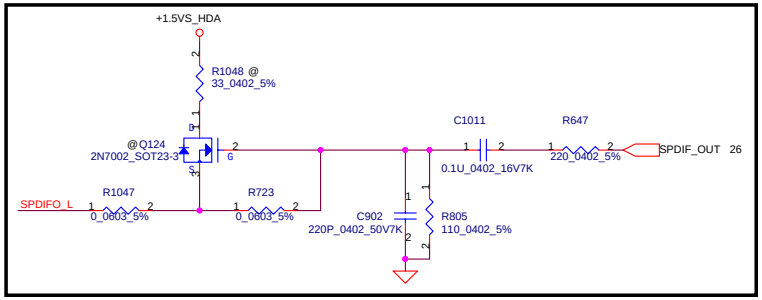


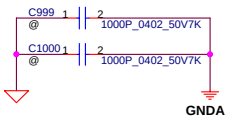


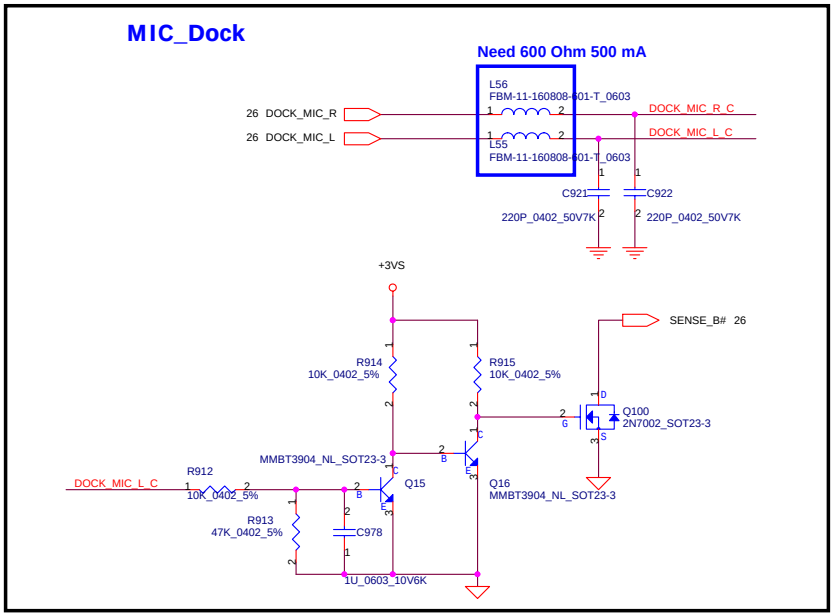












Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

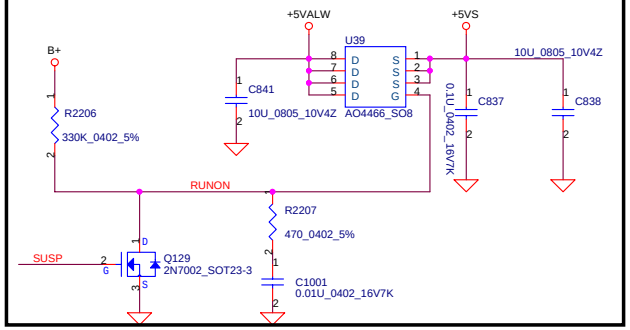
Compal Electronics, Inc.

Title: DOCK CONN.

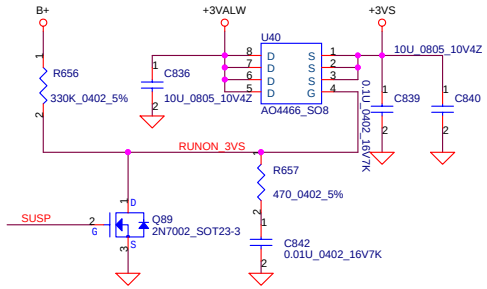
Size: Custom | Document Number: Montevina Consumer Discrete | Rev: 0.3

Date: Friday, May 23, 2008 | Sheet 33 of 44

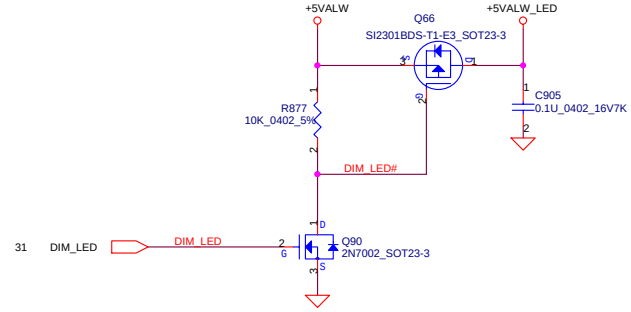
+5VALW to +5VS Transfer

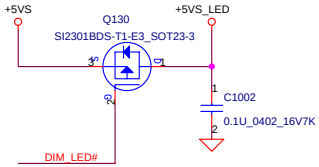


+3VALW to +3VS Transfer

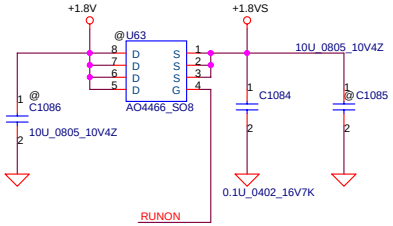


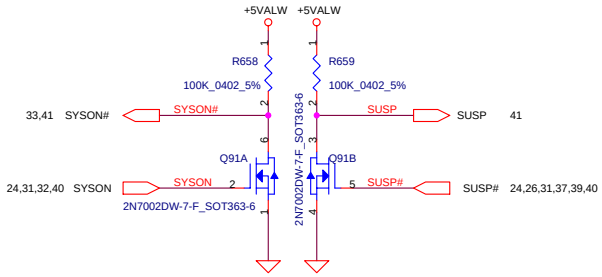
DIM LED





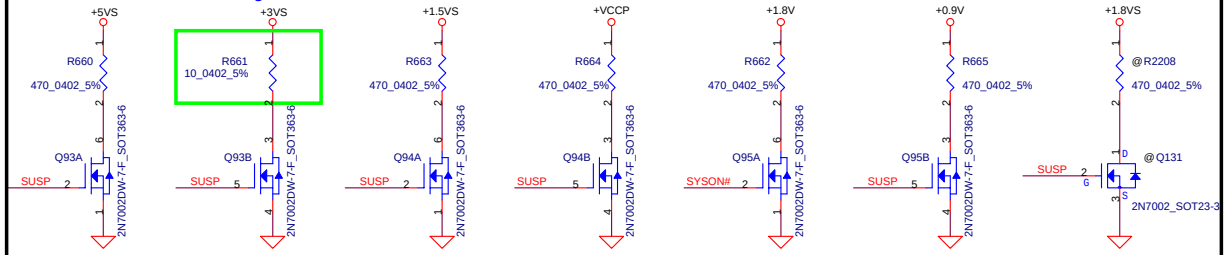
+1.8V to +1.8VS Transfer

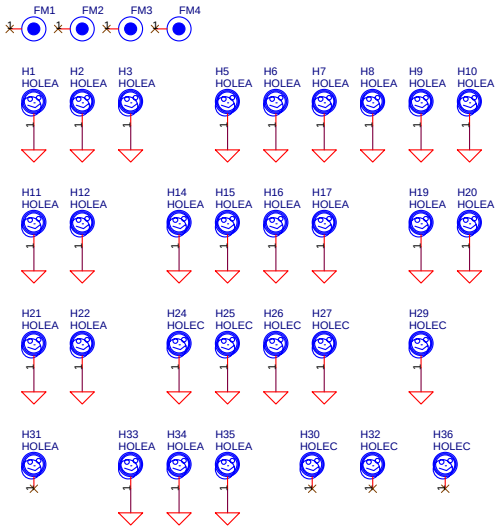




Discharge circuit

0512_Change from 470 ohm to 10 ohm.





Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Title	*Compal Electronics, Inc.*
	DC/DC Interface
Size	Document Number: *Montevina Consumer Discrete*
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EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommanded)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB

0512_change from 4.7K to 3.09K ohm.

0522_Add R712 and pull high to +3VS_LS.

0522_Change from STHDLS10QTR to STHDLS10TQTR.

0505_Reserve R45 for new HDMI level shifter.

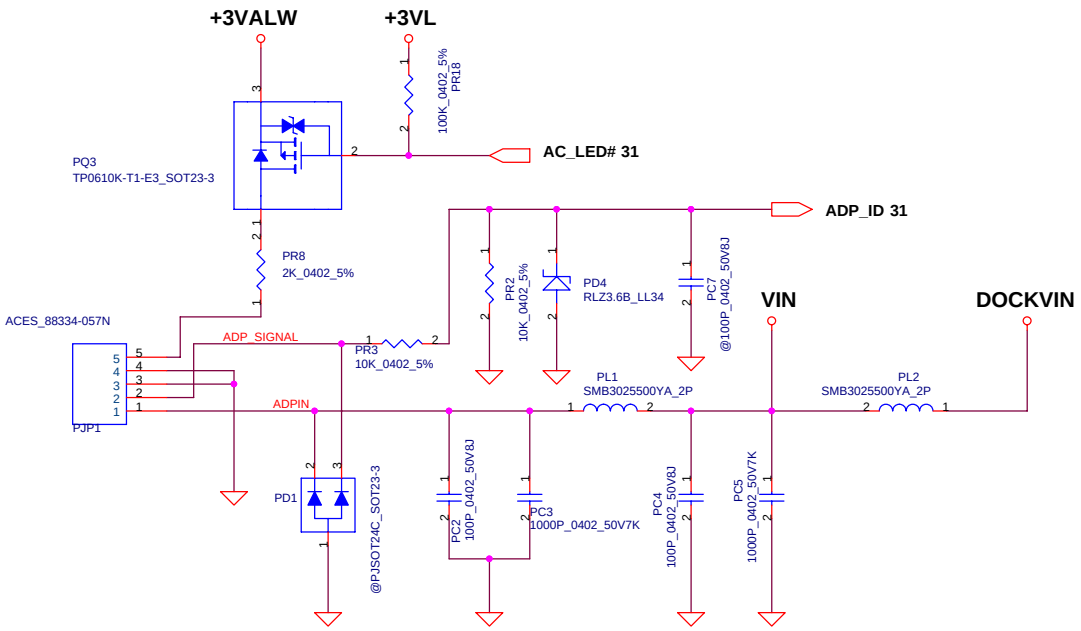
0522_Stuff R45 and reserve Q102 and R563.

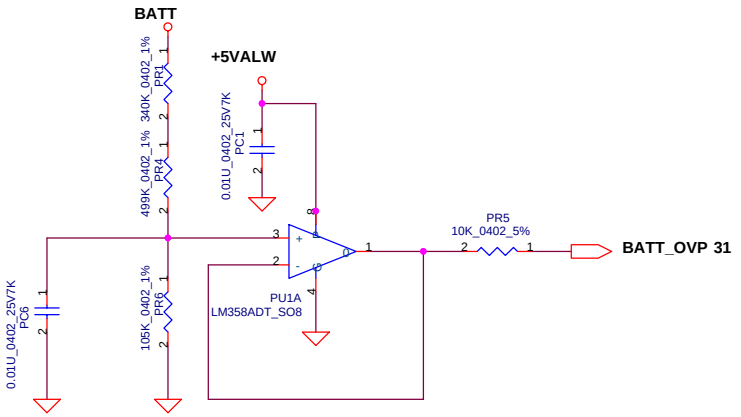
HDMI Connector

Internal pull down in STHDLS101.

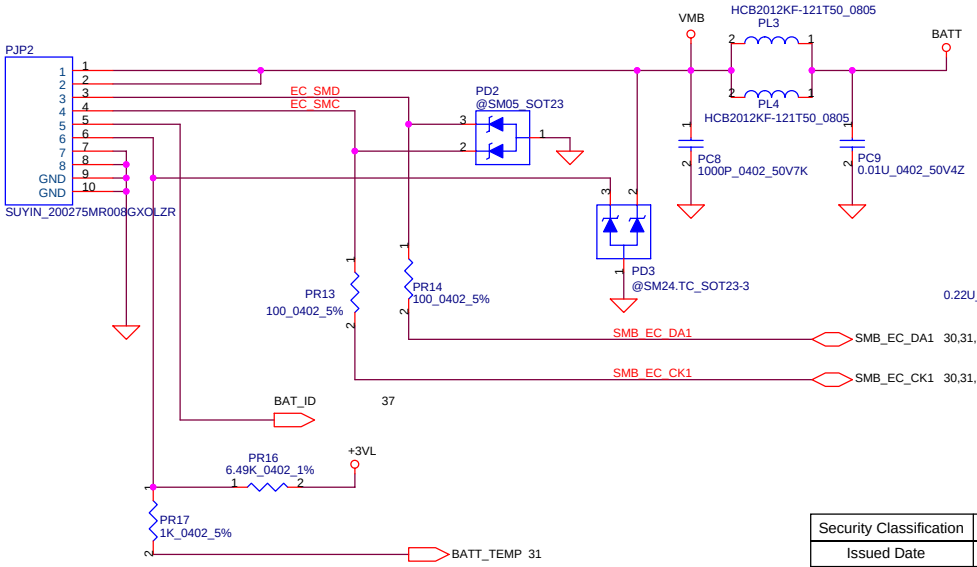
Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

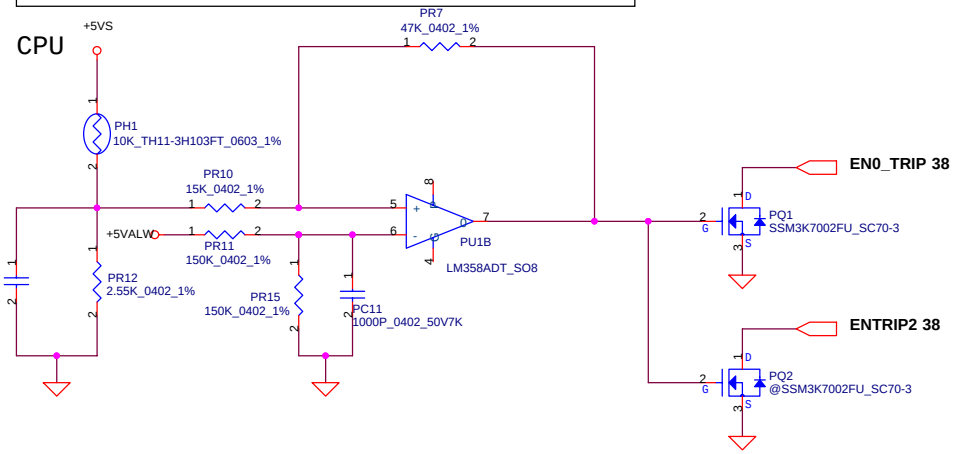
Title	Compal Electronics, Inc.
	HDMI LS & Conn.
Size: Custom	Document Number: Montevina Consumer Discrete
Rev	0.3
Date: Friday, May 23, 2008	Sheet 35 of 44





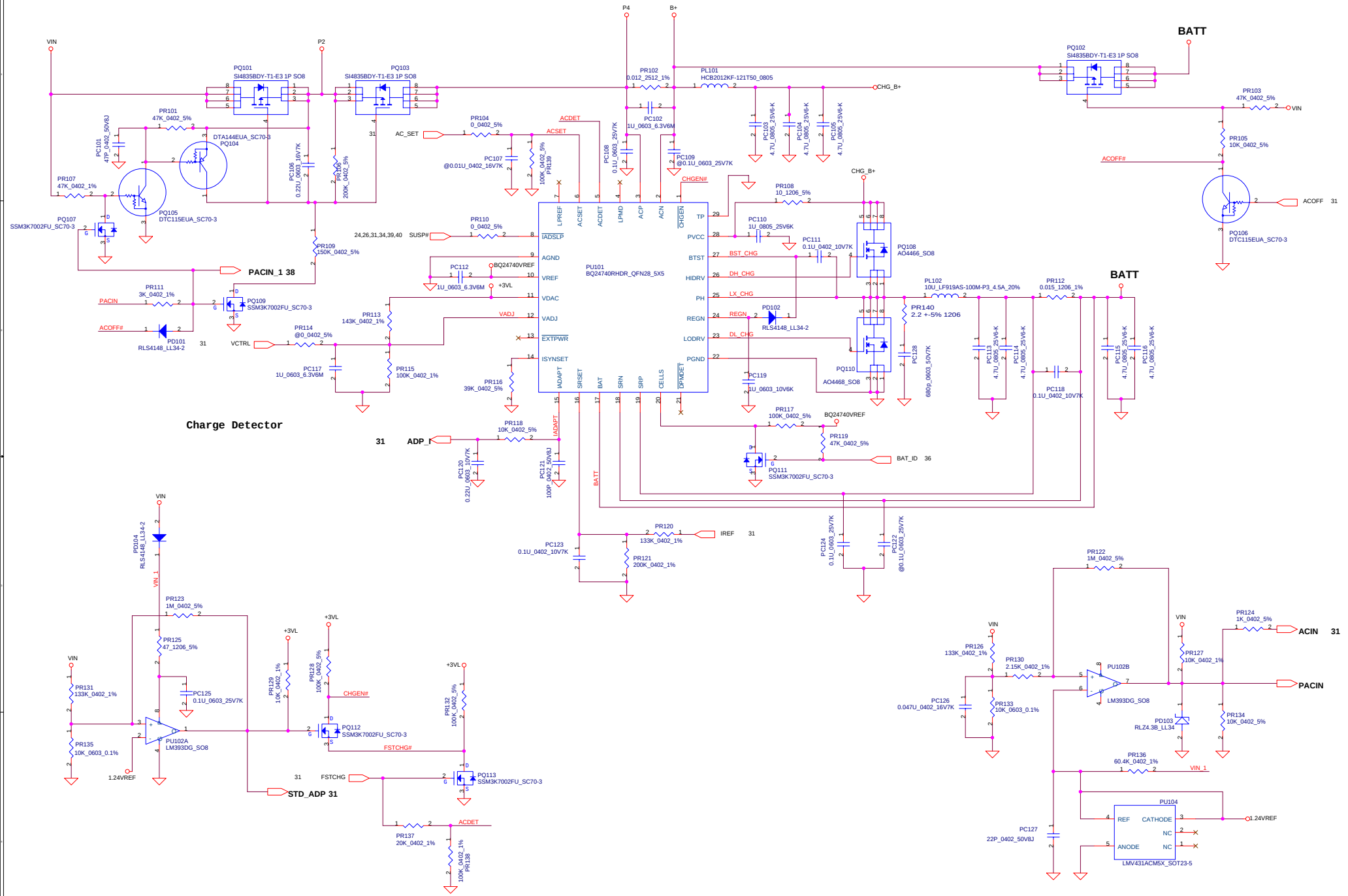
PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C





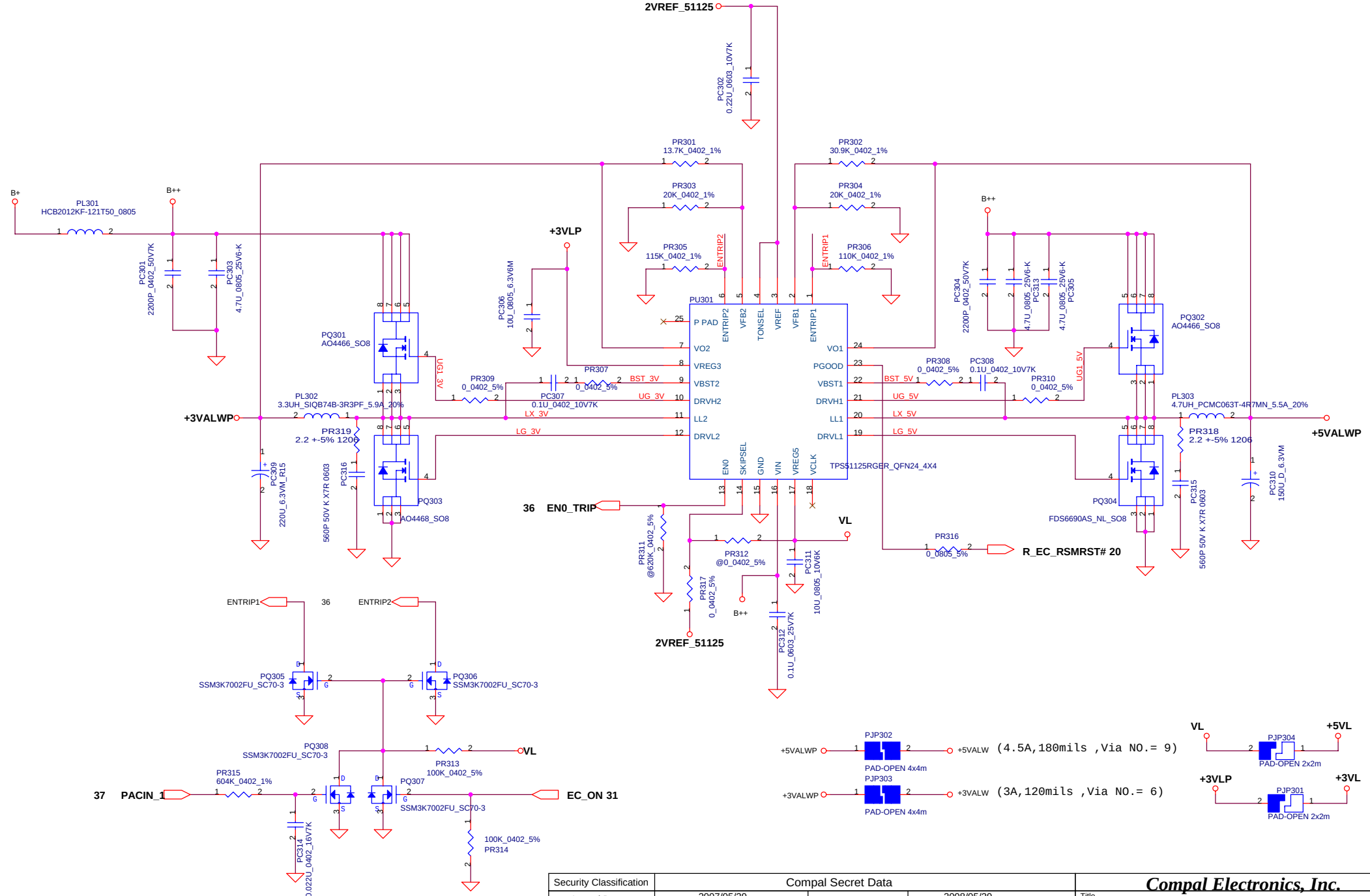
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title: DC Connector/CPU_OTP			
Size	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Friday, May 23, 2008	Sheet 36 of 44		



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title: Charger			
Size	Document Number: Montevina Consumer Discrete		Rev: 0.3
Date: Friday, May 23, 2008	Sheet 37 of 44		



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.			
Title	3.3VALWP/5VALWP		
Size	Document Number	Rev	
	Montevina Consumer Discrete	0.3	
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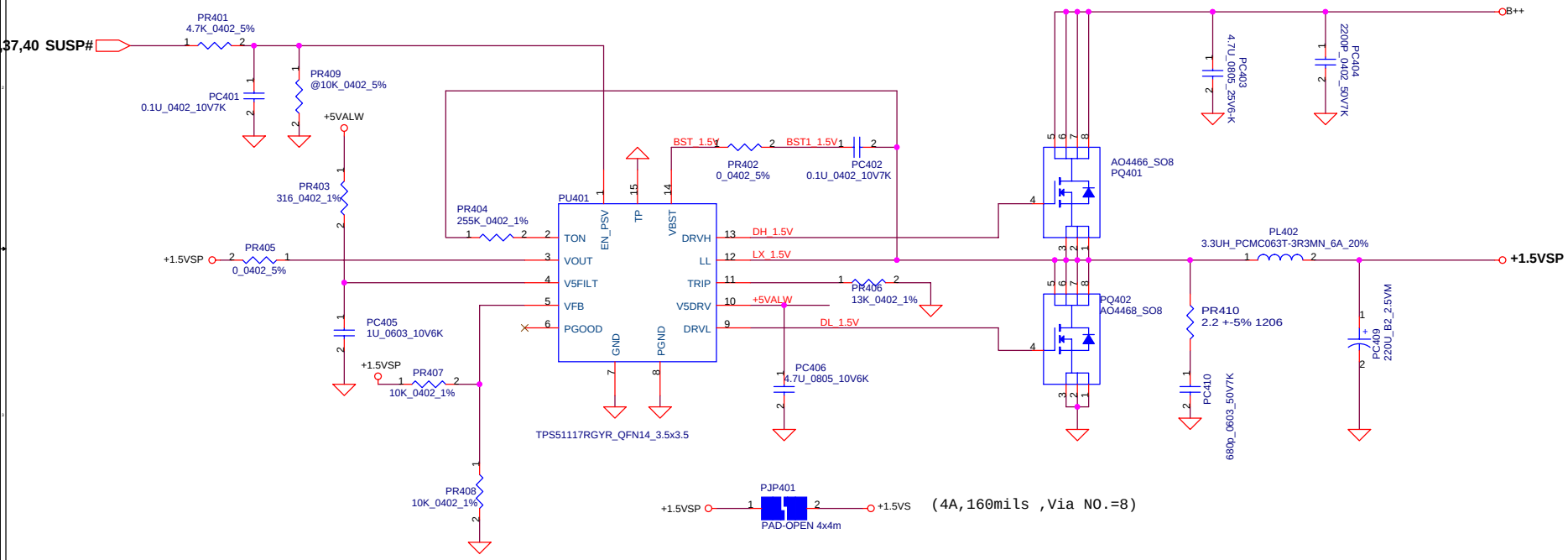


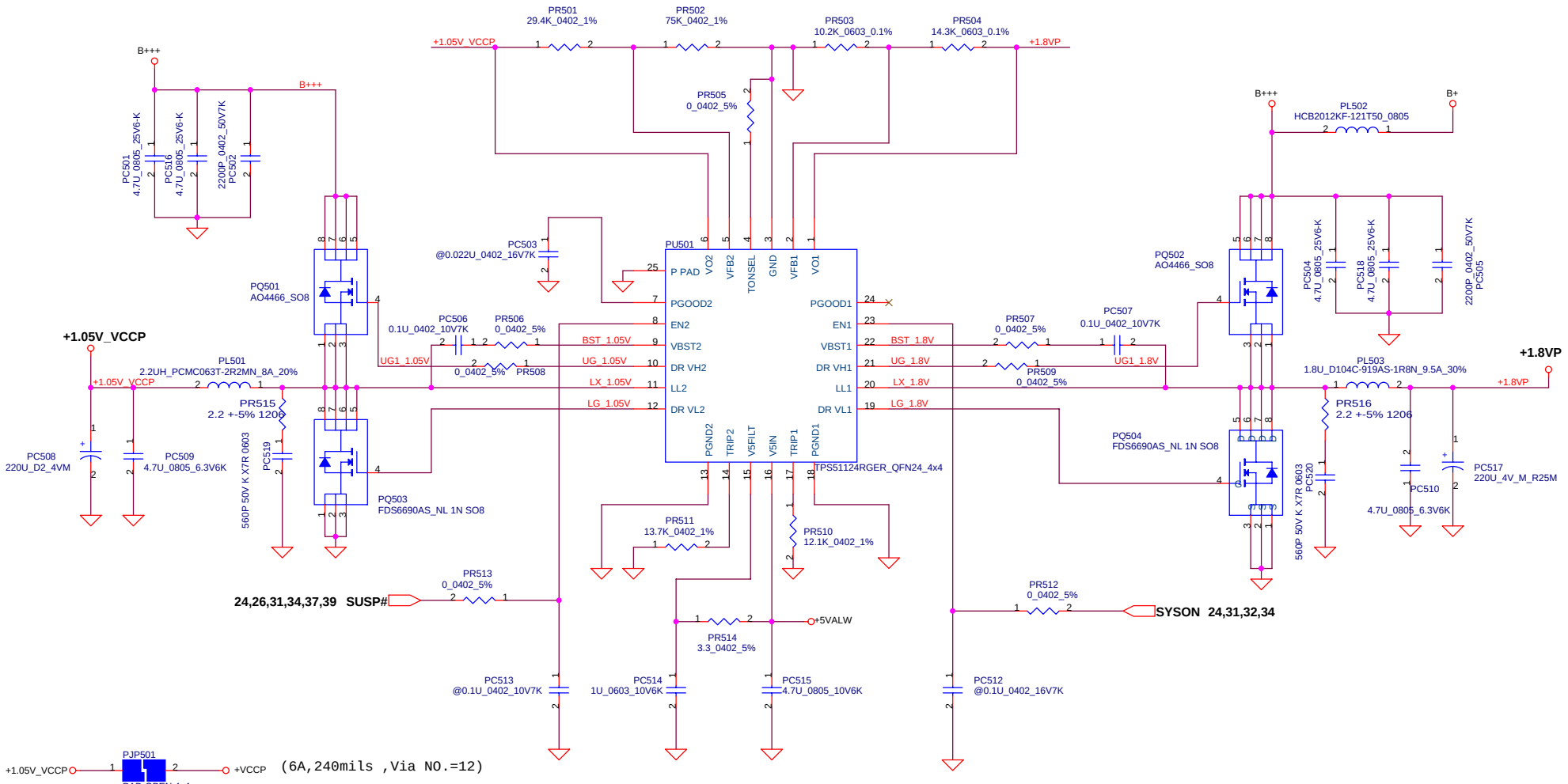
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.5VSP**

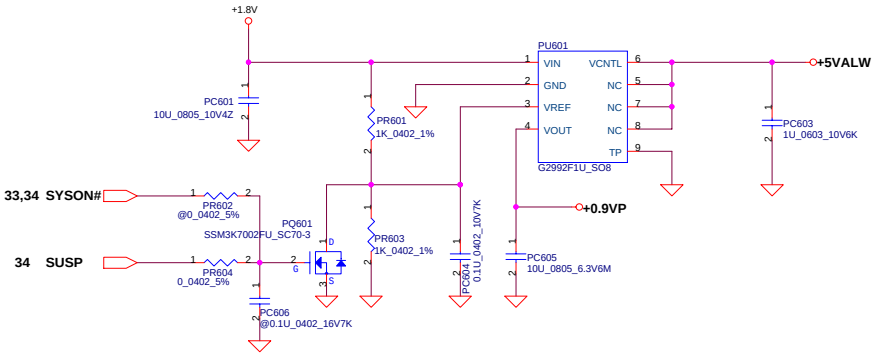
Size | Document Number: *Montevina Consumer Discrete* | Rev: 0.3

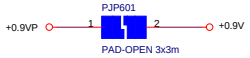
Date: Friday, May 23, 2008 | Sheet 39 of 44



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.		
Title: 1.05V_VCCP/1.8VP		
Size	Document Number: Montevina Consumer Discrete	Rev: 0.3
Date: Friday, May 23, 2008	Sheet 40 of 44	





(2A,80mils ,Via NO.= 4)

Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **0.9VP**

Size | Document Number: **Montevina Consumer Discrete** | Rev: 0.3

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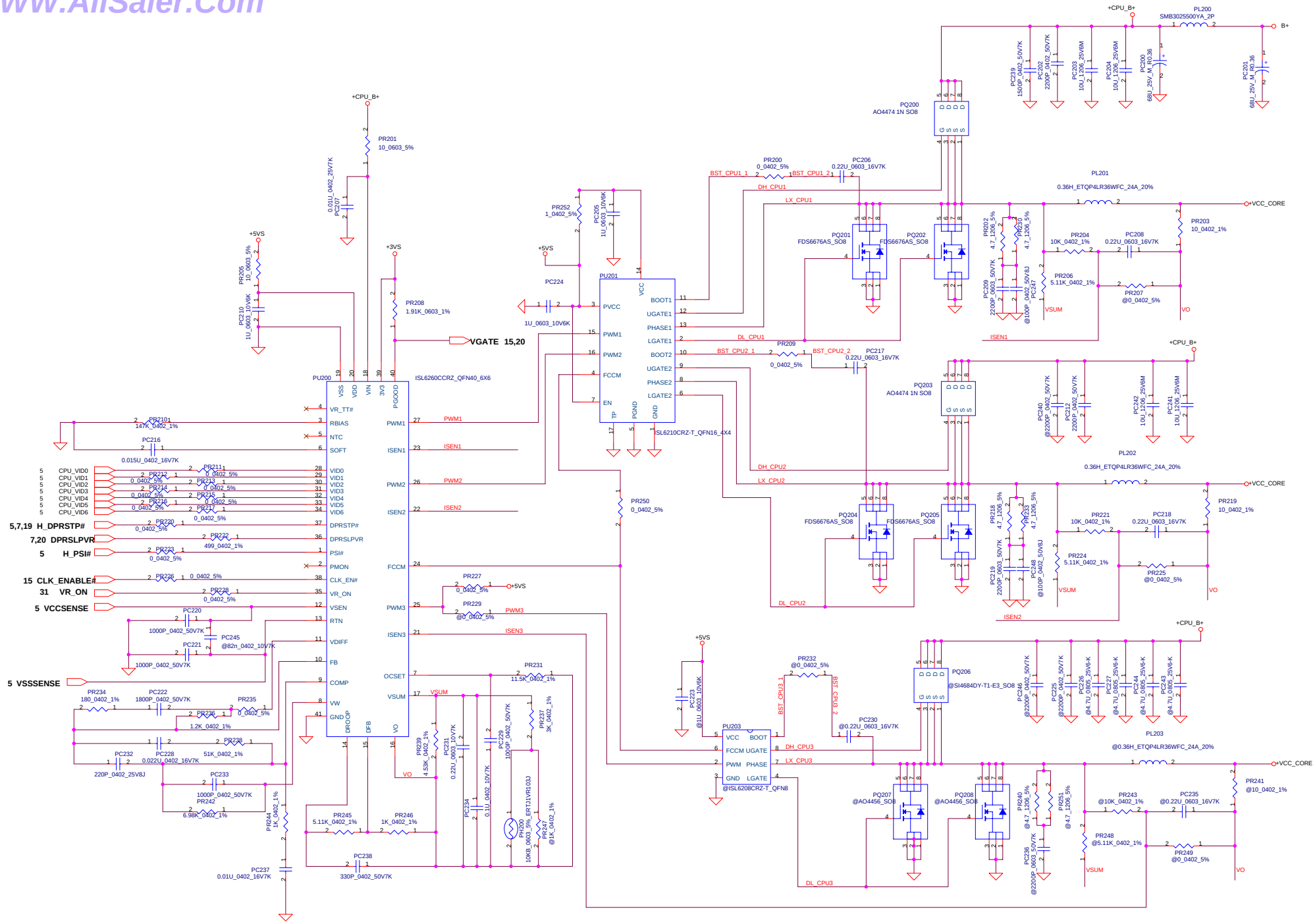

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.	
Title	CPU_CORE
Size: C	Document Number: Montevina Consumer Discrete
Rev	
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Title	<Title>		
Size A	Document Number <Doc>		Rev 0.3
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Item	PAGE	Fixed Issue	Request by	Modify List	Date	Note
01	04	System thermal shutdown when use NS thermal sensor	HW	Change R8 and R9 from 100 ohm to 0 ohm. Comfirm with SMSC this change is no risk for EMC1402.	0430	SI --> PV
02	31	Follow JAK00 DIS design	HW	Change R2189 and R615 from 100K ohm to 8.2K ohm.	0430	SI --> PV
03	31	Follow JAK00 DIS design	HW	Change EC_PME# pull high power rail from +3VL to +3VALW.	0430	SI --> PV
04	31	Solve AC LED always light even without AC adapter.	HW	Reverse D54 for AC_IN.	0430	SI --> PV
05	32	Solve T/P LED always light even power off.	HW	Change T/P LED power rail from +5VALW_LED to +5VS_LED.	0430	SI --> PV
06	24	Solve +3VS/+5VS has leakage power when S5 and S3.	HW	Reseve R2160.	0430	SI --> PV
07	09	Remove useless component because JAK00 do not support WWAN.	HW	Remove C1018~C1025.	0430	SI --> PV
08	28	Remove useless component.	HW	Remove C990 and C991 (1uF_0603).	0430	SI --> PV
09	31	For ENE cap. board.	HW	Add R442 and R443.	0430	SI --> PV
10	32	Fine-tune LED brightness (Power LED and Cap Lock LED).	HW	Change R2202 to 1.8K ohm and R986 to 750 ohm.	0502	SI --> PV
11	31	To avoid Lid function abnormal when battery mode only.	HW	Chagne Lid Switch power rail from +3VALW to +3VL.	0502	SI --> PV
12	28	Reserve 0603 package if EMI need to stuff bead.	HW	Change from 0402 to 0603 size.	0502	SI --> PV
13	35	To match ST new chipset (internal Hot Plug inverse circuit).	HW	Reserve R45.	0505	SI --> PV
14	09	Double confirm NB strapping setting with CRB. it can solve flash display.	HW	Change R70 to pull low ; reserve R65 ; reserve R66, R77 (reserve R66, R77 to solve flash display)	0505	SI --> PV
15	19	Follow Intel design guild, add pull high 10k ohm for SATA_LED#	HW	Add R49 and pull high to +3VS.	0505	SI --> PV
16	15	Reserve R714 because already pull high near North Bridge.	HW	Reserve R714.	0505	SI --> PV
17	24	Solve +3VS power leakage when S3/S4/S5.	HW	Reserve R485.	0505	SI --> PV
18	17	Solve internal MIC has noise when recording.	HW	Reserve C302 and C303.	0509	SI --> PV
19	26	Solve EMI issue for digital MIC (follow Vader DIS).	EMI	Add L10.	0509	SI --> PV
20	30	Follow common design.	HW	Add pull high R61 for SPI WP# and HOLD#.	0510	SI --> PV
21	19	Follow Intel check list.	HW	Change R363 from 180K ohm to 20K ohm and C538 from 0.1uF to 1uF.	0510	SI --> PV
22	24	Follow vender's recommend.	HW	Separate PCIE and USB card present.	0510	SI --> PV
23	04	Delete XDP debug port to solve EMI issue.	EMI	Delete JP42, R730, R733~R735, R738~R741, C851.	0512	SI --> PV
24	15	Delete XDP debug port to solve EMI issue.	EMI	Delete R134 and R135 (Remove XDP clock for XDP port).	0512	SI --> PV
25	20	Remove external HDCP interface.	HW	Delete R440~R441, R1008~R1010.	0512	SI --> PV
26	30	Remove external HDCP ROM.	HW	Delete R438~R439, R415, R422, R427, C304, and U8.	0512	SI --> PV
27	20	Remove useless function.	HW	Reserve R1040.	0512	SI --> PV
28	35	Fine-tune HDMI signal quality.	HW	Change R706 from 4.7K to 3.09K ohm.	0512	SI --> PV
29	15	Solve EMI issue.	EMI	Reserve R126.	0512	SI --> PV
30	34	Solve leakage power for VCC_HV of north bridge when S3/S4/S5..	HW	Base on Intel recommend, change R661 of +3VS discharge circuit from 470 ohm to 10 ohm	0512	SI --> PV
31	31	Solve can not power on issue if +3VL output cap. total over 20uF.	HW	Delete C1009.	0512	SI --> PV
32	28	Audio fail for ESD test.	ESD	Connect U30 thermal PAD to GNDA.	0515	SI --> PV
33	26	Audio fail for ESD test.	ESD	Connect U56 thermal PAD to GNDA.	0515	SI --> PV
34	16	Follow Blade/Vader DIS use the same material.	HW	Change L13, L15, L17.	0515	SI --> PV
35	32	Solve EMI issue for ENE cap. board.	ENE	Stuff R2192, R2193, and C996.	0515	SI --> PV
36	32	Solve EMI issue for ENE cap. board.	ENE	Add C1082, C1087, C1089~C1093.	0515	SI --> PV
37	32	Remove useless parts (LDO for ENE cap. board).	HW	Remove U79, R2139, C2126, C2127, PJP607.	0516	SI --> PV
38	32	Remove useless parts (LDO for ENE cap. board).	HW	Chagne JP38 pin1 power from +3VL_CAP to +3VL.	0516	SI --> PV
39	26	Solve MIC jack detect abnormal when plug in Dock.	HW	Change to right part number for R524 (39.2K_0402).	0519	SI --> PV
40	20	Solve pop noise when press CTRL+ALT+DEL.	HW	Reserve R424.	0520	SI --> PV
41	17	Solve wavey issue in CRT monitor.	HW	Add PJP305 to sparate GND.	0521	SI --> PV
42	17	Remove useless part.	HW	Remove L8.	0521	SI --> PV
43	26	Solve ESD test fail for Audio.	HW	Reserve R69 and C728.	0521	SI --> PV
44	29	For ESD request.	ESD	Delete R2183.	0522	SI --> PV
45	35	There is inverse circuit internal in new version chipset for HPD signal.	HW	Change U50 from STHDLS10QTR to STHDLS10TQTR.	0522	SI --> PV
46	35	Reserve inverse circuit.	HW	Reserve Q102 and R563.	0522	SI --> PV
47	35	Follow vender's recommend.	HW	Add R712 and pull high to +3VS_LS.	0522	SI --> PV
48	10	To prevent wavy issue in CRT.	HW	Add C148.	0522	SI --> PV

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: PIR

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