COMPAL CONFIDENTIAL

MODEL NAME : *JAL21*

PCB NO : *LA-4042P (DAA00000T0L)*

BOM P/N : *43153331L01*

M09 Maybach DIS

uFCPGA Mobile Penryn
Intel Cantiga PM + ICH9M

2007-10-31

REV : 0.1

@ : Nopop Component

MB PCB

Part Number	Description
DAA00000R0L	PCB 03P LA-4051P REV0 M/B

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Title: Cover Sheet

Size | Document Number: LA-4042P | Rev: 0.1

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Block Diagram
Compal confidential
Model : JAL22

FAN
+FAN1_VOUT
page 18

Thermal
GUARDIAN III
EMC4002
+3.3V_SUS
page 18

Pentium-M
Penryn -4MB (Socket P)
uFCPGA CPU
+1.5V_RUN
+1.05V_VCCP
+VCC_CORE
478pin
page 7,8,9

CPU ITP Port
+1.05V_VCCP
page 7

Clock Generator
CK505
SLG8LP554
+3.3V_M
page6

CRT CONN
+5V_RUN
page 20

Video Switch
TS3DV520
+3.3V_RUN
page 20

VGA
VGA/SVID
SVID

NV G98
+FBVDDQ
+3.3V_RUN
+1.1V_GFX_PCIE
+GPU_CORE
page 51,52,53,54,55,56

PCIE-E 16X

H_A#(3..35)
System Bus
H_D#(0..63)
FSB 1066 MHz

INTEL
Cantiga
1329pin BGA
+1.5V_RUN
+1.8V_MEM
+1.05V_VCCP
+3.3V_RUN
+1.05V_M
page 10,11,12,13,14,15

Memory BUS (DDR2)
+1.8V_MEM 667/800 MHz

DDRII-DIMM X2
BANK 0, 1, 2, 3, 4 ,5 ,6 ,7 ,8
page 16,17
+0.9V_DDR_VTT
+1.8V_MEM

LVDS CONN
+5V_ALW
+3.3V_RUN on M/B Board
+PWR_SRC
page 19

LVDS
DPC

DP Switch
TS2DP512
+5V_RUN
page 21

DPB

DMI
+1.5V_RUN
100MHz

PCI BUS
+3VRUN 33MHz
IDSEL:AD17
(GNT#1,REQ#1)
(PIRQD#,PIRQB#,PIRQC#)

CardBus
R5C847
+3.3V_RUN
page 31,32

SNIFFER
IEEE1394
page 31

Through FPC to IO Board

DOCKING PORT
+PWR_SRC
+1.8V_LAN_M
page 35

DP CONN
+5V_RUN
page 21

SD CONN
+3.3V_RUN
page 31

Through FPC to SD Board

DAI
SATA5
USB[8,9]
USB[7]

INTEL
ICH9-M
676pin BGA
+5V_ALW
+5V_RUN
+RTC_CELL
+3.3V_RUN
+3.3V_ALW_ICH
+1.5V_RUN
+1.05V_VCCP
page 22,23,24,25

48MHz

USB[11]
USB[2,3] LEFT SIDE
USB[0,1] RIGHT SIDE

Trough LVDS Cable
USB Port
Camera
page 19

E-SATA
USB Port1 X1
Charger USB Port X1
+5V_ALW
page 33

SATA4

USB Ports X2
+5V_ALW
On IO/B

GLCI/LCI
Azalia I/F

S-ATA(4)
SATA1
SATA0

Intel Boazman
82567LF
+3.3V_ALW
+1.8V_LAN_M
+1V_LAN_M
page 29

LAN Switch
P13L500
+3.3V_LAN
page 30

PCI Express BUS
PCIE3
PCIE2
PCIE1

Mini Card 3
WPAN/BT/Robson
+3.3V_RUN
+1.5V_RUN
page 34

Mini Card 2
WLAN
+3.3V_WLAN
+1.5V_RUN
page 34

Mini Card 1
WWAN
+3.3V_RUN
+1.5V_RUN
page 34

SIM card
page 34

USB[6]
USB[4]
USB[5]

LPC BUS
+3V_RUN
33MHz

LPC BUS

E-Module
+5V_MOD
page 26

S-HDD
+3.3V_RUN
+5V_HDD
page 26

SPI

W25X32VSSIG
+3.3V_LAN
page 24

32Mbit

W25X32VSSIG
+3.3V_LAN
page 24

Azalia Codec
92HD71B
+3.3V_RUN
+VDDA
page 27

AMP & INT.
Speaker
+5V_RUN
page 28

RJ45
On IO/B

Trough LVDS Cable
Dig. MIC
+VDDA

DAI
SSM2602
+3.3V_RUN
page 27

DOCKING

RFID
page 36

USH I/F
BCM5880
TPM 1.2
+3.3V_RUN
+2.5V_AVDD_5880
+1.2V_AVDD_5880
page 36

USB[10]

SMSC KBC
MEC5035
+RTC_CELL
+3.3V_ALW
page 38

SCREW HOLE LED
page 42

DC IN
BATT IN
page 43

3V/5V
page 44

GPUCORE / 1.1V
page 41

1.5V/1.05V
page 45

Selector
page 40

1.8V/0.9V
page 46

CHARGER
page 48

VCORE (IMVP-6)
page 47

73S8009CN
+3.3V_RUN
page 36

Smart Card
page 36

USBH

ME & LED
page 42

SMBus

BC

SPI

SST25VF
16Mbit
+3.3V_ALW
page 38

BC BUS

Expend GPIO
ECE1088
+3.3V_ALW
page 39

MDC
+3V_SUS

HeadPhone &
MIC Jack
+3.3V_RUN

On IO/B

RJ11

Through Cable

Biometric
+3.3V_RUN
page 33

ECE1077
+3.3V_ALW

Touch Pad
page 39

Int.KBD &
Stick
page 39

Trough Cable

BC BUS

SMSC SIO
ECE5028
+3.3V_ALW
page 37

DOCK LPC BUS

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Title: Block Diagram

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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.8V_MEM	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +0.9V_DDR_VTT +GPU_CORE +VCC_CORE +1.05V_VCCP +FBVDDQ +1.1V_GFX_PCIE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C847	AD17	REQ#1 / GNT#1	PIRQ[B..D]

	USB PORT#	DESTINATION
ICH9-M	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Bottom)
	3	JESA1 (Ext Left Side TOP)
	4	WLAN
	5	WWAN
	6	WPAN
	7	Card Bus/Express card
	8	DOCKING
	9	DOCKING
	10	USH->BIO
	11	Camera

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 BT/UWB
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	10/100/1G LAN

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Title: Index and Config.

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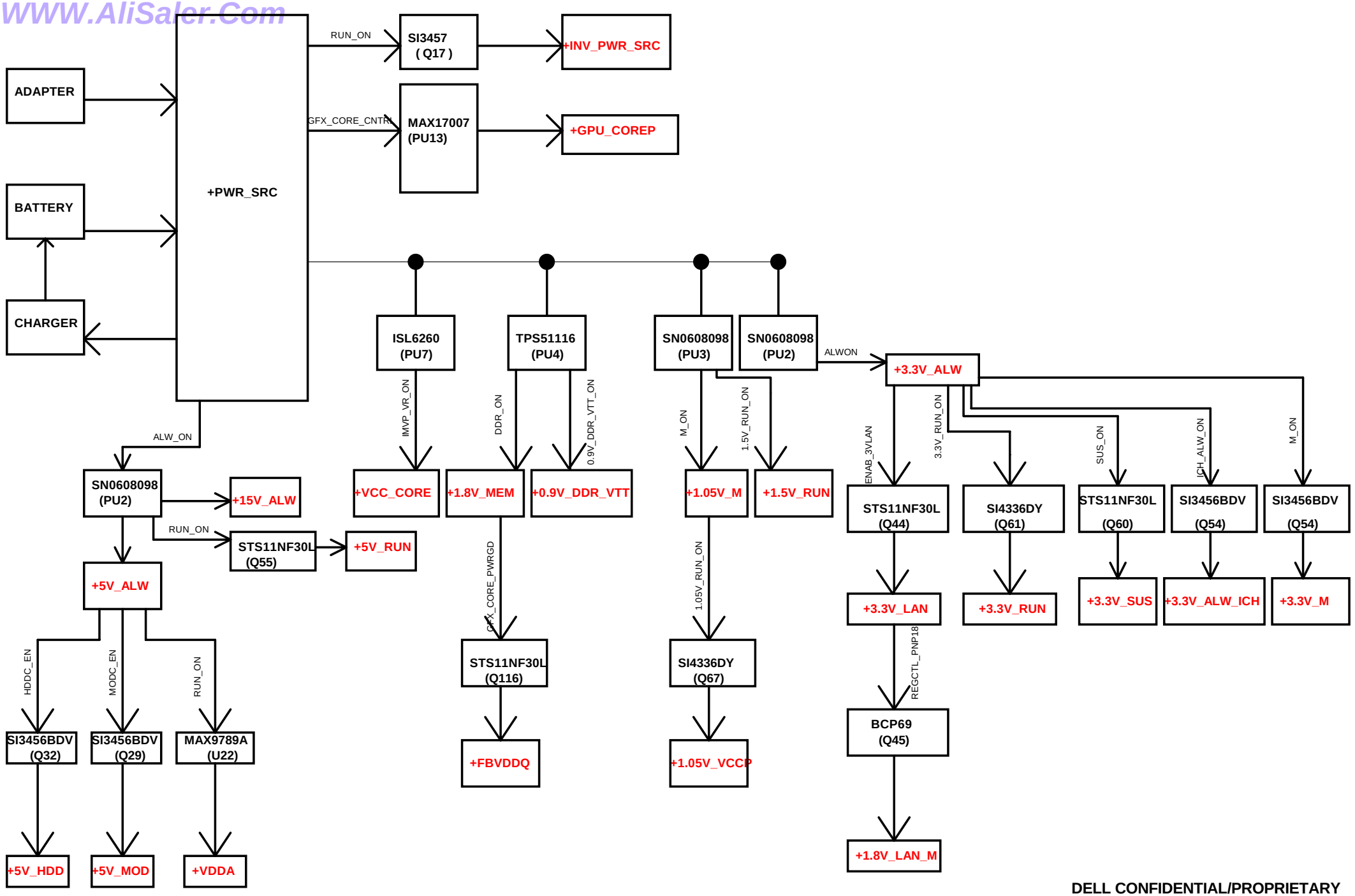

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Title: Power Rail

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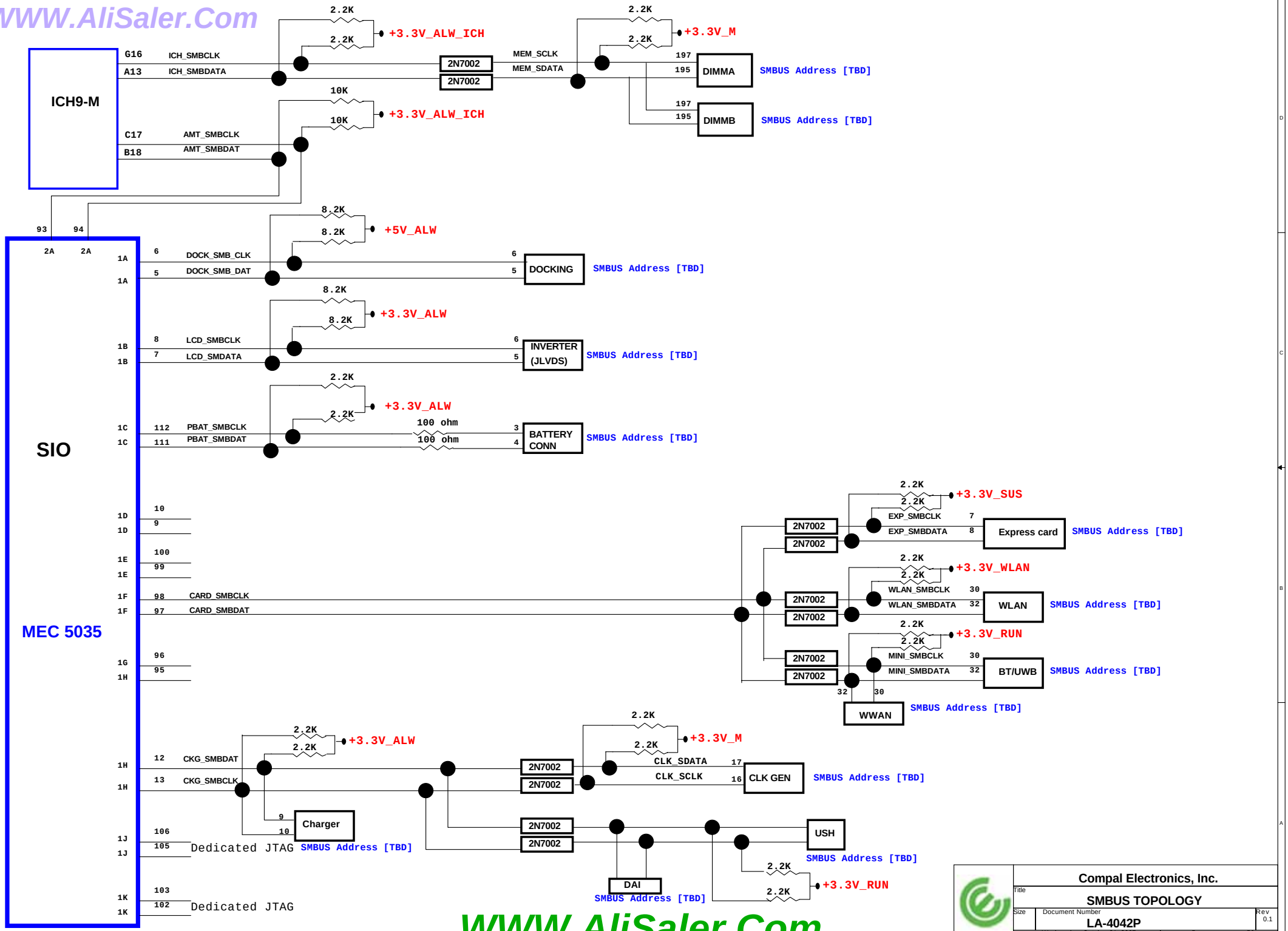

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Title: SMBUS TOPOLOGY

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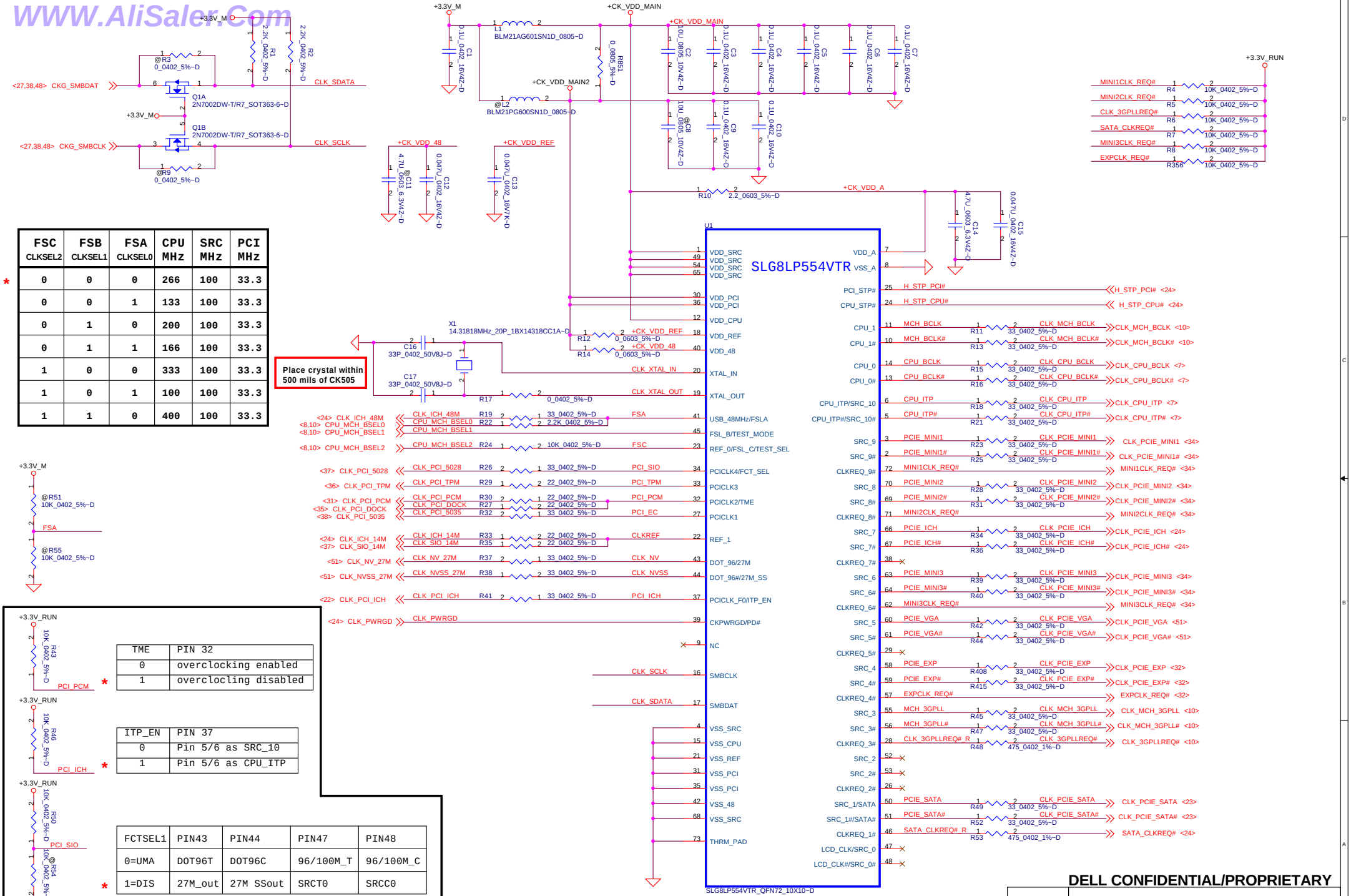

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3

TME	PIN 32
0	overclocking enabled
1	overclocling disabled

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
1	Pin 5/6 as CPU_ITP

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1=DIS	27M_out	27M SSout	SRCT0	SRCC0

0=UMA
1=Disc. GRFX down

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Title: Clock Generator

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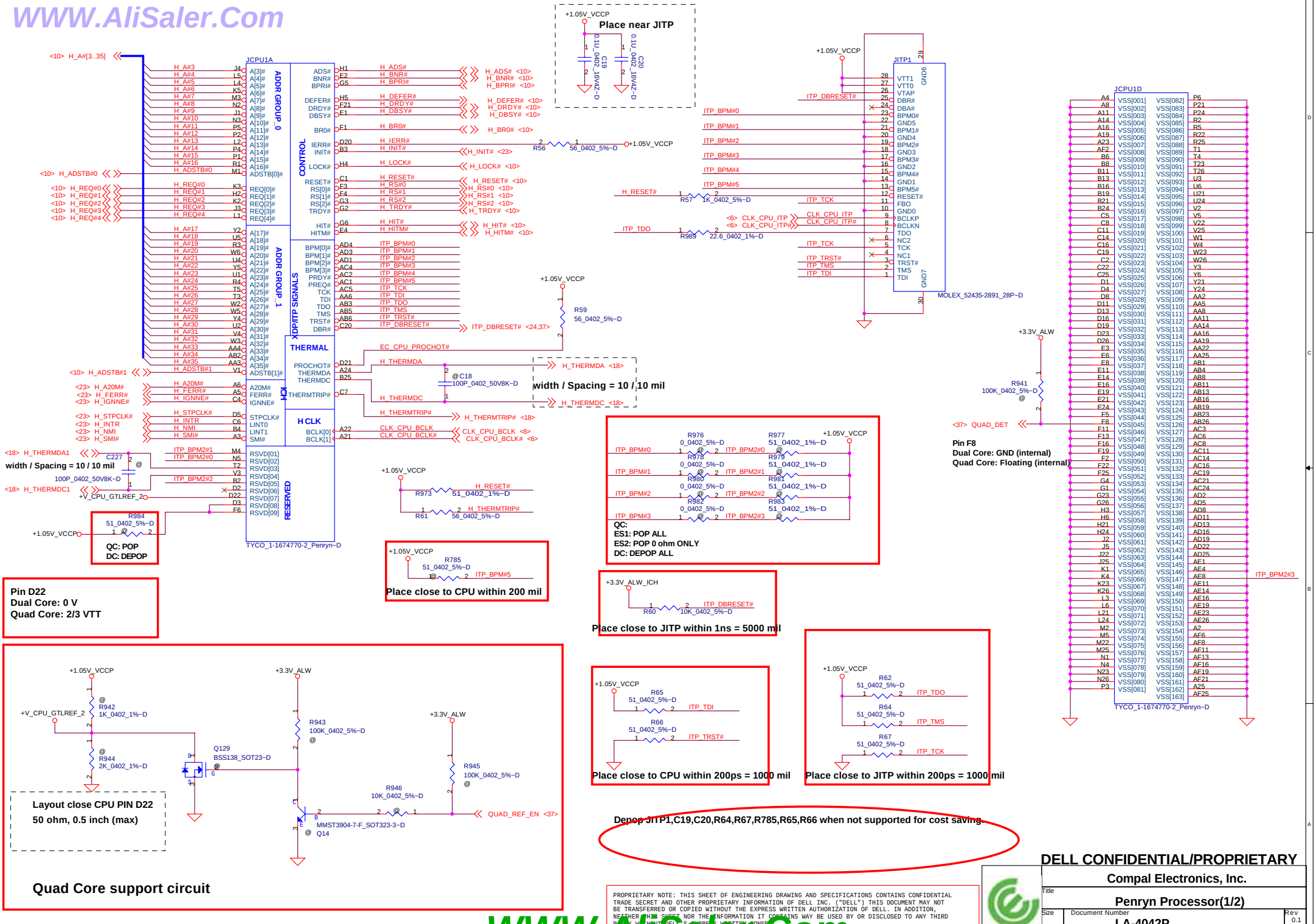

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Title: Penryn Processor(1/2)

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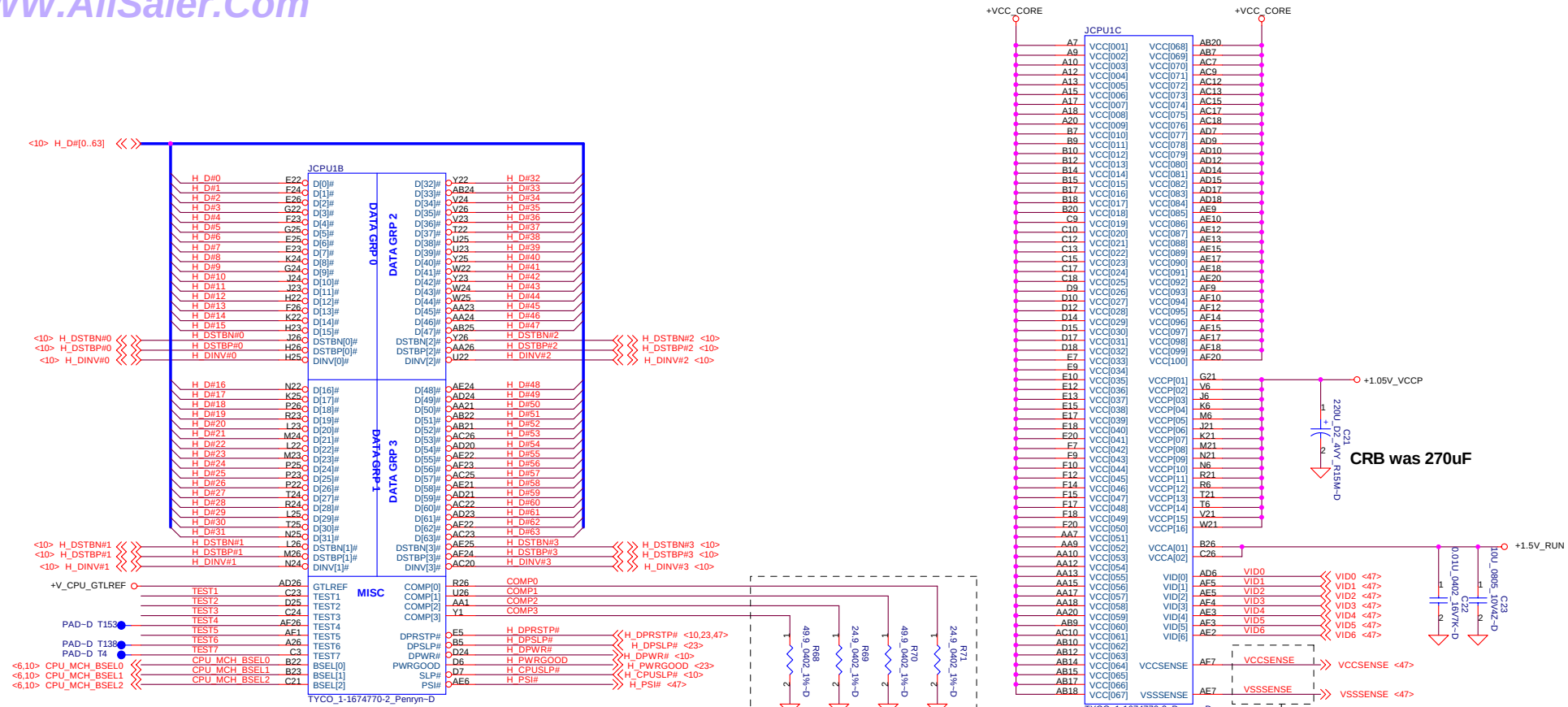
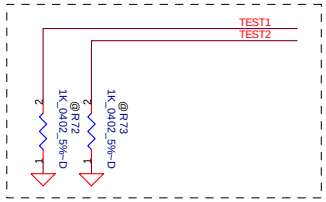
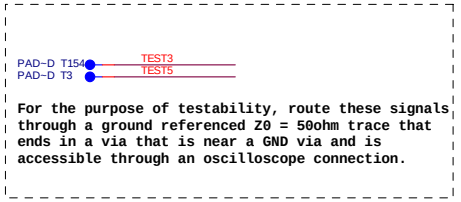


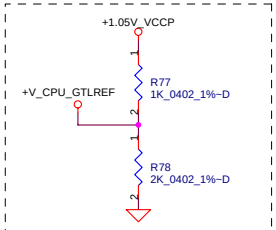
Dual Core Should follow Quad Core value
Avia should support Quad / Dual Core CPU





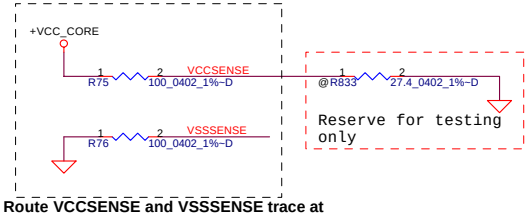
For the purpose of testability, route these signals through a ground referenced Z0 = 50ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



Layout close CPU PIN AD26
50 ohm, 0.5 inch (max)

Place R75 and R76 near CPU



Route VCCSENSE and VSSSENSE trace at
27.4 ohms, 7 mils spacing and the placement should be within 1 inch (max)

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Title	Penryn Processor(2/2)
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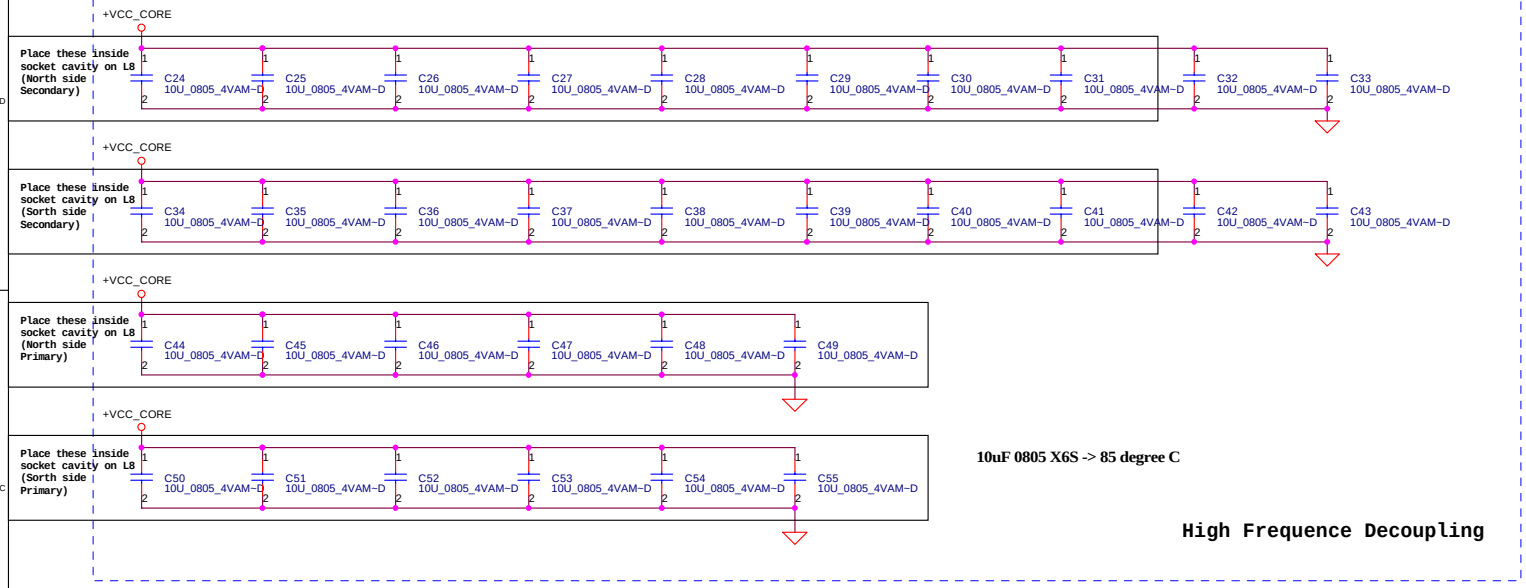
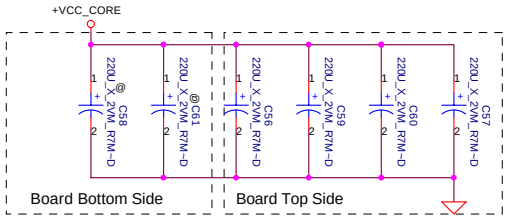


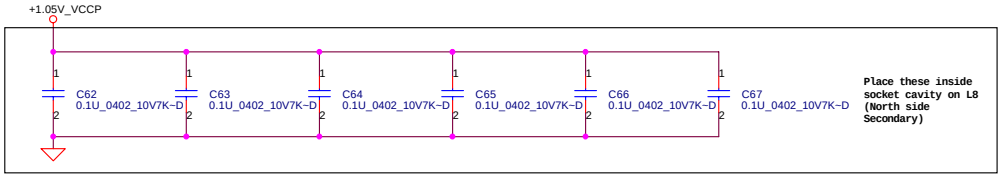
10uF 0805 X6S -> 85 degree C

High Frequence Decoupling

Near VCORE regulator.



ESR <= 1.5m ohm
Capacitor > 1320uF



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Title: CPU Bypass

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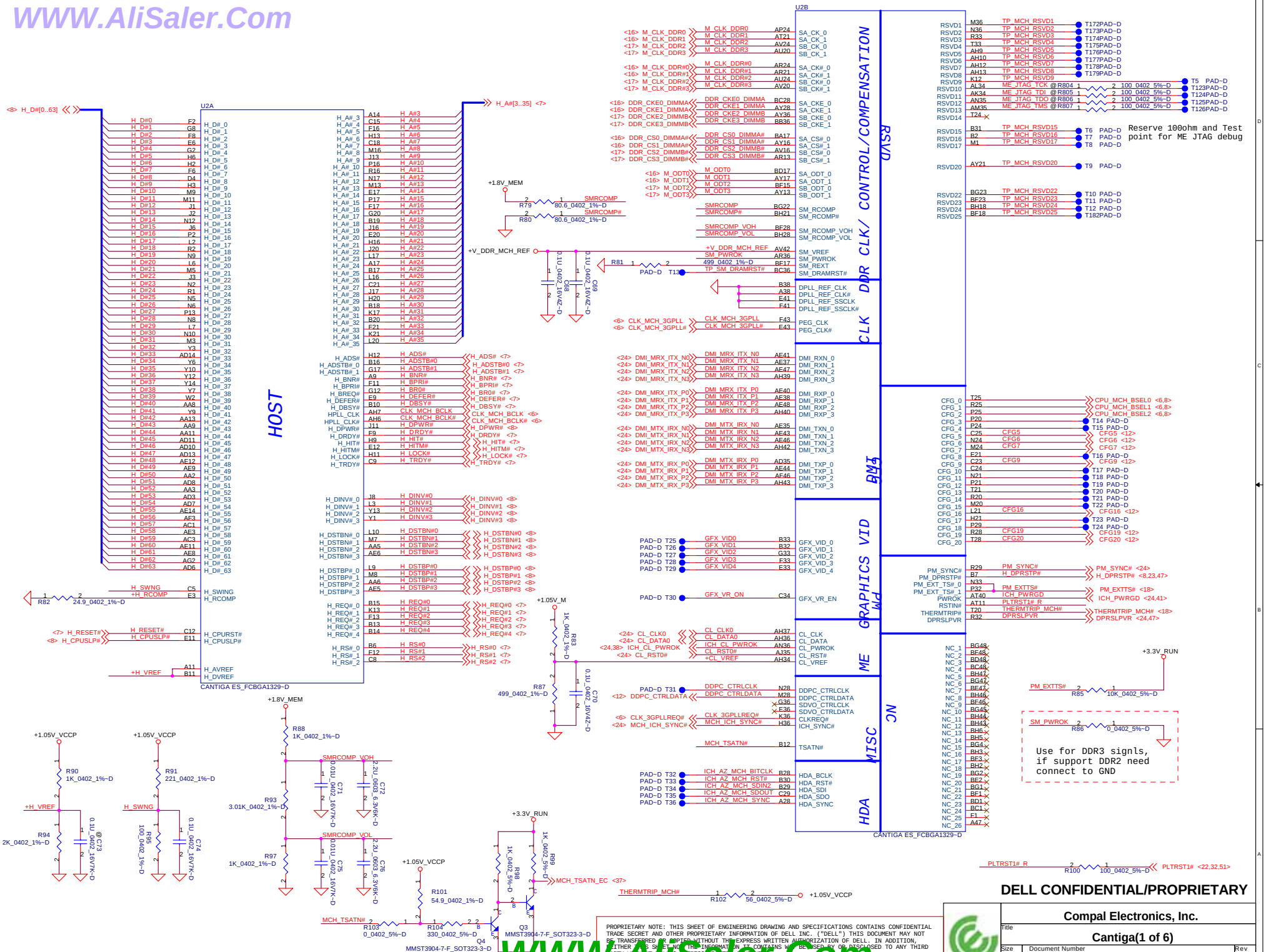

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Title: Cantiga(1 of 6)

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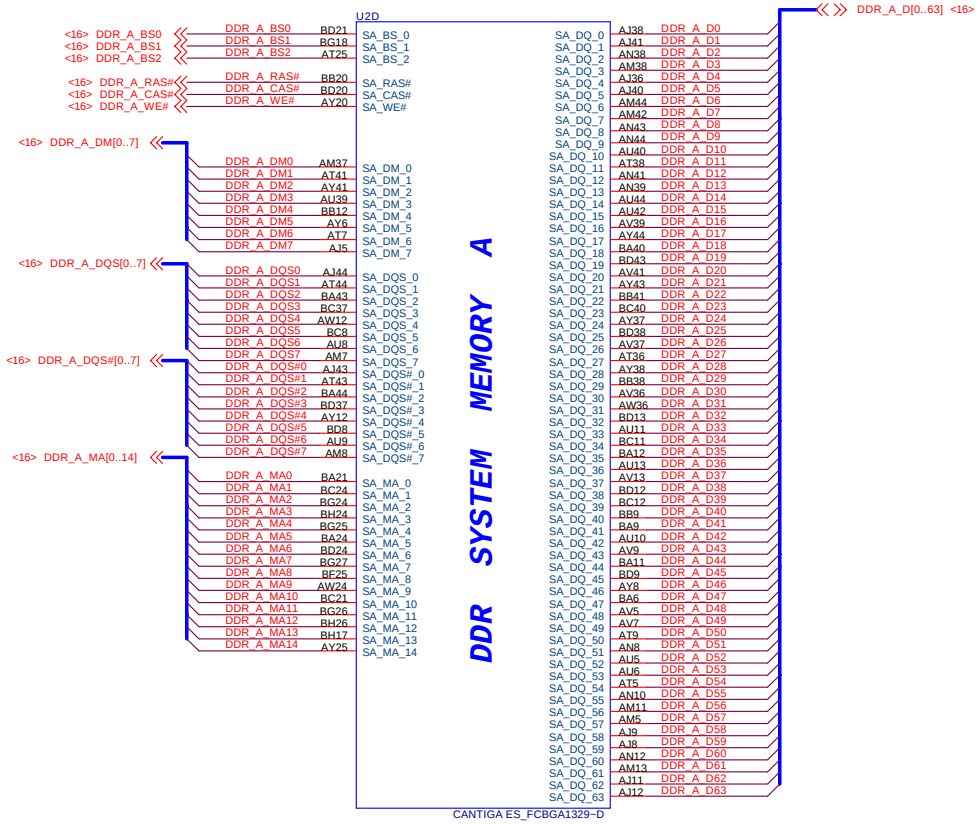

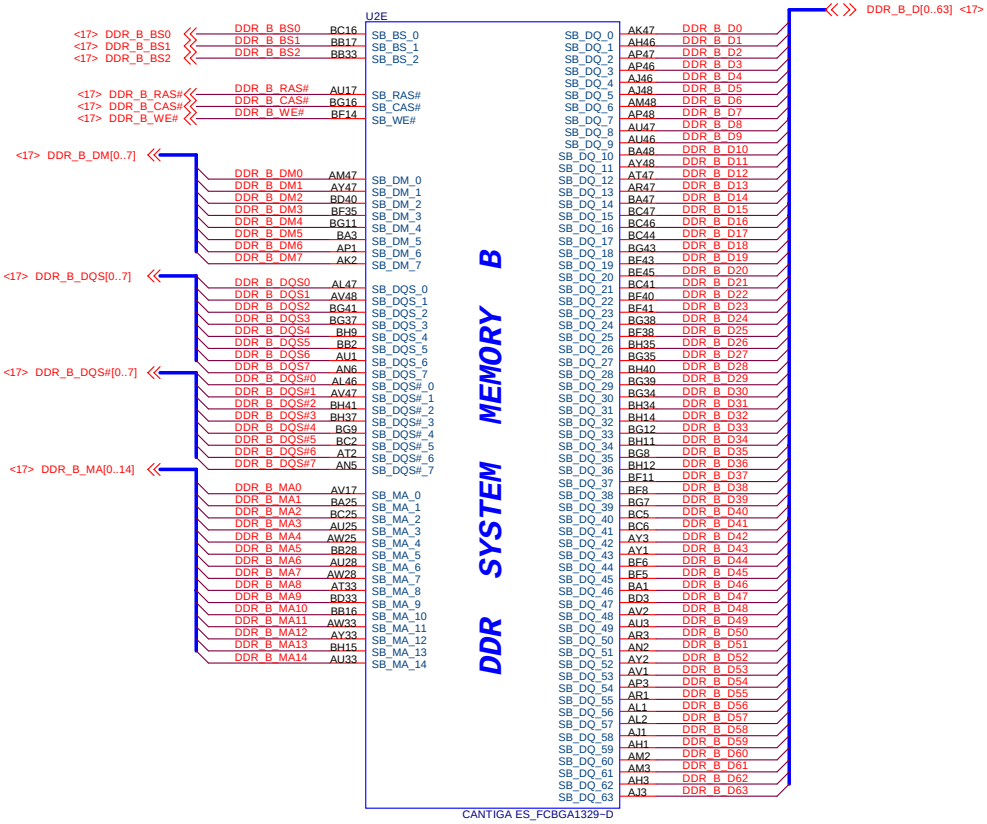

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Title	Cantiga(2 of 6)
Size	Document Number: LA-4042P
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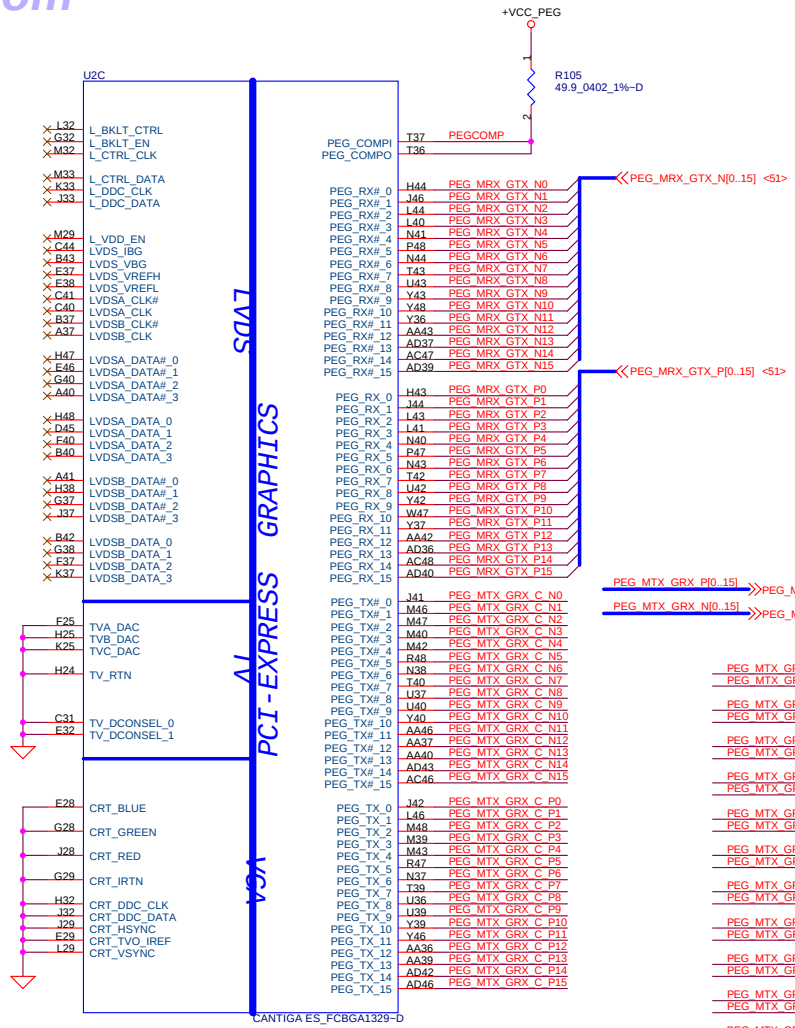

Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Defult)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	Digital Display Port Concurrent Operation	Low=Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port
SDVO_CRTL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present

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Title: Cantiga(3 of 6)

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CRB 270uF

+1.05V_VCCP

U2H

VTT
VTT_1 VTT_2 VTT_3 VTT_4 VTT_5 VTT_6 VTT_7 VTT_8 VTT_9 VTT_10 VTT_11 VTT_12 VTT_13 VTT_14 VTT_15 VTT_16 VTT_17 VTT_18 VTT_19 VTT_20 VTT_21 VTT_22 VTT_23 VTT_24 VTT_25

C109 220U_D2_4VY_R15M-D
C110 0.47U_0402_10V4Z-D
C114 4.7U_0603_6.3V6M-D
C115 4.7U_0603_6.3V6M-D
C116 2.2U_0603_10V7K-D

CRT
VCCA_CRT_DAC_1 B27
VCCA_CRT_DAC_2 A26
VCCA_DAC_BG A25
VSSA_DAC_BG B25

PLL
VCCA_DPLLA F47
VCCA_DPLLB L48
VCCA_HPLL AD1 +1.05V_M_HPLL
VCCA_MPLL AE1 +1.05V_M_MPLL

LVDS
VCCA_LVDS J48
VSSA_LVDS J47

A PEG
VCCA_PEG_BG AD48 +VCCA_PEG_BG
VCCA_PEG_PLL AA48 +1.05V_M_PEGPLL

R778 0_0402_5%-D +1.5V_RUN
@R779 0_0402_5%-D +3.3V_RUN

C117 0.1U_0402_16V4Z-D

A SM
VCCA_SM_1 AB20
VCCA_SM_2 AP20
VCCA_SM_3 AN20
VCCA_SM_4 AR17
VCCA_SM_5 AP17
VCCA_SM_6 AN17
VCCA_SM_7 AT16
VCCA_SM_8 AR16
VCCA_SM_9 AP16

+1.05V_M_A_SM
R116 0_0805_5%-D
C121 1U_0603_10V4Z-D
C122 4.7U_0603_6.3V6M-D
C123 22U_0805_6.3V6M-D
@C124 22U_0805_6.3V6M-D
C120 100U_D2E_6.3VM_R15M-D

A CK
VCCA_SM_CK_1 AP28
VCCA_SM_CK_2 AN28
VCCA_SM_CK_3 AP25
VCCA_SM_CK_4 AN25
VCCA_SM_CK_5 AN24
VCCA_SM_CK_NCTF_1 AM28
VCCA_SM_CK_NCTF_2 AM26
VCCA_SM_CK_NCTF_3 AM25
VCCA_SM_CK_NCTF_4 AL25
VCCA_SM_CK_NCTF_5 AM24
VCCA_SM_CK_NCTF_6 AL24
VCCA_SM_CK_NCTF_7 AM23
VCCA_SM_CK_NCTF_8 AL23

+1.05V_M_SM_CK
R119 0_1210_5%-D
C127 0.1U_0402_16V4Z-D
C128 22U_0805_6.3V6M-D
@C129 2.2U_0603_6.3V6K-D

D TV/CRT
TV
VCCA_TV_DAC_1 B24
VCCA_TV_DAC_2 A24

HDA
VCC_HDA A32
+1.5V_RUN
C998 0.1U_0402_16V4Z-D

VCCD_TVDAC M25
VCCD_QDAC L28
VCCD_HPLL AF1
VCCD_PEG_PLL AA47

LVDS
VCCD_LVDS_1 M38
VCCD_LVDS_2 L37

+1.05V_M_PEGPLL
C141 0.1U_0402_16V4Z-D
C140 0.1U_0402_16V4Z-D
C139 0.1U_0402_16V4Z-D
C138 0.01U_0402_25V7K-D

AXF
VCC_AXF_1 B22
VCC_AXF_2 B21
VCC_AXF_3 A21

+1.05V_M
R118 0_1210_5%-D
+VCC_AXF
10U_0805_4VAM-D
@C125
1U_0603_10V4Z-D
C126

SM CK
+1.8V_SM_CK
VCC_SM_CK_1 BF21
VCC_SM_CK_2 BH20
VCC_SM_CK_3 BG20
VCC_SM_CK_4 BF20

HV
VCC_TX_LVDS K47
VCC_HV_1 C35
VCC_HV_2 B35
VCC_HV_3 A35

+3.3V_RUN
C136 0.1U_0402_16V4Z-D

PEG
+VCC_PEG
VCC_PEG_1 V48
VCC_PEG_2 U48
VCC_PEG_3 V47
VCC_PEG_4 U47
VCC_PEG_5 U46

DMI
+VCC_DMI
C137 0.1U_0402_16V4Z-D
VCC_DMI_1 AH48
VCC_DMI_2 AE48
VCC_DMI_3 AH47
VCC_DMI_4 AG47

VTTLF
GMCH_VTTLF1 A8
GMCH_VTTLF2 L1
GMCH_VTTLF3 AB2
VTTLF1
VTTLF2
VTTLF3
C142 0.47U_0402_10V4Z-D
C143 0.47U_0402_10V4Z-D
C144 0.47U_0402_10V4Z-D

CANTIGA ES_FCBGA1329-D

+VCC_PEG
220U_D2_4VY_R15M-D C111
4.7U_0603_6.3V6M-D C112
22U_0805_6.3V6M-D C113
R114 0_1210_5%-D +1.05V_M
@R115 0_1210_5%-D +1.05V_VCCP

Follow ERB,CRB option
to select +1.05V_M or
+1.05V_VCCP

+1.05V_M
L3 BLM21PG221SN1D_0805-D +1.05V_M_PEGPLL
C118 10U_0805_4VAM-D
R117 1_0402_5%-D
C119 0.1U_0402_16V4Z-D

+1.05V_M_HPLL
24mA Max.
L4 BLM18AG121SN1D_0603-D +1.05V_M
0.1U_0402_16V4Z-D C130
4.7U_0603_6.3V6M-D C131

+1.05V_M_MPLL
139.2mA Max.
L5 LQH32CNR15M33L_1210-D +1.05V_M
0.1U_0402_16V4Z-D C132
R120 0_0603_5%-D
C133 22U_0805_6.3VAM-D

+VCC_DMI
PJP21 PAD-OPEN1x1m +VCC_PEG
@L6 LBC2518T91NM_1210-D +1.05V_M
@C145 220U_D2_4VY_R15M-D

+1.8V_MEM
L7 LQM21FN1R0N00_0805-D
Rdc=0.1~0.2,rated current=220mA(MAX)
C147 10U_0805_4VAM-D
R121 1_0603_5%-D
+1.8V_SM_CK
C146 0.1U_0402_16V4Z-D

+1.05V_VCCP
D1 RB751V_SOD323-2-D
+1.05V_VCCP/+3.3V_RUN
R122 10_0603_5%-D
+3.3V_RUN

Follow CRB to
VCC_HV(C35,B35,A35)

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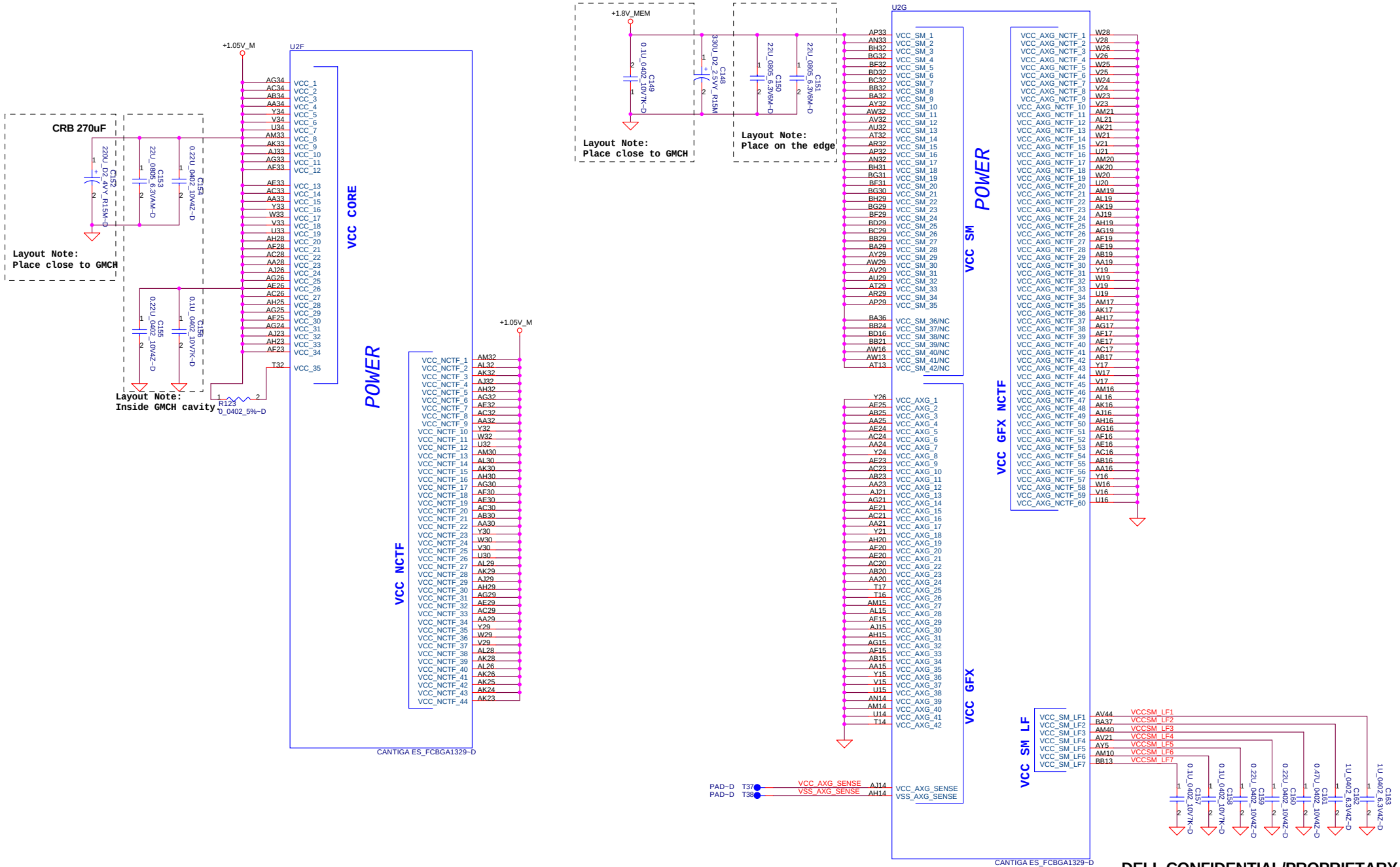
Title: Cantiga(4 of 6)

Size: Document Number: LA-4042P Rev: 0.1

Date: Wednesday, October 31, 2007 Sheet 13 of 56

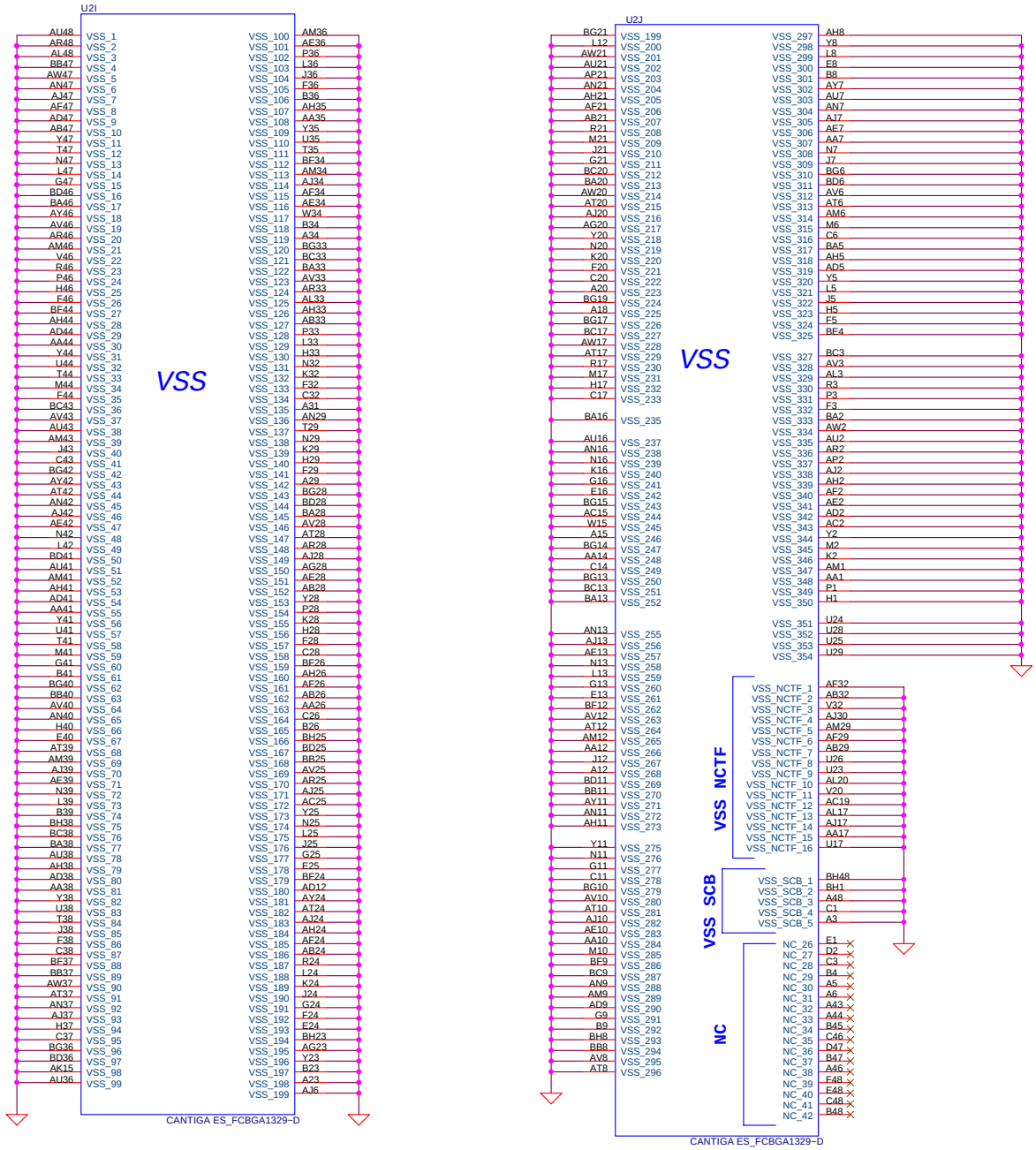


Compal Electronics, Inc.

Title: Cantiga(5 of 6)

Size: | Document Number: LA-4042P | Rev: 0.1

Date: Wednesday, October 31, 2007 | Sheet 14 of 56



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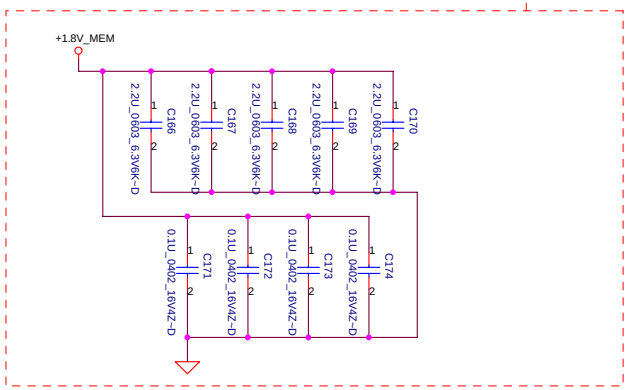
Title: Cantiga(6 of 6)

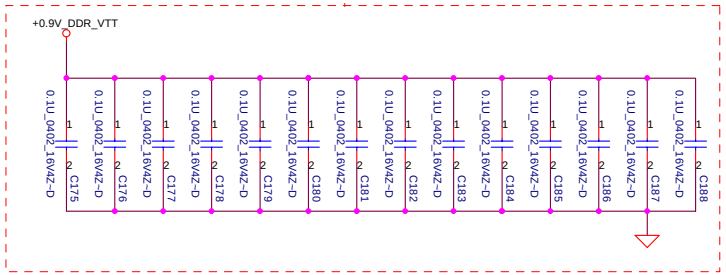
Size: | Document Number: LA-4042P | Rev: 0.1

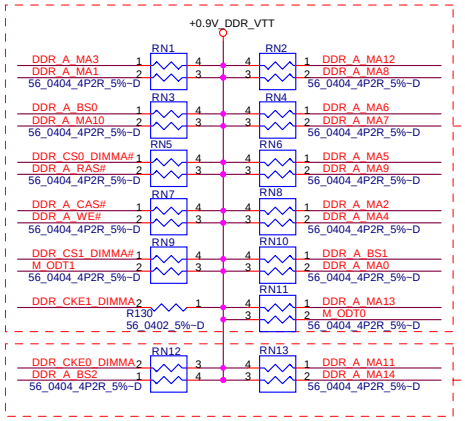
Date: Wednesday, October 31, 2007 | Sheet 15 of 56

Layout Note:
Place near JDIMMA



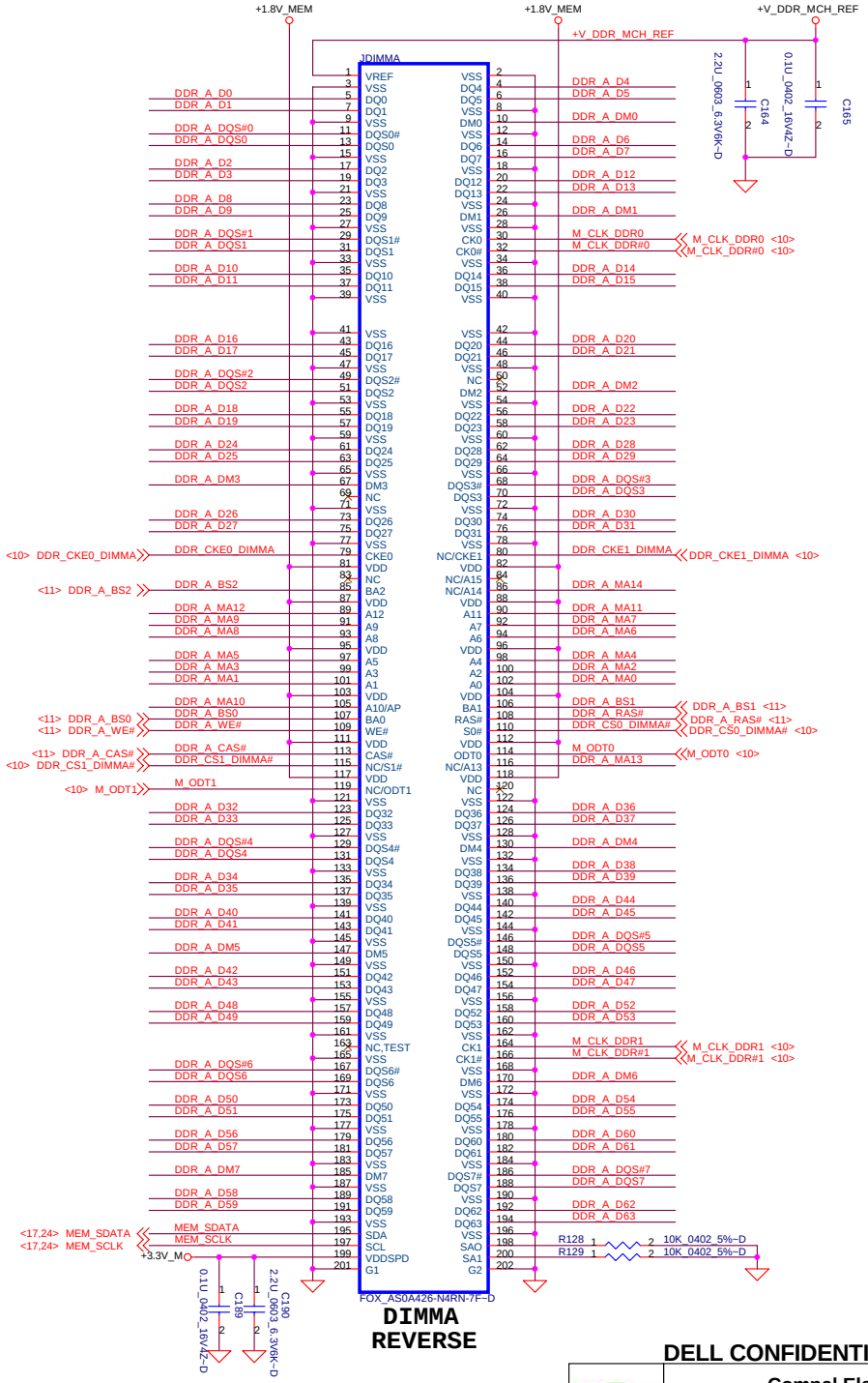
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





Layout Note:
Place these resistor closely JDIMMA,all trace length<750 mil

Layout Note:
Place these resistor closely JDIMMA,all trace length Max=1.3"



DIMMA REVERSE

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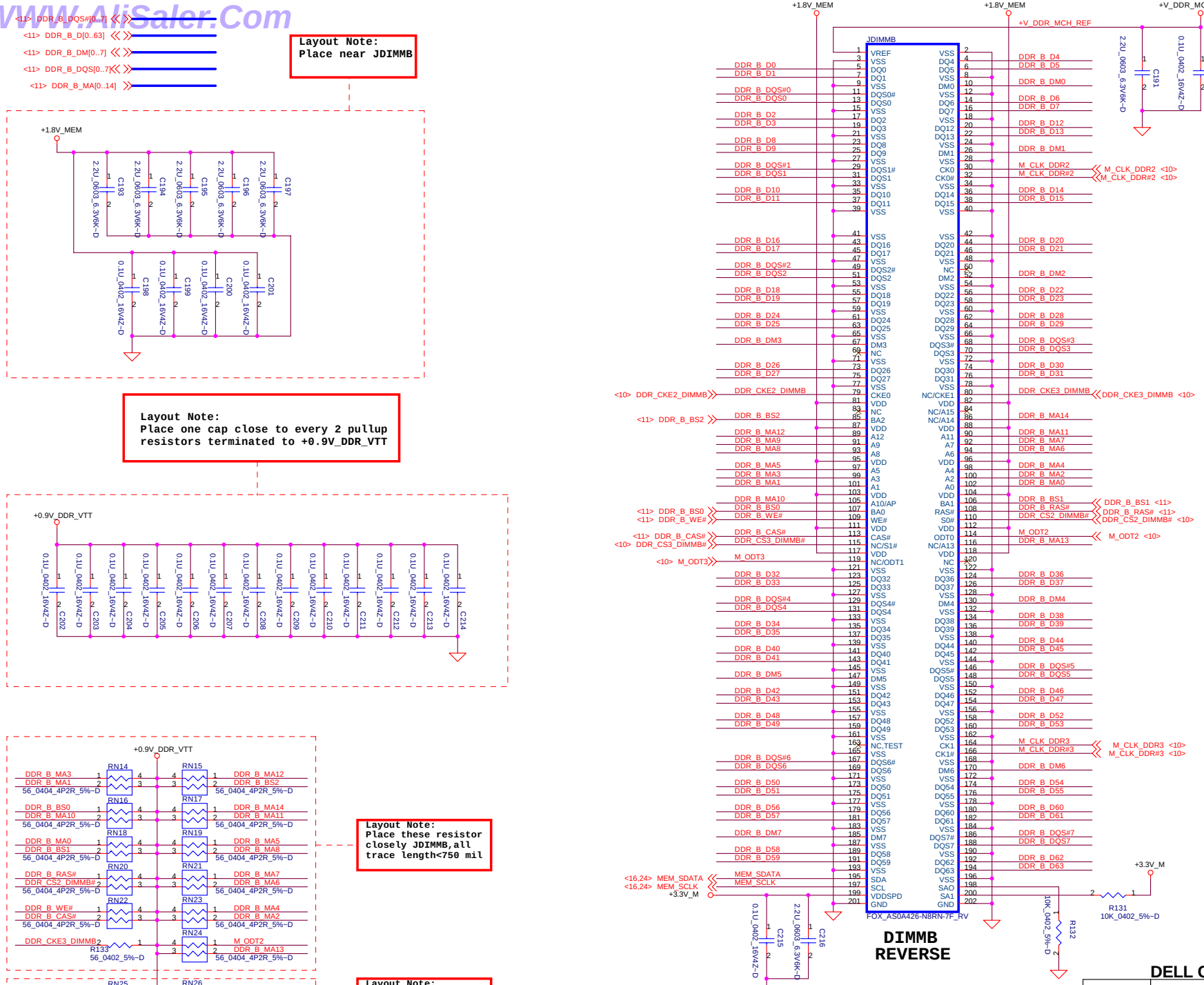
Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT1

Size: | Document Number: LA-4042P | Rev: 0.1

Date: Wednesday, October 31, 2007 | Sheet 16 of 56



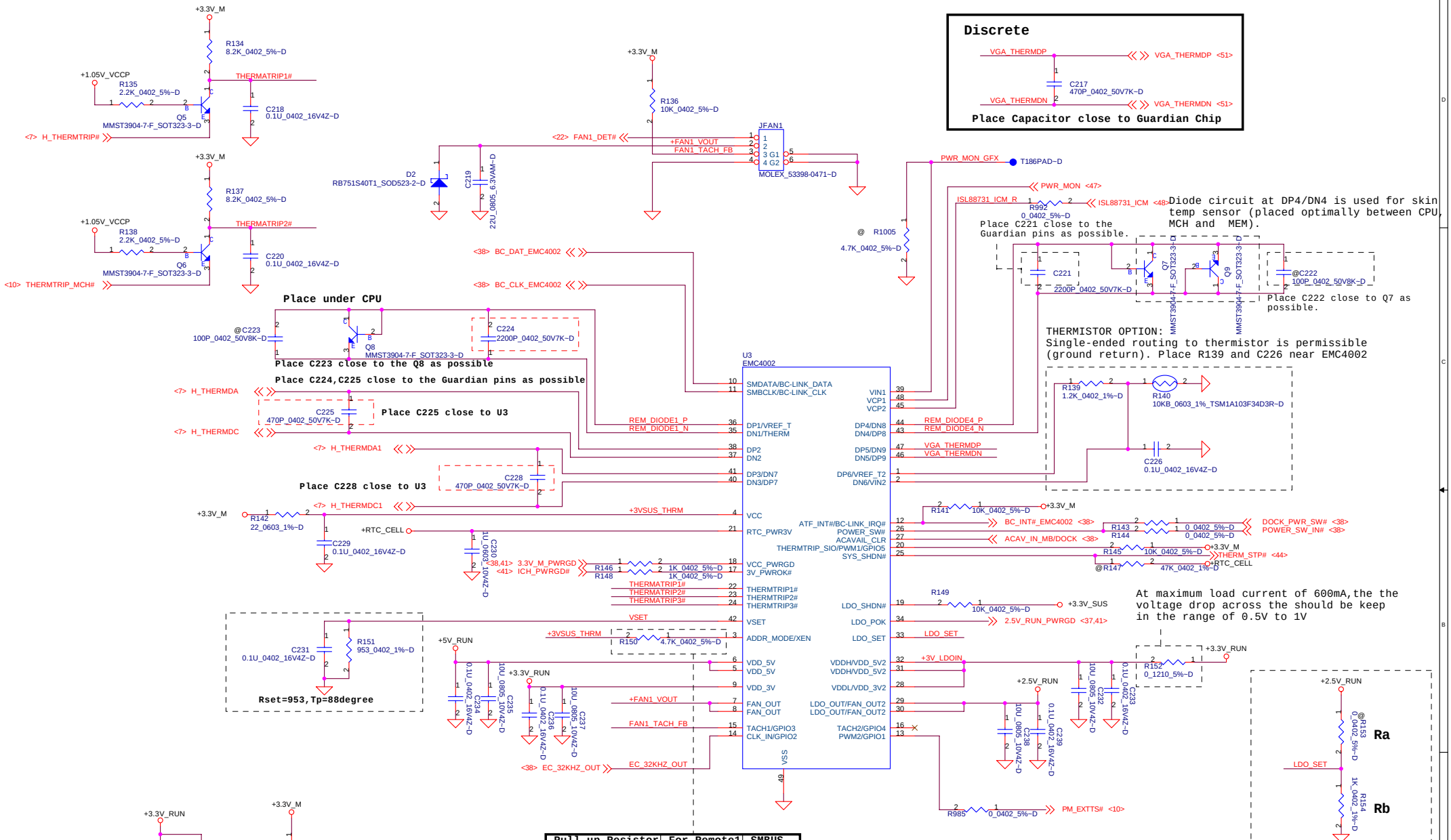
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT2

Size: | Document Number: LA-4042P | Rev: 0.1

Date: Wednesday, October 31, 2007 | Sheet 17 of 56



Pull-up Resistor on ADDR_MODE/XEN	For Remote1 mode	SMBUS Address
<= 4.7K +/- 5%	2N3904	2F(r/w)
10K	2N3904	2E(r/w)
18K	Thermistor	2F(r/w)
>= 33K	Thermistor	2E(r/w)

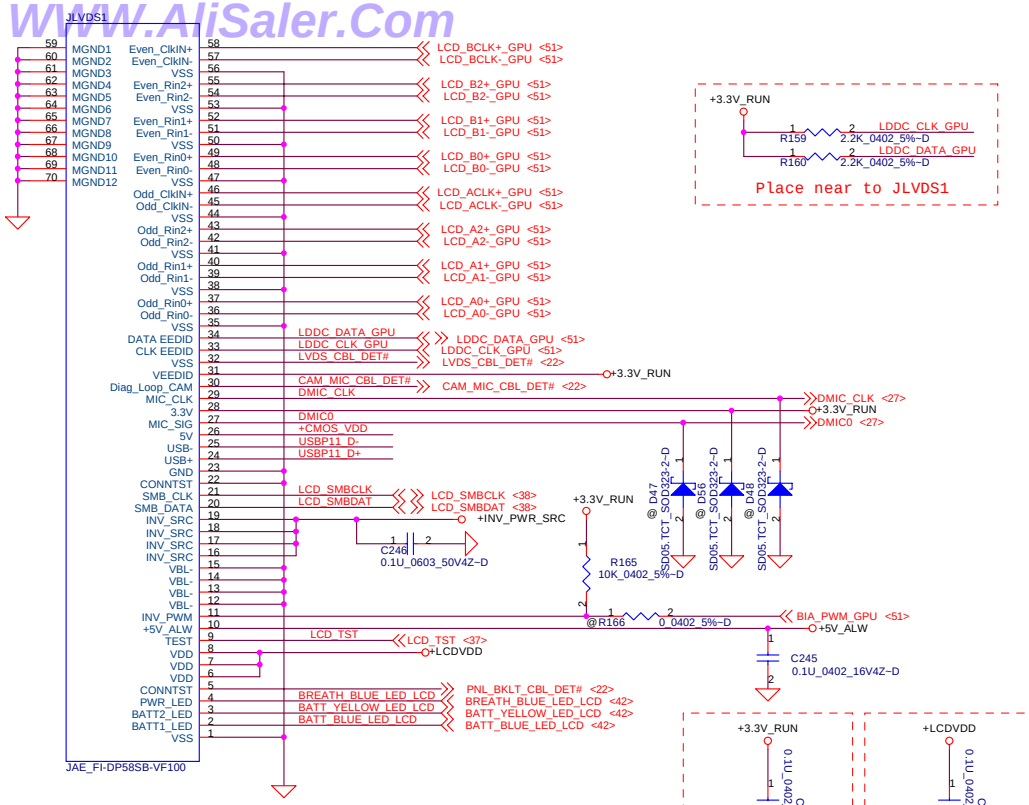
*

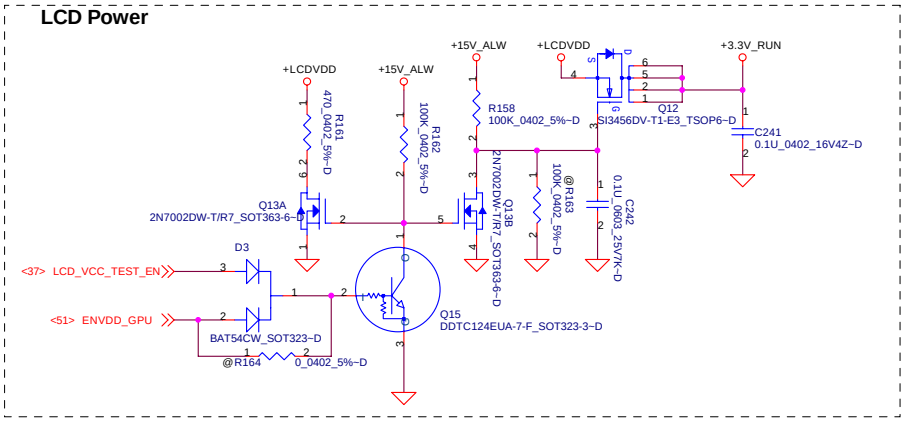
Compal Electronics, Inc.

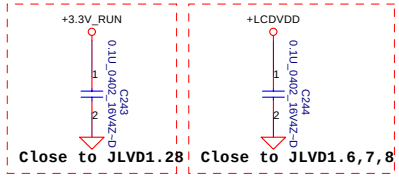
Title: FAN & Thermal Sensor

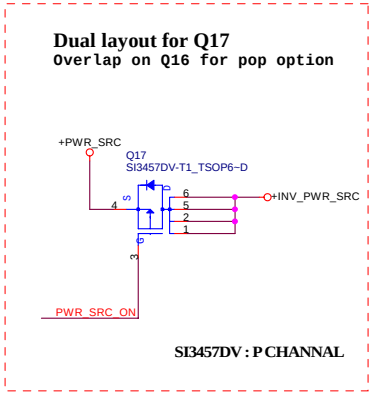
Size: | Document Number: LA-4042P | Rev: 0.1

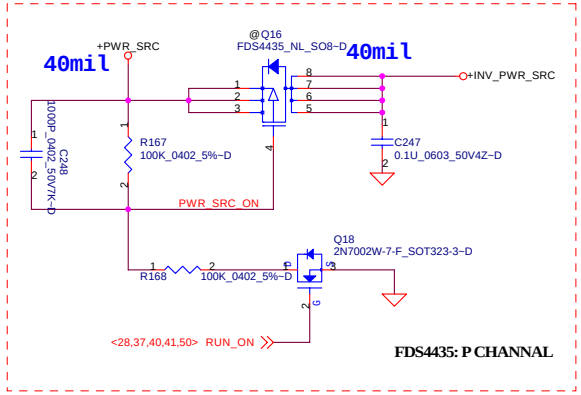
Date: Wednesday, October 31, 2007 | Sheet 18 of 56

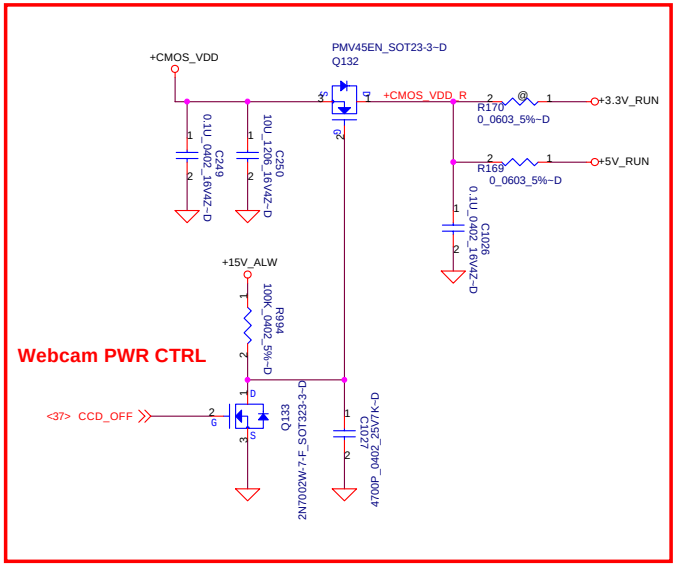


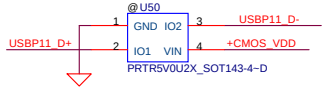


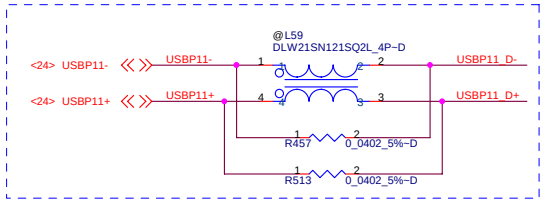












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Title	LVDS Conn
Size	Document Number: LA-4042P
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Date:	Wednesday, October 31, 2007
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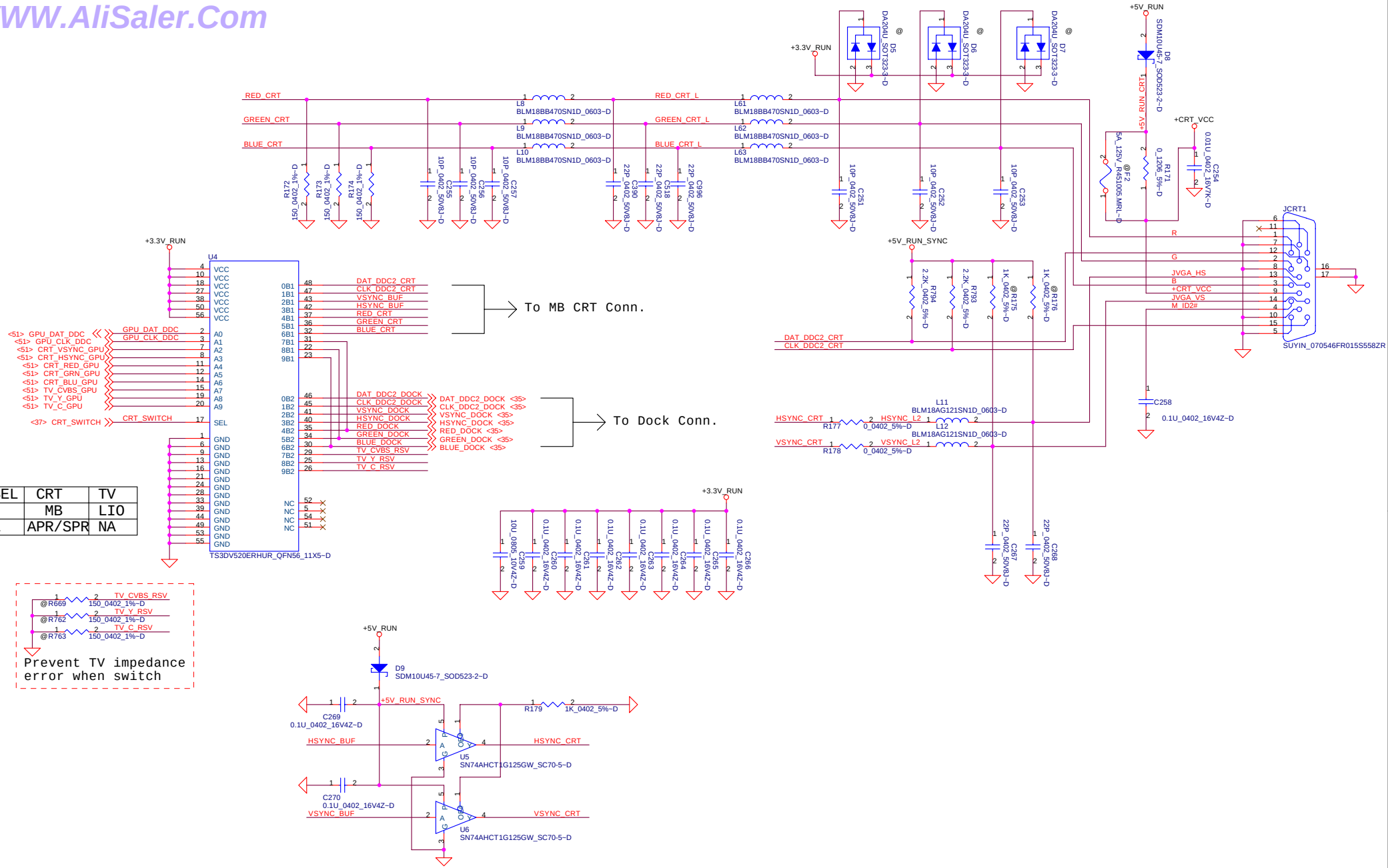


SEL	CRT	TV
0	MB	LIO
1	APR/SPR	NA

Compal Electronics, Inc.

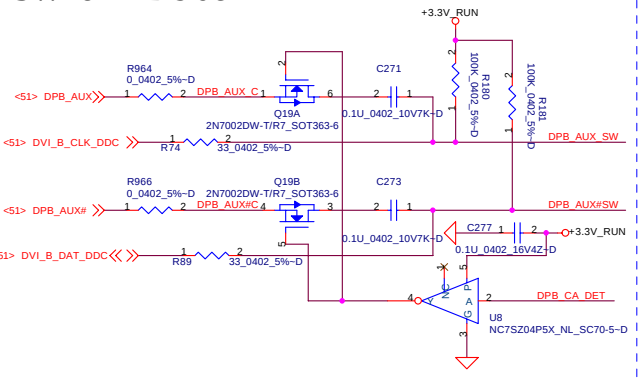
Title: CRT/Video switch

Size: | Document Number: LA-4042P | Rev: 0.1

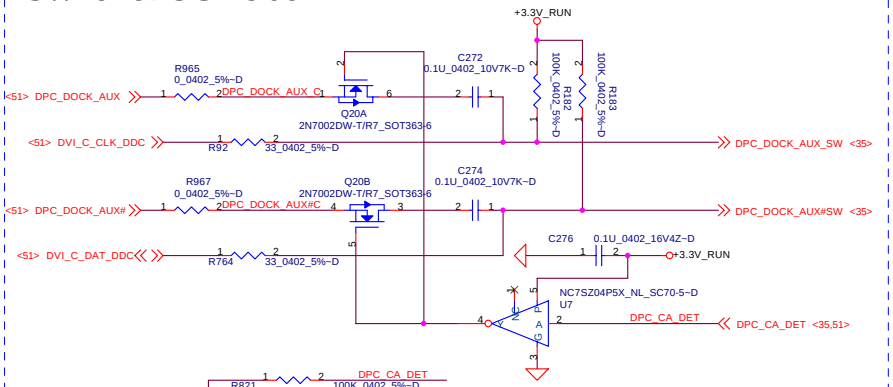
Date: Wednesday, October 31, 2007 | Sheet 20 of 56

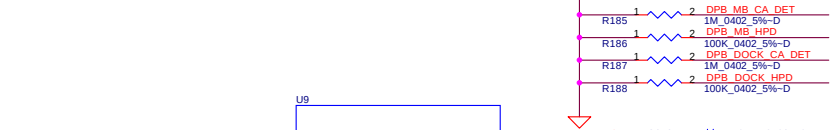
Display port Connector

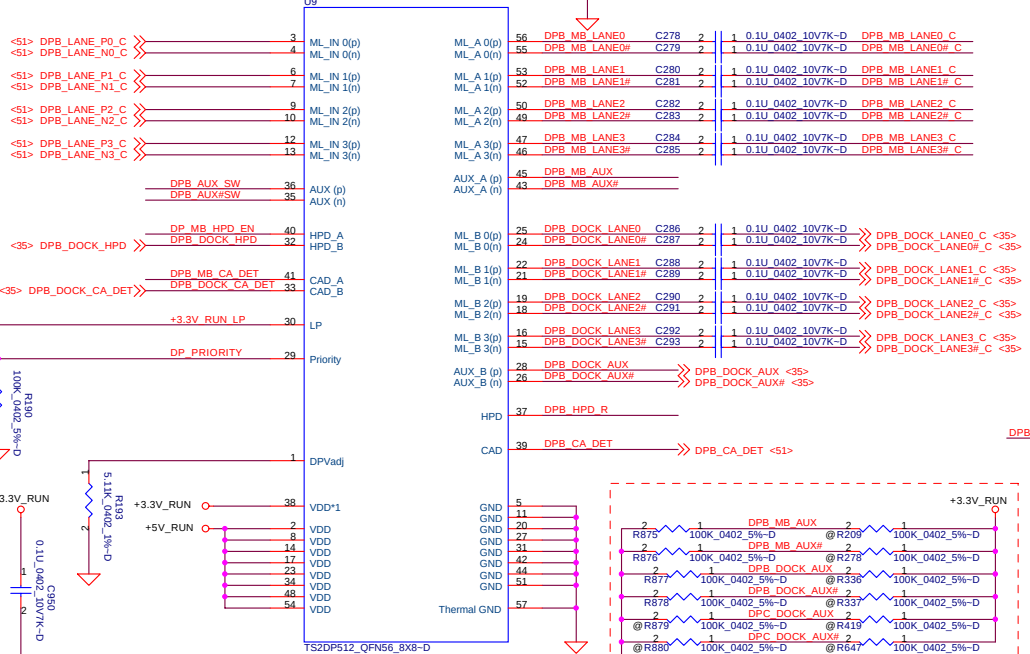
SW for MB side

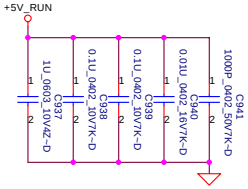


SW for eDOCK side

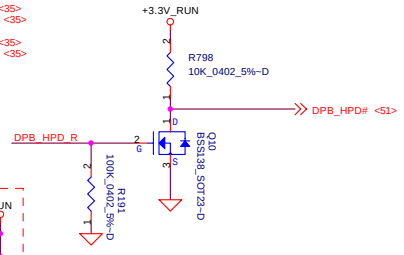


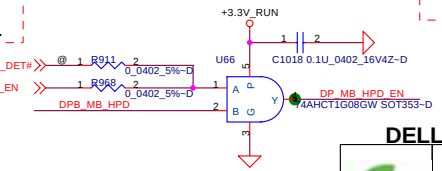


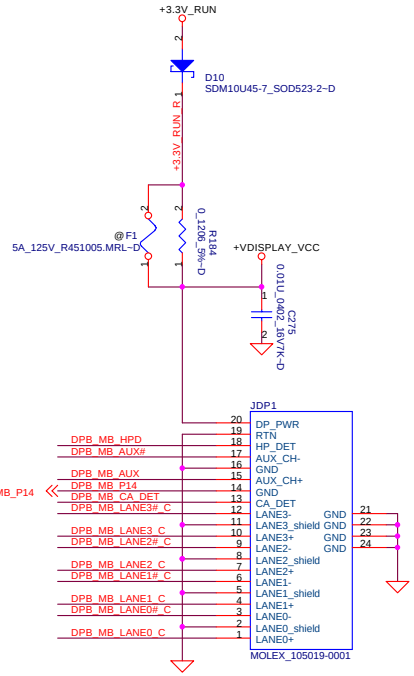


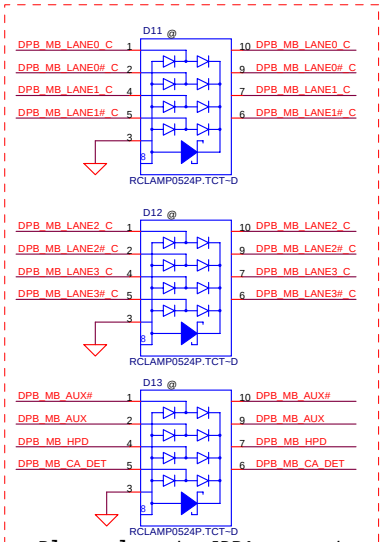


Pads for interoperability,
remove in X01 if not needed.









Place close to JDP1 connector

Pin30	Level	State	Description
LP	Hi	Normal Mode	Standard operational mode for device
	Low	Low power Mode	Device is forced into a low power mode causing the output s to go to a high-Z state, all other inputs are ignore

Compal Electronics, Inc.

Title: Display port

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A16 away override strap.	
PCI_GNT3#/(MDC_RST_DIS#)	Low = A16 swap override enabled. High = Default. pull up internal

*

Boot BIOS Strap		
PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

Compal Electronics, Inc.

Title: ICH9-M(1/4)

Size: | Document Number: LA-4042P | Rev: 0.1

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CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

Package
9.6X4.06 mm

ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Close to U55

XOR Chain Entrance Strap		
ICH RSVD_TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

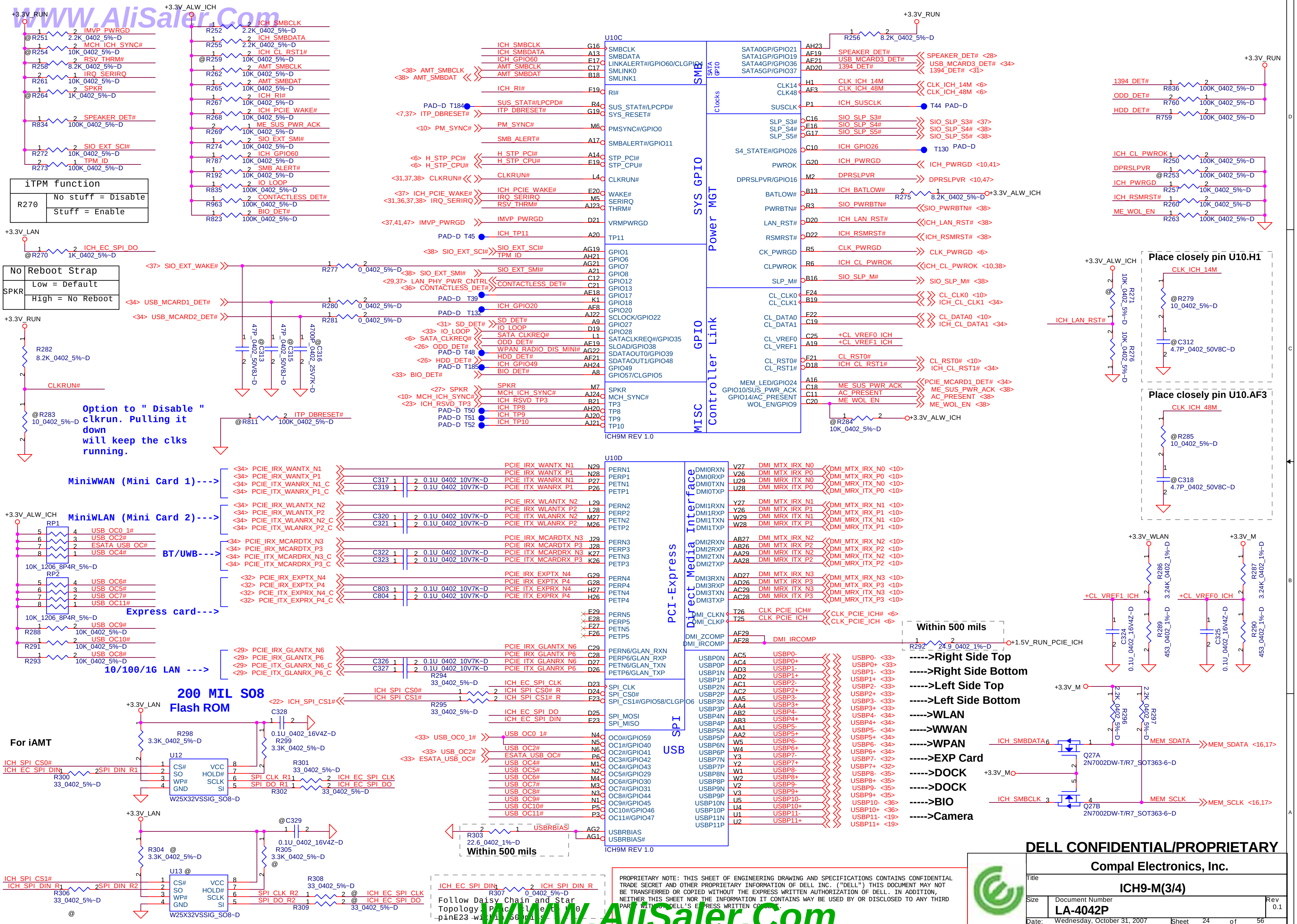
R375, R961, R960, R962 Q130 remove for RTC detect function

Compal Electronics, Inc.

Title: ICH9-M(2/4)

Size: | Document Number: LA-4042P | Rev: 0.1

Date: Wednesday, October 31, 2007 | Sheet 23 of 56



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Title	ICH9-M(3/4)
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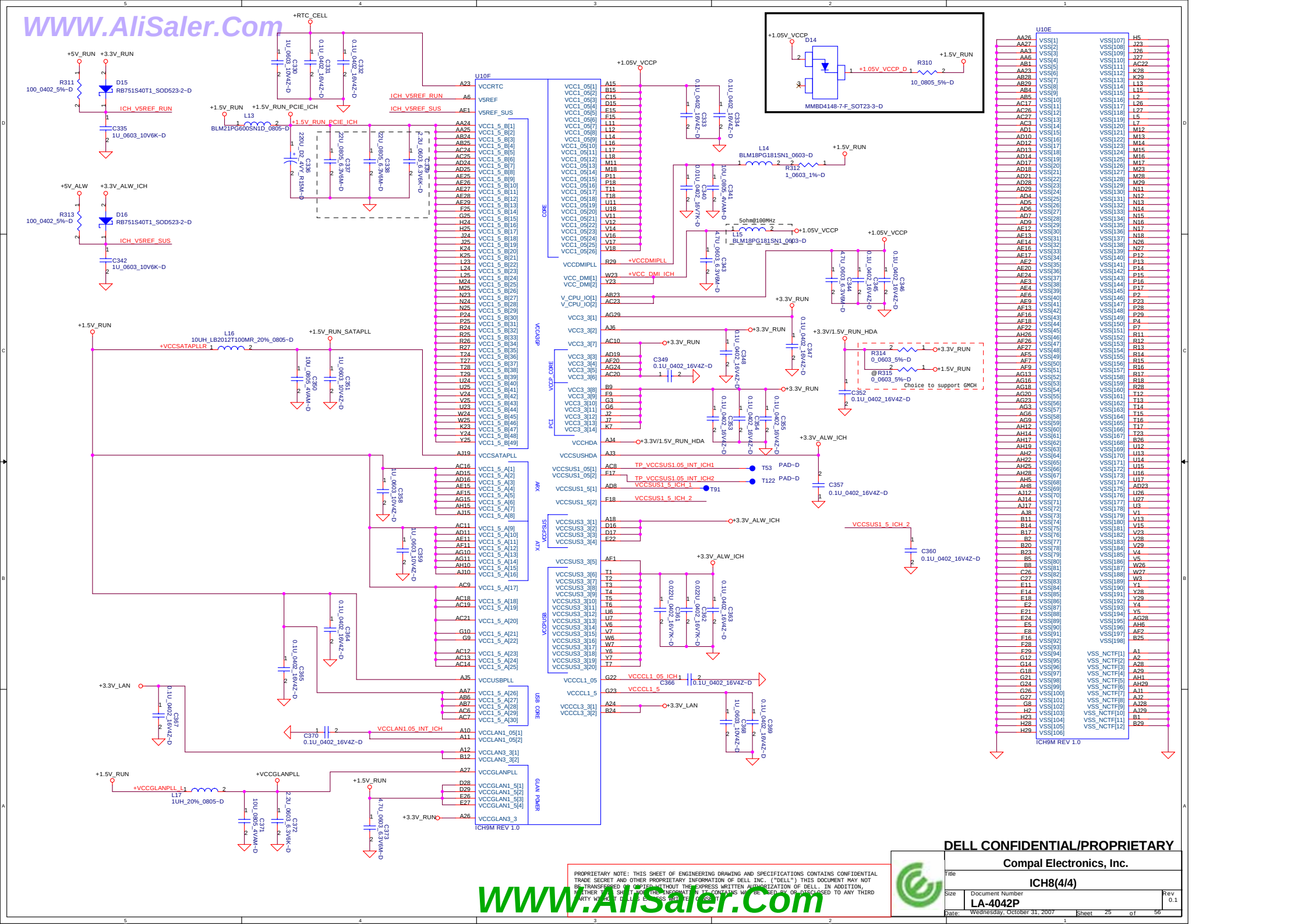


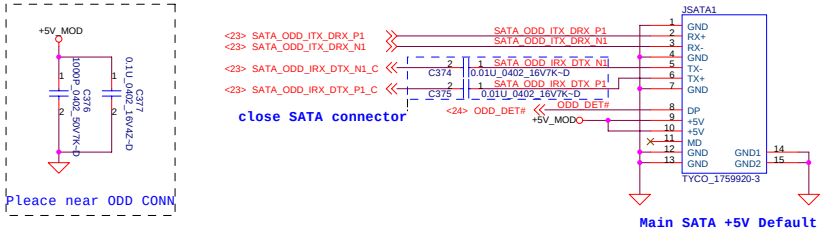
Compal Electronics, Inc.

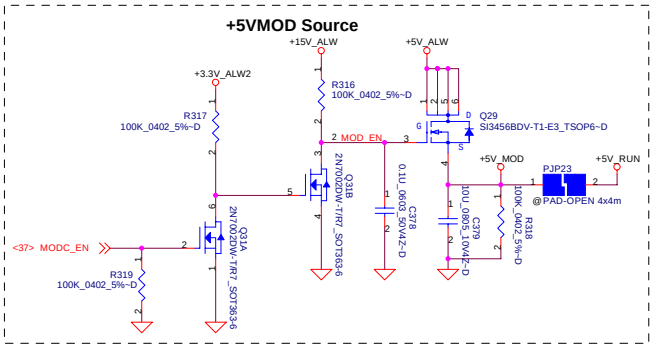
Title: ICH8(4/4)

Size: | Document Number: LA-4042P | Rev: 0.1

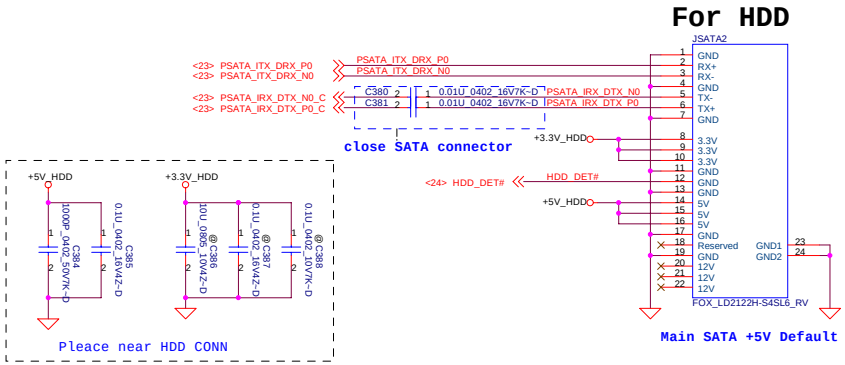
Date: Wednesday, October 31, 2007 | Sheet 25 of 56

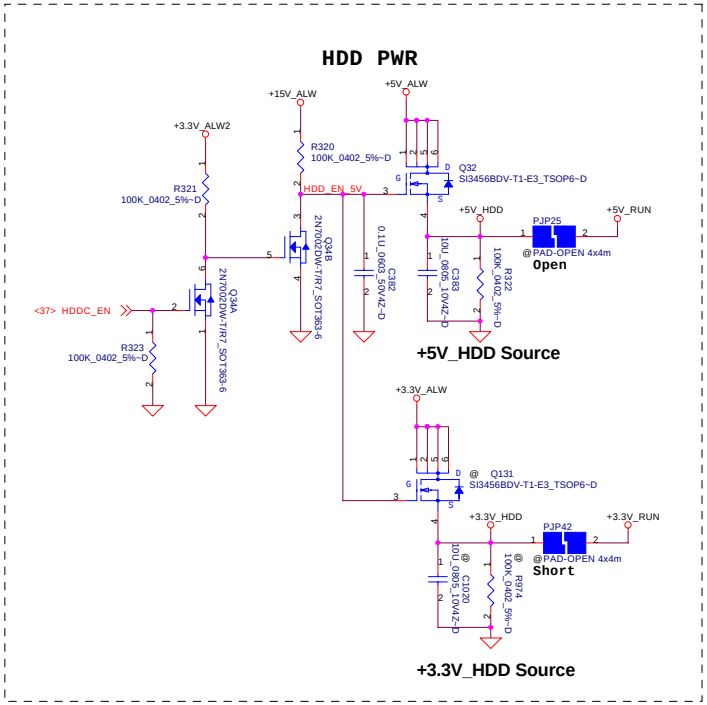
For ODD





For HDD





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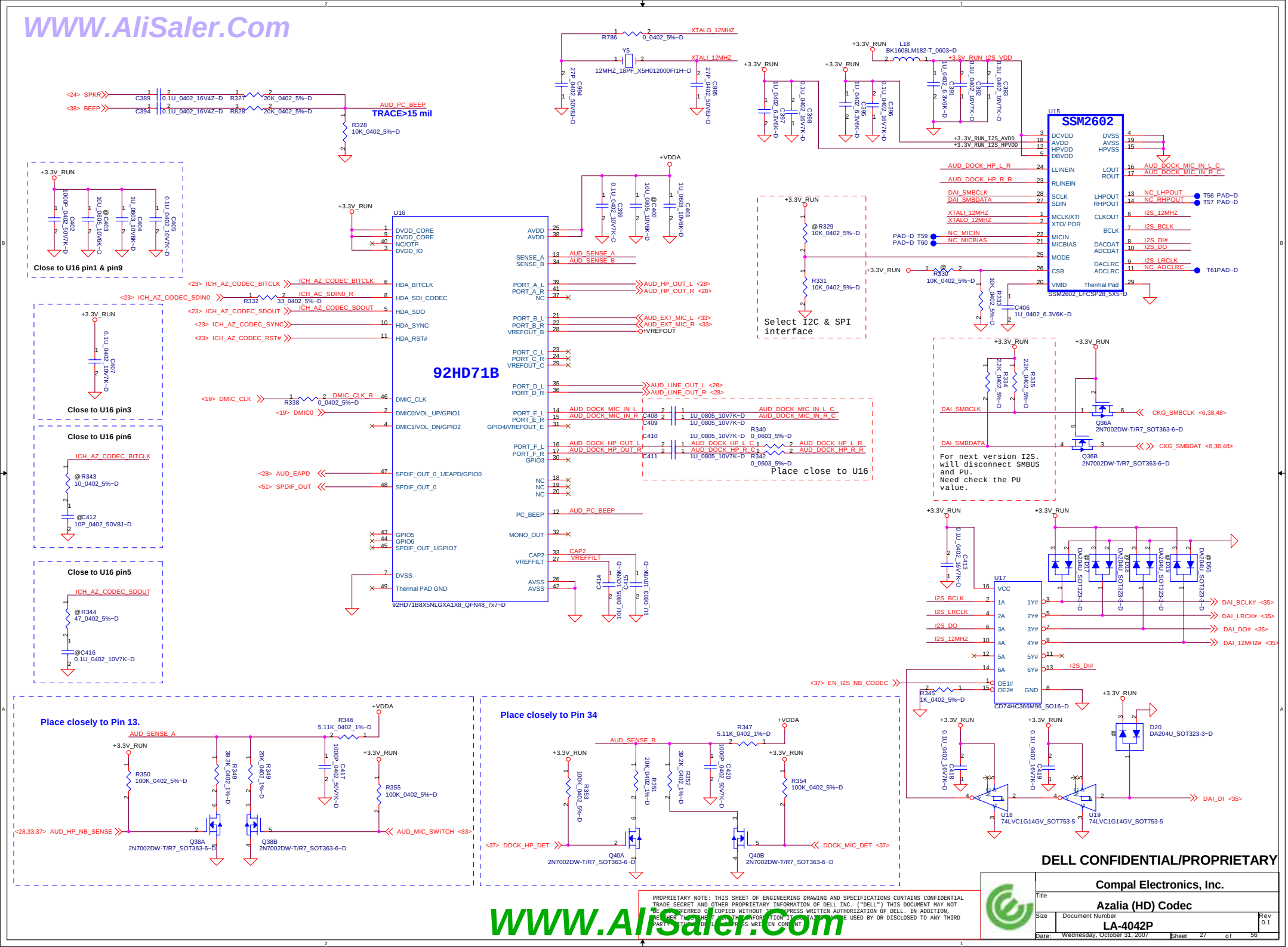
Compal Electronics, Inc.		
Title: ODD/HDD CONNECTOR		
Size	Document Number: LA-4042P	Rev: 0.1
Date: Wednesday, October 31, 2007	Sheet 26 of 56	



Compal Electronics, Inc.	
Title	Azalia (HD) Codec
Size	Document Number: LA-4042P
Rev	0.1
Date:	Wednesday, October 31, 2007
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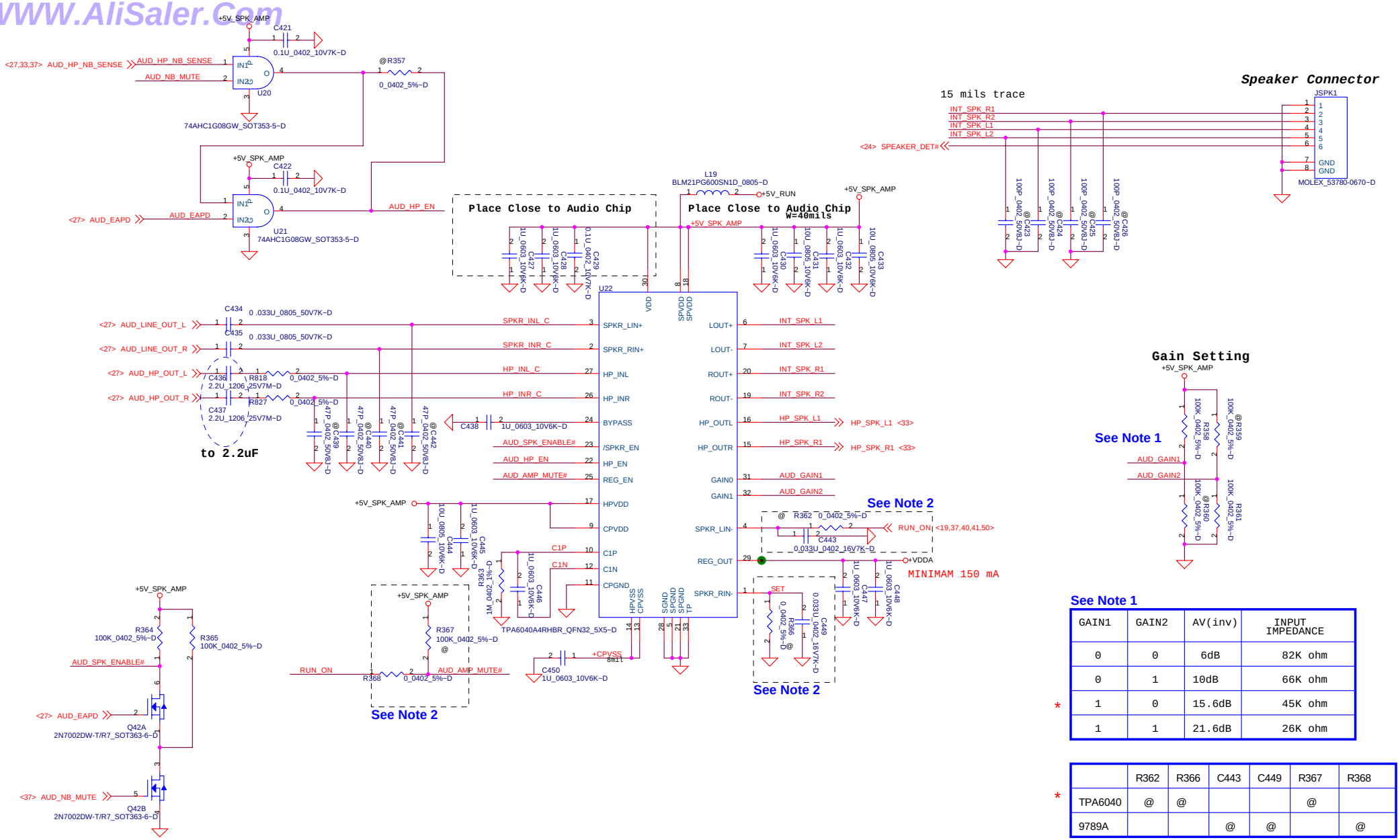

See Note 1

GAIN1	GAIN2	AV(inv)	INPUT IMPEDANCE
0	0	6dB	82K ohm
0	1	10dB	66K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	26K ohm

*

	R362	R366	C443	C449	R367	R368
TPA6040	@	@			@	
9789A			@	@		@

*

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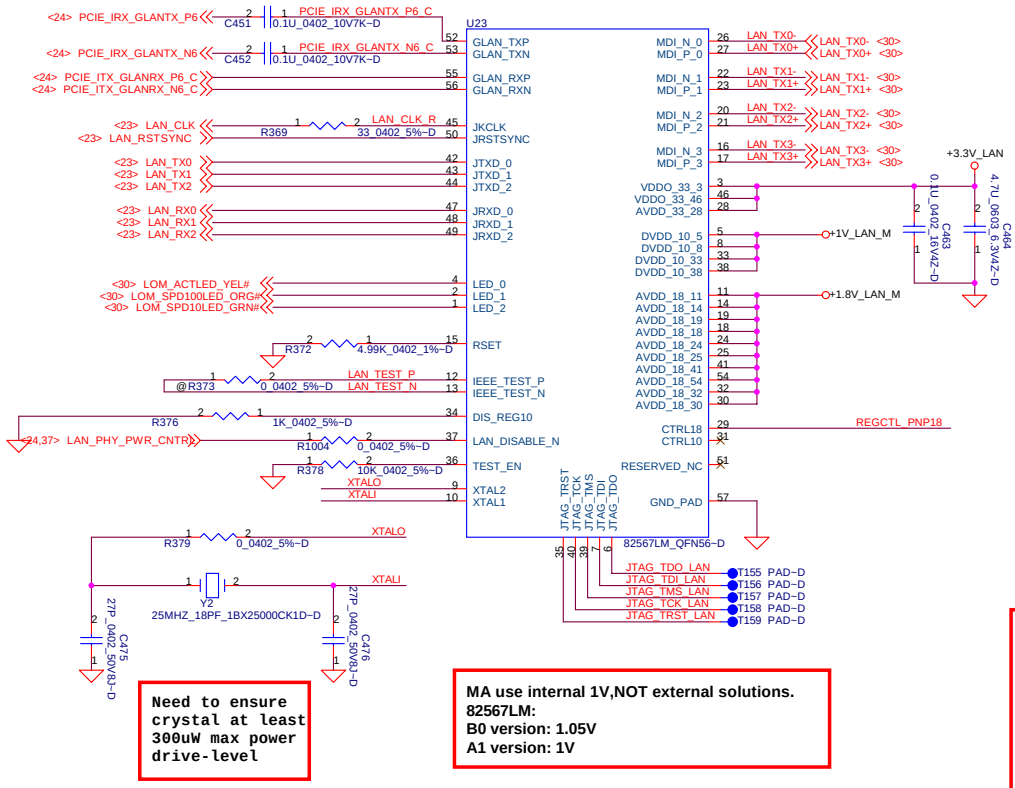
Compal Electronics, Inc.

Title: AMP and PHONE JACK

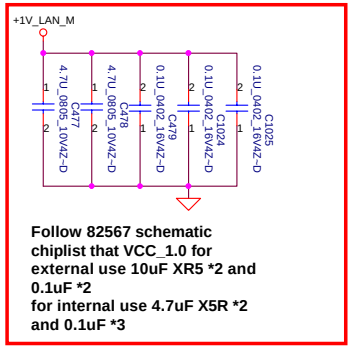
Size: Document Number: LA-4042P Rev: 0.1

Date: Wednesday, October 31, 2007 Sheet 28 of 56



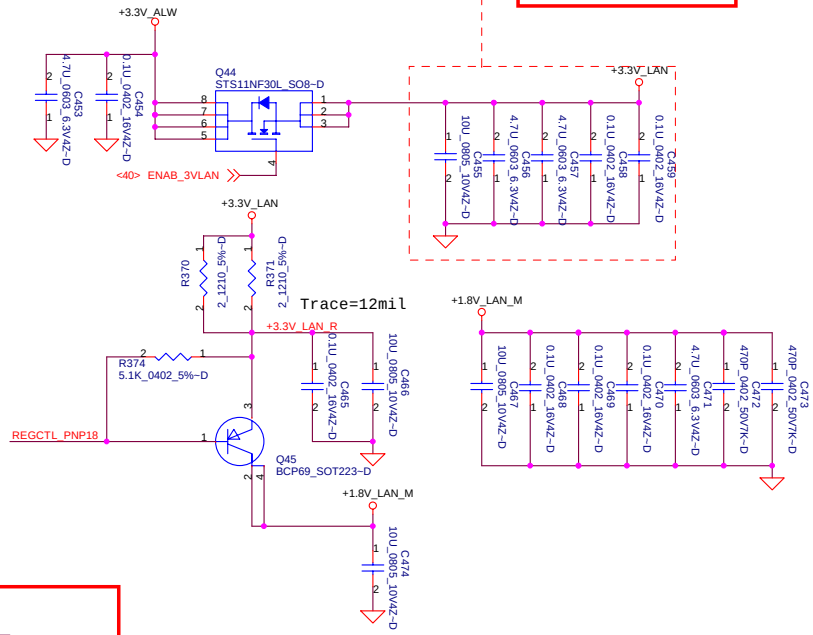
Need to ensure crystal at least 300uW max power drive-level

MA use internal 1V,NOT external solutions.
82567LM:
B0 version: 1.05V
A1 version: 1V



Follow 82567 schematic chiplist that VCC_1.0 for external use 10uF XR5 *2 and 0.1uF *2
for internal use 4.7uF X5R *2 and 0.1uF *3

Layout Notice : Place as close chip as possible.



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Compal Electronics, Inc.

Title: LAN-82567LM

Size: | Document Number: LA-4042P | Rev: 0.1

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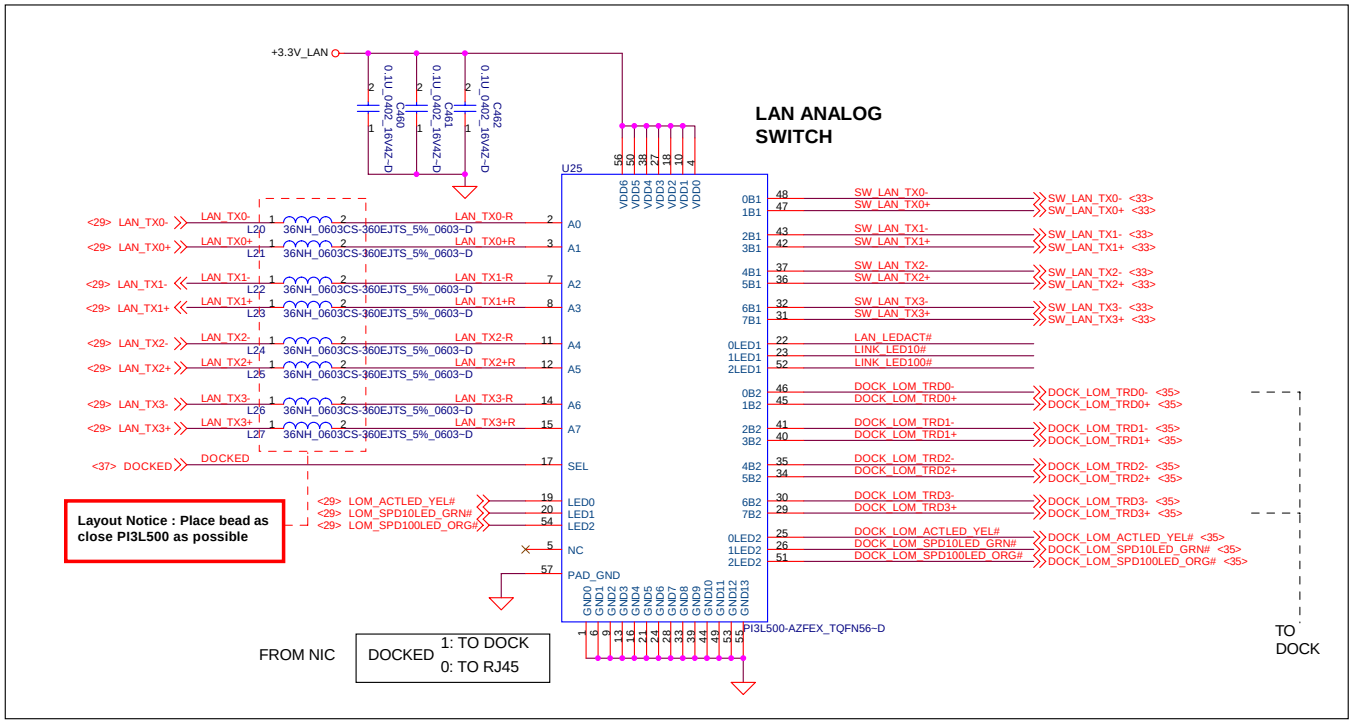

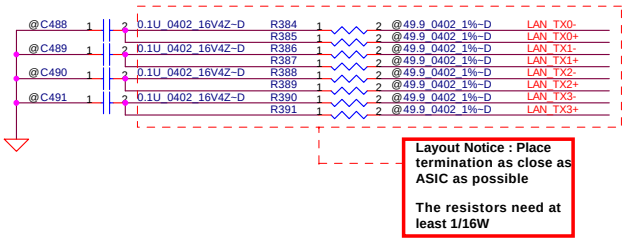

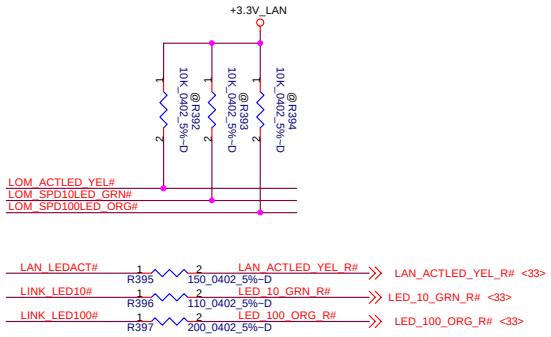

Compal Electronics, Inc.

Title: LAN TRANSFOMER

Size: | Document Number: LA-4042P | Rev: 0.1

Date: Wednesday, October 31, 2007 | Sheet 30 of 56

U26A

R5C847-CSP208Q

PCI I/F

16 bit PC card I/F

RST& INT &

CLK

AUDIO

1394 I/F

Media Card I/F

USB TEST

R5C847-CSP208Q_CSP208-D

must have clean layout

must have clean layout

For MMC PLUS

close to U26

close to R5C847

Close to U26

Close to Pin A16,B16

Close to JP5 pin5

Close to JP5 pin5

Some SD Caps move to SD board.

U27

R5531V002-E2-FA_SSOP16-D

JS1394

HRS_FH28E-20S-0.5SH(11)

JSD1

HRS_FH28E-20S-0.5SH(11)

U28

AAT4250IGV-T1_SOT23-5-D

Compal Electronics, Inc.

Title: CardBus Controller(R5C847)

Size: | Document Number: LA-4042P | Rev: 0.1

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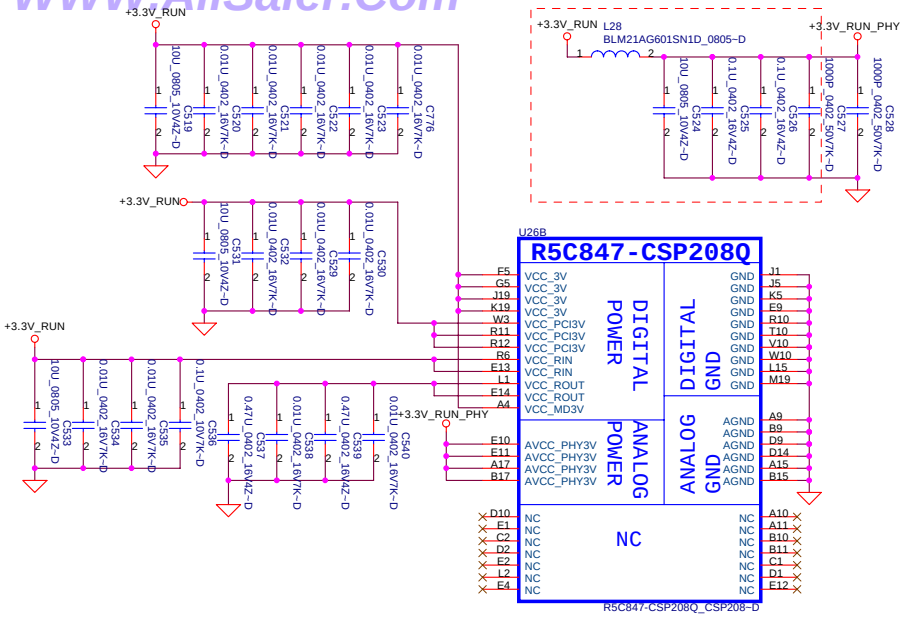
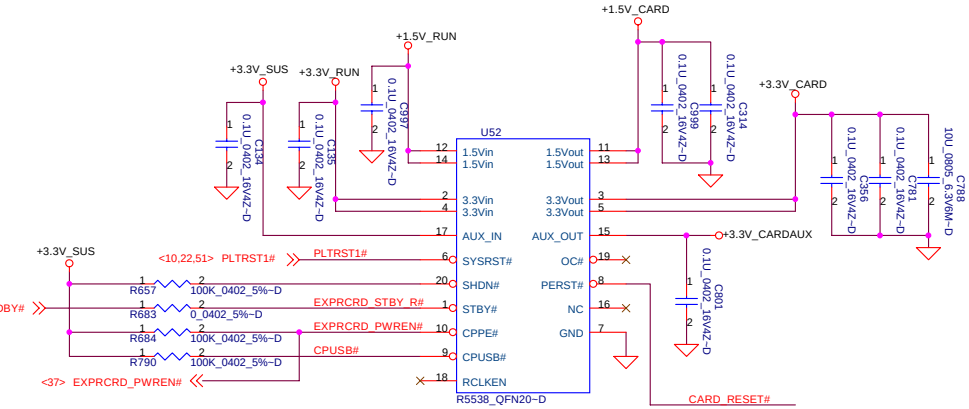
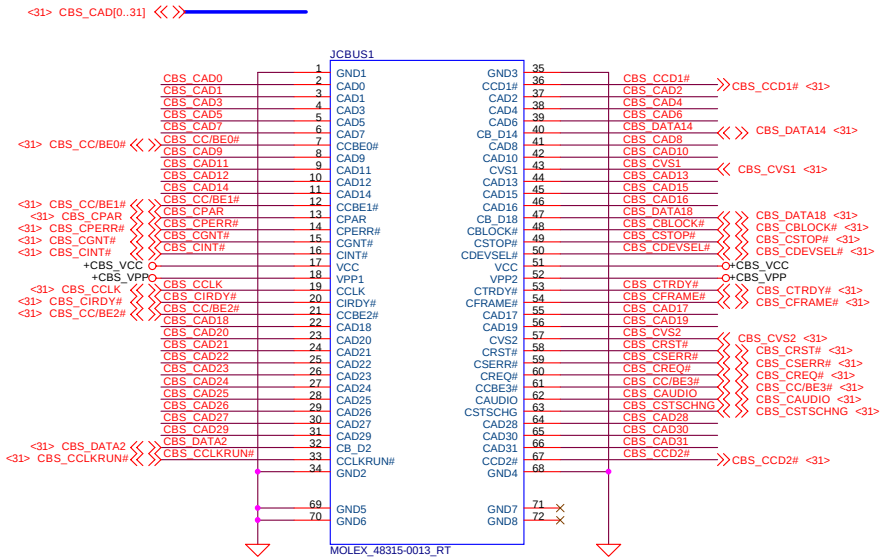
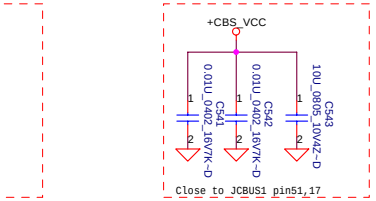


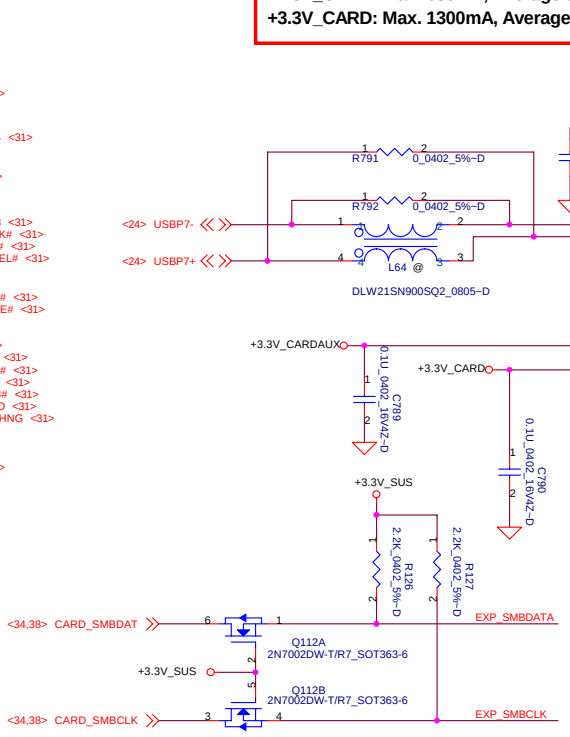


Express Card

+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA







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Compal Electronics, Inc.	
Title	CardBus/SD card Socket
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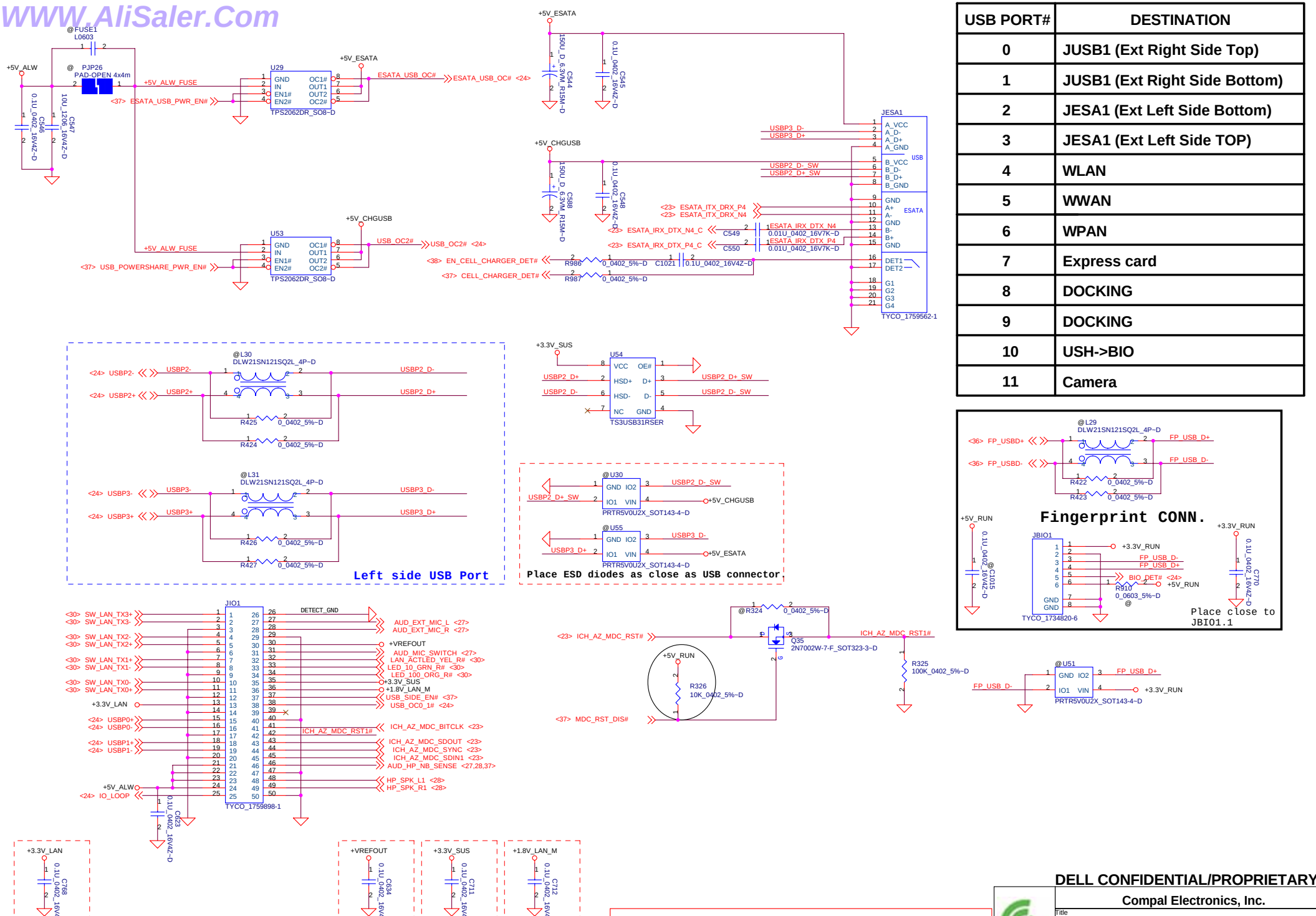
USB PORT#	DESTINATION
0	JUSB1 (Ext Right Side Top)
1	JUSB1 (Ext Right Side Bottom)
2	JESA1 (Ext Left Side Bottom)
3	JESA1 (Ext Left Side TOP)
4	WLAN
5	WWAN
6	WPAN
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	Camera



Compal Electronics, Inc.

Title: USB 2.0 PORT

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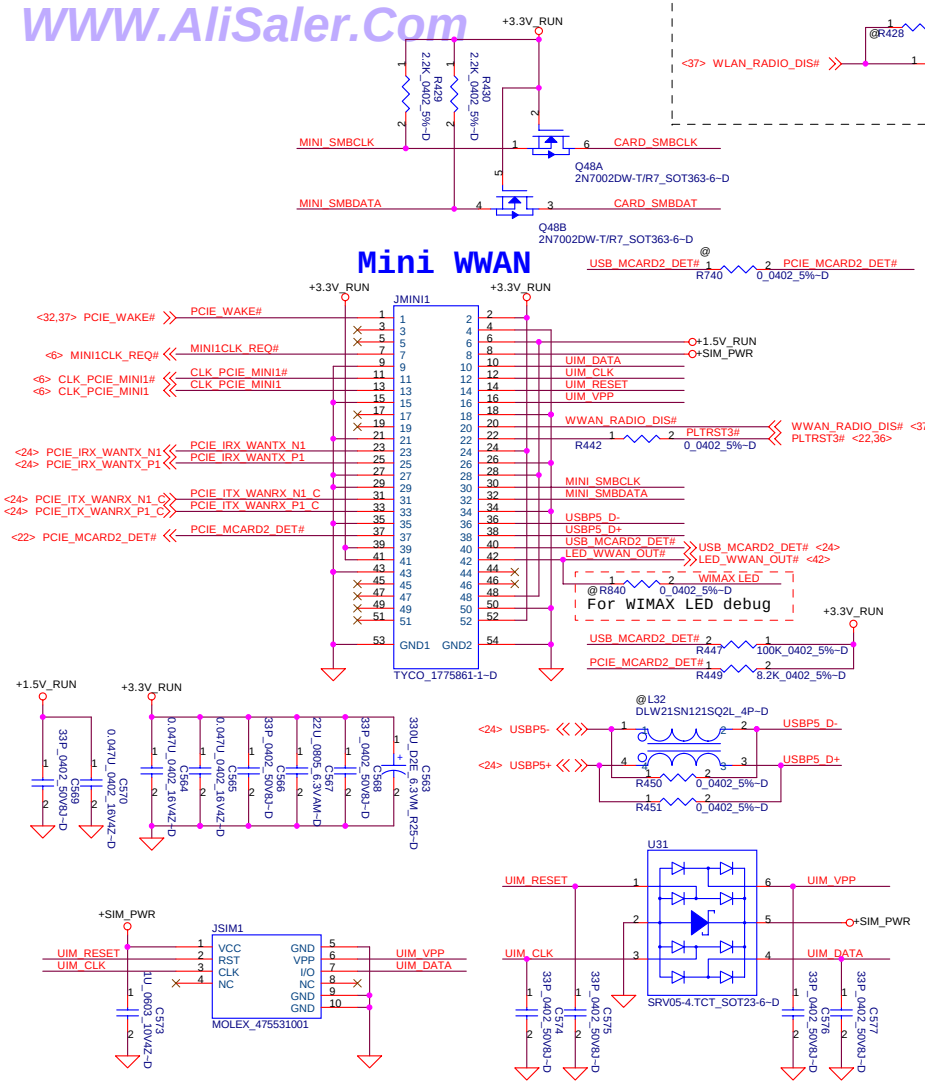
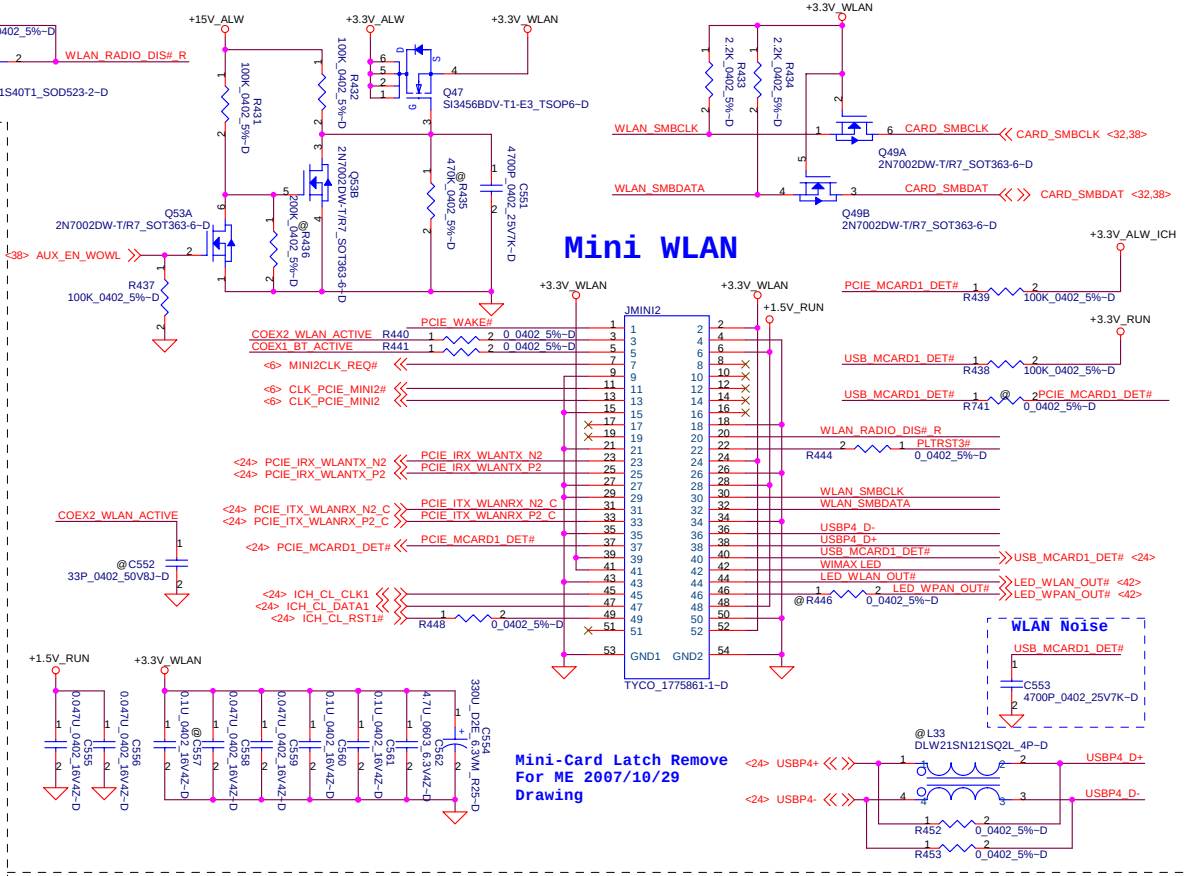
Mini WWAN

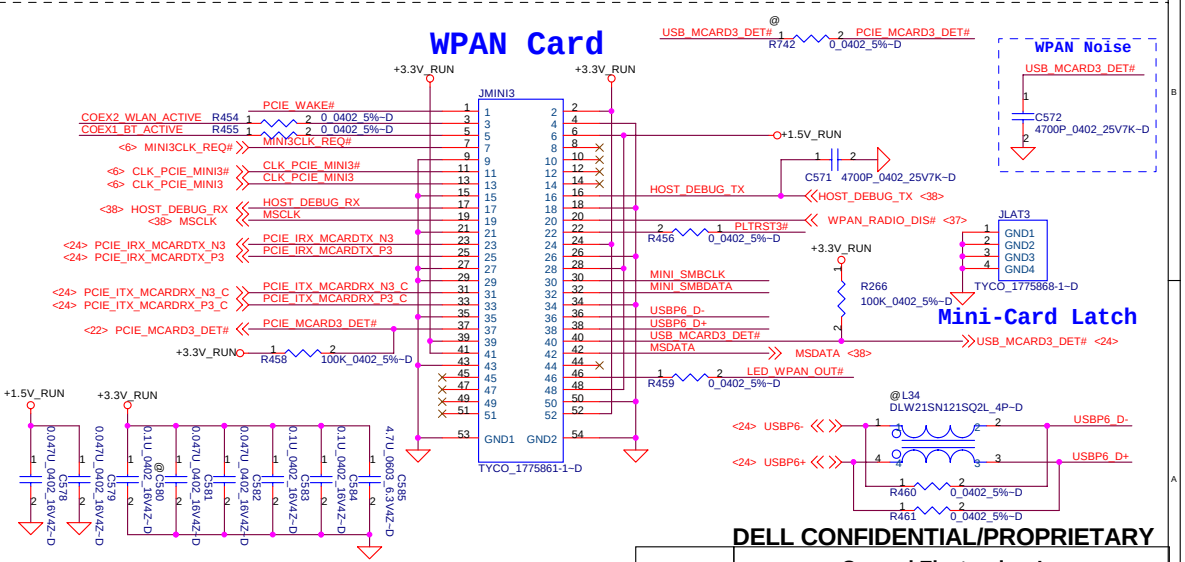


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

Mini WLAN



WPAN Card



Compal Electronics, Inc.

Title: Mini Card

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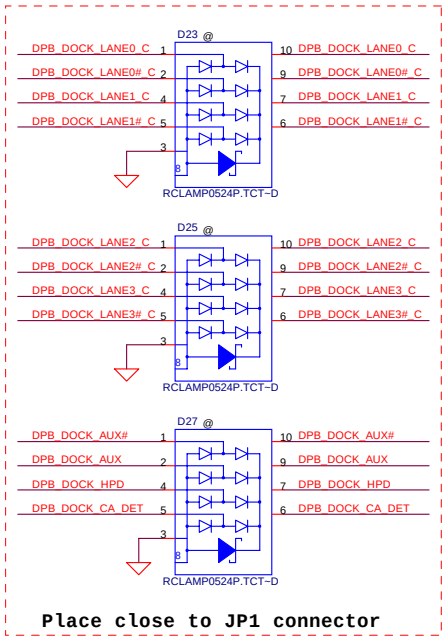

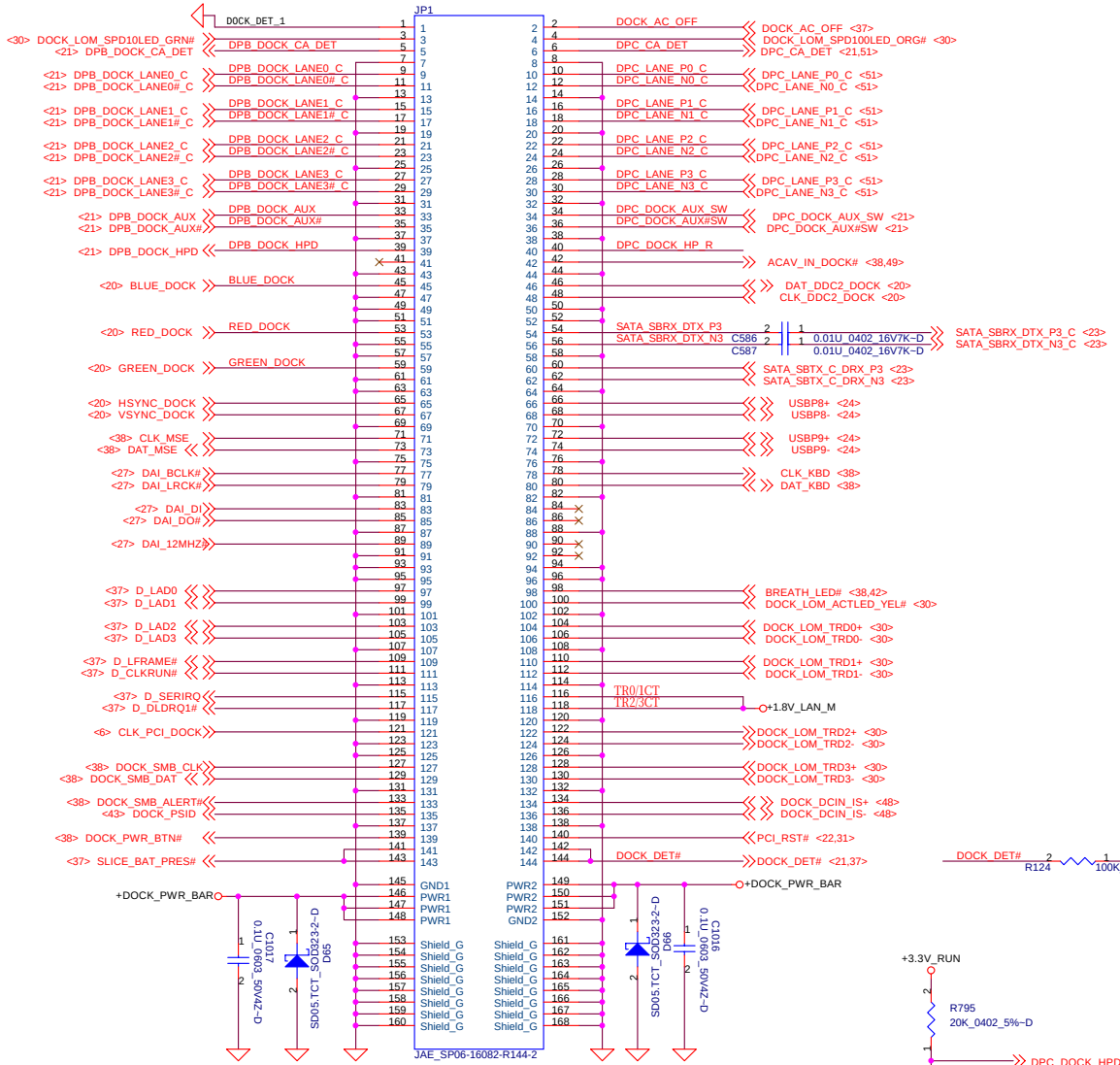

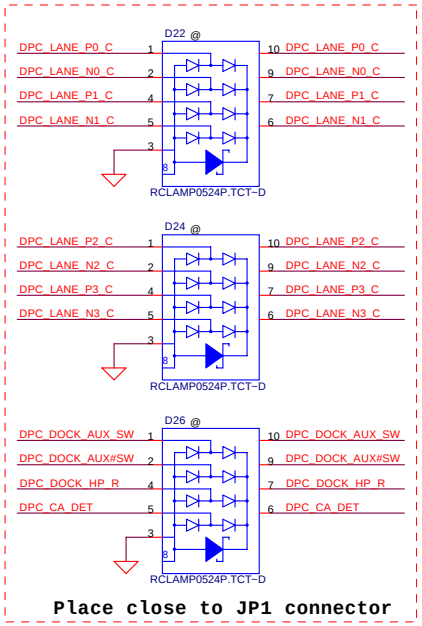

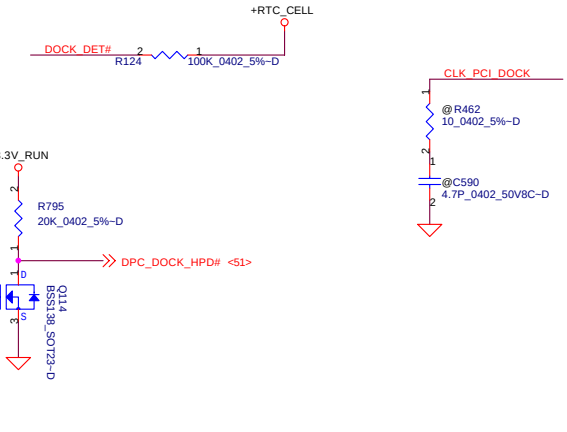

Compal Electronics, Inc.	
Title	DOCKING CONN
Size	Document Number: LA-4042P
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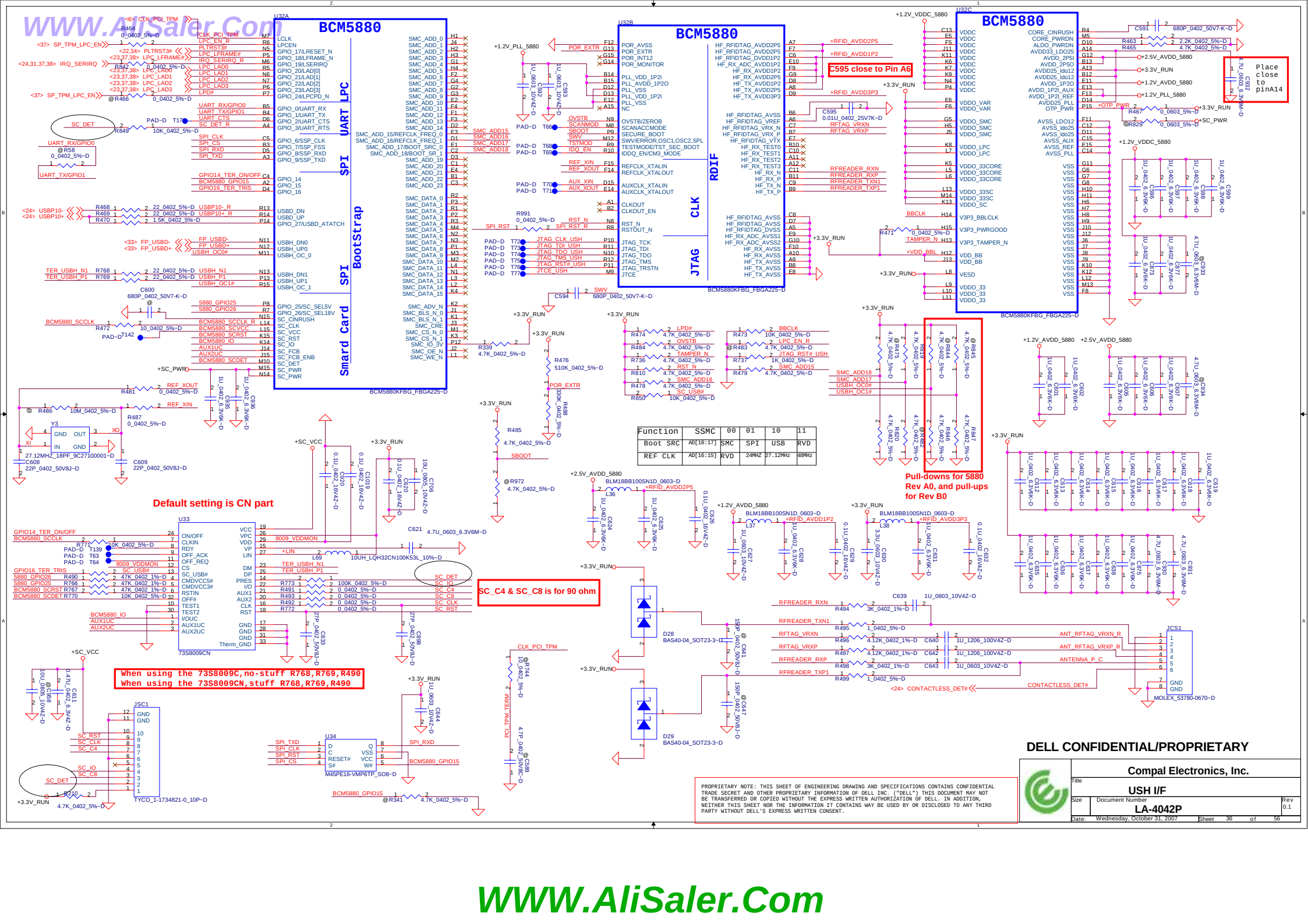

Function	SSMC	00	01	10	11
Boot SRC	AD[18:17]	SMC	SPI	USB	RVD
REF CLK	AD[16:15]	RVD	24MHZ	27.12MHz	48MHz

Compal Electronics, Inc.

Title: USH I/F

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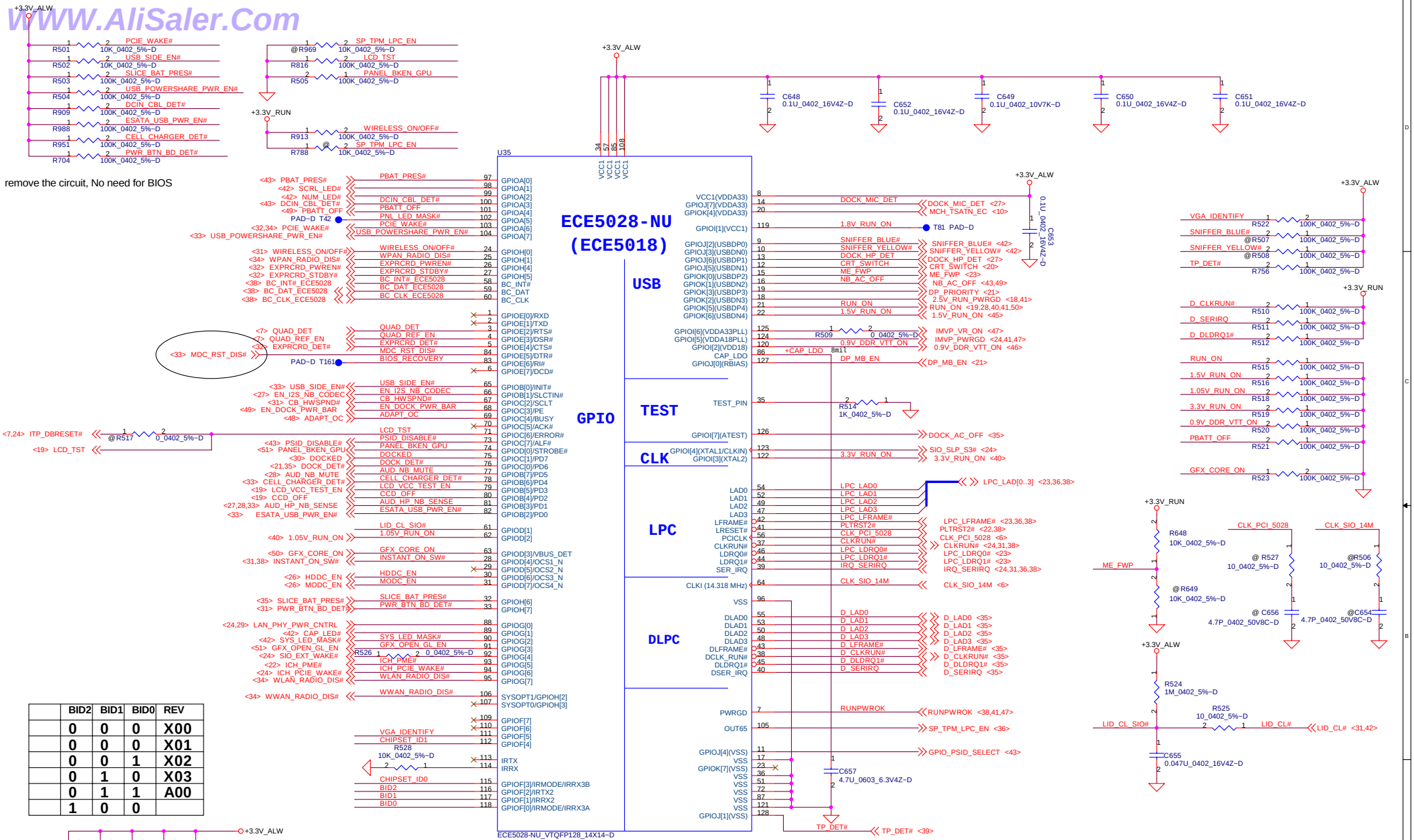

	BID2	BID1	BID0	REV
	0	0	0	X00
	0	0	0	X01
	0	0	1	X02
	0	1	0	X03
	0	1	1	A00
	1	0	0	

CHIPSET_ID1	CHIPSET_ID0	
0	0	Roush-I Foose-I
0	1	Roush-A
1	0	SmFF
1	1	Nike

Compal Electronics, Inc.

Title: ECE5028

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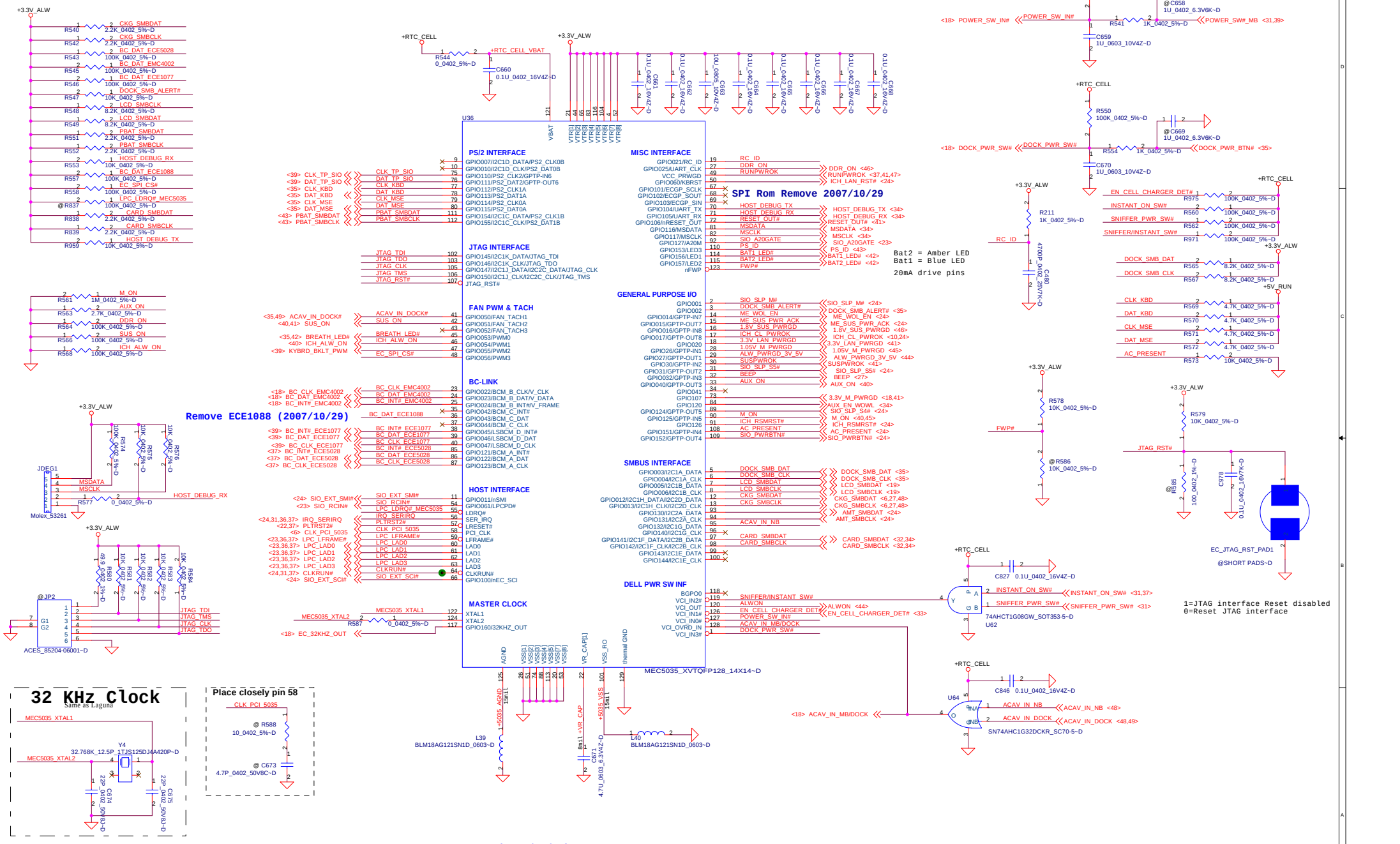

Compal Electronics, Inc.	
Title	EMC5035
Size	Document Number: LA-4042P
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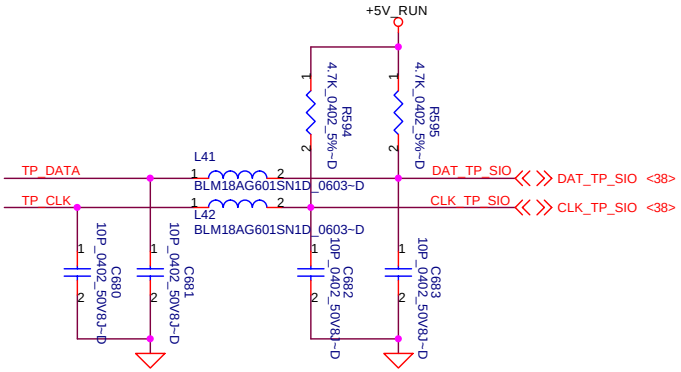

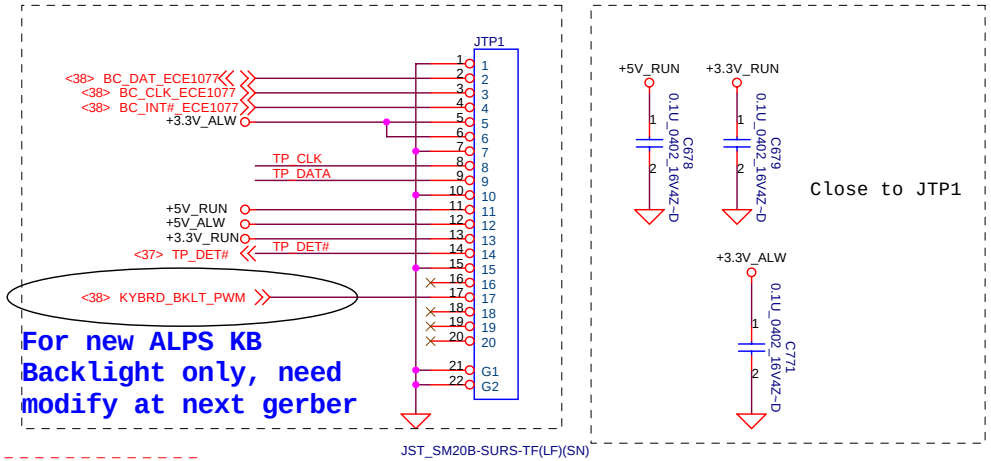

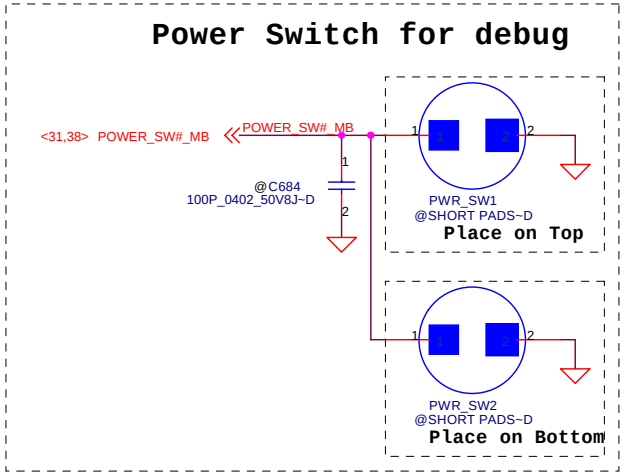

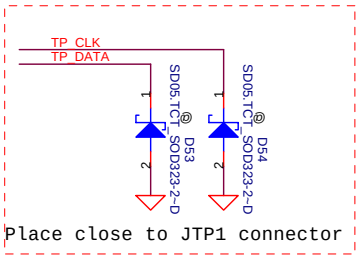

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Compal Electronics, Inc.	
Title	Touch PAD/Int KB/LID
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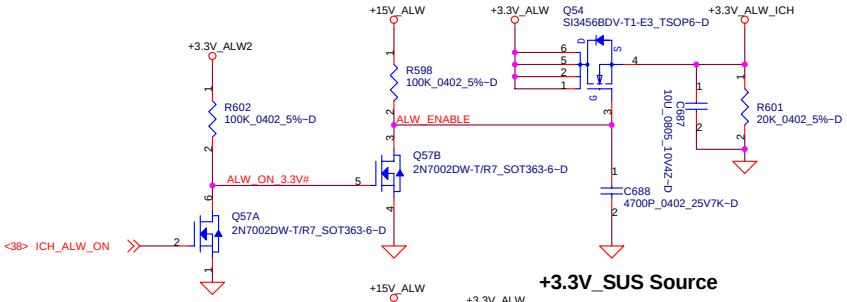
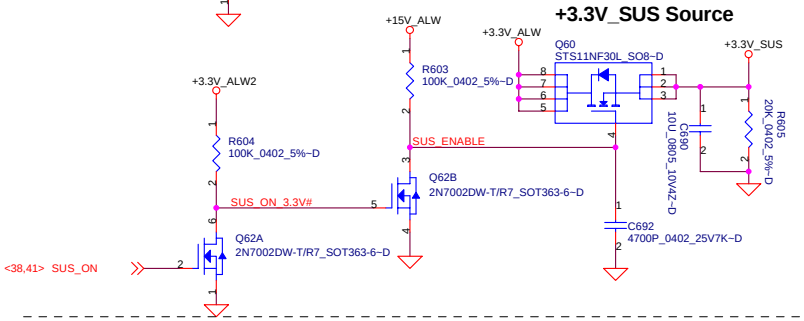
DC/DC Interface

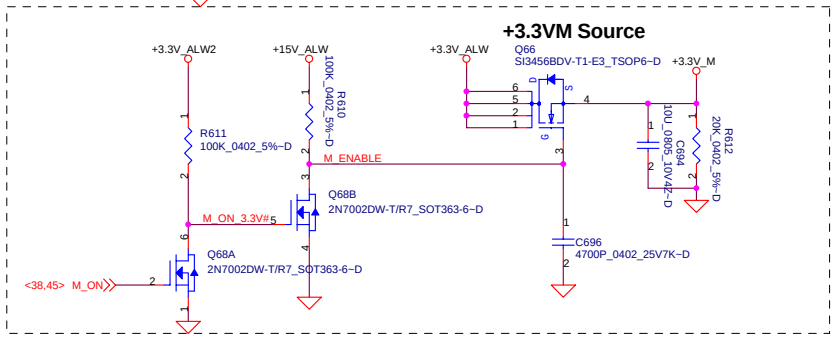
+3.3V_ALW_ICH Source

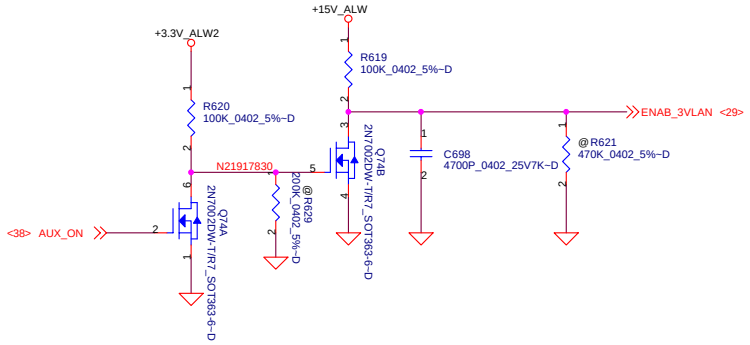


+3.3V_SUS Source

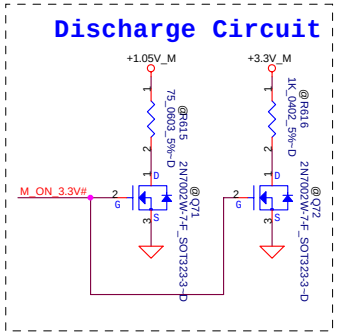


+3.3VM Source

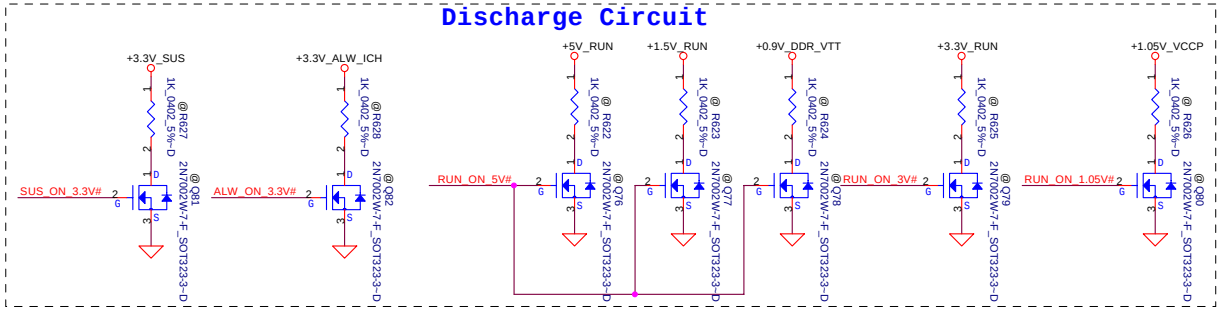




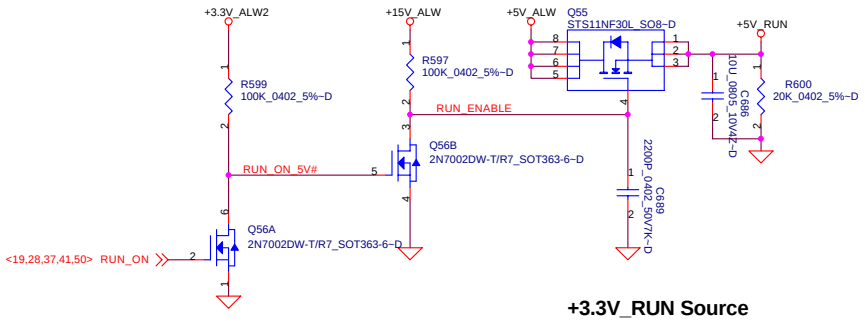
Discharge Circuit



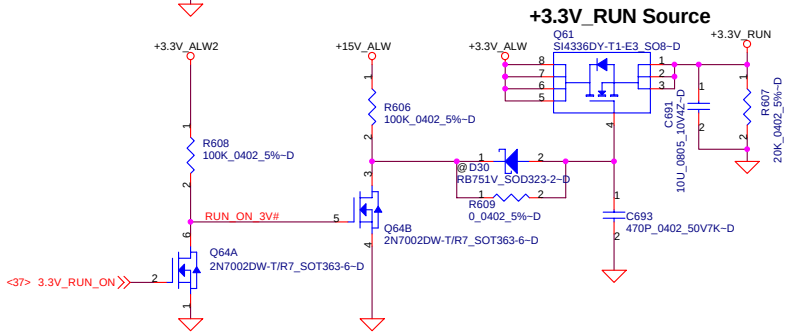
Discharge Circuit



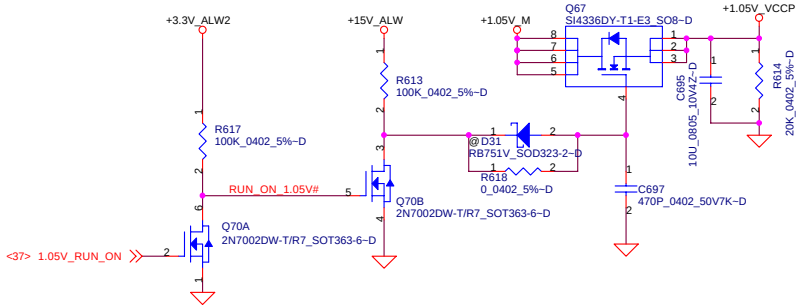
+5VRUN Source



+3.3V_RUN Source



+1.05V_VCCP Source



Compal Electronics, Inc.

Title: POWER CONTROL

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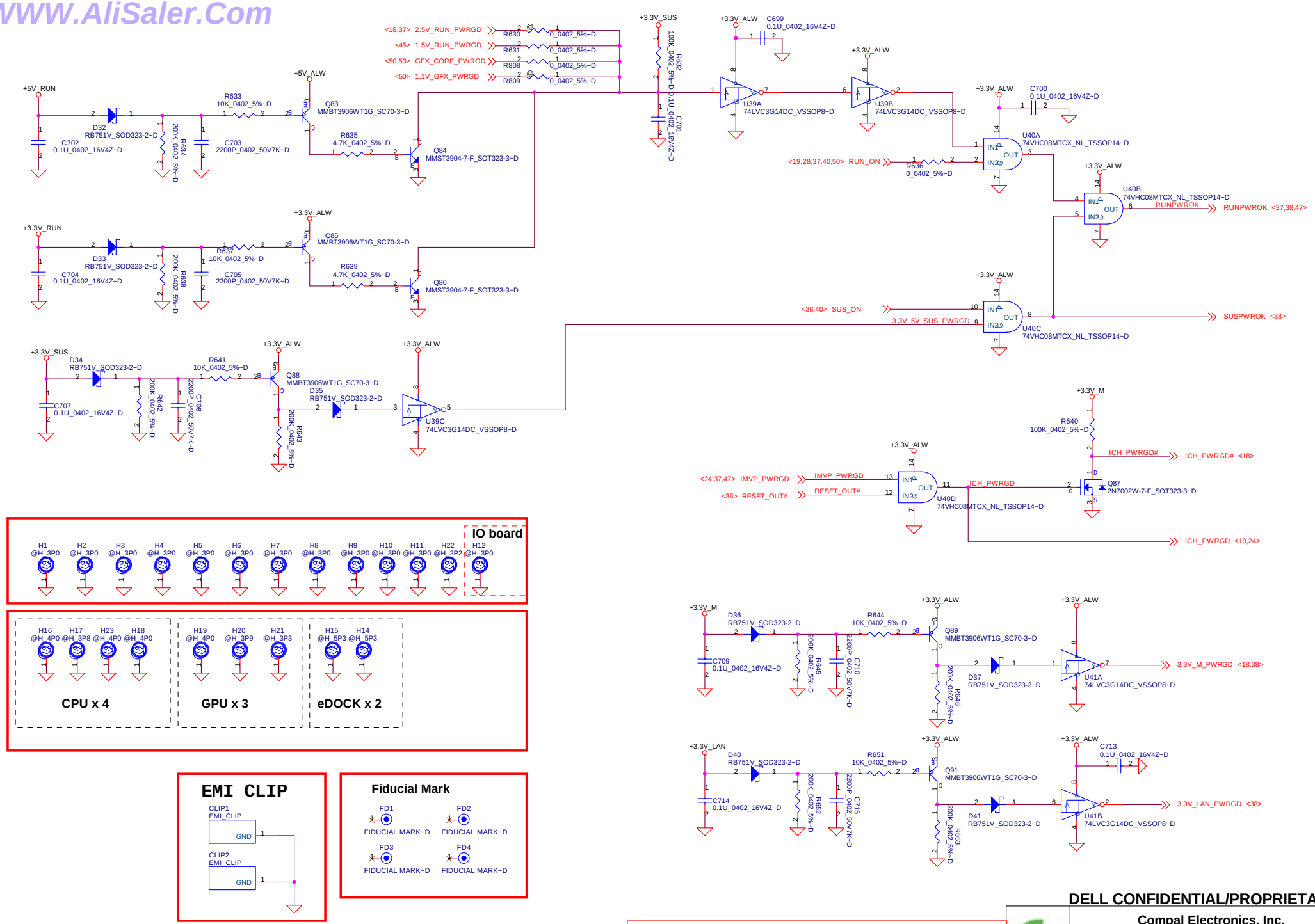

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Compal Electronics, Inc.	
Title	Power Good
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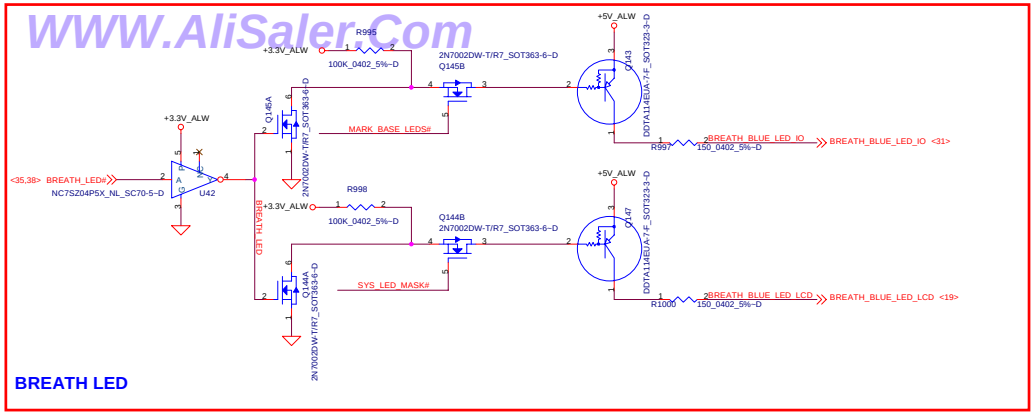
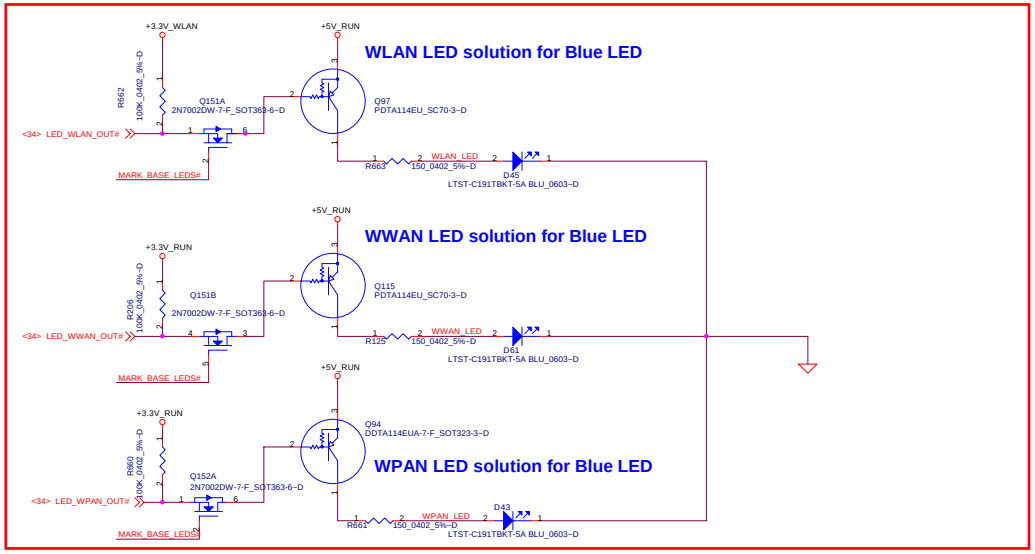
BREATH LED



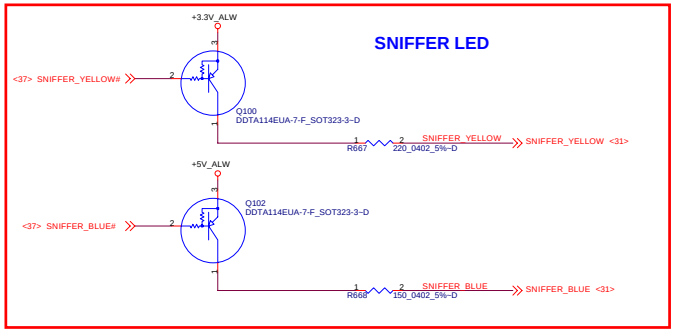
WLAN LED solution for Blue LED



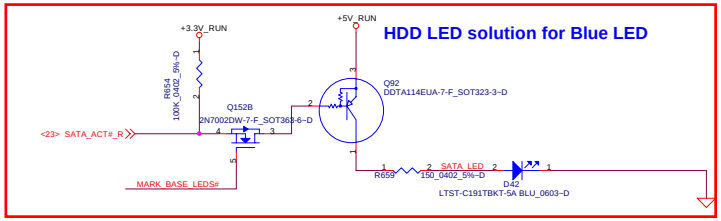
WWAN LED solution for Blue LED

WPAN LED solution for Blue LED

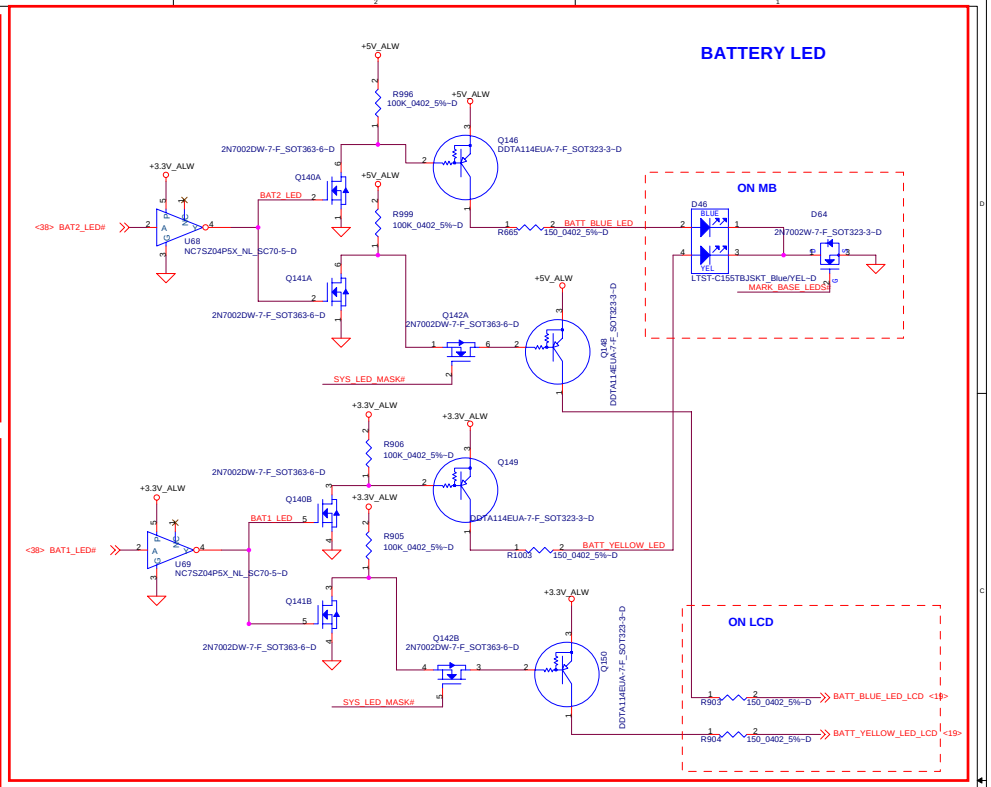
SNIFFER LED



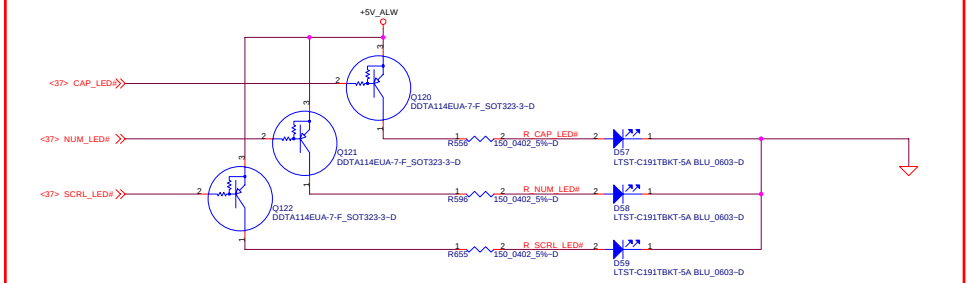
HDD LED solution for Blue LED

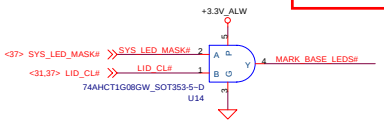


BATTERY LED



KEYBOARD STATUS LED





BIOS GPIO Table for LED Control

	SYS_LED_MARK#	LID_CL#
MARK ALL LED (SNIFFER FUNCTION)	Low	X
MARK BASE MB LEDs (Lid Closed)	High	Low
Do Not Mark LEDs (Lid Opened)	High	High

Compal Electronics, Inc.

Title: PAD and Standoff

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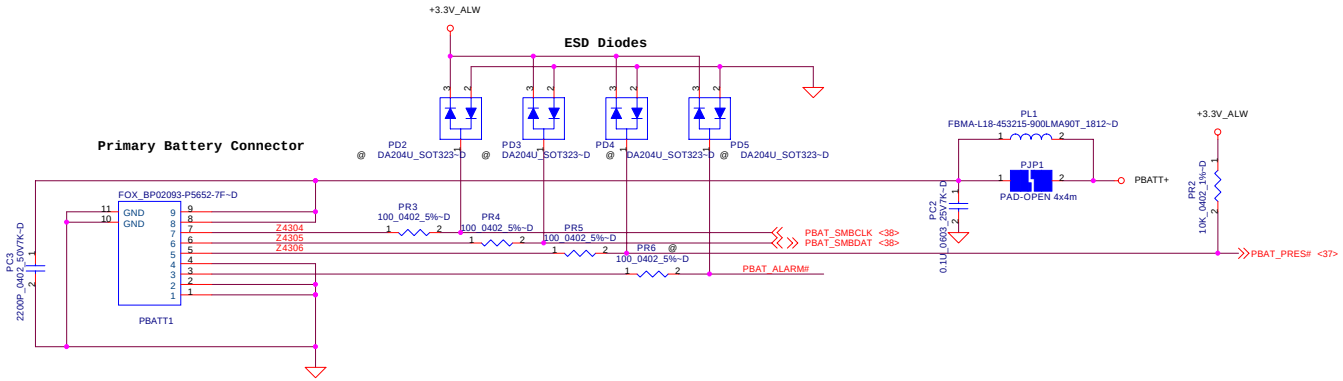

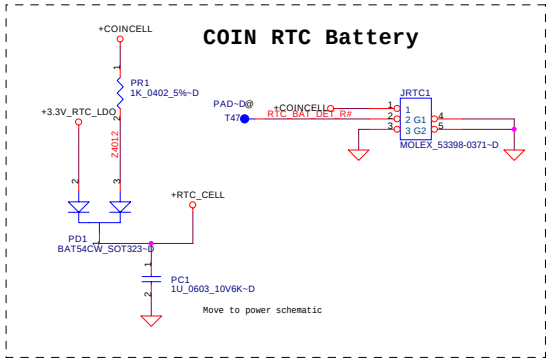

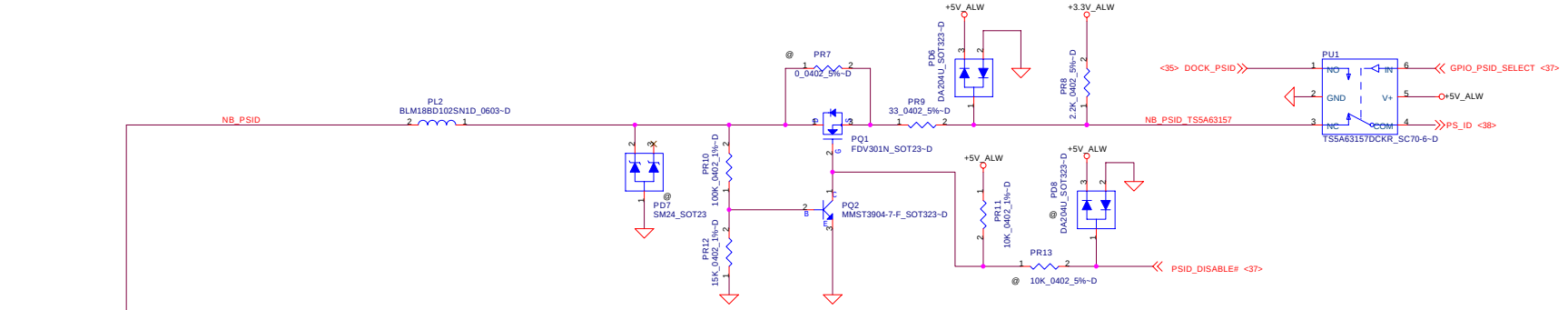

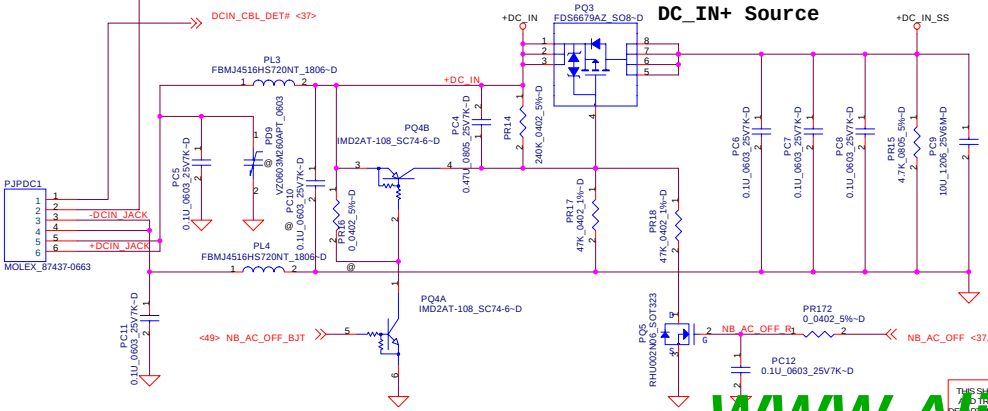

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Compal Electronics, Inc.

Title: +DCIN

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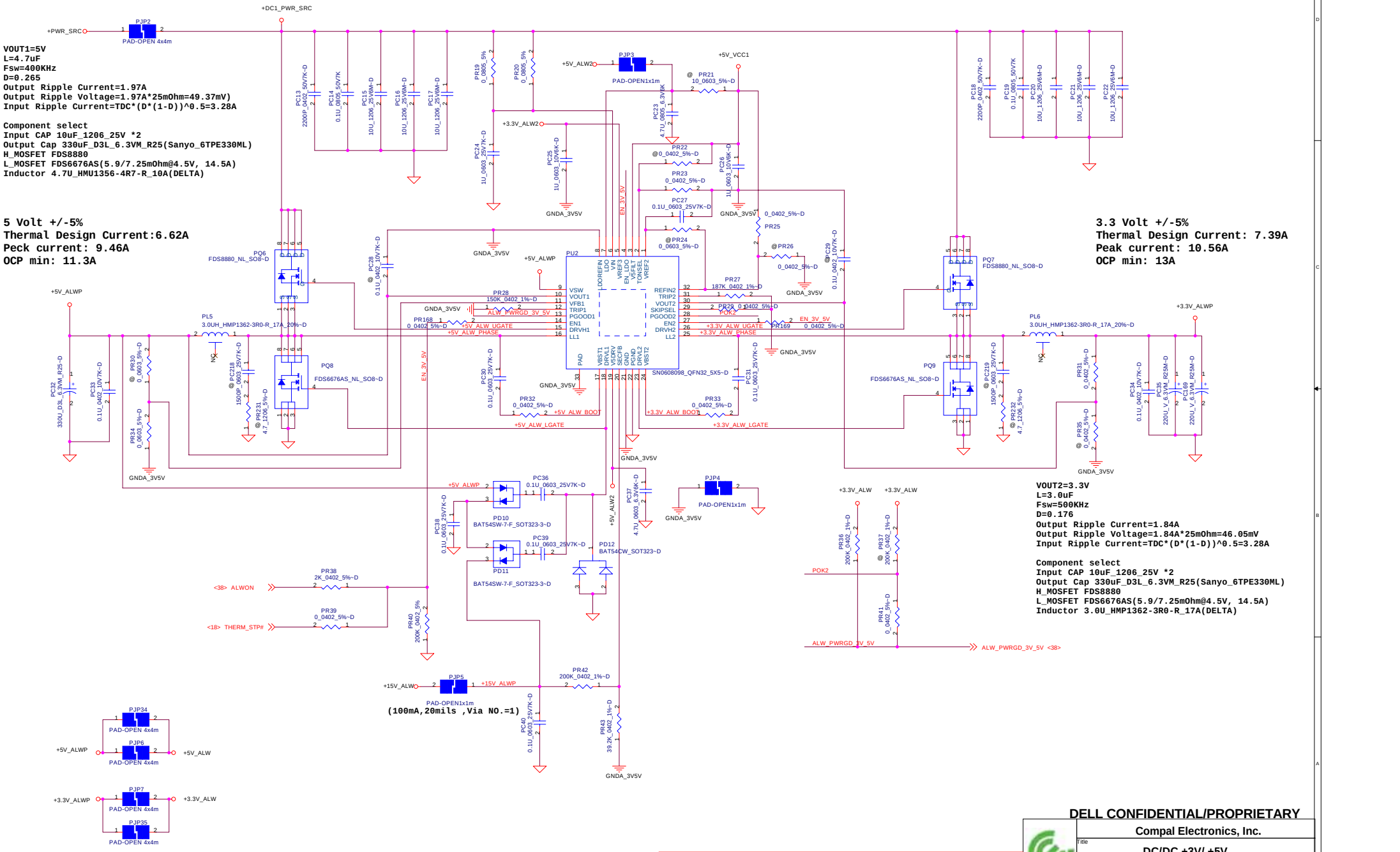
+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP



Compal Electronics, Inc.		
Title: DC/DC +3V/ +5V		
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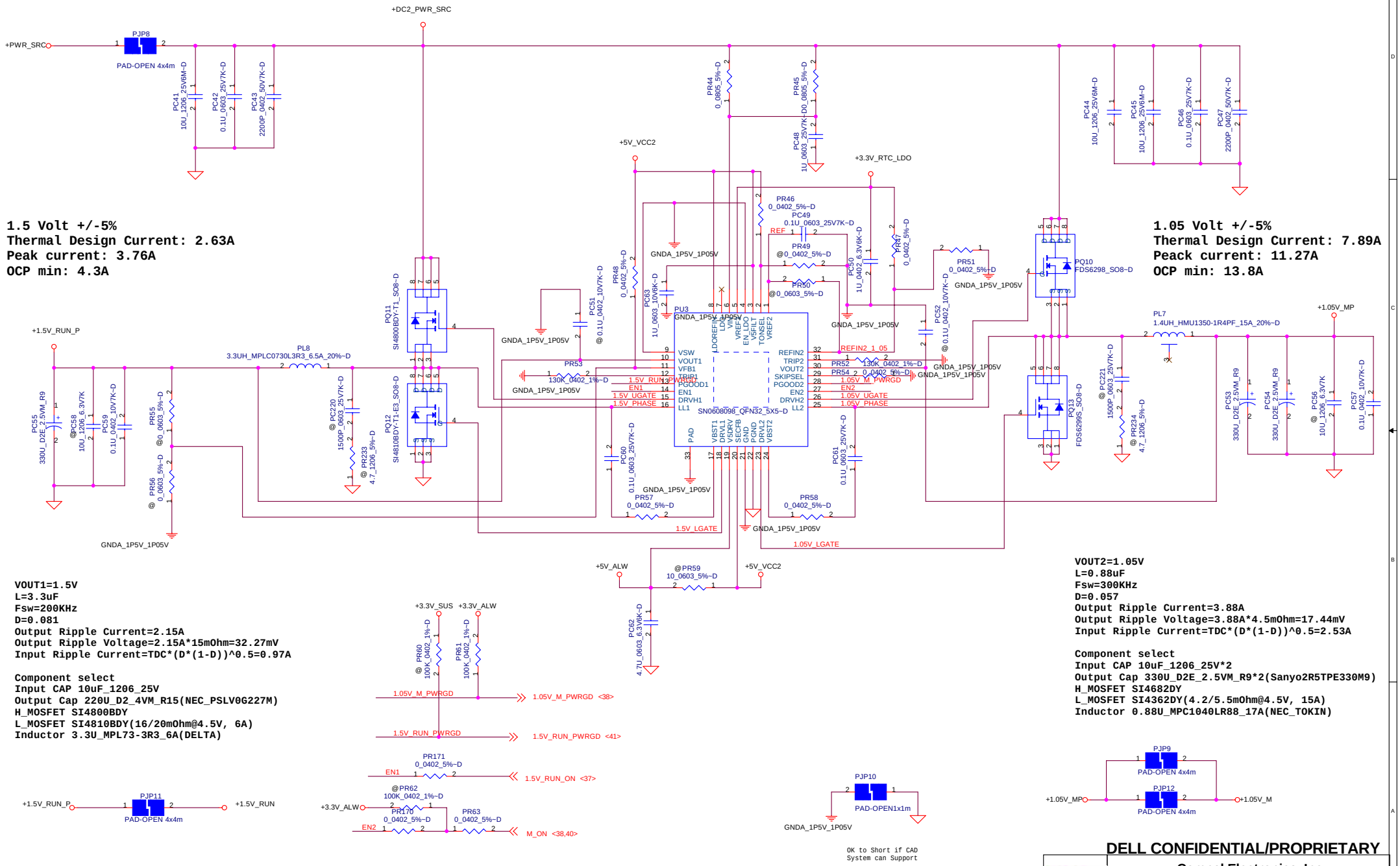
+1.5V_RUN / +1.05V_M/ +3.3V_RTC_LDO



Compal Electronics, Inc.

Title: +1.5V_RUN / +1.05V_VCCP

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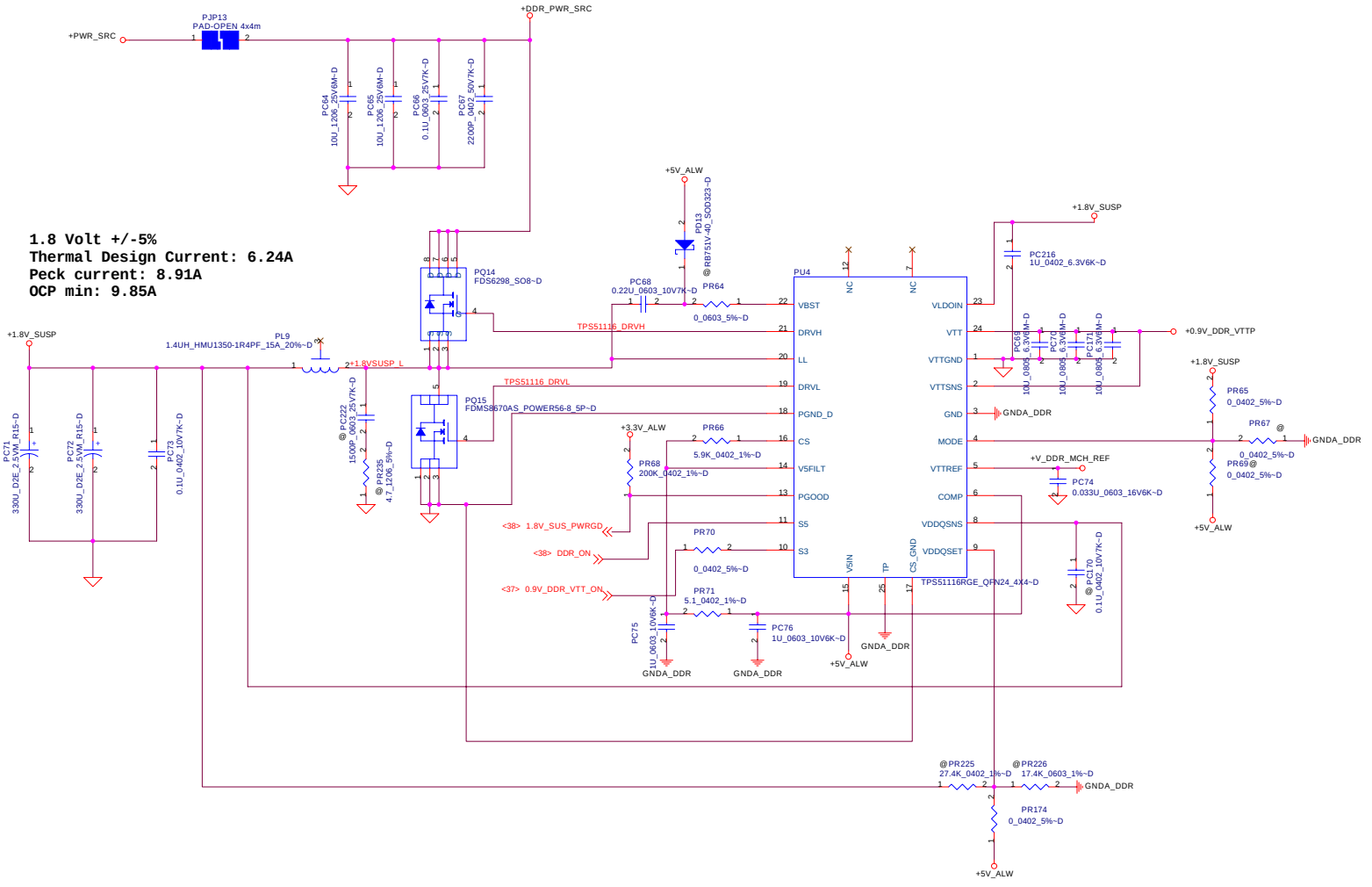
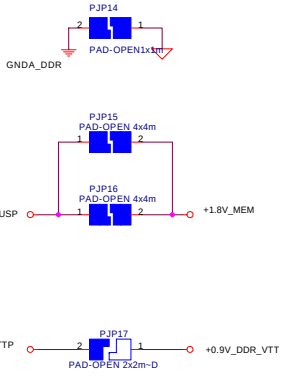
+1.8VSUSP/ +0.9V_DDR_VTT

DDR2 Termination

1.8 Volt +/-5%
Thermal Design Current: 6.24A
Peck current: 8.91A
OCP min: 9.85A

Design current 0.7A for +0.9V_DDR_VTTP
Peak current 1A for +0.9V_DDR_VTTP





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Compal Electronics, Inc.	
Title	1.8VSUSP/0.9VDDR
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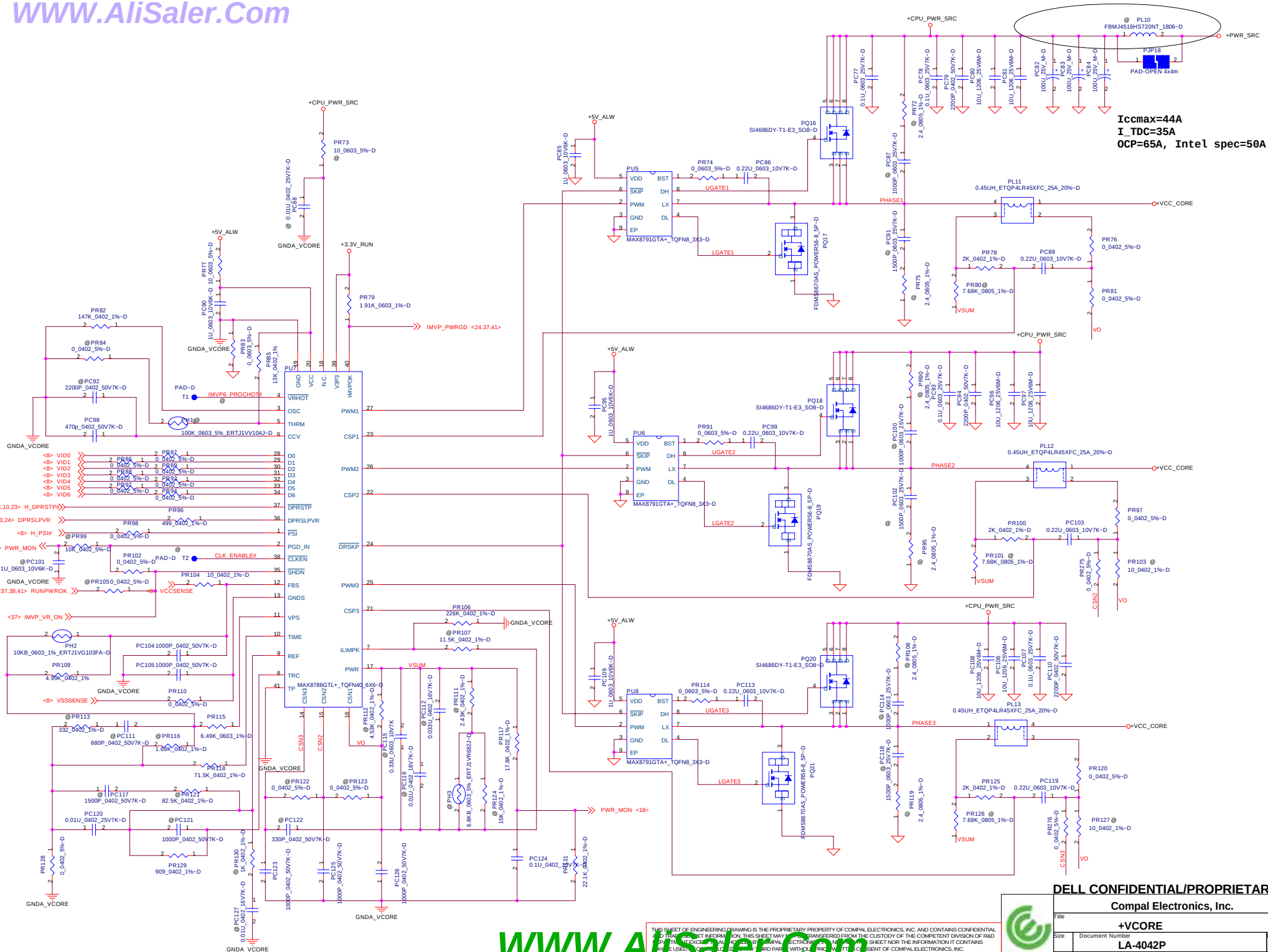

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Compal Electronics, Inc.		
Title: +VCORE		
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TABLE 3, PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

Maximum charging current is 6.24A

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Compal Electronics, Inc.	
Title	Charger
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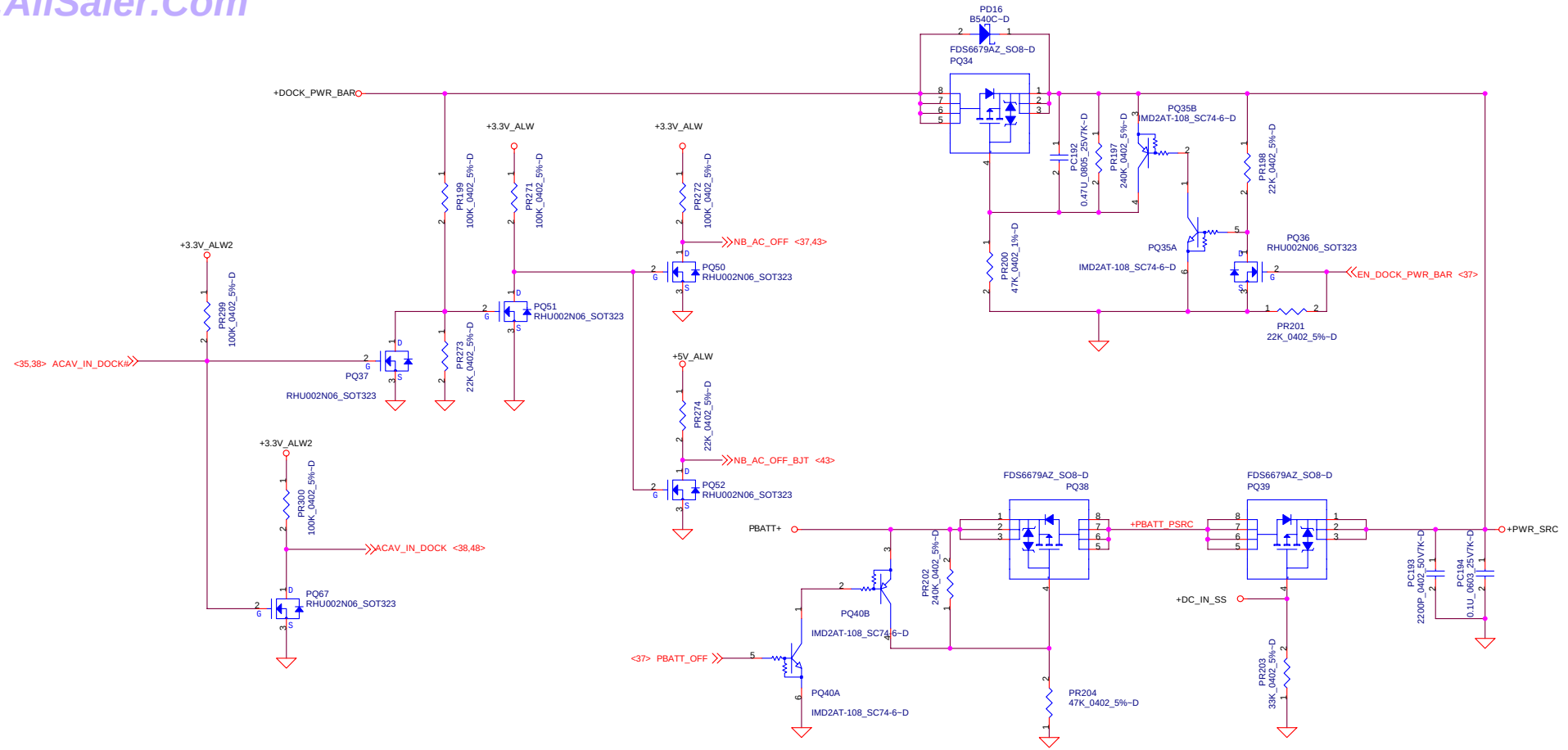

Compal Electronics, Inc.

Title: Selector

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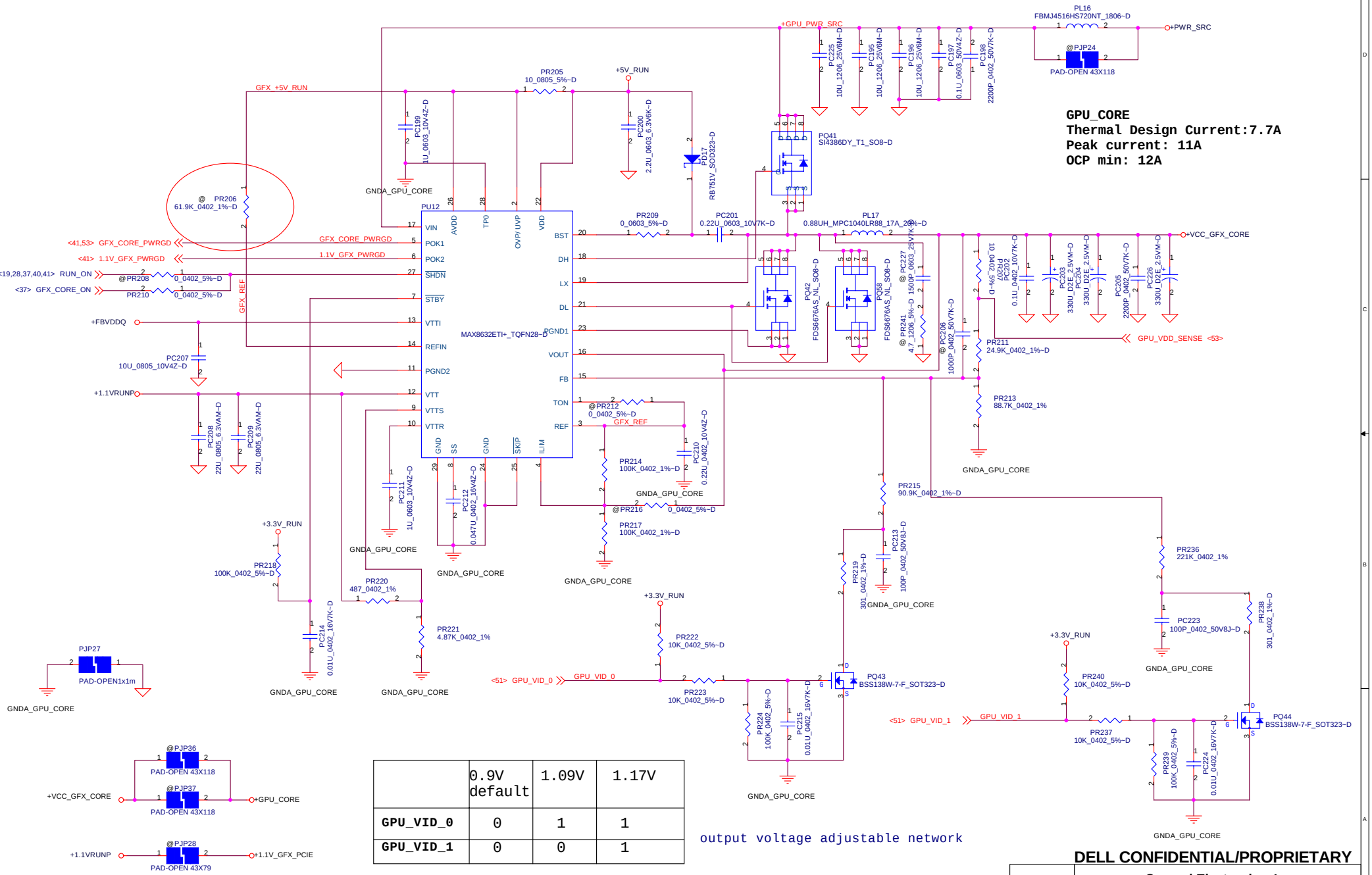

	0.9V default	1.09V	1.17V
GPU_VID_0	0	1	1
GPU_VID_1	0	0	1

Compal Electronics, Inc.

Title: NVG72M VDD_CORE

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GPIO16	GPIO17	DP Conn. function
1	X	DP
0	0	DVI
0	1	HDMI

<---CRT
<---DVI C
<---LVDS
<---DVI B

check GDDR3 and nonOpenGL

Strap pin define

Stuff R718 with 4.99K, not stuff R726.
Stuff R719 with 15K, not stuff R716.
Stuff R725 with 10K, not stuff R717.
Stuff R715 with 20K, not stuff R730.
Stuff R729 with 10K, not stuff R714.
Stuff R713 with 45.3K, not stuff R728

Stuff R824 for standard I2C ROM.
Stuff R801 for crypto ROM

Compal Electronics, Inc.

Title: NVG98 PCIE,GPIO,CLK,LVDS

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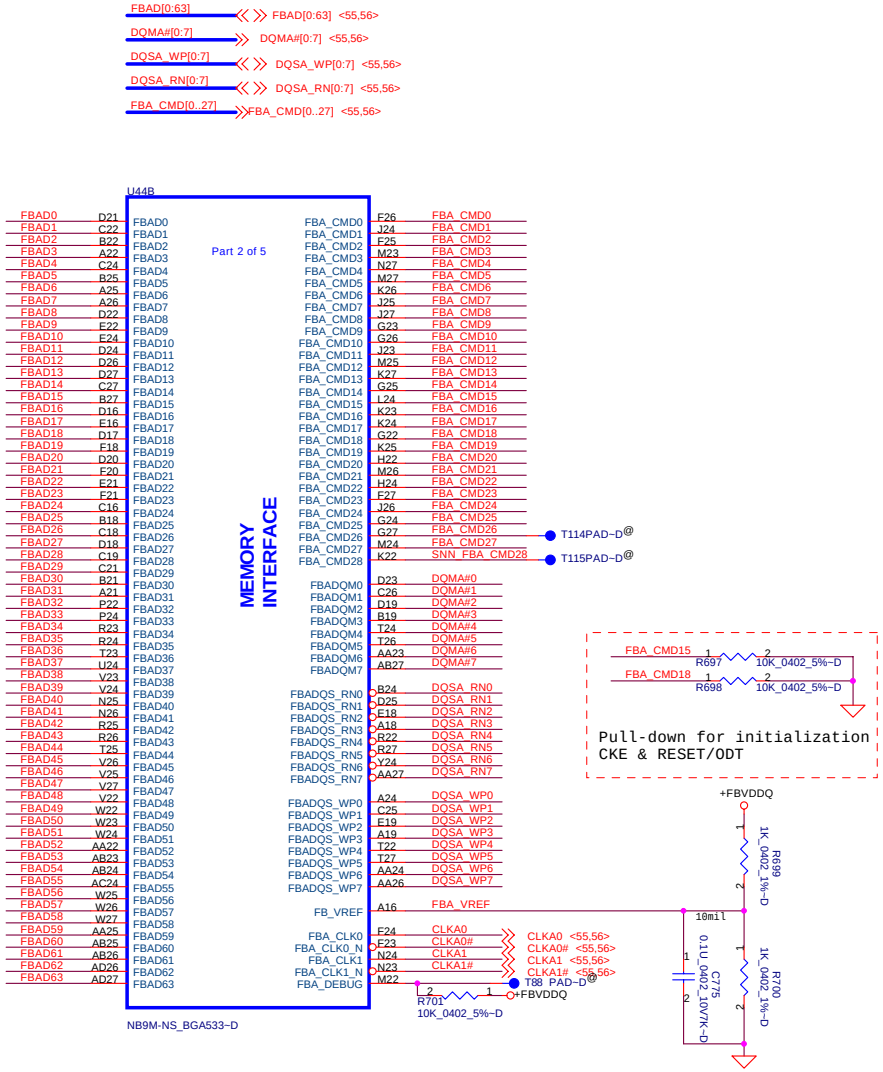

	0..31	32..63
FBA_CMD0	A4	
FBA_CMD1	RAS#	RAS#
FBA_CMD2	A5	
FBA_CMD3	BA1	BA1
FBA_CMD4		A2
FBA_CMD5		A4
FBA_CMD6		A3
FBA_CMD7	CS1#	CS1#
FBA_CMD8	CS0#	CS0#
FBA_CMD9	A11	A11
FBA_CMD10	CAS#	CAS#
FBA_CMD11	WE#	WE#
FBA_CMD12	BA0	BA0
FBA_CMD13		A5
FBA_CMD14	A12	A12
FBA_CMD15	RST/ODT	RST/ODT
FBA_CMD16	A7	A7
FBA_CMD17	A10	A10
FBA_CMD18	CKE	CKE
FBA_CMD19	A0	A0
FBA_CMD20	A9	A9
FBA_CMD21	A6	A6
FBA_CMD22	A2	
FBA_CMD23	A8	A8
FBA_CMD24	A3	
FBA_CMD25	A1	A1
FBA_CMD26	A13	A13
FBA_CMD27	BA2	BA2
FBA_CMD28	RFU0	RFU0
FBA_CMD29	RFU1	RFU1
FBA_CMD30	RFU2	RFU2

Compal Electronics, Inc.

Title: NVG98 Memory Interface

Size: | Document Number: LA-4042P | Rev: 0.4

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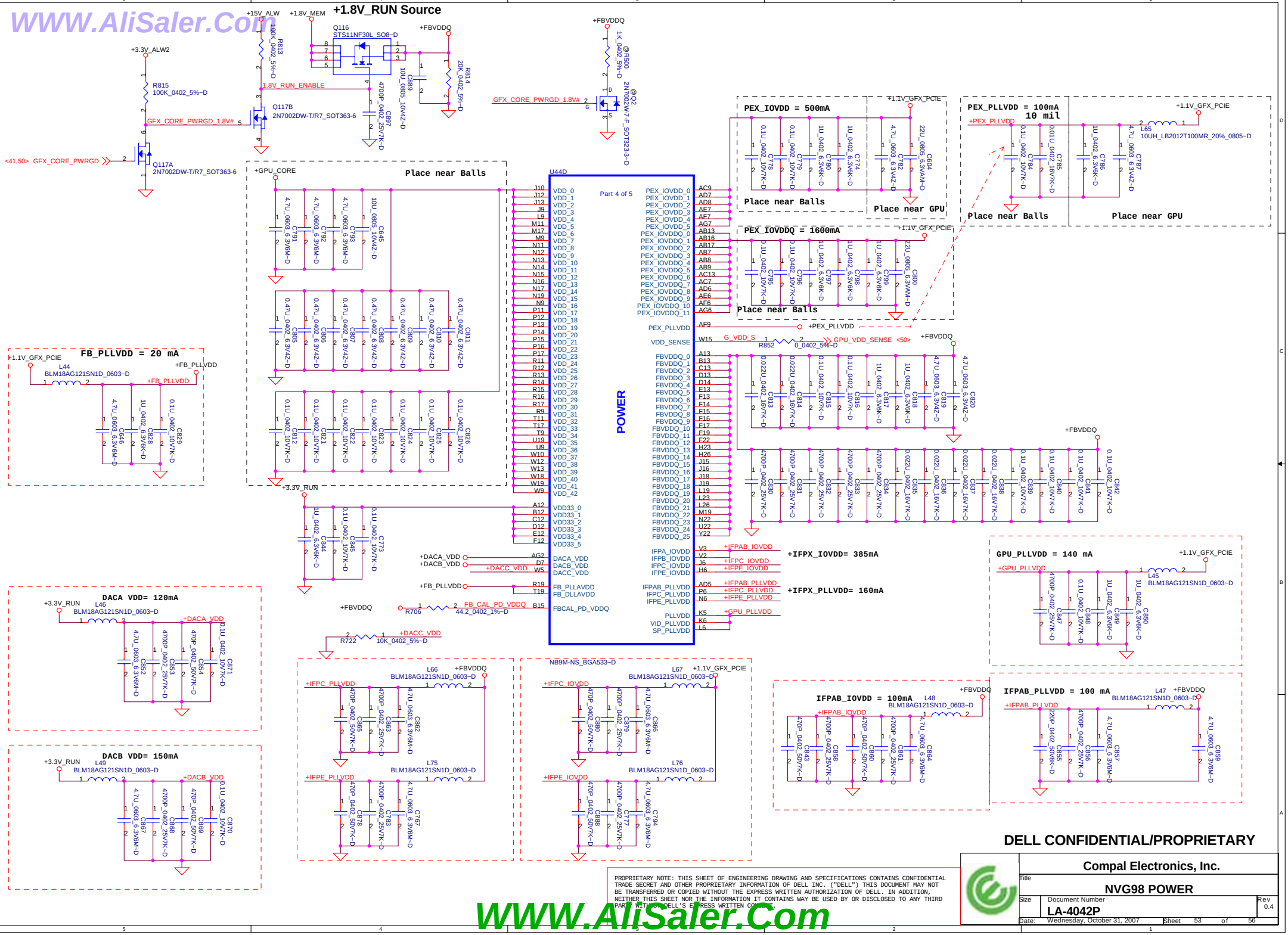

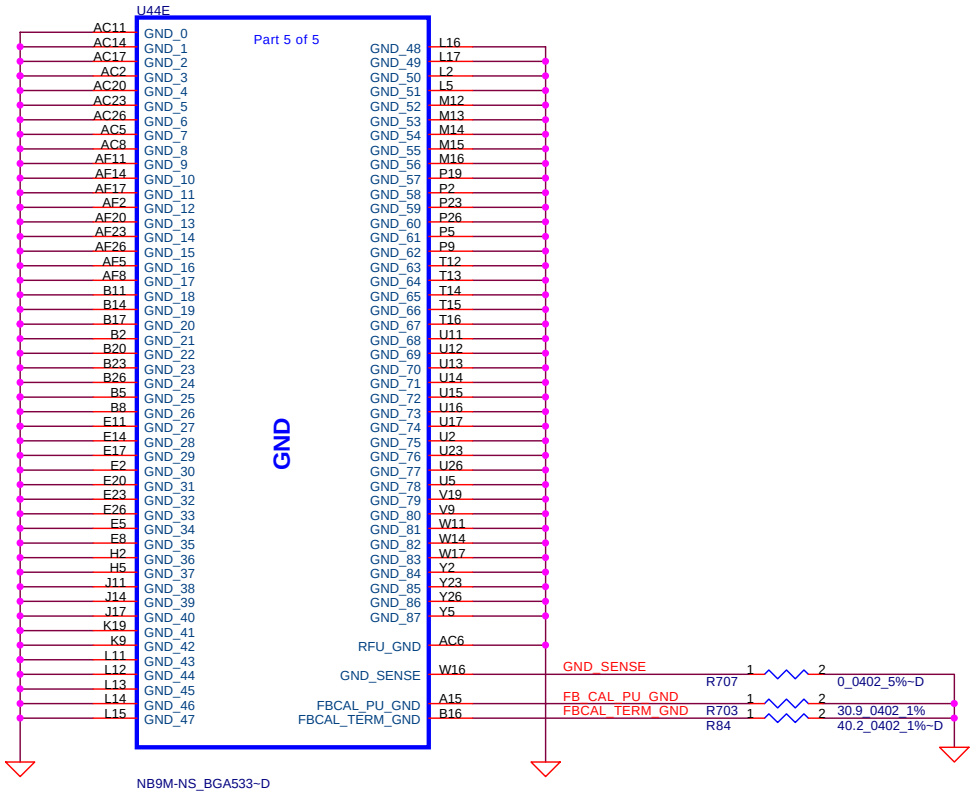

Compal Electronics, Inc.

Title: NVG98 GND

Size | Document Number: LA-4042P | Rev: 0.4

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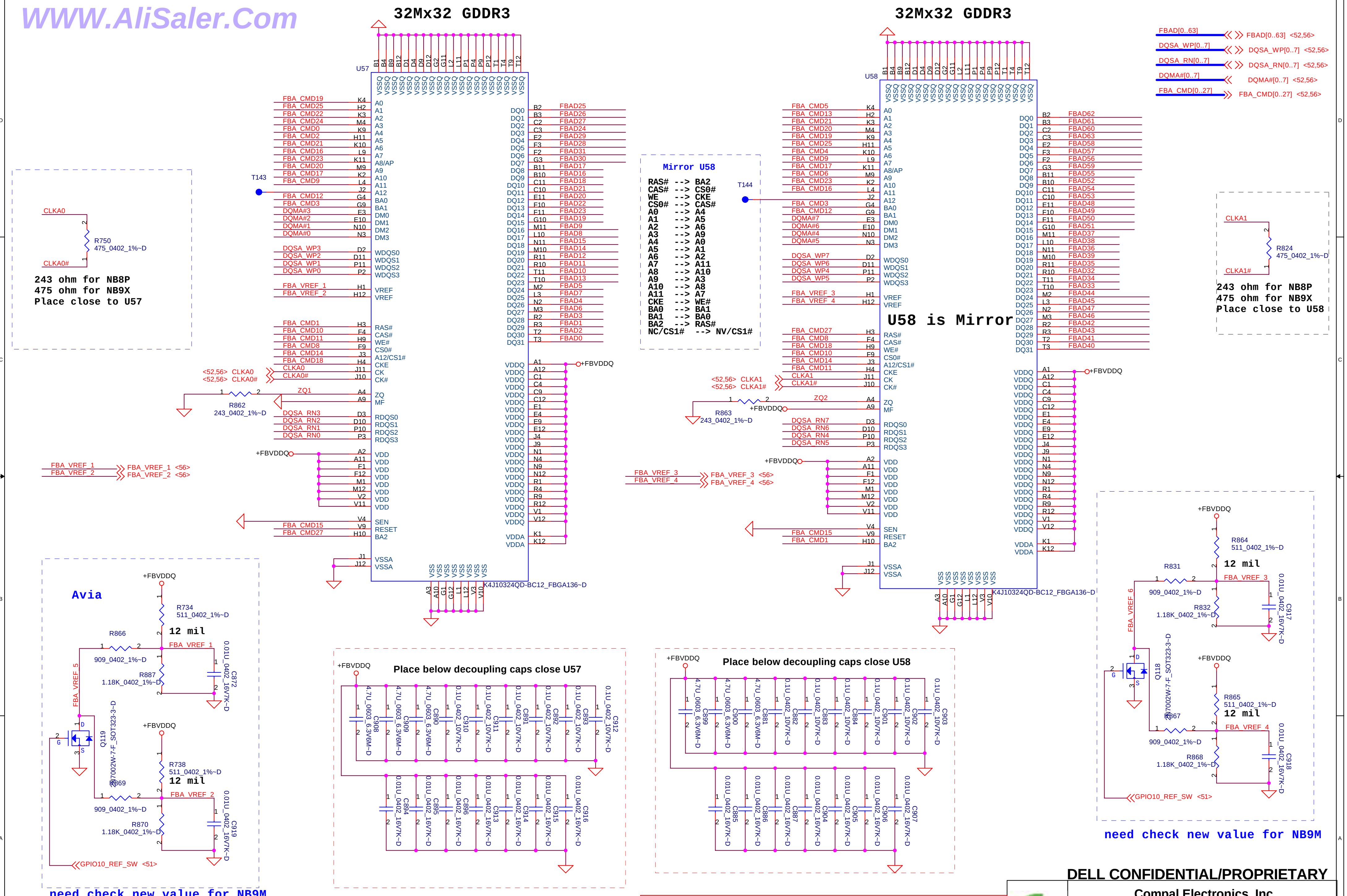

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Title	NVG98 External GDDR2-A	
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32Mx32 GDDR3

U59

Mirror U59

RAS# --> BA2
CAS# --> CS0#
WE --> CKE
CS0# --> CAS#
A0 --> A4
A1 --> A5
A2 --> A6
A3 --> A9
A4 --> A0
A5 --> A1
A6 --> A2
A7 --> A11
A8 --> A10
A9 --> A3
A10 --> A8
A11 --> A7
CKE --> WE#
BA0 --> BA1
BA1 --> BA0
BA2 --> RAS#
NC/CS1# --> NV/CS1#

U59 is Mirror

T40

FBA_CMD0 FBA_CMD2 FBA_CMD21 FBA_CMD20 FBA_CMD19 FBA_CMD25 FBA_CMD22 FBA_CMD9 FBA_CMD17 FBA_CMD24 FBA_CMD23 FBA_CMD16 FBA_CMD3 FBA_CMD12 DQMA#2 DQMA#3 DQMA#0 DQMA#1

DQSA_WP2 DQSA_WP3 DQSA_WP0 DQSA_WP1

FBA_VREF_1 FBA_VREF_2

FBA_CMD27 FBA_CMD7 FBA_CMD18 FBA_CMD10 FBA_CMD14 FBA_CMD11 CLKA0 CLKA0#

ZQ3 R873 243_0402_1%~D +FBVDDQ

DQSA_RN2 DQSA_RN3 DQSA_RN0 DQSA_RN1

FBA_CMD15 FBA_CMD1

FBAD17 FBAD16 FBAD18 FBAD21 FBAD20 FBAD22 FBAD19 FBAD25 FBAD26 FBAD27 FBAD24 FBAD29 FBAD28 FBAD31 FBAD30 FBAD5 FBAD7 FBAD4 FBAD6 FBAD3 FBAD1 FBAD2 FBAD0 FBAD9 FBAD8 FBAD15 FBAD14 FBAD12 FBAD11 FBAD10 FBAD13

+FBVDDQ

K4J10324QD-BC12_FBGA136~D

FBA_VREF_1 <55> FBA_VREF_2 <55>

32Mx32 GDDR3

U60 K4J10324QD-BC12_FBGA136~D

T146

FBA_CMD19 FBA_CMD25 FBA_CMD4 FBA_CMD6 FBA_CMD5 FBA_CMD13 FBA_CMD21 FBA_CMD16 FBA_CMD23 FBA_CMD20 FBA_CMD17 FBA_CMD9 FBA_CMD12 FBA_CMD3 DQMA#6 DQMA#7 DQMA#5 DQMA#4

DQSA_WP6 DQSA_WP7 DQSA_WP5 DQSA_WP4

FBA_VREF_3 FBA_VREF_4

FBA_CMD1 FBA_CMD10 FBA_CMD11 FBA_CMD7 FBA_CMD14 FBA_CMD18 CLKA1 CLKA1#

ZQ4 R874 243_0402_1%~D

DQSA_RN6 DQSA_RN7 DQSA_RN5 DQSA_RN4

FBA_CMD15 FBA_CMD27

FBAD55 FBAD52 FBAD54 FBAD53 FBAD48 FBAD49 FBAD50 FBAD51 FBAD62 FBAD61 FBAD60 FBAD63 FBAD58 FBAD57 FBAD56 FBAD59 FBAD44 FBAD45 FBAD47 FBAD46 FBAD42 FBAD43 FBAD41 FBAD40 FBAD37 FBAD38 FBAD36 FBAD39 FBAD35 FBAD32 FBAD34 FBAD33

+FBVDDQ

FBA_VREF_3 <55> FBA_VREF_4 <55>

FBAD[0..63] <52,55>
DQSA_WP[0..7] <52,55>
DQSA_RN[0..7] <52,55>
DQMA#[0..7] <52,55>
FBA_CMD[0..27] <52,55>

Place below decoupling caps close U48

+FBVDDQ

4.7U_0603_6.3V6M~D C960 C961 C942 C943 C944 C945 C962 C963 C964

0.01U_0402_16V7K~D C946 C947 C948 C965 C966 C967 C968

0.1U_0402_10V7K~D

Place below decoupling caps close U49

+FBVDDQ

4.7U_0603_6.3V6M~D C969 C970 C951 C952 C953 C971 C972 C954 C973

0.01U_0402_16V7K~D C955 C956 C957 C974 C975 C976 C977

0.1U_0402_10V7K~D

Compal Electronics, Inc.

Title: NVG98 External GDDR2-B

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