

Compal confidential

JBK00 LA-4092P Schematics Document

Mobile AMD S1G2 CPU with ATI
RX781 & SB700 core logic with M82-S

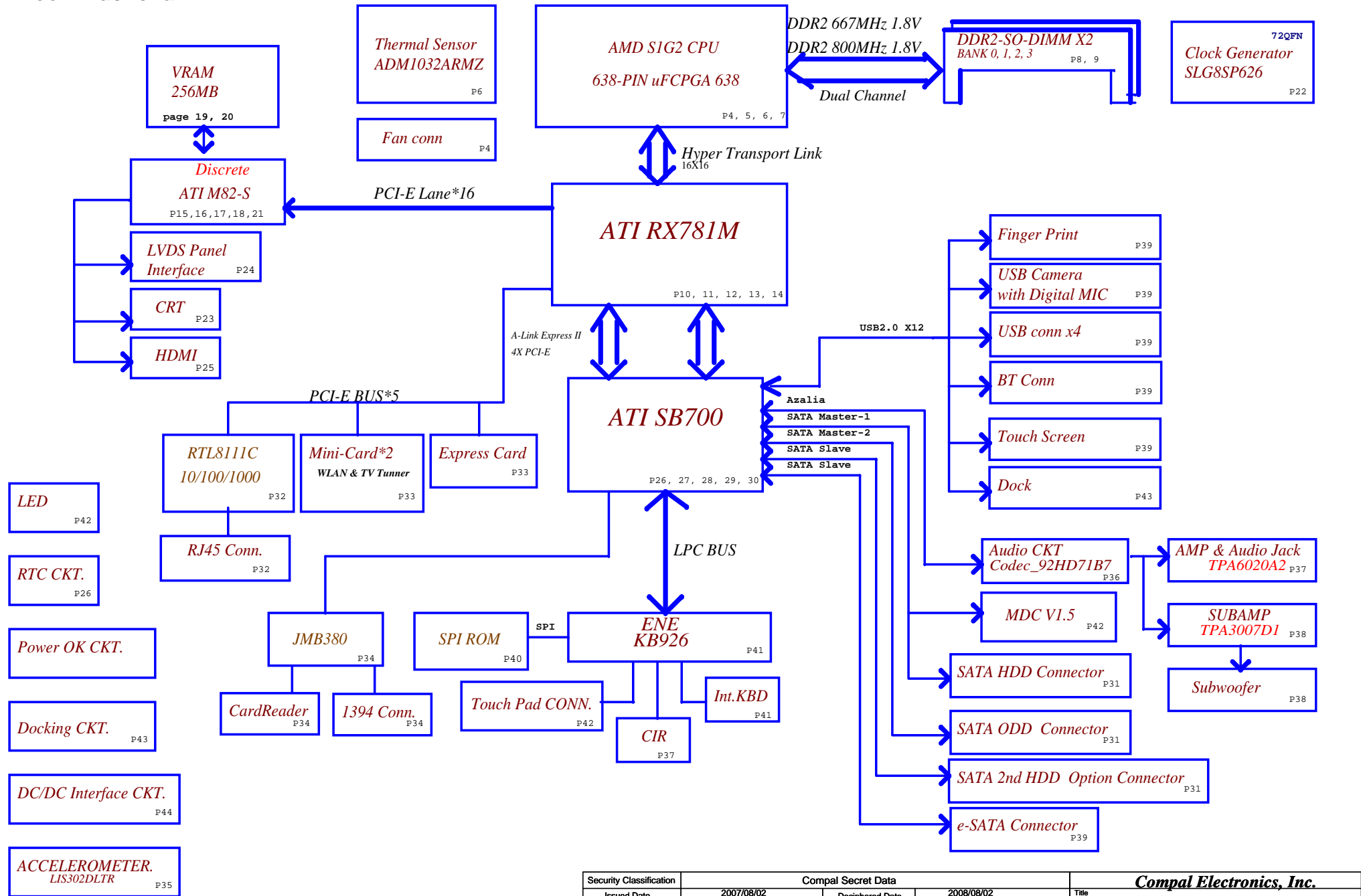
2008-02-20

REV:0.4

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| | | | | Date: | Thursday, February 21, 2008 |
| | | | | Sheet | 1 of 53 |

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Consumer AMD UMA/DISCRETE 17"



| | | | | | | |
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Voltage Rails

| power plane State | +B +3VL +5VL | +5VALW +3VALW +1.2VALW +3V_LAN | +1.8V +0.9V | +5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1 |
|--------------------------------|--------------------|---|----------------|---|
| S0 | O | O | O | O |
| S1 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC | O | O | X | X |
| S5 S4/ Battery only | O | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X |

O MEANS ON X MEANS OFF

I2C / SMBUS ADDRESSING

| DEVICE | HEX | ADDRESS |
|------------------------|-----|-----------------|
| DDR SO-DIMM 0 | A0 | 1 0 1 0 0 0 0 0 |
| DDR SO-DIMM 1 | A4 | 1 0 1 0 0 1 0 0 |
| CLOCK GENERATOR (EXT.) | D2 | 1 1 0 1 0 0 1 0 |
| ACCELEROMETER | 3A | 0 0 1 1 1 0 1 0 |

EC SM Bus1 address

EC SM Bus2 address

| Device | HEX | Address |
|-------------------|-----|-------------|
| Smart Battery | 16H | 0001 011X b |
| 24C16 | A0H | 1010 000X b |
| CPU SIC interface | 98H | 1001 100X b |

| Device | HEX | Address |
|---------------|-----|-------------|
| ADI1032-2 CPU | 9AH | 1001 101X b |
| ADI1032-1 VGA | 98H | 1001 100X b |

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

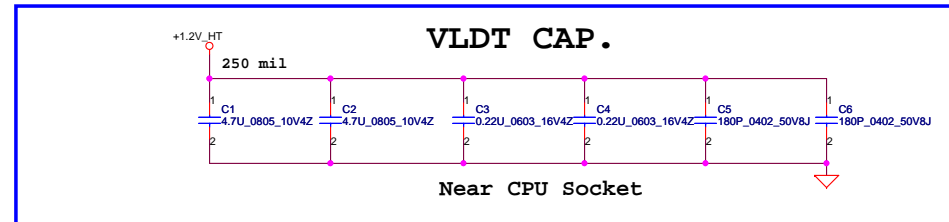
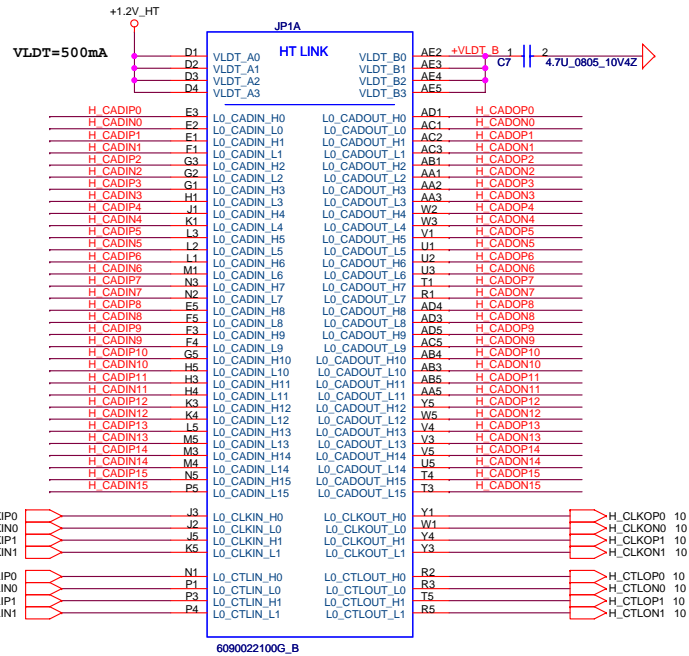
DEBUG@ : means just reserve for debug.

 Layout Notes

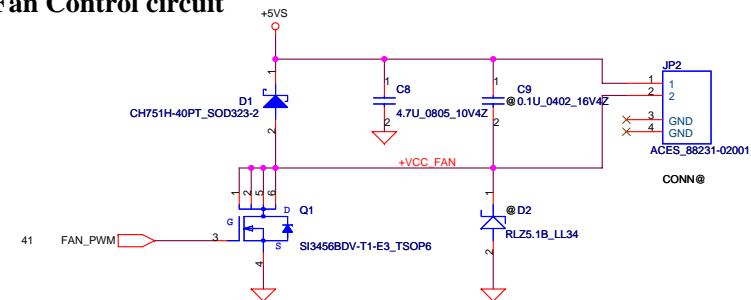
SMBUS Control Table

| | SOURCE | INVERTER | BATT | SERIAL EEPROM | THERMAL SENSOR CPU & ADM1032 | SODIMM I / II | CLK CHIP | MINI CARD Slot 2 | LCD | HDMI | G-Sensor |
|--------------------------|--------|----------|------|---------------|------------------------------|---------------|----------|------------------|-----|------|----------|
| SMB_EC_CK1 SMB_EC_DA1 | KB926 | X | V | V | X | X | X | X | X | X | X |
| SMB_EC_CK2 SMB_EC_DA2 | KB926 | X | X | X | V | X | X | X | X | X | X |
| I2C_CLK I2C_DATA | RS780M | X | X | X | X | X | X | X | V | X | X |
| DDC_CLK0 DDC_DATA0 | RS780M | X | X | X | X | X | X | X | X | V | X |
| DDC_CLK1 DDC_DATA1 | RS780M | X | X | X | X | X | X | X | X | X | X |
| SCL0 SDA0 | SB700 | X | X | X | X | V | V | X | X | X | V |
| SCL1 SDA1 | SB700 | X | X | X | X | X | X | V | X | X | X |
| SCL2 SDA2 | SB700 | X | X | X | X | X | X | X | X | X | X |
| SCL3 SDA3 | SB700 | X | X | X | X | X | X | X | X | X | X |

| | | | | | | |
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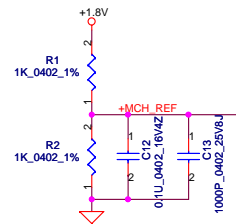


PWM Fan Control circuit

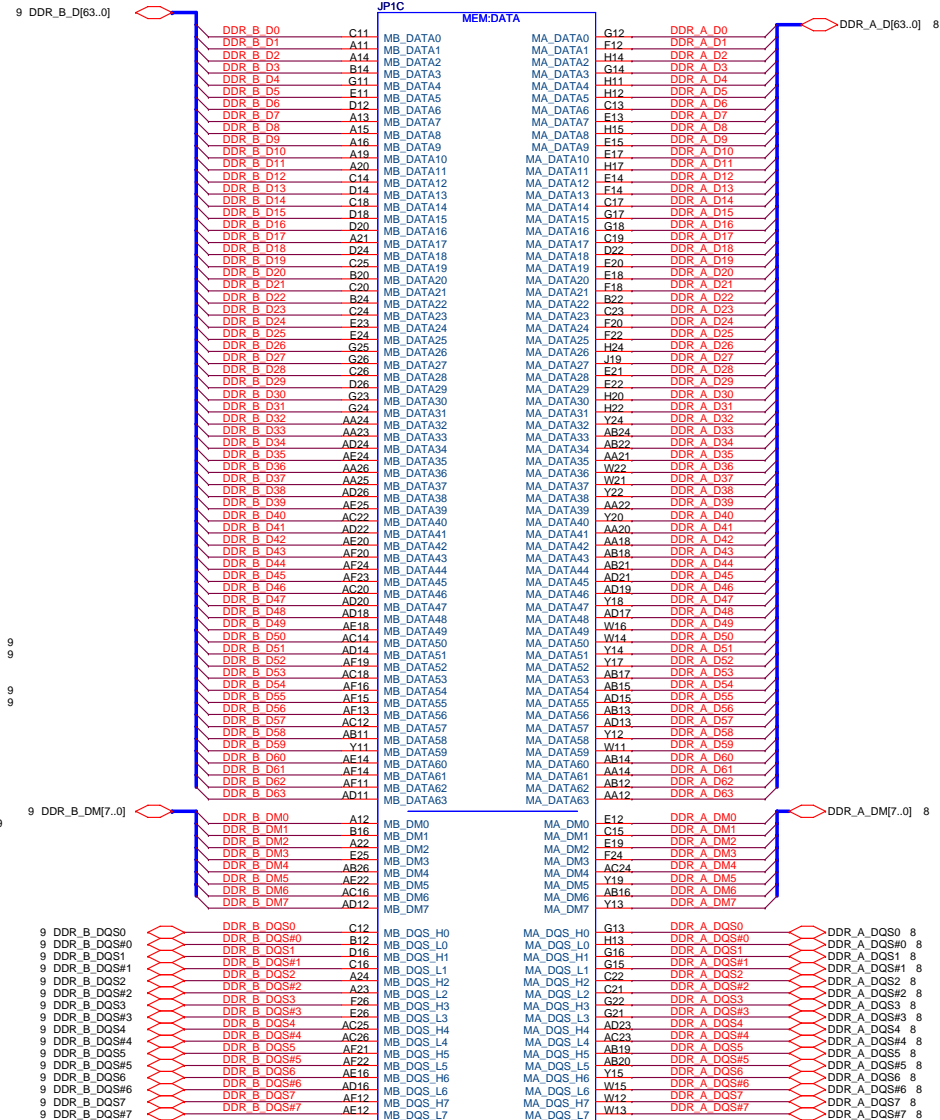
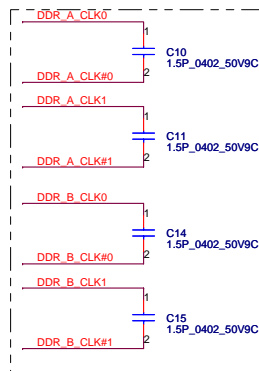


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| Sheet | | 4 | | of 53 |

Processor DDR2 Memory Interface

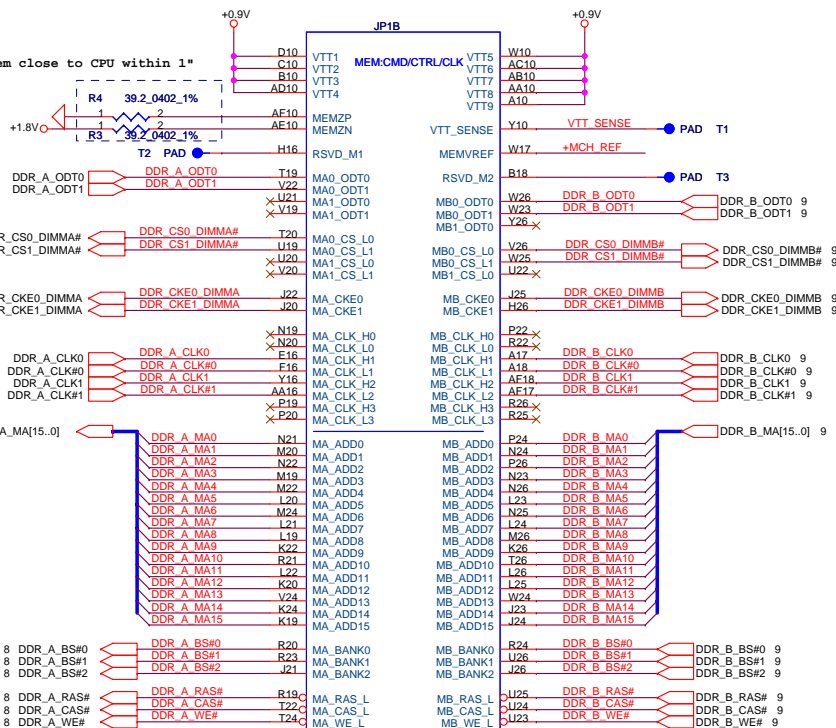


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

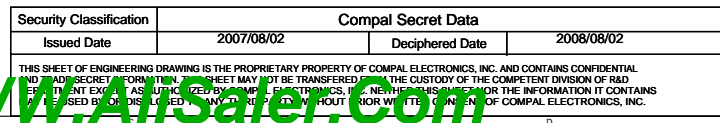


6090022100G

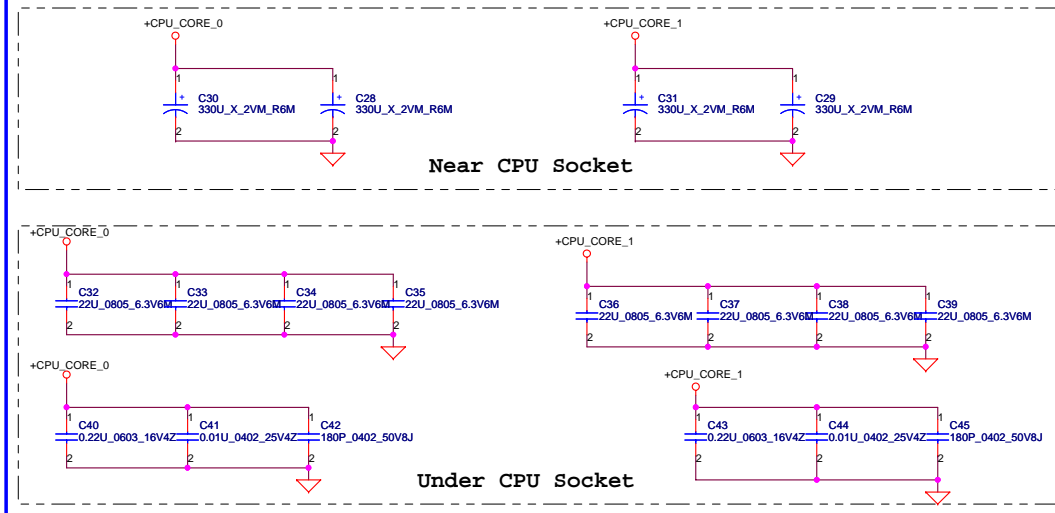
Place them close to CPU within 1'



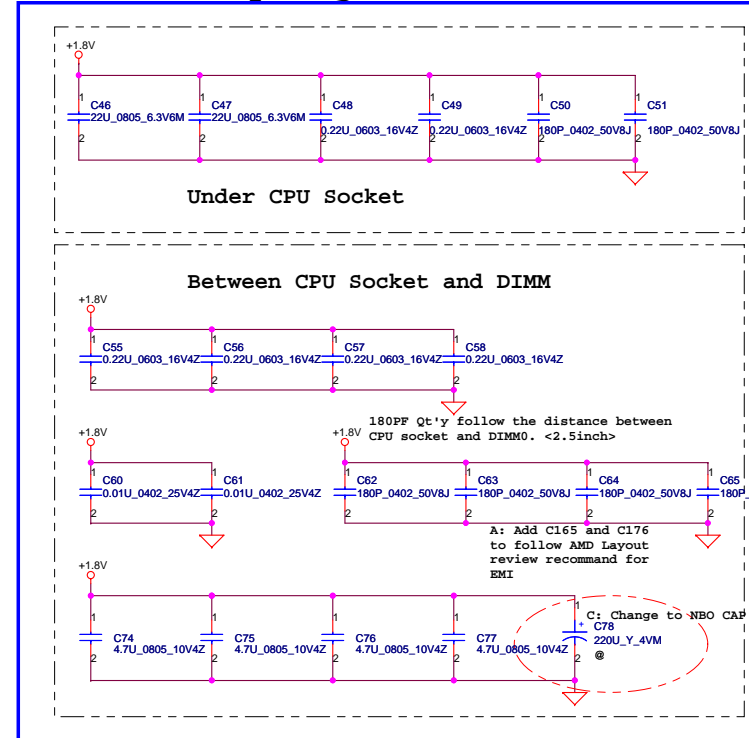
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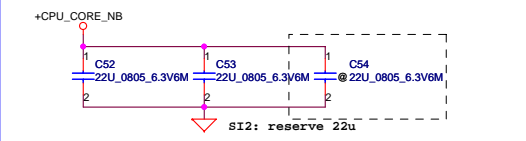
VDD(+CPU_CORE) decoupling.



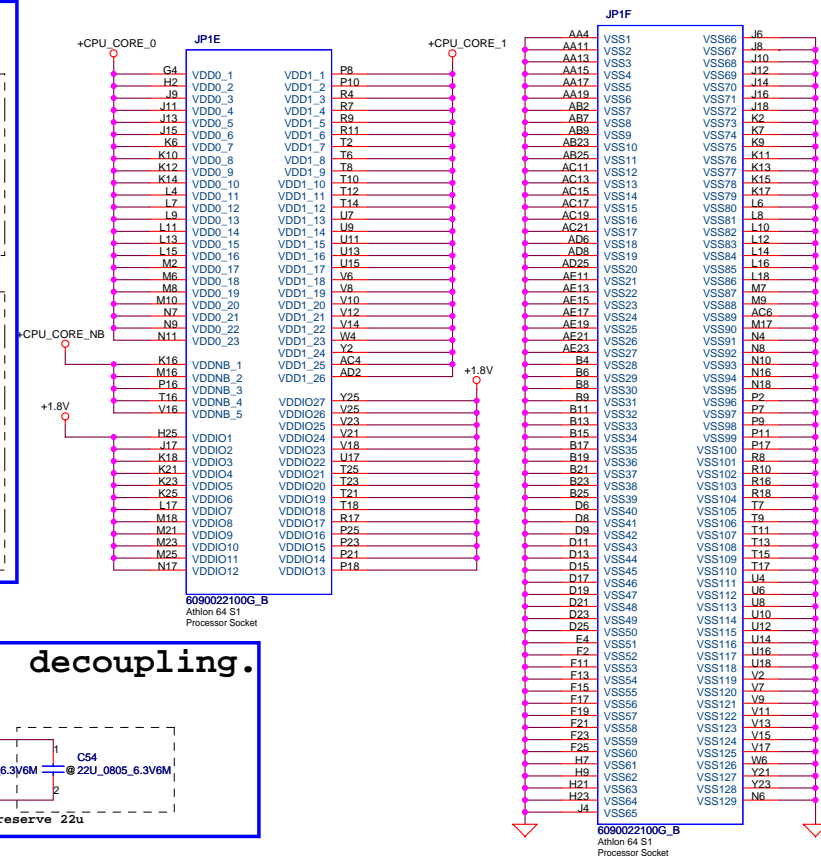
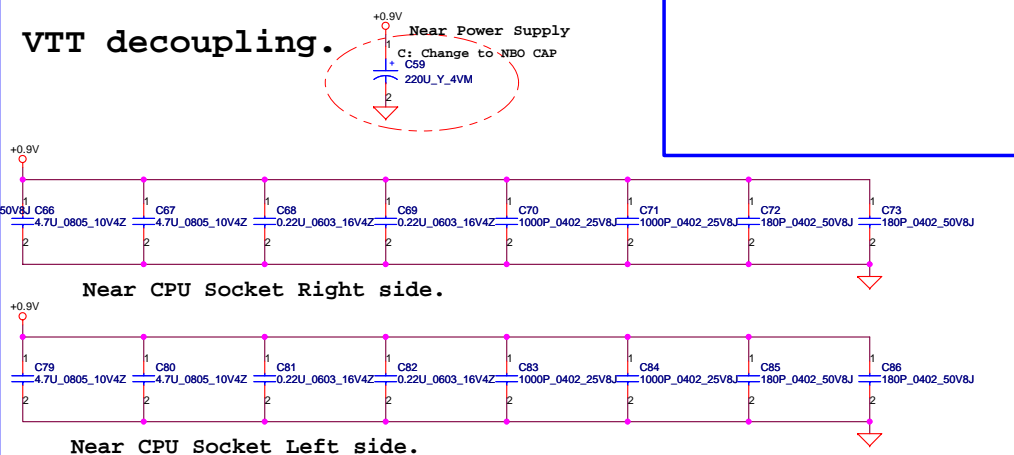
VDDIO decoupling.



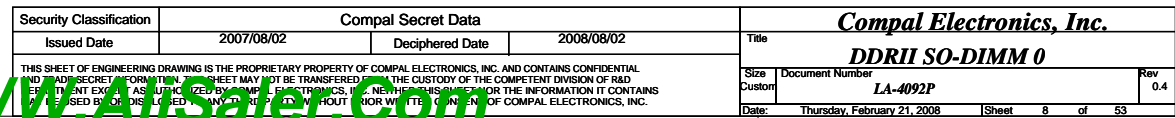
+CPU_CORE_NB decoupling.

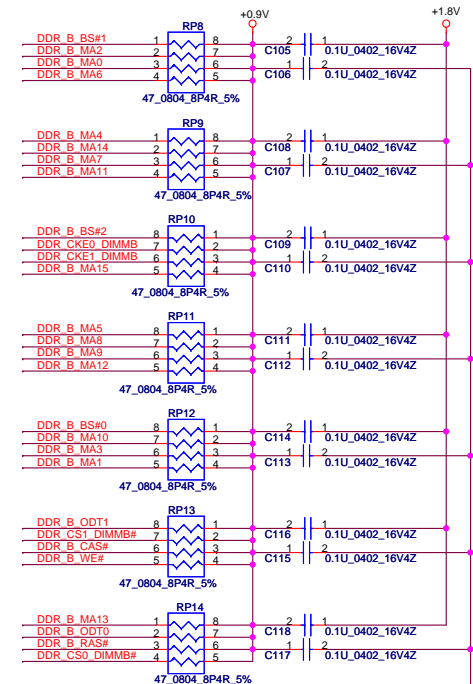



VTT decoupling.



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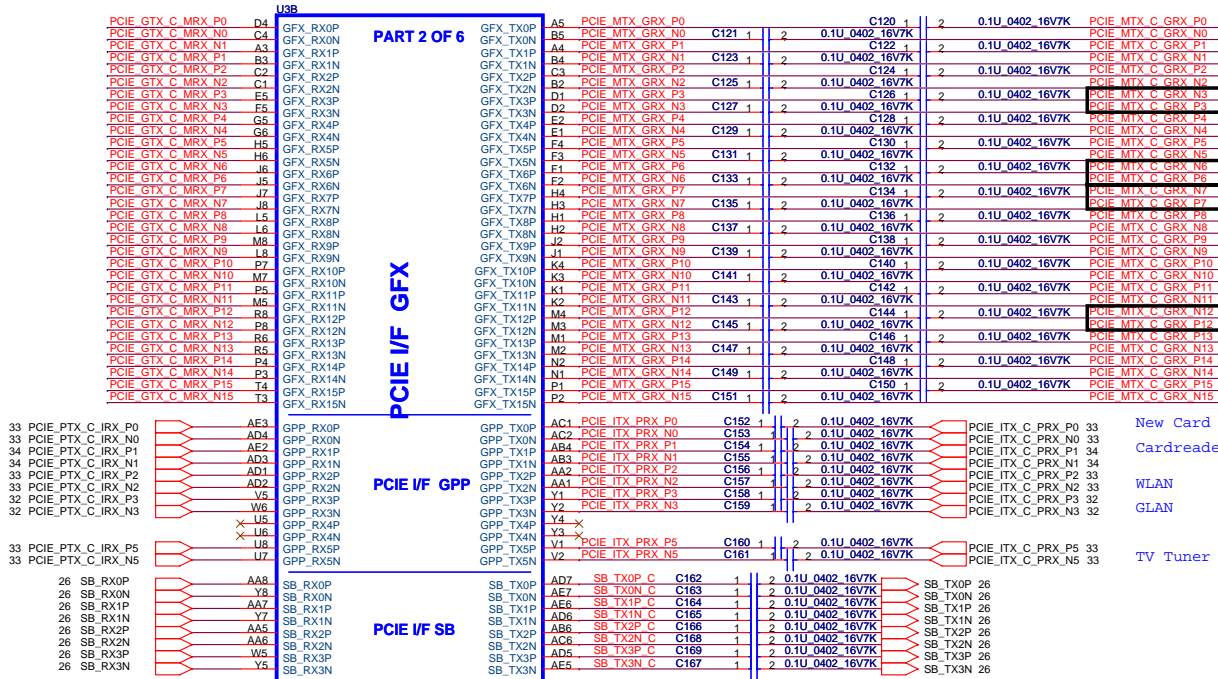




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15 PCIE_GTX_C_MRX_P0[0..15] PCIE GTX_C_MRX_P0[0..15]
15 PCIE_GTX_C_MRX_N0[0..15] PCIE GTX_C_MRX_N0[0..15]

PCIE_MTX_C_GRX_P0[0..15] PCIE_MTX_C_GRX_P0[0..15]
PCIE_MTX_C_GRX_N0[0..15] PCIE_MTX_C_GRX_N0[0..15]



RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

| | |
|-----|--|
| DP0 | GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0 |
| DP1 | GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1 |

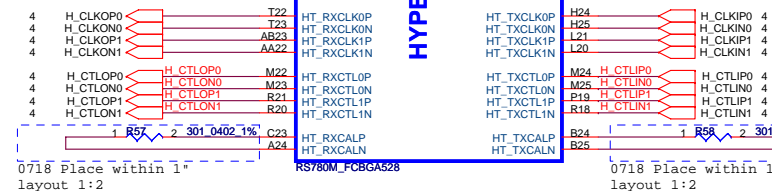
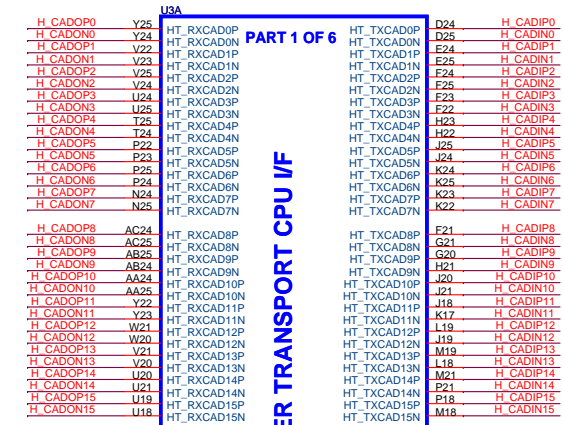
Polarity inversion

Polarity inversion

Polarity inversion

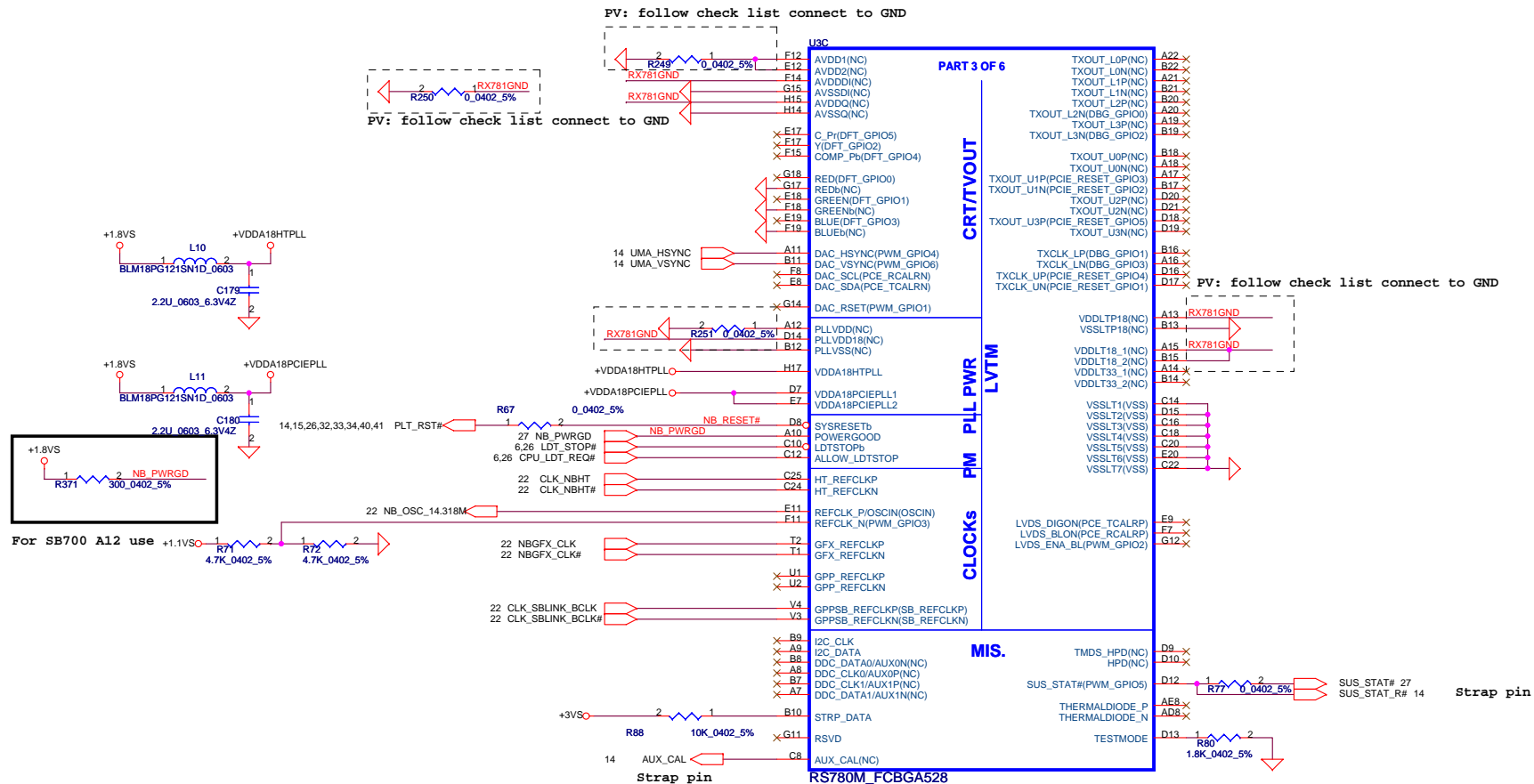
New Card
Cardreader
WLAN
GLAN
TV Tuner

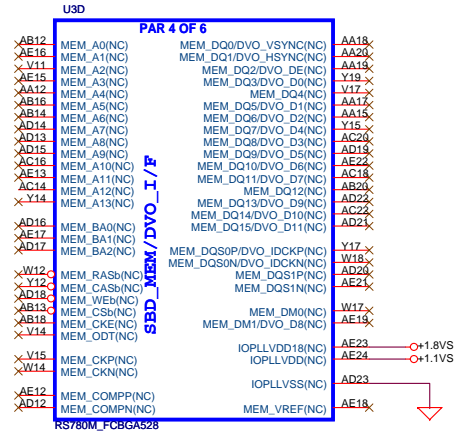
4 H_CADOP[0..15] H_CADOP[0..15]
4 H_CADIN[0..15] H_CADIN[0..15]

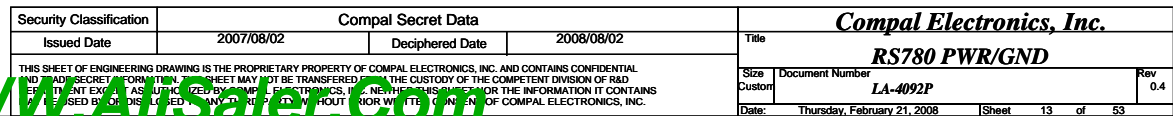


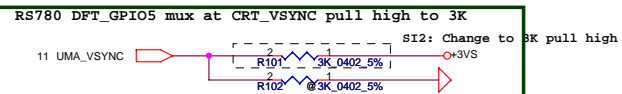
NEED CHECK R68 & R69 WITH AMD

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| Custom | LA-4092P | Sheet | | 10 of 53 |









DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO.

1 : Enable (RX780, RS780)

0 : Disable (RX780, RS780)

PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

000 : 00001

001 : 00010

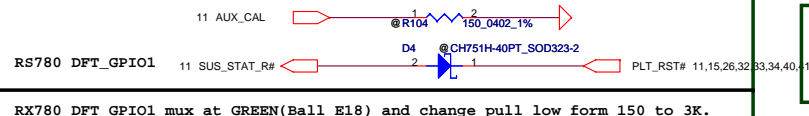
010 : 01011

011 : 00100

100 : 01010

101 : 01100

111 : 01011



DFT_GPIO1: LOAD_EEPROM_STRAPS

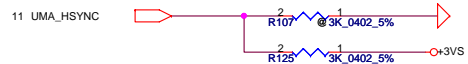
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

RS780 use HSYNC to enable SIDE PORT (internal pull high)



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED

RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)

0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS780)

0 : Enable (RS780)

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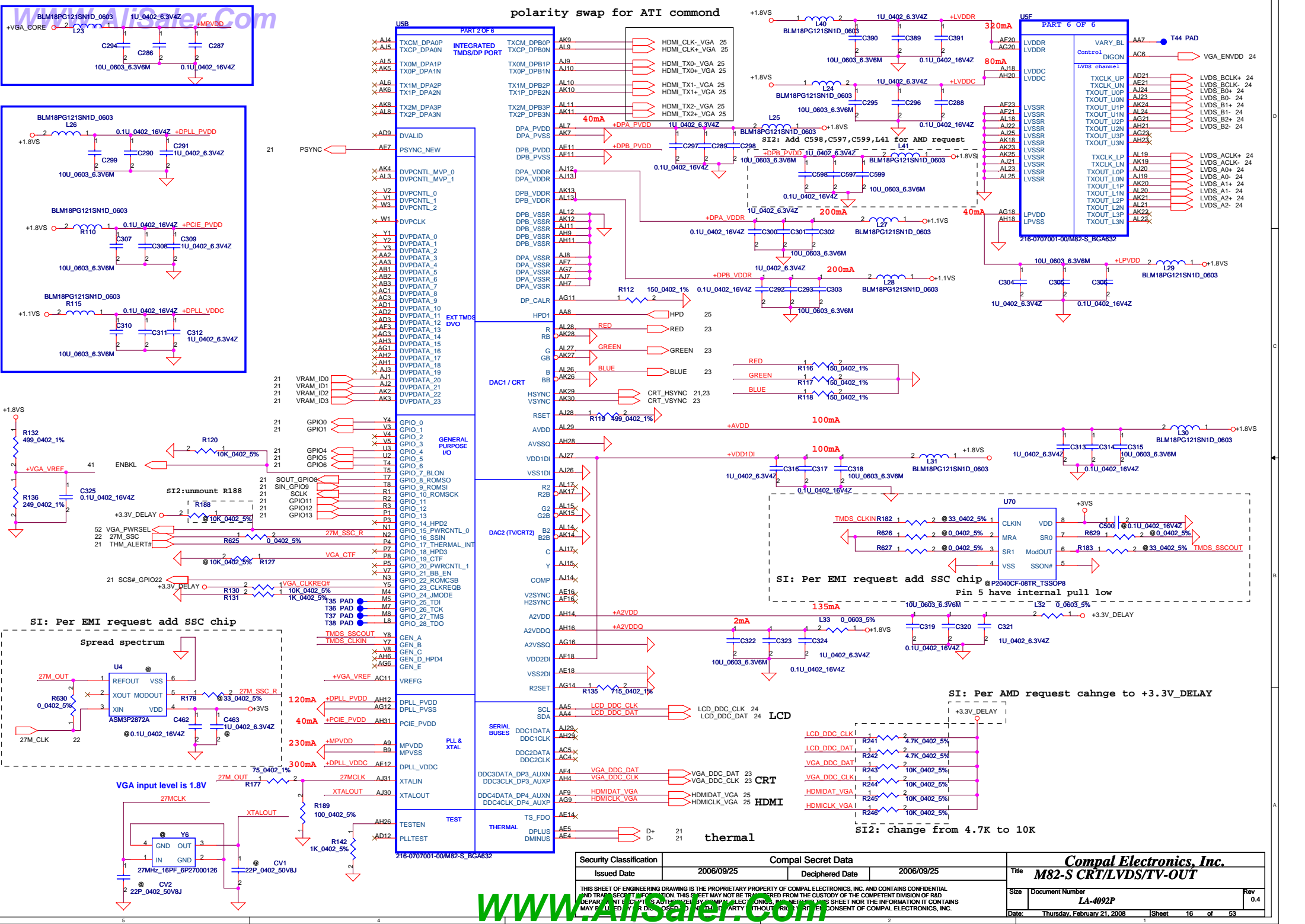
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10 PCIE_MTX_C_GRX_P[0..15] ← PCIE MTX C GRX P[0..15]
10 PCIE_MTX_C_GRX_N[0..15] ← PCIE MTX C GRX N[0..15]

PCIE LANE REVERSAL

PCIE LANE REVERSAL

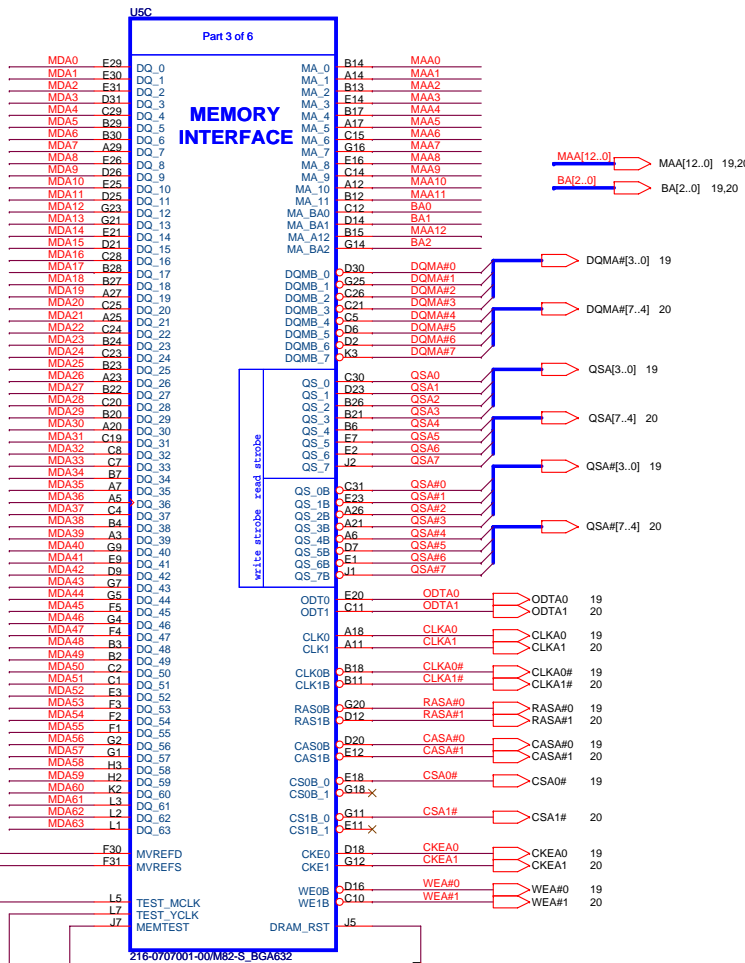


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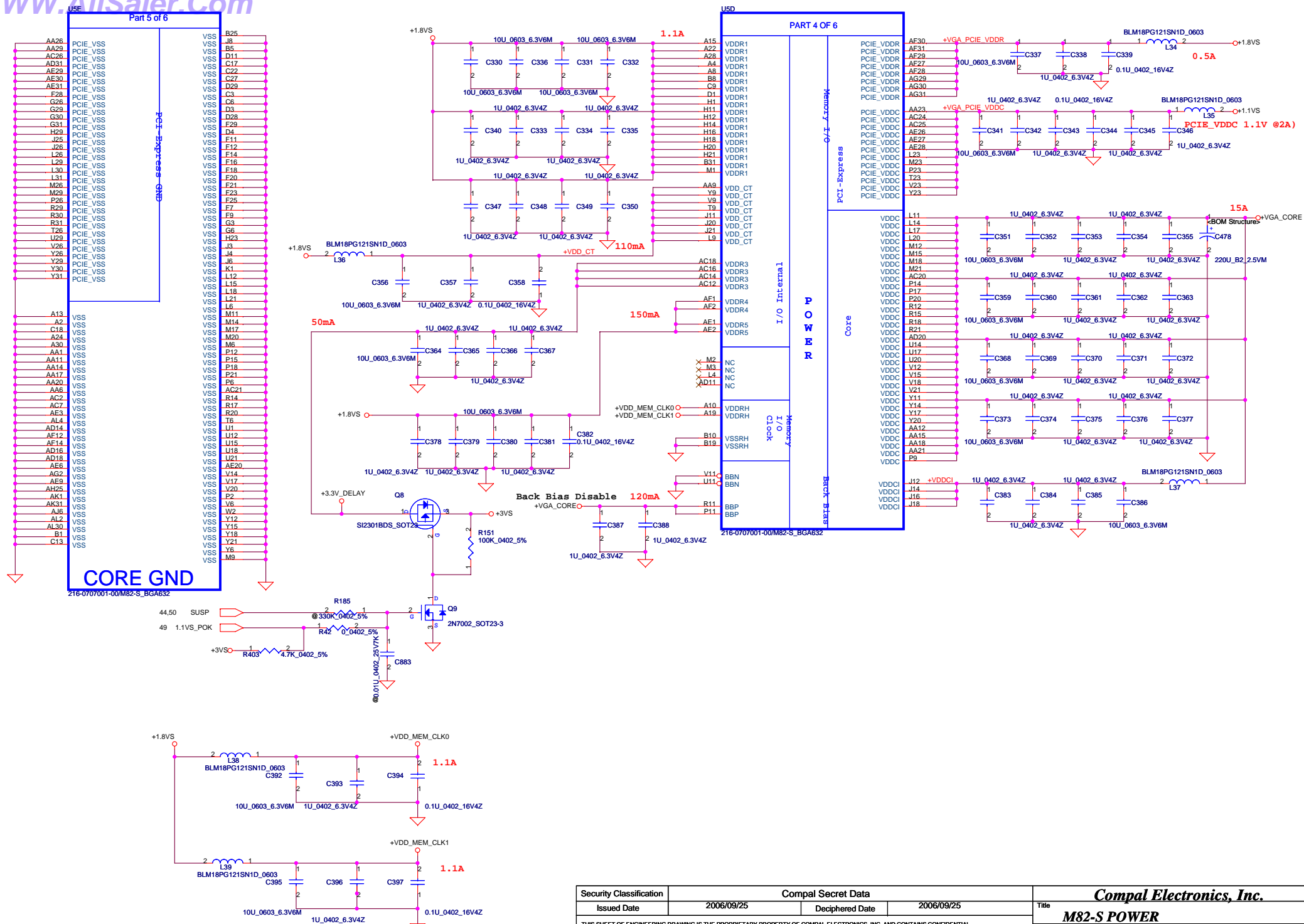


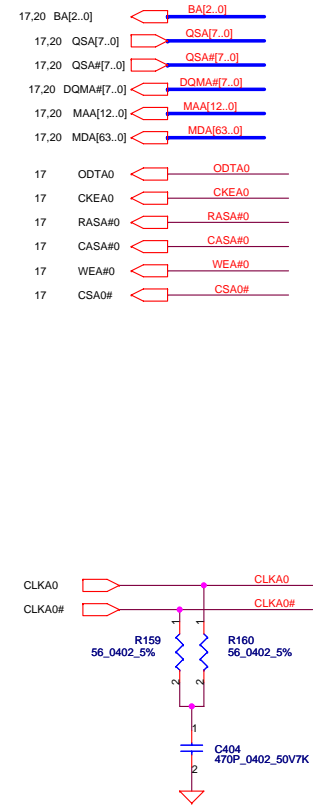
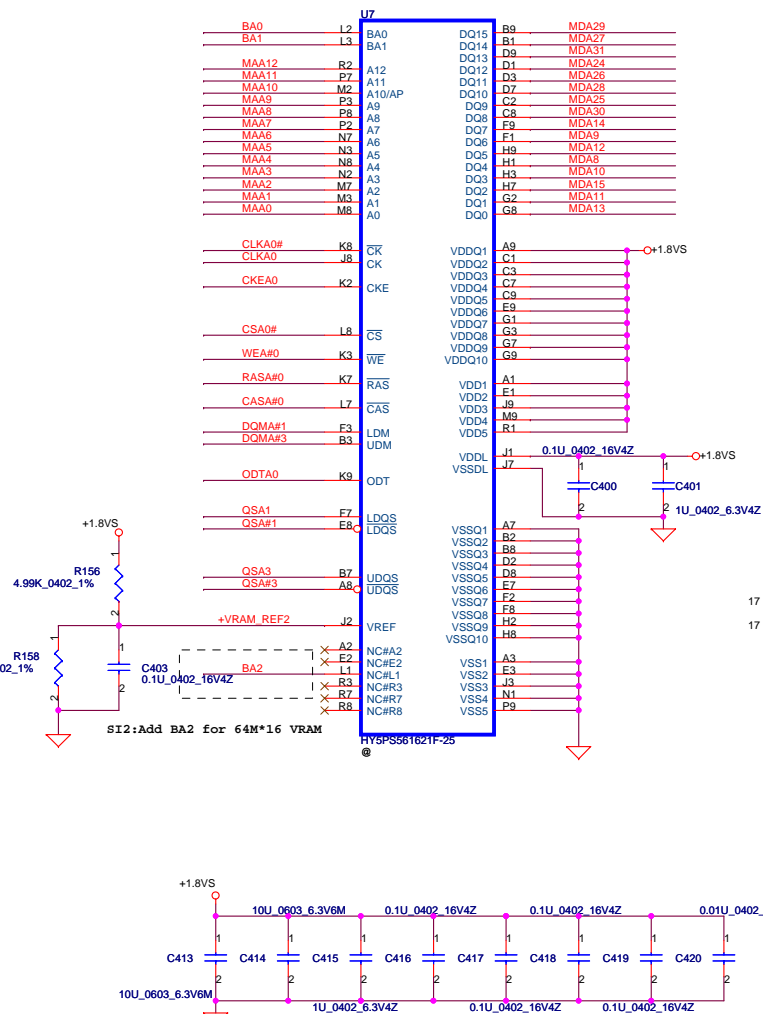
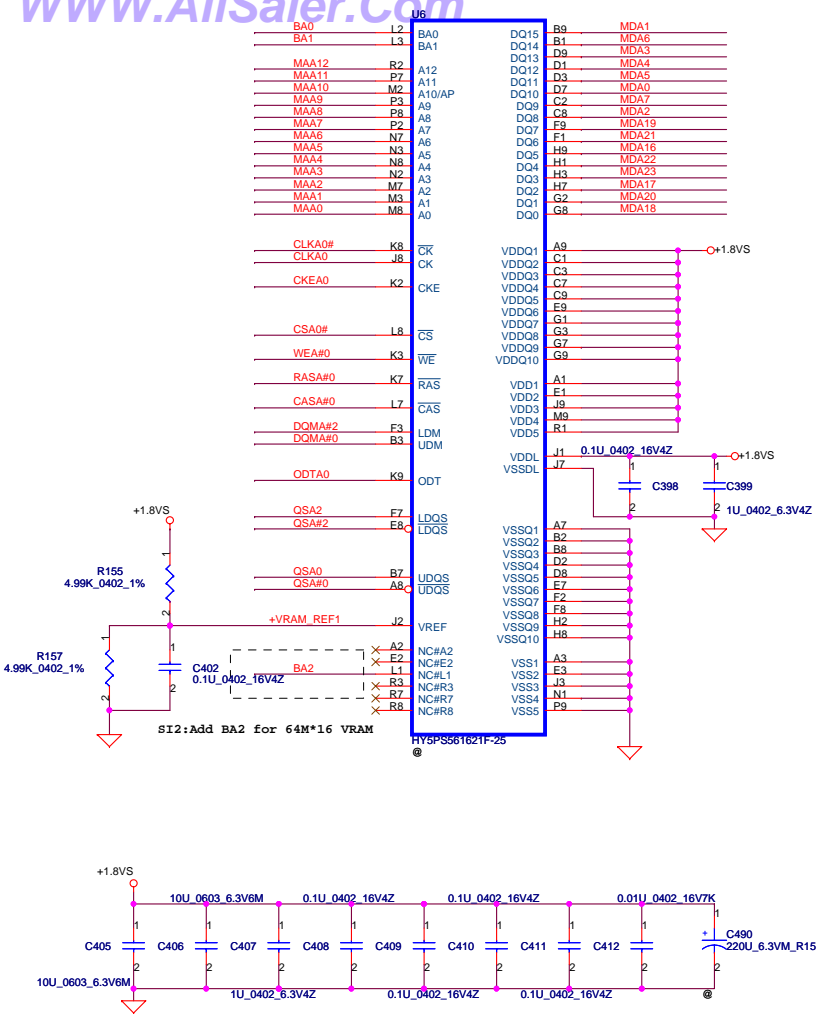
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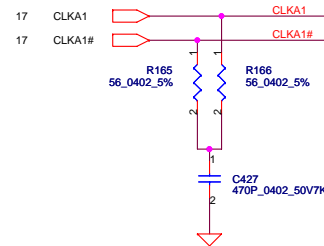
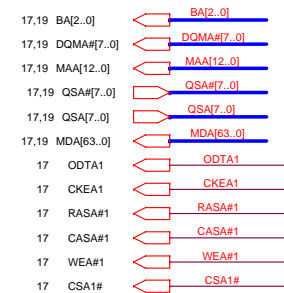
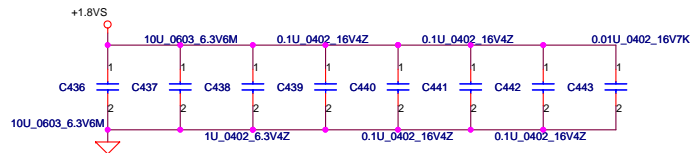
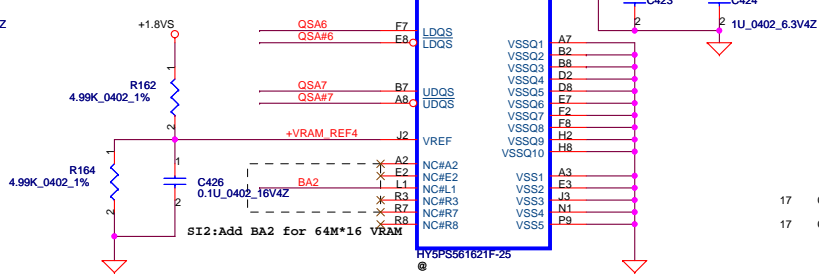
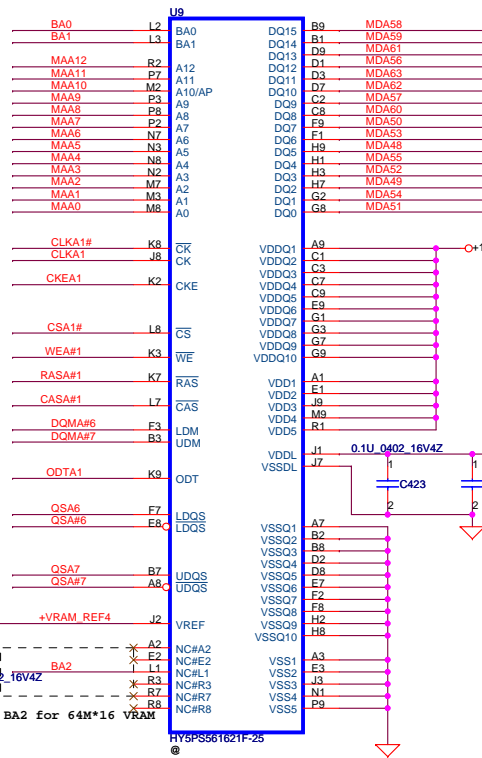
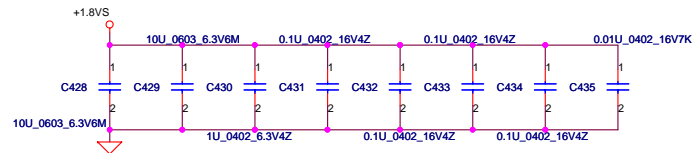
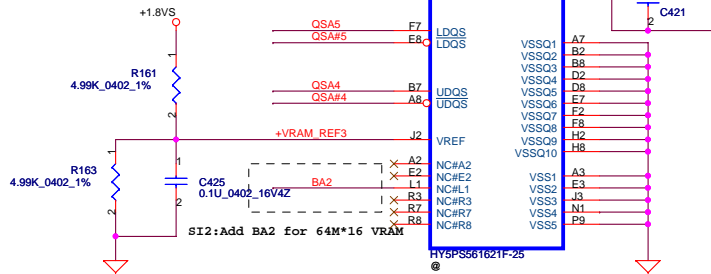
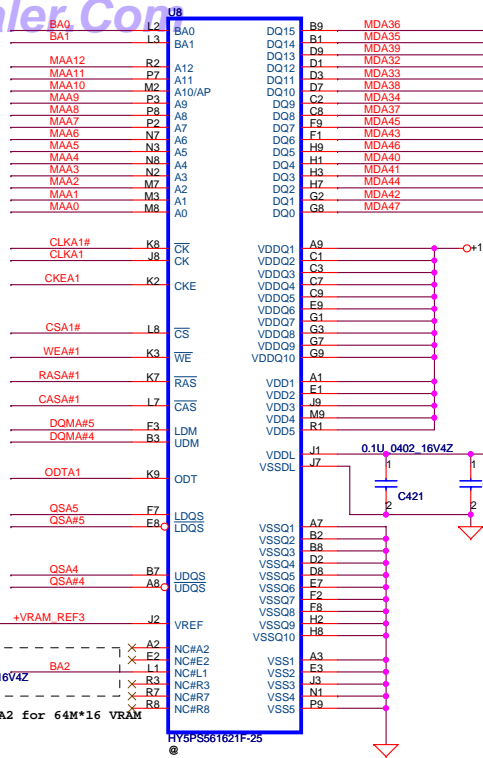
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19 MDA[31..0] MDA[31..0]



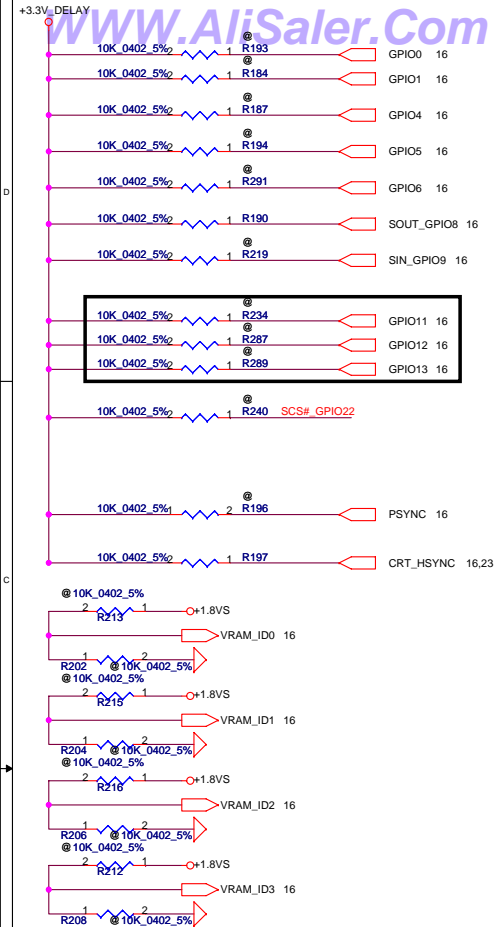
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| | | | | | | | | M82-S MEM | | | |
| Size | | Document Number | | | | | | Rev | | | |
| | | LA-4092P | | | | | | 0.4 | | | |
| Date: | | Thursday, February 21, 2008 | | Sheet | | 17 | | of 53 | | | |



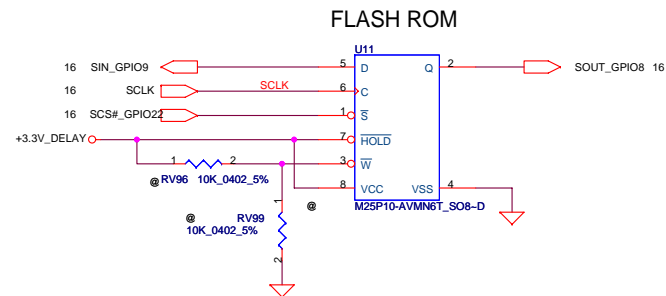
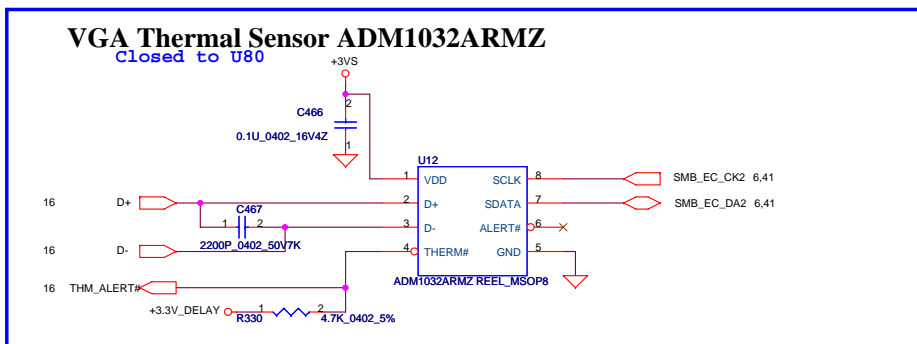




| STRAPS | PIN | DESCRIPTION OF RECOMMENDED SETTING | RECOMMENDED M8X |
|------------------|-----------------------|--|--------------------|
| TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING | 0 |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLES | 0 |
| BIF_DEBUG_ACCESS | GPIO4 | DEBUG SIGNALS MUXED OUT | 0 |
| BIF_GEN2_EN_A | GPIO5 | PCI-E 5.0GT/s or 2.5 GT/s select | 0 |
| DEBUG_I2C_ENABLE | GPIO6 | Internal use only | 0 |
| BIF_AUDIO_EN | GPIO8 | ENABLE HD AUDIO(M8X) | 1 |
| ROMIDCFG[3:0] | GPIO [9,13,12,11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | 0 1 0 1 |
| BIOS_ROM_EN | GPIO_22_ROMCSS | DISABLE EXTERNAL BIOS ROM | 0 |
| | | | |
| | | | |
| BIF_VGA_DIS | PSYNC | VGA ENABLED===0 is enable | 0 |
| BIF_HDMI_EN | HSYNC | HDMI ENABLE | 1 |
| VRAM_ID[3:0] | DVPDATA (23,22,21,20) | | VRAM_ID 3 ,2 ,1 ,0 |
| | | Samsung 64Mx16 1.8V | 0 0 0 0 |
| | | Samsung 32Mx16 1.8V | 0 0 0 1 |
| | | Hynix 64Mx16 1.8V | 0 0 1 0 |
| | | Hynix 32Mx16 1.8V | 0 0 1 1 |
| | | Qimonda 32Mx16 1.8V | 0 1 0 0 |
| | | Qimonda 64Mx16 1.8V | 0 1 0 1 |

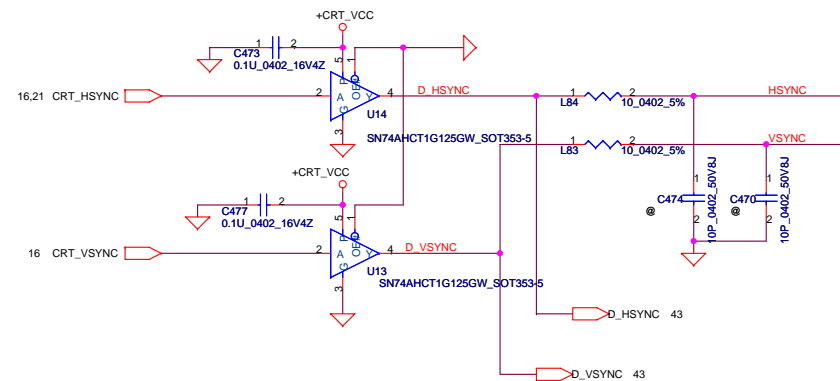
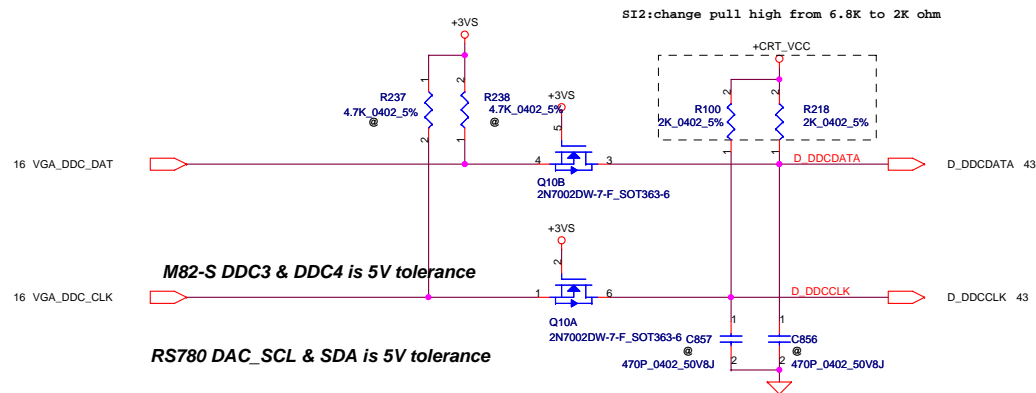
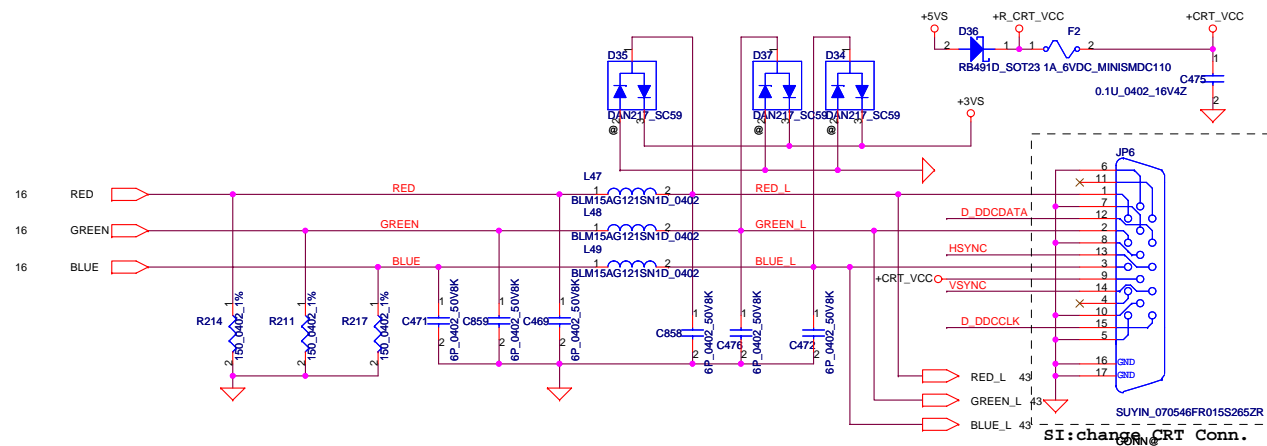


| | | | | | | | | | |
|--|--|--|--|--|--|--|--|--|--|
| <p align="center">ATI RESERVED CONFIGURATION STRAPS</p> <p align="center">ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESE</p> | | | | | | | | | |
| <p align="center">GPIO2 GPIO3 GPIO5 GPIO6 DVALID H2SYNC V2SYNC</p> | | | | | | | | | |
| <p align="center">PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</p> | | | | | | | | | |
| <p align="center">GENERICC GPIO21_BB_EN GPIO_28_TDO</p> | | | | | | | | | |

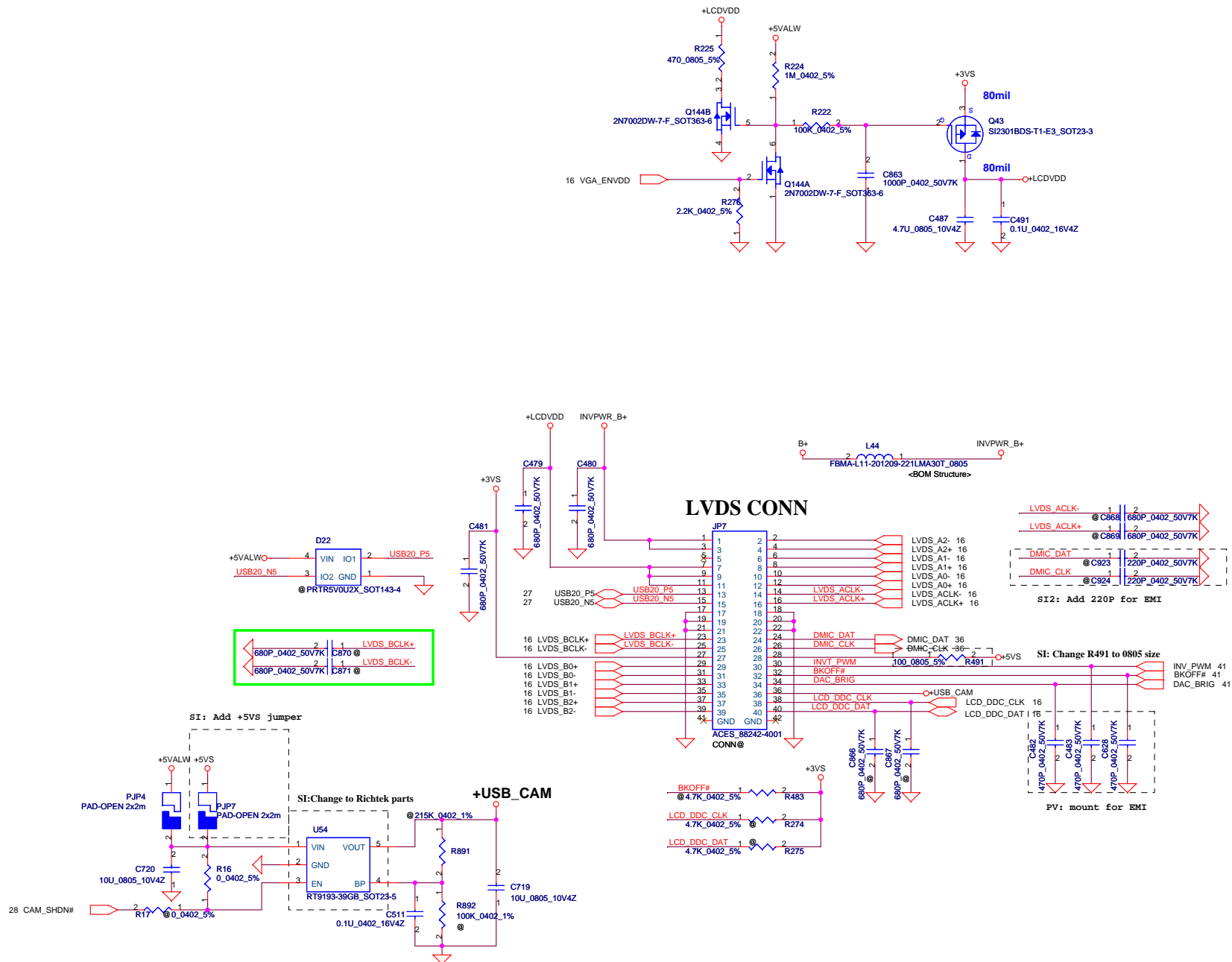


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| Date: Thursday, February 21, 2008 | | | | | | Sheet | | 21 | | of 53 | |

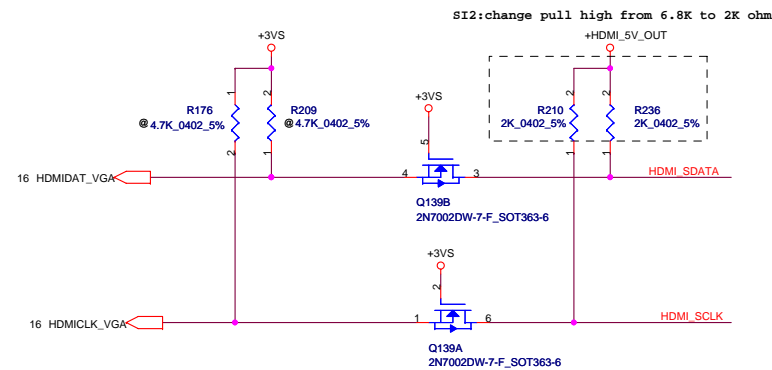
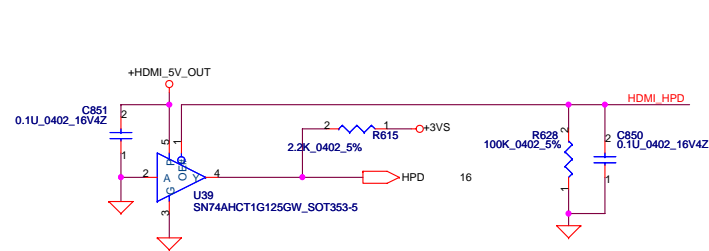
CRT CONNECTOR



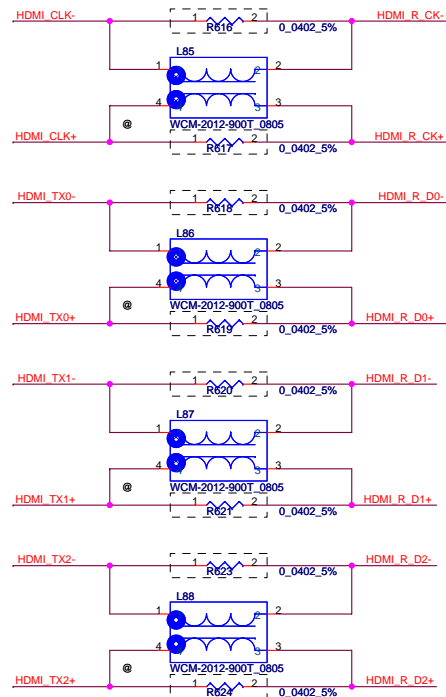
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| Date: | | | | Thursday, February 21, 2008 | | | | Sheet | | | |
| 23 | | | | of | | | | 53 | | | |



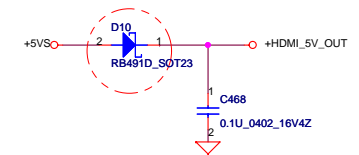
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| Size | Custom | Document Number | LA-4092P | Rev | 0.4 |
| Date: | | Thursday, February 21, 2008 | | Sheet | 24 of 53 |



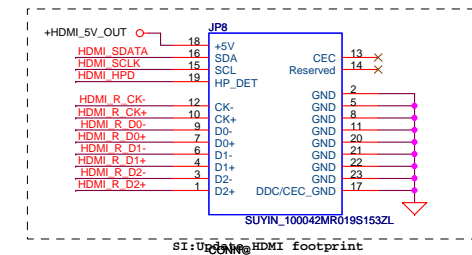
SI:Add R6161-R624 for EMI request



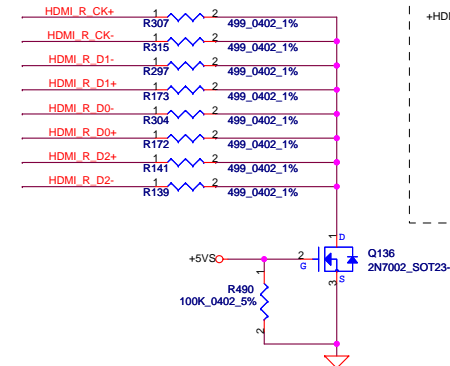
MP:Update D10 to meet HDMI.



HDMI Connector

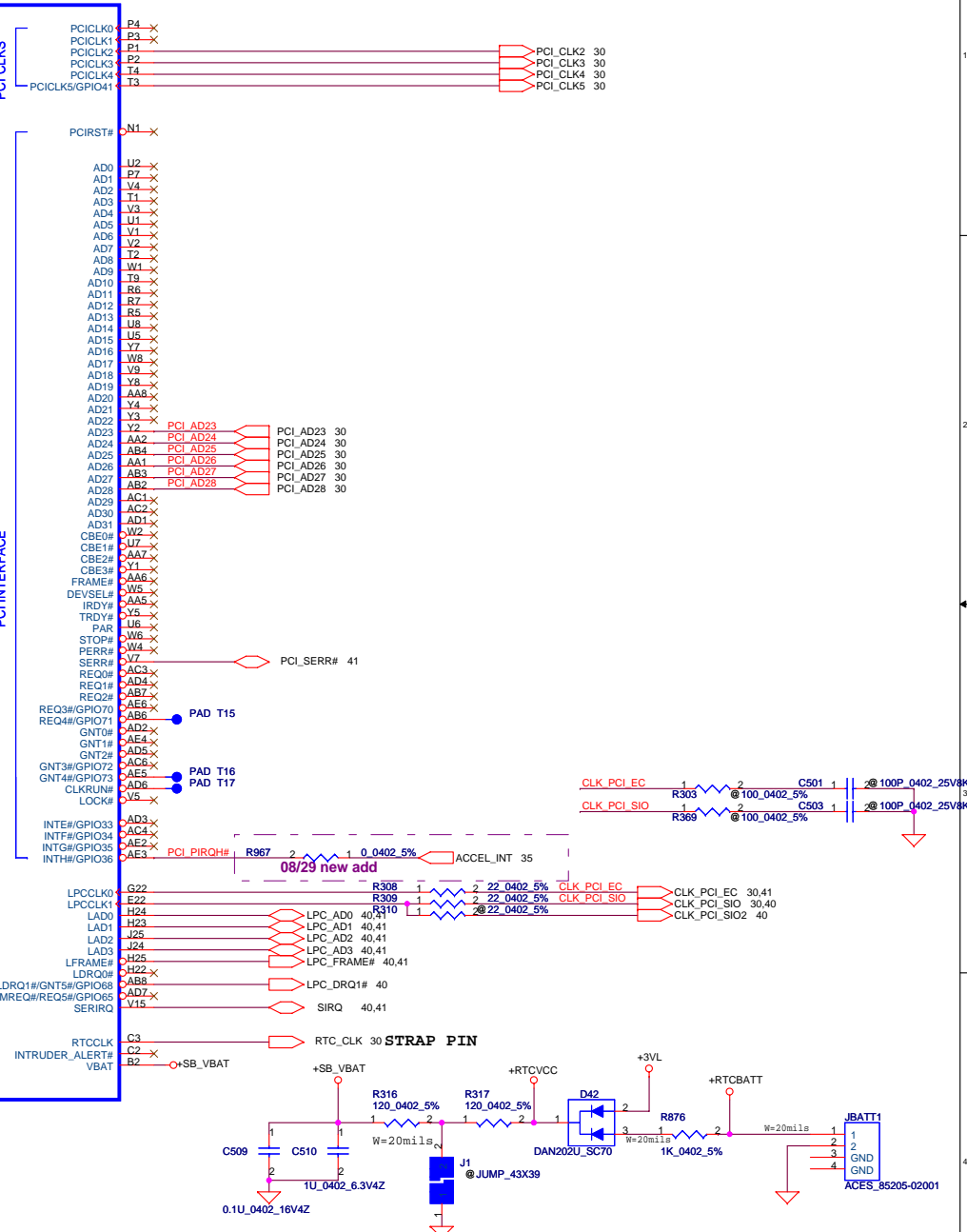
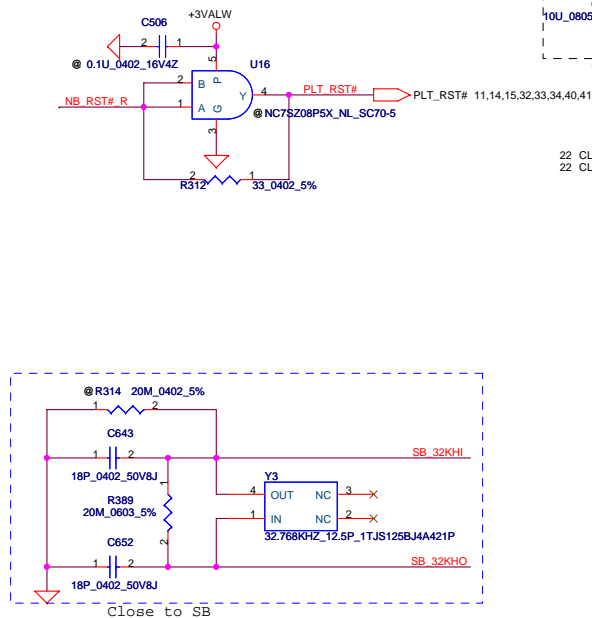
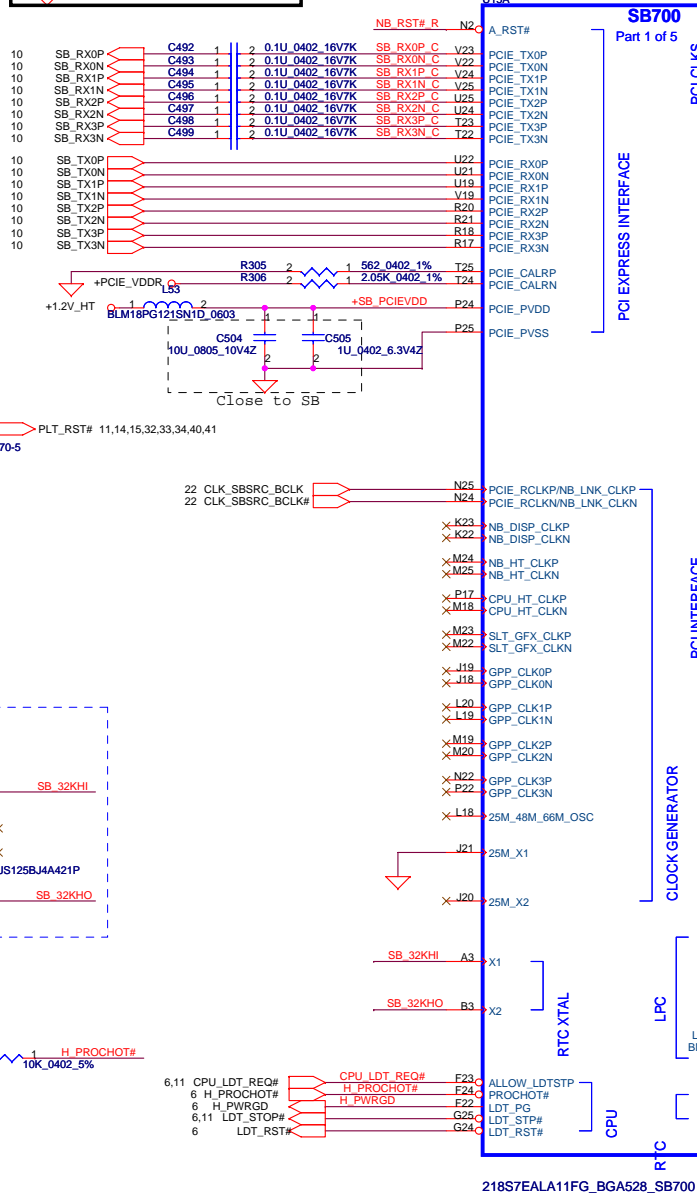
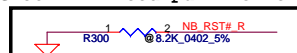


SI:Update HDMI footprint



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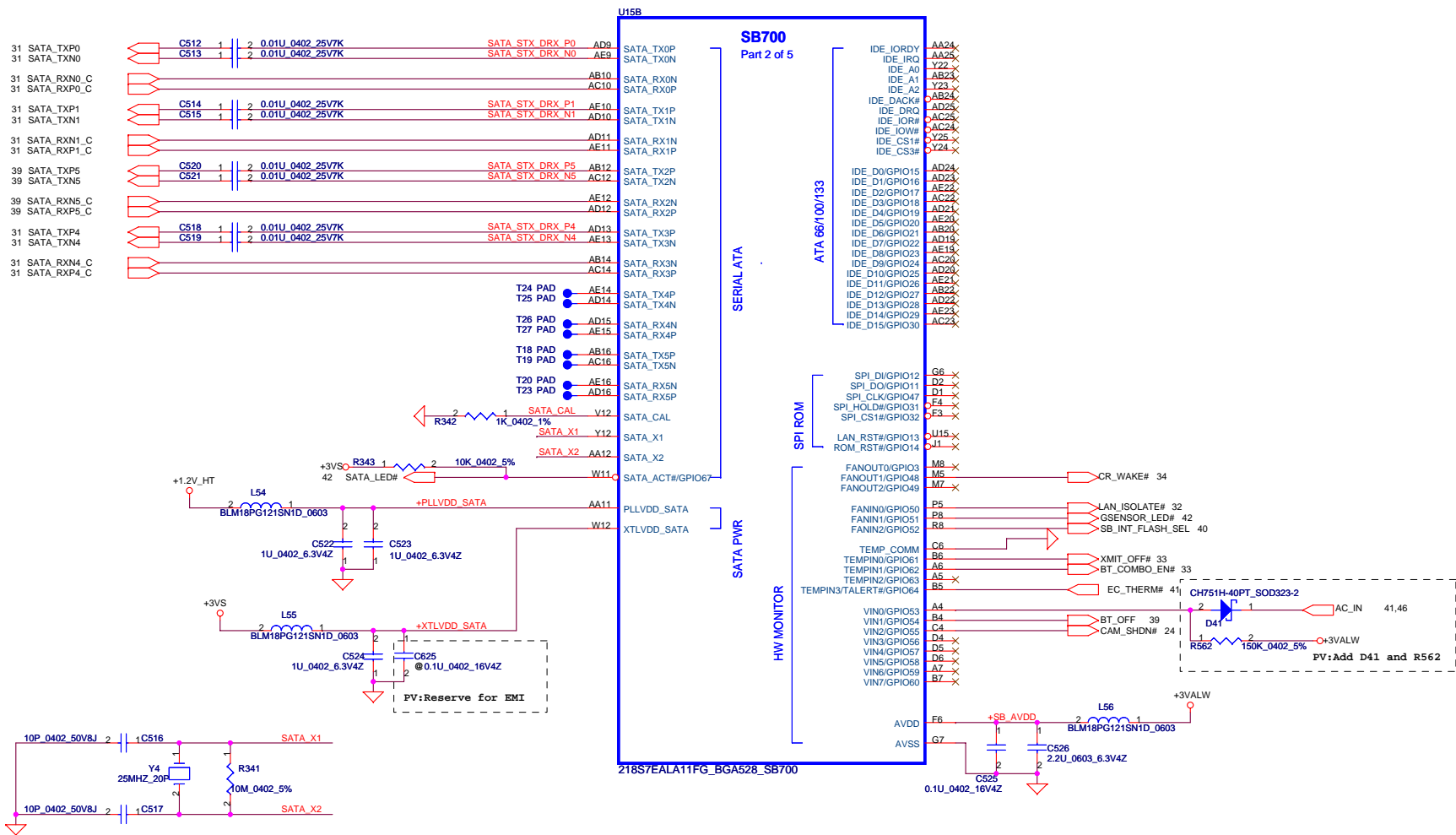
Check AMD need pull low or not



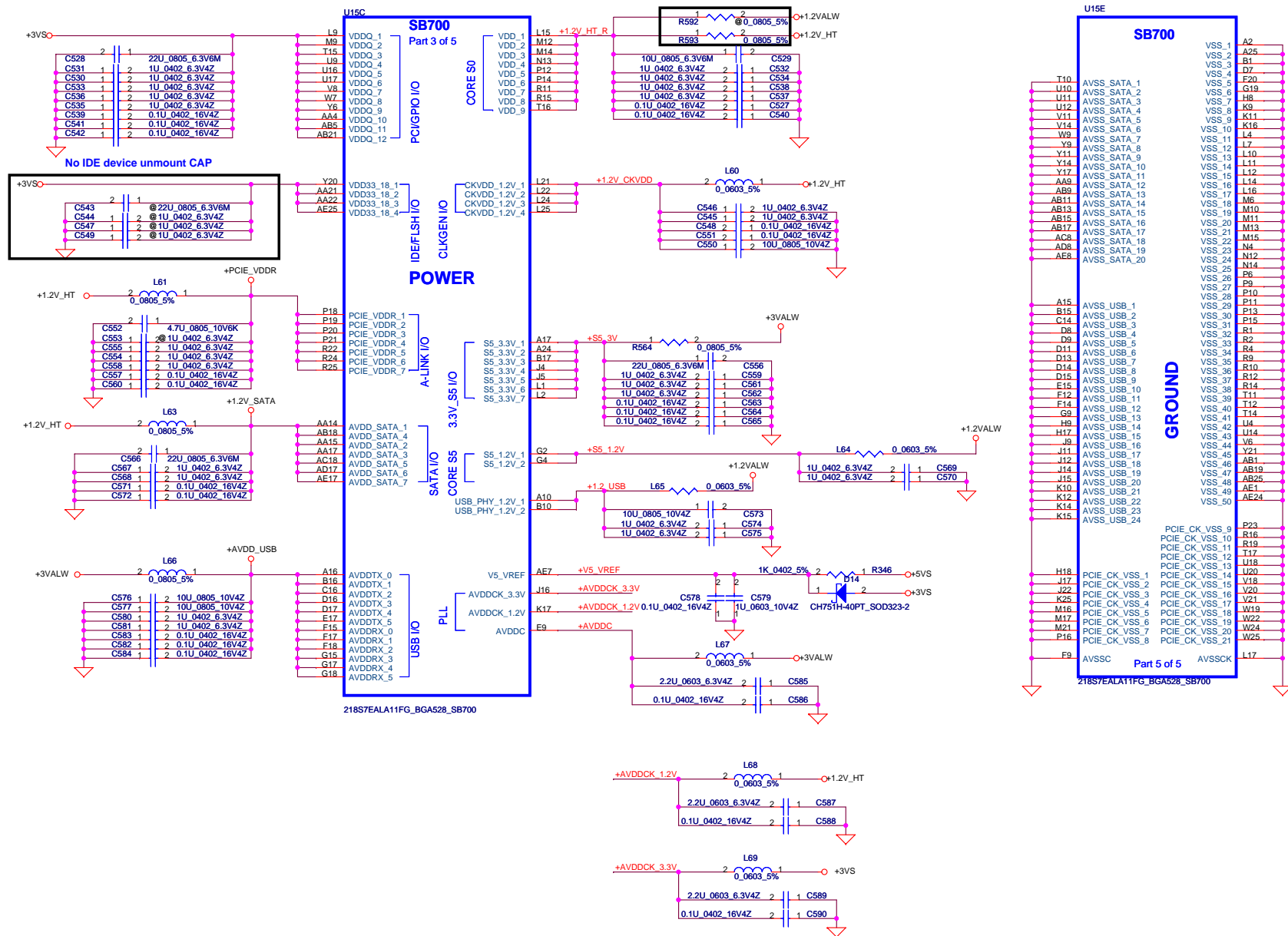
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. SB700-PCIE/PCI/ACPI/LPC/RTC | |
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| | | | | of | |
| | | | | 53 | |



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| | | | | Rev | 0.4 |

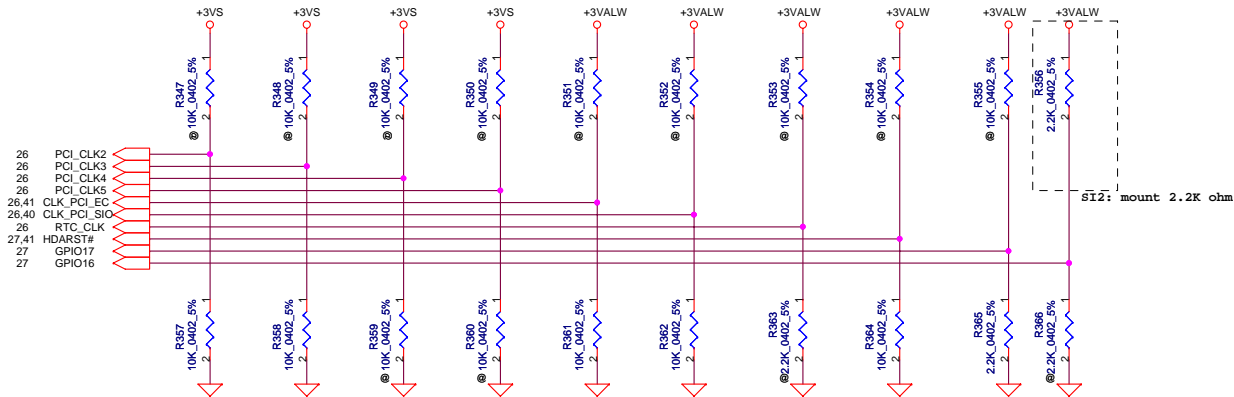


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| | | | | Rev | 0.4 |
| | | | | Date: | Thursday, February 21, 2008 |
| | | | | Sheet | 29 of 53 |

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

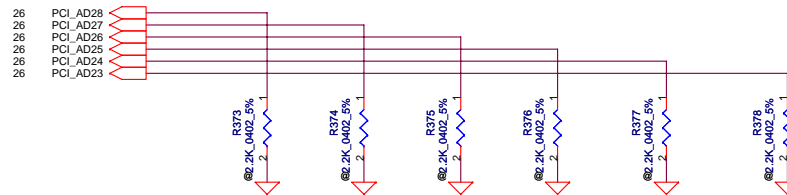
| | PCI_CLK2 | PCI_CLK3 | PCI_CLK4 | PCI_CLK5 | LPC_CLK0 | LPC_CLK1 | RTC_CLK | AZ_RST_CD# | GP17 | GP16 |
|-----------|--|--------------------------------------|----------|----------|------------------------------------|-------------------------------|---|---------------------------|---|--|
| PULL HIGH | BOOTFAIL TIMER ENABLED | USE DEBUG STRAPS | RESERVED | RESERVED | ENABLE PCI MEM BOOT | CLKGEN ENABLED | INTERNAL RTC DEFAULT | EC ENABLED | Internal pull up H,H = Reserved H,L = SPI ROM | |
| PULL LOW | BOOTFAIL TIMER DISABLED DEFAULT | IGNORE DEBUG STRAPS DEFAULT | | | DISABLE PCI MEM BOOT DEFAULT | CLKGEN DISABLED DEFAULT | EXT. RTC (PD on X1, apply 32KHz to RTC_CLK) | EC DISABLED DEFAULT | | L,H = LPC ROM (Default) L,L = FWH ROM |



DEBUG STRAPS

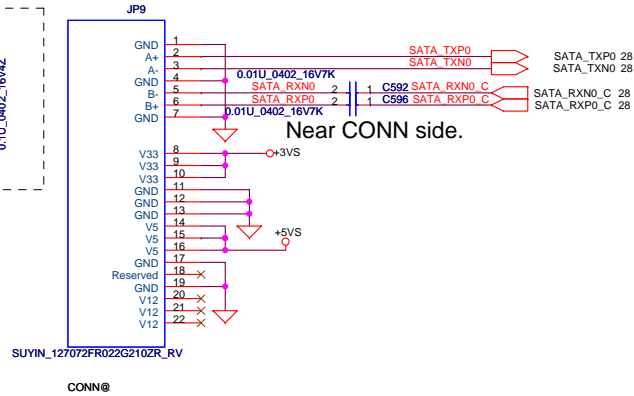
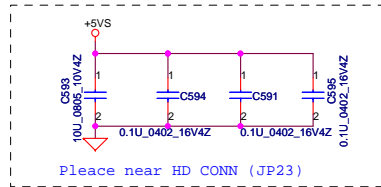
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

| | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|-----------|---------------------------------|---------------------------|-----------------------------|---------------------------|---------------------------------------|----------|
| PULL HIGH | USE LONG RESET DEFAULT | USE PCI PLL DEFAULT | USE ACPI BCLK DEFAULT | USE IDE PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | RESERVED |
| PULL LOW | USE SHORT RESET | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | |

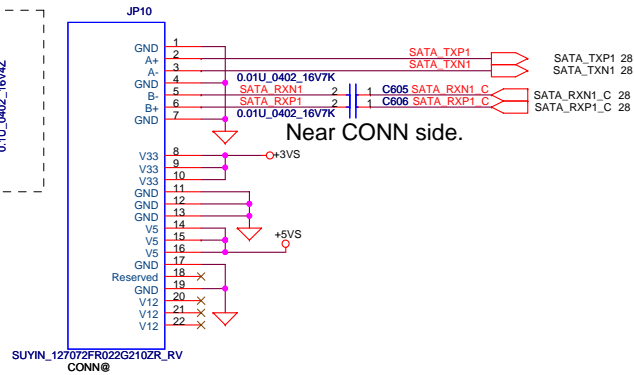
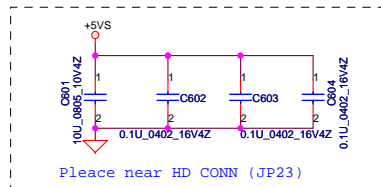


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| Size | Custom | Document Number | LA-4092P | Rev | 0.4 |
| Date: | | Thursday, February 21, 2008 | | Sheet | 30 of 53 |

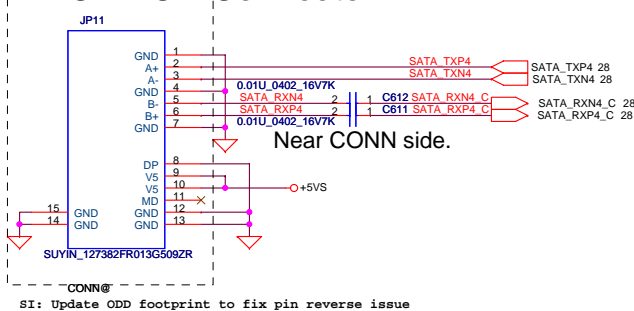
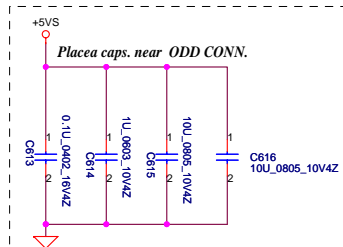
HDD Connector



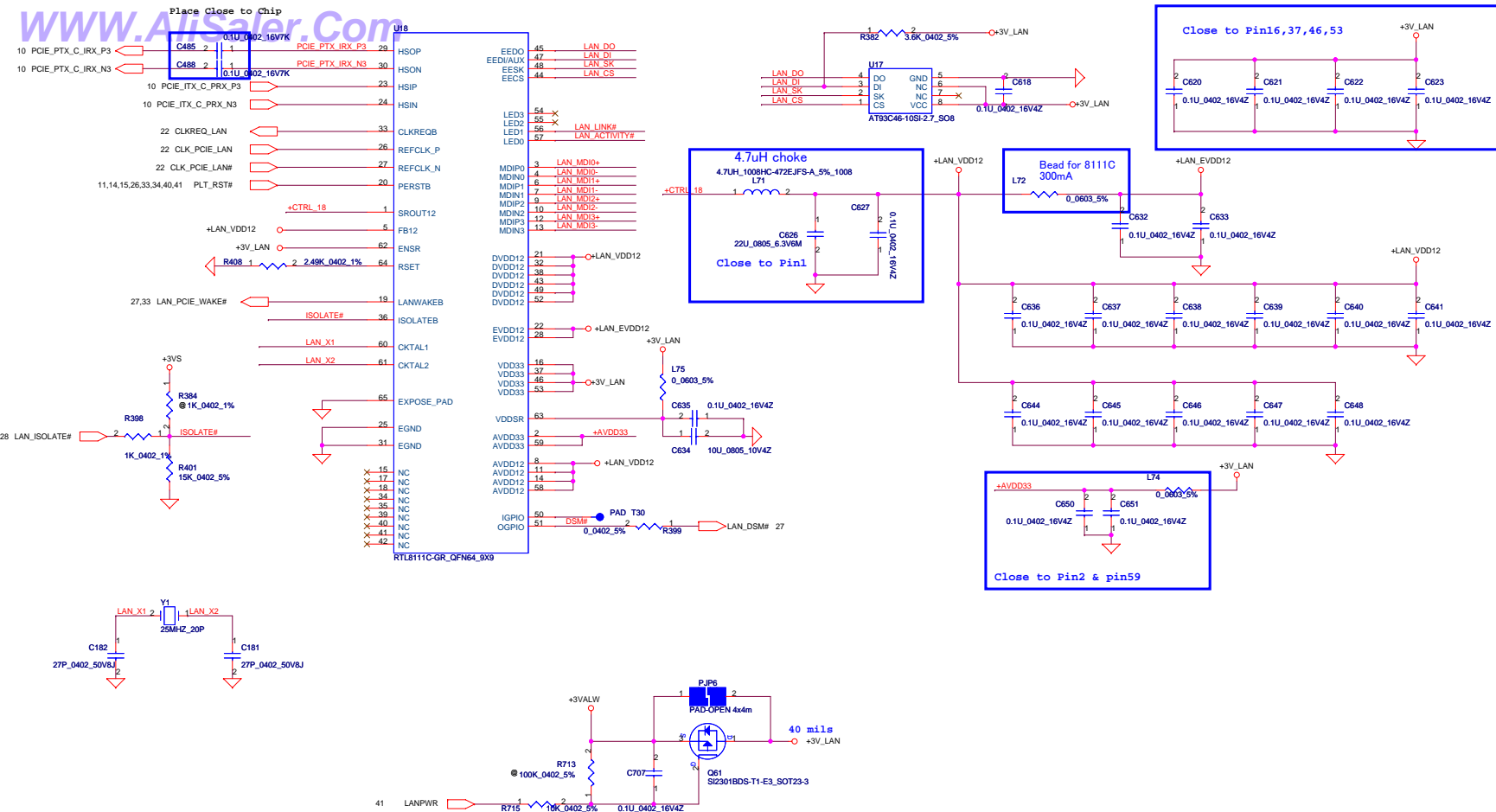
2nd HDD Connector-option



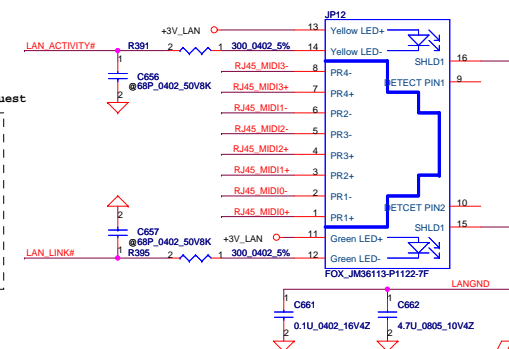
CD-ROM Connector



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| Size | Document Number | Rev | | 0.4 | |
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| | | Sheet | | 31 of 53 | |



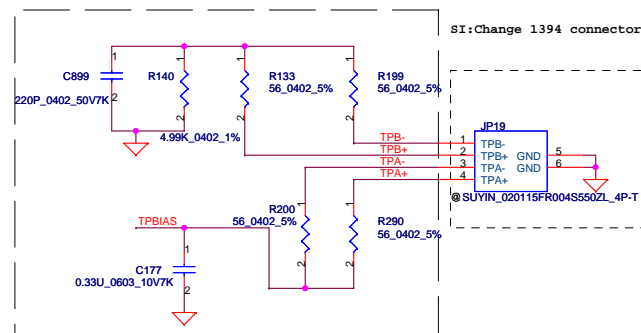
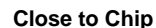
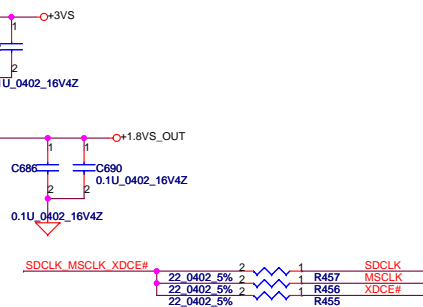
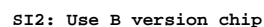
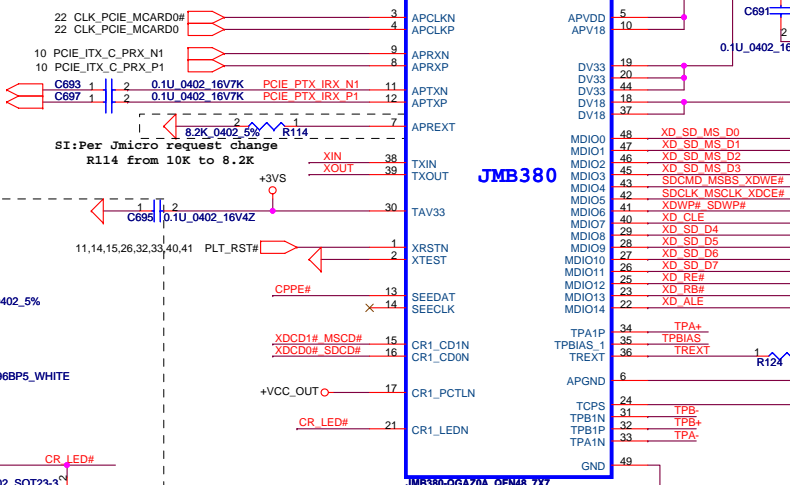
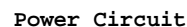
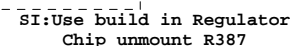
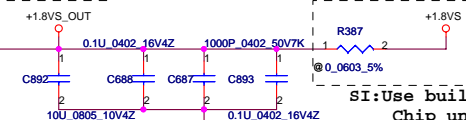
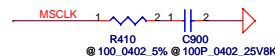
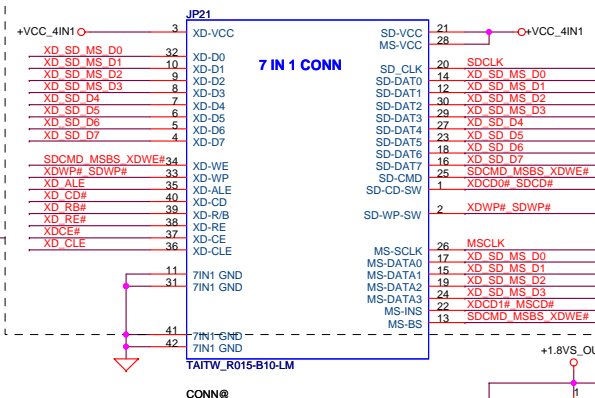
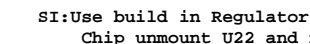
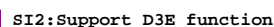
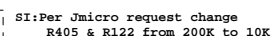
LAN Conn.



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| Date: | | Thursday, February 21, 2008 | | Sheet 32 of 53 | |

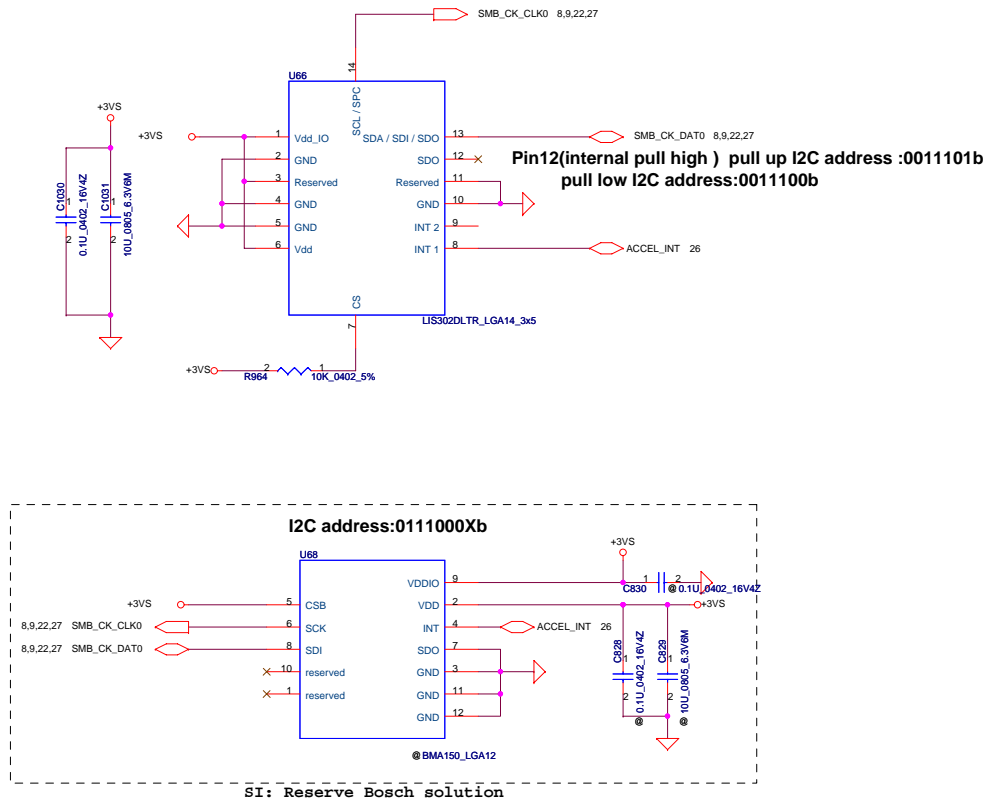
Power Switch internal pull high

WWW.AllSaver.Com



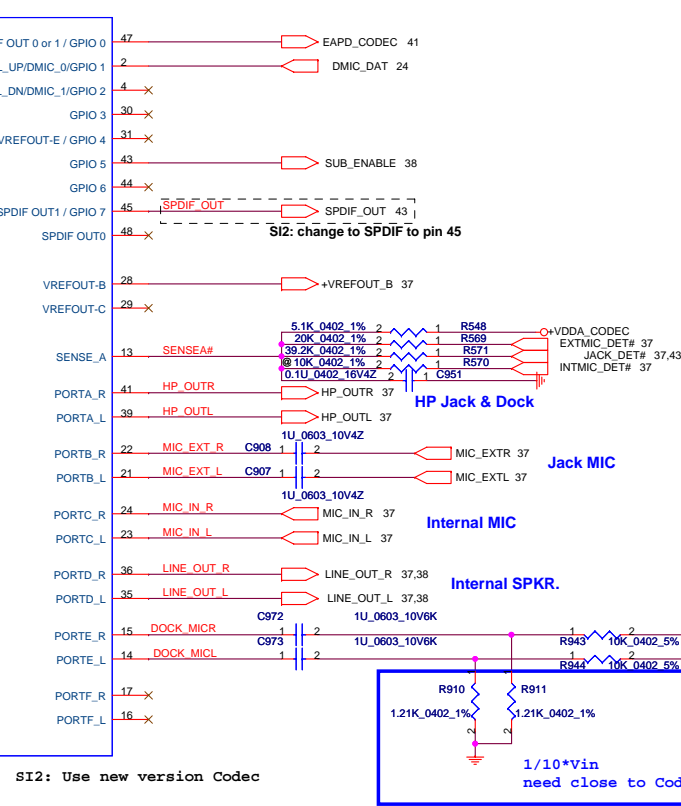
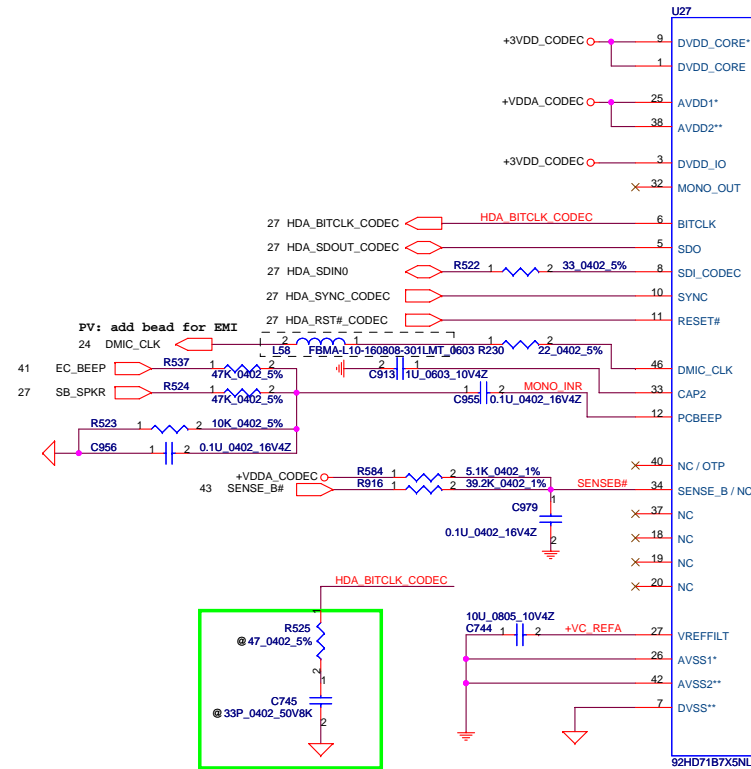
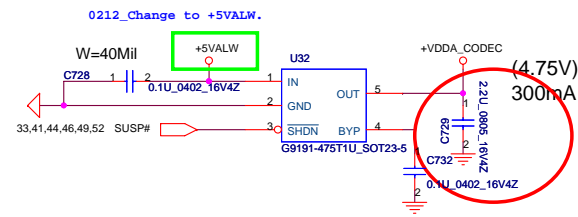
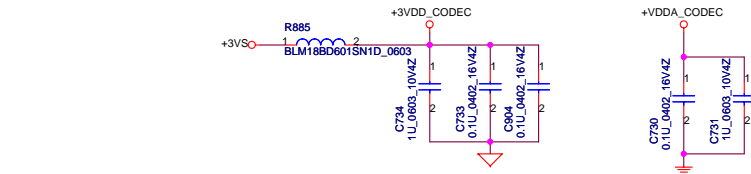
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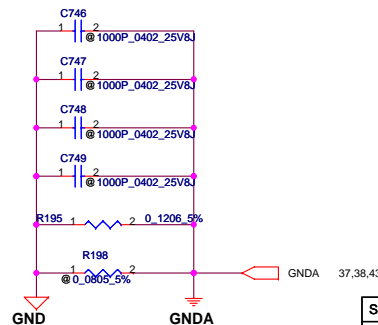


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| | | | | Document Number LA-4092P |
| | | | | Rev 0.4 |
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| | | | | Sheet 35 of 53 |

CODEC POWER

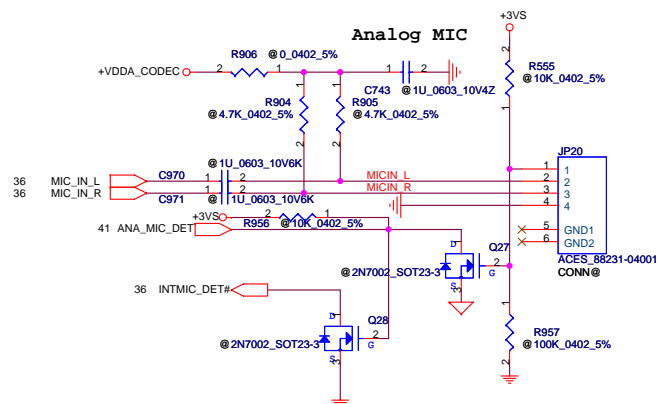
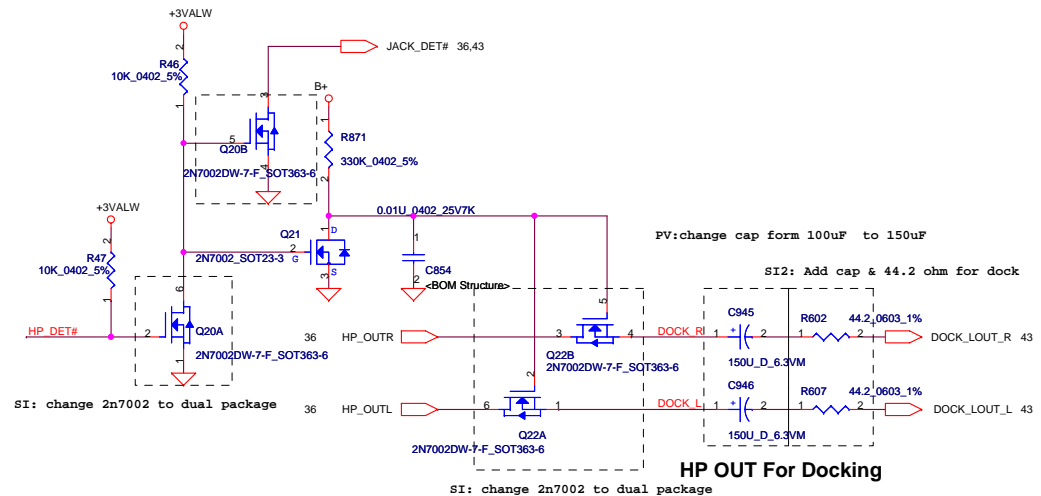
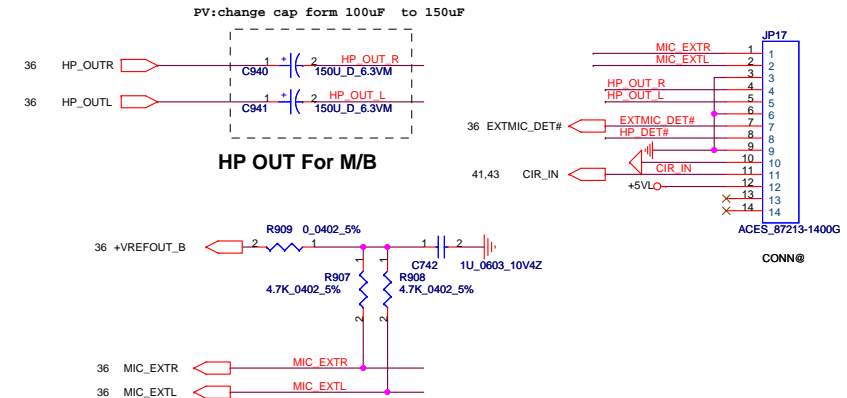
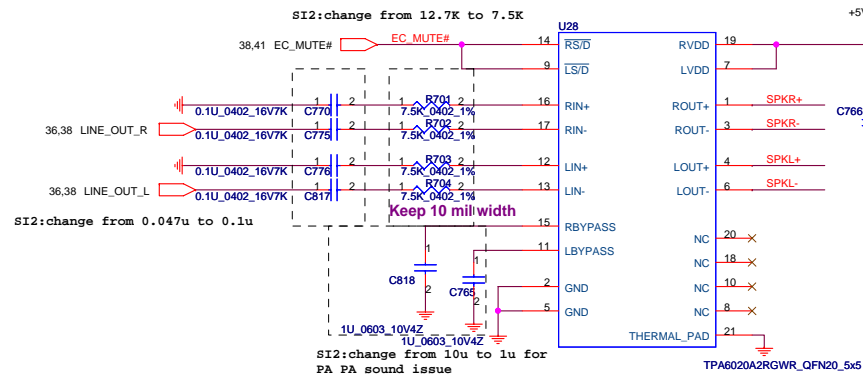


| SENSE A | | SENSE B | |
|---------|----------|---------|----------|
| Port | Resistor | Port | Resistor |
| A | 39.2K | E | 39.2K |
| B | 20K | F | 20K |
| C | 10K | G | 10K |
| D | 5.11K | H | 5.11K |

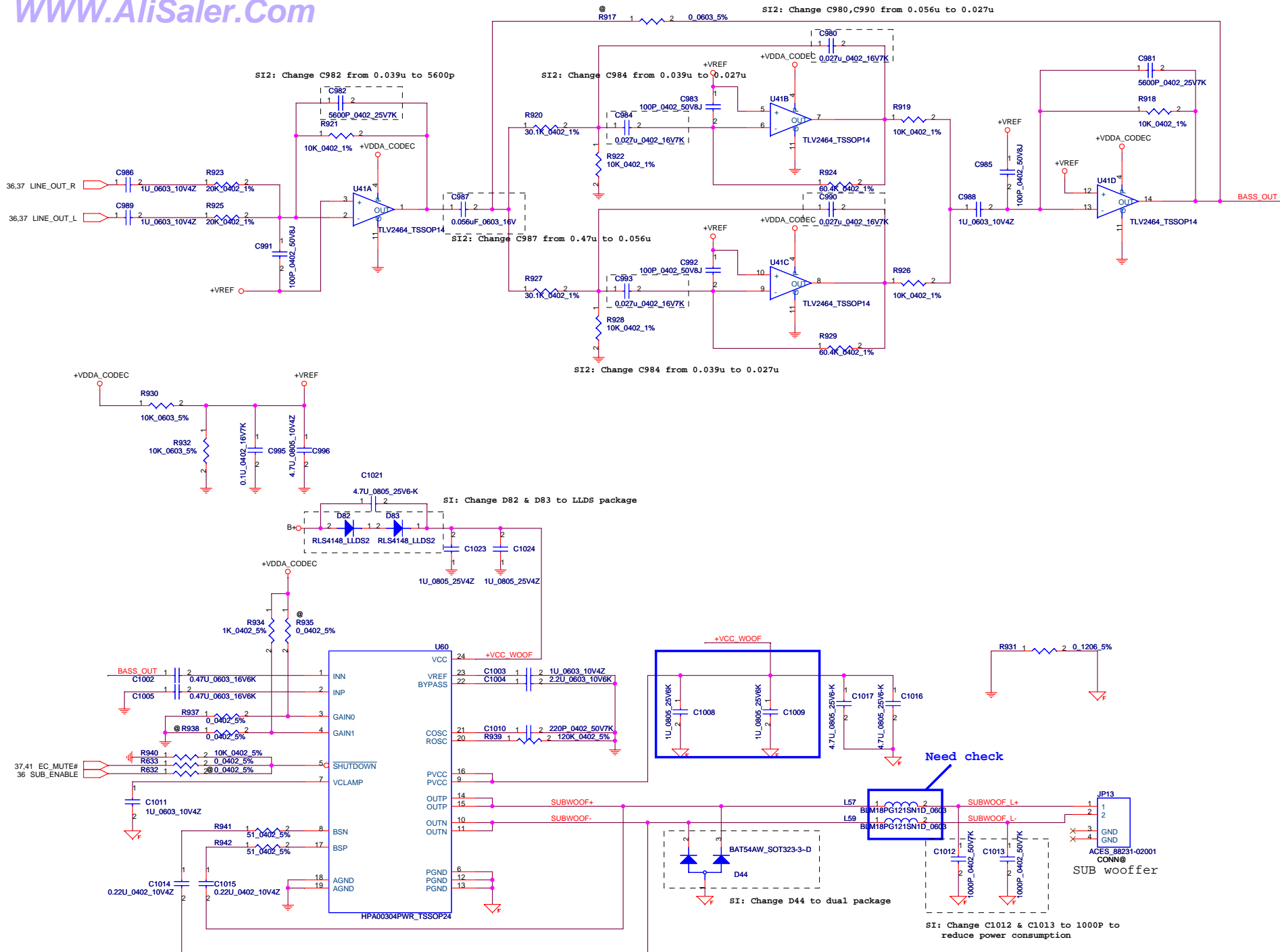


| HP_DET# | MIC_DET | LINEOUT | PORT-A <Earphone OUT> | MIC | EQ |
|---------|---------|---------|--------------------------|-----|---------|
| 0 (LOW) | 0 (LOW) | OFF | ON | ON | Disable |
| 0 (LOW) | NC | OFF | ON | OFF | Disable |
| NC | 0 (LOW) | ON | OFF | ON | Enable |
| NC | NC | ON | OFF | OFF | Enable |

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| Size | Document Number | LA-4092P | | Rev | 0.4 |
| Date: | Thursday, February 21, 2008 | Sheet | 36 | of | 53 |

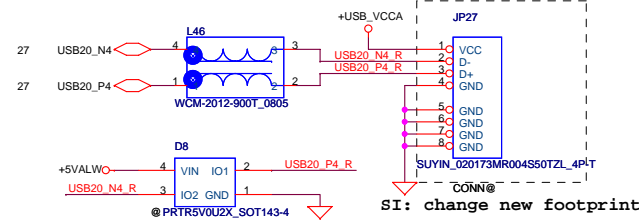
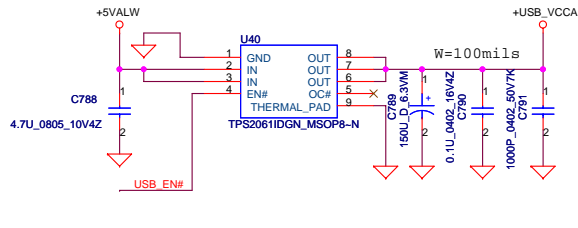


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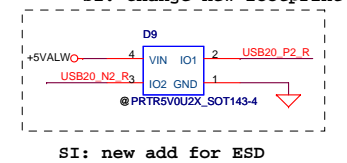
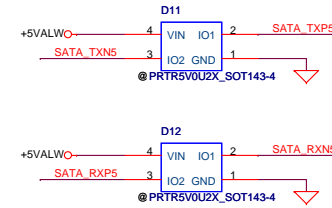
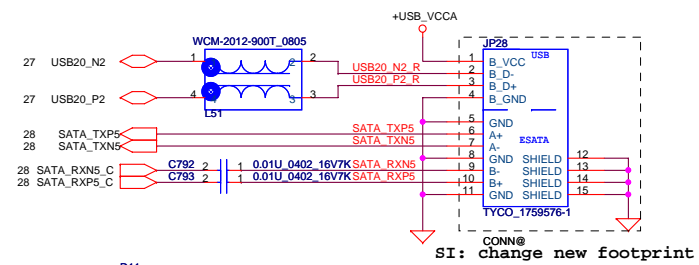


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| | | | | Rev | 0.4 |

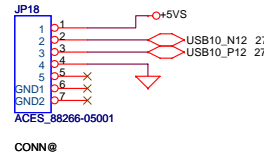
Left side USB CONNECTOR 0



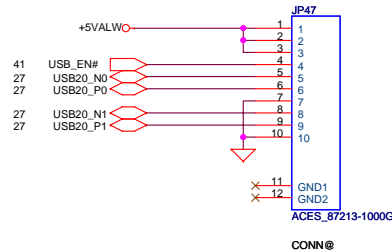
Left side ESATA/USB combination Connector



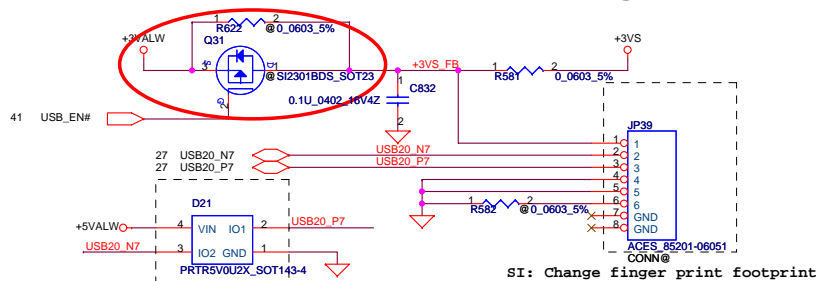
Touch screen



USB Board Conn

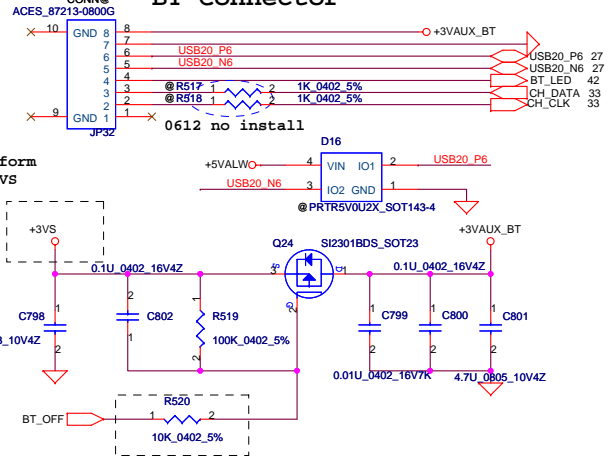


Finger printer



PV: Change PN to SC300000K00 for ESD request

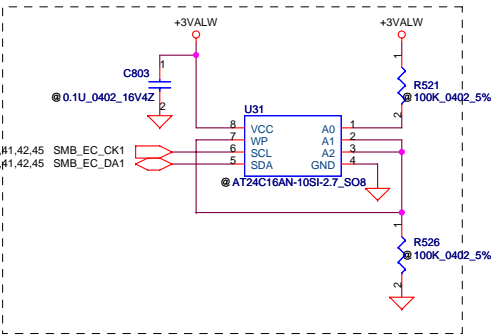
BT Connector



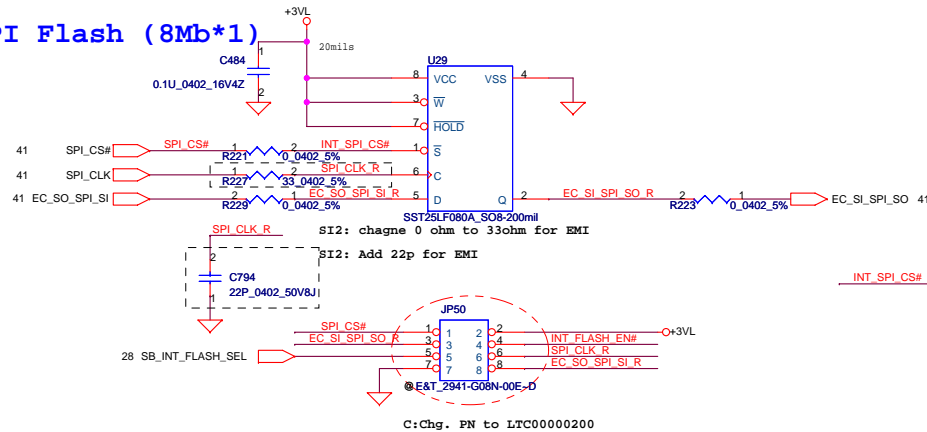
SI: change to 10K ohm to make sure MOS can turn on

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| | | | | Sheet | 39 of 53 |
| | | | | Rev | 0.4 |

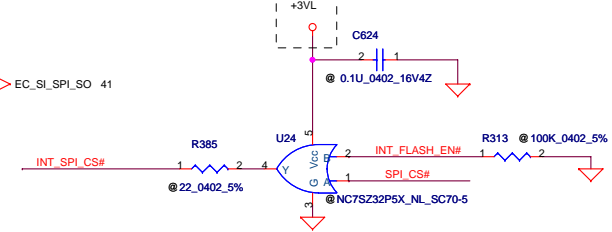
SI2: Change from +3VL to +3VALW and unmount this EEPROM



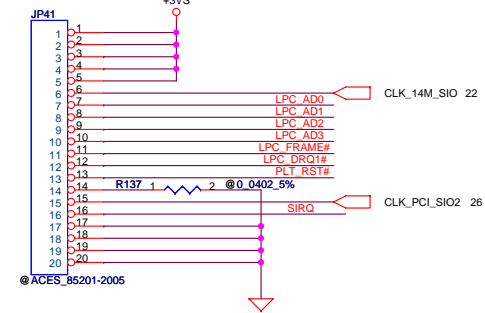
SPI Flash (8Mb*1)



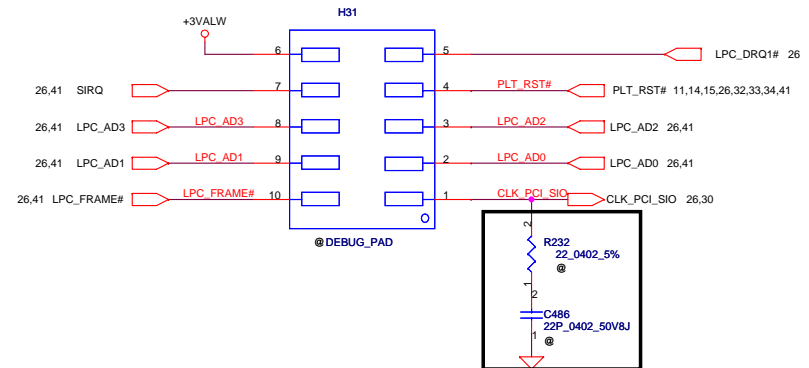
SI2: Change from +3VALW to +3VL



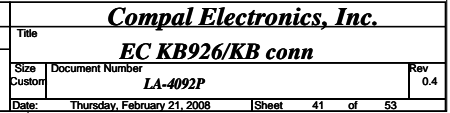
LPC Debug Port



LPC Debug Port

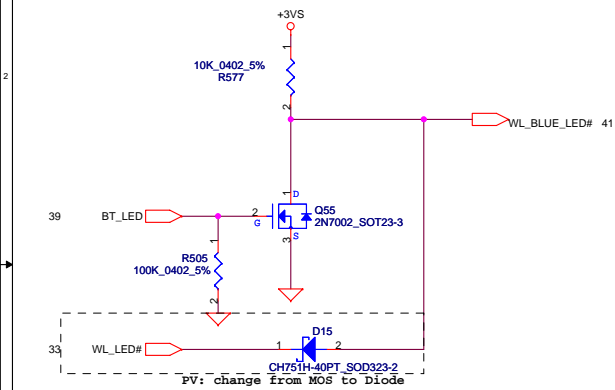
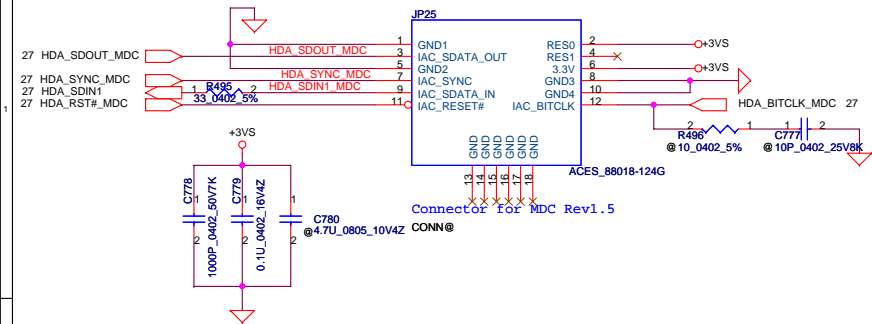


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| | | | | 40 | | | | of | | | |
| | | | | 53 | | | | | | | |

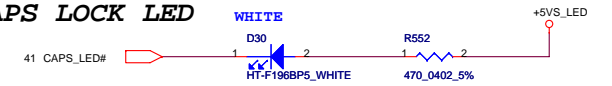
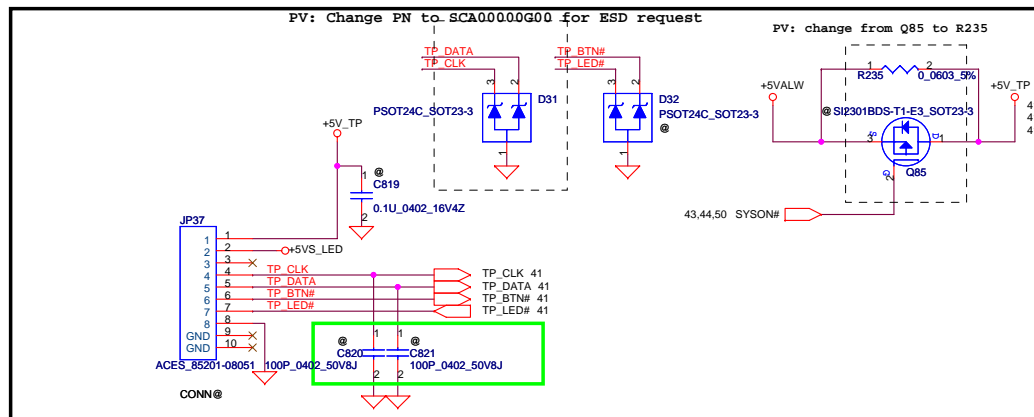


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Change type 4/25



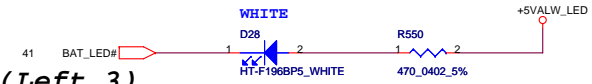
T/P Board (Inculde T/P_ON/OFF)



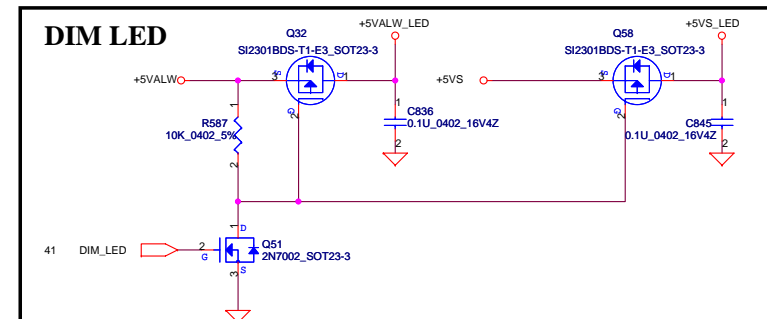
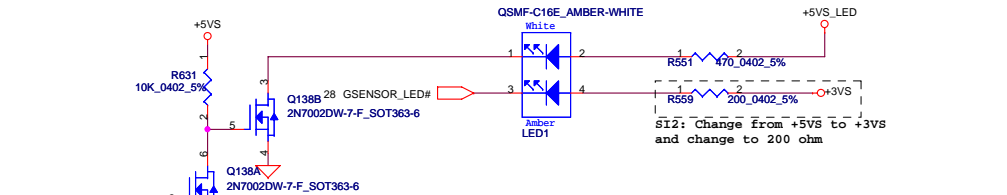
POWER LED(Left 1) WHITE
D27



Battery Charge LED(Left 2)

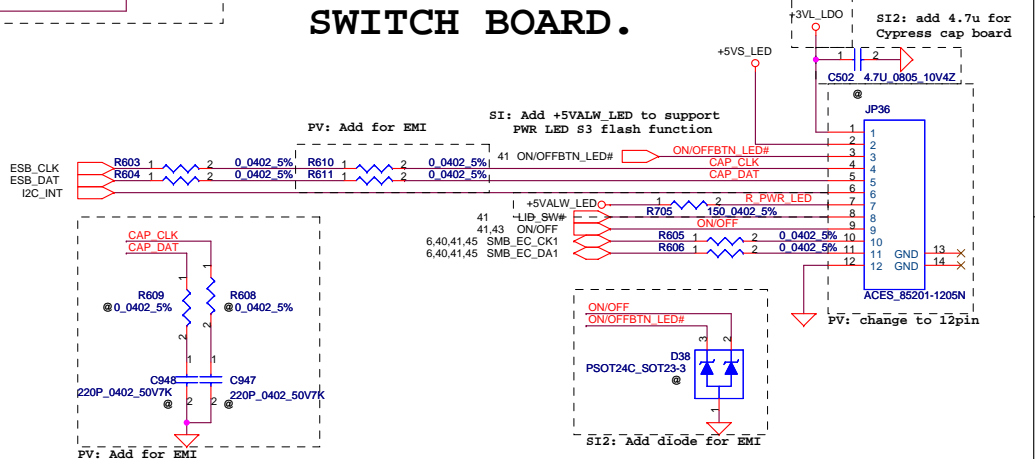


HDD LED(Left 3)



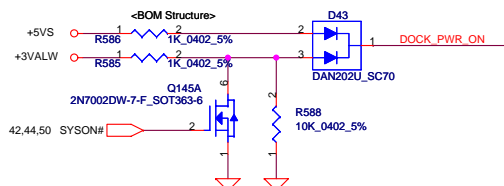
SI: Change to +3VL to support Qplay
bottom boot in BATT mode

SWITCH BOARD.



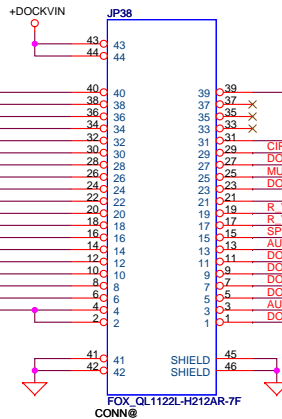
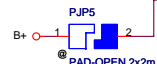
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| | | | | Document Number | 0.4 |
| | | | | LA-4092P | |
| Date: Thursday, February 21, 2008 | | | | Sheet | 42 of 53 |

Atlas/ Saturn Dock

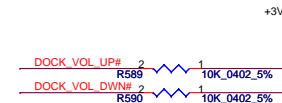


DOCK_PWR_ON Spec
 0V = Notebook S4/S5, Dock off
 2.5V = Notebook S3, Dock on
 4V = Notebook S0, Dock on

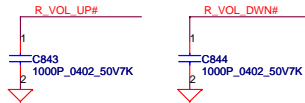
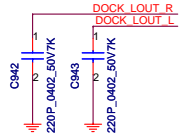
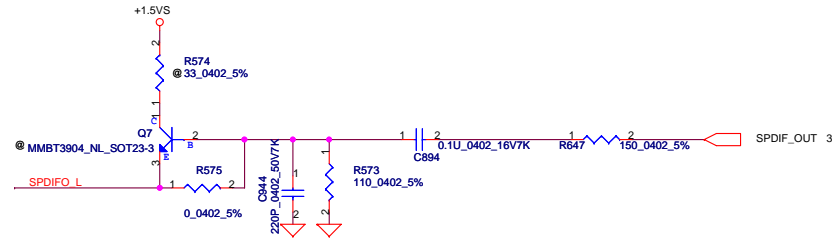
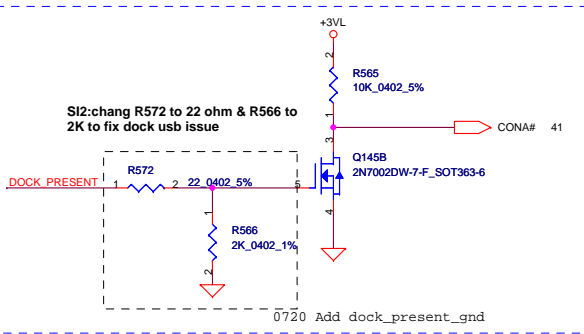
- 23 GREEN_L
- 23 RED_L
- 23 BLUE_L
- 23 D_HSYNC
- 23 D_DDCCLK
- 27 USB20_N3
- 23 D_VSYNC
- 27 USB20_P3
- 32 RJ45_MIDI3+
- 32 RJ45_MIDI3-
- 32 RJ45_MIDI2+
- 32 RJ45_MIDI2-
- 32 RJ45_MIDI1+
- 32 RJ45_MIDI1-
- 32 RJ45_MIDI0+
- 32 RJ45_MIDI0-



need change to reverse type connector

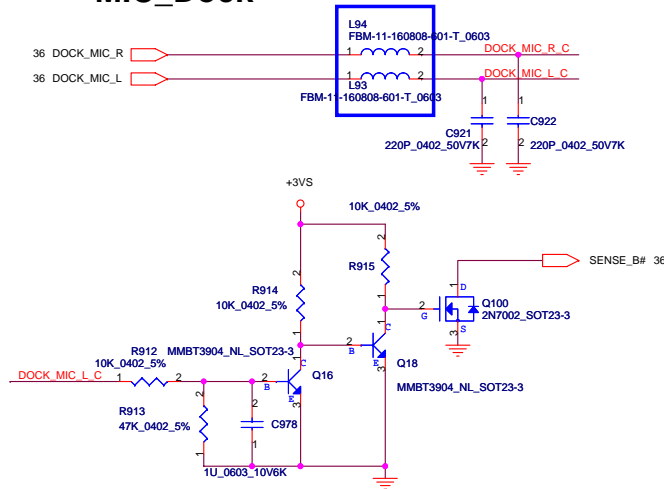


- MUTE_LED 41
- DOCK_SLP_BTN# 41,42
- JACK_DET# 36,37
- DOCK_VOL_UP# 41
- DOCK_VOL_DWN# 41



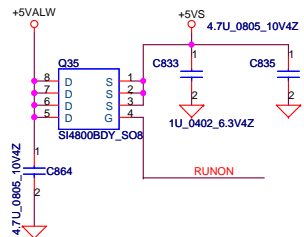
MIC_Dock

Need 600 Ohm 500 mA

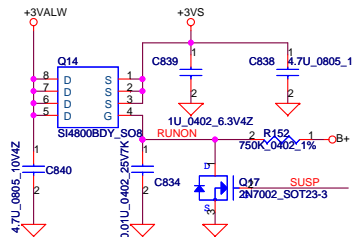


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| Custom | LA-4092P | 0.4 | | Thursday, February 21, 2008 | |
| Sheet | | 43 | | of | |
| E | | 43 | | of | |
| E | | 43 | | of | |

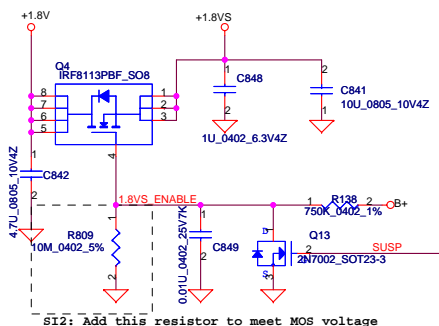
+5VALW TO +5VS



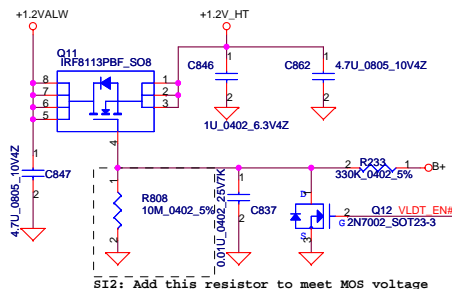
+3VALW TO +3VS



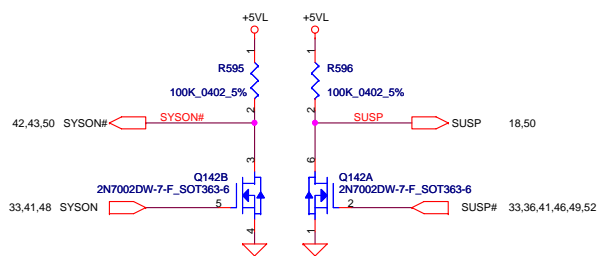
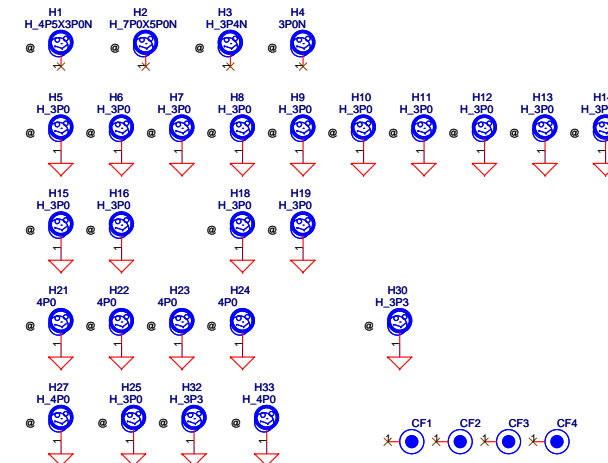
+1.8V TO +1.8VS



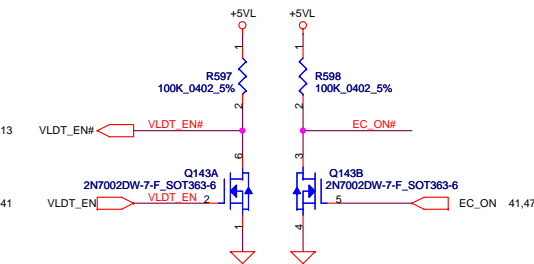
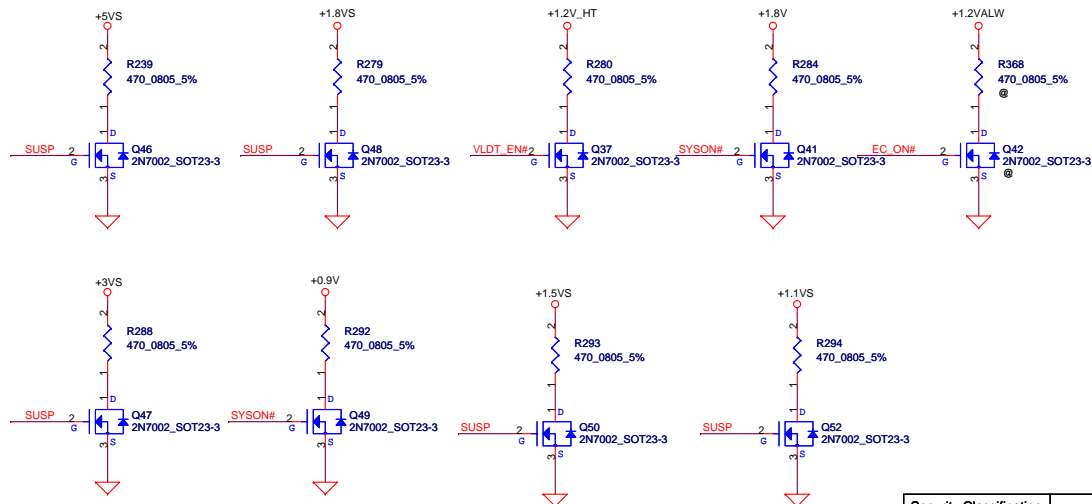
+1.2VALW TO +1.2V_HT



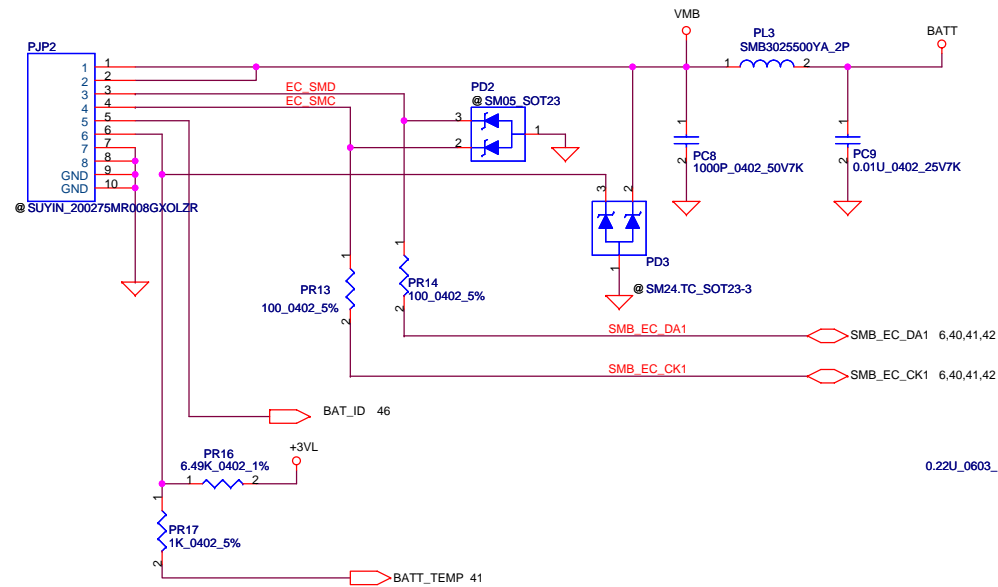
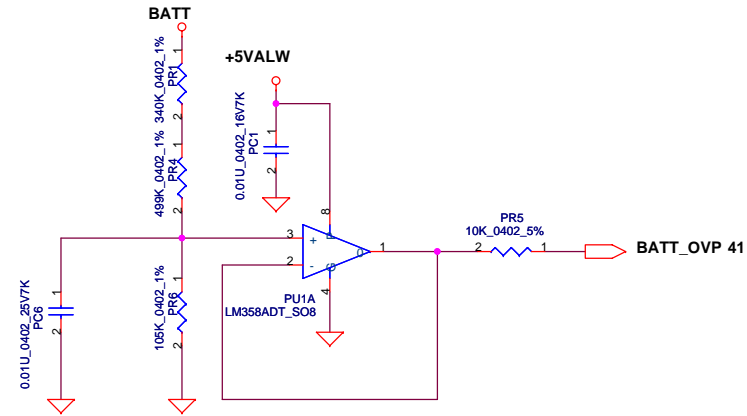
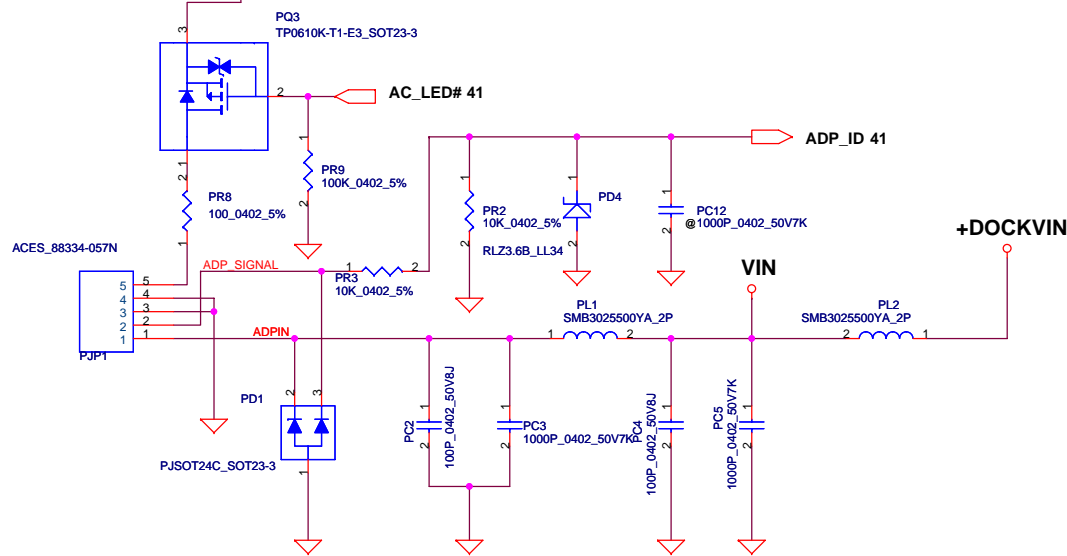
SI2: Add this resistor to meet MOS voltage



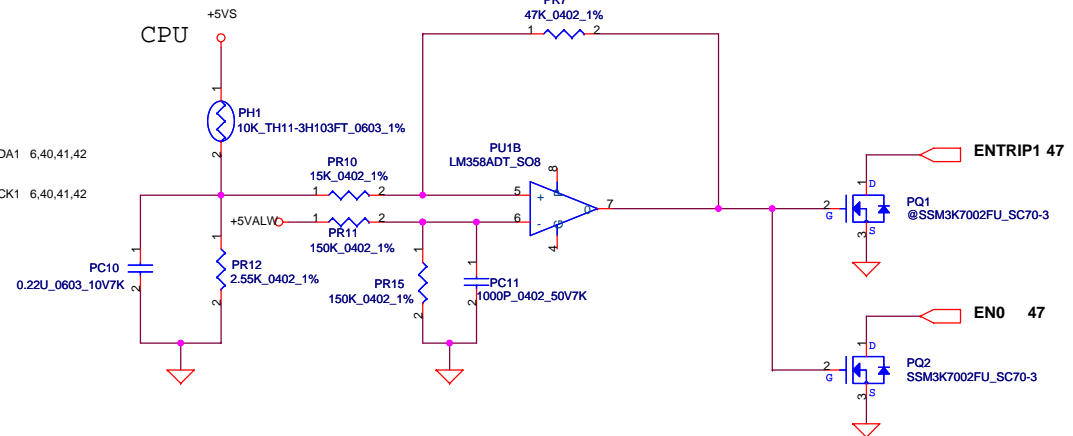
Discharge circuit



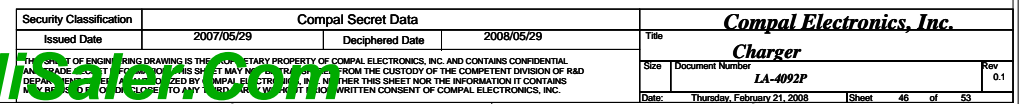
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|---|------------|--------------------|------------|----------------|-----------------------------|
| Issued Date | 2007/08/02 | Deciphered Date | 2008/08/02 | DC/DC Circuits | |
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| | | | | Sheet | 44 of 53 |

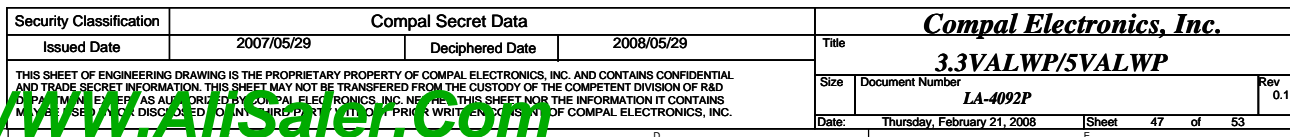


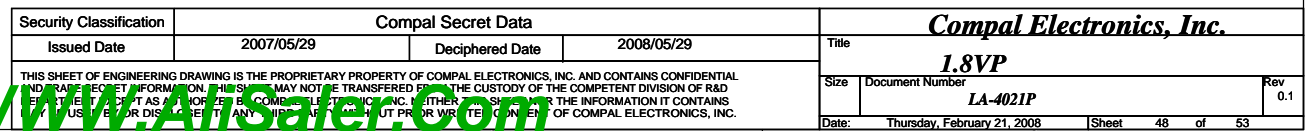
PH1 under CPU bottom side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



| | | | | | |
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| | | | | Sheet | 45 of 53 |
| | | | | Rev | 0.1 |







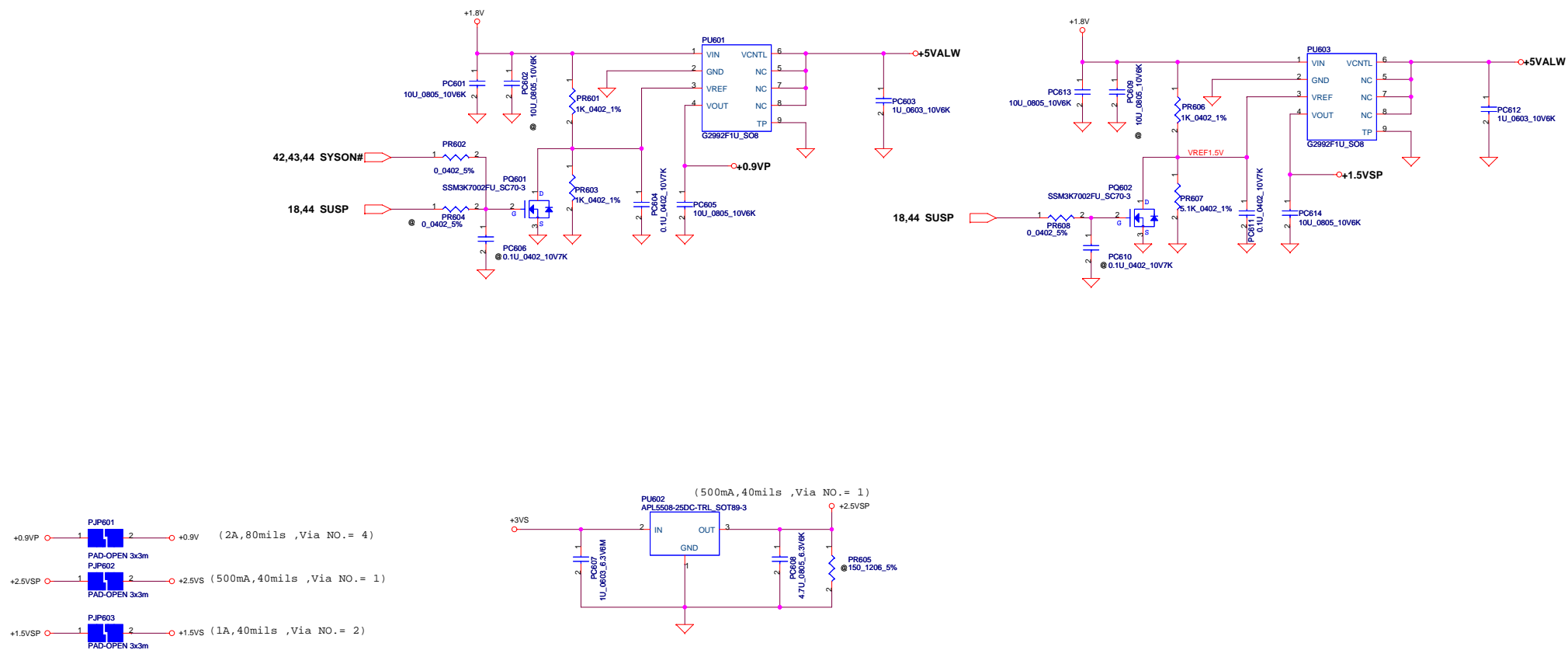
OCP=4.487(min)
MOSTemperature Factor=1.3 (100C)

OCP=9.6(min)
MOSTemperature Factor=1.3 (100C)

+1.1VSP 1 PJP501 2 +1.1VS (6A,240mils ,Via NO.=12)
PAD-OPEN 4x4m

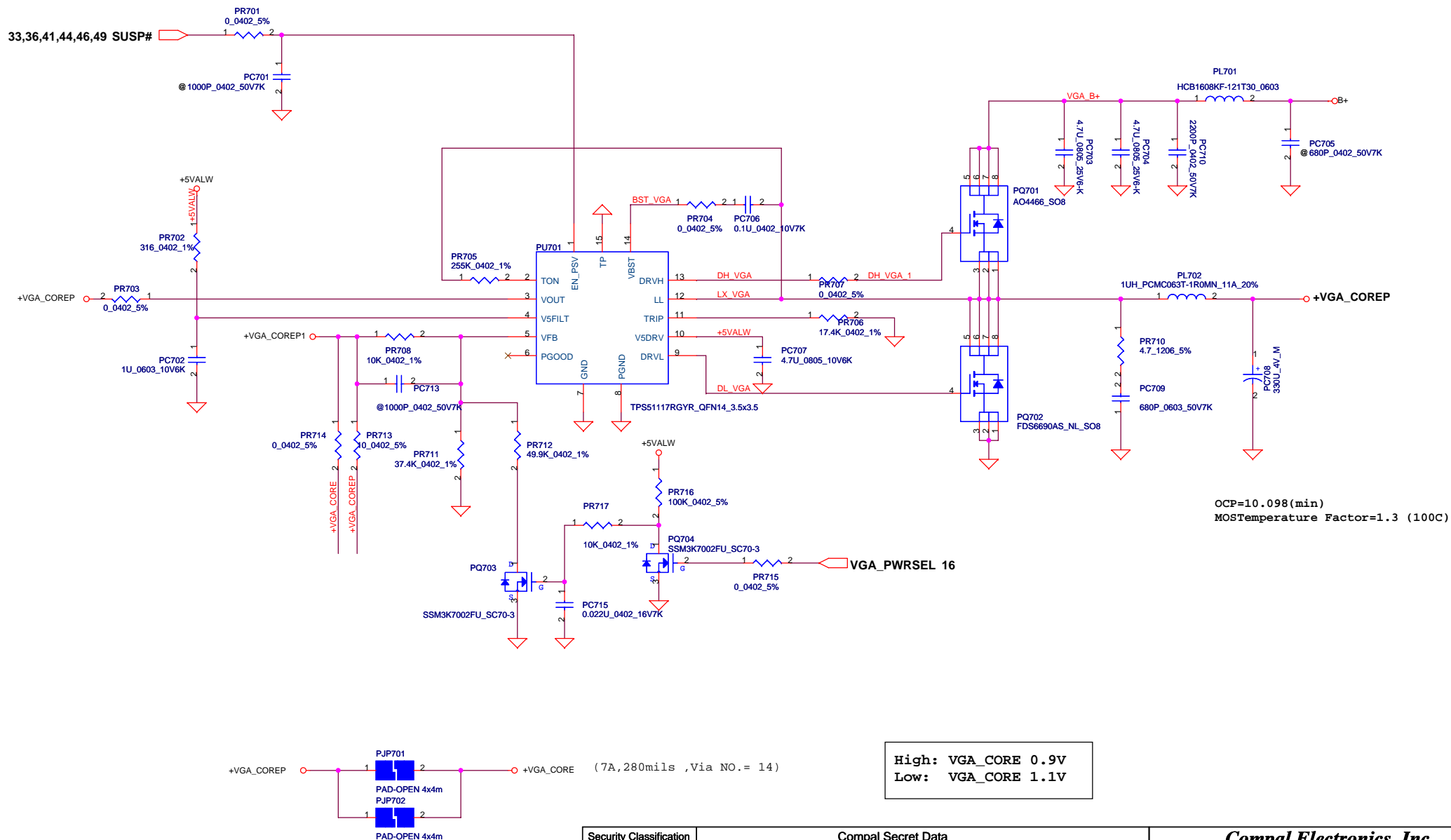
+1.2VALWP 1 PJP502 2 +1.2VALW (4A,160mils ,Via NO.=8)
PAD-OPEN 4x4m

| | | | | | | |
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| | | | | Size | Document Number | Rev |
| | | | | | LA-4092P | 0.1 |
| Date: Thursday, February 21, 2008 | | | | Sheet | 49 of 53 | |



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| 2006/11/23 | | 2007/11/23 | | 0.9VSP/2.5VSP/1.5VSP | |
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| | | | | | | | | 0.1 | | | |
| | | | | Date: | | | | Thursday, February 21, 2008 | | | |
| | | | | Sheet | | | | 52 of 53 | | | |

Version Change List (P. I. R. List) for Power Circuit

| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|------|-------|--------------|-------|---------------|-------------------|--|------|
| 1 | 48 | 1.8VP | 10/23 | Compal | for power request | PU401 change the IC from "S IC RT8204PQW WQFN 16P" to "S IC TPS51117RGYR QFN 14P". | |
| 2 | 46 | Charger | 10/30 | Compal | for power request | PQ104 swap the PQ104 1,3 Pin | |
| 3 | 47 | 3V/5V | 10/30 | Compal | for power request | Change PR301 to 13.7K modify output voltage | |
| 4 | 47 | 3V/5V | 10/30 | Compal | for power request | Change PR305 to 180K modify OCP | |
| 5 | 47 | 3V/5V | 10/30 | Compal | for power request | Change PR306 to 150K modify OCP | |
| 6 | 47 | 3V/5V | 10/30 | Compal | for power request | Change PR311 to 620K | |
| 7 | 47 | 3V/5V | 10/30 | Compal | for power request | Change PR315 to 604K modify sequence | |
| 8 | 49 | +1.1VSP | 10/30 | Compal | for power request | Change PR510 to 19.1K modify OCP | |
| 9 | 49 | +1.2VALWP | 10/30 | Compal | for power request | Change PR511 to 19.1K modify OCP | |
| 10 | 46 | Charger | 10/30 | Compal | for power request | Del PR119 | |
| 11 | 51 | CPU_CORE | 10/30 | Compal | for power request | Change PC202 to B2 type for ME limit | |
| 12 | 51 | CPU_CORE | 10/30 | Compal | for power request | Change PR223 to 17.8K and PR224 to 100K modify OCP | |
| 13 | 51 | CPU_CORE | 10/30 | Compal | for power request | Change PR221,PR231 to 16.5K and PR217,PR233 to 4.02K for CPU_CORE compensation | |
| 14 | 45 | DC connector | 10/30 | Compal | for power request | Add PR3,PD4,PC12 for ADP_ID function | |
| 15 | 47 | 3V/5V | 10/30 | Compal | for power request | Add PR317,PR318 | |
| 16 | 46 | Charger | 10/30 | Compal | for power request | Change net from +3VLP to +3VL | |
| 17 | 49 | +1.1VSP | 10/30 | Compal | for power request | Change PR513 to 21K for HW power scquence. | |
| 18 | 46 | Charger | 11/09 | Compal | for power request | Pop PR119 Unpop PR9 | |
| 19 | 50 | 0.9VSP | 11/09 | Compal | for power request | Change PC601,PC605,PC611,PC603,PC613,PC614,PC612, PC201 for common part | |
| 20 | 46 | Charger | 11/09 | Compal | for power request | Change PR112 to 0.015 Ohm | |
| 21 | 49 | +1.2VALWP | 11/09 | Compal | for power request | Change PC508 to D2 size for ME limit | |
| 22 | 51 | CPU_CORE | 12/05 | Compal | for EMI request | Add PR220,PR229 for EMI | |
| 23 | 49 | CPU_CORE | 12/05 | Compal | for EMI request | Add PC218,PC226 for EMI | |
| | | | | | | | |

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| | | | | Custom | LA-4111P | 0.1 |
| | | | | Date: Thursday, February 21, 2008 Sheet 53 of 52 | | |

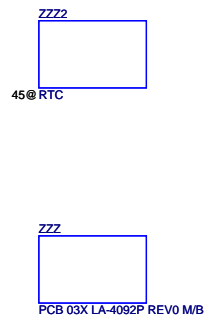
| | Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|------|-------|-----------------------|-------|---------------|-------------------|--|------|
| 1 | 1 | 46 | Charger | 12/05 | Compal | for power request | Change PR120 to 133K to change charger current | |
| | 2 | 47 | 3V/5V | 12/05 | Compal | for power request | Change PR302 to 30.9K for common part | |
| | 3 | 47 | 3V/5V | 12/05 | Compal | for power request | Change PR304 to 20K for common part | |
| | 4 | 48 | +1.8VP | 12/05 | Compal | for power request | Change PR408 to 18.2K modify OCP | |
| | 5 | 52 | VGA_CORE | 12/05 | Compal | for power request | Change PR306 to 150K modify OCP | |
| | 6 | 52 | VGA_CORE | 12/05 | Compal | for power request | Change PR714 to 0 Ohm | |
| | 7 | 52 | VGA_CORE | 12/05 | Compal | for power request | Add PR713 100 Ohm | |
| | 8 | 45 | DC Connector /CPU_OTP | 12/25 | Compal | for power request | Del PR9 | |
| 2 | 9 | 46 | Charger | 12/25 | Compal | for power request | Reconnect from BQ24740VREF to +3VL | |
| | 10 | 47 | 3V/5V | 12/25 | Compal | for power request | Add PU302 | |
| | 11 | 52 | VGA_CORE | 12/25 | Compal | for power request | Del PC714 Change PC715 to 0.022u & PR713 to 10 Ohm | |
| | 12 | 51 | CPU_CORE | 12/27 | Compal | for power request | ADD PC204 & PC211 68uF | |
| → | 13 | 48 | +1.8VP | 1/2 | Compal | for EMI request | Add PR410 4.7ohm and PC410 680P | |
| | 14 | 48 | +1.8VP | 1/2 | Compal | for EMI request | Add PC405 680P and 408 3.3nF | |
| | 15 | 51 | CPU_CORE | 1/2 | Compal | for EMI request | ADD PC241 820p & PC242 3300p | |
| | 16 | 52 | VGA_CORE | 1/2 | Compal | for EMI request | Add PR710 and PC709 | |
| 3 | 17 | 51 | CPU_CORE | 1/2 | Compal | for EMI request | ADD PC243 to 3.3n PC244 to 820p | |
| | 18 | 51 | CPU_CORE | 1/3 | Compal | for power request | ADD PR234 & PQ115 | |

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|--|------------|--------------------|------------|--|-----------------------------|----------------|
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| | | | | | LA-4111P | 0.1 |
| | | | | Date: | Thursday, February 21, 2008 | Sheet 54 of 54 |

HW4 Product Improvement Record (P.I.R.)

1. Change R538 Pull high from +3VL to +3VALW
2. New add R563,R571 Pull high +3VS
3. Unmount BKOFF# Pull high R483
4. Unmount CPU_LDT_REQ# Pull high R318
5. Change LED1 P/N to SC500004C00
6. Change JP36 Pin2 from +5VS_LED to +5VALW_LED
7. Change C1012 & C1013 from 4700P to 1000P
8. Change R186 size from 0603 to 0402
9. Delete TV function and relation component
10. Add R554 for CIR pull high
- 11.Add C327 on BATT_OVT
- 12.Change L57 & L59 to 0603 BLM18PG121SN1D
13. exchange TV & WLAN mini card location
- 14.add LAN cable detect circuit
- 15.update ODD CONN footporint and symbol
- 16.delete Lid switch baord Conn
- 17.Change Cap sensor board power to +3VL to support Qplay boot

RTC



| | | | | | |
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| | | | | Sheet | 55 of 54 |
| | | | | Rev | 0.4 |