

# Compal confidential

JBK00 LA-4091P Schematics Document

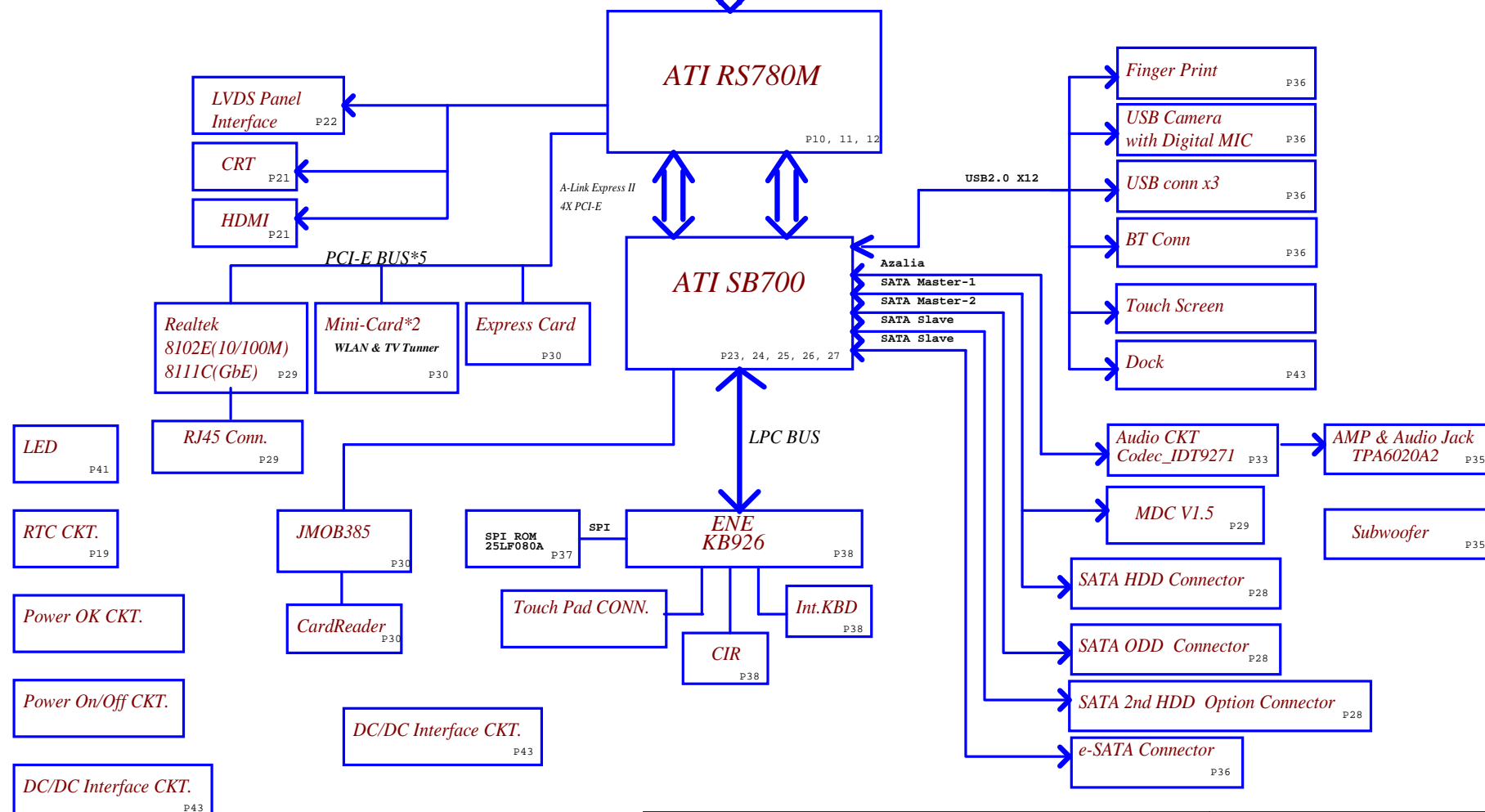
Mobile AMD S1G2 CPU with ATI  
RS780M & SB700 core logic

2007-10-30

REV:0.2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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The diagram illustrates the test system architecture. At the center is the **AMD S1G2 CPU** (638-PIN uFCPGA 638). To its left, a **Thermal Sensor** (ADM1032ARMZ) is connected to pin P6, and a **Fan conn** is connected to pin P4. To the right, **DDR2 800MHz 1.8V** memory (DDR2-SO-DIMM X2, BANK 0, 1, 2, 3) is connected to pins P8 and P9, and a **Clock Generator** (SLG8SP626) is connected to pins P20 and P21. A **Hyper Transport Link** connects the CPU to the memory and clock generator.



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## Voltage Rails

O MEANS ON X MEANS OFF

power plane State	+B +3VL	+5VALW +3VALW +1.2VALW	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

## Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

 Layout Notes

UMA@ : means for RS780M.

## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
ACCELEROMETER	3A	00111010

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM 1 / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_DA1	KB926	X	X	X	V	X	X	X	X	X	X
SMB_EC_CK2	KB926	X	X	X	V	X	X	X	X	X	X
SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK	RS780M	X	X	X	X	X	X	X	V	X	X
I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1	RS780M	X	X	X	X	X	X	X	X	X	X
DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0	SB700	X	X	X	X	V	V	X	X	X	V
SDA0	SB700	X	X	X	X	X	X	V	X	X	X
SCL1	SB700	X	X	X	X	X	X	V	X	X	X
SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2	SB700	X	X	X	X	X	X	X	X	X	X
SDA2	SB700	X	X	X	X	X	X	X	X	X	X
SCL3	SB700	X	X	X	X	X	X	X	X	X	X
SDA3	SB700	X	X	X	X	X	X	X	X	X	X

## EC SM Bus1 address

## EC SM Bus2 address

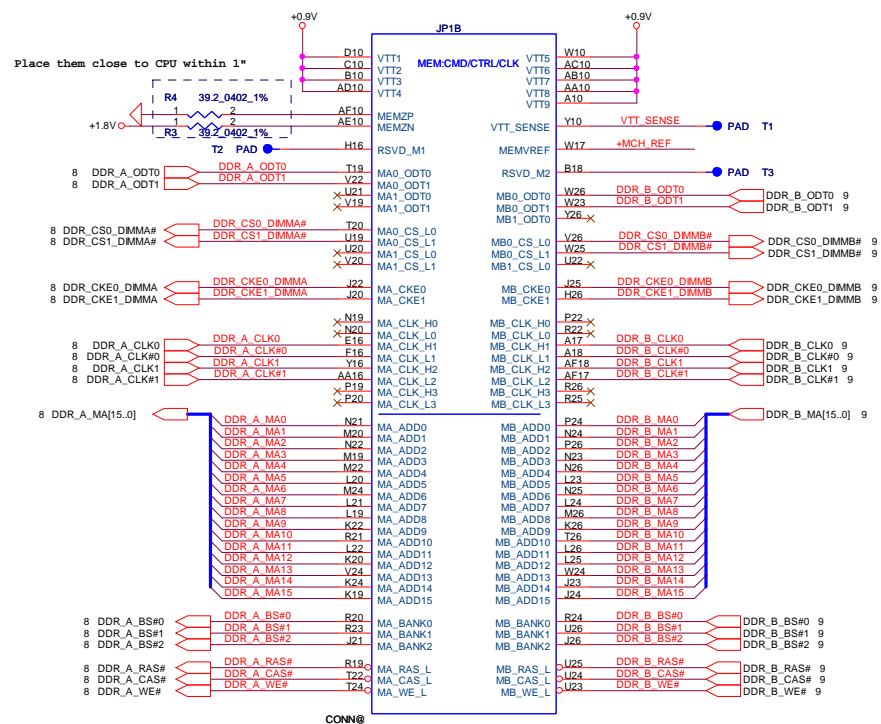
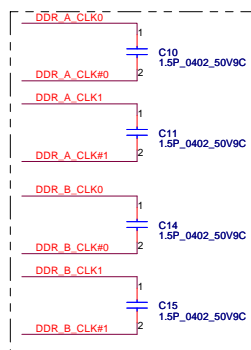
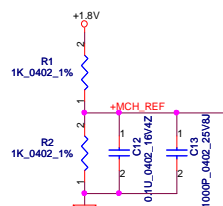
Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	AD1032-2 CPU	9AH	1001 101X b
24C16	A0H	1010 000X b			
CPU SIC interface	98H	1001 100X b			

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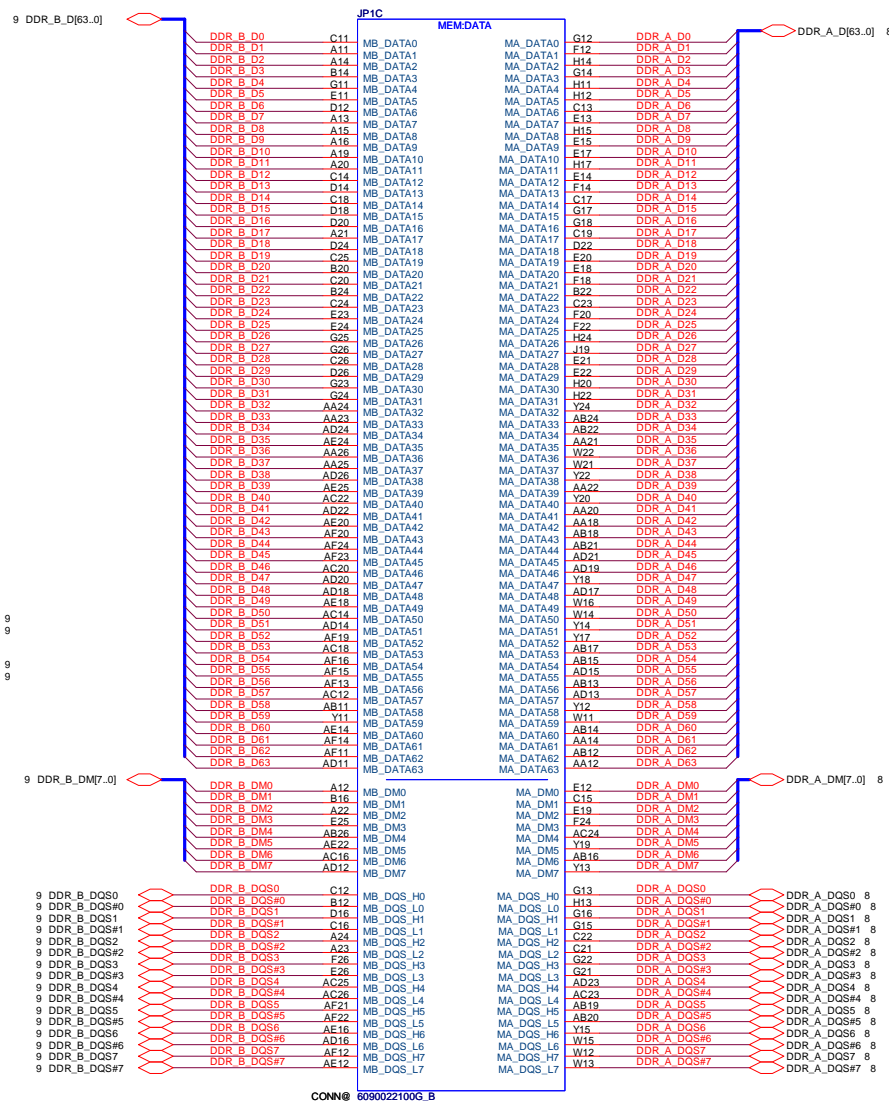
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>AMD CPU S1G2 HT I/F</b>		
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PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH

## Processor DDR2 Memory Interface

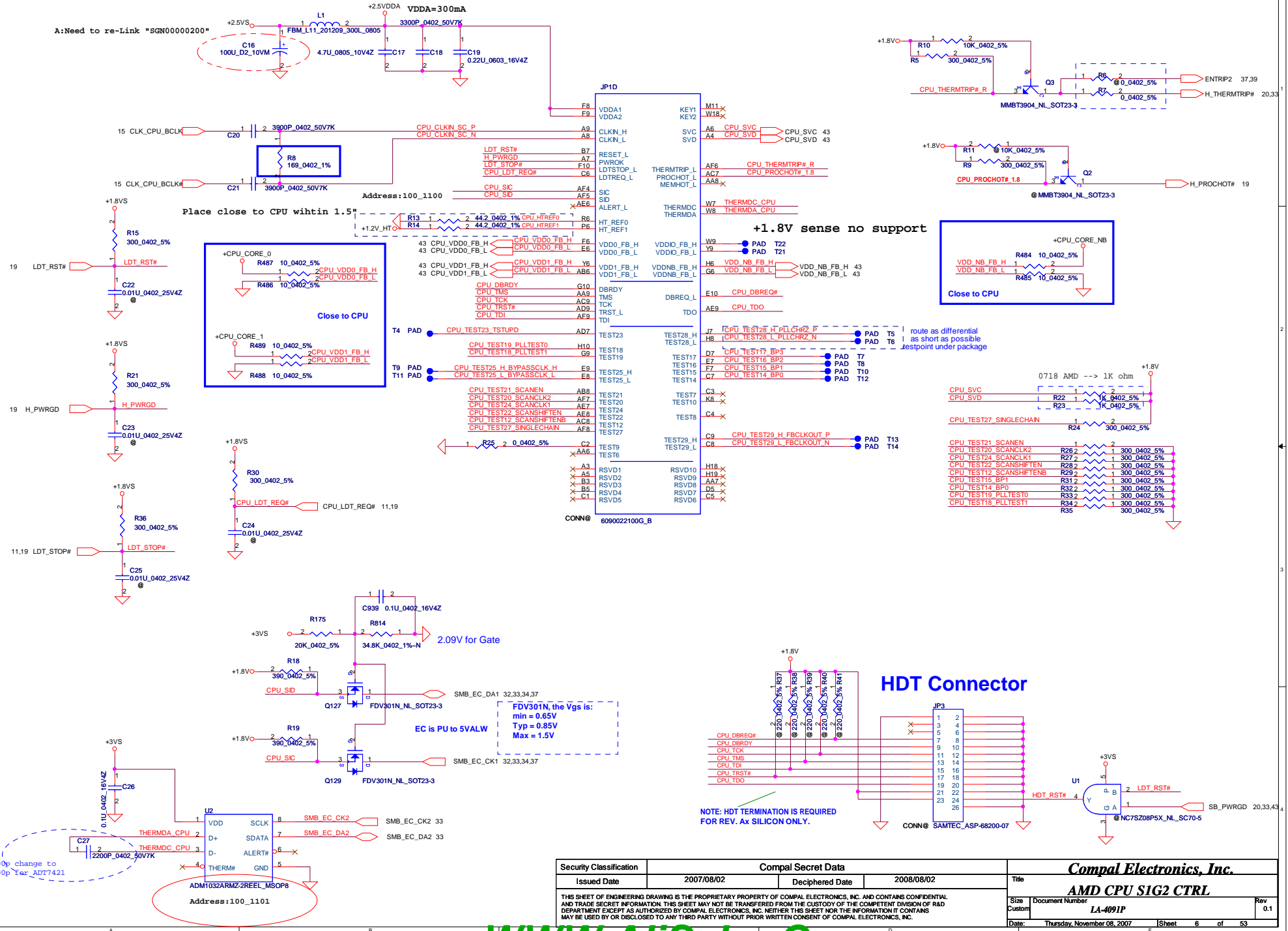


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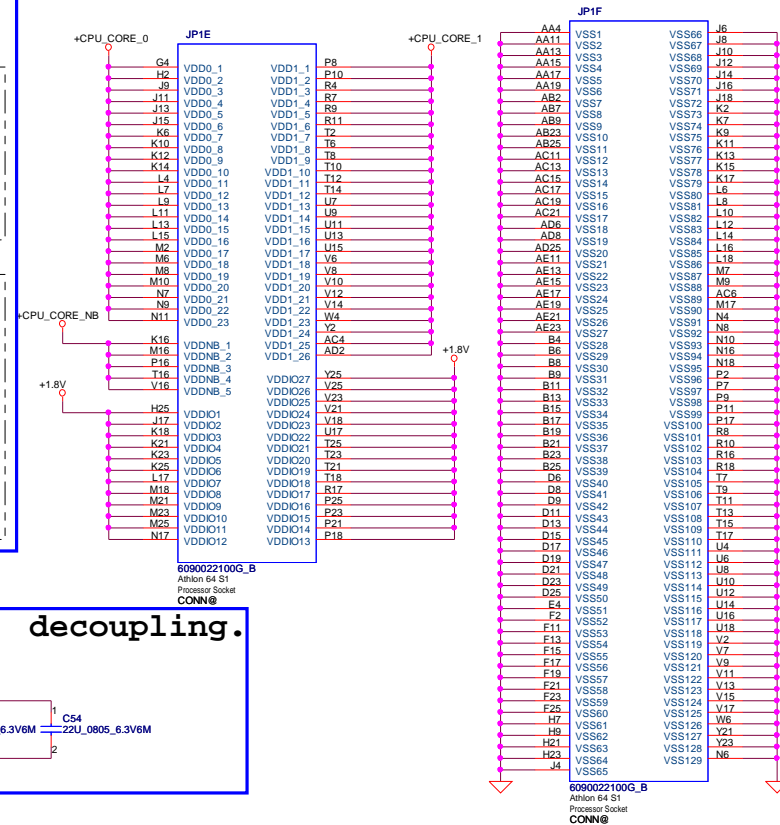
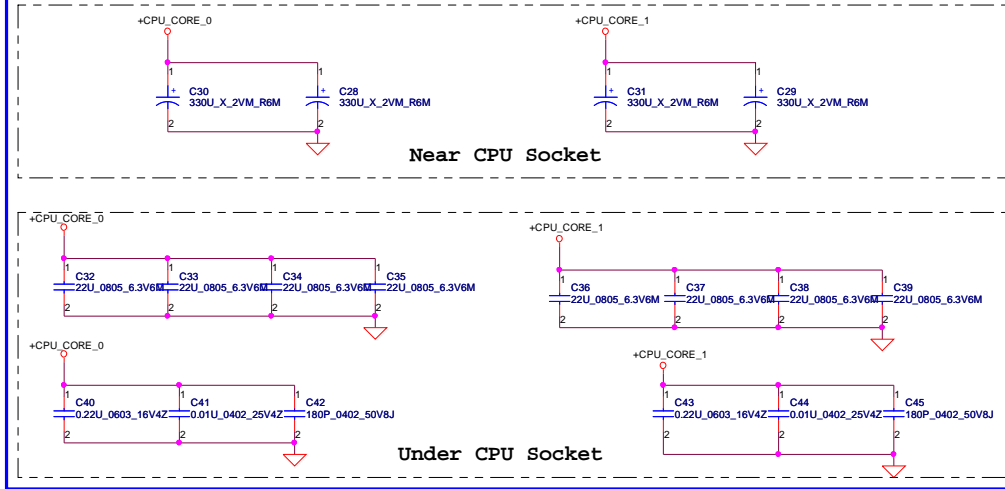


CONN@ 6090022100G F

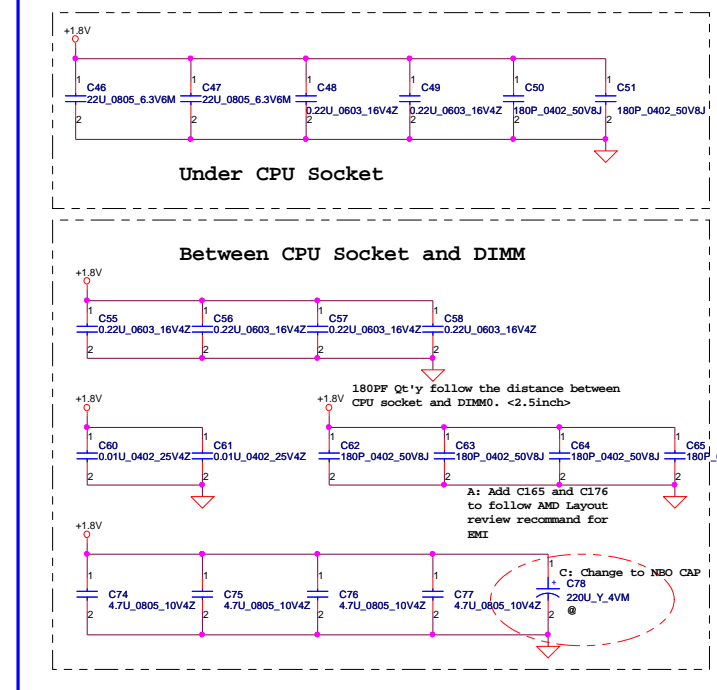
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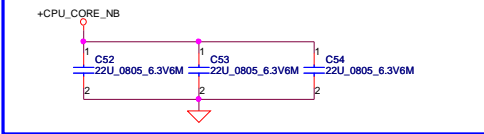
## VDD(+CPU\_CORE) decoupling.



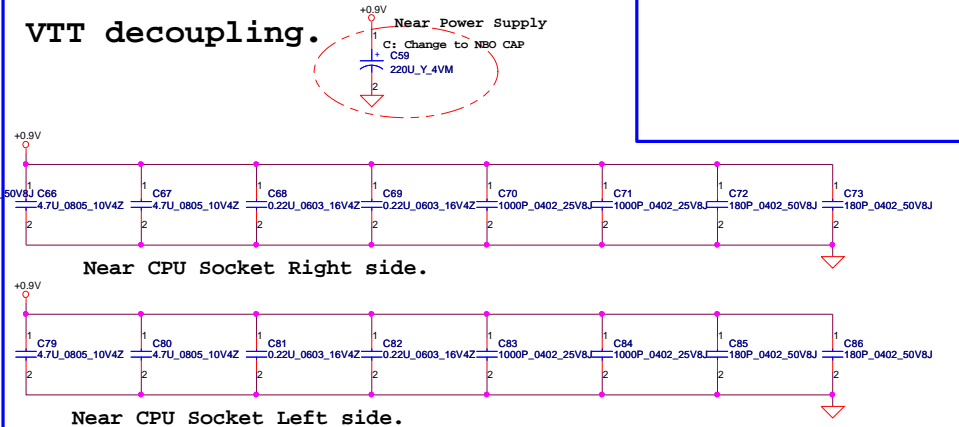
## VDDIO decoupling.



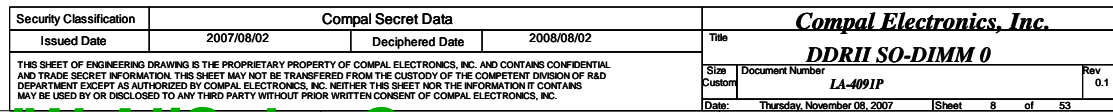
## +CPU\_CORE\_NB decoupling.



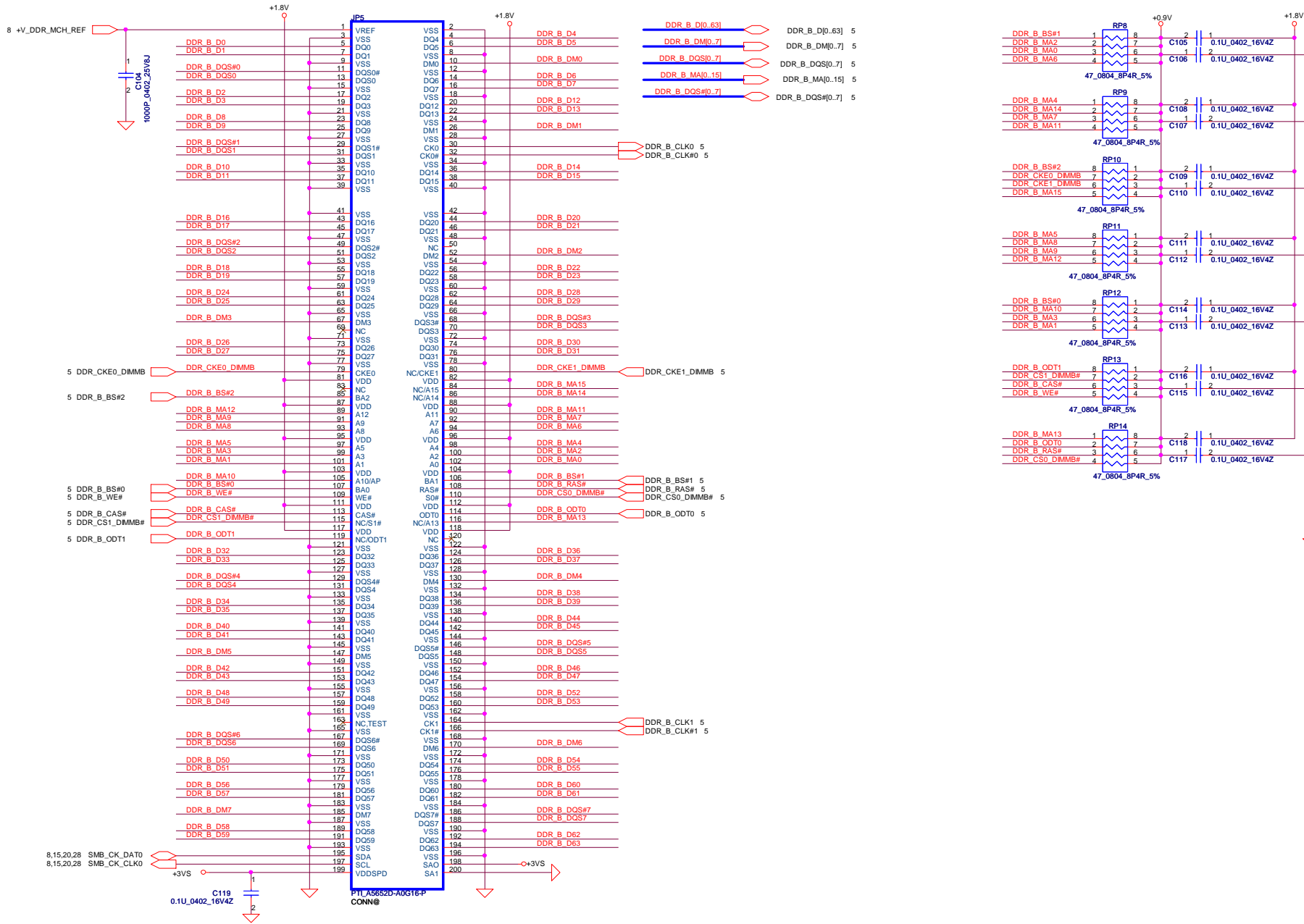
## VTT decoupling.



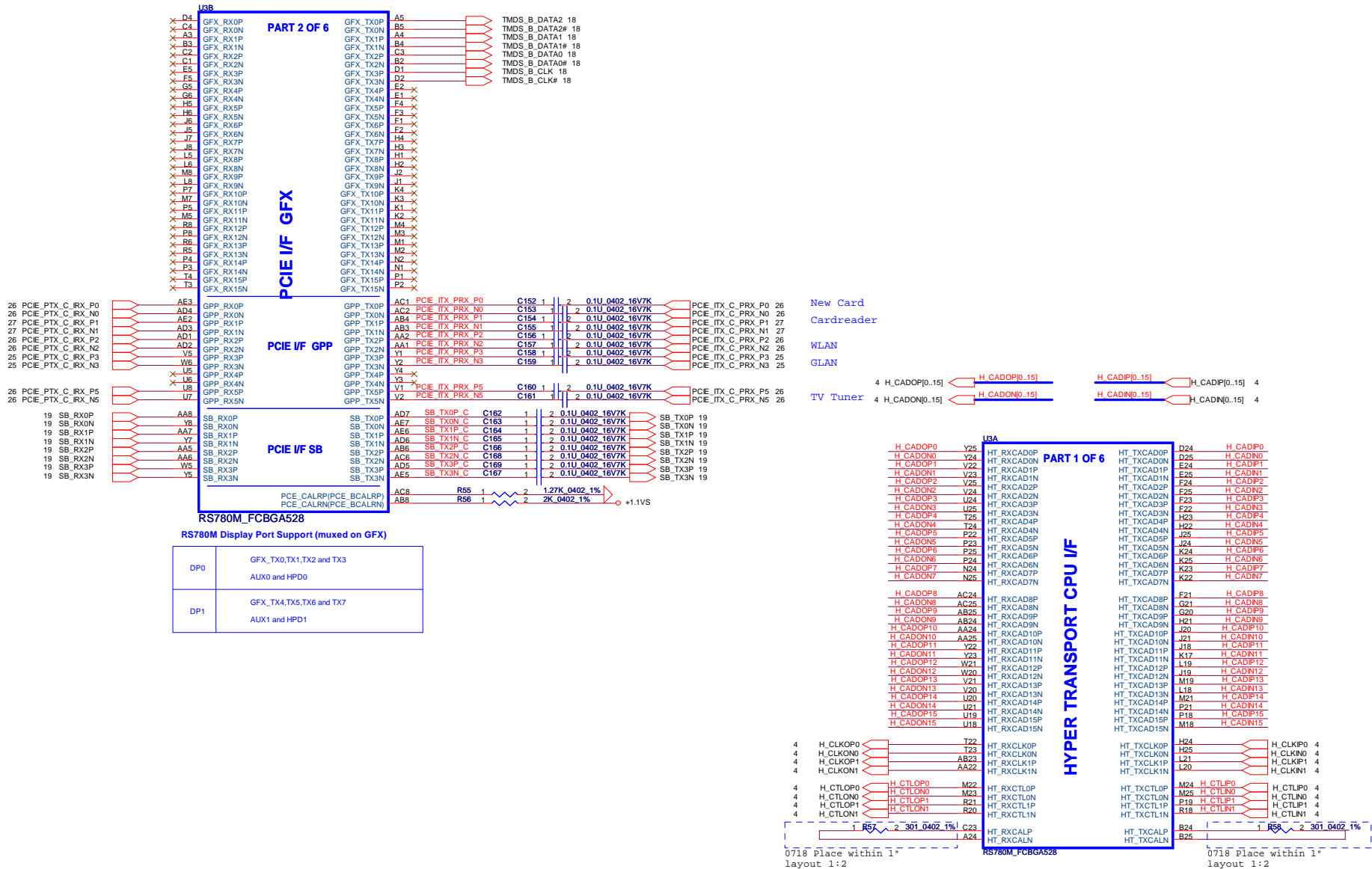
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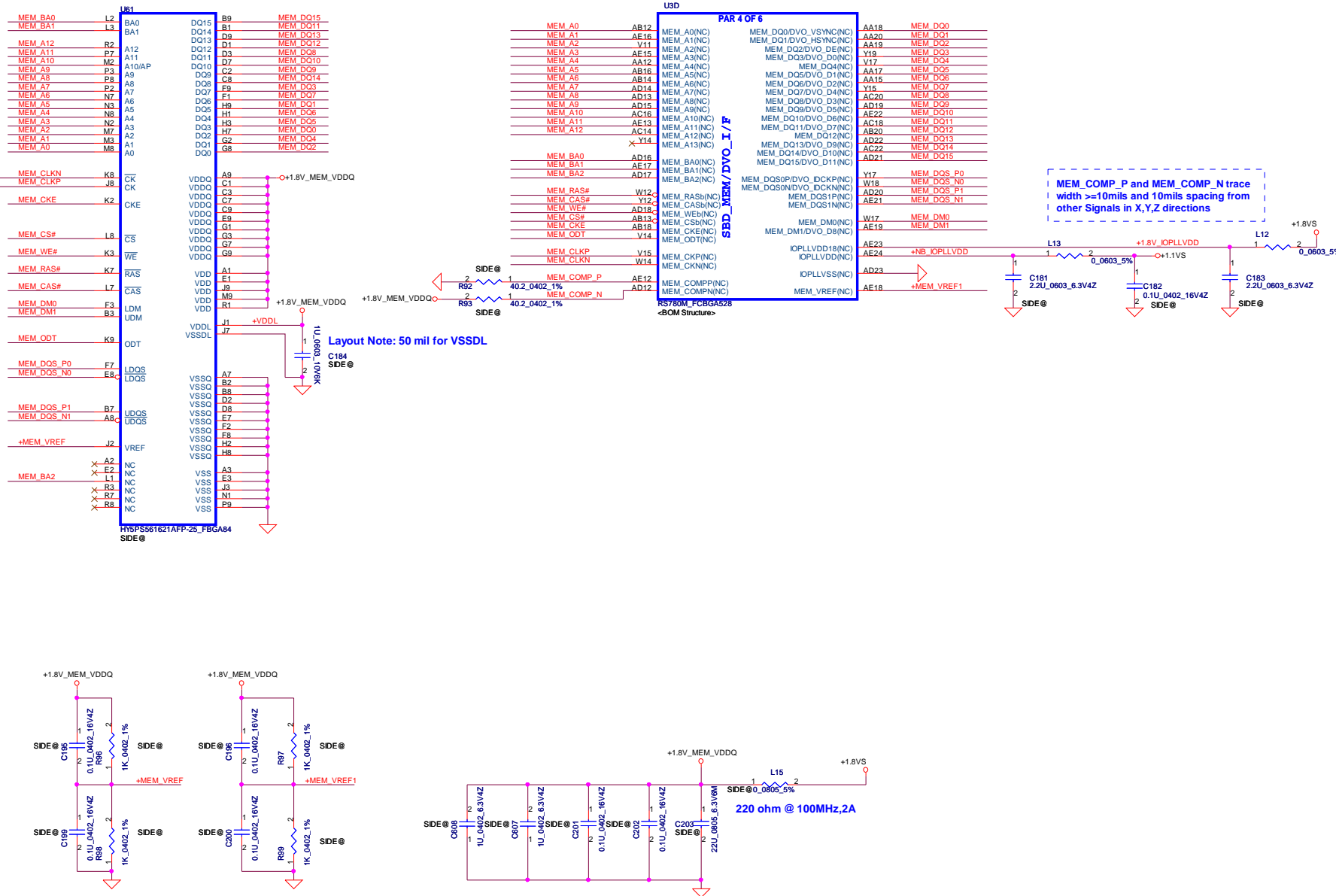


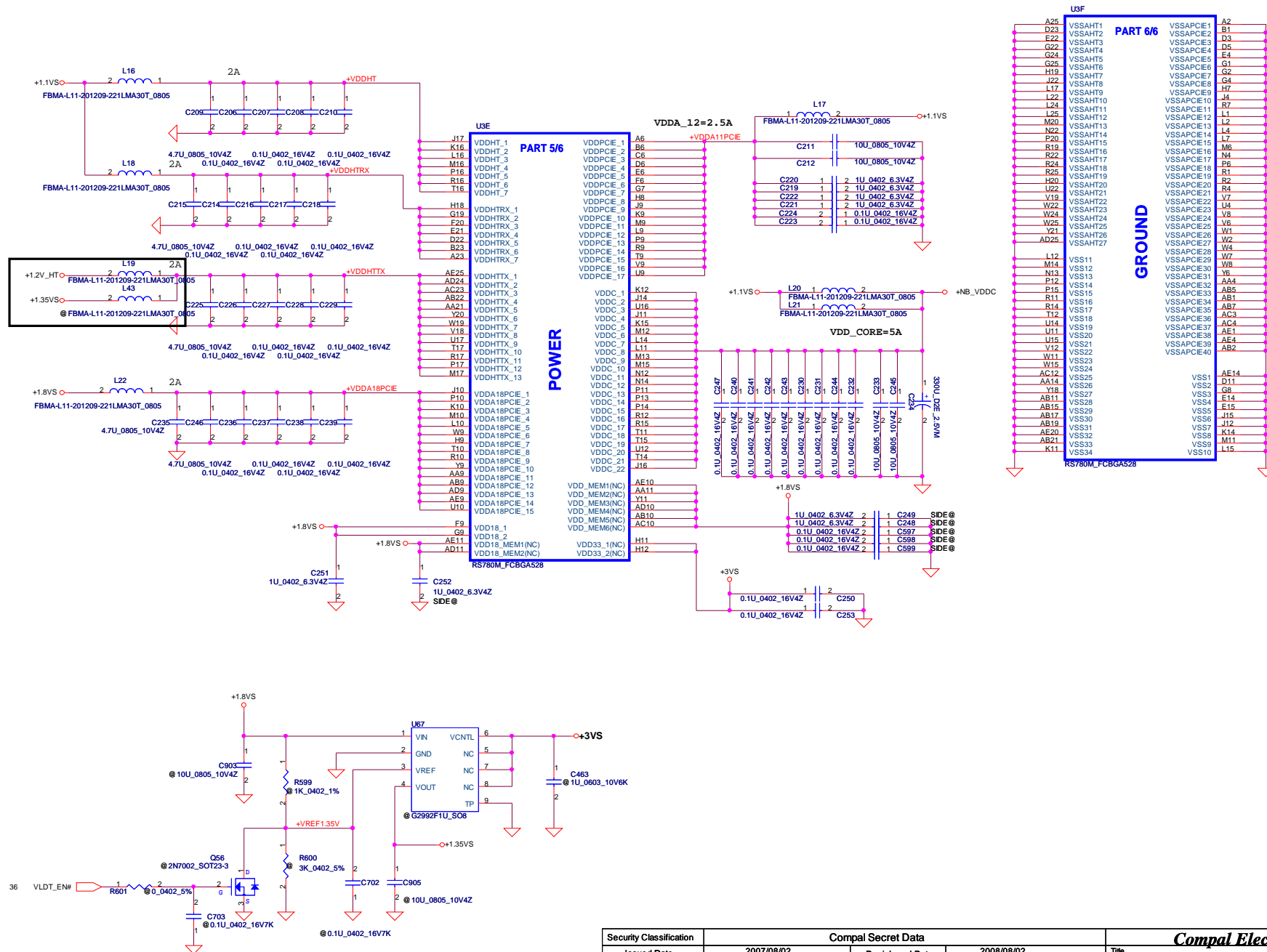
NEED CHECK R68 & R69 WITH AMD

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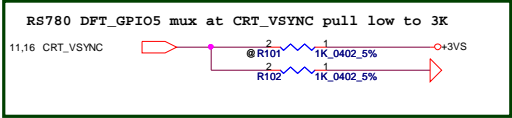


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DFT\_GPIO5:STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb

Enables the Test Debug Bus using GPIO.

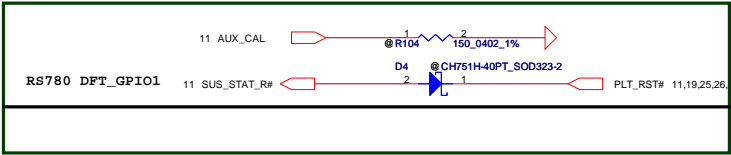
1 : Enable (RX780, RS780)  
0 : Disable (RX780, RS780)  
PIN: RS740-->RS780\_AUX\_CAL; RX780-->NB\_TV\_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

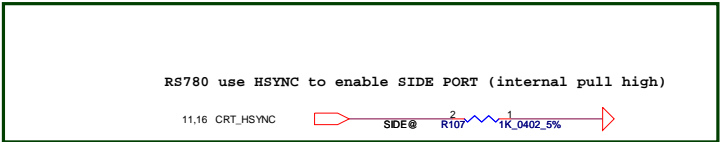
000 : 00001  
001 : 00010  
010 : 01011  
011 : 00100  
100 : 01010  
101 : 01100  
111 : 01011



DFT\_GPIO1: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS740/RX780: DFT\_GPIO1 RS780:SUS\_STAT



DFT\_GPIO0:STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb

RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable

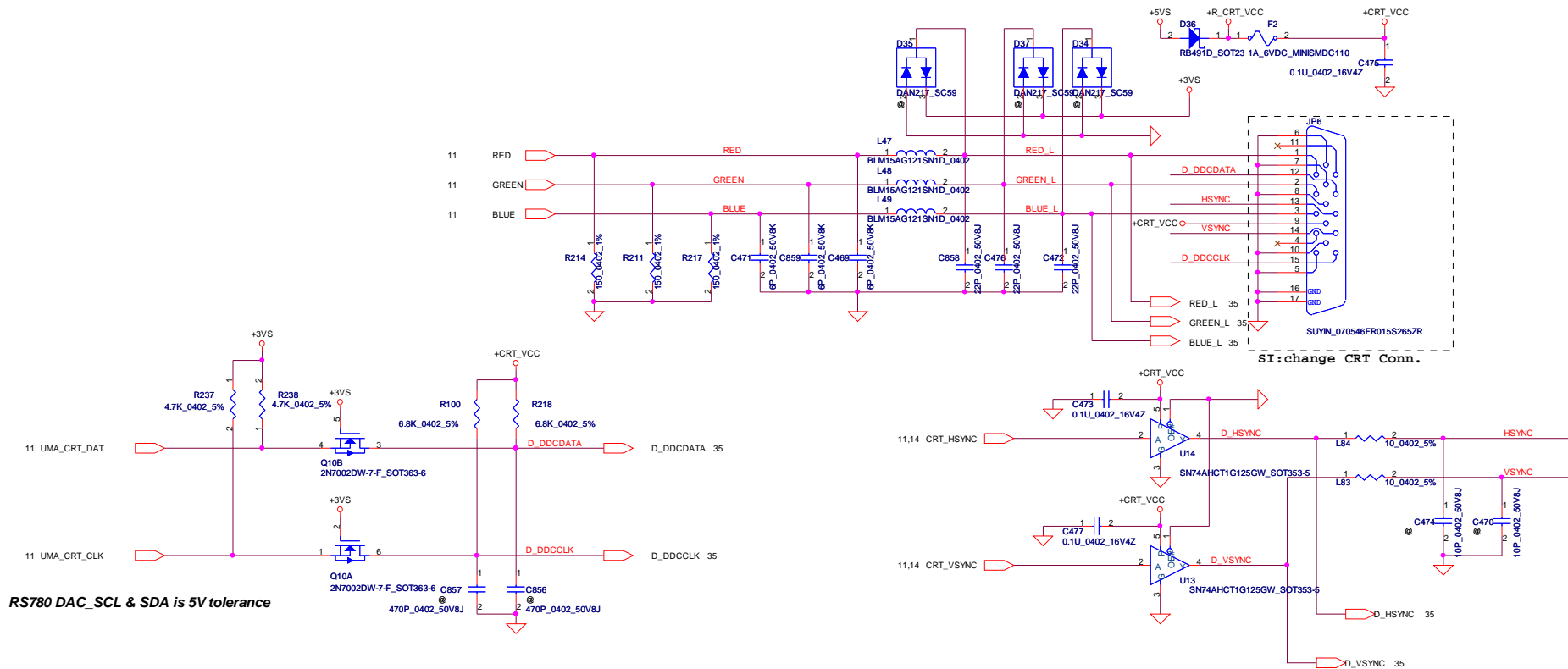
RS780: Enables Side port memory ( RS780 use HSYNC#)

1. Disable (RS780)  
0 : Enable (RS780)

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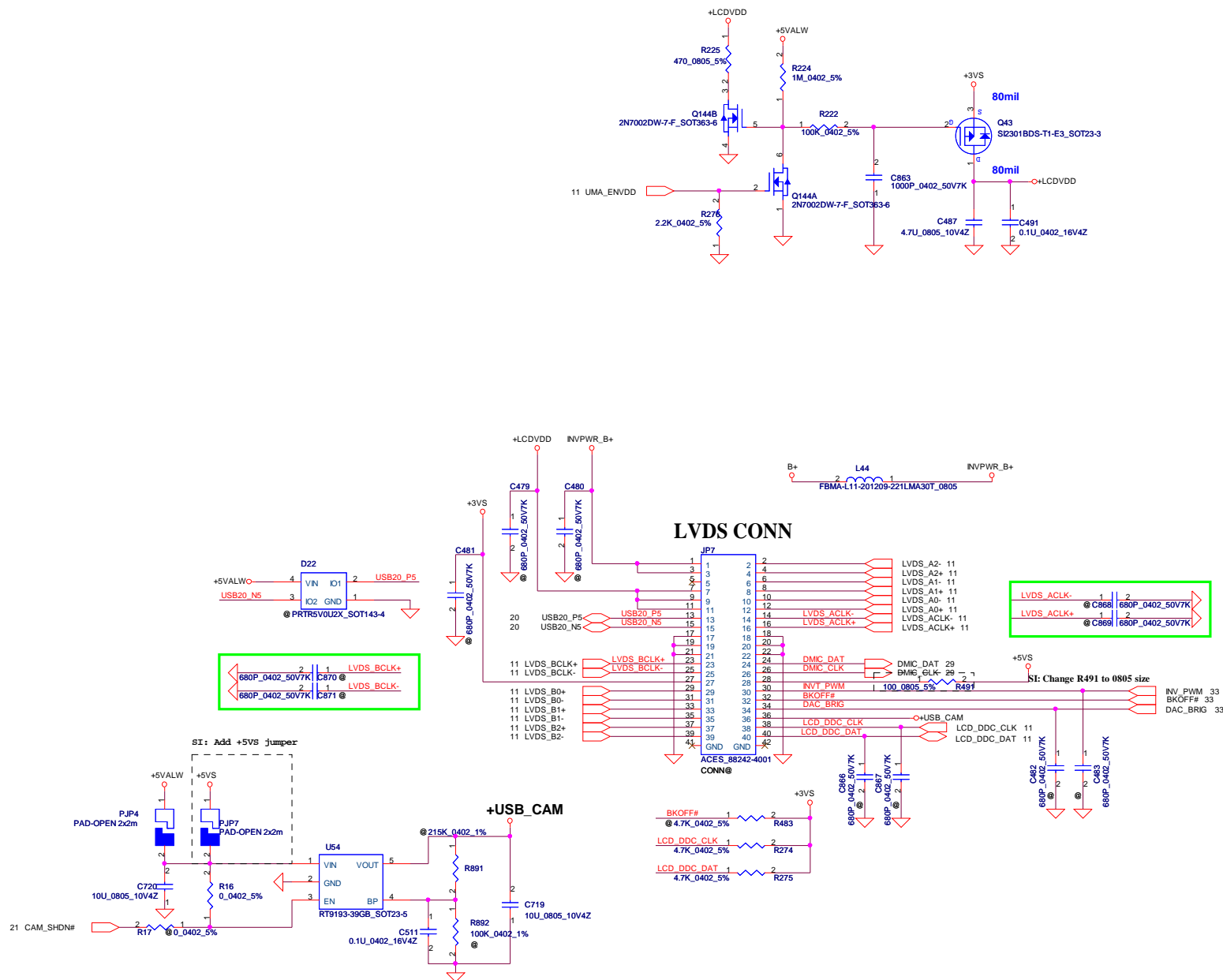
CRT CONNECTOR



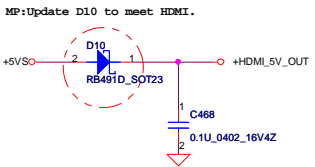
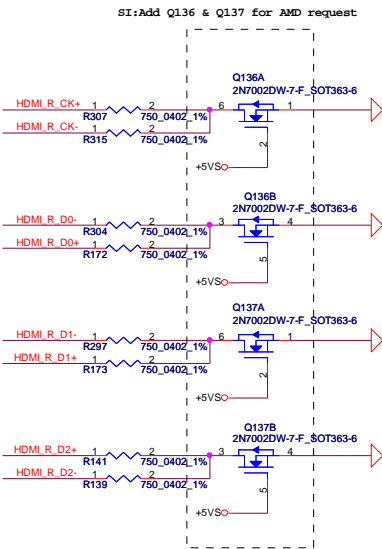
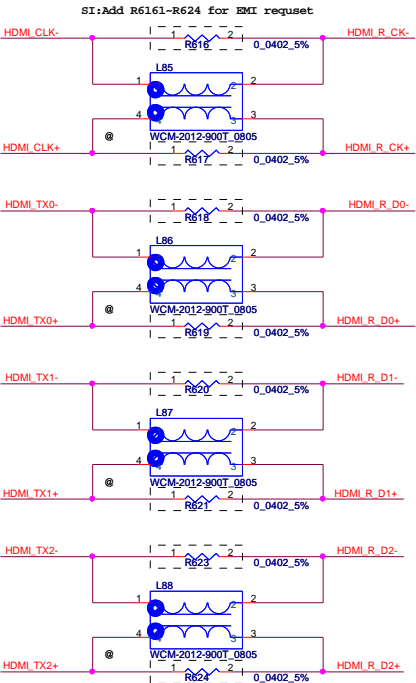
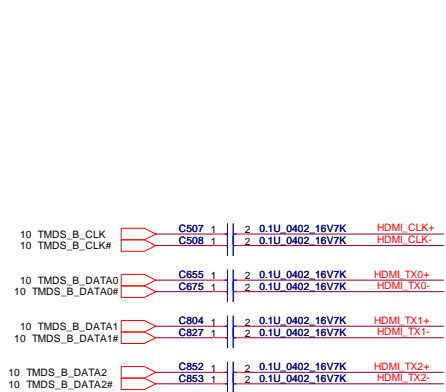
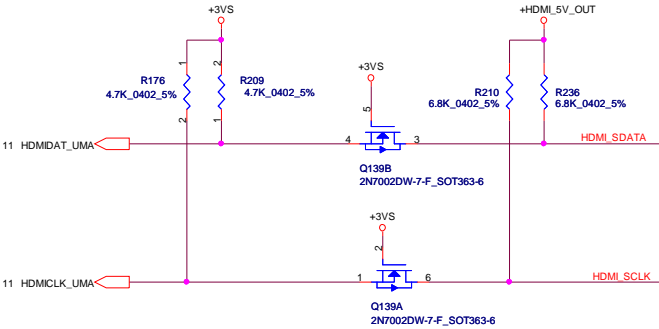
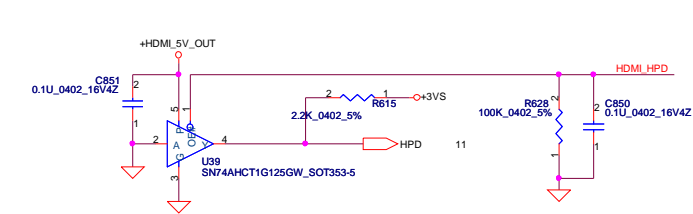
RS780 DAC\_SCL & SDA is 5V tolerance

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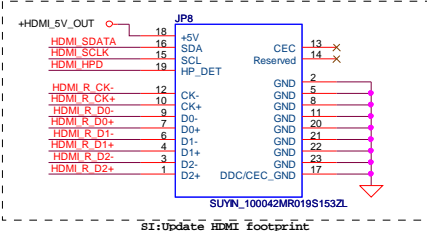




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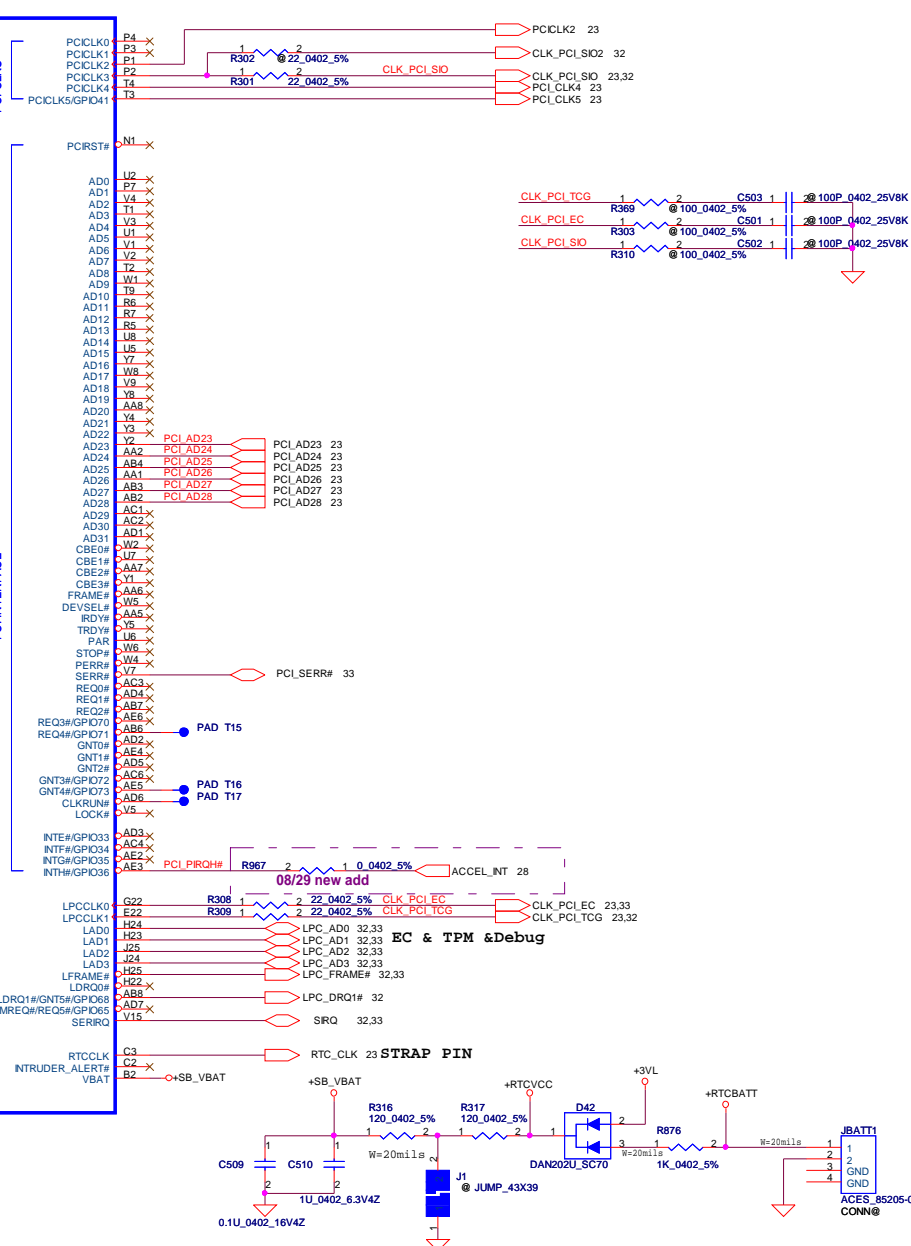
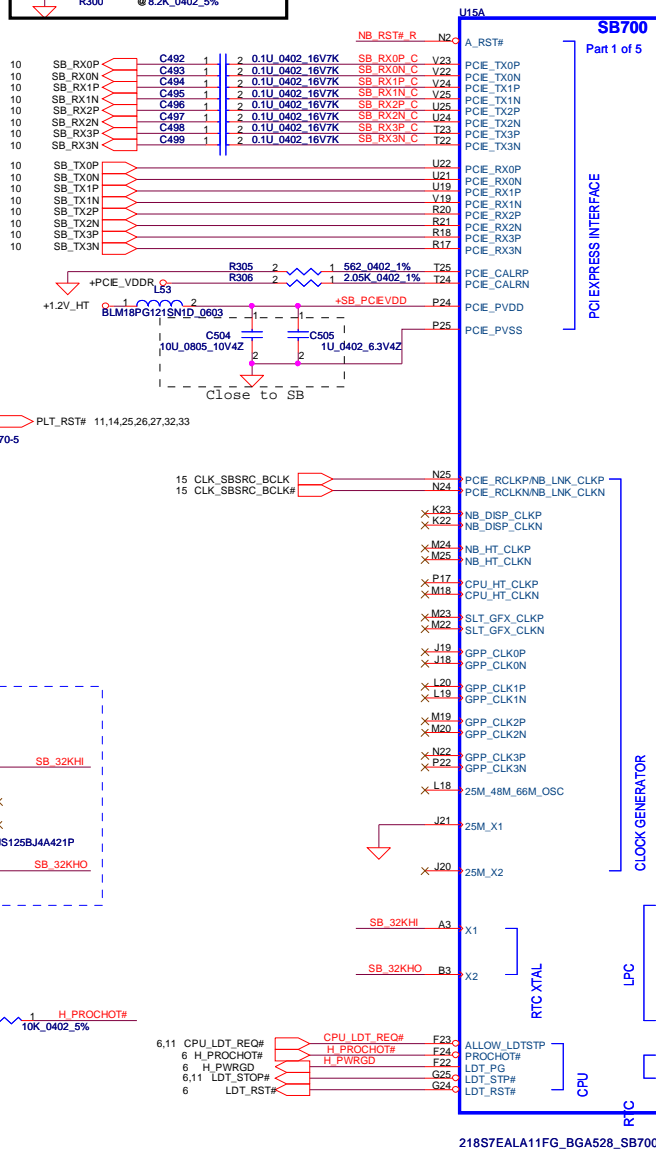
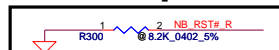


HDMI Connector

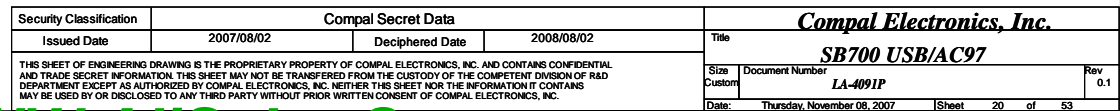


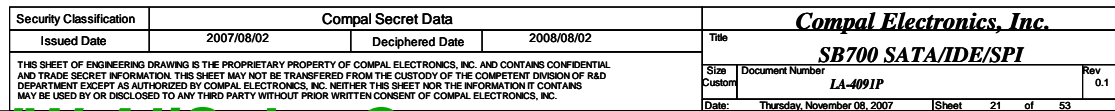
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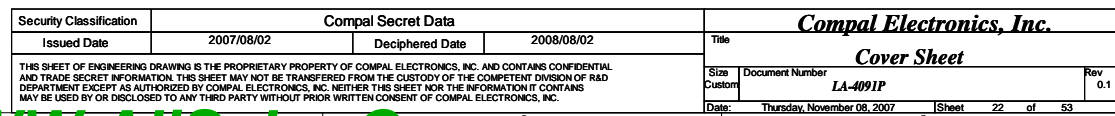
Check AMD need pull low or not



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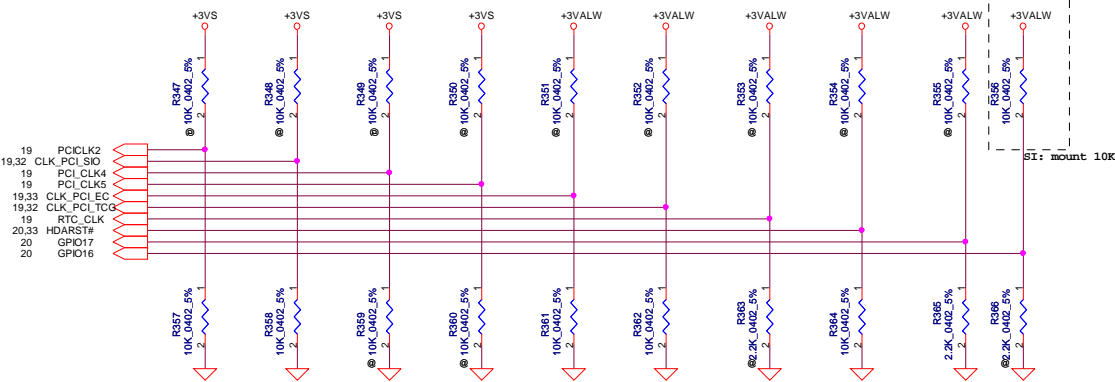




REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

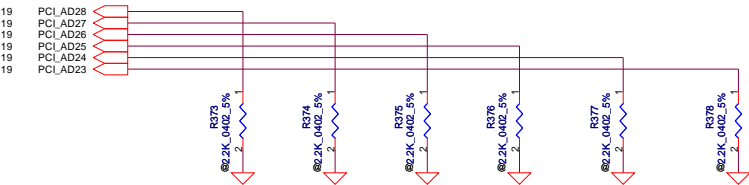
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	EC ENABLED	Internal pull up H,H = Reserved  H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT  DEFAULT	CLKGEN DISABLED  DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM



DEBUG STRAPS

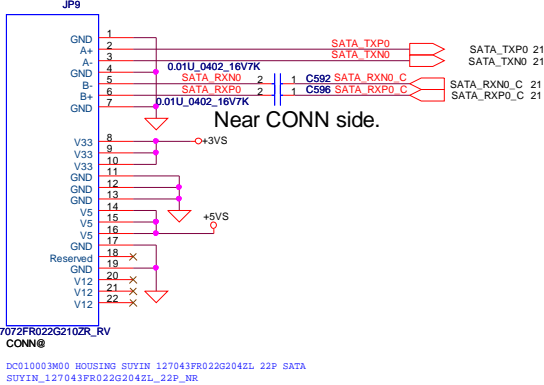
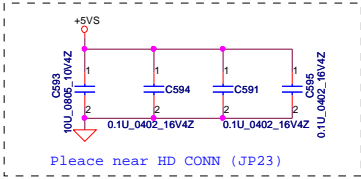
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

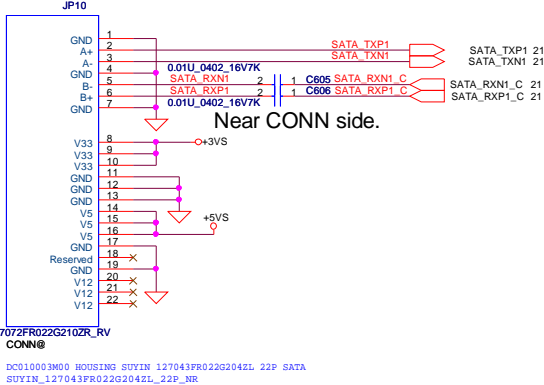
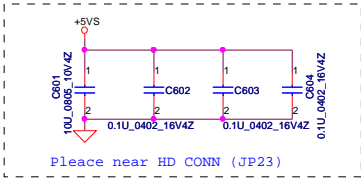


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				Size Custom	Document Number LA-4091P
				Date Thursday, November 08, 2007	Rev 0.1
				Sheet	23 of 53

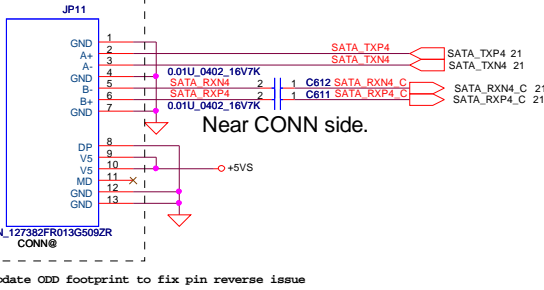
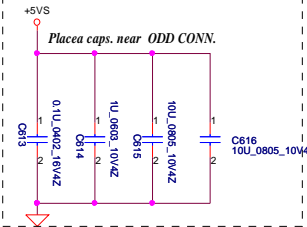
HDD Connector



2nd HDD Connector-option

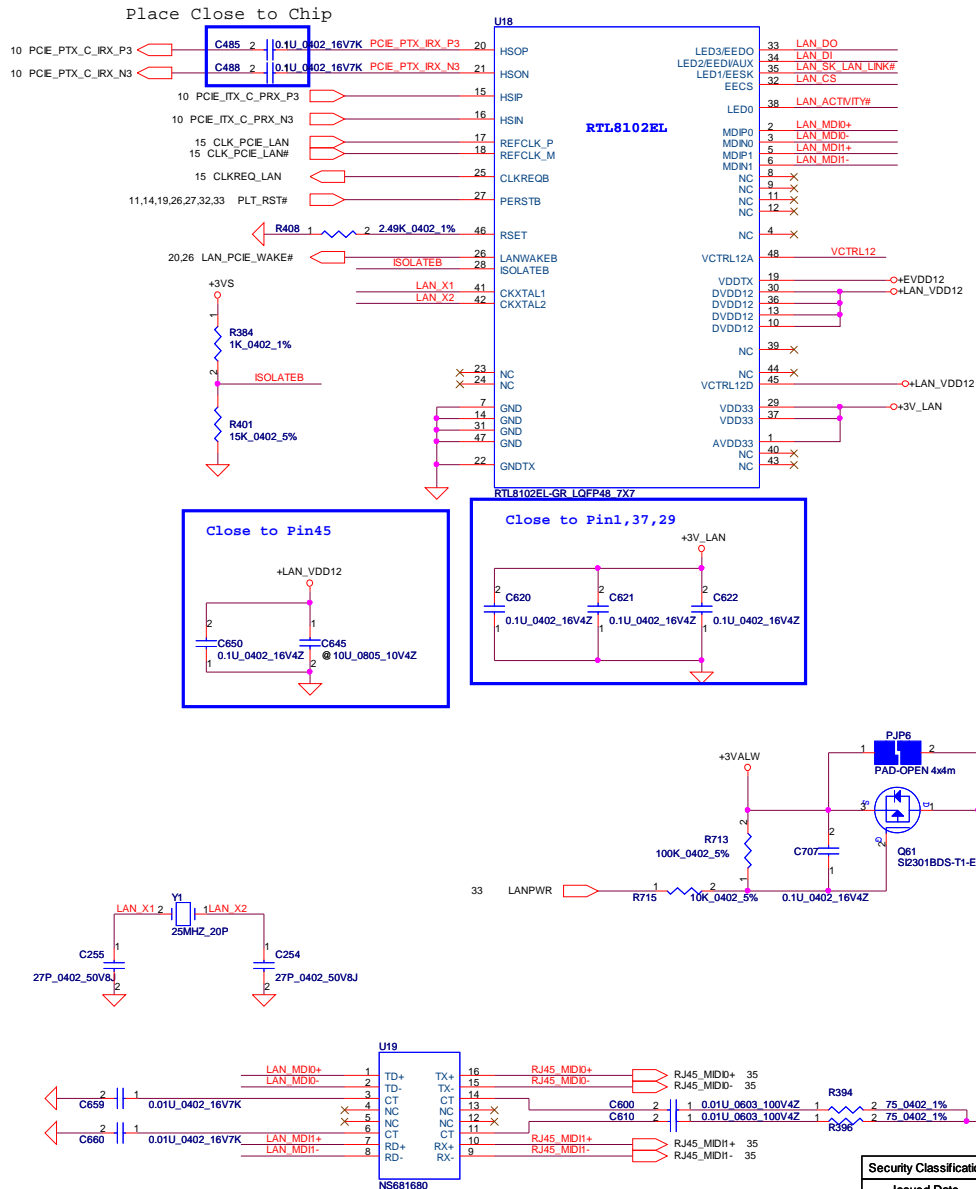


CD-ROM Connector



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				Size	Rev
				Custom	0.1
Date		Thursday, November 08, 2007		Sheet	24 of 53

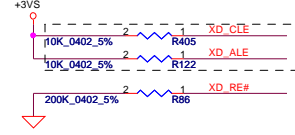
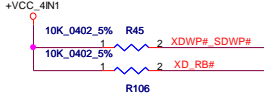
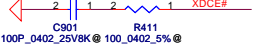
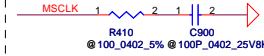
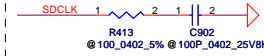
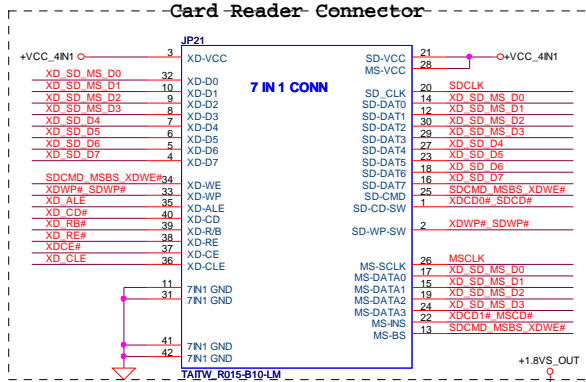




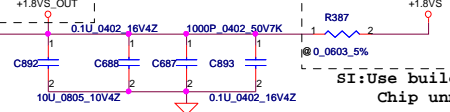
## Mini Card---TV tuner

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>Mini-Card/Mini-PCI/Express Card</b>	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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SI:Per ME request change  
JP21 to new one

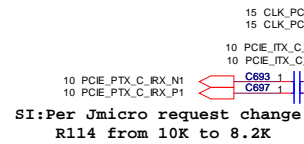


SI:Per Jmicro request change  
R405 & R122 from 200K to 10K



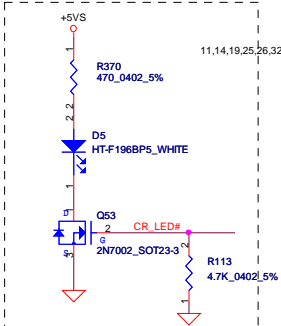
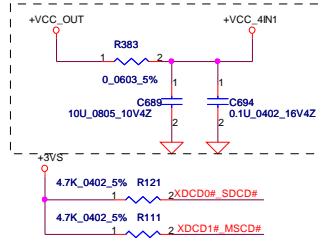
SI:Use build in Regulator  
Chip unmount R387

**Power Circuit**



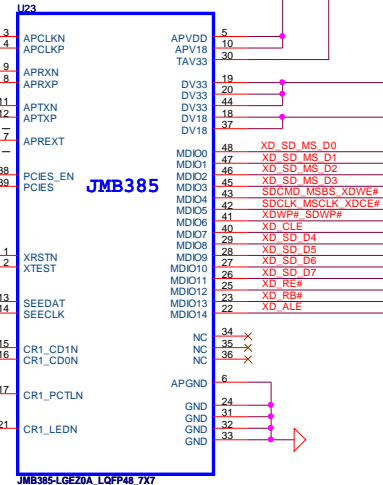
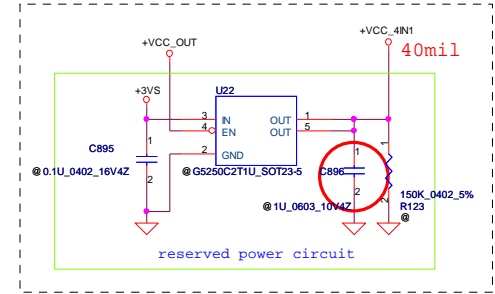
SI:Per Jmicro request change  
R114 from 10K to 8.2K

SI:Use build in Regulator  
Chip mount R383,C689,C694

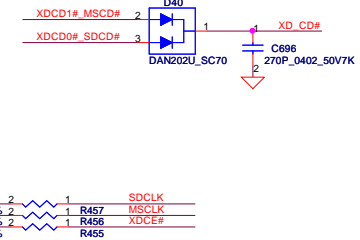


SI:Use new chip ,change to  
High active control

SI:Use build in Regulator  
Chip unmount U22 and relation parts

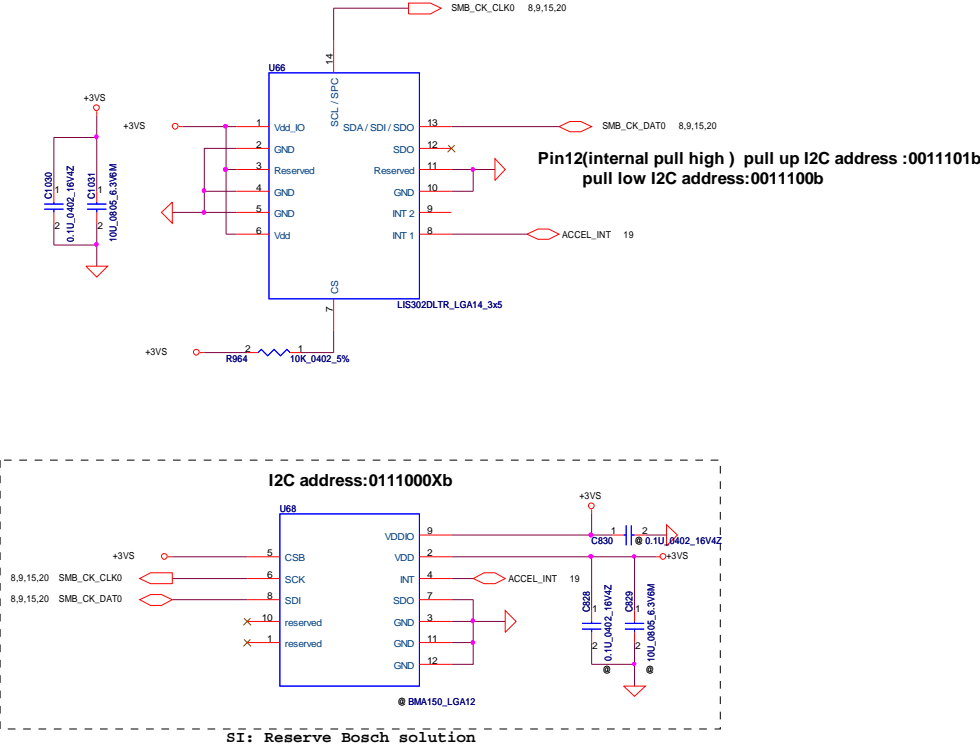


SI: Use 0740 date code chip



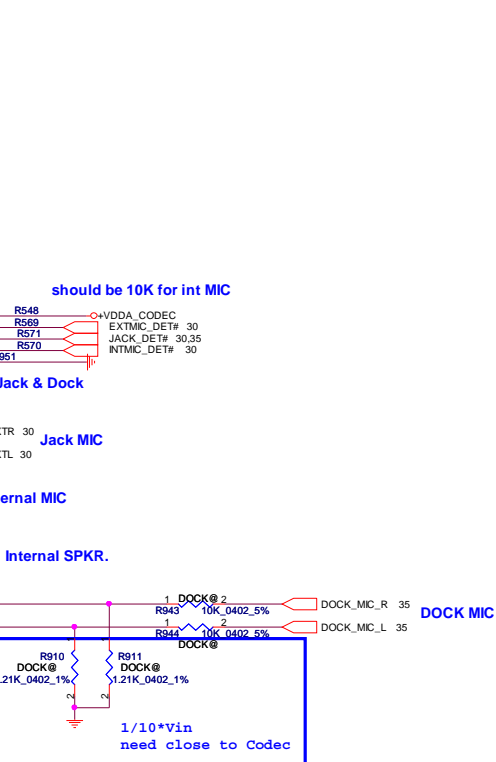
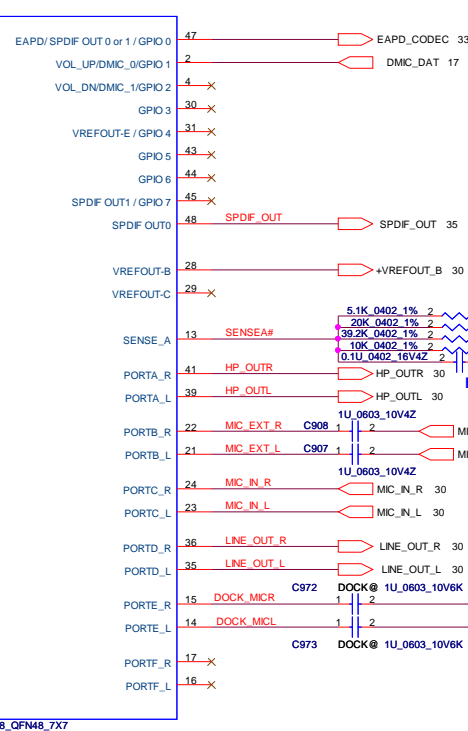
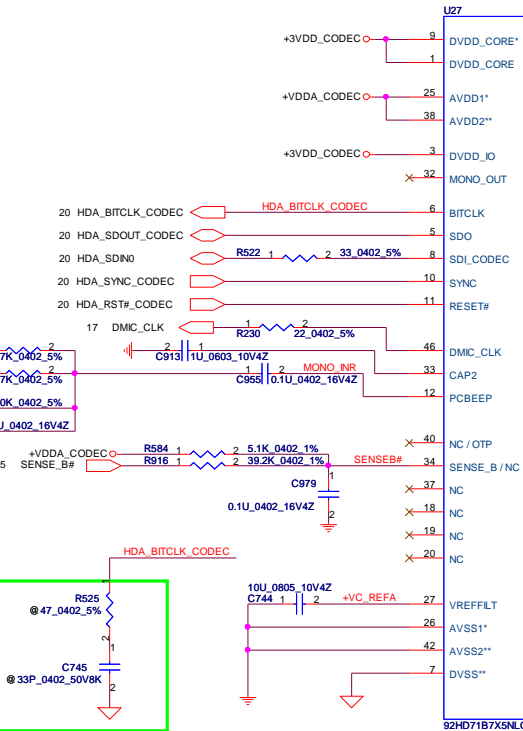
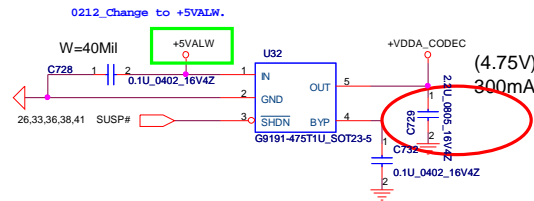
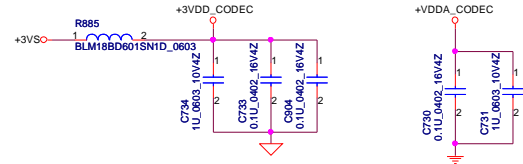
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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Size	Custom	Document Number	LA-4091P	Rev	0.1
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ACCELEROMETER

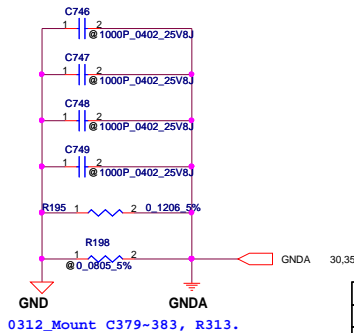


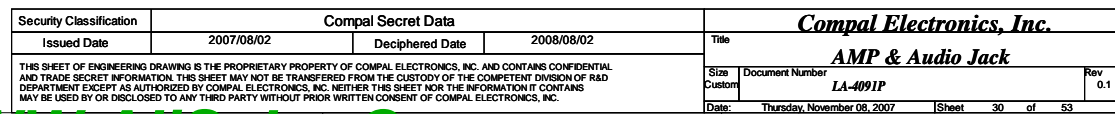
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	R5C833_1394
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				Date: Thursday, November 06, 2007	Sheet 28 of 53

# CODEC POWER

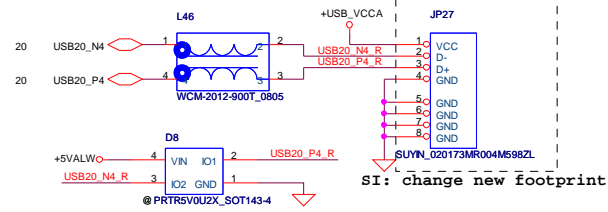
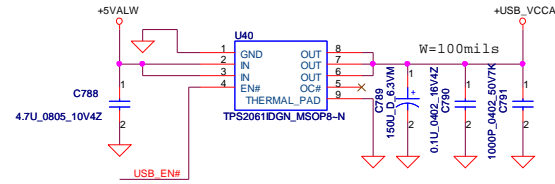


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

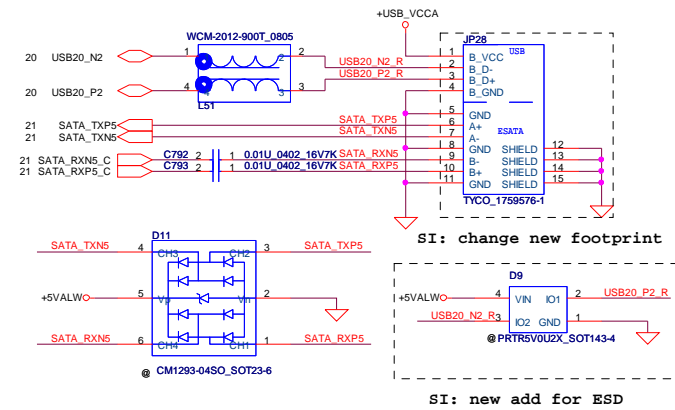




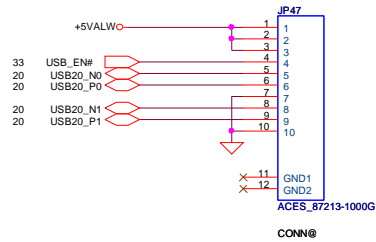
# Left side USB CONNECTOR 0



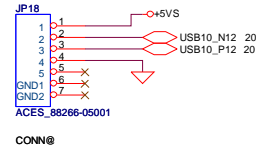
# Left side ESATA/USB combination Connector



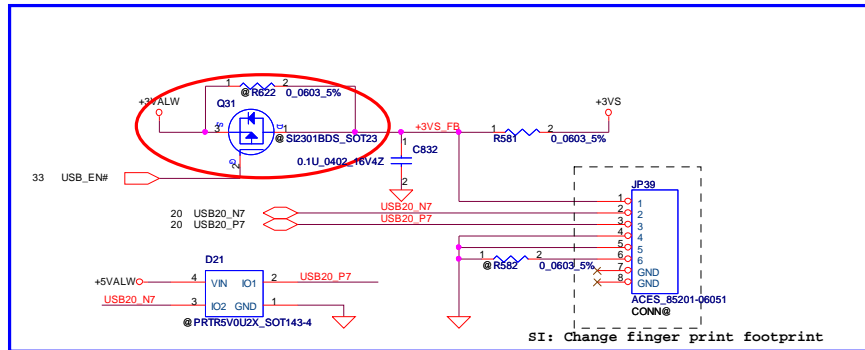
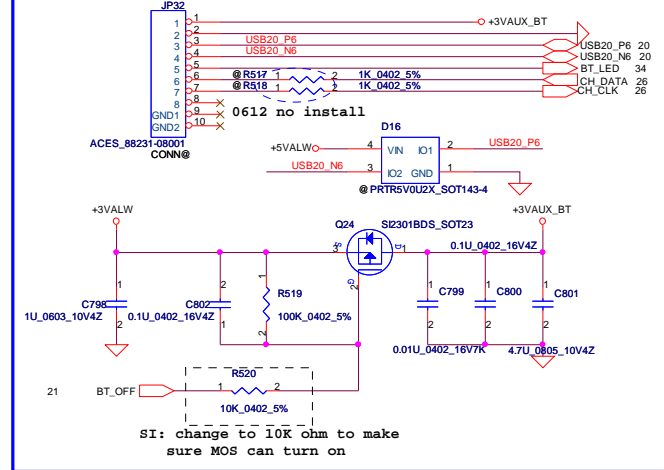
## USB Board Conn



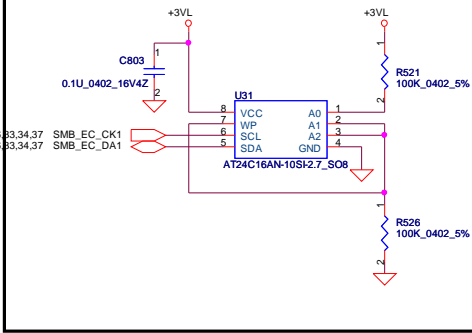
## Touch screen



## BT Connector

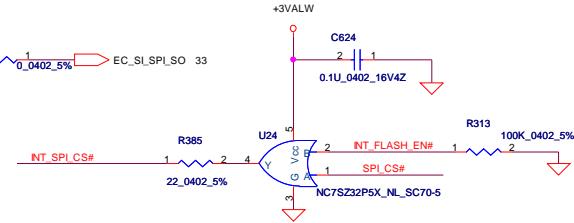
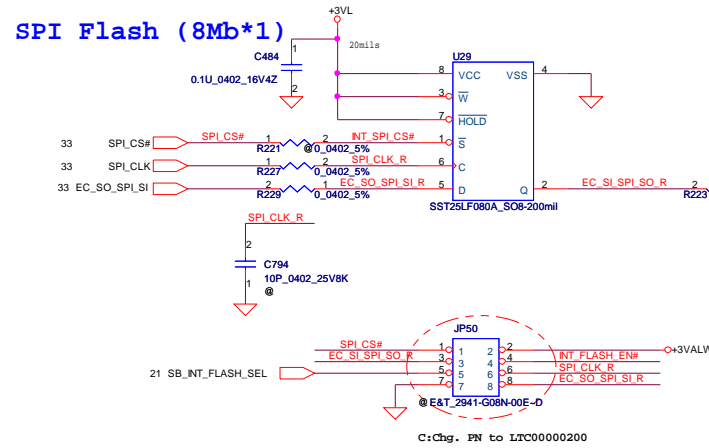


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Cover Sheet	
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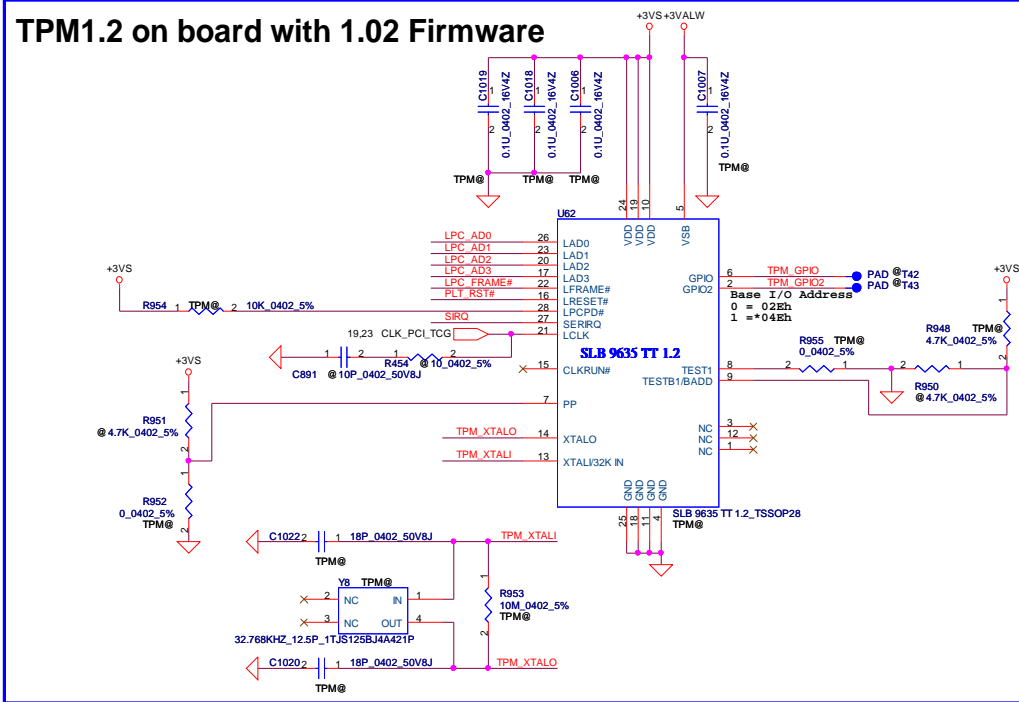


EEPROM need merge to BIOS ROM

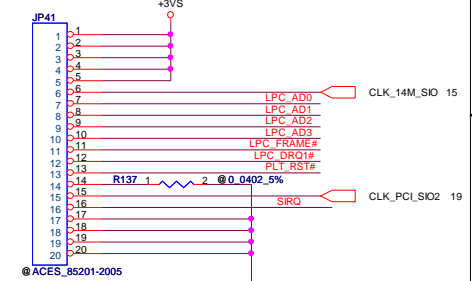
### SPI Flash (8Mb\*1)



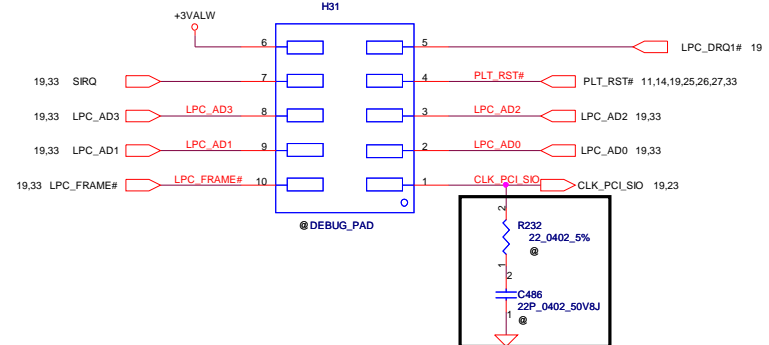
### TPM1.2 on board with 1.02 Firmware



### LPC Debug Port

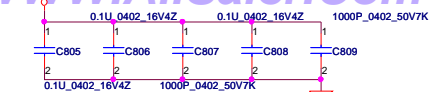


### LPC Debug Port

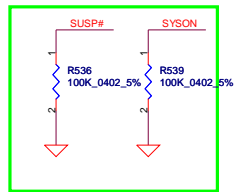
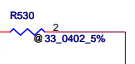
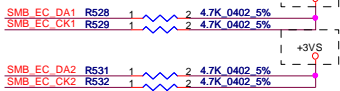


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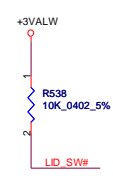




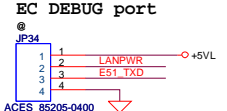
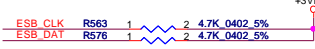
SI: Change to +5V\_L to support read battery in batt mode



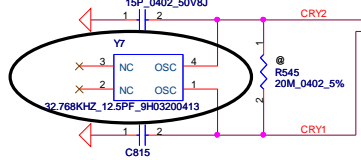
0205 Add Pull down R402 for SUSP#.



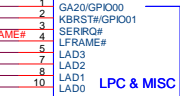
0205 Add Pull down R402 for SUSP#.



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



EC DEBUG port



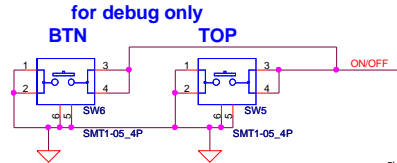
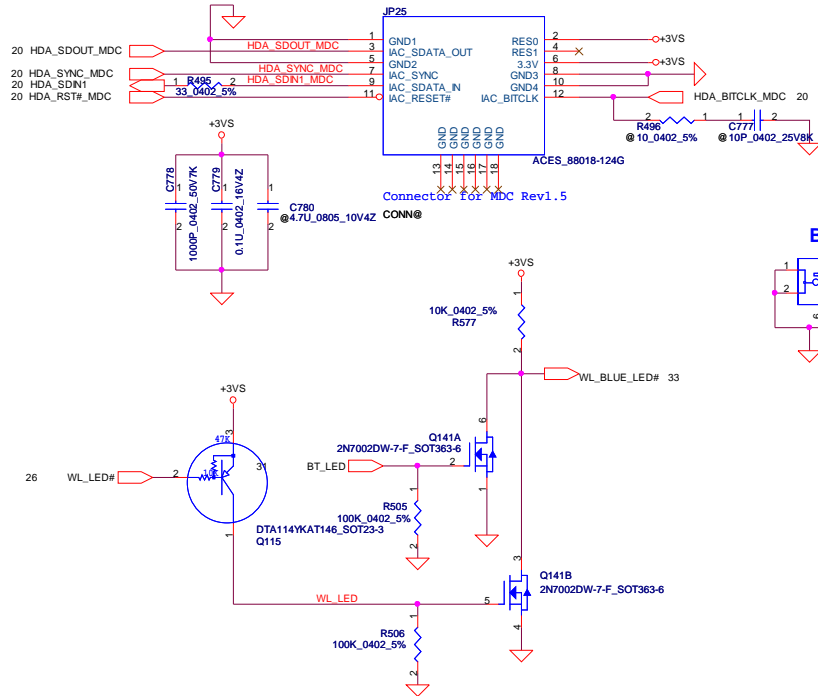
EC DEBUG port



EC DEBUG port

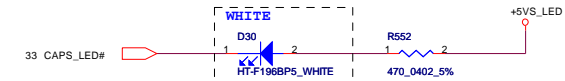


Change type 4/25



## CAPS LOCK LED

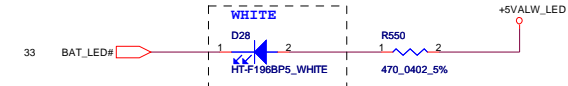
SI: Modify LED footprint



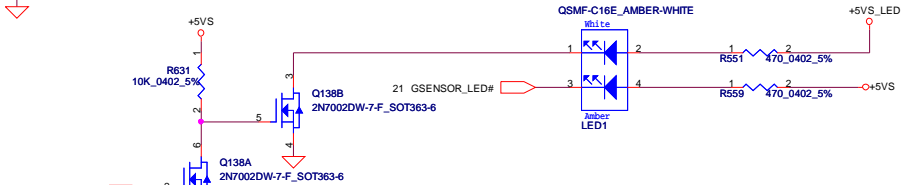
## POWER LED(Left 1)



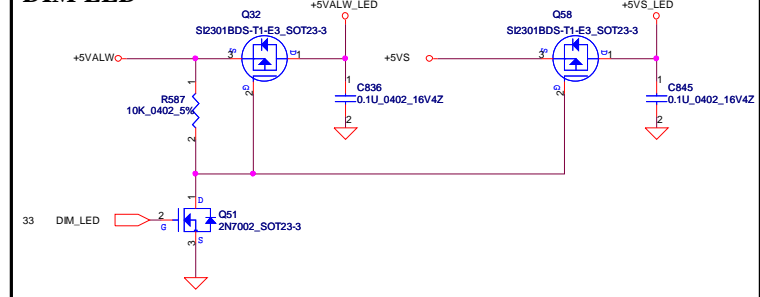
## Battery Charge LED(Left 2)



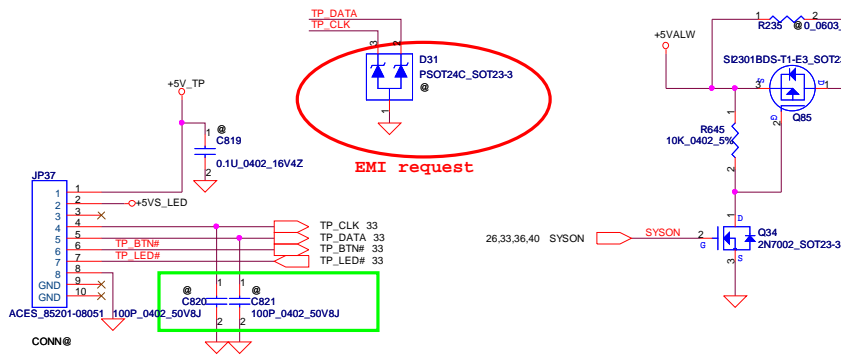
## HDD LED(Left 3)



## DIM LED

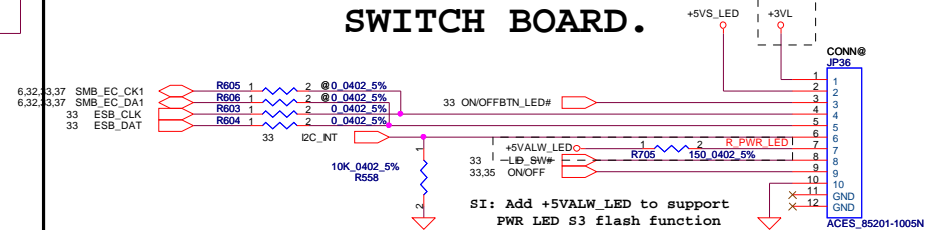


## T/P Board (Inculde T/P\_ON/OFF)



SI: Change to +3VL to support Qplay bottom boot in BATT mode

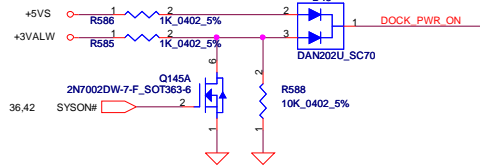
## SWITCH BOARD.



SI: Add +5VALW\_LED to support PWR LED S3 flash function

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# Atlas/ Saturn Dock



**DOCK\_PWR\_ON Spec**  
0V = Notebook S4/S5, Dock off  
2.5V = Notebook S3, Dock on  
4V = Notebook S0, Dock on

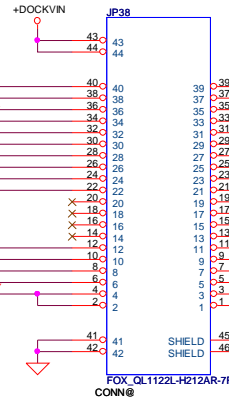
16 GREEN\_L  
16 RED\_L  
16 BLUE\_L  
16 D\_HSYNC  
16 D\_DDCCLK  
20 USB20\_N3  
16 D\_VSYNC  
20 USB20\_P3

25 RJ45\_MIDI+  
25 RJ45\_MIDI-  
25 RJ45\_MIDI0+  
25 RJ45\_MIDI0-

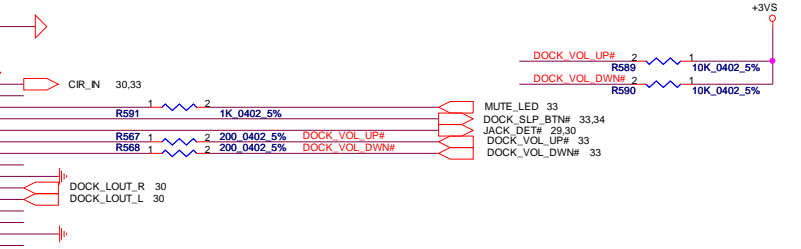
PJP5  
PAD-OPEN 2x2m

D\_DDCDATA  
D\_HSYNC  
D\_DDCCLK  
USB20\_N3  
D\_VSYNC  
USB20\_P3

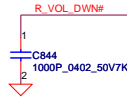
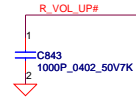
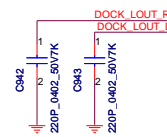
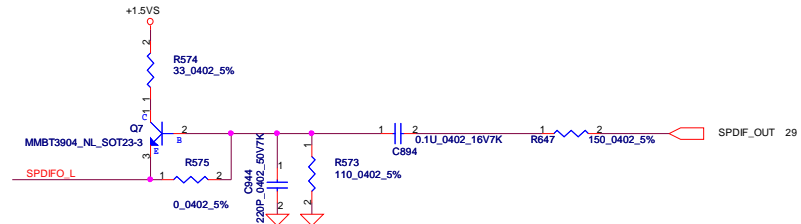
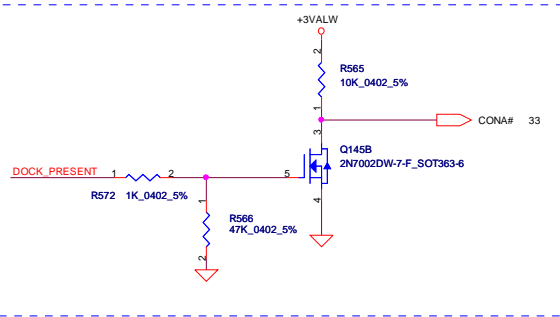
RJ45\_MIDI+  
RJ45\_MIDI-  
RJ45\_MIDI0+  
RJ45\_MIDI0-  
AV\_BATTERY



need change to reverse type connector

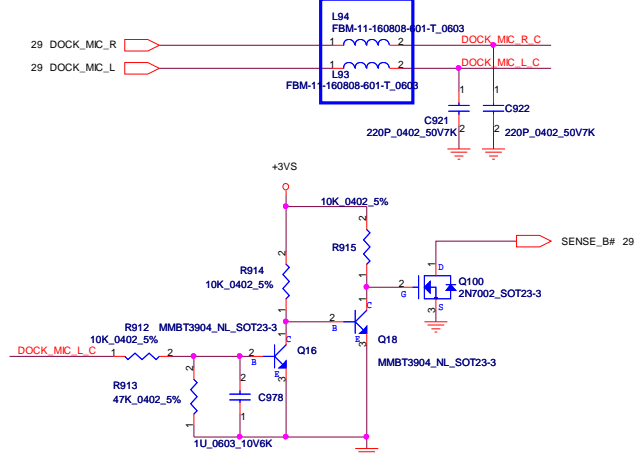


MUTE\_LED 33  
DOCK\_SLP\_BTN# 33,34  
JACK\_DET# 29,30  
DOCK\_VOL\_UP# 33  
DOCK\_VOL\_DWN# 33



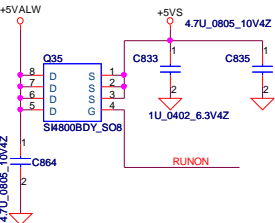
## MIC\_Dock

Need 600 Ohm 500 mA

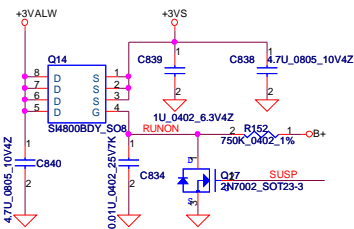


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Issued Date	2007/08/02	Deciphered Date	2008/08/02	DOCK CONN	
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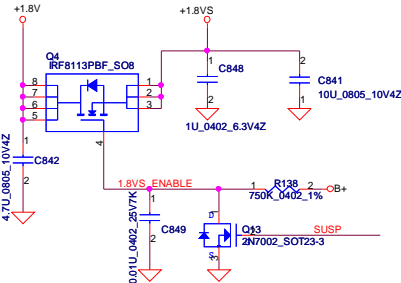
+5VALW TO +5VS



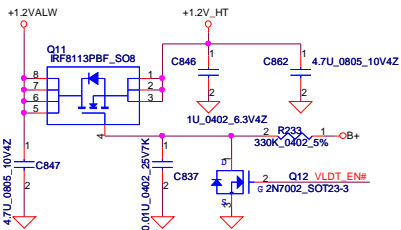
+3VALW TO +3VS



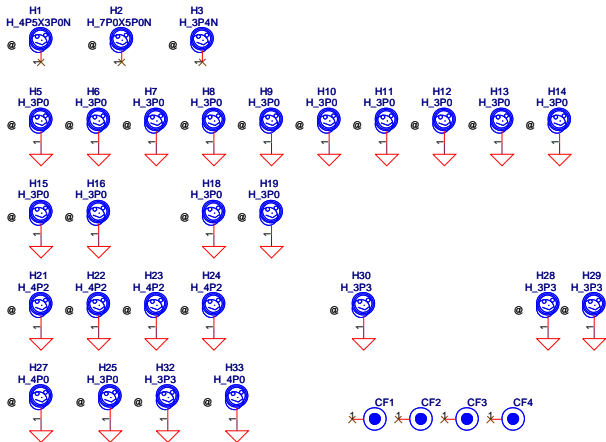
+1.8V TO +1.8VS



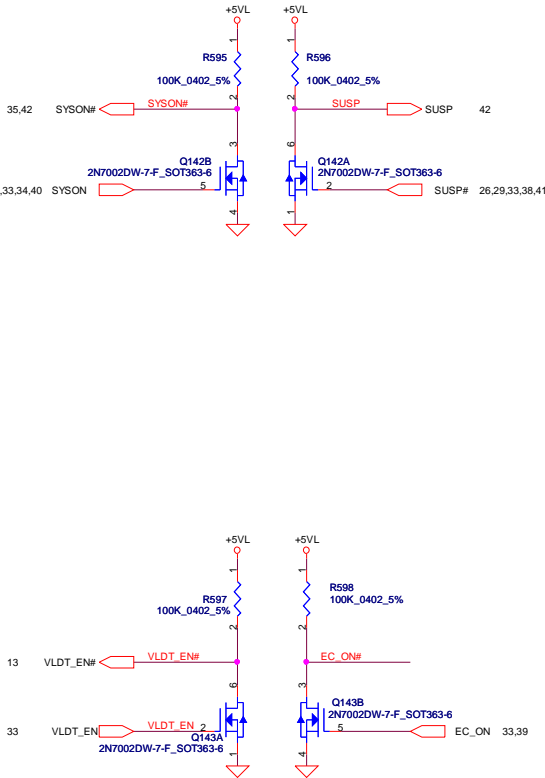
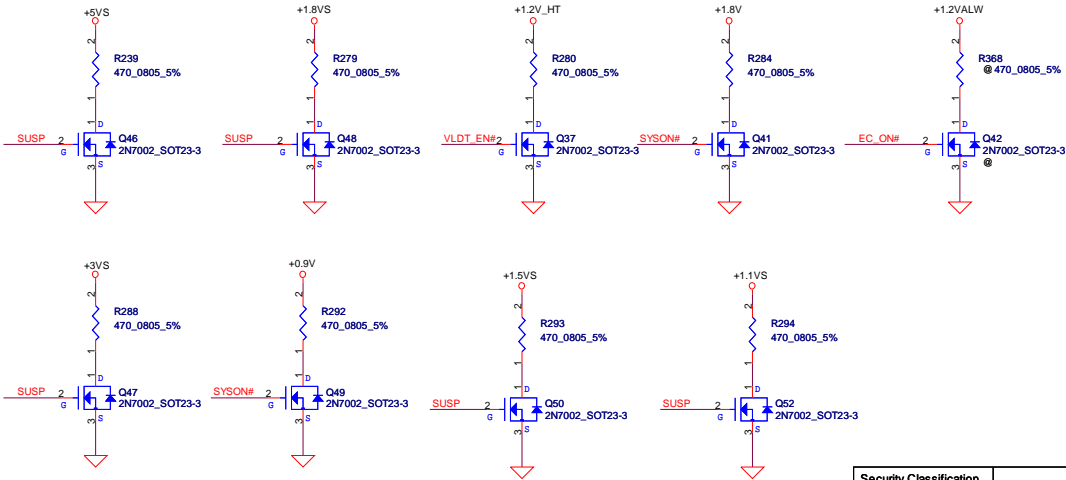
+1.2VALW TO +1.2V\_HT



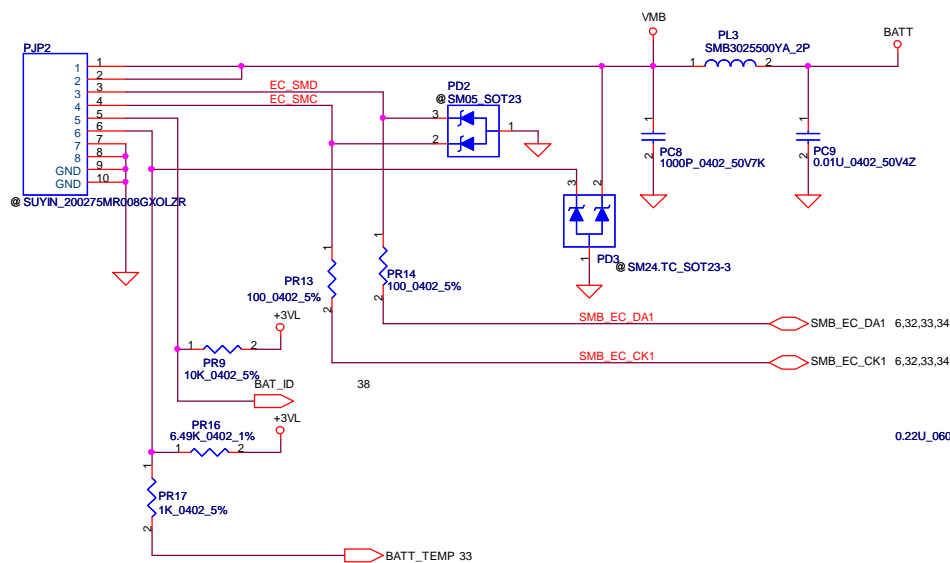
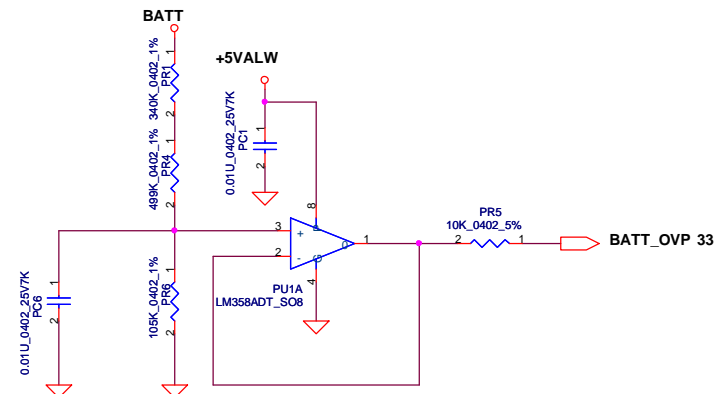
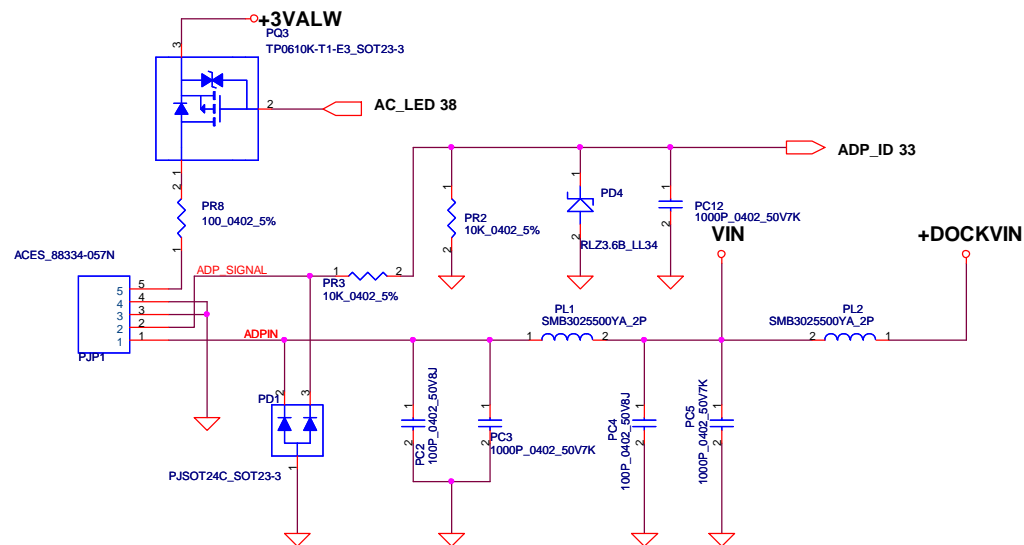
Screw Hole



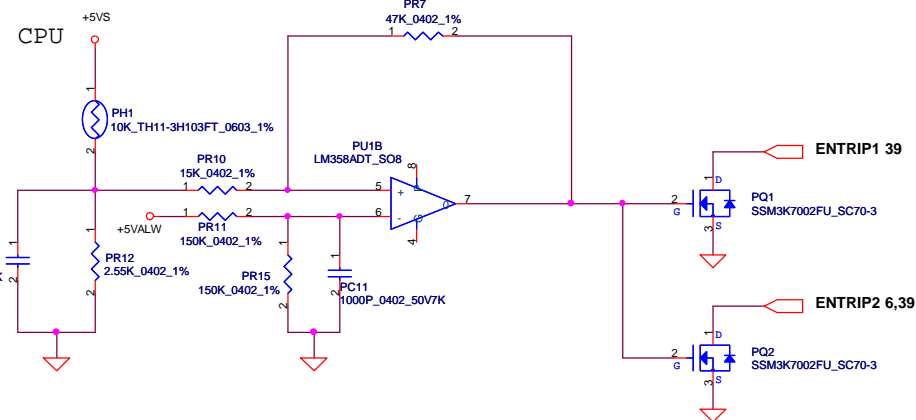
Discharge circuit



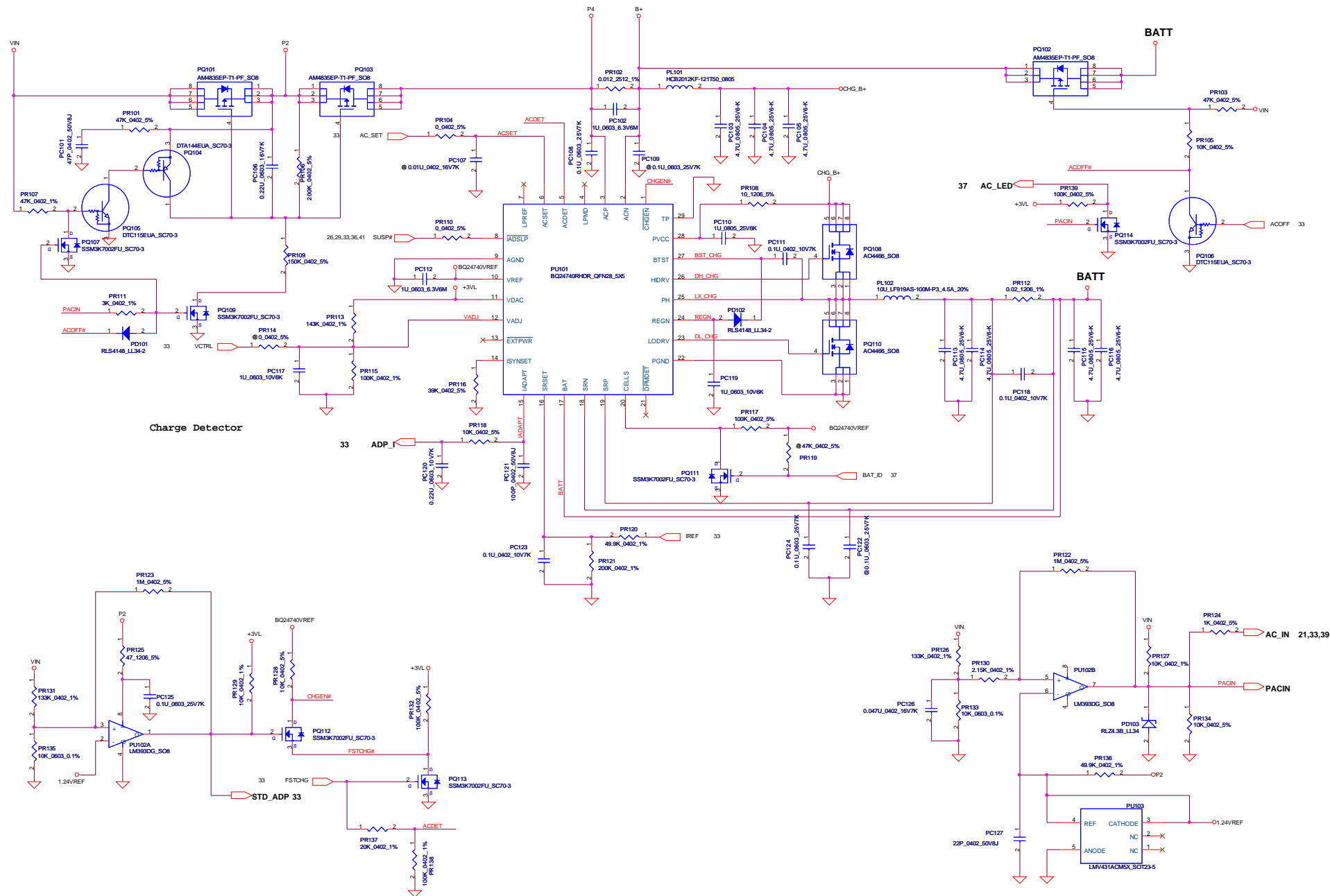
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title	
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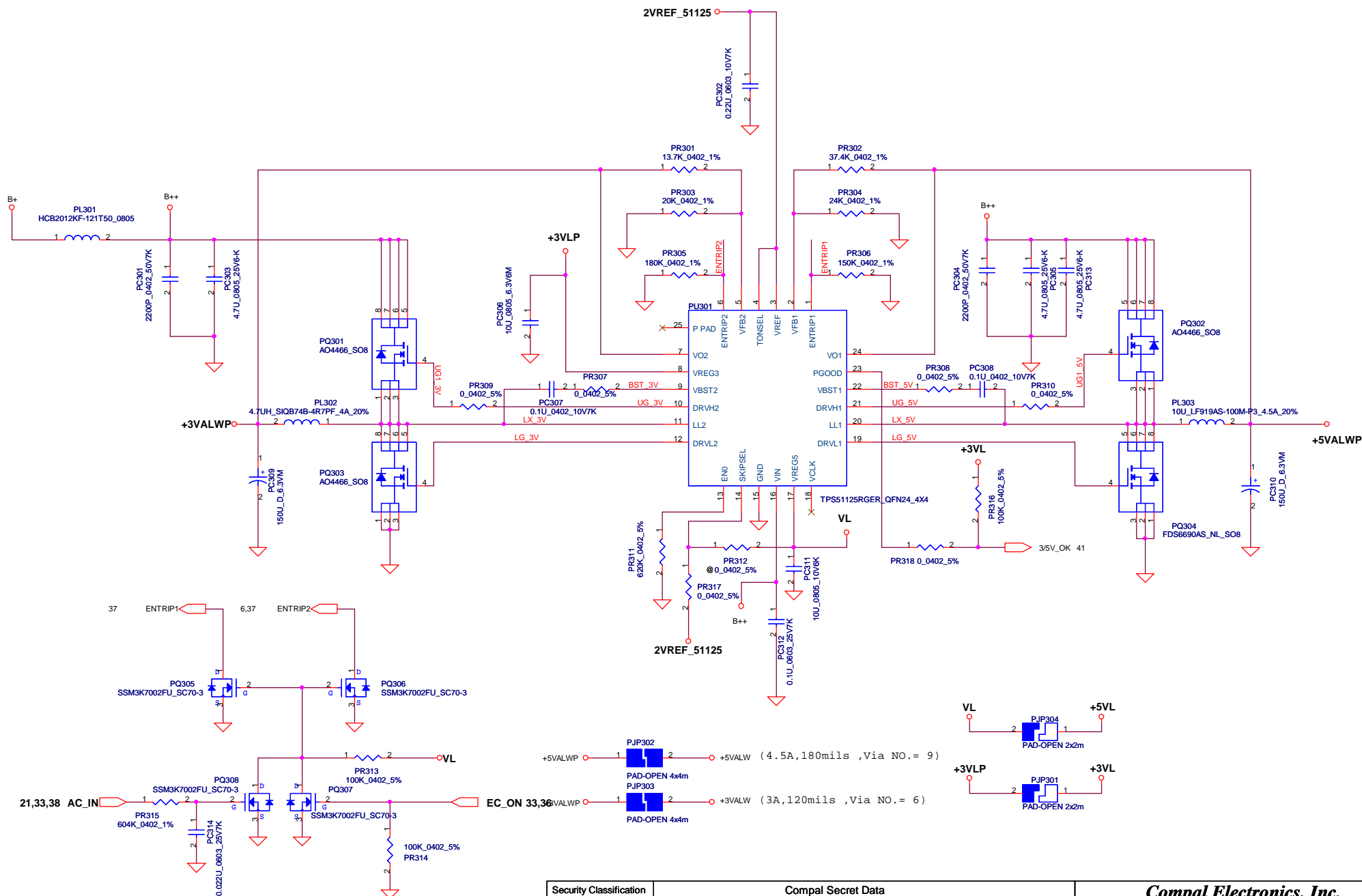
PH1 under CPU bottom side :  
CPU thermal protection at 90 +-3 degree C  
Recovery at 47 +-3 degree C



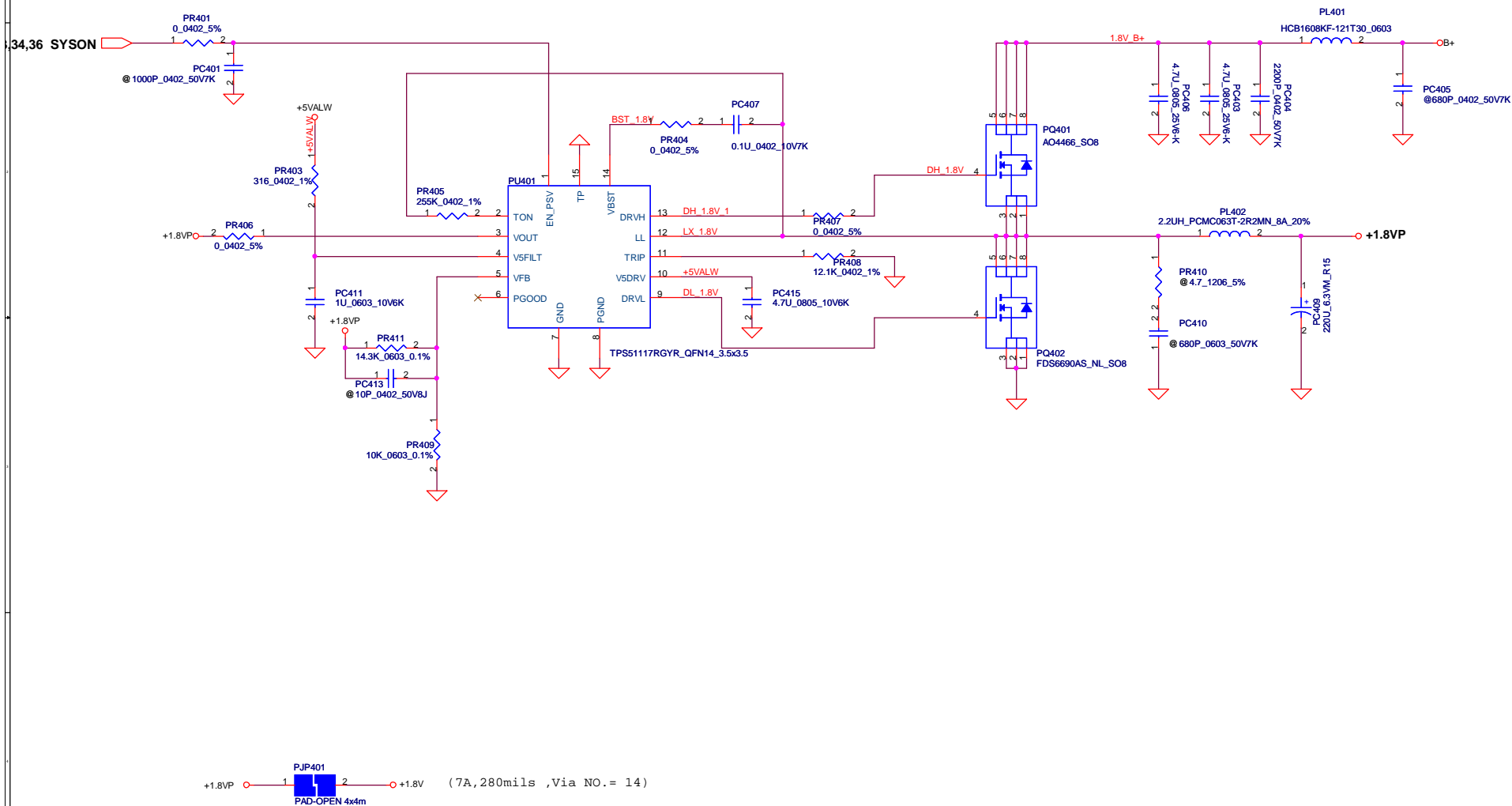
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title
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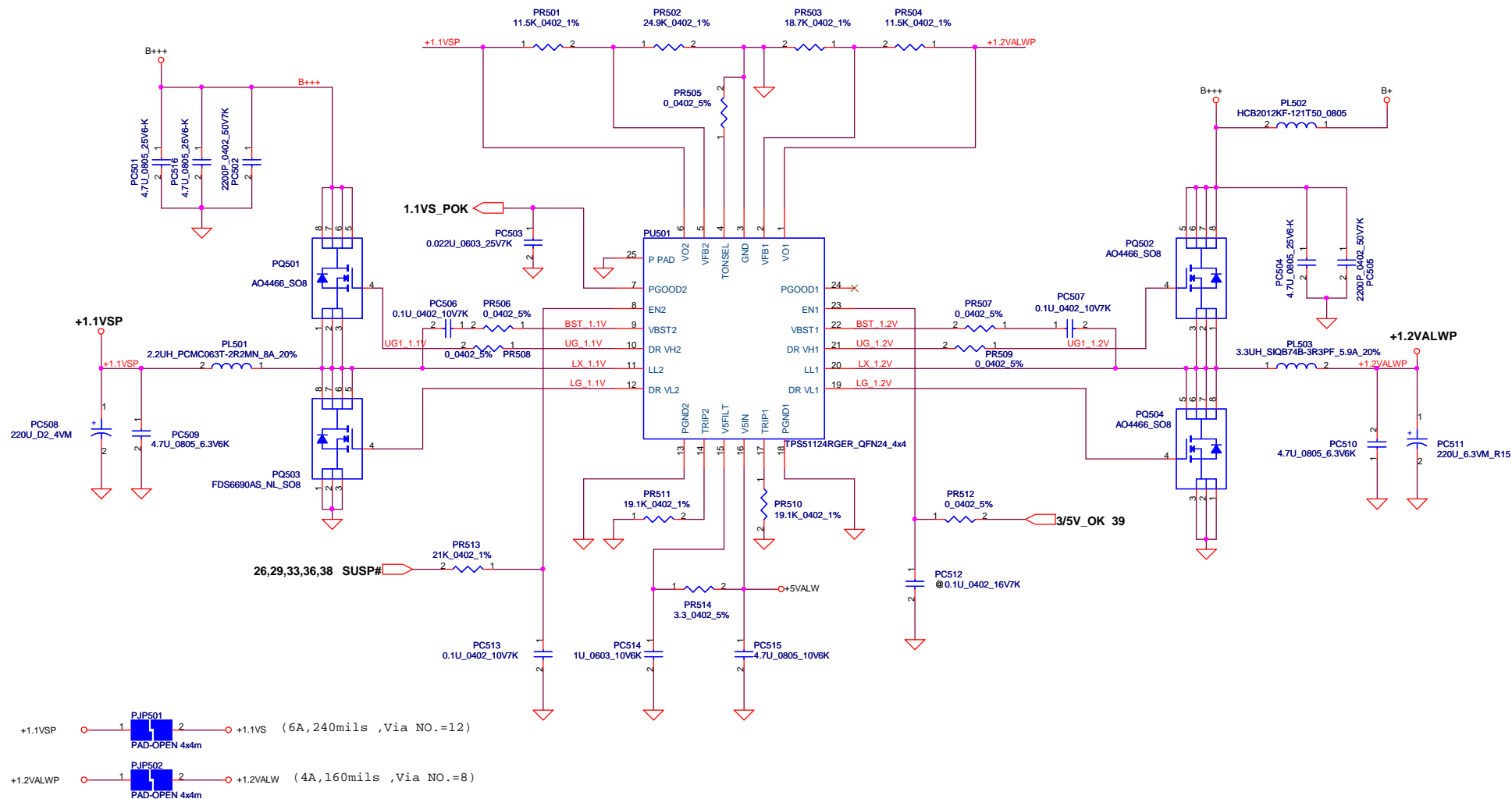


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Issued Date	2007/05/29	Deciphered Date	2008/05/29	3.3VALWP/5VALWP	
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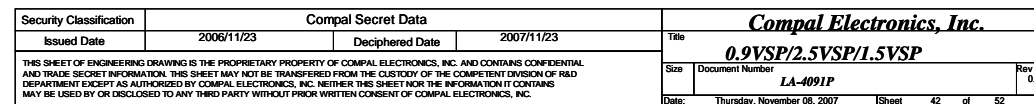


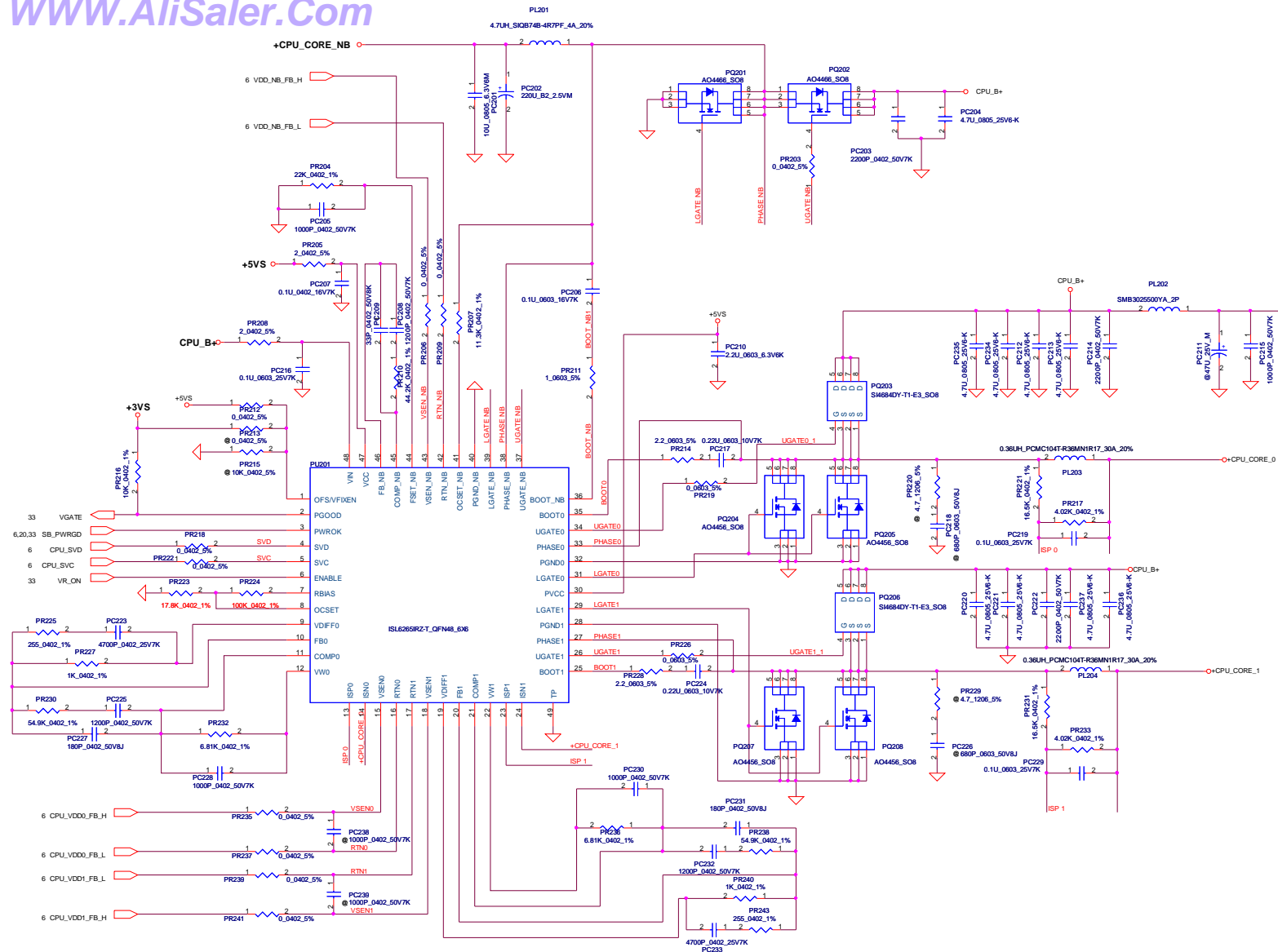
Security Classification			Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Title	1.8VP	
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Issued Date	2007/05/29	Deciphered Date	2008/05/29	1.1VSP/1.2VALWP	
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# Version Change List (P. I. R. List )for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	1.8VP	10/23	Compal	for power request	PU401 change the IC from "S IC RT8204PQW WQFN 16P" to "S IC TPS51117RGYR QFN 14P".	
2	38	Charger	10/30	Compal	for power request	PQ104 swap the PQ104 1,3 Pin	
3	39	3V/5V	10/30	Compal	for power request	Change PR301 to 13.7K modify output voltage	
4	39	3V/5V	10/30	Compal	for power request	Change PR305 to 180K modify OCP	
5	39	3V/5V	10/30	Compal	for power request	Change PR306 to 150K modify OCP	
6	39	3V/5V	10/30	Compal	for power request	Change PR311 to 620K	
7	39	3V/5V	10/30	Compal	for power request	Change PR315 to 604K modify sequence	
8	41	+1.1VSP	10/30	Compal	for power request	Change PR510 to 19.1K modify OCP	
9	41	+1.2VALWP	10/30	Compal	for power request	Change PR511 to 19.1K modify OCP	
10	38	Charger	10/30	Compal	for power request	Del PR119	
11	43	CPU_CORE	10/30	Compal	for power request	Change PC202 to B2 type for ME limit	
12	43	CPU_CORE	10/30	Compal	for power request	Change PR223 to 17.8K and PR224 to 100K modify OCP	
13	43	CPU_CORE	10/30	Compal	for power request	Change PR221,PR231 to 16.5K and PR217,PR233 to 4.02K for CPU_CORE compensation	
14	37	DC connector	10/30	Compal	for power request	Add PR3,PD4,PC12 for ADP_ID function	
15	39	3V/5V	10/30	Compal	for power request	Add PR317,PR318	
16	38	Charger	10/30	Compal	for power request	Change net from +3VLP to +3VL	
17	41	+1.1VSP	10/30	Compal	for power request	Change PR513 to 21K for HW power scquence.	

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HW4 Product Improvement Record (P.I.R.)

RTC



45 @ RTC

PCB



PCB 03X LA-4091P REV0 M/B

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				Size	Document Number
				Date: Thursday, November 08, 2007	Rev 0.1
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