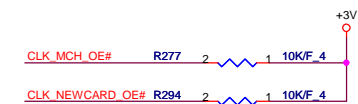
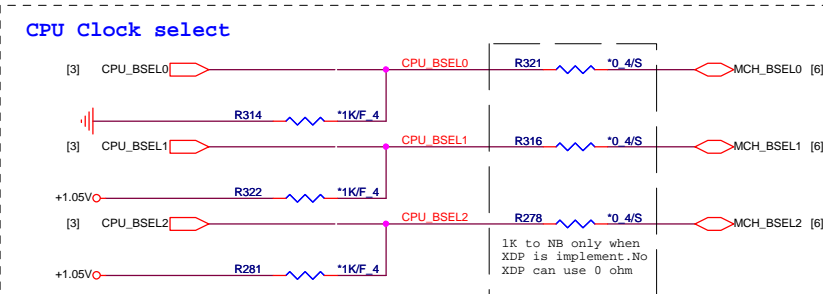



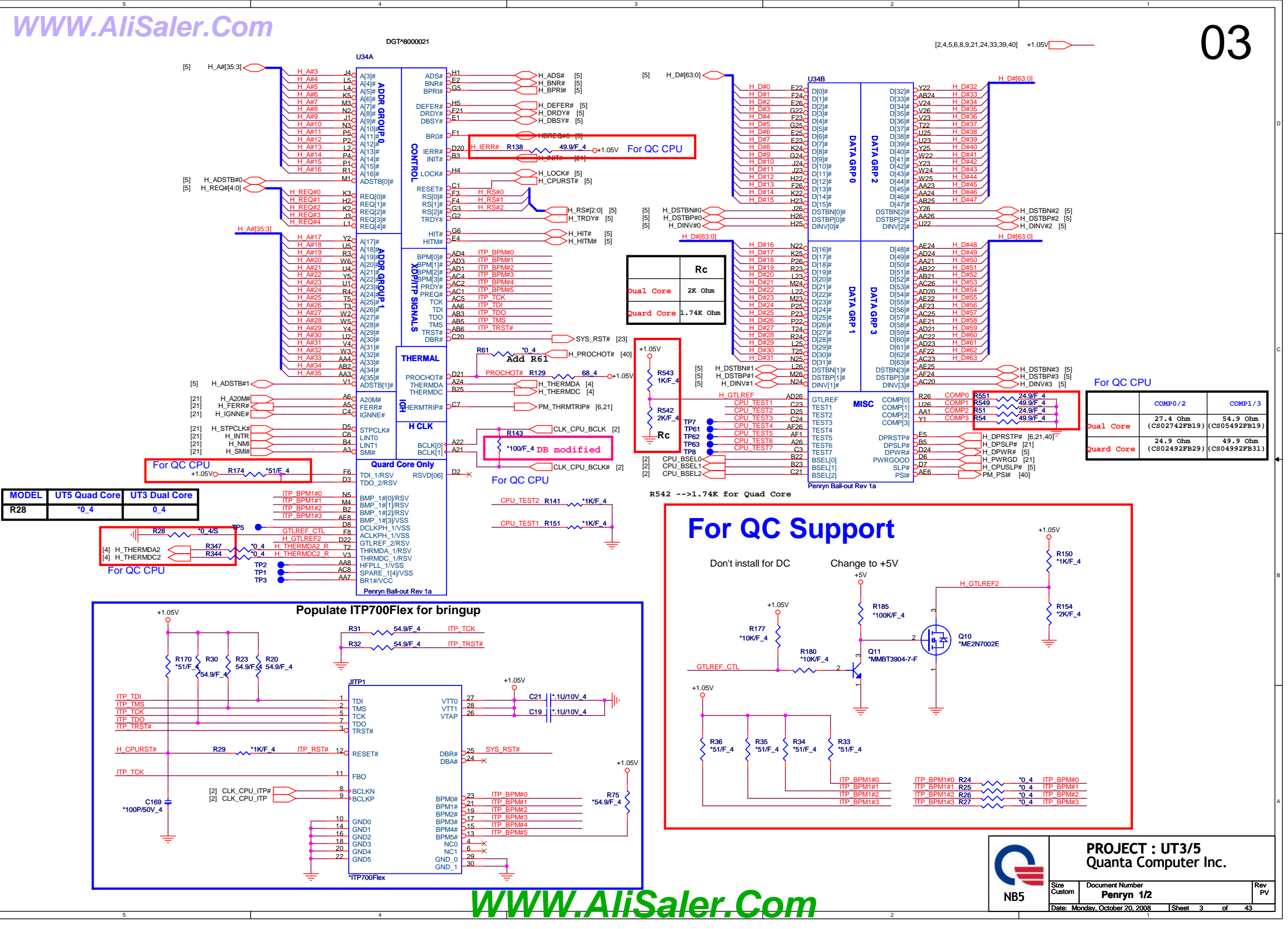
CK505	QFN64	
ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000
SPECTRALINEAR	SL28541BQCT	AL028541000



for EMI



 NB5	PROJECT : UT3/5 Quanta Computer Inc.		
	Size Custom	Document Number Clock Generator	Rev PV
Date: Monday, October 20, 2008		Sheet 2 of 43	



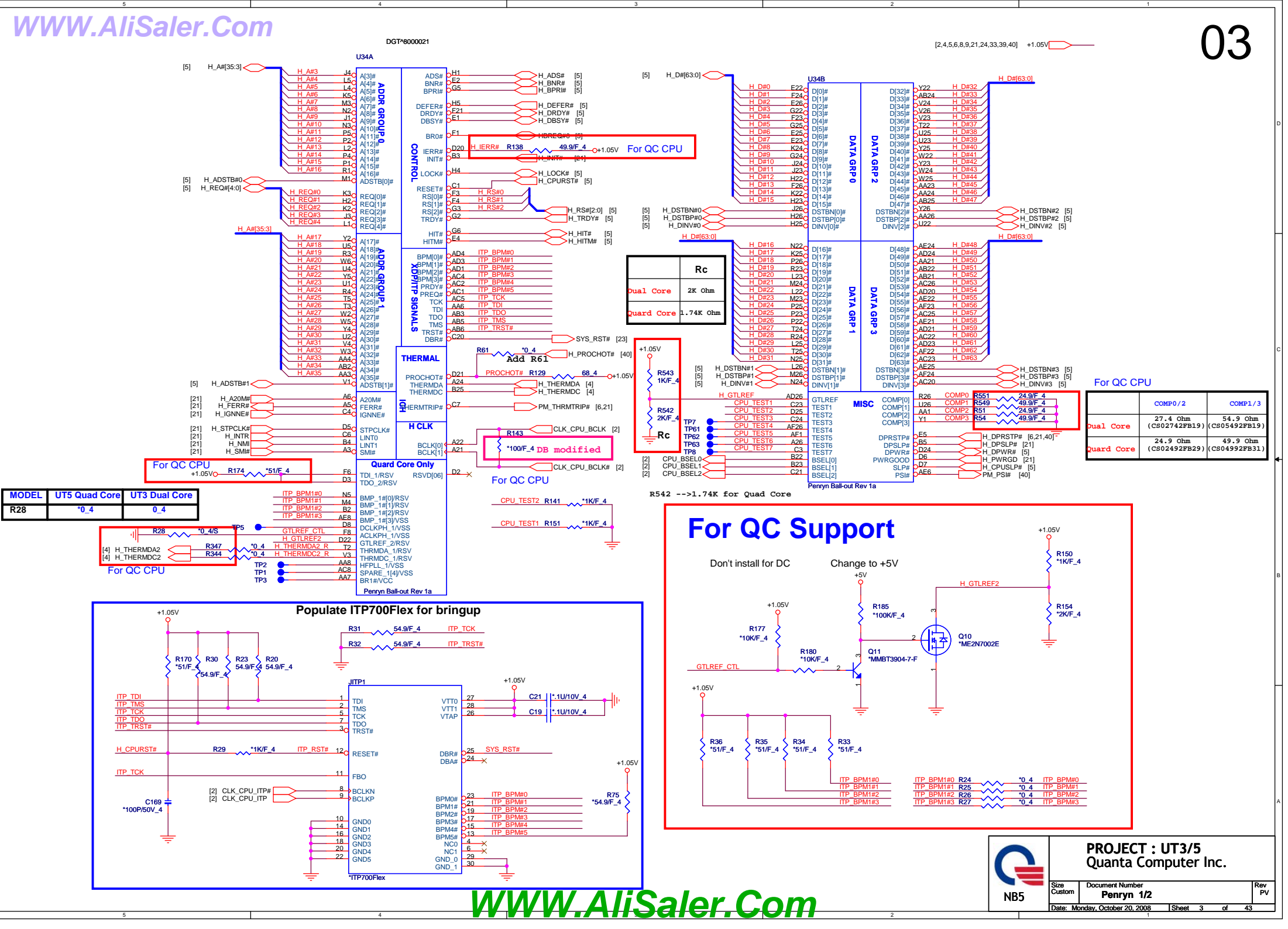
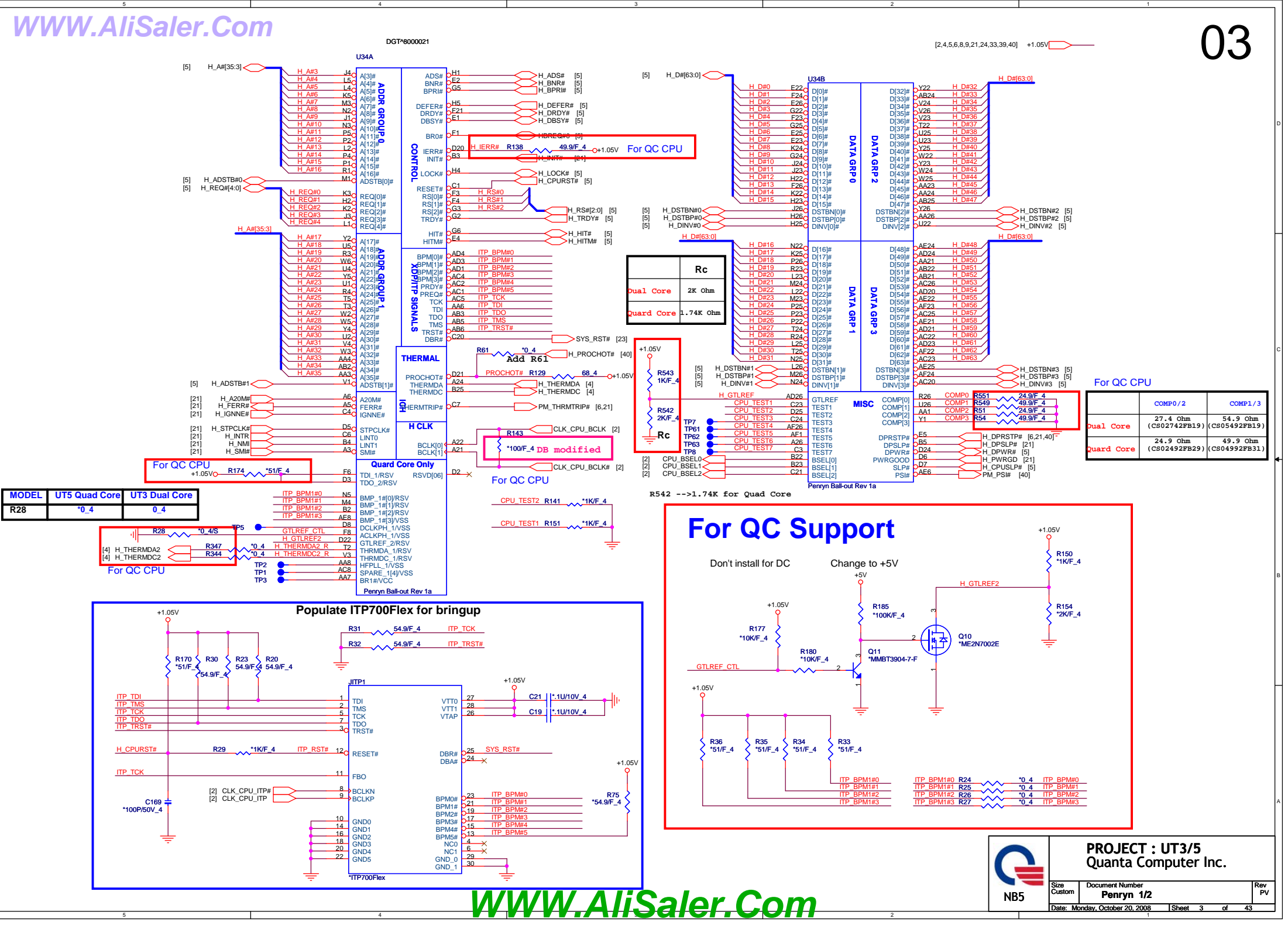
WWW.AliSaler.Com

03

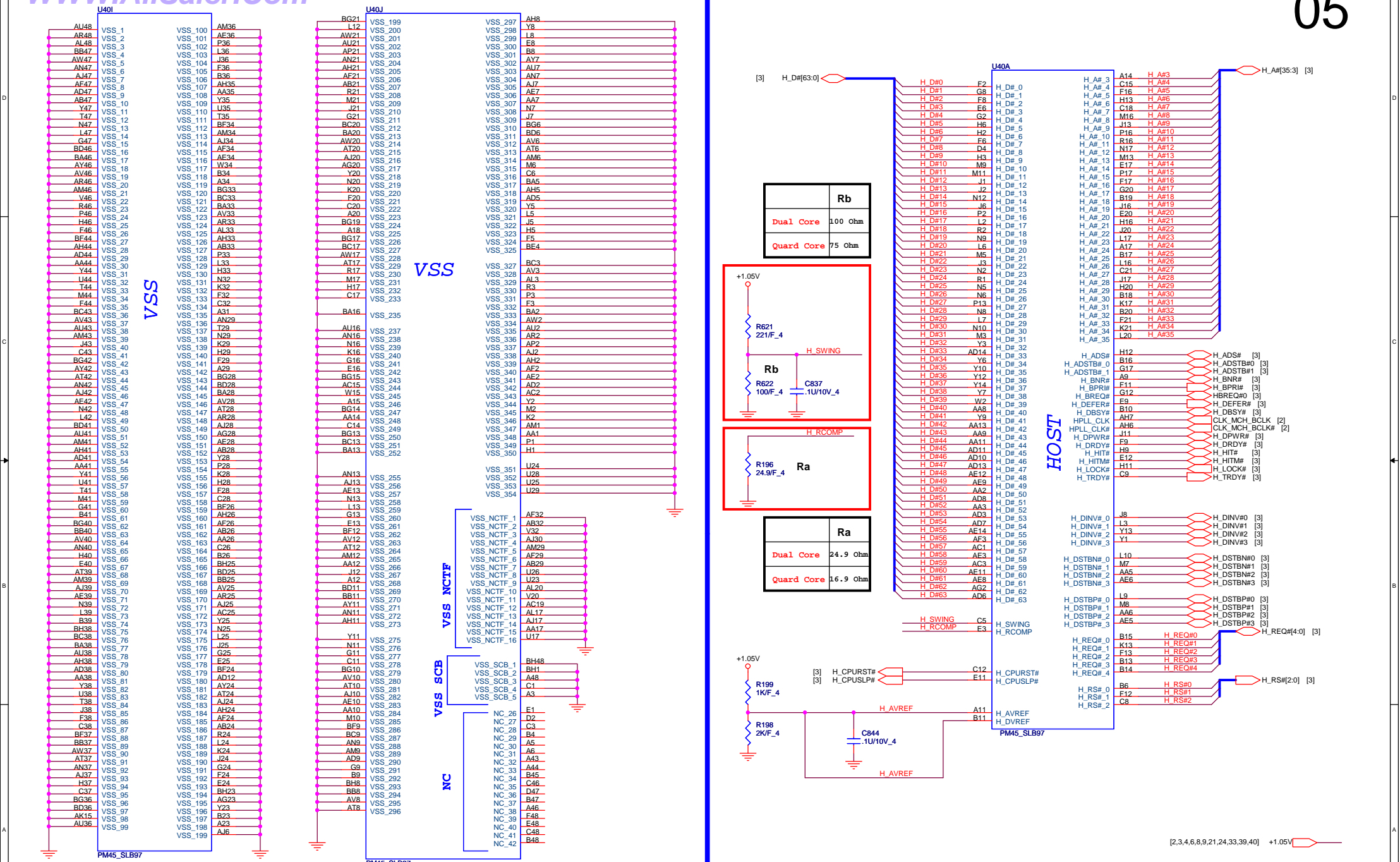
The diagram is a detailed schematic for a Penryn Ball-out Rev 1a processor. It shows various signal paths, component values, and configuration options. Key sections include:

- Top Section:** Shows the processor's pins and their connections to various components. It includes a table for "Rc" values: Dual Core (2K Ohm) and Quad Core (1.74K Ohm).
- Left Section:** Shows the processor's pins and their connections to various components. It includes a table for "Rc" values: Dual Core (2K Ohm) and Quad Core (1.74K Ohm).
- Right Section:** Shows the processor's pins and their connections to various components. It includes a table for "Rc" values: Dual Core (2K Ohm) and Quad Core (1.74K Ohm).
- Bottom Section:** Shows the processor's pins and their connections to various components. It includes a table for "Rc" values: Dual Core (2K Ohm) and Quad Core (1.74K Ohm).

The diagram also includes various component values and configuration options, such as "For QC CPU" and "For QC CPU".







MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)
MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes
MCH_CFG_6 ITPM Host Interface
Low = The ITPM Host Interface is enabled2
High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel(R) Management Engine Crypto
Low: Intel(R) Management Engine Crypto
High: Intel(R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel(R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)
MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High: Disabled (Default)
MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating
MCH_CFG_13 MCH_CFG_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe
Low = Only digital display port (SDVO/DP/HDMI) or PCIe is operational (default)
High = Digital display port (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port

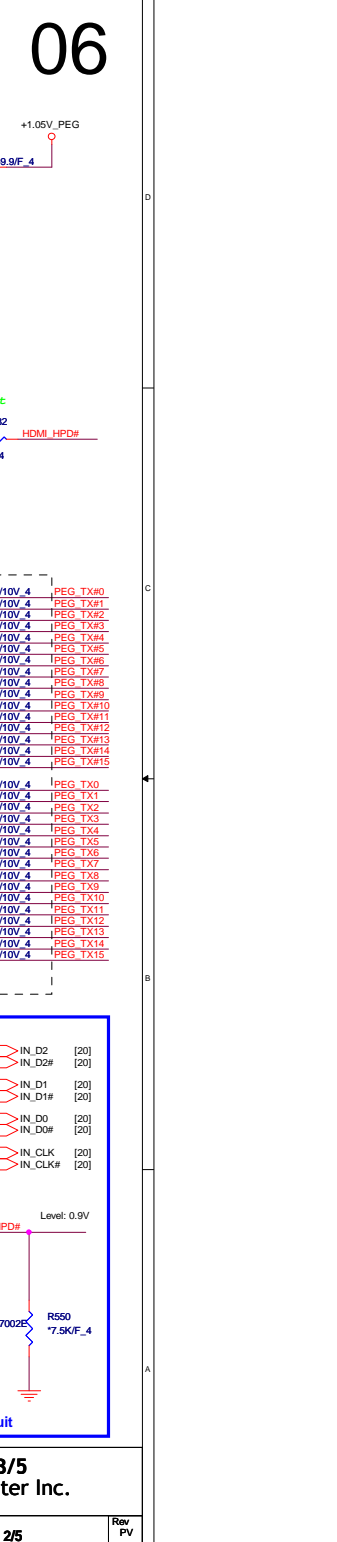
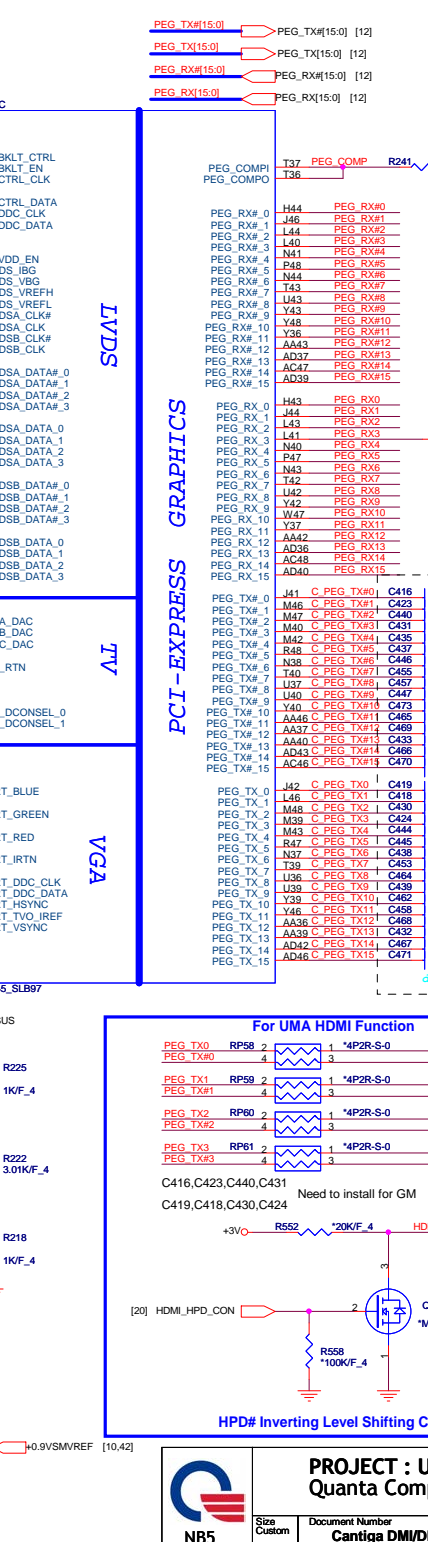
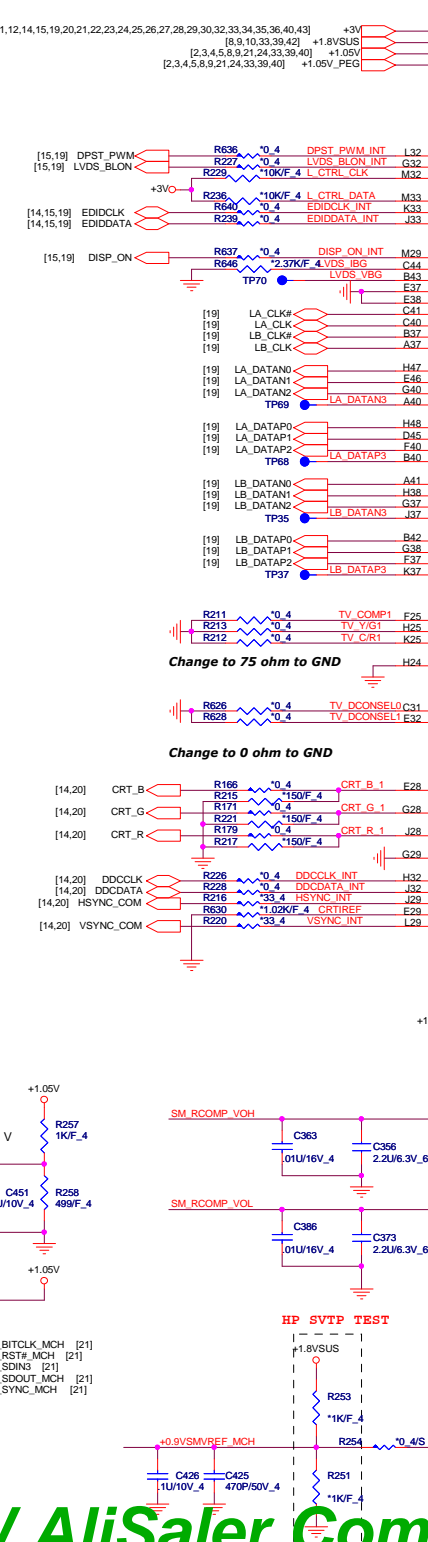
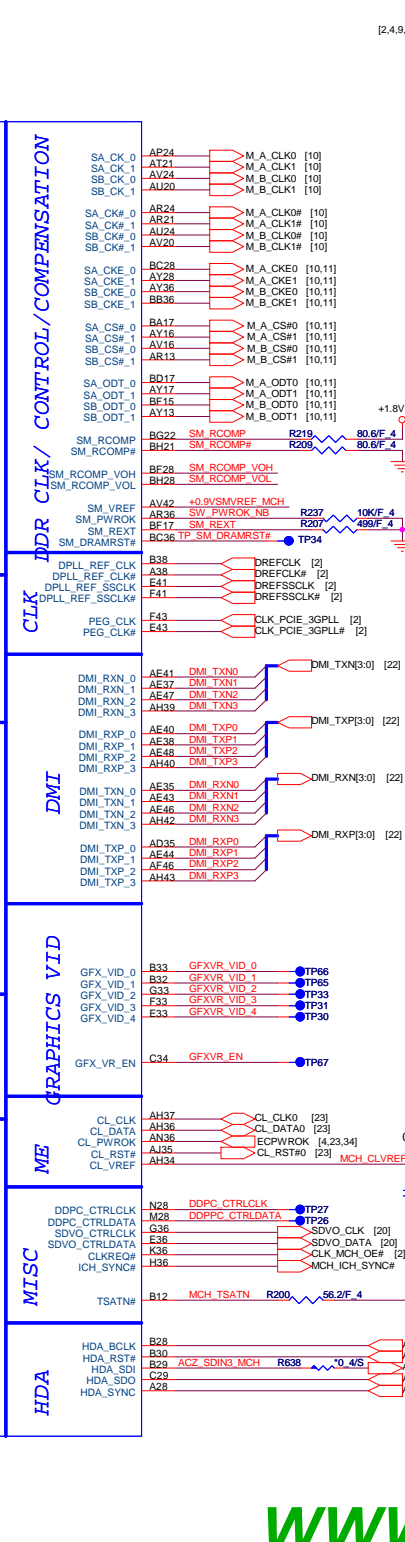
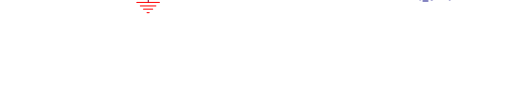
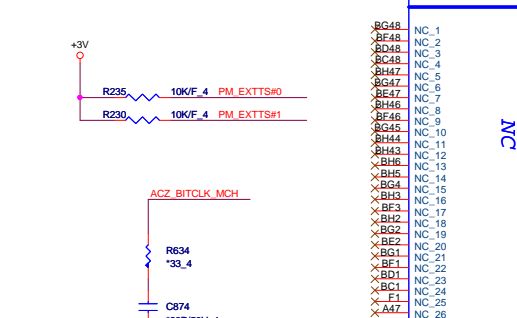
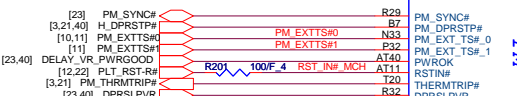
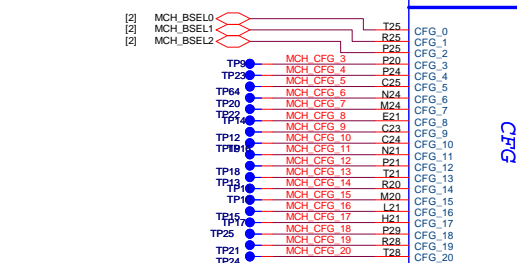
MCH_CFG2:0

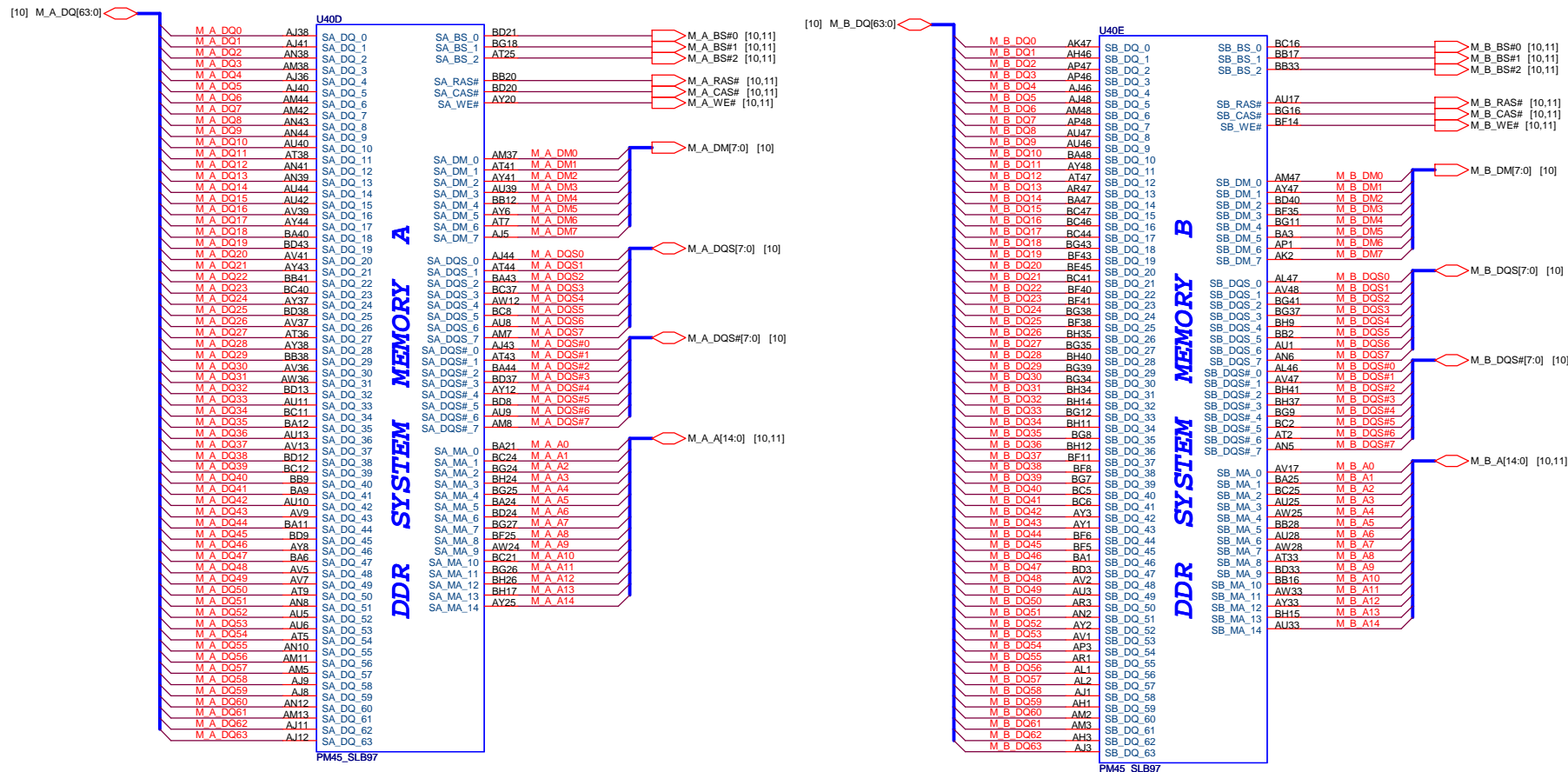
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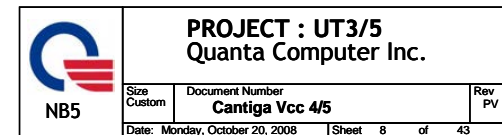
010 = FSB800

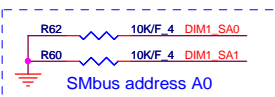
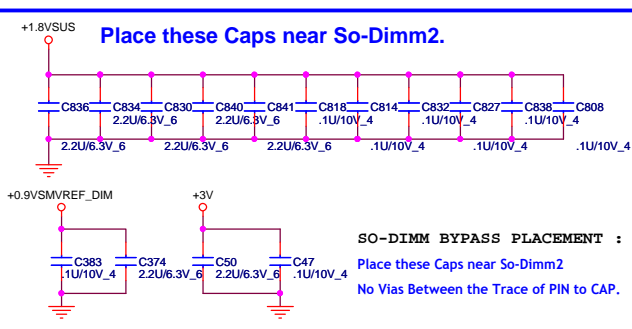
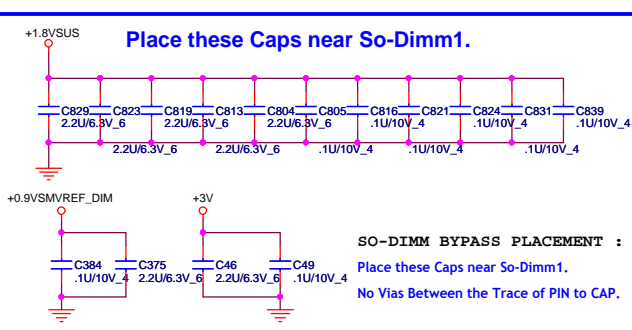
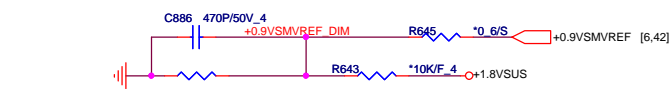
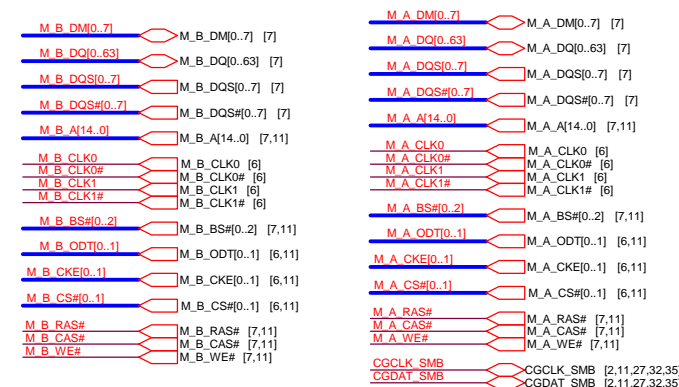
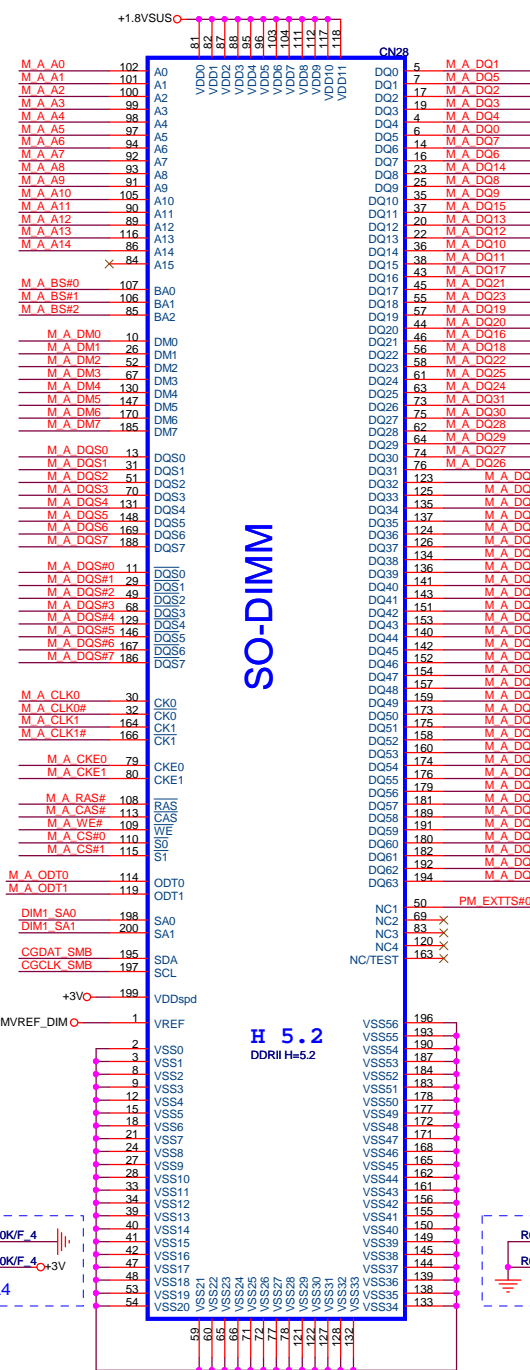
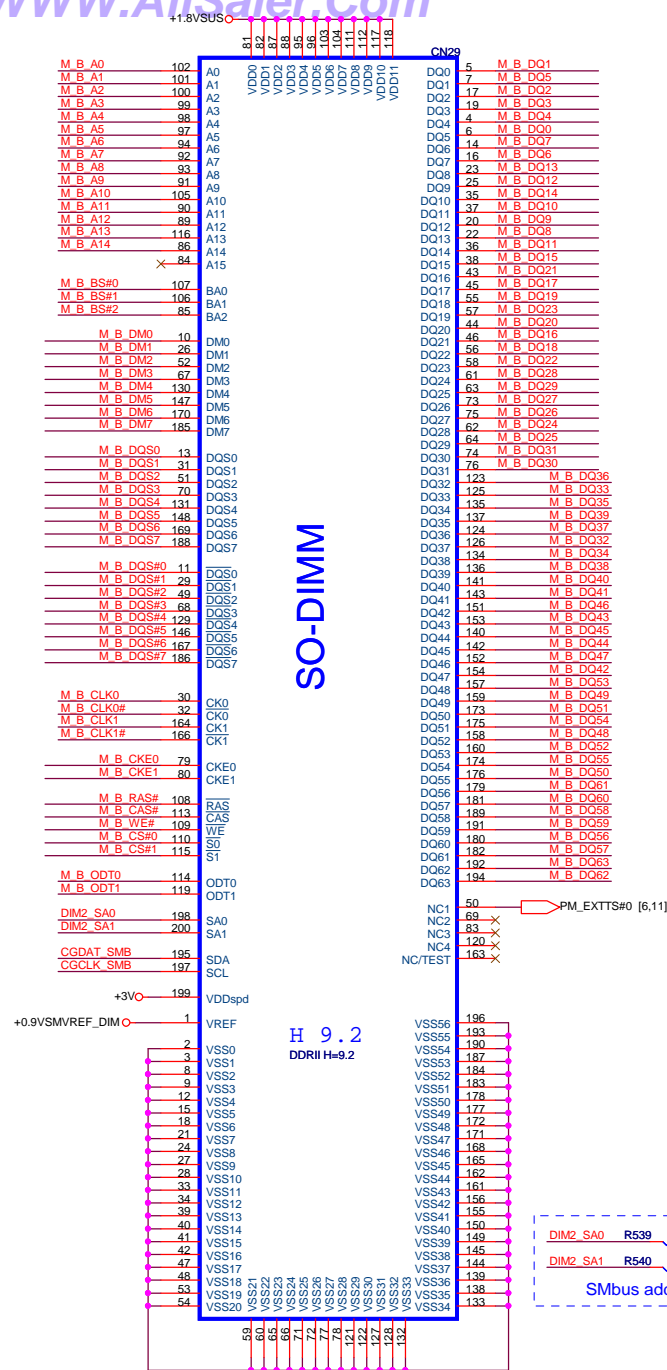
011 = FSB667

Others = Reserved

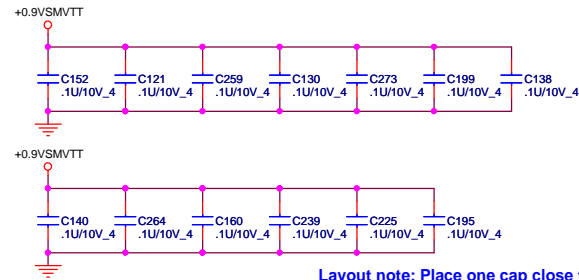




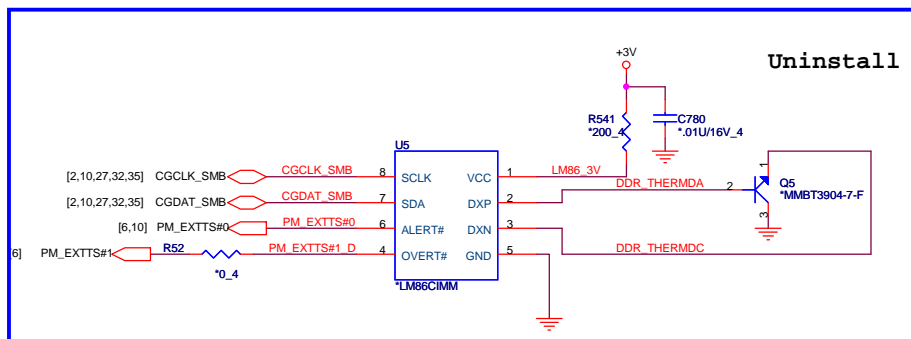
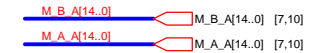
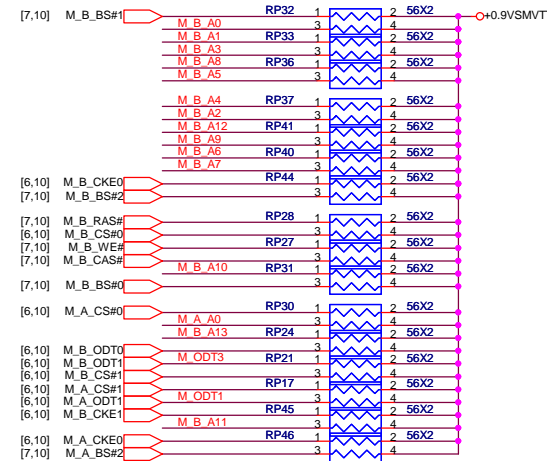
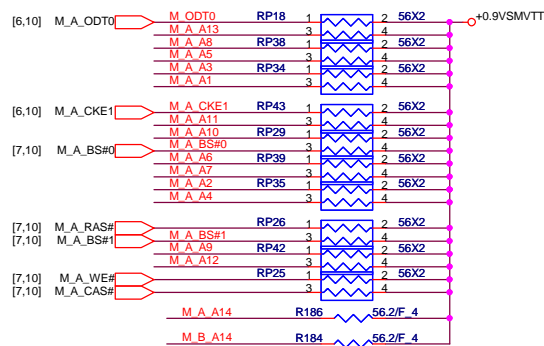
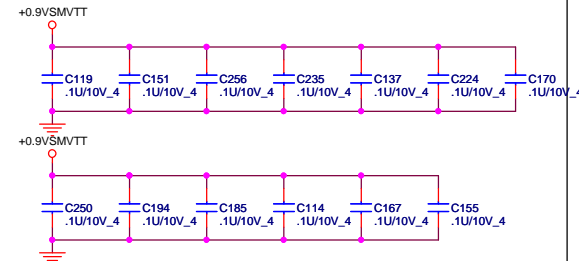


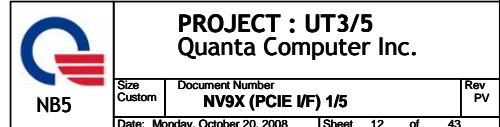


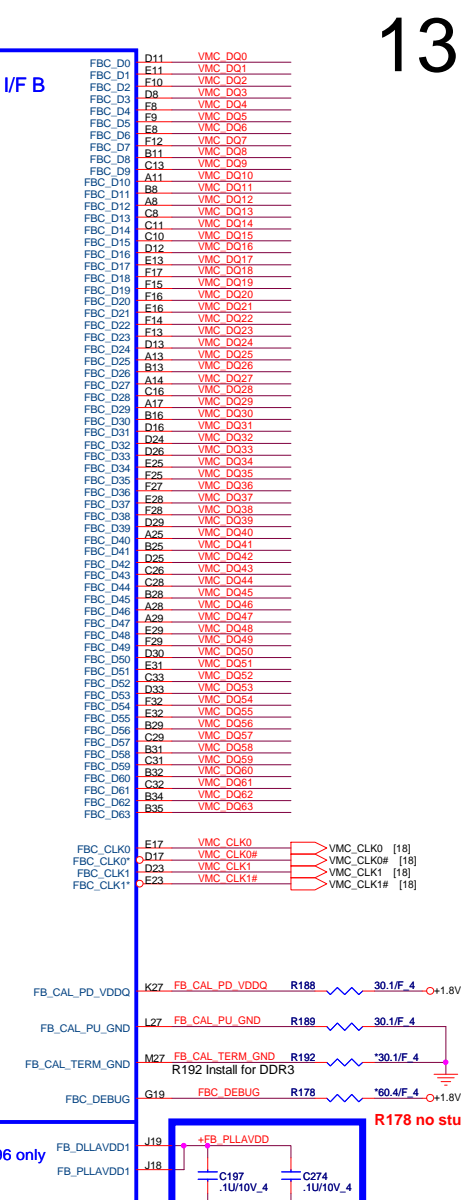
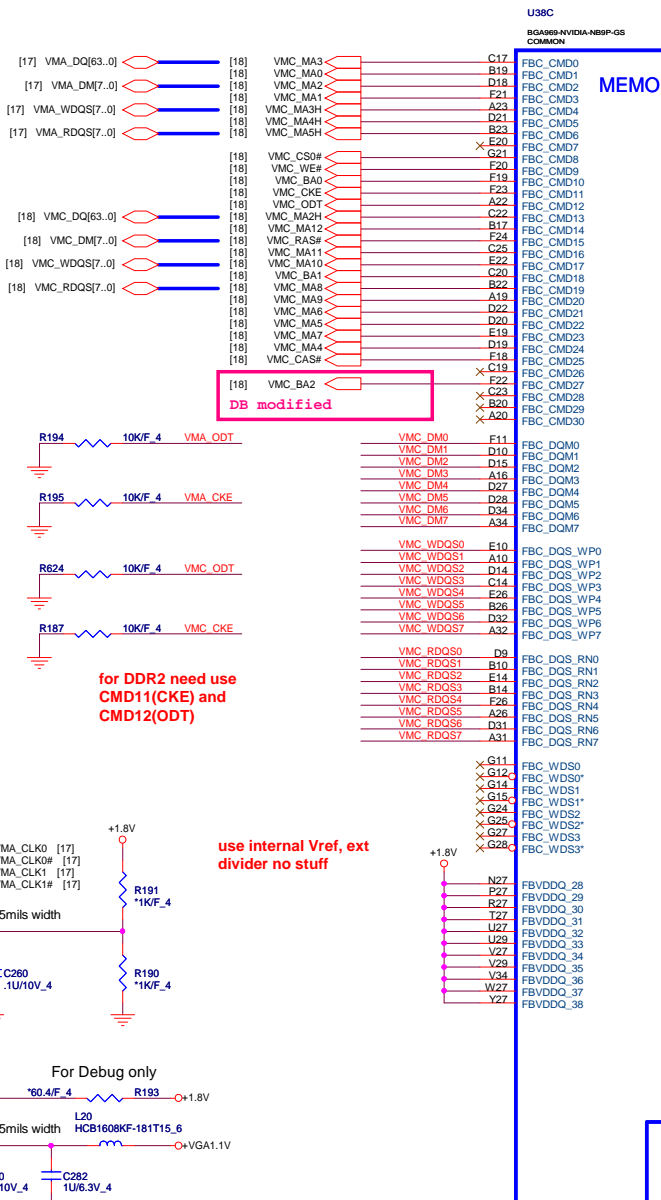
DDR II B CHANNEL

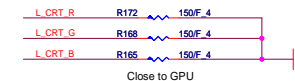
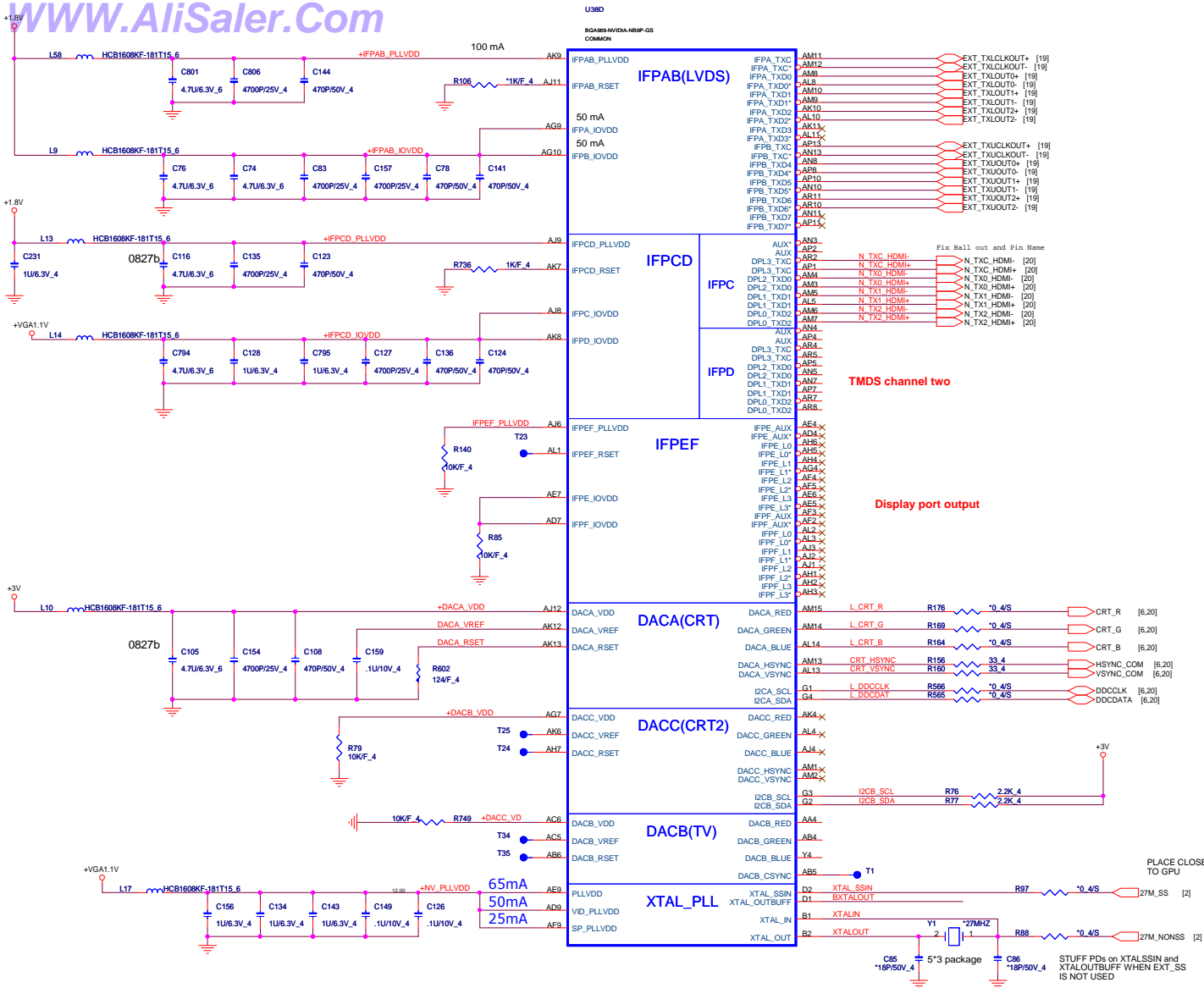


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM









PLACE CLOSE TO GPU

27M_SS [2]

BXTALOUT

27M_NONSS [2]

R88 0.4/S

R89 0.4/S

R90 0.4/S

R91 0.4/S

R92 0.4/S

R93 0.4/S

R94 0.4/S

R95 0.4/S

R96 0.4/S

R97 0.4/S

R98 0.4/S

R99 0.4/S

R100 0.4/S

R101 0.4/S

R102 0.4/S

R103 0.4/S

R104 0.4/S

R105 0.4/S

R106 0.4/S

R107 0.4/S

R108 0.4/S

R109 0.4/S

R110 0.4/S

R111 0.4/S

R112 0.4/S

R113 0.4/S

R114 0.4/S

R115 0.4/S

R116 0.4/S

R117 0.4/S

R118 0.4/S

R119 0.4/S

R120 0.4/S

R121 0.4/S

R122 0.4/S

R123 0.4/S

R124 0.4/S

R125 0.4/S

R126 0.4/S

R127 0.4/S

R128 0.4/S

R129 0.4/S

R130 0.4/S

R131 0.4/S

R132 0.4/S

R133 0.4/S

R134 0.4/S

R135 0.4/S

R136 0.4/S

R137 0.4/S

R138 0.4/S

R139 0.4/S

R140 0.4/S

R141 0.4/S

R142 0.4/S

R143 0.4/S

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R147 0.4/S

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R165 0.4/S

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R191 0.4/S

R192 0.4/S

R193 0.4/S

R194 0.4/S

R195 0.4/S

R196 0.4/S

R197 0.4/S

R198 0.4/S

R199 0.4/S

R200 0.4/S

R201 0.4/S

R202 0.4/S

R203 0.4/S

R204 0.4/S

R205 0.4/S

R206 0.4/S

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R251 0.4/S

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R256 0.4/S

R257 0.4/S

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R263 0.4/S

R264 0.4/S

R265 0.4/S

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R267 0.4/S

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R276 0.4/S

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R287 0.4/S

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R290 0.4/S

R291 0.4/S

R292 0.4/S

R293 0.4/S

R294 0.4/S

R295 0.4/S

R296 0.4/S

R297 0.4/S

R298 0.4/S

R299 0.4/S

R300 0.4/S

R301 0.4/S

R302 0.4/S

R303 0.4/S

R304 0.4/S

R305 0.4/S

R306 0.4/S

R307 0.4/S

R308 0.4/S

R309 0.4/S

R310 0.4/S

R311 0.4/S

R312 0.4/S

R313 0.4/S

R314 0.4/S

R315 0.4/S

R316 0.4/S

R317 0.4/S

R318 0.4/S

R319 0.4/S

R320 0.4/S

R321 0.4/S

R322 0.4/S

R323 0.4/S

R324 0.4/S

R325 0.4/S

R326 0.4/S

R327 0.4/S

R328 0.4/S

R329 0.4/S

R330 0.4/S

R331 0.4/S

R332 0.4/S

R333 0.4/S

R334 0.4/S

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R336 0.4/S

R337 0.4/S

R338 0.4/S

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R340 0.4/S

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R346 0.4/S

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R349 0.4/S

R350 0.4/S

R351 0.4/S

R352 0.4/S

R353 0.4/S

R354 0.4/S

R355 0.4/S

R356 0.4/S

R357 0.4/S

R358 0.4/S

R359 0.4/S

R360 0.4/S

R361 0.4/S

R362 0.4/S

R363 0.4/S

R364 0.4/S

R365 0.4/S

R366 0.4/S

R367 0.4/S

R368 0.4/S

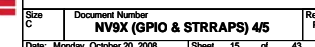
R369 0.4/S

R370 0.4/S

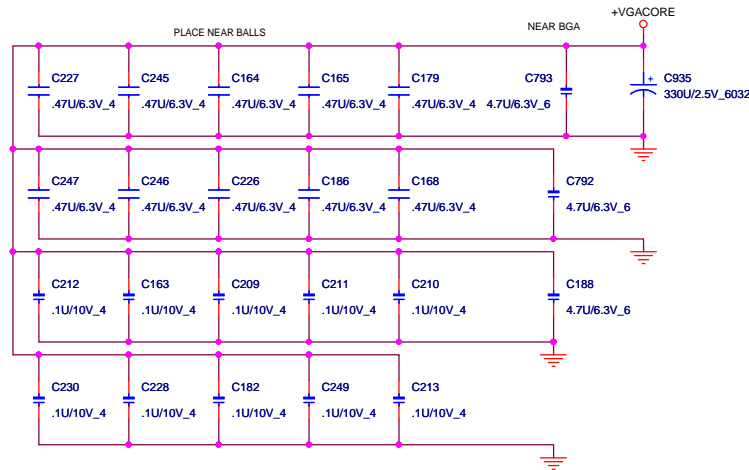
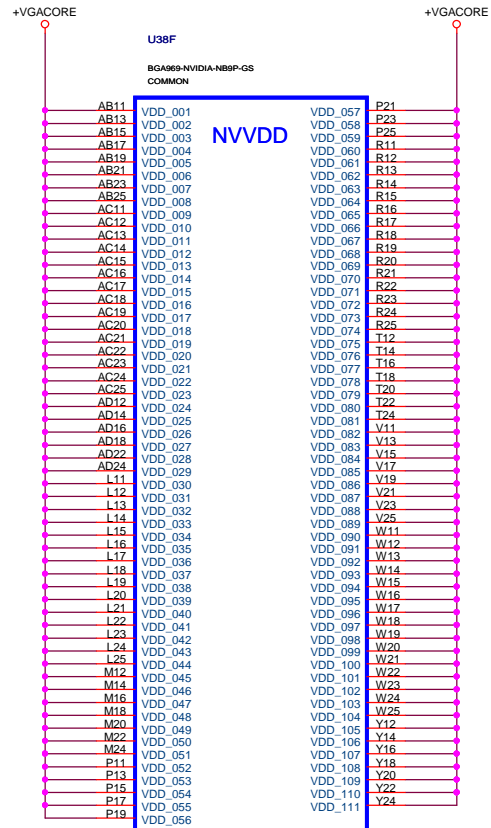
R371 0.4/S

R372 0.4/S

R373 0.4/S



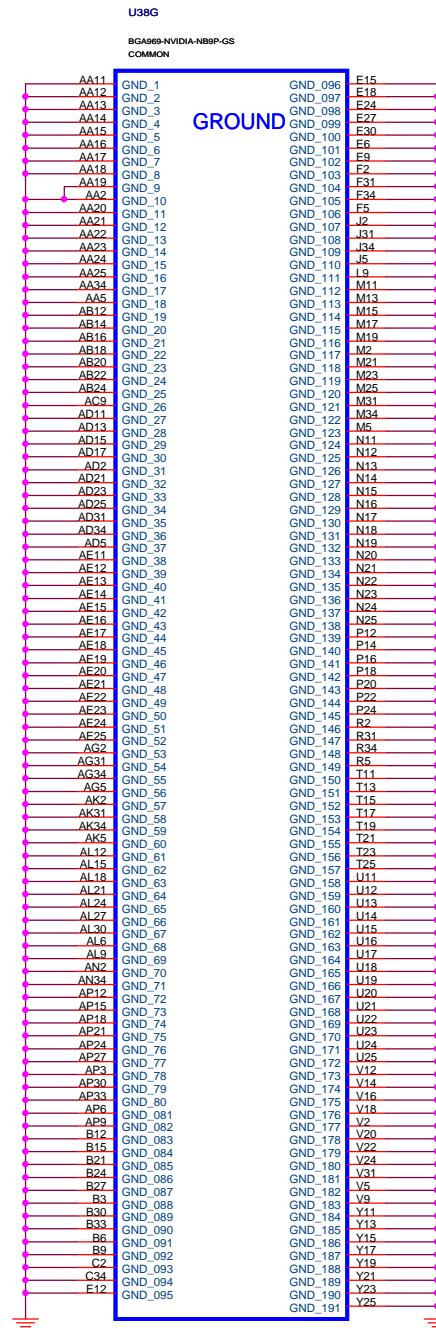
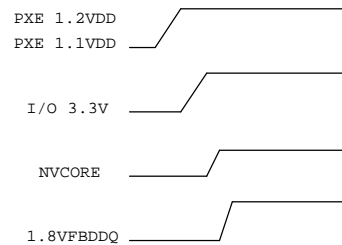
NVVDD Decoupling

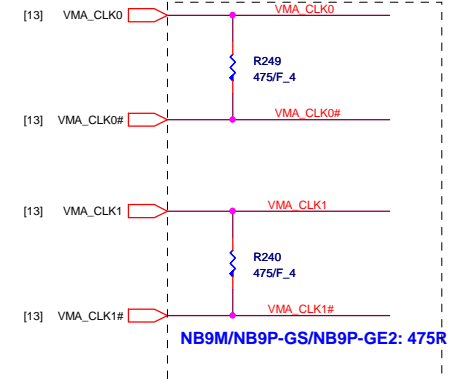
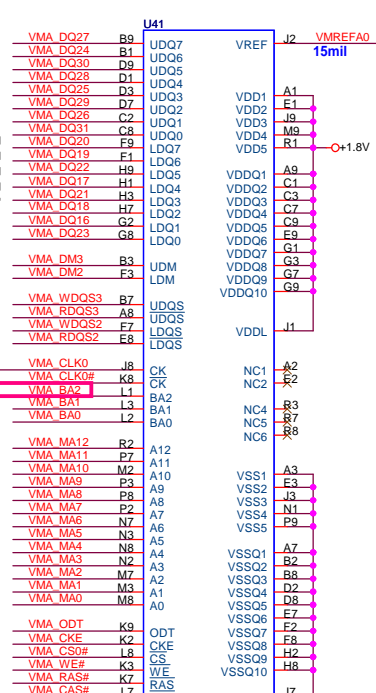
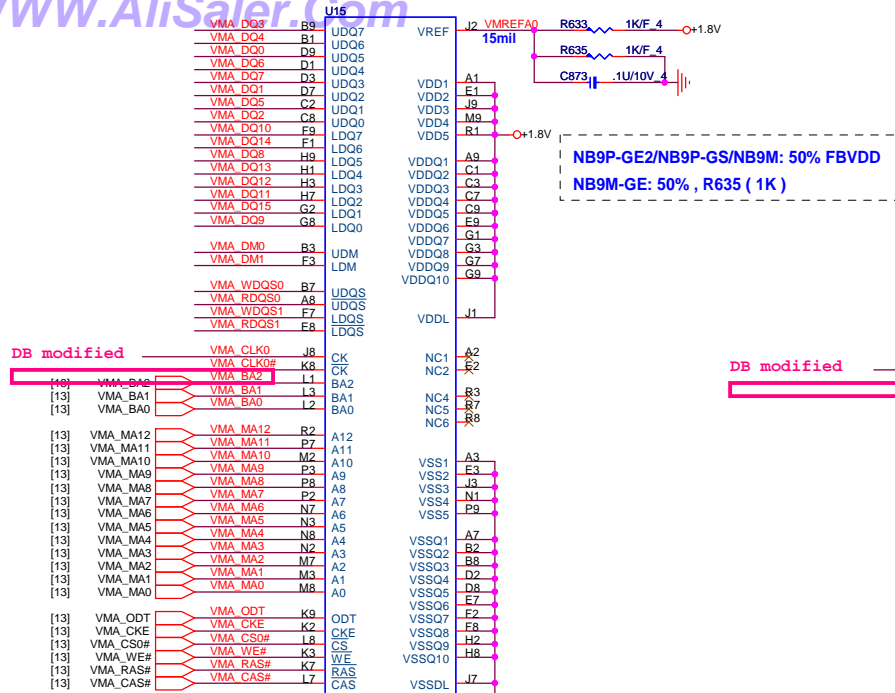


Follow Design Guide DG-03276-001 4.7uFx3
and 0.47x10 uF instead of 0.1uF x10

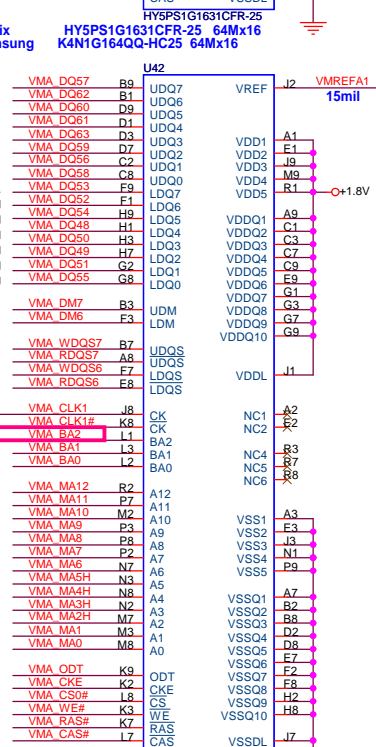
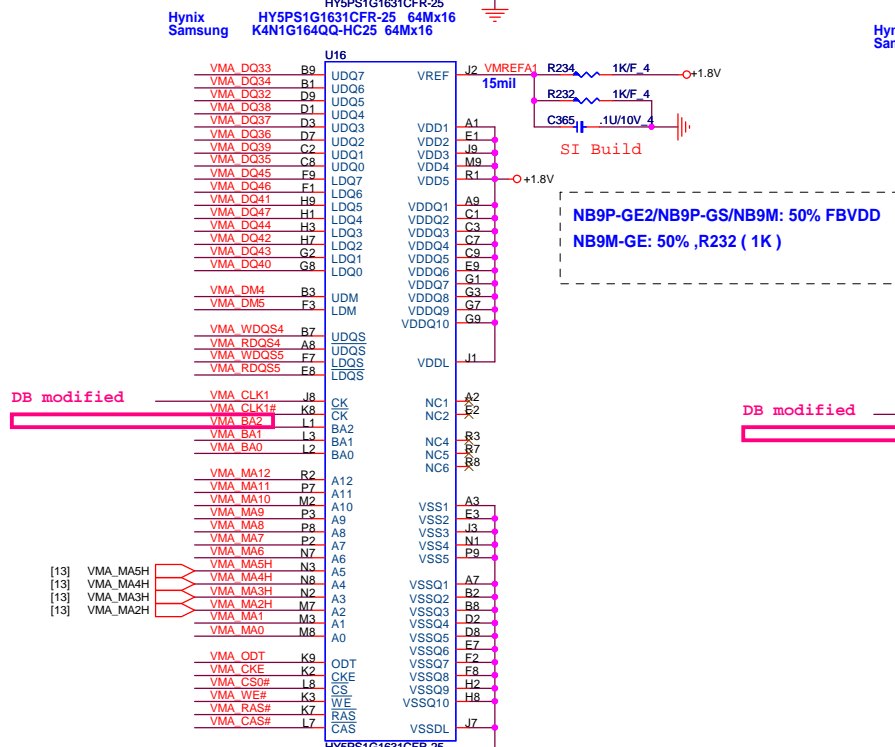
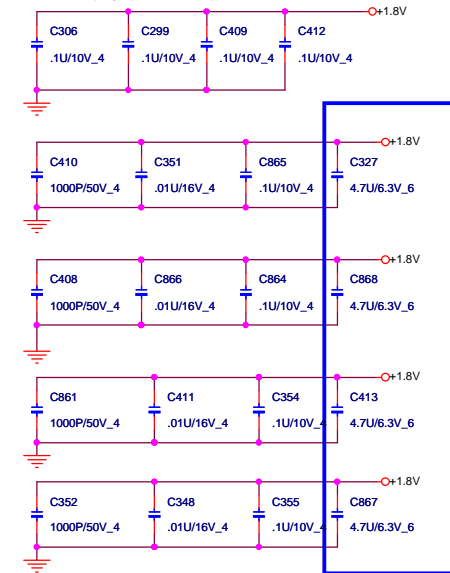
NB9M: VGACORE +0.90V (Normal) , +1.09V

power up sequence





(By pass capacitor)

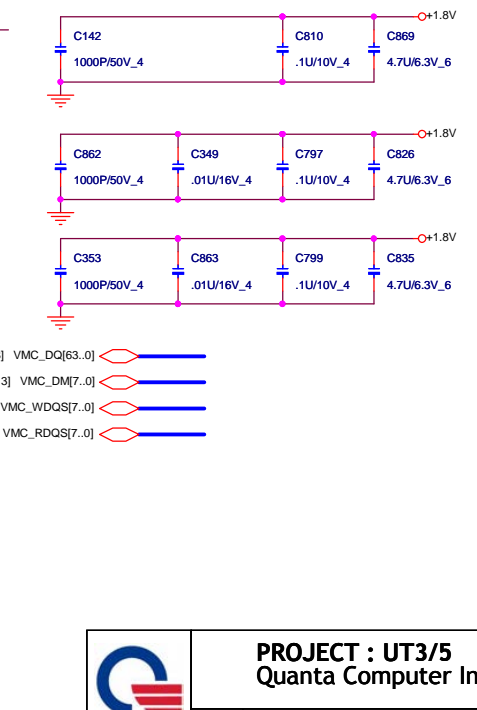
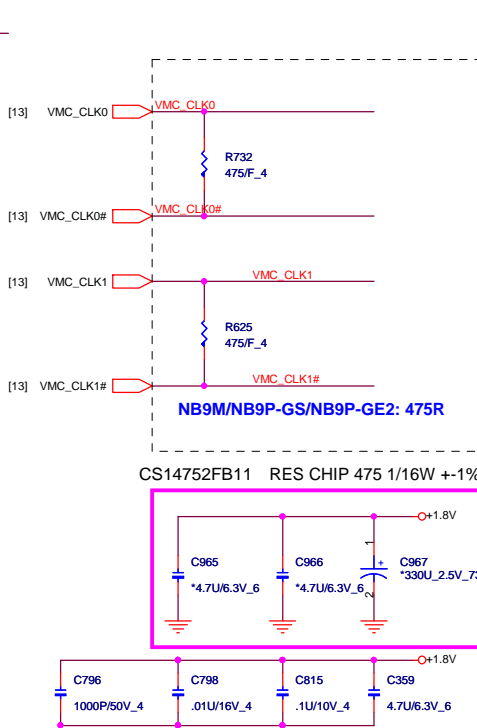
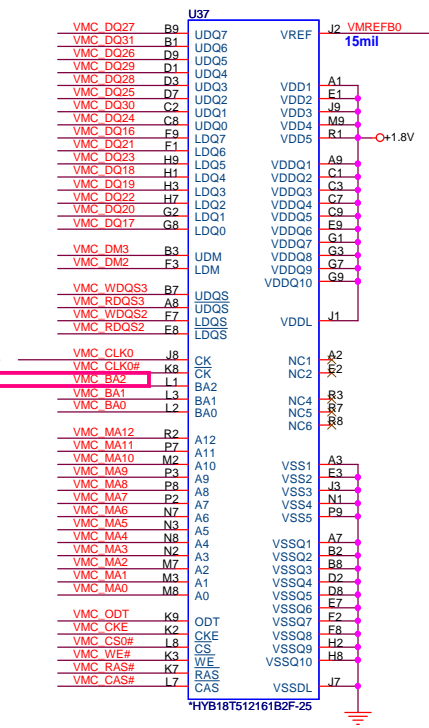
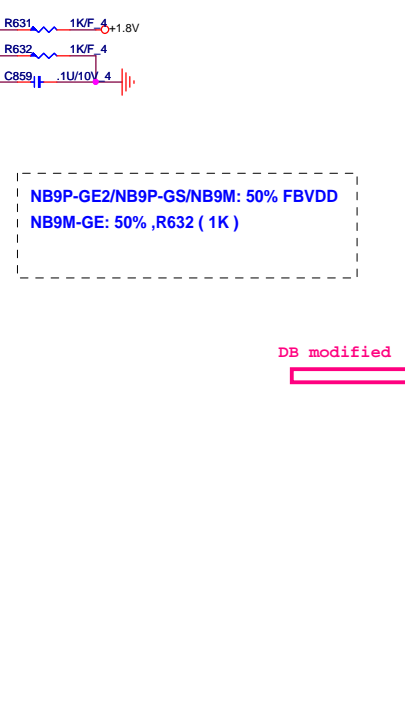
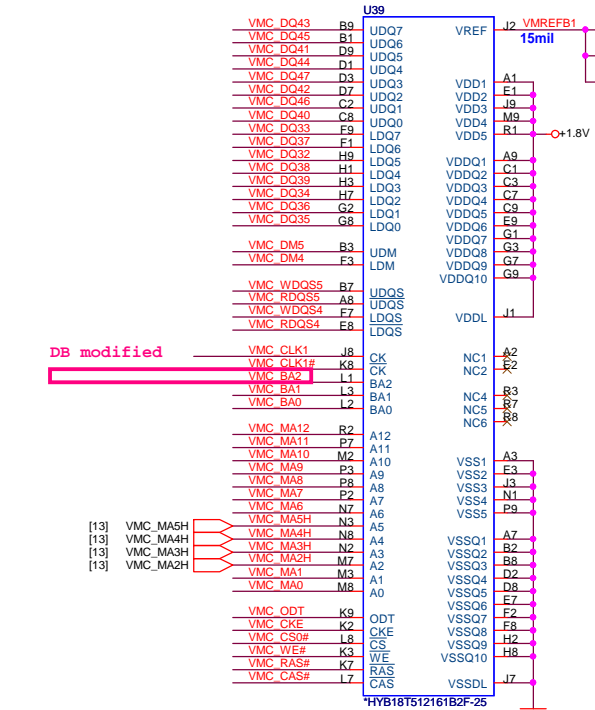
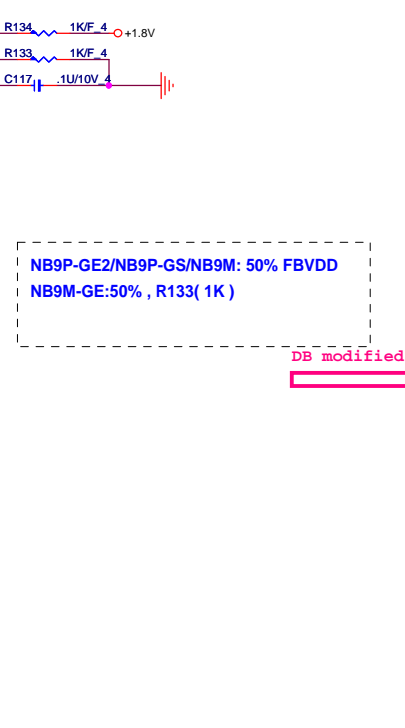
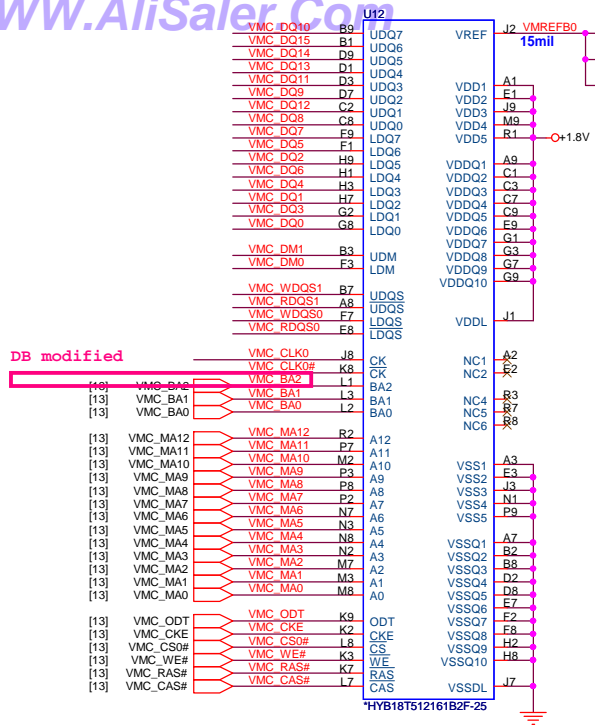


- [13] VMA_CLK0
- [13] VMA_CLK0#
- [13] VMA_CLK1
- [13] VMA_CLK1#

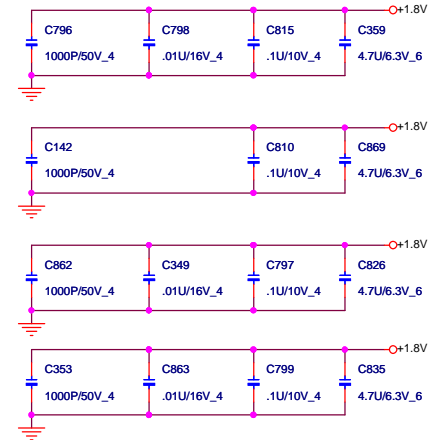
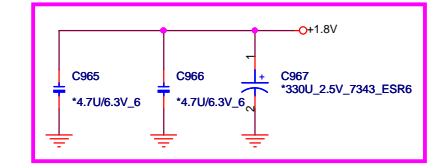


PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X VRAM-1(GDDR2 BGA84)	PV
Date:	Monday, October 20, 2008	Sheet 17 of 43



CS14752FB11 RES CHIP 475 1/16W +-1%(0402)



- [13] VMC_DQ[63..0]
- [13] VMC_DM[7..0]
- [13] VMC_WDQS[7..0]
- [13] VMC_RDQS[7..0]

Samsung
Qimonda
Hynix

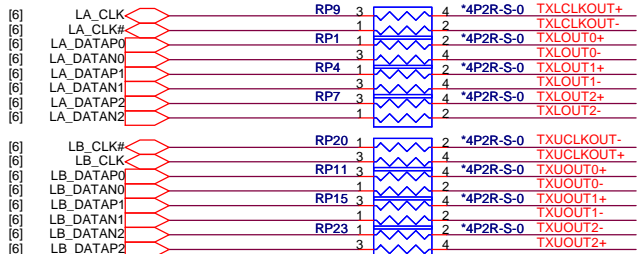


PROJECT : UT3/5
Quanta Computer Inc.

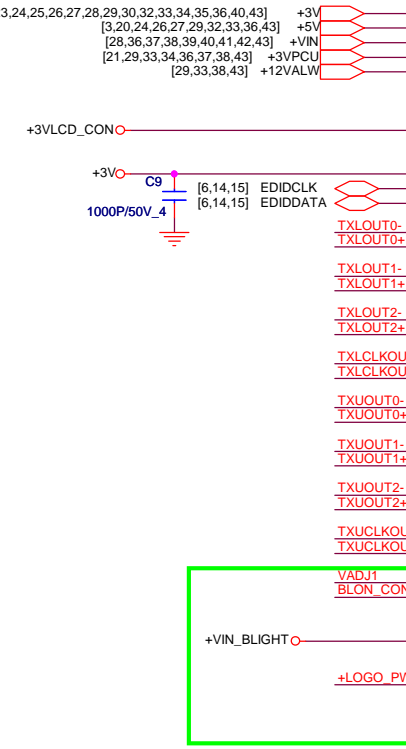
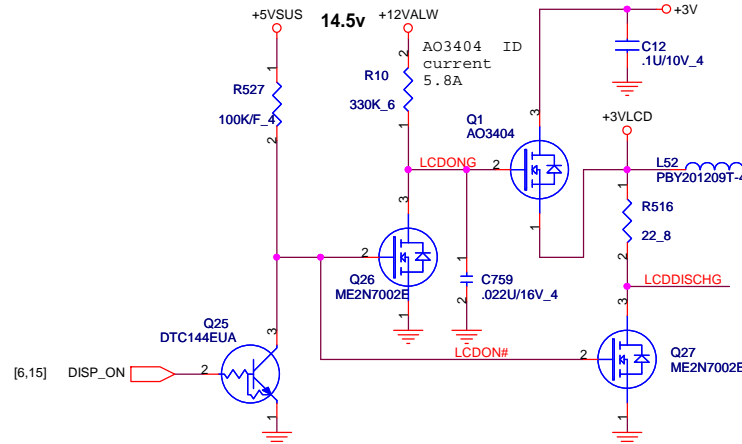
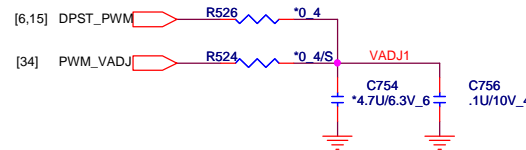
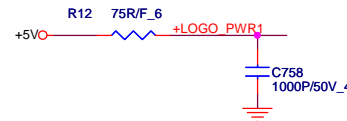
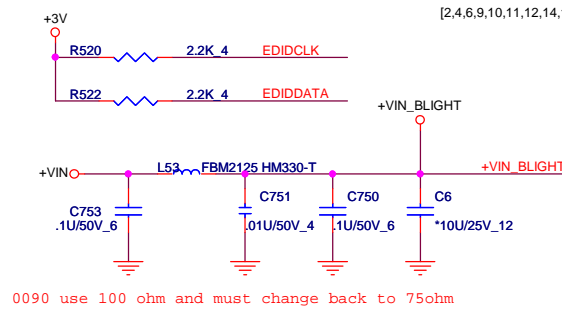
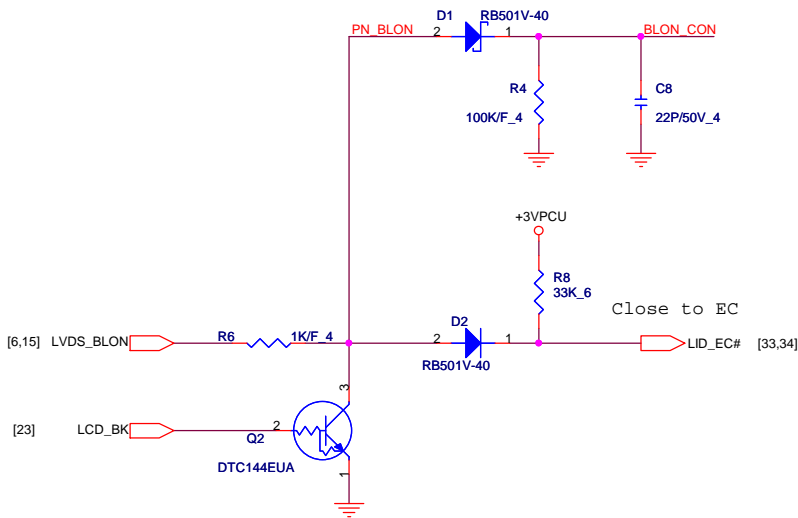
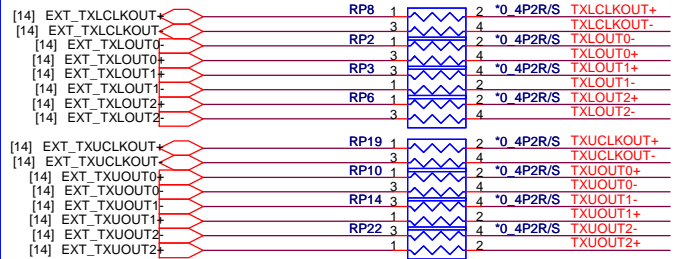
Size	Document Number	Rev
Custom	NV9X VRAM-2(GDDR2 BGA84)	PV
Date: Monday, October 20, 2008	Sheet 18 of 43	

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA



PROJECT : UT3/5
Quanta Computer Inc.

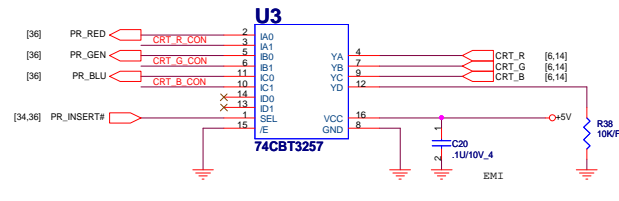
Size	Document Number	Rev
B	LCD CONN/Lid function	PV
Date:	Monday, October 20, 2008	Sheet 19 of 43

CRT PORT

Change Layout footprint to dsb-070546fr015sx682r-15p-v

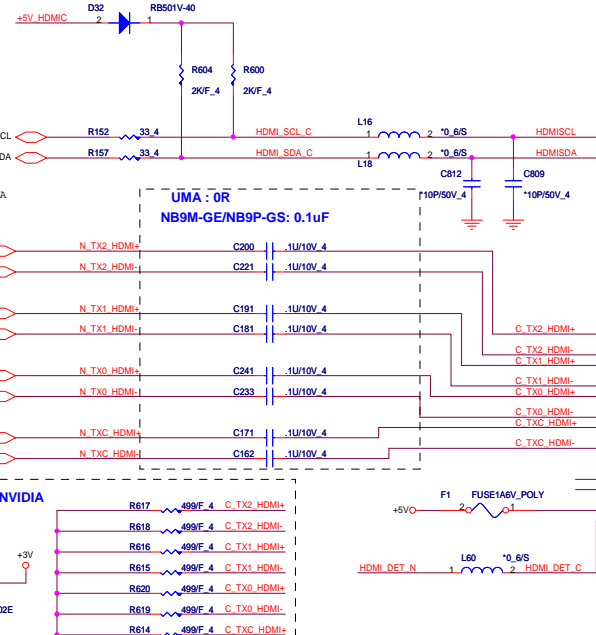
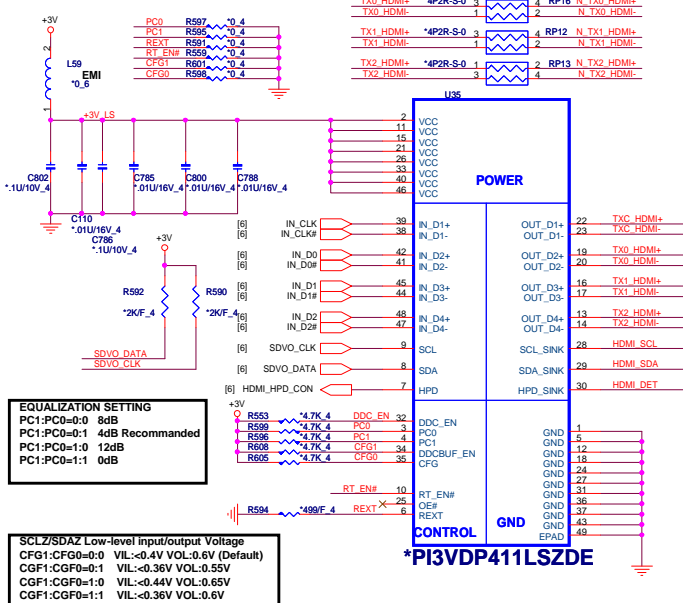
Change ESD protection to +5V

CRT SWITCH



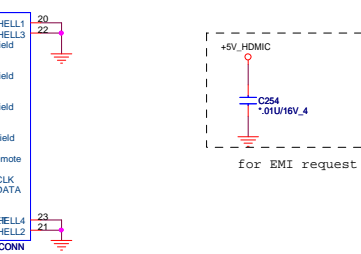
inputs	function
/E	SET
L	Y - port 0
L	Y - port 1
H	Disconnect

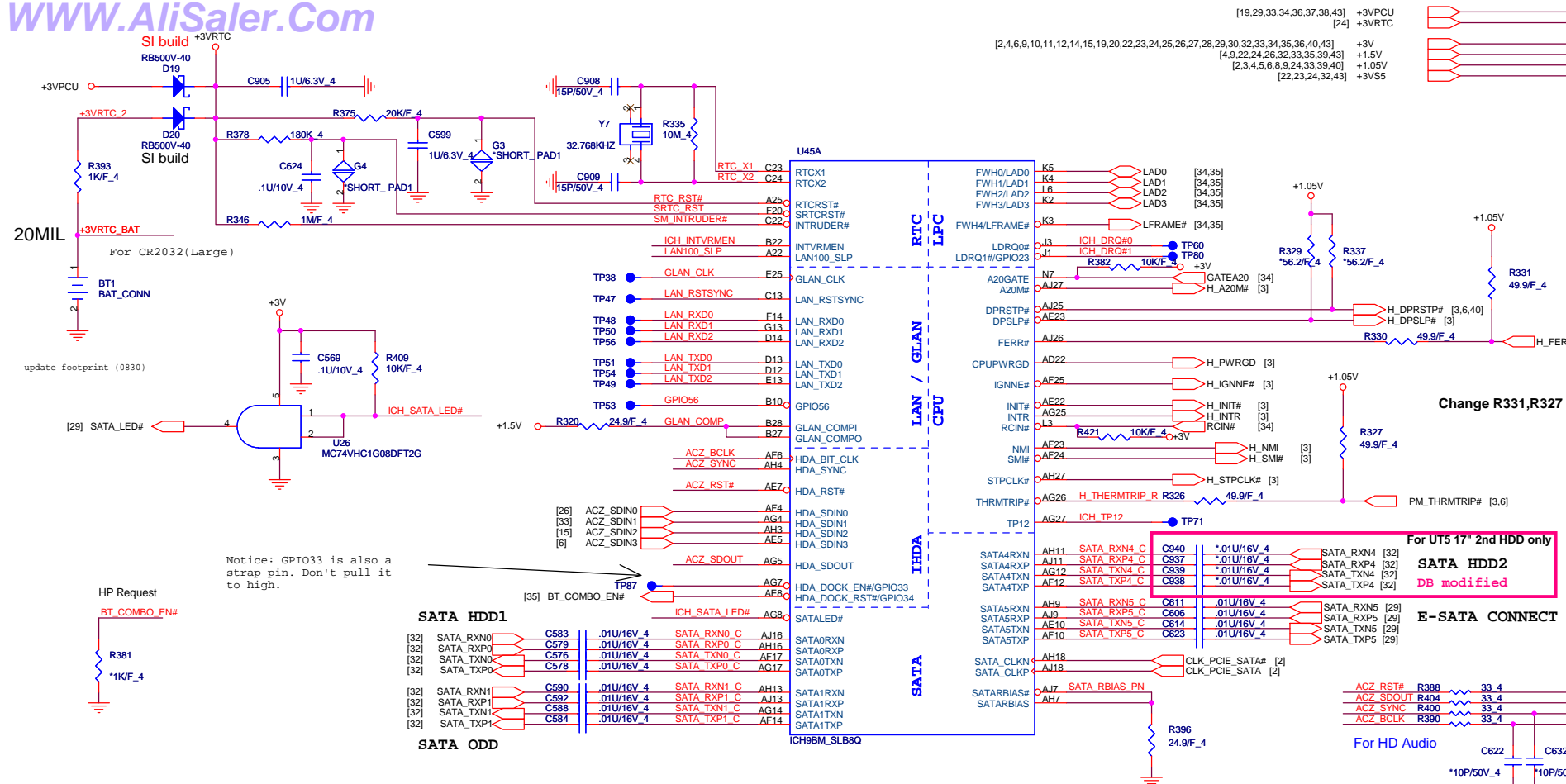
For UMA HDMI function



HDMI PORT

DFHD19MR021





SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsusi_05,VccSus1_5 and VccCL1 5)	ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)
---	---

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)	LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
----------	---	------------	---

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

*1K/F_4 R391 GNT3# [22]

No Reboot Strap	
CZ_SPKR	Low: Default Hi: No reboot

TPM physical presence	
CH_GPIO57	Low: Default

For UT5 17" 2nd HDD only

[32]	
[32]	SATA HDD2
[32]	
[32]	DB modified

[29] **E-SATA CONNECT**

ACZ_RST#	R388	33.4	ACZ_RST#_AUDIO	[26]
ACZ_SDOUT	R404	33.4	ACZ_SDOUT_AUDIO	[26]
ACZ_SYNC	R400	33.4	ACZ_SYNC_AUDIO	[26]
ACZ_BCLK	R390	33.4	BIT_CLK_AUDIO	[26]

For HD Audio

ACZ_RST# R387 33 4

ACZ_SDOUT R394 33 4

ACZ_SYNC R406 33 4

ACZ_BCLK R398 33 4

ACZ_RST#_MDC [33]

ACZ_SDOUT_MDC [33]

ACZ_SYNC_MDC [33]

BIT_CLK_MDC [33]

For MDC

C635 C656 C657

*10P/50V_4 *10P/50V_4 *10P/50V_4

ACZ_RST# R389 **33.4
ACZ_SDOUT R376 **33.4
ACZ_SYNC R377 **33.4
ACZ_BCLK R395 **33.4

For UMA

C631 C602 C601

*10P/50V_4 *10P/50V_4 *10P/50V_4

ACZ RST#	R745	22.4	NV_HDA_RST		NV_HDA_RST [15]
ACZ SDOUT	R747	22.4	NV_HDA_SDO		NV_HDA_SDO [15]
ACZ SYNC	R748	22.4	NV_HDA_SYNC		NV_HDA_SYNC [15]
ACZ BCLK	R744	22.4	NV_HDA_BCLK		NV_HDA_BCLK [15]

Close to U45 C691 C605 C693

For Discrete *10P/50V_4 *10P/50V_4 *10P/50V_4

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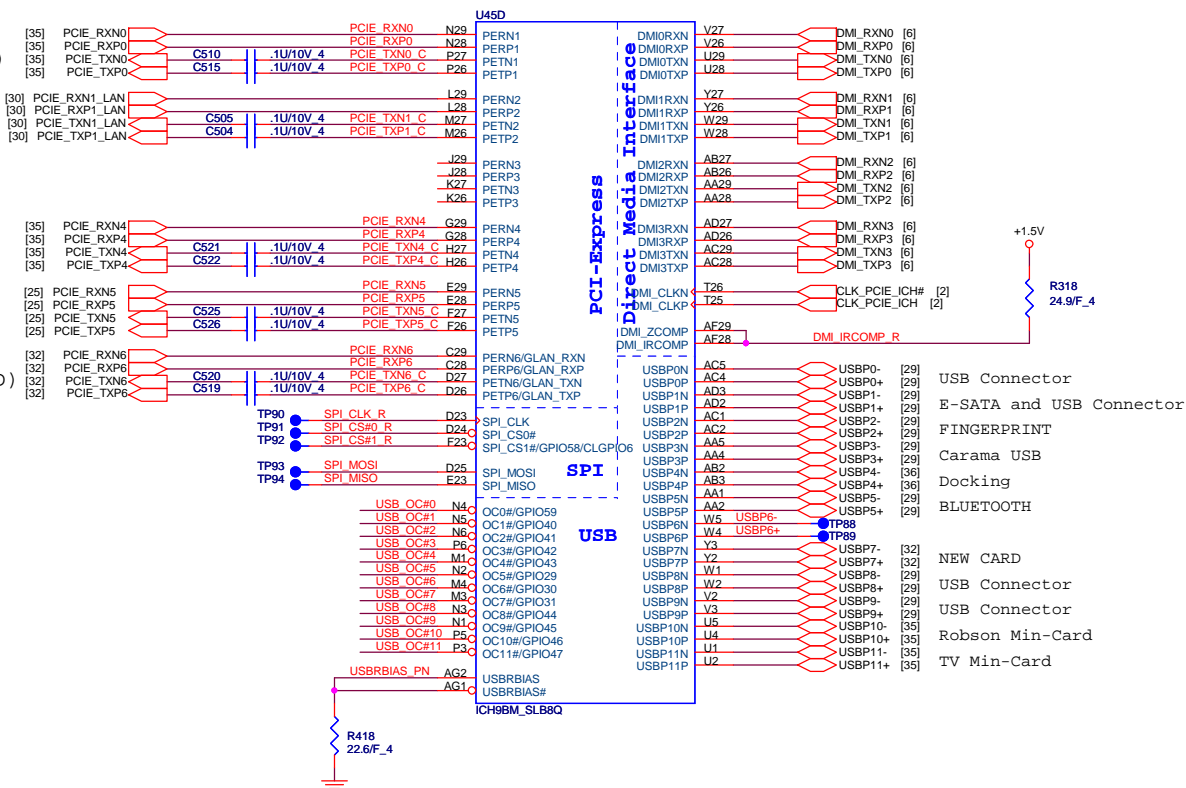
Size Custom	Document Number ICH9-M Host 1/4
Date: Monday, October 20, 2008	Sheet 21 of 43

MINI CARD PCI-E(WLAN)

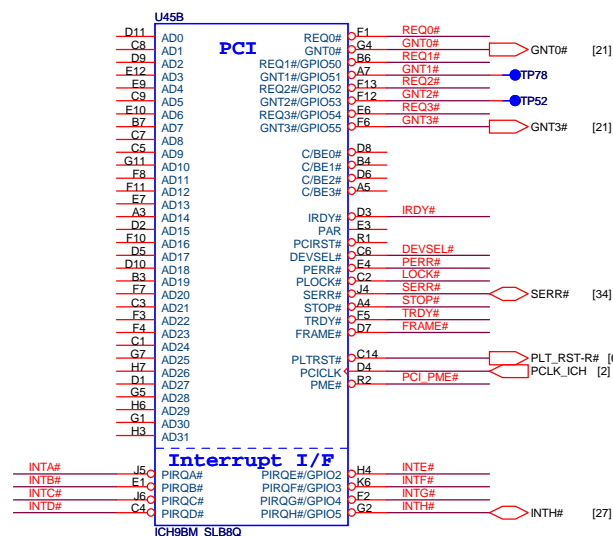
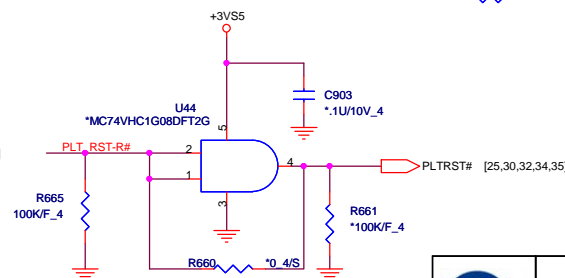
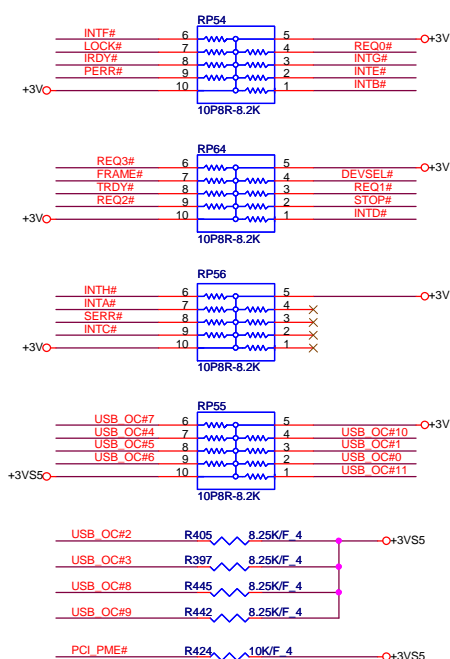
PCIE-LAN

TV CARD PCI-E

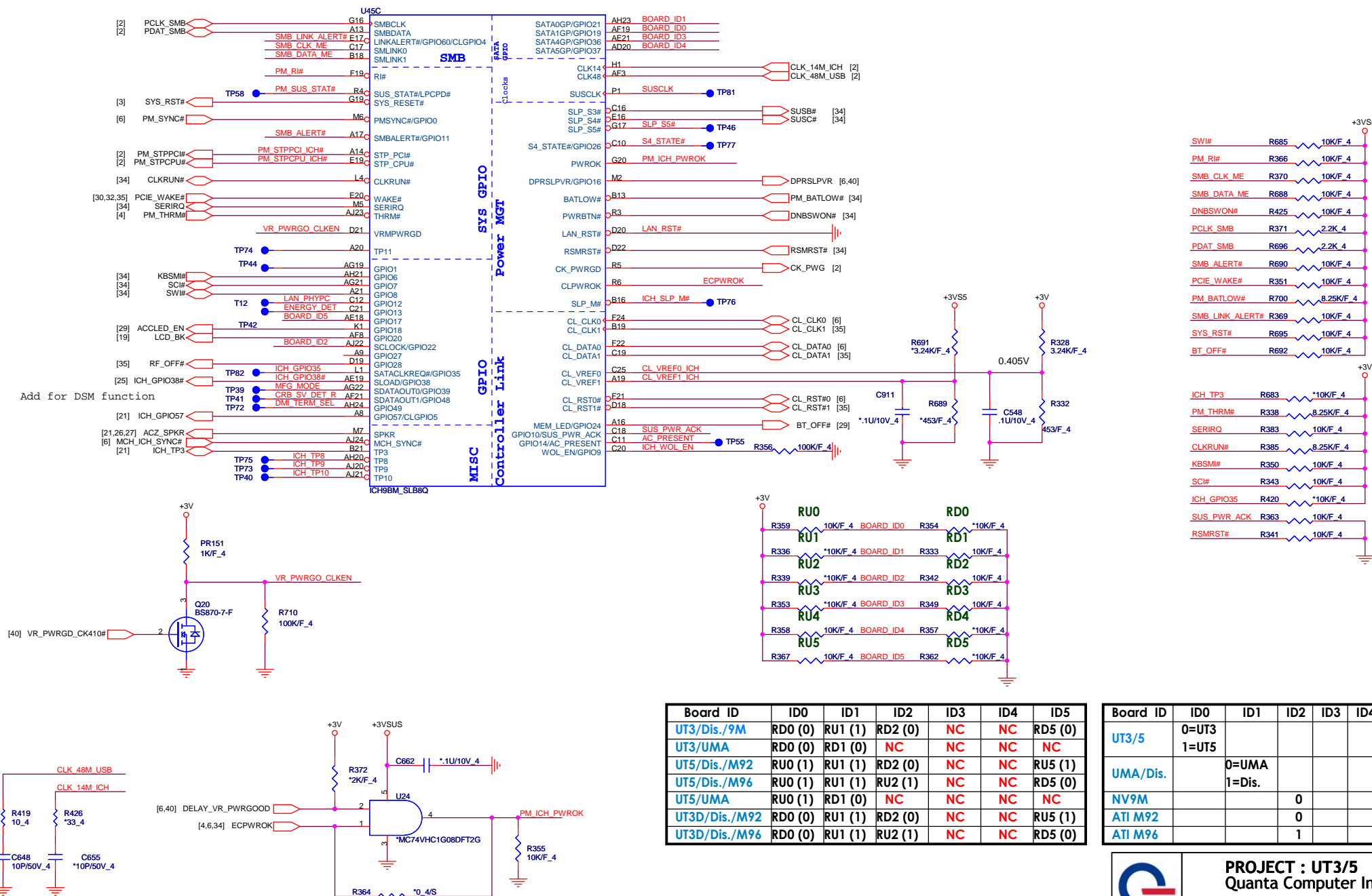
EXPRESS CARD (NEW CARD)



SI-2 Delete
Delete RP53,RP57 and tied from SB to CR(USB6)



[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +1.5V
[4,9,21,22,24,26,32,33,35,39,43] +3V
[21,22,24,32,43] +3VS5
[29,35,39,40,41,43] +3VSUS



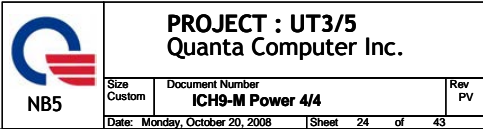
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/Dis./9M	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RD5 (0)
UT3/UMA	RD0 (0)	RD1 (0)	NC	NC	NC	NC
UT5/Dis./M92	RU0 (1)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT5/Dis./M96	RU0 (1)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)
UT5/UMA	RU0 (1)	RD1 (0)	NC	NC	NC	NC
UT3D/Dis./M92	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT3D/Dis./M96	RD0 (0)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)

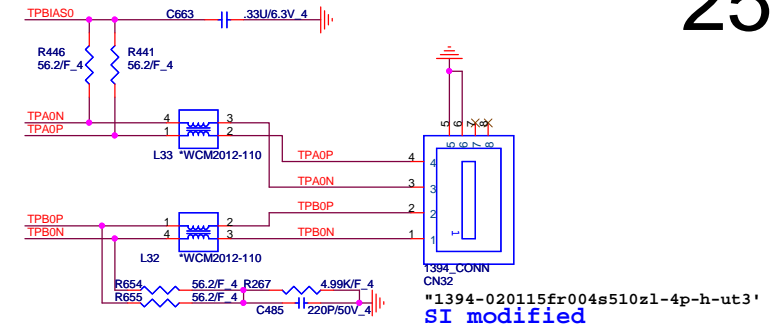
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/5	0=UT3 1=UT5					
UMA/Dis.		0=UMA 1=Dis.				
NV9M			0			0
ATI M92			0			1
ATI M96			1			0



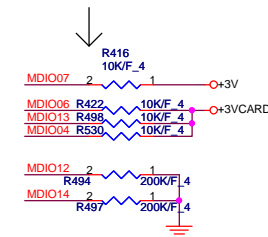
PROJECT : UT3/5
Quanta Computer Inc.

Size Custom Document Number ICH9-M GPIO 3/4 Rev PV
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Change to 10K



	SD/MMC	MS	XD
MD1D0	SD DAT0	MS D0	XD D0
MD1D1	SD DAT1	MS D1	XD D1
MD1D2	SD DAT2	MS D2	XD D2
MD1D3	SD DAT3	MS D3	XD D3
MD1D4	SD CMD	MS BS	XD WE#
MD1D5	SD CLK	MS SCLK	XD CE#
MD1D6	SD WP		XD WP#
MD1D7			XD CLE
MD1D8	SD DAT4		XD D4
MD1D9	SD DAT5		XD D5
MD1D10	SD DAT6		XD D6
MD1D11	SD DAT7		XD D7
MD1D12			XD RE#
MD1D13			XD R/#
MD1D14			XD ALE
CR1 LEON	SD1 LE0N	MS1 LE0N	XD LE0N
CR1 PCTLIN	SD1 PCTL#MS1	PCTL#MS1	PCTL#
CR1 CD0	SD1 CD#		XD CV#
CR1 CDB		MS1 CD#	XD CD#

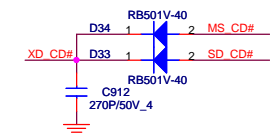
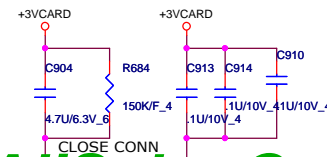
CN36

Pin	Signal	Pin	Signal
1	MDIO13	23	GND
2	MDIO12	24	XD-R/B
3	MDIO05	25	XD-RE
4	MDIO07	26	XD-CE
5	MDIO14	27	XD-CLE
6	MDIO04	28	XD-ALE
7	XD-1VPH L	29	XD-WE
8	MDIO00	30	XD-WP
9	MDIO01	31	XD-D0
10	MDIO02	32	XD-D1
11	MDIO03	33	SD-DAT2
12	MDIO04	34	SD-DAT3
13	MDIO05	35	SD-CMD
14	MS_CD#	36	GND
15	MDIO00	37	MS-VCC
16	MDIO03	38	MS-SDLK
17	MS_CD#	39	MS-DATA3
18	MDIO02	40	MS-NS
19	MDIO00	41	XD-D4
20	MDIO01	42	XD-D3
21	MDIO04	43	XD-D2
22	GND	44	XD-D1
		45	SD-CLK
		46	MS-BS
		47	GND
		48	SD-VCC
		49	SD_CD#
		50	MDIO06
		51	XD_CD#
		52	MDIO11
		53	MDIO09
		54	MDIO08
		55	MDIO07
		56	MDIO06
		57	MDIO05
		58	MDIO04
		59	MDIO03
		60	MDIO02
		61	MDIO01
		62	MDIO00

+3VCCARD

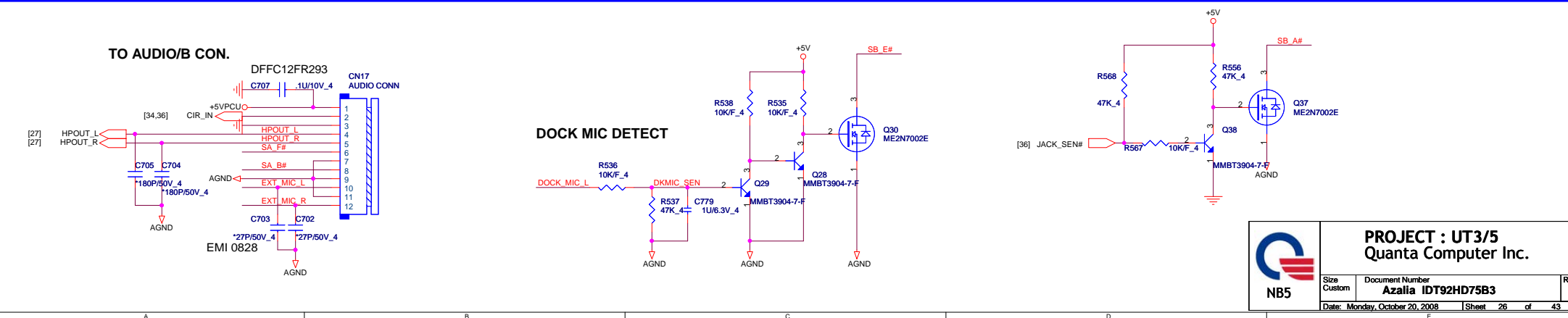
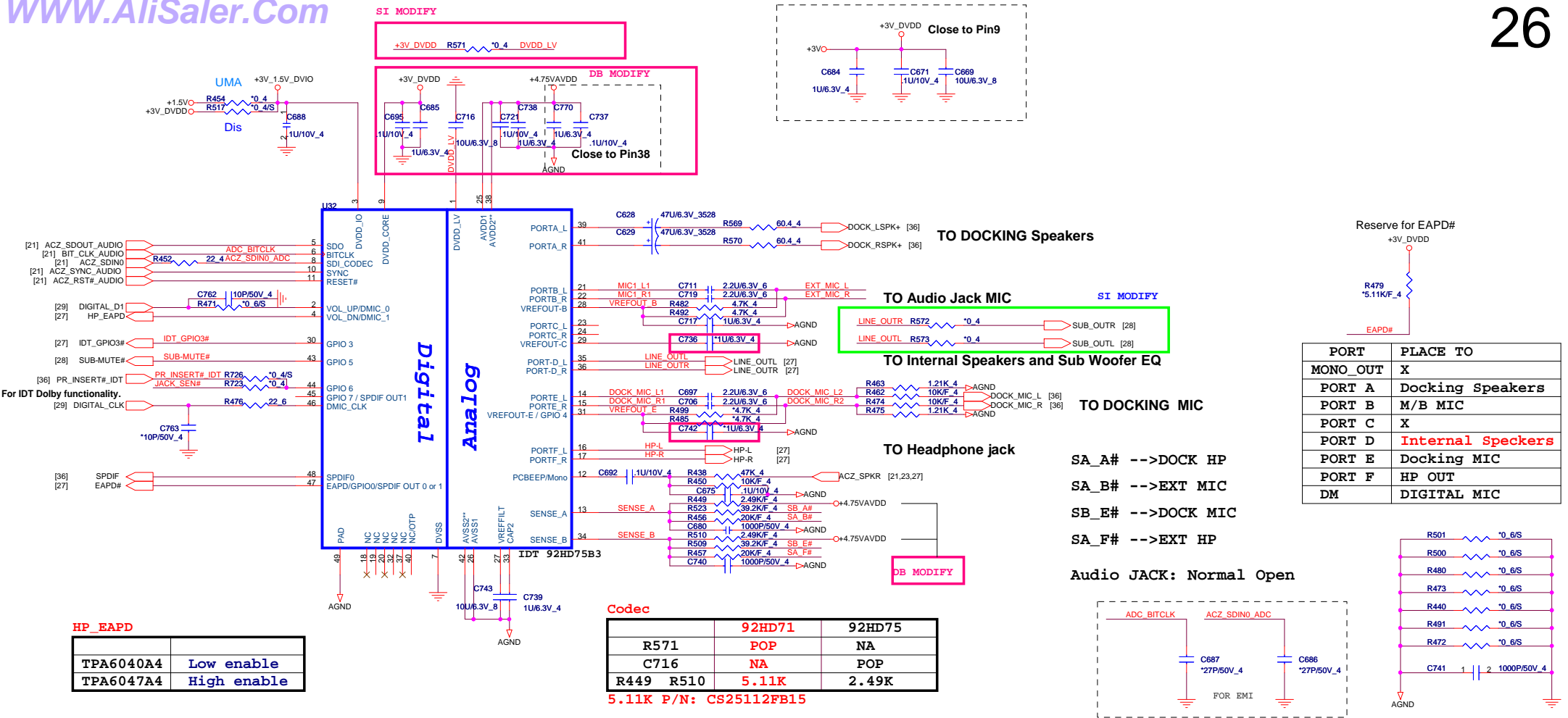
+3VCCARD

***TAI TWUM 51N1 CARD READER SOCKET**

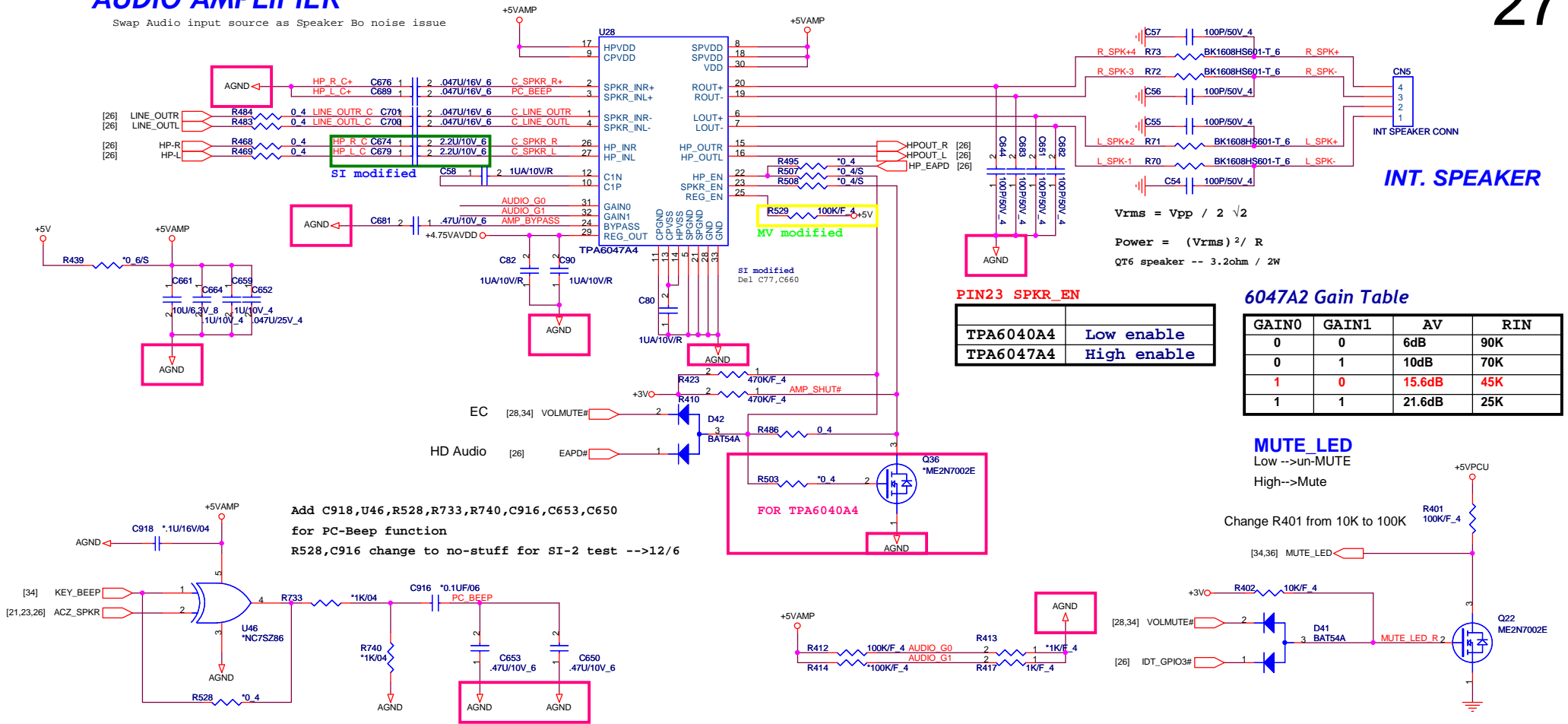


NB5

Size Custom	Document Number RTS5158 & CR SOCKET &HOLE	Rev PV
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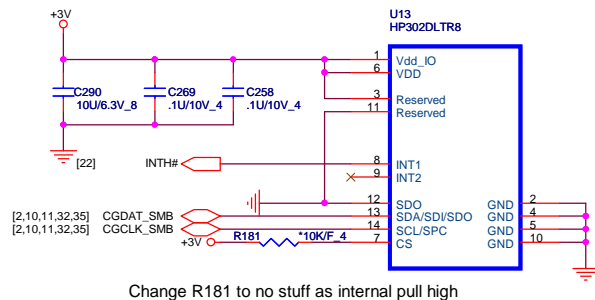


Swap Audio input source as Speaker Bo noise issue

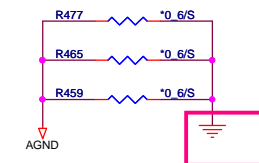
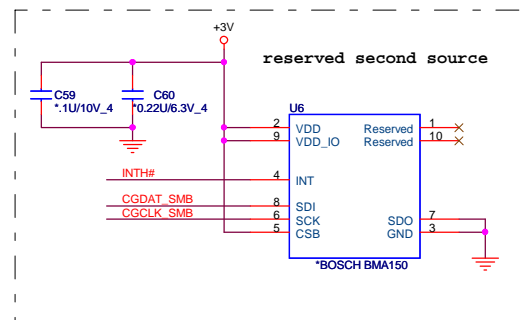


Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi, BIOS need to programming 22h to change status from active Hi to low

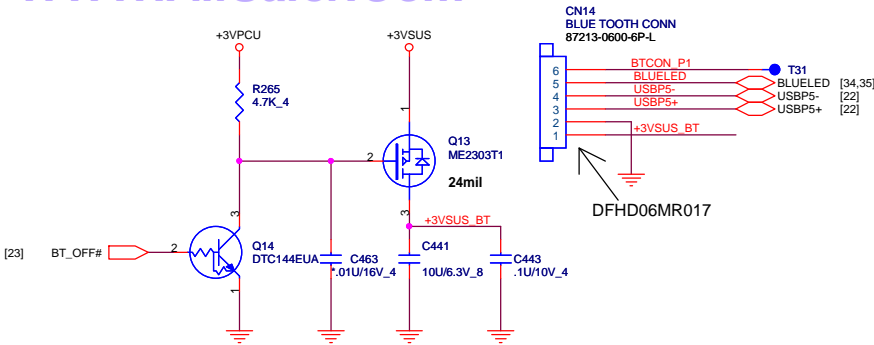


Pin 12: Low 38hex
Pin 12: unconnected/floating 3Ahex



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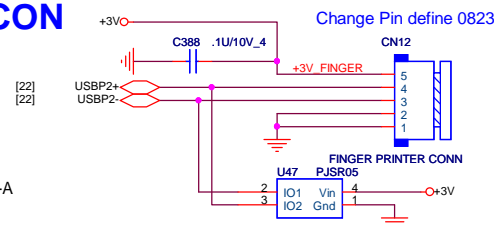
Size	Document Number	Rev
Custom	AMP_TPA6017/Accelerometer	PV
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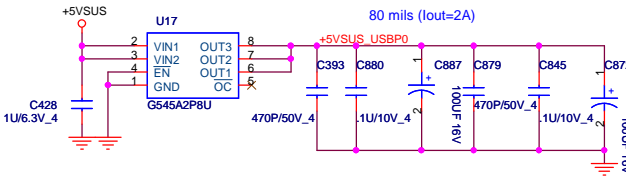
USB fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+

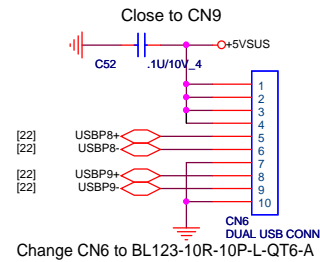
Change CN12 to BL123-05R-5P-L-QT6-A
Add U47 for Finger print USB signal



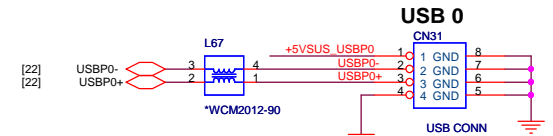
LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2



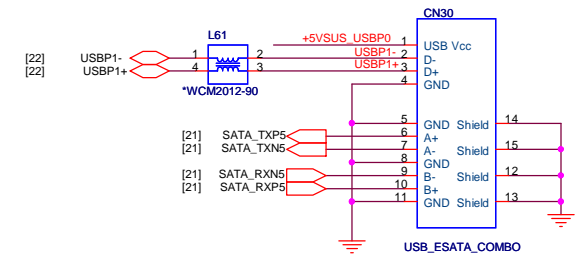
Change CN6 to BL123-10R-10P-L-QT6-A



SI modified

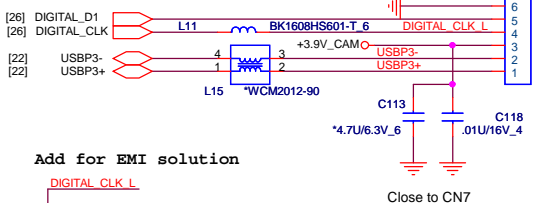
usb-020173mr004s51-4p-r-h-ut3

USB & ESATA

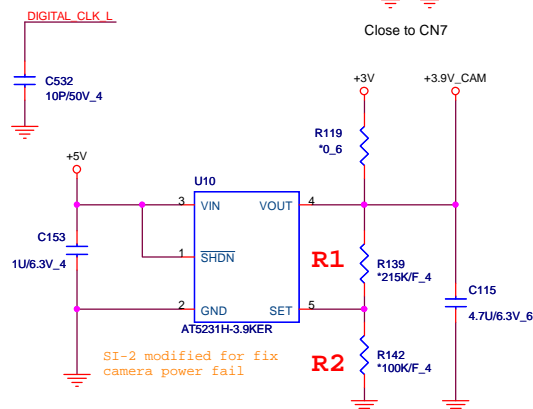


USB CAMERA /DIGITAL MIC CONNECT

SI-2 Build CN9
Change Footprint to 88266-0600-6P-L-QT8

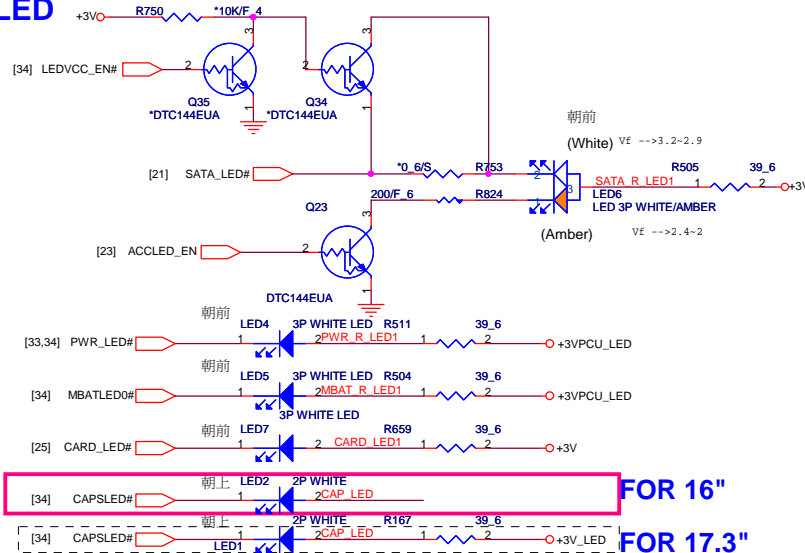


Add for EMI solution



$$V_{out} = 1.25(1 + R_1/R_2)$$

LED



FOR 16"

FOR 17.3'

FOR 16"

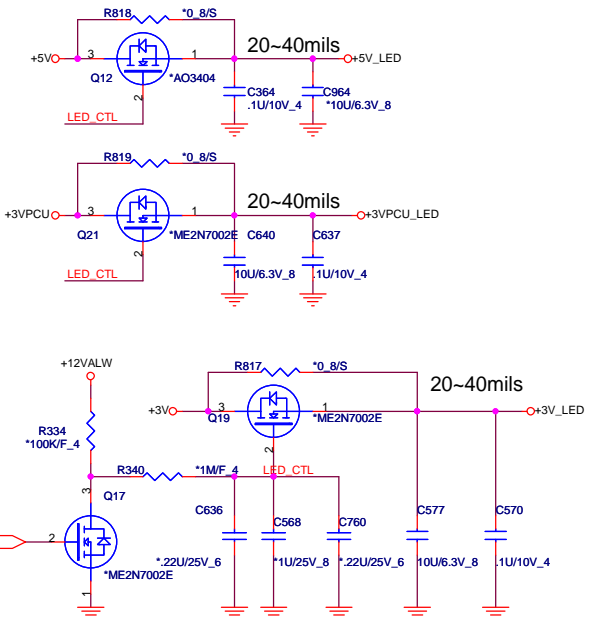
 V_{CC}

FOR 17.3"

WWW.AliSaler.Com

LED PWR CONTROL

Change Q12 to AO3404 as LED current limited



PROJECT : UT3/5
Quanta Computer Inc.

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Stuffed for 8102E/RTL8111C

U18#63 wider than 40 mils
U18#1 wider than 60 mils

+LAN_A1.8_FB12
C531
.1u/10V_4
New add and Close to Pin 5
From Vendor EMI suggest

8111C = No Mount
8102E = Mount

```
Swap PCIE from Port 6 to PCIE Port 2
```

Remove 8111B and 8101E support in PV Build

1. Delete R264 (For 8111B)
2. Delete R650 and T28
3. Delete R651 and U18#33 for 8111B support
4. Delete R231 as RSET
5. Delete R242,R243,R244,R245,C394,C395 8101E support

Stuffed for RTL8101E

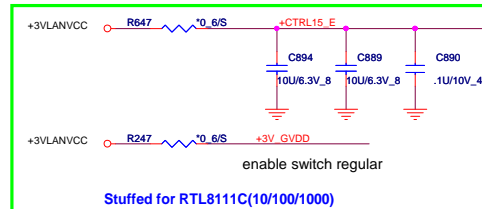
Add C898,C899,C900,C902 as HP request

Link

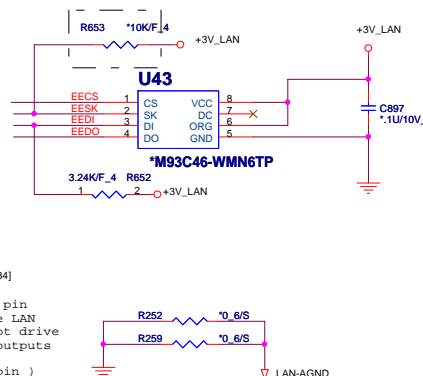
AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
AL08102E001 IC CTRL(64P) RTL8102E-VB-GR(QFN)

```
| NS892402:GIGABIT | DB0AT9LAN05
```

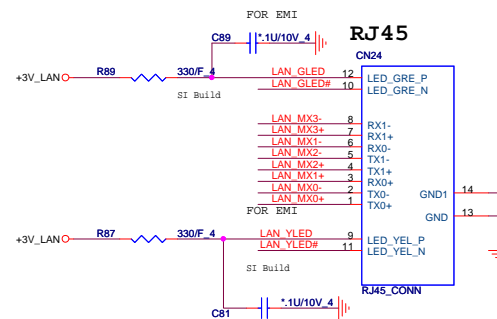
110581-1



for 93C56 used. NC if 93C46 is used.

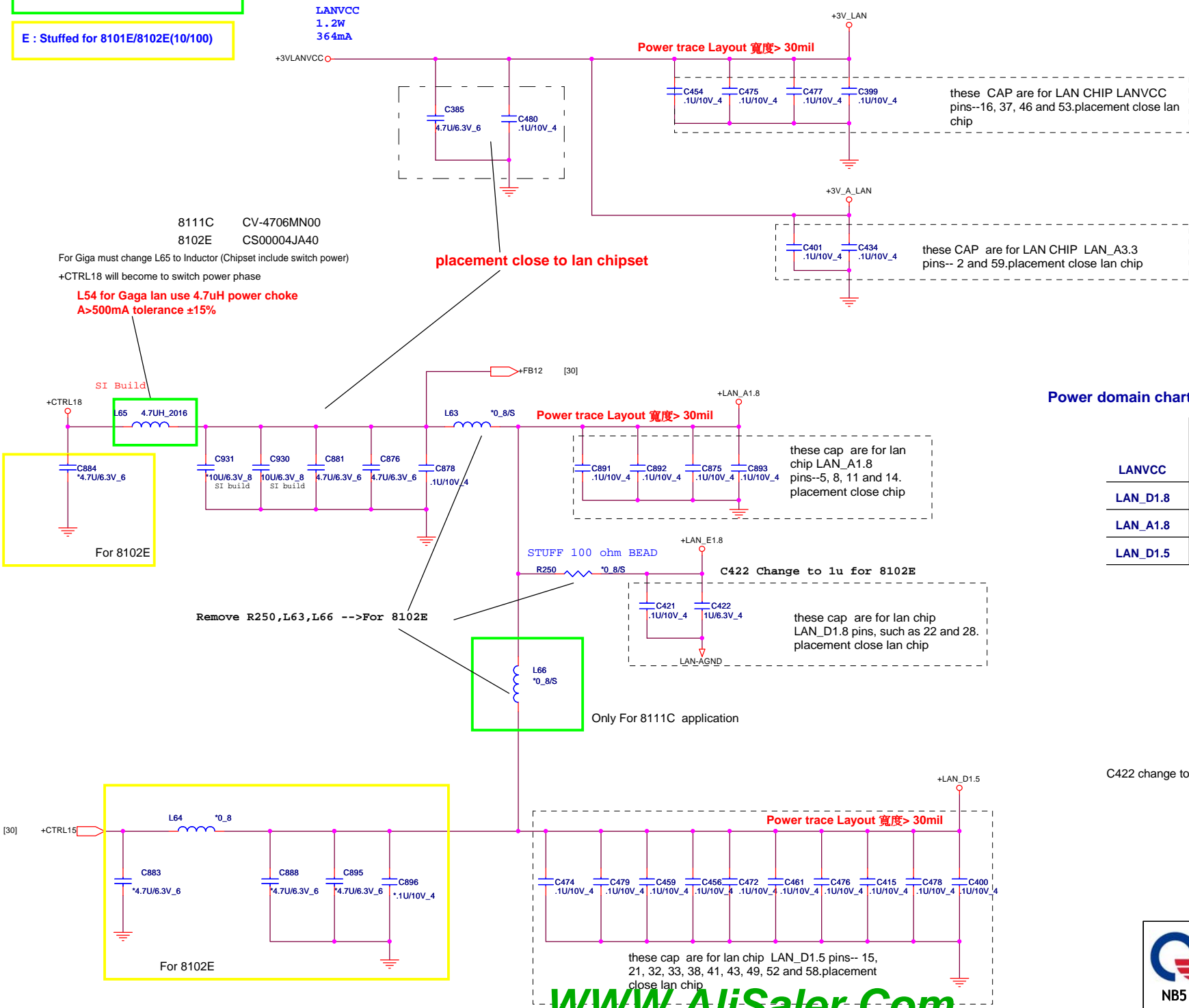


Swap PCIE from Port 6 to PCIE Port 1



T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

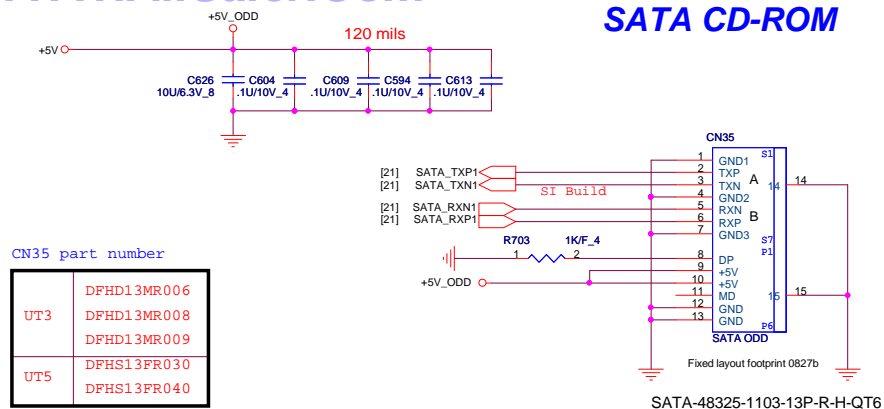


Power domain chart

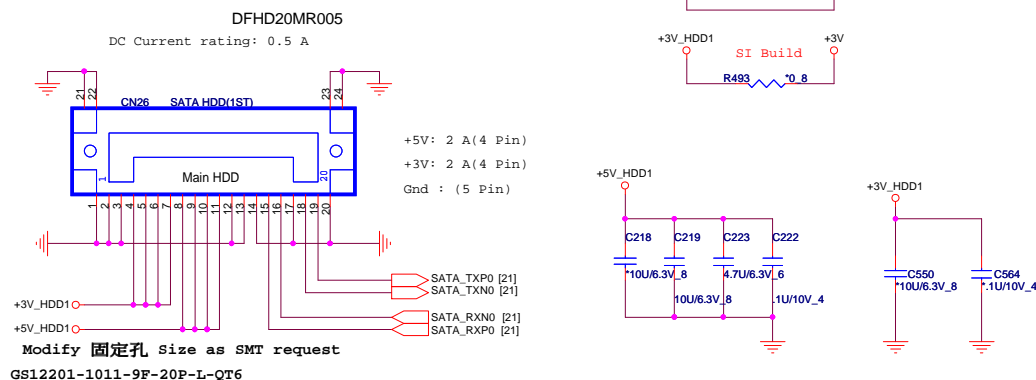
	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

C422 change to 1uf

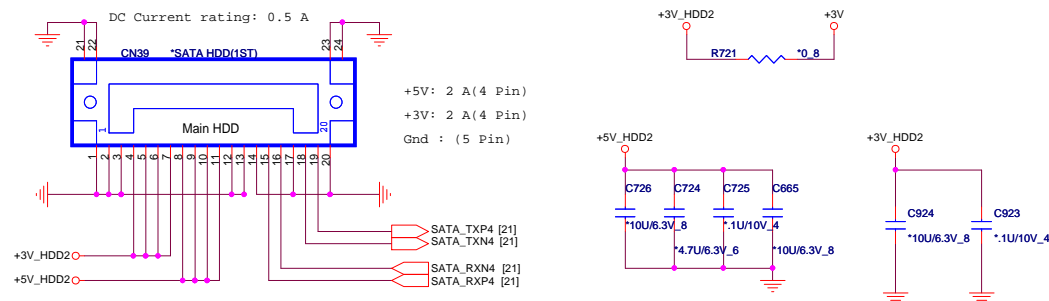
SATA CD-ROM



SATA HDD CONNECTOR

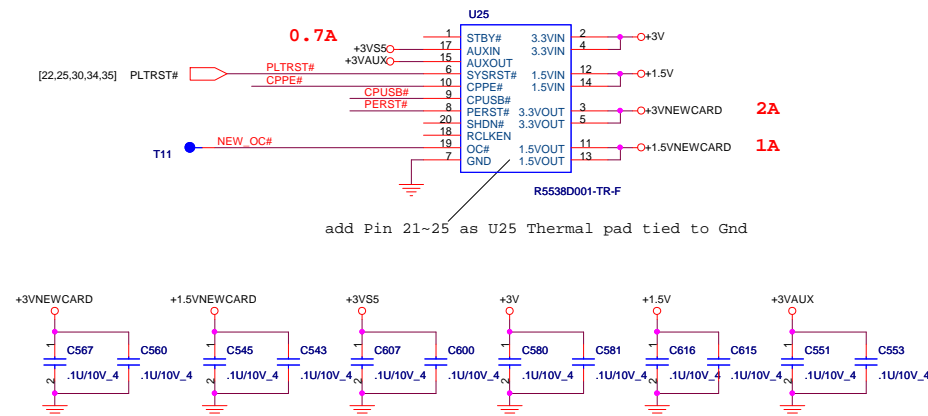
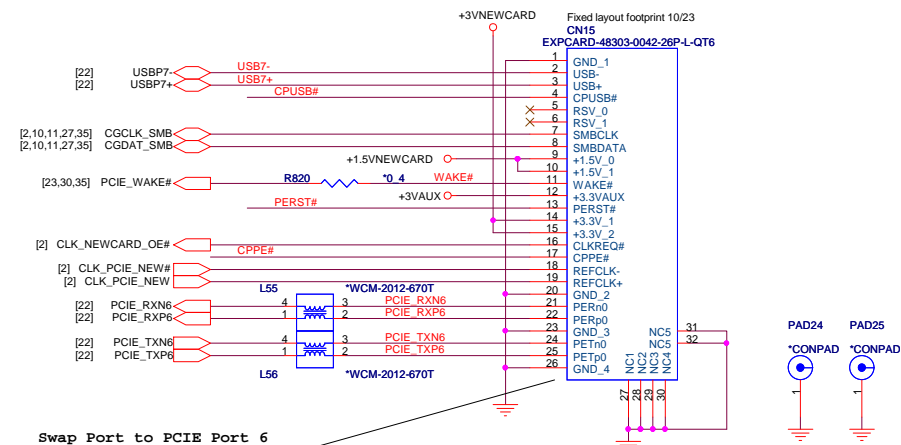


SATA_2 CONNECTOR



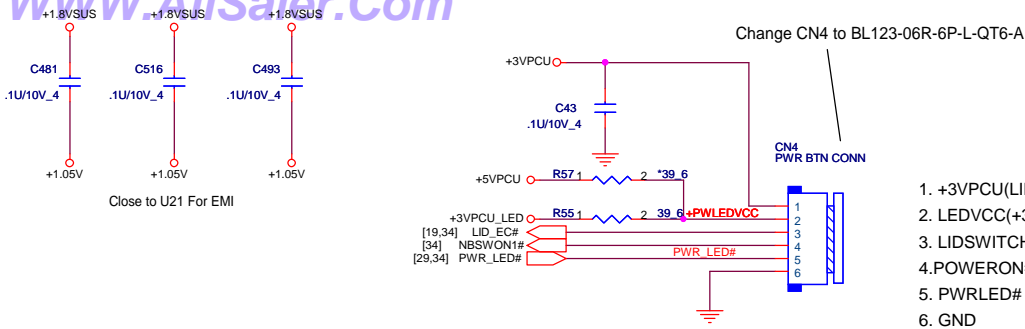
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

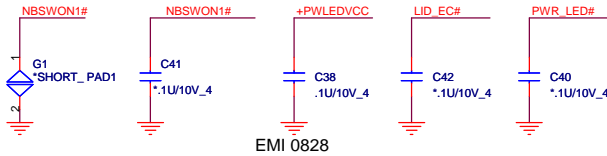


	Header	Housing
MLX	DFHD26MS012	DFHS26FR023
FOX	DFHD26MS013	DFHS26FR024
DGN	DFHD26MS017	DFHS26FR028

PROJECT : UT3/5 Quanta Computer Inc.		
Size Custom	Document Number ODD/HDD/NEW CARD	Rev PV
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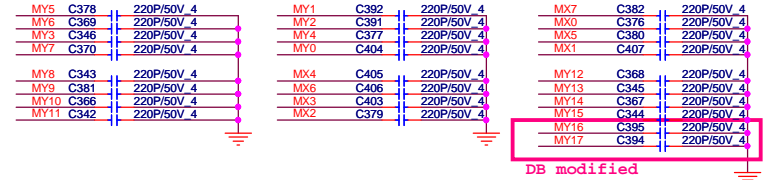
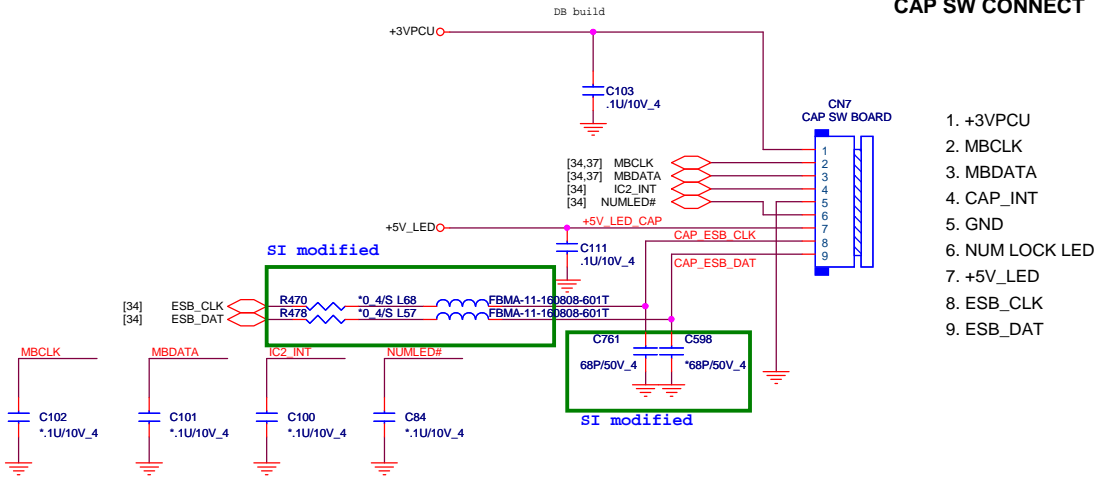


POWER BOTTOM CONNECT

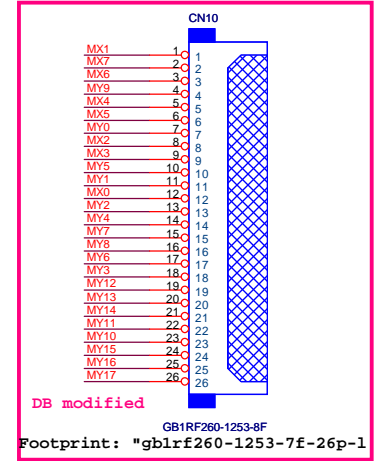
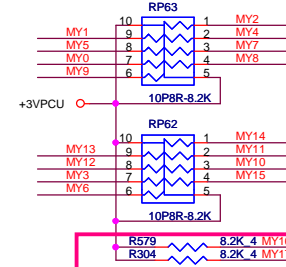


POWER SW CONNECT

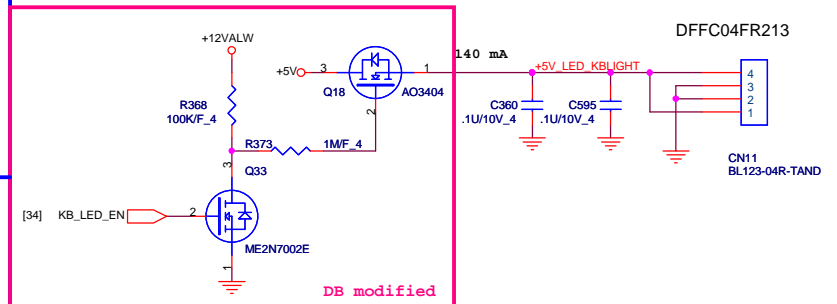
CAP SW CONNECT



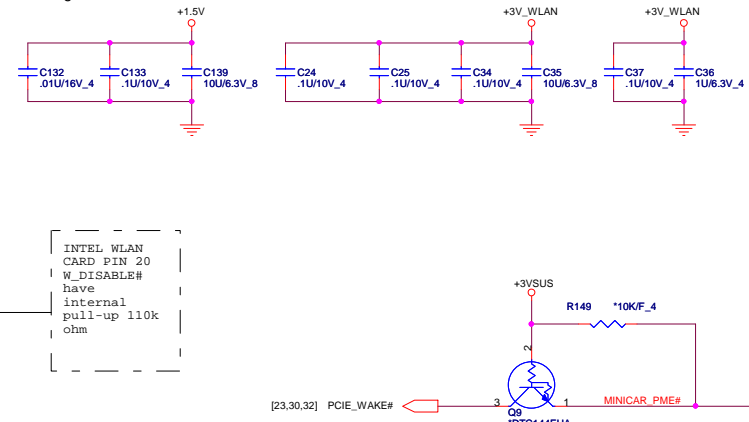
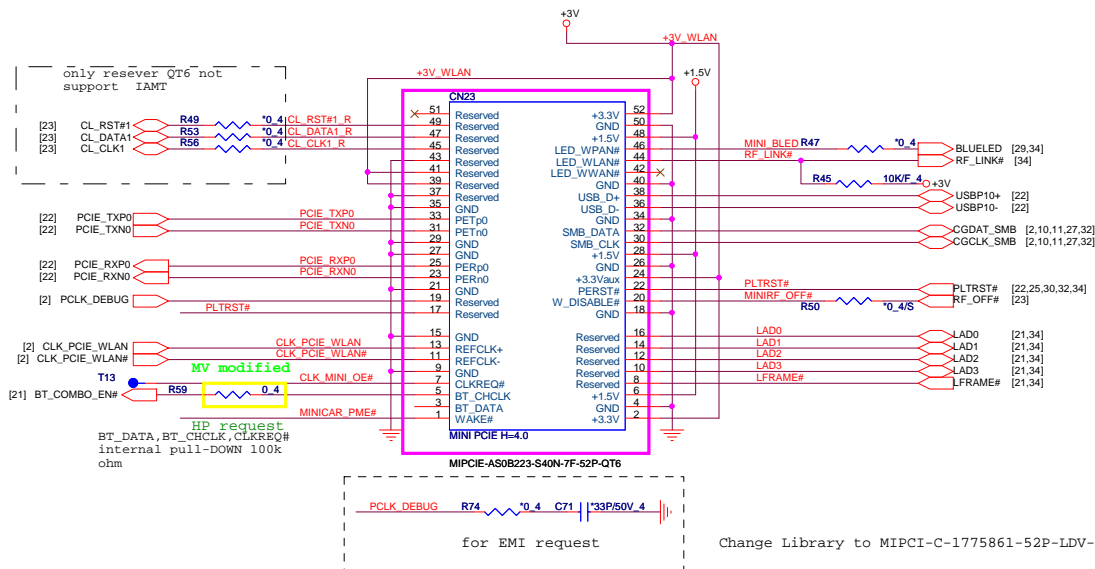
KEYBOARD PULL-UP



clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

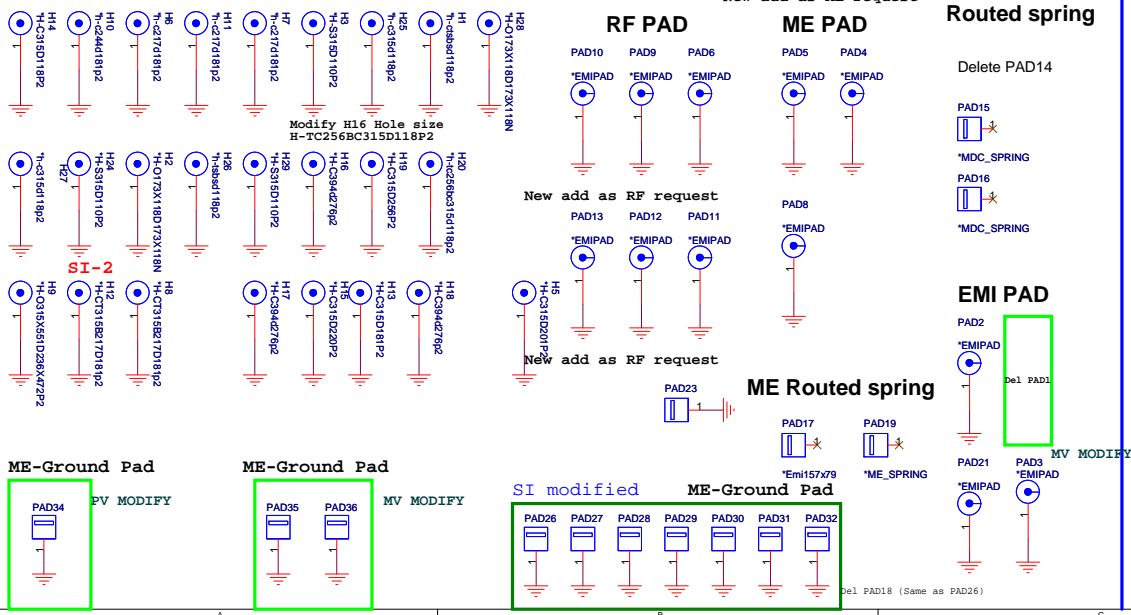




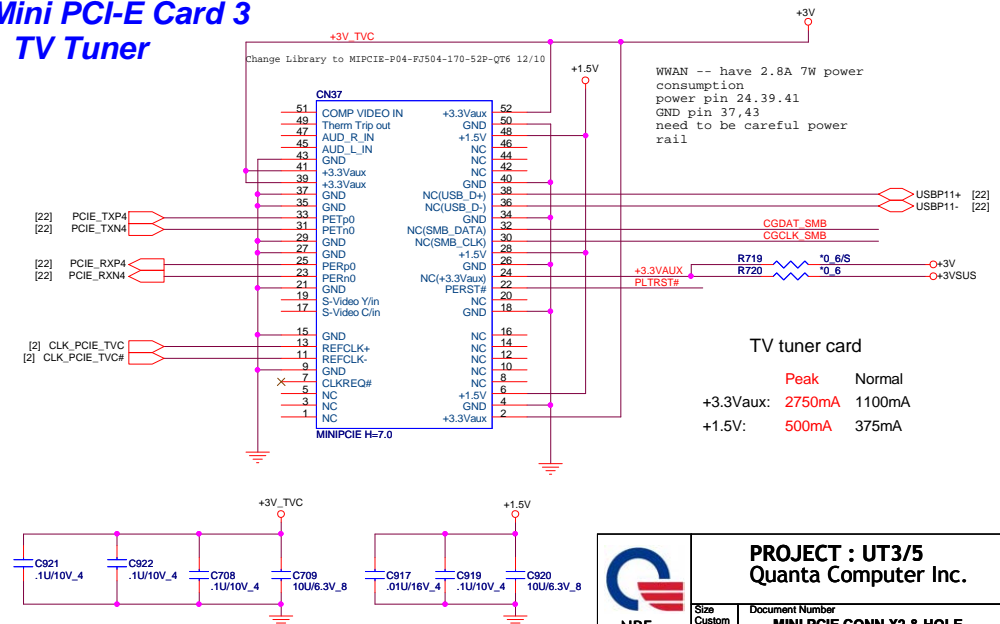



M/B Screw Hole

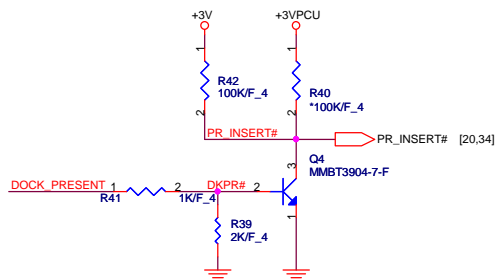
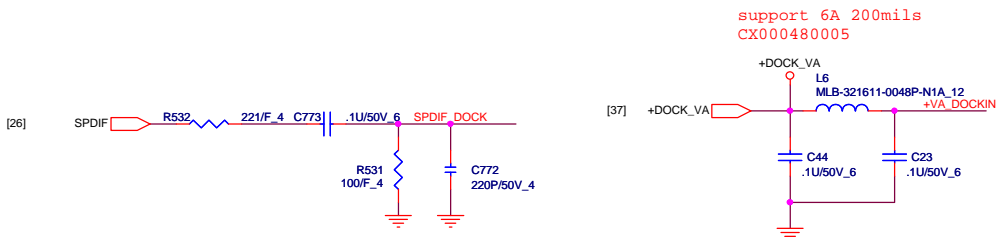
SI-2,h-e276x315d118p2



Mini PCI-E Card 3 TV Tuner

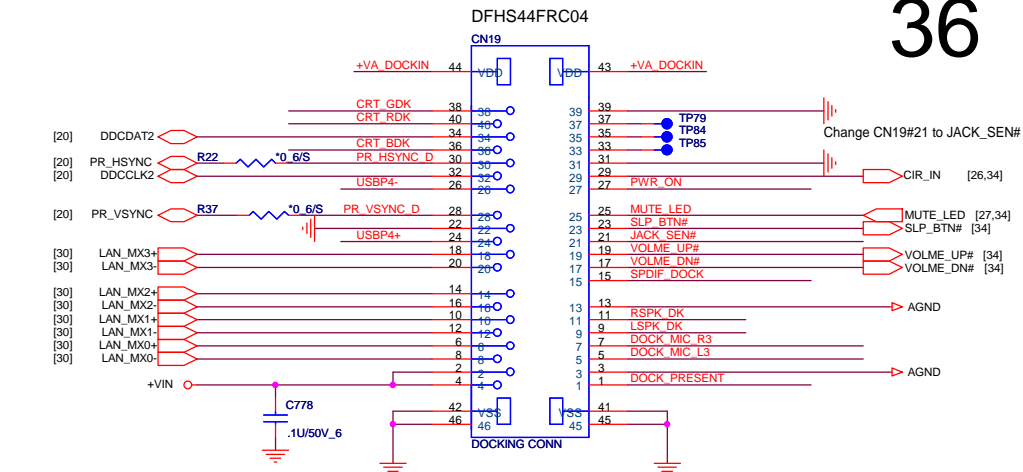
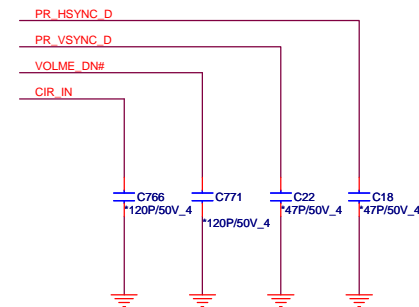
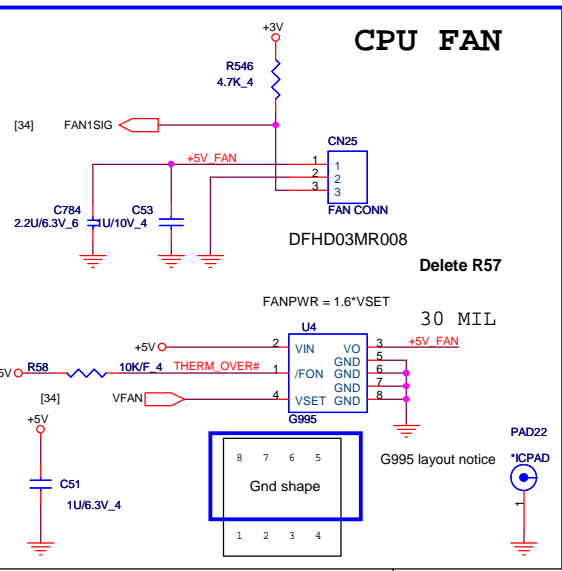
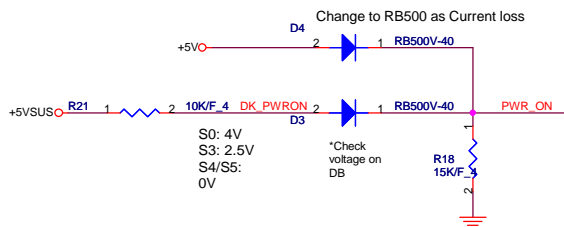


 NB5	PROJECT : UT3/5 Quanta Computer Inc.		
	Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev PV
Date: Monday, October 20, 2008		Sheet 35 of 43	



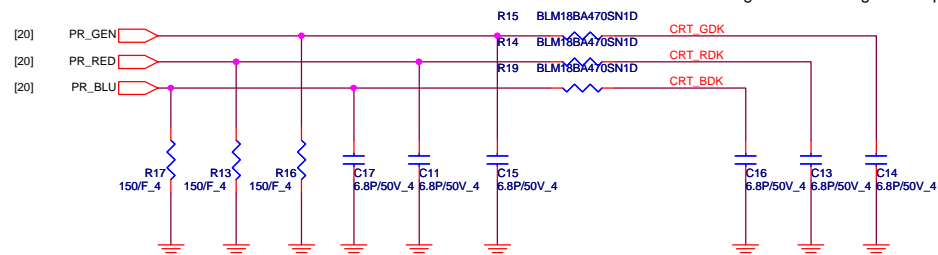
For IDT Dolby functionality.

DB modified

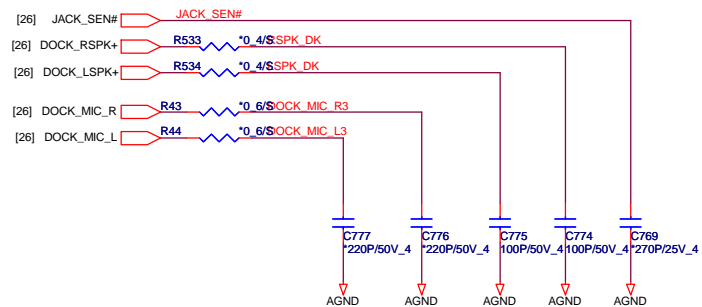


R13,R16,R17 Change to install

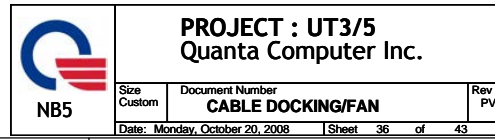
Delete CX08T470000 as CRT rising time and falling time request

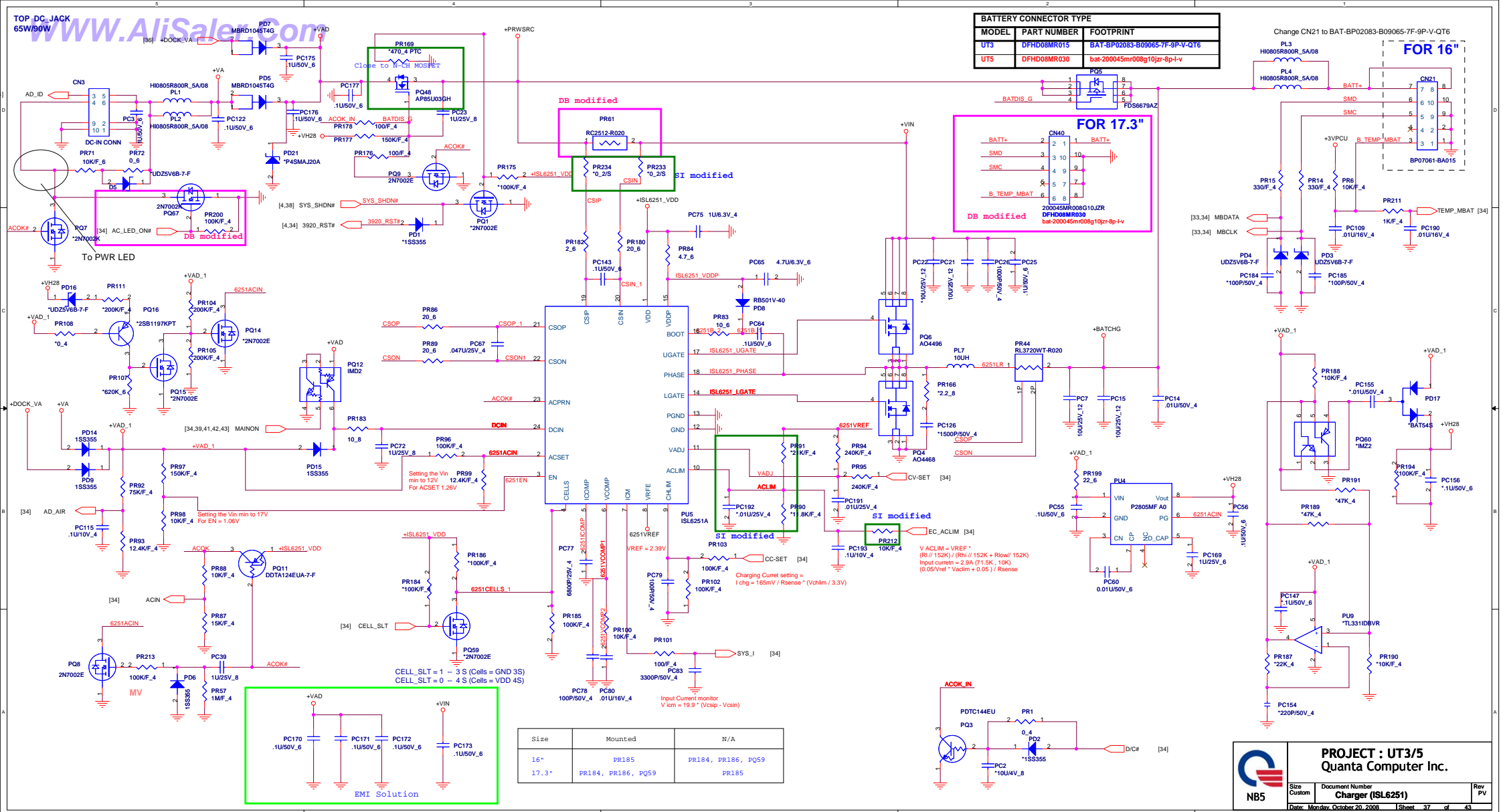


Add Loss net(GND Net)



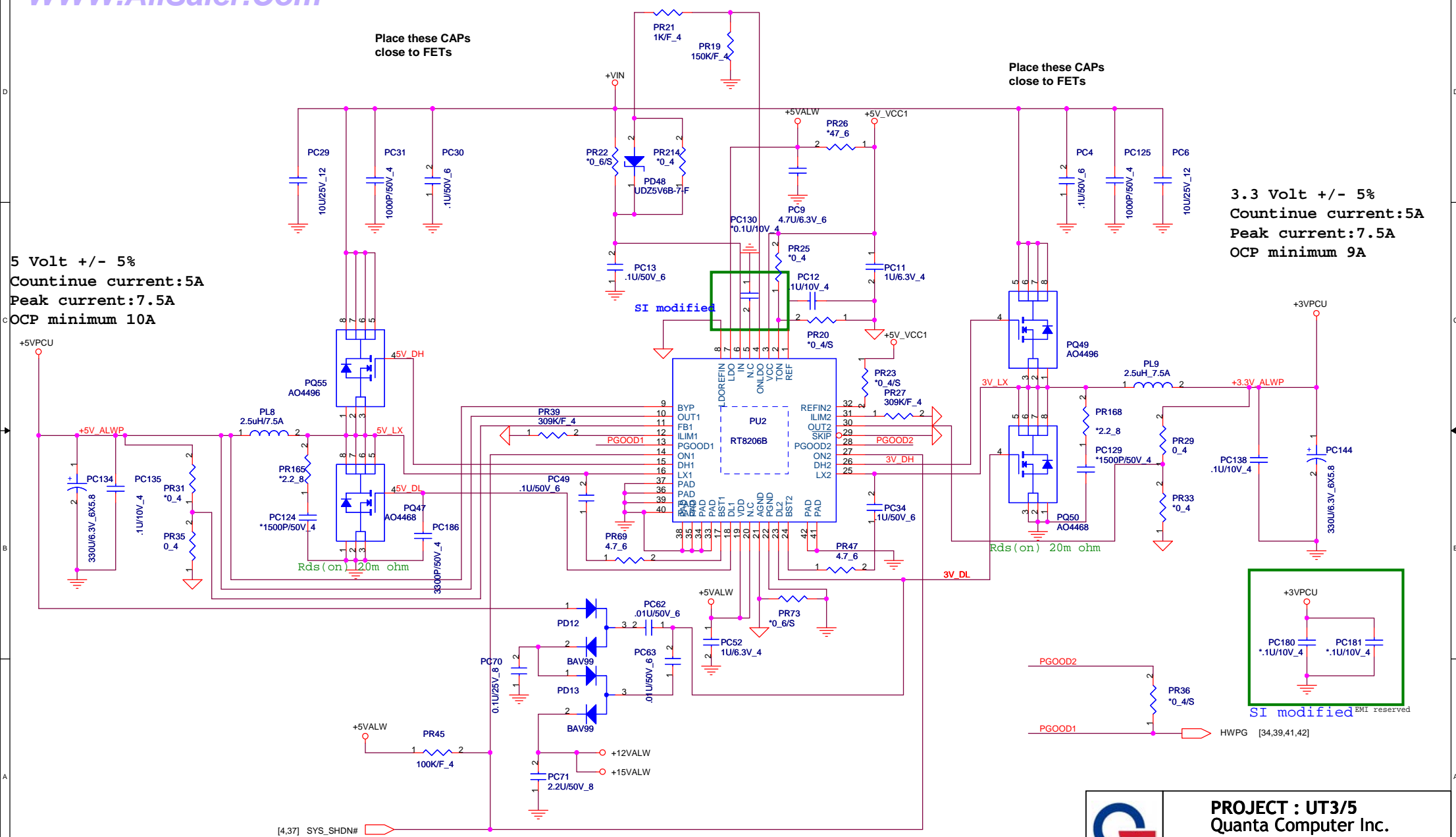
Change to Analog Gnd





5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

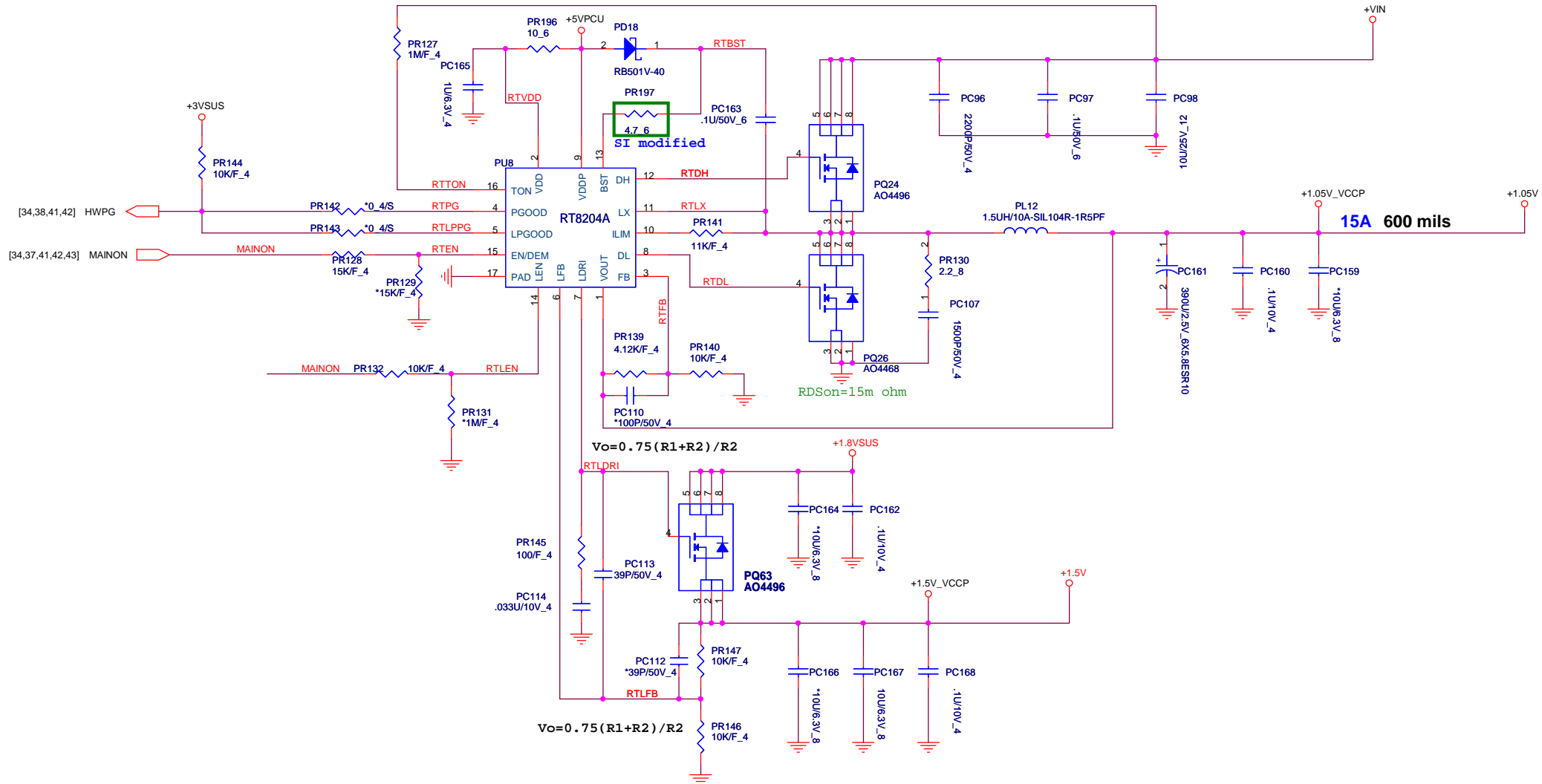
3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A




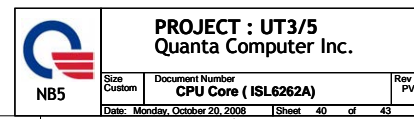
PROJECT : UT3/5
Quanta Computer Inc.

Size B	Document Number +5V/+3V (ISL6237)	Rev PV
Date: Monday, October 20, 2008 Sheet 38 of 43		

+1.05Volt +/- 5%
Countinue current:7.5A
Peak current:10A
OCP minimum 15A



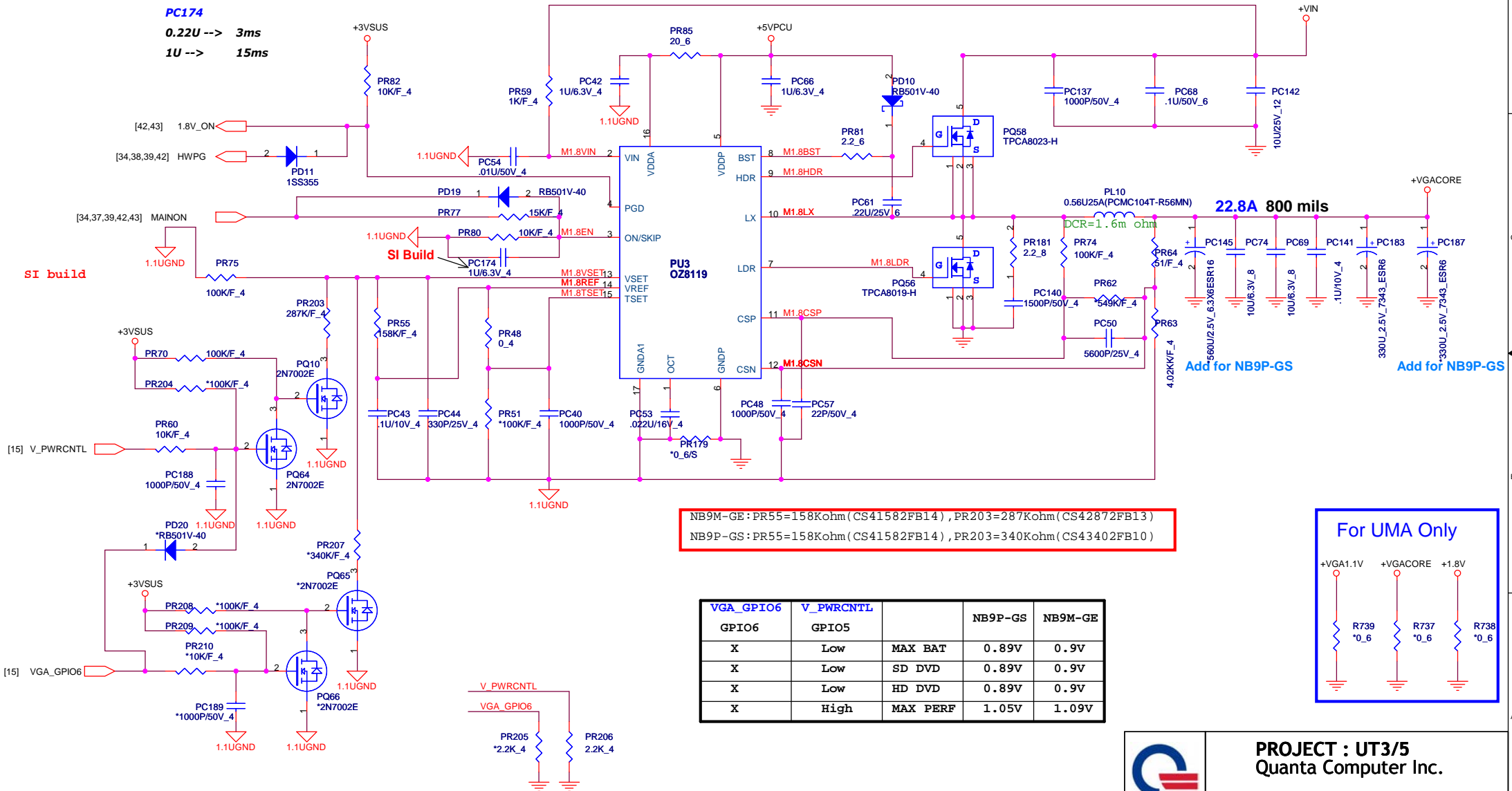
	PROJECT : UT3/5 Quanta Computer Inc.		
	Size B	Document Number +1.05V/+1.5V (RT8204)	Rev PV
Date: Monday, October 20, 2008		Sheet 39 of 43	



+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A

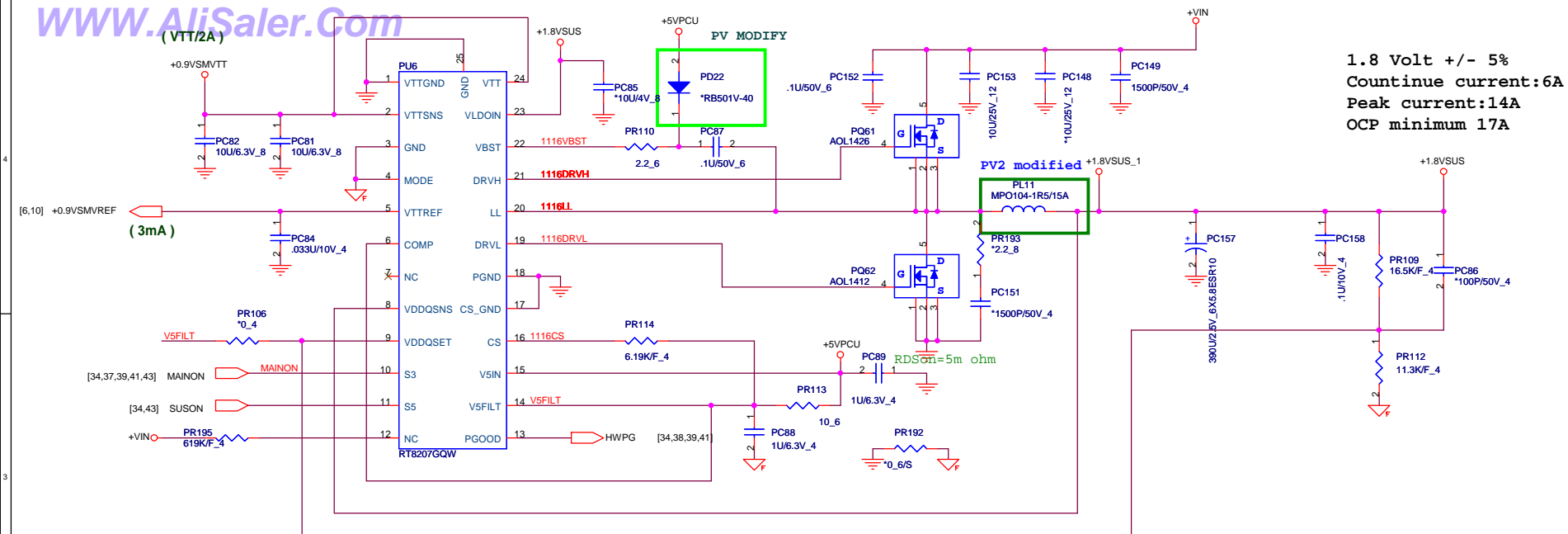
PC174

0.22U --> 3ms
1U --> 15ms



PROJECT : UT3/5
Quanta Computer Inc.

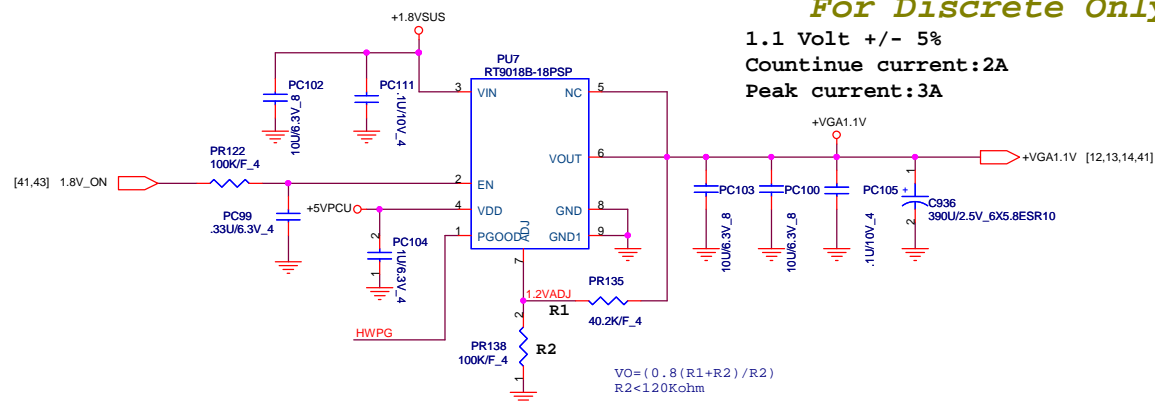
Size	Document Number	Rev
B	VGA Core OZ8119	PV
Date: Monday, October 20, 2008	Sheet 41 of 43	



Change PR122 tied to 1.8V_ON as power sequence reuquest

For Discrete Only

1.1 Volt +/- 5%
Continue current: 2A
Peak current: 3A



for G73&G8X VGA
PLL power

[43] 1.8V_OND

+1.8V_SUS

5 6 7 8

PC101
.1U/10V_4

PG33
S4634DY

(2.24A)

+1.8V

PC108
.1U/10V_4

+1.8V [13,14,17,18,41,43]

