

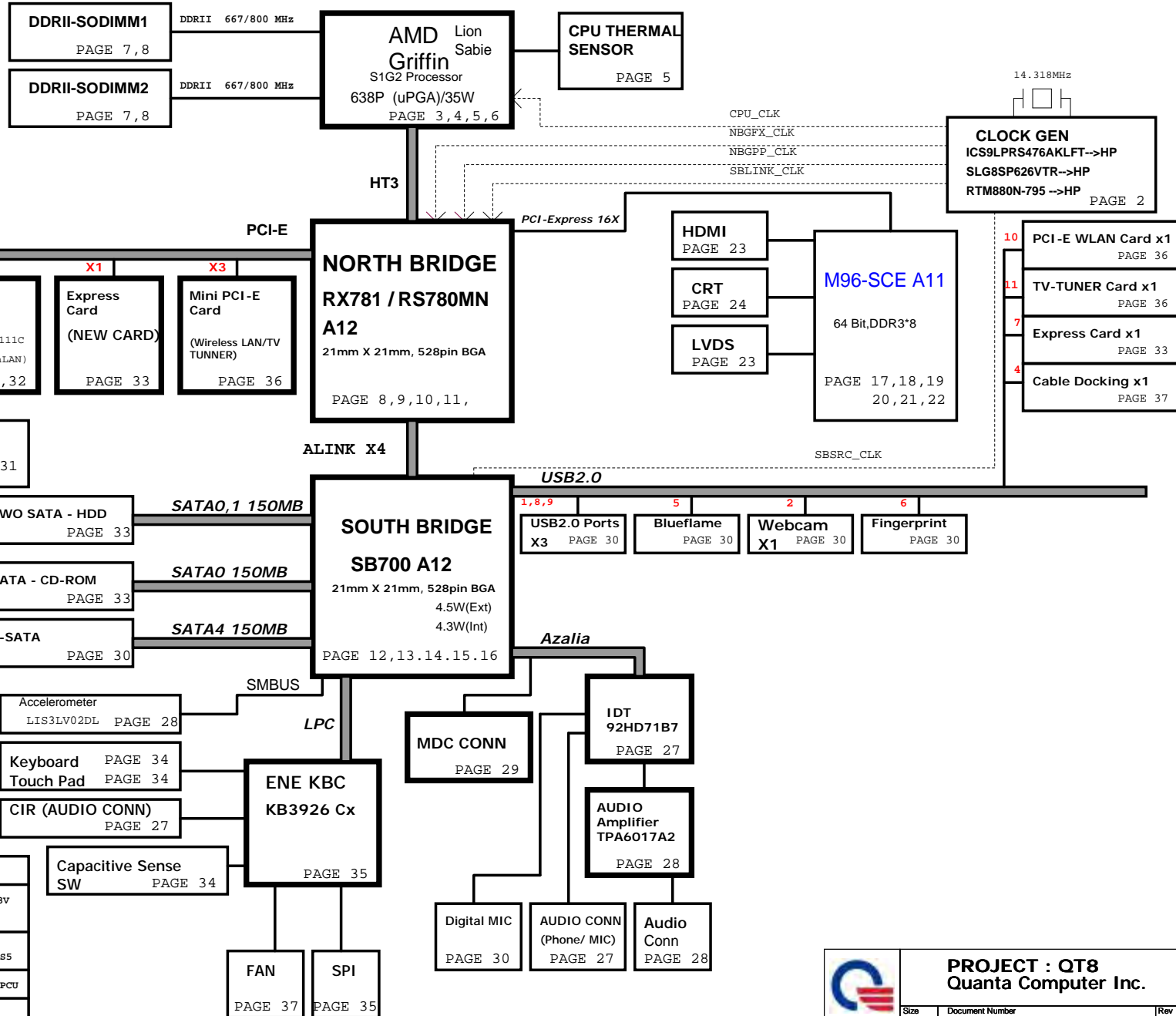
UT12 SYSTEM DIAGRAM



01

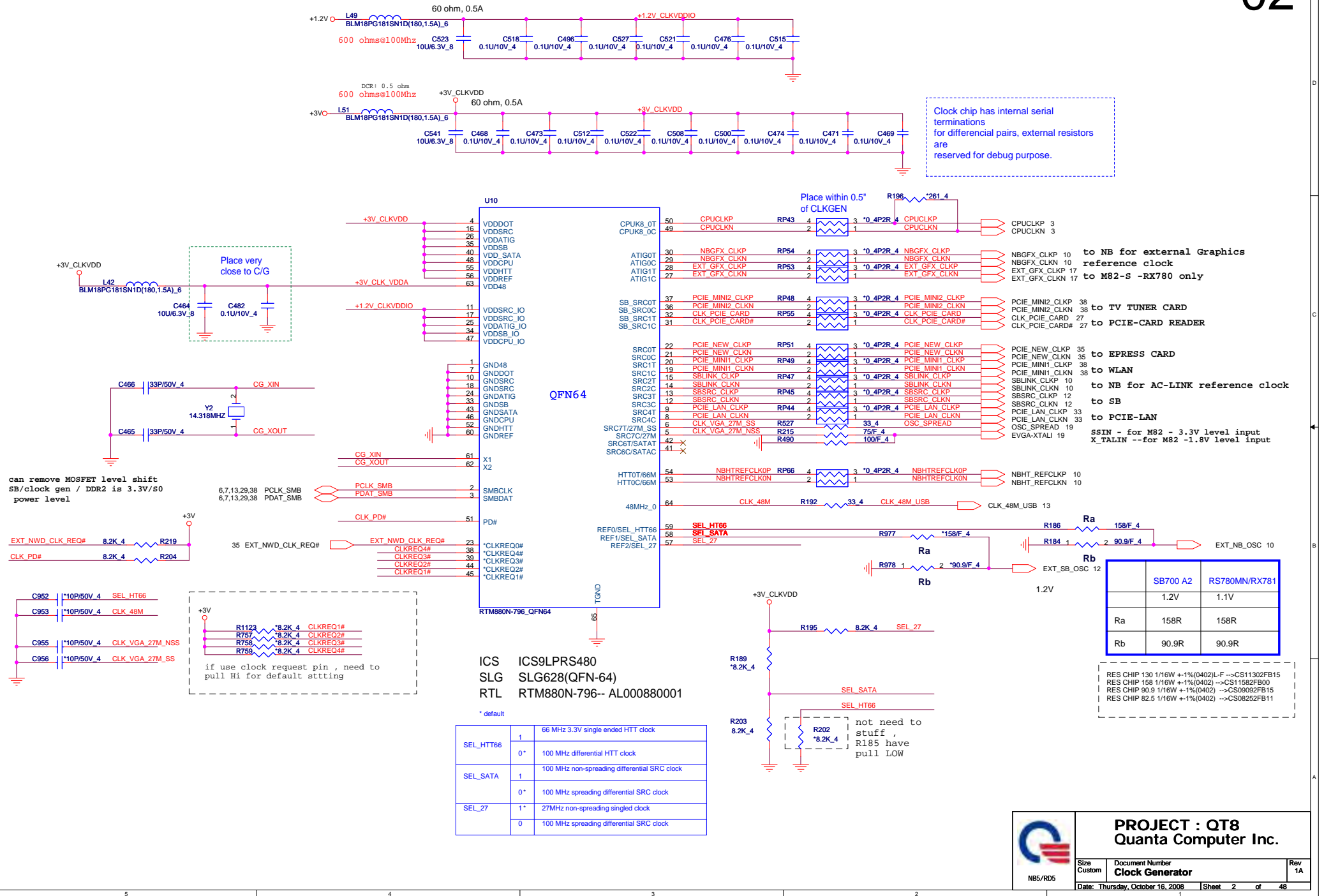
PCB STACK UP

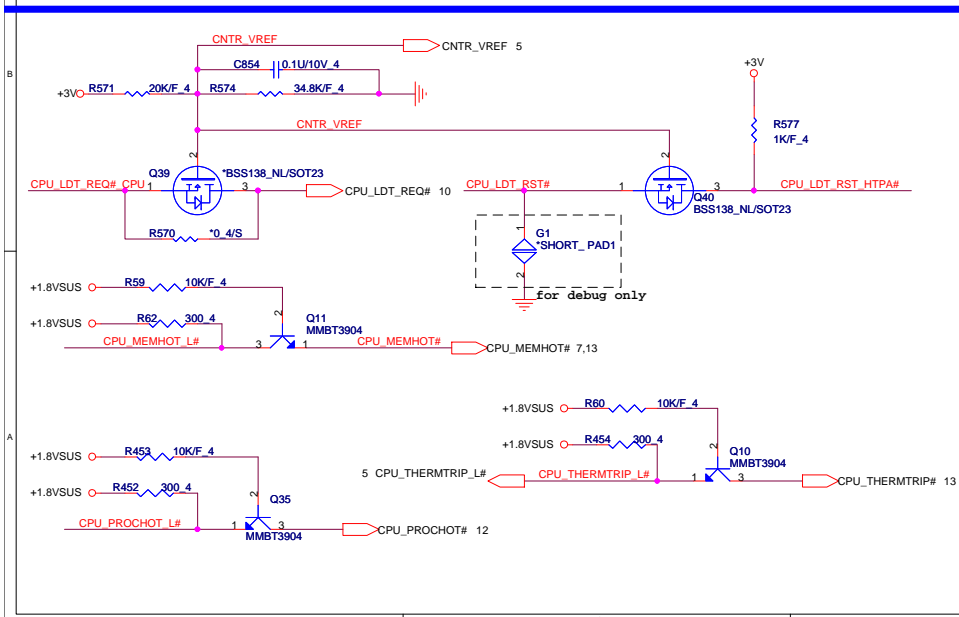
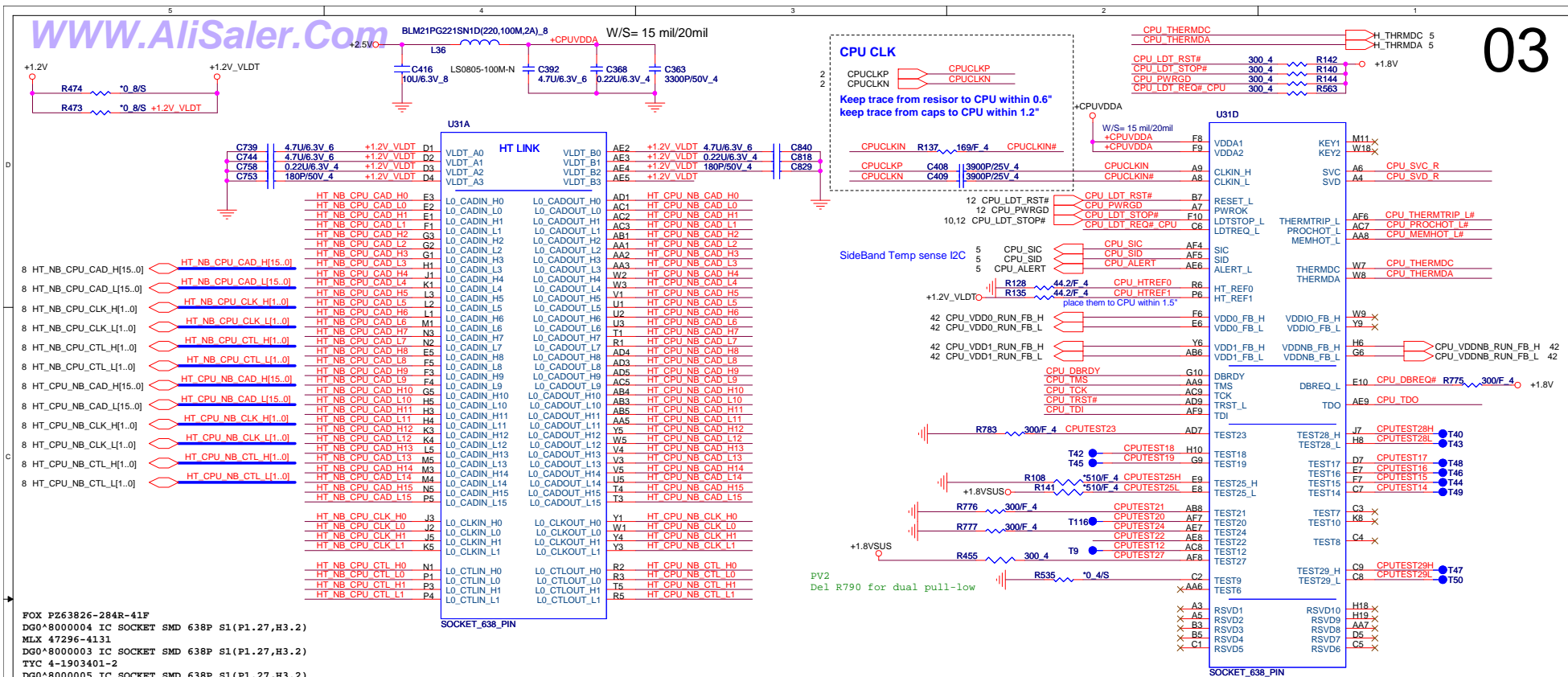
LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT



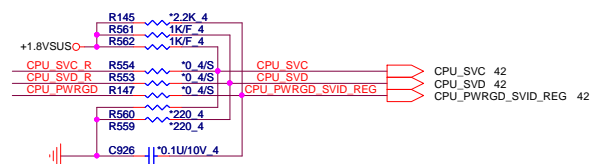
PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number
Block Diagram
Date: Thursday, October 16, 2008 Sheet 1 of 48
Rev 1A

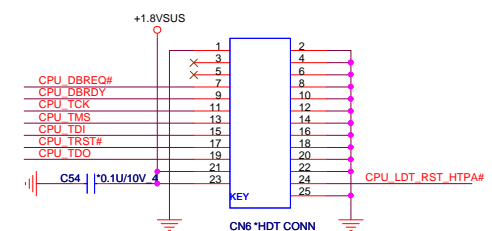




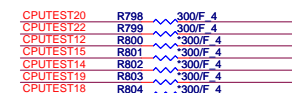
Serial VID



HDT Connector

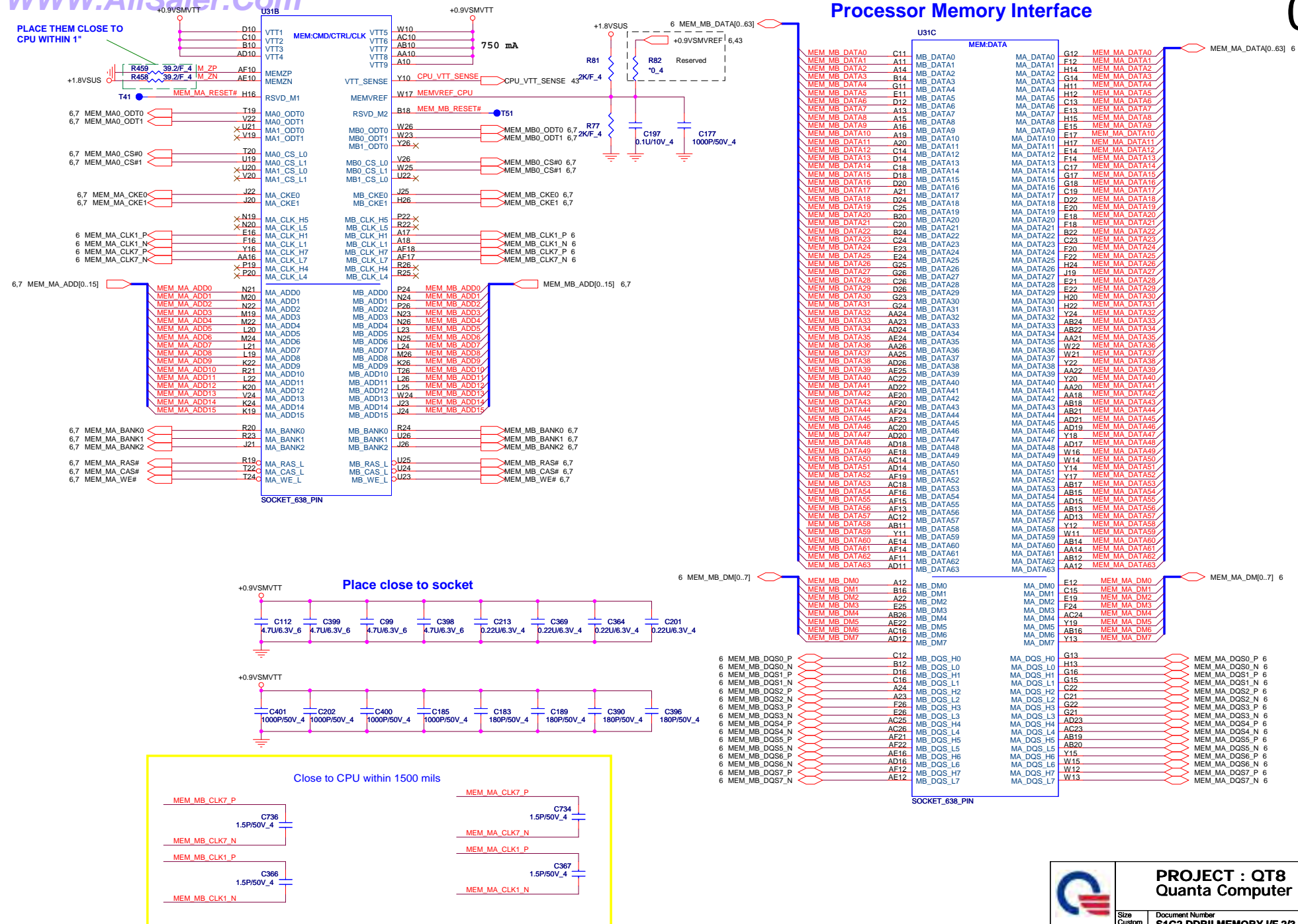
VFIX MODE VID Override Circuit

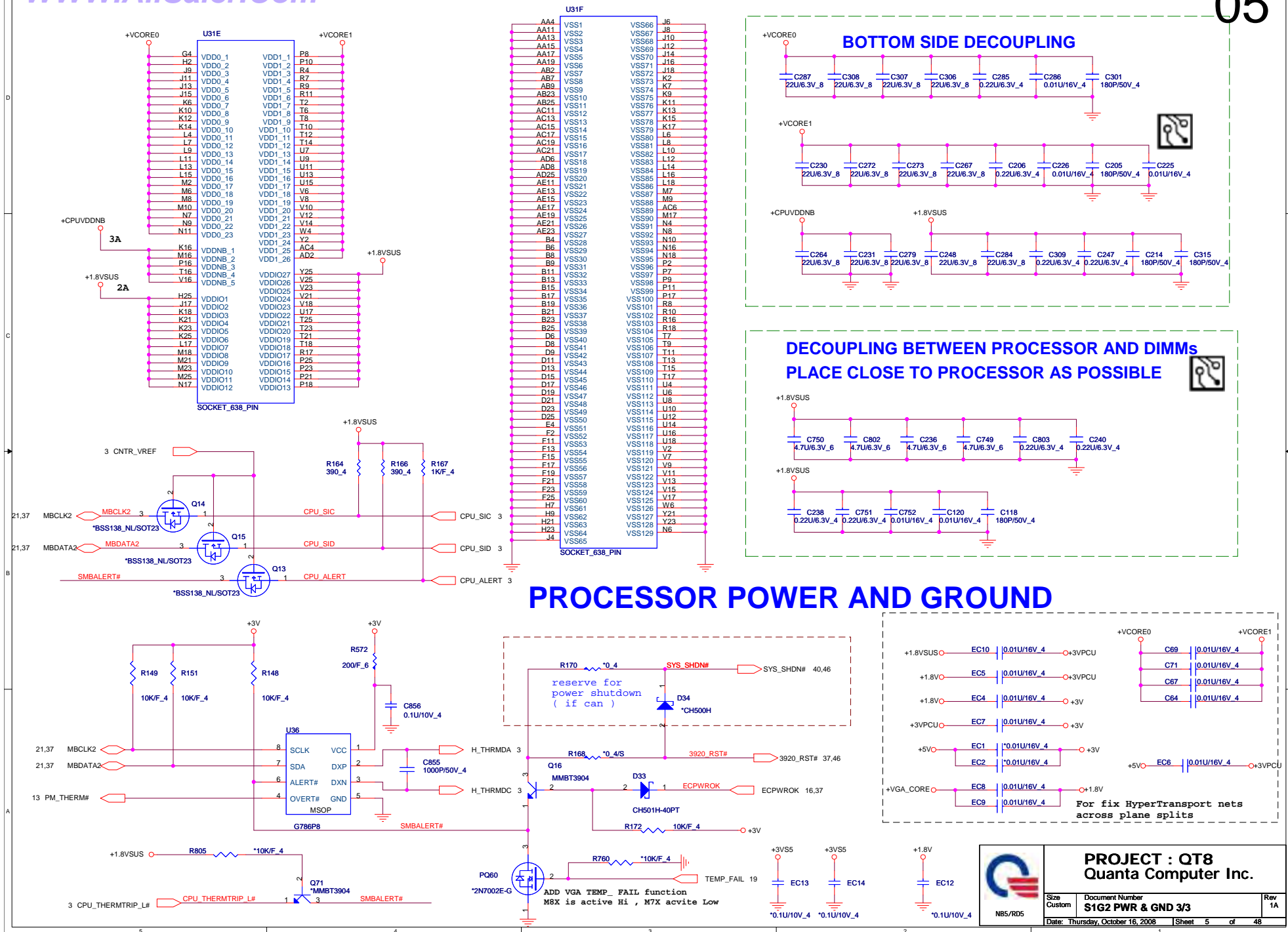
SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

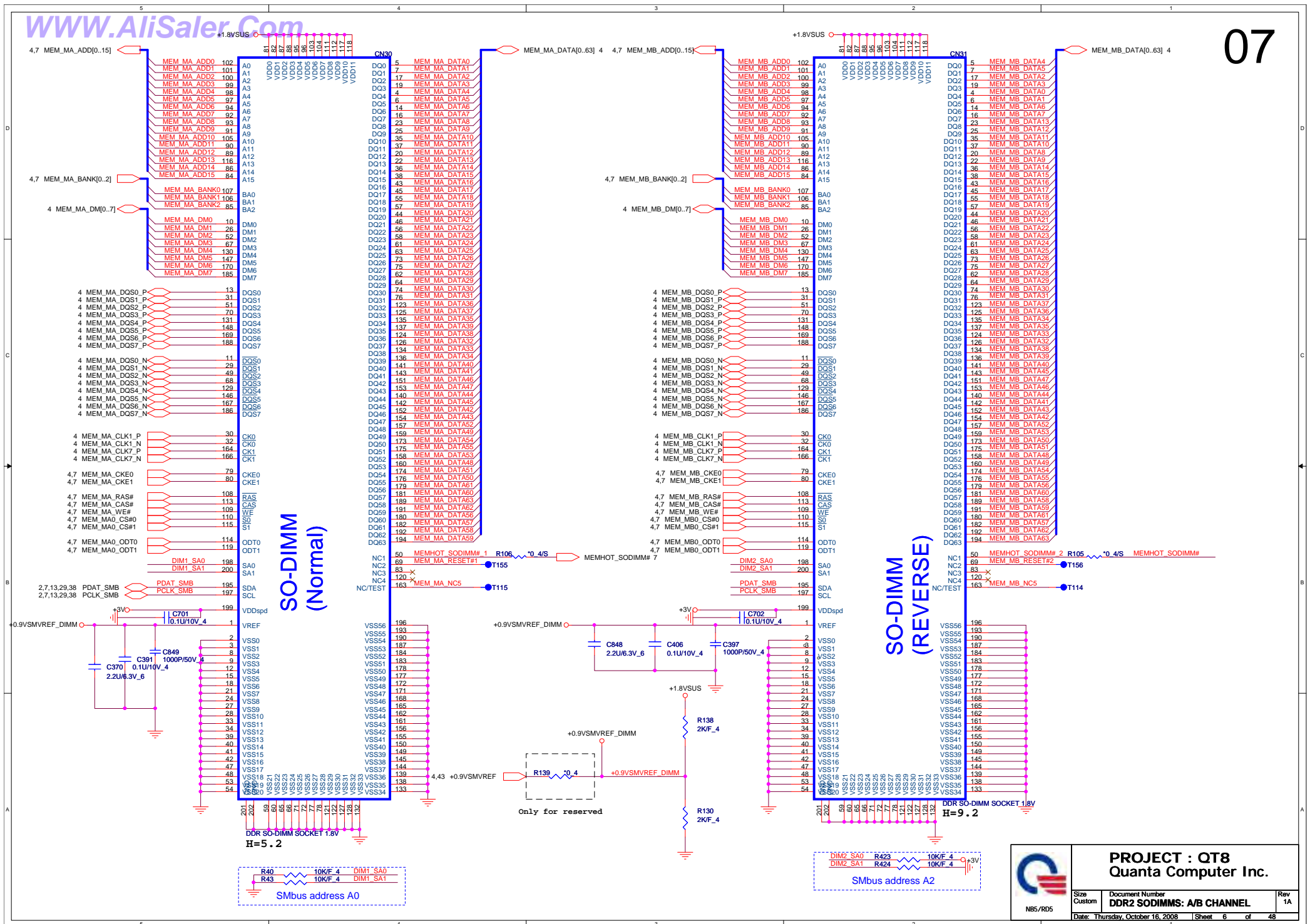


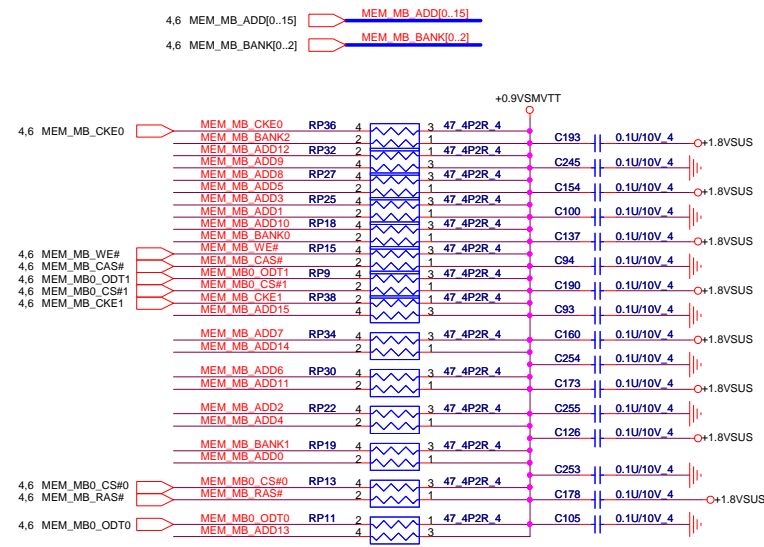
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number S1G2 HT,CTL I/F 1/3	Rev 1
Date: Thursday, October 16, 2008	Sheet 3 of 48	

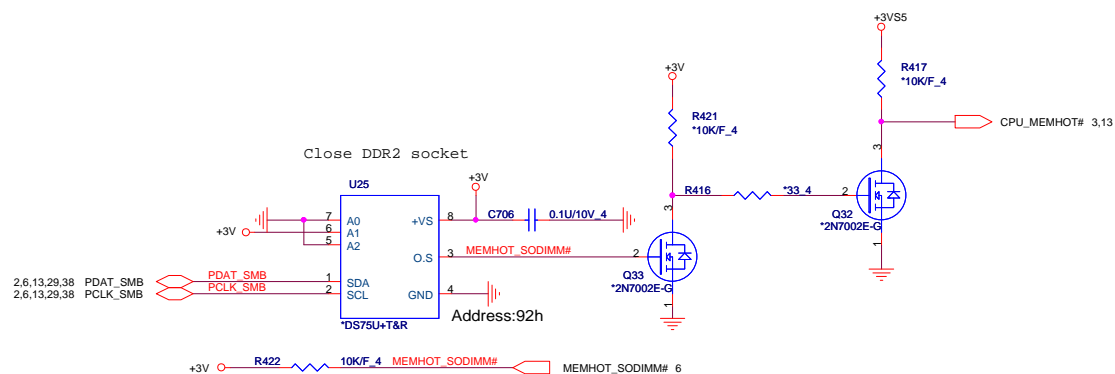
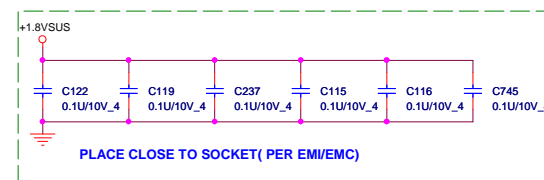


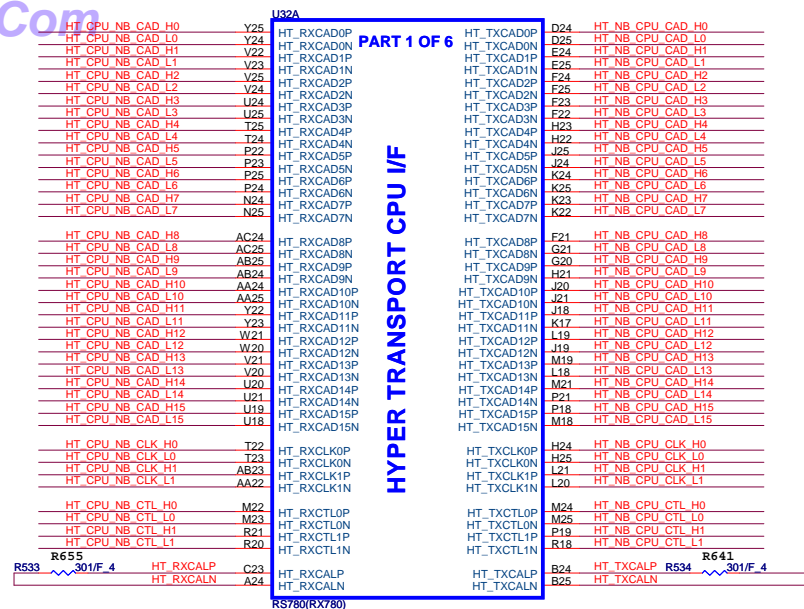






PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



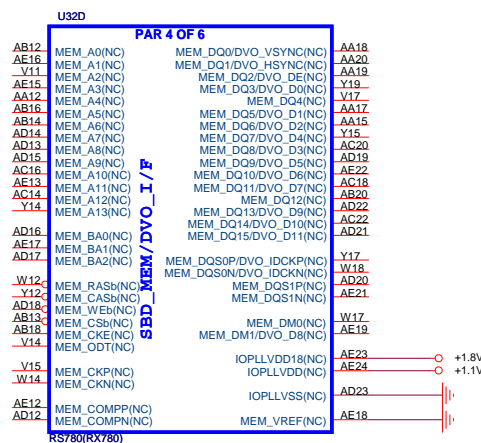


signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14

This block is for UMA RS780 only , RX780 can remove all component



IOPLLVDD18 - memory PLL
not applicable to RX780

IOPLLVD- memory PLL
not applicable to RX780

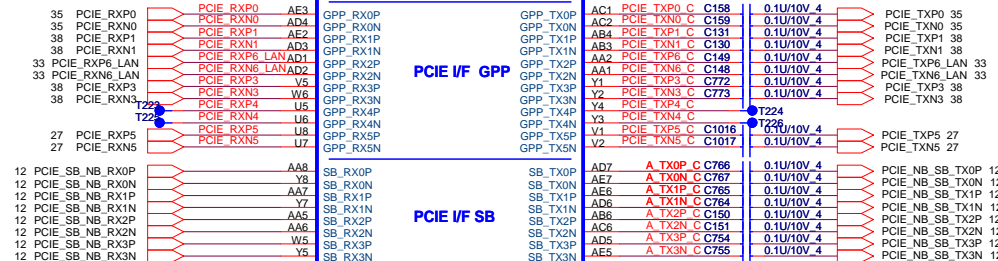
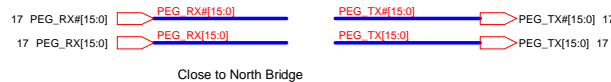
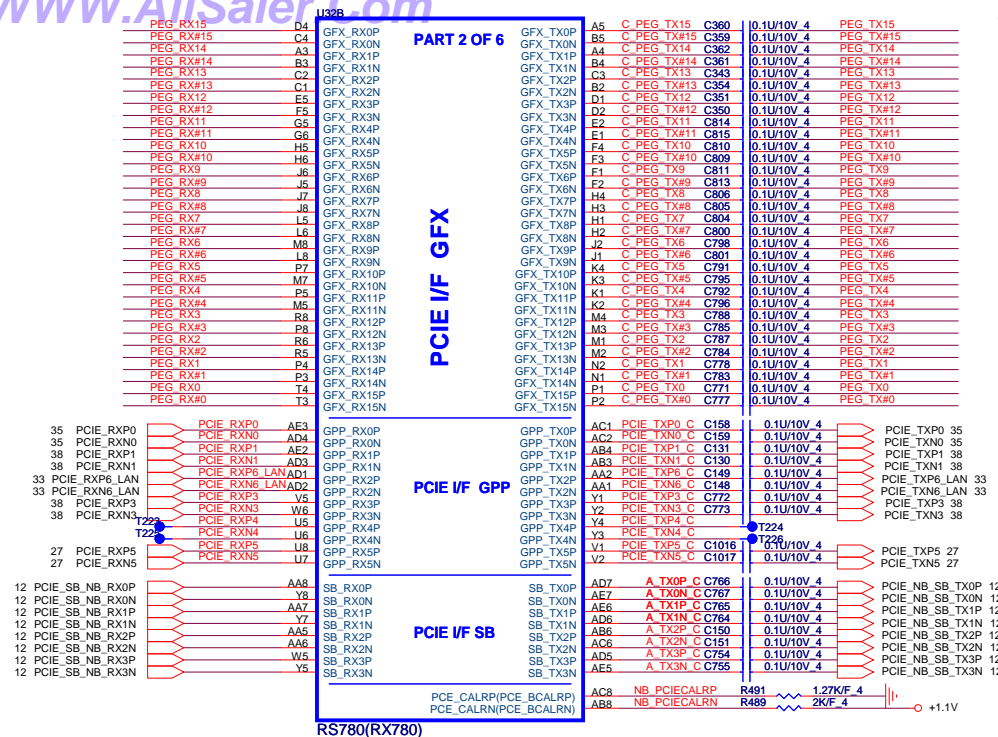


PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number RS740/RS780-HT LINK I/F 1/5
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Date: Thursday, October 16, 2008	Sheet 8 of 48
----------------------------------	---------------

Rev
1/



TO EPRESS CARD

TO WLAN

TO PCIE-LAN

TO TV TUNNER

TO PCIE CARD READER

RS780/RX780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

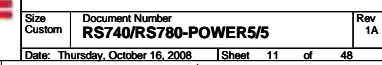
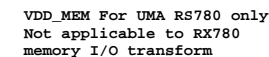


PROJECT : QT8
Quanta Computer Inc.

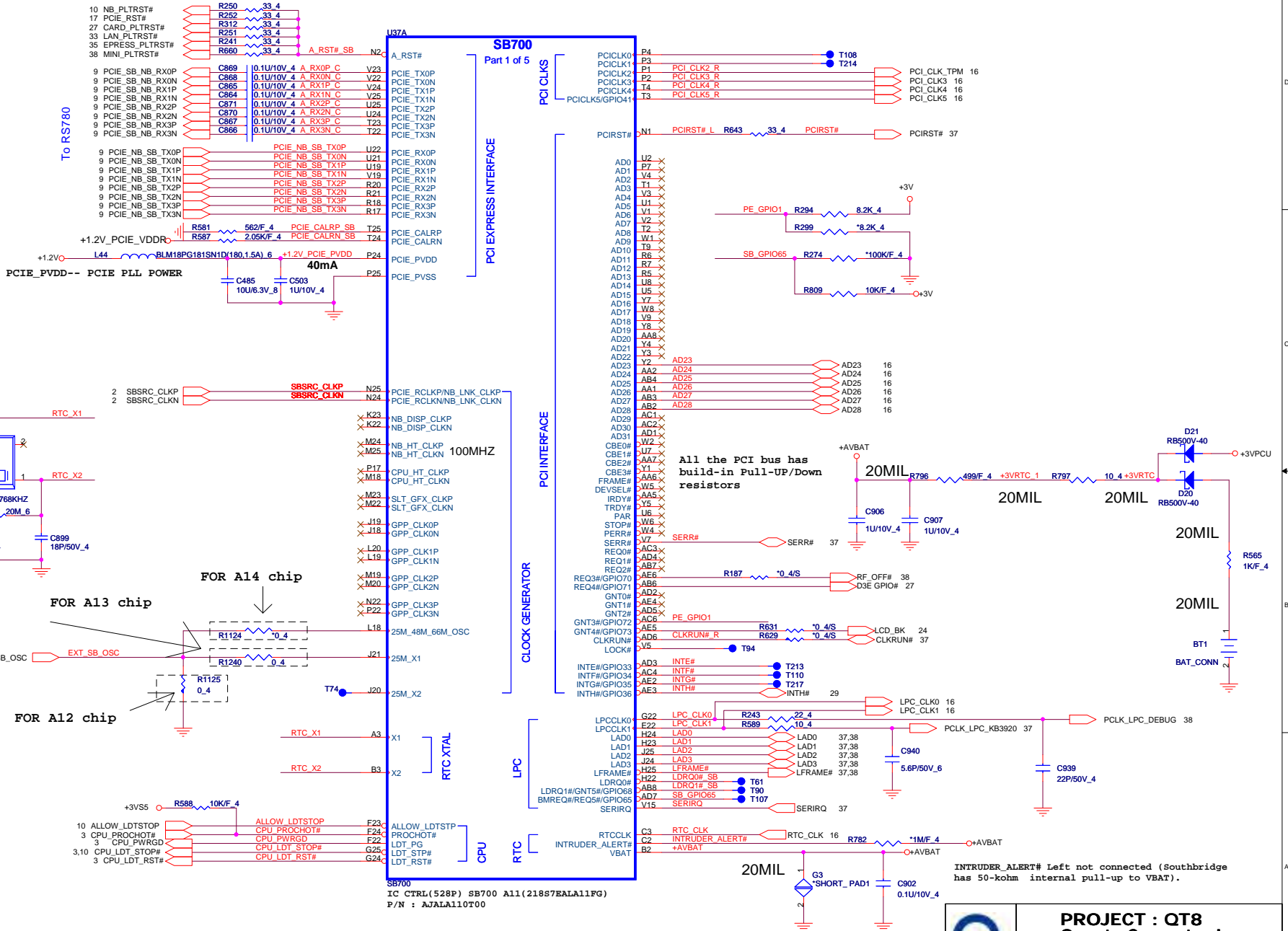
Size Custom	Document Number RS740/RS780-PCIE I/F 2/5	Rev 1A
Date: Thursday, October 16, 2008	Sheet 9 of 48	



PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL18	NC	NC



PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600



PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number SB700-PCIE/CPU/LPC/1/4 Rev 1A
Date: Thursday, October 16, 2008 Sheet 12 of 48



SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB600

SATA1

SATA ODD

E-SATA

SATA HDD2

SATA PORT 4,5
are only
support IDE
mode



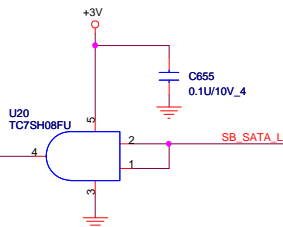
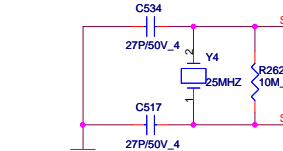
PLACE SATA CAL
RES VERY CLOSE
TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

PLVDD_SATA--
SATA PLL
POWER

+3V R382 10K/F 4
+1.2V_PLLVDD_SATA
+3V_XTLVDD_SATA

XTLVDD_SATA-- SATA
crystal power



U37B

SB700
Part 2 of 5

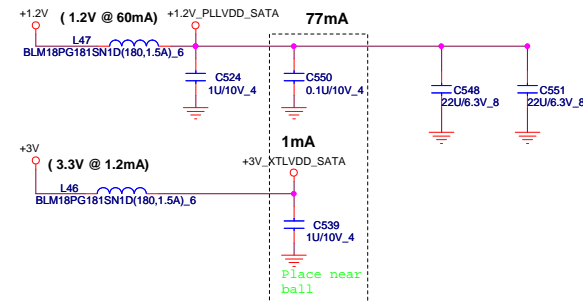
SERIAL ATA

SATA PWR

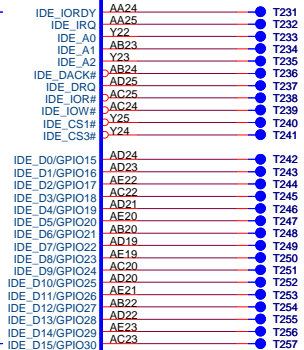
HW MONITOR

+1.2V (1.2V @ 60mA) +1.2V_PLLVDD_SATA

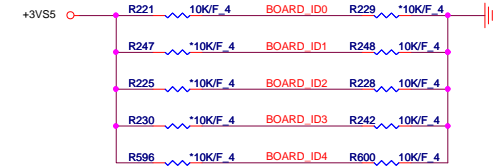
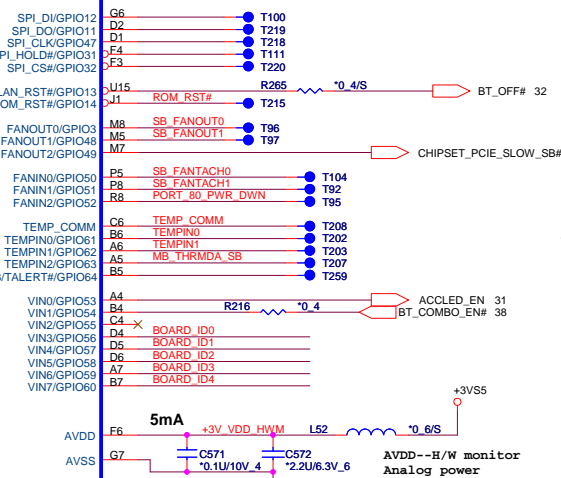
77mA



Place near ball



IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

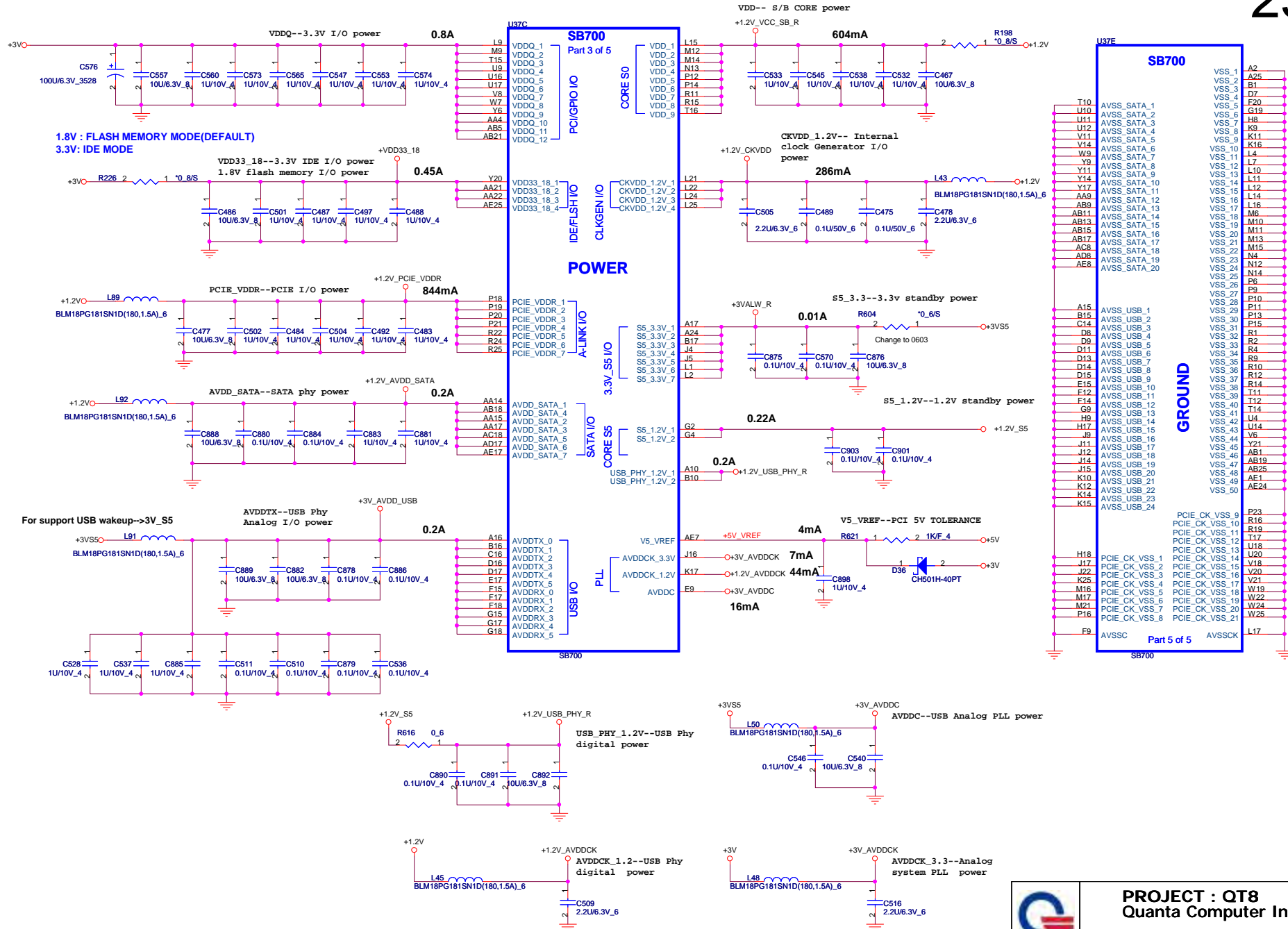


ID4 GP60	ID3 GP59	ID2 GP58	ID1 GP57	
0	0	0	0	UT1 UMA
0	0	0	1	UT2 UMA
0	0	1	0	UT1 M92
0	0	1	1	UT2 M92
0	1	0	0	UT1 M96
0	1	0	1	UT2 M96



PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number SB700-ACPI/GPIO/USB 2/4 Rev 1A
Date: Thursday, October 16, 2008 Sheet 14 of 48

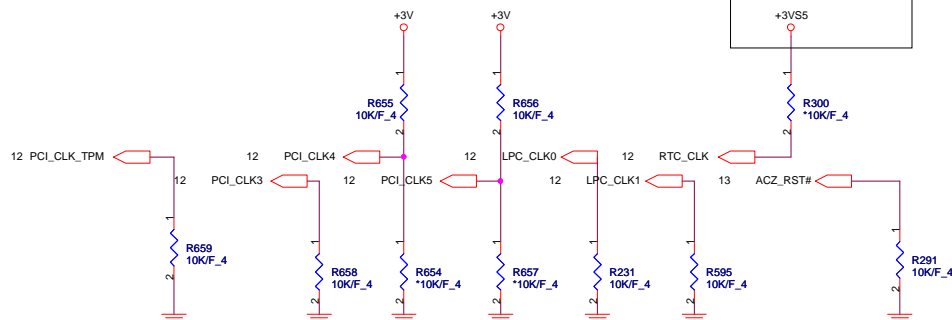




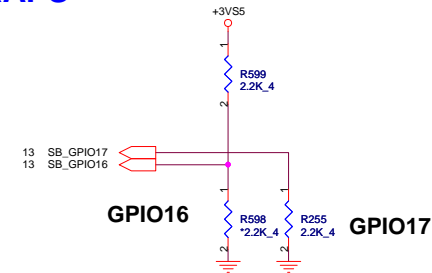
OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

It must ready
before RSMRST#

REQUIRED STRAPS



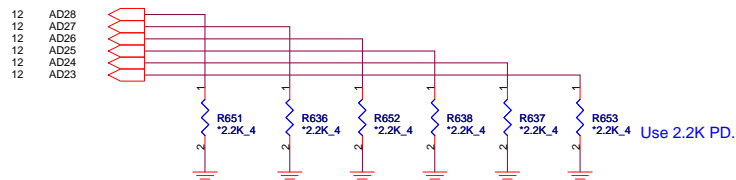
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

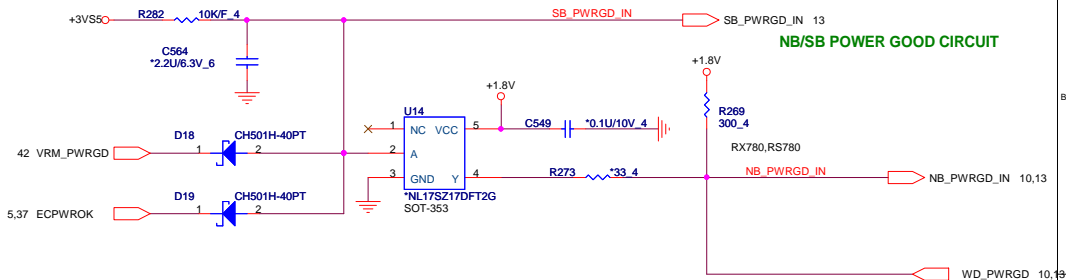
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

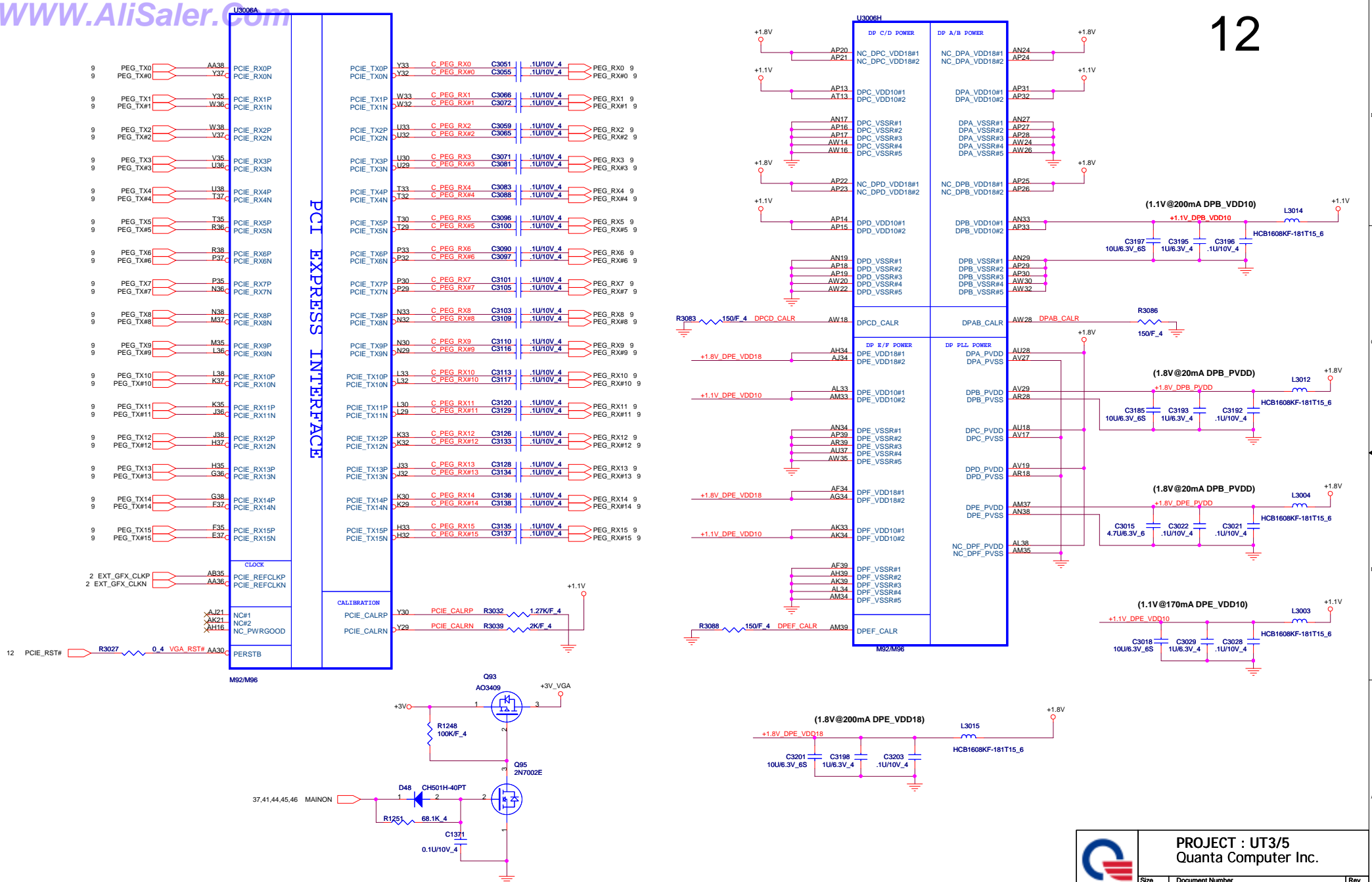


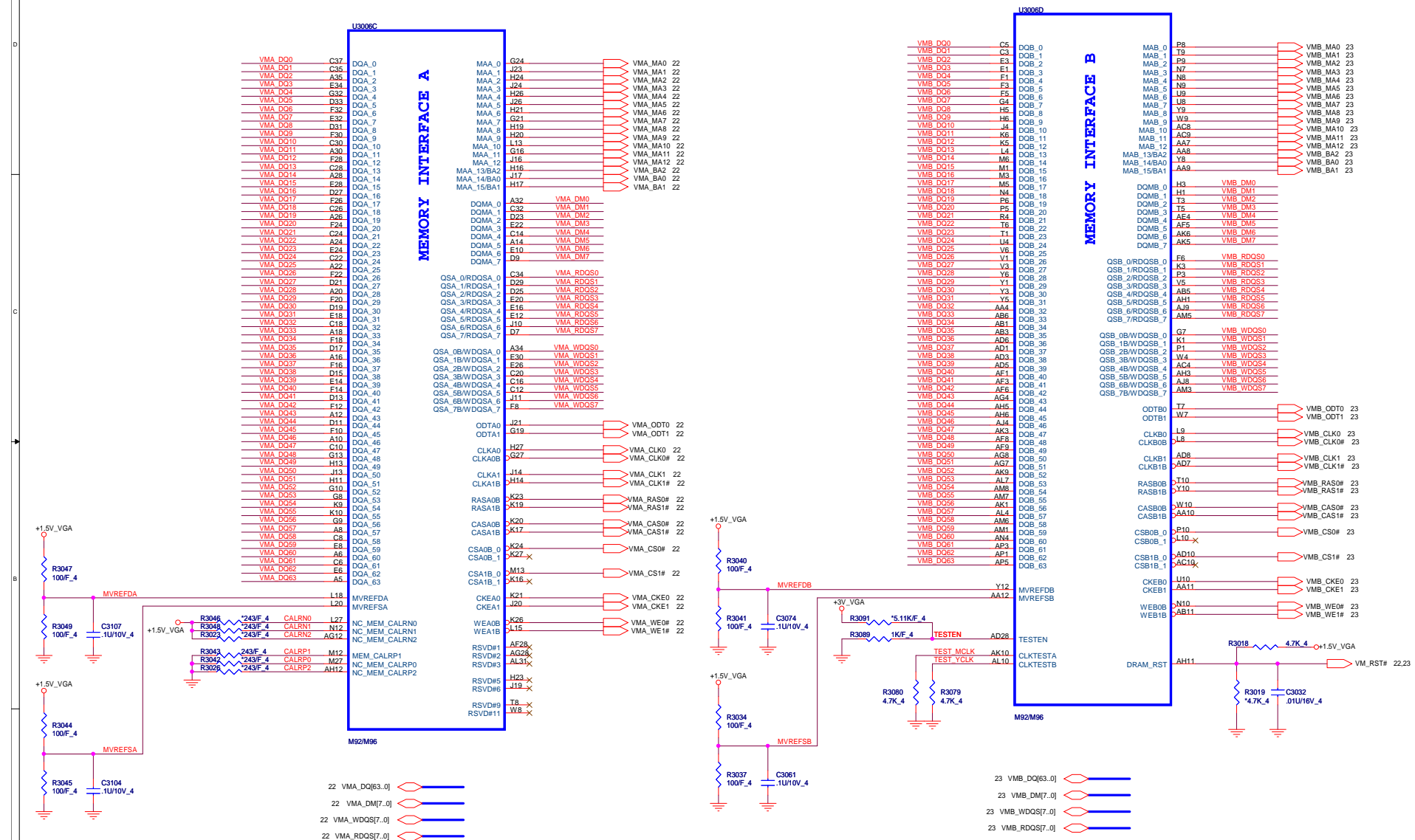
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

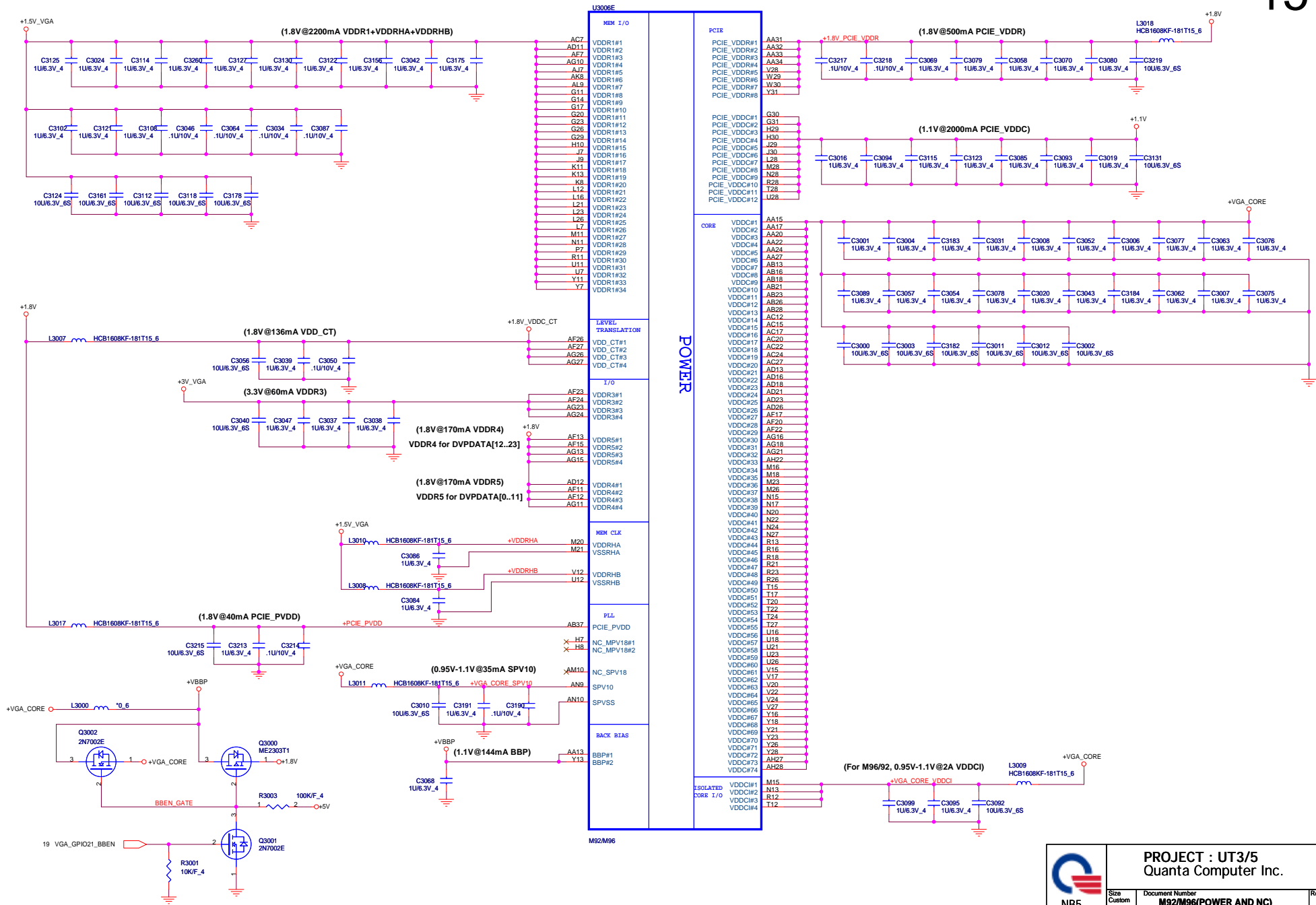


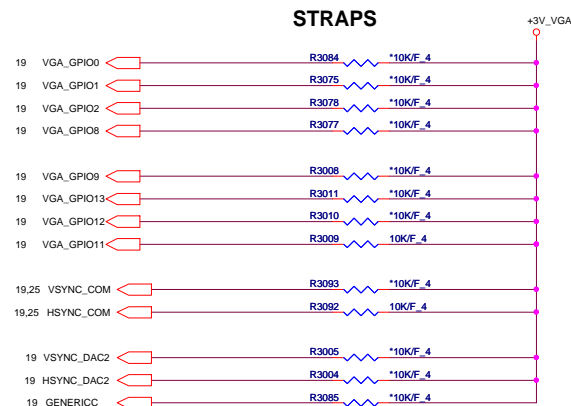
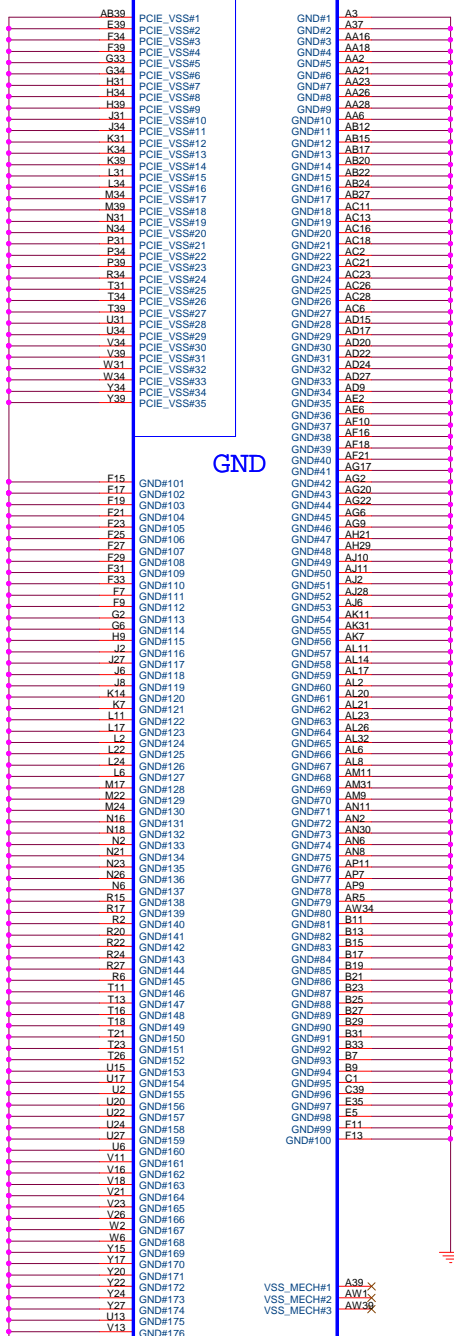
PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	1A
Date: Thursday, October 16, 2008 Sheet 16 of 48		

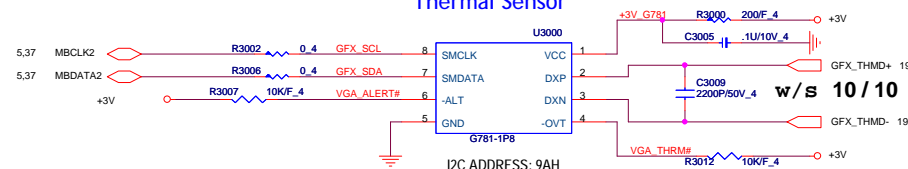
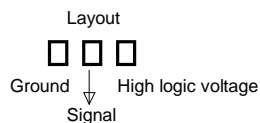








Overlap pads to save space and to prevent assembly of both resistors.

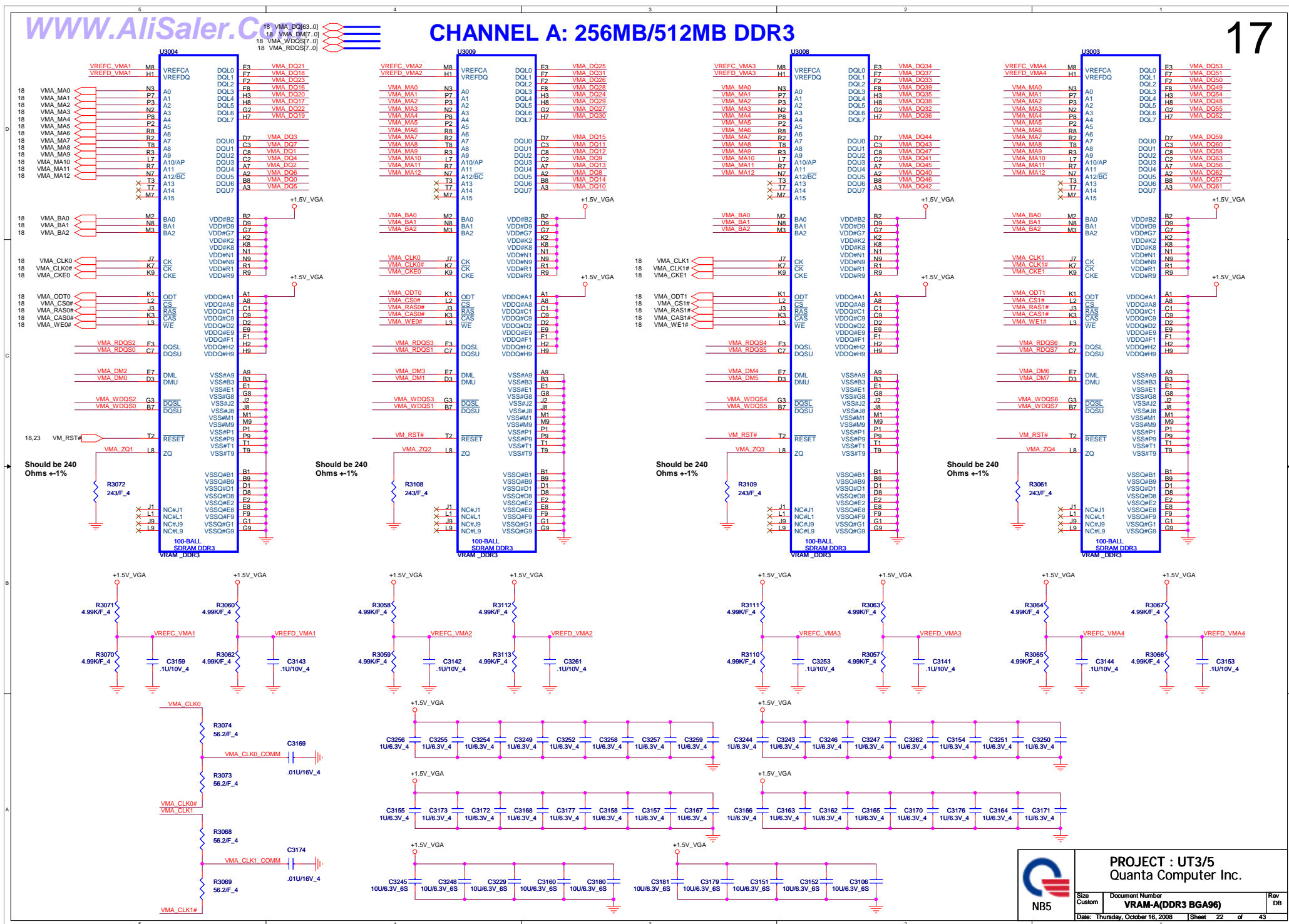


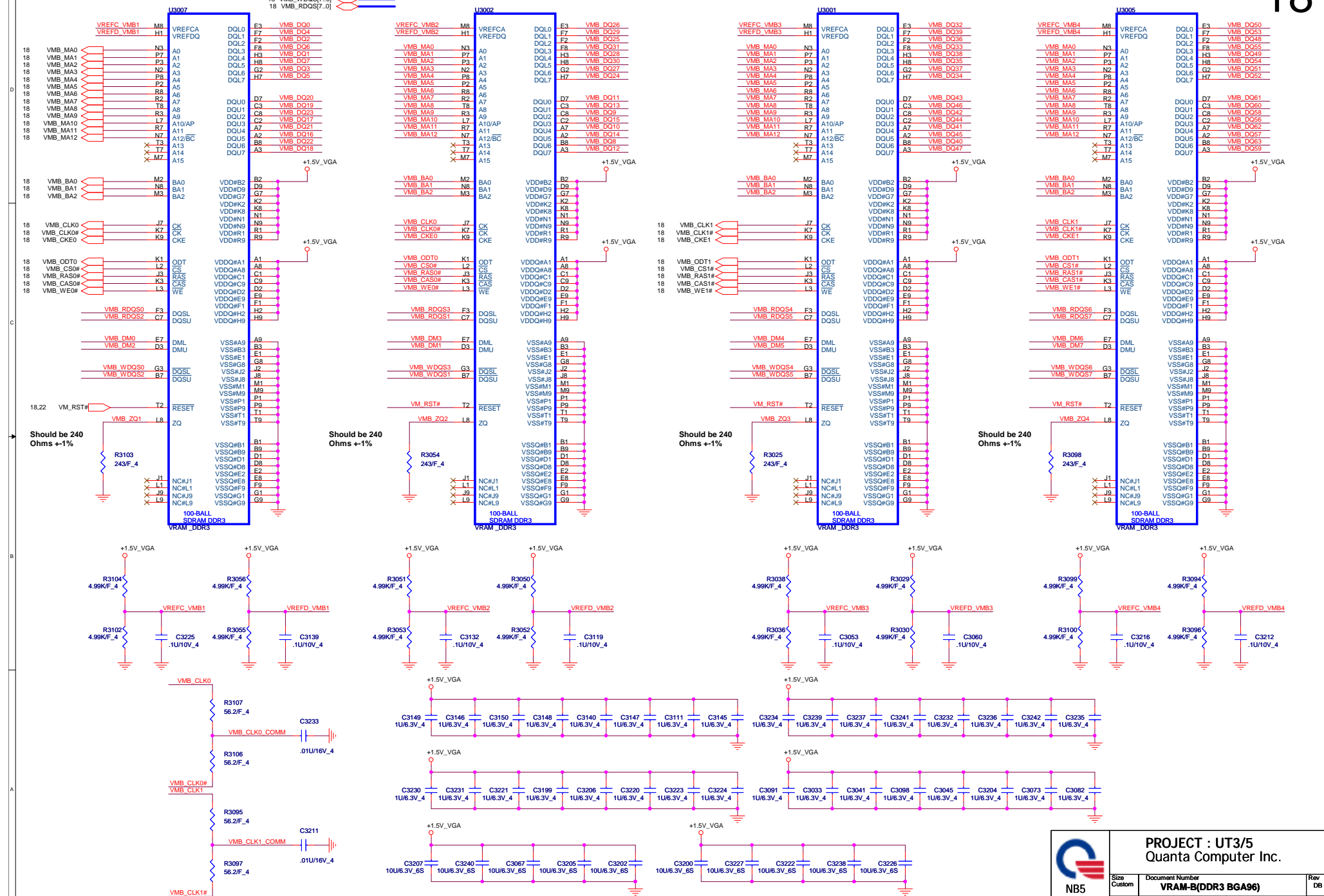
Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
BIF_GEN2_EN	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
STRAP_BIF_CLK_PM_EN	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	GPIO9 GPIO13 GPIO12 GPIO11	GPIO9,13,12,11 (config 3,2,1,0): a= #BIOS_ROM_EN = 1, then Config[3,0] defines the ROM Type: b> #BIOS_ROM_EN = 0, then Config[3,0] defines the Aperture size:Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0:No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VIP_DEVICE_STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e., its value during reset is unimportant), and it can be used as a regular GPIO	0
SMS_EN_HARD	H2SYNC		0
CCBPASS	GENERICC		0

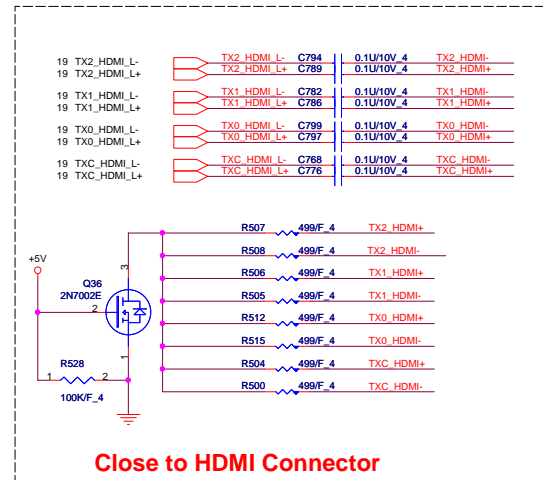


PROJECT : UT3/5
Quanta Computer Inc.

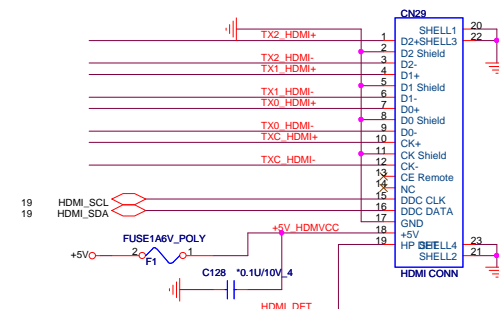
Size Custom	Document Number M92/M96 (GND/Straps/Therm)
Date: Thursday, October 16, 2008	Sheet 21 of 43





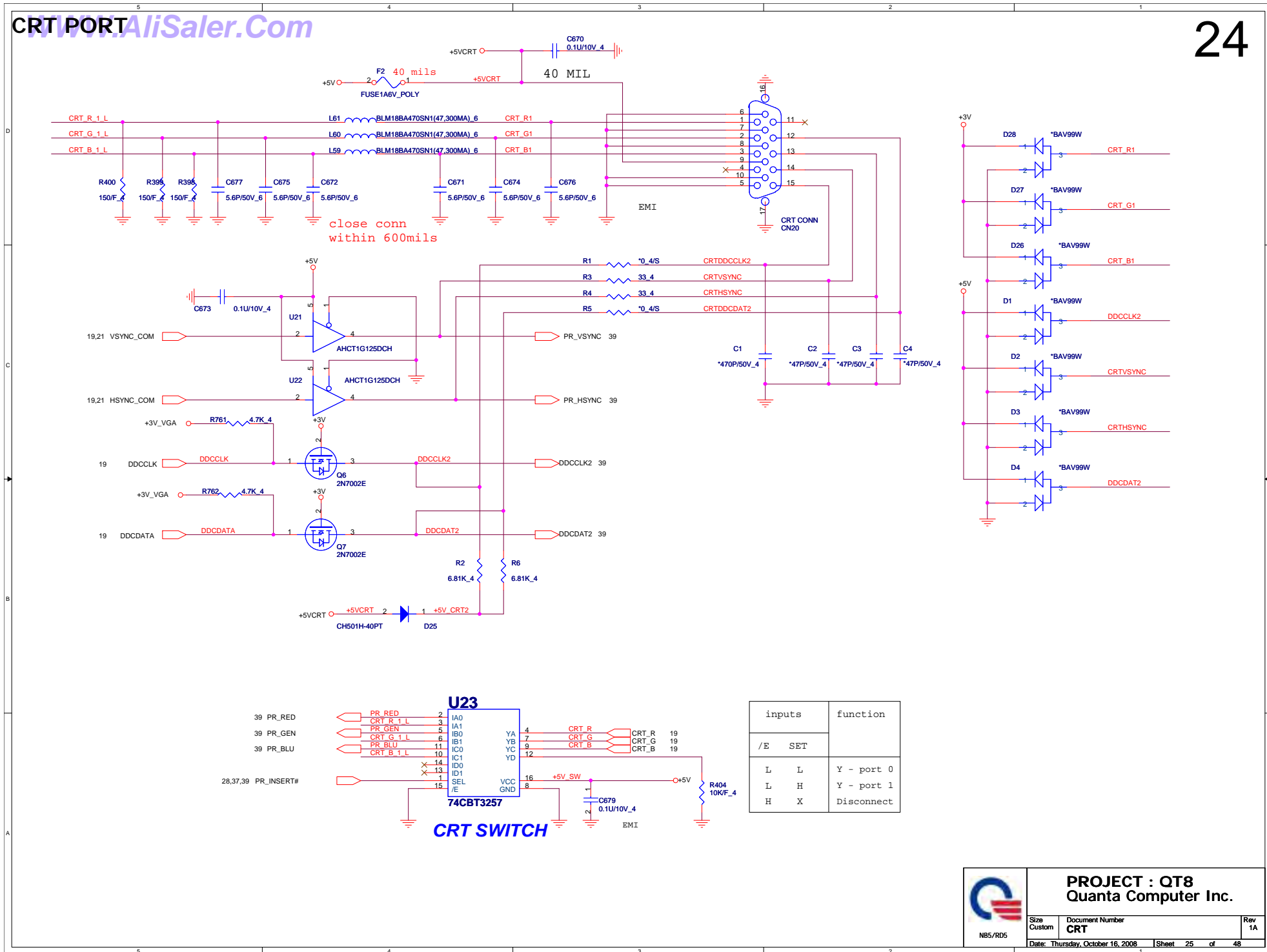


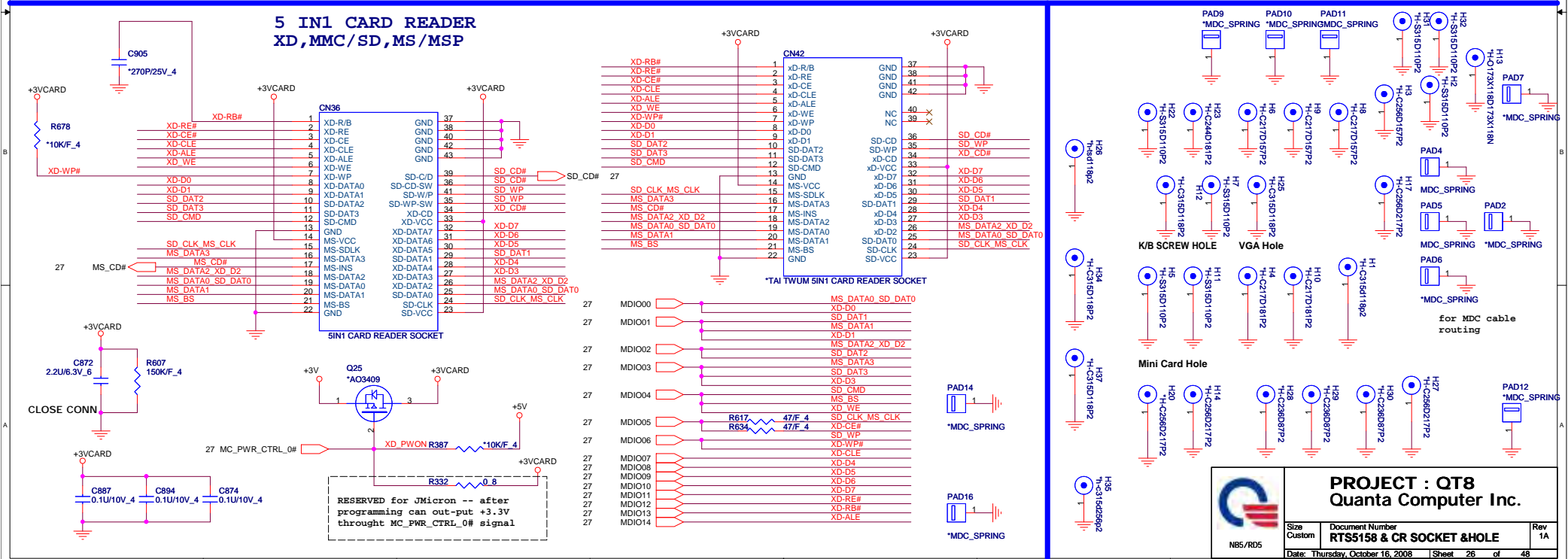
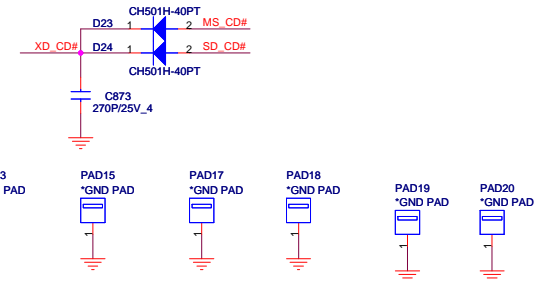
HDMI PORT

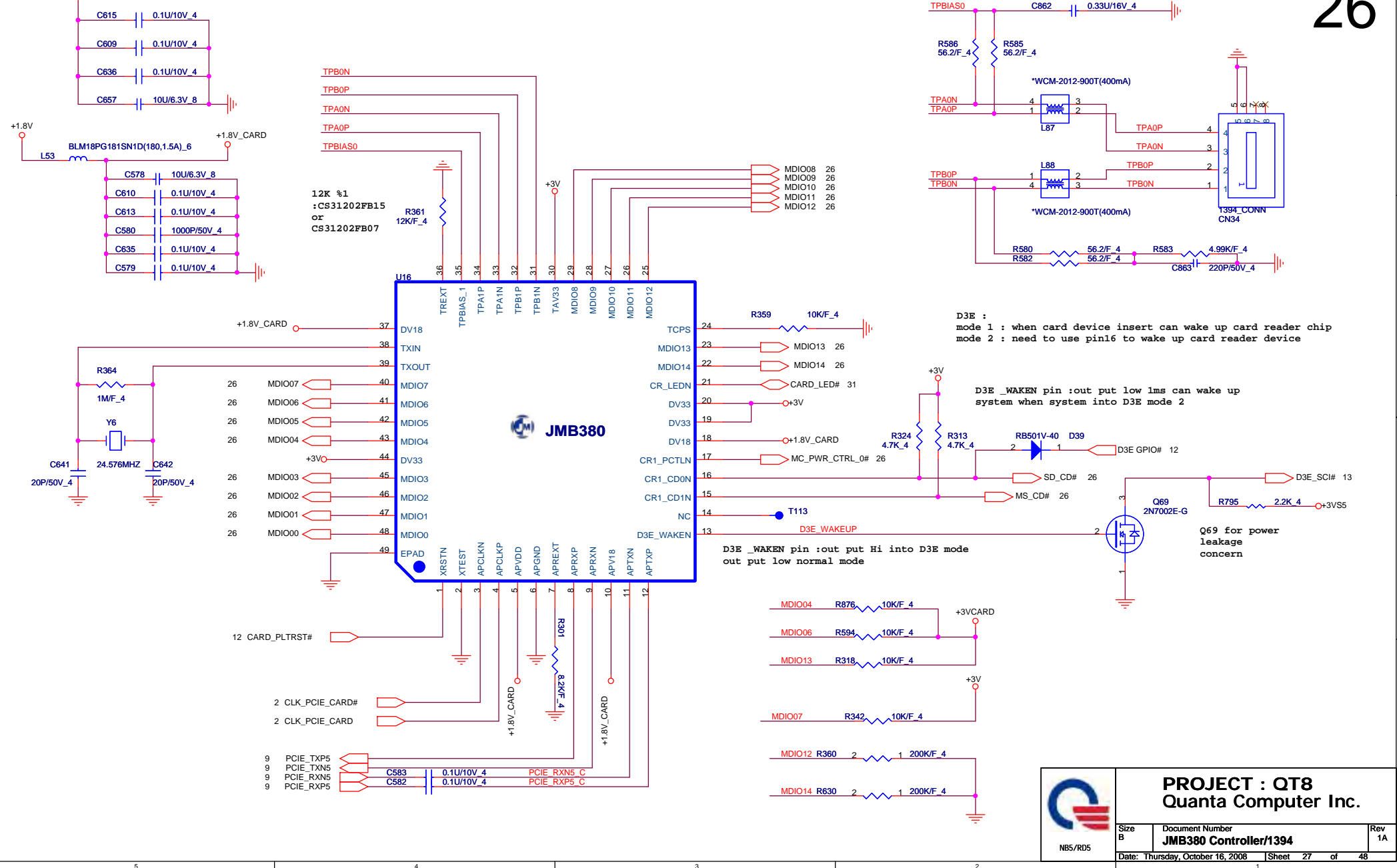


NBS/RD5

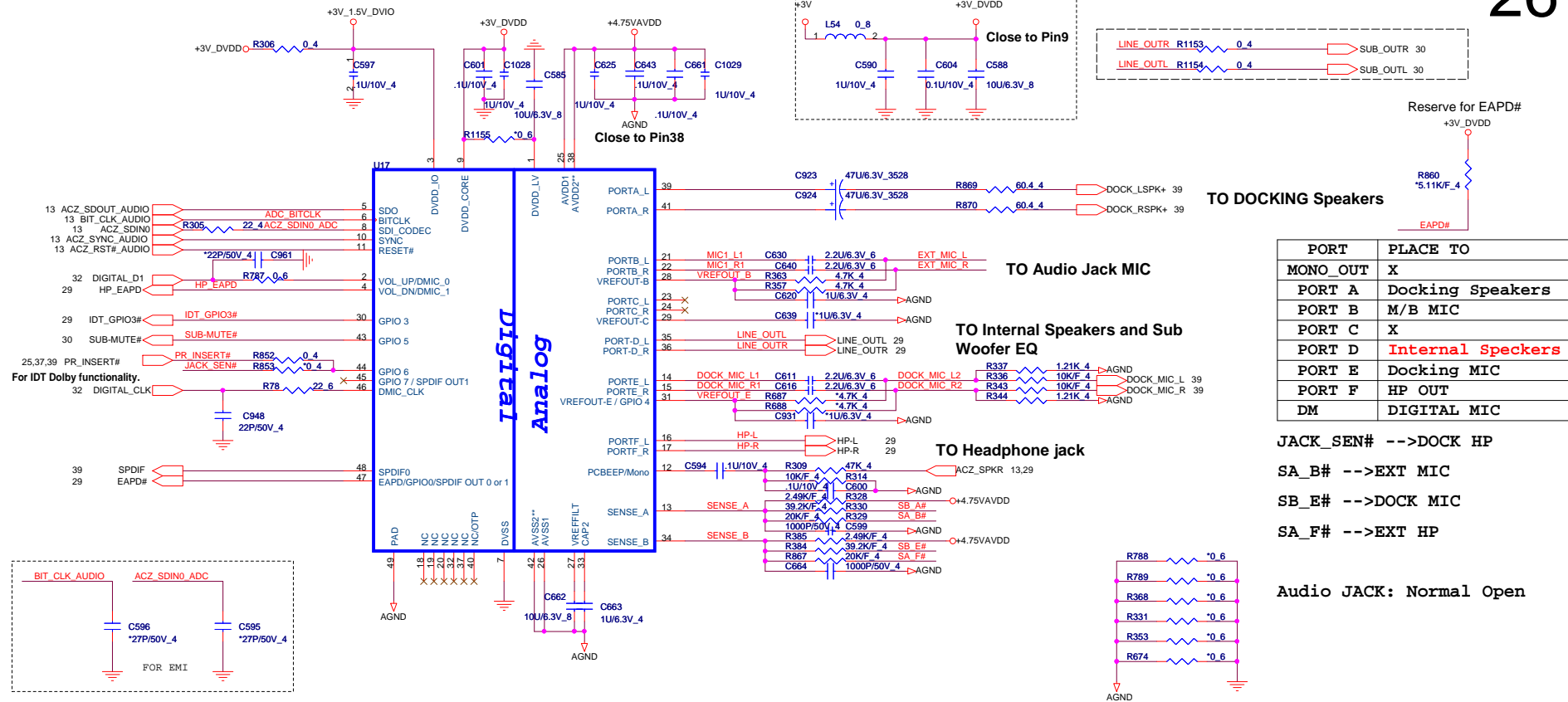
Size Custom	Document Number LCD CONN,HDMI CONN
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PROJECT : QT8 Quanta Computer Inc.		
Size B NB5/RD5	Document Number JMB380 Controller/1394	Rev 1A
Date: Thursday, October 16, 2008 Sheet 27 of 48		



PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

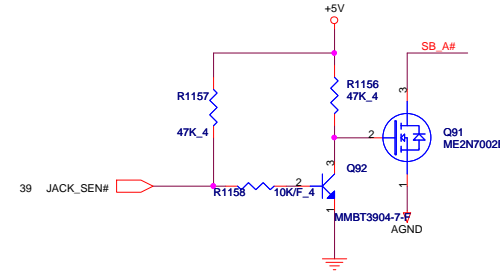
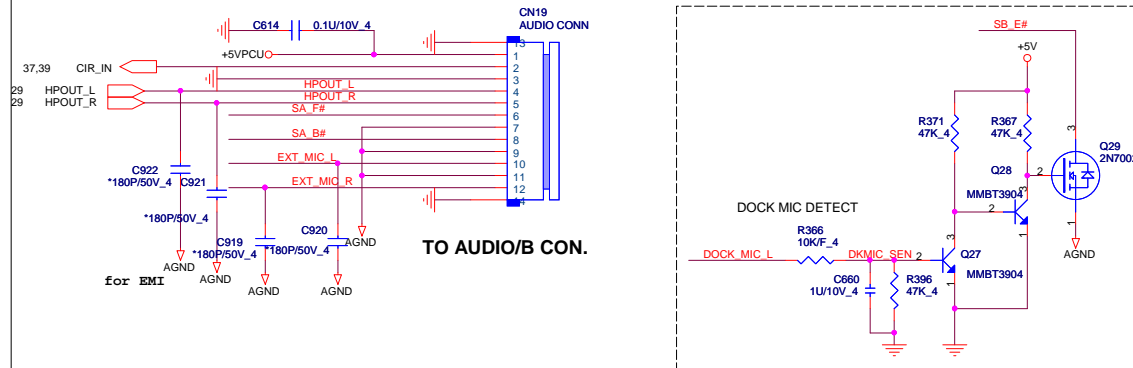
JACK_SEN# -->DOCK HP

SA_B# -->EXT MIC

SB_E# -->DOCK MIC

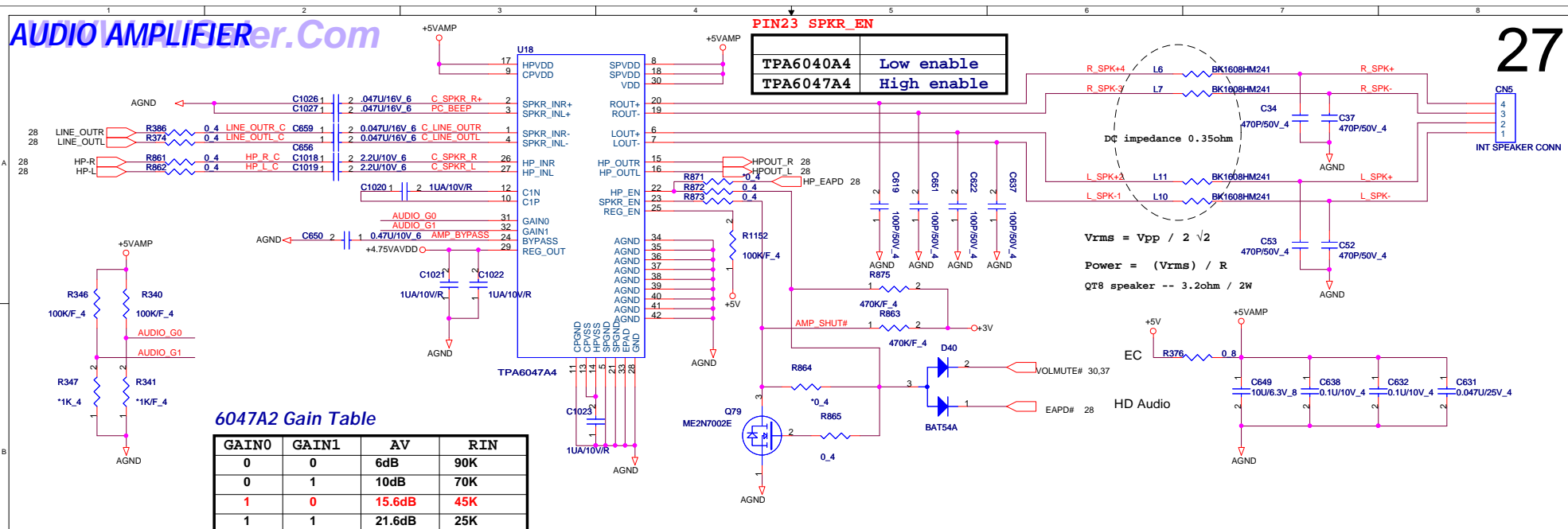
SA_F# -->EXT HP

Audio JACK: Normal Open

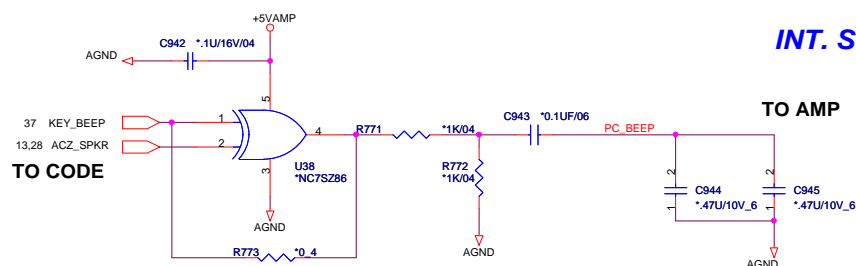


PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number Azalia AD1883	Rev 1A
Date: Thursday, October 16, 2008 Sheet 26 of 48		

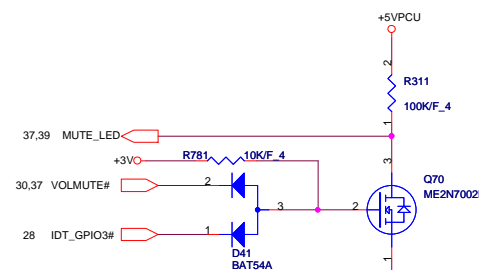


PC-BEEP

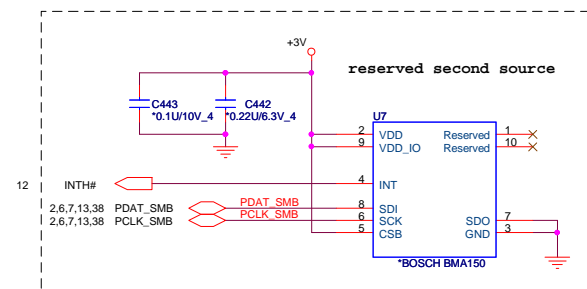
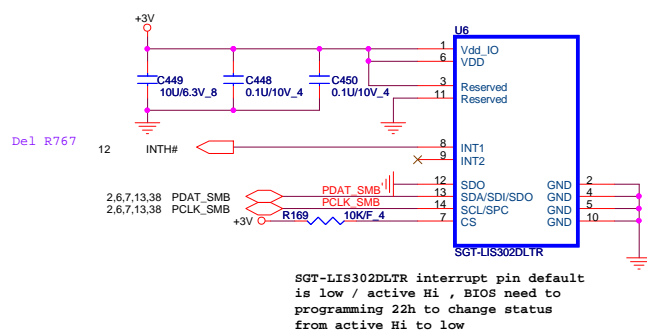


MUTE_LED

Low -->un-MUTE
High-->Mute

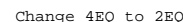


Acceleration sensor

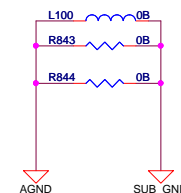


PROJECT : QT8
Quanta Computer Inc.

Size Custom Document Number
AMP_TPA6017/INT SPK
Date: Thursday, October 16, 2008 Sheet 29 of 48

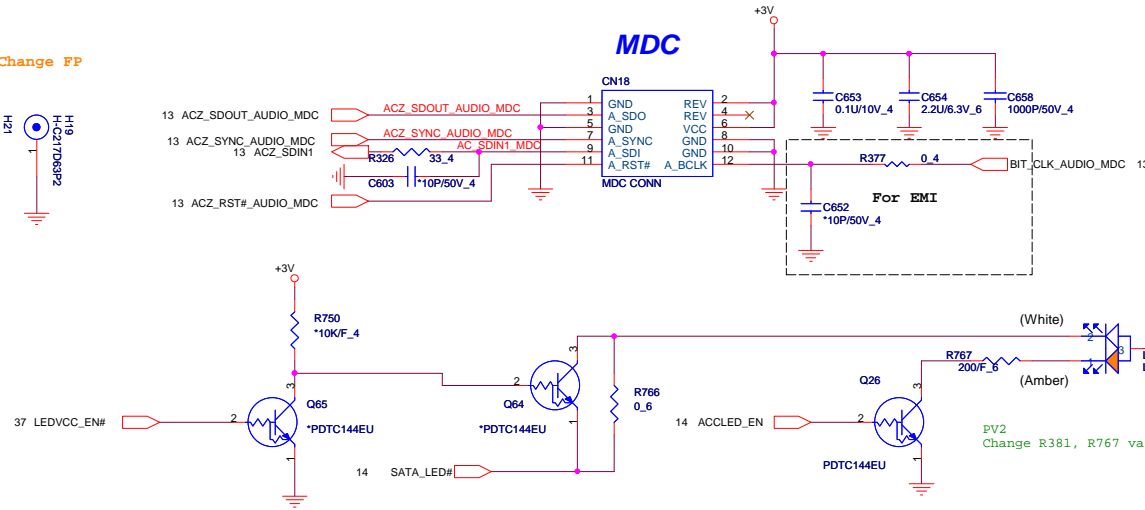
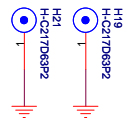


05/16 (PV) Change footprint for SMT line recommend



Size Custom	Document Number SUBWOOFER(EQ & AMP.)
Date: Thursday, October 16, 2008	Sheet 30 of 48

DB-1 Change Fp

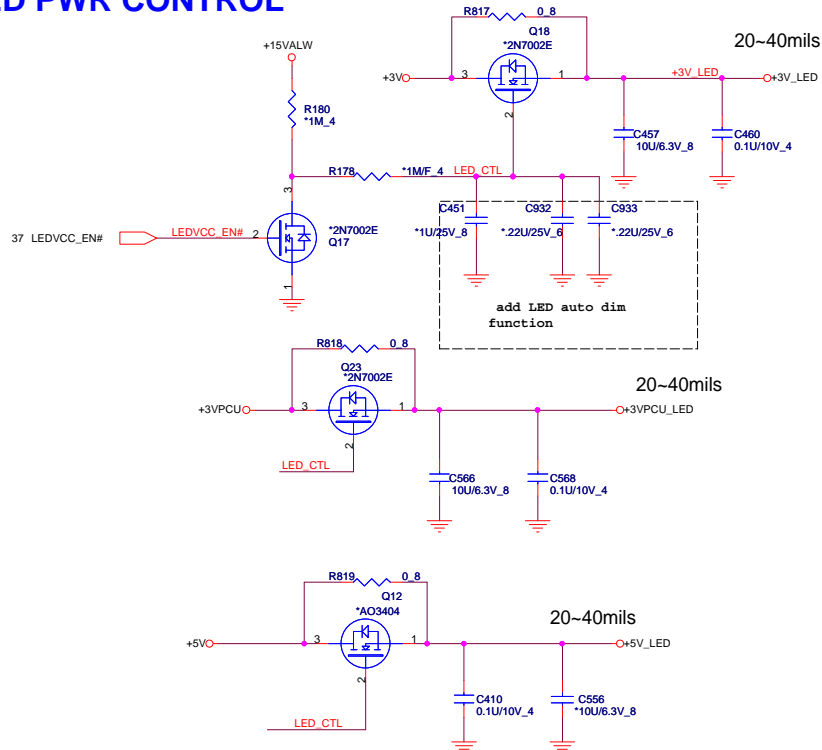


LED



SI-1 modified --
for fix SATA LED
no support LED
light control

LED PWR CONTROL

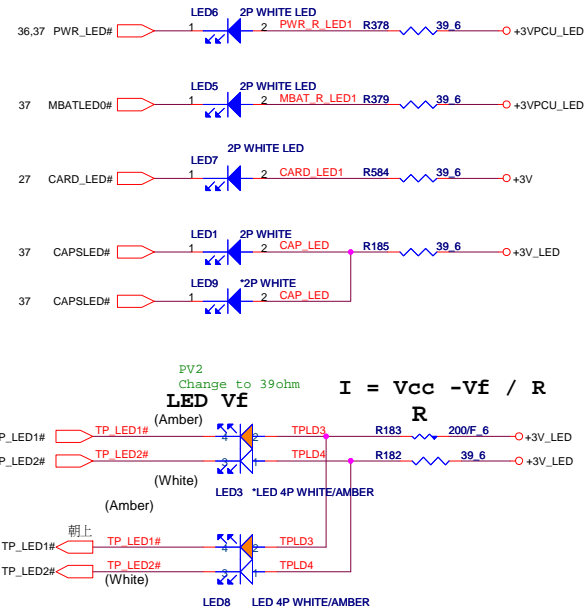


LED1 for 17.3"

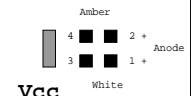
LED9 for 16.3"

LED3 for 16.3"

LED8 for 17.3"

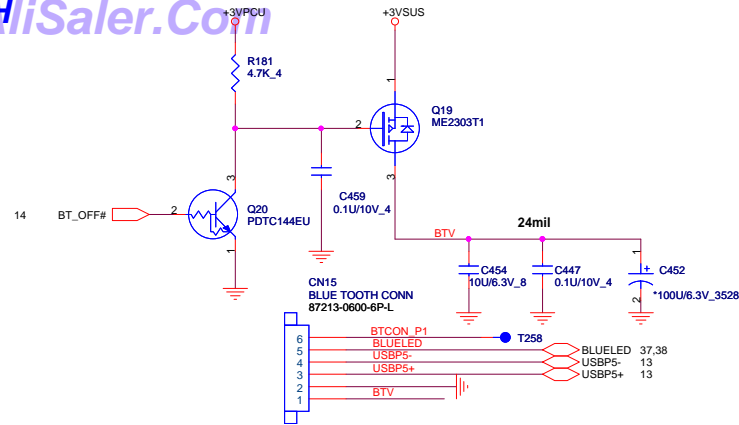


SI-1 modified --
change LED part
number

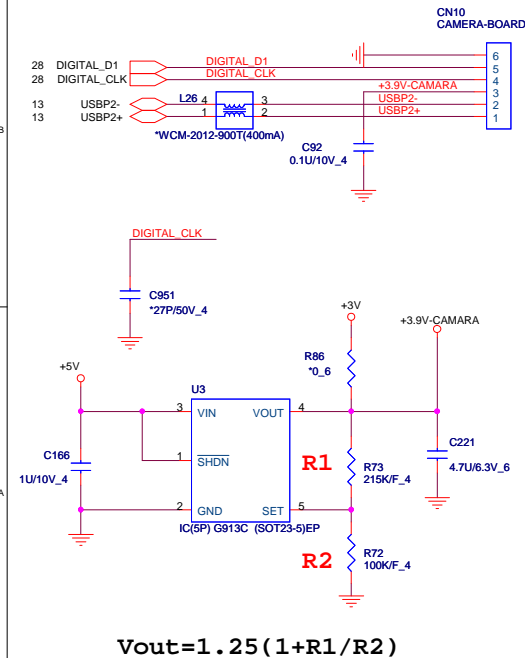


PROJECT : QT8
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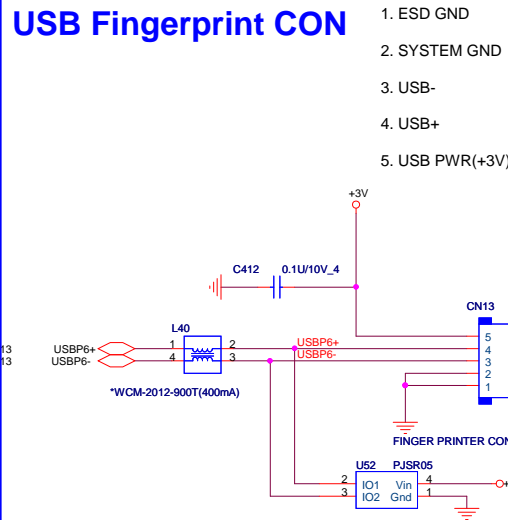
Size Custom	Document Number MDC1.5 Con Accelerometer/LED	Rev 1A
Date: Thursday, October 16, 2008	Sheet 31	of 48



USB CAMERA CONNECT



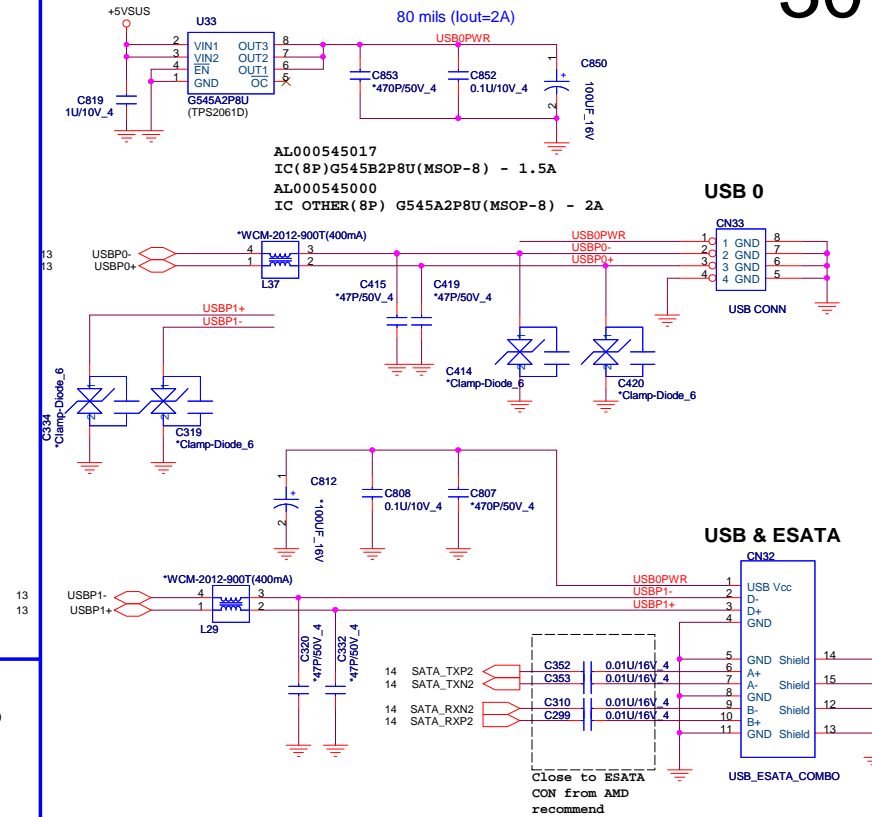
USB Fingerprint CON



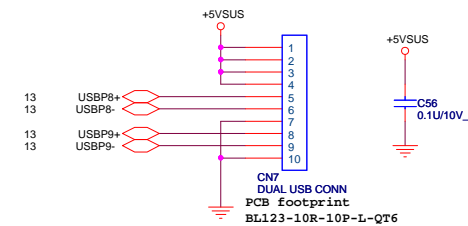
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

LEFT SIDE USBX1 and E-SATA/USB COMBO

30

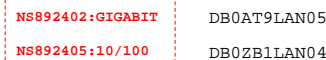


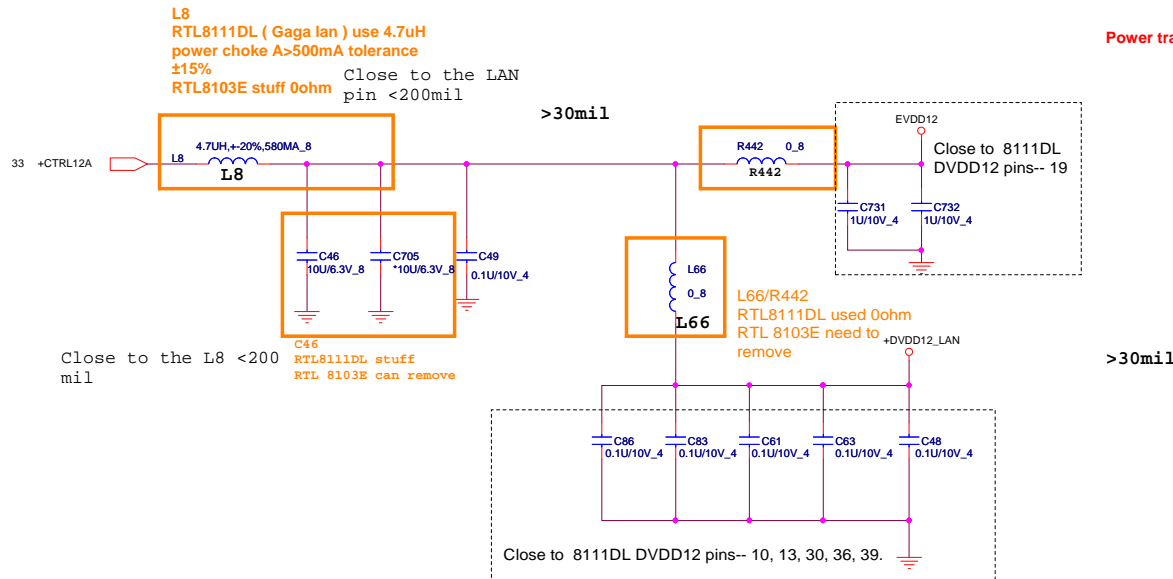
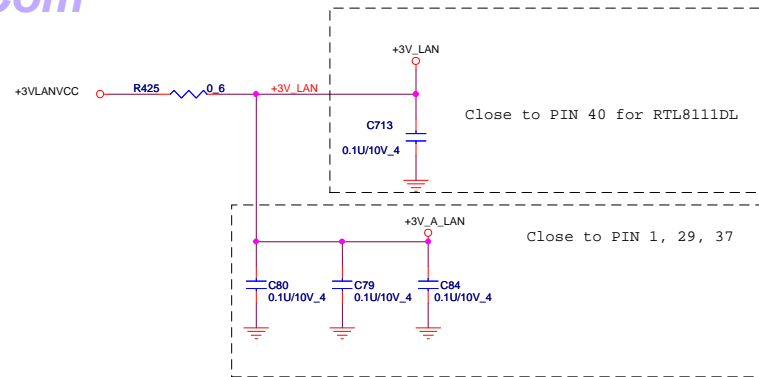
RIGHT SIDE USBX2



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Size Custom	Document Number BT/WEBCAM/FT/USBX4/ESATA	Rev 1A
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Power trace Layout 寬度> 30mil

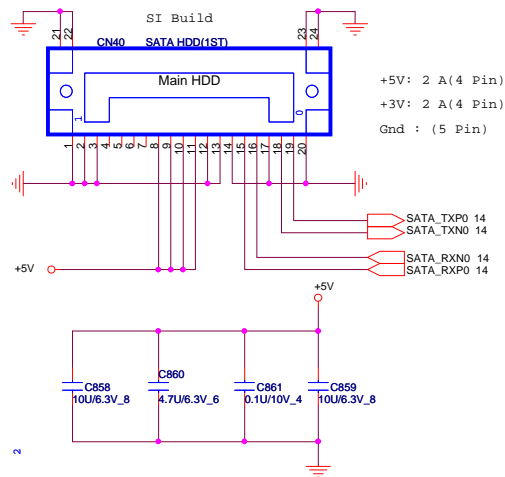
Power trace Layout 寬度> 30mil



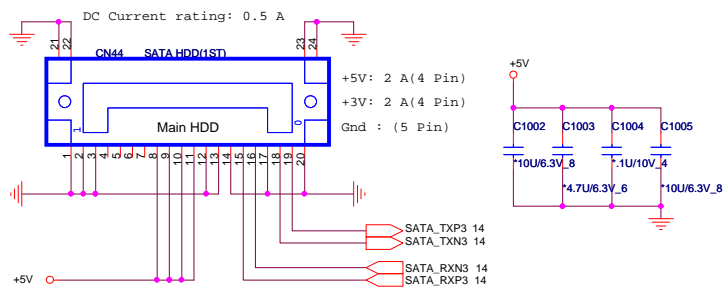
PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number LAN Power	Rev 1A
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SATA_1 HDD CONNECTOR



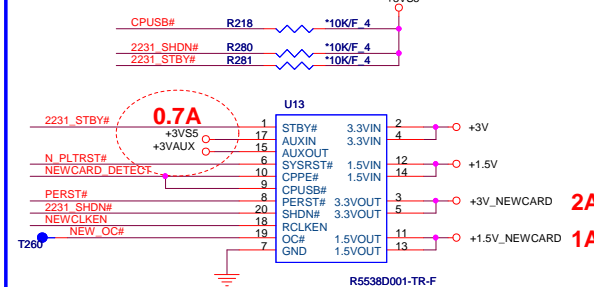
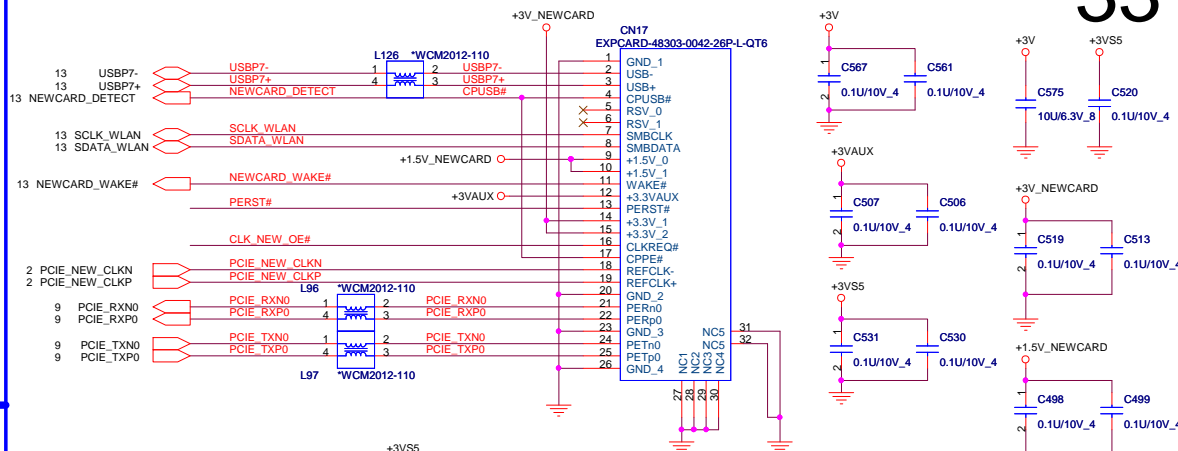
SATA_2 CONNECTOR



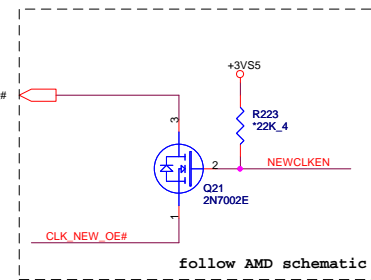
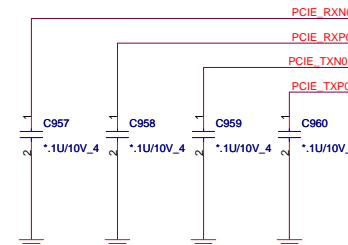
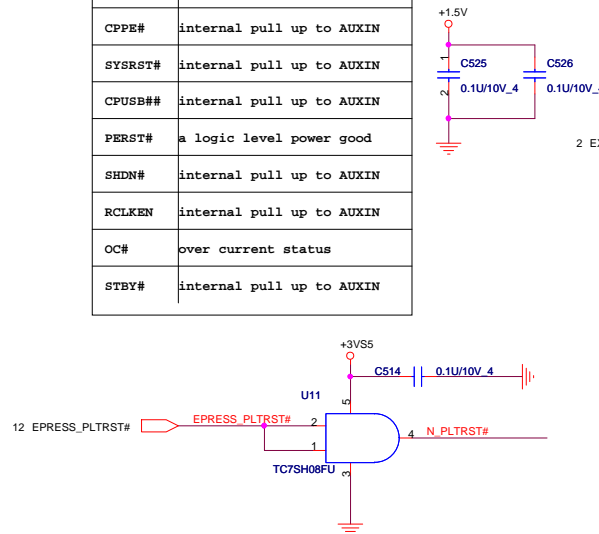
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

33

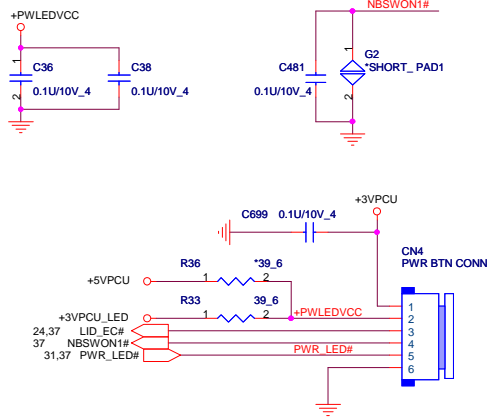


pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN

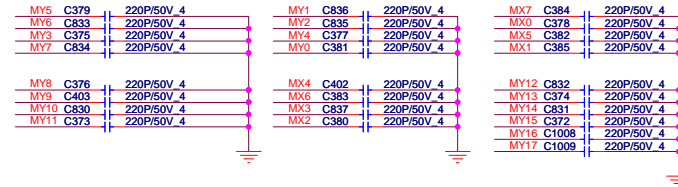


PROJECT : QT8
Quanta Computer Inc.

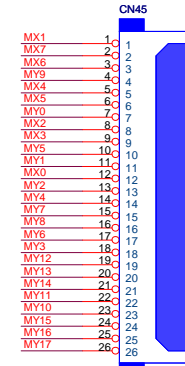
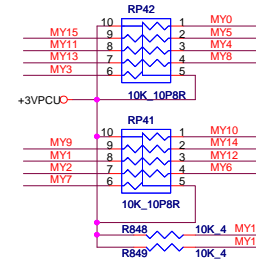
Size Custom	Document Number NEW CARD/SATA ODD/SATA HDD	Rev 1A
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1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

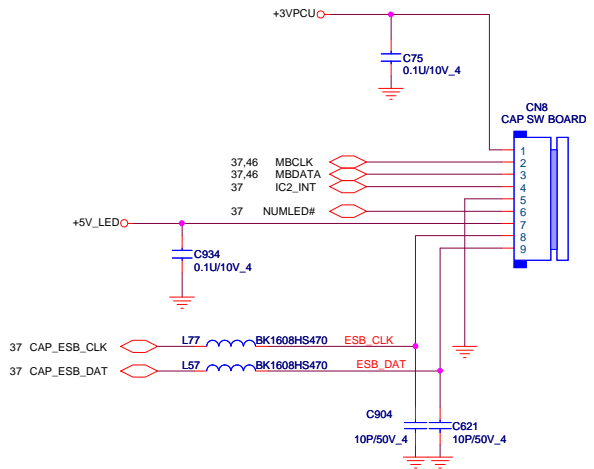


KEYBOARD PULL-UP

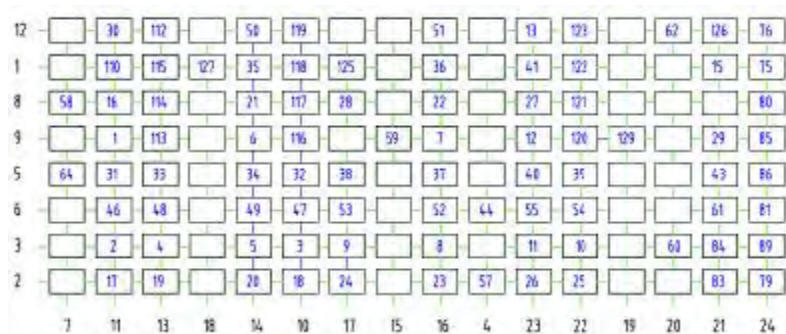
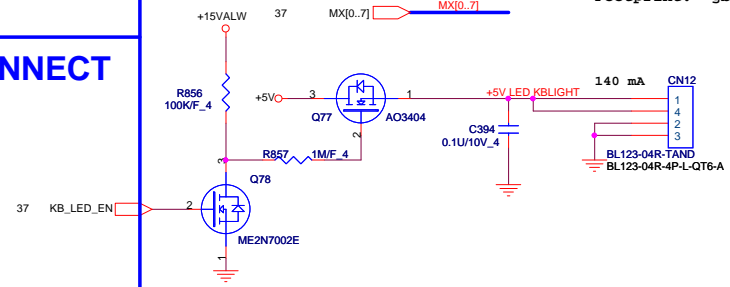


Footprint: "gb1rf260-1253-7f-26p-1"

CAP SW CONNECT

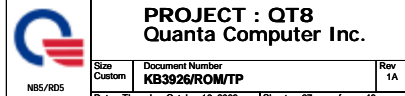


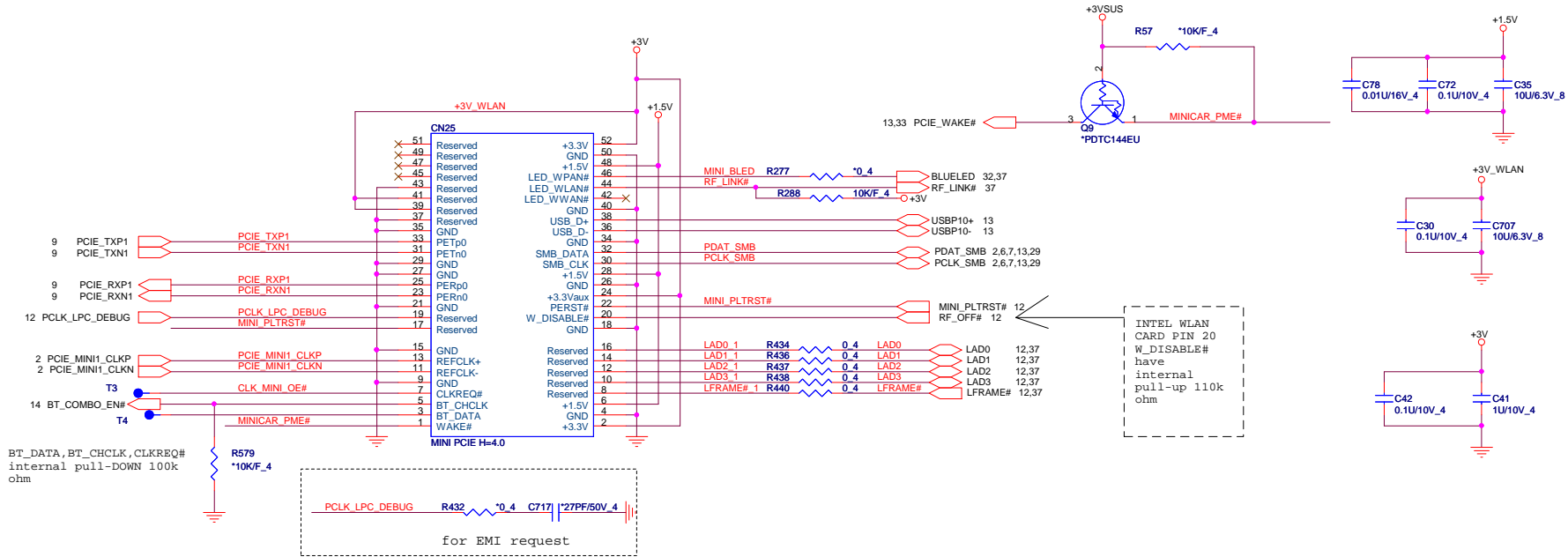
1. +3VPCU
2. MBCLK
3. MBCLK
4. MBCLK
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT



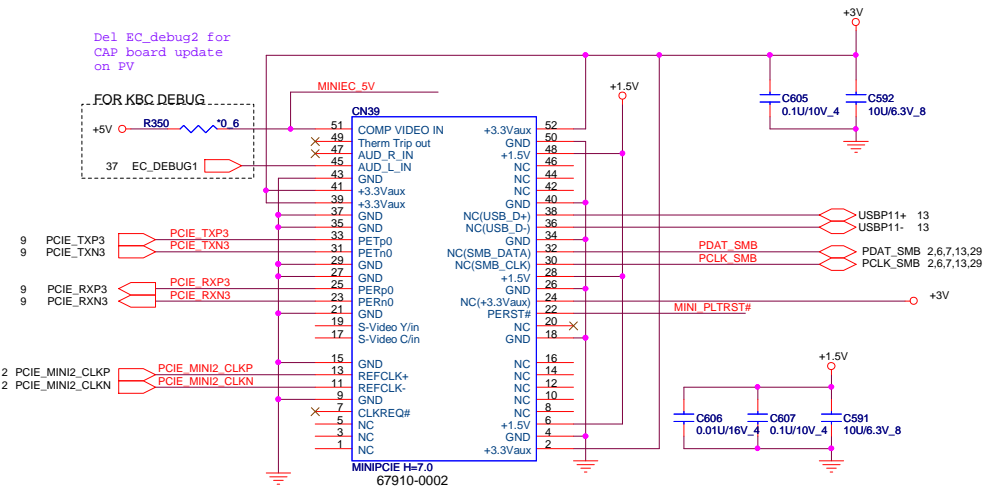
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number LED/KEYBOARD/SW	Rev 1A
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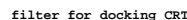
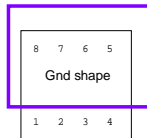


Mini PCI-E Card 2 TV tuner card

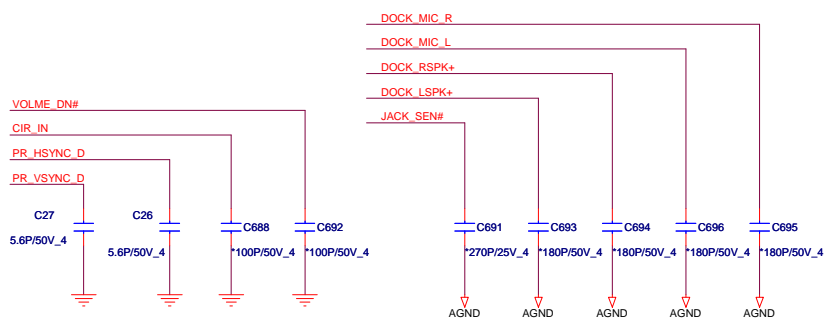


PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number Mini CARD X 3	Rev 1A
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**CPU FAN**

G995 layout notice

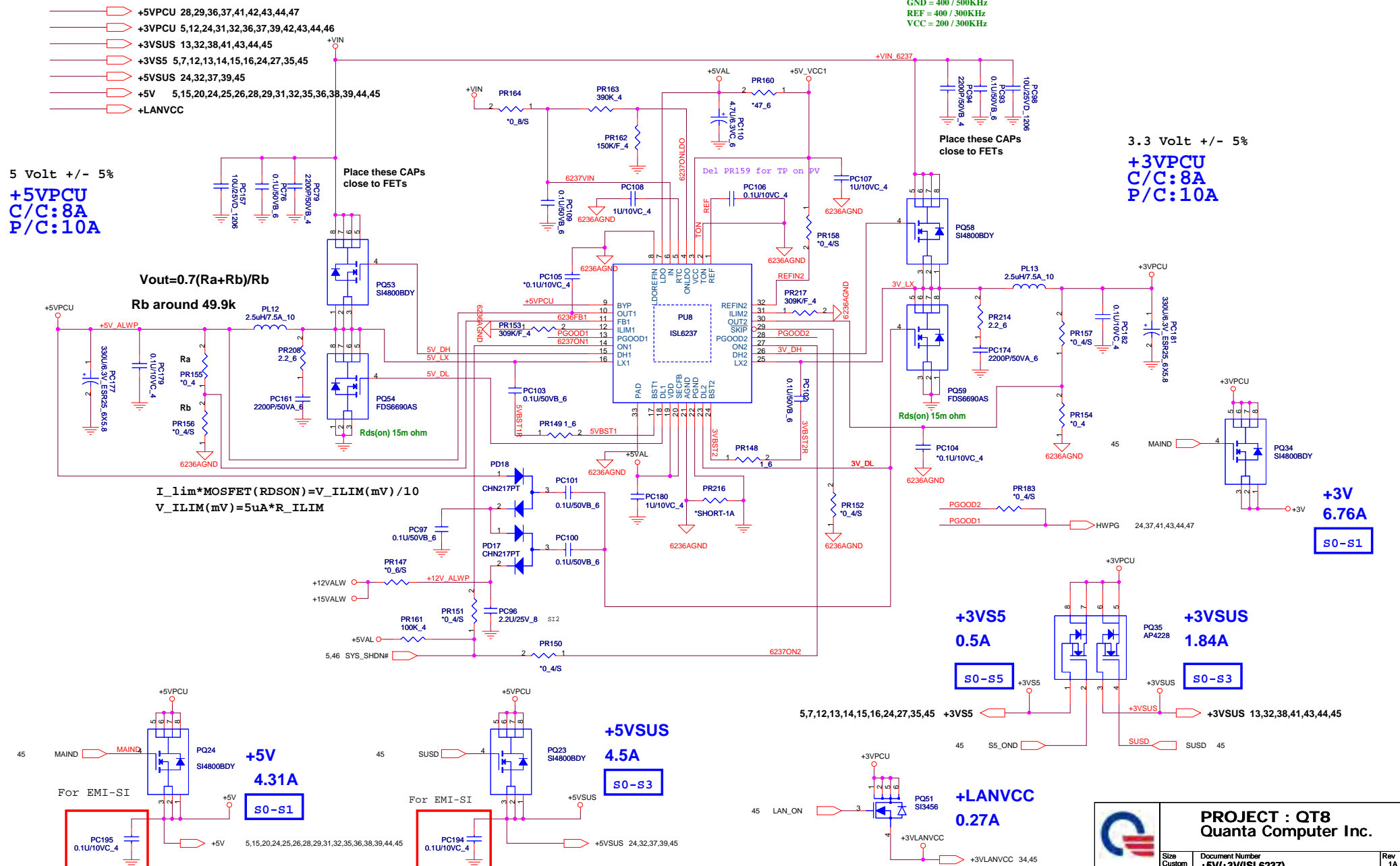


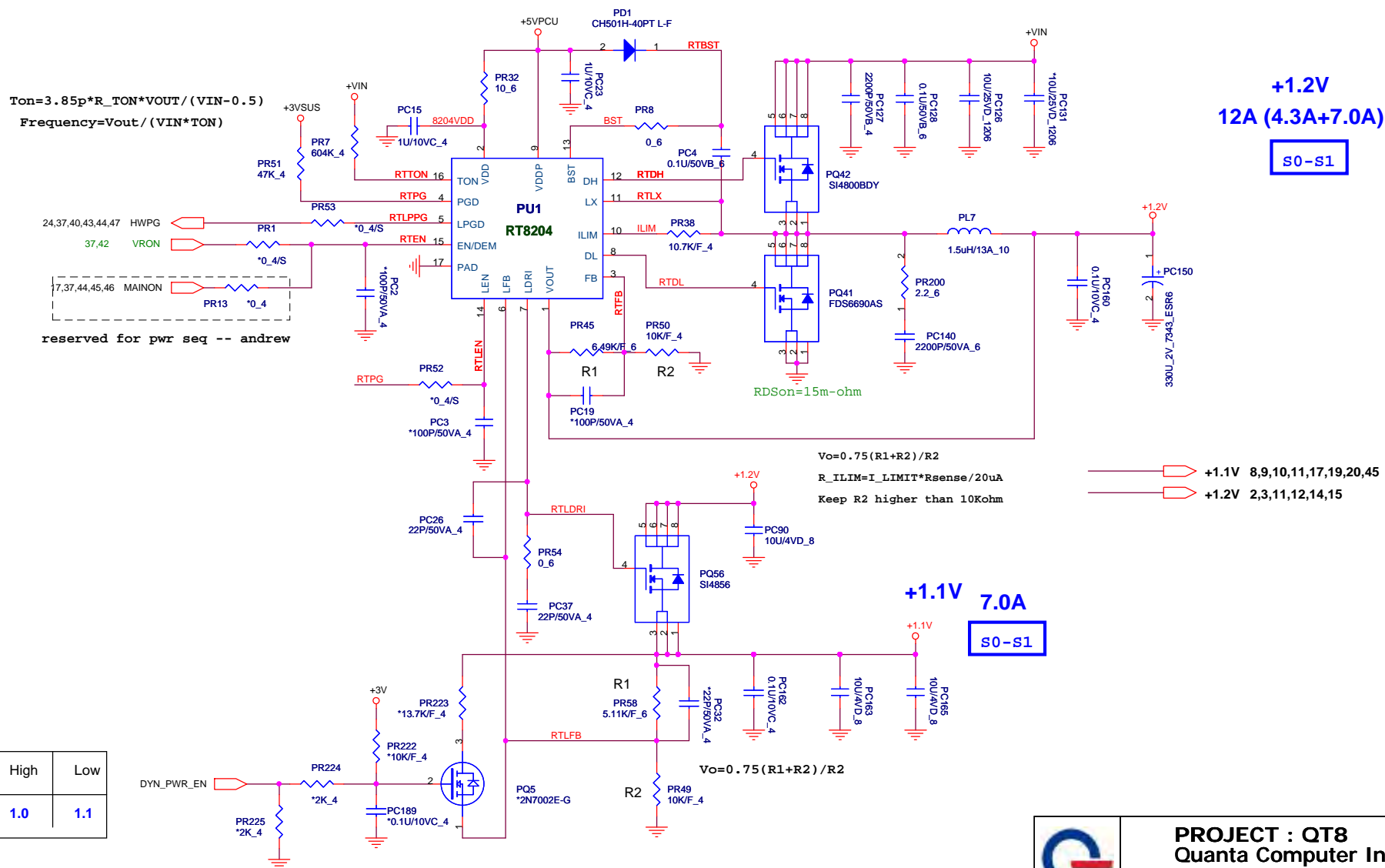
PROJECT : QT8
Quanta Computer Inc.

Size Custom	Document Number CABLE DOCKING/FAN
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DC/DC +3VPCU/+ 5VPCU/ +12VALW

40






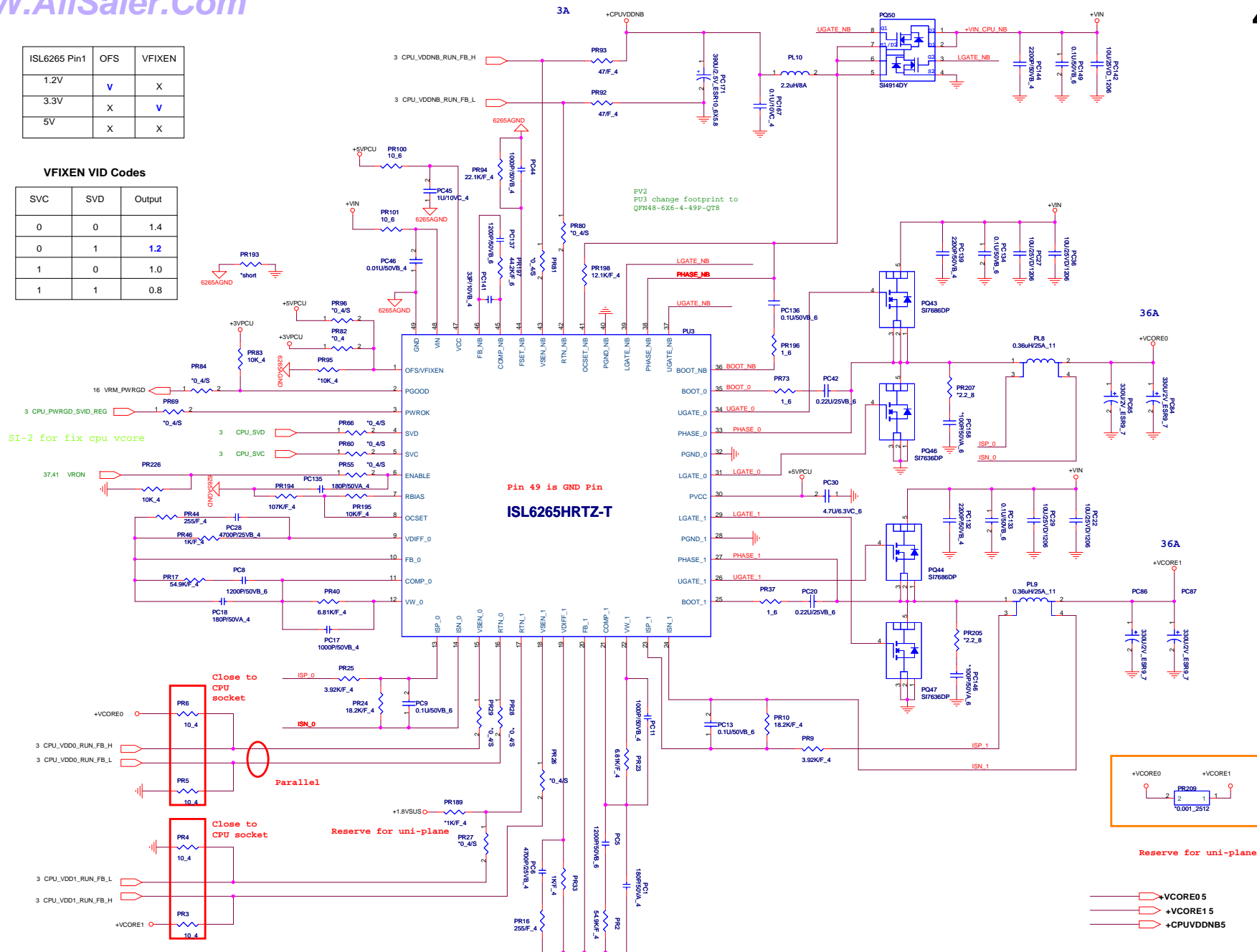
PROJECT : QT8
Quanta Computer Inc.

Size B	Document Number +1.2V & +1.1V(RT8204)	Rev 1A
Date: Thursday, October 16, 2008		Sheet 41 of 48

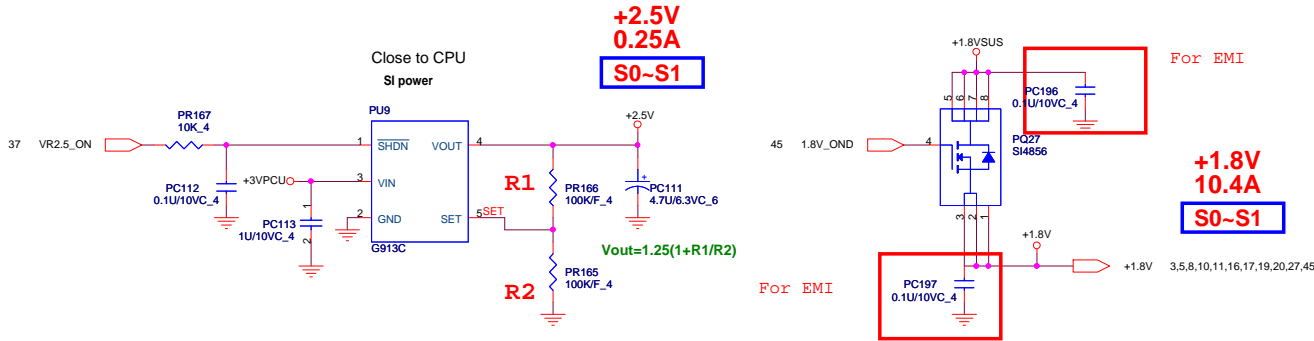
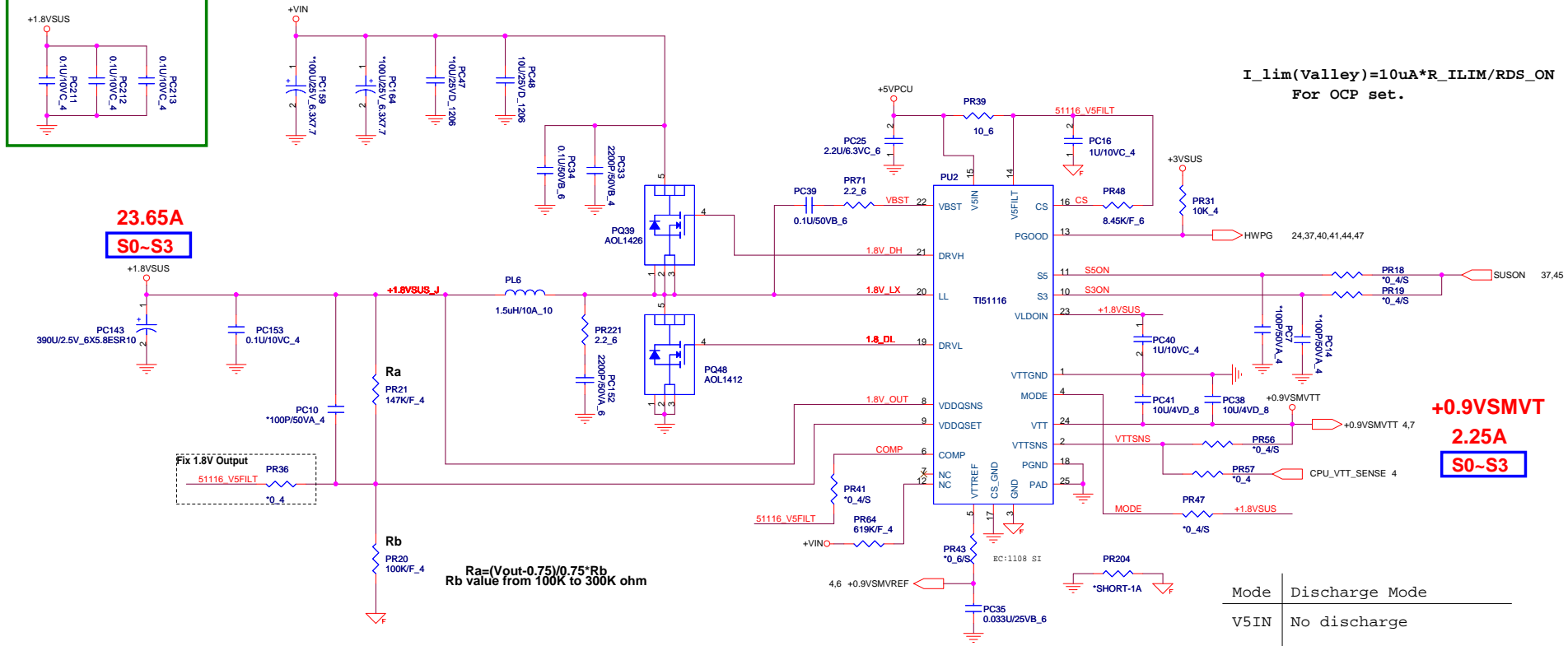
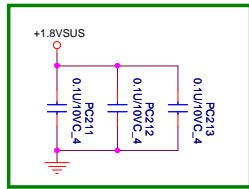
PROJECT : QT8
Quanta Computer Inc.

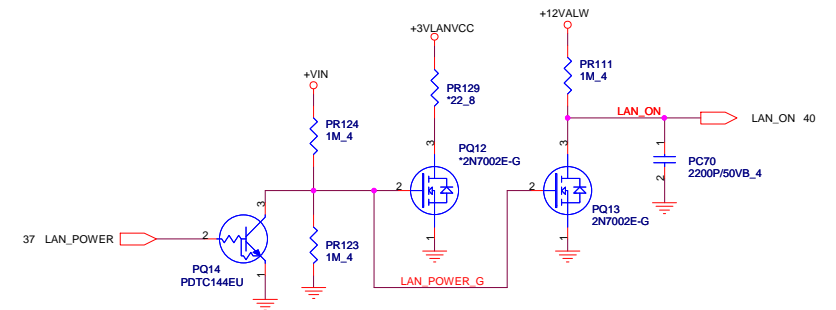
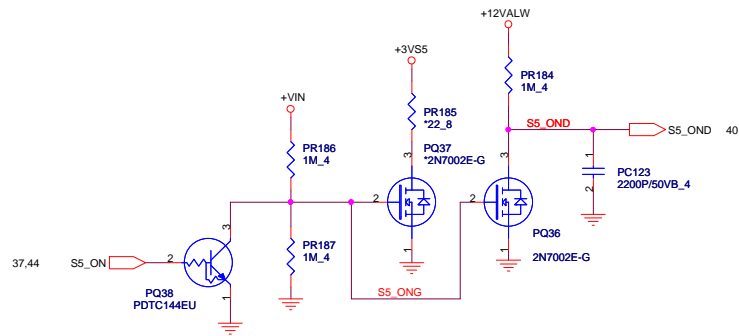
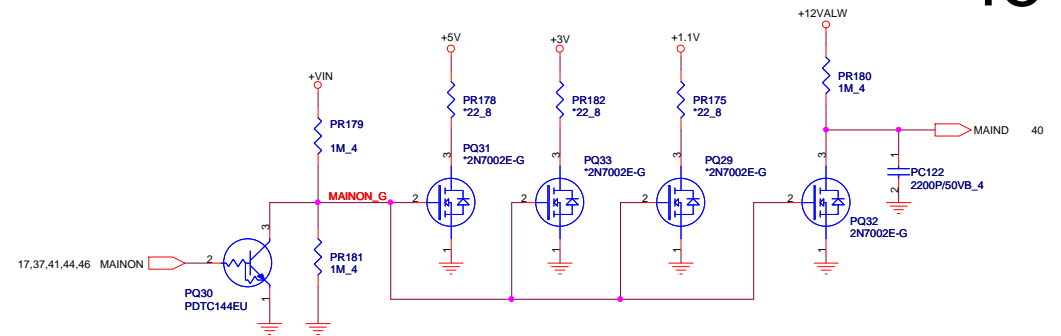
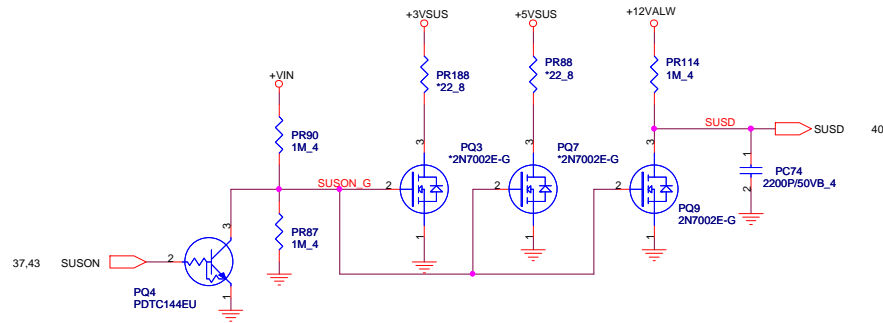
Size C	Document Number CPU_CORE(ISL6265)
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 +VCORE0 5
 +VCORE1 5
 +CPUVDDNB5

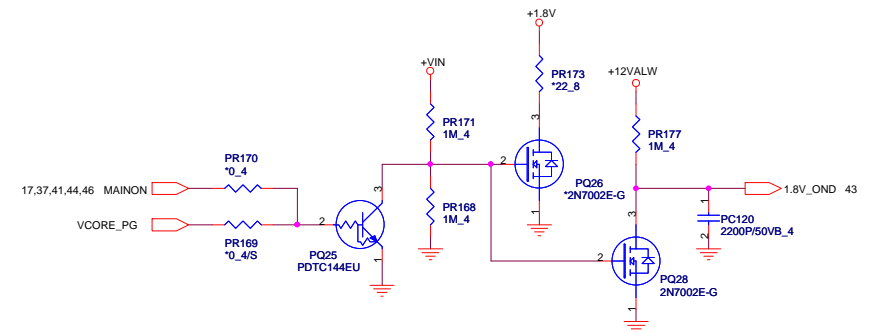
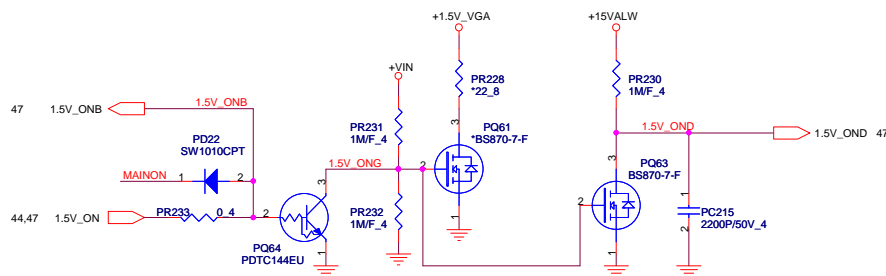



Add 0.1u CAP PC211, PC212, PC213 for EMI





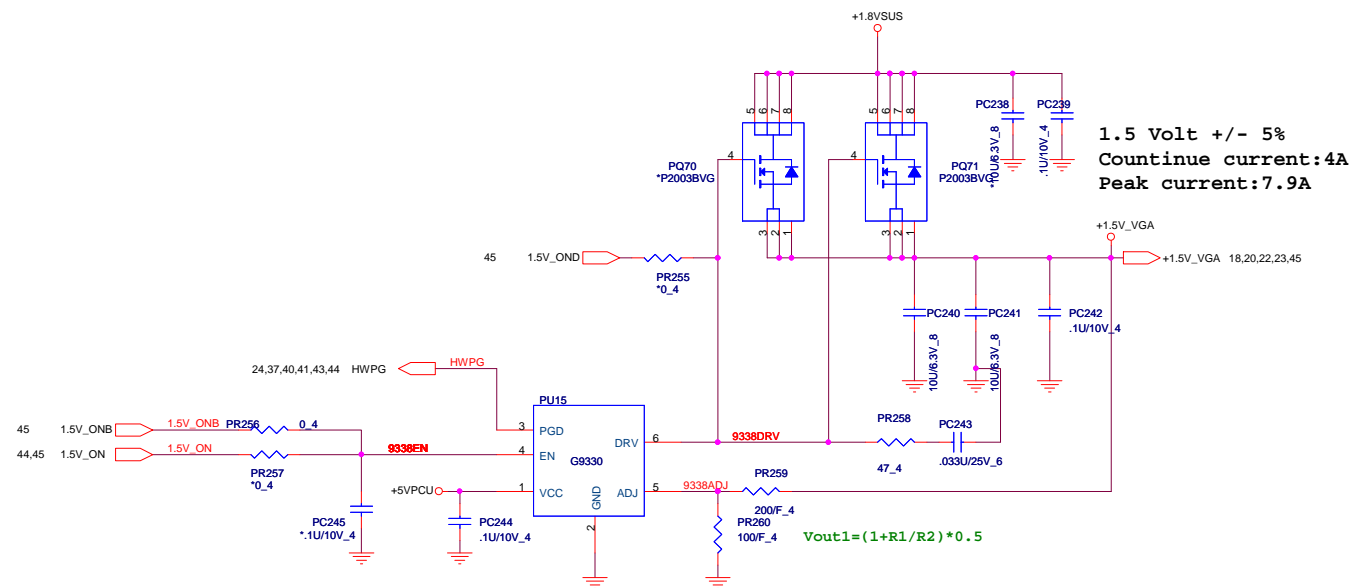
For Discrete Only



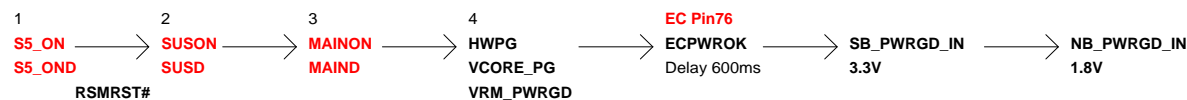
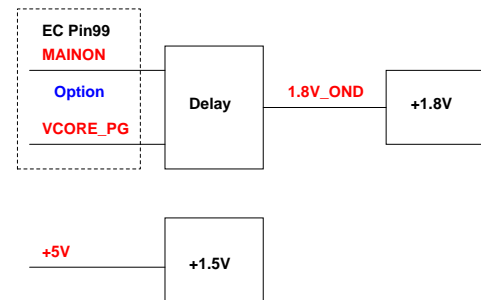
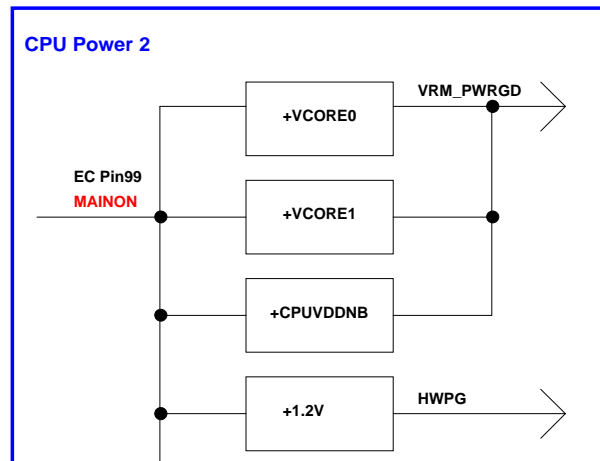
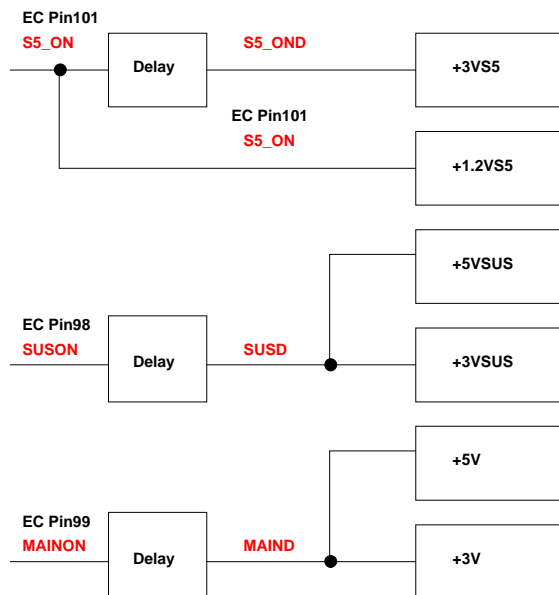
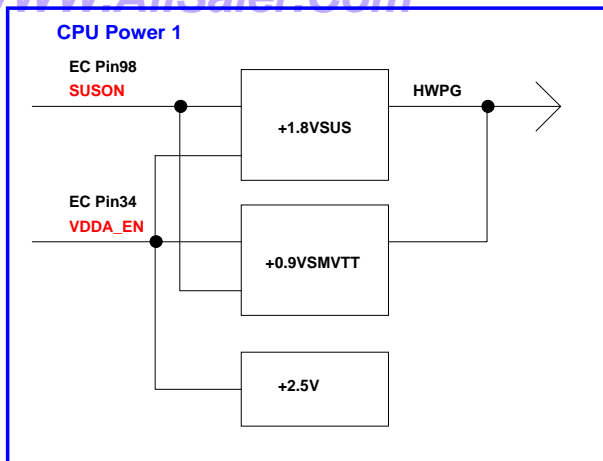
	PROJECT : QT8		
	Quanta Computer Inc.		
NB5/RD5	Size	Document Number	Rev
	Custom	DISCHARGE	1A
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Size Custom	Document Number CHARGER (ISL6251)	Rev 1A
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VRAM	Mounted	N/A	PQ33 P/N
Others	PR218, PR219, PR220, PR226, PR231, PC196, PC197, PC199, PC201, PD20, PU10	PR232	BAM44960000
Samsung	PR232	PR218, PR219, PR220, PR226, PR231, PC196, PC197, PC199, PC201, PD20, PU10	BAM48560029



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Quanta Computer Inc.

Size Custom	Document Number Power control	Rev 1A
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