QT8 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

DDRII-SODIMM1 PAGE 7,8
DDRII-SODIMM2 PAGE 7,8
DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

14.318MHz
CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2
CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

HT3

PCI-E
PCI-Express 16X

NORTH BRIDGE
RX781 / RS780MN
A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11,

HDMI PAGE 23
CRT PAGE 24
LVDS PAGE 23

ATI M82-S for Discrete only
64 Bit,DDR2*4
M82-SCE A11
PAGE 17,18,19 20,21,22

Side port
256mb RAM for UMA only PAGE 8

ALINK X4

SOUTH BRIDGE
SB700 A12
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

USB2.0
1,8,9 USB2.0 Ports X3 PAGE 30
5 Blueflame PAGE 30
2 Webcam X1 PAGE 30
6 Fingerprint PAGE 30
3 Flash Media for UMA only RTS5158 PAGE 25
Touch Screen for Discrete only

10 PCI-E WLAN Card x1 PAGE 36
11 TV-TUNER Card x1 PAGE 36
7 Express Card x1 PAGE 33
4 Cable Docking x1 PAGE 37

Cable Docking PAGE 37
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

X1 LAN Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN) PAGE 31,32
RJ45 PAGE 31

X1 Express Card (NEW CARD) PAGE 33

X3 Mini PCI-E Card (Wireless LAN/TV TUNNER) PAGE 36

SYSTEM CHARGER(ISL6251A) PAGE 44
SYSTEM POWER ISL6236IRZA-T PAGE 38
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 41
VCCP +1.1V AND +1.2V(MAX8717) PAGE 39
VGACORE(1.1V~1.2V)Oz8118 PAGE 42
CPU CORE ISL6265A PAGE 40

TWO SATA - HDD PAGE 33
SATA0,1 150MB
SATA - CD-ROM PAGE 33
SATA0 150MB
E-SATA PAGE 30
SATA4 150MB

PCIE BUS
JMICRON JMD380 for Discrete only PAGE 27

Azalia
IDT 92HD71B7 PAGE 27
MDC CONN PAGE 29
AUDIO Amplifier TPA6017A2 PAGE 28
IEEE1394 connect for Discrete only PAGE 26
Memory CardReader PAGE 25

SMBUS
Accelerometer LIS3LV02DL PAGE 28
LPC
Keyboard PAGE 34
Touch Pad PAGE 34
CIR (AUDIO CONN) PAGE 27
Capacitive Sense SW PAGE 34

ENE KBC
KB3926 Cx
PAGE 35

Digital MIC PAGE 30
AUDIO CONN (Phone/ MIC) PAGE 27
Audio Conn PAGE 28

FAN PAGE 37
SPI PAGE 35

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, February 19, 2008 Sheet 1 of 45

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653,R656,R612 STUFF	R653,R656,R612 NC	To M82-S 27Mhz - RX780 only

+1.2V L49 BLM18PG181SN1D(180,1.5A)_6 60 ohm, 0.5A
600 ohms@100Mhz
C523 10U/6.3V_8
C518 C496 C527 C521 C476 C515 0.1U/10V_4
+1.2V_CLKVDDIO

DCR: 0.5 ohm
600 ohms@100Mhz
+3V L51 BLM18PG181SN1D(180,1.5A)_6 +3V_CLKVDD 60 ohm, 0.5A
C541 10U/6.3V_8
C468 C473 C512 C522 C508 C500 C474 C471 C469 0.1U/10V_4

+3V_CLKVDD L42 BLM18PG181SN1D(180,1.5A)_6 +3V_CLK_VDDA
C464 10U/6.3V_8
C482 C470 0.1U/10V_4
Place very close to C/G

U10A

49	VDDA	CPUKG0T_LPRS	56 CPUCLKP
48	GNDA	CPUKG0C_LPRS	55 CPUCLKN
62	VDDREF	ATIG0T_LPRS	33 NBGFX_CLKP
66	GNDREF	ATIG0C_LPRS	32 NBGFX_CLKN
		ATIG1T_LPRS	31 EXT_GFX_CLKP
		ATIG1C_LPRS	30 EXT_GFX_CLKN
		ATIG2T_LPRS	26
		ATIG2C_LPRS	25
69	VDD48	SB_SRC0T_LPRS	40 PCIE_MINI2_CLKP
29	VDDATIG	SB_SRC0C_LPRS	39 PCIE_MINI2_CLKN
54	VDDCPU	SB_SRC1T_LPRS	35 CLK_PCIE_CARD
61	VDDHTT	SB_SRC1C_LPRS	34 CLK_PCIE_CARD#
38	VDDSB_SRC		
17	VDDSRC		
44	VDDSATA		
3	VDDDOT		
53	VDDCPU_IO	SRC0T_LPRS	23 NBGPP_CLKN_R
28	VDDATIG_IO	SRC0C_LPRS	22 NBGPP_CLKN_L
37	VDDSB_SRC_IO	SRC1T_LPRS	21 PCIE_NEW_CLKP
12	VDDSRC_IO1	SRC1C_LPRS	20 PCIE_NEW_CLKN
18	VDDSRC_IO2	SRC2T_LPRS	16 PCIE_MINI1_CLKP
		SRC2C_LPRS	15 PCIE_MINI1_CLKN
		SRC3T_LPRS	14 SBLINK_CLKP
		SRC3C_LPRS	13 SBLINK_CLKN
		SRC4T_LPRS	10 SBSRC_CLKP
		SRC4C_LPRS	9 SBSRC_CLKN
		SRC5T_LPRS	8 PCIE_LAN_CLKP
		SRC5C_LPRS	7 PCIE_LAN_CLKN
72	GND48	SRC6T/SATAT_LPRS	46
27	GNDATIG1	SRC6C/SATAC_LPRS	45
6	GNDDOT	SRC7T_LPRS/27Mhz_SS	5 CLK_VGA_27M_SS
52	GNDCPU	SRC7C_LPRS/27Mhz_NS	4 CLK_VGA_27M_NSS
58	GNDHTT		
47	GNDSATA		
36	GNDSB_SRC		
11	GNDSRC1		
19	GNDSRC2		
67	X1	HTT0T/66M_LPRS	60
68	X2	HTT0C/66M_LPRS	59 NBHTREFCLK0P
		48MHz_0	71 NBHTREFCLK0N
		48MHz_1	70 CLK48MUSB
57	PD#	REF0/SEL_HTT66	65 SEL_HT66
		REF1/SEL_SATA	64 SEL_SATA
1	SMBCLK	REF2/SEL_27	63 SEL_27
2	SMBDAT		
		CLKREQ0#	24 CLKREQ0#
		CLKREQ1#	51 EXT_NWD_CLK_REQ#
		CLKREQ2#	50 CLKREQ2#
		CLKREQ3#	43 CLKREQ3#
41	SB_SRC_SLOW#	CLKREQ4#	42 CLKREQ4#

SLG8SP626VTR

THERMAL GND
73 eGND73
74 eGND74
75 eGND75
77 eGND77
76 eGND76
78 eGND78
U10B
SLG8SP626VTR

C466 33P/50V_4 CG_XIN
Y2 14.318MHZ
C465 33P/50V_4 CG_XOUT
CG_XIN CG_XOUT CLK_PD# PCLK_SMB PDAT_SMB
6,7,13,28,36 PCLK_SMB
6,7,13,28,36 PDAT_SMB
14 CHIPSET_PCIE_SLOW_SB# D17 *CH501H-40PT L-F SB_SRC_SLOW#

can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/S0
power level

when driven low SB_SRC clocks slow only supported with to reduced setpoint custom CG IC

Place within 0.5" of CLKGEN
R196 *261_4
Del RP for TP on PV

RP43 CPUCLKP
RP54 NBGFX_CLKP
RP53 EXT_GFX_CLKP
T196
T84
RP48 PCIE_MINI2_CLKP
RP55 CLK_PCIE_CARD
Del RP52 for NBGPP CLK
T59
T62
RP51 PCIE_NEW_CLKP
RP49 PCIE_MINI1_CLKP
RP47 SBLINK_CLKP
RP45 SBSRC_CLKP
RP44 PCIE_LAN_CLKP
R527 33_4 OSC_SPREAD
R415 75/F_4
R490 100/F_4
R193 0_4 NBHT_REFCLKP
R194 0_4 NBHT_REFCLKN
R201 33_4 CLK_48M_CR
R192 33_4 CLK_48M_USB
T58
T167
EXT_NWD_CLK_REQ# 33

CPUCLKP 3
CPUCLKN 3
NBGFX_CLKP 10
NBGFX_CLKN 10
EXT_GFX_CLKP 17
EXT_GFX_CLKN 17
to NB for external Graphics reference clock
to M82-S -RX780 only
PCIE_MINI2_CLKP 36
PCIE_MINI2_CLKN 36
CLK_PCIE_CARD 26
CLK_PCIE_CARD# 26
to TV TUNER CARD
to PCIE-CARD READER
PCIE_NEW_CLKP 33
PCIE_NEW_CLKN 33
PCIE_MINI1_CLKP 36
PCIE_MINI1_CLKN 36
SBLINK_CLKP 10
SBLINK_CLKN 10
SBSRC_CLKP 12
SBSRC_CLKN 12
PCIE_LAN_CLKP 31
PCIE_LAN_CLKN 31
to EPRESS CARD
to WLAN
to NB for AC-LINK reference clock
to SB
to PCIE-LAN
SI-1 Modified --remove to ROBSON
OSC_SPREAD 18
EVGA-XTALI 18
SSIN - for M82 - 3.3V level input
X_TALIN --for M82 -1.8V level input
NBHT_REFCLKP 10
NBHT_REFCLKN 10
CLK_48M_CR 25
CLK_48M_USB 13

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

R186 Ra 158/F_4
R184 1 2 90.9/F_4 Rb
EXT_NB_OSC 10

	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

C952 *10P/50V_4 EXT_NB_OSC
C953 *10P/50V_4 CLK_48M_USB
C954 *10P/50V_4 CLK_48M_CR
C955 *10P/50V_4 EVGA-XTALI
C956 *10P/50V_4 OSC_SPREAD
SI-1 modified -- reserve for EMT

+3V
R756 *8.2K_4 CLKREQ0#
R757 *8.2K_4 CLKREQ2#
R758 *8.2K_4 CLKREQ3#
R759 *8.2K_4 CLKREQ4#
if use clock request pin , need to pull Hi for default sttting

ICS ICS9LPR476BKLFT--AJRS4760000
SLG SLG8SP626VTR--AJ006260000
RTL RTM880N-795-- AJ008800000

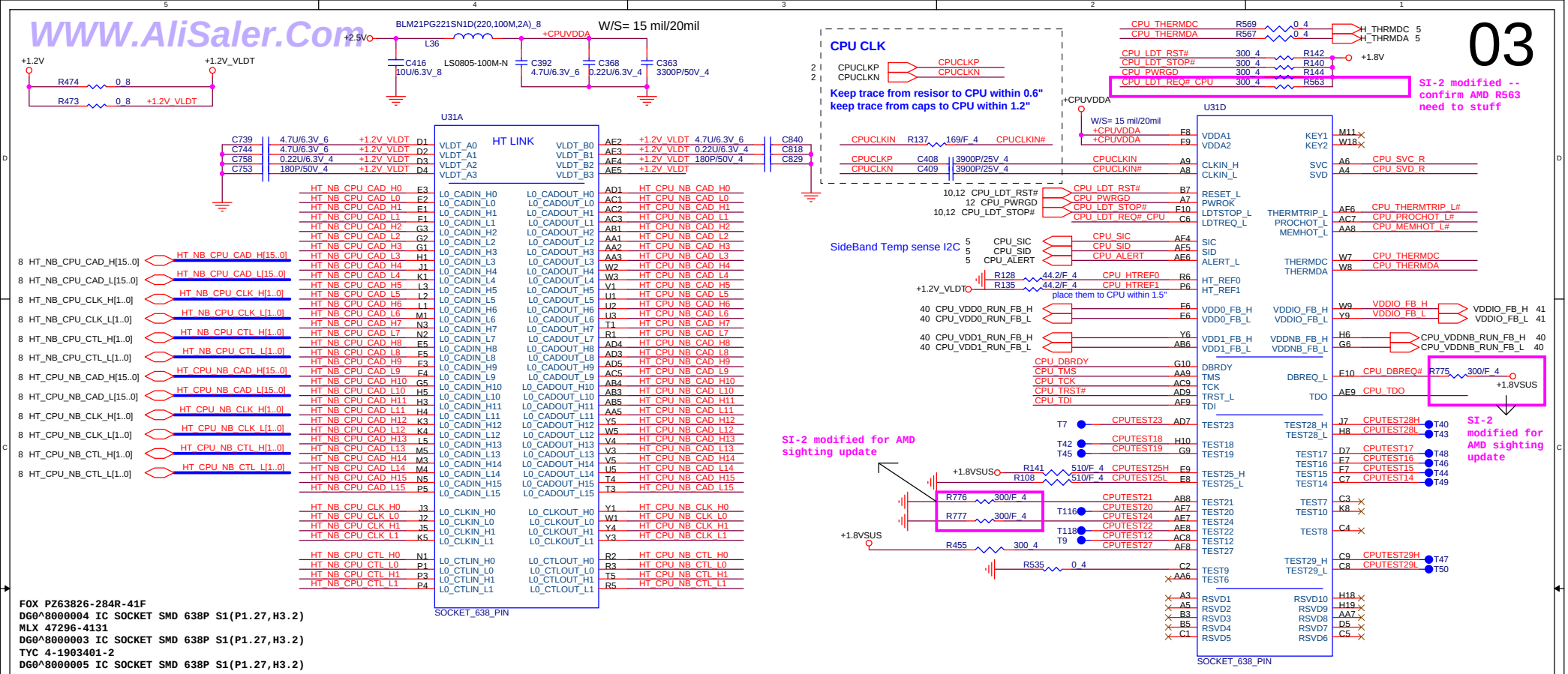
* default

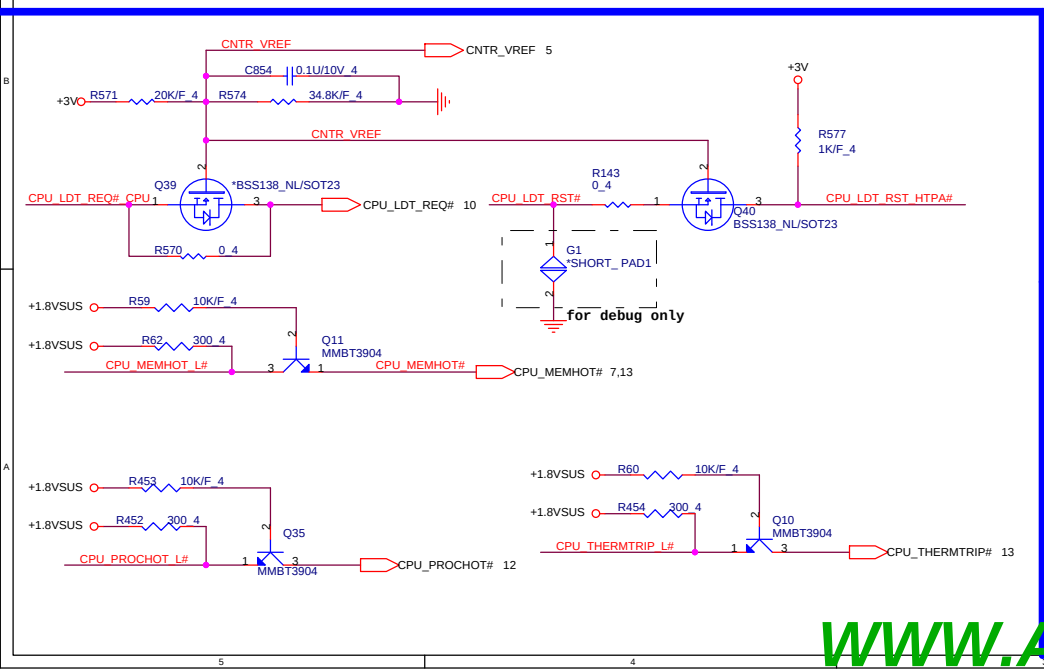
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

+3V_CLKVDD
R189 *8.2K_4
R195 8.2K_4
SEL_27
SEL_SATA
SEL_HT66
R203 8.2K_4
R202 *8.2K_4
RS780M/RX780M

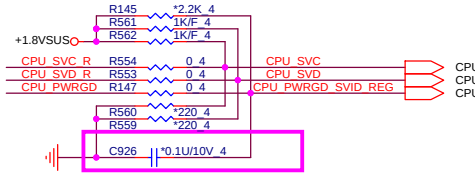
+3V
EXT_NWD_CLK_REQ# 8.2K_4 R219
CLK_PD# 8.2K_4 R204
SB_SRC_SLOW# 8.2K_4 R261

PROJECT : QT8
Quanta Computer Inc.
NB5/RD5
Size Custom
Document Number Clock Generator
Rev 1A
Date: Tuesday, February 19, 2008
Sheet 2 of 45





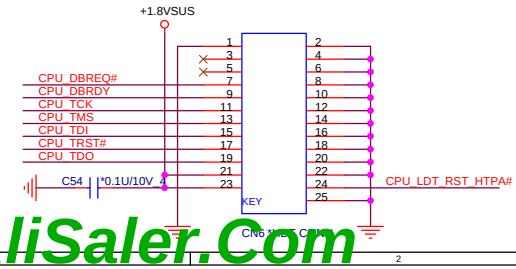
Serial VID



VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

HDT Connector



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 HT,CTL I/F 1/3	1A

NB5/RD5

Date: Tuesday, February 19, 2008 Sheet 3 of 45

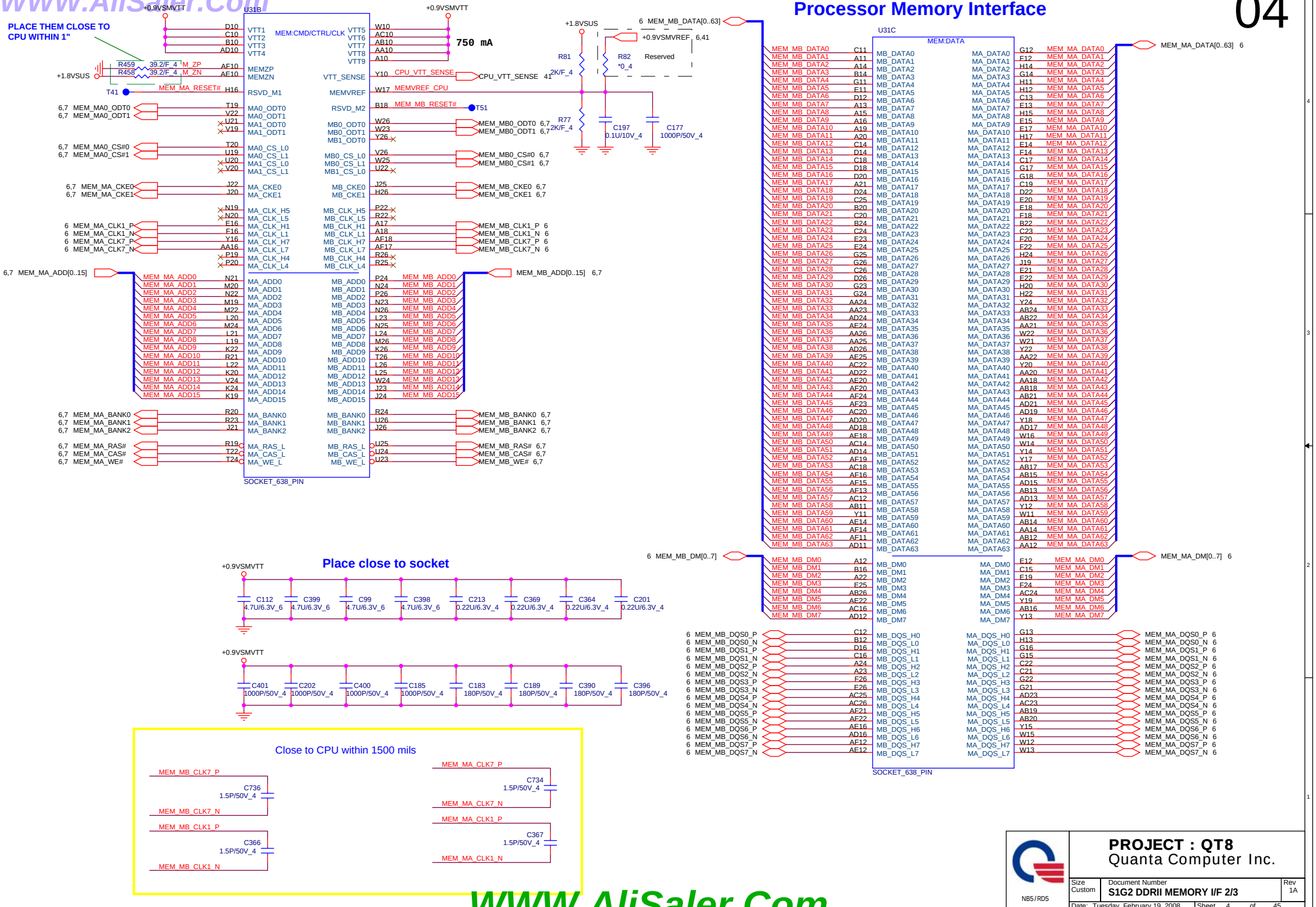
Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"

750 mA

Place close to socket

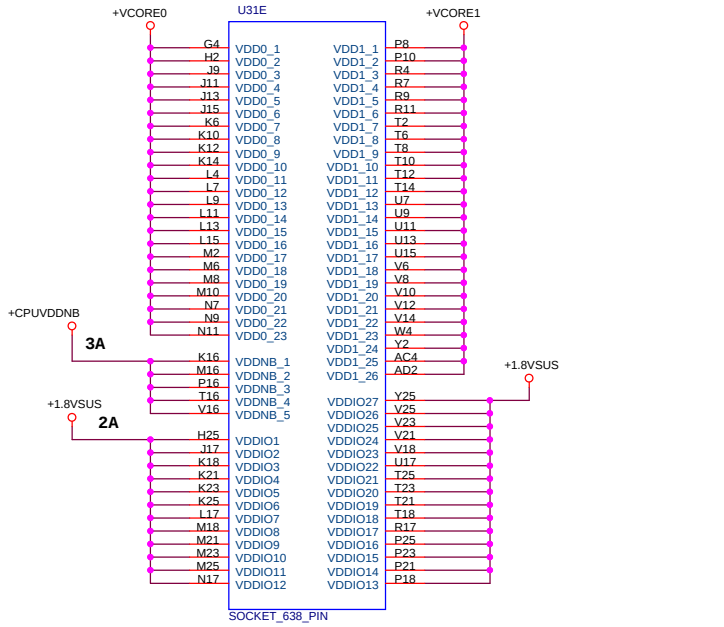
Close to CPU within 1500 mils

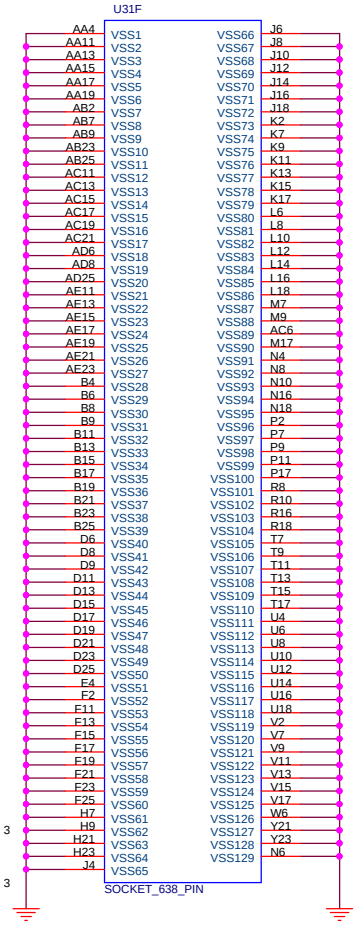


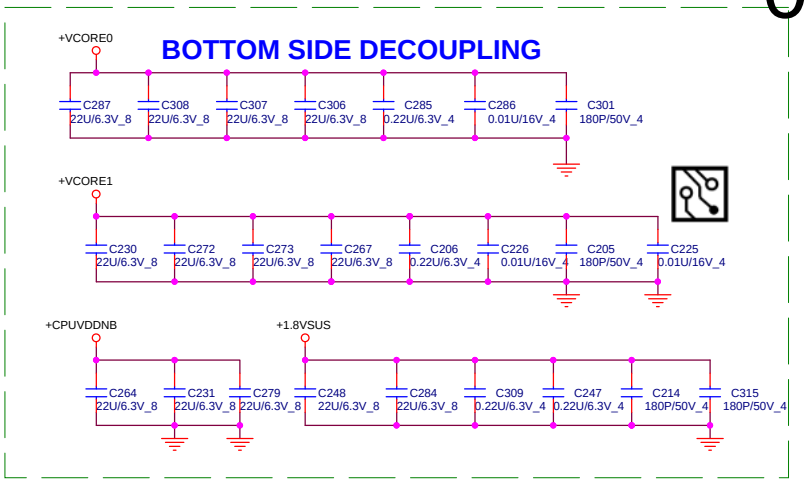
PROJECT : QT8		
Quanta Computer Inc.		
Size: Custom	Document Number: S1G2 DDRII MEMORY I/F 2/3	Rev: 1A
Date: Tuesday, February 19, 2008	Sheet 4 of 45	

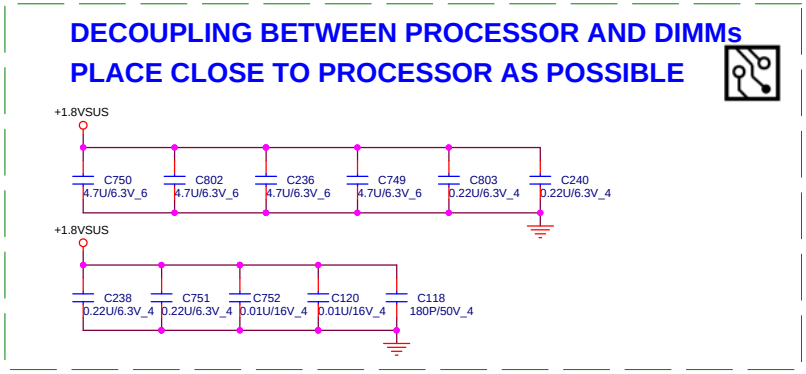
NB5/RD5

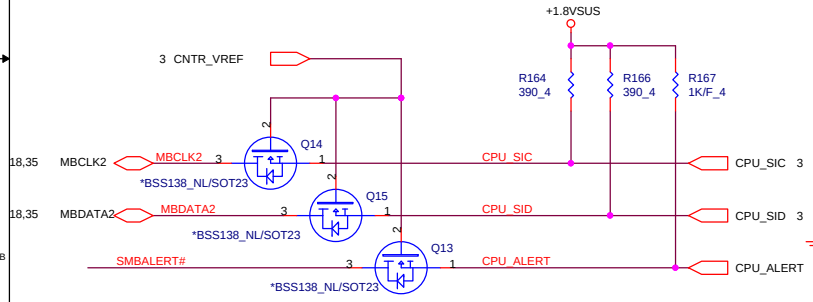
PROCESSOR POWER AND GROUND

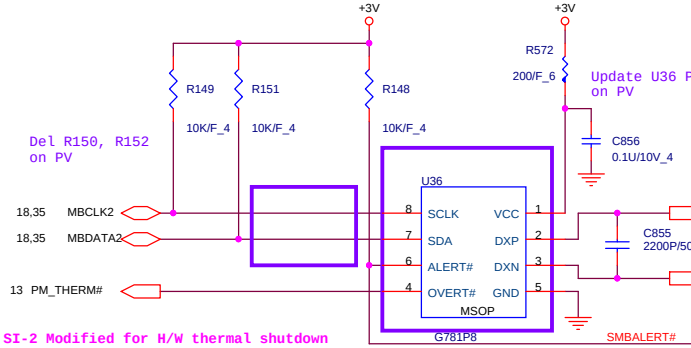


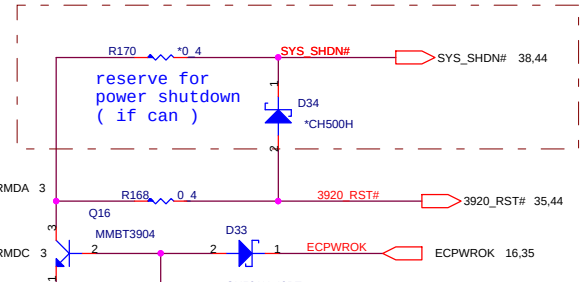


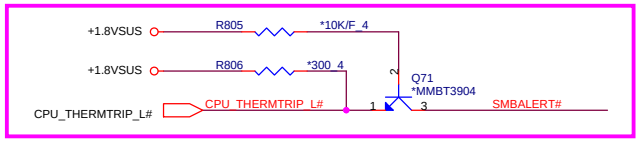


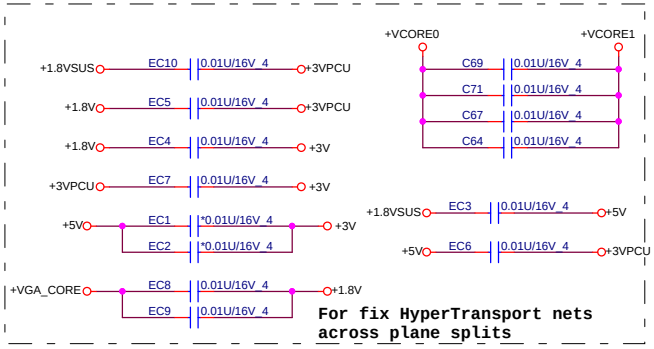


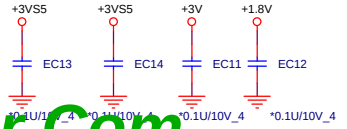












PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	1A

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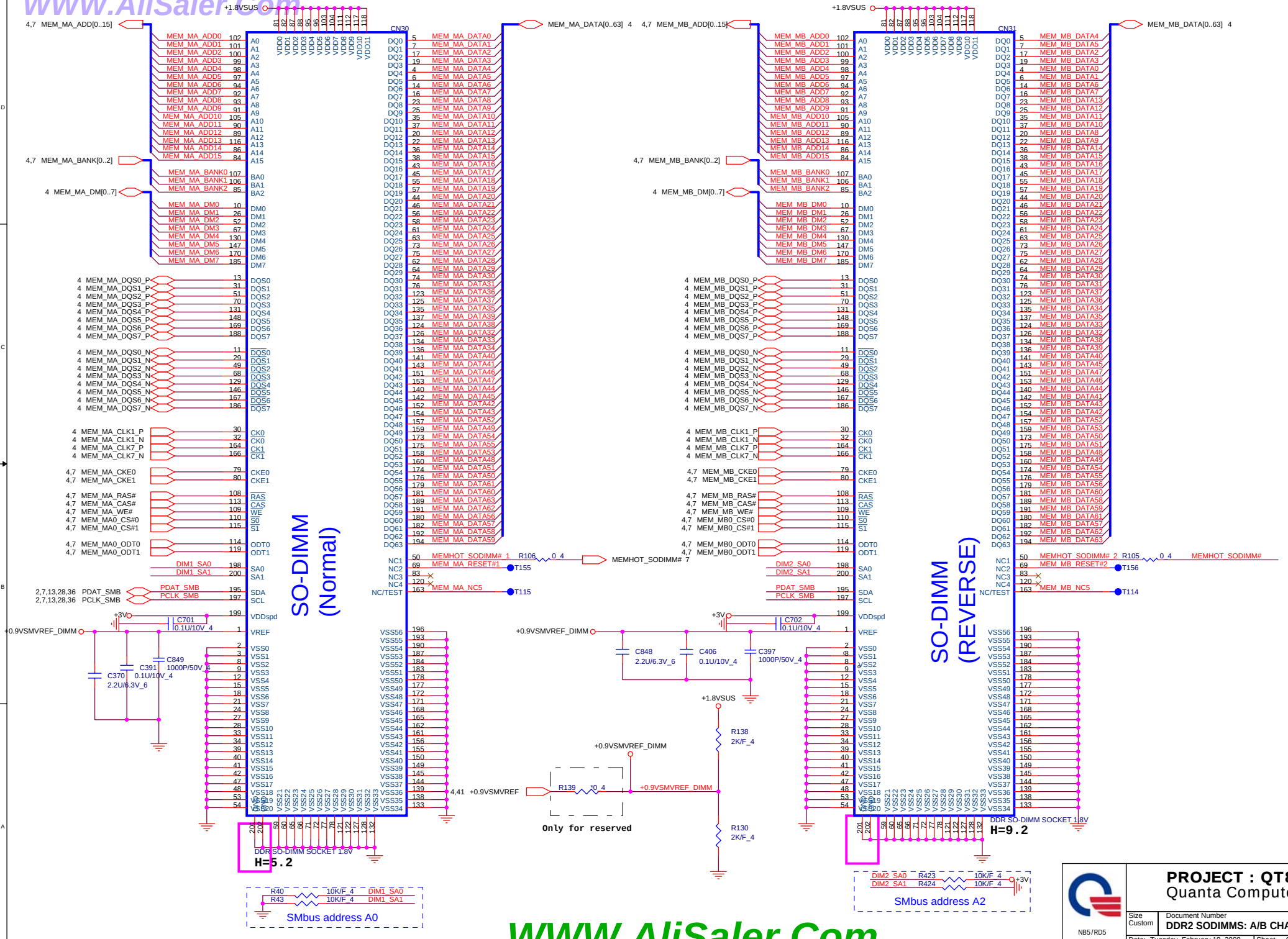
NB5/RD5



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS: A/B CHANNEL	1A

NB5/RD5

Date: Tuesday, February 19, 2008 Sheet 6 of 45

4,6 MEM_MA_ADD[0..15] — MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2] — MEM_MA_BANK[0..2]

4,6 MEM_MB_ADD[0..15] — MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2] — MEM_MB_BANK[0..2]

+0.9VSMVTT

4,6 MEM_MA_CKE0	MEM_MA_CKE0	RP40	47_4P2R_4	C176	0.1U/10V_4	+1.8VSUS	
	MEM_MA_BANK2						
	MEM_MA_ADD12	RP35	47_4P2R_4	C256	0.1U/10V_4		
	MEM_MA_ADD9			C223	0.1U/10V_4	+1.8VSUS	
	MEM_MA_ADD8	RP28	47_4P2R_4	C104	0.1U/10V_4		
	MEM_MA_ADD5			C217	0.1U/10V_4	+1.8VSUS	
	MEM_MA_ADD3	RP26	47_4P2R_4	C96	0.1U/10V_4		
	MEM_MA_ADD1			C152	0.1U/10V_4	+1.8VSUS	
	MEM_MA_ADD10	RP20	47_4P2R_4	C271	0.1U/10V_4		
	MEM_MA_BANK0						
4,6 MEM_MA_WE#	MEM_MA_WE#	RP16	47_4P2R_4	C162	0.1U/10V_4	+1.8VSUS	
4,6 MEM_MA_CAS#	MEM_MA_CAS#			C101	0.1U/10V_4		
4,6 MEM_MA0_ODT1	MEM_MA0_ODT1	RP10	47_4P2R_4	C208	0.1U/10V_4	+1.8VSUS	
4,6 MEM_MA0_CS#1	MEM_MA0_CS#1			C102	0.1U/10V_4		
	MEM_MA_ADD15	RP39	47_4P2R_4	C107	0.1U/10V_4	+1.8VSUS	
4,6 MEM_MA_CKE1	MEM_MA_CKE1			C270	0.1U/10V_4		
	MEM_MA_ADD7	RP33	47_4P2R_4	C146	0.1U/10V_4	+1.8VSUS	
	MEM_MA_ADD14			C269	0.1U/10V_4		
	MEM_MA_ADD6	RP29	47_4P2R_4				
	MEM_MA_ADD11						
	MEM_MA_ADD2	RP24	47_4P2R_4				
	MEM_MA_ADD4						
	MEM_MA_BANK1	RP21	47_4P2R_4				
	MEM_MA_ADD0						
4,6 MEM_MA0_CS#0	MEM_MA0_CS#0	RP14	47_4P2R_4				
4,6 MEM_MA_RAS#	MEM_MA_RAS#						
	MEM_MA_ADD13	RP12	47_4P2R_4				
4,6 MEM_MA0_ODT0	MEM_MA0_ODT0						

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8VSUS — C239 0.1U/10V_4 — C121 0.1U/10V_4 — C241 0.1U/10V_4 — C242 0.1U/10V_4 — C117 0.1U/10V_4 — C235 0.1U/10V_4

PLACE CLOSE TO SOCKET(PER EMI/EMC)

4,6 MEM_MB_CKE0	MEM_MB_CKE0	RP36	47_4P2R_4	C193	0.1U/10V_4	+1.8VSUS	
	MEM_MB_BANK2						
	MEM_MB_ADD12	RP32	47_4P2R_4	C245	0.1U/10V_4		
	MEM_MB_ADD9			C154	0.1U/10V_4	+1.8VSUS	
	MEM_MB_ADD8	RP27	47_4P2R_4	C100	0.1U/10V_4		
	MEM_MB_ADD5			C137	0.1U/10V_4	+1.8VSUS	
	MEM_MB_ADD3	RP25	47_4P2R_4	C94	0.1U/10V_4		
	MEM_MB_ADD1			C190	0.1U/10V_4	+1.8VSUS	
	MEM_MB_ADD10	RP18	47_4P2R_4	C93	0.1U/10V_4		
	MEM_MB_BANK0						
4,6 MEM_MB_WE#	MEM_MB_WE#	RP15	47_4P2R_4	C160	0.1U/10V_4	+1.8VSUS	
4,6 MEM_MB_CAS#	MEM_MB_CAS#			C254	0.1U/10V_4		
4,6 MEM_MB0_ODT1	MEM_MB0_ODT1	RP9	47_4P2R_4	C173	0.1U/10V_4	+1.8VSUS	
4,6 MEM_MB0_CS#1	MEM_MB0_CS#1			C255	0.1U/10V_4		
4,6 MEM_MB_CKE1	MEM_MB_CKE1	RP38	47_4P2R_4	C126	0.1U/10V_4	+1.8VSUS	
	MEM_MB_ADD15			C253	0.1U/10V_4		
	MEM_MB_ADD7	RP34	47_4P2R_4	C178	0.1U/10V_4	+1.8VSUS	
	MEM_MB_ADD14			C105	0.1U/10V_4		
	MEM_MB_ADD6	RP30	47_4P2R_4				
	MEM_MB_ADD11						
	MEM_MB_ADD2	RP22	47_4P2R_4				
	MEM_MB_ADD4						
	MEM_MB_BANK1	RP19	47_4P2R_4				
	MEM_MB_ADD0						
4,6 MEM_MB0_CS#0	MEM_MB0_CS#0	RP13	47_4P2R_4				
4,6 MEM_MB_RAS#	MEM_MB_RAS#						
4,6 MEM_MB0_ODT0	MEM_MB0_ODT0	RP11	47_4P2R_4				
	MEM_MB_ADD13						

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8VSUS — C122 0.1U/10V_4 — C119 0.1U/10V_4 — C237 0.1U/10V_4 — C115 0.1U/10V_4 — C116 0.1U/10V_4 — C745 0.1U/10V_4

PLACE CLOSE TO SOCKET(PER EMI/EMC)

+3VS5 — SI-2 modified --SB internal pull HI to 3vs5

+3V — R421 *10K/F_4

+3VS5 — R417 *10K/F_4 — CPU_MEMHOT# 3,13

Close DDR2 socket

U25 *DS75U+T&R

+3V — A0, A1, A2 — +VS — C706 0.1U/10V_4

O.S — MEMHOT_SODIMM# — R416 — *33_4 — Q32 *2N7002E-G

Q33 *2N7002E-G

2,6,13,28,36 PDAT_SMB — PDAT_SMB — SDA

2,6,13,28,36 PCLK_SMB — PCLK_SMB — SCL

GND

Address:92h

+3V — R422 10K/F_4 MEMHOT_SODIMM# — MEMHOT_SODIMM# 6

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

NB5/RD5

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U32A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS780(RX780)

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1
	C23	HT_RXCALP	HT_TXCALP	B24	HT_TXCALP
	A24	HT_RXCALN	HT_TXCALN	B25	HT_TXCALN

SI-2 modified -- follow AMD check list to change part number 300 ohm to 301 ohm

R655 — R533 301/F_4 — HT_RXCALP, HT_RXCALN

SI-2 modified -- follow AMD check list to change part number 300 ohm to 301 ohm

R641 — R534 301/F_4 — HT_TXCALP, HT_TXCALN

HT_CPU_NB_CAD_H[15..0]	HT_CPU_NB_CAD_H[15..0] 3
HT_CPU_NB_CAD_L[15..0]	HT_CPU_NB_CAD_L[15..0] 3
HT_CPU_NB_CLK_H[1..0]	HT_CPU_NB_CLK_H[1..0] 3
HT_CPU_NB_CLK_L[1..0]	HT_CPU_NB_CLK_L[1..0] 3
HT_CPU_NB_CTL_H[1..0]	HT_CPU_NB_CTL_H[1..0] 3
HT_CPU_NB_CTL_L[1..0]	HT_CPU_NB_CTL_L[1..0] 3
HT_NB_CPU_CAD_H[15..0]	HT_NB_CPU_CAD_H[15..0] 3
HT_NB_CPU_CAD_L[15..0]	HT_NB_CPU_CAD_L[15..0] 3
HT_NB_CPU_CLK_H[1..0]	HT_NB_CPU_CLK_H[1..0] 3
HT_NB_CPU_CLK_L[1..0]	HT_NB_CPU_CLK_L[1..0] 3
HT_NB_CPU_CTL_H[1..0]	HT_NB_CPU_CTL_H[1..0] 3
HT_NB_CPU_CTL_L[1..0]	HT_NB_CPU_CTL_L[1..0] 3

signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14

U27

*HYB18T512161B2F-25

SPM_BA0	L2	BA0	DQ15	B9	SPM_DQ15
SPM_BA1	L3	BA1	DQ14	B1	SPM_DQ14
			DQ13	D9	SPM_DQ9
SPM_A12	R2	A12	DQ12	D1	SPM_DQ12
SPM_A11	P7	A11	DQ11	D3	SPM_DQ8
SPM_A10	M2	A10/AP	DQ10	D7	SPM_DQ10
SPM_A9	P3	A9	DQ9	C2	SPM_DQ13
SPM_A8	P8	A8	DQ8	C8	SPM_DQ11
SPM_A7	P2	A7	DQ7	F9	SPM_DQ5
SPM_A6	N7	A6	DQ6	F1	SPM_DQ3
SPM_A5	N3	A5	DQ5	H9	SPM_DQ4
SPM_A4	N8	A4	DQ4	H1	SPM_DQ1
SPM_A3	N2	A3	DQ3	H3	SPM_DQ0
SPM_A2	M7	A2	DQ2	H7	SPM_DQ7
SPM_A1	M3	A1	DQ1	G2	SPM_DQ2
SPM_A0	M8	A0	DQ0	G8	SPM_DQ6
SPM_CLKN					
R56 *100_4 SPM_CLKP	J8	CK	VDDQ1	A9	+1.8V_MEM_VDDQ
Within 200mils		CK	VDDQ2	C1	
			VDDQ3	C3	
SPM_CKE	K2	CKE	VDDQ4	C7	
			VDDQ5	C9	
			VDDQ6	E9	
SPM_CS#	L8	CS	VDDQ7	G1	
SPM_WE#	K3	WE	VDDQ8	G3	
			VDDQ9	G7	
SPM_RAS#	K7	RAS	VDDQ10	G9	
SPM_CAS#	L7	CAS	VDD1	A1	
			VDD2	E1	L76
SPM_DM0	F3	LDM	VDD3	J9	*BLM18PG181SN1D(180,1.5A)_6
SPM_DM1	B3	UDM	VDD4	M9	
			VDD5	R1	
SPM_ODT	K9	ODT	VDDL	J1	MEM_VDDQ_VDDL
			VSSDL	J7	C757 *1U/10V_4
SPM_DQS0P	F7	LDQS			
SPM_DQS0N	E8	LDQS	VSSQ1	A7	
			VSSQ2	B2	
SPM_DQS1P	B7	UDQS	VSSQ3	B8	
SPM_DQS1N	A8	UDQS	VSSQ4	D2	
			VSSQ5	D8	
SPM_VREF	J2	VREF	VSSQ6	E7	
			VSSQ7	E2	
	A2	NC#A2	VSSQ8	F8	
	E2	NC#E2	VSSQ9	H2	
SPM_BA2	L1	NC#L1	VSSQ10	H8	
	R3	NC#R3	VSS1	A3	
	R7	NC#R7	VSS2	E3	
	R8	NC#R8	VSS3	J3	
			VSS4	N1	
			VSS5	P9	

+1.8V_MEM_VDDQ

C95 *0.1U/10V_4 — R63 *1K_4 — SPM_VREF

C89 *0.1U/10V_4 — R61 *1K_4

This block is for UMA RS780 only , RX780 can remove all component

U32D

PAR 4 OF 6

SBD_MEM/DVO_I/F

RS780(RX780)

SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19	SPM_DQ3
SPM_A4	AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17	SPM_DQ5
SPM_A6	AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15	SPM_DQ6
SPM_A7	AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15	SPM_DQ7
SPM_A8	AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20	SPM_DQ8
SPM_A9	AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19	SPM_DQ9
SPM_A10	AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22	SPM_DQ10
SPM_A11	AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18	SPM_DQ11
SPM_A12	AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20	SPM_DQ12
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22	SPM_DQ13
			MEM_DQ14/DVO_D10(NC)	AC22	SPM_DQ14
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21	SPM_DQ15
SPM_BA1	AE17	MEM_BA1(NC)			
SPM_BA2	AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17	SPM_DQS0P
			MEM_DQS0N/DVO_IDCKN(NC)	W18	SPM_DQS0N
SPM_RAS#	W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20	SPM_DQS1P
SPM_CAS#	Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21	SPM_DQS1N
SPM_WE#	AD18	MEM_WEb(NC)			
SPM_CS#	AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17	SPM_DM0
SPM_CKE	AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19	SPM_DM1
SPM_ODT	V14	MEM_ODT(NC)			
			IOPLLVDD18(NC)	AE23	+1.8_IOPLLVDD18_NB
SPM_CLKP	V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24	+1.1V_IOPLLVDD
SPM_CLKN	W14	MEM_CKN(NC)			
			IOPLLVSS(NC)	AD23	
R502 *40.2/F_4 SPM_COMPP	AE12	MEM_COMPP(NC)			
R501 *40.2/F_4 SPM_COMPN	AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18	SPM_VREF1

+1.8V_MEM_VDDQ

T24

40mils wdith or more

+1.8V_MEM_VDDQ

R487 *0_6

C70 *1U/10V_4 — C738 *10U/6.3V_8 — C76 *10U/6.3V_8

C87 *0.1U/10V_4 — C77 *0.1U/10V_4 — C74 *1U/10V_4

IOPLLVDD18 - memory PLL not applicable to RX780

C762 *2.2U/6.3V_6 — C763 *2.2U/6.3V_6

IOPLLVDD- memory PLL not applicable to RX780

Del L77, L78 for TP on PV

R498 *1K_4 — R497 *1K_4

C775 *0.1U/10V_4 — C774 *0.1U/10V_4 — +1.8V_MEM_VDDQ

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-HT LINK I/F 1/5	1A

NB5/RD5

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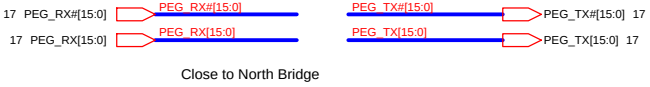
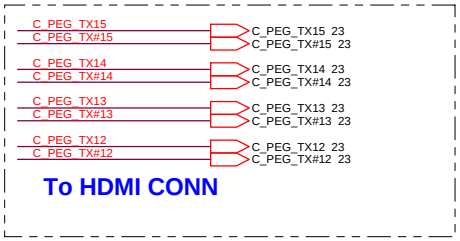


Close to North Bridge



TO EPRESS CARD
TO WLAN
TO PCIE-LAN
TO TV TUNNER

TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-PCIE I/F 2/5	1A

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NB5/RD5

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RX780
3,12 CPU_LDT_RST# — R157 *0_4 — NB_RST# IN
RS780
12 NB_PLTRST# — R160 0_4
North Bridge RESET

R109 for UAM use 140 ohm

U32C — PART 3 OF 6 — RS780(RX780)

CRT/TVOUT
18,24 CRT_R — R446 *0_4, R109 *150/F_4 — CRT_R_1
18,24 CRT_G — R445 0_4, R110 *150/F_4 — CRT_G_1
18,24 CRT_B — R444 0_4, R111 *150/F_4 — CRT_B_1
18,19,24 HSYNC_COM — R549 *0_4 — HSYNC_INT
18,19,24 VSYNC_COM — R540 *0_4 — VSYNC_INT
18,24 DDCDATA — R133 *0_4 — DDCDATA_INT
18,24 DDCCLK — R134 *0_4 — DDCCLK_INT
R119 *715/F_6 — DAC_RSET_NB

PLL PWR
+1.1V_PLLVDD, +1.8V_PLLVDD18
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL

PM
16 NB_PWRGD_IN — NB_RST#_IN, NB_PWRGD_IN, NB_LDT_STOP#, NB_ALLOW_LDTSTOP

CLOCKS
2 NBHT_REFCLKP — NBHT_REFCLKP
2 NBHT_REFCLKN — NBHT_REFCLKN
2 EXT_NB_OSC — R117 0_4 — NB_REFCLK_P, NB_REFCLK_N
+1.1V — R125 4.7K_4, R520 RS780, R120 4.7K_4 — NBGFX_CLKP, NBGFX_CLKN
2 NBGFX_CLKP, 2 NBGFX_CLKN — T168, T169
2 SBLINK_CLKP, 2 SBLINK_CLKN — NBGPP_CLKP, NBGPP_CLKN, SBLINK_CLKP, SBLINK_CLKN
Del NBGPP CLK

I/O
GFX_REFCLKP, GFX_REFCLKN
GPP_REFCLKP, GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP), GPPSB_REFCLKN(SB_REFCLKN)

MIS.
I2C_DATA, I2C_CLK, DDC_DATA/AUX0N(NC), DDC_CLK/AUX0P(NC), AUX1P(NC), AUX1N(NC)
STRP_DATA — 39 DYN_PWR_EN — R27 0_4 STRP_DATA
RSVD — G11
AUX_CAL(NC) — T164 RS780_AUX_CAL — C8

LVTM
TXOUT_L0P(NC) A22 LA_DATAP0 — TXOUT_L0N(NC) B22 LA_DATAN0 — TXOUT_L1P(NC) A21 LA_DATAP1 — TXOUT_L1N(NC) B21 LA_DATAN1 — TXOUT_L2P(NC) B20 LA_DATAP2 — TXOUT_L2N(DBG_GPIO0) A20 LA_DATAN2 — TXOUT_L3P(NC) A19 LA_DATAP3 T159 — TXOUT_L3N(DBG_GPIO2) B19 LA_DATAN3 T157
TXOUT_U0P(NC) B18 LB_DATAP0 — TXOUT_U0N(NC) A18 LB_DATAN0 — TXOUT_U1P(PCIE_RESET_GPIO3) A17 LB_DATAP1 — TXOUT_U1N(PCIE_RESET_GPIO2) B17 LB_DATAN1 — TXOUT_U2P(NC) D20 LB_DATAP2 — TXOUT_U2N(NC) D21 LB_DATAN2 — TXOUT_U3P(PCIE_RESET_GPIO5) D18 LB_DATAP3 T163 — TXOUT_U3N(NC) D19 LB_DATAN3 T160
TXCLK_LP(DBG_GPIO1) B16 LA_CLK — TXCLK_LN(DBG_GPIO3) A16 LA_CLK# — TXCLK_UP(PCIE_RESET_GPIO4) D16 LB_CLK — TXCLK_UN(PCIE_RESET_GPIO1) D17 LB_CLK#
VDDLTP18(NC) A13 +1.8V_VDDLTP18_NB — VSSLTP18(NC) B13
VDDLT18_1(NC) A15 +1.8V_VDDLT_18_NB — VDDLT18_2(NC) B15 — VDDLT33_1(NC) A14 +3V_VDLT33_NB — VDDLT33_2(NC) B14
VSSLT1(VSS) C14 — VSSLT2(VSS) D15 — VSSLT3(VSS) C16 — VSSLT4(VSS) C18 — VSSLT5(VSS) C20 — VSSLT6(VSS) E20 — VSSLT7(VSS) C22
RS780 only
LVDS_DIGON(PCE_TCALRP) E9 — R132 *0_4 — DISP_ON — DISP_ON 19,23
LVDS_BLON(PCE_RCALRP) E7 — R126 *0_4 — LVDS_BLON — LVDS_BLON 18,23
LVDS_ENA_BL(PWM_GPIO2) G12 — R118 *0_4 — DPST_PWM — DPST_PWM 19,23
R121 *1.27K/F_4, R127 *1.27K/F_4 — For RX780 only
TMDS_HPD(NC) D9 TMDS_HPD0 — HPD(NC) D10 TMDS_HPD1 T162 — R545 *0_4 — TMDS_HPD 18,23 — UMA only
TVCLKIN(PWM_GPIO5) D12 — SUS_STAT#_NB R131 0_4 — SUS_STAT# 13
THERMALDIODE_P AE8 R_NB_THRMDA T136 — THERMALDIODE_N AD8 R_NB_THRMDC T135
TESTMODE D13 TEST_EN — R541 1.82K/F_4

RS780 only
+3V — R536 4.7K_4 HDTV_DET — R539 4.7K_4 NB_I2C_DATA — R538 4.7K_4 NB_I2C_CLK
18,23 EDIDDATA — R547 *0_4 — NB_I2C_DATA
18,23 EDIDCLK — R546 *0_4 — NB_I2C_CLK
23 HDMI_DDC_DATA — R537 *0_4 — HDTV_DET
23 HDMI_DDC_CLK — R544 *0_4 — RS740_DFT_GPIO0
T161 — RS740_DFT_GPIO1
T158

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT
RX780
RS780_AUX_CAL — R543 3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780
VSYNC_COM — R124 3K_4 — +3V

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780
HSYNC_COM — R129 3K_4 — +3V, R136 *3K_4

For extrnal EEPROM Debug only
RS780/RX780
STRP_DATA — R548 10K/F_4 — +VDDG_NB, R558 *10K/F_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780
RX780
S-CD1 — R810 *3K_4
Reserved only

RX780 -->NC / RS780 --- ADD

AVDD-DAC Analog not applicable to RX780
+3V — L35 BLM18PG181SN1D(180,1.5A)_6 — +3V_AVDD_NB — C340 2.2U/6.3V_6

PLLVDD - Graphics PLL not applicable to RX780
+1.1V — BLM18PG181SN1D(180,1.5A)_6 L82 — +1.1V_PLLVDD — C842 2.2U/6.3V_6

PLLVDD18 - Graphics PLL not applicable to RX780
+1.8V — L33 BLM18PG181SN1D(180,1.5A)_6 — +1.8V_PLLVDD18 — C405 10U/6.3V_8, C333 2.2U/6.3V_6

AVDDI-DAC Digital not applicable to RX780
+1.8V — R107 0_6 — +1.8V_AVDDDI_NB — C321 2.2U/6.3V_6

AVDDQ-DAC Bandgap Reference not applicable to RX780
BLM18PG181SN1D(180,1.5A)_6 L34 — +1.8V_AVDDQ_NB — C349 2.2U/6.3V_6

VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
+1.8V — BLM18PG181SN1D(180,1.5A)_6 L83 — +1.8V_VDDLTP18_NB — C841 2.2U/6.3V_6

VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780
BLM21PG221SN1D(220,100M,2A)_8 L85 — +1.8V_VDDLT_18_NB — C846 4.7U/6.3V_6, C838 0.1U/10V_4

VDDA18PCIEPLL -PCIE PLL
+1.8V — L32 BLM18PG181SN1D(180,1.5A)_6 — 20mils width +1.8V_VDDA18PCIEPLL — C358 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL
L31 BLM18PG181SN1D(180,1.5A)_6 — 20mils width +1.8V_VDDA18HTPLL — C356 2.2U/6.3V_6

RS780
Q37 BSS138_NL/SOT23 — 3,12 CPU_LDT_STOP# — R555 *0_4 — RX780 — R556 4.7K_4 — +1.8V, +VDDG_NB — NB_LDT_STOP#
Q38 BSS138_NL/SOT23 — 3 CPU_LDT_REQ# — R568 0_4 — NB_ALLOW_LDTSTOP — R557 4.7K_4 — +VDDG_NB

RX780 — R566 *0_6 — +1.8V — +VDDG_NB
RS780 — R565 0_6 — +3V

VDDLT33 - LVDS or DVI/HDMI ANALOG RS740 only
+3V — *BLM21PG221SN1D(220,100M,2A)_8 L84 — +3V_VDLT33_NB — C844 *2.2U/6.3V_6

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-SYSTEM I/F 3/5	1A

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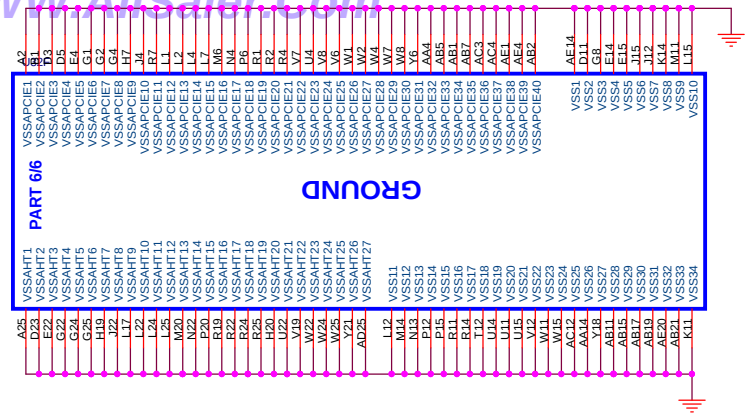
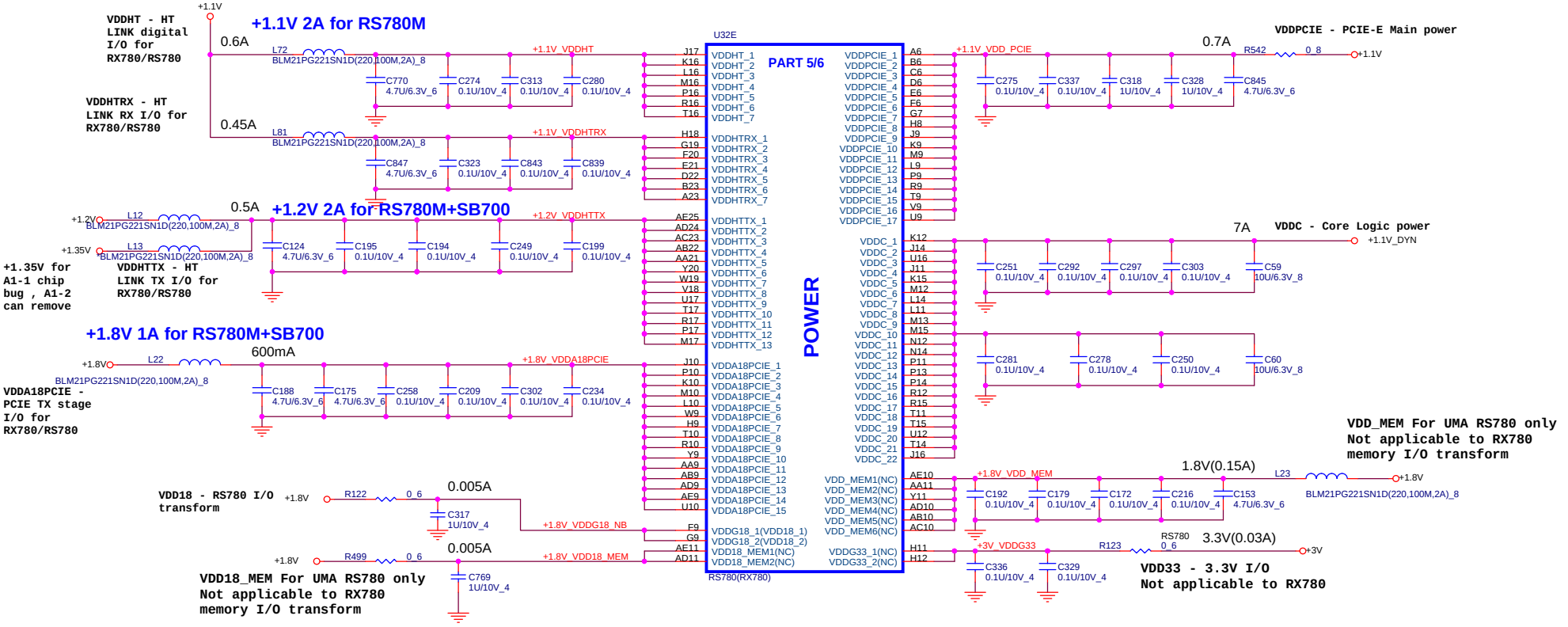
RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC





PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS740/RS780-POWER5/5	1A

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NB5/RD5

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780

10 NB_PLTRST#
17 PCIE_RST#
26 CARD_PLTRST#
31 LAN_PLTRST#
33 EPRESS_PLTRST#
36 MINI_PLTRST#

R250 33_4
R252 33_4
R312 33_4
R251 33_4
R241 33_4
R660 33_4
A_RST#_SB

U37A
SB700
Part 1 of 5
A_RST# N2

9 PCIE_SB_NB_RX0P
9 PCIE_SB_NB_RX0N
9 PCIE_SB_NB_RX1P
9 PCIE_SB_NB_RX1N
9 PCIE_SB_NB_RX2P
9 PCIE_SB_NB_RX2N
9 PCIE_SB_NB_RX3P
9 PCIE_SB_NB_RX3N

C869 0.1U/10V_4 A_RX0P_C
C868 0.1U/10V_4 A_RX0N_C
C865 0.1U/10V_4 A_RX1P_C
C864 0.1U/10V_4 A_RX1N_C
C871 0.1U/10V_4 A_RX2P_C
C870 0.1U/10V_4 A_RX2N_C
C867 0.1U/10V_4 A_RX3P_C
C866 0.1U/10V_4 A_RX3N_C

PCIE_TX0P V23
PCIE_TX0N V22
PCIE_TX1P V24
PCIE_TX1N V25
PCIE_TX2P U25
PCIE_TX2N U24
PCIE_TX3P T23
PCIE_TX3N T22

9 PCIE_NB_SB_TX0P
9 PCIE_NB_SB_TX0N
9 PCIE_NB_SB_TX1P
9 PCIE_NB_SB_TX1N
9 PCIE_NB_SB_TX2P
9 PCIE_NB_SB_TX2N
9 PCIE_NB_SB_TX3P
9 PCIE_NB_SB_TX3N

PCIE_NB_SB_TX0P U22
PCIE_NB_SB_TX0N U21
PCIE_NB_SB_TX1P U19
PCIE_NB_SB_TX1N V19
PCIE_NB_SB_TX2P R20
PCIE_NB_SB_TX2N R21
PCIE_NB_SB_TX3P R18
PCIE_NB_SB_TX3N R17

PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N

R581 562/F_4 PCIE_CALRP_SB T25
R587 2.05K/F_4 PCIE_CALRN_SB T24
+1.2V_PCIE_VDDR
PCIE_CALRP
PCIE_CALRN

+1.2V L44 BLM18PG181SN1D(180,1.5A)_6 +1.2V_PCIE_PVDD P24
40mA
PCIE_PVDD
P25 PCIE_PVSS
C485 10U/6.3V_8
C503 1U/10V_4

PCIE_PVDD-- PCIE PLL POWER

PCI EXPRESS INTERFACE

2 SBSRC_CLKP
2 SBSRC_CLKN
SBSRC_CLKP N25
SBSRC_CLKN N24
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN

K23 NB_DISP_CLKP
K22 NB_DISP_CLKN
M24 NB_HT_CLKP
M25 NB_HT_CLKN
100MHZ
P17 CPU_HT_CLKP
M18 CPU_HT_CLKN
M23 SLT_GFX_CLKP
M22 SLT_GFX_CLKN
J19 GPP_CLK0P
J18 GPP_CLK0N
L20 GPP_CLK1P
L19 GPP_CLK1N
M19 GPP_CLK2P
M20 GPP_CLK2N
N22 GPP_CLK3P
P22 GPP_CLK3N
L18 25M_48M_66M_OSC

RTC_X1
Y8
32.768KHZ
R632 *20M_6
R626 20M_6
RTC_X2
C900 18P/50V_4
C899 18P/50V_4

R257 0_4
J21 25M_X1
T74
J20 25M_X2

CLOCK GENERATOR

If CPU have pull Hi ,this
pin should be not need

RTC_X1 A3 X1
RTC_X2 B3 X2
RTC XTAL

PV-1
Modified
-- change
to pull hi
to 3VS5
for power
leakage
issue

+1.8V R232 *10K/F_4
+3VS5 R588 10K/F_4

10 ALLOW_LDTSTOP
3 CPU_PROCHOT#
3 CPU_PWRGD
3,10 CPU_LDT_STOP#
3,10 CPU_LDT_RST#

ALLOW_LDTSTOP F23
CPU_PROCHOT# F24
CPU_PWRGD F22
CPU_LDT_STOP# G25
CPU_LDT_RST# G24

ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
CPU

SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00

PCI CLKS

PCICLK0 P4
PCICLK1 P3
PCICLK2 P1
PCICLK3 P2
PCICLK4 T4
PCICLK5/GPIO41 T3

Del R639, R640, R641, R642 on PV

T108
T214
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
PCI_CLK_TPM 16
PCI_CLK3 16
PCI_CLK4 16
PCI_CLK5 16

PCIRST# N1 PCIRST#_L R643 33_4 PCIRST#
PCIRST# 35

AD0 U2
AD1 P7
AD2 V4
AD3 T1
AD4 V3
AD5 U1
AD6 V1
AD7 V2
AD8 T2
AD9 W1
AD10 T9
AD11 R6
AD12 R7
AD13 R5
AD14 U8
AD15 U5
AD16 Y7
AD17 W8
AD18 V9
AD19 Y8
AD20 AA8
AD21 Y4
AD22 Y3
AD23 Y2
AD24 AA2
AD25 AB4
AD26 AA1
AD27 AB3
AD28 AB2
AC1
AC2
AD1
W2
U7
AA7
Y1
AA6
W5
AA5
Y5
U6
W6
W4
V7 SERR#
AC3
AD4
AB7
AE6
AB6
AD2
AE4
AD5
AC6
AE5
AD6
V5
AD3 INTE#
AC4 INTF#
AE2 INTG#
AE3 INTH#

+3V
PE_GPIO1 R294 8.2K_4
R299 *8.2K_4
SB_GPIO65 R274 *100K/F_4
R809 8.2K_4 +3V

AD23 AD23 16
AD24 AD24 16
AD25 AD25 16
AD26 AD26 16
AD27 AD27 16
AD28 AD28 16

change D21, D20 type for PV

All the PCI bus has
build-in Pull-UP/Down
resistors

+AVBAT
20MIL
SI-2 mofified for satify --
remove R560 , add R796 ,R797
R796 499/F_4 +3VRTC_1 R797 10_4 +3VRTC
20MIL 20MIL
D21 RB500V-40
D20 RB500V-40
+3VPCU
+VCCRTC_2
20MIL
R298 0_4
+BAT
20MIL
BT1
BAT_CONN
C906 1U/10V_4
C907 1U/10V_4

SERR# SERR# 35
SI-2 Modified-- for power leakage issue
Del R783 for
TP on PV
R187 0_4
RF_OFF# 36
D3E GPIO# 26
SI-2 Modified-- Add GPIO pin for control D3E wake up (need low 1ms
for Jmicron request)
PE_GPIO1
R631 0_4 LCD_BK 23
R629 0_4 CLKRUN# 35
CLKRUN#_R
T94
T213
T110
T217
INTH# 28
R589 change to 10 ohm on PV

PCI INTERFACE

INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
REQ0#
REQ1#
REQ2#
REQ3#/GPIO70
REQ4#/GPIO71

LPC

LPCCLK0 G22 LPC_CLK0
LPCCLK1 E22 LPC_CLK1
R243 22_4
R589 10_4
LPC_CLK0 16
LPC_CLK1 16
PCLK_LPC_DEBUG 36
PCLK_LPC_KB3920 35
LAD0 H24
LAD1 H23
LAD2 J25
LAD3 J24
LFRAME# H25
LDRQ0# H22
LDRQ1#/GNT5#/GPIO68 AB8
BMREQ#/REQ5#/GPIO65 AD7
SERIRQ V15
LAD0 35,36
LAD1 35,36
LAD2 35,36
LAD3 35,36
LFRAME# 35,36
LDRQ0#_SB
LDRQ1#_SB
SB_GPIO65
SERIRQ
T61
T90
T107
SERIRQ 35
C940 5.6P/50V_6
C939 22P/50V_4
SI-2
modified
-- for EMI
suggestion
SI-1 Modified - for EMI

RTC

RTCCLK C3 RTC_CLK
INTRUDER_ALERT# C2 INTRUDER_ALERT#
VBAT B2 +AVBAT
RTC_CLK 16
R782 *1M/F_4 +AVBAT
SI-2 Modified--reserve
20MIL
G3 *SHORT_PAD1
C902 0.1U/10V_4
INTRUDER_ALERT# Left not connected (Southbridge
has 50-kohm internal pull-up to VBAT).

PROJECT : QT8
Quanta Computer Inc.
NB5/RD5
Size Custom
Document Number SB700-PCIE/PCI/CPU/LPC 1/4
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NC only ,Can't be install

+3VSUS R297 *2.2K_4 SB_TEST0
R240 *2.2K_4 SB_TEST1
R287 *2.2K_4 SB_TEST2

+3VSUS R289 *10K/F_4 SWI#

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R245 2.2K_4 PCLK_SMB
R253 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner
/DDR2/DDR2
thermal/Accelerometer

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R648 *2.2K_4 SB_SMBCLK1
R649 *2.2K_4 SB_SMBDATA1

remove pull hi
(chip internal
have pull hi)

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R222 *2.2K_4 SB_SCLK2
R227 *2.2K_4 SB_SDATA2

+3V R276 4.7K_4 SUS_STAT#
G4
2 1 SYS_RST#
*SHORT_ PAD1

+3VS5 R763 2.2K_4 DNBSWON#

SI-2 modified add D3E function

SI-2 modified -- Change lan disable control from SB to EC SB reserve

D3E_SCI# from Gevent5# change to Gevent7# on PV

SI-2 modified Del D35

HD audio interface is 3.3S5 voltage

SI-2 Modified --for EMI suggestion

SI-2 Modified -- discrete remove RP56

U37D

SB700 Part 4 of 5

33 NEWCARD_DETECT	NEWCARD_DETECT	E1 PCI_PME#/GEVENT4#
T211	RI#	E2 RI#/EXTEVNT0#
T99	SLP_S2	H7 SLP_S2/GPM9#
35 SUSB# R271 *0_4	SUSB#	F5 SLP_S3#
35 SUSC# R191 *0_4	SUSC#	G1 SLP_S5#
35 DNBSWON# R233 *0_4	DNBSWON#	H2 PWR_BTN#
16 SB_PWRGD_IN	SB_PWRGD_IN	H1 PWR_GOOD
10 SUS_STAT#	SUS_STAT#	K3 SUS_STAT#
	SB_TEST2	H5 TEST2
	SB_TEST1	H4 TEST1
	SB_TEST0	H3 TEST0
35 GATEA20	GATEA20	Y15 GA20IN/GEVENT0#
35 RCIN#	RCIN#	W15 KBRST#/GEVENT1#
35 SCI#	SCI#	K4 LPC_PME#/GEVENT3#
35 KBSMI#	KBSMI#	K24 LPC_SMI#/EXTEVNT1#
T109	GEVENT5#	F1 S3_STATE/GEVENT5#
	SYS_RST#	J2 SYS_RESET#/GPM7#
31,33,36 PCIE_WAKE#	PCIE_WAKE#	H6 WAKE#/GEVENT8#
35 SWI# R211 *0_4	SWI#	F2 BLINK/GPM6#
3 CPU_THERMTRIP# R786 0_4	SB_THERMTRIP#	J6 SMBALERT#/THRMTRIP#/GEVENT2#
16 WD_PWRGD	WD_PWRGD	W14 NB_PWRGD
35 RSMRST# R284 *0_4	RSMRST#	D3 RSMRST#
T63	SATA_IS1	AE18 SATA_IS0#/GPIO10
T194	LAN_DISABLE# SB	AD18 CLK_REQ3#/SATA_IS1#/GPIO6
31,35 LAN_DISABLE# R217 *0_4		AA19 SMARTVOLT/SATA_IS2#/GPIO4
	SB_NWD_CLK_REQ#	W17 CLK_REQ0#/SATA_IS3#/GPIO0
T222		Y17 CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
		W20 CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
27,28 ACZ_SPKR R302 *0_4	ACZ_SPKR	W21 SPKR/GPIO2
2,6,7,28,36 PCLK_SMB	PCLK_SMB	AA18 SCL0/GPOC0#
2,6,7,28,36 PDAT_SMB	PDAT_SMB	W18 SDA0/GPOC1#
	SB_SMBCLK1	K1 SCL1/GPOC2#
	SB_SMBDATA1	K2 SDA1/GPOC3#
T69		AA20 DDC1_SCL/GPIO9
T75		Y18 DDC1_SDA/GPIO8
35 PM_BATLOW#	PM_BATLOW#	C1 LLB#/GPIO66
T72	SES_INT	Y19 SHUTDOWN#/GPIO5
26 D3E_SCI#		G5 DDR3_RST#/GEVENT7#
3,7 CPU_MEMHOT#	CPU_MEMHOT# IN	B9 USB_OC6#/IR_TX1/GEVENT6#
5 PM_THERM# R275 *0_4	SMBALERT# 1	B8 USB_OC5#/IR_TX0/GPM5#
+3VS5 R279 *10K/F_4		A8 USB_OC4#/IR_RX0/GPM4#
	SB_JTAG_TDO	A9 USB_OC3#/IR_RX1/GPM3#
	SB_JTAG_TCK	E5 USB_OC2#/GPM2#
	SB_JTAG_TDI	F8 USB_OC1/GPM1#
	SB_JTAG_RST#	E4 USB_OC0#/GPM0#
ACZ_BCLK		M1 AZ_BITCLK
ACZ_SDOUT		M2 AZ_SDOUT
ACZ_SDIN0_R		J7 AZ_SDIN0/GPIO42
ACZ_SDIN1_R		J8 AZ_SDIN1/GPIO43
T98		L8 AZ_SDIN2/GPIO44
T209		M3 AZ_SDIN3/GPIO46
ACZ_SYNC		L6 AZ_SYNC
16 ACZ_RST#	ACZ_RST#	M4 AZ_RST#
		L5 AZ_DOCK_RST#/GPM8#
+3VS5 R592 22K_4	HDD_AUX_RST#	H19 IMC_GPIO0
		H20 IMC_GPIO1
		H21 SPI_CS2#/IMC_GPIO2
		F25 IDE_RST#/F_RST#/IMC_GPO3
		D22 IMC_GPIO4
		E24 IMC_GPIO5
		E25 IMC_GPIO6
		D23 IMC_GPIO7

USB MISC
USB 1.1
USB 2.0
ACPI / WAKE UP EVENTS
GPIO
USB OC
HD AUDIO
INTEGRATED uC

	USBCLK/14M_25M_48M_OSC	C8 CLK_48M_USB
	USB_RCOMP	G8 USB_RCOMP_SB R267 11.8K/F_6
USB_FSD13P	USB_FSD13P	E6 USB_FSD13P
USB_FSD13N	USB_FSD13N	E7 USB_FSD13N
USB_FSD12P	USB_FSD12P	F7 USB_FSD12P
USB_FSD12N	USB_FSD12N	E8 USB_FSD12N
USB_HSD11P	USBP11+	H11
USB_HSD11N	USBP11-	J10
USB_HSD10P	USBP10+	E11
USB_HSD10N	USBP10-	F11
USB_HSD9P	USBP9+	A11
USB_HSD9N	USBP9-	B11
USB_HSD8P	USBP8+	C10
USB_HSD8N	USBP8-	D10
USB_HSD7P	USBP7+	G11
USB_HSD7N	USBP7-	H12
USB_HSD6P	USBP6+	E12
USB_HSD6N	USBP6-	E14
USB_HSD5P	USBP5+	C12
USB_HSD5N	USBP5-	D12
USB_HSD4P	USBP4+	B12
USB_HSD4N	USBP4-	A12
USB_HSD3P	USBP3+	G12
USB_HSD3N	USBP3-	G14
USB_HSD2P	USBP2+	H14
USB_HSD2N	USBP2-	H15
USB_HSD1P	USBP1+	A13
USB_HSD1N	USBP1-	B13
USB_HSD0P	USBP0+	B14
USB_HSD0N	USBP0-	A14

USBP11+ 36 / USBP11- 36 TV Min-Card
USBP10+ 36 / USBP10- 36 WLAN Min-Card
USBP9+ 30 / USBP9- 30 USB Connector
USBP8+ 30 / USBP8- 30 USB Connector
USBP7+ 33 / USBP7- 33 NEW CARD
USBP6+ 30 / USBP6- 30 FINGERPRINT
USBP5+ 30 / USBP5- 30 BLUETOOTH
USBP4+ 37 / USBP4- 37 Docking
USBP3+ / USBP3- USB card reader or Touch screen
USBP2+ 30 / USBP2- 30 Carama USB
USBP1+ 30 / USBP1- 30 E-SATA and USB Connector
USBP0+ 30 / USBP0- 30 USB Connector

CLK_48M_USB C554 *2.2P/50V_4

for EMI & del R268 change 2.2P

IMC_GPIO8		A18
IMC_GPIO9		B18
IMC_PWM0/IMC_GPIO10		F21
SCL2/IMC_GPIO11	SB_SCLK2	D21
SDA2/IMC_GPIO12	SB_SDATA2	F19
SCL3_LV/IMC_GPIO13	SB_SCLK3	E20 T64
SDA3_LV/IMC_GPIO14	SB_SDATA3	F21 T70
IMC_PWM1/IMC_GPIO15		E19
IMC_PWM2/IMC_GPO16	SB_GPIO16	D19 SB_GPIO16 16
IMC_PWM3/IMC_GPO17	SB_GPIO17	E18 SB_GPIO17 16 SPI/LPC define
IMC_GPIO18		G20
IMC_GPIO19		G21
IMC_GPIO20		D25
IMC_GPIO21		D24
IMC_GPIO22		C25
IMC_GPIO23		C24
IMC_GPIO24		B25
IMC_GPIO25		C23
IMC_GPIO26		B24
IMC_GPIO27		B23
IMC_GPIO28		A23
IMC_GPIO29		C22
IMC_GPIO30		A22
IMC_GPIO31		B22
IMC_GPIO32		B21
IMC_GPIO33		A21
IMC_GPIO34		D20
IMC_GPIO35		C20
IMC_GPIO36		A20
IMC_GPIO37		B20
IMC_GPIO38		B19
IMC_GPIO39		A19
IMC_GPIO40		D18
IMC_GPIO41		C18

+3VS5 R764 2K/04 +3V
33,36 SCLK_WLAN 3 Q66 1 PCLK_SMB
2N7002EPT

+3VS5 R765 2K/04 +3V
33,36 SDATA_WLAN 3 1 PDAT_SMB
2N7002EPT Q67

To Azalia

ACZ_SDOUT	R644 33_4	C908 *10P/50V_4	ACZ_SDOUT_AUDIO 27
ACZ_SYNC	R290 33_4	C569 *10P/50V_4	ACZ_SYNC_AUDIO 27
ACZ_BCLK	R646 33_4	C910 10P/50V_4	BIT_CLK_AUDIO 27
ACZ_RST#	R296 33_4		ACZ_RST#_AUDIO 27
ACZ_SDIN0_R	R295 0_4		ACZ_SDIN0 27

To Modem Board

ACZ_SDOUT	R645 33_4	C909 *10P/50V_4	ACZ_SDOUT_AUDIO_MDC 29
ACZ_SYNC	R292 33_4	C577 *10P/50V_4	ACZ_SYNC_AUDIO_MDC 29
ACZ_BCLK	R647 33_4	C911 10P/50V_4	BIT_CLK_AUDIO_MDC 29
ACZ_RST#	R293 33_4		ACZ_RST#_AUDIO_MDC 29
ACZ_SDIN1_R	R286 0_4		ACZ_SDIN1 29

SB JTAG

CN16 +3VSUS C462 10P/50V_4
1 SB_JTAG_TCK
2 SB_JTAG_TDO
3 SB_JTAG_TDI
4 SB_TEST1
5
6 SB_JTAG_RST#
7
8
*S/W JTAG DEBUG

USBP3- USBP3+ RP50 *0_4P2R_4 USBP6_CR- 25 USBP6_CR+ 25
CLOSE TO SB
UMA

PROJECT : QT8			
Quanta Computer Inc.			
Size: Custom	Document Number: SB700-ACPI/GPIO/USB 2/4		Rev: 1A
NB5/RD5	Date: Tuesday, February 19, 2008	Sheet 13 of 45	

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SATA1

SATA ODD

E-SATA

SATA PORT 4,5 are only support IDE mode

U37B

SB700

Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:

R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

Del R220 for TP on PV

Del WAN off# and R597 on PV

SI-2 modified -- SB internal pull Hi to 3VS5 , modified to same power rail with SB

SI-2 modified -- for fix +3V power leakage in S5 mode

AVDD--H/W monitor Analog power

SI-2 modified for SATA LED fail issue

Place near ball

ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

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Del R285 for TP on PV

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove

POWER

SB700 Part 3 of 5

U37C

VDDQ--3.3V I/O power — 0.8A

+3V → C576 100U/6.3V_3528 → C557 10U/6.3V_8, C560 1U/10V_4, C573 1U/10V_4, C565 1U/10V_4, C547 1U/10V_4, C553 1U/10V_4, C574 1U/10V_4

VDDQ_1 L9, VDDQ_2 M9, VDDQ_3 T15, VDDQ_4 U9, VDDQ_5 U16, VDDQ_6 U17, VDDQ_7 V8, VDDQ_8 W7, VDDQ_9 Y6, VDDQ_10 AA4, VDDQ_11 AB5, VDDQ_12 AB21 — PCI/GPIO I/O

VDD-- S/B CORE power — 604mA

+1.2V_VCC_SB_R → R590 *0_8 → +1.2V_S5

VDD_1 L15, VDD_2 M12, VDD_3 M14, VDD_4 N13, VDD_5 P12, VDD_6 P14, VDD_7 R11, VDD_8 R15, VDD_9 T16 — CORE S0

C533 1U/10V_4, C545 1U/10V_4, C538 1U/10V_4, C532 1U/10V_4, C467 10U/6.3V_8

R198 0_8 → +1.2V

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power / 1.8V flash memory I/O power — 0.45A

+3V → R226 0_8 → +VDD33_18
+1.8V → R751 *0_8 → +VDD33_18

C486 10U/6.3V_8, C501 1U/10V_4, C487 1U/10V_4, C497 1U/10V_4, C488 1U/10V_4

VDD33_18_1 Y20, VDD33_18_2 AA21, VDD33_18_3 AA22, VDD33_18_4 AE25 — IDE/FLSH I/O

CKVDD_1.2V-- Internal clock Generator I/O power — 286mA

+1.2V_CKVDD → C505 2.2U/6.3V_6, C489 0.1U/50V_6, C475 0.1U/50V_6, C478 2.2U/6.3V_6 → L43 BLM18PG181SN1D(180,1.5A)_6 → +1.2V

CKVDD_1.2V_1 L21, CKVDD_1.2V_2 L22, CKVDD_1.2V_3 L24, CKVDD_1.2V_4 L25 — CLKGEN I/O

PCIE_VDDR--PCIE I/O power — 844mA

+1.2V → L89 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_PCIE_VDDR
C477 10U/6.3V_8, C502 1U/10V_4, C484 1U/10V_4, C504 1U/10V_4, C492 1U/10V_4, C483 1U/10V_4

PCIE_VDDR_1 P18, PCIE_VDDR_2 P19, PCIE_VDDR_3 P20, PCIE_VDDR_4 P21, PCIE_VDDR_5 R22, PCIE_VDDR_6 R24, PCIE_VDDR_7 R25 — A-LINK I/O

S5_3.3--3.3v standby power — 0.01A

+3VALW_R → R604 0_6 (Change to 0603) → +3VS5
C875 0.1U/10V_4, C570 0.1U/10V_4, C876 10U/6.3V_8

S5_3.3V_1 A17, S5_3.3V_2 A24, S5_3.3V_3 B17, S5_3.3V_4 J4, S5_3.3V_5 J5, S5_3.3V_6 L1, S5_3.3V_7 L2 — 3.3V_S5 I/O

S5_1.2V--1.2V standby power — 0.22A

S5_1.2V_1 G2, S5_1.2V_2 G4 — CORE S5 → +1.2V_S5
C903 0.1U/10V_4, C901 0.1U/10V_4

Del R661 for TP on PV

AVDD_SATA--SATA phy power — 0.2A

+1.2V → L92 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_AVDD_SATA
C888 10U/6.3V_8, C880 0.1U/10V_4, C884 0.1U/10V_4, C883 1U/10V_4, C881 1U/10V_4

AVDD_SATA_1 AA14, AVDD_SATA_4 AB18, AVDD_SATA_2 AA15, AVDD_SATA_3 AA17, AVDD_SATA_5 AC18, AVDD_SATA_6 AD17, AVDD_SATA_7 AE17 — SATA I/O

0.2A

USB_PHY_1.2V_1 A10, USB_PHY_1.2V_2 B10 — CORE S5 → +1.2V_USB_PHY_R

For support USB wakeup-->3V_S5 / AVDDTX--USB Phy Analog I/O power — 0.2A

+3VS5 → L91 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDD_USB
C889 10U/6.3V_8, C882 10U/6.3V_8, C878 0.1U/10V_4, C886 0.1U/10V_4
C528 1U/10V_4, C537 1U/10V_4, C885 1U/10V_4, C511 0.1U/10V_4, C510 0.1U/10V_4, C879 0.1U/10V_4, C536 0.1U/10V_4

AVDDTX_0 A16, AVDDTX_1 B16, AVDDTX_2 C16, AVDDTX_3 D16, AVDDTX_4 D17, AVDDTX_5 E17, AVDDRX_0 F15, AVDDRX_1 F17, AVDDRX_2 F18, AVDDRX_3 G15, AVDDRX_4 G17, AVDDRX_5 G18 — USB I/O

V5_VREF--PCI 5V TOLERANCE — 4mA

+5V_VREF → R621 1K/F_4 → +5V
D36 CH501H-40PT → +3V
C898 1U/10V_4

V5_VREF AE7

PLL

AVDDCK_3.3V J16 → +3V_AVDDCK — 7mA
AVDDCK_1.2V K17 → +1.2V_AVDDCK — 44mA
AVDDC E9 → +3V_AVDDC — 16mA

USB_PHY_1.2V--USB Phy digital power

+1.2V_S5 → R616 0_6 → +1.2V_USB_PHY_R
C890 0.1U/10V_4, C891 0.1U/10V_4, C892 10U/6.3V_8

AVDDC--USB Analog PLL power

+3VS5 → L50 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDC
C546 0.1U/10V_4, C540 10U/6.3V_8

AVDDCK_1.2--USB Phy digital power

+1.2V → L45 BLM18PG181SN1D(180,1.5A)_6 → +1.2V_AVDDCK
C509 2.2U/6.3V_6

AVDDCK_3.3--Analog system PLL power

+3V → L48 BLM18PG181SN1D(180,1.5A)_6 → +3V_AVDDCK
C516 2.2U/6.3V_6

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U37E

AVSS_SATA_1 T10, AVSS_SATA_2 U10, AVSS_SATA_3 U11, AVSS_SATA_4 U12, AVSS_SATA_5 V11, AVSS_SATA_6 V14, AVSS_SATA_7 W9, AVSS_SATA_8 Y9, AVSS_SATA_9 Y11, AVSS_SATA_10 Y14, AVSS_SATA_11 Y17, AVSS_SATA_12 AA9, AVSS_SATA_13 AB9, AVSS_SATA_14 AB11, AVSS_SATA_15 AB13, AVSS_SATA_16 AB15, AVSS_SATA_17 AB17, AVSS_SATA_18 AC8, AVSS_SATA_19 AD8, AVSS_SATA_20 AE8

AVSS_USB_1 A15, AVSS_USB_2 B15, AVSS_USB_3 C14, AVSS_USB_4 D8, AVSS_USB_5 D9, AVSS_USB_6 D11, AVSS_USB_7 D13, AVSS_USB_8 D14, AVSS_USB_9 D15, AVSS_USB_10 E15, AVSS_USB_11 F12, AVSS_USB_12 F14, AVSS_USB_13 G9, AVSS_USB_14 H9, AVSS_USB_15 H17, AVSS_USB_16 J9, AVSS_USB_17 J11, AVSS_USB_18 J12, AVSS_USB_19 J14, AVSS_USB_20 J15, AVSS_USB_21 K10, AVSS_USB_22 K12, AVSS_USB_23 K14, AVSS_USB_24 K15

PCIE_CK_VSS_1 H18, PCIE_CK_VSS_2 J17, PCIE_CK_VSS_3 J22, PCIE_CK_VSS_4 K25, PCIE_CK_VSS_5 M16, PCIE_CK_VSS_6 M17, PCIE_CK_VSS_7 M21, PCIE_CK_VSS_8 P16

AVSSC F9, AVSSCK L17

VSS_1 A2, VSS_2 A25, VSS_3 B1, VSS_4 D7, VSS_5 F20, VSS_6 G19, VSS_7 H8, VSS_8 K9, VSS_9 K11, VSS_10 K16, VSS_11 L4, VSS_12 L7, VSS_13 L10, VSS_14 L11, VSS_15 L12, VSS_16 L14, VSS_17 L16, VSS_18 M6, VSS_19 M10, VSS_20 M11, VSS_21 M13, VSS_22 M15, VSS_23 N4, VSS_24 N12, VSS_25 N14, VSS_26 P6, VSS_27 P9, VSS_28 P10, VSS_29 P11, VSS_30 P13, VSS_31 P15, VSS_32 R1, VSS_33 R2, VSS_34 R4, VSS_35 R9, VSS_36 R10, VSS_37 R12, VSS_38 R14, VSS_39 T11, VSS_40 T12, VSS_41 T14, VSS_42 U4, VSS_43 U14, VSS_44 V6, VSS_45 Y21, VSS_46 AB1, VSS_47 AB19, VSS_48 AB25, VSS_49 AE1, VSS_50 AE24

PCIE_CK_VSS_9 P23, PCIE_CK_VSS_10 R16, PCIE_CK_VSS_11 R19, PCIE_CK_VSS_12 T17, PCIE_CK_VSS_13 U18, PCIE_CK_VSS_14 U20, PCIE_CK_VSS_15 V18, PCIE_CK_VSS_16 V20, PCIE_CK_VSS_17 V21, PCIE_CK_VSS_18 W19, PCIE_CK_VSS_19 W22, PCIE_CK_VSS_20 W24, PCIE_CK_VSS_21 W25

GROUND

Part 5 of 5

SB700

Size: Custom	Document Number: SB700-PWR/DECOUPLING 4/4		Rev: 1A
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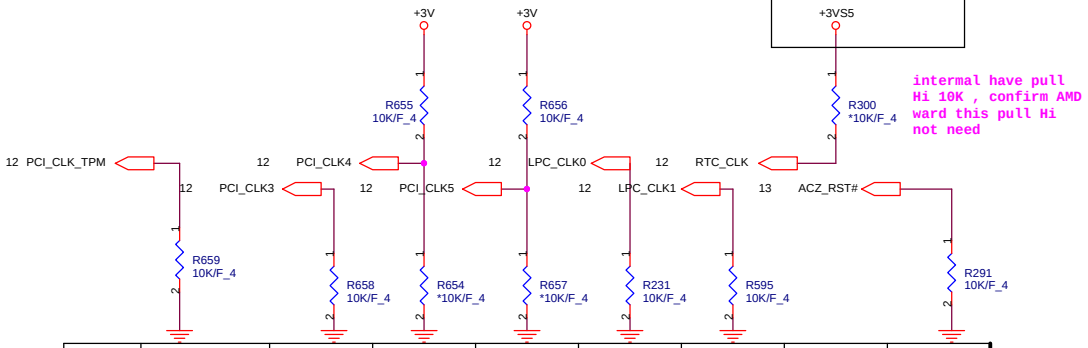
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

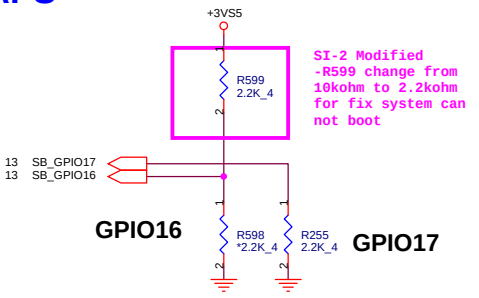
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#

REQUIRED STRAPS



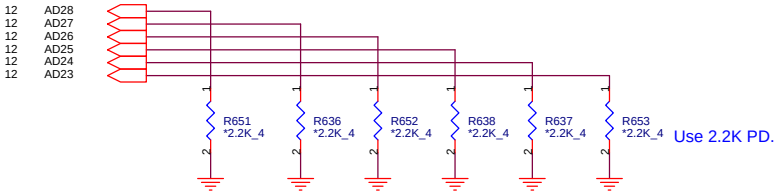
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

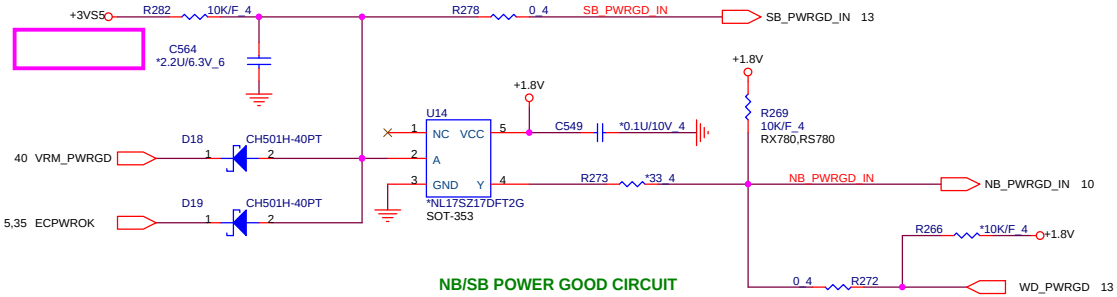


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff

SI-2 modified -- remove +3V pull Hi resistor .



NB/SB POWER GOOD CIRCUIT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

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Custom	SB700-STRAPS	1A

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IC CTRL(632P) 216-0707001-00(BGA)
VGA P/N : AJ070700T00

2.5Gb/s bit rate

PART 1 OF 6

PCI-EXPRESS INTERFACE

9 PEG_TX0	PEG_TX0	AC30	PCIE_RX0P	PCIE_TX0P	AA28	C_PEG_RXP0	C163	0.1U/10V_4	PEG_RX0 9
9 PEG_TX#0	PEG_TX#0	AC31	PCIE_RX0N	PCIE_TX0N	AA27	C_PEG_RXN0	C156	0.1U/10V_4	PEG_RX#0 9
9 PEG_TX1	PEG_TX1	AC29	PCIE_RX1P	PCIE_TX1P	AA25	C_PEG_RXP1	C167	0.1U/10V_4	PEG_RX1 9
9 PEG_TX#1	PEG_TX#1	AB29	PCIE_RX1N	PCIE_TX1N	AA24	C_PEG_RXN1	C170	0.1U/10V_4	PEG_RX#1 9
9 PEG_TX2	PEG_TX2	AB31	PCIE_RX2P	PCIE_TX2P	Y28	C_PEG_RXP2	C180	0.1U/10V_4	PEG_RX2 9
9 PEG_TX#2	PEG_TX#2	AB30	PCIE_RX2N	PCIE_TX2N	Y27	C_PEG_RXN2	C196	0.1U/10V_4	PEG_RX#2 9
9 PEG_TX3	PEG_TX3	AA31	PCIE_RX3P	PCIE_TX3P	Y25	C_PEG_RXP3	C164	0.1U/10V_4	PEG_RX3 9
9 PEG_TX#3	PEG_TX#3	AA30	PCIE_RX3N	PCIE_TX3N	Y24	C_PEG_RXN3	C157	0.1U/10V_4	PEG_RX#3 9
9 PEG_TX4	PEG_TX4	W30	PCIE_RX4P	PCIE_TX4P	V28	C_PEG_RXP4	C218	0.1U/10V_4	PEG_RX4 9
9 PEG_TX#4	PEG_TX#4	W31	PCIE_RX4N	PCIE_TX4N	V27	C_PEG_RXN4	C204	0.1U/10V_4	PEG_RX#4 9
9 PEG_TX5	PEG_TX5	W29	PCIE_RX5P	PCIE_TX5P	V25	C_PEG_RXP5	C203	0.1U/10V_4	PEG_RX5 9
9 PEG_TX#5	PEG_TX#5	V29	PCIE_RX5N	PCIE_TX5N	V24	C_PEG_RXN5	C187	0.1U/10V_4	PEG_RX#5 9
9 PEG_TX6	PEG_TX6	V31	PCIE_RX6P	PCIE_TX6P	T28	C_PEG_RXP6	C220	0.1U/10V_4	PEG_RX6 9
9 PEG_TX#6	PEG_TX#6	V30	PCIE_RX6N	PCIE_TX6N	T27	C_PEG_RXN6	C224	0.1U/10V_4	PEG_RX#6 9
9 PEG_TX7	PEG_TX7	U31	PCIE_RX7P	PCIE_TX7P	T25	C_PEG_RXP7	C243	0.1U/10V_4	PEG_RX7 9
9 PEG_TX#7	PEG_TX#7	U30	PCIE_RX7N	PCIE_TX7N	T24	C_PEG_RXN7	C252	0.1U/10V_4	PEG_RX#7 9
9 PEG_TX8	PEG_TX8	P30	PCIE_RX8P	PCIE_TX8P	P28	C_PEG_RXP8	C276	0.1U/10V_4	PEG_RX8 9
9 PEG_TX#8	PEG_TX#8	P31	PCIE_RX8N	PCIE_TX8N	P27	C_PEG_RXN8	C268	0.1U/10V_4	PEG_RX#8 9
9 PEG_TX9	PEG_TX9	P29	PCIE_RX9P	PCIE_TX9P	P25	C_PEG_RXP9	C259	0.1U/10V_4	PEG_RX9 9
9 PEG_TX#9	PEG_TX#9	N29	PCIE_RX9N	PCIE_TX9N	P24	C_PEG_RXN9	C246	0.1U/10V_4	PEG_RX#9 9
9 PEG_TX10	PEG_TX10	N31	PCIE_RX10P	PCIE_TX10P	M28	C_PEG_RXP10	C289	0.1U/10V_4	PEG_RX10 9
9 PEG_TX#10	PEG_TX#10	N30	PCIE_RX10N	PCIE_TX10N	M27	C_PEG_RXN10	C277	0.1U/10V_4	PEG_RX#10 9
9 PEG_TX11	PEG_TX11	M31	PCIE_RX11P	PCIE_TX11P	M25	C_PEG_RXP11	C290	0.1U/10V_4	PEG_RX11 9
9 PEG_TX#11	PEG_TX#11	M30	PCIE_RX11N	PCIE_TX11N	M24	C_PEG_RXN11	C296	0.1U/10V_4	PEG_RX#11 9
9 PEG_TX12	PEG_TX12	K30	PCIE_RX12P	PCIE_TX12P	L28	C_PEG_RXP12	C288	0.1U/10V_4	PEG_RX12 9
9 PEG_TX#12	PEG_TX#12	K31	PCIE_RX12N	PCIE_TX12N	L27	C_PEG_RXN12	C295	0.1U/10V_4	PEG_RX#12 9
9 PEG_TX13	PEG_TX13	K29	PCIE_RX13P	PCIE_TX13P	L25	C_PEG_RXP13	C330	0.1U/10V_4	PEG_RX13 9
9 PEG_TX#13	PEG_TX#13	J29	PCIE_RX13N	PCIE_TX13N	L24	C_PEG_RXN13	C324	0.1U/10V_4	PEG_RX#13 9
9 PEG_TX14	PEG_TX14	J31	PCIE_RX14P	PCIE_TX14P	J28	C_PEG_RXP14	C325	0.1U/10V_4	PEG_RX14 9
9 PEG_TX#14	PEG_TX#14	J30	PCIE_RX14N	PCIE_TX14N	J27	C_PEG_RXN14	C331	0.1U/10V_4	PEG_RX#14 9
9 PEG_TX15	PEG_TX15	H31	PCIE_RX15P	PCIE_TX15P	G28	C_PEG_RXP15	C304	0.1U/10V_4	PEG_RX15 9
9 PEG_TX#15	PEG_TX#15	H30	PCIE_RX15N	PCIE_TX15N	G27	C_PEG_RXN15	C316	0.1U/10V_4	PEG_RX#15 9

Clock

2 EXT_GFX_CLKP	EXT_GFX_CLKP	AD29	PCIE_REFCLKP
2 EXT_GFX_CLKN	EXT_GFX_CLKN	AD30	PCIE_REFCLKN

100MHz (+/-300ppm) input frequency, 0-0.7V single-ended swing

SM BUS

AC28		NC_SMBCLK
AC27		NC_SMBDATA

12 PCIE_RST#	R71	0_4	AG25	PERSTB

Calibration

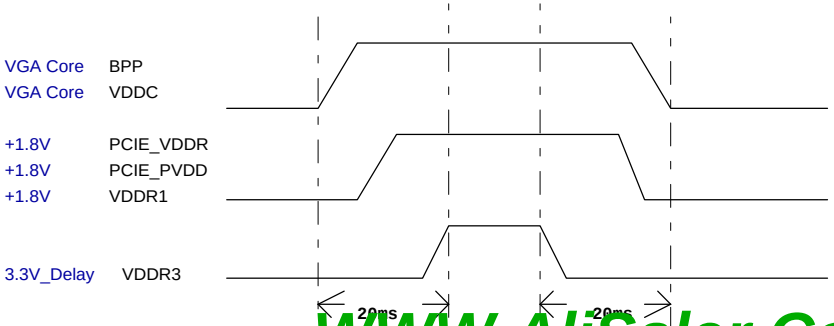
PCIE_CALRN	AF25	M72_PCIE_CALRN	R74	2K/F_4	+1.1V_PCIE_VDDC
PCIE_CALRP	AE25	M72_PCIE_CALRP	R70	1.27K/F_4	

1.27K for M82-S

NC_1	AE23
NC_2	AH30

M72-S/M82-S
U29A

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S



PROJECT : QT8		
Quanta Computer Inc.		
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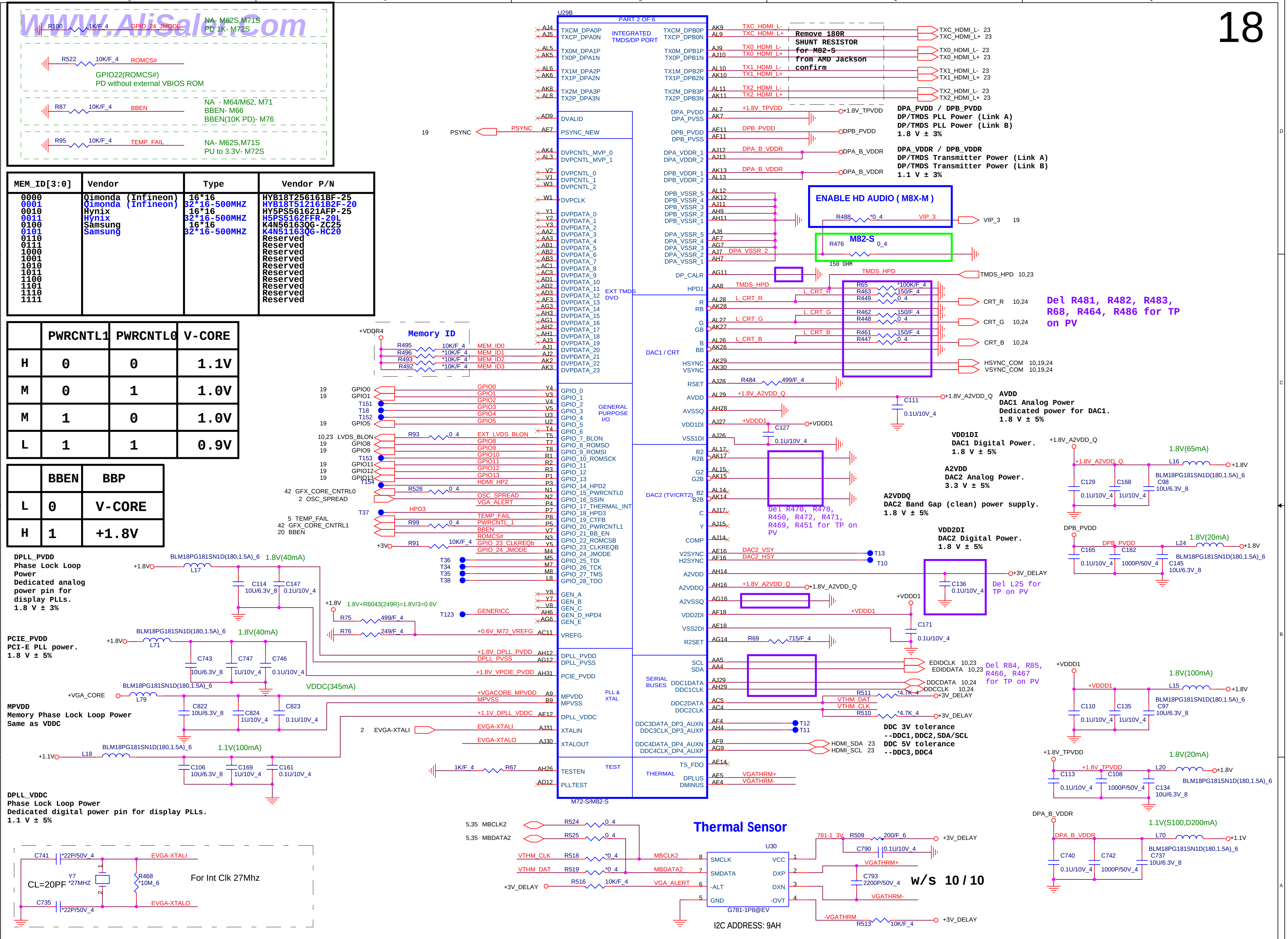
NB5/RD5

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T256161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161B2F-20
0010	Hynix	16*16	HY5PS561621AFP-25
0011	Hynix	32*16-500MHZ	H5PS5162FFR-20L
0100	Samsung	16*16	K4N56163QG-ZC25
0101	Samsung	32*16-500MHZ	K4N51163QG-HC20
0110			Reserved
0111			Reserved
1000			Reserved
1001			Reserved
1010			Reserved
1011			Reserved
1100			Reserved
1101			Reserved
1110			Reserved
1111			Reserved

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V



NA- M62S,M71S
PD 1K- M72S
GPIO22(ROMCS#)
PD without external VBIOS ROM
NA - M64/M62, M71
BBEN- M66
BBEN(10K PD)- M76
NA- M62S,M71S
PU to 3.3V- M72S
Memory ID
U29B
PART 2 OF 6
INTEGRATED TMDS/DP PORT
Remove 180R SHUNT RESISTOR for M82-S from AMD Jackson confirm
DPA_PVDD / DPB_PVDD
DP/TMDS PLL Power (Link A)
DP/TMDS PLL Power (Link B)
1.8 V ± 3%
DPA_VDDR / DPB_VDDR
DP/TMDS Transmitter Power (Link A)
DP/TMDS Transmitter Power (Link B)
1.1 V ± 3%
ENABLE HD AUDIO (M8X-M)
M82-S
Del R481, R482, R483, R68, R464, R486 for TP on PV
AVDD
DAC1 Analog Power
Dedicated power for DAC1.
1.8 V ± 5%
VDD1DI
DAC1 Digital Power.
1.8 V ± 5%
A2VDD
DAC2 Analog Power.
3.3 V ± 5%
A2VDDQ
DAC2 Band Gap (clean) power supply.
1.8 V ± 5%
VDD2DI
DAC2 Digital Power.
1.8 V ± 5%
Del R470, R478, R450, R472, R471, R469, R451 for TP on PV
Del L25 for TP on PV
Del R84, R85, R466, R467 for TP on PV
DDC 3V tolerance
--DDC1,DDC2,SDA/SCL
DDC 5V tolerance
--DDC3,DDC4
DPLL_PVDD
Phase Lock Loop Power
Dedicated analog power pin for display PLLs.
1.8 V ± 3%
PCIE_PVDD
PCI-E PLL power.
1.8 V ± 5%
MPVDD
Memory Phase Lock Loop Power
Same as VDDC
DPLL_VDDC
Phase Lock Loop Power
Dedicated digital power pin for display PLLs.
1.1 V ± 5%
VDDC(345mA)
CL=20PF
For Int Clk 27Mhz
Thermal Sensor
G781-1P8@EV
I2C ADDRESS: 9AH
W/S 10 / 10
M72-S/M82-S

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Quanta Computer Inc.

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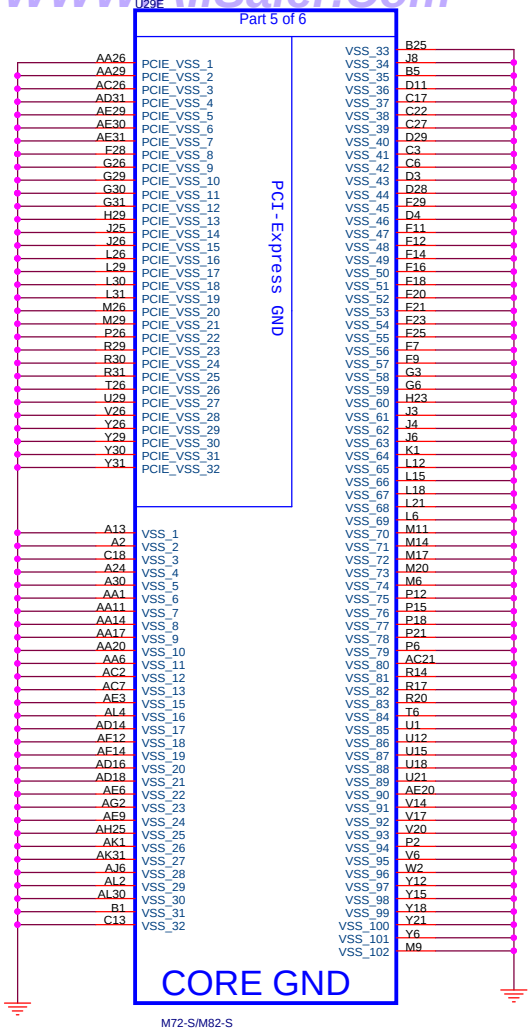
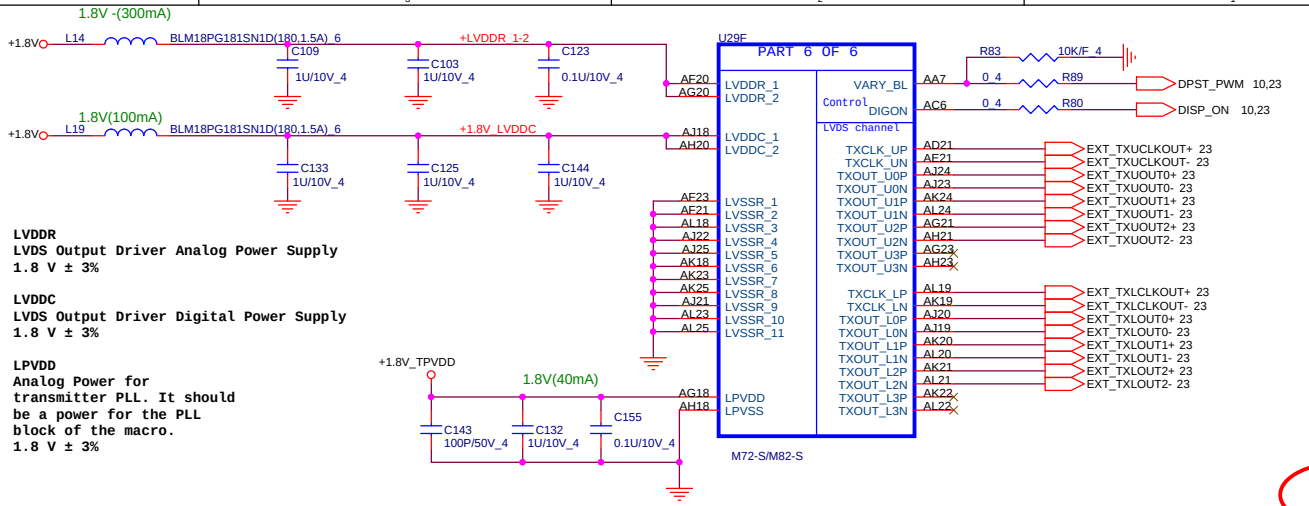




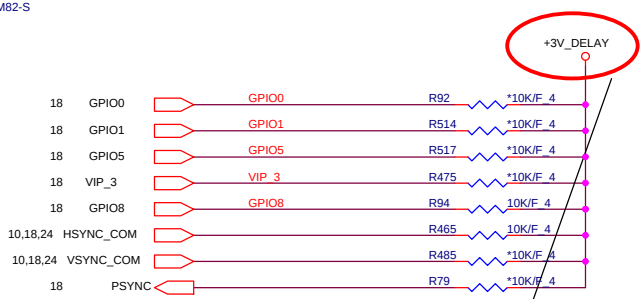
LVDDR
LVDS Output Driver Analog Power Supply
1.8 V ± 3%

LVDDC
LVDS Output Driver Digital Power Supply
1.8 V ± 3%

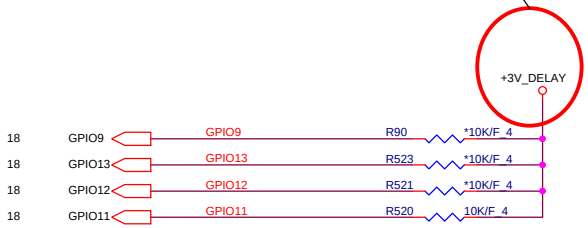
LPVDD
Analog Power for transmitter PLL. It should be a power for the PLL block of the macro.
1.8 V ± 3%

CONFIGURATION STRAPS

PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows eitherPCIe 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO (M8X-M)	1
GPIO8	ENABLE HD AUDIO (M82-S)	1
HSYNC	ENABLED HDMI	1



SI-1 Modified -- follow AMD reference schematic change for reduce leakage to VDDR3 BUS



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

NB5/RD5

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Quanta Computer Inc.

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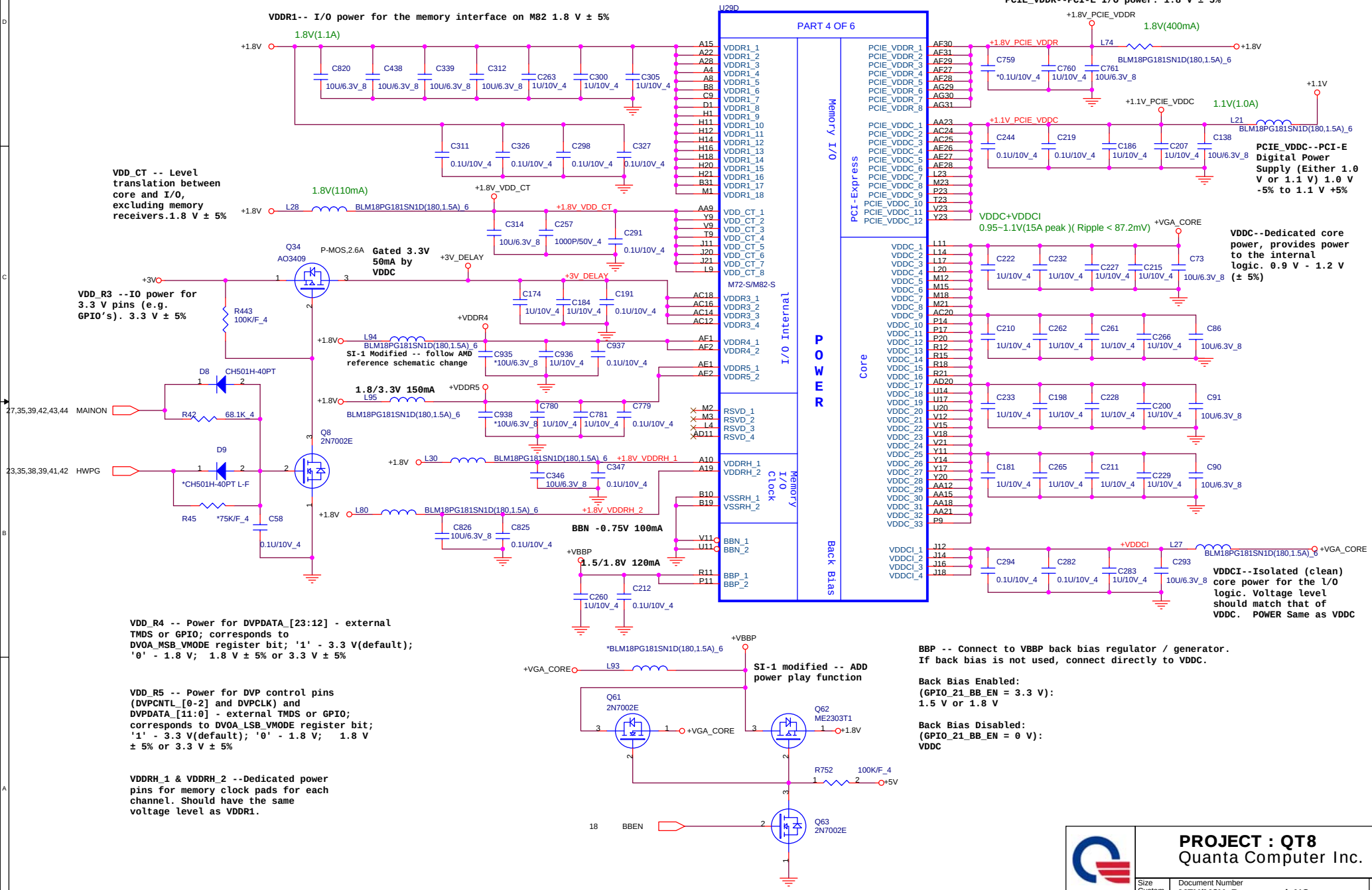

PROJECT : QT8
Quanta Computer Inc.

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NB5/RD5

U29C

Part 3 of 6

MEMORY INTERFACE

M72-S/M82-S

MDA0	E29	DQ_0	MA_0	B14	MAA0
MDA1	E30	DQ_1	MA_1	A14	MAA1
MDA2	E31	DQ_2	MA_2	B13	MAA2
MDA3	D31	DQ_3	MA_3	E14	MAA3
MDA4	C29	DQ_4	MA_4	B17	MAA4
MDA5	B29	DQ_5	MA_5	A17	MAA5
MDA6	B30	DQ_6	MA_6	C15	MAA6
MDA7	A29	DQ_7	MA_7	G16	MAA7
MDA8	E26	DQ_8	MA_8	E16	MAA8
MDA9	D26	DQ_9	MA_9	C14	MAA9
MDA10	E25	DQ_10	MA_10	A12	MAA10
MDA11	D25	DQ_11	MA_11	B12	MAA11
MDA12	G23	DQ_12	MA_BA0	C12	A_BA0
MDA13	G21	DQ_13	MA_BA1	D14	A_BA1
MDA14	E21	DQ_14	MA_A12	B15	MAA12
MDA15	D21	DQ_15	MA_BA2	G14	A_BA2
MDA16	C28	DQ_16			
MDA17	B28	DQ_17	DQMb_0	D30	DQMA#0
MDA18	B27	DQ_18	DQMb_1	G25	DQMA#1
MDA19	A27	DQ_19	DQMb_2	C26	DQMA#2
MDA20	C25	DQ_20	DQMb_3	C21	DQMA#3
MDA21	A25	DQ_21	DQMb_4	C5	DQMA#4
MDA22	C24	DQ_22	DQMb_5	D6	DQMA#5
MDA23	B24	DQ_23	DQMb_6	D2	DQMA#6
MDA24	C23	DQ_24	DQMb_7	K3	DQMA#7
MDA25	B23	DQ_25			
MDA26	A23	DQ_26	QS_0	C30	QSA0
MDA27	B22	DQ_27	QS_1	D23	QSA1
MDA28	C20	DQ_28	QS_2	B26	QSA2
MDA29	B20	DQ_29	QS_3	B21	QSA3
MDA30	A20	DQ_30	QS_4	B6	QSA4
MDA31	C19	DQ_31	QS_5	E7	QSA5
MDA32	C8	DQ_32	QS_6	E2	QSA6
MDA33	C7	DQ_33	QS_7	J2	QSA7
MDA34	B7	DQ_34			
MDA35	A7	DQ_35	QS_0B	C31	QSA#0
MDA36	A5	DQ_36	QS_1B	E23	QSA#1
MDA37	C4	DQ_37	QS_2B	A26	QSA#2
MDA38	B4	DQ_38	QS_3B	A21	QSA#3
MDA39	A3	DQ_39	QS_4B	A6	QSA#4
MDA40	G9	DQ_40	QS_5B	D7	QSA#5
MDA41	E9	DQ_41	QS_6B	E1	QSA#6
MDA42	D9	DQ_42	QS_7B	J1	QSA#7
MDA43	G7	DQ_43			
MDA44	G5	DQ_44	ODT0	E20	ODTA0
MDA45	F5	DQ_45	ODT1	C11	ODTA1
MDA46	G4	DQ_46			
MDA47	F4	DQ_47	CLK0	A18	CLKA0
MDA48	B3	DQ_48	CLK1	A11	CLKA1
MDA49	B2	DQ_49			
MDA50	C2	DQ_50	CLK0b	B18	CLKA0#
MDA51	C1	DQ_51	CLK1b	B11	CLKA1#
MDA52	E3	DQ_52			
MDA53	F3	DQ_53	RAS0b	G20	RASA0#
MDA54	F2	DQ_54	RAS1b	D12	RASA1#
MDA55	F1	DQ_55			
MDA56	G2	DQ_56	CAS0b	D20	CASA0#
MDA57	G1	DQ_57	CAS1b	E12	CASA1#
MDA58	H3	DQ_58			
MDA59	H2	DQ_59	CS0b_0	E18	CSA0#_0
MDA60	K2	DQ_60	CS0b_1	G18	
MDA61	L3	DQ_61			
MDA62	L2	DQ_62	CS1b_0	G11	CSA1#_0
MDA63	L1	DQ_63	CS1b_1	E11	
	F30	MVREFD	CKE0	D18	CKEA0
	F31	MVREFS	CKE1	G12	CKEA1
	L5	TEST_MCLK	WE0b	D16	WEA0#
	L7	TEST_YCLK	WE1b	C10	WEA1#
	J7	MEMTEST	DRAM_RST	J5	

write strobe

read strobe

22	ODTA0	ODTA0	
22	ODTA1	ODTA1	
22	RASA0#	RASA0#	
22	RASA1#	RASA1#	
22	CASA0#	CASA0#	
22	CASA1#	CASA1#	
22	WEA0#	WEA0#	
22	WEA1#	WEA1#	
22	CSA0#_0	CSA0#_0	
22	CSA1#_0	CSA1#_0	
22	CKEA0	CKEA0	
22	CKEA1	CKEA1	
22	CLKA0	CLKA0	
22	CLKA0#	CLKA0#	
22	CLKA1	CLKA1	
22	CLKA1#	CLKA1#	
22	QSA#[7..0]	QSA#[7..0]	
22	QSA[7..0]	QSA[7..0]	
22	DQMA#[7..0]	DQMA#[7..0]	
22	MDA[63..0]	MDA[63..0]	
22	MAA[12..0]	MAA[12..0]	
22	A_BA0	A_BA0	
22	A_BA1	A_BA1	

A_BA2 22

SI-1 modified -- for support 1Gbit VRAM (64M X 16)

+1.8V

R116 100/F_4

MVREFD

+1.8V

R113 100/F_4

C338 0.1U/10V_4

R532 100/F_4

MVREFS

C817 0.1U/10V_4

R529 100/F_4

R98 4.7K_4

R102 4.7K_4

R97 240/F_4

Change MEMTEST to 240 1% ohm to GND , AMD update

R101 4.7K_4 +1.8V

N85/RD5

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Quanta Computer Inc.

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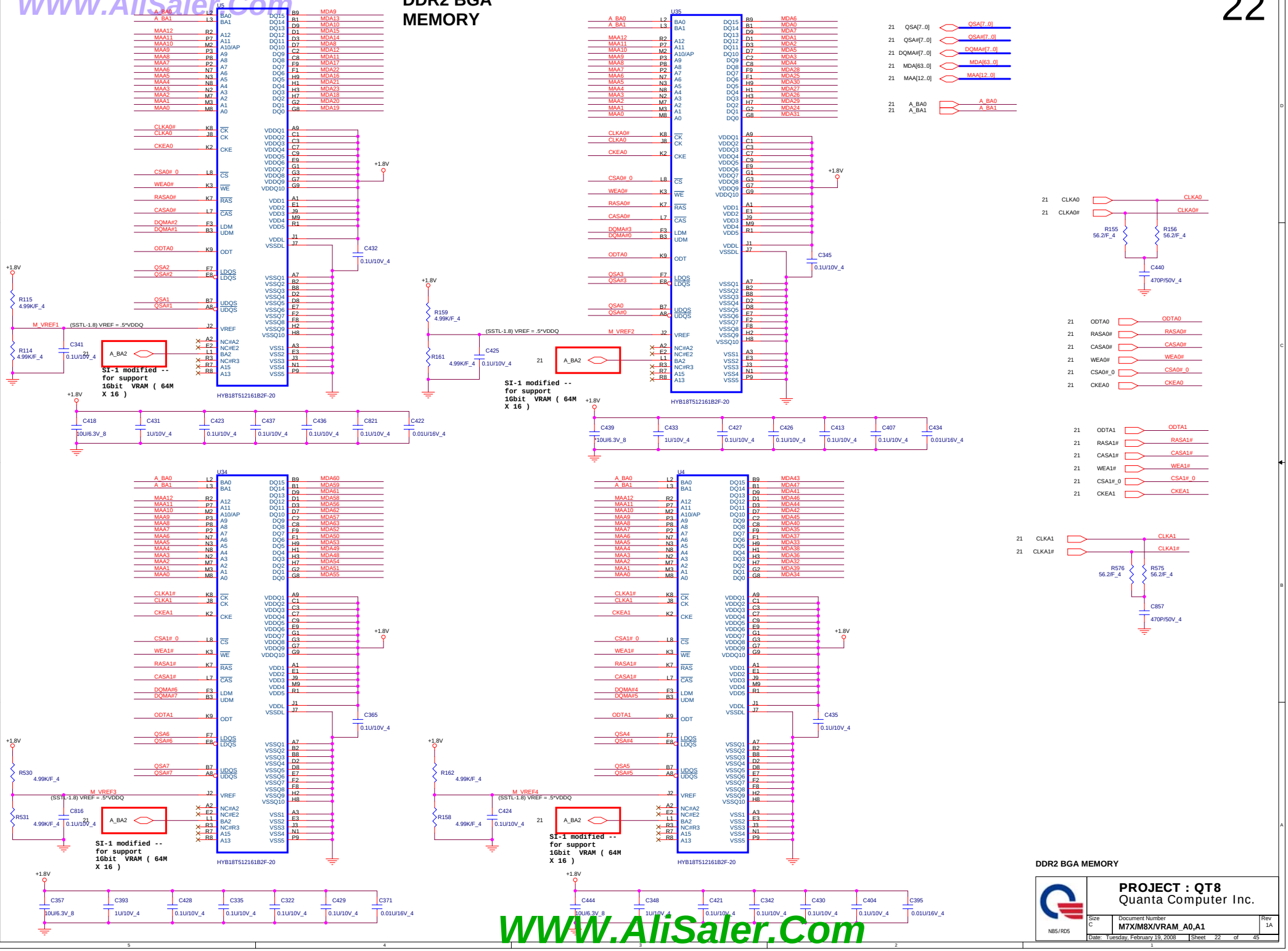
DDR2 BGA MEMORY



1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB to LVDS for UMA

10 LA_CLK — LA_CLK — RP3 — *0_4P2R_4 — TXLCLKOUT+
10 LA_CLK# — LA_CLK# — TXLCLKOUT-
10 LA_DATAP0 — LA_DATAP0 — RP1 — *0_4P2R_4 — TXLOUT0+
10 LA_DATAN0 — LA_DATAN0 — TXLOUT0-
10 LA_DATAP1 — LA_DATAP1 — RP4 — *0_4P2R_4 — TXLOUT1+
10 LA_DATAN1 — LA_DATAN1 — TXLOUT1-
10 LA_DATAP2 — LA_DATAP2 — RP5 — *0_4P2R_4 — TXLOUT2+
10 LA_DATAN2 — LA_DATAN2 — TXLOUT2-

10 LB_CLK — LB_CLK — RP2 — *0_4P2R_4 — TXUCLKOUT+
10 LB_CLK# — LB_CLK# — TXUCLKOUT-
10 LB_DATAP0 — LB_DATAP0 — RP6 — *0_4P2R_4 — TXUOUT0+
10 LB_DATAN0 — LB_DATAN0 — TXUOUT0-
10 LB_DATAP1 — LB_DATAP1 — RP8 — *0_4P2R_4 — TXUOUT1+
10 LB_DATAN1 — LB_DATAN1 — TXUOUT1-
10 LB_DATAN2 — LB_DATAN2 — RP7 — *0_4P2R_4 — TXUOUT2+
10 LB_DATAP2 — LB_DATAP2 — TXUOUT2+

OPTION SIGNAL FROM M8X to LVDS for discrete

19 EXT_TXLCLKOUT- — EXT_TXLCLKOUT- — RP59 — 0_4P2R_4 — TXLCLKOUT-
19 EXT_TXLCLKOUT+ — EXT_TXLCLKOUT+ — TXLCLKOUT+
19 EXT_TXLOUT0- — EXT_TXLOUT0- — RP57 — 0_4P2R_4 — TXLOUT0-
19 EXT_TXLOUT0+ — EXT_TXLOUT0+ — TXLOUT0+
19 EXT_TXLOUT1- — EXT_TXLOUT1- — RP60 — 0_4P2R_4 — TXLOUT1-
19 EXT_TXLOUT1+ — EXT_TXLOUT1+ — RP61 — 0_4P2R_4 — TXLOUT1+
19 EXT_TXLOUT2+ — EXT_TXLOUT2+ — TXLOUT2+
19 EXT_TXLOUT2- — EXT_TXLOUT2- — TXLOUT2-

19 EXT_TXUCLKOUT- — EXT_TXUCLKOUT- — RP58 — 0_4P2R_4 — TXUCLKOUT-
19 EXT_TXUCLKOUT+ — EXT_TXUCLKOUT+ — TXUCLKOUT+
19 EXT_TXUOUT0+ — EXT_TXUOUT0+ — RP62 — 0_4P2R_4 — TXUOUT0+
19 EXT_TXUOUT0- — EXT_TXUOUT0- — TXUOUT0-
19 EXT_TXUOUT1- — EXT_TXUOUT1- — RP64 — 0_4P2R_4 — TXUOUT1-
19 EXT_TXUOUT1+ — EXT_TXUOUT1+ — TXUOUT1+
19 EXT_TXUOUT2- — EXT_TXUOUT2- — RP63 — 0_4P2R_4 — TXUOUT2-
19 EXT_TXUOUT2+ — EXT_TXUOUT2+ — TXUOUT2+

UMA/DISCRETE select for HDMI

From RS780M

for Layout concern ,placement close north bridge

9 C_PEG_TX#15 — C_PEG_TX#15 C386 — *0.1U/10V_4 — TX2_HDMI-L — RP31 — *0_4P2R_4 — TX2_HDMI+
9 C_PEG_TX15 — C_PEG_TX15 C387 — *0.1U/10V_4 — TX2_HDMI+L — TX2_HDMI+L — TX2_HDMI-
9 C_PEG_TX#14 — C_PEG_TX#14 C388 — *0.1U/10V_4 — TX1_HDMI-L — RP23 — *0_4P2R_4 — TX1_HDMI-
9 C_PEG_TX14 — C_PEG_TX14 C389 — *0.1U/10V_4 — TX1_HDMI+L — TX1_HDMI+L — TX1_HDMI+
9 C_PEG_TX#13 — C_PEG_TX#13 C355 — *0.1U/10V_4 — TX0_HDMI-L — RP37 — *0_4P2R_4 — TX0_HDMI+
9 C_PEG_TX13 — C_PEG_TX13 C344 — *0.1U/10V_4 — TX0_HDMI+L — TX0_HDMI+L — TX0_HDMI-
9 C_PEG_TX#12 — C_PEG_TX#12 C827 — *0.1U/10V_4 — TXC_HDMI-L — RP17 — *0_4P2R_4 — TXC_HDMI-
9 C_PEG_TX12 — C_PEG_TX12 C828 — *0.1U/10V_4 — TXC_HDMI+L — TXC_HDMI+L — TXC_HDMI+

for Layout concern ,placement close HDMI conn

From M82-S

18 TX2_HDMI_L- — TX2_HDMI_L- C794 — 0.1U/10V_4 — TX2_HDMI-
18 TX2_HDMI_L+ — TX2_HDMI_L+ C789 — 0.1U/10V_4 — TX2_HDMI+
18 TX1_HDMI_L- — TX1_HDMI_L- C782 — 0.1U/10V_4 — TX1_HDMI-
18 TX1_HDMI_L+ — TX1_HDMI_L+ C786 — 0.1U/10V_4 — TX1_HDMI+
18 TX0_HDMI_L- — TX0_HDMI_L- C799 — 0.1U/10V_4 — TX0_HDMI-
18 TX0_HDMI_L+ — TX0_HDMI_L+ C797 — 0.1U/10V_4 — TX0_HDMI+
18 TXC_HDMI_L- — TXC_HDMI_L- C768 — 0.1U/10V_4 — TXC_HDMI-
18 TXC_HDMI_L+ — TXC_HDMI_L+ C776 — 0.1U/10V_4 — TXC_HDMI+

for Layout concern ,placement close HDMI conn

+5V — Q36 2N7002E — R528 100K/F_4

TX2_HDMI+ — R507 499/F_4
TX2_HDMI- — R508 499/F_4
TX1_HDMI+ — R506 499/F_4
TX1_HDMI- — R505 499/F_4
TX0_HDMI+ — R512 499/F_4
TX0_HDMI- — R515 499/F_4
TXC_HDMI+ — R504 499/F_4
TXC_HDMI- — R500 499/F_4

UMA RS780M
上 750 ohm CS17502FB19

DIS M82-S
上 499 ohm CS14992FB24

Close to HDMI Connector

+12VALW / +3V / +5VSUS / +3VLCD

R19 330K_6 — A03404 ID current 5.8A — C16 0.1U/10V_4
R14 100K/F_4 — LCDONG — Q1 AO3404 N-MOS,5.8A — R10 22_8 — LCDDISCHG
Q3 PDTC144EU — Q4 2N7002E — C22 0.1U/10_4
10,19 DISP_ON — R17 2.2K_4 — LCDON# — Q2 2N7002E

R401 75R/F_6 — +LOGO_PWR

SI-2 modified-delete R402 and R401 from 0ohm to 75ohm

+3VLCD — L1 PBY201209T-4A_8 — +3VLCD_CON — C12 10U/6.3V_8 — C10 0.1U/10V_4 — C13 0.01U/16V_4

+VIN_BLIGHT — +3VLCD_CON

C6 1000P/50V_4 — C678 1000P/50V_4

10,18 EDIDDATA — EDIDDATA — +LOGO_PWR — BLONCON

CN1 (41 / 42)

VADJ1 — EDIDCLK 10,18 — Camera Pin

TXLCLKOUT+ / TXLCLKOUT- — TXLOUT0+ / TXLOUT0- — TXLOUT1+ / TXLOUT1- — TXLOUT2+ / TXLOUT2- — TXUCLKOUT+ / TXUCLKOUT- — TXUOUT0+ / TXUOUT0- — TXUOUT1+ / TXUOUT1- — TXUOUT2+ / TXUOUT2-

PN_BLON / LVDS_BLON / LCD_BK

PN_BLON — D5 CH501H-40PT — BLONCON — C28 22P/50V_4 — R22 100K/F_4
+3VPCU — R24 33K_6 — D6 CH501H-40PT — LID_EC# — LID_EC# 34,35
10,18 LVDS_BLON — R23 1K/F_4 — PN_BLON — D7 CH501H-40PT — HWPG — 20,35,38,39,41,42
12 LCD_BK — Q5 PDTC144EU — R259 *10K/F_4 — +3VS5

Del R21 and Pull hi R259 to +3VS5, add D7 to HWPG on PV

PV del logo light

10,19 DPST_PWM — DPST_PWM R88 — LCD CONN *0_4
35 PWM_VADJ — PWM_VADJ R96 — 0_4 — VADJ1
C5 *4.7U/6.3V_6 — C7 0.1U/10V_4

+VIN / +VIN_BLIGHT

+VIN — L2 FBM2125 HM330-T(4A,0.015) 8 — +VIN_BLIGHT
C15 0.1U/50V_6 — C11 0.01U/50V_4 — C9 0.1U/50V_6 — C14 *10U/25V_12 — C8 0.1U/50V_6

HDMI HPD SENSE

10,18 TMDS_HPD — TMDS_HPD R66 20K/F_4 — HDMI_DET
check 3v or 5v
D10 UDZS2.7BTE-17 — R64 100K/F_4

+5V_HDMVCC

+5V_HDMVCC — D31 CH501H-40PT — R494 4.7K_4 — HDMI_SCLK
+5V_HDMVCC — D32 CH501H-40PT — R503 4.7K_4 — HDMI_SDATA

Change R494, R503 to 4.7K for AMD on PV

HDMI PORT

CN29 HDMI CONN

TX2_HDMI+ / TX2_HDMI- / TX1_HDMI+ / TX1_HDMI- / TX0_HDMI+ / TX0_HDMI- / TXC_HDMI+ / TXC_HDMI-
SHELL1 SHELL3 SHELL2 SHELL4
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET

Del C748, C756 for HDMI on PV

HDMI_SCLK — L73 0_6 — HDMISCL
HDMI_SDATA — L75 0_6 — HDMISDA
+5V_HDMVCC
+5V — FUSE1A6V_POLY F1 — C128 *0.1U/10V_4 — HDMI_DET

UMA AND DISCRETE HDMI I2C SELECT

Close to HDMI Connector

18 HDMI_SDA — HDMI_SDA — RP65 0_4P2R_4 — HDMI_SDATA
18 HDMI_SCL — HDMI_SCL — HDMI_SCLK

Discrete DDC4 is 5V tolerance , the MOSFET level shifter no need
UMA DDC is 3V tolerance,the MOSFET level shifter is need

DIS

+3V — R680 *2K/04 — +5V
10 HDMI_DDC_CLK — Q59 *FDV301N — 3 HDMI_SCLK
HDMI_DDC_CLK — R753 *0_4 — HDMI_SCLK
HDMI_DDC_DATA — R755 *0_4 — HDMI_SDATA
+3V — R681 *2K/04 — +5V
10 HDMI_DDC_DATA — Q60 *FDV301N — 3 HDMI_SDATA

Change 2N7002 to FDV301N for AMD on PV

UMA

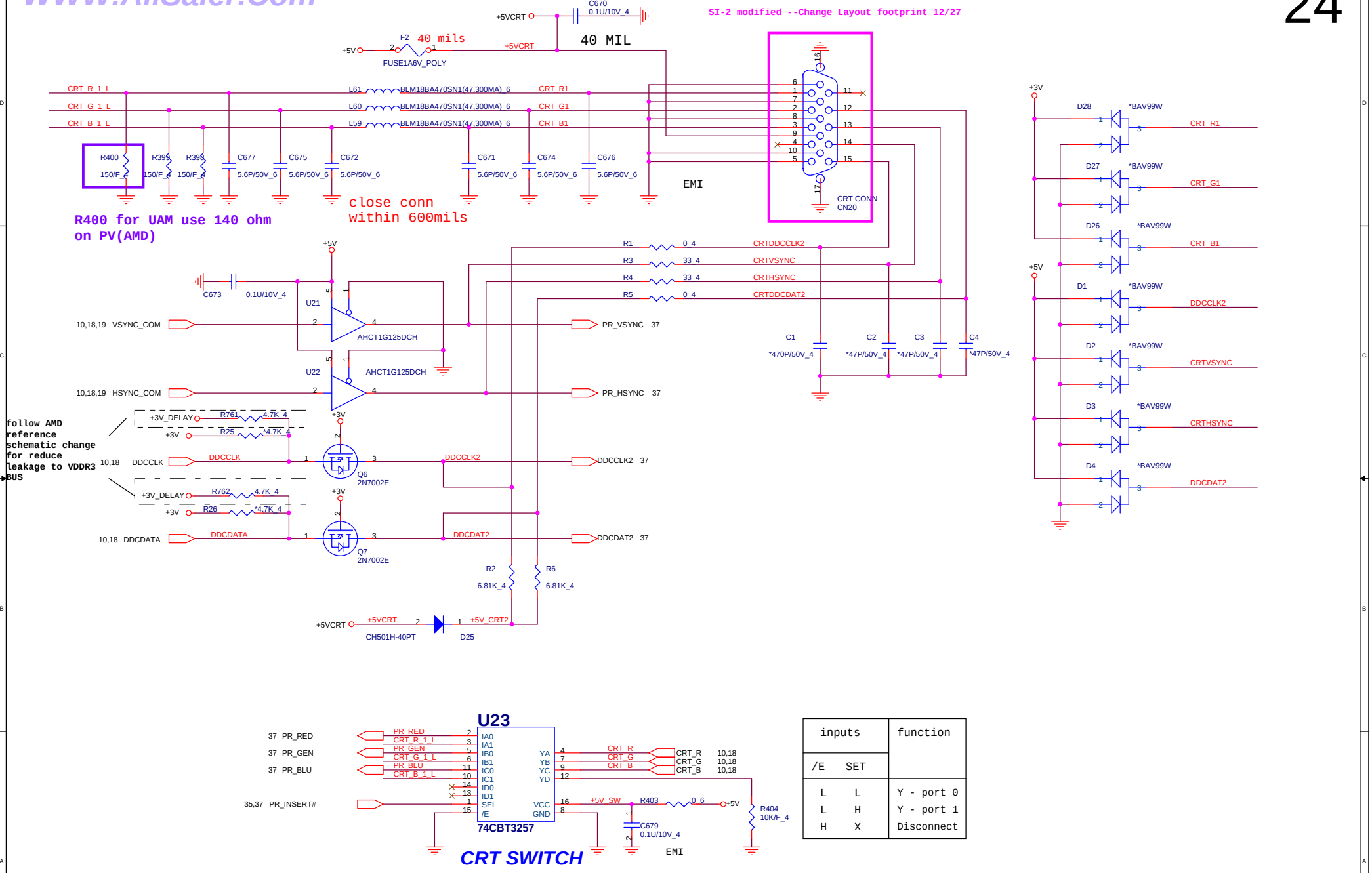
PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	LCD CONN,HDMI CONN	1A

Date: Tuesday, February 19, 2008 — Sheet 23 of 45

CRT PORT



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT	1A

NB5/RD5

Date: Tuesday, February 19, 2008 Sheet 24 of 45

For 5158E

2 CLK_48M_CR — R397 *0_4 XTLO — UMA BOM need to add

+3VSUS — R321 *100K/F_4

26,29 CARD_LED# — R320 *0_4 CARD_LED0

U19 *RTS5158

CF_CD# GPIO0 CF_D10 CF_D9 CF_D2 CF_D8/SM_CD# CF_D1/XD_CD# CF_D0/SM_WPM#/SD_WP CF_A0/SD_CD# CF_DMACK# CF_A1/XD_D4 CF_DMARQ

XD_CD# SP2 SD_CD# SP4

SI-2 modified --Fix Y5 layout footprint to XTAL-5X3_2-3_8 (ME placement)

R362 *6.19K/F_4 RREF

13 USBP6_CR- 13 USBP6_CR+ DM DP

C665 *5.6P/50V_4 XTLO — R395 *270K_4 — *12MHz Y5 — C668 *5.6P/50V_4 XTLI

For 5158 BG6120000717

MODE_SEL R394 *10K/F_4 C667 *47P/50V_4 For 5158

+3VSUS — R667 *100K/F_4 5158_RST# — C925 *1U/10V_4

If SD_DAT1 connect to SP4 , MOD_SEL need to let it to N.C

XD_CLE/CF_D3 XD_CE#/CF_D11 XD_ALE/CF_D4

SD_DAT2/XD_RE#/CF_D12 SD_DAT3/XD_WE#/CF_D5 XD_RDY/CF_D13 SD_DAT4/XD_WP#/CF_D6

SD_CMD SD_DAT5/XD_D0/CF_D14 SD_CLK/XD_D1/MS_CLK/CF_D7 SD_DAT6/XD_D7/MS_D3/CF_D15 CF_CS0#

MS_INS#/CF_IORD# SD_DAT7/XD_D2/MS_D2/CF_IOWR# SD_DAT0/XD_D6/MS_D0/CF_RST# SD_DAT1/XD_D3/MS_D1/CF_IORDY XD_D5/MS_BS/CF_A2

AV_PLL_IN VREG_OUT 5V_IN A3V3_IN D3V3_IN D3V3_OUT A3V3_OUT CARD_3V3_OUT AG33 AG_PLL DGND2 DGND1

For 5158: SP6 R339 *0_4 SD_DAT1; SP4 R333 *0_4

For 5158E

AL005158B10 -->RTS5158E

AL005158B00 -->RTS5158

SI-2 remove R673 not need -- UMA BOM remove

C647 *0.1U/10V_4 — C918 *1U/10V_4

VREG +3VSUS_RTS R323 *0_6 +3VSUS

C633 *0.1U/10V_4 — C634 *0.1U/10V_4 — C593 *0.1U/10V_4 — C598 *4.7U/6.3V_6

C612 *0.1U/10V_4 — C589 *4.7U/6.3V_6 — +3VSUS

+3VCARD — C629 *1U/10V_4 — C624 *0.1U/10V_4 — C917 *0.1U/10V_4

C628 *0.1U/10V_4 — C618 *0.1U/10V_4 — C617 *0.1U/10V_4

Note:

	SD/MMC	MS	XD
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

SP7	R315 *0_4	MS_DATA0_SD_DAT0	
	R316 *0_4	XD-D6	
SP6	R334 *0_4	MS_DATA1	
	R338 *0_4	XD-D3	
SP8	R345 *0_4	MS_DATA2_XD_D2	
SP16	R666 *0_4	SD_DAT2	
	R676 *0_4	XD-RE#	
SP5	R327 *0_4	MS_BS	
	R335 *0_4	XD-D5	
SP15	R675 *0_4	SD_DAT3	
	R390 *0_4	XD_WE	
SP11	R354 *0_4	SD_CLK_MS_CLK	
	R358 *0_4	XD-D1	
SP2	R319 *0_4	SD_WP	
SP13	R677 *0_4	XD-WP#	
SP19	R393 *0_4	XD-CLE	
SP4	R317 *0_4	XD-D4	
SP10	R351 *0_4	MS_DATA3	
	R348 *0_4	XD-D7	
SP14	R389 *0_4	XD-RB#	
SP12	R369 *0_4	XD-D0	
SP17	R391 *0_4	XD-ALE	
SP18	R392 *0_4	XD-CE#	
SD_CMD_R	R372 *0_4	SD_CMD	

CH501H-40PT: D23 MS_CD# / SD_CD# — XD_CD# — C873 270P/25V_4

RTS5158 need to remove D23/D24/C873

JMB 380 Note:

	SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN1 CARD READER

XD,MMC/SD,MS/MSP

+3VCARD — C905 *270P/25V_4

R678 *10K/F_4 — XD-WP#

Del R625 for TP on PV

CN36 5IN1 CARD READER SOCKET

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

SD_CLK_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

GND MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

SD-C/D SD-CD-SW SD-W/P SD-WP-SW XD-CD XD-VCC XD-DATA7 XD-DATA6 XD-DATA5 XD-DATA4 XD-DATA3 XD-DATA2 SD-DATA0 SD-CLK SD-VCC

SD_CD# SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

+3VCARD — C872 2.2U/6.3V_6 — R607 150K/F_4 — CLOSE CONN

Q25 *AO3409 — +3V — +5V

26 MC_PWR_CTRL_0# — XD_PWON R387 *10K/F_4

C887 0.1U/10V_4 — C894 0.1U/10V_4 — C874 0.1U/10V_4

R332 0_8

RESERVED for JMicron -- after programming can out-put +3.3V throught MC_PWR_CTRL_0# signal

SI-2 for 台端Conn

CN42

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP# XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

SD_CLK_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

GND MS-VCC MS-SDLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0 MS-DATA1 MS-BS GND

SD-CD SD-WP XD-CD XD-VCC XD-D7 XD-D6 XD-D5 XD-D4 XD-D3 XD-D2 SD-DATA0 SD-CLK SD-VCC

SD_CD# SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_CLK_MS_CLK

*TAI TWUM 5IN1 CARD READER SOCKET

MDIO00 R611 0_4 MS_DATA0_SD_DAT0

MDIO01 R623 0_4 XD-D0; R608 0_4 SD_DAT1; R610 0_4 MS_DATA1; R622 0_4 XD-D1

MDIO02 R612 0_4 MS_DATA2_XD_D2; R620 0_4 SD_DAT2

MDIO03 R614 0_4 MS_DATA3; R619 0_4 SD_DAT3

MDIO04 R606 0_4 XD-D3; R618 0_4 SD_CMD; R609 0_4 MS_BS; R627 0_4 XD_WE

MDIO05 R617 47/F_4 SD_CLK_MS_CLK; R634 47/F_4 XD-CE#; R593 0_4 SD_WP

MDIO06 R591 0_4 XD-WP#; R633 0_4 XD-CLE; R605 0_4 XD-D4; R603 0_4 XD-D5; R602 0_4 XD-D6; R601 0_4 XD-D7; R679 0_4 XD-RE#; R635 0_4 XD-RB#; R628 0_4 XD-ALE

MDIO07 MDIO08 MDIO09 MDIO10 MDIO11 MDIO12 MDIO13 MDIO14

SI-2 modified for JMicron 380

PAD8 MDC_SPRING — PAD9 MDC_SPRING — PAD10 MDC_SPRING — PAD11 MDC_SPRING

H32 *H-S315D110P2 — H31 *H-S315D110P2 — H13 *H-C273X118D173X118N — PAD7 *MDC_SPRING

H22 *H-S315D110P2 — H23 *H-C244D186P2 — H3 *H-C256D157P2 — H6 *H-C217D157P2 — H9 *H-C217D157P2 — H8 *H-C217D157P2

H12 *H-C315D118P2 — H7 *H-S315D110P2 — H25 *H-C315D118P2 — H18 *H-C256D217P2 — H17 *H-C256D217P2

K/B SCREW HOLE — VGA Hole

H5 *H-S315D110P2 — H11 *H-S315D110P2 — H4 *H-C217D181P2 — H10 *H-C217D181P2 — H1 *H-C315D118P2

Del PAD1 for TP on PV

PAD4 — PAD5 MDC_SPRING — PAD6 MDC_SPRING — PAD2 *MDC_SPRING — PAD3 *MDC_SPRING

for MDC cable routing

Mini Card Hole

H20 *H-C256D217P2 — H14 *H-C256D217P2

SI-2 for CN37

H28 *H-C236D87P2 — H29 *H-C236D87P2 — H30 *H-C236D87P2

H26 *H-C256D217P2 — H27 *H-C256D217P2

PAD12 MDC_SPRING

NB5/RD5

PROJECT : QT8

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	1A

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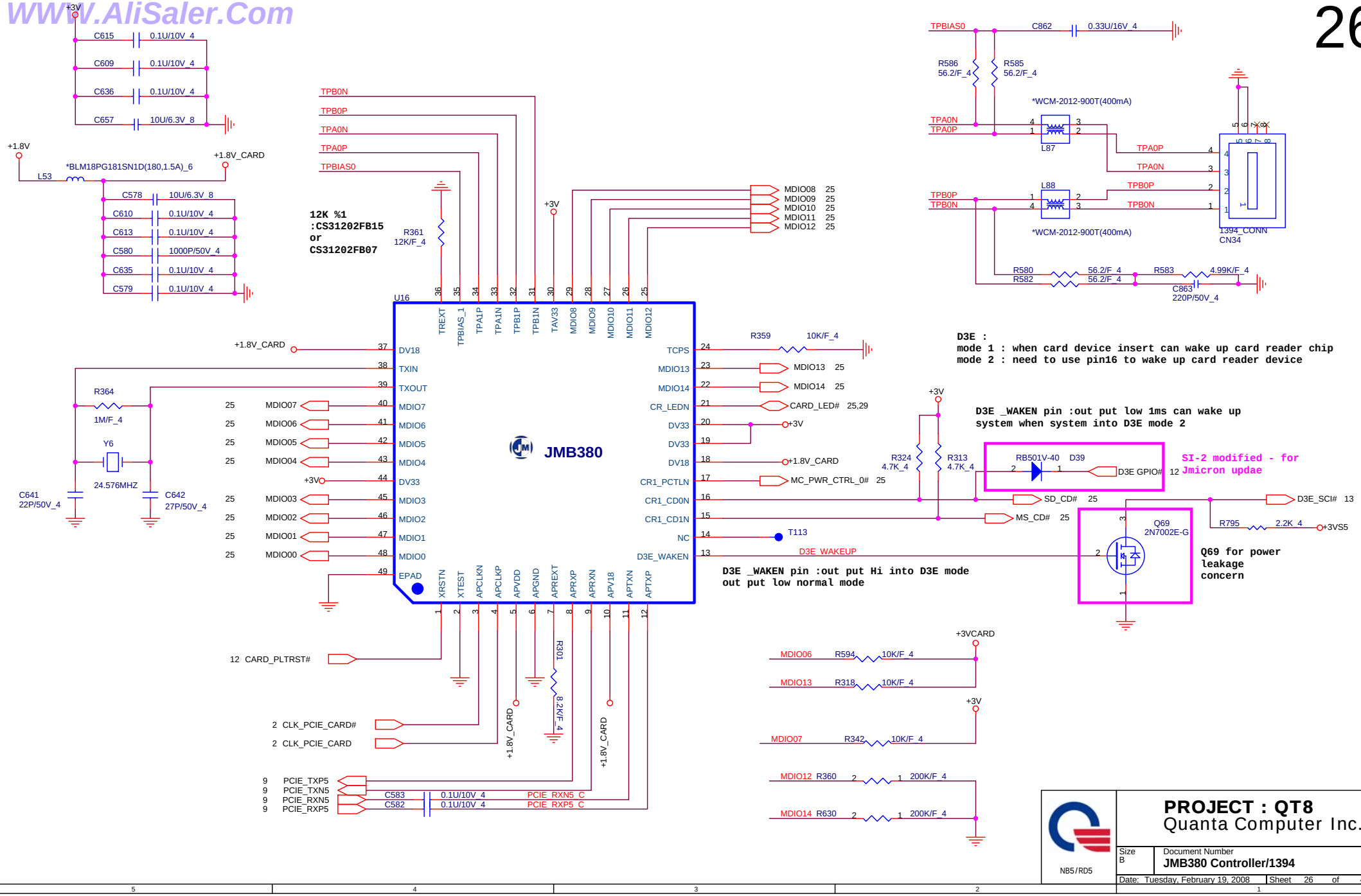

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	JMB380 Controller/1394	1A

Date: Tuesday, February 19, 2008 Sheet 26 of 45

NB5/RD5

SI-2 Modified -- change footrint QFN48-7X7-5-49P-1H for datasheet update

SI-2 Modified

EAPD#--DEFAULT is Hi

Del R672 direct on PV

Del R686, R356, R349 direct on PV

Change C923, 924 footprint

TO Headphone jack

TO Internal Speakers

92HD71B7

SI-2 for EMI

recommand use X7R /10V

TO EXTERNAL MIC

TO DOCK MIC

Audio JACK: Normal Open
SA_A# -->EXT HP
SA_B# -->EXT MIC
SB_E#-->DOCK MIC

Change to SHORT-1A for EMI on PV

R807 change to 330K for HP on PV

Change C962, 963 footprint

Del R814, R815 on PV

TO DOCK Headphone

Add C141 for soft star on PV

TO AUDIO/B CON.

SI-2 modified -- Change footprint for ME request , pin 13,14 are 固定pin

for EMI

TO Headphone jack

DOCK MIC DETECT

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia AD1883	1A

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NB5/RD5

AUDIO AMPLIFIER

SI-2 Modified -- remove C621/C623

LIN-,RIN- and LIN+,RIN+ swap for BOBO noise on PV

PV-1 Modified --R383 , R373 change from 20Kohm to 0 ohm for Volume too low issue

U18 TPA6017A2/FAN7031/LM4874

6017A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

SI-2 modified -- for EMI suggestion

DC impedance 0.35ohm

INT. SPEAKER

Vrms = Vpp / 2 √2

Power = (Vrms)²/ R

QT8 speaker -- 3.2ohm / 2W

SI-2 modified -- remove D22 , add D40

R386, R310 change to SHORT-1A on PV

PC-BEEP

SI-2 modified - from Hp suggestion

TO AMP

TO CODE

MUTE_LED

Low -->un-MUTE

High-->Mute

SI-2 Modified

SI-2 modified -- remove R307,Q24 , add R781,D41,Q70

SI-2 Modified -- R311 change from 10k to 100k

Acceleration sensor

Del R767

Del R768

reserved second source

*BOSCH BMA150

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/INT SPK	1A

NB5/RD5

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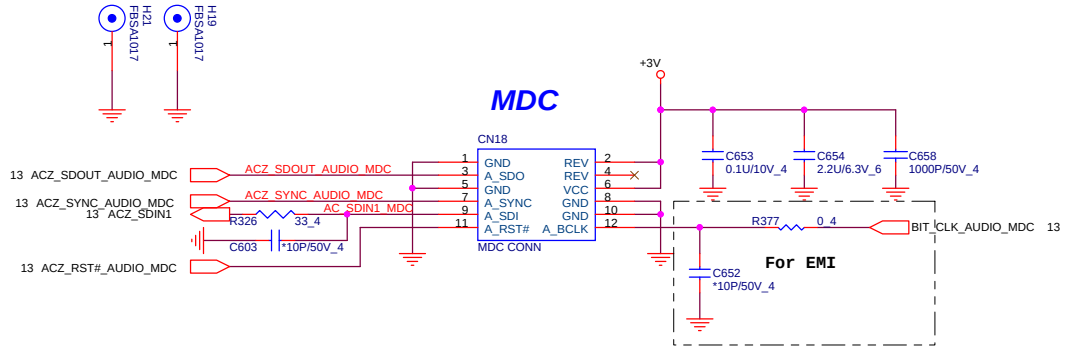
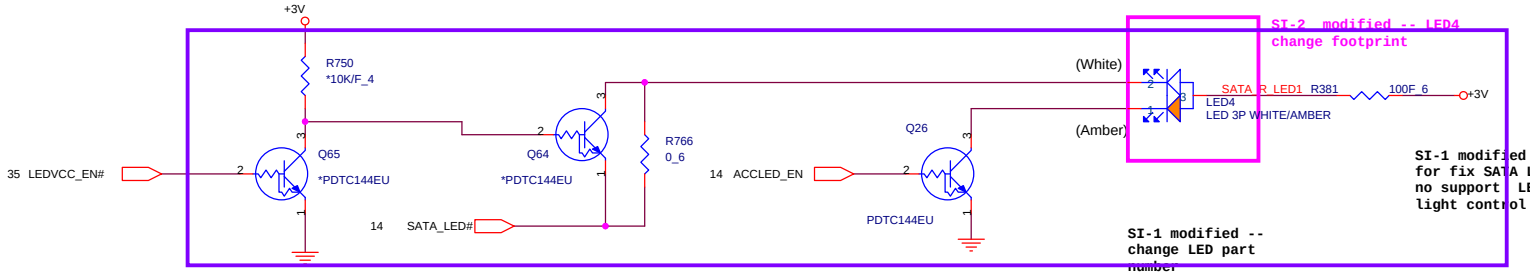
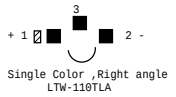
Modem CONN

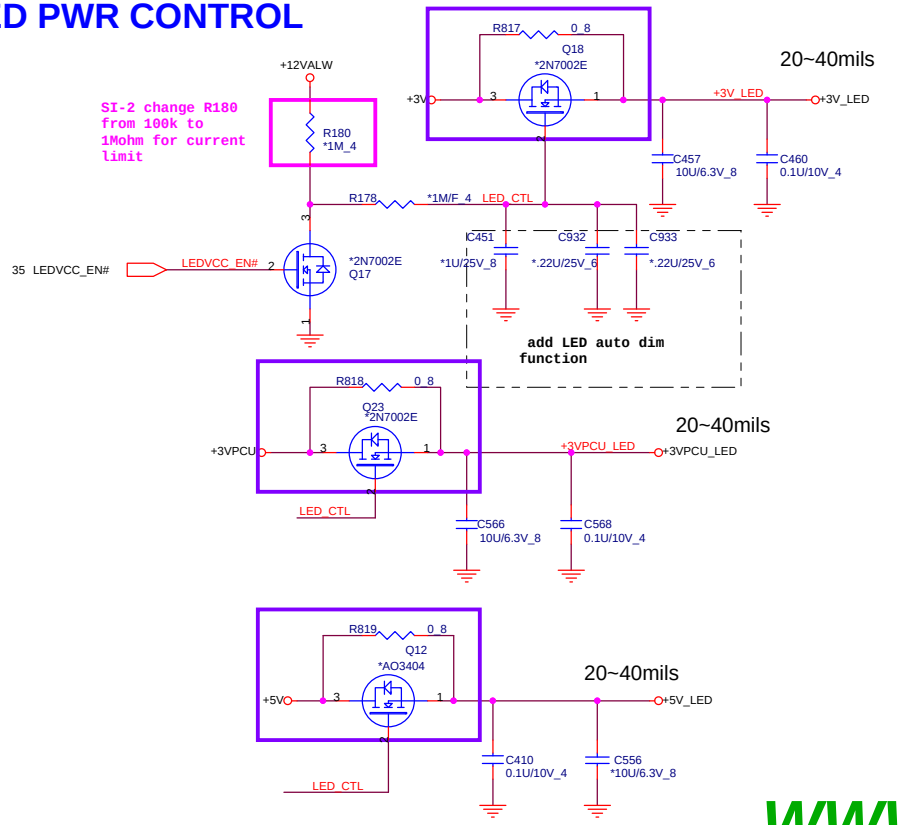




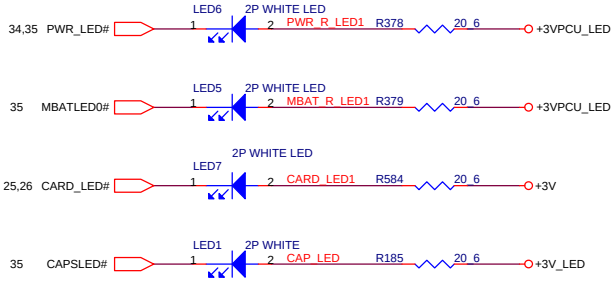
LED

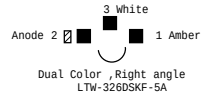


LED PWR CONTROL

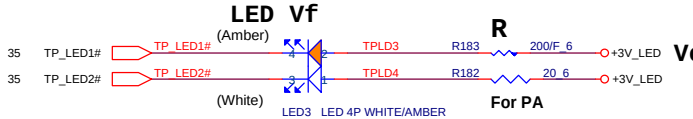


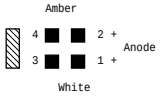
Del R380
Change R381 to 100
Add R766, R817, R818, R819
LED PWR control no-stuff on PV





I = Vcc -Vf / R





NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MDC1.5 Con Accelerometer/ILED	1A

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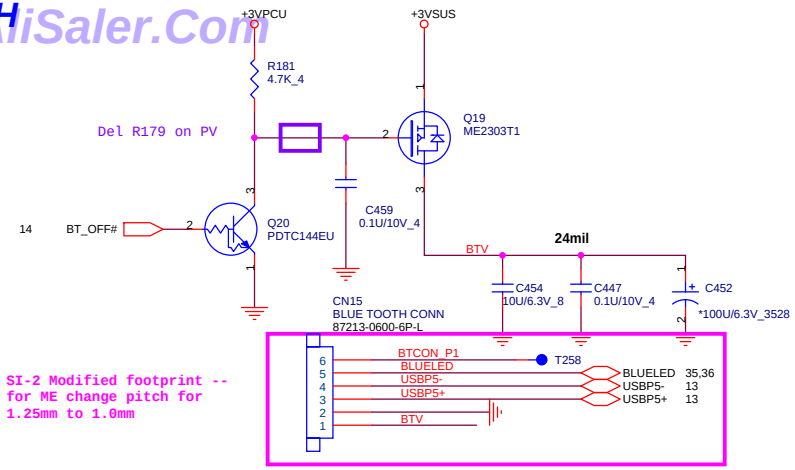
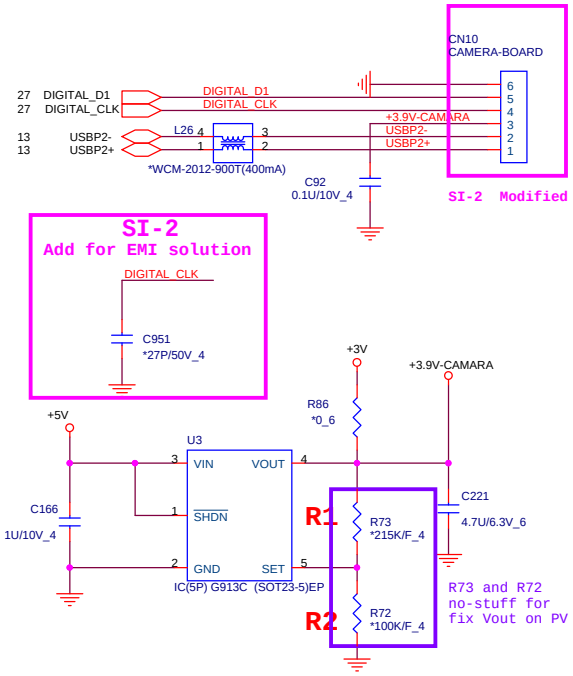
BLUETOOTH



For Discrete Touch-Screen

SI-2 Modified -- remove touch-screen function

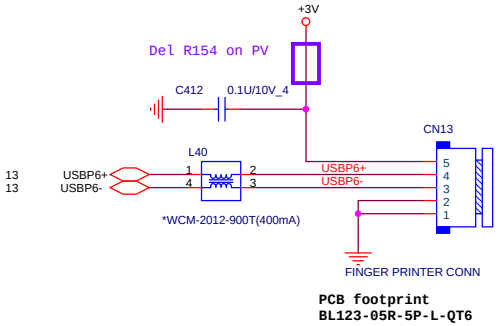
USB CAMERA CONNECT



Vout=1.25(1+R1/R2)

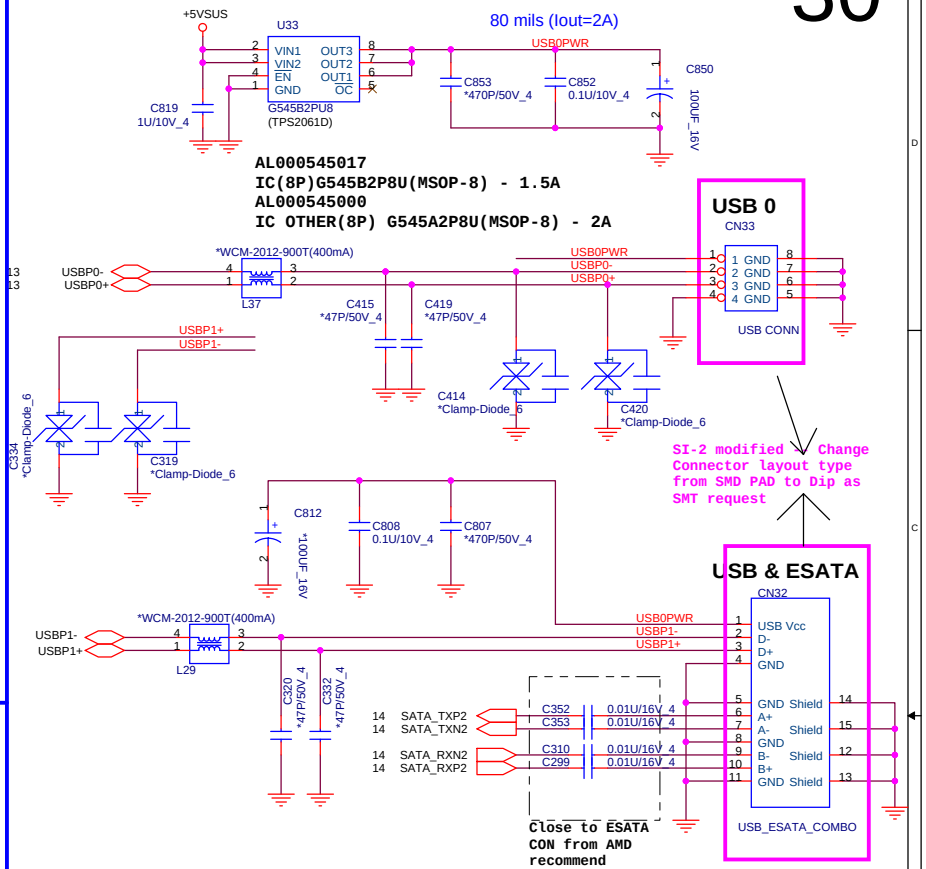
USB Fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

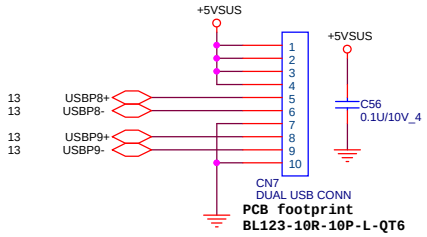


PCB footprint
BL123-05R-5P-L-QT6

LEFT SIDE USBX1 and E-SATA/USB COMBO



RIGHT SIDE USBX2



PCB footprint
BL123-10R-10P-L-QT6

NB5/RD5	PROJECT : QT8 Quanta Computer Inc.	
	Size: Custom Document Number: BT/WEBCAM/FT/USBX4/ESATA	Rev: 1A
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32 +FB12 R41 0_6 +LAN_A1.8_FB12

Stuffed for 8101E/8102E/RTL8111C

+3VLANVCC R425 0_6 +CTRL15_E

C713 0.1U/10V_4 C700 10U/6.3V_8 C703 10U/6.3V_8

+3VLANVCC R426 0_6 +3V_GVDD

Stuffed for RTL8111C(10/100/1000)

32 +CTRL15 R418 *0_6 +CTRL15_E

Stuffed for 8102E/RTL8101E

Del R50 on PV

Y1 25MHZ C45 30P/50V_4 C44 30P/50V_4

Del R36, C712, C710 on PV

R37 2.49K/F_4 LANRSET

U2 RTL8111C-VB-GR

LAN_TX# +LAN_D1.5 R38 0_6 +LAN_D1.5_RVD +3V_A_LAN +3V_A_LAN XTAL1 XTAL2 +3V_GVDD +CTRL15_E

LAN_LED_100# R30 0_4 LAN_GLINK100# LAN_GLINK10# LAN_GLINK1000# +3V_LAN +3V_LAN LAN CABLE DETECT 35 +LAN_D1.5

Del R766 for TP on PV

use BIOS to programming EEPROM , EEDI should be pull Hi

R427 3.6K_6

Del U1, R46 on PV

R46 only for 8111B, 8101E&8102E&8111C can remove

Remove R456 and Add D42 on PV

R456 *1K/F_4 ISOLATEB R457 100_4 LAN_DISABLE# 13,35

R441 15K/F_4 *RB501V-40 D42

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R778 *0_4

R778 SI-2 modified -- RTL8111C remove , RTL8111B,8101E,8102E need to stuff

T5 T6

13,33,36 PCIE_WAKE# PCIE_WAKE#

PCIE_RXN6_LAN_L PCIE_RXP6_LAN_L C82 C81 0.1U/10V_4 PCIE_RXN6_LAN 9 PCIE_RXP6_LAN 9

PCIE_LAN_CLKN 2 PCIE_LAN_CLKP 2

9 PCIE_TXP6_LAN 9 PCIE_TXN6_LAN PCIE_TXP6_LAN PCIE_TXN6_LAN

35 LAN_REST# R460 *0_4 LAN_REST_R#

Del R429, R431, R433, R435, C718, C726 for 8111B on PV

EMI C88 *0.1U/50V_6 C40 *0.1U/50V_6 LAN_YLED LAN_GLED

RJ45 CN27 RJ45_CONN

+3V_LAN R58 330_4 LAN_GLED LAN_GLED# LED_GRE_P LED_GRE_N

LAN_MX3- LAN_MX3+ LAN_MX1- LAN_MX2- LAN_MX2+ LAN_MX1+ LAN_MX0- LAN_MX0+ RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ GND1 GND

+3V_LAN R34 330_4 LAN_YLED LAN_YLED# LED_YEL_P LED_YEL_N

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

AL08101E005 IC(64P)RTL8101E-GR(QFN)

Del R428 on PV

U26 NS892402

C709 C68 C62 C65 0.01U/16V_4 V_DAC

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-

TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4- MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4-

LAN_MCT0 LAN_MX0+ LAN_MX0- LAN_MCT1 LAN_MX1+ LAN_MX1- LAN_MCT2 LAN_MX2+ LAN_MX2- LAN_MCT3 LAN_MX3+ LAN_MX3-

C927 C928 C929 C930 0.01U/100V_6 R39 R44 R47 R51 75/F_4

LAN_MX0+ 37 LAN_MX0- 37 LAN_MX1+ 37 LAN_MX1- 37 LAN_MX2+ 37 LAN_MX2- 37 LAN_MX3+ 37 LAN_MX3- 37

C708 1000P/3KV_1808

LAN_GLINK10# LAN_GLINK100# D37 BAT54A

LAN_GLINK1000# D38 RB501V-40 LAN_GLED#

LAN_TX# R55 0_4 LAN_YLED#

Link

C39 C85 *0.01U/16V_4 *0.01U/16V_4

+3V_LAN C733 0.1U/10V_4 U28 TC7SH08FU

12 LAN_PLTRST# LAN_PLTRST# LAN_REST_R#

R785 *0_4

SI-2 modified -- LAN_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

NS892402:GIGABIT DB0AT9LAN05

NS892405:10/100 DB0ZB1LAN04

PROJECT : QT8
Quanta Computer Inc.

Size Custom | Document Number RTL8111C/8101E/RJ11-RJ45 CN | Rev 1A

NB5/RD5

Date: Tuesday, February 19, 2008 | Sheet 31 of 45

LANVCC
1.2W
364mA

+3VLANVCC

>30mil

Power trace Layout 寬度> 30mil

+3V_LAN

Del L68, L69 direct on PV

C720 10U/6.3V_8
C723 0.1U/10V_4

placement close to lan chipset

C719 0.1U/10V_4
C722 0.1U/10V_4
C716 0.1U/10V_4
C729 0.1U/10V_4

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

+3V_A_LAN

>30mil

C715 0.1U/10V_4
C714 0.1U/10V_4

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

L8
RTL8111C (Gaga lan) use 4.7uH power choke A>500mA tolerance ±15%
RTL8101E & RTL8102E stuff 0ohm

L9
RTL8111C stuff
RTL8102E need to remove L9

+FB12 31

+CTRL18

L8 4.7UH,+-20%,580MA_8

L9 0_8

>30mil

+LAN_A1.8

Power trace Layout 寬度> 30mil

C50 *10U/6.3V_8

RTL 8101E /8102E stuff , RTL 8111C need to remove

C46 10U/6.3V_8

C46

C51 10U/6.3V_8
C57 0.1U/10V_4

placement close to lan chipset

C46
RTL8111C stuff
RTL8101E / 8102E can remove

C728 0.1U/10V_4
C727 0.1U/10V_4
C721 0.1U/10V_4
C730 0.1U/10V_4

these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

+LAN_E1.8

R442 0_8

R220

R220
8102E need to remove
8101E use 0 ohm
8111C use 4.7uH

C731 0.1U/10V_4
C732 1U/10V_4

C732 change to 1U on PV

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

L66 0_8

L66

L66
RTL8111C used 0ohm
RTL 8101E/8102E need to remove

C705
RTL8111C stuff
RTL8101E / 8102E can remove

+CTRL15

L67 L67 *0_8

C704

L67 & C704
8101E/8102E stuff
8111C need to remove

C704 *10U/6.3V_8

C705 10U/6.3V_8

C705

C711 10U/6.3V_8
C49 0.1U/10V_4
C79 0.1U/10V_4
C84 0.1U/10V_4
C83 0.1U/10V_4
C61 0.1U/10V_4
C63 0.1U/10V_4
C48 0.1U/10V_4
C47 0.1U/10V_4
C80 0.1U/10V_4
C55 0.1U/10V_4
C66 0.1U/10V_4

>30mil

Power trace Layout 寬度> 30mil

+LAN_D1.5

these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.placement close lan chip

Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Power	1A

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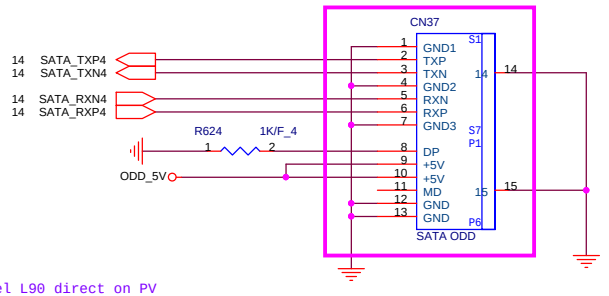
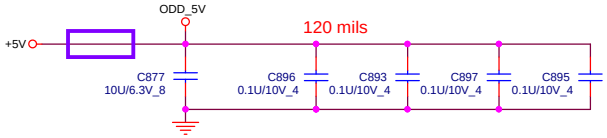
NB5/RD5

SATA CD-ROM

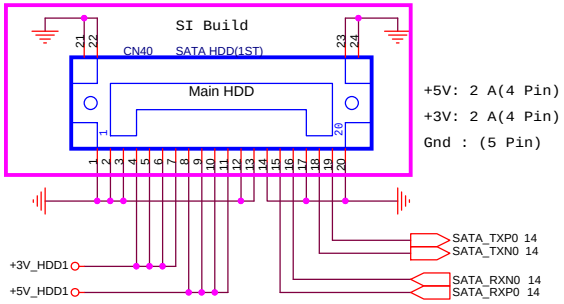
SI-2 Modified footprint -- Modify 12/27

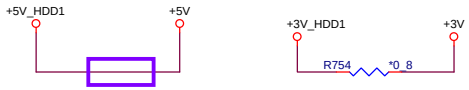


Del L90 direct on PV

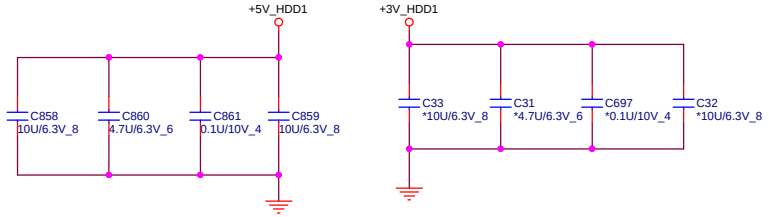


SI-2 Modified footprint -- Modify 固定孔 Size as SMT request





Del R578 direct on PV

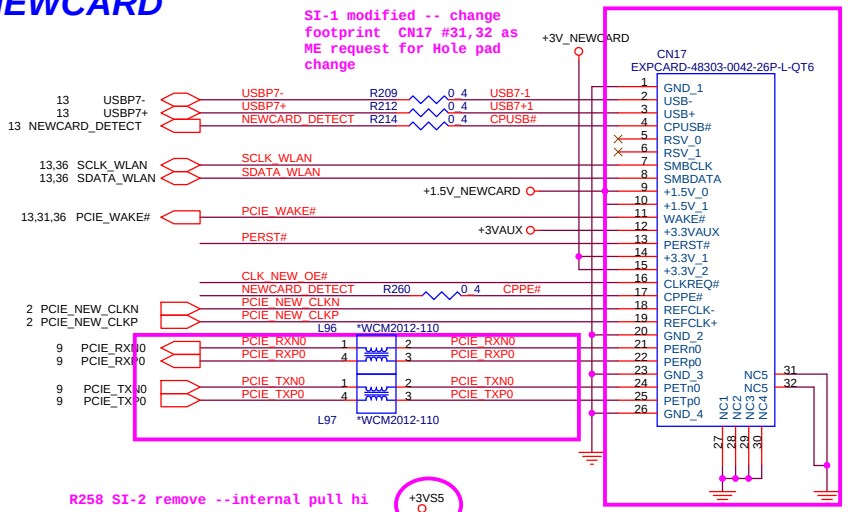


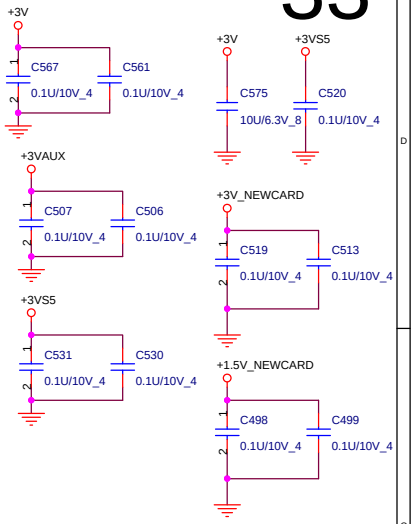
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

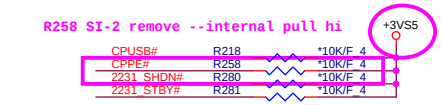
33

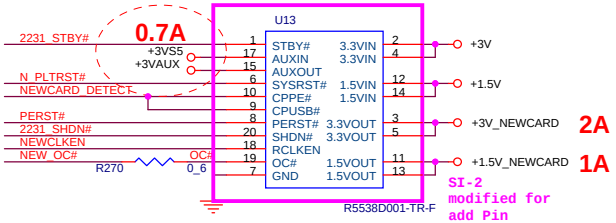
SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change





R258 SI-2 remove --internal pull hi





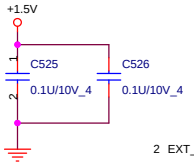
2A

1A

SI-2 modified for add Pin 21~25 as U25 Thermal pad tied to Gnd

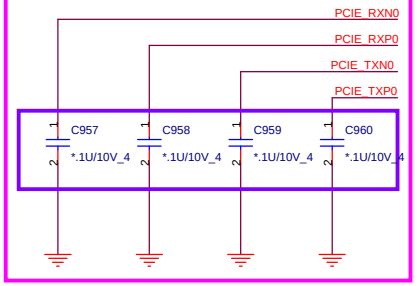
Del R790, R791, R792, R793 for RF on PV

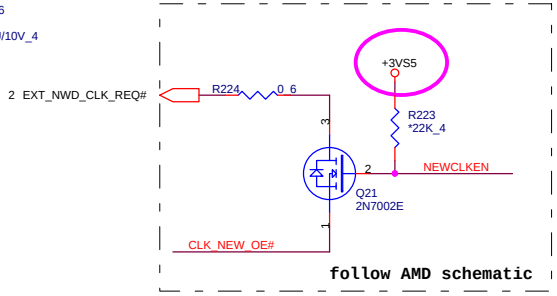
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN

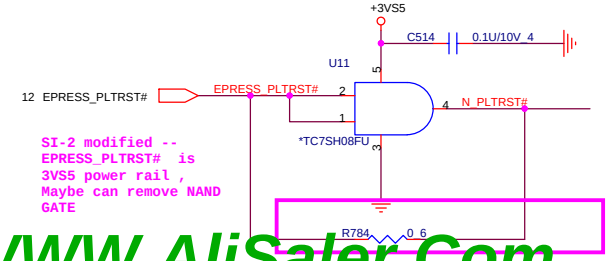


SI-2

For HP request to reserve







SI-2 modified -- EPRESS_PLTRST# is 3VS5 power rail , Maybe can remove NAND GATE

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD/SATA ODD/SATA HDD	1A

NB5/RD5

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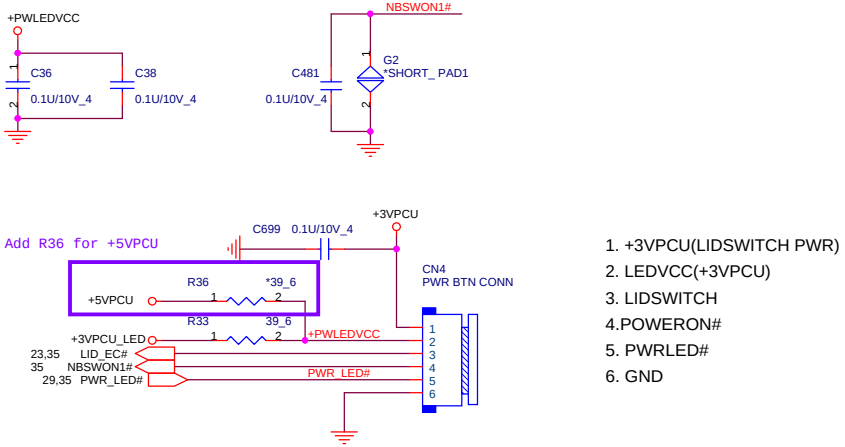
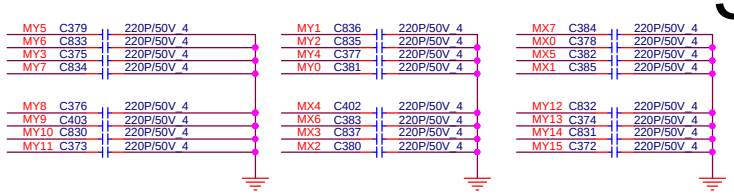
POWER BUTTON CONNECT

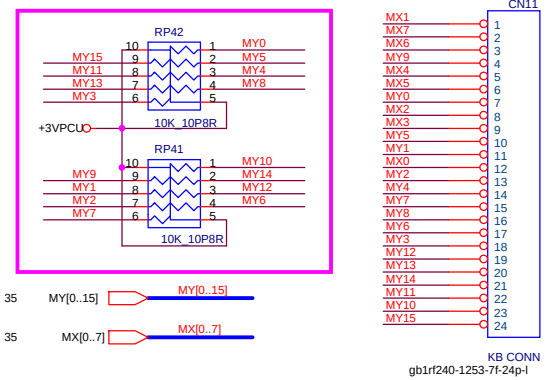


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND



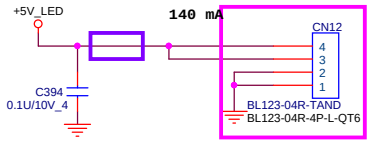
SI-2 Modified
-- net swap for
layout concern

KEYBOARD PULL-UP



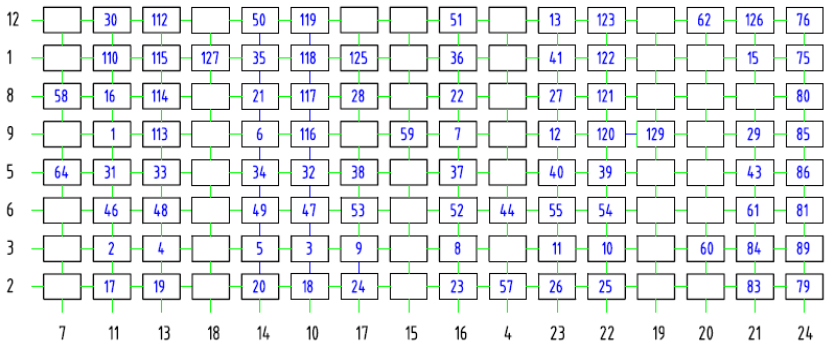
Del R770 on PV

SI-2 Modified 12/27

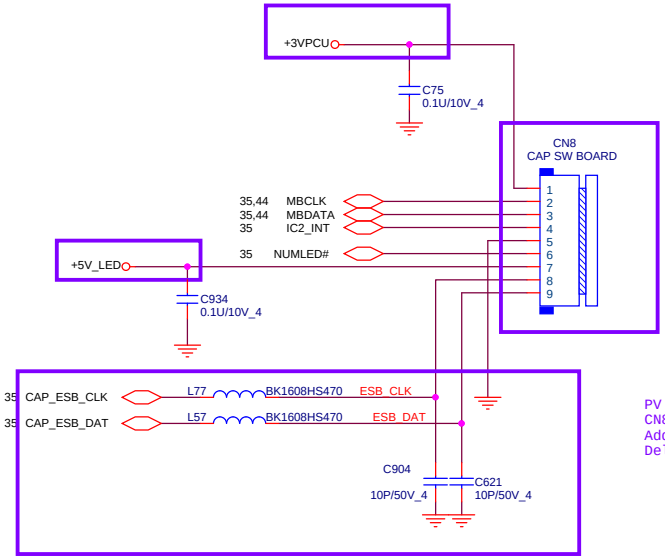


1.LEDVCC
2.LEDVCC
3. NC
4. GND

SI-2 Modified



CAP SW CONNECT



1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB_CLK
9. ESB_DAT

PV modified:
CN8 update type
Add L57, L77, C904, C621 for ESB
Del R104, R103

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KEYBOARD/SW	1A

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NB5/RD5

Change U9 layout footprint to LQFP128-16X16-4-AA1

U9 — KB3926

SI-2 for fix cpu vcore

SI-2 Modified for hp request

Del R249 on PV

Battery charge/discharge Cap button

VGA thermal system thermal

Pin 17 (GPIO0B) ==> assigned for ESB_CLK / Pull high 4.7K
Pin 18 (GPIO0C) ==> assigned for ESB_DAT / Pull high 4.7K

LAN_RESET# move to Pin 25
pin 18 (SWI#1) move to Pin 31

reserved for H/W CIR

Del R256 for TP on PV

SI-2 ADD R256 for H/W CIR

SB780 internal have pull hi

SI-1 modified -- change vaule

change D11 type for PV

UMA BOM missing

SI-2 modified for avoid AD-_ID noise

64.9K -->65W
33.7K -->90W

CS36492FB17 RES CHIP 64.9K 1/16W +-1%(0402)
CS33322FB13 RES CHIP 33.2K 1/16W +-1% (0402)

SI-2 Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier

SB internal pull Hi 10k to 3v_s5

Change D12, D16 to RB500 for current loss

SB internal pull Hi 10k to 3v_s5

For KB3926 C version

close conn

TOUCH PAD CONNECTOR

Del L86 on PV

25 mils

CN14 TOUCH PAD CONN

PCB footprint BL121-12R-12P-L-QT6

PA

TOUCH PAD ON/OFF

Update SW2, SW4, SW6 P/N on PV

TOUCH PAD L/R

Blue LED change to 100K ohm pull low on PV

Del R246, R254 direct on PV

SST AKE5GFK0Z09 1M byte SPI
WINBOND AKE3GFP0N08 BIOS
PME AKE3GZP0500
EON AKE3GZP0Q00

PROJECT : QT8
Quanta Computer Inc.

NB5/RD5

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

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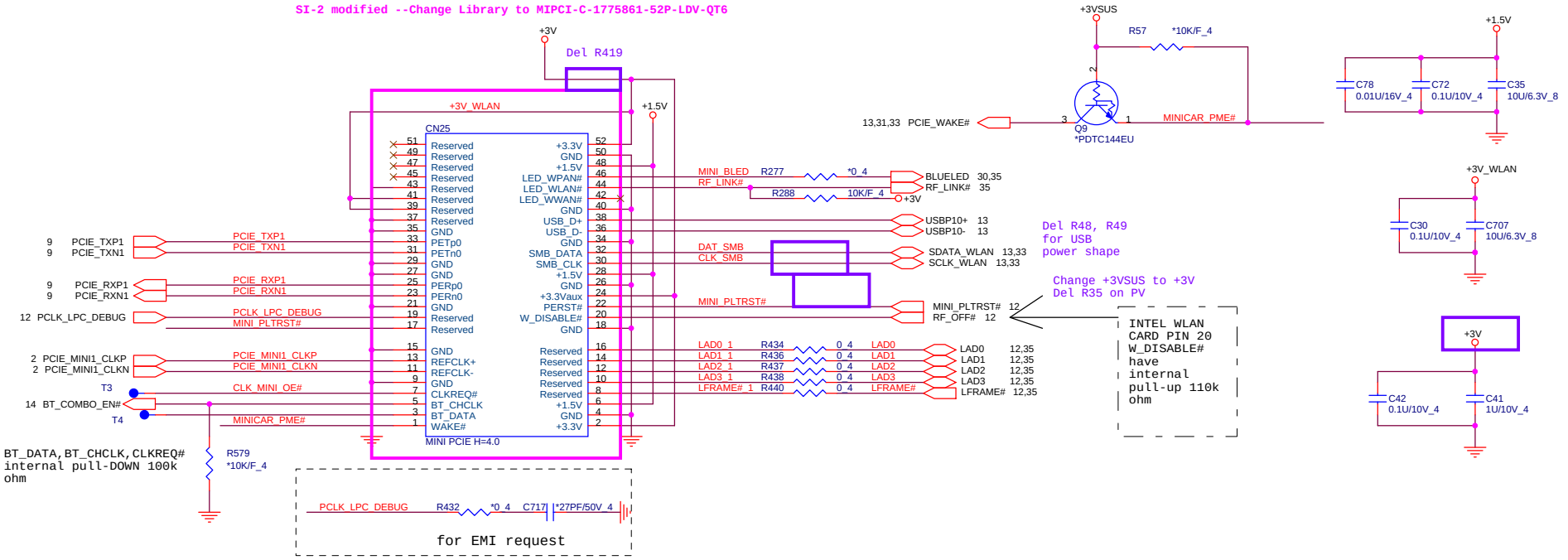
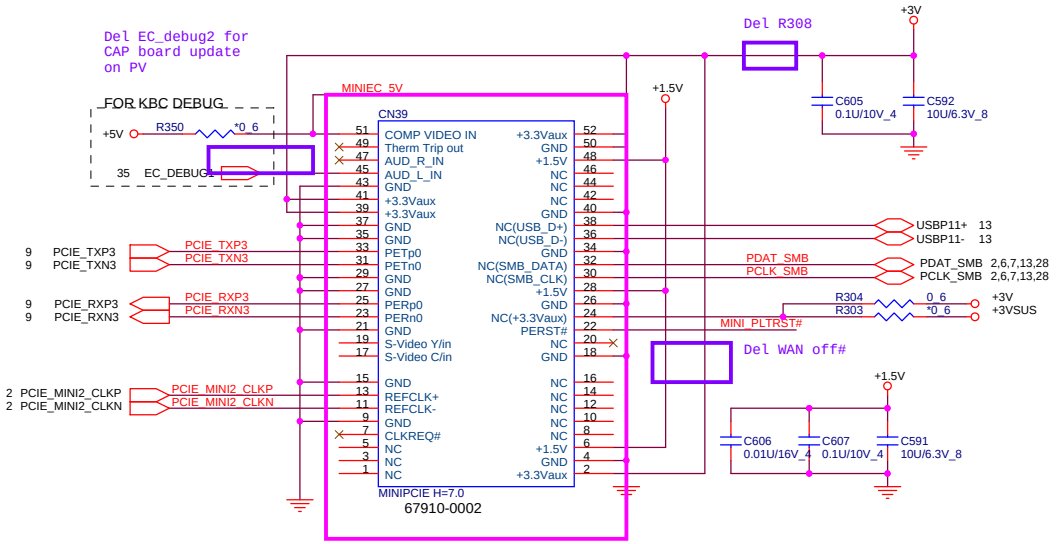
Mini PCI-E Card 1 WLAN

SI-2 modified --Change Library to MIPCI-C-1775861-52P-LDV-QT6



Mini PCI-E Card 2 TV tuner card



SI-2 modified --Change Library to MIPCIE-P04-FJ504-170-52P-QT6

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Mini CARD X 3	1A

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NB5/RD5

CABLE DOCK

support 6A 200mils
CX000480005

SI-2 modified follow QT6 schematic
remove R671,R670,C916,Q30,L65,C669,R388

27 SPDIF — R779 221/F_4 — C949 .1U/50V_6 — SPDIF_DOCK
R780 100/F_4
C950 220P/50V_4

+DOCK_VA
44 +DOCK_VA — L5 48/6A_12 — VA_P
C29 0.1U/50V_6
C17 0.1U/50V_6

13 USBP4-
13 USBP4+
L4 *WCM-2012-900T(400mA)
USBP4-
USBP4+

CN21 DOCKING CONN

VA_P	44 VDD	VDD 43	VA_P
CRT_GDK	38	39	
CRT_RDK	40	37	
	34	35	
CRT_BDK	36	33	
24 DDCDAT2	30	31	
24 PR_HSYNC — R18 33_6 — PR_HSYNC_D	32	29	CIR_IN 27,35
24 DDCCLK2	26	27	PWR_ON
USBP4-	28	25	MUTE_LED
24 PR_VSYNC — R20 33_6 — PR_VSYNC_D	22	23	SLP_BTN#
USBP4+	24	21	JACK_SEN#
31 LAN_MX3+	18	19	VOLME_UP#
31 LAN_MX3-	20	17	VOLME_DN#
		15	SPDIF_DOCK
31 LAN_MX2+	14	13	AGND
31 LAN_MX2-	16	11	RSPK_DK_L
31 LAN_MX1+	10	9	LSPK_DK_L
31 LAN_MX1-	12	7	
31 LAN_MX0+	6	5	DOCK_MIC_R
31 LAN_MX0-	8	3	DOCK_MIC_L
+VIN	2	1	DOCK_PRESENT
	4		
	VSS 42	VSS 41	
	46	45	

MUTE_LED 28,35
SLP_BTN# 35
JACK_SEN# 27
VOLME_UP# 35
VOLME_DN# 35
Remove R410, R411
AGND
RSPK_DK 27
LSPK_DK 27
DOCK_MIC_R 27
DOCK_MIC_L 27
AGND
C698 0.1U/50V_6

SI-2 modified -- for power leakage concern

+3V — R413 100K/F_4
+3VPCU — R415 *100K_4
PR_INSERT# — PR_INSERT# 24,35

docking insert is HI voltage

Q31 MMBT3904
DOCK_PRESENT — R412 — DKPR# 1K/F_4
R414 2K/F_4

Change D29, D30 to RB500 for current loss on PV

D29 RB500V-40
D30 RB500V-40
+5V
+5VSUS — R409 10K/F_4 — DK_PWRON
PWR_ON
R408 15K/F_4

S0: 4V
S3: 2.5V
S4/S5: 0V
*Check voltage on DB

24 PR_GEN — R12 0_6 — CRT_GDK
24 PR_RED — R11 0_6 — CRT_RDK
24 PR_BLU — R15 0_6 — CRT_BDK
R16 150/F_4
R9 150/F_4
R13 150/F_4
C25 5.6P/50V_6
C19 5.6P/50V_6
C23 5.6P/50V_6
C24 5.6P/50V_6
C20 5.6P/50V_6
C21 5.6P/50V_6

filter for docking CRT

CPU FAN

+3V — R177 4.7K_6
35 FAN1SIG
20 mil
+5VFAN1
CN26 FAN CONN
C725 2.2U/6.3V_6
C724 0.1U/10V_4

G955 /FON signal have internal pull Hi to VIN , R420 maybe can remove

+5V
C687 1U/10V_4
R420 10K/F_4
U24
FAN_SMBALERT#
35 FAN1ON
FANPWR = 1.6*VSET
G995
+5VFAN1

VIN VO
/FON GND
GND
VSET GND

8 7 6 5
Gnd shape
1 2 3 4

G995 layout notice

VOLME_DN#
CIR_IN
PR_HSYNC_D
PR_VSYNC_D
C27 *47P/50V_4
C26 *47P/50V_4
C688 *100P/50V_4
C692 *100P/50V_4

DOCK_MIC_R
DOCK_MIC_L
RSPK_DK_L
LSPK_DK_L
JACK_SEN#
C691 *270P/25V_4
C693 *180P/50V_4
C694 *180P/50V_4
C696 *180P/50V_4
C695 *180P/50V_4
AGND AGND AGND AGND AGND
SI-2 modified

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	1A

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DC/DC +3VPCU/+ 5VPCU/ +12VALW

+3V 2,3,5,6,7,10,11,12,13,14,15,16,18,20,23,24,25,26,27,28,29,30,31,33,35,36,37,39,43

+5VPCU 27,28,34,35,39,40,41,42,43
+3VPCU 5,12,23,29,30,34,35,37,40,41,42,44
+3VSUS 13,25,30,36,39,41,43
+3VS5 5,7,12,13,14,15,16,23,26,33,43
+5VSUS 23,30,35,37,43
+5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
+LANVCC

TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

Place these CAPs close to FETs

Rds(on) 15m ohm

SI-1 Modified - ECAP6_3X6_1-7_2-QT8

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

Del PR159 for TP on PV

3.3 Volt +/- 5%
+3VPCU
C/C:8A
P/C:10A

SI-1 Modified -ECAP6_3X6_1-7_2-QT8

+3V
6.76A
S0-S1

+3VS5
0.5A
S0-S5

+3VSUS
1.84A
S0-S3

+5V
4.31A
S0-S1

+5VSUS
4.5A
S0-S3

+LANVCC
0.27A

5,7,12,13,14,15,16,23,26,33,43 +3VS5
+3VSUS 13,25,30,36,39,41,43
+5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
+5VSUS 23,30,35,37,43
+3VLANVCC 31,32,43
HWPG 20,23,35,39,41,42

For EMI-SI

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V(ISL6237)	1A

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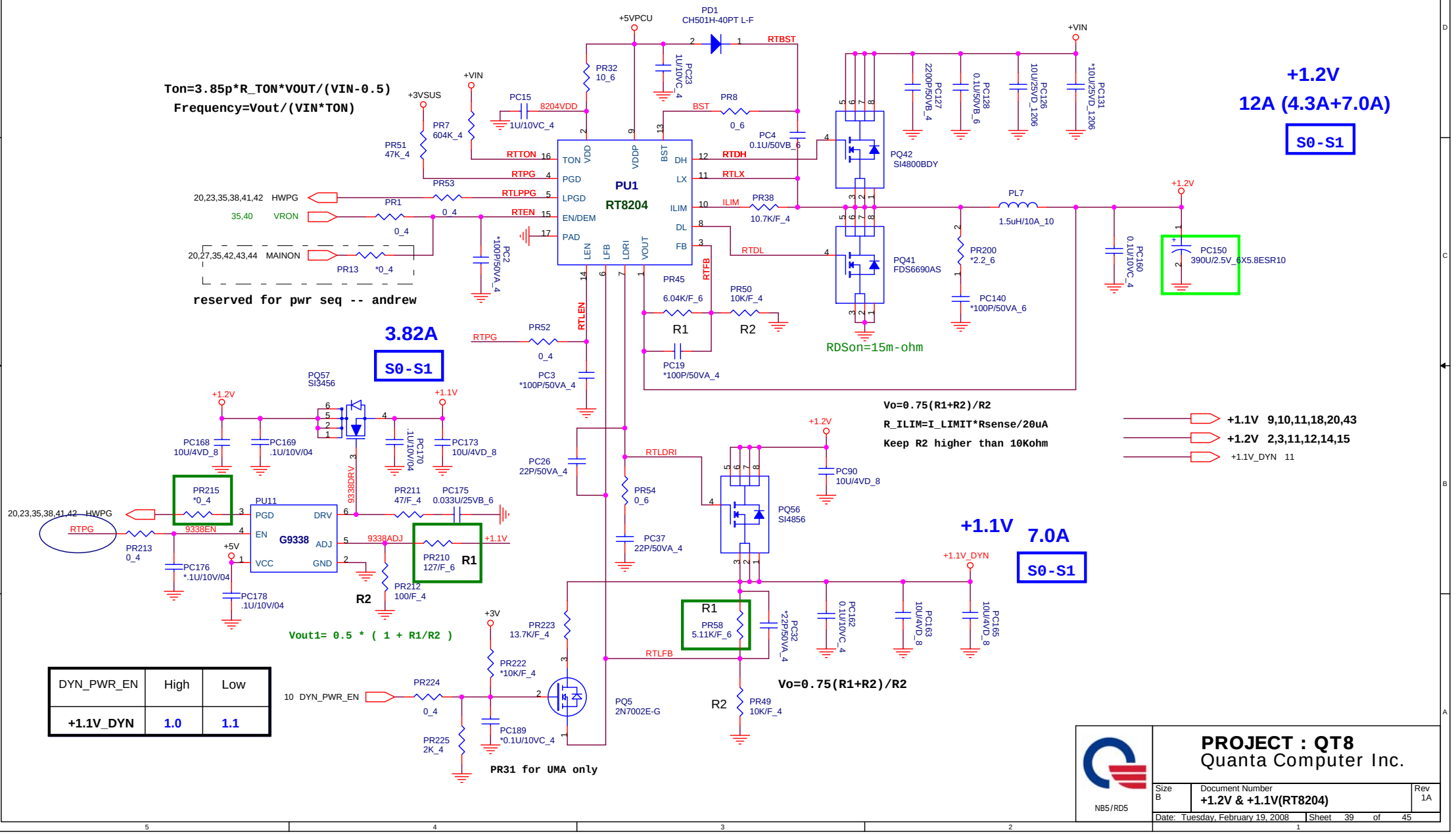
NB5/RD5

+1.1V & +1.2V



DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.2V & +1.1V(RT8204)	1A

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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

36A

36A

SI-1 Modified - ECAP6_3X6_1-7_2-QT8

SI-2 for fix cpu vcore

Pin 49 is GND Pin

ISL6265HRTZ-T

Close to CPU socket

Parallel

Close to CPU socket

Reserve for uni-plane

Reserve for uni-plane

+VCORE0 5
+VCORE1 5
+CPUVDDNB5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
C	CPU_CORE(ISL6265)	1A

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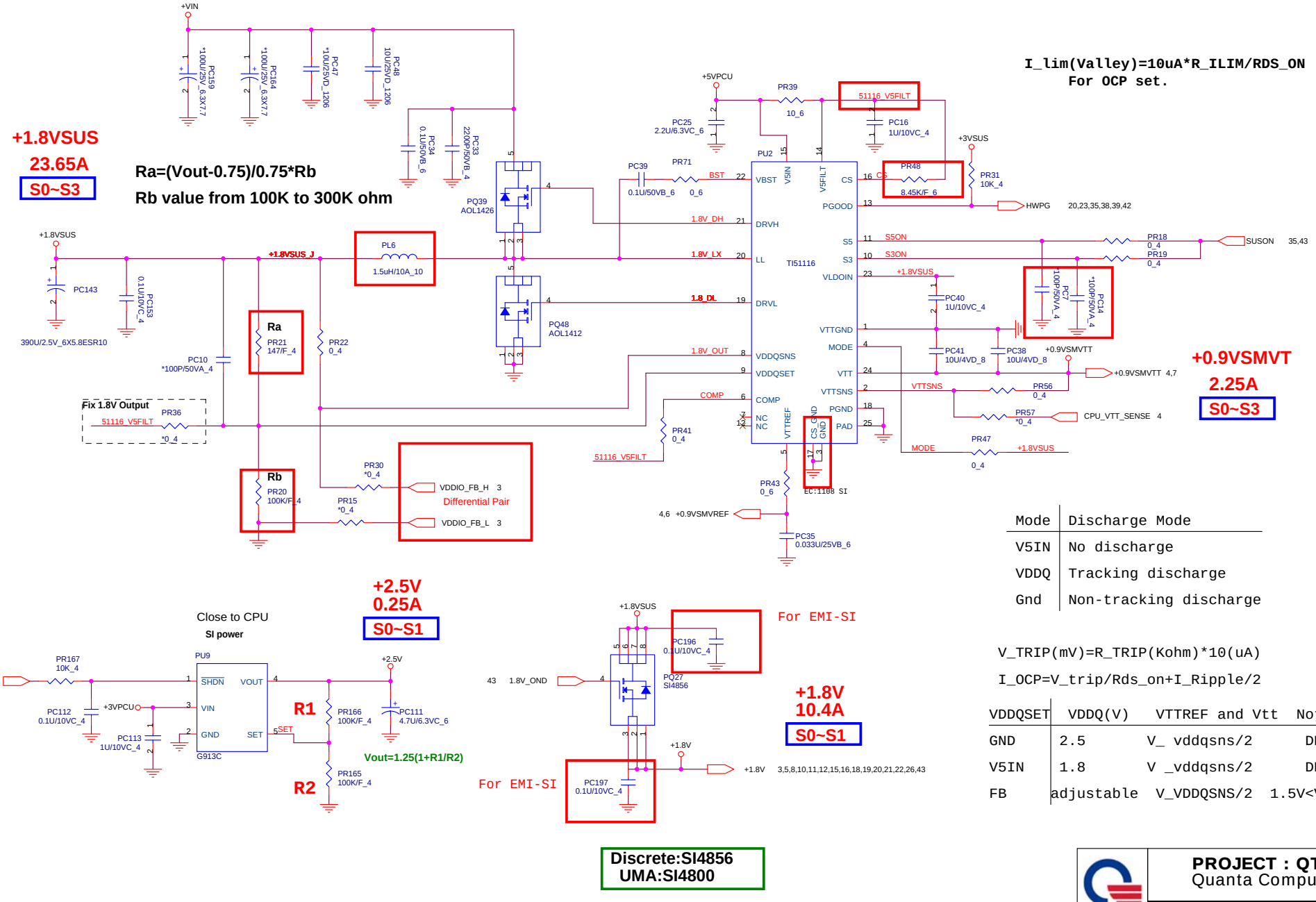
NB5/RD5



Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8VSUS/DDR_VTER/+1.8V/2.5V	1A

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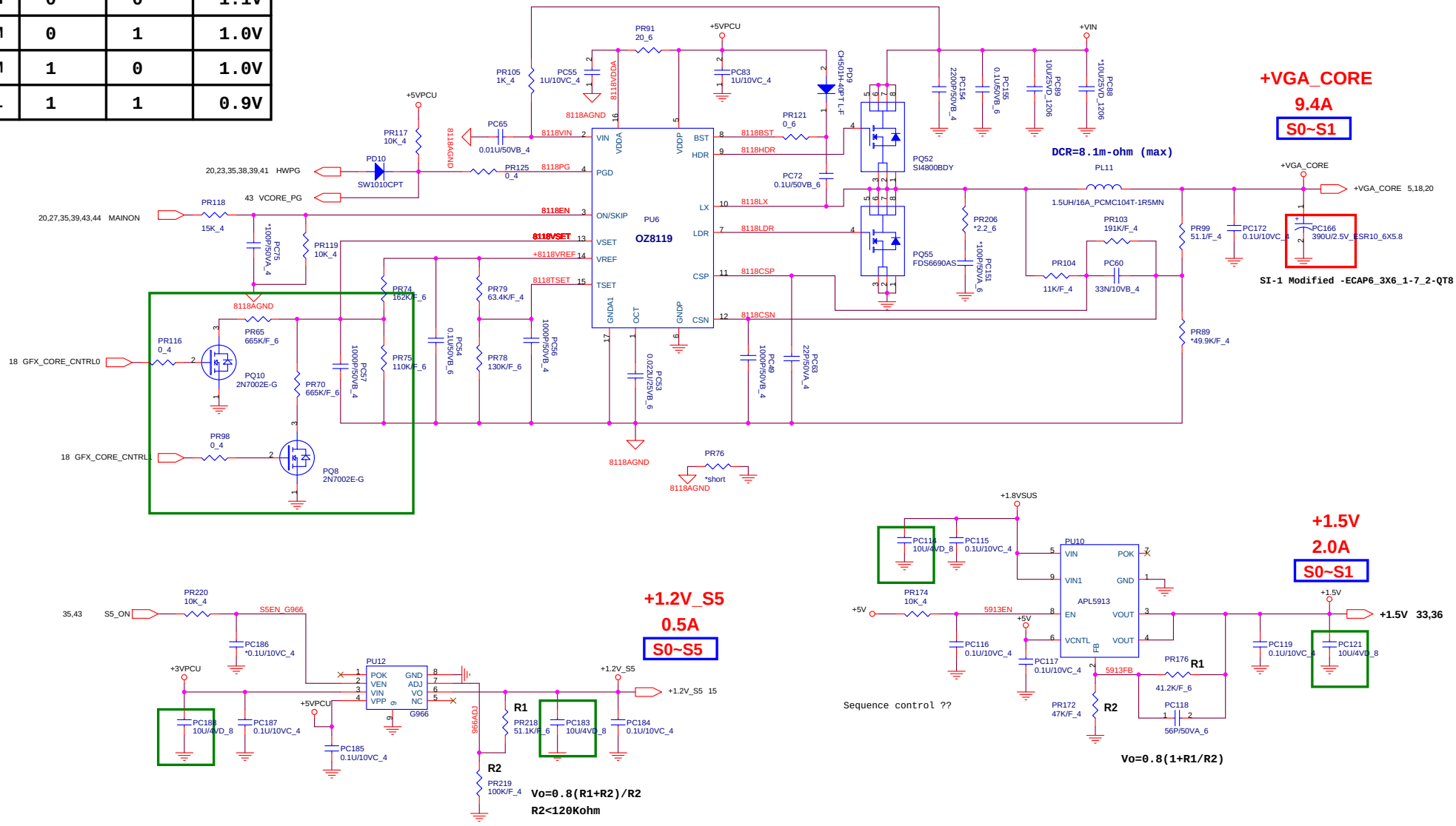
ATI M82-SE

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

+VGA_CORE5,18,20
+1.2V_S5 15
+1.5V 33,36



PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA PWR OZ8118/1.2V_S5/+1.5	1A

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N85/RD5

SI-1 Modified - can remove +1.35V for AMD update

0.5A

S0-S1

20,27,35,39,42,44 MAINON

PR109 *10K_4

PC66 *0.1U/10VC_4

PU5

+1.8VSUS

PC67 *10U/4VD_8

PC58 *0.1U/10VC_4

+5VPCU

PC51 *0.1U/10VC_4

POK VEN VIN VPP GND ADJ VO NC *G966

+1.35V

R1

PR106 *69.8K/F_6

PC68 *10U/4VD_8

PC73 *0.1U/10VC_4

R2

PR113 *100K/F_4

Vo=0.8(R1+R2)/R2

R2<120Kohm

+VIN

PR179 1M_4

PR181 1M_4

PQ30 PDTC144EU

MAINON_G

+5V

PR178 *22_8

PQ31 *2N7002E-G

+3V

PR182 *22_8

PQ33 *2N7002E-G

+1.1V

PR175 *22_8

PQ29 *2N7002E-G

+12VALW

PR180 1M_4

PQ32 2N7002E-G

PC122 *2200P/50VB_4

MAIND 38

+3VSUS

+5VSUS

+12VALW

+VIN

PR90 1M_4

PR87 1M_4

PQ4 PDTC144EU

35,41 SUSON

SUSON_G

PR188 *22_8

PR88 *22_8

PR114 1M_4

PQ3 *2N7002E-G

PQ7 *2N7002E-G

PQ9 2N7002E-G

SUSD

PC74 *2200P/50VB_4

SUSD 38

+3VLANVCC

+12VALW

+VIN

PR124 1M_4

PR123 1M_4

PQ14 PDTC144EU

35 LAN_POWER

LAN_POWER_G

PR129 *22_8

PQ12 *2N7002E-G

PR111 1M_4

PQ13 2N7002E-G

LAN_ON

PC70 *2200P/50VB_4

LAN_ON 38

For Discrete Only

+12VALW

+3VS5

+VIN

PR186 1M_4

PR187 1M_4

PQ38 PDTC144EU

35,42 S5_ON

S5_ONG

PR185 *22_8

PR184 1M_4

PQ37 *2N7002E-G

PQ36 2N7002E-G

S5_OND

PC123 *2200P/50VB_4

S5_OND 38

+1.8V

+VIN

+12VALW

PR170 *0_4

PR169 0_4

20,27,35,39,42,44 MAINON

42 VCORE_PG

PR171 1M_4

PR168 1M_4

PQ25 PDTC144EU

PR173 *22_8

PQ26 *2N7002E-G

PR177 1M_4

PQ28 2N7002E-G

PC120 *2200P/50VB_4

1.8V_OND 41

	PROJECT : QT8 Quanta Computer Inc.	
N85/RD5	Size: Custom Document Number: DISCHARGE Date: Tuesday, February 19, 2008 Sheet 43 of 45	Rev: 1A

TOP DC JACK
65W/90W

ISL6251A

Close to AC soft start MOSFET

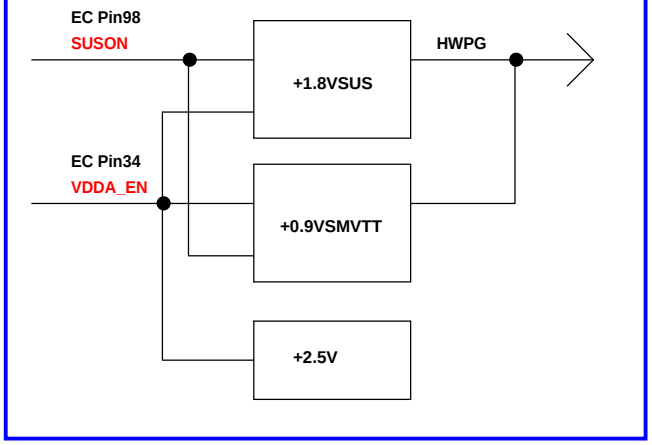
SI-2 modified -- EMI

ONLY for 3S battery pack

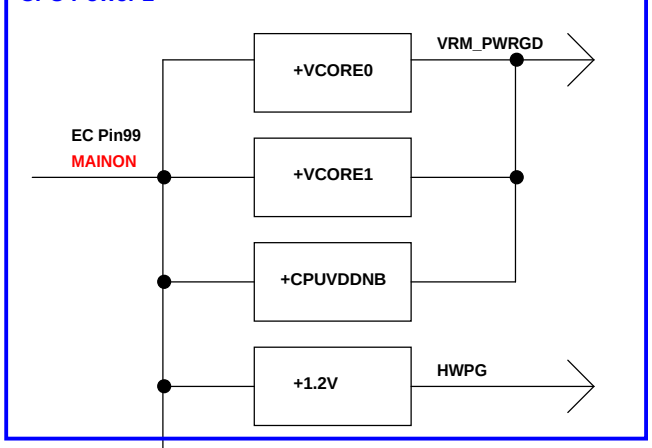
ADP TYPE	PR72 Value	P/N
65W	102K/F	CS41022FB19
90W	7.5K/F	CS27502FB11

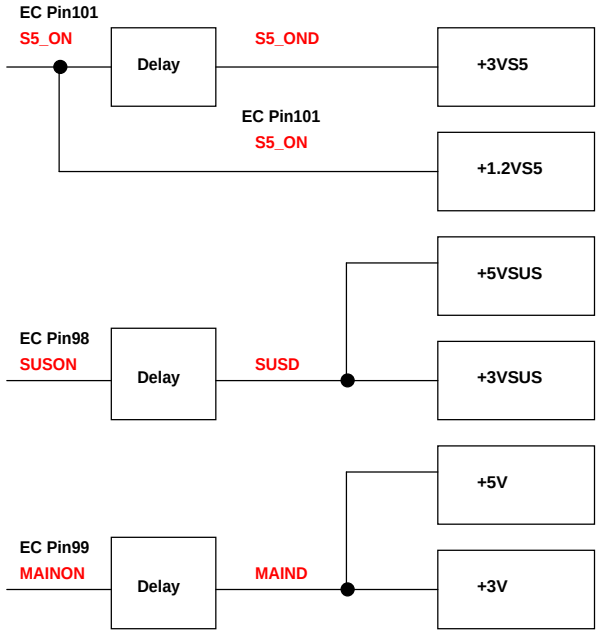
PROJECT : QT8
Quanta Computer Inc.
CHARGER (ISL6251)
Size: Custom | Rev: 1A
Date: Tuesday, February 19, 2008 | Sheet 44 of 45
NB5/RD5

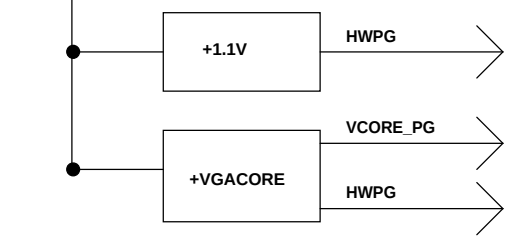
CPU Power 1

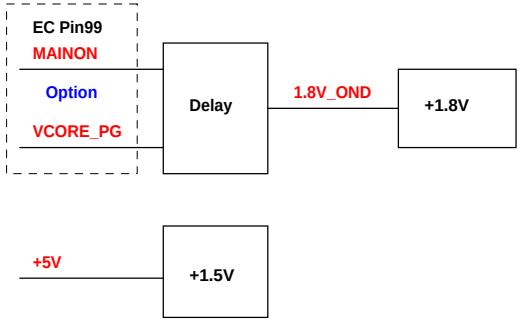


CPU Power 2









1	2	3	4			
S5_ON S5_OND RSMRST#	SUSON SUSD	MAINON MAIND	HWPG VCORE_PG VRM_PWRGD	EC Pin76 ECPWROK Delay 600ms	SB_PWRGD_IN 3.3V	NB_PWRGD_IN 1.8V

NB5/RD5

PROJECT : QT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	1A

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